BURR-BROWN
IC DATA BOOK

1995

DATA CONVERSION
PRODUCTS

ISO9001
CERTIFIED

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BURR-BROWN IC DATA BOOK
DATA CONVERSION PRODUCTS

1995

Model Index

NOTE: (*) This product can be found in the 1995
Burr-Brown IC Data Book—Linear Products.

Model Index

For information on any of these products or to receive the *Burr-Brown Linear Products IC Data Book*, call our automated literature request line at 1-602-741-3884, or contact your local sales representative.

How to Use This Book

If you know the **MODEL NUMBER,**	Use the Model Index on the **INSIDE FRONT COVER.**
If you know the **PRODUCT TYPE,**	Use the **TABBED TABLE OF CONTENTS,** or use the **SELECTION GUIDE TABLES** at the front of each tabbed section.
If you want **NEW MODELS,**	Use the Model Index on the **INSIDE FRONT COVER** or the **SELECTION GUIDE TABLES** at the front of each tabbed section. All new models contained in this edition are shown in **boldface.** Also, contact your local Burr-Brown representative for information on new models released since publication of this data book.
If you want a **PRICE,**	Contact your local Burr-Brown representative. See **INSIDE BACK COVER.**
If you want **TAPE & REEL SPECS,**	See **TAPE & REEL SPECIFICATIONS,** Appendix C, or contact your local Burr-Brown representative.

Burr-Brown
Integrated Circuits
Data Book

Data Conversion
Products

1995

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BURR-BROWN CORPORATION

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NOTE: (1) As of March 19, 1995, the area code for Arizona (except for the metropolitan Phoenix area) will be changed from 602 to 520, please dial your operator for further assistance.

Table of Contents

1 Burr-Brown Corporation

About Burr-Brown

Burr-Brown Corporation is an international leader in the design and manufacturing of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, and control applications throughout the world.

The Company's produces a wide range of precision linear integrated circuits. The Company's integrated circuit components are used in analog and digital signal processing applications found in medical and scientific instrumentation, factory automation, automatic test equipment, process control, and consumer products such as electronic musical instruments and professional audio equipment.

Company Facts

*   Founded in 1956.

*   Corporate headquarters: Tucson, Arizona.

*   1470 employees.

*   1000+ products.

*   Manufacturing and technical facilities in: Tucson, Arizona; Atsugi, Japan; Livingston, Scotland.

*   7 North American direct sales offices, 130 sales representatives and distributors in 180+ locations.

*   International sales and distribution subsidiaries in Austria, France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom; 26 sales representatives throughout the rest of the world.

*   Over 200 sales and service staff worldwide.

Burr-Brown Receives ISO9001 Certification in U.S. and Europe

In September 1993, Burr-Brown Corporation received ISO9001 certification in the United States and Europe, simultaneously. In the United States, registration is recognized through the AT&T Quality Registrar by the Registration Accreditation Board (RAB). Certification is accepted through the Electronics Industries Quality Registrar by the Dutch Registration Board (RCV) in Europe.

ISO9001 is the international standard for assessing the quality systems of companies that design, manufacture, and test products. Adopted by 91 member countries, it's the international quality standard for manufacturing, trade, and communications industries. Certification indicates that a formal quality system exists for all processes and that these processes are audited on a timely basis.

BURR-BROWN CORPORATION

Applications Library

Applications Bulletins, Design Software

APPLICATIONS LIBRARY

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APPLICATIONS BULLETINS

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BURR-BROWN CORPORATION

Sales and Service

ABOUT THIS BOOK

To keep with the easy-to-use format we established last year, the *Burr-Brown Integrated Circuits Data Books* for 1995 will be similar to the 1994 books. Both the Linear Products and Data Conversion Products books are available free from your local salesperson or representative—see **Sales Office Listings** at back of book—or by calling our literature request line at **1-800-548-6132**. Order both, or just the one that fits your needs.

How to Use This Book

Burr-Brown model numbers are listed in the Selection Guides at the beginning of each tabbed section. With these tables you can quickly compare specs among different models and choose the best part for your design. Products appearing in **boldface** type are new products introduced by Burr-Brown since publication of the 1994 data books.

Data sheets are arranged alphanumerically by product type, so if you know the name of the part you can find it quickly. Or, use the Model Index on the **inside front cover**, or page numbers as listed in the Selection Guide tables.

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In addition to individual data sheets, Burr-Brown also provides its customers with applications bulletins, a comprehensive product selection guide on either a PC or Macintosh diskette, promotional samples, comprehensive brochures featuring many product types, and applications assistance by calling **1-800-548-6132.**

Literature requests may also be posted 24 hours/day by calling our automated literature request line at **(602) 741-3884.** When using this service, please be prepared to give your name, company, full address and phone number, as well as the product name or type of literature you are requesting.

FAX*Line*

The Burr-Brown **FAX***Line* is now available for customer requests for product literature. Call **1-800-548-6133** (USA Only) to receive a Component Literature Fax Form, complete with **FAX***Line* literature order numbers. Up to three pieces of literature may be requested per call.

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Sales and Service

1

Returns and Warranty Service

When returning products for any reason, contact Burr-Brown prior to shipping for authorization and shipping instructions. For complete instructions, contact your local salesperson or representative. Customers outside the USA should call the nearest sales office for details and information—see **International Sales Office Listing** at back of book.

To return product, please call for your RMA number. Ship units prepaid and supply the original purchase order number and date, along with an explanation of the malfunction. Upon receipt of the returned devices, Burr-Brown will verify the mal-

function and inform you of the warranty status, cost to repair or replace, credits, and status of replacements where applicable.

Area Code Alert!

Beginning March 19, 1995, the area code for Arizona will be changed from a single area code state to a dual area code state. The area code for the entire state, with the exception of the Phoenix Metropolitan area, will change from **602** to **520**. The phone company will provide a new number change message until June, 1995.

BURR-BROWN CORPORATION

2 A/D Converters, Data Acquisition Components

The Burr-Brown Analog-to-Digital (A/D) converter product line offers a broad selection of resolutions, 12-, 14-, and 16-bit for industrial applications, and 16-, 18-, and 20-bit designed especially for audio applications.

The Burr-Brown industrial A/D line includes industry standard pinouts including two CMOS versions with internal sample holds—the ADS574 and ADS774.

A new family of 12- and 16-bit A/D converters is included in this data book, ADS7804 through ADS7819. This family emphasizes low power, small size, single supply, ease-of-use and upgradability from 12- to 16-bits using the same pc layout and digital interface.

The DDC101 is a 20-bit, 15kHz integrating A/D converter with digital error correction and direct photosensor interface.

High Speed A/D Converters

Burr-Brown's ADS605 and ADC614 offer some of the industry's best performance for high-speed, high resolution sampling A/D converters. Dynamic performance on these converters result in an excellent cost-to-performance ratio. The 16-bit 512ksps ADC701 is the industry's leading low-noise high-speed hybrid A/D converter.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS   Boldface = NEW

Description	Model	Resolution (Bits)	Linearity Error, max (%FSR)	Input Range (V)	Sampling Rate	THD (dB, typ)	Temp Range[1]	Pkg[2]	Q[3] Screen	Page No.
High	ADC701	16	±0.003	10V/20	512kHz	−94w/SHC702	Com	TDIP	Q	2.88
Accuracy,	ADC750	22	±0.003	10	400kHz	—	Com	Board	—	A
High Resolution										
High Speed	ADC614	14	±0.006	±1.25	5.12MHz	−88/Nyquist	Ind	QDIP	Q	2.55
Medium	ADC603	12	±0.018	±1.25	10MHz	−68	Com, Ind, Mil	QDIP	Q	2.37
Resolution	ADC601	12	±0.012	10V/20	1MHz	−70w/SHC804	Com	TDIP	—	2.33
	ADS602	12	±0.03	10V/20	1MHz	−66	Com	TDIP	—	2.139
	ADS605	**12**	**±0.012**	**±1.0**	**10MHz**	**−78/Nyquist**	**Com**	**DDIP**	—	**2.147**
	ADC803	12	±0.012	10V/20	1MHz	NA	Ind, Mil	HMD	Q	2.110

AUDIO ANALOG-TO-DIGITAL CONVERTERS

See Section 8 of this data book for Burr-Brown's selection of Audio Analog-to-Digital Converters.

DSP COMPATIBLE ANALOG-TO-DIGITAL CONVERTERS

Description	Model	Resolution (Bits)	Typical DC Linearity Accuracy	Input Range (V)	Conversion Time (μs)	THD+N dB, max ($V_{IN} = \pm FS$)	Output Format	Pkg[2]	Page No.
Single Channel	DSP101	18	14-Bit	±2.75	5	−90	Serial	DDIP	2.345
Dual Channel	DSP102	18	14-Bit	±2.75	5	−90	Serial	DDIP	2.345

NOTES: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C, Mil = −55°C to +125°C. (2) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount. QDIP = 1.2" wide DIP. (3) Q indicates optional reliability screening is available for this model.

INSTRUMENTATION ANALOG-TO-DIGITAL CONVERTERS

Boldface = NEW

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Conversion Time or Sampling Rate	NMC Reso-lution	Temp Range[2]	Pkg[3]	Page No.
Data-Bus Interface	ADC700	16	±0.003	5, 10, 20 U/B	17µs	14	Mil, Ind, Com	TDIP	2.76
Industry Std Pinouts	ADC71	16	±0.003	5, 10, 20 U/B	50µs	14	Ind, Com	TDIP	2.3
	ADC76	16	±0.003	5, 10, 20 U/B	17µs	14	Ind, Com	TDIP	2.7
Sampling 574 Type	ADS574	12	±0.012	10, 20, U/B	40kHz	12	Com, Mil	DIP, DDIP SO	2.126
Sampling 774 Type	ADS774	12	±0.012	10, 20, U/B	8.5µs	12	Com, Mil	DIP, DDIP SO	2.174
Sampling, Interface	ADS7800	12	±0.012	10, 20 B	333kHz	12	Com, Ind	DIP SO	2.188
High-Accuracy, 4-Channel, Auto-Calibration, Sampling	ADC7802	12	±0.012	0 to +5	8.5µs	12	Ext	DDIP, PLCC	2.113
	ADS7803	12	±0.018	0 to +5	8.5µs	12	Ext	DDIP, PLCC	2.199
CMOS Sampling Family	ADS7804	12	±0.012	20B	10µs	12	Ext	PDIP, SO	2.212
	ADS7805	16	±0.0015	20B	10µs	16	Ext	PDIP, SO	2.222
	ADS7806	12	±0.012	4, 5, 20U/B	25µs	12	Ext	PDIP, SO	2.232
	ADS7807	16	±0.0015	4, 5, 20U/B	25µs	16	Ext	PDIP, SO	2.250
	ADS7808	12	±0.012	4, 5, 10, 20U/B	10µs	12	Ext	PDIP, SO	2.269
	ADS7809	16	±0.0015	4, 5, 10, 20U/B	10µs	16	Ext	PDIP, SO	2.279
	ADS7810	12	±0.012	20B	1.25µs	12	Ext	PDIP, SO	2.289
	ADS7819	12	±0.012	5B	1.25µs	12	Ext	PDIP, SO	2.298
Industry Std Pinout and Interface Medium Speed Monolithic	ADC574A	12	±0.012	10, 20 U/B	25µs	12	Mil,Ind,Com	DDIP	2.23
	ADC674A	12	±0.012	10, 20 U/B	15µs	12	Mil,Ind,Com	DDIP	2.70
	ADC774	12	±0.012	10, 20 U/B	8.5µs	12	Mil,Ind,Com	DDIP	2.103
	ADC80AG	12	±0.012	5, 10, 20 U/B	25µs	12	Ind	TDIP	2.11
	ADC80MAH	12	±0.012	5, 10, 20 U/B	25µs	12	Ind	TDIP	2.15
Medium Speed	ADC84KG	12	±0.012	5, 10, 20 U/B	10µs	12	Ind	TDIP	2.19
	ADC85H	12	±0.012	5, 10, 20 U/B	10µs	12	Com	TDIP	2.19
Mil Temperature Range	ADC87H	12	±0.012	5, 10, 20 U/B	10µs	12	Mil	TDIP	2.19
High Accuracy	**DDC101**	**20**	**±2.5ppm[4]**	**Current and Voltage**	**64µs**	**18**	**Ind**	**DDIP, SOIC**	**2.318**

NOTES: (1) U/B indicates the input voltage range for the model: U = unipolar, B = Bipolar. (2) Com = 0°C to +70°C, Ext = −40°C to +85°C, Ind = −25°C to +85°C, Mil = −55°C to +125°C. (3) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount. (4) Linearity errors ±0.025% reading ±2.5ppm FSR.

DATA ACQUISITION COMP

Model	Channels	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Throughput Rate (kHz)	Temp Range[2]	Pkg[3]	Page No.
SDM862	16 single ended	12	±0.012	±5, ±10, +10	33	Com, Ind, Mil	LCC, PGA	2.367
SDM863	8 differential	12	±0.012	±5, ±10, +10	33	Com, Ind, Mil	LCC, PGA	2.367
SDM872	16 single ended	12	±0.012	±5, ±10, +10	50	Com, Ind, Mil	LCC, PGA	2.367
SDM873	8 differential	12	±0.012	±5, ±10, +10	50	Com, Ind, Mil	LCC, PGA	2.367

NOTES: (1) Internal instrumentation amplifier can be pin programmed for G = 1, 10, 100. (2) Temperature Range: Com = 0°C to +70°C, Ind = −25°C to +85°C, Mil = −55°C to +125°C. (3) LCC = Hermetic 0.95" (typ) square Leadless Chip Carrier, PGA = Hermetic 1.1" (typ) square Pin Grid Array. (4) Linearity error is ±0.025% reading ±2.5ppm FSR.

STILL AVAILABLE BUT NOT IN DATA BOOK

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Conversion Time or Sampling Rate	NMC Reso-lution	Temp Range[2]	Pkg[3]	Page No.
Serial Output	ADC804	12	±0.012	5,10,20 U/B	17µs	12	Mil,Ind,Com	DDIP	A

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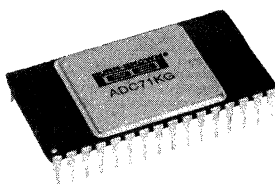
ADC71

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-1060.

ADC71

2

16-Bit
ANALOG-TO-DIGITAL CONVERTER

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FEATURES

● **16-BIT RESOLUTION**
● **±0.003% MAXIMUM NONLINEARITY**
● **COMPACT DESIGN: 32-pin Hermetic Ceramic Package**
● **CONVERSION SPEED: 50μs max**

DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit succes-
sive approximation analog-to-digital converter. It uses
laser-trimmed ICs and is packaged in a convenient 32-
pin hermetic ceramic dual-in-line package. The con-
verter is complete with internal reference, clock, com-
parator, and thin-film scaling resistors, which allow
selection of analog input ranges of ±2.5V, ±5V, ±10V,
0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with
corresponding clock and status output. All digital
inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.

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SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71J, K MIN	TYP	MAX	ADC71A, B MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUTS							
ANALOG							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10,			0 to +5, 0 to +10,		V
		0 to +20			0 to +20		
Input Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL[1]							
	Convert Command Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1				TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%
Offset[2]: Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR[3]
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error: K, B			±0.003			±0.003	% of FSR
J, A			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_S
+5VDC		0.001			0.001		% of FSR/%V_S
CONVERSION TIME[4]							
14 Bits			50			50	µs
WARM-UP TIME	5			*			min
DRIFT							
Gain		±10	±15		*	*	ppm/°C
Offset: Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-Bits)	0		+70	−25		+85	°C
K, B (14-Bits)	0		+70	−25		+85	°C
OUTPUT							
DIGITAL DATA							
(All Codes Complementary)							
Parallel Output Codes[5]: Unipolar		CSB					
Bipolar		COB, CTC[6]					
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB					
Output Drive			2			*	TTL Loads
Status		Logic "1" During Conversion					
Status Output Drive			2			2	TTL Loads
Clock Output Drive			2			2	TTL Loads
Frequency[7]		280			*		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with							
No Degradation of Specs			±200			±200	µA
Temp Coefficient			±10			*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		655			655		mW
Rated Voltage, Analog	±11.4	±15	±16	*	*	*	VDC
Rated Voltage, Digital	+4.75	+5	+4.75	*	*	*	VDC
Supply Drain +15VDC		+10	+15		*	*	mA
Supply Drain −15VDC		−28	−35		*	*	mA
Supply Drain +5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	−25		+85	°C
Operating (Derated Specs)	−25		+85	−55		+125	°C
Storage	−55		+125	−55		+125	°C

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max Logic "1" = 2.4V min. (2) Adjustable to zero. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section. (5) See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (Pin 1).

PIN CONFIGURATION

Top View   DIP

(MSB) Bit 1	1	32	Short Cycle
Bit 2	2	31	Convert Command
Bit 3	3	30	+5VDC Supply
Bit 4	4	29	Gain Adjust
Bit 5	5	28	+15VDC Supply
Bit 6	6	27	Comparator In
Bit 7	7	26	Bipolar Offset
Bit 8	8	25	10V
Bit 9	9	24	20V
Bit 10	10	23	Ref Out 6.3V
Bit 11	11	22	Analog Common[1]
Bit 12	12	21	−15VDC Supply
(LSB for 13 bits) Bit 13	13	20	Clock Out
(LSB for 14 bits) Bit 14	14	19	Digital Common
Bit 15	15	18	Status
Bit 16	16	17	Serial Out

Reference · 16-Bit SAR · 16-Bit D/A Converter · 6.3kΩ · 5kΩ · 5kΩ · Comparator · Clock

NOTE: (1) Metal lid of package is connected to pin 22 (Analog Common).
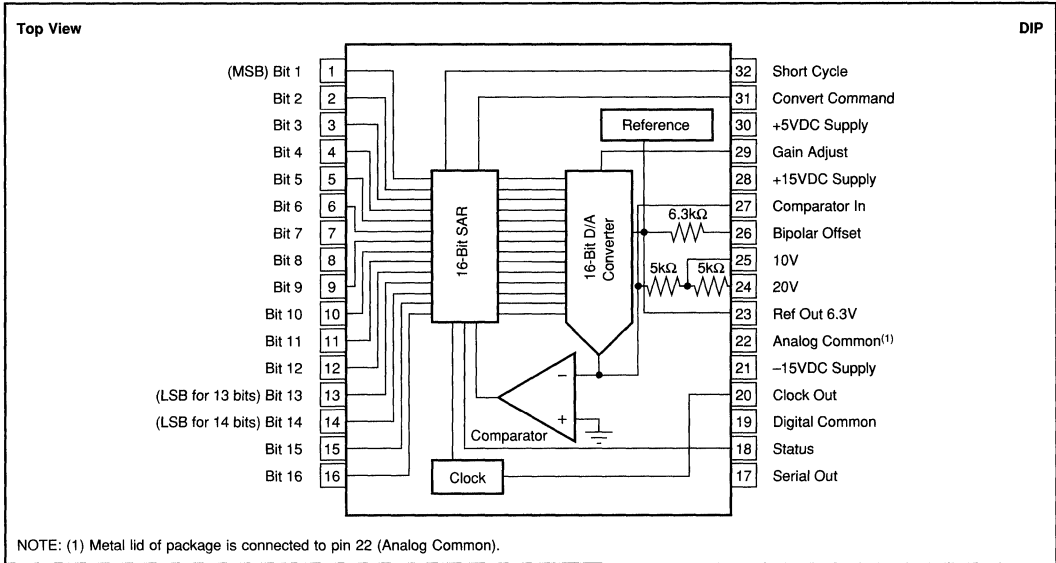
ABSOLUTE MAXIMUM SPECIFICATIONS

+V_{CC} to Common .... 0 to +16.5V
−V_{CC} to Common .... 0V to −16.5V
+V_{DD} to Common .... 0V to +7V
Analog Common to Digital Common .... ±0.5V
Logic Inputs to Common .... 0V to V_{DD}
Maximum Power Dissipation 1000mW
Lead Temperature (10s) .... 300°C

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	NONLINEARITY
ADC71JG	0°C to +70°C	±0.006% FSR
ADC71KG	0°C to +70°C	±0.003% FSR
ADC71AG	−25°C to +85°C	±0.006% FSR
ADC71BG	−25°C to +85°C	±0.003% FSR

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC71JG	32-Pin Hermetic DIP	172-5
ADC71KG	32-Pin Hermetic DIP	172-5
ADC71AG	32-Pin Hermetic DIP	172-5
ADC71BG	32-Pin Hermetic DIP	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ADC71

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS
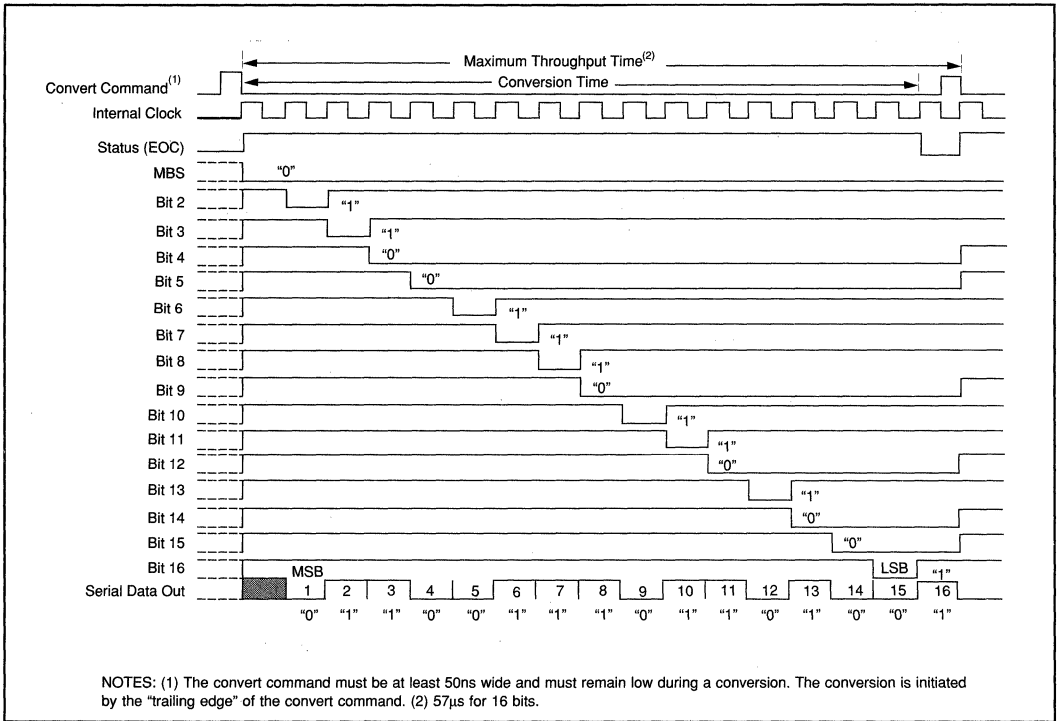
FIGURE 1. ADC71 Timing Diagram.

NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 57μs for 16 bits.

FIGURE 2. Timing Relationship of Serial Data to Clock.

FIGURE 3. Timing Relationship of Valid Data to Status.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	$\dfrac{FSR}{2^n}$	$\dfrac{20V}{2^n}$	$\dfrac{10V}{2^n}$	$\dfrac{5V}{2^n}$	$\dfrac{10V}{2^n}$	$\dfrac{5V}{2^n}$	$\dfrac{20V}{2^n}$
	$n = 12$	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	$n = 13$	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	$n = 14$	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values MSB LSB							
000 ... 000[4]	+Full Scale	+10V−3/2LSB	+5V−3/2LSB	+2.5V−3/2LSB	+10V−3/2LSB	+5V−3/2LSB	+20V−3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	−Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

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ADC76

ABRIDGED DATA SHEET
For Additional Technical
Information, Request PDS-1063

ADC76
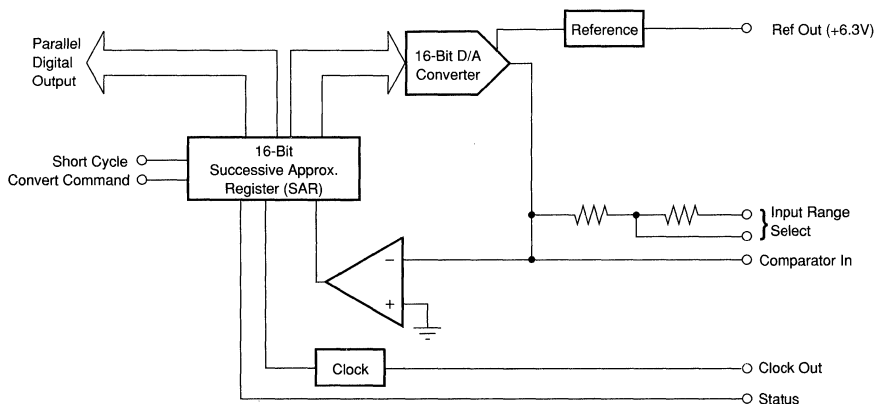
2

16-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **16-BIT RESOLUTION**
● **LINEARITY ERROR ±0.003% max (KG, BG)**
● **NO MISSING CODES GUARANTEED FROM −25°C TO +85°C**
● **17μs CONVERSION TIME (16-Bit)**
● **SERIAL AND PARALLEL OUTPUTS**

DESCRIPTION

The ADC76 is a high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art laser-trimmed IC thin-film resistors and is packaged in a hermetic 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and −25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®
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SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76J, K			ADC76A, B			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10			*		V
		0 to +20			*		
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS[1]							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		*	*	%
Offset Error: Unipolar[2]		±0.05	±0.1		*	*	% of FSR[3]
Bipolar[2]		±0.1	±0.2		*	*	% of FSR
Linearity Error: K, B			±0.003			*	% of FSR
J, A			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.001	±0.003		*	*	% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V$_s$
+5VDC		0.001			*		% of FSR/%V$_s$
CONVERSION TIME[4]							
14 Bits			15		*		µs
15 Bits			16		*		µs
16 Bits			17		*		µs
WARM-UP TIME	5			*			Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4	*		*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3	*		*	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-bit)	0		+70	−25		+85	°C
K, B (14-bit)	0		+70	−25		+85	°C
OUTPUT DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]: Unipolar		CSB			*		
Bipolar		COB, CTC[6]			*		
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status	Logic "1" during conversion				*		
Status Output Drive			2			*	TTL Loads
Internal Clock: Clock Output Drive			2			*	TTL Loads
Frequency[7]	933		1400	*		*	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.655			*		W
Rated Voltage: Analog	±11.4	±15	±16	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+10	+15		*	*	mA
−15VDC		−28	−35		*	*	mA
+5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	−25		+85	°C
Storage	−55		+125	*		*	°C

*Specification same as ADC76J, K.

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1" = 2.4V, min. (2) Adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz.

PIN CONFIGURATION

Top View   **DIP**

MSB Bit 1 — 1	32 — Short Cycle
Bit 2 — 2	31 — Convert Command
Bit 3 — 3	30 — +5V Supply
Bit 4 — 4	29 — Gain Adjust
Bit 5 — 5	28 — +15V Supply
Bit 6 — 6	27 — Comparator In
Bit 7 — 7	26 — Bipolar Offset
Bit 8 — 8	25 — 10V
Bit 9 — 9	24 — 20V
Bit 10 — 10	23 — Clock Rate Control
Bit 11 — 11	22 — Analog Common[1]
Bit 12 — 12	21 — −15V Supply
(LSB for 13 Bits) Bit 13 — 13	20 — Clock Out
(LSB for 14 Bits) Bit 14 — 14	19 — Digital Common
Bit 15 — 15	18 — Status
Bit 16 — 16	17 — Serial Out

Internal blocks: 16-Bit SAR, 16-Bit D/A Converter, Reference, Comparator, Clock, 6.3kΩ, 5kΩ, 5kΩ

NOTE: (1) Metal lid is connected to pin 22 (Analog Common).

ADC76

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

ABSOLUTE MAXIMUM SPECIFICATIONS

+V_{CC} to Common .... 0V to +16.5V
−V_{CC} to Common .... 0V to −16.5V
+V_{DD} to Common .... 0V to +7V
Analog Common to Digital Common .... ±0.5V
Logic Inputs to Common .... 0V to V_{DD}
Maximum Power Dissipation 1000mW
Lead Temperature (soldering, 10s) .... 300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC76JG	32-Pin Hermetic DIP	172-5
ADC76KG	32-Pin Hermetic DIP	172-5
ADC76AG	32-Pin Hermetic DIP	172-5
ADC76BG	32-Pin Hermetic DIP	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
ADC76AG	±0.006	−25°C to +85°C
ADC76BG	±0.003	−25°C to +85°C
ADC76JG	±0.006	0°C to +70°C
ADC76KG	±0.003	0°C to +70°C

FIGURE 1. ADC76 Timing Diagram.

NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 17µs for 16 bits.

FIGURE 2. Timing Relationship of Serial Data to Clock.

FIGURE 3. Timing Relationship of Valid Data to Status.

BINARY (BIN) OUTPUT		INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +IOV	0 to +5V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	$\dfrac{FSR}{2^n}$	$\dfrac{20V}{2^n}$	$\dfrac{10V}{2^n}$	$\dfrac{5V}{2^n}$	$\dfrac{10V}{2^n}$	$\dfrac{5V}{2^n}$	$\dfrac{20V}{2^n}$
	$n = 12$	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	$n = 13$	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	$n = 14$	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB 000 ... 000[4]	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

BURR - BROWN®

ADC80

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-676

ADC80

2

General Purpose
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **INDUSTRY-STANDARD 12-BIT ADC**
- **±0.012% LINEARITY**
- **25µs max CONVERSION TIME**
- **±12V OR ±15V OPERATION**
- **NO MISSING CODES: –25°C to +85°C**
- **HERMETIC 32-PIN PACKAGE**
- **PARALLEL AND SERIAL OUTPUTS**
- **595mW max DISSIPATION**

DESCRIPTION

The ADC80 is a 12-bit successive-approximation ana-log-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25µs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80AG			UNITS
	MIN	TYP	MAX	
RESOLUTION				
ADC80AG-12, ADC80-AGZ-12[1]			12	Bits
ADC80AG-10			10	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
0 to +10V, +5V	4.9	5	5.1	kΩ
±10V	9.8	10	10.2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			−150	μA
I_{IL} (V_{IN} = +0.4V)			500	μA
Convert Command Pulse Width[2]	100		2000	ns
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.1	±0.3	% of FSR[4]
Offset Error[3]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error: ADC80AG-12, ADC80AGZ-12			±0.012	% of FSR
ADC80AG-10			±0.048	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11.4V ≤ ±V_{CC} ≤ 16.5V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[5]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[6]				
ADC80AG-12, ADC80-AGZ-12	15	22	25	μs
ADC80AG-10	13	20	22	μs
OUTPUT				
DIGITAL (Bits 1-12 , Clock Out, Status, Serial Out)				
Output Codes[7]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[8]		CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{SOURCE} ≤ 80μA)	+2.4			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	V
Source Current Available for External Loads[9]	200			μA
Temperature Coefficient		±10	±30	ppm/°C

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80AG			UNITS
	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS (For all models)				
Voltage: $\pm V_{CC}$	±11.4	±15	±16.5	V
V_{DD}	+4.5	+5	+5.5	V
Current: $+I_{CC}$		5	8.5	mA
$-I_{CC}$		21	26	mA
I_{DD}		11	15	mA
Power Dissipation ($\pm V_{CC}$ = 15V)		450	595	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Operating (derated specs)	−55		+125	°C
Storage	−65		+150	°C

NOTES: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12. (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 2µs (max) to assure the specified conversion time. (3) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drifts. (6) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time: see "Short Cycle Feature" section. (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table 1 for additional information. (8) NRZ means Non-Return-to-Zero coding. (9) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10 (LSB-10 Bits)
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB-12 Bits)
7	NC[1]	26	Serial Out
8	Bit 1 ($\overline{\text{MSB}}$)	25	$-V_{CC}$
9	+5V Digital Supply	24	Reference Out (+6.3V)
10	Digital Common[2]	23	Clock Out
11	Comparator In	22	Status
12	Bipolar Offset	21	Short Cycle
13	R_1 10V Range	20	Clock Inhibit
14	R_2 20V Range	19	External Clock
15	Analog Common	18	Convert Command
16	Gain Adjust	17	$+V_{CC}$

NOTE: (1) +5V applied to pin 7 has no effect on circuit. (2) Metal lid of package is connected to pin 10.

CONNECTION DIAGRAM

Top View

ADC80

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

ABSOLUTE MAXIMUM RATINGS

+V_{CC} to Analog Common .... 0 to +16.5V
−V_{CC} to Analog Common .... 0 to −16.5V
V_{DD} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±0.5V
Logic Inputs (Convert Command, Clock In)
   to Digital Common .... −0.3V to +V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset)
   to Analog Common .... ±16.5V
Reference Output .... Indefinite Short to Common,
                                                                   Momentary Short to V_{CC}
Lead Temperature, (soldering, 10s) .... +300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	RESOLUTION (Bits)
ADC80AG-10	10
ADC80G-12	12
ADC80GZ-12[1]	12

NOTE: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC80AG-10	32-Pin Hermetic	172
ADC80G-12	32-Pin Hermetic	172
ADC80AZ-12[1]	32-Pin Hermetic	172

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

SYMBOL	PARAMETER	TYP	UNITS
t_{CD}	Clock delay from convert command	30	ns
t_{CP}	Nominal clock period	1.65	μs
t_{CW}	Nominal clock pulse width	0.65	μs
t_{SD}	Status delay from convert command	130	ns
t_R	All bits reset delay from convert command	65	ns
t_{DV}	Data valid time from clock pulse high	−5	ns
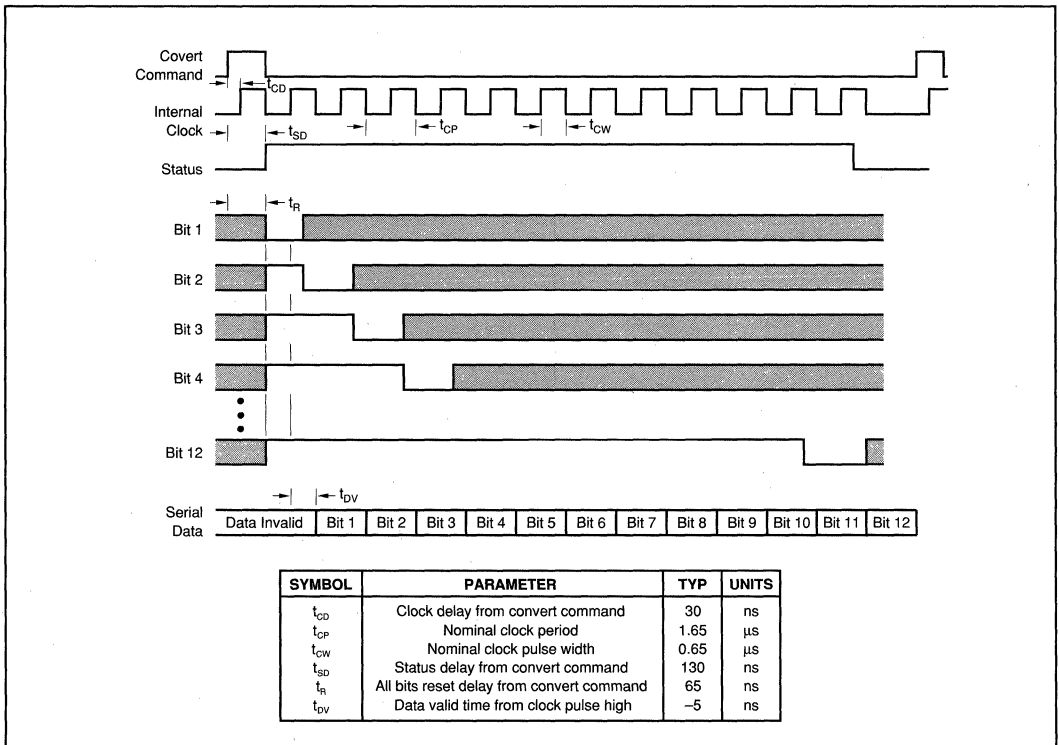
FIGURE 1. ADC80 Timing Diagram (nominal values at +25°C with internal clock).

BURR - BROWN®
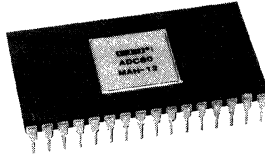
ADC80MAH-12

ABRIDGED DATA SHEET
For Additional Technical
Information, Request PDS-694

ADC80MAH-12

2

Monolithic12-Bit
ANALOG-TO-DIGITAL CONVERTER

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FEATURES

- **INDUSTRY-STANDARD 12-BIT ADC**
- **MONOLITHIC CONSTRUCTION**
- **LOW COST**
- **±0.012% LINEARITY**
- **25μs max CONVERSION TIME**
- **±12V OR ±15V OPERATION**
- **NO MISSING CODES: –25°C to +85°C**
- **HERMETIC 32-PIN PACKAGE**
- **PARALLEL OR SERIAL OUTPUTS**
- **705mW max DISSIPATION**

DESCRIPTION

The ADC80MAH-12 is a 12-bit single-chip succes-sive-approximation analog-to-digital converter for low cost converter applications. It is complete with a comparator, a 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, a successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25μs makes the ADC80MAH-12 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, this A/D converter may be short-cycled for faster conversion speed with re-duced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation. The convert command

circuits have been redesigned to allow simplified free-running operation with internal or external clock.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resis-tors on digital inputs not requiring connection. The ADC80MAH-12 operates equally well with either ±15V or ±12V analog power supplies, and also re-quires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line pack-age.

BURR-BROWN®

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, ±V_{CC} = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80MAH-12 MIN	TYP	MAX	UNITS
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
0 to +10V, ±5V	4.9	5	5.1	kΩ
±10V	9.8	10	10.2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			20	μA
I_{IL} (V_{IN} = +0.4V)	−20			μA
Convert Command Pulse Width[1]	100ns		20	μs
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.01	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11.4V ≤ ±V_{CC} ≤ 16.5V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ ±V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		±85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]		22	25	μs
OUTPUT				
DIGITAL (Bits 1-12 , Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{SOURCE} ≤ 80μA)	+2.4			V
Internal Clock Frequency		520		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.20	+6.3	+6.40	V
Source Current Available for External Loads[8]	200			μA
Temperature Coefficient		±10	±30	ppm/°C

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

| PARAMETER | ADC80MAH-12 | | | UNITS |
	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS				
Rated Supply Voltages		+5, ±12 or ±15		V
Supply Ranges: $\pm V_{CC}$	±11.4		+16.5	V
V_{DD}	+4.5		+5.5	V
Supply Drain: $+I_{CC}$ ($+V_{CC}$ = 15V)		8.5	11	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)		21	24	mA
I_{DD} (V_{CC} = 5V)		30	36	mA
Power Dissipation ($\pm V_{CC}$ = 15V, V_{DD} = 5V)		593	705	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Operating (derated specs)	−55		+125	°C
Storage	−65		+150	°C

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 20µs (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means Non-Return-to-Zero coding. (8) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

ABSOLUTE MAXIMUM RATINGS PCM1760

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to −16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In)	
to Digital Common	−0.3V to $+V_{CC}$
Analog Inputs (Analog In, Bipolar Offset)	
to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, (soldering, 10s)	+300°C
Maximum Junction Temperature	+160°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	RESOLUTION (Bits)
ADC80MAH-12	12
BURN-IN SCREENING OPTION	
MODEL	BURN-IN TEMPERATURE (160h)[1]
ADC80MAH-12-BI	12

NOTE: (1) Or equivalent.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC80MAH-12	32-Pin Hermetic	212

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ADC80MAH-12

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

CONNECTION DIAGRAM

Top View

PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10 (LSB-10 Bits)
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB-12 Bits)
7	NC[1]	26	Serial Out
8	Bit 1 ($\overline{\text{MSB}}$)	25	$-V_{CC}$
9	+5V Digital Supply	24	Reference Out (+6.3V)
10	Digital Common	23	Clock Out
11	Comparator In	22	Status
12	Bipolar Offset	21	Short Cycle
13	R_1 10V Range	20	Clock Inhibit
14	R_2 20V Range	19	External Clock
15	Analog Common	18	Convert Command
16	Gain Adjust	17	$+V_{CC}$

NOTE: (1) +5V applied to pin 7 has no effect on circuit.

SYMBOL	PARAMETER	TYP	UNITS
t_{CD}	Clock delay from convert command	153	ns
t_{CP}	Nominal clock period	1.81	μs
t_{CW}	Nominal clock pulse width	0.87	μs
t_{SD}	Status delay from convert command	186	ns
t_R	All bits reset delay from convert command	141	ns
t_{DV}	Data valid time from clock pulse high	−15	ns

FIGURE 1. Timing Diagram (nominal values at +25°C with internal clock).

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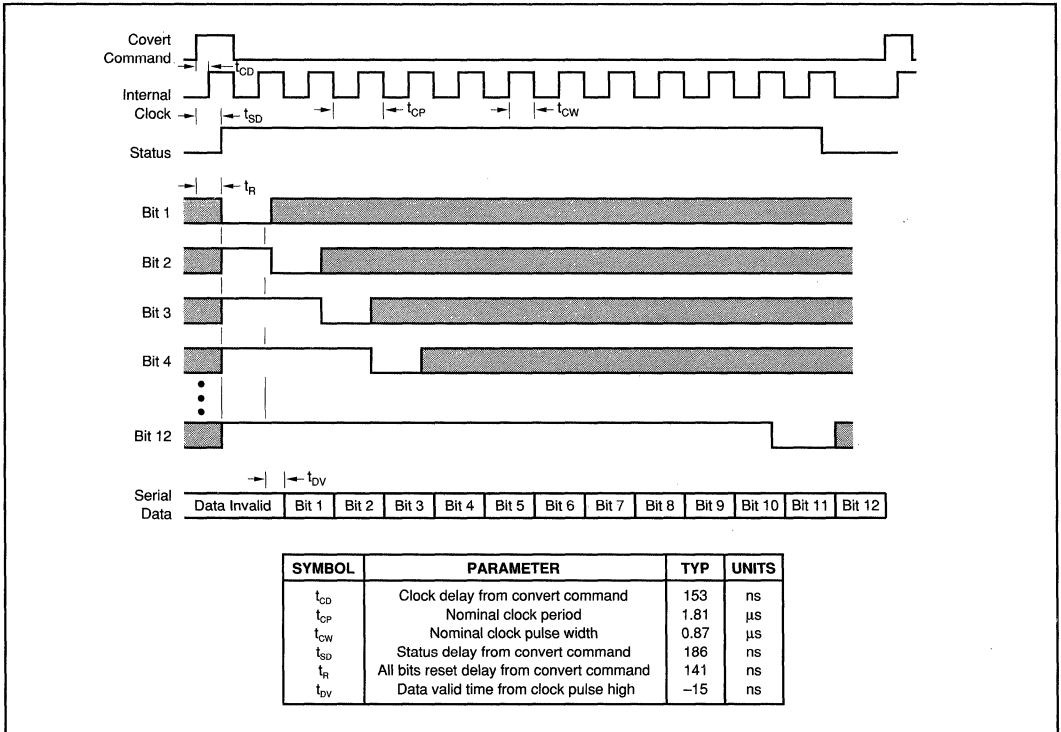
ADC84

ADC85H

ADC87H

ADC84/85/87H

2

IC ANALOG-TO-DIGITAL CONVERTERS

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FEATURES

● **INDUSTRY STANDARD 12-BIT A/D CONVERTERS**

● **COMPLETE WITH CLOCK AND INPUT BUFFER**

● **HIGH SPEED CONVERSION: 10μs (max)**

● **REDUCED CHIP COUNT—HIGH RELIABILITY**

● **LOWER POWER DISSIPATION: 450MW (typ)**

● **±0.012% max LINEARITY ERROR**

● **THREE TEMPERATURE RANGES:**
  0°C to +70°C — ADC84
  –25°C to +85°C — ADC85H
  –55°C to +125°C — ADC87H

● **NO MISSING CODES OVER FULL TEMPERATURE RANGE**

● **PARALLEL AND SERIAL OUTPUTS**

● **±12V OR ±15V POWER SUPPLY OPERATION**

● **HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP**

DESCRIPTION

ADC84, ADC85H, and ADC87H analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

They are complete with internal reference and input buffer amplifier. Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast 10μs conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ±12VDC or ±15VDC and +5VDC.

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SPECIFICATIONS

ELECTRICAL

Specified at +25°C and rated supplies, unless otherwise noted.

PARAMETER	ADC84KG-12[(1)] MIN	TYP	MAX	ADC85H-12 MIN	TYP	MAX	ADC87H-12 MIN	TYP	MAX	UNITS
RESOLUTION			12			*			*	Bits
ANALOG INPUTS										
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*			*		V
Unipolar		0 to +5, 0 to +10			*			*		V
Impedance (Direct Input): 0 to +5V, ±2.5V	2.45	2.5	2.55	*	*	*	*	*	*	kΩ
0 to +10V, ±5V	4.9	5	5.1	*	*	*	*	*	*	kΩ
±10V	9.8	10	10.2	*	*	*	*	*	*	kΩ
Buffer Amplifier: Impedance	100			*			*			MΩ
Bias Current		50		*			*			nA
Settling Time to 0.01% for 20V Step[(2)]		2		*			*			µs
DIGITAL INPUTS[(3)]										
Convert Command			Postive pulse 50ns (min), trailing edge initiates conversion							
Logic Loading		1			*			*		TTL Load
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error [(4)]		±0.1	±0.25		*	*		*	*	%
Offset Error[(4)]: Unipolar		±0.05	±0.2		*	*		*	*	% of FSR[(5)]
Bipolar		±0.1	±0.25		*	*		*	*	% of FSR
Linearity Error[(6)]			±0.012			*			*	% of FSR
Inherent Quantization Error		±0.5			*			*		LSB
Differential Linearity Error		±0.5			*			*		LSB
No Missing Codes Temperature Range	0		+70	−25		+85	−55		+125	°C
POWER SUPPLY SENSITIVITY										
Gain and Offset: ±15V		±0.004			*			*		% of FSR/%V_S
+5V		±0.001			*			*		% of FSR/%V_S
DRIFT										
Gain			±30			±15			±15	ppm/°C
Offset: Unipolar		±3			±3	±5			±5	ppm of FSR/°C
Bipolar			±15			±7			±10	ppm of FSR/°C
Linearity			±3			±2			±2	ppm of FSR/°C
Monotonicity		Guaranteed			*			*		
CONVERSION TIME			10			*			*	µs
DIGITAL OUTPUT[(3)]										
(All Modes Complementary)										
Parallel Output Codes: Unipolar		CSB			*			*		
Bipolar		COB, CTC			*			*		
Output Drive		2			*			*		TTL Loads
Serial Data Codes (NRZ)		CSB, COB			*			*		
Output Drive		2			*			*		TTL Loads
Status		Logic "1" During Conversion			*			*		
Output Drive		2			*			*		TTL Loads
Internal Clock: Output Drive		2			*			*		TTL Loads
Frequency[(7)]		1.35			*			*		MHz
INTERNAL REFERENCE VOLTAGE										
Reference Output	+6.2	+6.3	+6.4	*	*	*	*	*	*	V
Max. External Current with No Degradation		200				*			*	µA
Tempco of Drift		±20		±5		±10	±5		±10	ppm/°C
POWER SUPPLY REQUIREMENTS										
Rated Supply Voltages		+5, ±12 or ±15			*			*		V
Supply Ranges: V_DD	+4.75		+5.25	*		*	*		*	V
±V_CC	±11.4		±16.5	*		*	*		*	V
Supply Drain: +I_CC			20			*			*	mA
−I_CC			25			*			*	mA
I_DD			10			*			*	mA
Total Power Dissipation		450	725	*		*	*		*	mW
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating (with Derated Specs)	−25		+85	−55		+125				°C
Storage	−65		+150	*		*	*		*	°C

*Specification is the same as ADC84KG-12.

NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6µs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V (min). For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.

CONNECTION DIAGRAM — ADC84, 85H, 87H

Top View

Pin	Signal		Pin	Signal
1	(LSB for 12 bits) Bit 12		32	Serial Out
2	Bit 11		31	$-V_{CC}$
3	(LSB for 10 bits) Bit 10		30	Buffer In
4	Bit 9		29	Buffer Out
5	Bit 8		28	$+V_{CC}$
6	Bit 7		27	Gain Adjust
7	Bit 6		26	Analog Common
8	Bit 5		25	R_2 20V Range
9	Bit 4		24	R_1 10V Range
10	Bit 3		23	Bipolar Offset
11	Bit 2		22	Comparator In
12	Bit 1 (MSB)		21	Convert Command
13	Bit 1 (MSB)		20	Status
14	Short Cycle		19	Clock Out
15	Digital Common[1]		18	Reference Out (+6.3V)
16	V_{DD}		17	Clock Rate Control

Internal blocks: SAR/Clock Logic, 12-Bit D/A Converter (Internal Reference), 5kΩ, 5kΩ, 6.3kΩ

NOTE: (1) Metal lid of package is connected to pin 15 (Digital Common).

ORDERING INFORMATION

MODEL	RESOLUTION (Bits)	TEMPERATURE RANGE
ADC84KG-10	10	0°C to +70°C
ADC84KG-12	12	0°C to +70°C
ADC85H-12	12	−25°C to +85°C
ADC87H-12	12	−55°C to +125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC84KG-10	Case Ceramic DIP	172-5
ADC84KG-12	Case Ceramic DIP	172-5
ADC85H-12	32-Pin Side-brazed	172-5
ADC87H-12	32-Pin Side-brazed	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ADC84/85/87H

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FIGURE 1. Timing Diagram.

NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 10.5µs for 12 bits and 6.4µs for 10 bits. (3) Use trailing edge of clock to strobe serial output

BURR - BROWN®

ADC574A

Microprocessor-Compatible
ANALOG-TO-DIGITAL CONVERTER

ADC574A

FEATURES

● **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, or 16-BIT MICROPROCESSOR BUS INTERFACE**

● **IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS**
 Conversion Time: 25µs max
 Bus Access Time: 150ns max
 A$_O$ Input: Bus Contention During Read Operation Eliminated

● **DUAL IN-LINE PLASTIC, PLCC AND HERMETIC CERAMIC**

● **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**

● **NO MISSING CODES OVER TEMPERATURE:**
 0°C to +75°C: ADC574AJ and K Grades
 −55°C to +125°C: ADC574ASH, TH

DESCRIPTION

The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed

for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 25µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, and a hermetic side-brazed ceramic DIP.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC574AJP, JH, SH MIN	TYP	MAX	ADC574AKP, KH, TH MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	*	*	*	kΩ
±10V, 0V to +20V	9.4	10	10.6	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	*		*	V
Logic 0	–0.5		+0.8	*		*	V
Current	–5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			*	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(Adjustable to Zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1] : J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < + 12.6V			±2			±1	LSB
–16.5V < V_{EE} < –13.5V or –12.6V < V_{EE} < – 11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			*	LSB
CONVERSION TIME [4]							
8-Bit Cycle	10	13	17	*	*	*	μs
12-Bit Cycle	15	20	25	*	*	*	μs
OUTPUTS							
DIGITAL (DB_{11} – DB_0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar		Unipolar Straight Binary (USB)					
Bipolar		Bipolar Offset Binary (BOB)					
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500μA)	+2.4			*			V
Leakage, Data Bits Only, High -Z State	–5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETERS	ADC574AJP, JH, SH			ADC574AKP, KH, TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	*	*	*	V
Source Current Available for External Loads [5]	2.0			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

* Same specifications as ADC574AJP, AJH, ASH.
NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at ±25°C (see Optional External Full Scale and Offset Adjustments section). (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendors' 574 and 574A type specifications tables. (3) Using internal reference. (4) See Controlling the ADC574A section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common .... 0V to +16.5V
V_{EE} to Digital Common .... 0V to –16.5V
V_{LOGIC} Digital Common .... 0V to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_O, 12/$\overline{8}$, R/$\overline{C}$)
   to Digital Common .... –0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, 10V_{IN})
   to Analog Common .... ±16.5V
20V_{IN} to Analog Common .... ±24V
Ref Out .... Indefinite Short to Common,
                                           Momentary Short to V_{CC}
Max Junction Temperature .... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) .... +300°C
Thermal Resistance, θ_{JA} : Ceramic .... 50°C/W
                                 Plastic .... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC574s. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

    Plastic "–BI" models: +85°C
    Ceramic "–BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "–BI" to the base model number (e.g. ADC574AKP-BI).

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})
ADC574AJP	Plastic DIP	0°C to +75°C	±1LSB
ADC574AKP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC574AJH	Ceramic DIP	0°C to +75°C	±1LSB
ADC574AKH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC574ASH	Ceramic DIP	–55°C to +125°C	±1LSB
ADC574ATH	Ceramic DIP	–55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMP (160 Hours)
ADC574AJP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC574AKP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC574AJH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC574AKH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC574ASH-BI	Ceramic DIP	–55°C to +125°C	+125°C
ADC574ATH-BI	Ceramic DIP	–55°C to +125°C	+125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC574AJP	Plastic DIP	215
ADC574AKP	Plastic DIP	215
ADC574AJH	Ceramic DIP	149
ADC574AKH	Ceramic DIP	149
ADC574ASH	Ceramic DIP	149
ADC574ATH	Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).
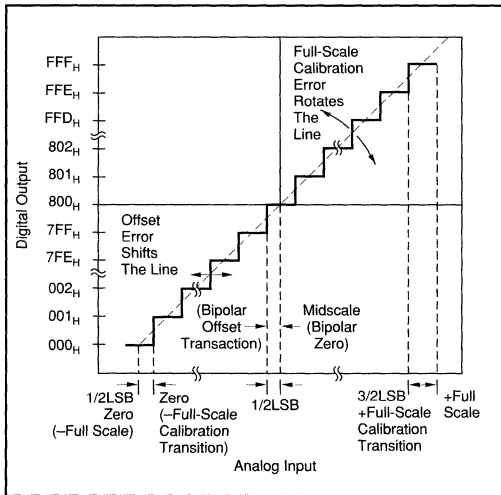

FIGURE 1. ADC574A Transfer Characteristics Terminology.

Thus, for a converter connected for biopolar operation and with a full-scale range (or span) of 20V ($\pm$10V), the zero value of -10V is 2.44mV below the first code transition (000_H to 001_H at -9.99756V) and the plus full-scale value of $+10$V is 7.32mV above the last code transition (FFE_H to FFF_H at $+9.99268$) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination to appear in a monotonically-increasing sequence as the analog input is increased through-

out the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of -1LSB), a missing code will occur.

ADC574AKP, KN, KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2 LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output transiton (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and $\pm$12V or $\pm$15V. The major effect of power supply voltage

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined as:	$\pm$10V	$\pm$5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\dfrac{FSR}{2^n}$ n = 8 n =12	$\dfrac{20V}{2^n}$ 78.13mV 4.88mV	$\dfrac{10V}{2^n}$ 39.06mV 2.44mV	$\dfrac{10V}{2^n}$ 39.06mV 2.44mV	$\dfrac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FF_H$ to 800_H	+Full-Scale Calibration Midscale Calibration (Bipolar Offset)	+10V − 3/2LSB 0 − 1/2LSB	+5 − 3/2LSB 0 − 1/2LSB	+10V − 3/2LSB +5V − 1/2LSB	+10V − 3/2LSB $\pm$10V − 1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

ADC574A

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10μF tantalum-type capacitors located close to the converter

to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC574A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset and gain adjustments are still perfomed as described below. However, you must recalculate full-scale adjustment voltages proportionately. A fixed metal-film resistor can be used because the input impedance of the ADC574A is trimmed to less than ±6% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC574A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE — UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV
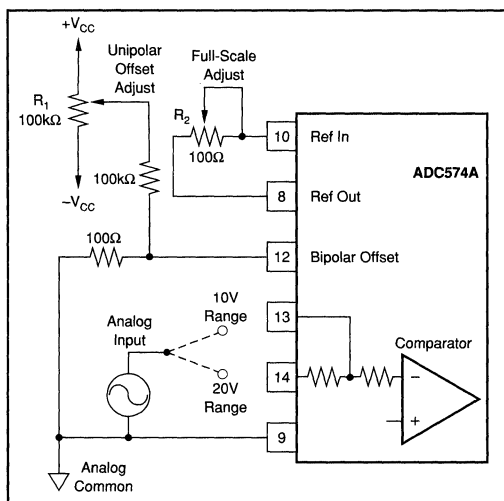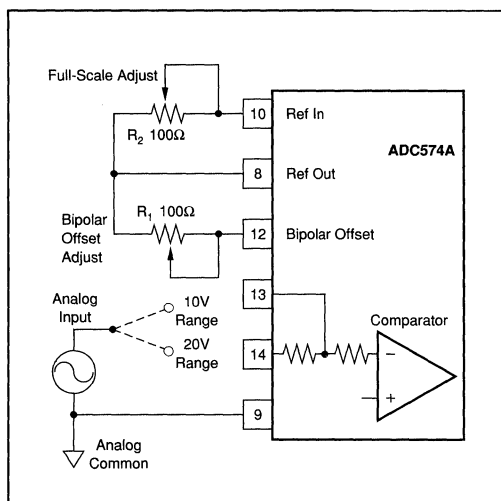
FIGURE 2. Unipolar Configuration.

FIGURE 3. Bipolar Configuration.

for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for

DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC574A

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$(Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode.When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADC574A Control Line Functions.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A$_0$	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit convesion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit convesion
1	↓	0	X	1	Initiate 8-bit coversion
1	0	↓	X	0	Initiate 12-bit convesion
1	0	↓	X	1	Initiate 8-bit coversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A$_0$ are connected to digital common and CE and 12/$\overline{8}$ are connected to V$_{LOGIC}$ (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t$_{HRL}$	Low R/$\overline{C}$ Pulse Width	50			ns
t$_{DS}$	STS Delay from R/$\overline{C}$			200	ns
t$_{HDR}$	Data Valid After R/$\overline{C}$ Low	25			ns
t$_{HS}$	STS Delay After Data Valid	300	400	1000	ns
t$_{HRH}$	High R/$\overline{C}$ Pulse Width	150			ns
t$_{DDR}$	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A$_0$ input, which is latched upon receipt of a conversion start transition (described below). If A$_0$ is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A$_0$ is low. If all 12 bits are read following

FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.
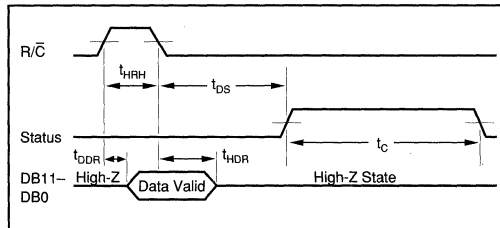
FIGURE 5. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

an 8-bit conversion, the 3LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A$_0$ is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occuring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A$_0$ changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A$_0$, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	$R/\overline{C}$ to CE setup	50	0		ns
t_{HRC}	$R/\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12-bit cycle	15	20	25	μs
	8-bit cycle	10	13	17	μs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	$R/\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	$R/\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	300	400	1000	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

TABLE V. Timing Specifications.
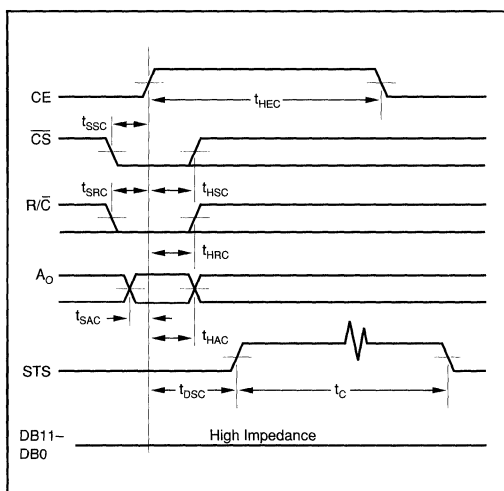
FIGURE 6. Conversion Cycle Timing.
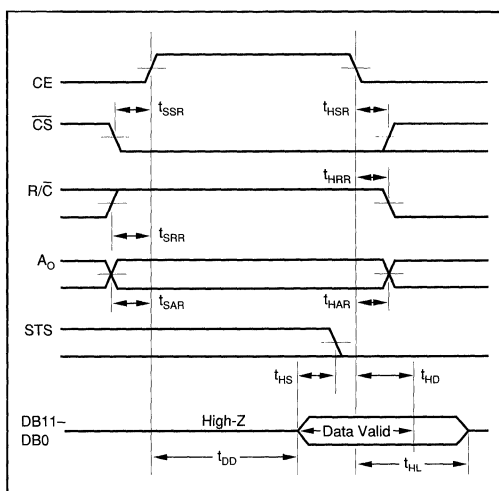
FIGURE 7. Read Cycle Timing.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: $R/\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs $12/\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the $12/\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if de-

sired. When $12/\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When $12/\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

ADC574A

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

When A_O is low, the byte addressed contains the 8MSBs. When A_O is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_O input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15µs (t_{DD} max + t_{HS} min) before STATUS goes low. Refer to Figure 7 for these timing relationships.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.
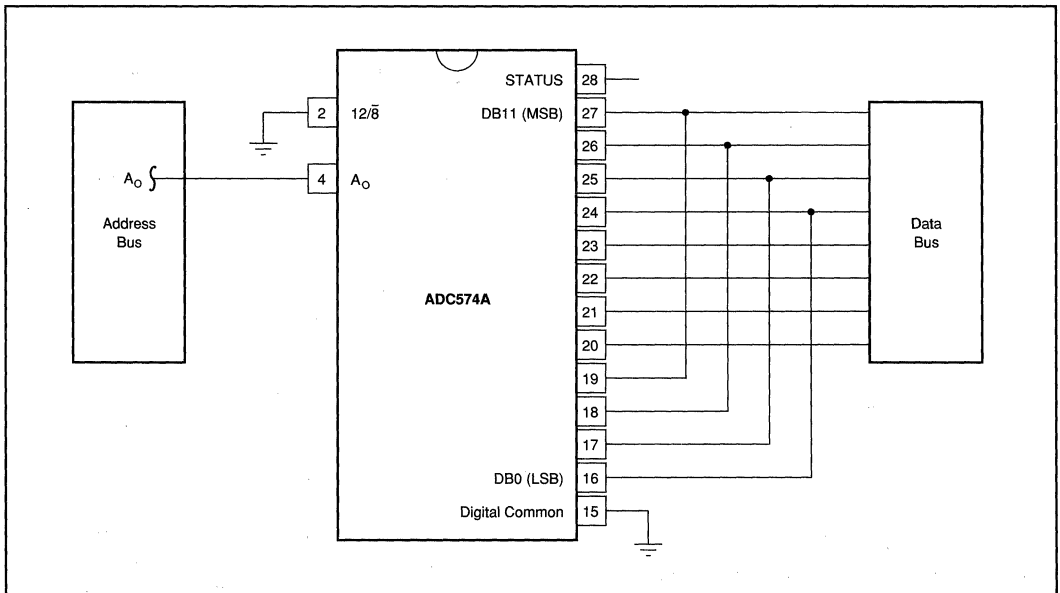
FIGURE 9. Connection to an 8-Bit Bus.

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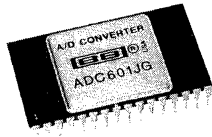
ADC601

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-867.

12-Bit 900ns
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **FAST CONVERSION: 900ns**
● **CAN BE SHORT-CYCLED**
● **INPUT RANGES: ±5V, ±10V, 0 to –10V**
● **HIGH SIGNAL/NOISE RATIO: 68dB**
● **LOW IMD: 75dB**
● **PARALLEL AND SERIAL OUTPUT**
● **32-PIN CERAMIC DIP PACKAGE**

APPLICATIONS

● **DIGITAL SIGNAL PROCESSING**
● **HIGH-SPEED DATA ACQUISITION SYSTEMS**
● **MEDICAL INSTRUMENTATION**
● **ANALYTICAL INSTRUMENTATION**
● **TEST AND IMAGING SYSTEMS**
● **WAVEFORM ANALYZERS**

DESCRIPTION

The ADC601 is a high-speed Duolithic™ (two chips) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADC601 has been tested with several sample/hold amplifiers and distortion results are documented in this data sheet.

The ADC601 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed

with no missing codes over the full input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of ±5V, ±10V and 0V to –10V. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.

Duolithic™ Burr-Brown Corporation

BURR-BROWN®

A/D CONVERTERS, DATA ACQUISITION COMPONENTS **ADC601**

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADC601JG MIN	TYP	MAX	ADC601KG MIN	TYP	MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale(FSR)[1][2]		±5, ±10			*		V
Unipolar	Full Scale(FSR)[1][2]		0 to −10			*		V
Impedance: −10V to 0V, ±5V			1.4			*		kΩ
±10V			2.4			*		kΩ
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[3]	990ns Conversion Time		±0.08	±0.55		*	±0.2	%
Input Offset Error[3]: Unipolar	990ns Conversion Time		±0.12	±1.2		*	±0.5	% of FSR
Bipolar	990ns Conversion Time		±0.08	±0.8		*	±0.25	% of FSR
Integral Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
Differential Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
No Missing Codes				Guaranteed				
Power Supply Rejection of Offset and Gain	$\Delta +V_{CC} = \pm5\%$		±0.0036			*		%FSR/%V_{CC}
	$\Delta -V_{CC} = \pm5\%$		±0.0005			*		%FSR/%V_{CC}
	$\Delta +V_{DD} = \pm5\%$		±0.001				*	%FSR/%V_{DD}
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS					
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			−150				µA
	Logic High			−150				µA
Convert Command			High Level When Converting					
CONVERSION TIME								
Factory Set	Without User Adjustment		0.9	1		*	*	µs
Power Supply Rejection of Conversion Time	$D +V_{DD} = \pm5\%$		±1			*		ns/%V_{DD}
OUTPUT								
Logic Family			TTL-Compatible CMOS					
Bits 1 through 12, Serial, Status, Clock Out	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4	*		*	V
	Logic High, I_{OH} = −1mA	+2.7	+4.9		*	*	*	V
Internal Clock Frequency			13			*		MHz
Status			Low Level When Data Valid					
DYNAMIC CHARACTERISTICS [4][5][6] Tested using Sample/Hold Amplifier SHC804 and ADC601 (See Typical Performance Curves)								
Differential Linearity Error	f_C = 10kHz: 68.3% of All Codes		0.5			0.4		LSB
	99.7% of All Codes		0.8			0.6		LSB
	100% of All Codes		1.0			0.7		LSB
Total Harmonic Distortion	f_C = 10kHz, f_S = 500kHz		−70			*		dBc
	f_C = 10kHz, f_S = 1MHz		−74			*		dBc
	f_C = 250kHz, f_S = 500kHz		−70			*		dBc
	f_C = 500kHz, f_S = 1MHz		−68			*		dBc
Two-Tone Intermodulation Distortion[7]	f_C = 11kHz and 15kHz, f_S = 500kHz		−79			*		dBc
	f_C = 50kHz and 55kHz, f_S = 500kHz		−78			*		dBc
	f_C = 90kHz and 110kHz, f_S = 500kHz		−77			*		dBc
Signal-to-Noise and Distortion (SINAD) Ratio	f_C = 250kHz, f_S = 500kHz		66			*		dB
	f_C = 500kHz, f_S = 1MHz		65			*		dB
Signal-to-Noise Ratio (SNR)	f_C = 250kHz, f_S = 500kHz		68			*		dB
	f_C = 500kHz, f_S = 1MHz		67			*		dB
PERFORMANCE OVER TEMPERATURE								
Gain	T_{MIN} to T_{MAX}		±10	±30		*	*	ppm of FSR/°C
Input Offset: Unipolar	T_{MIN} to T_{MAX}		±2	±7		*	*	ppm of FSR/°C
Bipolar	T_{MIN} to T_{MAX}		±3	±10		*	*	ppm of FSR/°C
Internal Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
Differential Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
No Missing Codes	0.9µs Conversion Time T_{MIN} to T_{MAX}			Guaranteed				
Conversion Drift			2			*		ns/°C

SPECIFICATIONS (CONT)

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = $\pm$15V, +V_{DD} = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADC601JG			ADC601KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: +V_{CC}		+14.25	+15	+15.75	*	*	*	V
−V_{CC}		−14.25	−15	−15.75	*	*	*	V
+V_{DD}		+4.75	+5	+5.25	*	*	*	V
Supply Currents: +I_{CC}			5.4	7.0		*	*	mA
−I_{CC}			−65	−84.5		*	*	mA
+I_{DD}			53	68.9		*	*	mA
Power Consumption	Nominal $\pm V_{CC}$ and +V_{DD}		1.3	1.7		*	*	W
Thermal Resistance, θ_{JC}			25			*	*	°C/W
TEMPERATURE RANGE[8]								
Specification		0		+70	*		*	°C
Operating		−25		+85	*		*	°C

* Same specifications as for ADC601JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) Dynamic tests are performed using SHC804 with ADC601 unless otherwise specified. Performance may vary depending upon choice of sample/hold. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = 0dB; f_c = input frequency; f_s = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. For example, unit connected for $\pm$10V has 20V FSR. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board; with the test device in a (zero insertion force) socket. Thermal resistance will be lower if the ADC601 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	$\pm$18V
+V_{DD}	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{CC}$
Comparator Input	–3.7V to +0.7V
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

```
                                    ADC601  ( )  G
Basic Model Number ─────────────────┘       │   │
Performance Grade Code ──────────────────────┘   │
    J, K: 0°C to +70°C Case Temperature           │
Package Code ─────────────────────────────────────┘
    G: Ceramic DIP
```

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC601JG	32-Pin Hermetic DIP	172–2
ADC601KG	32-Pin Hermetic DIP	172–2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.
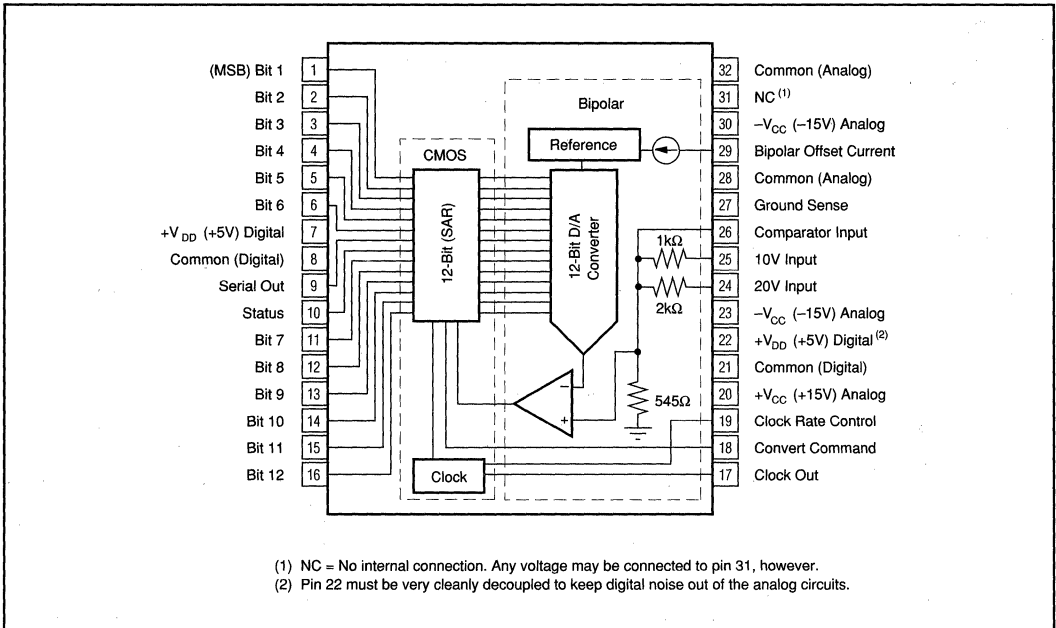
ADC601

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN CONFIGURATION

(MSB) Bit 1	1		32	Common (Analog)
Bit 2	2		31	NC [1]
Bit 3	3	Bipolar	30	−V$_{CC}$ (−15V) Analog
Bit 4	4	Reference	29	Bipolar Offset Current
Bit 5	5	CMOS	28	Common (Analog)
Bit 6	6		27	Ground Sense
+V$_{DD}$ (+5V) Digital	7	12-Bit (SAR) / 12-Bit D/A Converter	26	Comparator Input
Common (Digital)	8		25	10V Input
Serial Out	9	1kΩ	24	20V Input
Status	10	2kΩ	23	−V$_{CC}$ (−15V) Analog
Bit 7	11		22	+V$_{DD}$ (+5V) Digital [2]
Bit 8	12		21	Common (Digital)
Bit 9	13	545Ω	20	+V$_{CC}$ (+15V) Analog
Bit 10	14		19	Clock Rate Control
Bit 11	15		18	Convert Command
Bit 12	16	Clock	17	Clock Out

(1) NC = No internal connection. Any voltage may be connected to pin 31, however.
(2) Pin 22 must be very cleanly decoupled to keep digital noise out of the analog circuits.

PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data capable of sinking 3.2mA.
9	Serial Out	12-bit serial data output synchronized with the negative edge of each appropriate clock cycle.
10	Status	Conversion status strobe is high during data conversion; low when parallel data is valid. Negative edge may be used to latch parallel data, however, appropriate latch set-up time must be provided. Refer to t$_{BBL}$ in the ADC601 timing diagram.
17	Clock Out	Negative edge indicates when serial data is valid. After convert command goes high, fist cycle clocks bit 1 (MSB). The clock continues to run when convert command is high and resets low with convert command.
18	Convert Command	High transition starts conversion; and should remain high during conversion. Low will reset clock and SAR logic.
19	Clock Rate Control	May be used to increase clock speed, by increasing the positive portion of the clock. High is normal operation.
24	20V Input	20V input range allows ±10Vp-p analog input signal. Short to ground when not used.
25	10V Input	10V input range allows 0 to −10Vp-p or ±5Vp-p input range.
26	Comparator In	Only used in bipolar mode when it is connected to bipolar offset pin through short lead with low resistance.
27	Ground Sense	Ground Sense pin. (See text for use).
29	Bipolar Offset Current	Bipolar offset current short to comparator In through very short lead with very low resistance for bipolar operation. Short to ground for unipolar operation.

BURR - BROWN®

ADC603

12-Bit 10MHz Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● HIGH SPURIOUS-FREE DYNAMIC RANGE
● SAMPLE RATE: DC to 10MHz
● HIGH SIGNAL/NOISE RATIO: 68.2dB
● HIGH SINAD RATIO: 66dB
● LOW HARMONIC DISTORTION: –69.6dBc
● LOW INTERMOD. DISTORTION: –77.7dBc
● COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
● 46-PIN DIP PACKAGE
● 0°C TO +70°C AND –55°C TO +100°C

APPLICATIONS

● DIGITAL SIGNAL PROCESSING
● RADAR SIGNAL ANALYSIS
● TRANSIENT SIGNAL RECORDING
● FFT SPECTRUM ANALYSIS
● HIGH-SPEED DATA ACQUISITION
● IR IMAGING SYSTEMS
● DIGITAL RECEIVERS
● SIGINT, ECM, AND EW SYSTEMS
● DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC603 is an high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion.

The ADC603 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. Logic is TTL. Two temperature ranges are available: 0°C to +70°C (JH, KH) and –55°C to +100°C, environmentally screened (SHQ).

A/D CONVERTERS, DATA ACQUISITION COMPONENTS — **ADC603** — **2**

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH			ADC603KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	−1.25		+1.25	*	*	*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family		TTL Compatible						
Convert Command	Start Conversion	Positive Edge						
Pulse Width	t = Conversion Period	10		t − 20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	1		±0.1	0.8	%FSR[1]
Input Offset	DC		±0.2	0.75		*	0.5	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.3			0.25	0.5	LSB
	99.7% of all Codes		0.4			0.3	0.65	LSB
	100% of all Codes		0.5	1		0.4	0.75	LSB
No Missing Codes		Guaranteed			Guaranteed			
Power Supply Rejection	Δ $+V_{CC}$ = ±10%		±0.03			*	±0.07	%FSR/%
	Δ $-V_{CC}$ = ±10%		±0.04			*	±0.07	%FSR/%
	Δ $+V_{DD1}$ = ±10%		±0.004			*	±0.03	%FSR/%
	Δ $-V_{DD2}$ = ±10%		±0.01			*	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable	1, 2 or 3 Convert Command Periods						
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.3			*		LSB
	99.7% of all Codes		0.75			0.5		LSB
	100% of all Codes		1	1.25		0.6	0.9	LSB
Spurious Free Dynamic Range								
f = 5MHz (−0.5dB)	f_s = 9.99MHz	63	72		66	74		dB
Total Harmonic Distortion[2](THD)								
f = 5MHz (−0.5dB)	f_s = 9.99MHz		−68	−61		−69	−64	dBc[3]
f = 100kHz			−70	−65		−72	−68	dBc
Two-Tone Intermodulation Distortion[2][4]								
f = 2.2MHz (−6.5dB)	f_s = 8.006MHz		−75	−67		−7	−71	dBc
f = 2.5MHz (−6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (−0.5dB)	f_s = 9.99MHz	60	65		62	66		dB
f = 100kHz (−0.5dB)		64	67		66	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (−0.5dB)	f_s = 9.99MHz	63	67		66	68		dB
f = 100kHz (−0.5dB)		66	68		67	70		dB
Aperture Delay Time			−5			*	+9	ns
Aperture Jitter			9			*	20	ps rms
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*	140	ns
OUTPUTS								
Logic Family		TTL Compatible						
Logic Coding	Logic Selectable	Two's Complement or Inverted Two's Complement						
Logic Levels	Logic LO, I_{OL} = −3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		−14.25	−15	−15.75	−14.25	−15	−15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		−4.95	−5.2	−5.46	−4.95	−5.2	−5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			−60			−60	−80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			−565			−565	−630	mA
Power Consumption	Operating		6.1			6.1		W

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH MIN	ADC603JH TYP	ADC603JH MAX	ADC603KH MIN	ADC603KH TYP	ADC603KH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	1.5		*	1	%FSR
Input Offset	DC		±0.4	1		*	0.5	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.4			0.3	0.6	LSB
	99.7% of all Codes		0.5			0.4	0.75	LSB
	100% of all Codes		0.75			0.6	1	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta + V_{CC} = \pm 10\%$		±0.04			*	±0.08	%FSR/%
	$\Delta - V_{CC} = \pm 10\%$		±0.05			*	±0.08	%FSR/%
	$\Delta + V_{DD1} = \pm 10\%$		±0.004			*	±0.05	%FSR/%
	$\Delta - V_{DD2} = \pm 10\%$		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.5			0.4		LSB
	99.7% of all Codes		1			0.6		LSB
	100% of all Codes		1.25	1.5		0.7	1	LSB
Spurious Free Dynamic Range[6]	f = 5MHz (–0.5dB)	60	65		65	72		dB
Total Harmonic Distortion[2]								
f = 5MHz (–0.5dB)	$f_S = 9.99$MHz		–67	–58		–69	–62	dBc
f = 100kHz			–69	–62		–69.5	–67	dBc
Two-Tone Intermodulation Distortion								
f = 2.2MHz (–6.5dB)	$f_S = 8.006$MHz		–72	–64		–74.5	–68	dBc
f = 2.5MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (–0.5dB)	$f_S = 9.99$MHz	57	65		61	65.5		dB
f = 100kHz (–0.5dB)		62	66		64	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (–0.5dB)	$f_S = 9.99$MHz	60	67		64	68		dB
f = 100kHz (–0.5dB)		64	68		66	69.5		dB
Aperture Delay Time			–6			*	+10	ns
Aperture Jitter			10			*	20	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		70		50	*		MHz
Full Power	0dB Input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale Input		80			*		ns
OUTPUTS								
Logic Levels								
Logic LO, $I_{OL} = -3.2$mA		0	+0.3	+0.8	*	*	+0.5	V
Logic HI, $I_{OH} = 160\mu$A		+2.4	+3.5	+5	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	$I_{OL} = -6.4$mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			–61			*	–80	mA
$+I_{DD1}$ [6]			+285			*	+333	mA
$-I_{DD2}$ [7]			–570			*	–630	mA
Power Consumption	Operating		6.1			*		W

* Same specifications as ADC603JH.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level referred to carrier-input signal ≈ 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 6dB lower. (5) SFDR tested at temperature for K grade only. (6) Pins 3 and 30 (analog) typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (7) Pin 6 (analog) typically draws 45% of the total –5.2V current. Pin 31 (digital) typically draws 55%.

ADC603

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS

ELECTRICAL

$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 15-minute warmup $F_S = 10MHz$ ($-55°C$ to $+85°C$), $F_S = 8MHz$ ($+85°C$ to $+100°C$).

PARAMETER	CONDITIONS	ADC603SHQ			UNITS
		MIN	TYP	MAX	
TEMPERATURE RANGE[4]	T_{CASE}	−55		+100	C°
RESOLUTION				12	Bits
ANALOG					
Input Range		−1.25		+1.25	V
Input Resistance		1.5			MΩ
Input Capacitance		5			pF
DIGITAL					
Logic Family			TTL Compatible		
Convert Command	Start Conversion		Positive Edge		
Pulse Width	t = conversion period	10		20	ns
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	DC			1.0	%FSR[1]
Input Offset	DC			1.0	%FSR
Integral Nonlinearity	f = 100kHz		0.75		LSB
Differential Nonlinearity	f = 100KHz, all codes		0.6	1.0	LSB
No Missing Codes			Guaranteed		
Power Supply Rejection	$\Delta + V_{CC} = \pm 10\%$	−0.1		0.1	%FSR%
	$\Delta - V_{CC} = \pm 10\%$	−0.1		0.1	%FSR%
	$\Delta + V_{DD} = \pm 10\%$	−0.05		0.05	%FSR%
	$\Delta - V_{DD} = \pm 10\%$	−0.05		0.05	%FSR%
CONVERSION CHARACTERISTICS					
Sample Rate	$-55°C \le T_C \le +85°C$	DC		10M	Samples/s
	$+85°C \le T_C \le +100°C$	DC		8M	Samples/s
DYNAMIC CHARACTERISTICS					
Differential Nonlinearity	f = 4.9MHz: All Codes		0.6	1.0	LSB
Spurious Free Dynamic Range	f = 5.0MHz (−0.5dB)	65	72		dBc
Total Harmonic Distortion[2]	f = 5.0MHz (−0.5dB)		−68	−63	dBc
	f = 100kHz (−0.5dB)		−73	−68	dBc
2-Tone Intermodulation Distortion[3]					
$f_1 = 2.2MHz$ (−6.5dB)			−74	−70	
$f_2 = 2.3MHz$ (−6.5dB)					dBc
Signal-to-Noise and Distortion	f = 5.0MHz (−0.5dB)	63	65		dB
(SINAD ratio)	f = 100kHz (−0.5dB)	67	69		dB
Signal-to-Noise Ratio (SNR)	f = 5.0MHz (−0.5dB)	65	68		dB
	f = 100kHz (−0.5dB)	66	69		dB
Aperture Delay Time				10	ns
Aperture Jitter				10	ps rms
Analog Input Bandwidth (−3dB)					
Small Signal	−20dB Input		70		MHz
Full Power	0dB Input		40		MHz
Overload Recovery Time	2 x Full Scale Input			140	ns
OUTPUTS					
Logic Family			TTL Compatible		
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement		
Logic Levels	Logic LO, $I_{OL} = -3.2mA$	0	+0.3	+0.5	V
	Logic HI, $I_{OH} = 160\mu A$	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		ns
Tri-State Enable/Disable Time	$I_{OL} = -6.4mA$, 50% In to 50% Out		42	100	ns
Data Valid Pulse Width		20	45	60	ns
POWER SUPPLY REQUIREMENTS					
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	V
$-V_{CC}$		−14.25	−15	−15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	V
$-V_{DD2}$		−4.95	−5.2	−5.46	V
Supply Currents: $+I_{CC}$	Operating		+60	+80	mA
$-I_{CC}$			−60	−80	mA
$+I_{DD1}$			+280	+333	mA
$-I_{DD2}$			−565	−630	mA
Power Consumption	Operating		6.1		W

NOTE: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) dBc = level referred to carrier-input signal ≈ 0dB; f = input frequency; F_S = sampling frequency. (3) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 6dB lower. (4) Temperature is specified as −55°C ambient, +100°C case.

PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	NC	45	Analog Signal In
3	+V_{DD1} (+5V) Analog	44	+V_{CC} (+15V) Analog
4	S/H Out	43	–V_{CC} (–15V) Analog
5	A/D In	42	NC
6	–V_{DD2} (–5.2V) Analog	41	NC
7	NC	40	NC
8	NC	39	DNC
9	Bit 1(MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	+V_{CC} (+15V) Analog
14	Bit 6	33	–V_{CC} (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	–V_{DD2} (–5.2V) Digital
17	Bit 9	30	+V_{DD1} (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12 (LSB)	27	Output Logic Invert
21	+V_{DD1} (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State ENABLE
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC603 ( ) H Q

Basic Model Number ——————
Performance Grade Code ——
   J, K: 0°C to +70°C Case Temperature
   S: –55°C to +100°C Case Temperature
Package Code ——
   H: Metal and Ceramic
Environmental Screening Option ——————

ABSOLUTE MAXIMUM RATINGS

±V_{CC} .... ±16.5V
+V_{DD1} .... +7V
±V_{DD2} .... –7V
Analog Input .... ±5V
Logic Input .... –0.5V to +V_{DD1}
Case Temperature .... +125°C
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +165°C
Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

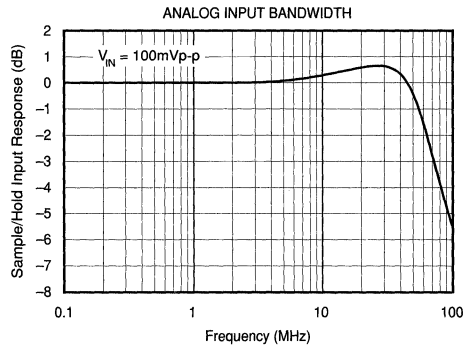| MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC603JH	Metal and Ceramic	234
ADC603KH	Metal and Ceramic	234
ADC603SHQ	Metal and Ceramic	234

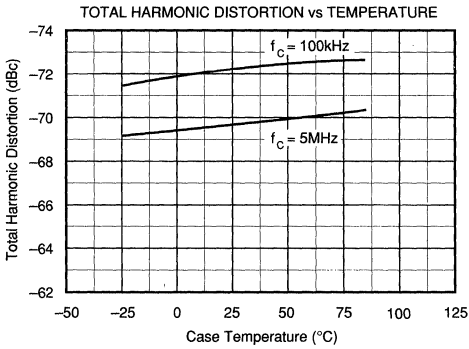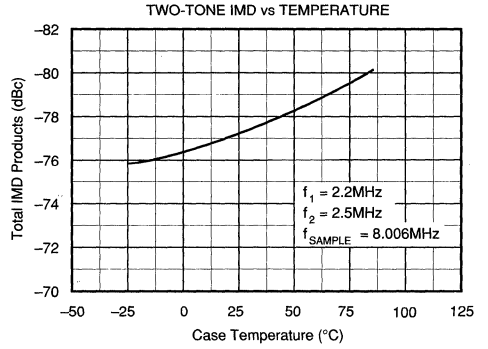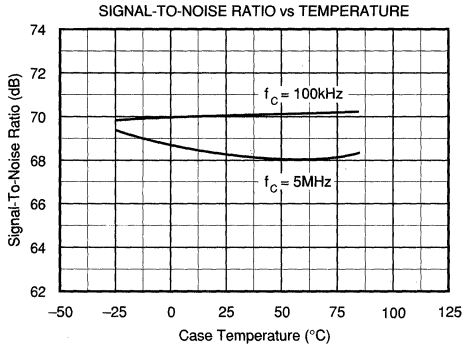NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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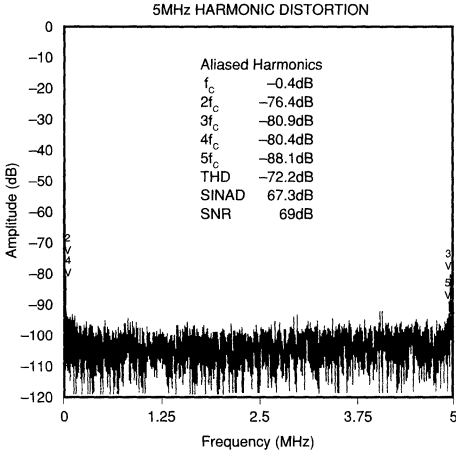**A/D CONVERTERS, DATA ACQUISITION COMPONENTS**

TYPICAL PERFORMANCE CURVES

$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 15-minute warmup, and $T_C = +25°C$, unless otherwise noted. All plots are 4096 point FFTs.
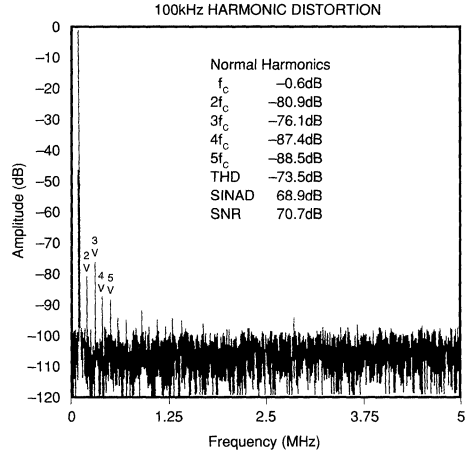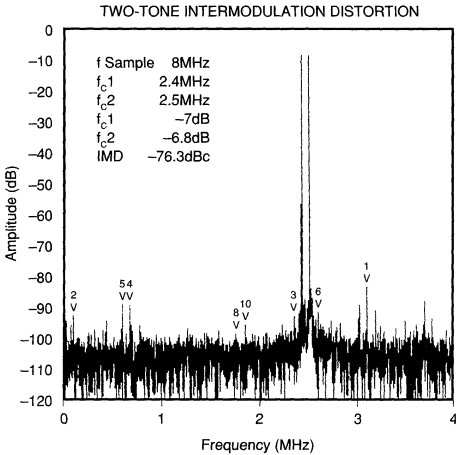
SIGNAL-TO-NOISE RATIO vs TEMPERATURE

TWO-TONE IMD vs TEMPERATURE

TOTAL HARMONIC DISTORTION vs TEMPERATURE

ANALOG INPUT BANDWIDTH

Burr-Brown IC Data Book—Data Conversion Products **BURR - BROWN** **BB**

TYPICAL PERFORMANCE CURVES (CONT)

±V$_{CC}$ = ±15V, +V$_{DD1}$ = +5V, −V$_{DD2}$ = −5.2V, R$_S$= 50Ω, 10MHz sample rate, 15-minute warmup, and T$_C$ = +25°C, unless otherwise noted. All plots are 4096-point FFTs.

5MHz HARMONIC DISTORTION

Aliased Harmonics
f$_c$	−0.4dB
2f$_c$	−76.4dB
3f$_c$	−80.9dB
4f$_c$	−80.4dB
5f$_c$	−88.1dB
THD	−72.2dB
SINAD	67.3dB
SNR	69dB

NOTE: Sample rate = 9.99 MHz; even harmonics folded to left edge and odd harmonics folded to right edge. Any non-harmonically related spurious products show clearly in the center.

100kHz HARMONIC DISTORTION

Normal Harmonics
f$_c$	−0.6dB
2f$_c$	−80.9dB
3f$_c$	−76.1dB
4f$_c$	−87.4dB
5f$_c$	−88.5dB
THD	−73.5dB
SINAD	68.9dB
SNR	70.7dB

NOTE: Sample rate = 9.99 MHz; harmonics appear in normal order.

TWO-TONE INTERMODULATION DISTORTION

f Sample	8MHz
f$_c$1	2.4MHz
f$_c$2	2.5MHz
f$_c$1	−7dB
f$_c$2	−6.8dB
IMD	−76.3dBc

NOTE: Sample rate = 8MHz; highest IMD product is cursor number 1: f1 +f2. The second-order −76.3dBc product determines the wideband spurious-free dynamic range of this example. For RF applications third-order IMD products such as those at cursors 3 and 6 are the limiting spurs. Under these conditions spurious-free dynamic range is limited by 2f2+ f1 to 84.3dBc.

Sample rates of 10MHz show similar results.

TWO-TONE INTERMODULATION DISTORTION PRODUCTS

CURSOR	IMD	FREQUENCY	dB
1	2nd order : f1 + f2	3.086395621579MHz	−83.1
2	2nd order : f2 − f1	0.080140734949MHz	−91.4
3	3rd order : 2f1 − f2	2.339718530102MHz	−92.4
4	3rd order : 2f1 + f2	0.666536356529MHz	−88.4
5	3rd order : 2f2 − f1	0.586395621579MHz	−88.2
6	3rd order : 2f2 + f1	2.580140734949MHz	−91.1
7	4th order : 3f1 − f2	3.246677091478MHz	−109
8	4th order : 3f1 + f2	1.753322908522MHz	−100
9	4th order : 2f2 − 2f1	0.130281469898MHz	−114.8
10	4th order : 2f2 + 2f1	1.833463643471MHz	−95
11	4th order : 3f2 − f1	2.926114151681MHz	−115.4
12	4th order : 3f2 + f1	1.913604378421MHz	−98.2

NOTE: IMD products in this table are refered to full-scale (0dB). To refer IMD to carrier, subtract the larger of f$_c$1 or f$_c$2. In this example, IMD referred to carrier will be 6.8dB higher (worse) than the full-scale value shown.

THEORY OF OPERATION

The ADC603 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC603 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer,

the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns, while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) function are performed by multiplexing one high-speed 7-bit resolution converter formed by parallel-connecting two 6-bit flash ADCs. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.
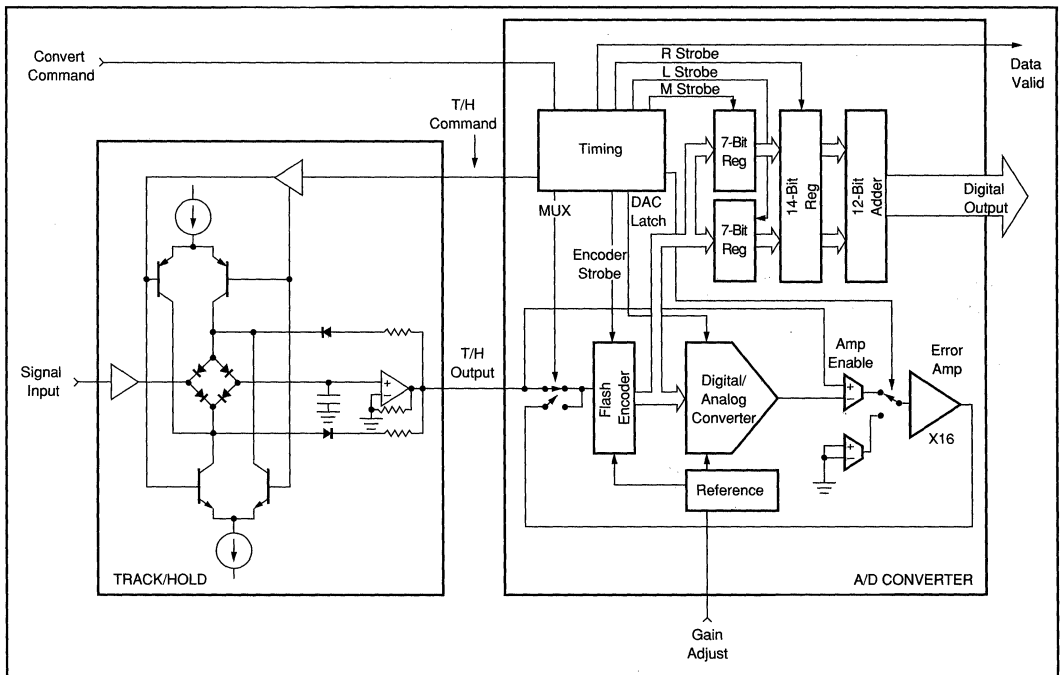

FIGURE 1. ADC603 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC603. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC603 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 67ns ADC conversion time. ADC603 conversion rates are therefore possible somewhat above the 10MHz specification, but S/H acquisition time is sacrificed and accuracy is rapidly degraded. Converters with guaranteed operation at 10.24MHz sample rate are available on special order.

The output of the MSB and LSB encoders are read into separate 7-bit latches. The latched MSB data, along with latched LSB data, is then read into a 14-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 6ns after the output data has settled to allow sufficient set-up time for an external TTL data latch. A high-speed latch such as a 74F174 is recommended.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the

most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC603 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To
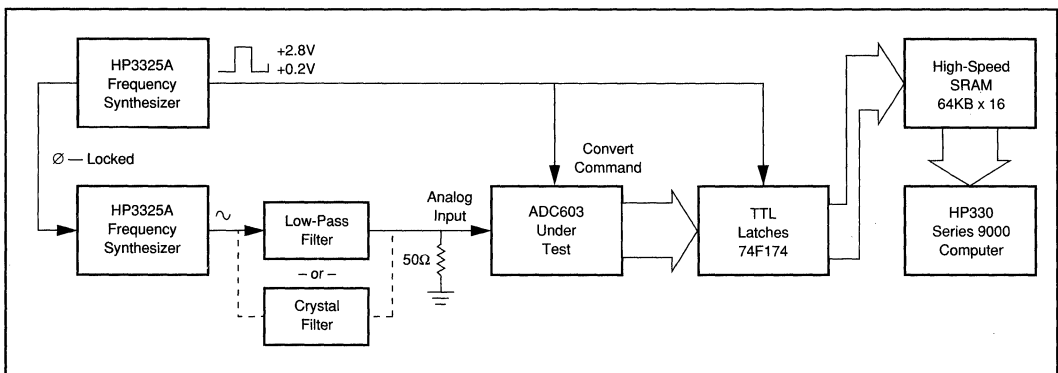

FIGURE 2. Block Diagram of FFT Test for THD, SNR, and SINAD.

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assure that the majority of codes are exercised in the ADC603 (12 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (i.e., a 10-sample average of 512-point FFTs).

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

4. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.

2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.

3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator.

4. Test signal generators must have exceptional noise performance (better than –155dBC/Hz) to achieve accurate SNR measurements.[4] Good generators together with fifth-order elliptical bandpass filters are recommended for

9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2x cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

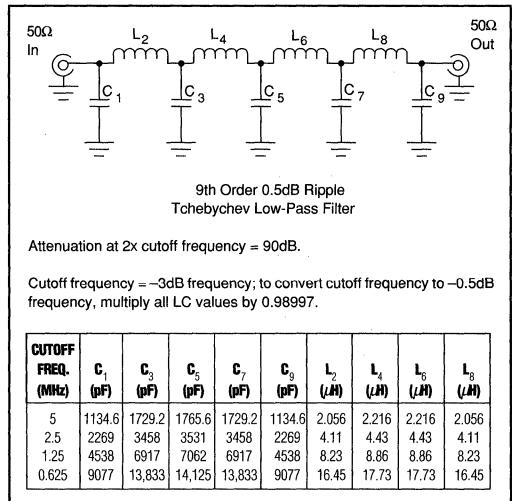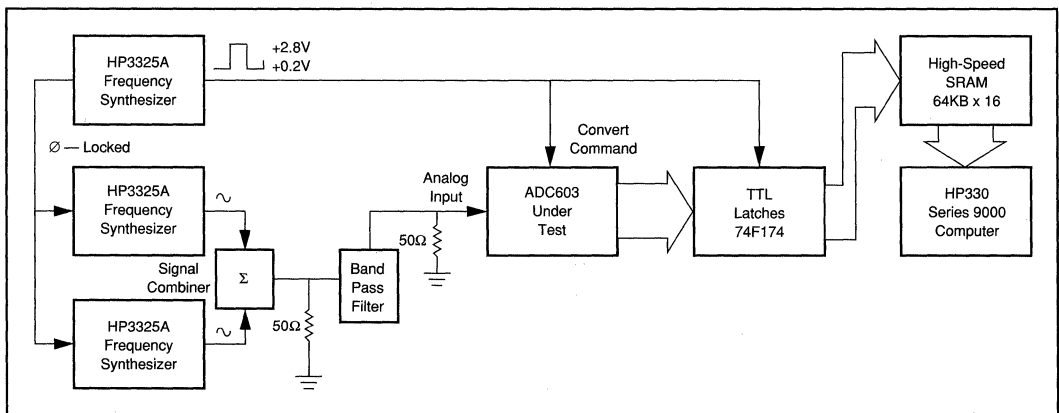| CUTOFF FREQ. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (μH)	L_4 (μH)	L_6 (μH)	L_8 (μH)
5	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

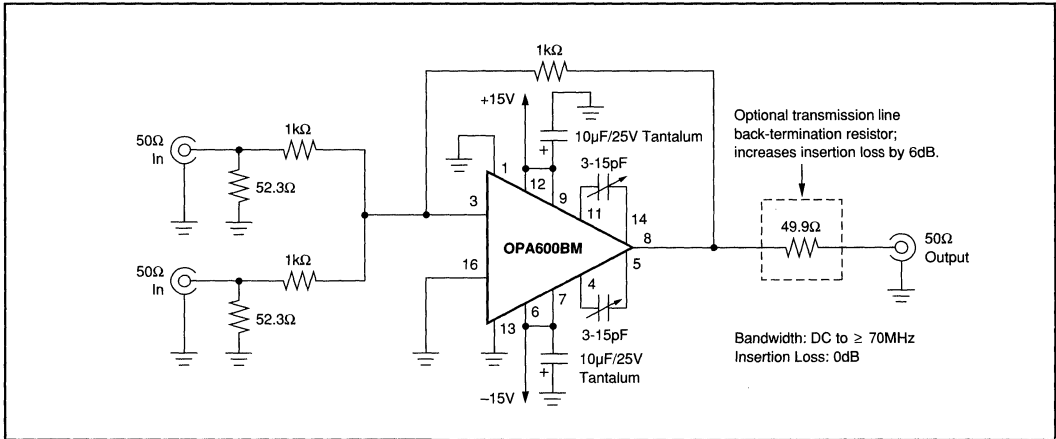FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.

FIGURE 5. Active Signal Combiner.

SNR tests. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.

5. The analog input of the ADC603 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA642/643. Short leads are necessary to prevent digital noise pickup.

6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. Short leads are necessary to preserve fast TTL rise times.

7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 5. This circuit will provide excellent performance from DC to 5MHz with harmonic and intermodulation distortion products typically better than –70dBC. A passive (hybrid transformer) signal combiner can also be used (Figure 6) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBC for the powdered-iron core specified.

8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]

9. Digital data must be latched into an external TTL 12-bit register by the Data Valid output pulse or by using the convert command pulse (Figures 11, 12, 13, and 14). Latches should be mounted on PC boards in very close proximity to the ADC603. Avoid long leads.
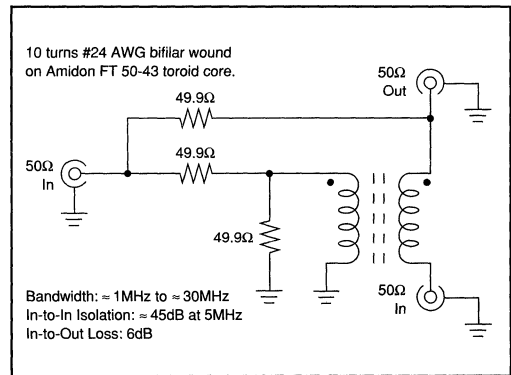

FIGURE 6. Passive Signal Combiner.

10. Do not overload the data output logic. These outputs are designed to drive 2 TTL loads. Do not connect ADC603 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.

11. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[5, 6] Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.

12. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.

13. Floating inputs can eliminate ground-loop noise. A simple common-mode choke (balun) shown in Figure 7 and 8, or a differential amplifier (Figure 9 and 10) can reduce analog input noise.

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14. Connect analog and digital ground pins of the ADC603 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering[7] is optional and may improve noise rejection.

NOTES:

1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.

2. SINAD test includes harmonics whereas SNR does not include these important spurious products.

3. If IMD is referenced to peak envelope power, distortion will be of 6dB better.

4. "Test Report: FFT Characterization of Burr-Brown ADC600K", Signal Conversion Ltd., Swansea, Wales, U.K.

5. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.

6. Motorola MECL, Motorola Corp.

7. Murata-Erie BNX002-01.
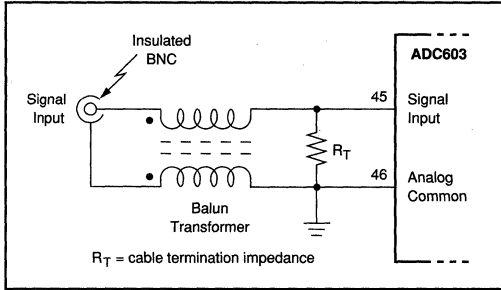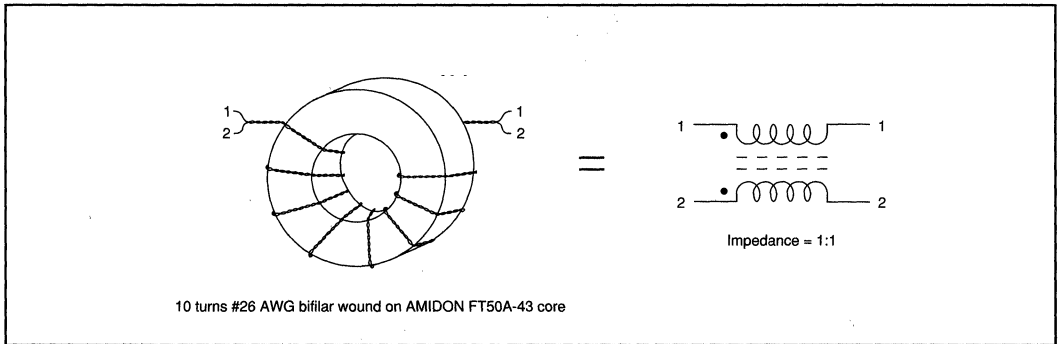

FIGURE 7. Floating-Input Balun Transformer.
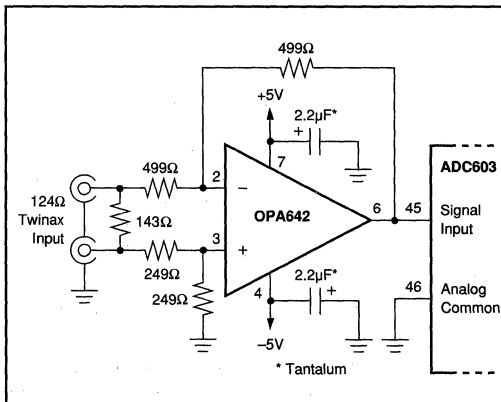

FIGURE 8. Balun Transformer Windings.

FIGURE 9. Differential Input Buffer Amplifier
(Gain = –1V/V).
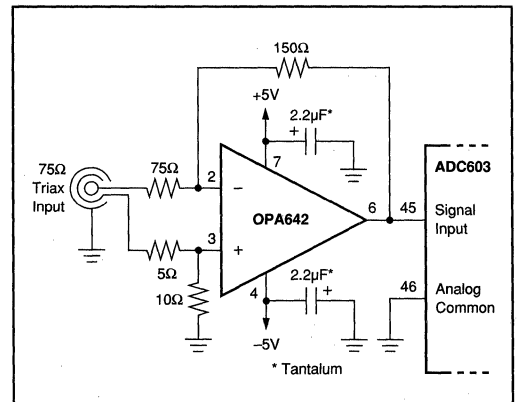

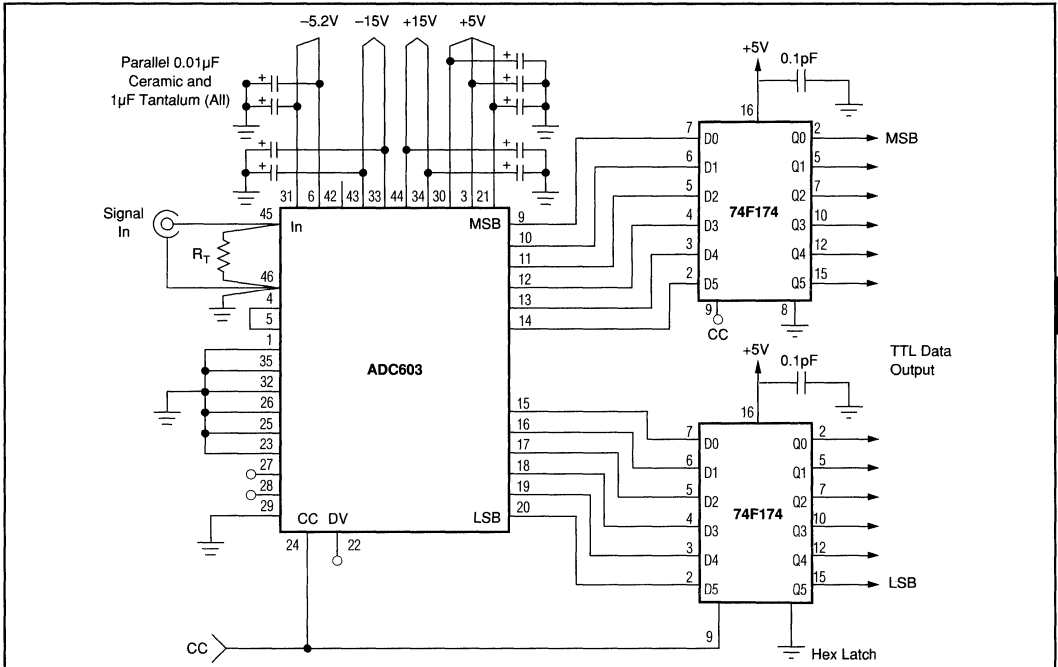FIGURE 10. Differential Input Buffer Amplifier
(Gain = –2V/V).

FIGURE 11. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane (recommended circuit).
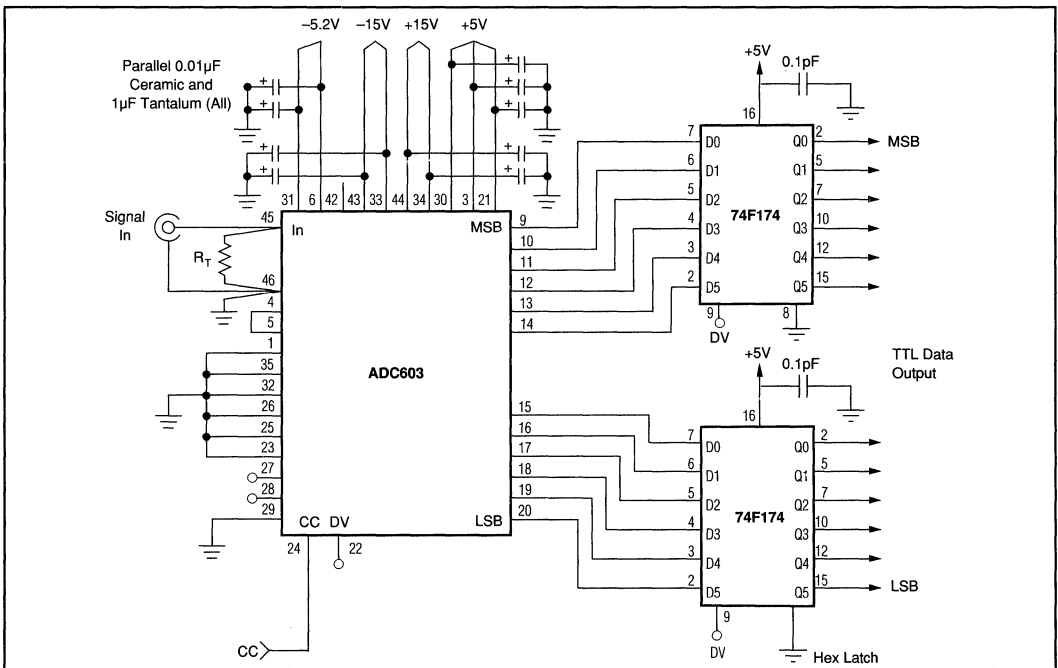

FIGURE 12. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane.

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NOTES: (1) t_{CID} = Delay time from Convert Command to Invalid Data. Typical value = 40ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical value = 93ns. Independent of conversion rate. (3) The ◻ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = Delay time from Convert Command to the internal hold. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by:

$$t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$$
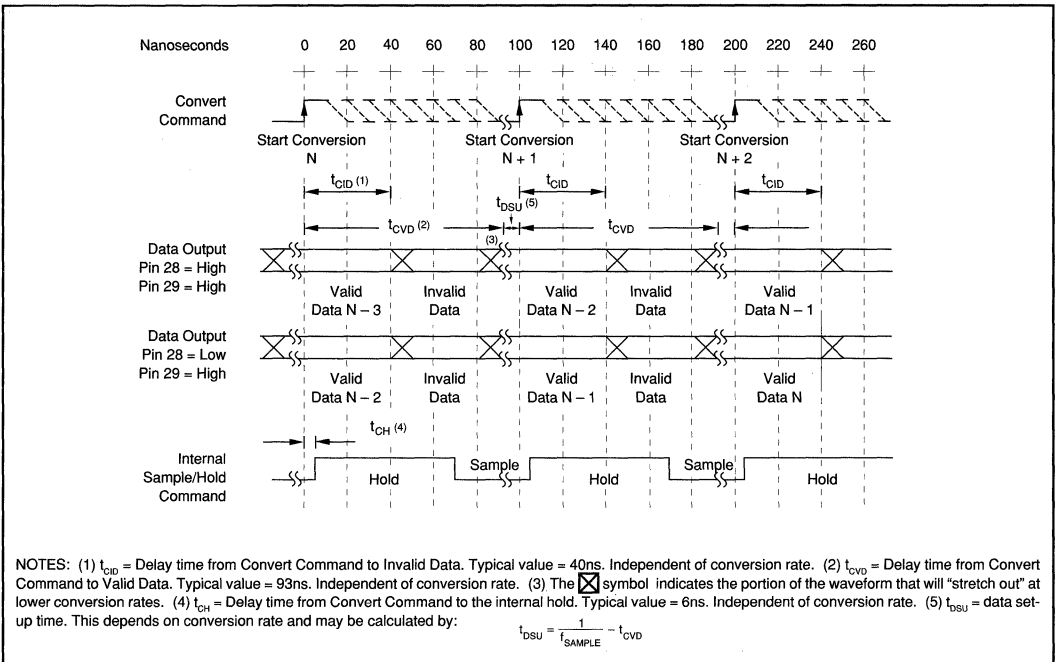
FIGURE 13. Convert Command Strobe Timing.

NOTES: (1) t_{CDL} = Delay time from Convert Command to the falling edge of Data Valid Strobe. Typical value = 85ns. Independent of conversion rate. (2) t_{CDH} = Delay time from Convert Command to the rising edge of Data Valid Strobe. Typical value = 135ns. Independent of conversion rate. (3) If Conversion "N" is the first conversion, then there is no Strobe N-1, and the Data Valid Strobe Signal will simply be high until t_{CDL} after the first Convert Command. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical value = 120ns. Independent of conversion rate. (5) t_{CH} = Delay time from Convert Command to Internal Hold Command. Typical value = 6ns. Independent of conversion rate. (6) The ◻ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates.
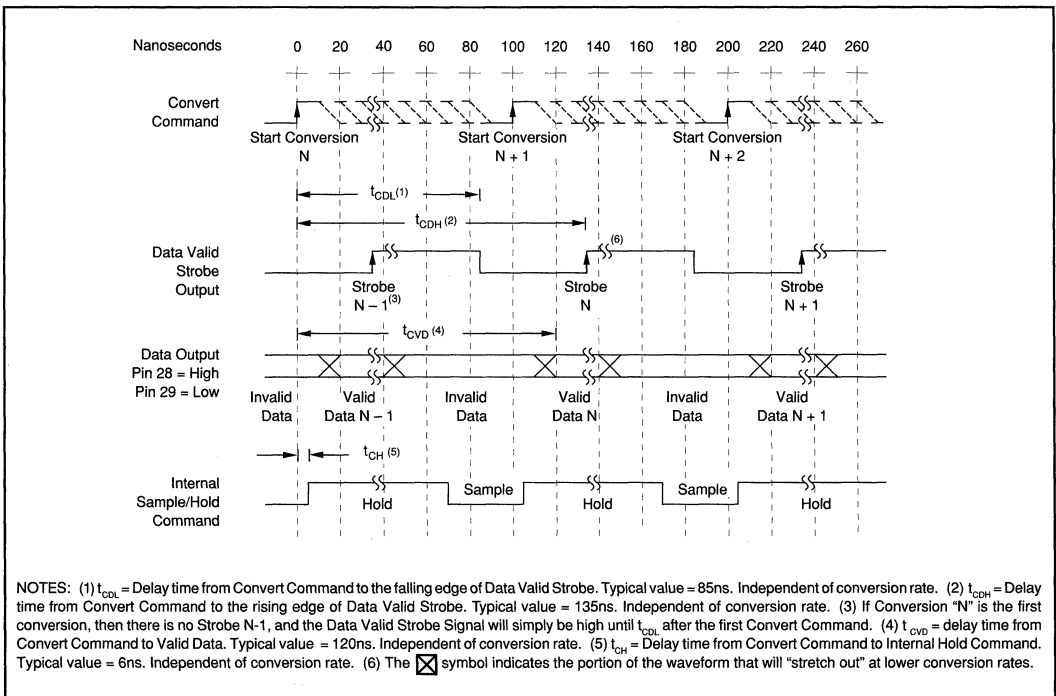
FIGURE 14. Data Valid Strobe Timing.
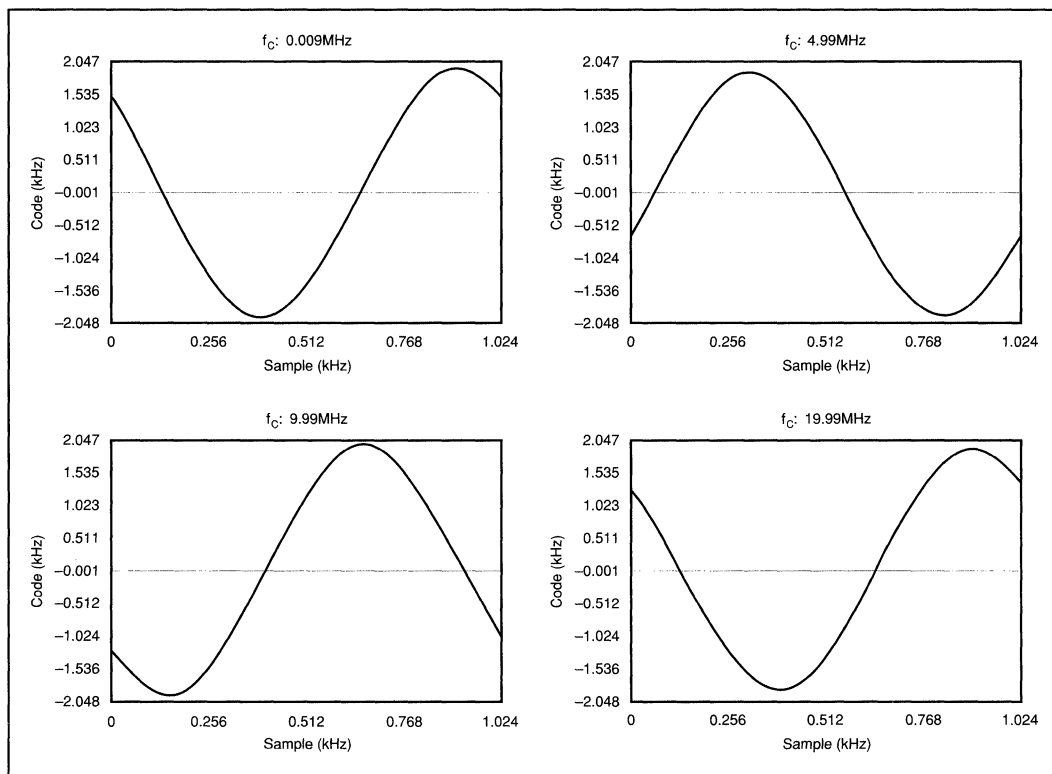
FIGURE 15. Digitized Sine Waves (f_s = 10MHz).

DIGITIZING INPUT WAVEFORMS

The response of the ADC603 is illustrated by the digitized waveforms of Figure 15. The 4.99MHz sine wave near the Nyquist limit is virtually identical to much lower frequency sine wave input. The under-sampled 19.999MHz sine wave illustrates the ADC603's excellent analog input full-power bandwidth.

HISTOGRAM TESTING

Histogram testing is used to test differential nonlinearity of the ADC603. This system's block diagram (the same for FFT testing and waveform digitizing) is shown in Figure 2 and histogram test results for a typical converter are shown in Figure 16. Note that low-frequency differential nonlinearity is 1/2LSB and it shows virtually no degradation near the Nyquist limit of 5MHz; there are no missing codes present and the peak nonlinearity does not exceed 1LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SPECTRUM ANALYZER TESTING

A beat-frequency technique (Figure 17) can be used to view digitized waveforms on an oscilloscope and, with care, this technique can also be used for testing high-speed ADC dynamic characteristics with an analog spectrum analyzer.

In this method a test signal is digitized by the ADC603 and the output digital data is latched into an external latch by the converter Data Valid output pulse driving a divide-by-N counter. The buffered ECL/TTL level translator latch drives a 12-bit video-speed DAC which reconstructs the digital signal back into an analog replica of the ADC603 input. This analog signal, including distortion products and noise resulting from digitization, can then be viewed on an ordinary analog RF spectrum analyzer.

It is important to realize that the distortion and noise measured by this technique include not only that from the ADC603, but also from the entire analog-to-analog test system. Nonlinearity of the reconstruction circuit must be very low to measure a high performance ADC, and this places severe requirements on the ADC, deglitcher, and buffer amplifiers.

Using a high-speed video DAC600 in the analog reconstruction circuit allows excellent test circuit linearity to be achieved. Clocking the DAC (demodulating) at f_c/N allows a longer DAC settling time and keeps linearity high in the digital-to-
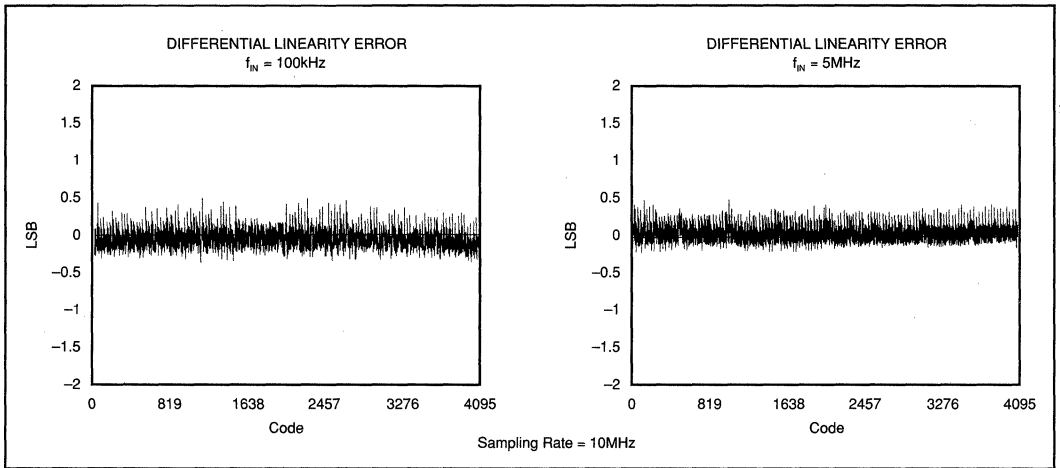
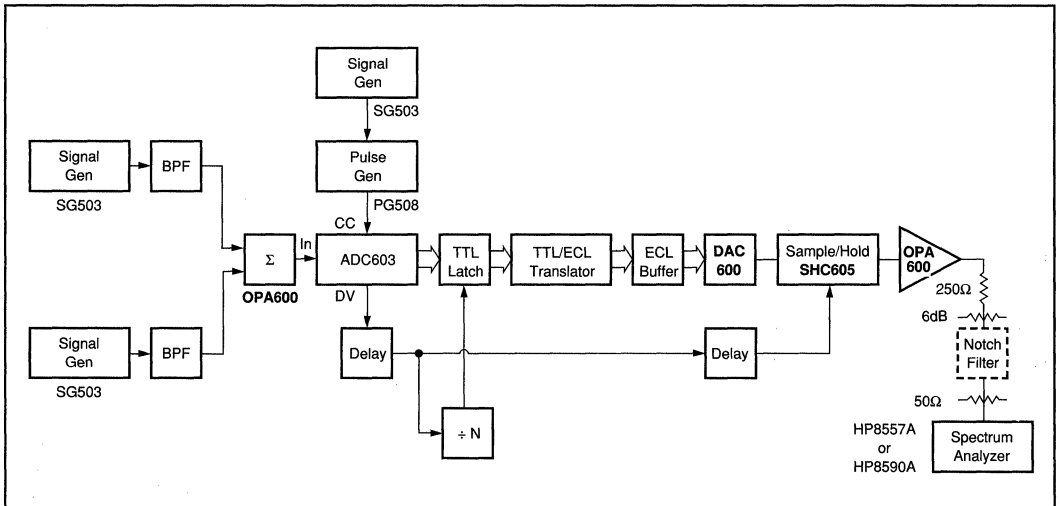FIGURE 16. 100kHz and 5MHz Differential Linearity.

FIGURE 17. Analog-to-Analog Spectral Analysis by Beat-Frequency Techniques.

analog portion of the test circuit. Spectrum analyzer dynamic range can be a limiting factor in this method. To increase dynamic range, a sharp notch filter can be used to attenuate the high-level fundamental frequency. Attenuating the high-level fundamental signal allows the analog spectrum analyzer to be used on a more sensitive range without generating distortion products within its front end.

Note that even though the signal is demodulated at a frequency of sample rate/N, the distortion products still maintain a correct frequency relationship to the fundamental. While this analog technique can give good performance, it cannot exclude some distortion products unavoidably generated within the analog reconstruction portion of the test

system. For this reason, the digital FFT technique is capable of more accurate high-speed analog/digital converter dynamic performance measurements and is the preferred method of testing high-performance A/D converters.

TIMING

The ADC603 generates all necessary timing signals internally. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below.

Convert Command Timing Option (pin 29 = HI)
With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data

from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously.

See Figure 13 for timing relationships.

Pin 28 is used to control the amount of pipeline delay. If pin 28 is held LO, then output data "N – 2" will be valid on the rising edge of Convert Command "N." If pin 28 is held HI, then output data "N – 3" will be valid on the rising edge of Convert Command "N." These timing relationships are valid at any conversion rate up to 10MHz. At rates approaching 10MHz, however, the data setup time before the rising Convert Command edge may become as short as 6ns. Therefore, the use of high-speed TTL latches such as the 74F174 hex flip-flop is recommended to capture the data. If slower latches must be used, then the setup time can effectively be improved by adding several nanoseconds of delay between the Convert Command and the latch clock signal.

Data Valid Timing Option (pin 29 = LO)

With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N." The delay is approximately 135ns, at which time the Data Valid strobe signal will rise. This signal may be connected directly to the clock input of the user's data latch.

See Figure 18 for timing relationships. Pin 28 must be left HI at all times when using the Data Valid timing option.

The advantages of this method are that no subsequent conversions are required in order to read the data, and the data is available as soon as possible after the start of conversion. Therefore, the Data Valid option is most useful in systems where the ADC may be operated asynchronously, or where the very first data latch output after power-up must represent a valid conversion. Note that because the delay is fixed at approximately 135ns independent of conversion rate, the Data Valid pulse will overlap into the next conversion at rates above 7.4MHz. This does not preclude proper operation at any rate up to 10MHz.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data formats are available (Table II).

The ADC603 output logic is TTL compatible. The tri-state output is controlled by ENABLE pin 25. For normal operation, pin 25 may be tied LO. A logic HI on pin 25 will switch the ouput data register to a high-impedance state (Figure 20). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. Tri-state output should be isolated from noisy digital

bus lines, since the noise can couple back through the OFF data register and create noise in the ADC.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

NOTES:

1. *FAST*™ *Applications Handbook*, 1987. Fairchild Semiconductor Corp.

2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.

3. "Impedance Matching Tweaks Advance CMOS IC Testing", Gerald C. Cox, *Electronic Design*, April, 1987.

4. "Grounding for Electromagnetic Compatibility", Jerry H. Boogar, *Design News*, 23 February, 1987.

OFFSET AND GAIN ADJUSTMENT

The ADC603 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers (Figure 23). Trim range is typically 2%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier allows a convenient point for injecting large offset voltages and making wide gain adjustments.

If offset and gain trim is not used, pins 36 and 37 should be left unconnected.

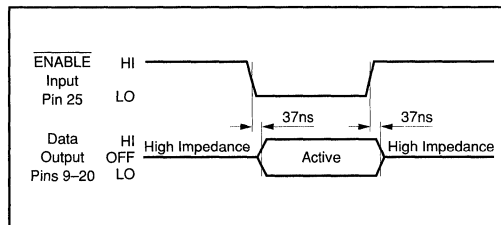|	DIGITAL DATA OUTPUT LOGIC CODING	
INPUT VOLTAGE (Exact Center of Code)	Binary Two's Complement (BTC) Pin 27 = LO	Inverted Binary Two's Complement (BTC) Pin 27 = HI
	MSB LSB	MSB LSB
+FS (+1.25V)	011111111111*	100000000000*
+FS – 1LSB (+1.2494V)	011111111111	100000000000
+FS – 2LSB (+1.2488V)	011111111110	100000000001
+3/4FS (+0.9375V)	011000000000	100111111111
+1/2FS (+0.625V)	010000000000	101111111111
+1/4FS (+0.3125V)	001000000000	110111111111
+1LSB (+610µV)	000000000001	111111111110
Bipolar Zero (0V)	000000000000	111111111111
–1LSB (–610µV)	111111111111	000000000000
–1/4FS (–0.3125V)	111000000000	000111111111
–1/2FS (+0.625V)	110000000000	001111111111
–3/4FS (–0.9375V)	101000000000	010111111111
–(FS – 1LSB) (–1.2494V)	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111
* Indicates overrange condition.		

TABLE II. Digital Data Output Logic Coding.

FIGURE 22. Digital Data Tri-State Output.

	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
PIN NUMBER	N–3	N–2	N–1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

ADC603

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

THERMAL REQUIREMENTS

The ADC603 is tested and specified over a temperature range of 0°C to +70°C (J, K grade) and –55°C to +100°C (S grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. With a small heat sink (Figure 24) the ADC603 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.[1]

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC603 package is: $\theta_{JC} =$ 4.8°C/W, measured to the underside of the case.

NOTES:

1. "Maximizing Heat Transfer from PCBs", *Machine Design*, March 26, 1987, Jeilong Chung.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device —it cannot be improved by testing. However, environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels.

Burr-Brown offers environmentally screened versions of our standard military temperature range products, designed to provide enhanced reliability at moderate cost. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and

basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

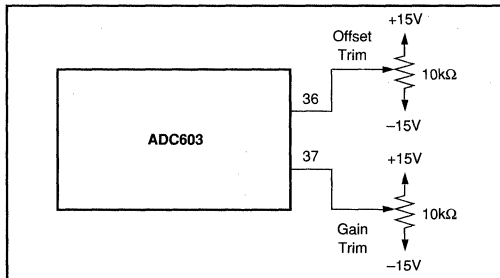| SCREEN	MIL-STD-883 METHOD, CONDITION	SCREENING LEVEL
Internal Visual	2017	Visual requirements only (par 3.1 through 3.1.8)
Electrical Test	Burr-Brown Test Procedure	
High Temperature Storage (Stabilization Bake)	1008	24hr, +100°C
Temperature Cycling	1010	10 cycles, –55°C to –125°C
Constant Acceleration	2001, A	2000G; Y Axis Only
Burn-In	1015, D	160hr, +125°C T_J, No PDA
Hermeticity, Gross Leak	1014, C	Bubble Test Only, Preconditioning Omitted
Final Electrical	Burr-Brown Test Procedure	
External Visual	2009	

TABLE III. Optional Screening Flow for ADC603SHQ.

FIGURE 21. A Multiplexed-Input Buffer Amplifier (Gain = +16V/V).

FIGURE 19. Optional Gain and Offset Trim.
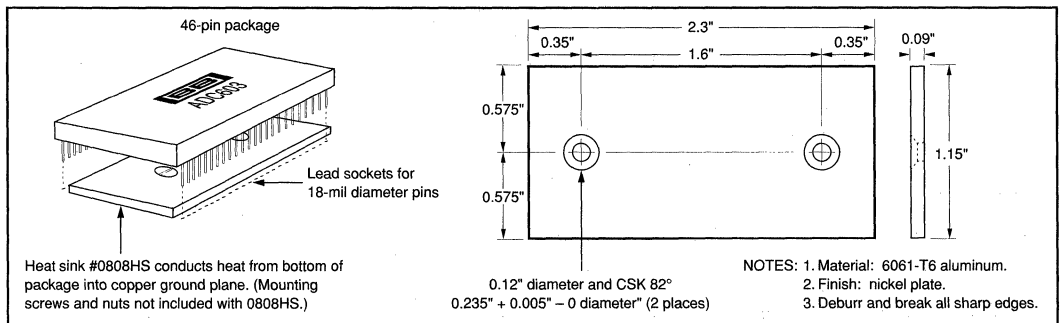
FIGURE 20. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.

BURR - BROWN®
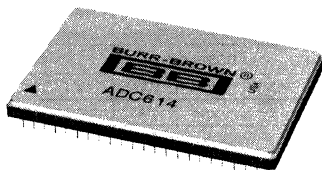
ADC614

14-Bit 5.12MHz Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **HIGH SPURIOUS-FREE DYNAMIC RANGE: –90dB (L Grade)**
● **WIDEBAND SAMPLE/HOLD: 60MHz**
● **SAMPLE RATE: DC to 5.12MHz**
● **HIGH SIGNAL/NOISE RATIO: 78dB**
● **NO MISSING CODES**
● **SINGLE 46-PIN DIP PACKAGE**
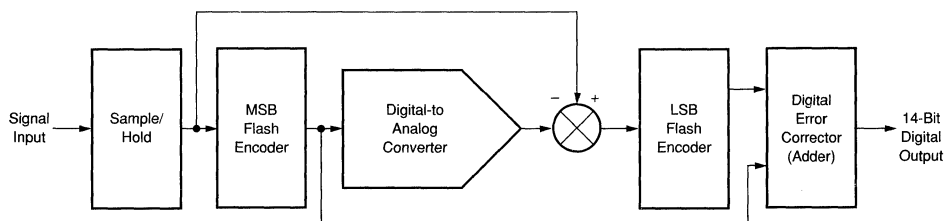● **COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference**

APPLICATIONS

● **FFT SPECTRAL ANALYSIS**
● **MEDICAL IMAGING**
● **RADAR SIGNAL ANALYSIS**
● **CCD IMAGING SYSTEMS**
● **DIGITAL RECEIVERS**
● **TRANSIENT SIGNAL RECORDING**
● **HIGH-SPEED DATA ACQUISITION**
● **SIGINT, ECM, AND EW SYSTEMS**

DESCRIPTION

The ADC614 is a high dynamic range analog-to-digital converter capable of digitizing signals at any rate from DC to 5.12 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing potential distortion sources.

The ADC614 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. The logic interface is TTL. An evaluation board (DEM-ADC614-E) is available for quick evaluation.

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 5.12MHz sampling rate, output data latched with the convert command, R_S = 50Ω, ±V_{CC} = +15V, +V_{DD1} = +5V, −V_{DD2} = −5.2V, and 15-minute warmup in convection, enviroment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC614JH MIN	ADC614JH TYP	ADC614JH MAX	ADC614KH MIN	ADC614KH TYP	ADC614KH MAX	ADC614LH MIN	ADC614LH TYP	ADC614LH MAX	UNITS
RESOLUTION				14			14			14	Bits
INPUTS											
ANALOG											
Input Range	Full Scale	−1.25		+1.25	*		*	*		*	V
Input Impedance			1.5			*			*		MΩ
Input Capacitance			5			*			*		pF
DIGITAL											
Logic Family											
Convert Command	Start Conversion										
Pulse Width	t = Conversion Period	10		t-20	*		*	*		*	ns
TRANSFER CHARACTERISTICS											
ACCURACY											
Gain Error	DC		±0.8	±2		±0.4	±1		*	*	%FSR[1]
Input Offset	DC		±0.4	±2		±0.2	±0.75		*	*	%FSR
Differential Linearity Error	f = 100kHz: 100% of all Codes		1.3	1.5		0.9	1.25		*	*	LSB
No Missing Codes			Guaranteed			Guaranteed			Guaranteed		
Power Supply Rejection	Δ+V_{CC} = ±5%		±0.03	±0.1	*	*	*		*	*	%FSR/%
	Δ−V_{CC} = ±5%		±0.04	±0.1	*	*	*		*	*	%FSR/%
	Δ+V_{DD1} = ±5%		±0.004	±0.07	*	*	*		*	*	%FSR/%
	Δ−V_{DD2} = ±5%		±0.01	±0.07	*	*	*		*	*	%FSR/%
CONVERSION CHARACTERSITICS											
Sample Rate	DC			5.12M	*		*	*		*	Samples/s
Pipeline Delay	Logic Selectable			1, 2 or 3 Convert Command Periods							
DYNAMIC CHARACTERISTICS[1][2]											
Differential Linearity Error	f = 2.3MHz: 100% of all Codes		1.3	2.0		0.8	1.25		*	*	LSB
Spurious-Free Dynamic Range (SFDR)											
f = 2.3MHz (−0.5dB)	f_s = 5.12MHz	77	82		82	88		88	90		dBFS[3]
f = 100kHz (−0.5dB)		79	82		83	88		88	90		dBFS[3]
Two-Tone Intermodulation Distortion[6]											
f = 2.2MHz (−6.5dB)	f_s = 5.12MHz		−82	−75		−88	−80		*	*	dBFS[3]
f = 2.3MHz (−6.5dB)											
Signal-to-Noise Ratio (SNR)[6]											
f = 2.3MHz (−0.5dB)	f_s = 5.12MHz	73	75		74	76		75	78		dB
f = 100kHz (−0.5dB)		75	77		75	78		76	80		dB
SINAD											
f = 2.3MHz (−0.5dB)	f_s = 5.12MHz		74			76			78		dB
f = 100kHz (−0.5dB)			76			78			80		dB
Aperature Delay Time		−20	−5	+20	*	*	*	*	*	*	ns
Aperature Jitter			3	10	*	*	*	*	*	*	ps rms
Analog Input Bandwidth (−3dB)											
Small Signal	−20dB Input	40	60		*	*		*	*		MHz
Full Power	0dB Input		30		*	*		*	*		MHz
Overload Recovery Time	2x Full-Scale Input		205	400	*	*		*	*		ns
OUTPUTS											
Logic Family				TTL Compatible							
Logic Coding	Logic Selectable			Two's Complement or Inverted Two's Complement							
Logic Levels	Logic "LO" I_{OL} = −3.2mA	0	+0.3	+0.5	*	*	*	*	*	*	V
	Logic "HI" I_{OH} = 160µA	+2.4	+3.5	+5.0	*	*	*	*	*	*	V
EOC Delay Time	Data Out to DV			See Timing Diagram: Figure 13							
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% in to 50% Out		37	100		*	*		*	*	ns
Data Valid Pulse Width				See Timing Diagram: Figure 13							
POWER SUPPLY REQUIREMENTS											
Supply Voltages: +V_{CC}	Operating	+14.25	+15	+15.75	*	*	*	*	*	*	V
−V_{CC}		−14.25	−15	−15.75	*	*	*	*	*	*	V
+V_{DD1}		+4.75	+5	+5.25	*	*	*	*	*	*	V
−V_{DD2}		−4.95	−5.2	−5.46	*	*	*	*	*	*	V
Supply Currents: +I_{CC}	Operating		+60		*	*	+80		*	*	mA
−I_{CC}			−60		*	*	−80		*	*	mA
+I_{DD1}[4]			+305		*	*	+330		*	*	mA
−I_{DD2}[5]			−550		*	*	−630		*	*	mA
Power Consumption	Operating		6.1	6.5	*	*	*		*	*	W

*Same specifications as next grade to the left.

SPECIFICATIONS (CONT)
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

±V_{CC} = +15V, +V_{DD1} = +5V, −V_{DD2} = −5.2V, R_S = 50Ω, 5.12MHz sampling rate, output data latched with the convert command, and 15-minute warmup, and T_C = T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC614JH MIN	ADC614JH TYP	ADC614JH MAX	ADC614KH MIN	ADC614KH TYP	ADC614KH MAX	ADC614LH MIN	ADC614LH TYP	ADC614LH MAX	UNITS
TEMPERATURE RANGE											
Specification	T_{CASE}	0		+85	*		*	*		*	°C
TRANSFER CHARACTERISTICS											
ACCURACY											
Gain Error	DC		±0.9	±2		±0.4	±1.5		*	*	%FSR(1)
Input Offset	DC		±0.5	±2		±0.2	±1.5		*	*	%FSR
Differential Linearity Error	f = 100kHz: 100% of all Codes		1.4	2.0		1.0	1.5		*	*	LSB
No Missing Codes			Guaranteed			Guaranteed			Guaranteed		
Power Supply Rejection	Δ+V_{CC} = ±5%		±0.04	±0.2		*	*		*	*	%FSR/%
	Δ−V_{CC} = ±5%		±0.05	±0.2		*	*		*	*	%FSR/%
	Δ+V_{DD1} = ±5%		±0.004	±0.1		*	*		*	*	%FSR/%
	Δ−V_{DD2} = ±5%		±0.02	±0.1		*	*		*	*	%FSR/%
CONVERSION CHARACTERSITICS											
Sample Rate	DC			5.12M	*		*	*		*	Samples/s
Pipeline Delay		1, 2 or 3 Convert Command Periods									
DYNAMIC CHARACTERISTICS(2)											
Differential Linearity Error	f = 2.3MHz: 100% of all Codes		1.4	2.0		1.0	1.5		*	*	LSB
Spurious-Free Dynamic Range (SFDR)											
f = 2.3MHz (−0.5dB)	f_s = 5.12MHz	75	82		80	87		85	87		dBFS(3)
f = 100kHz (−0.5dB)		77	82		80	87		85	88		dBFS(3)
Two-Tone Intermodulation Distortion(6)											
f = 2.20MHz (−6.5dB)	f_s = 5.12MHz		−82	−73		−87	−78		*	*	dBFS(3)
f = 100kHz (−6.5dB)											
Signal-to-Noise Ratio (SNR)											
f = 2.3MHz (−0.5dB)	f_s = 5.12MHz		70			74			76		dB
f = 100kHz (−0.5dB)			74			76			78		dB
SINAD											
f = 2.3MHz (−0.5dB)	f_s = 5.12MHz		70			73			*		dB
f = 100kHz (−0.5dB)			73			75			*		dB
Aperature Delay Time		−25	−6	+25	*	*	*	*	*	*	ns
Aperature Jitter			3	10		*	*		*	*	ps rms
Analog Input Bandwidth (−3dB)											
Small Signal	−20dB Input		60			*			*		MHz
Full Power	0dB Input		30			*			*		MHz
Overload Recovery Time	2x Full-Scale Input		220			*			*		ns
OUTPUTS											
Logic Levels	Logic "LO" I_{OL} = −3.2mA,	0	+0.3	+0.8	*	*	*	*	*	*	V
	Logic "HI" I_{OH} = 160µA,	+2.4	+3.5	+5.0	*	*	*	*	*	*	V
EOC Delay Time	Data Out to DV	See Figure 13; Δ Timing Typically Within ±20% Over Temperature									
Tri-State Enable/Disable Time 50% in to 50% Out	I_{OL} = −6.4mA,		42	100		*	*		*	*	ns
Data Valid Pulse Width		See Figure 13; Δ Timing Typically Within ±20% Over Temperature									
POWER SUPPLY REQUIREMENTS											
Supply Currents: +I_{CC}	Operating		+65	+80		*	*		*	*	mA
−I_{CC}			−61	−80		*	*		*	*	mA
+I_{DD1}(4)			+305	+333		*	*		*	*	mA
−I_{DD2}(5)			−550	−630		*	*		*	*	mA
Power Consumption	Operating		6.1	6.5		*	*		*	*	W

*Same specifications as next grade to the left.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with lower distortion are available on special order; inquire. (3) dBFS = level referred to full scale. The input signal is within 1 dB of full scale; f = input frequency; f_s = sampling frequency. (4) Pins 3 and 30 (analog typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (5) Pin 6 (analog) typically draws 45% of the total −5.2V current. Pin 31 (digital) typically draws 55%. (6) SNR and two-tone intermodulation distortion are guaranteed but not 100% tested.

(Right margin vertical text) ADC614 · A/D CONVERTERS, DATA ACQUISITION COMPONENTS · 2

PIN ASSIGNMENTS

1	Common (Analog)	46	Common (Analog)
2	DNC	45	Analog Signal In
3	+V_{DD1} (+5V) Analog	44	+V_{CC} (+15V) Analog
4	S/H Out	43	–V_{CC} (–15V) Analog
5	A/D In	42	NC
6	–V_{DD2} (–5.2V) Analog	41	NC
7	Bit 13	40	NC
8	Bit 14 (LSB)	39	DNC
9	Bit 1 (MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	+V_{CC} (+15V) Analog
14	Bit 6	33	–V_{CC} (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	–V_{DD2} (–5.2V) Digital
17	Bit 9	30	+V_{DD1} (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12	27	Output Logic Invert
21	+V_{DD1} (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	3-State ENABLE
23	Common (Digital-Case)	24	Convert Command In

NOTE: NC = no connection, DNC = do not connect.

ORDERING INFORMATION

```
                                          ADC614 ( ) H Q
Basic Model Number ─────────────────────────┘ │   │ │
Performance Grade Code ───────────────────────┘   │ │
    J, K, L: 0°C to +85°C Case Temperature         │ │
Package Code ──────────────────────────────────────┘ │
    H: Metal and Ceramic                              │
Enviromental Screening Option ────────────────────────┘
```

ABSOLUTE MAXIMUM RATINGS

±V_{CC}	±16.5V
+V_{DD1}	+7.0V
±V_{DD2}	–7.0V
Analog Input	±5.0V
Logic Input	–0.5V to +V_{DD1}
Case Temperature (Operating)	+85°C
Junction Temperature	+100°C
Storage Temperature	–65°C to +125°C

Stresses above these ratings may permanently damage the device.

PACKAGING INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC614JH	Metal and Ceramic	234
ADC614KH	Metal and Ceramic	234
ADC614LH	Metal and Ceramic	234

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 5.12MHz sampling rate, 15-minute warmup, and $T_C = +25°C$, unless otherwise noted.
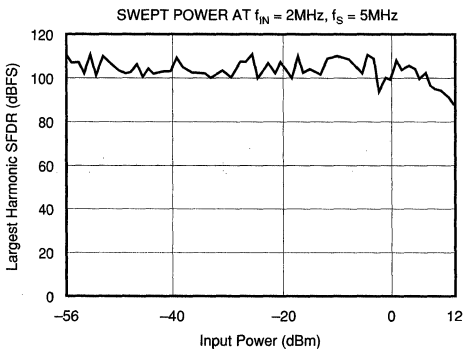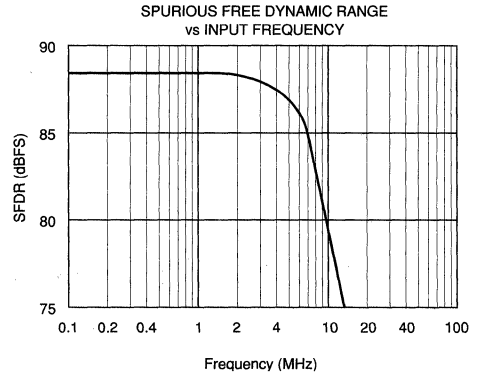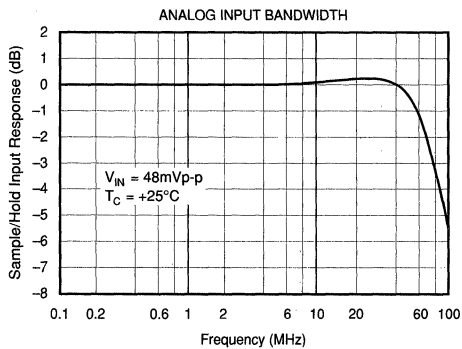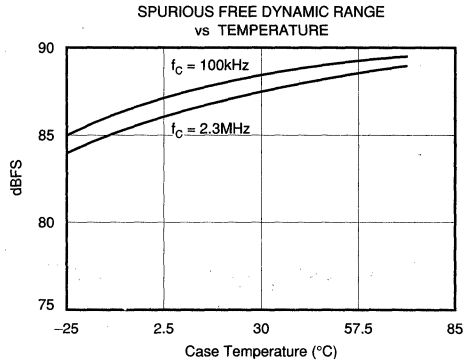
ADC614

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

2.3MHz SPECTRAL PERFORMANCE

$f_{IN} = 2.3MHz$

100kHz SPECTRAL PERFORMANCE

$f_{IN} = 100kHz$

UNDERSAMPLING AT 5.0MHz

$f_{IN} = 5.00MHz$

TWO TONE INTERMODULATION DISTORTION

100kHz DIFFERENTIAL LINEARITY ERROR

$f_S = 5.12MHz$
$f_{IN} = 100kHz$

2.3MHz DIFFERENTIAL LINEARITY ERROR

$f_S = 5.12MHz$
$f_{IN} = 2.3MHz$

TYPICAL PERFORMANCE CURVES (CONT)

$\pm V_{CC} = \pm 15V$, $+V_{DD1} = +5V$, $-V_{DD2} = -5.2V$, $R_S = 50\Omega$, 5.12MHz sampling rate, 15-minute warmup, and $T_C = +25°C$, unless otherwise noted.

SIGNAL-TO-NOISE RATIO
vs TEMPERATURE

SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE

ANALOG INPUT BANDWIDTH

SPURIOUS FREE DYNAMIC RANGE
vs INPUT FREQUENCY

SWEPT POWER AT f_{IN} = 2MHz, f_S = 5MHz

THEORY OF OPERATION

The ADC614 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC614 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 65ns. The low-bias-current output buffer is then required to settle to only the resolution (8 bits) of the first (MSB) flash encoder in 65ns, while an additional 85ns is allowed for settling to the resolution (14 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) functions are performed by one 8-bit flash encoder. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 8-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.
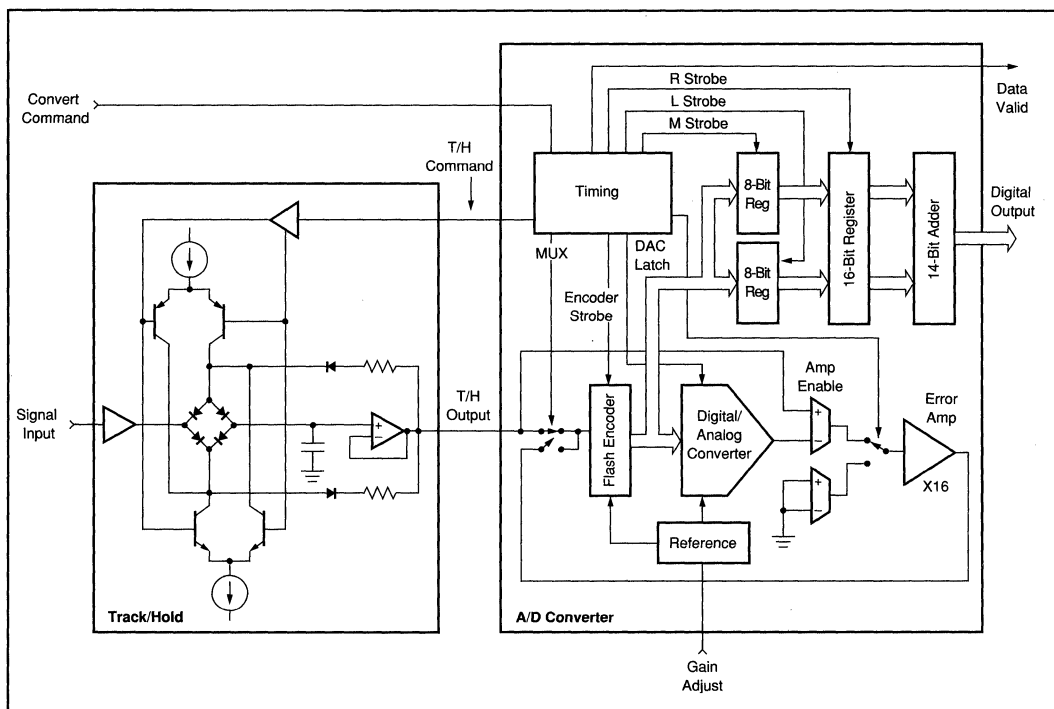

FIGURE 1. ADC614 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC614. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC614 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 135ns ADC conversion time. ADC614 conversion rates are therefore possible somewhat above the 5.12MHz specification but S/H acquisition time is sacrificed and accuracy is rapidly degraded.

The output of the MSB and LSB encoders are read into separate 8-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 16-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 8-bit words from the two flash encoders into a 14-bit output word.

The 16-bit register output is then sent to a 14-bit adder where the final data output word is created. The MSB data forms the most significant eight bits of a 14-bit word, with the last six bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first six bits being assigned zeros. As two 14-bit words are being added, the output of the adder could exceed 14 bits in range; however, the final data output is only a 14-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC614 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: spurious free dynamic range (SFDR), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2 and 3. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC614 (14 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (i.e., a 10-sample average of 512-point FFTs).

DYNAMIC PERFORMANCE DEFINITIONS

1. Spurious Free Dynamic Range:

$$\frac{\text{Largest Harmonic Power (first 9 harmonics)}}{\text{Full Scale Power}}$$

2. Intermodulation Distortion (IMD):

$$\frac{\text{Highest IMD Product Power (to 5th order)}}{\text{Sinewave Signal Power}}$$

3. Signal-to-Noise Ratio (SNR):

$$\frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

4. Signal-to-(Noise + Distortion)[2] Ratio (SINAD):

$$\frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The DC frequency bin is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
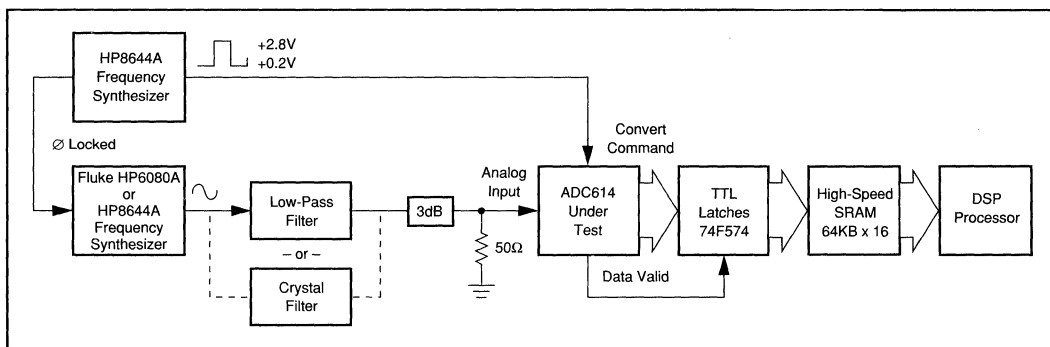
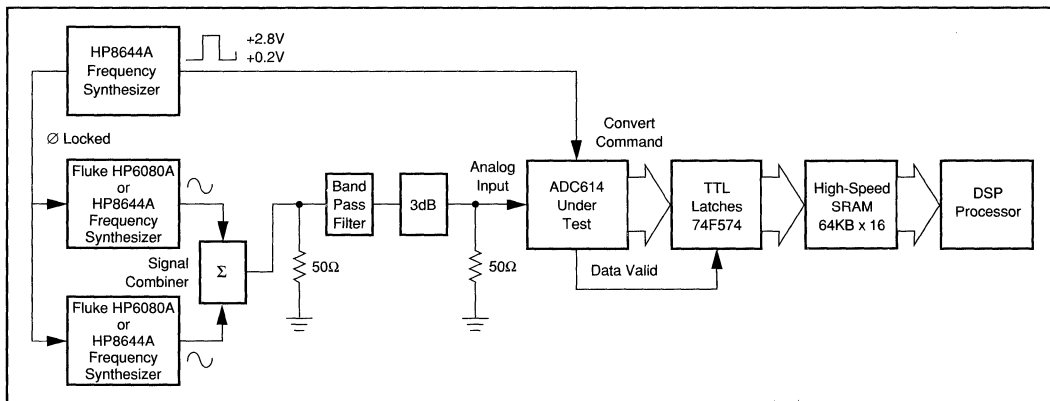FIGURE 2. Block Diagram of FFT Test for SNR, SFDR and Swept-Power Test.

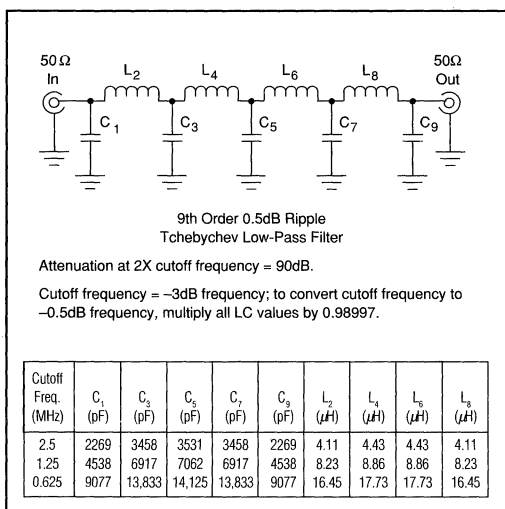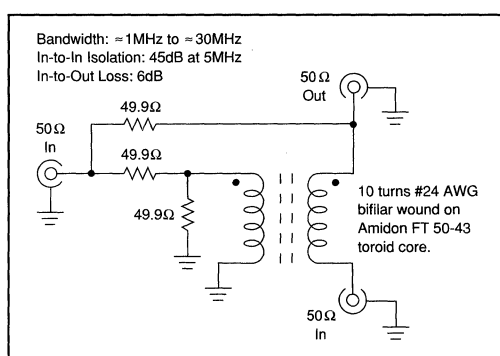FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.

9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2X cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to
–0.5dB frequency, multiply all LC values by 0.98997.

Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (μH)	L_4 (μH)	L_6 (μH)	L_8 (μH)
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

FIGURE 5. Passive Signal Combiner.

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2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6B to prevent "hard limiting" on peaks.

3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator. Care must be taken not to saturate the filter. Saturation of these filters may cause odd order harmonics.

4. Test signal generators must have exceptional noise performance to achieve accurate SNR measurements. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR tests. Recommended generators are the Fluke 6080A or HP8644A. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.

5. The analog input of the ADC614 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA642. Short leads are necessary to prevent digital noise pickup.

6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. A HP 8644A generator is a good clock source. Short leads are necessary to preserve fast TTL rise times.

7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. A passive (hybrid transformer) signal combiner can also be used (Figure 5) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBC.

8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.[1]

9. Floating inputs can eliminate ground-loop noise. A simple common-mode choke shown in Figure 6 and 7, or a single-ended amplifier (Figure 8 and 9) can be used for gain. Optimized harmonic performance can only be achieved with a very low distortion buffer. Burr-Brown OPA642 is an ideal op amp for driving the ADC614.

10. Digital data must be latched into an external TTL 14-bit register, preferably using the convert command pulse (Figures 10 and 11). Latches should be mounted on PC boards in very close proximity to the ADC614. Avoid long leads.

11. Do not overload the data output logic. These outputs are designed to drive 2 TTL loads. Do not connect ADC614 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.

12. A well-designed, clean PC board layout will assure proper operation and clean spectral response.[4, 5] Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (20oz-foil) ground planes can give excellent results, if carefully designed.

13. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.

14. Connect analog and digital ground pins of the ADC614 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering[6] is optional and may improve noise rejection. The manual for the evaluation board (DEM-ADC614-E) gives a recommended layout.

15. If using a cable to drive the input of the ADC614, avoid reflections down the cable that could degrade dynamic performance by placing a 3dB attenuator at the end of the cable. Input amplitude should be doubled to maintain signal amplitude.

NOTES:
1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.

2. SINAD test includes harmonics whereas SNR does not include these important spurious products.

3. If IMD is referenced to peak envelope power, distortion will be 6dB better.

4. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.

5. Motorola MECL, Motorola Corp.

6. Murata-Erie BNX002-01.

TIMING

The ADC614 generates all necessary timing signals internally. Only timing between Convert Command, Output Data, and Data Valid must be considered. Proper timing is shown in Figures 12 and 13. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below:

(I) Convert Command timing option (pin 29 = HIGH)— With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously. See Figure 12 for timing relationships.

Pin 28 is used to control the amount of pipeling delay. If pin 28 is held LOW, then output data "N-2" will be valid on the rising edge of Convert Command "N". If pin 28 is held

HIGH, then output data "N-3" will be valid on the rising edge of Convert Command "N". These timing relationships are valid at any conversion rate up to 5.12MHz, the data setup time before the rising Convert Command edge is about 50ns.

(2) Data Valid timing option (pin 29 = LOW)—With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N". The delay is about 165ns . At about t = 185ns, the Data Valid strobe signal will rise. This strobe signal may be connected directly to the clock input of the external data latches, providing a data setup time of approximately 20ns.

See Figure 13 for timing relationships. Pin 28 must be left HIGH at all times when using the Data Valid timing option.

This method does not require subsequent conversions in order to read the data (ie, single-shot conversion capability). Therefore, the Data Valid option is useful in systems where the very first data latch output after power-up must represent a valid conversion.

PIN NUMBER	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
	N-2	N-1	N-1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

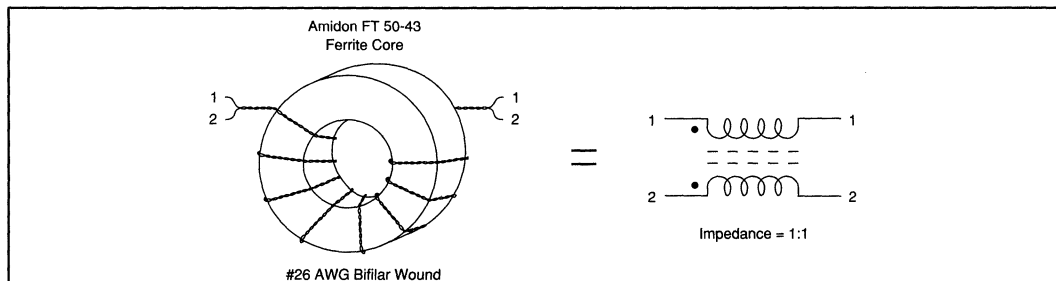| INPUT VOLTAGE (EXACT CENTER OF CODE)	DIGITAL DATA OUTPUT LOGIC CODING	
	BINARY TWO'S COMPLEMENT (BTC) PIN 27 = LO	INVERTED BINARY TWO'S COMPLEMENT ($\overline{BTC}$) PIN 27 = HI
+FS (+1.25V)	01111111111111(1)	10000000000000(1)
+FS −1LSB (+1.24985V)	01111111111111	10000000000000
+FS −2LSB (+1.24969V)	01111111111110	10000000000001
+3/4 FS (+0.9375V)	01100000000000	10011111111111
+1/2 FS (+0.6250V)	01000000000000	10111111111111
+1/4 FS (+0.3125V)	00100000000000	11011111111111
+1 LSB (+152µV)	00000000000001	11111111111110
Bipolar Zero (0V)	00000000000000	11111111111111
−1 LSB (−152µV)	11111111111111	00000000000000
−1/4 FS (−0.3125V)	11100000000000	00011111111111
−1/2 FS (−0.625V)	11000000000000	00111111111111
−3/4 FS (−0.9375V)	10100000000000	01011111111111
−FS + 1LSB (−1.24985V)	10000000000001	01111111111110
−FS (−1.25V)	10000000000000	01111111111111
	MSB LSB	MSB LSB
NOTE: (1) Indicates overrange condition.		

TABLE II. Coding Table for 14-bit±1.25V ADC Function.

Data should be latched into external TTL latches that can operate reliably with a set-up time of 6ns minimum. Two 74F574 hex latches are recommended.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data format is available (Table II).

The ADC614 output logic is TTL compatible. The 3-state output is controlled by ENABLE pin 25. For normal operation pin 25 will be tied LO. A logic HI on pin 25 will switch the output data register to a high-impedance state (Figure 14). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. The 3-state output should be isolated from noisy digital bus lines as the noise can couple back through the OFF data register and create noise in the ADC.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

OFFSET AND GAIN ADJUSTMENT

The ADC614 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed with external potentiometers (Figure 15). Trim range is typically
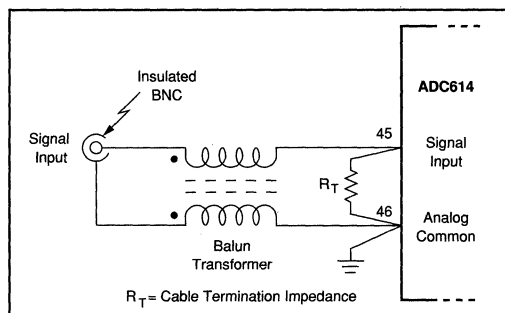

FIGURE 6. Floating-Input Balun Transformer.

FIGURE 7. Common-Mode Choke Transformer Windings.

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only 0.1%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier is the preferred way for injecting offset voltages and making wide gain adjustments.

THERMAL REQUIREMENTS

The ADC614 is tested and specified over a temperature range of 0°C to +85°C. The converters are tested in a forced-air environment with a 10 SCFM air flow. The ADC614 can be operated in a normal convection ambient air environment, provided the case temperature does not exceed the upper limit of its specification.

Proper heat transfer can be assured by placing a small heat sink (#0808HS) and an appropriately sized piece of 10mil. Berquist Sil-Pad 400 between the unit and PC board ground plane. Refer to Figure 16 for details.

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC614 package is: $\theta_{JC} = 4.8°C/W$. measured to the underside of the case.

NOISE FIGURE

The noise figure is defined as the degradation of signal-to-noise ratio as an analog input is processed through the ADC614. An approximation of the noise figure of the ADC614 can be derived from the SNR specifications.

The signal-to-noise ratio of the ADC614 is measured typically at 78dB. The full-scale input signal of the ADC614 is +12dBm, so the noise level at the output of the ADC614 is –66dBm for the 2.56MHz band. The input noise is derived from the formula:

$$N = 10\log (4kTB/0.001) = -168dBm$$

The noise figure can be calculated using the following equation:

$$NF = \text{output noise} - (10\log BWo/BWi) - \text{input noise}$$

$$NF = -66dB - 64dB - (-168dB) = 38dB$$

An important consideration when using the Noise Figure for an analog-to-digital converter is the effect of input signal range on the noise figure. As the input range increases, the noise figure directly decreases. The best indicator of the noise performance of the ADC614 is SNR, which is –78dB

typical for the LH grade. When the input is grounded, the RMS noise of the ADC614 is 72µV, and 99.7% of all codes will fall within a span of four codes. This figure represents the entire noise contribution of the ADC614.

CUSTOM SCREENING OPTIONS

Custom screened versions of the ADC614 are available. Screening may include extended temperature ranges, higher guaranteed dynamic specifications, additional enviromental screens, higher sampling rates, etc. Inquire with your local sales representative or contact factory.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of enviromental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-screening" provides enviromental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in Table III is performed to selected levels similar to those of MIL-STD-883. The "Q" version of the ADC614KH and LH guarantee data sheet specifications over –25°C to +85°C.

| SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24hrs
Temperature Cycling	Temperature = –55°C to +125°C 10 cycles
Burn-in Test	85°C, 160 Hours Minimum (Parallel Exitation)
Hermetic Seal	Fine: He leak rate < 1x10⁻⁷atm cc/S Gross: Perfluorocarbon Bubble Test
Electrical Tests	Static at 25°C, per Table I Dynamic at 0°C, +25°C, +85°C, per Table I
External Visual	Burr-Brown QC5150

TABLE III. ADC614 Q-Screening Methods.
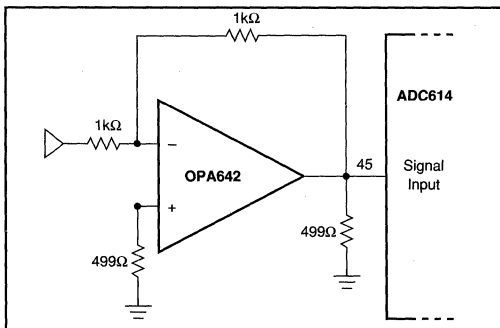
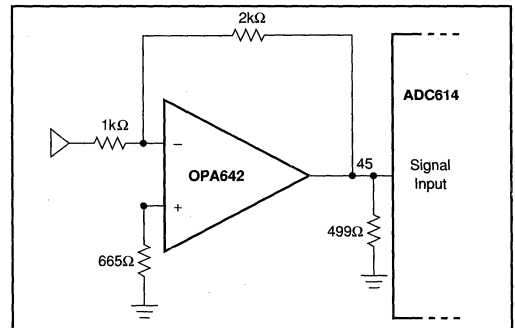FIGURE 8. Single Ended Input Amplifier (Gain = –1V/V).

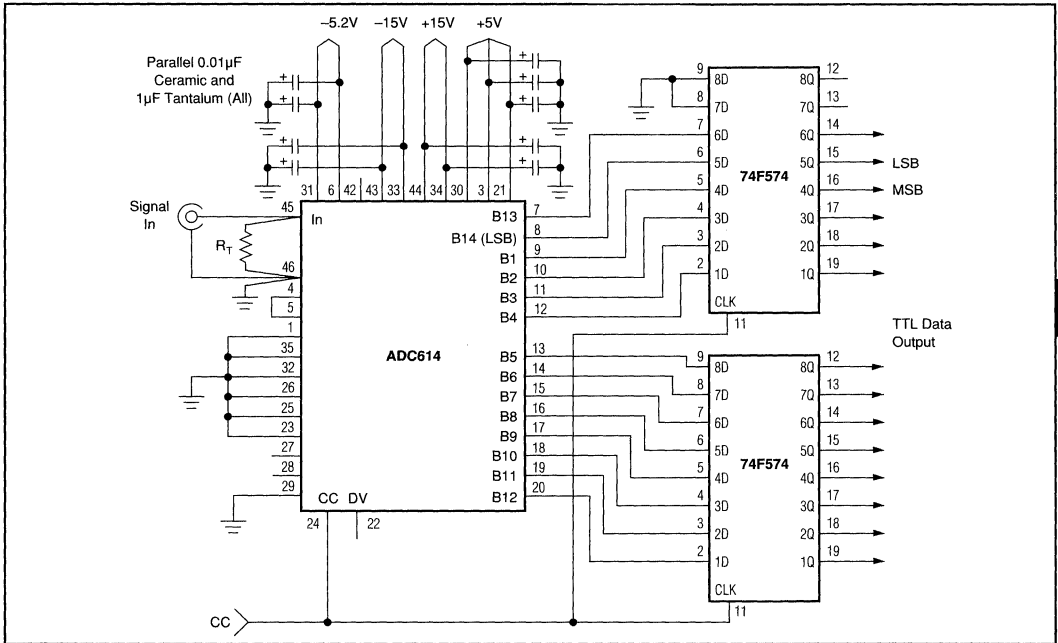FIGURE 9. Single Ended Input Low Noise Amplifier (Gain = –2V/V).

FIGURE 10. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane. Optimum noise performance is achieved when strobing the output data with the convert command.
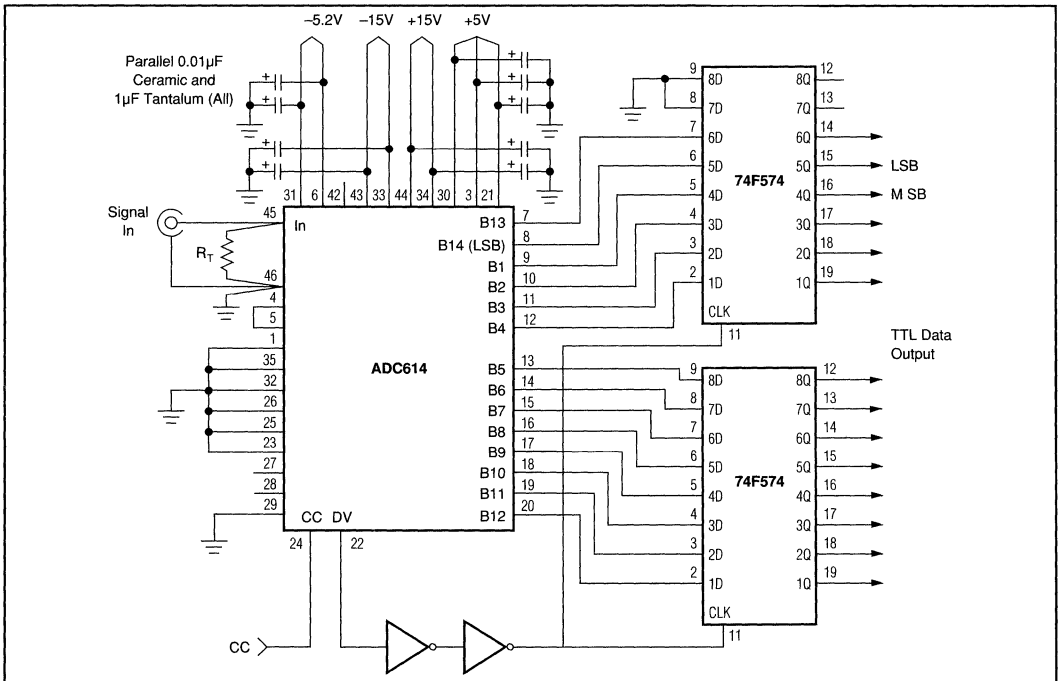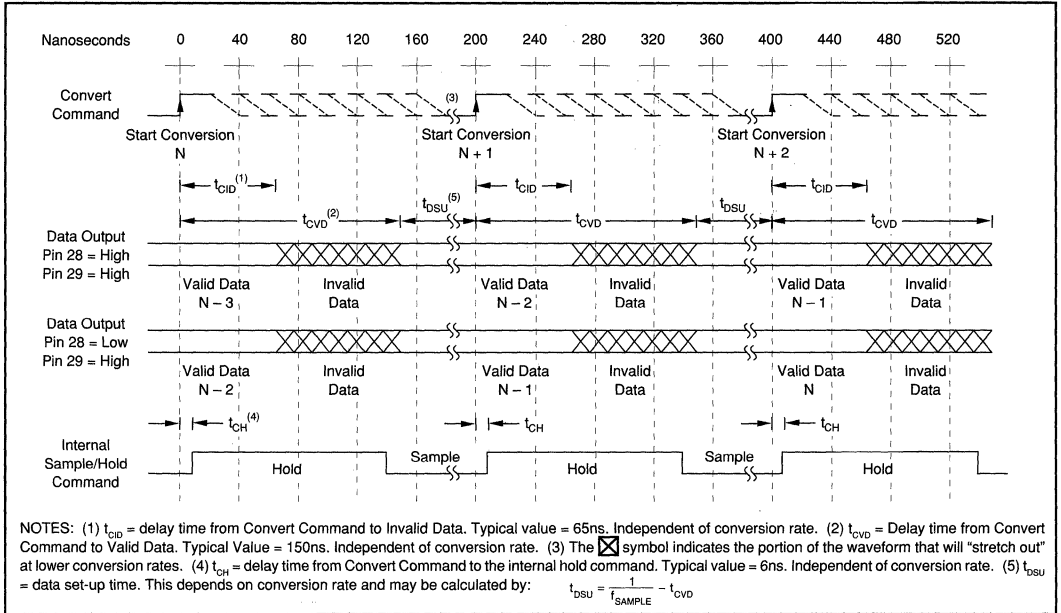

FIGURE 11. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins, using common ground plane.

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NOTES: (1) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical Value = 150ns. Independent of conversion rate. (3) The ⊠ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by: $t_{DSU} = \dfrac{1}{f_{SAMPLE}} - t_{CVD}$

FIGURE 12. Convert Command Strobe Timing for a 5MHz Conversion Rate.

NOTES: (1) t_{CDL} = delay time from Convert Command to the falling edge of Data Valid strobe. Typical value = 140ns. Independent of conversion rate. (2) t_{CDH} = delay time from Convert Command to the rising edge of Data Valid strobe. Typical value = 195ns. Independent of conversion rate. (3) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical Value = 188ns. Independent of conversion rate. (5) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (6) The ⊠ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (7) t_{DSU} = data setup time. Typical value = 7ns. Independent of conversion rate.

FIGURE 13. Data Valid Strobe Timing for a 5MHz Conversion Rate.
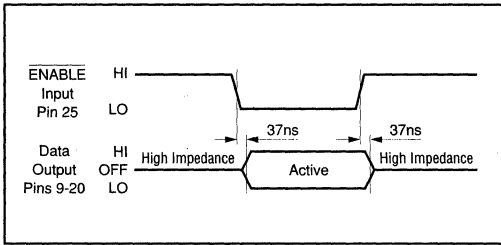
FIGURE 14. Digital Data 3-State Output.
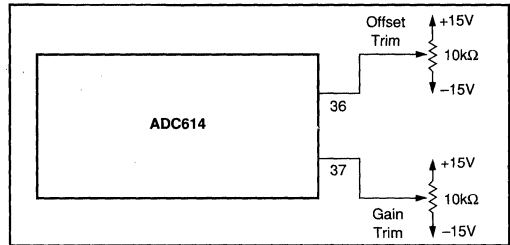
FIGURE 15. Optional Gain and Offset Trim.

2
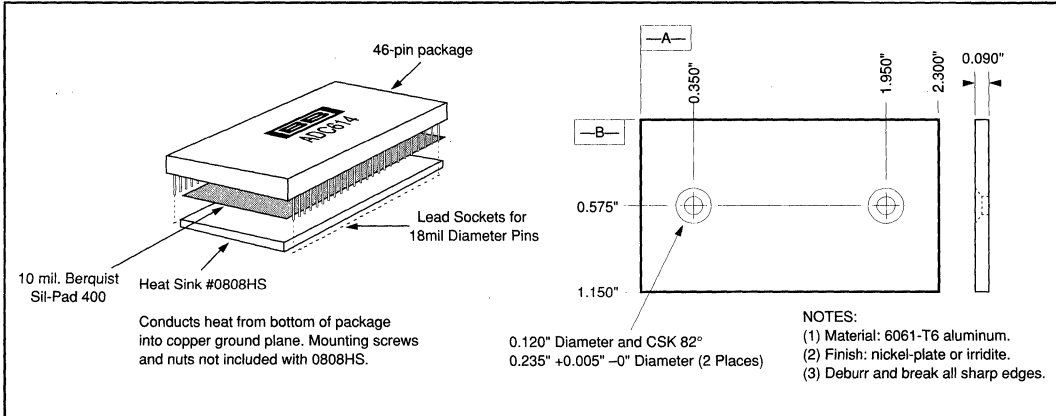
ADC614

FIGURE 16. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

ADC674A

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-551.

Microprocessor-Compatible
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**

● **IMPROVED PERFORMANCE SECOND SOURCE FOR ADC574A/674A-TYPE A/D CONVERTERS**
Conversion Time: 15µs max
Bus Access Time:150ns max
A_0 Input: Bus Contention During Read Operation Eliminated

● **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**

● **NO MISSING CODES OVER TEMPERATURE:**
0°C to +75°C ADC674AJH, KH, JP, KP Grades
−55°C to +125°C (ADC674ASH, TH Grades)

DESCRIPTION

The ADC674A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC674A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.

PDS-551D

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = ±12V or +15V, V_{EE} = −12V or −15VDC, V_{LOGIC} = +5V, unless otherwise noted.

PARAMETER	ADC674AJP,JH,SH MIN	TYP	MAX	ADC674AKP,KH,TH MIN	TYP	MAX	UNITS
RESOULUTION			12			*	Bits
ANALOG INPUTS							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	*	*	*	kΩ
±10V, 0V to +20V	9.4	10	10.6	*	*	*	kΩ
DIGITAL INPUTS (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		±5.5	*		*	V
Logic 0	−0.5		±0.8	*		*	V
Current	−5	0.2	±5	*	*	*	μA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C			±1			±1/2	LSB
Linearity Error			±2			*	LSB
Unipolar Offset Error (adjustable to zero)			±10			±4	LSB
Bipolar Offset Error (adjustable to zero)							
Full-Scale Calibration Error[1] (adjustable to zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (differential linearity)	11	±1/2		12			Bits
Inherent Quantization Error					*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (differential linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SENSITIVITY							
Change in Full-Sclae Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
+16.5V < V_{EE} < +13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			*	LSB
CONVERSION TIME[4]							
8-Bit Cycle	6	8	10	*	*	*	μs
12-Bit Cycle	9	12	15	*	*	*	μs
DIGITAL OUTPUT (DB_{11} — DB_0, Status)							
(Over Temperature Range)							
Outputs Codes:Unipolar		Unipolar Straight Binary (USB)					
Bipolar		Bipolar Offset Binary (BOB)					
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500μA)	+2.4			*			V
Leakage, Data Bits Only , High-Z State	−5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	±10	±10.1	*	*	*	V
Source Current Available for External Loads[5]	2			*			mA

ADC674A

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = ±12V or +15V, V_{EE} = −12V or −15VDC, V_{LOGIC} = +5V, unless otherwise noted.

PARAMETER	ADC674AJP, AJH, ASH			ADC674AKP, AKH, ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC} +11.4		+16.5	*		*	V	
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specification: K, J Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

* Specifications same as ADC674AJP, AJH, ASH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see Optional External Full Scale and Offset Adjustments section). (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20 V; for a 0 to +10V range, FS means 10V. The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendor's 674A type specification tables. (3) Using internal reference. (4) See Controlling the ADC674A section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to −16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)	
to Digital Common	−0.5V to V_{LOGIC} +0.5V
Analog Inputs REF IN, BIP. OFF., 10V_{IN})	
to Analog Common	±16.5V
20V_{IN} to Analog Common	±24V
REF OUT	Indefinite Short to Common,
	Momentary Short to V_{CC}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Ceramic	50°C/W
Plastic	100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC674As. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g., ADC674AKP-BI).

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR, max (T_{MIN} to T_{MAX})
ADC674AJP	Plastic DIP	0°C to +75°C	±1LSB
ADC674AKP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC674AJH	Ceramic DIP	0°C to +75°C	±1LSB
ADC674AKH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC674ASH	Ceramic DIP	−55°C to +125°C	±1LSB
ADC674ATH	Ceramic DIP	−55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMPERATURE (160 Hours)[1]
ADC674AJP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC674AKP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC674AJH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC674AKH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC674ASH-BI	Ceramic DIP	−55°C to +125°C	+125°C
ADC674ATH-BI	Ceramic DIP	−55°C to +125°C	+125°C

NOTE: (1) Or equivalent combination of time and temperature.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC674AJP	Plastic DIP	215
ADC674AKP	Plastic DIP	215
ADC674AJH	Ceramic DIP	149
ADC674AKH	Ceramic DIP	149
ADC674ASH	Ceramic DIP	149
ADC674ATH	Ceramic DIP	149
ADC674AJP-BI	Plastic DIP	215
ADC674AKP-BI	Plastic DIP	215
ADC674AJH-BI	Ceramic DIP	149
ADC674AKH-BI	Ceramic DIP	149
ADC674ASH-BI	Ceramic DIP	149
ADC674ATH-BI	Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION
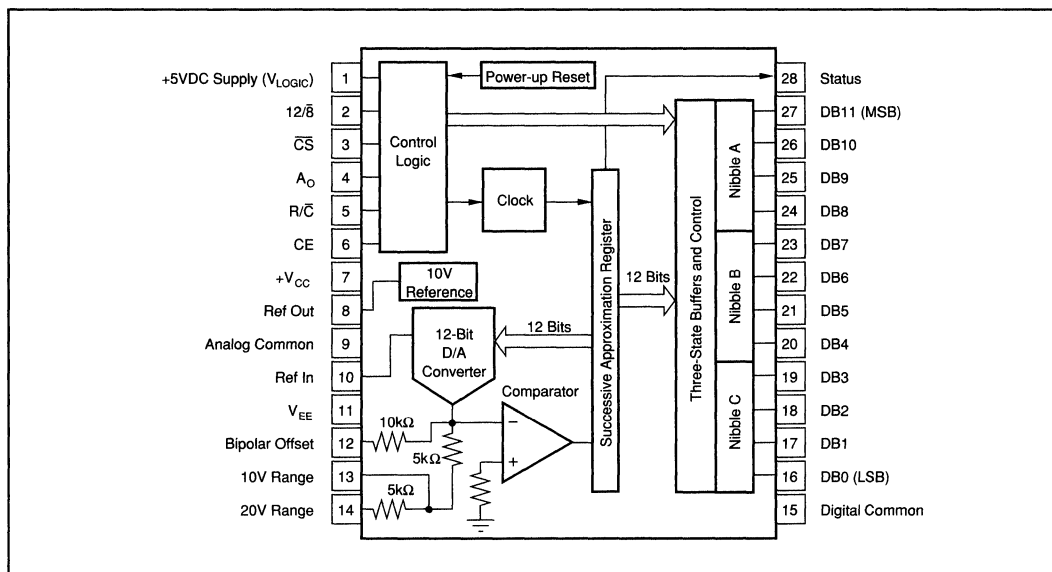
CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 112-bit conversion cycle, initiating the conversion, and the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A$_0$, R/$\overline{C}$, and CE) are all TTL-/CMOS-compatible. The functions of the control inputs are described in Table I. The control function truth table is listed in Table II.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A$_0$	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. Control Input Truth Table.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") ot either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A$_0$ (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A$_0$ selects 8-bit (A$_0$ = "1") or 12-bit (A$_0$ = "0") conversion mode. When reading output data in two 8-bit bytes, A$_0$ = "0" accesses ±8MSBs (high byte) and A$_0$ = "1" accesses 4LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12-bits) ("0" = 8-bits)	When reading output data. 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A$_0$ line.

TABLE I. ADC674A Control Line Functions.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/C̄. In this mode C̄S̄ and A_O are connected to digital common and CE and 12/8̄ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/C̄. The three-state data output buffers are enabled when R/C̄ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case, the R/C̄ pulse must remain low for a minimum of 50ns.

Figure 1 illustrates timing when conversion is initiated by an R/C̄ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/C̄ and are enabled for external access of the data after completion of the conversion. Figure 2 illustrates the timing when conversion is initiated by a positive R/C̄ pulse. In this mode, the output data from the previous conversion is enabled during the positive portion of R/C̄. A new conversion is started on the falling edge of R/C̄, and the three-state outputs return to the high impedance state until the next occurrence of a high R/C̄ pulse. Timing specifications for stand-alone operation are listed in Table III.

FIGURE 1. R/C̄ Pulse Low — Outputs Enabled After Conversions.

FIGURE 2. R/C̄ Pulse High — Outputs Enabled Only While R/C̄ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C̄ Pulse Width	50			ns
t_{DS}	STS Delay from R/C̄			200	ns
t_{HDR}	Data Valid After R/C̄ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/C̄ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE III. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_O input, which is latched upon receipt of a conversion start transition (described below). If A_O is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_O is low. If all 12 bits are read following an 8-bit conversion the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1). A_O is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, C̄S̄, and R/C̄) as shown in Table II. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 3. The specifications for timing are contained in Table IV.

FIGURE 3. Conversion Cycle Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_O To CE Setup	0			ns
t_{HAC}	A_O Valid During CE high	50	20		ns
t_C	Conversion Time, 12 Bit Cycle	9	12	15	μs
	8 Bit Cycle	6	8	10	μs
Read Mode					
t_{DD}	Access Time From CE		75	150	ns
t_{HD}	Data Valid After CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_O to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0		ns
t_{HRR}	R/$\overline{C}$ high After CE Low		0		ns
t_{HAR}	A_O Valid After CE Low		50		ns
t_{HS}	STS delay After Data Valid	100	300	600	ns

NOTE: Specifications are at + 25°C and measured at 50% level of transitions.

TABLE IV. Timing Specifications

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The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_O changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_O, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_O. See Figure 4 and Table IV for timing relationships and specifications.

FIGURE 4. Read Cycle Timing.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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ADC700

16-Bit Resolution With Microprocessor Interface A/D CONVERTER

FEATURES

● **COMPLETE WITH REFERENCE, CLOCK, 8-BIT PORT MICROPROCESSOR INTERFACE**

● **CONVERSION TIME: 17µs max**

● **LINEARITY ERROR: ±0.003% FSR max**

● **NO MISSING CODES TO 14 BITS OVER TEMPERATURE**

● **SPECIFIED AT ±12V AND ±15V SUPPLIES**

● **OUTPUT BUFFER LATCH FOR IMPROVED INTERFACE TIMING FLEXIBILITY**

● **PARALLEL AND SERIAL DATA OUTPUT**

● **SMALL PACKAGE: 28-Pin DIP**

DESCRIPTION

The ADC700 is a complete 16-bit resolution successive approximation analog-to-digital converter.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient.

The clock oscillator is current-controlled for excellent stability over temperature. Gain and Zero errors may be externally trimmed to zero. Analog input ranges of 0V to +5V, 0V to +10V, 0V to +20V, ±2.5V, ±5V, and ±10V are available.

The conversion time is 17µs max for a 16-bit conversion over the three specification temperature ranges.

After a conversion, output data is stored in a latch separate from the successive approximation logic. This permits reading data during the next conversion, a feature that provides flexible interface timing, especially for interrupt-driven interfaces.

Data is available in two 8-bit bytes from TTL-compatible three-state output drivers. Output data is coded in Straight Binary for unipolar input signals and Bipolar Offset Binary or Twos complement for bipolar input signals. BOB or BTC is selected by a logic function available on one of the pins.

The ADC700 is available in commercial, industrial and military temperature ranges. It is packaged in a hermetic 28-pin side-braze ceramic DIP.
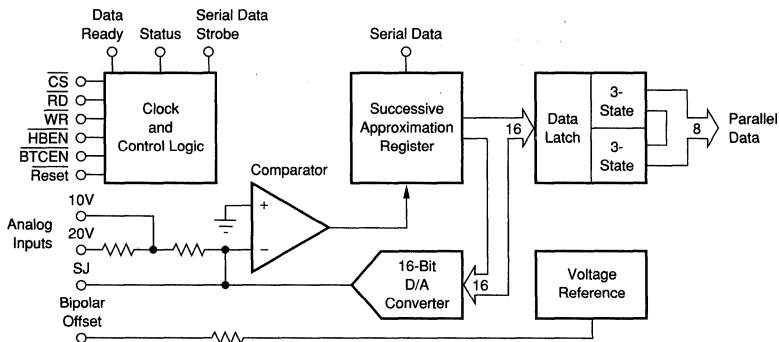
PDS-856A

BURR-BROWN®

BB

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and at rated supplies: V_{DD} = +5V, +V_{CC} = +12V or +15V, –V_{CC} = –12V or –15V unless otherwise noted.

CHARACTERISTICS	ADC700JH,AH,RH			ADC700KH,BH,SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0V to +5V, ±2.5V		2.5 ±1%			*		kΩ
0V to +10V, ±5V		5 ±1%			*		kΩ
0V to +20V, ±10V		10 ±1%			*		kΩ
DIGITAL SIGNALS (Over Specification Temperature Range)							
Inputs							
Logic Levels[1]							
V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	μA
I_{IL} (V_I = +0.4V)			±20			*	μA
Outputs							
Logic Levels							
V_{OL} (I_{OL} = –1.6mA)			+0.4			*	V
V_{OH} (I_{OH} = +20μA)	+2.4			*			V
$I_{LEAKAGE}$							
Data Outputs Only, High Z		10			*		nA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.006			±0.003	% of FSR[2]
Differential Linearity Error			±0.012			±0.006	% of FSR
Gain Error[3]		±0.1	±0.2		*		%
Zero Error[3]							
Bipolar Zero		±0.1	±0.2		*	*	% of FSR
Unipolar Zero		±0.05	±0.1		*	*	% of FSR
Noise at Transitions (3σp-p)		±0.001	±0.003		*	*	% of FSR
Power Supply Sensitivity							
+V_{CC}		±0.0015			*		%FSR/%V_{CC}
–V_{CC}		±0.0015			*		%FSR/%V_{CC}
V_{DD}		±0.0005			*		%FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)							
Gain Drift		±8	±15		*	*	ppm/°C
Zero Drift							
Bipolar Zero		±5	±10		*	*	ppm of FSR/°C
Unipolar Zero		±2	±4		*	*	ppm of FSR/°C
Linearity Drift		±1	±3		*	±2	ppm of FSR/°C
No Missing Codes Temperature Range							
JH (13-bit), KH (14-bit)	0		+70	*		*	°C
AH (13-bit), BH (14-bit)	–25		+85	*		*	°C
RH (13-bit), SH (14-bit)	–55		+125	*		*	°C
CONVERSION TIME 16 bits		15	17		*	*	μs
WARM–UP TIME	5			*			min
OUTPUT DATA CODES[4]							
Unipolar Parallel		USB			*		
Bipolar Parallel[5]		BTC, BOB			*		
Serial Output (NRZ)		USB, BOB			*		
POWER SUPPLY REQUIREMENTS							
Voltage Range							
+V_{CC}	+11.4	+15	+16	*	*	*	VDC
–V_{CC}	–11.4	–15	–16	*	*	*	VDC
V_{DD}	+4.75	+5	+5.25	*	*	*	VDC
Current[5]							
+V_{CC}		+10	+15		*	*	mA
–V_{CC}		–28	–35		*	*	mA
V_{DD}		+17	+20		*	*	mA
Power Dissipation		645	765		*	*	mW
TEMPERATURE RANGE							
Specification							
J, K Grades	0		+70	*		*	°C
A, B Grades	–25		+85	*		*	°C
R, S Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

ADC700

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

TIMING SPECIFICATIONS [6]

V_{DD} = +5V, +V_{CC} = +12V or +15V, $-V_{CC}$ = -12V or -15V unless otherwise noted.

PARAMETER	LIMIT AT T_A = 25°C	LIMIT AT T_A = 0, +70°C -25°C, +85°C	LIMIT AT T_A = -55°C, +125°C	UNITS	DESCRIPTION
CONVERSION AND SERIAL DATA OUTPUT TIMING					
t_1	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Setup time
t_2	110	130	145	ns, max	$\overline{WR}$ to Status delay
t_3	40	40	40	ns, min	$\overline{WR}$ pulse width
t_4	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Hold time
t_5	15	17	17	µs, max	Conversion time
t_6	550	600	650	ns, max	Data Ready to Status time
t_7	1100	1150	1250	ns, max	$\overline{WR}$ to first Serial Data Strobe
t_8	250	210	200	ns, min	First Serial Data to first Serial Data Strobe
t_9	310	360	400	ns, max	Last Serial Data Strobe to Status
t_{10}	0	0	0	ns, min	Status to $\overline{WR}$ Setup time
PARALLEL DATA OUTPUT TIMING					
t_{11}	0	0	0	ns, min	$\overline{HBEN}$ to $\overline{RD}$ Setup time
t_{12}	0	0	0	ns, min	$\overline{CS}$ to $\overline{RD}$ Setup time
t_{13} [7]	50	58	66	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 20pF (High Byte bus access time)
	70	81	95	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 100pF (High Byte bus access time)
t_{14}	40	40	40	ns, min	$\overline{RD}$ pulse width
t_{15}	40	45	50	ns, max	Data Ready delay from $\overline{RD}$ ($\overline{HBEN}$ asserted)
t_{16} [8]	50	60	65	ns, max	Data Hold time after $\overline{RD}$ (bus relinquish time)
t_{17}	0	0	0	ns, min	$\overline{RD}$ to $\overline{CS}$ Hold time
t_{18}	0	0	0	ns, min	$\overline{RD}$ to $\overline{HBEN}$ Hold time
RESET TIMING					
t_{19}	60	70	80	ns, max	Data Ready low delay from $\overline{Reset}$
t_{20}	70	81	95	ns, max	Status low delay from $\overline{Reset}$

*Same specs as ADC700JH, AH, RH.
NOTES: (1) TTL, LSTTL, and 5V CMOS compatible. (2) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (3) Externally adjustable to zero. (4) See Table I. USB – Unipolar Straight Binary; BTC – Binary Two's Complement; BOB – Bipolar Offset Binary; NRZ – Non Return to Zero. (5) Max supply current is specified at rated supply voltages. (6) All input control signals are specified with t_{RISE} = t_{FALL} = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. (7) t_{13} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. (8) t_{16} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

ABSOLUTE MAXIMUM RATINGS

+V_{DD} to Digital Common .... 0V to +7V
+V_{CC} to Analog Common .... 0V to +18V
$-V_{CC}$ to Analog Common .... 0V to -18V
Digital Common to Analog Common .... -1V to +1V
Digital Inputs to Digital Common .... -0.5V to V_{DD} + 0.5V
Analog Inputs .... +16.5V
Power Dissipation 1000mW
Storage Temperature .... -60°C to +150°C
Lead Temperature, (soldering, 10s) .... +300°C

NOTES: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGING INFORMATION [1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC700JH	28-Pin Ceramic DIP	237
ADC700KH	28-Pin Ceramic DIP	237
ADC700AH	28-Pin Ceramic DIP	237
ADC700BH	28-Pin Ceramic DIP	237
ADC700RH	28-Pin Ceramic DIP	237
ADC700SH	28-Pin Ceramic DIP	237

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	LINEARITY ERROR (%FSR)
ADC700JH	0°C to 70°C	±0.006
ADC700KH	0°C to 70°C	±0.003
ADC700AH	-25°C to +85°C	±0.006
ADC700BH	-25°C to +85°C	±0.003
ADC700RH	-55°C to +125°C	±0.006
ADC700SH	-55°C to +125°C	±0.003
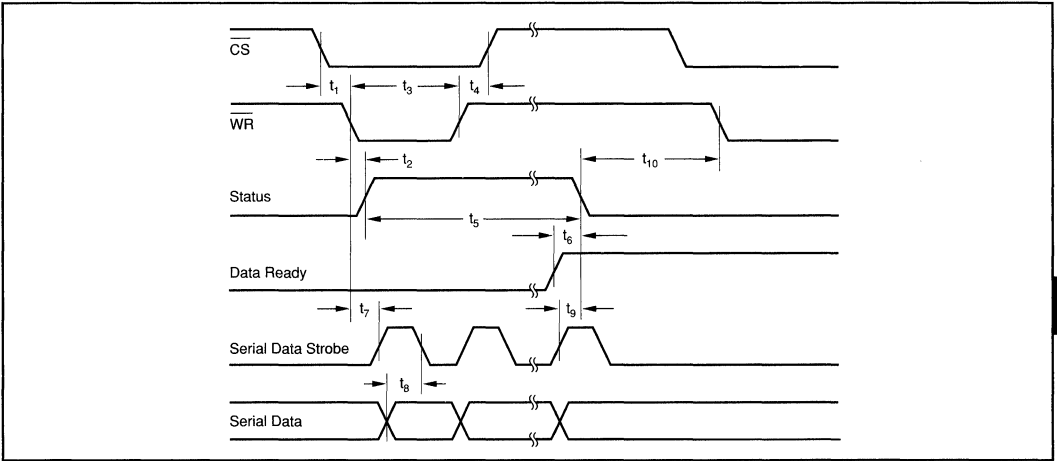
Start of Conversion and Serial Data Output Timing.
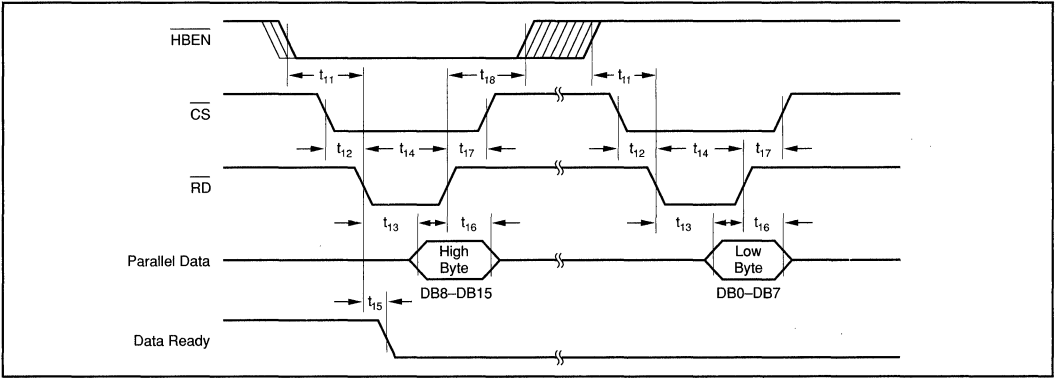
ADC700 Parallel Output Timing.
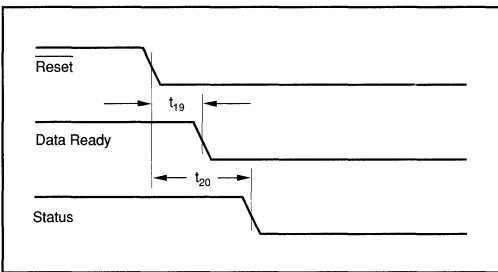
ADC700 Reset Function Timing Diagram.

ADC700

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN CONFIGURATION

Comparator In	1	28	20V Range
Bipolar Offset	2	27	10V Range
+V$_{CC}$	3	26	Analog Common
Gain Adjust	4	25	Digital Common
−V$_{CC}$	5	24	V$_{DD}$
$\overline{Reset}$	6	23	$\overline{BTCEN}$
$\overline{WR}$	7	22	DB15/DB7
$\overline{RD}$	8	21	DB14/DB6
$\overline{CS}$	9	20	DB13/DB5
$\overline{HBEN}$	10	19	DB12/DB4
Serial Data	11	18	DB11/DB3
Data Ready	12	17	DB10/DB2
Status	13	16	DB9/DB1
Serial Data Strobe	14	15	DB8/DB0

Blocks shown internally: Voltage Reference, Control Logic, 16-Bit D/A Converter, Successive Approximation Register, Data Latch, 3-State Drivers, Clock and Clock Logic. 5kΩ and 5kΩ resistors, MSB LSB.

All internal control lines not shown. Refer to Figures 4 and 5 for Offset and Gain Adjust connections.
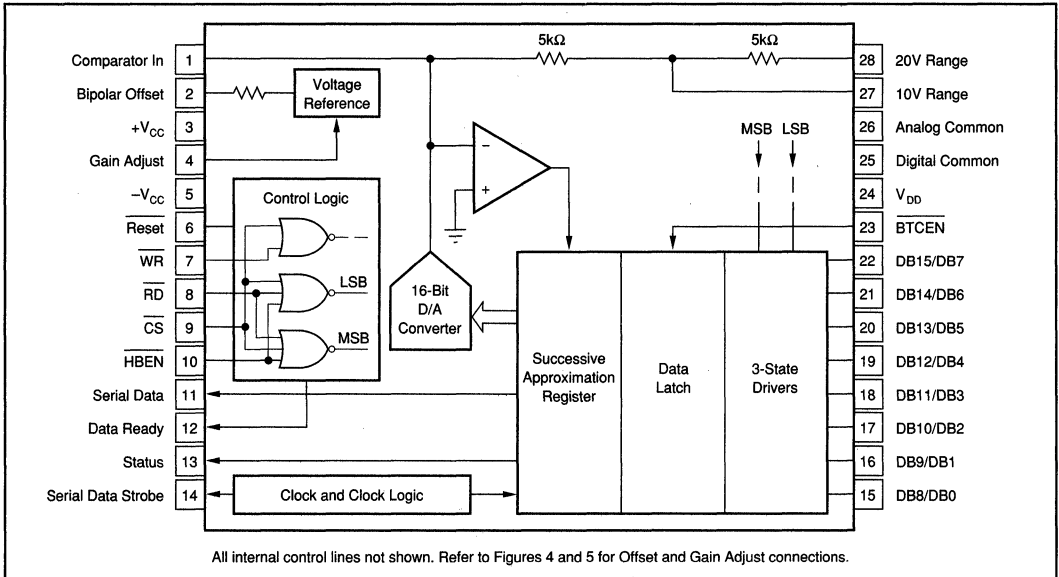
DESCRIPTION
AND OPERATING FEATURES

The ADC700 is a 16-bit resolution successive approximation A/D converter. Parallel digital data as well as serial data is available. Several features have been included in the ADC700 making it easier to interface with microprocessors and/or serial data systems. Several analog input ranges are available.

Some of the key operating features are described here. More detail is given in later sections of the data sheet. Refer to the block diagram above.

RESET

The ADC700 has a $\overline{Reset}$ input that must be asserted upon power-up or after a power interruption. This initializes the SAR, the output buffer register and Data Ready flag. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700.

PARALLEL DATA

The parallel data output is available through an 8-bit port with 3-state output drivers. High byte and low byte are selected by $\overline{HBEN}$ (pin 10).

A buffer/latch is included between the successive approximation register (SAR) and the 3-state drivers. This feature permits more flexible interface timing than is possible from most successive approximation converters.

The "old" word can be read during the next conversion. A Data Ready flag (pin 12) is asserted when a "new" word is

in the buffer register. The Data Ready flag goes low ("0") when the most significant byte (high byte) is read. If the "old" word is not read, or if only the least significant byte (low byte) is read, Data Ready is not reset. The next conversion output will overwrite the data latch when the conversion is complete. The Data Ready flag remains high. Refer to timing diagrams in the Specifications section.

SERIAL DATA

Sixteen-bit serial data output is available (pin 11) along with a serial output strobe (pin 14). This serial data strobe is not the internal SAR clock but is a special strobe for serial data consisting of 16 negative-going edges (during conversion) occurring about 200ns after each serial data bit is valid. This feature eases the interface to shift registers or through opto-couplers for applications requiring galvanic isolation.

STATUS

The familiar Status (or Busy) flag, present in successive approximation A/D converters, is available (pin 13) and indicates that a conversion is in progress. Status is valid 110ns after assertion of the convert command (WR low). Status cannot be used as a sample-hold control because there is not enough time for the sample-hold to settle to the required error band before the ADC700 makes its first conversion decision.

CHIP SELECT

$\overline{CS}$ (pin 9) selects the ADC700. No other functions can be implemented unless $\overline{CS}$ is asserted. $\overline{WR}$ (pin 7) is the start-of-conversion strobe. $\overline{RD}$ strobes each output data byte, selected by $\overline{HBEN}$ (pin 10), to the 3-state drivers.

TWO'S COMPLEMENT DATA CODE

$\overline{BTCEN}$ (pin 23) is a logic function that implements the Binary Two's Complement output code for bipolar (+ and −) analog input signal operation. This feature is compatible with twos complement arithmetic in microprocessor math algorithms.

INTERNAL CLOCK

The ADC700 has a self-contained clock to sequence the A/D logic. The clock is not available externally. An external 16-pulse strobe (pin 14) is brought out to clock serial data only. Use of ADC700 with external clock is not possible.

INTERNAL VOLTAGE REFERENCE

The ADC700 has an internal low-noise buried-zener voltage reference. The reference circuit has been drift compensated over the MIL temperature range using a laser trim algorithm. The reference voltage is not available externally.

DISCUSSION
OF SPECIFICATIONS

BASIC DEFINITIONS

Refer to Figure 3 for an illustration of A/D converter terminology and to Table II in the Calibration section.

Full Scale Range, FSR

The nominal range of the A/D converter. For ADC700, the FSR is 20V for the 0V to +20V and the −10V to +10V input ranges or 10V for the 0V to +10V and −5V to +5V input ranges.

Least Significant Bit, LSB

The smallest analog input change resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is $FSR(2^{-N})$.
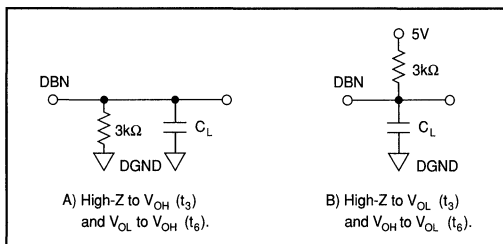
Most Significant Bit, MSB

That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution

An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

ACCURACY

Linearity Error, Integral Linearity Error (ILE)

Linearity Error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near positive full scale (at $+V_{FS}$ −1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at Zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$). Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADC700KH ILE is ±0.003% of FSR which is 1/2 LSB at 14-bits.

Differential Linearity Error (DLE), No Missing Codes

Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than −1LSB anywhere along the range, the A/D will have at least one missing code. ADC700KH is specified to have a DLE of ±0.006% of FSR, which is ±1LSB at 14 bits. ADC700KH is specified to have *no missing codes* at the 14-bit level over specified temperature ranges.

Gain Error

The deviation from the ideal magnitude of the input span between the first code midpoint (at $-V_{FS}$ + 1/2LSB, for bipolar operation; at Zero for unipolar operation) to the last code midpoint (V_{FS} −1LSB). As with the linearity error

FIGURE 1. Load Circuits for Access Time.

FIGURE 2. Load Circuits for Output Float Delay.
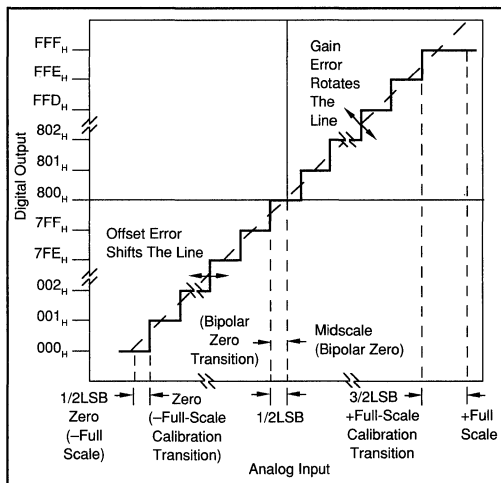
FIGURE 3. Transfer Characteristic Terminology.

ADC700

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

measurements, code transition values are the locations actually measured for this spec. The ideal gain is V_{FSR} –2LSB. Gain Error is expressed in % (of reading). See Figure 3.

Gain Error of the ADC700 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error—The deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error—The deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at – V_{FS} +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADC700 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a percentage of FSR.

Bipolar Zero Error—The deviation of the actual mid-scale-code midpoint value from zero. Transition values are the actual measured parameter and it is 1/2 LSB below zero volts. The error is comprised of Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error of bit 1. Bipolar Zero Error is expressed as a percentage of FSR.

Power Supply Sensitivity

Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. PSR is specified in units of %FSR/% change in each supply voltage.

The major effect of power supply voltage deviations from the rated values will be a small change in the Gain (scale factor). Power Supply Sensitivity is also a function of ripple frequency. Figure 4 illustrates typical Power Supply Sensitivity performance of ADC700 versus ripple frequency.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADC700, system design problems such as ground path resistance and contact resistance become very important. For a 16-bit resolution converter with a +10V Full-Scale Range, 1LSB is 153µV. Circuit situations that cause only second- or third-order errors in 8-, 10-, or 12-bit A/D converters can induce first-order errors in 16-bit resolution devices.

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the analog and digital common lines.

Power Supply Returns
(Analog Common and Digital Common)

Connect Analog Common and Digital Common together right at the converter with the ground plane. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. Connect a 1 to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing

Every power-supply line leading into an A/D converter must be bypassed to its common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground—connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 10µF to 100µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals

Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Shield Other Sensitive Points

The most critical of these is the comparator input (pin 1). If this pin is not used for offset adjustment, then it should be surrounded with ground plane or low-impedance power
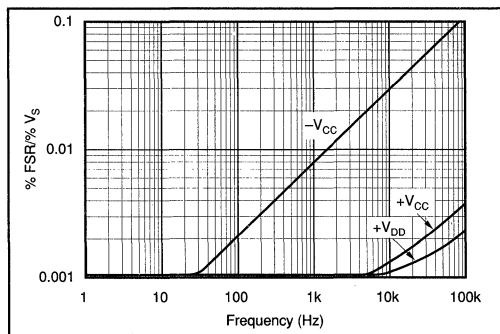
FIGURE 4. Power Supply Rejection Ripple vs Frequency.

supply plane. If it is used for offset adjustment, the series resistor and potentiometer should be located as close to the converter as possible.

The Gain Adjust (pin 4) is an input that has a relatively high input impedance and is susceptible to noise pickup. The Gain Adjust pin should be bypassed with a 0.01μF to 0.1μF capacitor whether or not the gain adjust feature is used.

If the 20V Analog input range is used (pin 28), the 10V Range input (pin 27) may need to be shielded with ground plane to reduce noise pickup.

ANALOG SIGNAL SOURCE IMPEDANCE

The input impedance of the ADC700, typical of most successive approximation A/D converters, is relatively low (2.5kΩ to 10kΩ). The input current of a successive approximation A/D converter changes rapidly during the conversion algorithm as each bit current is compared to the analog input current. Since the output impedance of a closed-loop amplifier or a sample-hold amplifier increases with frequency and, in addition, the amplifier must settle to the required accuracy in time for the next comparison/decision after such a disturbance, care must be taken to select the proper driving amplifier.

Unfortunately, high-accuracy operational amplifiers tend to have low bandwidth, while wide-band amplifiers tend to have lower accuracy. One solution is to use a wide-band but perhaps less precise amplifier. Another solution is to add a wide-band buffer amplifier such as the Burr-Brown OPA633 inside the feedback loop of a slower (but precision) amplifier, Figure 5. This reduces the output impedance at high frequencies yet preserves the accuracy at low frequencies. When a sample/hold is needed, a high-linearity, high-speed sample/hold such as the Burr-Brown SHC76 should be used to drive the ADC700.

ANALOG INPUT RANGES

The analog input circuits of the ADC700 can be connected to accept unipolar or bipolar input signals. These ranges and connections are tabulated in Table I. Circuit connections are shown in Figures 6 and 7. Gain and offset adjustments are described in the calibration section.

To operate the ADC700 with a range that gives other convenient values for the LSB, the input resistor may be increased or decreased slightly without seriously affecting the Gain Drift of the converter. Since the input resistors of the ADC700 are within ±2% from unit to unit, this can be
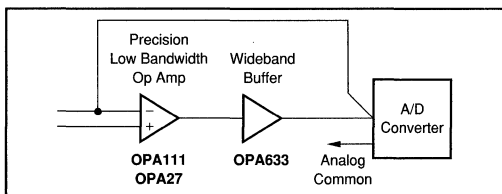
FIGURE 5. Wideband Buffer Reduces Output Impedance at High Frequencies.

consistently done with a fixed series or parallel resistor. The ADC700 can then be calibrated using the Gain and Offset adjustments described in the calibration section. For example, using the ±10V input range, one can decrease the range slightly by paralleling the 10kΩ input resistor (pin 28 to pin 1) with a 610kΩ metal film resistor to achieve a 300μV LSB instead of the nominal standard 305.17578μV binary LSB.

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Gain and Offset Error may be trimmed to zero using external Gain and Offset trim potentiometers connected to the ADC700 as shown in Figures 6 and Figure 7. A calibration procedure in described in the Operating Instructions section.

Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature. These potentiometers may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 1 (Comparator In) and pin 4 (Gain Adjust) may be left open if no external adjustment is planned; however, pin 4 should always be bypassed with 0.01μF or larger to Analog Common.

OPERATING INSTRUCTIONS

CALIBRATION

Offset and Gain may be trimmed by external Offset and Gain potentiometers. Offset is adjusted first and then Gain. Calibration values are listed in Table II for all ADC700 input ranges. Offset and Gain calibration can be accomplished to a precision of about ±1/2LSB using a static adjustment procedure described below. By summing a small sine or triangular wave voltage with the accurate calibration voltage applied to the analog input, the output can be swept through each of the calibration codes to more accurately determine the transition points listed in Table II. NOTE: The transition points are not the same as the code midpoints used in the static calibration example.

OFFSET ADJUSTMENT, 14-BIT RESOLUTION EXAMPLE

Static Adjustment Procedure (At Code Midpoints)

0V to +10V Range—Set the analog input to $+1LSB_{14} = 0.00061V$. Adjust the Offset potentiometer for a digital output of 0004_H. Set the analog input to +Full Scale $-2LSB_{14} = +9.9987V$. Adjust the Gain potentiometer for a digital output of $FFFC_H$. For a half-scale calibration check, set the analog input to +5.0000V and read a digital output code of 8000_H.

INPUT SIGNAL RANGE	OUTPUT CODE		CONNECT PIN 2 TO PIN	CONNECT PIN 28 TO PIN	CONNECT SIGNAL TO PIN
	BTCEN = 1	BTCEN = 0			
±10V	BOB	BTC	1	Input Signal	28
±5V	BOB	BTC	1	Open	27
±2.5V	BOB	BTC	1	Pin 1	27
0V to +5V	USB	—	26	Pin 1	27
0V to +10V	USB	—	26	Open	27
0V to +20V	USB	—	26	Input Signal	28

TABLE I. ADC700 Input Range Connections.

ANALOG INPUT RANGE	VOLTAGE (V)					
	±10	±5	±2.5	0 TO +20	0 TO +10	0 TO +5
+V_FS	+10	+5	+2.5	+20	+10	+5
−V_FS	−10	−5	−2.5	0	0	0
FSR	20	10	5	20	10	5
TRANSITION CODES (Hexadecimal)	**TRANSITION VALUES (V)**					
For 16-bit Resolution (Reading all 16 bits)						
$FFFE_H$ to $FFFF_H$	+9.999542	+4.999771	+2.499886	+19.999542	+9.99971	+4.999886
$7FFF_H$ to 8000_H	−152.5µV	−38µV	−19µV	+9.999847	+4.999924	+2.499962
0000_H to 0001_H	−9.999847	−4.999924	−2.499962	+152µV	+76µV	+38µV
LSB $(FSR/2^{16})$	305µV	153µV	38µV	305µV	153µV	76µV
For 15-bit Resolution (Reading all 16 bits, Ignoring DB_0)						
$FFFD_H$ to $7FFE_H$	+9.999084	+4.999542	+2.499771	+19.999084	+9.999542	+4.999771
$7FFE_H$ to 8000_H	−305µV	−153µV	−76µV	+9.999625	+4.999847	+2.499924
0000_H to 0002_H	−9.999695	−4.999847	−2.499924	+305µV	+152µV	+76µV
LSB $(FSR/2^{15})$	610µV	305µV	153µV	610µV	305µV	153µV
For 14-bit Resolution (Reading all 16 bits, Ignoring DB_0 and DB_1)						
$FFFC_H$ to $FFFD_H$	+9.99817	+4.99908	+2.49954	+19.99817	+9.99908	+4.99954
$7FFD_H$ to 8000_H	−610µV	−305µV	−153µV	+9.99939	+4.999695	+2.499847
0000_H to 0004_H	−9.999390	−4.999694	−2.499847	+610µV	+305µV	+153µV
LSB $(FSR/2^{14})$	1221µV	610µV	305µV	1221µV	610µV	305µV

TABLE II. Transition Values for Calibration.
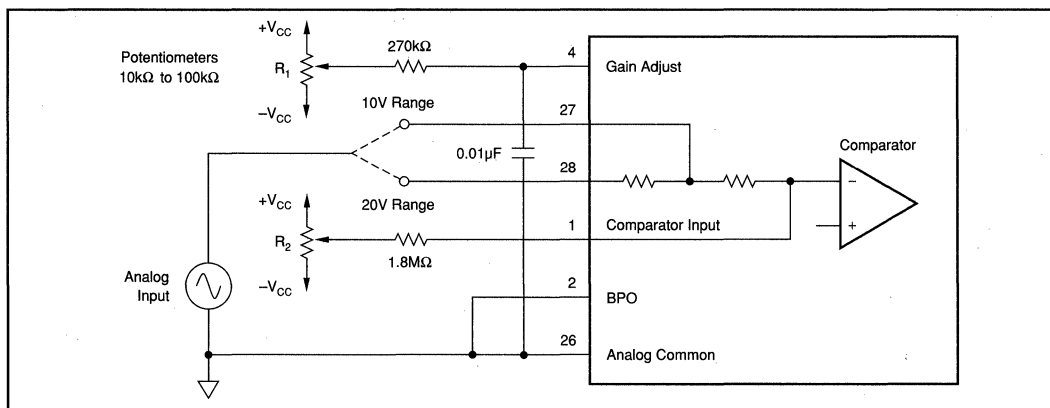
FIGURE 6. Unipolar Input Configuration with Gain and Offset Adjust Connections.
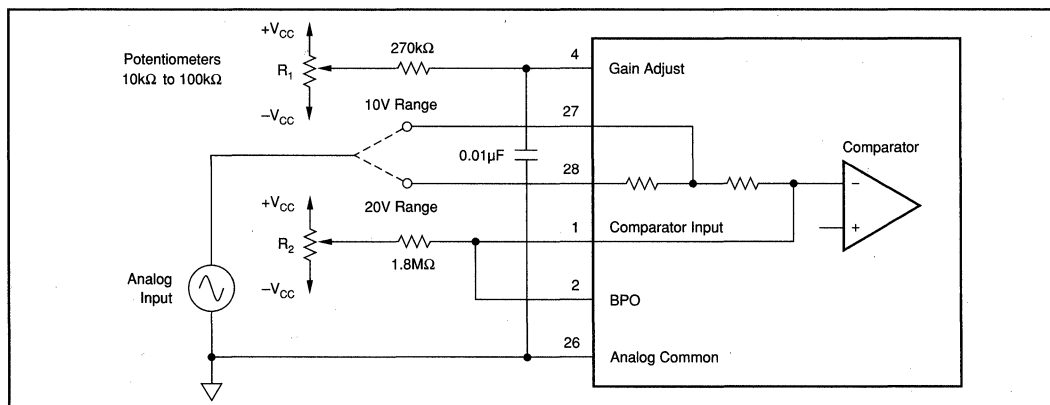
FIGURE 7. Bipolar Input Configuration with Gain and Offset Adjust Connections.

–10V to +10V Range—Set the analog input to –FS + 1LSB$_{14}$ = –9.99878V. Adjust the Offset potentiometer for a digital output of 0004$_H$ (8004$_H$ if $\overline{\text{BTCEN}}$ is asserted). Set the analog input to +9.9976V. Adjust the Gain potentiometer for a digital output of FFFC$_H$ (7FFC$_H$ if $\overline{\text{BTCEN}}$ is assrted). For a half-scale calibration check, set the analog input to 0.0000V and read a digital output code of 8000$_H$ (0000$_H$ if $\overline{\text{BTCEN}}$ is asserted).

CONTROLLING AND INTERFACING THE ADC700

RESET

The ADC700 requires a Reset command upon power-up or after a power interruption to guarantee the condition of internal registers. If Status powers-up High, no conversion can be started. Reset initializes the SAR, the output buffer register, and the Data Ready flag and terminates a conversion in progress. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700. A power-up circuit is shown in Figure 8. Refer to Reset function timing diagram following the Timing Specifications Table.
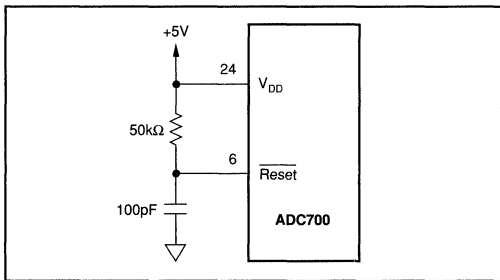
FIGURE 8. Power-Up Reset Circuit.
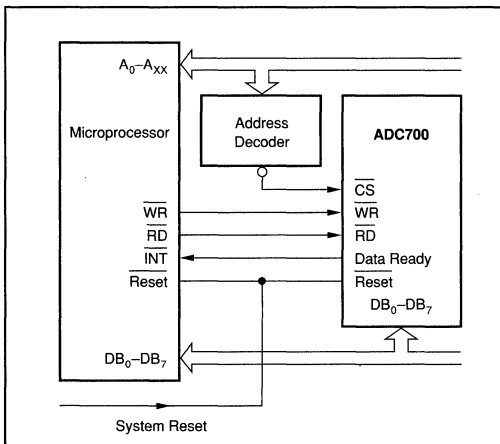
FIGURE 9. Parallel Data Bus Interface.

START OF CONVERSION

A conversion is started by asserting $\overline{\text{CS}}$ and $\overline{\text{WR}}$ Low. Status goes high about t = t$_1$ + t$_2$ = 110ns later. The first successive approximation decision occurs about 900ns after $\overline{\text{WR}}$ is asserted. Status goes Low after the conversion is complete. Refer to Start of Conversion and Serial Data Output Timing following the Timing Specifications Table.

DATA READY FLAG

The data latch feature permits data to be read during the following conversion. The Data Ready flag indicates that the data from the most recent conversion is latched in the output data latch and that it hasn't been read. Data Ready remains High until the most significant data byte is read. If a subsequent conversion is initiated and completed, the new word will be stored in the output data latch regardless of the state of the Data Ready flag. The preceding word will be overwritten and lost.

READING PARALLEL DATA

Parallel data is latched in the output data latch at the end of a conversion. Data can be read any time, even during the subsequent conversion. The output data latch is not cleared by reading the data. Only the Data Ready flag is cleared by reading the MSB.

The output three-state drivers are enabled by asserting the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs Low. When $\overline{\text{HBEN}}$ is Low, the most significant eight bits are enabled and the Data Ready flag is cleared. When $\overline{\text{HBEN}}$ is High, the least significant eight bits are enabled. Refer to Parallel Data Output Timing information following the Timing Specifications Table.

To reduce noise interference to the absolute minimum, data should be read after the current conversion is complete. However, data can be read during the following conversion, with minimal interference, to maximize the sampling rate of the converter.

A typical parallel interface is illustrated in Figure 9.

READING SERIAL DATA

Serial data output of the ADC700 is facilitated by a Serial Data Strobe that provides 16 negative-going edges for strobing an external serial to parallel shift register located perhaps on the other side of an opto-coupler. Refer to the Serial Data Timing information following the Timing Specifications Table. An example of an isolation connection using the serial port feature is illustrated in Figure 10.

CONTINUOUS CONVERSION OPERATION

When $\overline{\text{CS}}$ is permanently connected to Digital Common and Status is connected to $\overline{\text{WR}}$, Figure 11, the ADC700 will continuously convert. The repetition time will not be precise and will vary slightly with the temperature for the ADC700 because the time will be determined by the internal clock frequency and control-circuit gate delays. If a precise repetition rate is needed, the continuous conversion connection should not be used.
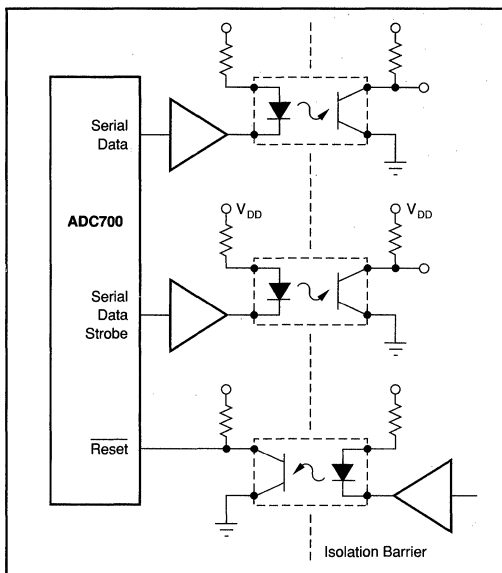
FIGURE 10. Serial Data Output Providing Convenient Isolation.
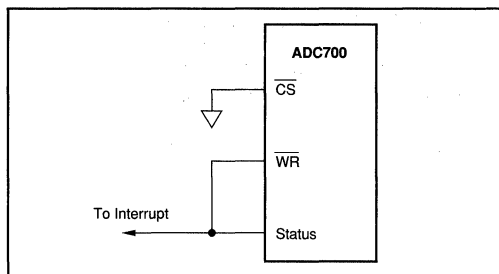
FIGURE 11. Continuous Conversion Circuit Connection.

PIN DESIGNATION	DEFINITION	FUNCTION
$\overline{CS}$ (Pin 9)	Chip Select	Must be Low to either initiate a conversion or read output data.
$\overline{WR}$ (Pin 7)	Write (Convert)	Conversion begins after the High-to-Low transition.
$\overline{RD}$ (Pin 8)	Read	Turns ON the three-state output drivers upon being asserted low.
$\overline{HBEN}$ (Pin 10)	High Byte Enable "1" = Low Byte "0" = High Byte	Selects the MSB or the LSB for readout. Data Ready is cleared when $\overline{HBEN}$ is Low and $\overline{RD}$ is asserted.
$\overline{Reset}$ (Pin 6)	Reset	Resets internal logic. Must be asserted after power-up or a power interruption clears Status and Data Ready to Low.
$\overline{BTCEN}$ (Pin 23)	BTC Enable	Sets the output code to Binary Twos Complement (BTC) when Low. Output code is Bipolar Offset Binary (BOB) when High.

TABLE III. Control Line Functions.

CONTROL LINE					OPERATION
RESET	$\overline{WR}$	$\overline{RD}$	HBEN	$\overline{CS}$	
0	X	X	X	X	Reset converter logic. Status and Data Ready set Low.
1	X	X	X	1	No operation.
1	0	X	X	0	Initiate conversion.
1	1	0	0	0	Places High Byte on output port. Clears Data Ready flag.
1	1	0	1	0	Placed Low Byte on output port. Does not clear Data Ready flag.
1	0	0	0	0	Initiates conversion and places High Byte or output port. Clears Data Ready.
1	0	0	1	0	Initiates conversion and places Low Byte on output port. Does not clear Data Ready flag.

NOTE: If a conversion command is asserted while a conversion is in progress, the command is ignored. If the conversion command remains asserted when a conversion is finished, a new conversion will begin.

TABLE IV. Control Input Truth Table.

Because the last data-word is stored in the data latch, it is possible to read it during the next A/D conversion. Assertion of $\overline{CS}$ and $\overline{HBEN}$ for reading parallel data should be timed from Status going low. The two-byte read operation must be complete before the conversion in process is complete or the Data Read is invalid.

Serial Data is available during continuous conversion with word synchronization available from STATUS.

USING A SAMPLE/HOLD WITH ADC700

Figure 12 illustrates using ADC700 with the Burr-Brown SHC76. The sample-to-hold settling time (to 14 bits, ±0.003%FSR) of the SHC76 is 1μs typ, 3μs max. The time from the Status going High to the first conversion decision is about 900ns. Therefore a time delay between the Sample-to-Hold command to the $\overline{WR}$ command to the ADC700 is required.
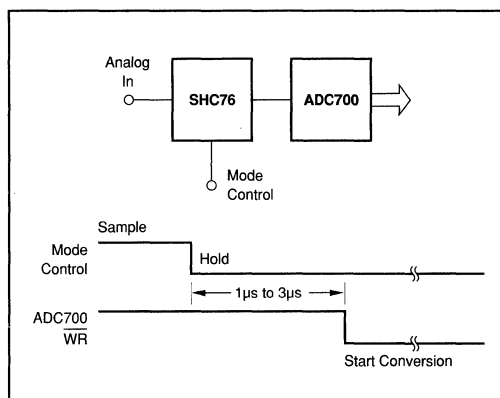
FIGURE 12. Using Sample/Hold with ADC700 Requires Time Delay Between Sample and Start-of-Conversion.

ADC700

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

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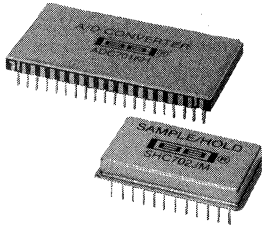
ADC701

SHC702

16-Bit 512kHz
SAMPLING A/D CONVERTER SYSTEM

FEATURES

- **CONVERSION RATE: to 512kHz Over Temp**
- **NO MISSING CODES AT 16 BITS**
- **SPURIOUS-FREE DYNAMIC RANGE: 107dB**
- **LOW NONLINEARITY: ±0.0015%**
- **SELECTABLE INPUT RANGES: ±5V, ±10V, 0 to +10V, 0 to +5V, −10V to 0**
- **LOW POWER DISSIPATION: 2.8W Typical Including Sample/Hold**
- **METAL AND CERAMIC DIP PACKAGES**

APPLICATIONS

- **MEDICAL IMAGING**
- **SONAR**
- **PROFESSIONAL AUDIO RECORDING**
- **AUTOMATIC TEST EQUIPMENT**
- **HIGH PERFORMANCE FFT SPECTRUM ANALYSIS**
- **ULTRASOUND SIGNAL PROCESSING**
- **HIGH SPEED DATA ACQUISITION**
- **REPLACES DISCRETE MODULAR ADCs**

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.

PDS-877C

BURR - BROWN®

BB

SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH			ADC701KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar			0 to +5, 0 to +10, −10 to 0				V
	Bipolar			±5, ±10				V
Resistance	0 to +5V Range	2.45	2.5	2.55	*	*	*	kΩ
	0 to +10V, −10 to 0, ±5V Ranges	4.9	5	5.1	*	*	*	kΩ
	±10V Range	9.8	10	10.2	*	*	*	kΩ
Capacitance	All Ranges		5			*		pF
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Convert Command	Start Conversion			Rising Edge				
Pulse Width	t = Conversion Period	50		t − 50	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[1]	0 to +10V Range		±0.03	±0.1		*	*	%
	±10V Range		±0.03	±0.1		*	*	%
Power Supply Sensitivity of Gain	All Ranges, All Supplies		±0.005	±0.1		*	*	%/V
Input Offset Error[1]	0 to +10V Range		±1	±3		*	*	mV
	±10V Range		±5	±10		*	*	mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		±0.006	±0.1		*	*	%FSR/V
Integral Linearity Error[2]			±0.002	±0.003		±0.0012	*	%FSR[3]
Differential Linearity Error[2]			±0.0006	±0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{SOURCE} \le 50\Omega$		0.6			*		LSB rms
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		512	*		*	kHz
Conversion Time[4]	Unadjusted		1.45	1.5		*	*	μs
OUTPUTS								
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Data Coding	Unipolar Ranges			Straight Binary				
	Bipolar Ranges			Offset Binary				
Logic "0" Levels (V_{OL})	$I_{OL} \le 3.2mA$		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \le 80\mu A$	4	4.9		*	*		V
Data Valid Setup Time Before Strobe	Both Edges	28	37		*	*		ns
INTERNAL REFERENCE								
Voltage	$R_{LOAD} \ge 5k\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*		mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		−4.25	−5	−6	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30		*	*	mA
$-I_{CC}$			33	45		*	*	mA
$+I_{DD1}$			45	55		*	*	mA
$-I_{DD1}$			37	50		*	*	mA
$+I_{DD2}$			133	150		*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A Min to T_A Max	+15		+55	0		+70	°C
Gain Error	All Ranges		±10	±15		*	*	ppm/°C
Input Offset Error	All Unipolar Ranges		±1	±5		*	*	ppm FSR/°C
	All Bipolar Ranges		±1	±5		*	*	ppm FSR/°C
Integral Linearity Error[2]			±0.2			*	±0.5	ppm/°C
Differential Linearity Error[2]			±0.05			*	±0.3	ppm/°C
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			±3			*		ppm/°C
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/°C
Sample Rate	Unadjusted	DC		512	*		*	kHz

* Same specifications as ADC701JH.

ADC701/SHC702

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS

ELECTRICAL (SHC702 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = $\pm$15V, $+V_{DD1}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	SHC702JM			UNITS
		MIN	TYP	MAX	
INPUTS (Without Input Buffer)					
ANALOG					
Voltage Range		±10.25	±11		V
Resistance		0.98	1	1.02	kΩ
Capacitance			3		pF
DIGITAL					
Logic Family			LSTTL		
Input Loading			2		LSTTL Loads
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain	R_{SOURCE} = 0Ω		−1		V/V
Gain Error	R_{SOURCE} = 0Ω		±0.02	±0.1	%
Linearity Error	Sample Mode		±0.0003		%FSR
Offset Error	Sample Mode		±0.5	±3	mV
Charge Offset (Pedestal) Error	Sample/Hold Mode, R_{SOURCE} ≤ 50Ω		±0.5	±5	mV
Droop Rate	Hold Mode		±0.2	±2	μV/μs
Dynamic Nonlinearity	Sample/Hold Mode		±0.0005		%FSR
Power Supply Sensitivity	Offset Plus Charge Offset, All Supplies		±0.003		%FSR/V
DYNAMIC CHARACTERISTICS					
Acquisition Time	10V Step to ±150μV		600		ns
	5V Step to ±150μV		500		ns
Sample-to-Hold Settling Time[5]	to ±150μV		120		ns
Aperture Delay Time			20		ns
Aperture Uncertainty (Jitter)			10	25	ps rms
Slew Rate			150		V/μs
Small Signal Bandwidth	V_{IN} = ±1V		3.1		MHz
Full-Power Bandwidth	V_{IN} = ±10V		2		MHz
Feedthrough Rejection	Hold Mode, 10Vp-p Square Wave Input		0.001		%
OUTPUT					
Voltage Range	R_{LOAD} ≥ 1kΩ	±10.25	±11		V
Output Current		±40			mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
Output Impedance	DC		0.01	0.1	Ω
INPUT BUFFER CHARACTERISTICS					
INPUT					
Impedance			10^{13} ∥ 3		Ω ∥ pF
Bias Current	V_{IN} = ±10V		±2	±15	pA
Offset Voltage	R_{SOURCE} ≤ 10kΩ		±0.3	±1.5	mV
Voltage Range		±10.25	±11		V
DYNAMIC CHARACTERISTICS					
Slew Rate		20	35		V/μs
Full-Power Bandwidth	V_{IN} = ±10V		570		kHz
Settling Time	10V Step to ±150μV		1.7		μs
OUTPUT					
Output Current		±15	±20		mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$	Operating	+13.5	+15	+16.5	V
$-V_{CC}$		−13.5	−15	−16.5	V
$+V_{DD1}$		+4.75	+5	+5.25	V
Current: $+I_{CC}$	Operating		33	40	mA
$-I_{CC}$			18	25	mA
$+I_{DD1}$			5	10	mA
Power Dissipation	Nominal Voltages		790	950	mW
PERFORMANCE OVER TEMPERATURE					
Specification Temperature Range	T_A Min to T_A Max	0		+70	°C
Sample/Hold Gain Error	R_{SOURCE} = 0Ω		±1	±5	ppm/°C
Sample/Hold Offset Error	R_{SOURCE} ≤ 50Ω		±10	±30	μV/°C
Sample/Hold Charge Offset Error	R_{SOURCE} ≤ 50Ω		±10	±80	μV/°C
Droop Rate				±50	μV/μs
Buffer Offset Error	R_{SOURCE} ≤ 10kΩ		±3	±15	μV/°C

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and ±10V ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected; i.e., the duration of the Sample/Hold command. This time must be added to the Sample/Hold accusition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

SPECIFICATIONS

ELECTRICAL (COMBINED ADC701/SHC702)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = $\pm$15V, $\pm V_{DD1}$ = $\pm$5V, +V_{DD2} = +5V, and five minute warmup in a convection environment, $\pm$5V input range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Rate	Unadjusted	DC		512	kHz
Dynamic Nonlinearity			±0.002		%FSR
Total Harmonic Distortion (THD)	f_{IN} = 20kHz (–0.3dB)		–103		dB
	f_{IN} = 199kHz (–0.2dB)		–82		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 20kHz (–0.3dB)		107		dB
	f_{IN} = 199kHz (–12dB)		94		dB
Two-Tone Intermodulation Distortion (IMD)	f_1 = 195kHz (–6.5dB), f_2 = 200kHz (–6.5dB)		–81		dBC
	f_1 = 195kHz (–12.5dB), fF_2 = 200kHz (–12.5dB)		–86		dBC
Signal-to-Noise Ratio (SNR)	f_{IN} = 5kHz (–0.5dB)		93		dB
Total Power Dissipation	Operating		2.8	3.25	W

ADC701 PIN ASSIGNMENTS

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Bit 1/9 (Bit 1 = MSB)	40	–V_{DD1} (–5V) Analog
2	Bit 2/10	39	Common (Analog)
3	Bit 3/11	38	+V_{DD1} (+5V) Analog
4	Bit 4/12	37	Reference (Gain) Adjust
5	Bit 5/13	36	+10V Reference Output(2)
6	Bit 6/14	35	Common (Reference)
7	Bit 7/15	34	DNC
8	Bit 8/16	33	Common (Analog)
9	Clip Detect Output	32	+10V Reference Input(2)
10	+V_{DD2} (+5V) Digital	31	Input D (1)
11	Common (Digital)	30	Input C (1)
12	Data Strobe	29	Common (Signal)
13	High/Low Byte Select	28	Input B (1)
14	Convert Command	27	Input A (1)
15	Sample/Hold Control(3)	26	–V_{CC} (–15V) Analog
16	Common (Digital)	25	Common (Power)
17	Common (Digital)	24	+V_{CC} (+15V) Analog
18	Clock Adjust	23	DNC(4)
19	Common (Digital)	22	Offset Adjust
20	+V_{DD2} (+5V) Digital	21	Offset Adjust

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

PACKAGING INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC701JH	Metal and Ceramic	234
ADC701KH	Metal and Ceramic	234

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ADC701 ORDERING INFORMATION

ADC701 ( ) H

Basic Model Number ————
Performance Grade Code ————
  K: 0°C to +70°C Ambient Temperature
  J: +15°C to +55°C Ambient Temperature
Package Code ————
  H: Metal and Ceramic

ADC701 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$ .... ±18V
$\pm V_{DD1}$, +V_{DD2} .... ±7V, +7V
Analog Input .... ±V_{CC}
Logic Input .... –0.5V to (+V_{DD2} + 0.3V)
Logic Output .... ±25mA
Case Temperature .... +150°C
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +165°C
Power Dissipation 3W
Stresses above these ratings may permanently damage the device.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS   2   ADC701/SHC702

ADC701 OUTPUT CODING

INPUT LEVEL (Exact Center of Code)	NOMINAL INPUT VOLTAGE TO ADC701 (Multiply by –1 for SHC702 Input Voltage)			OUTPUT CODE (1 = Logic High)		CLIP DETECT
	0–10V RANGE (1LSB ≈ 153µV)	±10V RANGE (1LSB ≈ 305µV)	±5V RANGE (1LSB ≈ 153µV)	MSB	LSB	
Underrange	< –76µV	< –10.000153V	< –5.000076V	0000 0000 0000 0000		1
–FS	0V	–10V	–5V	0000 0000 0000 0000		0
–FS + 1LSB	+153µV	–9.999695V	–4.999847V	0000 0000 0000 0001		0
–3/4FS	+1.25V	–7.5V	–3.75V	0010 0000 0000 0000		0
–1/2FS	+2.5V	–5V	–2.5V	0100 0000 0000 0000		0
–1/4FS	+3.75V	–2.5V	–1.25V	0110 0000 0000 0000		0
–1LSB	+4.999847V	–305µV	–153µV	0111 1111 1111 1111		0
Mid-Scale	+5V	0V	0V	1000 0000 0000 0000		0
+1LSB	+5.000153V	+305µV	+153µV	1000 0000 0000 0001		0
+1/4FS	+6.25V	+2.5V	+1.25V	1010 0000 0000 0000		0
+1/2FS	+7.5V	+5V	+2.5V	1100 0000 0000 0000		0
+3/4FS	+8.75V	+7.5V	+3.75V	1110 0000 0000 0000		0
+FS –2LSB	+9.999695V	+9.99939V	+4.999695V	1111 1111 1111 1110		0
+FS – 1LSB	+9.999847V	+9.999695V	+4.999847V	1111 1111 1111 1111		0
Overrange	> +9.999924V	> +9.999847V	> +4.999924V	1111 1111 1111 1111		1

SHC702 PIN ASSIGNMENTS

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Sample/Hold Output	24	+V$_{CC}$ (+15V) Analog
2	NC[3]	23	Common (Power)
3	NC	22	–V$_{CC}$ (–15V) Analog
4	NC	21	Common (Analog)
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	Buffer Amp Input[2]
9	+V$_{DD1}$ (+5V) Analog	16	NC
10	Common (Digital)	15	Common (Signal)
11	Hold Input[1]	14	Buffer Amp Output
12	Hold Input[1]	13	Analog Input

NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

PACKAGING INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC702JM	24-Pin	113

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

SHC702 ORDERING INFORMATION

```
                                        SHC702  J  M
Basic Model Number  ─────────────────────
Performance Grade Code  ──────────────────
  J: 0°C to +70°C Ambient Temperature
Package Code  ────────────────────────────
  M: Metal
```

SHC702 ABSOLUTE MAXIMUM RATINGS

±V$_{CC}$ .... ±18V
+V$_{DD1}$ .... +7V
Analog and Buffer Inputs .... ±V$_{CC}$
Outputs .... Indefinite Short to Common
Logic Inputs .... –0.5V to (+V$_{DD1}$ + 0.3V)
Case Temperature .... +150°C
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +165°C
Power Dissipation 1.5W
Stresses above these ratings may permanently damage the device.

TYPICAL DYNAMIC PERFORMANCE (ADC701/SHC702)[1]

ADC701/SHC702

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 20kHz
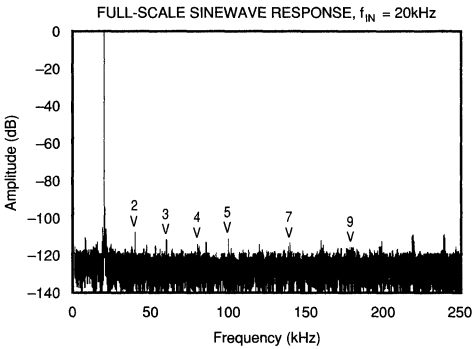
Input Frequency		19.9890136719 kHz	
Fundamental	−0.3 dB	4th Harmonic	−115.6 dB
2nd Harmonic	−107.5 dB	5th Harmonic	−111.2 dB
3rd Harmonic	−111.5 dB	6th Harmonic	−124.5 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 100kHz
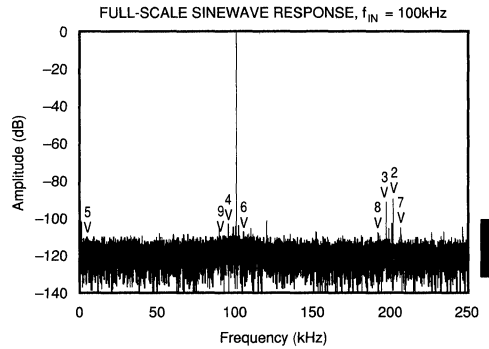
Input Frequency		100.982666016 kHz	
Fundamental	−0.5 dB	4th Harmonic	−102.5 dB
2nd Harmonic	−89.1 dB	5th Harmonic	−110.2 dB
3rd Harmonic	−90.5 dB	6th Harmonic	−106.8 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 200kHz
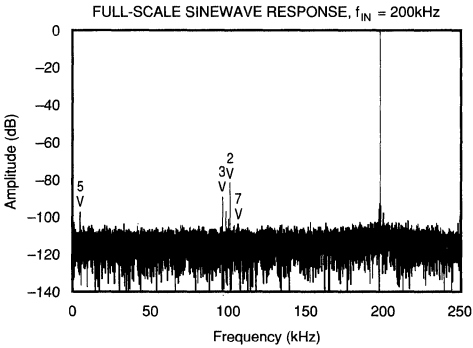
Input Frequency		199.005126953 kHz	
Fundamental	−0.7 dB	4th Harmonic	−111.5 dB
2nd Harmonic	−81.4 dB	5th Harmonic	−97.0 dB
3rd Harmonic	−89.4 dB	6th Harmonic	−112.5 dB

TWO-TONE INTERMODULATION RESPONSE, f_{IN} = 195kHz and 200kHz
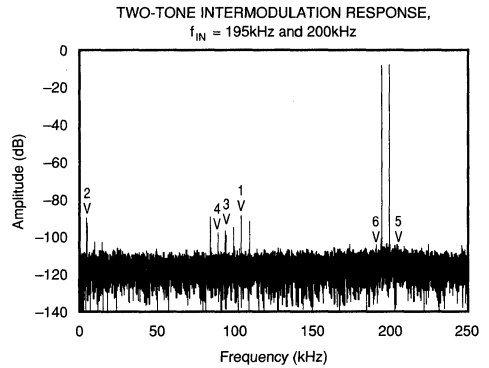
Frequency 1		194.976806641 kHz	
Frequency 2		199.981689453 kHz	
f_1	−6.8 dB	3> f_1+2f_2	−96.0 dB
f_2	−6.3 dB	4> $2f_1+f_2$	−96.8 dB
1> f_1+f_2	−87.7 dB	5> f_1-2f_2	−104.9 dB
2> f_1-f_2	−88.8 dB	6> $2f_1-f_2$	−109.0 dB

NOTE: (1) For figures above, sampling rate = 500.0000000000kHz. 16,384 point FFT, non-windowed. Noise floor limited by synthesized generators.

DIFFERENTIAL NONLINEARITY OF ALL CODES, 19.6 MILLION SAMPLES
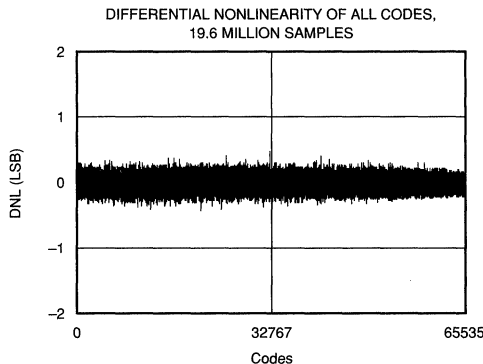
THEORY OF OPERATION

The ADC701 uses a three-step subranging architecture, meaning that the analog-to-digital conversion is performed in three passes which constitute coarse, medium and fine approximations of the input signal. Refer to Figures 1 and 2 for simplified block diagrams of the system.

Before the input signal is presented to the ADC, it must be sampled with high linearity and low aperture error by the sample/hold amplifier.

In the SHC702, the sampling switch is placed at the summing junction (virtual ground) of a high speed FET amplifier (Figure 1). This arrangement maintains constant charge injection independent of the signal amplitude, which is critically important for good linearity performance. The sampling switch itself is a high speed DMOS FET whose gate is driven from a fast-slewing control signal, thus minimizing the time aperture between the fully closed (sample mode) and the fully open (hold mode) states of the switch. The signal voltage is held across the feedback capacitor, forcing the op-amp to maintain a constant output voltage for the duration of the A/D conversion. Feedthrough from the input, already low due to the MOSFET's low capacitance, is further reduced by clamping the summing point to ground with another FET.

The ADC701 input voltage is converted to a current through the input scaling resistors (Figure 2), and this current is applied to the summing junction (virtual ground) of error amplifier A_1. The current output of the DAC (0 to 2mA) is also applied to the summing point. If bipolar operation is selected, the 10V reference output is applied to input D, creating a 1mA offset current which sums with the input current.
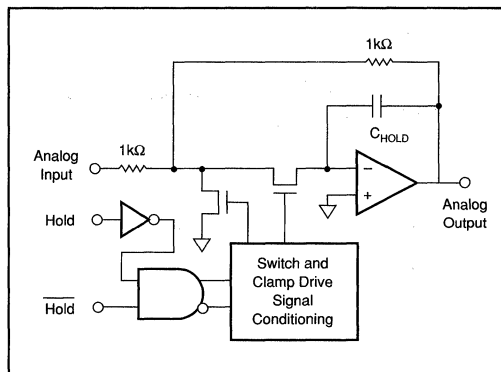
FIGURE 1. Simplified Block Diagram of the SHC702.
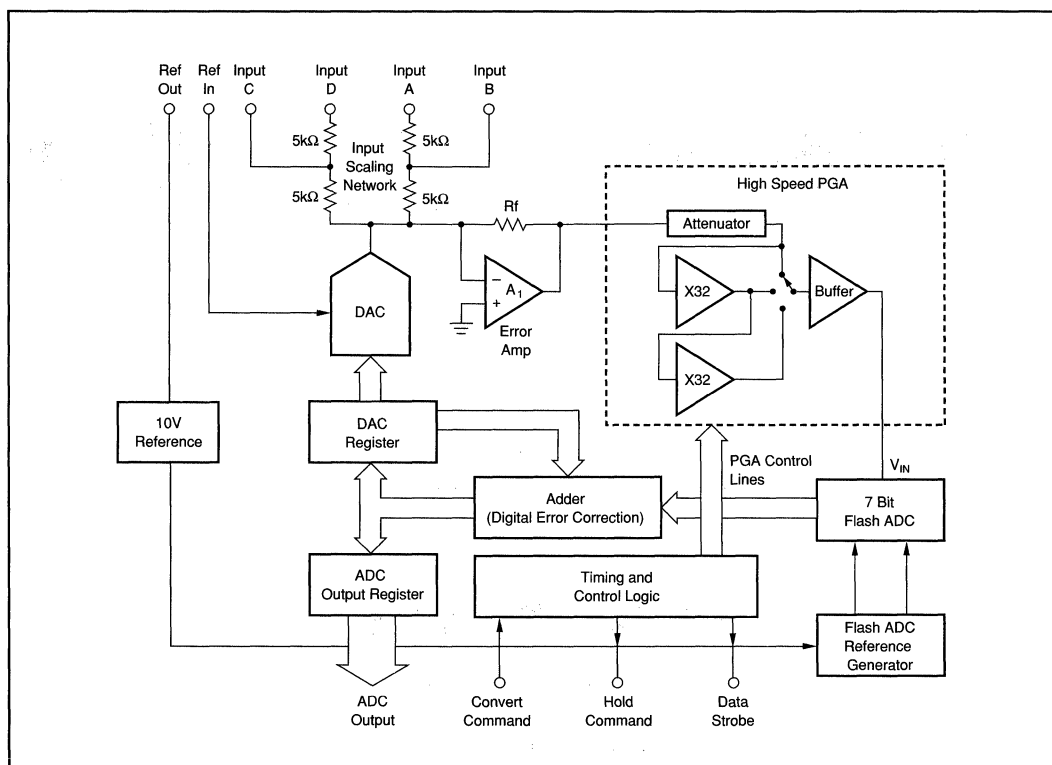
FIGURE 2. Simplified Block Diagram of the ADC701.

At the beginning of each conversion, the DAC is reset to mid-scale so that its output current is exactly 1mA. This 1mA is subtracted from the input signal current. The difference current flows through Rf and appears as an error voltage at the output of A_1.

During the first pass, the programmable gain amplifier (PGA) is set to unity gain, which matches the error voltage range to the input range of the flash ADC. The error signal is digitized to 7-bit resolution by the flash ADC, creating a coarse approximation of the digital output value, which is then applied to the DAC.

Since the DAC output is now approximately equal to the input signal current, the remaining difference current flowing through Rf is small—ideally less than 1/128 of full scale, which is due to the built-in quantizing uncertainty of the 7-bit flash ADC. However, other sources of error (e.g., integral and differential nonlinearity of the flash ADC, gain and offset of the PGA, settling and noise errors throughout the signal path) cause the possible error range to be significantly greater. In fact, the ADC701 is designed to handle remainder signals up to 1/32 of full scale, which is four times the "ideal" value.

Therefore, the PGA is set during the second pass to a gain of 32, allowing the small remainder signal to match the full range of the flash ADC. This is again digitized to 7-bit resolution and added to the previous result to create the "medium" approximation of the input signal. Because the full-scale range of the flash represents 1/32 of the input signal's full range, the 7-bit flash output is shifted right by 5 bits before being added to the original 7-bit "coarse" result, creating a 12-bit word. There is an overlap of two bits because the two least significant bits of the first-pass result correspond to the two most significant bits of the second-pass result. This overlap in the adder is called "digital error correction"—the mechanism that allows nonideal remainders from the first pass to be corrected in the second pass.

The 12-bit approximation is applied once again to the DAC, causing the remaining difference current to become yet smaller. For the third pass, the PGA's gain is increased by another factor of 32, and the remainder is again digitized by the flash ADC.

At this point in the conversion, all of the necessary data has been latched and it is no longer necessary to hold the analog signals from the sample/hold or the DAC. From a systems perspective, the conversion is now complete because the sample/hold is released to begin acquiring the next input sample and the DAC is reset to mid-scale for the next conversion. Meanwhile, the final result from the flash is added to the previous 12-bit result. Again there is a two-bit overlap to allow for error correction. The adder output is monitored to prevent a digital "rollover" condition, so that the ADC clips properly at the signal extremes. The upper sixteen bits of the final adder result are stored in the ADC's output register, ready to be presented in byte-sequential form at the eight output data lines. The overrange or "clip" condition can also be detected externally by monitoring pin 9. Refer to the section on ADC701 Digital I/O for further detail.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC701/SHC702 combination is designed to be easy to use in a wide variety of applications, without sacrificing flexibility of the analog and digital interface.

SHC702 INTERFACE

The connection diagram (Figure 3) shows the basic hookup. At the SHC702 input, the user may opt to connect the built-in FET buffer amplifier. The buffer is most useful in multichannel applications where the signal bandwidth is less than 100kHz. In those applications, it serves to isolate the multiplexer output from the 1kΩ input impedance of the sample/hold. For higher frequency applications and for any system that does not require the very high impedance, best results (lowest noise and distortion) will be achieved by driving the SHC702's analog input directly. If the buffer is not used, its input should be grounded to avoid random noise pickup and saturation of the buffer op-amp.

Only two connections are required between the SHC702 and the ADC701: SHC702 analog output to ADC701 input(s) and the digital Hold Command from the ADC701 to the SHC702. As always, it is best to avoid routing these analog and digital lines along parallel traces. Although the placement of the SHC702 relative to the ADC is not extremely critical, one good approach is to mount the SHC along one end of the ADC package as shown in Figure 4. This minimizes the length of the interconnections and keeps the digital lines well away from sensitive analog signals.

ADC701 INPUT CONNECTIONS

The ADC input network has four separate terminals, allowing many different input ranges. These should be connected as indicated in Table I. Most users will take advantage of the ADC701's built-in reference circuit, which has very low noise and excellent temperature stability. To use the internal reference, it is only necessary to connect pin 36 (Reference Output) to pin 32 (Reference Input). To use an external 10V reference (to cause the ADC gain to track a system reference, for example), pin 36 is left unconnected and the external reference is applied to pin 32. If required, the ADC701 will typically accommodate a five to ten percent variation in the 10V reference. External references should have very low noise to avoid degrading the excellent signal-to-noise ratio (SNR) of the ADC701.

INPUT RANGE	CONNECT V$_{IN}$ TO	CONNECT Ref In TO
0 to +10V	Input A and Input D	—
±10V	Input A	Input D
±5V	Input A and Input B	Input D
−10V to 0	Input A and Input B	Input C and Input D
0 to +5V	Input B and Input C	—

TABLE I. ADC701 Input Connection Table.

NOTES: (1) For lowest distortion at high input frequencies the non-buffered option should be used. If the buffer is not used, its input should be grounded. (2) Shown connected for ±5V input range. Refer to Input Connection Table for other options. (3) If the Clip Detect feature is used, then the signal may be latched with a simple D type flip-flop as shown. See the section on ADC701 Digital I/O for additional applications information. (4) The second octal flip-flop is recommended but optional — it provides added digital signal isolation and buffering, and also permits three-state logic output compatibility. (5) All commons should be connected to the analog ground plane. Refer to the section on "Power and Ground Connections." (6) The Offset Adjust circuit shown provides an adjustment range of approximately ±0.25% FSR.

FIGURE 3. ADC701/SHC702 Connection Diagram.

OFFSET, GAIN AND CONVERSION SPEED ADJUSTMENTS (OPTIONAL)

Adjustment of the reference voltage is the most straightforward way to adjust the ADC gain. For the internal reference, this is accomplished by connecting a 20kΩ potentiometer as shown in Figure 3. This will provide a gain trim range of about ±3%. It is also possible to use external series or parallel resistance in the input network, but that is more cumbersome and usually will degrade the gain stability over temperature due to tempco (temperature coefficient) mismatches among the resistors.

ADC offset may be adjusted by connecting a 500kΩ potentiometer to pins 21 and 22, with the wiper connected through a series 30kΩ resistor to ground as shown in Figure 3. This will provide an offset trim range of approximately ±0.25% FSR. For a larger trim range of offset or gain, it is recommended that trims be accomplished elsewhere in the system.

The Clock Adjust input (pin 18) is intended primarily for small adjustments of the conversion time. However, this will rarely be necessary because the ADC701 is guaranteed to convert up to 512kHz over the specified temperature range without external clock adjustment.

POWER AND GROUND CONNECTIONS

Experience with testing and applying the ADC701 shows that it will perform well in most board layouts, provided that appropriate care is taken with grounding and bypassing.

Power supplies may be shared between the ADC701, SHC702 and other analog circuitry without difficulty. It is recommended that each power pin be locally bypassed to the ground plane with a high quality tantalum capacitor of at least 1μF. If at all possible, power should be derived from well-regulated linear supplies—switching power supplies will require much more effort for proper decoupling and are not recommended for this or any high performance wideband analog system.

The +5V Digital supply pins, though not as sensitive to noise as the +5V Analog pin, should nonetheless be kept as quiet as possible. If the system digital supply is noisy, then it is best to use the system +5V analog supply for all of the +5V connections on the ADC701 and SHC702 rather than trying to separate them. If only one +5V supply is available and it is shared with other system logic, then extra bypassing and/or supply filtering may be required.

The –5V supply will operate with any voltage between –4.75 and –6V. If –5V is not available from the system supplies, then an industry-standard 7905 regulator may be used to derive –5V from the –15V supply.

All ground pins on both the ADC701 and the SHC702 should be connected directly to a common ground plane. This is true for both analog and digital grounds. However, it is also helpful to recognize where the digital ground currents flow in the system, and to provide PC board return paths for potentially troublesome digital currents in addition to the ground plane connections. For example, the ADC701 output

data lines will sink current (statically and/or dynamically) when in the low state. This current comes from the power supply that runs the interface logic, and so must return to that supply's ground. If the ground termination is placed such that this digital current will flow away from the ADC701, then the existing ground plane will suffice to carry the current. On the other hand, if the ground termination must be placed such that the digital current flows across the ADC or SHC layout, then it would be advisable to break the analog ground plane under the package (to stop the flow of current across the package) and to provide a separate trace (several centimeters wide) on another PC board layer to carry the digital return current from pins 11 and 19 to the termination point. If the ADC701 must interface into a fairly noisy digital environment, then another approach is to keep the first layer of latches and/or buffers connected to the ADC701 power and ground planes, so that the ADC itself is connected to "quiet" circuits with short return paths. This transfers the interface problem to the outputs of the latches, where it can be managed with less impact on the analog components.

PHYSICAL INSTALLATION

The packages may be soldered directly into a PC board or mounted in low-profile machined pin sockets with good results. Use of tall (long lead length) sockets, adapters or headers is not recommended unless a local ground plane and bypass capacitors can be mounted directly under the packages.

In a room-temperature environment or inside an enclosure with moderate airflow, the ADC701 and SHC702 normally do not require heat-sinking. However, to keep the devices running as cool as possible, it is helpful to install a thin heat-transfer plate under the packages to conduct heat into the ground plane. The plate may be made from metal (copper, aluminum or steel) or from a special heat-conductive material such as Sil-Pad[1]. The Sil-Pad material has the advantage of being electrically insulating and somewhat pliable, so that it will tend to distribute pressure evenly and conform to the package—an advantage in systems where the board may be flexed or subjected to vibration.

PC BOARD LAYOUT

An optimized layout has been designed for the DEM-ADC701-E demonstration fixture. For information concerning the demo board and the layout, contact your local sales representative.

ADC701 DIGITAL I/O

Refer to the timing diagram, Figure 4. The conversion process is initiated by a rising edge on the Convert Command input. This will immediately bring the sample/hold command output to a logic high state (Hold mode).

After the ADC701 conversion is completed (approximately 1.5µs after the convert command edge), the Sample/Hold Command falls to a low state, enabling the sample/hold to begin acquisition of the next input sample. However, the ADC701 internal clock continues to run so that the output data may be processed.

There are two methods of reading data from the ADC:

1. Strobed Output—This will usually be the easiest and fastest method. The data are presented sequentially as high and low bytes of the total 16-bit word. The sequence High-Low or Low-High is controlled by the state of the High/Low Byte Select input. The first byte is valid on the rising edge of the Data Strobe output; the second byte is valid on the falling edge.

2. Polled output—With this method, data strobes will occur as described above, but they are ignored by the user. Instead, the user waits until the Data Strobe output falls, and then manually selects high and low output data by means of the High/Low Byte Select input. This polling procedure may be carried out during the subsequent ADC conversion cycle, but two precautions must be observed: First, the user should avoid switching the High/Low Byte Select immediately before or after the next convert command. This will prevent digital switching noise from coupling into the system at the instant of analog sampling. Second, the polling sequence must be completed before the ADC begins to strobe out data from the subsequent conversion.

OPTIONS FOR STROBED OUTPUT

There are several ways in practice to implement the logic interface. Figure 3 shows the simplest configurations. In order to convert the ADC701's byte-sequential data into 16-bit parallel form, the minimum requirement is for one single octal flip-flop, such as a 74HC574 or equivalent. This will latch the first byte on the rising edge of the ADC701 Data Strobe. Then the second byte becomes valid, and all 16 bits may be strobed to the outside system on the falling edge of the Data Strobe.

For better noise isolation of the ADC701 from the digital system, or if full three-state capability is required for the 16 output lines, a second octal flip-flop can be added as shown in the dashed lines of Figure 3. This will also require an inverter to convert the falling Data Strobe edge into a rising clock edge for the second flip-flop IC.

If it is desirable to have all 16 output lines change simultaneously (for example when driving a D/A converter), then a third octal flip-flop (not shown in Figure 3) may be added to re-latch the output of the first byte. By driving that device's clock also from the inverted Data Strobe, fully synchronous switching of the 16 output bits will be achieved.

USING THE CLIP DETECT OUTPUT

The ADC701 provides a built-in Clip Detect signal on pin 9 which indicates an ADC overrange or underrange condition. The Clip Detect signal is only valid when the High Byte becomes valid as shown in Figure 4. Therefore, the simplest way to latch the Clip Detect signal is to provide an extra flip-flop which is clocked on the same strobe edge as the High Byte flip-flop. Such a setup is illustrated in Figure 3. The Clip Detect signal remains at logic 0 under normal conditions, and indicates a clip condition by rising to a logic 1.

NOTES: (1) Setup Time 28ns min, 37ns typ. (2) Hold Time 30ns min, 73ns typ. (3) High Byte refers to ADC bits 1–8, the most significant 8 bits. Also, the Clip Detect signal on pin 9 is valid simultaneously with High Byte. (4) Low Byte refers to ADC bits 9–16, the least significant bits.
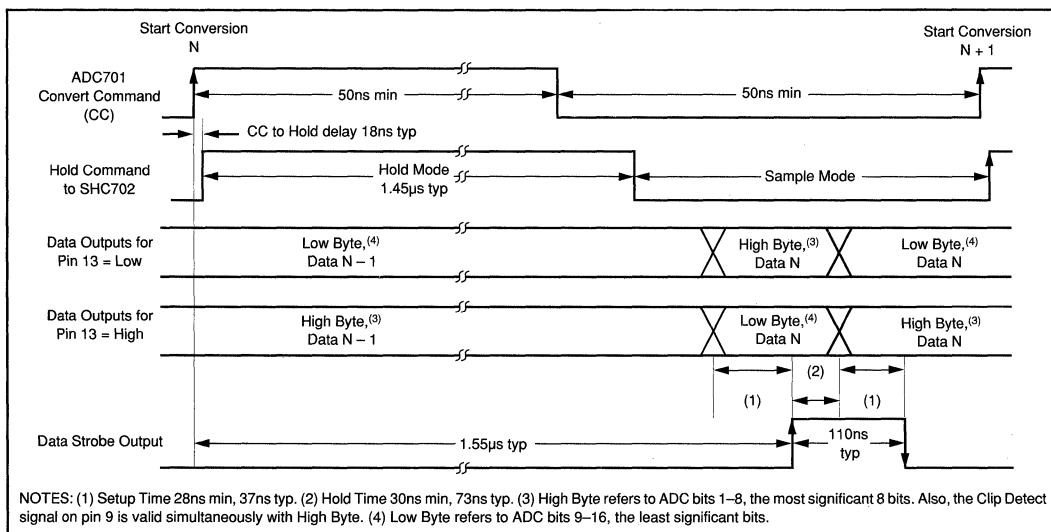
FIGURE 4. ADC701 Interface Timing Diagram.

The latched version of Clip Detect may be used to generate an interrupt to the user's system computer, which would then launch a service routine to generate the appropriate alarms or corrective action. Another possible application would be to stretch the pulse using a monostable so that it would be easily visible when driving an LED warning lamp.

In some systems, it may be desirable to provide separate latched outputs for Underrange and Overrange. These conditions may be separately detected by using simple logic to implement the boolean equations:

Underrange = Clip Detect AND $\overline{\text{Anybit}}$

Overrange = Clip Detect AND Anybit

where "Anybit" is any one of the data output bits.

The Underrange and Overrange signals would then be latched into two separate flip-flops. A simple solution using a single '74 dual flip-flop and a single '00 quad NAND provides enough logic to implement the logic equations, with a spare NAND gate left over to use for creating the inverted Data Strobe signal.

USING THE ADC701 AT MAXIMUM CONVERSION RATES

The ADC701 is guaranteed to accept Convert commands at a rate of DC to 512kHz over the specified operating temperature range. At a conversion rate of 500kHz, the total throughput time of 2µs allows for the 1.5µs ADC conversion time plus 500ns for the digital output timing and sample/hold acquisition time.

If the user tries to exceed the maximum conversion rate by a large amount, the Convert Command of conversion N+1 will occur before the Data Strobe has fallen from conversion N. In such a situation, the ADC701 will simply ignore every other Convert command so the actual conversion rate will become half of the Convert command rate. Otherwise, the conversion will proceed normally. Note that the ADC timing slows down at high temperatures, so the frequency at which this occurs will vary with temperature—although it is still guaranteed to be greater than 512kHz over the specified temperature range.

Another consideration for operation at very high rates is that the sample/hold acquisition time becomes shorter as the conversion rate is increased. Users will note that the available acquisition time becomes less than 550ns at rates above 500kHz, which is less than the typical SHC702 acquisition time for a 10V step to 150µV accuracy. However, the signal degradation is gradual as the acquisition time is shortened— even at 512kHz, there is enough time to acquire a 5V step to better than 500µV. Also, most signal processing environments do not contain full-power signals at the Nyquist frequency, but rather show a rolloff of signal power at high frequencies. If the ability to acquire extremely large input changes at extremely high conversion rates is of paramount importance, the user may elect to use a Burr-Brown model SHC803 sample/hold instead—it is pin compatible with the SHC702 and provides much faster acquisition time at the expense of some extra noise and higher distortion at low input frequencies.

TESTING THE ADC701/SHC702

The ADC701 and SHC702 together form a very high performance converter system and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digital output is the best method of examining system performance. Attempts to evaluate the system by analog reconstruction through a D/A converter will usually prove unsatisfactory; assuming that the static and dynamic distortions of the D/A can be brought below the required level (–110dB), the performance will still be beyond the range of presently available spectrum analyzers.

Even when the analysis is done using FFT techniques, several key issues must be addressed. First, the parameters of the FFT need to be adequate to perform the analysis and extract meaningful data. Second, the proper selection of test frequencies is critical for good results. Third, the limitations of commercial signal generators must be considered. These three points are addressed in later sections. Finally, the test board layout must follow the recommendations discussed on pages 8 through 10.

DYNAMIC PERFORMANCE DEFINITIONS

1. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to 3rd order)}}{\text{Sinewave Signal Power}}$$

4. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}}$$

IMD is referred to the larger of the test signals f_1 or f_2—**not** to the total signal power, which would result in a number approximately 6dB "better." The zero frequency bin (DC) is not included in these calculations—it represents total offset of the ADC, SHC and test equipment and is of little importance in dynamic signal processing applications.

ADC701/SHC702

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FFT Parameters

Accurate FFT analysis of 16-bit systems requires adequate computing hardware and software. The FFT length (number of points) should be relatively large—at least 4K and preferably 16K or larger. There are several reasons for this:

1. The converter itself has 64K codes. Ideally, the test would guarantee that all codes are tested at least once. Practically speaking, however, that would require immensely long FFTs (>>64K points) or averaging of a large number of smaller FFTs. By using an FFT length of 4K or greater and proper selection of the test frequencies, a very good statistical picture of the ADC performance will be obtained which shows the effect of any defects in the transfer function.

2. The noise floor of the output spectrum is not low enough if less than 4K points are taken. Shorter FFTs have fewer bins to cover the output spectrum, so a larger fraction of the total system noise appears in each bin. Although the SNR of the ADC701/SCH702 system is in the range of −93dB, the noise level of the available generators may increase the total measured noise power to −80dB. Every doubling of the FFT length will spread the noise power among twice as many bins, resulting in a 3dB reduction of the spectral noise floor. In order to resolve spurious components that are at the level of −110dB, an average noise floor of less than −113dB would be barely adequate. This requires at least 2048 bins in the output half-spectrum, corresponding to a 4K-point FFT. Even at this level, it will be difficult or impossible to separate higher order harmonics in the ADC701 response from the average noise level, indicating that longer FFTs are desirable.

3. Following the guidelines for test frequency selection which are outlined in the next section, it becomes clear that longer FFTs allow a much wider choice of test frequencies without concern for sophisticated data windowing or code coverage problems.

Besides the consideration of FFT length, it is important to realize that the FFT calculations must be performed with high-precision arithmetic. The use of 32-bit fixed or floating point calculations will generally be inadequate because the noise floor due to calculation errors alone will interfere with the ADC performance data. Unfortunately, this consideration precludes the use of most DSP accelerator boards and similar hardware. In order to preserve the full dynamic range of the ADC output, it is best to use standard 64- or 80-bit arithmetic. To avoid excessively long calculation times, the FFT algorithm should be written in an efficiently compiled language and make use of techniques such as trigonometric look-up tables in software and dedicated floating-point coprocessors in hardware. There are several commercial software packages available from Burr-Brown and others that meet these requirements.

SELECTION OF TEST FREQUENCIES

The FFT (and any similar DSP operation) treats the total time-domain record length as one cycle of an infinitely long periodic signal. Therefore, if the end of the sampled record does not match up smoothly with the beginning, the output spectrum will contain serious errors known as leakage or truncation error[2]. This well-known problem is usually handled by applying a windowing function to the time-domain samples, suppressing the worst effects of the mismatch. However, the most often used windows such as Hanning, Hamming, raised cosine, etc., are completely inadequate for 16-bit ADC testing. More sophisticated functions such as the four-sample Blackman-Harris window[3] will provide much better results, although there still will be obvious spreading of the spectral lines.

The most successful approach is to eliminate the need for windowing by properly selecting the test signal frequency (or frequencies) in relation to the ADC sampling frequency[4]. If the time sample contains exactly an integer number of cycles, then there is no mismatch or truncation error. Another point to consider is that the sampling frequency should not be an exact integer multiple of the signal frequency, which would tend to reduce the number of different ADC codes that are tested and also tend to artificially concentrate quantization error in the harmonics of the test signal.

Both of these criteria are met by choosing an FFT length which is a power of two (the most standard and fastest to compute) and choosing a test frequency which causes an exact **odd** integer number of cycles to appear in the time record. In software, this selection can be accomplished very easily:

1. Determine the desired sampling frequency f_S.

2. Determine the desired input signal frequency f_{APPROX}.

3. Determine the FFT length N, which should be a power of 2 (e.g., 4096 or 16384).

4. Divide f_{APPROX} by f_S, multiply the quotient by N, and round the result to the nearest odd integer. This is M, the number of cycles in the time record.

5. Multiply M by f_S and divide by N to obtain the exact input signal frequency f_{ACTUAL}.

SIGNAL GENERATOR CONSIDERATIONS

To suppress leakage effects, the calculated ratio of f_S to f_{ACTUAL} must be precisely maintained during the test. This requirement is met easily by the use of synthesized signal generators whose reference oscillators can be locked together. Other possible approaches include external phase locking of non-synthesized generators and direct digital synthesis techniques. If it is not possible to use phase-locked signals, then a Blackman-Harris window may be used as mentioned previously.

Another key issue is the purity of both the signal and sampling frequency generators. The sampling clock's phase noise (jitter) will act as another source of SNR degradation. This is not serious as long as the jitter is random and the noise sidebands contain no sharp peaks. The HP3325 synthesizer is suitable for this purpose. The input signal generator will require more attention because its distortion will usually be greater than that of the ADC701/SHC702. Presently, the lowest distortion synthesized generator is the Brüel & Kjær Model 1051 (or 1049). This is suitable for testing the system in the audio range. The upper frequency limit of the B&K synthesizer is 200kHz. Above 20kHz, the distortion becomes a limiting factor, and low-pass filters must be inserted into the signal path to reduce the harmonic and spurious content.

As noted previously, the combined noise contributions of the signal generator and sampling clock generator far exceed the SNR of the ADC701/SHC702 itself. The SNR has been measured separately by applying a highly filtered sinewave to the input, resulting in typical SNR performance of –93dB. However, the filters employed to achieve this low-noise test stimulus are found to cause reactive loading of the signal source which results in increased distortion. Therefore it is best to separate the tests for SNR from those for THD and IMD, unless a suitably pure **and** low-noise signal can be generated.

Figures 5 and 6 show block diagrams of FFT test setups for the ADC701 and SHC702, summarizing the placement of the major components discussed above. The Typical Dynamic Performance section shows typical results obtained from testing the ADC701/SHC702 at a 500kHz conversion rate, using 16K samples for the FFT analysis.
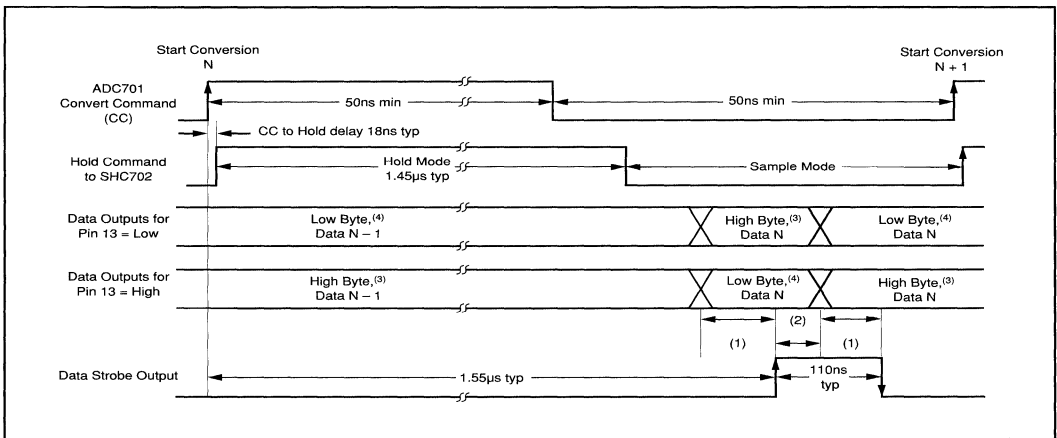
FIGURE 5. FFT Test Configuration for Single-Tone Testing.
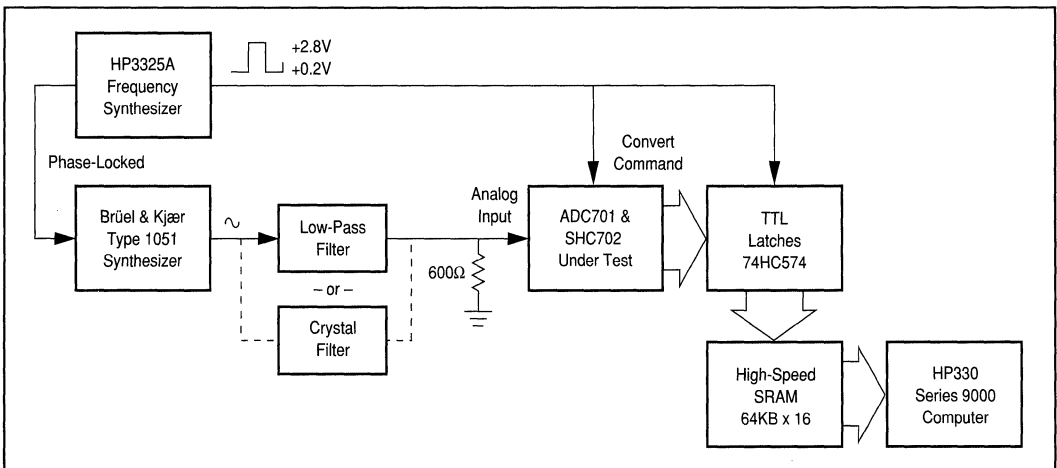
FIGURE 6. FFT Test Configuration for Two-Tone (Intermodulation) Testing.

ADC701/SHC702

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

HISTOGRAM TESTING

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral nonlinearity of the SHC and ADC. The influence of differential linearity errors is harder to distinguish in a spectral plot—it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity (DL) performance is by using the popular histogram test method [5]. Application of the histogram test to the ADC701/ SHC702 is relatively straightforward, though once again extra precision is required for a 16-bit system compared to 8- or 12-bit systems. Basically, this means that a very large number of samples are required to build an accurate statistical picture of each code width. If a histogram is taken using only one million points, then the average number of samples per code is less than fifteen. This is inadequate for good statistical confidence, and the resulting DL plot will look considerably worse than the actual performance of the converter. In practice 10 to 20 million samples will demonstrate good results for a 16-bit system and expose any serious flaws in the DL performance. If the memory incrementing hardware can keep pace with the ADC701, then 20 million samples can be accumulated in well under one minute. The last figure on page six shows the results of a 19.6 million point histogram taken at an input frequency of 1kHz.

NOTES:

1. Available from Bergquist, 5300 Edina Industrial Blvd., Minneapolis, MN 55435 (612) 835-2322.

2. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.

3. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.

4. Halbert, Joel M. and Belcher, R. Allan, "Selection of Test Signals for DSP-Based Testing of Digital Audio Systems", Journal of the Audio Engineering Society, Vol. 34, No. 7/8, July/August, 1986, pp 546-555.

5. "Dynamic Tests for A/D Converter Performance", Application Note AN-133, Burr-Brown Corporation, Tucson, AZ, 1985.

BURR - BROWN®
BB
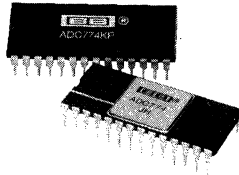
ADC774

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-835.

ADC774

2

Microprocessor-Compatible
ANALOG-TO-DIGITAL CONVERTER

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FEATURES

● **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, or 16-BIT MICROPROCESSOR BUS INTERFACE**

● **ALTERNATE SOURCE FOR HI774 A/D CONVERTER: 8.5μs Conversion Time, 150ns Bus Access Time**

● **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**

● **NO MISSING CODES OVER TEMPERATURE:**
  0°C to +75°C: ADC774J, K
  –55°C to +125°C: ADC774SH, TH

DESCRIPTION

The ADC774 is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC per-

formance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 8.5μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC774, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or a hermetic side-brazed ceramic DIP.

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH			ADC774K, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	3.75	5	6.25	*	*	*	kΩ
±10V, 0V to +20V	7.5	10	12.5	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			*	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(Adjustable to Zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1] : J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} <+16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} <−13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} <+5.5V			±1/2			*	LSB
CONVERSION TIME [4,5]							
8-Bit Cycle		5	5.3		*	*	µs
12-Bit Cycle		7.5	8.5		•	•	µs
OUTPUTS							
DIGITAL (DB11 – DB0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH			ADC774K, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10	+10.1	*	*	*	V
Source Current Available for External Loads [6]	2.0			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	–11.4		–16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

*Same specification as ADC774JH, JP, SH.

NOTES: (1) With fixed 50Ω resistor from Ref Out to Ref In. This parameter is also adjustable to zero at +25C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range FS means 20V; for a 0V to +10V range, FS means 10V. The term Full Scale for these specification instead of Full-Scale Range is used to be consistent with other vendors' specifications tables. (3) Using internal reference. (4) See "Controlling the ADC774" section for detailed information concerning digital timing. (5) The Harris HI-774 uses a subranging/error correction technique that allows one to begin conversion before a preceding sample-hold or multiplexer has settled to ±1/2LSB. For 12-bit accurate conversions, the input transient to the ADC774 must settle to less than ±1/2LSB before conversion is started. The ADC774 is compatible with HI-774 in all other respects. (6) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION

ADC774

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common .... 0V to +16.5V
V_{EE} to Digital Common .... 0V to −16.5V
V_{LOGIC} Digital Common .... 0V to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
 to Digital Common .... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, 10V_{IN})
 to Analog Common .... ±16.5V
20V_{IN} to Analog Common .... ±24V
Ref Out .... Indefinite Short to Common,
 Momentary Short to V_{CC}
Max Junction Temperature .... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) .... +300°C
Thermal Resistance, θ_{JA} : Ceramic .... 50°C/W
 Plastic .... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC774s. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

 Plastic "-BI" models: +85°C
 Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g. ADC774KP-BI). See Ordering Information for pricing.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC774JP	28-Pin Plastic DIP	215
ADC774KP	28-Pin Plastic DIP	215
ADC774JH	28-Pin Ceramic DIP	149
ADC774KH	28-Pin Ceramic DIP	149
ADC774SH	28-Pin Ceramic DIP	149
ADC774TH	28-Pin Ceramic DIP	149
ADC774JP-BI	28-Pin Plastic DIP	215
ADC774KP-BI	28-Pin Plastic DIP	215
ADC774JH-BI	28-Pin Ceramic DIP	149
ADC774KH-BI	28-Pin Ceramic DIP	149
ADC774SH-BI	28-Pin Ceramic DIP	149
ADC774TH-BI	28-Pin Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})
ADC774JP	Plastic DIP	0°C TO +75°C	±1LSB
ADC774KP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC774JH	Ceramic DIP	0°C to +75°C	±1LSB
ADC774KH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC774SH	Ceramic DIP	−55°C to +125°C	±1LSB
ADC774TH	Ceramic DIP	−55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMP (160 HOURS)[1]
ADC774JP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC774KP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC774JH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC774KH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC774SH-BI	Ceramic DIP	−55°C to +125°C	+125°C
ADC774TH-BI	Ceramic DIP	−55°C to +125°C	+125°C

CONTROLLING THE ADC774

This is an abridged data sheet. For Discussion of Specifications, Installation, Calibration refer to ADC574A data sheet or order PDS-835.

The Burr-Brown ADC774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A$_O$, R/$\overline{C}$, and CE) are all TTL-/CMOS-compatible. The functions of the control inputs are described in Table I. The control function truth table is listed in Table II.

Read footnote 5 to the Electrical Specifications table if using ADC774 to replace the HI-774.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A$_O$ are connected to digital common and CE and 12/$\overline{8}$ are connected to V$_{LOGIC}$ (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

FIGURE 1. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.
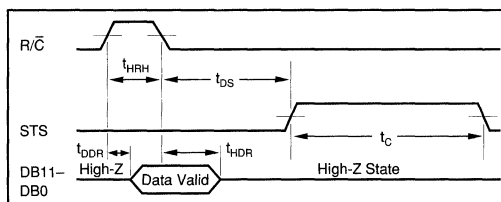
FIGURE 2. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A$_O$ (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A$_O$ selects 8-bit (A$_O$ = "1") or 12-bit (A$_O$ = "0") conversion mode. When reading output data in two 8-bit bytes, A$_O$ = "0" accesses 8 MSBs (high byte) and A$_O$ = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A$_O$ line.

TABLE I. ADC774 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A$_O$	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. Control Input Truth Table.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t$_{HRL}$	Low R/$\overline{C}$ Pulse Width	50			ns
t$_{DS}$	STS Delay from R/$\overline{C}$			200	ns
t$_{HDR}$	Data Valid After R/$\overline{C}$ Low	25			ns
t$_{HS}$	STS Delay After Data Valid		150	375	ns
t$_{HRH}$	High R/$\overline{C}$ Pulse Width	150			ns
t$_{DDR}$	Data Access Time			150	ns

TABLE III. Stand-Alone Mode Timing.

Figure 1 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 2 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table III.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_O input, which is latched upon receipt of a conversion start transition (described below). If A_O is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_O is low. If all 12 bits are read following an 8-bit conversion, the 3 LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_O is latched because it is also involved in enabling the output buffers. No other control inputs are latched.
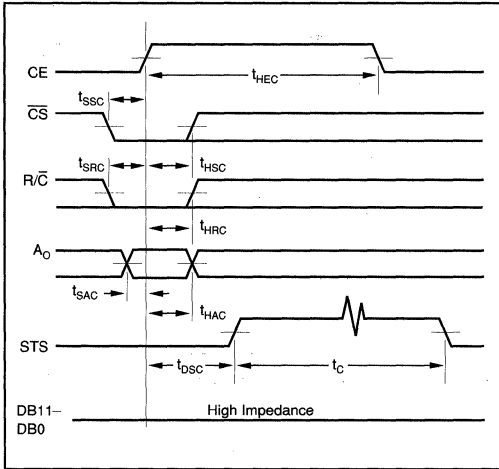
FIGURE 3. Conversion Cycle Timing.
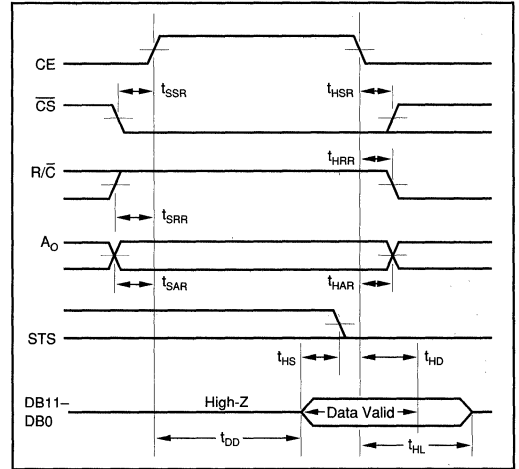
FIGURE 4. Read Cycle Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_O to CE setup	0			ns
t_{HAC}	A_O valid during CE high	50	20		ns
t_C	Conversion time				
	12-bit cycle at 25°C		7.5	8.5	µs
	0 to +75°C			9.0	µs
	−55°C to +125°C			9.5	µs
	8-bit cycle at 25°C		5	5.3	µs
	0 to +75°C			5.6	µs
	−55° to +125°C			6	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_O valid after CE low	50			ns
t_{HS}	STS delay after data valid		150	375	ns

TABLE IV. Timing Specifications.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occuring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table II. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 3. The specifications for timing are contained in Table IV.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 4 and Table IV for timing relationships and specifications.

ADC774

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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ADC803

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-493.

High Speed
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **12-BIT RESOLUTION**
- **LINEARITY ERROR: ±0.12%, max
  (C Grade)**
- **NO MISSING CODES: –55°C to +125°C
  (S Grade)**
- **HIGH SINAD RATIO: 72dB**
- **LOW HARMONIC DISTORTION: –73dB**
- **CONVERSION TIME: 500ns, 8 Bits**
  670ns, 10 Bits
  1.5µs, 12 Bits

DESCRIPTION

The ADC803 is a high speed hybrid successive approximation analog-to-digital converter utilizing laser-trimmed thin film components.

It is complete with internal reference, clock, and comparator, and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5µs.

With user-adjusted conversion time set at 1µs, ±1LSB accuracy can be achieved. The gain and offset errors may be externally trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to –10V, ±5V, and ±10V.

Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.

PDS-493D

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SPECIFICATIONS

At +25°C, rated power supplies, 1.5μs conversion time, and after 6-minute warm-up, unless otherwise noted.

PARAMETER	ADC803CM MIN	TYP	MAX	ADC803BM MIN	TYP	MAX	ADC803SM MIN	TYP	MAX	UNITS
RESOLUTION			12			12			12	Bits
INPUTS										
ANALOG										
Voltage Ranges: Bipolar		±5, ±10			*			*		V
Unipolar		0 to −10			*			*		V
Impedance: −10V to 0V, ±5V		1.4			*			*		kΩ
±10V		2.4			*			*		kΩ
DIGITAL										
Convert Command	Negative pulse 50ns wide (min) trailing edge (0 to 1) initialtes conversion.									
Logic Loading			4			*			*	TTL Loads
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error [1]		±0.04	±0.1		±0.08	±0.2		±0.04	±0.1	%
Offset Error[1]: Unipolar		±0.05	±0.2		±0.07	±0.3		*	*	% of FSR[2]
Bipolar		±0.02	±0.1		*	±0.2		*	*	% of FSR
Linearity Error:										
1.5μs Conversion Time		±0.009	±0.012			±0.020		±0.012	±0.015	% of FSR
1.0μs Conversion Time		±0.015	±0.020		±0.020					% of FSR
Differential Linearity Error:										
1.5μs Conversion Time		±0.012	±0.015			±0.020		*	*	% of FSR
1.0μs Conversion Time			±0.024		±0.024			*		% of FSR
Inherent Quantization Error		1/2			*			*		LSB
POWER SUPPLY SENSITIVITY										
Gain and Offset: +15VDC		±0.0036			*			*		% of FSR/%V$_{CC}$
−15VDC		±0.0005			*			*		% of FSR/%V$_{CC}$
+5VDC		±0.001			*			*		% of FSR/%V$_{DD}$
Conversion Time: +15VDC		±0.7			*			*		%/%V$_{CC}$
−15VDC		None			*			*		%/%V$_{CC}$
+5VDC		±0.8			*			*		%/%V$_{DD}$
CONVERSION TIME										
Factory Set	1.3		1.5	*		*	*		*	μs
Range of Adjustments	0.8		2.2	*		*	*		*	μs
DRIFT										
Gain		±10	±30		±15	*		*	*	ppm of FSR/°C
Offset: Unipolar		±2	±7		±3	*		*	*	ppm of FSR/°C
Bipolar		±3	±10		±5	*		*	*	ppm of FSR/°C
Linearity Error										
−25°C to +85°C:										
1.5μs Conversion Time		±0.012	±0.018			±0.024			*	% of FSR
1.0μs Conversion Time		±0.015			±0.020				*	% of FSR
−55°C to +125°C:										
1.7μs Conversion Time, max[4]								±0.015	±0.024	% of FSR
Differential Linearity Error										
−25°C to +85°C:										
1.5μs Conversion Time		±0.012	±0.018			±0.024				% of FSR
1.0μs Conversion Time		±0.015			±0.024					% of FSR
−55°C to +125°C:										
1.7μs Conversion Time, max[4]		±0.1						±0.015	±0.024	% of FSR
Conversion Time					*			*		% of FSR
No Missing Code Temp. Range:										
1.5μs Conversion Time	−25		+85	*		*				°C
1.7μs Conversion Time, max[4]							−55		+125	°C
OUTPUT										
DIGITAL DATA										
Parallel										
Output Codes: Unipolar	Complementary Straight Binary			*			*			
Bipolar	Bipolar Offset Binary			*			*			
Output Drive	6			*			*			TTL Loads
Status	Logic "1" During Conversion			*			*			
Status Output Drive	6			*			*			TTL Loads
Internal Clock										
Clock Output Drive	3			*			*			TTL Loads
Frequency (without external clock adj.)		8			*			*		MHz

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ADC803

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

At +25°C, rated power supplies, 1.5µs conversion time, and after 6-minute warm-up, unless otherwise noted.

PARAMETER	ADC803CM MIN	ADC803CM TYP	ADC803CM MAX	ADC803BM MIN	ADC803BM TYP	ADC803BM MAX	ADC803SM MIN	ADC803SM TYP	ADC803SM MAX	UNITS
POWER SUPPLY REQUIREMENTS										
Power Consumption										
Rated Voltage: Analog (±V$_{CC}$)	±14.25	±15	±15.75	*	*	*	*	*	*	VDC
Digital (V$_{DD}$)	+4.75	+5	+5.25	*	*	*	*	*	*	VDC
Supply Drain: +15V		+27	+32		*	*		*	*	mA
−15V		−38	−55		*	*		*	*	mA
+5V		+180	+210		*	*		*	*	mA
TEMPERATURE RANGE (Ambient)										
Specification	−25		+85	*		*	−55		+125	°C
Storage	−55		+125	*		*	*		*	°C

* Same specification as for ADC803CM.

NOTES: (1) Adjustable to zero. See Optional Gain and Offset Adjustment section. (2) FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR. (3) See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle. (4) Conversion time is factory-set at approximately 1.4µs at +25°C. As temperature increases, the conversion time increases. At +125°C the conversion time will be no more than 1.7µs. No Missing Codes is guaranteed over −55°C to +125°C provided the conversion time is allowed to increase with temperature.

ADC803 dynamic performance characteristics are described in a report titled "Analogue-to-Digital Converter Performance Tests Using the Fast Fourier Transform" by R. A. Belcher, University College of Swansea, Wales, UK. (available from Burr-Brown on letterhead request).

CONNECTION DIAGRAM

NOTE: (1) Serial data is not guaranteed.
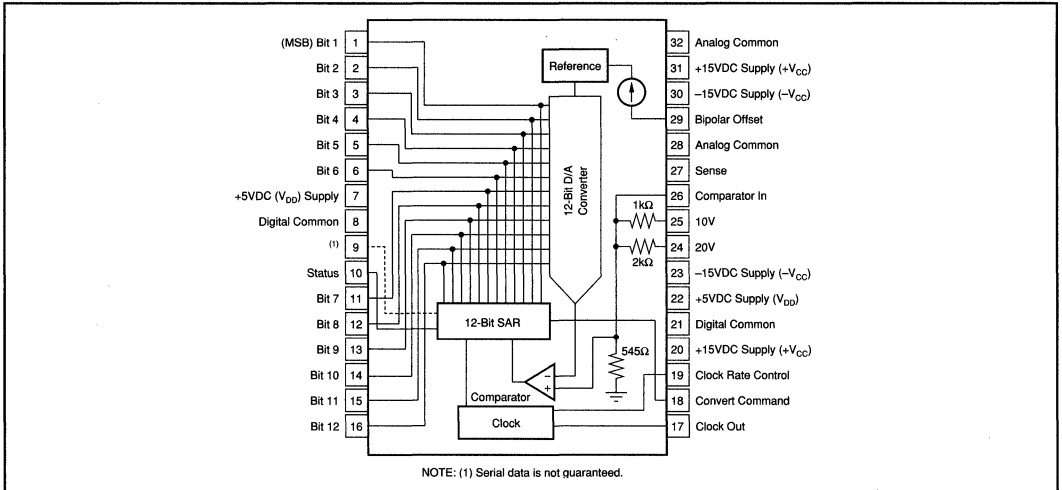
ORDERING INFORMATION

ADC803   X   M   Q

Basic Model Number

Performance Grade Code
- B, C = −25°C to +85°C
- S = −55°C to +125°C

Package Code
- M = Metal DIP

Reliability Screening
- Q = Q-Screened

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage To Analog Common .... ±18V
Digital Supply Voltage To Digital Common .... +7V
Digital Controls Inputs .... +5.5V
Analog Inputs .... ±15V
Operating Temperature: Ambient .... +125°C
                    Case .... +135°C
Storage Temperature .... +125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC803	32-Pin Metal	116

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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ADC7802

ADC7802

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- ● **TOTAL UNADJUSTED ERROR ≤ 1/2LSB OVER FULL TEMPERATURE RANGE**
- ● **FOUR-CHANNEL INPUT MULTIPLEXER**
- ● **LOW POWER: 10mW plus Power Down Mode**
- ● **SINGLE SUPPLY: +5V**
- ● **FAST CONVERSION TIME: 8.5μs Including Acquisition**
- ● **AUTOCAL: No Offset or Gain Adjust Required**
- ● **UNIPOLAR INPUTS: 0V to 5V**
- ● **MICROPROCESSOR-COMPATIBLE INTERFACE**
- ● **INTERNAL SAMPLE/HOLD**

DESCRIPTION

The ADC7802 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. An autocalibration cycle, occurring automatically at power on, guarantees a total unadjusted error within ±1/2LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part very easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADC7802 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial −40°C to +85°C temperature range.

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SPECIFICATIONS
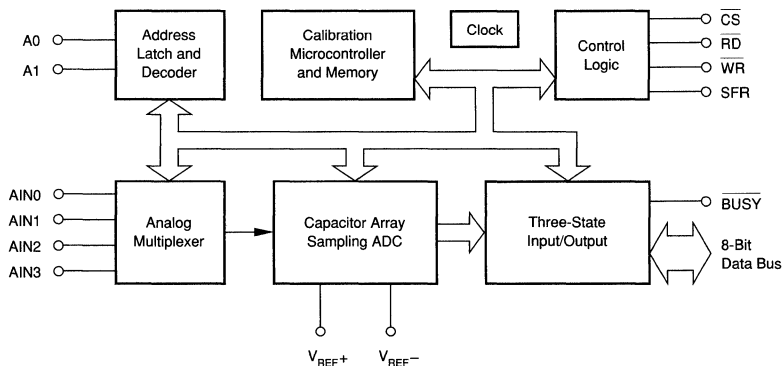
ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_A \geq V_D \geq V_{REF}+$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external with 50% duty cycle, $T_A = -40°C$ to $+85°C$, after calibration cycle at any temperature; unless otherwise specified.

PARAMETER	CONDITIONS	ADC7802BP/ADC7802BN			UNITS
		MIN	TYP	MAX	
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = 25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \leq V_A$			5	V
$V_{REF}-$				0	V
For Derated Performance: [1] $V_{REF}+$		4.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	μA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz, 50% Duty Cycle			8.5	μs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz, 50% Duty Cycle			17	μs
	CLK = 500kHz, 50% Duty Cycle			34	μs
With Internal Clock Using	$T_A = +25°C$			10	μs
Recommended Clock Components	$T_A = -40°C$ to $+85°C$		10		μs
Analog Signal Bandwidth [2]			500		Hz
Slew Rate [2]		8			mV/μs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
ACCURACY					
Total Adjusted Error, [3] All Channels				±1/2	LSB
Differential Nonlinearity				±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels			±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	μA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	μA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	μA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA
DIGITAL OUTPUTS					
V_{OL}	$I_{SINK} = 1.6mA$			0.4	V
V_{OH}	$I_{SOURCE} = 200μA$	4			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_D			±1	μA
Output Capacitance	High-Z State	4		15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY} = HIGH$		10		mW
Power Down Mode	See Table III, Page 9		50		μW
TEMPERATURE RANGE					
Specification		−40		+85	°C
Storage		−65		+150	°C

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 4.5V, the total error will typically not exceed ±1LSB. (2) Faster signals can be accurately converted by using an external sample/hold in front of the ADC7802. (3) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground 6.5V
V_D to Digital Ground 6.5V
Pin V_A to Pin V_D .... ±0.3V
Analog Ground to Digital Ground .... ±1V
Control Inputs to Digital Ground .... −0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground .... −0.3V to V_D + 0.3V
Maximum Junction Temperature .... 150°C
Internal Power Dissipation 875mW
Lead Temperature (soldering, 10s) .... +300°C
Thermal Resistance, θ_{JA}: Plastic DIP .... 75°C/W
　　　　　　　　　　　PLCC .... 75°C/W

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC7802BN	28-Pin PLCC	251
ADC7802BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE, °C	PACKAGE
ADC7802BN	±1/2	−40 to +85	PLCC
ADC7802BP	±1/2	−40 to +85	Plastic DIP

ADC7802

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN CONFIGURATIONS

Top View   **DIP**

Left pin	#		#	Right pin
SFR	1		28	V_A
AIN0	2		27	AGND
AIN1	3		26	$\overline{CAL}$
AIN2	4		25	A1
AIN3	5		24	A0
$V_{REF}+$	6		23	CLK
$V_{REF}-$	7		22	$\overline{BUSY}$
DGND	8		21	HBE
V_D	9		20	$\overline{WR}$
D7	10		19	$\overline{CS}$
D6	11		18	$\overline{RD}$
D5	12		17	D0
D4	13		16	D1
D3	14		15	D2

Top View   **LCC**

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	$V_{REF}+$	Positive voltage reference input. Normally +5V. Must be $\leq V_A$.
7	$V_{REF}-$	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be $\leq V_A$ and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$.)
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal/external clock operation. For external clock operation, connect pin 23 to a 74 HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 A0 Selected Channel LOW LOW AIN0 LOW HIGH AIN1 HIGH LOW AIN2 HIGH HIGH AIN3
26	$\overline{CAL}$	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be $\geq V_D$ and $V_{REF}+$.

TYPICAL PERFORMANCE CURVES

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, unless otherwise specified.

CHANNEL SEPARATION vs FREQUENCY

CODE TRANSITION NOISE

SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY

POWER SUPPLY REJECTION vs FREQUENCY

INTERNAL CLOCK FREQUENCY vs TEMPERATURE

INTERNAL CLOCK FREQUENCY vs R_{CLOCK}

ADC7802

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

THEORY OF OPERATION

ADC7802 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator. This allows offset errors to be corrected during the acquisition phase of each conversion cycle.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by a microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. This is faster than a complex digital error correction system, which could slow down the throughput rate. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADC7802 to most micro-controllers, microprocessors or digital storage systems.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADC7802 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 (BUSY) will output a LOW during the conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles, during which the comparator offset is also auto-zeroed to below 1/4LSB of error. The successive approximation conversion takes place during clock cycles 6 through 17.
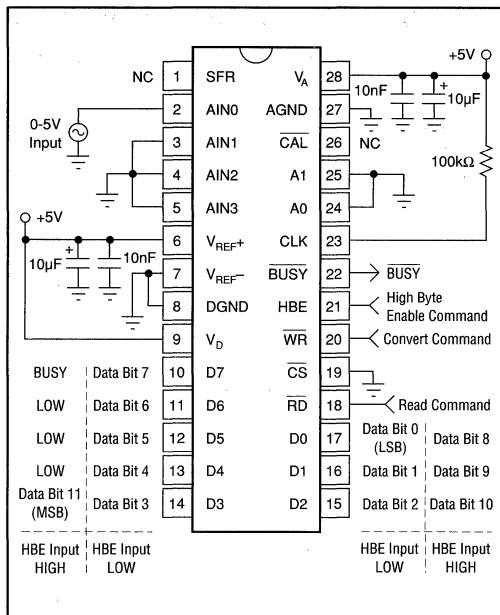
FIGURE 1. Basic Operation.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages and reference voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

READING DATA

Data from the ADC7802 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADC7802 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.
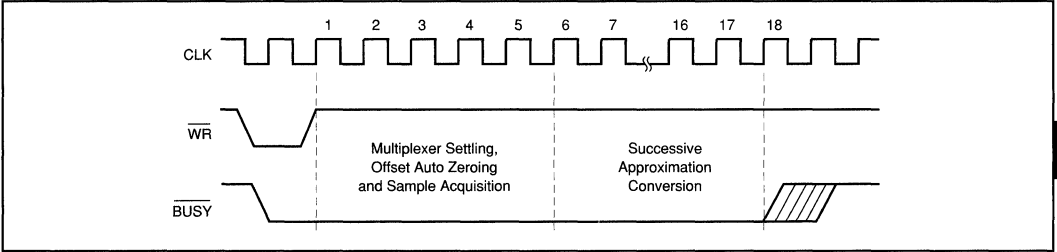
FIGURE 2. Converter Timing.
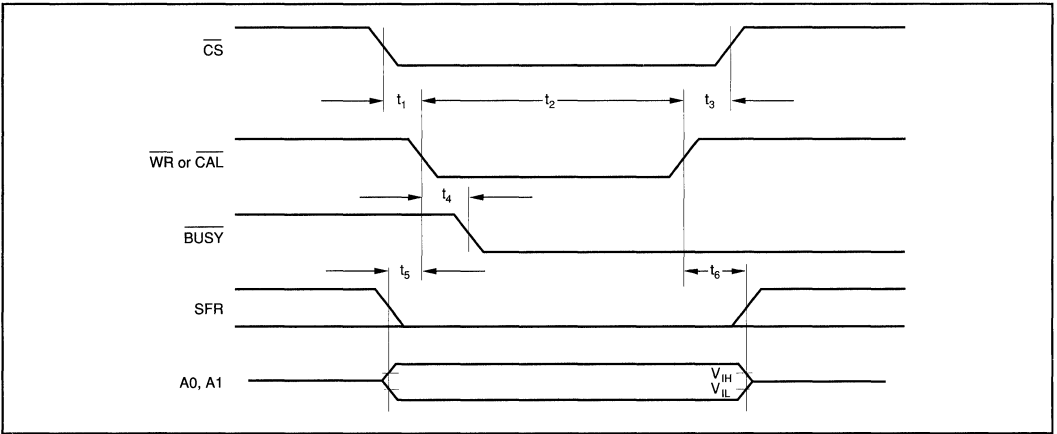
FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).
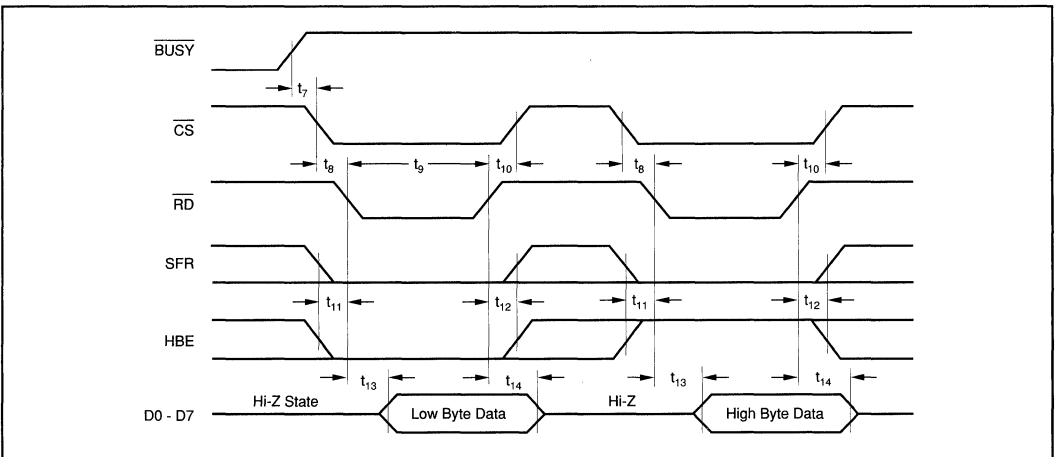
FIGURE 4. Read Cycle Timing.

TRANSPARENT MODE

This is the default mode for ADC7802. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 and LOWs to D1 to D7 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 8 show the digital timing of ADC7802 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADC7802, or to write additional instructions to the converter. Access to the Special Function Register is made by driving SFR HIGH.

SYMBOL	PARAMETER [1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time [2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time [2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time [2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time [2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time) [3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time) [3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR [3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL} = 20$ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal $\overline{RD}$ pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal $\overline{WR}$ pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 7 and 8 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 1MHz external, $T_A = -40°C$ to +85°C).
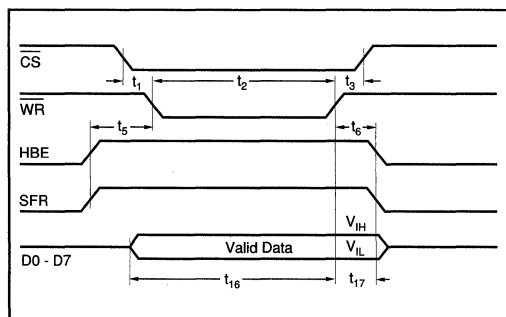
FIGURE 5. Writing to the SFR.
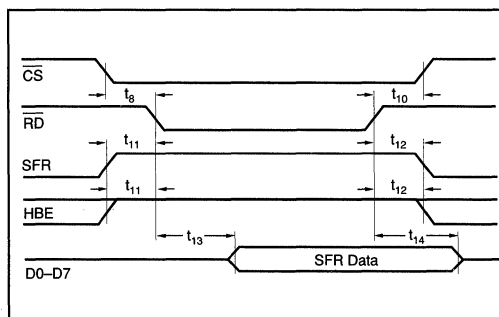
FIGURE 6. Reading the SFR.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH as shown in Figure 4.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADC7802 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

Writing a HIGH to D3 in the FSR puts the ADC7802 in the Power Down Mode. Power consumption is reduced to 50μW and D3 remains HIGH. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) The timing is shown in Figure 3. Note that writing to the SFR also initiates a new conversion.

CONTROL LINES

Table IV shows the functions of the various control lines on the ADC7802. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, Latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2		Reserved for factory use.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occured during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

	$\overline{CS}/\overline{WR}$	SFR/HBE	D0	D1	D3	D5	D7	D2/D4/D6
Enables Transparent Mode for Data Latches.	LOW	HIGH	LOW	X	LOW	X	LOW	LOW
Enables Latched Output Mode for Data Latches.	LOW	HIGH	HIGH	X	LOW	X	LOW	LOW
Initiates Calibration Cycle.	LOW	HIGH	X	HIGH	LOW	X	LOW	LOW
Resets Power Fail flag.	LOW	HIGH	X	X	LOW	LOW	LOW	LOW
Activates Power Down Mode.	LOW	HIGH	X	X	HIGH	X	LOW	LOW

NOTES: (1) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down. (2) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D2, D3, D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	BUSY	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle.
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

ADC7802

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

INSTALLATION

INPUT BANDWIDTH

From the typical performance curves, it is clear that ADC7802 can accurately digitize signals up to 500Hz, but distortion will increase beyond this point. Input signals slewing faster than 8mV/μs can degrade accuracy. This is a result of the high-precision auto-zeroing circuit used during the acquisition phase. For applications requiring higher signal bandwidth, any good external sample/hold, like the SHC5320, can be used.

INPUT IMPEDANCE

ADC7802 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.
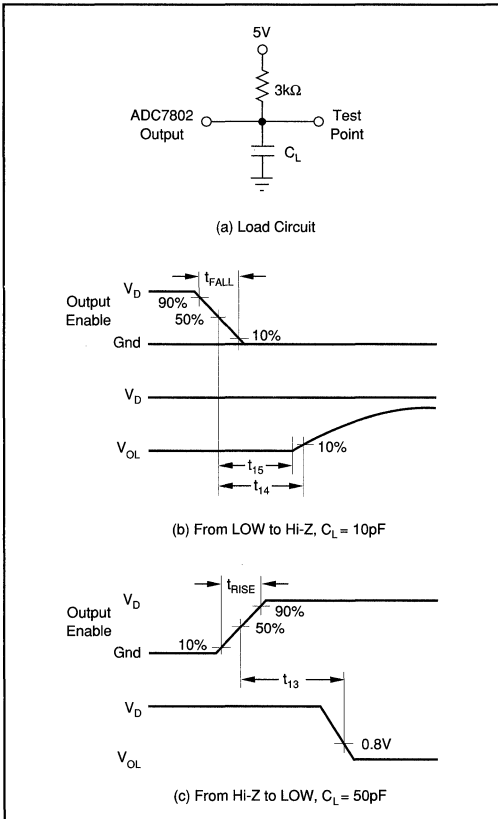
FIGURE 7. Measuring Active LOW to/from Hi-Z State.
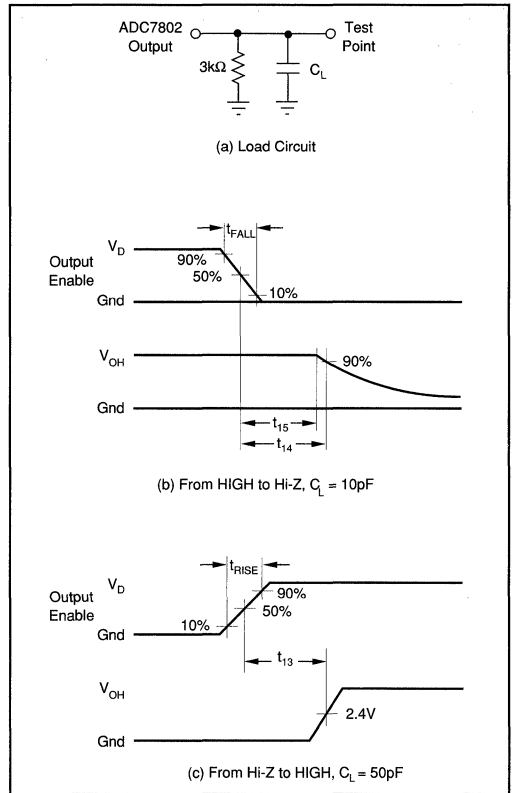
FIGURE 8. Measuring Active HIGH to/from Hi-Z State.

In many applications, a simple passive low-pass filter as shown in Figure 9a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 9a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 9b should be used.
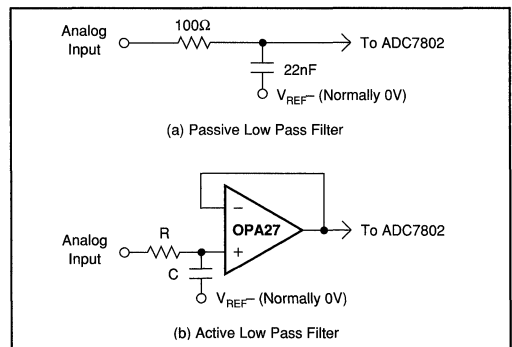
FIGURE 9. Input Signal Conditioning.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADC7802, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a $1k\Omega$ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A $10\mu F$ tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADC7802 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 2.5V and $V_{REF}-$ as high as 1V. As long as there is at least a 2.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ± 1LSB. (1/2LSB for a 5V span is $610\mu V$, which is 1LSB for a 2.5V span.)

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADC7802 should be bypassed with $10\mu F$ tantalum capacitors as close to the part as possible. Although ADC7802 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 10 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADC7802 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADC7802, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The $V_{REF}-$ pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADC7802 clock from an external source is shown in Figure 11a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The minimum pulse width of the external clock must be 200ns. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.2MHz.

INTERNAL CLOCK OPERATION

Figure 11b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.
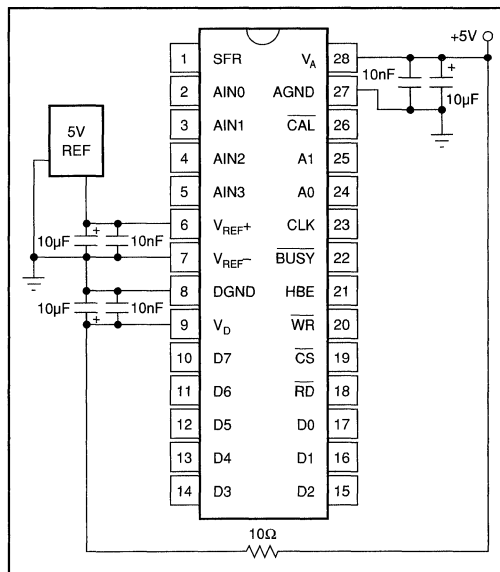
FIGURE 10. Power Supply and Reference Decoupling.
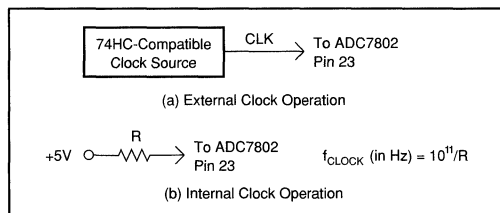
FIGURE 11. Internal Clock Operation.

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The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in many applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 12 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802, using a precision, low-cost complete difference amplifier, INA105.
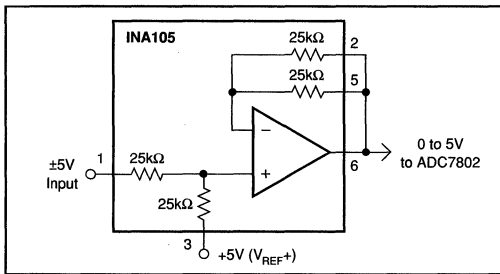
FIGURE 12. ±5V Input Range.

Figure 13 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802. The precision of this circuit will depend on the matching and tracking of the three resistors used.
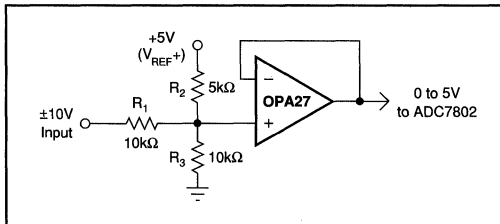
FIGURE 13. ±10V Input Range.

To trim this circuit for full 12-bit precision, R2 and R3 need to be adjustable over appropriate ranges. To trim, first have the ADC7802 converting continually and apply +9.9927V (+10V − 1.5LSB) at the input. Adjust R3 until the ADC7802 output toggles between the codes FFE hex and FFF hex. This makes R3 extremely close to R1. Then, apply −9.9976V (−10V + 0.5LSB) at the input, and adjust R2 until the ADC7802 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases.

More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADC7802, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 14 shows a typical interface to Motorola microprocessors, while Figure 15 shows how the result can be placed in register D0.
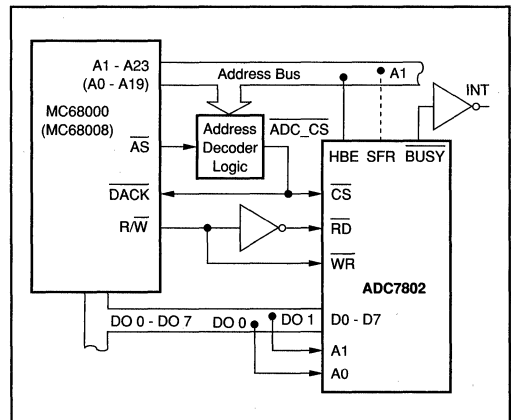
FIGURE 14. Interface to Motorola Microprocessors.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the DO register, as shown in Figure 15. The address decoder must pull down ADC_CS at ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 16 shows a typical interface to Intel.

A conversion is initiated by a write instruction to address ADC_CS. Data pins DO0 and DO1 select the analog input channel. The BUSY signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the ADC_CS address fetches the Low byte, and a read instruction from the ADC_CS address +2 fetches the High byte.

FIGURE 15. Conversion Results in Motorola Register D0.

FIGURE 16. Interface to Intel Microprocessors.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN ®

ADS574

Microprocessor-Compatible Sampling CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **COMPATIBLE WITH ADC574**

● **COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE**

● **FAST ACQUISITION AND CONVERSION: 25µs max**

● **ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS**

● **GUARANTEED AC AND DC PERFORMANCE**

● **SINGLE +5V SUPPLY OPERATION**

● **LOW POWER: 100mW max**

● **PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC**

DESCRIPTION

The ADS574 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574 models in most applications, with internal sampling, much lower power consumption, and capability to operate from a single +5V supply.

The ADS574 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time for 12-bit conversions is 25µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS574 is available in both commercial (0°C to +70°C) and military (–55°C to +125°C) ranges, and requires +5V, with –12V or –15V optional, depending on usage. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic or hermetic ceramic DIPs, and 28-pin SOICs.

PDS-1104D

BURR - BROWN ®

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = +5V$, $V_{EE} = -15V$ to $+5V$, sampling frequency of 40kHz, $f_{IN} = 10kHz$; unless otherwise specified.

PARAMETER	ADS574JE/JH/JP/JU/AU/SF/SH/D MIN	TYP	MAX	ADS574KE/KH/KP/KU/TF/TH MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	15	21		*	*		kΩ
±10V, 0V to +20V	60	84		*	*		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1]							
(adjustable to zero)			±0.25			*	% of FS [2]
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
T_{MIN} to T_{MAX} [3]							
Linearity Error: A, J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error: A, J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Unipolar Offset: A, J, K Grades			±4			±3	LSB
S, T Grades			±4			±3	LSB
Bipolar Offset: A, J, K Grades			±12			±5	LSB
S, T Grades			±14			±6	LSB
No Missing Codes Resolution	12			12			Bits
AC ACCURACY [4]							
Spurious Free Dynamic Range	73	78		76	*		dB
Total Harmonic Distortion		−77	−72		*	−75	dB
Signal-to-Noise Ratio	69	72		71	*		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	*		dB
Intermodulation Distortion		−75			*		
($F_{IN1} = 10kHz$, $F_{IN2} = 11.5kHz$)							
TEMPERATURE COEFFICIENTS [5]							
Unipolar Offset		±1			*		ppm/°C
Bipolar Offset		±2			*		ppm/°C
Full-Scale Calibration		±12			*		ppm/°C
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration [6]							
$+4.75V < V_{DD} < +5.25V$		±1/2			*		LSB
CONVERSION TIME (Including Acquisition Time)							
$t_{AQ} + t_C$ at 25°C:							
8-Bit Cycle		16	18		*	*	µs
12-Bit Cycle		22	25		*	*	µs
12-Bit Cycle, T_{MIN} to T_{MAX}		22	25		*	*	µs
SAMPLING DYNAMICS							
Sampling Rate	40			*			kHz
Aperture Delay, t_{AP}							
With $V_{EE} = +5V$		20			*		ns
With $V_{EE} = 0V$ to $-15V$		4.0			*		µs
Aperture Uncertainty (Jitter)							
With $V_{EE} = +5V$		300			*		ps, rms
With $V_{EE} = 0V$ to $-15V$		30			*		ns, rms

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = +5V$, $V_{EE} = -15V$ to $+5V$, sampling frequency of 40kHz, $f_{IN} = 10kHz$; unless otherwise specified.

PARAMETER	ADS574JE/JH/JP/JU/AU/SF/SH/D MIN	TYP	MAX	ADS574KE/KH/KP/KU/TF/TH MIN	TYP	MAX	UNITS
OUTPUTS							
DIGITAL (DB$_{11}$ - DB$_0$, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} [(7)]	–16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} [(7)] (V_{EE} = –15V)		–1			*	*	mA
I_{DD}		+13	+20		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX})							
(V_{EE} = 0V to +5V)		65	100		*	*	mW
TEMPERATURE RANGE							
Specification: J, K Grades	0		+70	*		*	°C
A Grade	–40		+85	*		*	°C
S, T Grades	–55		+125	*		*	°C
Operating: A, J, K Grades	–40		+85	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

*Same specification as ADS574JE/JH/JP/JU/SF/SH.
NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at T_{MIN} and T_{MAX}. (4) Based on using V_{EE} = +5V, which starts a conversion immediately upon a convert command. Using V_{EE} = 0V to –15V makes the ADS574/ADS774 emulate standard ADC574 operation. In this mode, the internal sample/hold acquires the input signal after receiving the convert command, and does not assume that the input level has been stable before the convert command arrives. (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

DICE INFORMATION

ADS574 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	V_{DD}	15	Digital Common
2	12/$\overline{8}$	16	DB0 (LSB)
3	$\overline{CS}$	17	DB1
4	A$_0$	18	DB2
5	R/$\overline{C}$	19	DB3
6	CE	20	DB4
7	NC	21	DB5
8	2.5V Ref Out	22	DB6
9A, 9B	Analog Common	23	DB7
10	2.5 Ref In	24	DB8
11	V_{EE} (Mode Control)	25	DB9
12	Bipolar Offset	26	DB10
13	10V Range	27	DB11 (MSB)
14	20V Range	28	Status

Substrate Bias: +V_{DD}
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	172 x 142 ±5	4.37 x 3.61 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 40kHz; unless otherwise specified. All plots use 4096 point FFTs.

FREQUENCY SPECTRUM (±10V, 2kHz Input)

S/(N + D) = 73.1dB
THD = −94.5dB
SNR = 73.1dB

SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE

−55°C
+125°C
+25°C

FREQUENCY SPECTRUM (±10V, 19kHz Input)

S/(N + D) = 68.4dB
THD = −75.9dB
SNR = 69.3dB

FREQUENCY SPECTRUM (±1V, 19kHz Input)

S/(N + D) = 53.3dB
THD = −74.5dB
SNR = 53.3dB

SPURIOUS FREE DYNAMIC RANGE, SNR AND THD
vs INPUT FREQUENCY

POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY

ADS574

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

CONNECTION DIAGRAM

*Not Internally Connected

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common .... $+V_{DD}$ to $-16.5V$
V_{DD} to Digital Common .... 0V to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_O, $12/\overline{8}$, $R/\overline{C}$)
  to Digital Common .... $-0.5V$ to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$)
  to Analog Common .... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V
Ref Out.. Indefinite Short to Common,
                                                         Momentary Short to V_{DD}
Max Junction Temperature .... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) .... +300°C
Thermal Resistance, θ_{JA} : Ceramic DIPs .... 50°C/W
                                     Plastic DIPs .... 100°C/W
                                     SOIC .... 100°C/W

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS574JE	0.3" Plastic DIP	246
ADS574KE	0.3" Plastic DIP	246
ADS574JP	0.6" Plastic DIP	215
ADS574KP	0.6" Plastic DIP	215
ADS574JU	SOIC	217
ADS574KU	SOIC	217
ADS574SF	0.3" Ceramic DIP	247
ADS574TF	0.3" Ceramic DIP	247
ADS574SH	0.6" Ceramic DIP	149
ADS574TH	0.6" Ceramic DIP	149
ADS574JH	0.6" Ceramic DIP	149
ADS574KH	0.6" Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	SINAD[1]	TEMPERATURE RANGE	LINEARITY ERROR
ADS574JE	0.3" Plastic DIP	68	0°C to +70°C	±1LSB
ADS574KE	0.3" Plastic DIP	70	0°C to +70°C	±1/2LSB
ADS574JP	0.6" Plastic DIP	68	0°C to +70°C	±1LSB
ADS574KP	0.6" Plastic DIP	70	0°C to +70°C	±1/2LSB
ADS574JU	SOIC	68	0°C to +70°C	±1LSB
ADS574KU	SOIC	70	0°C to +70°C	±1/2LSB
ADS574SF	0.3" Ceramic DIP	68	−55°C to +125°C	±1LSB
ADS574TF	0.3" Ceramic DIP	70	−55°C to +125°C	±1/2LSB
ADS574SH	0.6" Ceramic DIP	68	−55°C to +125°C	±1LSB
ADS574TH	0.6" Ceramic DIP	70	−55°C to +125°C	±1/2LSB
ADS574JH	0.6" Ceramic DIP	68	0°C to +70°C	±1LSB
ADS574KH	0.6" Ceramic DIP	70	0°C to +70°C	±1/2LSB

NOTE: (1) SINAD is Signal to (Noise and Distortion) expressed in dB.

THEORY OF OPERATION

In the ADS574, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_c is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_c is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G". Similarly, the second

approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum circuit required to operate the ADS574 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS574 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS574.

The ADS574 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS574 is designed to complete a conversion and accurately acquire a new signal in 25µs max over the full operating temperature range, so that conversions can take place at a full 40kHz.

CONTROLLING THE ADS574

The Burr-Brown ADS574 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to +5V. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

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FIGURE 2. Basic ±10V Operation.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output			Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:		±10V	+5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ $n = 8$ $n = 12$		$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (− Full-Scale Calibration)		+10V − 3/2LSB 0 − 1/2LSB −10V + 1/2LSB	+5V − 3/2LSB 0 − 1/2LSB −5V + 1/2LSB	+10V − 3/2LSB +5V − 1/2LSB 0 to +1/2LSB	+10V − 3/2LSB ±10V − 1/2LSB 0 to +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be LOW ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS574 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS574 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

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FIGURE 3. R/$\overline{\text{C}}$ Pulse Low—Outputs Enabled After Conversion.
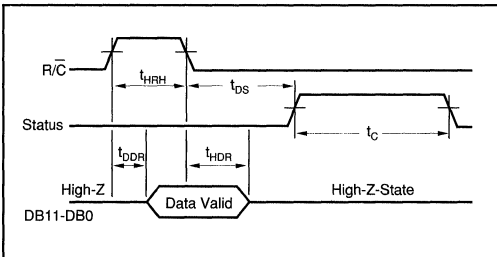
FIGURE 4. R/$\overline{\text{C}}$ Pulse High — Outputs Enabled Only While R/$\overline{\text{C}}$ Is High.

S/H CONTROL MODE AND ADC574 EMULATION MODE

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode it is assumed that during the required 4µs acquisition time the signal is not slewing faster than the slew rate of the ADS574. No assumption is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command.

This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized by the internal sample/hold circuit, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, no assumption is made about the input signal prior to the convert command. A delay time is introduced between the convert command and the start of conversion to allow the ADS574 enough time to acquire the input signal before converting. The delay increases the effective aperture time from 0.02µs to 4µs, but allows the ADS574 to replace the ADC574 in any circuit. Any slewing of the analog input prior to the convert command in existing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{\text{C}}$ Pulse Width	25			ns
t_{DS}	STS Delay from R/$\overline{\text{C}}$			200	ns
t_{HDR}	Data Valid After R/$\overline{\text{C}}$ Low	25			ns
t_{HRH}	High R/$\overline{\text{C}}$ Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{\text{CS}}$ to CE setup	50	20		ns
t_{HSC}	$\overline{\text{CS}}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{\text{C}}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{\text{C}}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{\text{CS}}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{\text{C}}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{\text{CS}}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{\text{C}}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STC delay after data valid	300	400	1000	ns

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).
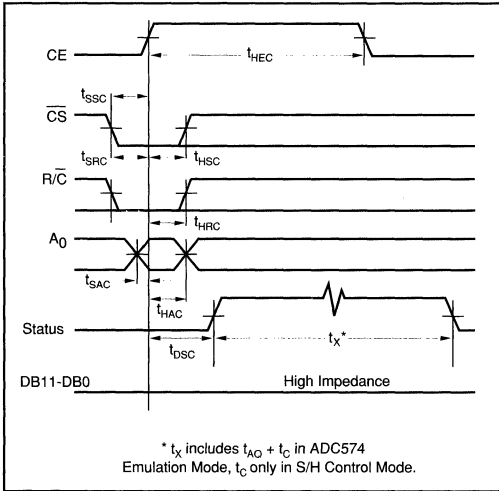
FIGURE 5. Conversion Cycle Timing.
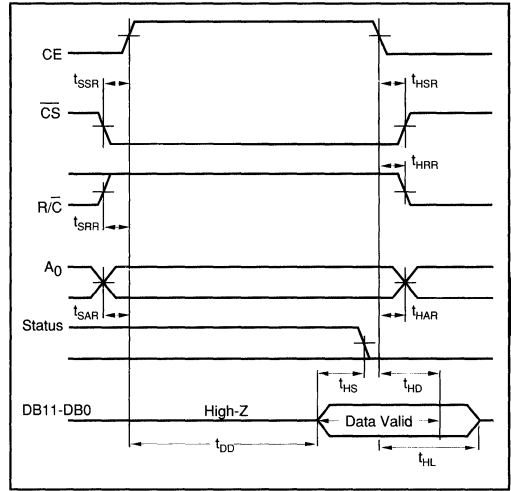
FIGURE 6. Read Cycle Timing.

		Word 1									Word 2							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4		DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

FIGURE 8. Connection to an 8-Bit Bus.

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systems (due to multiplexers, sample/holds, etc. in front of the converter) does not affect the accuracy of the ADS574 conversion in the Emulation Mode.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

Basically, the Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS574 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The Emulation Mode allows the ADS574 to be dropped into almost all existing ADC574 sockets without changes to any other existing system hardware or software. The input to the ADS574 in the Emulation Mode does not need to be stable before a convert command is received, so that multiplexers, programmable gain amplifiers, etc., can be slewing quickly any time before a convert command is given as long as the analog input to the ADS574 is stable after the convert command is received, as it needs to be in existing ADC574 systems for accurate operation. In fact, even in the Emula-

tion Mode, system throughput can be speeded up, since the input to the ADS574 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC574s.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS574, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

SYMBOL	PARAMETER	S/H CONTROL MODE (Pin 11 Connected to +5V)			ADC574 EMULATION MODE (Pin 11 Connected to 0V to –15V)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		22	25		22	25	µs
	8-bit Conversions		16	18		16	18	µs
t_C	Conversion Time:							
	12-bit Conversions		18			18		µs
	8-bit Conversions		12			12		µs
t_{AQ}	Acquisition Time		4			4		µs
t_{AP}	Aperture Delay		20			4000		ns
t_J	Aperture Uncertainty		0.3			30		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.
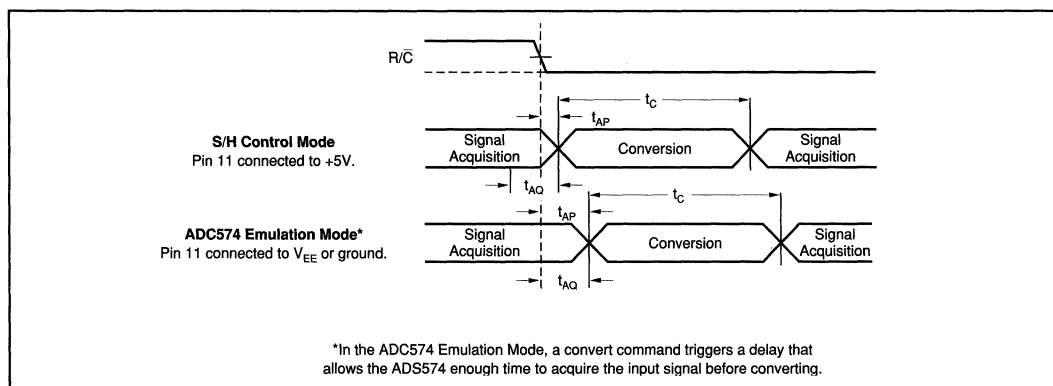
FIGURE 9. Signal Acquisition and Conversion Timing.
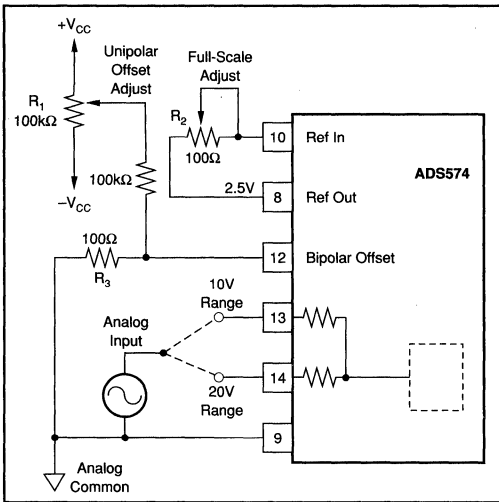
FIGURE 10. Unipolar Configuration.
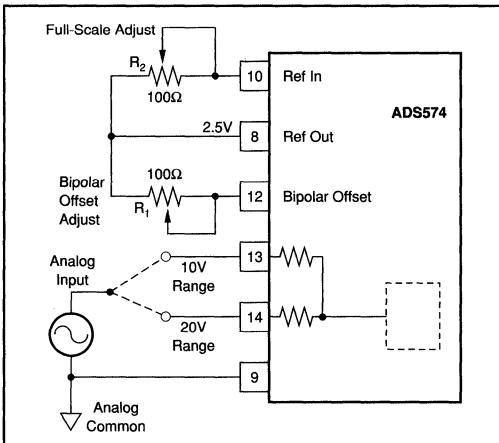
FIGURE 11. Bipolar Configuration.

If the 10V analog input range is used (either bipolar or unipolar), the 20V range input (pin 14) should be shielded with ground plane to reduce noise pickup.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS574.

POWER SUPPLY DECOUPLING

On the ADS574, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC574 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC574 socket, the –15V on pin 11 selects the ADC574 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS574 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out) or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS574 is typically 84kΩ in the 20V ranges and 21kΩ in the 10V ranges. This is significantly higher than that of traditional ADC574 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS574. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high imped-
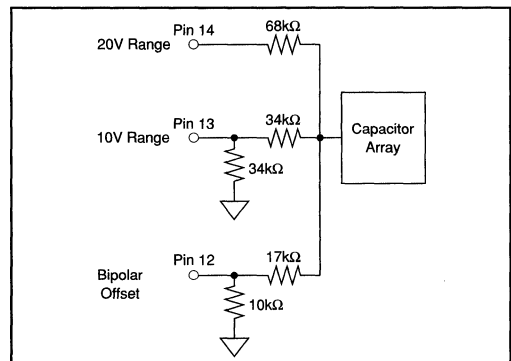
FIGURE 12. ADS574 Input Structure.

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ance node as compared with traditional ADC574 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS574 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected to analog common pin 9. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (68kΩ + 68kΩ || 17kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide offset adjust response the same as that of traditional ADC574 architectures without needing to change the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS574 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is where +12V or +15V is supplied on traditional ADC574s. Pin 11, the –12V or –15V supply input on traditional ADC574s, is used only as a logic input on the ADS574. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS574, and this resistor will add 10mW to 15mW to the power consumption of the ADS574 when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS574 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS574 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R$_2$ in Figure 10 with a 50Ω, 1% metal film resistor, omitting the other adjustment components. Connect pin 12 to pin 9.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R$_1$ until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R$_2$ until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, replace the potentiometers in Figure 11 by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R$_1$ for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R$_2$ for DB0 to toggle ON and OFF with all other bits ON.

BURR - BROWN®

ADS602

12-Bit 1MHz Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES
● **LOW LINEARITY ERROR**
● **SAMPLE RATE: 1MHz**
● **INPUT RANGES: ±5V, 0V to +10V**
● **COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference**
● **32-PIN CERAMIC DIP PACKAGE**

APPLICATIONS
● **DIGITAL SIGNAL PROCESSING**
● **HIGH-SPEED DATA ACQUISITION SYSTEMS**
● **MEDICAL INSTRUMENTATION**
● **ANALYTICAL INSTRUMENTATION**
● **TEST AND IMAGING SYSTEMS**
● **WAVEFORM ANALYZERS**

DESCRIPTION

The ADS602 is a high-speed successive approximation analog-to-digital converter with internal sample/hold amplifier. This unique design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADS602 is thoroughly tested for dynamic performance.

The ADS602 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Sample rate is set at the factory to 1MHz. Performance is guaranteed with no missing

codes over the input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

The user can switch between unipolar (0V to +10V) and bipolar (±5V) operation through one digital logic level input.

Output codes are available in complementary binary for unipolar inputs and complementary offset binary for bipolar inputs.

All digital input and output are TTL-compatible. Power supply requirements are ±15V and +5V.

BURR-BROWN®

ADS602

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 1MHz sampling rate, $\pm V_{CC}$ = $\pm$15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale (FSR) [1, 2]	−5		+5	*		*	V
Unipolar	Full Scale (FSR) [1, 2]	0		+10	*		*	V
Input Resistance			1			*		kΩ
Input Capacitance			5	10		*	*	pF
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error [3, 4]			±0.2	±0.3		±0.1	±0.2	% of FSR
Input Offset Error [3, 4]: Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.2	1.5		0.9	1.25	LSB
Differential Linearity Error			1.2	1.5		0.9	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain	$\Delta \pm V_{CC}$ = $\pm$10%		±0.0036	0.5		*	*	%FSR/%V_{CC}
	$\Delta \pm V_{DD}$ = $\pm$10%		±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	$\Delta +V_{DD}$ = $\pm$5%		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level ≈ −0.5dB, unless otherwise stated.)								
Differential Linearity Error[5]	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.6			0.5		LSB
	100% of All Codes		1.2			0.9	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		−74			−86	−76	dB
	f_C = 480kHz		−68			−73	−70	dB
Total Harmonic Distortion[6]	f_C = 10kHz		−79			−83	−75	dBc
	f_C = 480kHz		−70			−72	−70	dBc
Two-Tone Intermodulation Distortion [6, 7]	f_C = 90kHz and 110kHz (−6.5dB)		−77			*		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		70	72		dB
(SINAD) Ratio	f_C = 480kHz		63		64	67		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB Input		16			*		MHz
Full Power	0dB Input		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			−150			*	μA
Convert Command		High Level When Converting			*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = −1mA	+2.7	+4.9		*			V
Internal Clock Frequency			17			*		MHz
Status		Low Level When Data Valid			*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			−110	−140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC} [8]			8.7			*		°C/W

* Specification same as ADS602JG.

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SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE SPECIFICATIONS)

$\pm V_{CC} = \pm 15V$, $+V_{DD} = +5V$, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
TEMPERATURE RANGE SPECIFICATION	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error [4]			±0.2	±0.5		±0.1	±0.4	% of FSR
Input Offset Error [4]: Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.25	1.5		1	1.25	LSB
Differential Linearity Error			1.25	1.5		1	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain			±0.0036	0.5		*	*	$\%FSR/\%V_{CC}$
			±0.001	0.5		*	*	$\%FSR/\%V_{DD}$
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	$\Delta +V_{DD} = \pm 5\%$		±1			*		$ns/\%V_{DD}$
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level ≈ –0.5dB, unless otherwise stated.)								
Differential Linearity Error	$f_C = 480kHz$, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.7			0.6		LSB
	100% of All Codes		1.3			1	1.25	LSB
Spurious Free Dynamic Range	$f_C = 10kHz$		73			85	71	dB
	$f_C = 480kHz$		62			65		dB
Total Harmonic Distortion	$f_C = 10kHz$		–81			–83	–70	dBc
	$f_C = 480kHz$		–63			–65		dBc
Two-Tone Intermodulation Distortion [7]	$f_C = 90kHz$ and 110kHz (–6.5dB)		–77			–79		dBc
Signal-to-Noise and Distortion	$f_C = 10kHz$		71		68	70		dB
(SINAD) Ratio	$f_C = 480kHz$		63			64		dB
Signal-to-Noise Ratio (SNR)	$f_C = 10kHz$		71		70	73		dB
	$f_C = 480kHz$		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS			*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command		High Level When Converting			*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS			*	*	*	
Bits 1 through 12, Status	Logic Low, $I_{OL} = 3.2mA$		+0.1	+0.4		*	*	V
	Logic High, $I_{OH} = –1mA$	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status		Low Level When Data Valid			*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC} [8]			8.7			*		°C/W

* Specification same as ADS602JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) If gain and offset adjust pins are not used, they should be grounded. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal ≈ –0.5dB of full scale; f_C = input frequency, f_S = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 6dB lower. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board, with the test device in a zero-insertion-force socket. Thermal resistance will be lower if the ADS602 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

ADS602

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

2

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	(MSB) Bit 1		32	Common (Analog)
2	Bit 2		31	+V_{CC} (+15V) Analog
3	Bit 3		30	−V_{CC} (−15V) Analog
4	Bit 4		29	Unipolar/Bipolar Control
5	Bit 5		28	Common (Input Signal)
6	Bit 6		27	Common (Analog)
7	+V_{DD} (+5V) Digital		26	Offset Adjust Input
8	Common (Digital)		25	Analog Signal Input
9	Make No External Connection		24	Gain Adjust Input
10	Status		23	−V_{CC} (−15V) Analog
11	Bit 7		22	+V_{DD} (+5V) Digital
12	Bit 8		21	Common (Digital)
13	Bit 9		20	+V_{CC} (+15V) Analog
14	Bit 10		19	Make No External Connection
15	Bit 11		18	Convert Command
16	Bit 12		17	Make No External Connection

Internal blocks: Reference, 12-Bit (SAR), 12-Bit D/A Converter, S/H Amp, Clock.
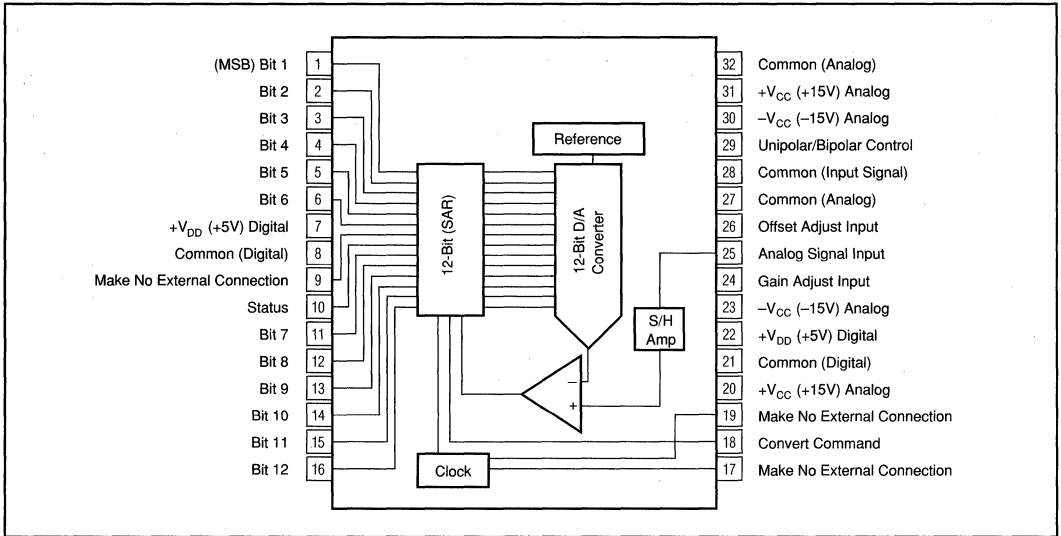
ABSOLUTE MAXIMUM RATINGS

±V_{CC} .... ±18V
+V_{DD} .... +7V
Digital Inputs .... +5.5V
Analog Inputs .... ±V_{CC}
Case Temperature .... +125°C
Junction Temperature .... +150°C
Storage Temperature .... −65°C to +150°C

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS602JG	32-Pin Ceramic	153

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

ADS602 ( ) G

Basic Model Number ————————————
Performance Grade Code
  J, K: 0°C to +70°C Case Temperature ————————
Package Code ————————————————————
  G: Ceramic Bottom Braze

TYPICAL PERFORMANCE CURVES

±V$_{CC}$ = ±15V, +V$_{DD}$ = +5V, 1MHz sampling rate, 6-minute warmup, and T$_C$ = +25°C unless otherwise noted.

ADS602

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SNR vs INPUT FREQUENCY

SINAD vs INPUT FREQUENCY

THD vs INPUT FREQUENCY

100kHz HARMONIC DISTORTION
(4096 Points)

Normal Harmonics (dB)	
f$_C$	−0.5
2f$_C$	−87.7
3f$_C$	−103.9
4f$_C$	−102.7
5f$_C$	−107.3
THD	−86.5
SINAD	71.8
SNR	71.9

100kHz DIFFERENTIAL NON-LINEARITY

480kHz DIFFERENTIAL NON-LINEARITY

PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data.
10	Status	Conversion status strobe is high during data conversion, low when parallel data is valid.
18	Convert Command	High transition starts conversion, and should remain high during conversion. Low will reset clock and SAR logic. Rising edge may be used to latch data from previous conversion.
24	Gain Adjust Input	Allows gain error to be externally adjusted to zero. Ground this pin if it is not used.
25	Analog Signal Input	Signal input to internal S/H amplifier.
26	Offset Adjust Input	Allows offset error to be externally adjusted to zero. Ground this pin if it is not used.
29	Unipolar/Bipolar Control	Ground on this pin engages unipolar operation (0V to +10V). Leaving this pin open engages bipolar (±5V).

The ADS602 is a sampling A/D converter that employs a successive approximation architecture. The ideal transfer function for an ADS602 in the bipolar mode is described in Figure 1. Initial gain and offset errors may be adjusted to zero, gain drift over temperature rotates the transfer function about –full scale end point, and offset drift shifts the transfer function left or right over the operating temperature range. Integral linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the converter. A differential linearity error of 0.012% means that the width of each bit step over the range of the converter is 1LSB, ±0.5LSB. The ADS602 is guaranteed to have no missing codes over its temperature range.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection for the ADS602 is shown in Figure 2. It is shown connected for ±5V bipolar operation. For unipolar operation, pin 29 should be grounded.

INTERFACING

The ADS602 has an impedance of approximately 1k; therefore, to maintain gain accuracy it must be driven from a low impedance source. The digital output lines should be buffered by a latch such as the 74AS574. These three-state drivers can then be connected directly to the data bus.

LAYOUT PRECAUTIONS

The ADS602 is a high-speed sampling analog-to-digital converter which requires more attention to circuit board layout than general purpose lower speed A/D converters.

The ADS602 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together since they are not connected together internally. Connecting all commons to a ground plane close to the ADS602 is the best method to maximize performance. The ground plane minimizes noise and provides additional heat dissipation.
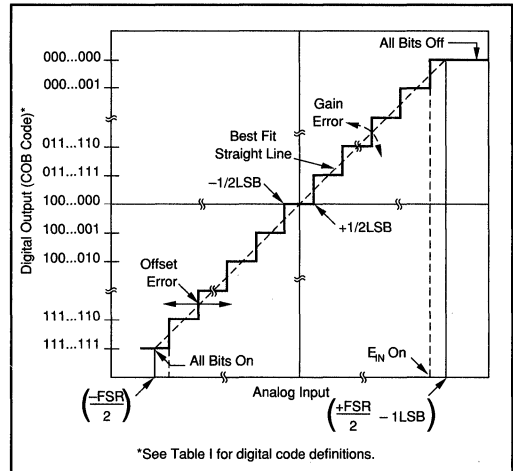
FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

ANALOG INPUT VOLTAGE RANGE	±5V	0V TO +10V
Code Designation	COB [1]	CSB [2]
One Least Significant Bit (LSB)	2.44mV	2.44mV
Transition Values MSB LSB [3]		
111...111 ⎫ 111...110 ⬋	–5V + 1/2LSB	0V + 1/2LSB
100...000 ⎫ 011...111 ⬋	–1/2LSB	+5 – 1/2LSB
000...001 ⎫ 000...000 ⬋	+5 – 3/2LSB	10V – 3/2LSB

NOTES: (1) COB = complementary offset binary. (2) CSB = complementary straight binary. (3) Voltages given are the nominal value for the transition from the next code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

POWER SUPPLY DECOUPLING AND POWER SUPPLY SENSITIVITY

The +15V and +5V power supply pins should be bypassed with a 10µF tantalum capacitor as shown in Figure 2. Pin 30 requires bypassing with a 150µF tantalum capacitor. These capacitors should be located close to the ADS602 supply pins. Ceramic 0.01µF bypass capacitors have been provided internally for more effective bypassing and need not be added externally.

Changes in the DC power supply voltages will affect accuracy. Regulated power supplies with 1% or less ripple are recommended for use with the ADS602. Power supply decoupling helps to keep ripple low.

POWER DISSIPATION

The ADS602 dissipates approximately 2.3W. The package has a junction-to-case thermal resistance (θ_{JC}) of 8.7°C/W and a case-to-ambient thermal resistance (θ_{CA}) of 13.7°C/W in a normal convection environment.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external trim potentiometers as shown in Figure 2. Multiturn potentiometers with 100ppm/°C temperature coefficient are recommended for minimum drift. If the gain adjust or offset adjust pins are not used, they must be grounded to meet the specified accuracy.

DYNAMIC PERFORMANCE TESTING

The ADS602 is a high performance sampling A/D converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on important dynamic performance parameters.
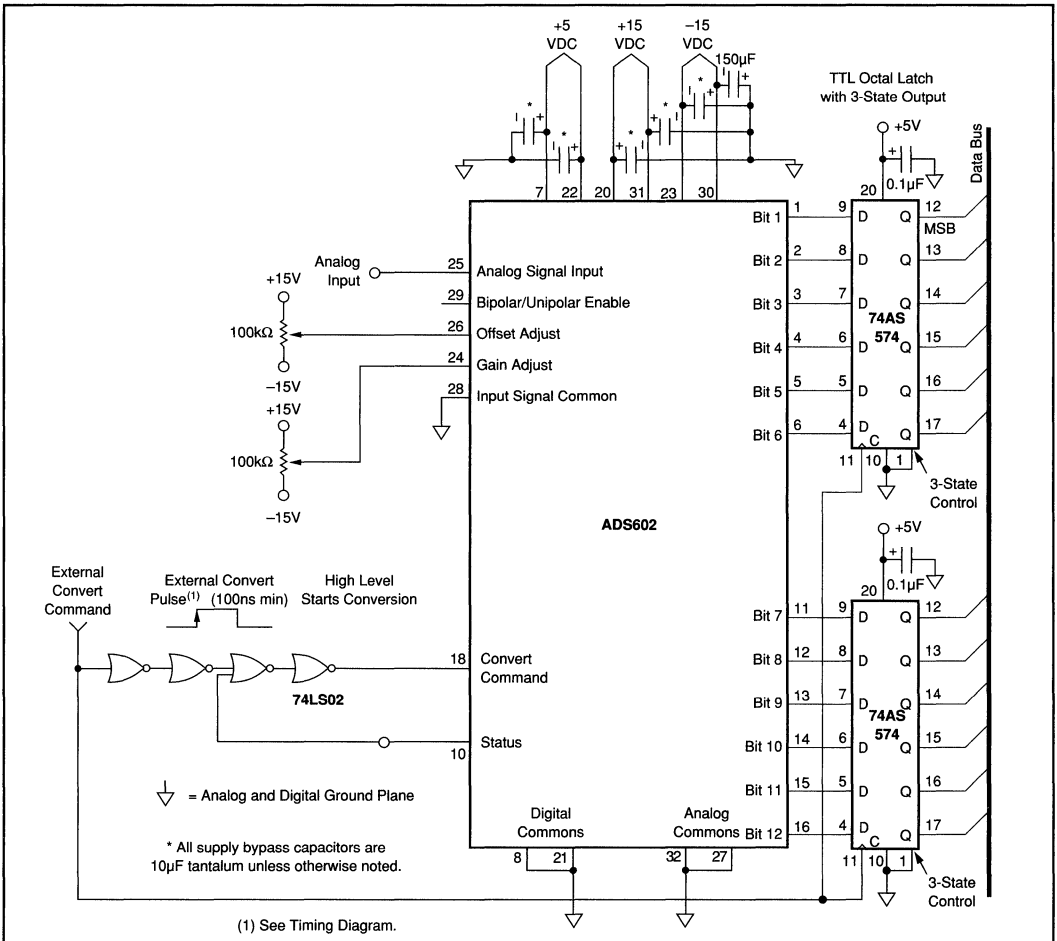
FIGURE 2. ADS602 Application Circuit.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise + harmonic power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{harmonic power (first 9 harmonics)}}{\text{sinewave signal power}}$$

4. Spurious Free Dynamic Range (SFDR):

$$10 \log \frac{\text{largest harmonic power}}{\text{sinewave signal power}}$$

5. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{highest IMD product power (to 5th order)}}{\text{sinewave signal power}}$$

IMD is referred to the larger of the test signals f1 or f2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

TIMING CONSIDERATIONS

In addition to the timing details in Figure 3, the following list contains some important timing considerations for the ADS602:

1. When power is first applied, the convert command should be held low or below the +5V supply to prevent latch up.

2. The rising edge of the convert command pulse initiates a conversion. This convert command should remain high until the Status falls (i.e., the internal ADC is finished converting). A simple circuit that provides the correct convert command (pin 18) pulse length, is shown in Figure 2.

3. The ADS602 goes directly into the "hold" mode when a convert command signal is given. The Status falls approximately 780ns later, indicating that the conversion is complete. At this time, the sample-hold (internal to the ADS602) enters the track mode. The ADS602 will remain in the track mode until the next convert command is given.

4. The data from conversion "N" can be latched directly by the convert command pulse "N + 1". This approach is illustrated in Figure 2. The falling edge of Status may be used to latch the data; however, Status must be delayed by t_{SD} (see Figure 3) plus the external latch (74AS574) setup time.

	MIN	TYP	MAX	
t_{CH}	100ns			External convert command pulse width.*
t_{CC}		780ns		
t_{CONV}	1μs			Convert command minimum period.
t_{SD}		17ns	50ns	Status low to data valid.
t_{SL}		780ns		Convert command to status low.
t_{CI}	11ns	20ns		Convert command to data invalid.
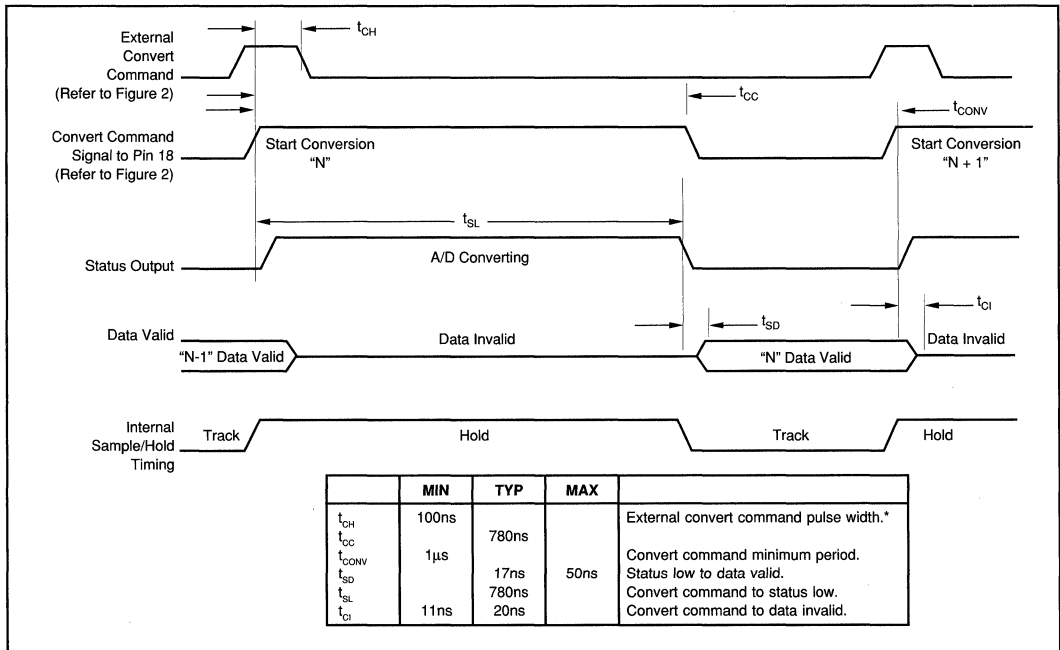
FIGURE 3. ADS602 Logic Timing Diagram.

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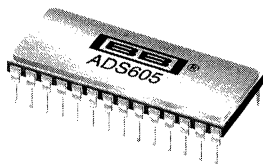
ADS605

DEMO BOARD
AVAILABLE
See Appendix A for
more information.

ADS605

2

12-Bit 10MSPS
ANALOG-TO-DIGITAL CONVERTER

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FEATURES

● COMPLETE, SELF-CONTAINED DESIGN
● HIGH SPURIOUS-FREE DYNAMIC RANGE:
   76dBc at Nyquist
● LOW DNL ERROR: 0.5 LSB
● HIGH SNR: 65dB at Nyquist
● SINGLE-ENDED TRACK/HOLD
● WIDEBAND TRACK/HOLD:
   32MHz Full Power Bandwidth
● LOW DRIFT REFERENCE: 20ppm/°C
● LOW POWER: 1.4W
● COMPACT 28-PIN DIP PACKAGE

APPLICATIONS

● MEDICAL IMAGING
● CCD IMAGING
● COMMUNICATIONS
● RADAR
● TEST INSTRUMENTATION
● HIGH SPEED DATA ACQUISITION
● PHOTOGRAPHIC IMAGING
● IR IMAGING
● SPECTRUM ANALYSIS

DESCRIPTION

The ADS605 is a high performance sampling analog-to-digital converter complete with a track/hold, low drift reference and internal timing. The wideband track/hold has a user-friendly single-ended input. Its robust, no compromise, design yields EXCELLENT NYQUIST PERFORMANCE for key specifications like spurious free dynamic range, SNR and differential

linearity. Both DC and dynamic specifications are guaranteed.

The ADS605 is packaged in a 28-pin hermetic DIP package. The logic interface is TTL. The DEM-ADS605 demonstration board is available to quickly evaluate this high performance device.

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FULL TEMPERATURE SPECIFICATIONS

ELECTRICAL

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

PARAMETER	CONDITIONS	ADS605H			ADS605HB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±1.0			*		V
Impedance			1.5			*		MΩ
Capacitance			5			*		pF
CONVERSION CHARACTERISTICS								
Sample Rate Range		DC		10	*		*	MHz
Throughput Rate		10			*			MHz
Pipeline Delay				One Convert Command Period				
Start Up Time to Rated Accuracy				1			*	minute
DC ACCURACY								
Integral Linearity Error	f_{IN} = 100kHz		±2.0			±1.7	±2.5	LSB[1]
Differential Linearity Error	f_{IN} = 100kHz		±0.6	–0.99, +1.5		±0.5	–0.99, +1.0	LSB
No Missing Codes	f_{IN} = 100kHz		Guaranteed			Guaranteed		
Gain Error[2, 3]	DC		0.9	±1.25		0.7	±1.0	%FSR
Bipolar Zero Error[2]	DC		0.2	±0.75		0.1	±0.3	%
Power Supply Sensitivity								
$+V_S$	$+4.75V < +V_S < +5.25V$		±0.002	±0.05		±0.001	±0.05	%FSR
$-V_S$	$-4.75V < -V_S < -5.46V$		±0.002	±0.05		±0.001	±0.05	%FSR
AC ACCURACY	Input Signal within 1dB of Full Scale							
Spurious-Free Dynamic Range	f_{IN} = 100kHz	73	78		78	82		dBFS[4]
	f_{IN} = 5MHz	67	73		71	76		dBFS
Total Harmonic Distortion	f_{IN} = 100kHz		–75	–70		–80	–75	dBFS
	f_{IN} = 5MHz		–70	–67		–74	–70	dBFS
Signal-to-(Noise+Distortion) Ratio	f_{IN} = 100kHz	61	65		64	67		dBc
	f_{IN} = 5MHz	60	63		62	65		dBc
Signal-to-Noise Ratio	f_{IN} = 100kHz	62	64		65	67		dB
	f_{IN} = 5MHz	61	63		63	64		dB
Differential Linearity Error	f_{IN} = 5MHz		±0.8	–0.99, +1.5		±0.6	±0.85	LSB
No Missing Codes	f_{IN} = 5MHz		Guaranteed			Guaranteed		
Full-Power Bandwidth[5]			32			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			1.0			*		ns
Aperture Jitter			3			*		ps rms
Overvoltage Recovery[6]			96	200		*	*	ns
CONVERT INPUT								
Pulse Width		30		42	*		*	ns
Logic Levels								
V_{IL}		–0.15		+0.8	*		*	V
V_{IH}		+2.0		V_D + 0.15	*		*	V
I_{IL}				±750			*	µA
I_{IH}				±750			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 12-bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.5			*	V
V_{OH}	I_{SOURCE} = 80µA	+2.4			*			V
POWER SUPPLIES								
Specified Performance								
$+V_S$		+4.75	+5	+5.25	*	*	*	V
$+I_S$			+60	+100		*	*	mA
$-V_S$		–5.46	–5.2	–4.75	*	*	*	V
$-I_S$			–200	+220		*	*	mA
Power Dissipation			1.35	1.7		*	1.5	W
TEMPERATURE RANGE								
Specified Performance	Case Temperature	0		+70	*		*	°C
θ_{JC}	Junction-to-Case		10			*		°C/W
θ_{CA}	Case-to-Ambient		28			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±1.0V input ADS605, one LSB is 488µV. (2) Adjustable to zero with external potentiometer. (3) Gain error scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) dBFS is dB relative to a full-scale ±1.0V input. (5) Full-Power Bandwidth defined as the –3dB frequency of the Track/Hold referred to as Full Scale. (6) Recovers to specified performance after 2 x FS input overvoltage.

PIN CONFIGURATION

Top View　　　　　　　　　　　　　　**DIP**

Pin			Pin
+V$_S$A	1	28	Ground
Bit 1	2	27	V$_{IN}$
Bit 2	3	26	Ground
Bit 3	4	25	–V$_S$A
Bit 4	5	24	–V$_S$A
Bit 5	6	23	Ground
Bit 6	7	22	V$_{OS}$
Bit 7	8	21	Gain
Bit 8	9	20	Ground
Bit 9	10	19	–V$_S$D
Bit 10	11	18	–V$_S$D
Bit 11	12	17	+V$_S$D
Bit 12	13	16	Conv
Data Strobe	14	15	Ground

ADS605
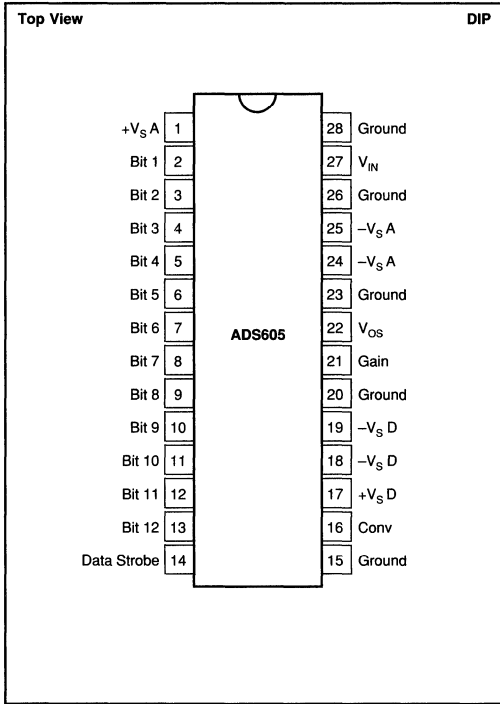
PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	Analog +V	+5V
2	Bit 1	Most Significant Bit
3	Bit 2	
4	Bit 3	
5	Bit 4	
6	Bit 5	
7	Bit 6	
8	Bit 7	
9	Bit 8	
10	Bit 9	
11	Bit 10	
12	Bit 11	
13	Bit 12	Least Significant Bit
14	Data Strobe	Rising edge can be used to latch data into external latches.
15	Ground	
16	Conv	Convert Command. A rising edge on this input initiates conversion.
17	Digital +V$_S$	+5V
18	Digital –V$_S$	–5.2V
19	Digital –V$_S$	
20	Ground	
21	Gain	Gain Adjust Input
22	V$_{OS}$	Offset Adjust Input
23	Ground	
24	Analog –V$_S$	–5.2V
25	Analog –V$_S$	–5.2V
26	Ground	
27	V$_{IN}$	Analog Input. Full scale range is ±1.0V
28	Ground	

ORDERING INFORMATION

ADS605　H　( )

Basic Model Number
Package Code
H: Metal and Ceramic
Performance Grade Code
No letter or "B": 0°C to +70°C Case Temperature

ABSOLUTE MAXIMUM RATINGS

+V$_S$ .... +7V
–V$_S$ .... –7V
Analog Input .... ±2.5V
Logic Input .... –0.5V to +V$_S$
Case Temperature .... +100°C
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +125°C

NOTE: (1) Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS605H	28-Pin Ceramic DIP	237
ADS605HB	28-Pin Ceramic DIP	237

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ADS605 — **A/D CONVERTERS, DATA ACQUISITION COMPONENTS** — **2**

TYPICAL PERFORMANCE CURVES

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

1MHz SPECTRAL PERFORMANCE

2MHz SPECTRAL PERFORMANCE

4.7MHz SPECTRAL PERFORMANCE

2MHz SPECTRAL PERFORMANCE
WITH A 5MHz SAMPLING RATE

TWO-TONE INTERMODULATION DISTORTION

2MHz SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE

TYPICAL PERFORMANCE CURVES (CONT)

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = -5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

5MHz SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE

2MHz TOTAL HARMONIC DISTORTION vs TEMPERATURE

5MHz TOTAL HARMONIC DISTORTION vs TEMPERATURE

100kHz DIFFERENTIAL NON-LINEARITY

2MHz DIFFERENTIAL NON-LINEARITY

5MHz DIFFERENTIAL NON-LINEARITY

ADS605

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

TYPICAL PERFORMANCE CURVES (CONT)

T = 0°C to +70°C case temperature, f$_s$ = 10MHz, +V$_S$ = +5V, –V$_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

100kHz SIGNAL-TO-NOISE RATIO
vs TEMPERATURE

2MHz SIGNAL-TO-NOISE RATIO
vs TEMPERATURE

5MHz SIGNAL-TO-NOISE RATIO
vs TEMPERATURE

OUTPUT CODE COUNTS
WITH THE INPUT GROUNDED

DIFFERENTIAL NON-LINEARITY ERROR
vs CONVERT COMMAND CLOCK PULSE WIDTH

100kHz SINAD vs TEMPERATURE

TYPICAL PERFORMANCE CURVES (CONT)

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = −5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

2MHz SINAD vs TEMPERATURE

5MHz SINAD vs TEMPERATURE

SWEPT POWER SFDR

ADS605

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FIGURE 1. ADS605 Timing Diagram.

SYMBOL	DESCRIPTION	MIN	TYP	MAX
t_{CC}	Convert Command Pulse Width	30ns		42ns
t_{INV}	Data Invalid Period	10ns		35ns
t_S	Data Strobe Rising Edge	65ns	75ns	85ns
t_{AQ}	Acquisition Time		30ns	
t_Q	Quantizer Time		70ns	

TABLE I. Timing Specifications.

THEORY OF OPERATION

The ADS605 is a two-step subranging analog-to-digital converter. Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high accuracy) DAC, subtract this voltage from the T/H output, amplify this "remainder," convert to digital with second coarse ADC, and combine the digital output from the first ADC with the digital output from the second ADC. In practice, however achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed track/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter).

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADS605. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used internally for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages.

The ADS605 timing technique generates a variable width T/H gate pulse which is determined by the conversion command pulse period minus a fixed 70ns ADC conversion time. ADS605 conversion rates are therefore possible somewhat above the 10MSPS specification but acquisition time is sacrificed and accuracy is rapidly degraded.

INPUT VOLTAGE (Exact Center of Code)	BINARY TWO'S COMPLEMENT (BTC) OUTPUT CODING
+FS (+1.0V)	011111111111
+FS – 1LSB	011111111111
+FS – 2LSB	011111111110
+3/4 Full Scale	011000000000
+1/2 Full Scale	010000000000
+1/4 Full Scale	001000000000
+1LSB	000000000001
Bipolar Zero (0V)	000000000000
–1LSB	111111111111
–1/4 Full Scale	111000000000
–1/2 Full Scale	110000000000
–3/4 Full Scale	101000000000
–FS – 1LSB	100000000001
–FS (–1.0V)	100000000000
	MSB LSB

TABLE II. Coding Table for the ADS605. One LSB = 488µV.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADS605 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: spurious free dynamic range (SFDR), signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

Highly accurate phase-locked signal sources allow high resolution coherent FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an odd integral number of signal frequency periods can be sampled. Because no spectral leakage results, a rectangular window (no window function) can be used. This was used to generate the typical FFT performance curves.

If generators cannot be phase-locked and set to extreme accuracy, every low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended. To assure that the majority of codes are exercised in the ADS605, a minimum 4096 point FFT should be taken.

APPLICATIONS

The following points must be followed carefully in order to accurately test the precision ADS605:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the AC+DC and "hard limit" on signal peaks.

2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.

3. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier

using an OPA642 is shown in Figure 2. This circuit will provide excellent performance from DC to 10MHz with harmonic and intermodulation components typically better than –85dBc. A passive (hybrid transformer) signal combiner can also be used (Figures 3 and 4) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be approximately 45dB between signal generators and its input-output insertion loss will be about 6dB. Distortion will be better than –85dBc for the powdered-iron core specified.
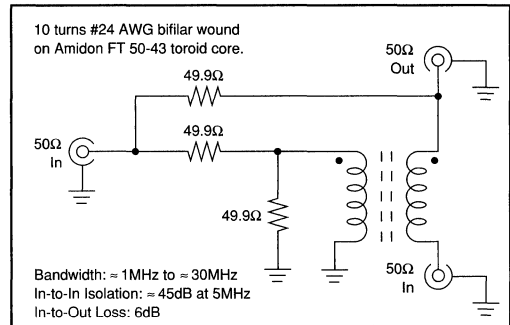
FIGURE 3. Passive Signal Divider.
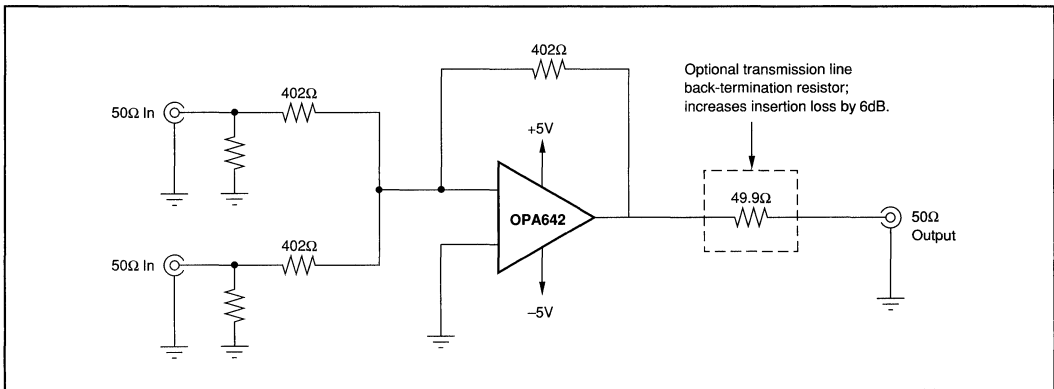
FIGURE 2. Active Signal Combiner.
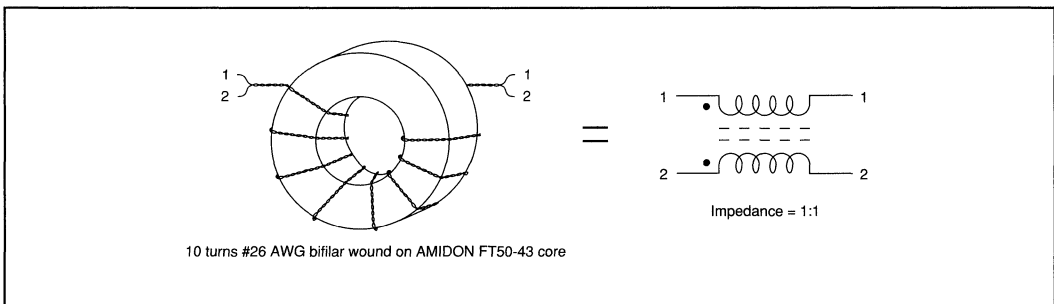
FIGURE 4. Transformer Details.

ADS605

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

4. The signal source must be filtered to provide a clean, harmonic-free input to the ADS605. This signal source must have exceptional noise performance to achieve accurate SNR measurements.

5. The analog input of the ADS605 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA642. Short leads are necessary to prevent digital noise pickup.

6. The convert command must be generated form a low jitter source. The convert command high time can range from 30ns to 42ns. A 50% convert command duty cycle will lead to excessive noise coupling in the converter. A high jitter convert command source will add significant noise to the system results. An HP8644A generator is a good clock source. Short leads are necessary to preserve fast TTL rise times.

7. The digital data at the output of the ADS605 must be buffered externally prior to latching. A buffered TTL 12-bit register such as two 74F574s is recommended. This data can be latched using the DATA STROBE pulse or the convert command pulse. The latches should be mounted on PC boards in very close proximity to the ADS605. Avoid long leads.

8. A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy ground planes can give excellent results, if carefully designed.

9. Prototyping "plug boards" or wire-wrap boards will not be satisfactory.

10. Connect analog and digital ground pins of the ADS605 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane.

11. Power supplies should be bypassed with 0.1μF and 2.2μF capacitors. The 0.1μF monoblock capacitors should be placed on the topside of the PC board as close to the pin as your manufacturing process allows.

12. If using a cable to drive the input of the ADS605, avoid reflections down the cable that could degrade dynamic performance by placing a 3dB attenuator at the end of the cable. The input amplitude may be doubled to maintain signal amplitude.

OFFSET AND GAIN ADJUSTMENT

The ADS605 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers by using the application circuits in Figure 5. Trim range is typically ±2.0% for gain and ±2.0% for offset. If gain and offset trim is not used, pins 21 and 22 should be grounded.

THERMAL REQUIREMENTS

The ADS605 is tested and specified over a case temperature range of 0°C to +70°C. The converter is tested in a forced-air environment with a 10 SCFM air flow. At extended temperatures, heat sinking may be required. The thermal resistances (θ_{JC} and θ_{CA}) of the ADS605 package are 10°C/W and 28°C/W, respectively, measured to the underside of the case.
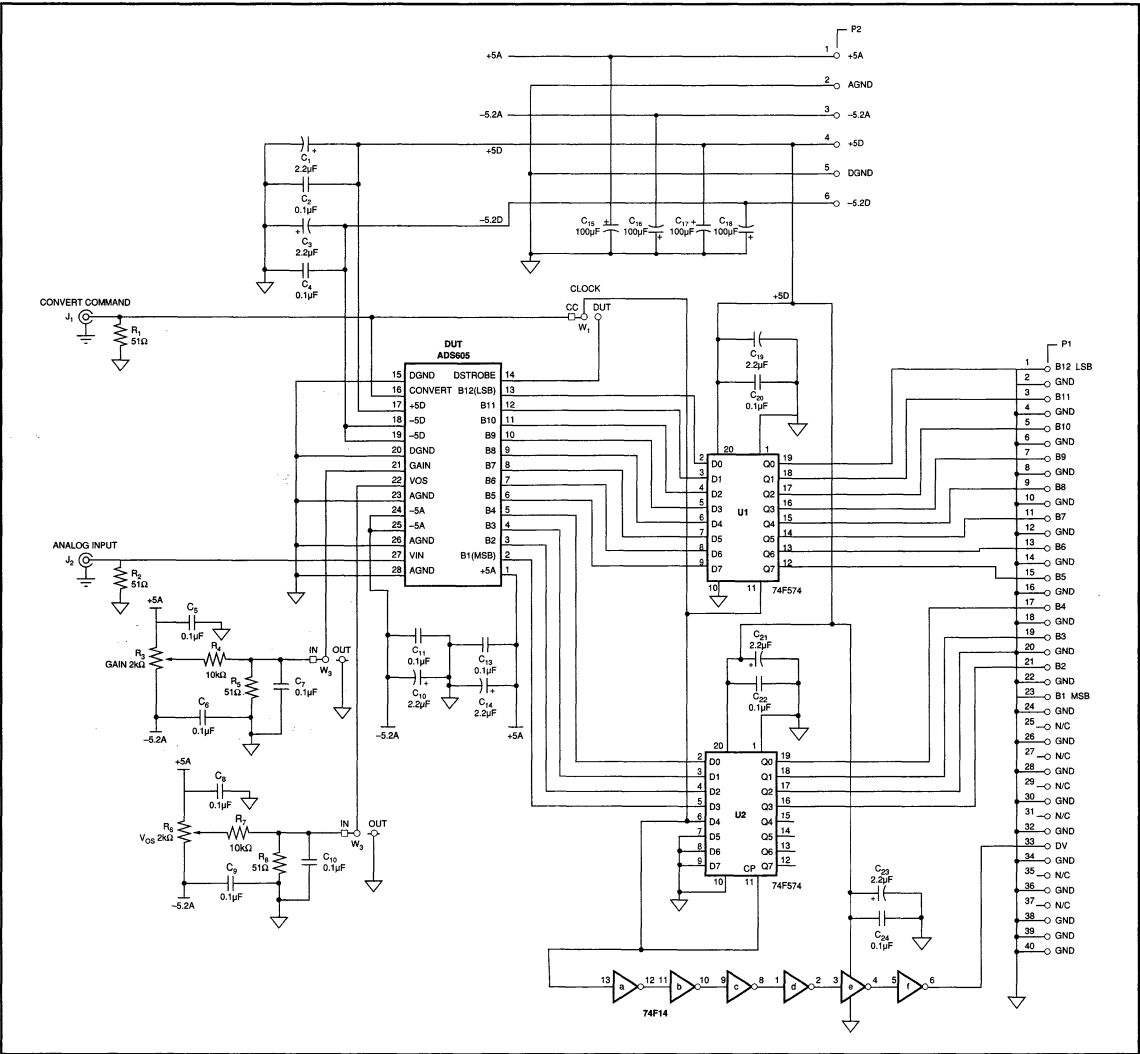
FIGURE 5. Application Diagram for the DEM-ADS605 Evaluation Board.
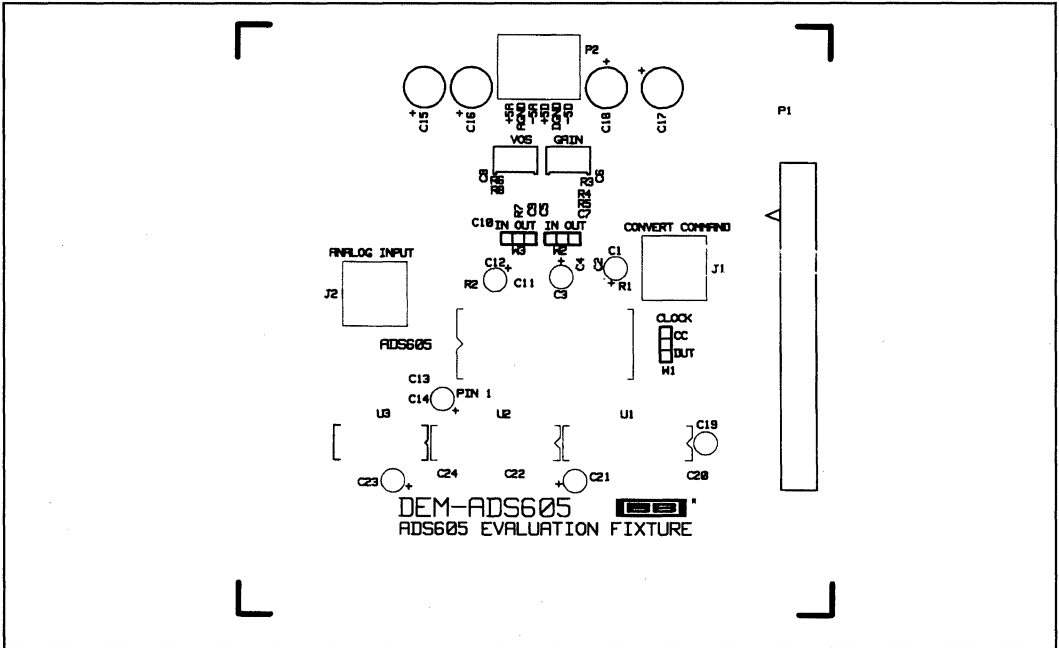
FIGURE 6. DEM-ADS605 Silkscreen.
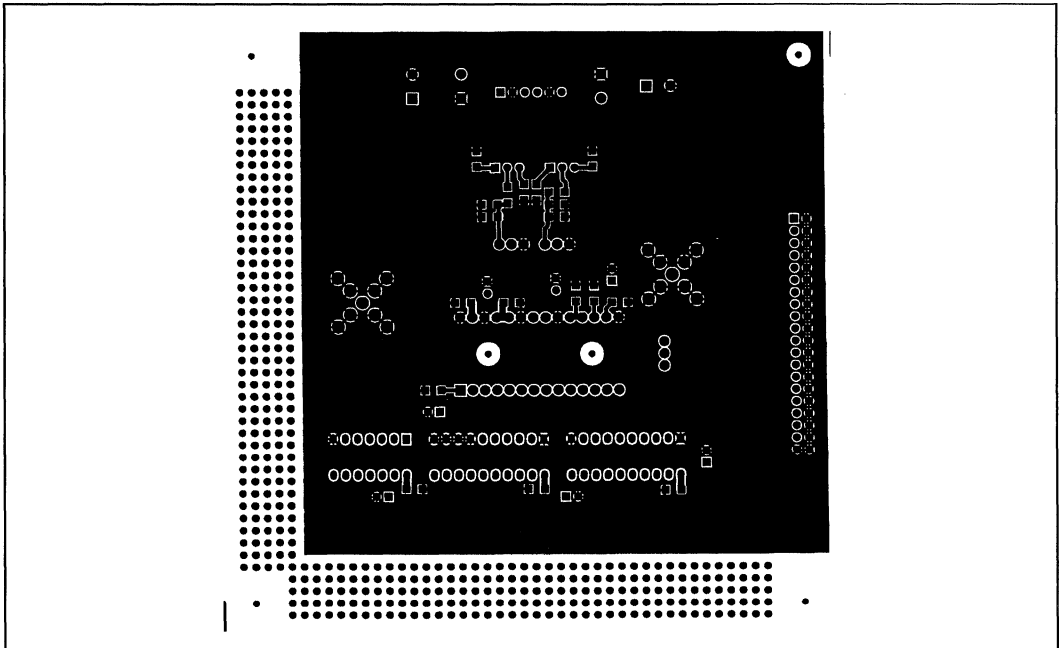
FIGURE 7. DEM-ADS605 Top PCB Layer. Analog Ground Plane, Top View.
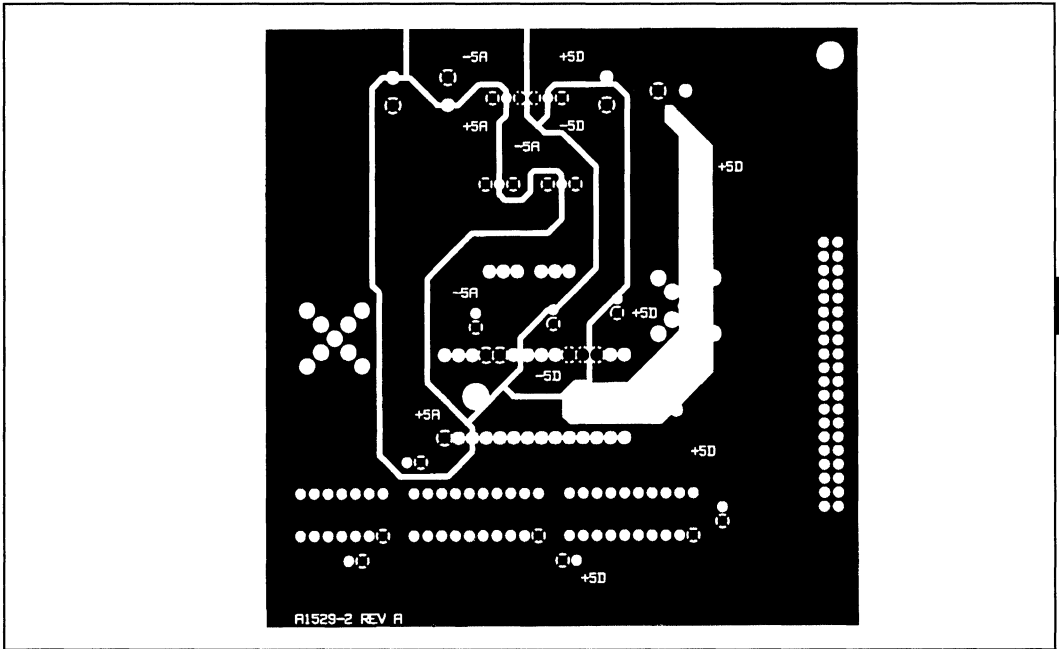
FIGURE 8. DEM-ADS605 Middle PCB Layer. Power Plane, Top View.
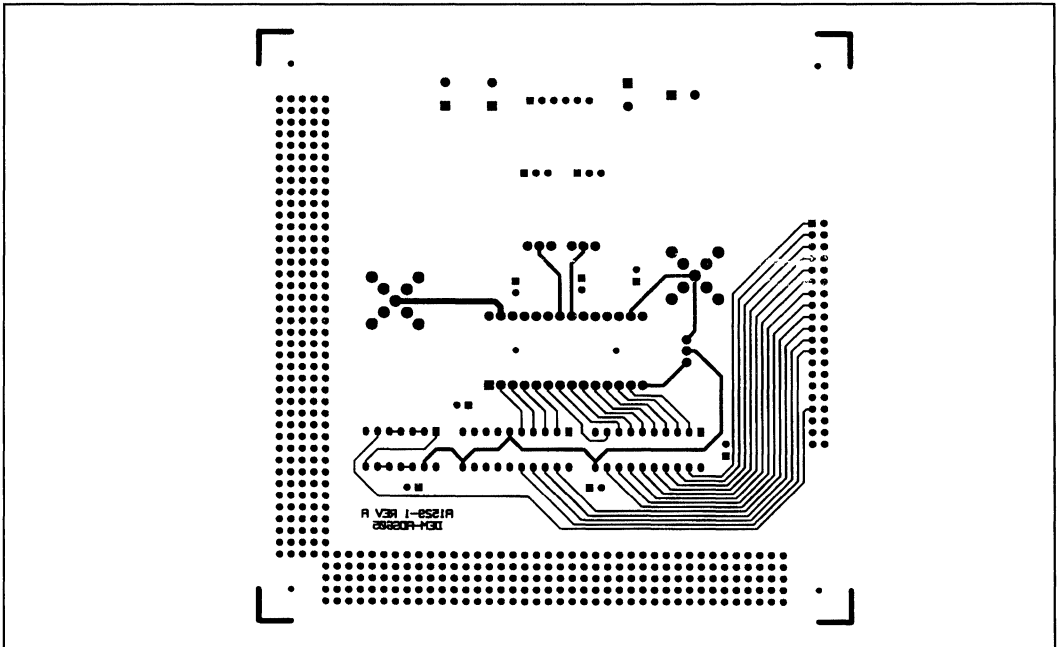
FIGURE 9. DEM-ADS605 Bottom PCB Layer. Interconnect, Top View.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS
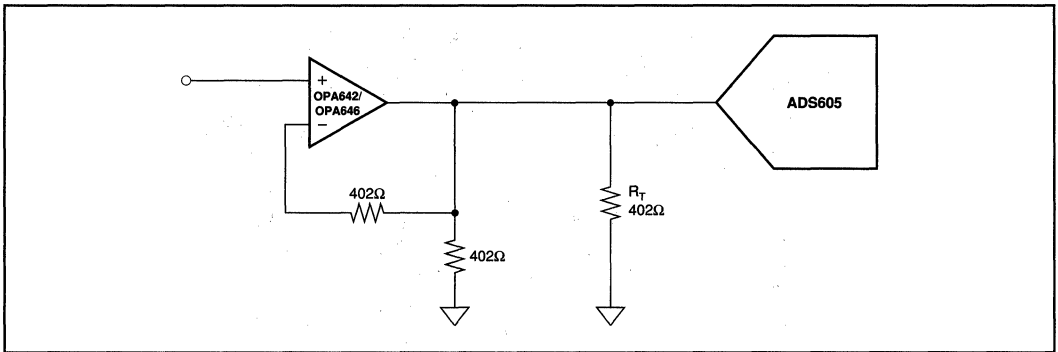
FIGURE 10. A Low Distortion or Low Power Amplifier Front End for the ADS605.
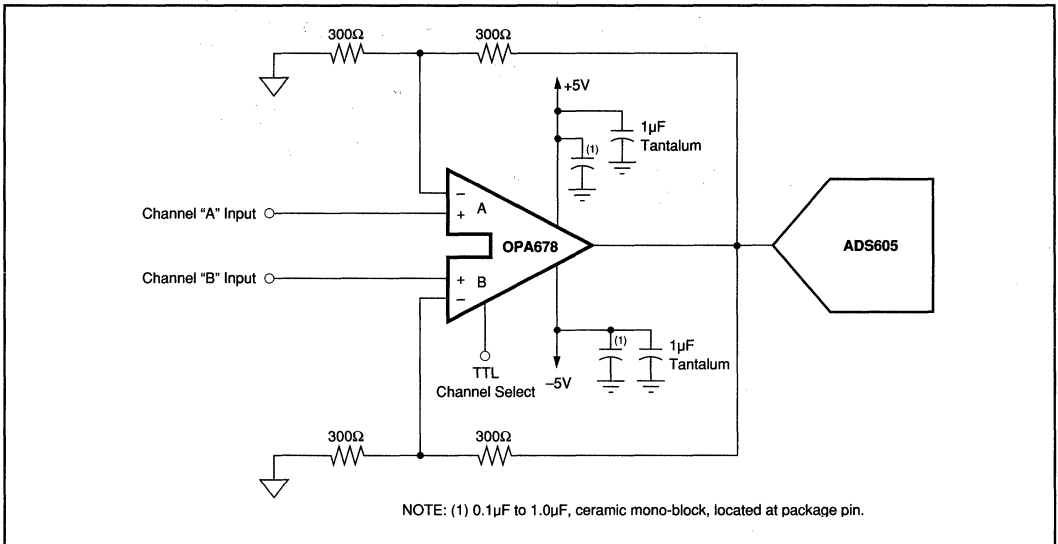
FIGURE 11. TTL-Controlled Input Multiplexer with Gain of +2V/V in Front of the ADS605.
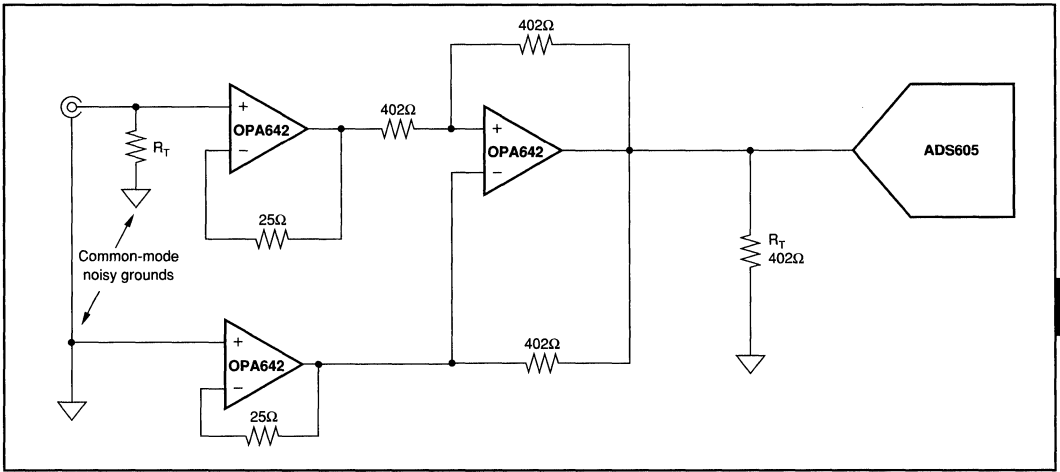
FIGURE 12. A Differential Amplifier Input for Rejecting Common-Mode Ground Noise.

ADS605

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN ®

ADS610

14-Bit 10MHz Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH SPURIOUS-FREE DYNAMIC RANGE: 90dB AT Nyquist**
- **WIDE FULL-POWER BANDWIDTH: 40MHz**
- **HIGH SIGNAL-TO-NOISE RATIO: 77dB**
- **NO MISSING CODES AT 14 BITS**
- **PIN CONSISTENT WITH ADS703, ADS704: (16-Bit 2.5MHz, 18-Bit 500kHz)**
- **±1.25V ANALOG INPUT RANGE**
- **LOW POWER: 2.5 Watts**
- **SMALL HERMETIC PACKAGE: 0.6" x 2.0"**

APPLICATIONS

- **COMMUNICATIONS SIGNAL PROCESSING**
- **RADAR SIGNAL PROCESSING**
- **CCD IMAGING**
- **MAGNETIC RESONANCE IMAGING**
- **ULTRASOUND SIGNAL PROCESSING**
- **AUTOMATIC TEST EQUIPMENT**
- **HIGH SPEED DATA ACQUISITION**

DESCRIPTION

The ADS610 is a very high speed, highly integrated 14-bit sampling A/D converter. It is designed for superior performance and low noise.

The ADS610 is a two-step subranging design containing a quantizer, sample/hold amplifier, voltage reference and timing circuitry in a slim 40-pin package. It is pin consistent with the ADS703 (16-bit 2.5MHz)

and the ADS704 (18-bit 500kHz) sampling ADC's, allowing the user to choose easily between speed and resolution. A convenient TTL-compatible logic interface is provided.

A demonstration board (DEM-ADS610) is available for quick evaluation.

BURR - BROWN ®

SPECIFICATIONS

$T_A = +25°C$, $+V_S = +5V$, $-V_S = -5.2V$, $\pm1.25V$ Input Range, Sampling Rate = 10MHz unless otherwise noted.

PARAMETER	CONDITIONS	TEMPERATURE	ADS610H MIN	ADS610H TYP	ADS610H MAX	ADS610HB MIN	ADS610HB TYP	ADS610HB MAX	UNITS
RESOLUTION					14			*	Bits
TEMPERATURE RANGE: H, HB	$T_{AMBIENT}$		−40		+70	*		*	°C
ANALOG INPUT									
Full Scale Input Range			−1.25		+1.25	*		*	V
Input Impedance				$0.3 \times 10^{12} \parallel 2$			*		$\Omega \parallel pF$
DIGITAL INPUTS									
Logic Family				TTL/HCT Compatible			*		
Convert Command	Start Conversion			Convert Command Rising Edge			*		
Pulse Width	t = Conversion Period		10		t −20	*		*	ns
CONVERSION CHARACTERISTICS									
Sample Rate			DC		10M	*		*	Samples/s
Data Latency				1			*		Convert Cycle
DC ACCURACY									
Gain Error		+25°C		0.3	0.7		0.2	0.5	% FSR
		Full							ppm/°C
Input Offset		+25°C		0.4	0.7		0.2	0.5	% FSR
		Full							ppm/°C
Power Supply Rejection	Delta $+V_S = 5\%$	Full		±0.03	±0.07	*		*	% FSR/%
	Delta $-V_S = 5\%$	Full		±0.01	±0.07	*		*	% FSR/%
DYNAMIC CHARACTERISTICS									
No Missing Codes		Full		Guaranteed			Guaranteed		
Differential Linearity Error									
f = 8kHz		+25°C		0.8	1.5		0.6	0.8	LSB
		Full		0.8	1.5		0.6	1.0	LSB
f = 5MHz		+25°C		0.9	2.0		0.6	1.0	LSB
		Full		0.9	2.0		0.7	1.0	LSB
Integral Linearity Error		+25°C		0.9	1.5		0.7	1.0	LSB
		Full		1.4	2.0		1.2	1.5	LSB
Spurious Free Dynamic Range (SFDR)									
f = 8kHz (−1dBFS Input)		+25°C	83	87		90	92		dBFS
		Full	82	86		87	91		dBFS
f = 5.0MHz (−1dBFS Input)		+25°C	83	86		90	91		dBFS
		Full	82	85		87	90		dBFS
Two-Tone Intermodulation Distortion									
f = 4.4 and 4.5MHz (−7dB each tone)		+25°C		−86			−91		dBFS
		Full		−85			−90		dBFS
Signal-to-Noise Ratio (SNR)									
f = 8kHz (−1dBFS Input)		+25°C	70	76		75	79		dB
		Full	70	75		75	78		dB
f = 5.0MHz (−1dBFS Input)		+25°C	70	75		75	77		dB
		Full	70	74		75	77		dB
SINAD									
f = 8kHz (−1dBFS Input)		+25°C	69	75		74	78		dB
		Full	69	74		74	77		dB
f = 5.0MHz (−1dBFS Input)		+25°C	69	74		74	77		dB
		Full	69	74		74	77		dB
Output Noise	Input Grounded	+25°C		0.6			*		LSBrms
Aperture Delay Time		+25°C		5			*		ns
Aperture Jitter		+25°C		5			*		ps rms
Analog Input Bandwidth (−3dB)									
Small Signal	−20dB Input	+25°C		120			*		MHz
Full Power	0dB Input	+25°C		40			*		MHz
Overload Recovery Time	2x Full Scale Input	+25°C		1			*		µs
OUTPUTS									
Logic Family				TTL Compatible			*		
Logic Coding	Logic Selectable			SOB or COB			*		
Logic Levels									
Logic "LO"	$I_{OL} < 3.2mA$	Full	0		0.5	*		*	V
Logic "HI"	$I_{OH} < 80µA$	Full	4	4.9		*		*	V
3-State Enable/Disable Time		Full		10	25		*	*	ns

ADS610

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS(CONT)

T_A = +25°C, +V_S = +5V, –V_S = –5.2V, ±1.25V Input Range, Sampling Rate = 10MHz unless otherwise noted.

PARAMETER	CONDITIONS	TEMPERATURE	ADS610H MIN	ADS610H TYP	ADS610H MAX	ADS610HB MIN	ADS610HB TYP	ADS610HB MAX	UNITS
POWER SUPPLY REQUIREMENTS									
Supply Voltages: +V_S	Operating	Full	+4.75	+5.0	+5.25	*	*	*	V
–V_S		Full	–5.46	–5.2	–4.94	*	*	*	V
Supply Currents: +I_S	Operating	Full		125			*		mA
–I_S		Full		375			*		mA
Power Consumption		Full		2.5	2.75		*	*	W
θ_{JC}				TBD			TBD		°C/W
θ_{JA}	Still Air			TBD			TBD		°C/W

ABSOLUTE MAXIMUM RATINGS

+V_S .... +6V
–V_S .... 0.3V to –6V
Logic Inputs .... 0V to –5.5V
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +165°C
Lead Temperature (soldering, 10s) .... +300°C

NOTE: Stresses above these ratings may permanently damage the device.

PIN CONFIGURATION

Top View			DIP
Bit 1	1	40	GND
Bit 2	2	39	Analog Input
Bit 3	3	38	+5V
Bit 4	4	37	GND
Bit 5	5	36	–5V
Bit 6	6	35	Reference Input
Bit 7	7	34	Reference Output
Bit 8	8	33	Ref (Gain) Adjust
Bit 9	9	32	GND
Bit 10	10	31	Offset Adjust
Bit 11	11	30	+5V
Bit 12	12	29	GND
Bit 13	13	28	–5V
Bit 14	14	27	–5V
No Internal Connection	15	26	GND
No Internal Connection	16	25	+5V
No Internal Connection	17	24	Test/Trim Enable
No Internal Connection	18	23	Polarity Control
Over/Underrange	19	22	OUTPUT ENABLE
Convert Command	20	21	GND

PACKAGING INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS610H, HB	40-Pin, 0.6" Wide Hermetic DIP	214

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

ADS610 H ( )

Basic Model Number ————————————————
Package Code ——————————————————————
Performance Grade Code ——————————————————
   No letter or "B" = –40°C to +70°C Ambient Temperature

TIMING DIAGRAM

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Command Period	100			ns
t_{CCH}	Convert Command Pulse Width High	20		$t_{CONV} -20$	ns
t_{CCL}	Convert Command Pulse Width Low	20		$t_{CONV} -20$	ns
t_{DV}	Data Valid After Convert Command	40	63		ns
t_X	Data Valid Before Convert Command	20	37		ns

NOTE: The time scale applies for a 10MHz conversion rate. The "〰" indicates the part of timing waveform that will "stretch out" at slower conversion rates.

ADS610

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

ADS703

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

16-Bit 2.5MHz Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **HIGH SPURIOUS-FREE DYNAMIC RANGE:**
  92dB AT 1MHz
● **HIGH SNR: 90dB AT 1MHz**
● **NO MISSING CODES AT 16 BITS**
● **LOW NONLINEARITY: ±1LSB**
● **PIN CONSISTENT WITH ADS610, ADS704:**
  (14-Bit 10MHz, 18-Bit 500kHz)
● **±2.5V ANALOG INPUT RANGE**
● **LOW POWER: 2.75Watts**
● **SMALL HERMETIC PACKAGE: 0.6" x 2.0"**

APPLICATIONS

● **MEDICAL IMAGING**
● **SPECTRUM ANALYZERS**
● **IR SPECTROMETERS**
● **CCD IMAGING**
● **ULTRASOUND SIGNAL PROCESSING**
● **SONAR SIGNAL PROCESSING**
● **AUTOMATIC TEST EQUIPMENT**
● **HIGH SPEED DATA ACQUISITION**

DESCRIPTION

The ADS703 is a very high speed, highly integrated 16-bit sampling A/D converter. It is designed for superior linearity, low noise and wideband spectral performance.

The ADS703 is a three-step subranging design containing a quantizer, sample/hold amplifier, voltage reference and timing circuitry in a slim 40-pin package. It is pin consistent with the ADS610 (14-bit 10MHz) and the

ADS704 (18-bit 500kHz) sampling ADC's, allowing the user to choose easily between speed and resolution. A convenient TTL-compatible logic interface is provided.

A demonstration board (DEM-ADS703) is available for quick evaluation.

BURR-BROWN®

PDS-1262

SPECIFICATIONS

T_A = +25°C, +V_S = +5V, −V_S = −5.2V, ±2.5V Input Range, Sampling Rate = 2.5MHz unless otherwise noted.

PARAMETER	CONDITIONS	TEMPERATURE	ADS703H MIN	TYP	MAX	ADS703HB MIN	TYP	MAX	UNITS
RESOLUTION					16			*	Bits
TEMPERATURE RANGE: H, HB	$T_{AMBIENT}$		−40		+70	*		*	°C
ANALOG INPUT									
Full Scale Input Range			−2.5		+2.5	*		*	V
Input Impedance				0.3 x 10^{12} ‖ 2			*		Ω ‖ pF
DIGITAL INPUTS									
Logic Family				TTL/HCT Compatible			*		
Start Conversion				Convert Command Rising Edge			*		
Convert Command Pulse Width	t = Conversion Period		10		t −20	*		*	ns
CONVERSION CHARACTERISTICS									
Sample Rate		Full	DC		2.5M	*		*	Samples/s
Data Latency				1			*		Convert Cycle
DC ACCURACY									
Gain Error		+25°C		0.3	0.7		0.2	0.5	% FSR
		Full		0.4	0.7		0.2	0.5	% FSR
Input Offset		+25°C		0.4	0.7		0.2	0.5	% FSR
		Full		0.4	0.7		0.3	0.5	% FSR
Power Supply Rejection	Delta +V_S = 5%	Full		±0.03	±0.07		*	*	% FSR/%
	Delta −V_S = 5%	Full		±0.01	±0.07		*	*	% FSR/%
DYNAMIC CHARACTERISTICS									
No Missing Codes		+25°C		Guaranteed			Guaranteed		
		Full		Typical			Guaranteed		
Differential Linearity Error									
f = 8kHz		+25°C		0.8	1.5		0.6	1.0	LSB
		Full		0.8	1.5		0.7	1.0	LSB
f = 1.0MHz		+25°C		0.9	1.5		0.7	1.0	LSB
		Full		0.9	1.5		0.8	1.0	LSB
Integral Linearity Error									
f = 8kHz		+25°C		0.0025	0.004		0.0015	0.0025	% FSR
		Full		0.003	0.006		0.002	0.003	% FSR
Spurious Free Dynamic Range (SFDR)									
f = 8kHz (−1dBFS Input)		+25°C	88	94		100	102		dBFS
		Full	85	92		97	100		dBFS
f = 1.0MHz (−1dBFS Input)		+25°C	85	88		90	92		dBFS
		Full	82	86		87	90		dBFS
Two-Tone Intermodulation Distortion									
f = 1.0 and 1.1MHz (−7dB each tone)		+25°C		−88			−91		dBFS
		Full		−86			−90		dBFS
Signal-to-Noise Ratio (SNR)									
f = 8kHz (−1dBFS Input)		+25°C	86	91		90	93		dB
		Full	85	91		89	93		dB
f = 1.0MHz (−1dBFS Input)		+25°C	84	88		87	91		dB
		Full	83	87		86	90		dB
SINAD									
f = 8kHz (−1dBFS Input)		+25°C	85	90		89	92		dB
		Full	84	90		88	92		dB
f = 1.0MHz (−1dBFS Input)		+25°C	84	89		87	91		dB
		Full	83	88		86	90		dB
Output Noise	Input Grounded	+25°C		1			*		LSBrms
Aperture Delay Time		+25°C		5			*		ns
Aperture Jitter		+25°C		5			*		ps rms
Analog Input Bandwidth (−3dB)									
Small Signal	−20dB Input	+25°C		30			*		MHz
Full Power	0dB Input	+25°C		5			*		MHz
Overload Recovery Time	2x Full Scale Input	+25°C		2			*		μs
OUTPUTS									
Logic Family				TTL/HCT Compatible			*		
Logic Coding	Logic Selectable			SOB or COB			*		
Logic Levels									
Logic "LO"		Full	0		0.5	*		*	V
Logic "HI"		Full	4	4.9		*	*		V
3-State Enable/Disable Time		Full		10	25		*	*	ns

ADS703

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS(CONT)

T_A = +25°C, $+V_S$ = +5V, $-V_S$ = –5.2V, ±2.5V Input Range, Sampling Rate = 2.5MHz unless otherwise noted.

PARAMETER	CONDITIONS	TEMPERATURE	ADS703H			ADS703HB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS									
Supply Voltages: $+V_S$	Operating	Full	+4.75	+5.0	+5.25	*	*	*	V
$-V_S$		Full	–5.46	–5.2	–4.94	*	*	*	V
Supply Currents: $+I_S$	Operating	Full		200			*		mA
$-I_S$		Full		300			*		mA
Power Consumption		Full		2.75	2.9		*	*	W
θ_{JC}		Full		TBD			*		°C/W
θ_{JA}	Still Air			TBD			*		°C/W

ABSOLUTE MAXIMUM RATINGS

$+V_S$ .... +6V
$-V_S$ .... 0.3V to –6V
Logic Inputs .... 0V to –5.5V
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +165°C
Lead Temperature (soldering, 10s) .... +300°C

NOTE: Stresses above these ratings may permanently damage the device.

PIN CONFIGURATION

Top View			DIP
Bit 1	1	40	GND
Bit 2	2	39	Analog Input
Bit 3	3	38	+5V
Bit 4	4	37	GND
Bit 5	5	36	–5V
Bit 6	6	35	Reference Input
Bit 7	7	34	Reference Output
Bit 8	8	33	Ref (Gain) Adjust
Bit 9	9	32	GND
Bit 10	10	31	Offset Adjust
Bit 11	11	30	+5V
Bit 12	12	29	GND
Bit 13	13	28	–5V
Bit 14	14	27	–5V
Bit 15	15	26	GND
Bit 16	16	25	+5V
No Internal Connection	17	24	Test/Trim Enable
No Internal Connection	18	23	Polarity Control
Over/Underrange	19	22	OUTPUT ENABLE
Convert Command	20	21	GND

PACKAGING INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS703H, HB	40-Pin, 0.5" Wide Hermetic DIP	214

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

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                                        ADS703  H  ( )

Basic Model Number ─────────────────────────────┘  │  │
Package Code ───────────────────────────────────────┘  │
Performance Grade Code ─────────────────────────────────┘
    No letter or "B" = –40°C to +70°C Ambient Temperature
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⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TIMING DIAGRAM

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Command Period	400			ns
t_{DV}	Data Valid After Convert Command	200	250		ns
t_X	Data Valid Time Before Convert Command	50	150		ns
t_{CCH}	Convert Command Pulse Width High	20		t_{CONV} −20	ns
t_{CCL}	Convert Command Pulse Width Low	20		t_{CONV} −20	ns

NOTE: The timescale applies for a 10MHz conversion rate. The "⌇" indicates the part of the timing waveform that will "stretch out" at slower conversion rates.

ADS703

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

ADS704

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

18-Bit 500kHz Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **HIGH SPURIOUS-FREE DYNAMIC RANGE: 100dB AT Nyquist**
● **HIGH SNR: 96dB**
● **NO MISSING CODES AT 18 BITS**
● **LOW NONLINEARITY: ±0.0015%**
● **PIN CONSISTENT WITH ADS610, ADS703: (14-Bit 10MHz, 16-Bit 2.5MHz)**
● **±2.5V ANALOG INPUT RANGE**
● **LOW POWER: 2.75Watts**
● **SMALL HERMETIC PACKAGE: 0.6" x 2.0"**

APPLICATIONS

● **MEDICAL IMAGING**
● **SPECTRUM ANALYZERS**
● **IR SPECTROMETERS**
● **CCD IMAGING**
● **ULTRASOUND SIGNAL PROCESSING**
● **SONAR SIGNAL PROCESSING**
● **AUTOMATIC TEST EQUIPMENT**
● **HIGH SPEED DATA ACQUISITION**

DESCRIPTION

The ADS704 is a very high speed, highly integrated 18-bit sampling A/D converter. It is designed for superior linearity, low noise and wideband spectral performance.

The ADS704 is a three-step subranging design containing a quantizer, sample/hold amplifier, voltage reference and timing circuitry in a slim 40-pin package. It is pin consistent with the ADS610 (14-bit 10MHz) and the

ADS703 (16-bit 2.5MHz) sampling ADC's, allowing the user to choose easily between speed and resolution. A convenient TTL-compatible logic interface is provided.

A demonstration board (DEM-ADS704) is available for quick evaluation.

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SPECIFICATIONS

T_A = +25°C, +V_S = +5V, −V_S = −5.2V, ±2.5V Input Range, Sampling Rate = 500kHz unless otherwise noted.

PARAMETER	CONDITIONS	TEMPERATURE	ADS704H MIN	ADS704H TYP	ADS704H MAX	ADS704HB MIN	ADS704HB TYP	ADS704HB MAX	UNITS
RESOLUTION					18			*	Bits
TEMPERATURE RANGE: H, HB	$T_{AMBIENT}$		−40		+85	*		*	°C
ANALOG INPUT									
Full Scale Input Range			−2.5		+2.5	*		*	V
Input Impedance				0.3 x 10¹² ‖ 2			*		Ω ‖ pF
DIGITAL INPUTS									
Logic Family				TTL/HCT Compatible			*		
Start Conversion				Convert Command Rising Edge			*		
Convert Command Pulse Width	t = Conversion Period		10		t −20	*		*	ns
CONVERSION CHARACTERISTICS									
Sample Rate	Full		DC		500k	*		*	Samples/s
Data Latency				1			*		Convert Cycle
DC ACCURACY									
Gain Error		Full		0.3	0.7		0.2	0.5	%FSR
Input Offset		Full		0.4	0.7		0.2	0.5	%FSR
Power Supply Rejection	Δ +V_S = 5%	Full		±0.03	±0.07		*	*	%FSR/%
	Δ −V_S = 5%	Full		±0.01	±0.07		*	*	%FSR/%
DYNAMIC CHARACTERISTICS									
No Missing Codes		+25°C		Guaranteed			Guaranteed		
		Full		Typical			Guaranteed		
Differential Linearity Error									
f = 8kHz		+25°C		0.8	1.5		0.6	1.0	LSB
		Full		0.8	1.5		0.7	1.0	LSB
f = 250kHz		+25°C		0.9	1.5		0.7	1.0	LSB
		Full		0.9	1.5		0.8	1.0	LSB
Integral Linearity Error									
f = 8kHz		+25°C		0.0025	0.004		0.0015	0.0025	%FSR
		Full		0.003	0.006		0.002	0.003	%FSR
Spurious Free Dynamic Range (SFDR)									
f = 8kHz (−1dBFS Input)		+25°C	88	94		100	102		dBFS
		Full	85	92		97	100		dBFS
f = 250kHz (−1dBFS Input)		+25°C	85	88		90	92		dBFS
		Full	82	86		87	90		dBFS
Two-Tone Intermodulation Distortion									
f = 200 and 210kHz (−7dB each tone)		+25°C		−88			−91		dBFS
		Full		−86			−90		dBFS
Signal-to-Noise Ratio (SNR)									
f = 8kHz (−1dBFS Input)		+25°C	90	93		91	96		dB
		Full	85	91		89	94		dB
f = 250kHz (−1dBFS Input)		+25°C	87	90		90	92		dB
		Full	84	89		87	91		dB
SINAD									
f = 8kHz (−1dBFS Input)		+25°C	85	90		89	92		dB
		Full	84	90		88	92		dB
f = 250kHz (−1dBFS Input)		+25°C	84	89		87	91		dB
		Full	83	88		86	90		dB
Output Noise	Input Grounded	+25°C		2			*		LSBrms
Aperture Delay Time		+25°C		5			*		ns
Aperture Jitter		+25°C		5			*		ps rms
Analog Input Bandwidth (−3dB)									
Small Signal	−20dB Input	+25°C		6			*		MHz
Full Power	0dB Input	+25°C		1			*		MHz
Overload Recovery Time	2x Full Scale Input	+25°C		2			*		μs
OUTPUTS									
Logic Family				TTL/HCT Compatible			*		
Logic Coding	Logic Selectable			SOB or COB			*		
Logic Levels									
Logic "LO"	I_{OL}<3.2mA	Full	0		0.5	*		*	V
Logic "HI"	I_{OH}<μA	Full	4.0	4.9		*	*		V
3-State Enable/Disable Time		Full		10	25		*	*	ns
POWER SUPPLY REQUIREMENTS									
Supply Voltages: +V_S	Operating	Full	+4.75	+5.0	+5.25	*	*	*	V
−V_S		Full	−5.46	−5.2	−4.94	*	*	*	V
Supply Currents: +I_S	Operating	Full		150			*		mA
−I_S		Full		425			*		mA
Power Consumption		Full		2.75	2.9		*	*	W
θ_{JC}				TBD			*		°C/W
θ_{JA}	Still Air			TBD			*		°C/W

ADS704

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

ABSOLUTE MAXIMUM RATINGS

+V$_S$ .... +6V
−V$_S$ .... 0.3V to −6V
Logic Inputs .... 0V to −5.5V
Junction Temperature .... +165°C
Storage Temperature .... −65°C to +165°C
Lead Temperature (soldering, 10s) .... +300°C

NOTE: Stresses above these ratings may permanently damage the device.

PIN CONFIGURATION

Top View		DIP
Bit 1	1	40 GND
Bit 2	2	39 Analog Input
Bit 3	3	38 +5V
Bit 4	4	37 GND
Bit 5	5	36 −5V
Bit 6	6	35 Reference Input
Bit 7	7	34 Reference Output
Bit 8	8	33 Ref (Gain) Adjust
Bit 9	9	32 GND
Bit 10	10	31 Offset Adjust
Bit 11	11	30 +5V
Bit 12	12	29 GND
Bit 13	13	28 −5V
Bit 14	14	27 −5V
Bit 15	15	26 GND
Bit 16	16	25 +5V
Bit 17	17	24 Test/Trim Enable
Bit 18	18	23 Polarity Control
Over/Underrange	19	22 Output Enable
Convert Command	20	21 GND

PACKAGING INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS704H, HB	40-Pin, 0.6" Wide Hermetic DIP	214

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

ADS704 H (_)

Basic Model Number
Package Code
Performance Grade Code
    No letter or "B" = −40°C to +70°C Ambient Temperature

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TIMING DIAGRAM

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Command Period	2000			ns
t_{CCH}	Convert Command Pulse Width High	20		$t_{CONV}-20$	ns
t_{CCL}	Convert Command Pulse Width Low	20		$t_{CONV}-20$	ns
t_{DV}	Data Valid After Convert Command	800	1250		ns
t_X	Data Valid Before Convert Command	400	750		ns

ADS704

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

BB

ADS774

Microprocessor-Compatible Sampling
CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

● **COMPATIBLE WITH ADC574, ADC674 AND ADC774 SOCKETS**

● **COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE**

● **FAST ACQUISITION AND CONVERSION: 8.5μs max OVER TEMPERATURE**

● **ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS**

● **GUARANTEED AC AND DC PERFORMANCE**

● **SINGLE +5V SUPPLY OPERATION**

● **LOW POWER: 120mW max**

● **PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC**

DESCRIPTION

The ADS774 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574, ADC674, and ADC774 models in most applications, with internal sampling, much lower power consumption, and the ability to operate from a single +5V supply.

The ADS774 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time is 8.5μs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS774 is available in both commercial (0°C to +70°C) and military (–55°C to +125°C) ranges, and requires +5V, with –15V optional. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic or hermetic ceramic DIPs, and 28-pin SOICs.

PDS-1109D

BURR - BROWN®

BB

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = +5V$, $V_{EE} = -15V$ to $+5V$, sampling frequency of 117kHz, $f_{IN} = 10kHz$; unless otherwise specified.

PARAMETER	ADS774JE/JH/JP/JU/SF/SH/D			ADS774KE/KH/KP/KU/TF/TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	8.5	12		*	*		kΩ
±10V, 0V to +20V	35	50		*	*		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	μA
Capacitance		5		*			pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1]			±0.25			*	% of FS [2]
(adjustable to zero)							
No Missing Codes Resolution	12			12			Bits
T_{MIN} to T_{MAX} [3]							
Linearity Error: A, J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error: A, J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Unipolar Offset: A, J, K Grades			±4			±3	LSB
S, T Grades			±4			±3	LSB
Bipolar Offset: A, J, K Grades			±12			±5	LSB
S, T Grades			±14			±6	LSB
No Missing Codes Resolution	12			12			Bits
AC ACCURACY [4]							
Spurious Free Dynamic Range	73	78		76	*		dB
Total Harmonic Distortion		−77	−72		*	−75	dB
Signal-to-Noise Ratio	69	72		71	*		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	*		dB
Intermodulation Distortion		−75			*		
($F_{IN1} = 20kHz$, $F_{IN2} = 23kHz$)							
TEMPERATURE COEFFICIENTS [5]							
Unipolar Offset		±1			*		ppm/°C
Bipolar Offset		±2			*		ppm/°C
Full-Scale Calibration		±12			*		ppm/°C
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration [6]							
+4.75V < V_{DD} < +5.25V							
Max Change: J, K Grades		±1/2			*		LSB
S, T Grades		±1			*		LSB
CONVERSION TIME (Including Acquisition Time)							
$t_{AQ} + t_C$ at 25°C:							
8-Bit Cycle		5.5	5.9		*	*	μs
12-Bit Cycle		7.5	8		*	*	μs
12-Bit Cycle, T_{MIN} to T_{MAX}:		8	8.5		*	*	μs

ADS774

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = +5V$, $V_{EE} = -15V$ to $+5V$, sampling frequency of 117kHz, $f_{IN} = 10kHz$; unless otherwise specified.

PARAMETER	ADS774JE/JH/JP/JU/SF/SH/D			ADS774KE/KH/KP/KU/TF/TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
SAMPLING DYNAMICS							
Sampling Rate at 25°C	125			*			kHz
T_{MIN} to T_{MAX}	117			*			kHz
Aperture Delay, t_{AP}							
With $V_{EE} = +5V$		20			*		ns
With $V_{EE} = 0V$ to $-15V$		1.6			*		μs
Aperture Uncertainty (Jitter)							
With $V_{EE} = +5V$		300			*		ps, rms
With $V_{EE} = 0V$ to $-15V$		10			*		ns,rms
Settling time to 0.01% for		1.4			*		μs
Full-Scale Input Change							
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500μA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	-5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} [(7)]	-16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} [(7)] (V_{EE} = -15V)		-1			*		mA
I_{DD}		+15	+24		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX})							
(V_{EE} = 0V to +5V)		75	120		*	*	mW
TEMPERATURE RANGE							
Specification: J, K Grades	0		+70	*		*	°C
S, T Grades	-55		+125	*		*	°C
Operating: J, K Grades	-40		+85	*		*	°C
S, T Grades	-55		+125	*		*	°C
Storage Temperature Range	-65		+150	*		*	°C

*Same specification as ADS774JE/JH/JP/JU/SF/SH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at T_{MIN} and T_{MAX}. (4) Based on using $V_{EE} = +5V$, which is the Control Mode. See the section "S/H Control Mode and ADC774 Emulation Mode." (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When $V_{EE} = -15V$, $I_{EE} = -1mA$ typ; when $V_{EE} = 0V$, $I_{EE} = ±5μA$ typ; when $V_{EE} = +5V$, $I_{EE} = +167μA$ typ.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common .... $+V_{DD}$ to $-16.5V$
V_{DD} to Digital Common .... 0V to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
  to Digital Common .... $-0.5V$ to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$)
  to Analog Common .... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V
Ref Out .... Indefinite Short to Common,
                                                               Momentary Short to V_{DD}
Max Junction Temperature .... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) .... +300°C
Thermal Resistance, θ_{JA} : Ceramic DIPs .... 50°C/W
                                  Plastic DIPs .... 100°C/W
                                  SOIC .... 100°C/W

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS774JE	28-pin 0.3" Plastic DIP	246
ADS774KE	28-pin 0.3" Plastic DIP	246
ADS774JH	28-pin 0.6" Ceramic DIP	149
ADS774KH	28-pin 0.6" Ceramic DIP	149
ADS774JP	28-pin 0.6" Plastic DIP	215
ADS774KP	28-pin 0.6" Plastic DIP	215
ADS774JU	28-pin SOIC	217
ADS774KU	28-pin SOIC	217
ADS774SF	28-pin 0.3" Ceramic DIP	247
ADS774TF	28-pin 0.3" Ceramic DIP	247
ADS774SH	28-pin 0.6" Ceramic DIP	149
ADS774TH	28-pin 0.6" Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	SINAD[1]	TEMPERATURE RANGE	LINEARITY ERROR
ADS774JE	0.3" Plastic DIP	68dB	0°C to +70°C	±1LSB
ADS774KE	0.3"Plastic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JH	0.6" Ceramic DIP	68dB	0°C to +70°C	±1LBB
ADS774KH	0.6" Ceramic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JP	0.6" Plastic DIP	68dB	0°C to +70°C	±1LSB
ADS774KP	0.6"Plastic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JU	SOIC	68dB	0°C to +70°C	±1LSB
ADS774KU	SOIC	70dB	0°C to +70°C	±1/2LSB
ADS774SF	0.3" Ceramic DIP	68dB	−55°C to +125°C	±1LSB
ADS774TF	0.3" Ceramic DIP	70dB	−55°C to +125°C	±1/2LSB
ADS774SH	0.6" Ceramic DIP	68dB	−55°C to +125°C	±1LSB
ADS774TH	0.6" Ceramic DIP	70dB	−55°C to +125°C	±1/2LSB

NOTE: (1) SINAD is Signal to (Noise and Distortion) expressed in dB.

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CONNECTION DIAGRAM

*Not Internally Connected
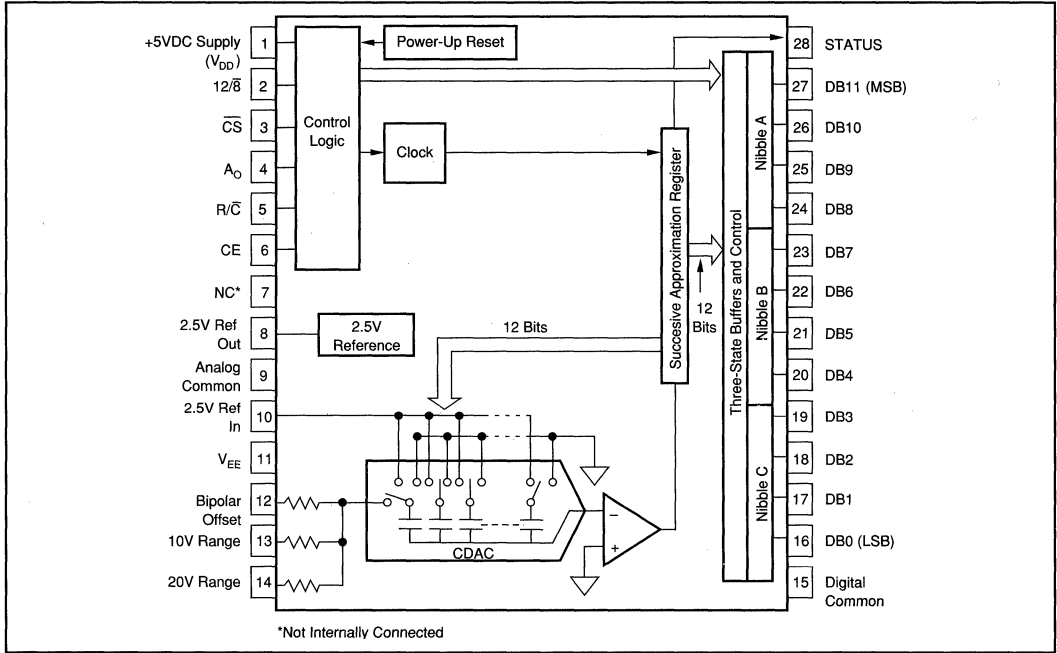
DICE INFORMATION

ADS774 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	V_{DD}	15	Digital Common
2	12/$\overline{8}$	16	DB0 (LSB)
3	$\overline{CS}$	17	DB1
4	A_0	18	DB2
5	R/$\overline{C}$	19	DB3
6	CE	20	DB4
7	NC	21	DB5
8	2.5V Ref Out	22	DB6
9A, 9B	Analog Common	23	DB7
10	2.5 Ref In	24	DB8
11	V_{EE} (Mode Control)	25	DB9
12	Bipolar Offset	26	DB10
13	10V Range	27	DB11 (MSB)
14	20V Range	28	Status

Substrate Bias: $+V_{DD}$
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	172 x 142 ±5	4.37 x 3.61 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization	Aluminum	

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 110kHz; unless otherwise specified. All plots use 4096 point FFTs.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FREQUENCY SPECTRUM (±10V, 2kHz Input)

S/(N + D) = 72.6dB
THD = –93.5dB
SNR = 72.6dB

SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY AND AMBIENT TEMPERATURE

FREQUENCY SPECTRUM (±10V, 20kHz Input)

S/(N + D) = 70.6dB
THD = –77.5dB
SNR = 71.5dB

FREQUENCY SPECTRUM (±1V, 20kHz Input)

S/(N + D) = 53.1dB
THD = –74.2dB
SNR = 53.1dB

SPURIOUS FREE DYNAMIC RANGE, SNR AND THD vs INPUT FREQUENCY

Spurious Free Dynamic Range

Total Harmonic Distrotion (THD)

Signal-to-Noise Ratio (SNR)

POWER SUPPLY REJECTION vs SUPPLY RIPPLE FREQUENCY

THEORY OF OPERATION

In the ADS774, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_c is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_c is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then

latch S_1 in position "R" or "G". Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the ADS774 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS774 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS774.

The ADS774 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS774 is designed to complete a conversion and accurately acquire a new signal in 8.5μs max over the full operating temperature range, so that conversions can take place at a full 117kHz.

CONTROLLING THE ADS774

The Burr-Brown ADS774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/C̄ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/8̄, C̄S̄, A_0, R/C̄, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/C̄. In this mode C̄S̄ and A_0 are connected to digital common and CE and 12/8̄ are connected to +5V. The output data are

FIGURE 2. Basic ±10V Operation.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion

will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs ($\overline{CE}$, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	±5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ $n = 8$ $n = 12$	$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (– Full-Scale Calibration)	+10V – 3/2LSB 0V – 1/2LSB –10V + 1/2LSB	+5V – 3/2LSB 0V – 1/2LSB –5V + 1/2LSB	+10V – 3/2LSB +5V – 1/2LSB 0V +1/2LSB	+20V – 3/2LSB +10V – 1/2LSB 0V +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be LOW ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the HIGH or LOW condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS774 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

FIGURE 3. R/C̄ Pulse Low—Outputs Enabled After Conversion.

FIGURE 4. R/C̄ Pulse High — Outputs Enabled Only While R/C̄ Is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C̄ Pulse Width	25			ns
t_{DS}	STS Delay from R/C̄			200	ns
t_{HDR}	Data Valid After R/C̄ Low	25			ns
t_{HRH}	High R/C̄ Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	C̄S̄ to CE setup	50	20		ns
t_{HSC}	C̄S̄ low during CE high	50	20		ns
t_{SRC}	R/C̄ to CE setup	50	0		ns
t_{HRC}	R/C̄ low during CE high	50	20		ns
t_{SAC}	A₀ to CE setup	0			ns
t_{HAC}	A₀ valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	C̄S̄ to CE setup	50	0		ns
t_{SRR}	R/C̄ to CE setup	0			ns
t_{SAR}	A₀ to CE setup	50	25		ns
t_{HSR}	C̄S̄ valid after CE low	0			ns
t_{HRR}	R/C̄ high after CE low	0			ns
t_{HAR}	A₀ valid after CE low	50			ns
t_{HS}	STATUS delay after data valid	75	150	375	ns

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).
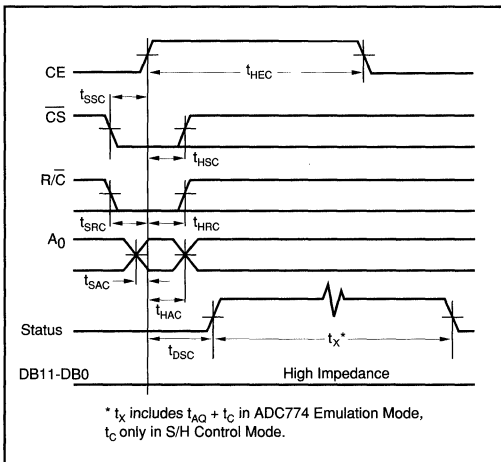
* t_X includes $t_{AQ} + t_C$ in ADC774 Emulation Mode, t_C only in S/H Control Mode.
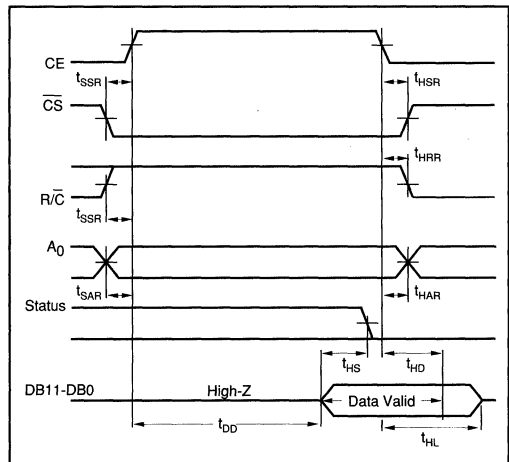
FIGURE 5. Conversion Cycle Timing.

FIGURE 6. Read Cycle Timing.

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	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.
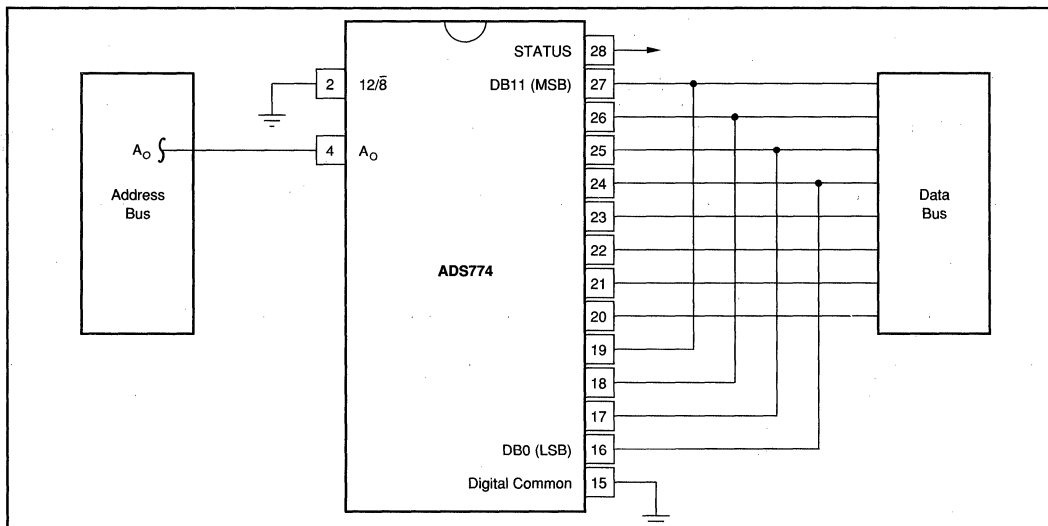
FIGURE 8. Connection to an 8-Bit Bus.

S/H CONTROL MODE
AND ADC774 EMULATION MODE

The Emulation Mode allows the ADS774 to be dropped into most existing ADC774 sockets without changes to other system hardware or software. In existing sockets, the analog input is held stable during the conversion period so that accurate conversions can proceed, but the input can change rapidly at any time before the conversion starts. The Emulation Mode uses the stability of the analog input during the conversion period to both acquire and convert in a maximum of 8µs (8.5µs over temperature.) In fact, system throughput can be increased, since the input to the ADS774 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC774s.

The Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS774 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode, it is assumed that during the required 1.4µs acquisition time the signal is not changing faster than the ADS774 can track. No assump-

tion is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command. This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized in the Control Mode, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, a delay time is introduced between the convert command and the start of conversion to allow the ADS774 enough time to acquire the input signal before converting. This increases the effective aperture delay time from 0.02µs to 1.6µs, but allows the ADS774 to replace the ADC774 in most circuits without additional changes. In designs where the input to the ADS774 is changing rapidly in the 200ns prior to a convert command, system performance may be enhanced by delaying the convert command by 200ns.

When using the ADS774 in the Emulation Mode to replace existing converters in current designs, a sample/hold amplifier often precedes the converter. In these cases, no additional delay in the convert command will be needed. The existing sample/hold will not be slewing excessively when going from the sample mode to the hold mode prior to a conversion.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

The speed of the ADS774 requires special caution regarding whichever input pin is unused. For 10V input ranges, pin 14 (20V Range) must be unconnected, and for 20V input ranges, pin 13 (10V Range) must be unconnected. In both cases, the unconnected input should be shielded with ground plane to reduce noise pickup.

In particular, the unused input pin should not be connected to any capacitive load, including high impedance switches. Even a few pF on the unused pin can degrade acquisition time.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS774.

POWER SUPPLY DECOUPLING

On the ADS774, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC774 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC774 socket, the –15V on pin 11 selects the ADC774 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

SYMBOL	PARAMETER	S/H CONTROL MODE (Pin 11 Connected to +5V)			ADC774 EMULATION MODE (Pin 11 Connected to 0V to –15V)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		8	8.5		8	8.5	μs
	8-bit Conversions		6	6.3		6	6.3	μs
t_C	Conversion Time:							
	12-bit Conversions		6.4			6.4		μs
	8-bit Conversions		4.4			4.4		μs
t_{AQ}	Acquisition Time		1.4			1.4		μs
t_{AP}	Aperture Delay		20			1600		ns
t_J	Aperture Uncertainty		0.3			10		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.
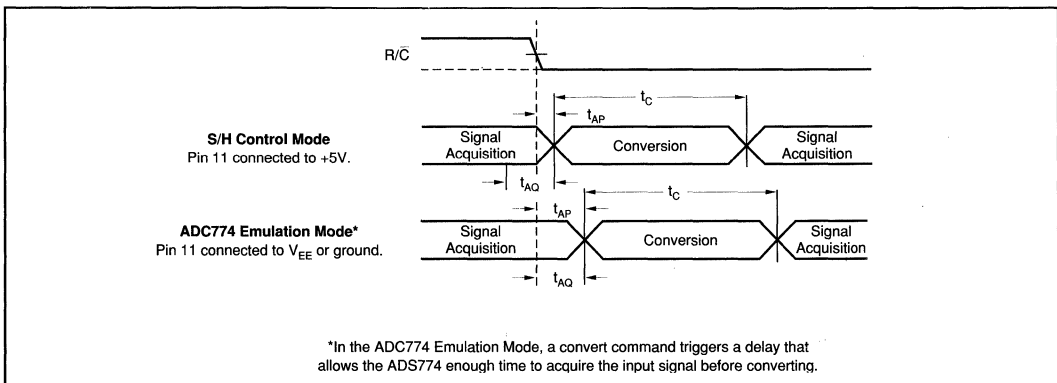
FIGURE 9. Signal Acquisition and Conversion Timing.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS
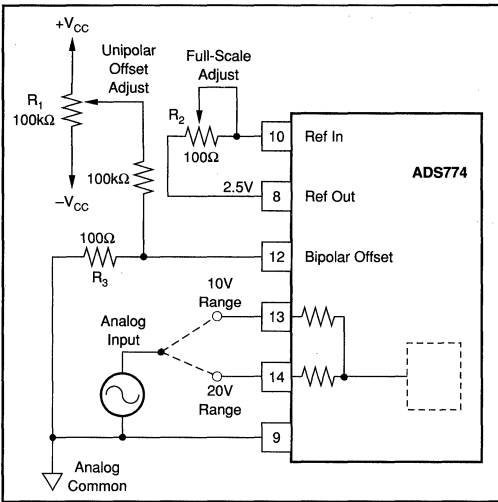
FIGURE 10. Unipolar Configuration.
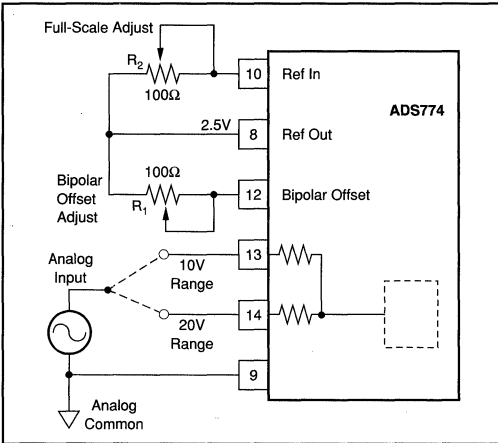
FIGURE 11. Bipolar Configuration.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of

the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS774 is typically 50kΩ in the 20V ranges and 12kΩ in the 10V ranges. This is significantly higher than that of traditional ADC774 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS774. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high impedance node as compared with traditional ADC774 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS774 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected to pin 9, analog common. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (42kΩ + 42kΩ || 10.5kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide the same offset adjust response as that of traditional ADC774 architectures without changing the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS774 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is
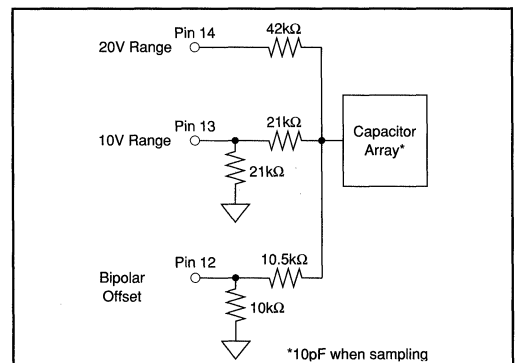
FIGURE 12. ADS774 Input Structure.

where +12V or +15V is supplied on traditional ADC774s. Pin 11, the −12V or −15V supply input on traditional ADC774s, is used only as a logic input on the ADS774. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS774, and this resistor will add 10mW to 15mW to the power consumption of the ADS774 when −15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS774 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS774 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 10 with a 50Ω 1% metal film resistor and connect pin 12 to pin 9, omitting the other adjustment components.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, replace the potentiometers in Figure 11 by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

ADS774

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

ADS7800

12-Bit 3μs Sampling
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **333k SAMPLES PER SECOND**

● **STANDARD ±10V AND ±5V INPUT RANGES**

● **DC PERFORMANCE OVER TEMP:**
  No Missing Codes
  1/2LSB Integral Linearity Error
  3/4LSB Differential Linearity Error

● **AC PERFORMANCE OVER TEMP:**
  72dB Signal-to-Noise Ratio
  80dB Spurious-free Dynamic Range
  −80dB Total Harmonic Distortion

● **INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND 3-STATE OUTPUTS**

● **POWER DISSIPATION: 215mW max**

● **PACKAGE: 24-Pin Single-wide DIP**
  24-Lead SOIC

DESCRIPTION

The ADS7800 is a complete 12-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70μs max over temperature, and the high speed sampling input stage insures a total acquisition and conversion time of 3μs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a −12V or −15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and −40°C to +85°C temperature ranges.

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH/D MIN	ADS7800JP/JU/AH/D TYP	ADS7800JP/JU/AH/D MAX	ADS7800KP/KU/BH MIN	ADS7800KP/KU/BH TYP	ADS7800KP/KU/BH MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V/±5V			*		V
Impedance	±10V Range	4.4	6.3	8.1	*	*	*	kΩ
	±5V Range	2.9	4.2	5.4	*	*	*	kΩ
THROUGHPUT SPEED								
Conversion Time	Conversion Alone		2.5	2.7		*	*	μs
Complete Cycle	Acquisition + Conversion		2.6	3.0		*	*	μs
Throughput Rate		333	380		*	*		kHz
DC ACCURACY								
Full Scale Error [1]				±0.50			±0.35	%
Full Scale Error Drift			6			*		ppm/°C
Integral Linearity Error				±1			±1/2	LSB [2]
Differential Linearity Error				±1			±3/4	LSB
No Missing Codes			Guaranteed			Guaranteed		
Bipolar Zero [1]				±4			±2	LSB
Bipolar Zero Drift			1			*		ppm/°C
Power Supply Sensitivity								
	$-16.5V < -V_S < -13.5V$			±1/2			*	LSB
	$-12.6V < -V_S < -11.4V$			±1/2			*	LSB
	$+4.75V < V_S < +5.25V$			±1			±1/2	LSB
Transition Noise [3]			0.1			*		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 47kHz$	74	77		77	80		dB [4]
Total Harmonic Distortion	$f_{IN} = 47kHz$		−77	−74		−80	−77	dB
Two-tone Intermodulation Distortion	$f_{IN1} = 24.4kHz$ (−6dB)		−77	−74		−80	−77	dB
	$f_{IN2} = 28.5kHz$ (−6dB)							
Signal to (Noise + Distortion) Ratio	$f_{IN} = 47kHz$	67	70		69	72		dB
Signal to Noise Ratio (SNR)	$f_{IN} = 47kHz$	68	71		70	73		dB
SAMPLING DYNAMICS								
Aperture Delay			13			*		ns
Aperture Jitter			150			*		ps,rms
Transient Response [5]			130			*		ns
Overvoltage Recovery [6]			150			*		ns
INTERNAL REFERENCE VOLTAGE								
Voltage		1.9	2.0	2.1	*	*	*	V
Source Current Available			10			*		μA
for External Loads								
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.4		+5.3	*		*	V
I_{IL}		−5			*			μA
I_{IH}		+5			*			μA
DIGITAL OUTPUTS								
Data Format			Parallel, 12-bit or 8-bit/4-bit					
Data Coding			Binary Offset Binary					
V_{OL}	$I_{SINK} = 1.6mA$	0.0		+0.4	*		*	V
V_{OH}	$I_{SOURCE} = 500μA$	+2.4		+5.0	*		*	V
$I_{LEAKAGE}$ (High-Z State)			±0.1	±5		*	*	μA
POWER SUPPLIES								
Rated Voltage								
$-V_S$		−11.4	−15	−16.5	*	*	*	V
V_S (V_{SA} and V_{SD})		+4.75	+5.0	+5.25	*	*	*	V
Current								
$-I_S$			3.5	6		*	*	mA
I_S			18	25		*	*	mA
Power Consumption			135	215		*	*	mW

ADS7800

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S$ = −15V, V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH/D			ADS7800KP/KU/BH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	JP/JU/KP/KU/D	0		+70	*		*	°C
	AH/BH	−40		+85	*		*	°C
Operating	JP/KP/JU/KU/D	−40		+85	*		*	°C
Storage		−65		+150	*		*	°C

* Same as specification for ADS7800JP/JU/AH.
NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the ±5V range, 1LSB = 4.88mV for the ±10V range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C. (4) All specifications in dB are referred to a full-scale input, either ±10V or ±5V. (5) For full-scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after 2 x F_S input overvoltage.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	IN1	±10V Analog Input. Connected to GND for ±5V range.
2	IN2	±5V Analog Input. Connected to GND for ±10V range.
3	REF	+2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads.
4	AGND	Analog Ground. Connect to pin 13.
5	D11	Data Bit 11. Most Significant Bit (MSB).
6	D10	Data Bit 10.
7	D9	Data Bit 9.
8	D8	Data Bit 8.
9	D7	Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.
10	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
11	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
12	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
13	DGND	Digital Ground. Connect to pin 4.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH.
18	HBE	High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion.
19	R/C̄	Read/Convert. Falling edge initiates conversion when CS is LOW, HBE is LOW, and BUSY is HIGH.
20	C̄S̄	Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.
21	B̄U̅S̄Y̅	Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode.
22	−V_S	Negative Power Supply. −12V or −15V. Bypass to GND.
23	V_SD	Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND.
24	V_SA	Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND.

ABSOLUTE MAXIMUM RATINGS

−V_S to ANALOG COMMON .... −16.5V
V_S to DIGITAL COMMON .... +7V
Pin 23 (V_SD) to Pin 24 (V_SA) .... ±0.3V
ANALOG COMMON to DIGITAL COMMON .... ±1V
Control Inputs to DIGITAL COMMON .... −0.3 to V_S + 0.3V
Analog Input Voltage .... ±20V
Maximum Junction Temperature .... 160°C
Internal Power Dissipation 750mW
Lead Temperature (soldering, 10s) .... +300°C
Thermal Resistance, θ_{JA}:
    Plastic DIP .... 100°C/W
    SOIC .... 100°C/W
    Ceramic .... 50°C/W

PIN CONFIGURATION

Top View   DIP/SOIC

IN1	1	24 V_SA
IN2	2	23 V_SD
REF	3	22 −V_S
AGND	4	21 B̄U̅S̄Y̅
D11	5	20 C̄S̄
D10	6	19 R/C̄
D9	7	18 HBE
D8	8	17 D0
D7	9	16 D1
D6	10	15 D2
D5	11	14 D3
D4	12	13 DGND
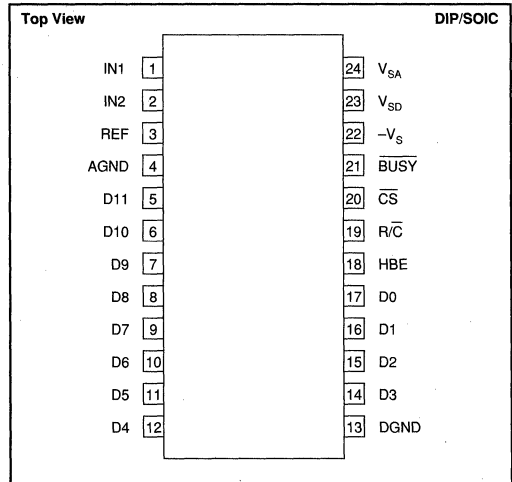
TYPICAL PERFORMANCE CURVES

+V_S = +5V, –V_S = –15V, and T_A = +25°C, unless otherwise noted. All plots use 1024 point FFTs.
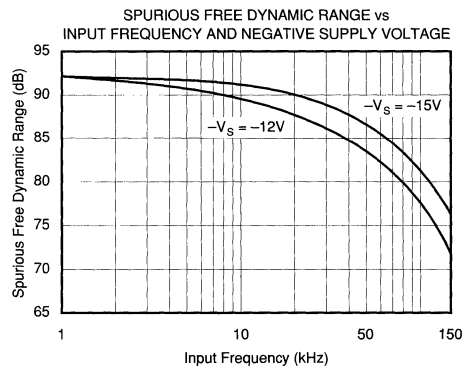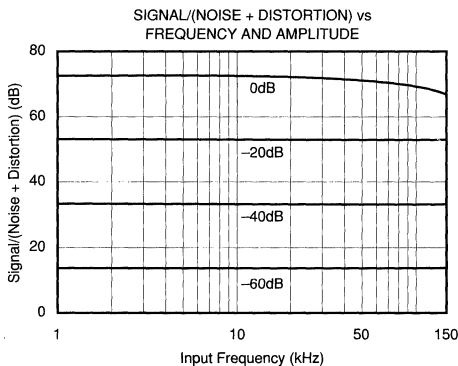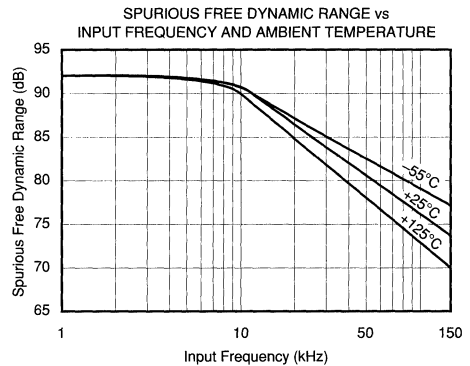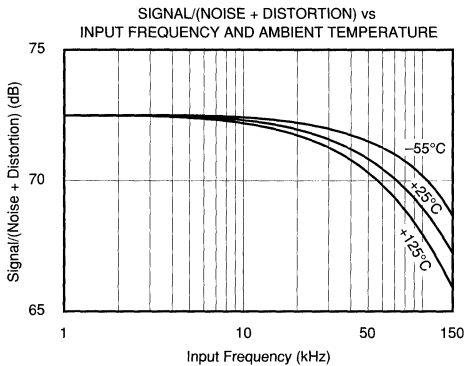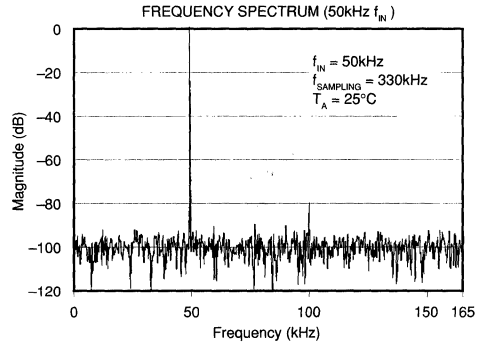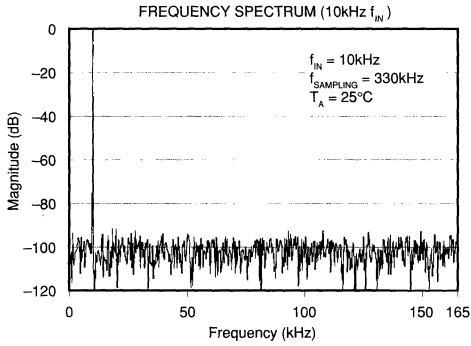
FREQUENCY SPECTRUM (10kHz f_{IN})

f_{IN} = 10kHz
$f_{SAMPLING}$ = 330kHz
T_A = 25°C

FREQUENCY SPECTRUM (50kHz f_{IN})

f_{IN} = 50kHz
$f_{SAMPLING}$ = 330kHz
T_A = 25°C

SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE

–55°C
+25°C
+125°C

SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE

–55°C
+25°C
+125°C

SIGNAL/(NOISE + DISTORTION) vs
FREQUENCY AND AMPLITUDE

0dB
–20dB
–40dB
–60dB

SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND NEGATIVE SUPPLY VOLTAGE

–V_S = –15V
–V_S = –12V

ADS7800

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

DICE INFORMATION
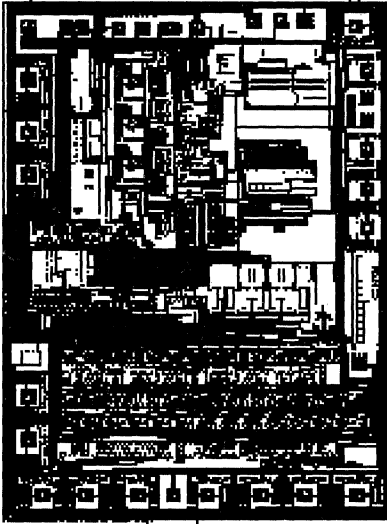
ADS7800 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	±10V Analog Input	15	D_2
2	±5V Analog Input	16	D_1
3	+2V Reference Output	17	D_0
4a	Analog Ground Sense[1]		
4b	Analog Ground [1]		
5	D_{11}(MSB)	18	HBE
6	D_{10}	19	R/E
7	D_9		
8	D_8		
9	D_7	20	$\overline{CS}$
10	D_6	21	$\overline{BUSY}$
11	D_5		
12	D_4	22	$-V_S$
13	Digital Ground	23	$+V_{SD}$
14	D_3	24	V_{SA}

NOTE: Bond pads 4 and 5 to same pin.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	136 x 181 ±5	3.45 x 4.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10

ORDERING INFORMATION

MODEL	INTEGRAL LINEARITY ERROR (LSB)	SIGNAL-TO- (NOISE+DISTORTION) RATIO (dB min)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7800JP	±1	67	0 to +70	Plastic DIP
ADS7800KP	±1/2	69	0 to +70	Plastic DIP
ADS7800JU	±1	67	0 to +70	Plastic SOIC
ADS7800KU	±1/2	69	0 to +70	Plastic SOIC
ADS7800AH	±1	67	−40 to +85	Ceramic DIP
ADS7800BH	±1/2	69	−40 to +85	Ceramic DIP

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7800JP	24-Pin Plastic DIP	243
ADS7800JP	24-Pin Plastic DIP	243
ADS7800JU	24-Pin Plastic SOIC	239
ADS7800KU	24-Pin Plastic SOIC	239
ADS7800AH	24-Pin Ceramic DIP	245
ADS7800BH	24-Pin Ceramic DIP	245

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

THEORY OF OPERATION

The ADS7800 combines the advantages of advanced CMOS technology (logic density, stable capacitors, and good analog switches) with Burr-Brown's proven skills in laser-trimmed thin-film resistors to provide a complete sampling analog-to-digital converter.

A basic charge-redistribution successive approximation architecture converts analog input voltages into digital words. Figure 1 shows the operation of a simplified three bit charge redistribution A-to-D. Precision laser-trimmed scaling resistors at the input divide standard input ranges (±10V or ±5V for the ADS7800) into levels compatible with the CMOS characteristics of the internal capacitor array.

While in the sampling mode, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal, and the remaining array switches (S_2 and S_3) are set to position "R" to provide an accurate bipolar offset from the reference source REF. At the same time, switch S_C is also in the closed position to auto-zero any offset errors in the CMOS comparator.

When a convert command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command, switches S_2 and S_3 are opened to trap an offset charge, and switch S_C is opened to float the comparator input. The charge trapped on the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2 and S_3 to positions "R" (to connect to REF) or "G" (to connect to GND) successively, changing the voltage generated at the comparator input node.

The first approximation connects the MSB capacitor via switch S_1 to REF, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G", and moves on to make the next approximation by connecting S_2 to REF and S_3 to GND. When the three successive approximation steps are made for this simple converter, the voltage level at the comparator will be within 1/2LSB of GND, and the data output word will be based on reading the positions of S_1, S_2 and S_3.
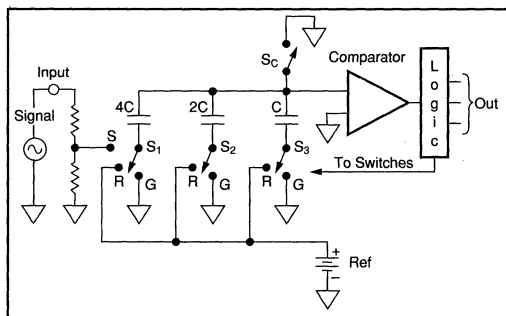
FIGURE 1. 3-Bit Charge Redistribution A-to-D.
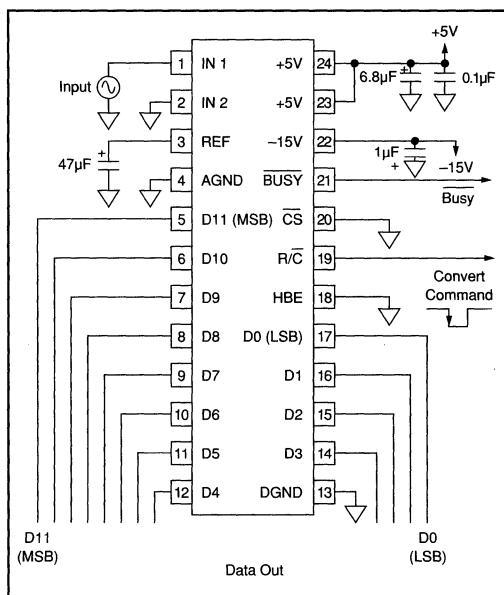
FIGURE 2. Basic ±10V Operation.

OPERATION

BASIC OPERATION

Figure 2 shows the simple hookup circuit required to operate the ADS7800 in a ±10V range in the Convert Mode. A convert command arriving on pin 19, R/$\overline{C}$, (a pulse taking pin 19 LOW for a minimum of 40ns) puts the ADS7800 in the hold mode, and a conversion is started. Pin 21, $\overline{BUSY}$, will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output latches. Thus, the rising edge of the signal on pin 21 can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits input lines. This means that pulses on pin 19 are ignored, so that new conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the ADS7800.

In the Read Mode, the input to pin 19 is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ on pin 19 will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the ADS7800 in a hold mode, and initiates a new conversion.

The ADS7800 will begin acquiring a new sample as soon as the conversion is completed, even before the BUSY output rises on pin 21, and will track the input signal until the next conversion is started, whether in the Convert Mode or the Read Mode.

ADS7800

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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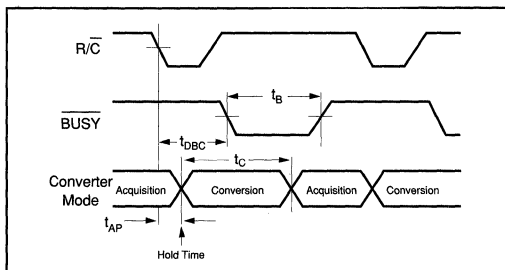
FIGURE 3. Acquisition and Conversion Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

TABLE I. Acquisition and Conversion Timing.

For use with an 8-bit bus, the data can be read out in two bytes under the control of pin 18, HBE. With a LOW input on pin 18, at the end of a conversion, the 8 LSBs of data are loaded into the latches on pins 9 through 12 and 14 through 17. Taking pin 18 HIGH then loads the 4 MSBs on pins 14 through 17, with pins 9 through 12 being forced LOW.

ANALOG INPUT RANGES

The ADS7800 offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration. (See Figures 4 and 5, or 10 and 11.)

CONTROLLING THE ADS7800

The ADS7800 can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the ADS7800 may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in Table II.

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	OPERATION
1	X	X	1	None - Outputs in Hi-Z State.
0	1↓0	0	1	Holds Signal and Initiates Conversion.
0	1	0	1	Output Three-State Buffers Enabled once Conversion has Finished.
0	1	1	1	Enable Hi-Byte in 8-bit Bus Mode.
0	1↓0	1	1	Inhibit Start of Conversion.
0	0	1	1	None - Outputs in Hi-Z State.
X	X	X	0	Conversion in Progress. Outputs Hi-Z State. New Conversion Inhibited until Present Conversion has Finished.

TABLE II. Control Line Functions.

For stand-alone operation, control of the ADS7800 is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition on R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and $\overline{BUSY}$ is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain LOW a minimum of 40ns.

Figure 6 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access of the data after completion of the conversion.

Figure 7 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

CONVERSION START

A conversion is initiated on the ADS7800 only by a negative transition occurring on R/$\overline{C}$, as shown in Table I. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$. Timing relationships for start of conversion are illustrated in Figure 8.

The $\overline{BUSY}$ output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

INTERNAL CLOCK

The ADS7800 has an internal clock that is factory trimmed to achieve a typical conversion time of 2.47μs, and a maximum conversion time over the full operating temperature range of 2.7μs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3μs.

READING DATA

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{\text{C}}$ is HIGH, $\overline{\text{BUSY}}$ is HIGH and $\overline{\text{CS}}$ is LOW. Upon satisfaction of these conditions, the data lines are enabled according to the state of HBE. See Figure 9 and Table III for timing relationships and specifications.

CALIBRATION

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS7800 as shown in Figures 10 and 11.

If adjustment of offset and full scale is not required, connections as shown in Figures 4 and 5 should be used.
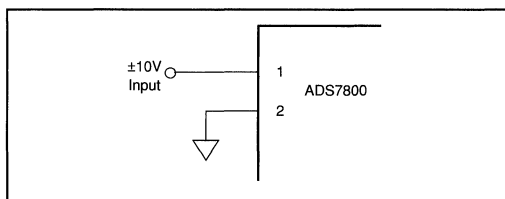
FIGURE 4. ±10V Range Without Trims.
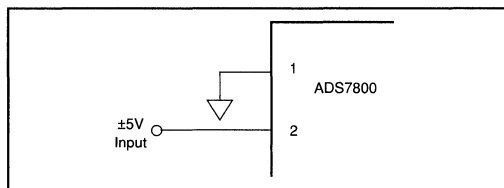
FIGURE 5. ±5V Range Without Trims.

CALIBRATION PROCEDURE

First, trim offset, by applying at the input (pin 1 or 2) the mid-point transition voltage (–2.44mV for the ±10V range, –1.22mV for the ±5V range.) With the ADS7800 converting continually, adjust potentiometer R_1 until the MSB (D11 on pin 5) is toggling alternately HIGH and LOW.

Next adjust full scale, by applying at the input a DC input signal that is 3/2LSB below the nominal full scale voltage (+9.9927V for the ±10V range, +4.9963V for the ±5V range.) With the ADS7800 converting continually, adjust R_2 until the LSB (D0 on pin 17) is toggling HIGH and LOW with all of the other bits HIGH.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADS7800, system design problems such as ground path resistance and contact resistance become very important.

ANALOG SIGNAL SOURCE IMPEDANCE

The input resistance of the ADS7800 is 6.3kΩ or 4.2kΩ (for the ±10V and ±5V ranges respectively.) To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal.

Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the ADS7800, to maximize accuracy on the chip. They should be connected together as close as possible to the unit.

ADS7800

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS
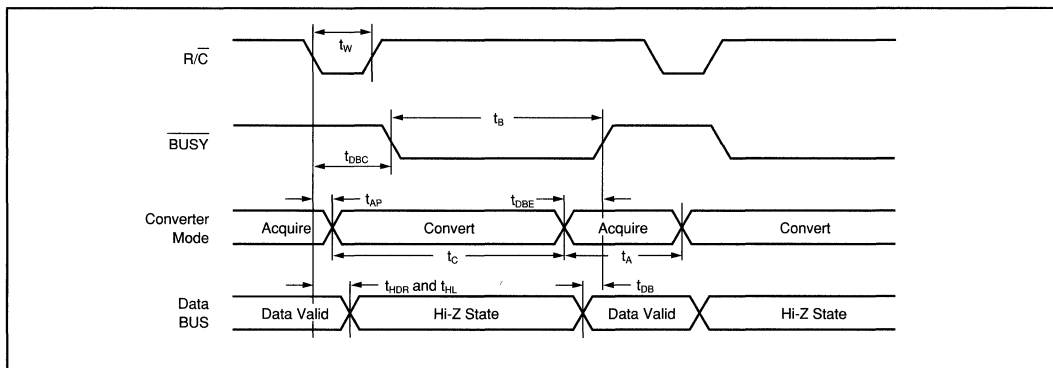
FIGURE 6. Convert Mode: R/$\overline{\text{C}}$ Pulse LOW — Outputs Enabled After Conversion.
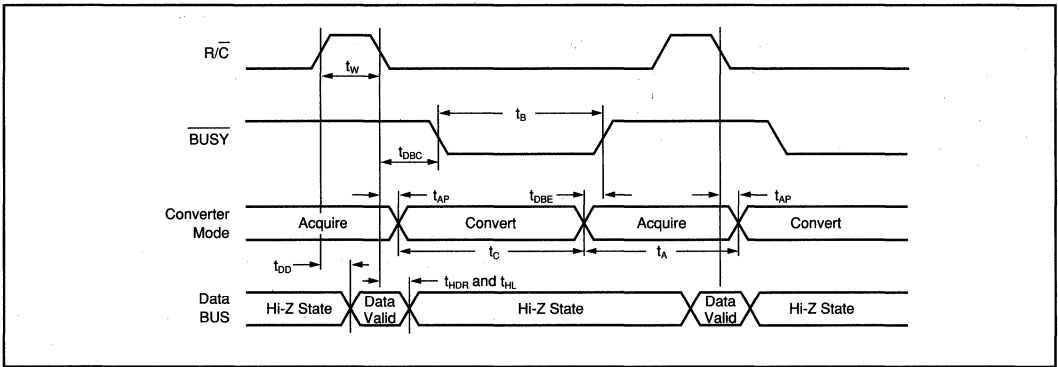
FIGURE 7. Read Mode: R/C̄ Pulse HIGH— Outputs Enabled Only When R/C̄ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	R/C̄ Pulse Width	40	10		ns
t_{DBC}	B̄Ū̄S̄Ȳ delay from R/C̄		80	150	ns
t_B	B̄Ū̄S̄Ȳ LOW		2.5	2.7	μs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	μs
t_{DBE}	B̄Ū̄S̄Ȳ from End of Conversion		100		ns
t_{DB}	B̄Ū̄S̄Ȳ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
t_A+t_C	Throughput Time		2.6	3.0	μs
t_{HDR}	Valid Data Held After R/C̄ LOW	20	50		ns
t_S	C̄S̄ or HBE LOW before R/C̄ Falls	25	5		ns
t_H	C̄S̄ or HBE LOW after R/C̄ Falls	25	0		ns
t_{DD}	Data Valid from C̄S̄ LOW, R/C̄ HIGH, and HBE in Desired State (Load ≈ 100pF)		65	150	ns
t_{HDR}	Valid Data Held After R/C̄ Low	20	50		ns
t_{HL}	Delay to Hi-Z State after R/C̄ Falls or C̄S̄ Rises (3kΩ Pullup or Pulldown)		50	150	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).
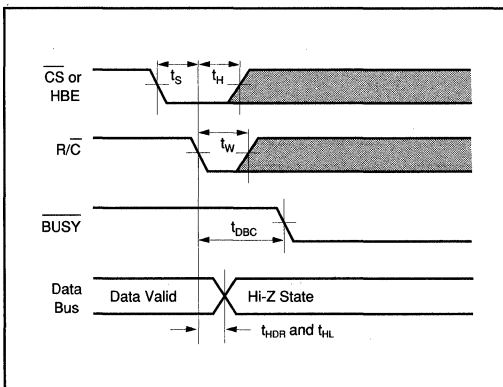
FIGURE 8. Conversion Start Timing.

Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain maximum system accuracy, both should be well isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the ADS7800.

The V_S pins (23 and 24) should be connected together and bypassed with a parallel combination of a 6.8μF tantalum capacitor and a 0.1μF ceramic capacitor located close to the converter to obtain noise-free operation. (See Figure 2.) The $-V_S$ pin 22 should be bypassed with a 1μF tantalum capacitor, again as close as possible to the ADS7800.

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the

converter if at all possible. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the ADS7800, which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the ADS7800 as possible.
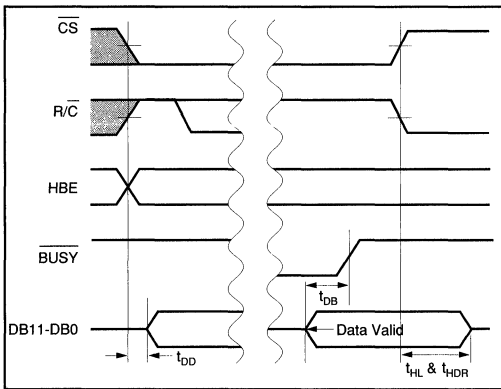
FIGURE 9. Read Cycle Timing.

REFERENCE BYPASS

Pin 3 (REF) should be bypassed with a 22µF to 47µF tantalum capacitor. A rated working voltage of 2V or more is acceptable here. This pin is used to enhance the system accuracy of the internal reference circuit, and is not recommended for driving external signals. If there are important system reasons for using the ADS7800 reference externally, the output of pin 3 must be appropriately buffered.

"HOT SOCKET" PRECAUTION

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the ADS7800 may "Latch Up" and draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to power the ADS7800 only after it has been socketed.
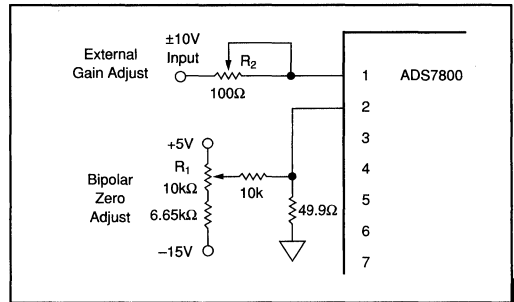
FIGURE 10. ±10V Range With External Trims.

MINIMIZING "GLITCHES"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using the ADS7800. These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the ADS7800 has an internal sample/hold function, the signal that puts it into the hold state (R/C̄ going LOW) is critical, as it would be on any sample/hold amplifier. The R/C̄ falling edge should be sharp and have minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitching the ADS7800 while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/C̄, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).
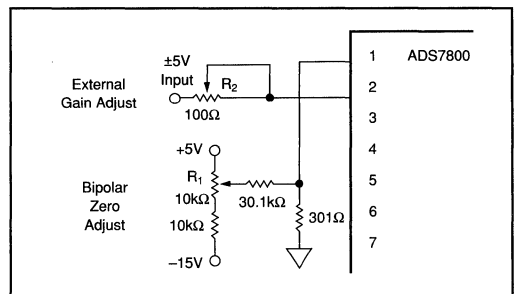
FIGURE 11. ±5V Range With External Trims.

Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the ADS7800. If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{\text{BUSY}}$ output can be used to enable the buffer.

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{\text{C}}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the ADS7800.

Finally, in multiplexed systems, the timing on when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{\text{C}}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the ADS7800 input. Whenever possible, it is safer to wait until the conversion is completed before switching the multiplexer. The extremely fast acquisition time and conversion time of the ADS7800 make this practical in many applications.

INPUT VOLTAGE RANGE AND LSB VALUES				
Input Voltage Range Defined As: Analog Input Connected to Pin Pin Connected to GND One Least Significant Bit (LSB)	FSR/2^{12}		±10V 1 2 20V/2^{12} 4.88mV	±5V 2 1 10V/2^{12} 2.44mV
OUTPUT TRANSITION VALUES				
FFE$_H$ to FFF$_H$		+Full Scale	+10V–3/2LSB +9.9927V	+5V–3/2LSB +4.9963V
7FF$_H$ to 800$_H$		Mid Scale (Bipolar Zero)	0V–1/2LSB –2.44mV	0V–1/2LSB –1.22mV
000$_H$ to 001$_H$		–Full Scale	–10V+1/2LSB –9.9976V	–5V+1/2LSB –4.9988V

TABLE IV. Input Voltages, Transition Values, and LSB Values.

BURR - BROWN®

ADS7803

Autocalibrating, 4-Channel, 12-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **LOW POWER: 10mW plus Power Down**
● **SIGNAL-TO-(NOISE + DISTORTION)**
  RATIO OVER TEMPERATURE:
  69dB min with f_{IN} = 1kHz
  66dB min with f_{IN} = 50kHz
● **FAST CONVERSION TIME: 8.5μs**
  Including Acquisition (117kHz Sampling
  Rate)
● **DC PERFORMANCE OVER**
  TEMPERATURE:
  ±3/4 LSB max Total Error
  ±1/4 LSB max Channel Mismatch
● **FOUR-CHANNEL INPUT MULTIPLEXER**
● **SINGLE SUPPLY: +5V**
● **PIN COMPATIBLE WITH ADC7802**

DESCRIPTION

The ADS7803 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. It is designed and tested for full dynamic performance with input signals to 50kHz. An autocalibration cycle guarantees a total unadjusted error within ±3/4LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADS7803 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

ADS7803

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BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
			ADS7803BP/ADS7803BN		
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = +25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \leq V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance[1]: $V_{REF}+$		4.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	μA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz			8.5	μs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz			17	μs
	CLK = 500kHz			34	μs
With Internal Clock Using Recommended	$T_A = +25°C$			10	μs
Clock Components	$T_A = -40°C$ to $+85°C$		10		μs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
DC ACCURACY					
Total Error, All Channels[2]			±1/2	±3/4	LSB
Differential Nonlinearity			±1/4	±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels		±1/8	±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels		±1/8	±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
AC ACCURACY					
Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 1kHz$	69	71		dB
	$f_{IN} = 50kHz$	66	69		dB
Total Harmonic Distortion	$f_{IN} = 50kHz$		−75		dB
Signal-to-Noise Ratio	$f_{IN} = 50kHz$		70		dB
Spurious Free Dynamic Range	$f_{IN} = 1kHz$		90		dB
	$f_{IN} = 50kHz$		82		dB
SAMPLING DYNAMICS					
Full Power Bandwidth	−3dB		4		MHz
Aperture Delay	SFR D2 LOW		2500		ns
Offset Error	SRF D2 HIGH		5		ns
	SFR D2 LOW		±1/8	±1/4	LSB
	SFR D2 HIGH, Internal Clock or		±1/2	±1	LSB
	Sampling Command Synchronous				
	to External Clock				
	SFR D2 HIGH, Sampling Command		±4		LSB
	Asynchronous to External Clock				
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	μA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	μA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	μA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 4.5V, the total error will typically not exceed ±1LSB. (2) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

SPECIFICATIONS (CONT)

ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7803BP/ADS7803BN MIN	ADS7803BP/ADS7803BN TYP	ADS7803BP/ADS7803BN MAX	UNITS
DIGITAL OUTPUTS					
V_{OL}	$I_{SINK} = 1.6mA$			0.4	V
V_{OH}	$I_{SOURCE} = 200\mu A$	4			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_D			±1	μA
Output Capacitance	High-Z State	4		15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III		50		μW
TEMPERATURE RANGE					
Specification		−40		+85	°C
Storage		−65		+150	°C

PIN CONFIGURATIONS

Top View — DIP

Top View — LCC
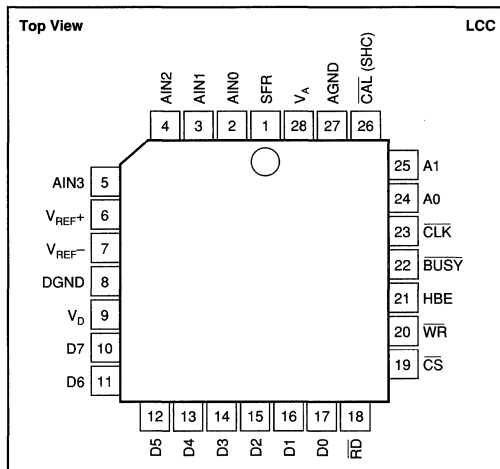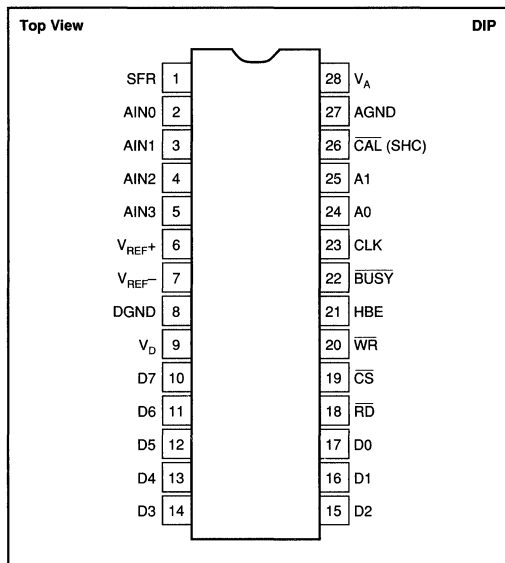
PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC7803BN	28-Pin LCC	251
ADS7803BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO, dB	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE
ADS7803BN	69	±3/4	−40°C to +85°C
ADS7803BP	69	±3/4	−40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground 6.5V
V_D to Digital Ground 6.5V
Pin V_A to Pin V_D .... ±0.3V
Analog Ground to Digital Ground .... ±1V
Control Inputs to Digital Ground .... −0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground .... −0.3V to V_D + 0.3V
Maximum Junction Temperature .... 150°C
Internal Power Dissipation 875mW
Lead Temperature (soldering, 10s) .... +300°C
Thermal Resistance, θ_{JA}: Plastic DIP .... 75°C/W
PLCC .... 75°C/W

TYPICAL PERFORMANCE CURVES

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, dynamic performance based on 2048 point FFTs , unless otherwise noted.

FREQUENCY SPECTRUM (1kHz f_{IN})

S/(N + D) = 71.4dB
$f_{SAMPLING}$ = 100kHz

Magnitude (dB) / Frequency (kHz)

FREQUENCY SPECTRUM (48kHz f_{IN})

S/(N + D) = 69.2dB
$f_{SAMPLING}$ = 100kHz

Magnitude (dB) / Frequency (kHz)

CHANNEL SEPARATION vs FREQUENCY

Channel AIN3
Channel AIN1
Channel AIN0

Channel Separation (dB) / Frequency of 5Vp-p Signal on Channel AIN2 (kHz)

CODE TRANSITION NOISE

Conversion Yielding Expected Code (%) / Analog Input Voltage – Expected Code Center (LSBs)

SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY

Signal/(Noise + Distortion) (dB) / Input Frequency (kHz)

POWER SUPPLY REJECTION vs FREQUENCY

V_A

V_D

Full-Scale Error vs Change in Supply Voltage (mV/V) / Frequency (kHz)

TYPICAL PERFORMANCE CURVES (CONT)

$V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, dynamic performance based on 2048 point FFTs , unless otherwise noted.

INTERNAL CLOCK FREQUENCY vs TEMPERATURE

$R_{CLOCK} = 70k\Omega$

INTERNAL CLOCK FREQUENCY vs R_{CLOCK}

THEORY OF OPERATION

ADS7803 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by an on-chip microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADS7803 to most micro-controllers, microprocessors or digital storage systems.

The on-chip sampling provides excellent dynamic performance for input signals to 50kHz, and has a full-power −3dB bandwidth of 4MHz. Full control over sample-to-hold timing is available for applications where this is critical.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW, with a 50µW power down option.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADS7803 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 (BUSY) will output a LOW during the conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).
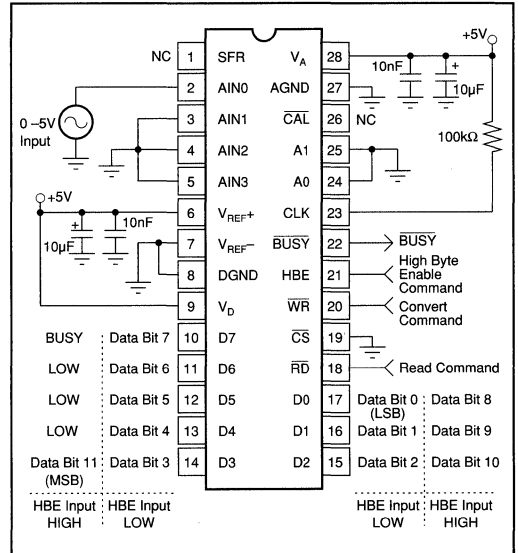
FIGURE 1. Basic Operation.

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles. The successive approximation conversion takes place during clock cycles 6 through 17.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

A conversion can also be initiated by a rising edge on pin 26, if a HIGH has been written to D2 of the Special Function Register, as discussed below.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. Thus, at the end of a calibration cycle, there is valid conversion data in the output registers. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	$V_{REF}+$	Positive voltage reference input. Normally +5V. Must be $\leq V_A$.
7	$V_{REF}-$	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be $\leq V_A$ and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$).
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal or external clock operation. For external clock operation, connect pin 23 to a 74HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 A0 Selected Channel LOW LOW AIN0 LOW HIGH AIN1 HIGH LOW AIN2 HIGH HIGH AIN3
26	$\overline{CAL}$ (SHC)	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. If D2 of the SFR is programmed HIGH, pin 26 will be used as an input to control the sample-to-hold timing. A rising edge on pin 26 will switch from sample-mode to hold-mode and initiate a conversion. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be $\geq V_D$ and $V_{REF}+$.

READING DATA

Data from the ADS7803 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are

FIGURE 2. Converter Timing.
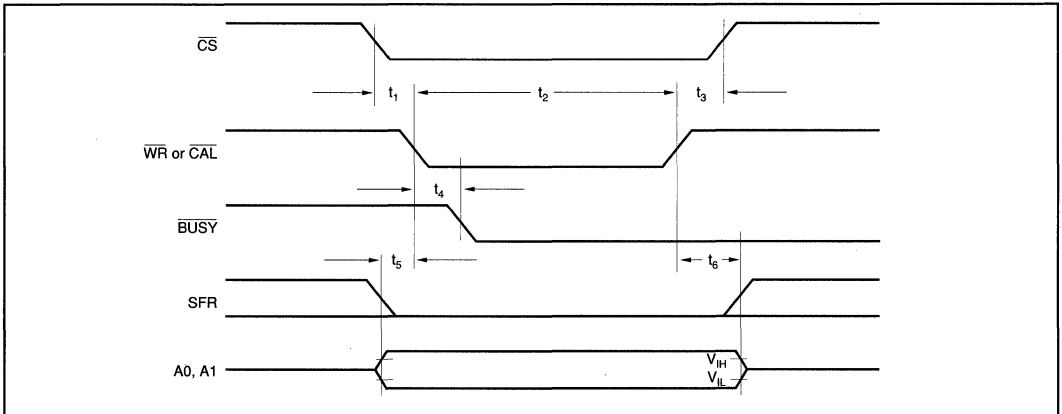
FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).
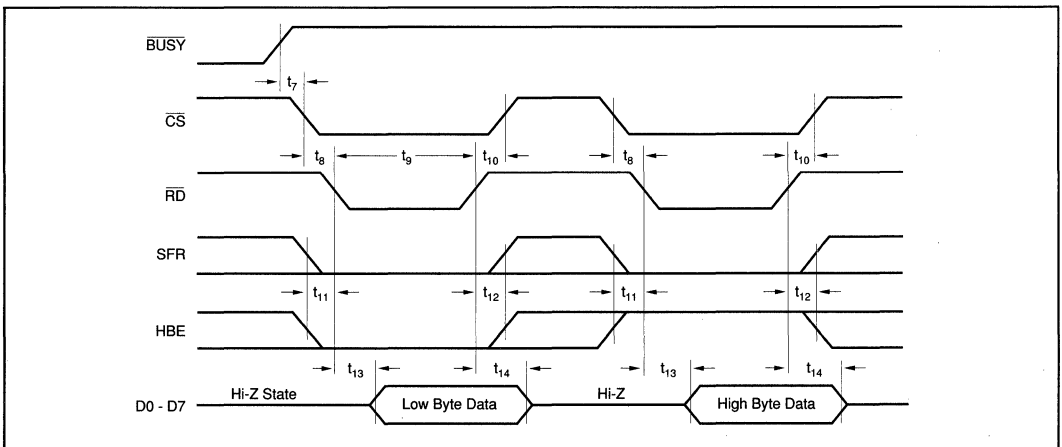
FIGURE 4. Read Cycle Timing.

LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADS7803 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

TRANSPARENT MODE

This is the default mode for ADS7803. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 9 show the digital timing of ADS7803 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADS7803, or to write additional instructions to the converter.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADS7803 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) Note that writing to the SFR also initiates a new conversion.

SYMBOL	PARAMETER[1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time[2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time[2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time[2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time[2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time)[3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time)[3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR[3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns
t_{18}	Acquisition Time. Pin 26 LOW with D2 in SFR HIGH	2.5			µs
t_{19}	Sample-to-Hold Aperture Delay. (D2 in SFR HIGH)		5		ns
t_{20}	Delay from rising edge on pin 26 to start of conversion. (D2 in SFR HIGH)			1.5	CLK cycles

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL} = 20ns$ (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 8 and 9 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 2MHz external, T_A = –40°C to +85°C).

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2	Pin 26 Status	If LOW, pin 26 used as input to initiate calibration cycle. If HIGH, pin 26 used as input to control sample-to-hold timing.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occurred during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

POWER DOWN MODE

Writing a HIGH to D3 in the SFR puts the ADS7803 in the Power Down Mode. Power consumption is reduced to $50\mu W$ and D3 remains HIGH. The internal clock and analog circuitry are turned off, although the output registers and SFR can still be accessed normally. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. Note that if the power supply falls below 3V and then recovers, a calibration is automatically initiated, and the SFR will be reset. D3 will be LOW, and the ADS7803 will not be in the Power Down Mode.

During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7803 will revert to power down. Also, writing to D1 and D3 in the SFR will initiate a calibration, do a single conversion and revert to the Power Down Mode, in 185 clock cycles. Accurate conversion results will be available in the output registers.

The activation delay from power down to normal operation is included in the sampling time. No extra time is required, either when coming out of the Power Down Mode or when making a single conversion in the Power Down Mode.

FIGURE 5. Writing to the SFR.

FIGURE 6. Reading the FSR.

SAMPLE/HOLD CONTROL MODE

With D2 in the SFR HIGH, a rising edge input on pin 26 will switch the ADS7803 from sample-mode to hold-mode with a 5ns aperture delay. This also initiates a conversion, which will start within 1.5 CLK cycles.

This mode allows full control over the sample-to-hold timing, which is especially useful where external events trigger sampling timing.

In the Sample/Hold Control Mode, pin 26 must be held LOW a minimum of $2.5\mu s$ between conversions to allow accurate acquisition of input signals. Also, offset error will increase in this mode, since auto-zeroing of the comparator is not synchronized to the sampling. Minimum offset is achieved by synchronizing the sampling signal to CLK, whether internal or external. Ideally, the sampling signal

OPERATION	CS/WR	SFR/HBE	D0	D1	D2	D3	D5	D4/D6/D7
Enables Transparent Mode for Data Latches	LOW	HIGH	LOW	X	X	X	X	LOW
Enables Latched Output Mode for Data Latches	LOW	HIGH	HIGH[1]	X	X	X	X	LOW
Initiates Calibration Cycle	LOW	HIGH	X	HIGH	X	X	X	LOW
Activates Sample/Hold Control Mode	LOW	HIGH	X	X	HIGH[1]	X	X	LOW
Activates Power Down Mode[2]	LOW	HIGH	X	X	X	HIGH[1]	X	LOW
Resets Power Fail Flag	LOW	HIGH	X	X	X	X	LOW	LOW

NOTES: (1) Writing a LOW here reactivates the standard mode of operation. (2) In Power Down, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7803 will revert to power down. (3) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

rising edge should be delayed 20ns from the falling edge of CLK. This will keep offset error to about 1LSB.

In the Sample/Hold Control Mode, a LOW pulse on $\overline{\text{WR}}$ (with $\overline{\text{CS}}$ LOW) will not initiate a conversion, but the rising edge will latch the multiplexer channel according to the inputs on A0 and A1. When changing channels, this must be done at least 2.5µs before pin 26 goes HIGH (to start a conversion.)

CONTROL LINES

Table IV shows the functions of the various control lines on the ADS7803. The use of standard $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

INSTALLATION

INPUT IMPEDANCE

ADS7803 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to

noise at the analog input, since it could be injected into the capacitor array.

In many applications, a simple passive low-pass filter as shown in Figure 10a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 10a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 10b should be used.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADS7803, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADS7803 to

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	SFR	HBE	CAL	BUSY	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle. (See SFR section for alternate use as Sample/Hold Control Mode input.)
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{\text{WR}}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

FIGURE 7. Timing for Initiating Conversion in Sample/Hold Control Mode (D2 in SFR HIGH).

FIGURE 8. Measuring Active LOW to/from Hi-Z State.
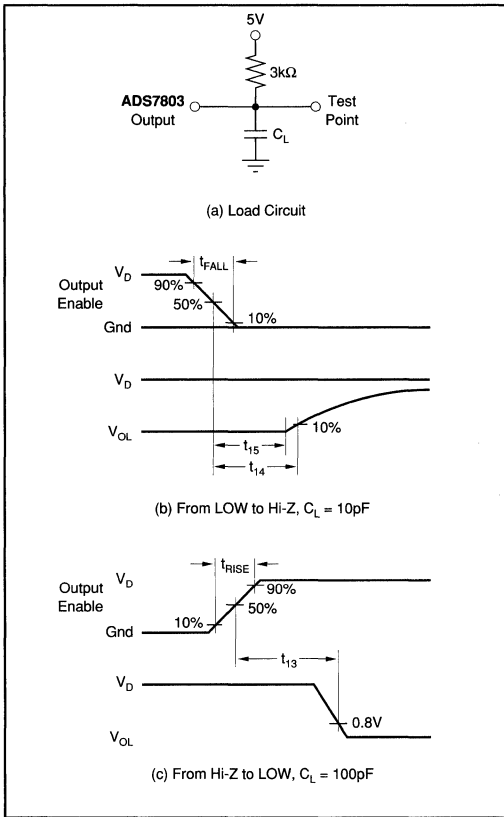
FIGURE 9. Measuring Active HIGH to/from Hi-Z State.

reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 4.5V and $V_{REF}-$ as high as 1V. As long as there is at least a 4.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADS7803 should be bypassed with 10µF tantalum capacitors as close to the part as possible. Although ADS7803 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 11 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This
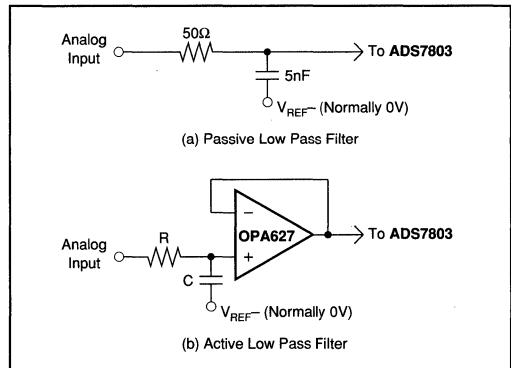
FIGURE 10. Input Signal Conditioning.

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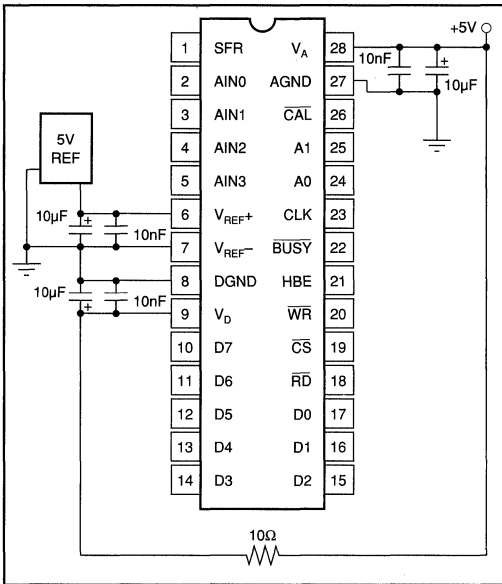
FIGURE 11. Power Supply and Reference Decoupling.

is also a good method to further isolate the ADS7803 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADS7803, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The $V_{REF}-$ pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADS7803 clock from an external source is shown in Figure 12a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The duty cycle of the external clock can vary as long as the LOW time and HIGH time are each at least 200ns wide. Synchro-
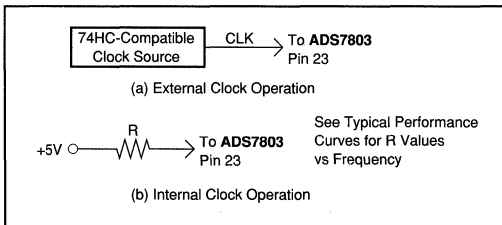
FIGURE 12. Internal Clock Operation.

nizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.4MHz.

INTERNAL CLOCK OPERATION

Figure 12b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 13 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADS7803, using a precision, low-cost complete difference amplifier, INA105.
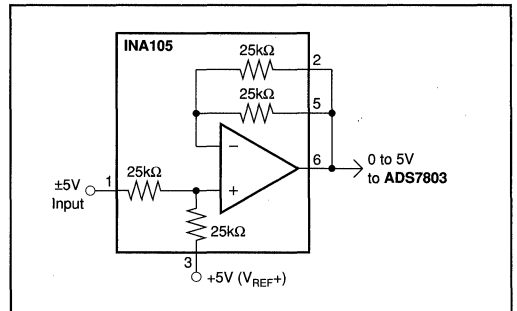
FIGURE 13. ±5V Input Range.
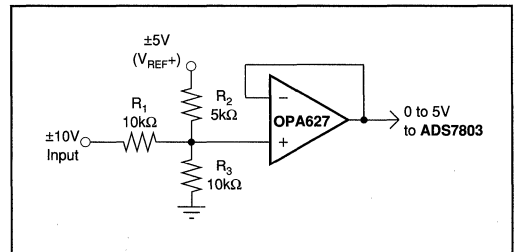
FIGURE 14. ±10V Input Range.

Figure 14 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADS7803. The precision of this circuit will depend on the matching and tracking of the three resistors used.

To trim this circuit for full 12-bit precision, R_2 and R_3 need to be adjustable over appropriate ranges. To trim, first have the ADS7803 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R_3 until the ADS7803 output toggles between the codes FFE hex and FFF hex. This makes R_3 extremely close to R_1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R_2 until the ADS7803 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADS7803, to match the performance of the self-calibration provided by the converter.

INTERFACING TO
MOTOROLA MICROPROCESSORS

Figure 15 show a typical interface to Motorola microprocessors, while Figure 16 shows how the result can be placed in register D0.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:
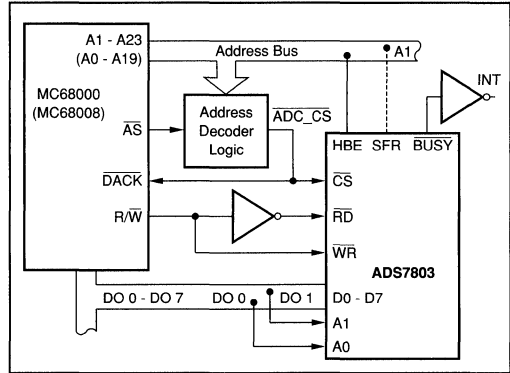
FIGURE 15. Interface to Motorola Microprocessors.

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the D0 register, as shown in Figure 15. The address decoder must pull down $\overline{ADC\_CS}$ AT ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 17 shows a typical interface to Intel.

A conversion is initiated by write instruction to address $\overline{ADC\_CS}$. Data pins DO0 and DO1 select the analog input channel. The $\overline{BUSY}$ signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the $\overline{ADC\_CS}$ address fetches the Low byte, and a read instruction from the $\overline{ADC\_CS}$ address +2 fetches the High byte.
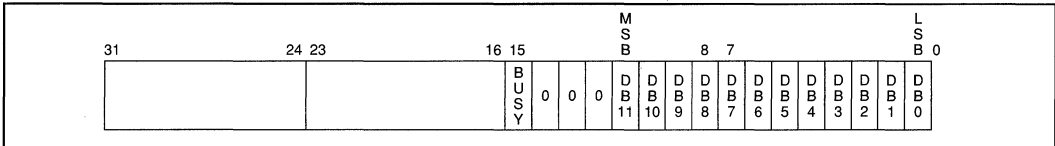
FIGURE 16. Conversion Results in Motorola Register D0.
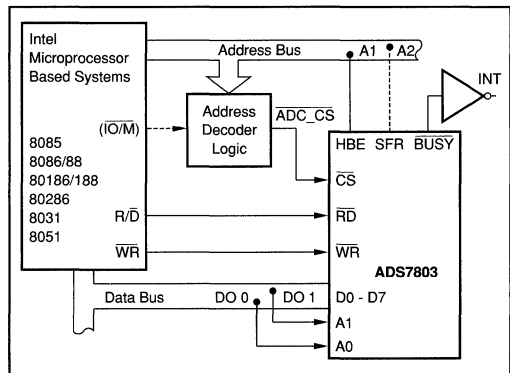
FIGURE 17. Interface to Intel Microprocessors.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®
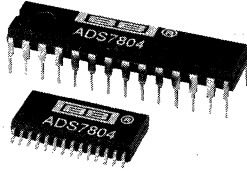
ADS7804

**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

12-Bit 10μs Sampling CMOS
ANALOG-to-DIGITAL CONVERTER

FEATURES

- ● **100kHz min SAMPLING RATE**
- ● **STANDARD ±10V INPUT RANGE**
- ● **86dB min SINAD WITH 45kHz INPUT**
- ● **±1.5 LSB max INL**
- ● **DNL: 12-Bits "No Missing Codes"**
- ● **SINGLE +5V SUPPLY OPERATION**
- ● **PIN-COMPATIBLE WITH 16-BIT ADS7805**
- ● **USES INTERNAL OR EXTERNAL
  REFERENCE**
- ● **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- ● **FULL PARALLEL DATA OUTPUT**
- ● **100mW max POWER DISSIPATION**
- ● **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7804 is a complete 12-Bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-Bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7804 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7804 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

PDS-1156B

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SPECIFICATIONS

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7804P/U			ADS7804PB/UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V			*		V
Impedance			23			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			5.7	8		*	*	μs
Complete Cycle	Acquire and Convert			10			*	μs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±0.9			±0.45	LSB[1]
Differential Linearity Error				±0.9			±0.45	LSB
No Missing Codes			Guaranteed			*		Bits
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±10			±10	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity	$+4.75V < V_D < +5.25V$			±0.5			*	LSB
($V_{DIG} = V_{ANA} = V_D$)								
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 45kHz$	80			*			dB[5]
Total Harmonic Distortion	$f_{IN} = 45kHz$			−80			*	dB
Signal-to-(Noise+Distortion)	$f_{IN} = 45kHz$	70			72			dB
Signal-to-Noise	$f_{IN} = 45kHz$	70			72			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter		Sufficient to meet AC specs			*			
Transient Response	FS Step			2			*	μs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			1		*	*		μA
(Must use external buffer.)								
Internal Reference Drift			8					ppm/°C
External Reference Voltage Range		2.3	2.5	2.7	*	*	*	V
for Specified Linearity								
External Reference Current Drain	Ext. 2.5000V Ref			100			*	μA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.0		$V_D +0.3V$	*		*	V
I_{IL}				±10			*	μA
I_{IH}				±10			*	μA
DIGITAL OUTPUTS								
Data Format			Parallel 12-bits					
Data Coding			Binary Two's Complement					
V_{OL}	$I_{SINK} = 1.6mA$			+0.4			*	V
V_{OH}	$I_{SOURCE} = 500μA$	+4			*		*	V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_{DIG}			±5			*	μA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

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SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7804P/U MIN	ADS7804P/U TYP	ADS7804P/U MAX	ADS7804PB/UB MIN	ADS7804PB/UB TYP	ADS7804PB/UB MAX	UNITS
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{ANA}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
$+I_{DIG}$			0.3			*		mA
$+I_{ANA}$			16			*		mA
Power Dissipation	$f_S = 100kHz$			100			*	mW
TEMPERATURE RANGE								
Specified Performance		−40		+85	*		*	°C
Derated Performance		−55		+125	*		*	°C
Storage		−65		+150	•		•	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, $\pm10V$ input ADS7804, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of −Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale $\pm10V$ input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	$\pm25V$
CAP	$+V_{ANA}$ +0.3V to AGND2 −0.3V
REF	Indefinite Short to AGND2
	Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2	$\pm0.3V$
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	−0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7804P	Plastic DIP	246
ADS7804PB	Plastic DIP	246
ADS7804U	SOIC	217
ADS7804UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7804P	±0.9	70	−40°C to +85°C	Plastic DIP
ADS7804PB	±0.45	72	−40°C to +85°C	Plastic DIP
ADS7804U	±0.9	70	−40°C to +85°C	SOIC
ADS7804UB	±0.45	72	−40°C to +85°C	SOIC

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V$_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/C	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	CS	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	BUSY	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V$_{ANA}$		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V$_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V$_{ANA}$.

TABLE I. Pin Assignments.

PIN CONFIGURATION

V$_{IN}$	1		28	V$_{DIG}$
AGND1	2		27	V$_{ANA}$
REF	3		26	$\overline{BUSY}$
CAP	4		25	$\overline{CS}$
AGND2	5		24	R/$\overline{C}$
D11 (MSB)	6		23	BYTE
D10	7	ADS7804	22	DZ
D9	8		21	DZ
D8	9		20	DZ
D7	10		19	DZ
D6	11		18	D0 (LSB)
D5	12		17	D1
D4	13		16	D2
DGND	14		15	D3

CHARACTERIZATION CURVES

Call factory for updated data sheet which includes characterization curves.

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BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7804 with a full parallel data output. Taking R/$\overline{\text{C}}$ (pin 24) LOW for a minimum of 40ns (6µs max) will initiate a conversion. $\overline{\text{BUSY}}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{\text{BUSY}}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{\text{BUSY}}$ is LOW.

The ADS7804 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{\text{CS}}$ (pin 25) and R/$\overline{\text{C}}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7804 in the hold state and starts conversion 'n'. $\overline{\text{BUSY}}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{\text{BUSY}}$ LOW will be ignored. $\overline{\text{CS}}$ and/or R/$\overline{\text{C}}$ must go HIGH before $\overline{\text{BUSY}}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7804 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to

Table II for a summary of $\overline{\text{CS}}$, R/$\overline{\text{C}}$, and $\overline{\text{BUSY}}$ states and Figures 3 through 5 for timing diagrams.

$\overline{\text{CS}}$ and R/$\overline{\text{C}}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{\text{CS}}$ or R/$\overline{\text{C}}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{\text{CS}}$ can be tied LOW using R/$\overline{\text{C}}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever R/$\overline{\text{C}}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{\text{CS}}$	R/$\overline{\text{C}}$	$\overline{\text{BUSY}}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion n in process.
0	↑	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion "n" in process.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{\text{CS}}$ and/or R/$\overline{\text{C}}$ must be HIGH when $\overline{\text{BUSY}}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in process.

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".
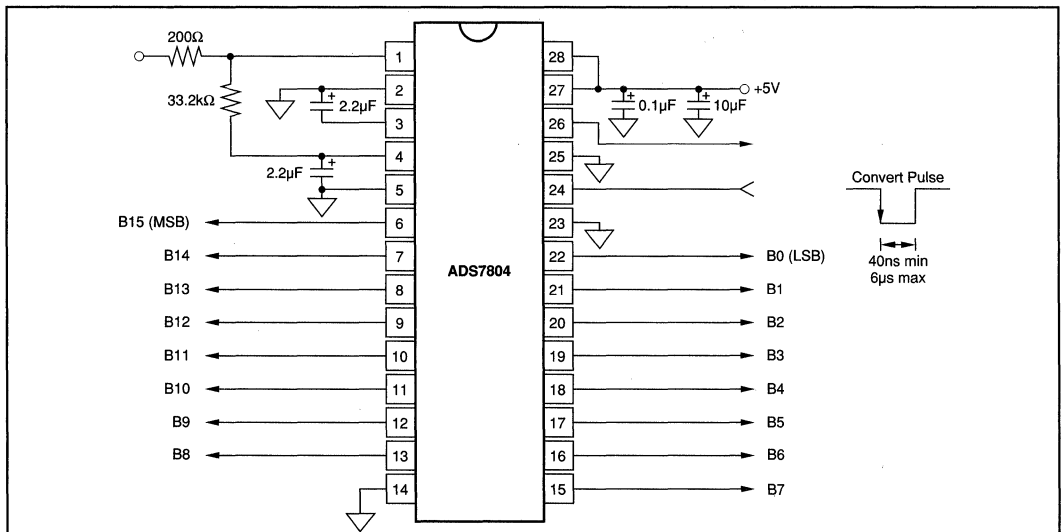
FIGURE 1. Basic Operation.

READING DATA

The ADS7804 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-Bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	4.88mV		
+Full Scale (10V – 1LSB)	9.99512V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	−4.88mV	1111 1111 1111	FFF
−Full Scale	−10V	1000 0000 0000	800

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D11-D0 (pin 6-13 and 15-18 when BYTE is LOW). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 16µs after the start of conversion 'n'. Do not attempt to read data from 16µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		6000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		7.4		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

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FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{\text{CS}}$ Tied LOW.)

FIGURE 4. Using $\overline{\text{CS}}$ to Control Conversion and Read Timing.

FIGURE 5. Using $\overline{\text{CS}}$ and BYTE to Control Data Bus.

INPUT RANGES

The ADS7804 offers a standard ±10V input range. Figure 6 shows the necessary circuit connections for the ADS7804 with and without hardware trim. Offset and full scale error[1] specifications are tested and guaranteed with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The nominal input impedance of 23kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection guaranteed to at leaset ±25V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

The ADS7804 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7804, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is ±15mV for the offset and ±60mV for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7804 in software, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Table V for range of offset and gain errors with and without external resistors.

NO CALIBRATION

See Figure 6b for circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7804 will be bound by the shaded region seen in Figure 7 with a typical offset of –30mV and a typical gain error of –1.5%. Refer to Table V for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPZ	–10 < BPZ < 10	–45 < BPZ < 5	mV
	–2 < BPZ < 2	–8 < BPZ < 1	LSBs
Gain Error	–0.5 < error < 0.5	–0.6 < error < –0.55	% of FSR
	–0.25 < error < 0.25[1]	–0.45 < error < –0.3[1]	
NOTE: (1) High Grade.			

TABLE VII. Bipolar Offset and Gain Errors With and Without External Resistors.

a)	±10V With Hardware Trim	b)	±10V Without Hardware Trim

NOTE: Use 1% metal film resistors.

FIGURE 6. Circuit Diagram With and Without External Resistors.

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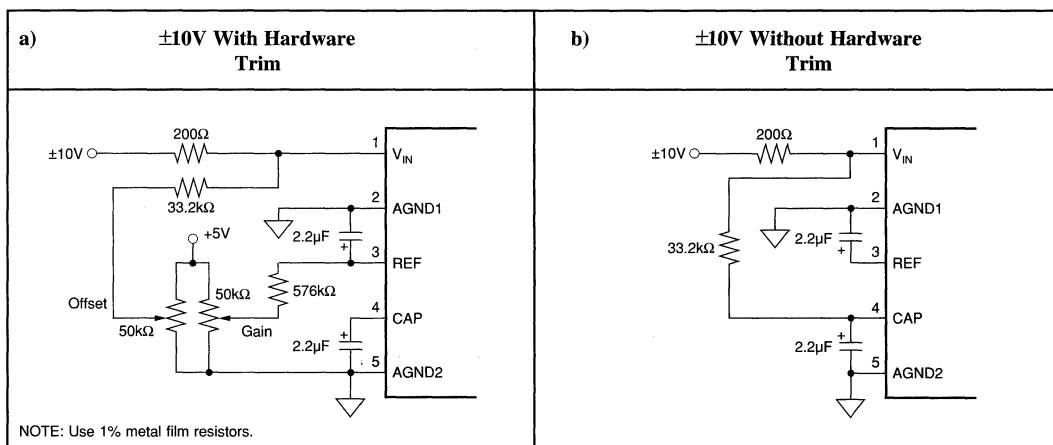
FIGURE 7. Full Scale Transfer Function.

REFERENCE

The ADS7804 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2μF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2μF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1μF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2μF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7804. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7804 uses 90% of its power for the analog circuitry. The ADS7804 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7804. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7804, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient to drive the signal in an application will be sufficient to drive the ADS7804.

The resistive front end of the ADS7804 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7804 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7804 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7805 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of 38µV.

APPLICATIONS

Call factory for updated data sheet which includes standard DSP, microprocessor, and microcontroller interfaces.

ADS7804

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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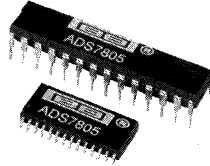
ADS7805

DEMO BOARD AVAILABLE
See Appendix A for more information.

16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- **100kHz min SAMPLING RATE**
- **STANDARD ±10V INPUT RANGE**
- **86dB min SINAD WITH 45kHz INPUT**
- **±1.5 LSB max INL**
- **DNL: 16-bits "No Missing Codes"**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 12-BIT ADS7804**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **FULL PARALLEL DATA OUTPUT**
- **100mW max POWER DISSIPATION**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7805 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7805 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7805 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

PDS-1157B

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SPECIFICATIONS

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U MIN	ADS7805P, U TYP	ADS7805P, U MAX	ADS7805PB, UB MIN	ADS7805PB, UB TYP	ADS7805PB, UB MAX	UNITS
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V			*		V
Impedance			23			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			7.6	8		*	*	μs
Complete Cycle	Acquire and Convert			10			*	μs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, −2			+1.5, −1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity	$+4.75V < V_D < +5.25V$			±8			*	LSB
($V_{DIG} = V_{ANA} = V_D$)								
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 45kHz$	90			96			dB[5]
Total Harmonic Distortion	$f_{IN} = 45kHz$			−90			−96	dB
Signal-to-(Noise+Distortion)	$f_{IN} = 45kHz$	83			86			dB
	−60dB Input		30			32		dB
Signal-to-Noise	$f_{IN} = 45kHz$	83			86			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		
Transient Response	FS Step			2			*	μs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			1		*			μA
(Must use external buffer.)								
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range		2.3	2.5	2.7	*	*	*	V
for Specified Linearity								
External Reference Current Drain	Ext. 2.5000V Ref			100			*	μA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.0		$V_D +0.3V$	*		*	V
I_{IL}				±10			*	μA
I_{IH}				±10			*	μA
DIGITAL OUTPUTS								
Data Format			Parallel 16-bits					
Data Coding			Binary Two's Complement					
V_{OL}	$I_{SINK} = 1.6mA$			+0.4			*	V
V_{OH}	$I_{SOURCE} = 500μA$	+4			*		*	V
Leakage Current	High-Z State,			±5			*	μA
	$V_{OUT} = 0V$ to V_{DIG}							
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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ADS7805

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{ANA}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}				0.3			*	mA
I_{ANA}				16			*	mA
Power Dissipation	$f_S = 100kHz$			100			*	mW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	°C
Derated Performance		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7805, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

```
Analog Inputs: V_IN ..................................................................... ±25V
              CAP ...................................... +V_ANA +0.3V to AGND2 –0.3V
              REF .......................................... Indefinite Short to AGND2,
                                                    Momentary Short to V_ANA
Ground Voltage Differences: DGND, AGND1, AGND2 ................... ±0.3V
V_ANA .............................................................................................. 7V
V_DIG to V_ANA ........................................................................ +0.3V
V_DIG ............................................................................................. 7V
Digital Inputs ............................................. –0.3V to +V_DIG +0.3V
Maximum Junction Temperature ................................................. +165°C
Internal Power Dissipation ........................................................ 825mW
Lead Temperature (soldering, 10s) ............................................ +300°C
```

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7805P	Plastic DIP	246
ADS7805PB	Plastic DIP	246
ADS7805U	SOIC	217
ADS7805UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7805P	±3	83	–40°C to +85°C	Plastic DIP
ADS7805PB	±1.5	86	–40°C to +85°C	Plastic DIP
ADS7805U	±3	83	–40°C to +85°C	SOIC
ADS7805UB	±1.5	86	–40°C to +85°C	SOIC

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2μF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2μF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	CS	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	BUSY	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be $\leq V_{ANA}$.

TABLE I. Pin Assignments.

PIN CONFIGURATION

V_{IN}	1	28	V_{DIG}
AGND1	2	27	V_{ANA}
REF	3	26	$\overline{BUSY}$
CAP	4	25	$\overline{CS}$
AGND2	5	24	R/$\overline{C}$
D15 (MSB)	6	23	BYTE
D14	7	22	D0 (LSB)
D13	8	21	D1
D12	9	20	D2
D11	10	19	D3
D10	11	18	D4
D9	12	17	D5
D8	13	16	D6
DGND	14	15	D7

ADS7805

CHARACTERIZATION CURVES

Call factory for updated data sheet which includes characterization curves.

ADS7805

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7805 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns (7µs max) will initiate a conversion. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of CS (pin 25) and R/C (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7805 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to

Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 3 through 5 for timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 3 and 4 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".
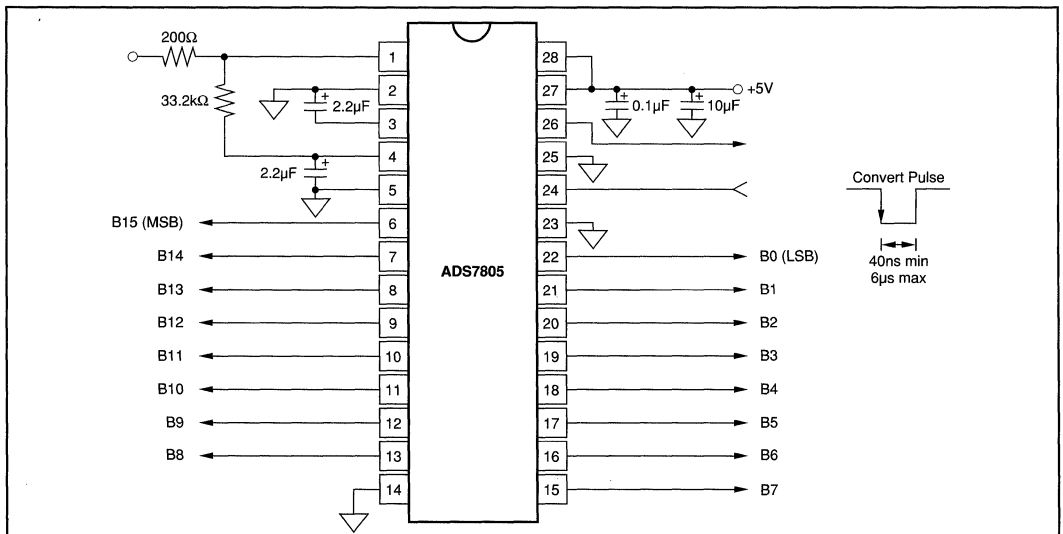
FIGURE 1. Basic Operation.

READING DATA

The ADS7805 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	305µV		
+Full Scale (10V – 1LSB)	9.999695V	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
One LSB below Midscale	–305µV	1111 1111 1111 1111	FFFF
–Full Scale	–10V	1000 0000 0000 0000	8000

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D15-D0 (pin 6-13 and 15-22). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 7µs after the start of conversion 'n'. Do not attempt to read data from 7µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		7000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		7.4		µs
$t_7 + t_8$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

INPUT RANGES

The ADS7805 offers a standard ±10V input range. Figure 6 shows the necessary circuit connections for the ADS7805 with and without hardware trim. Offset and full scale error[1] specifications are tested and guaranteed with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The nominal input impedance of 23kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection guaranteed to at lease ±25V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

The ADS7805 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7805, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is ±15mV for the offset and ±60mV for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7805 in software, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Table V for range of offset and gain errors with and without external resistors.

NO CALIBRATION

See Figure 6b for circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7805 will be bound by the shaded region seen in Figure 7 with a typical offset of –30mV and a typical gain error of –1.5%. Refer to Table V for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BP0	–10 < BPO < 10	–50 < BPO < –15	mV
	–30 < BPO < 30	–150 < BPO < –45	LSBs
Gain Error	–0.5 < error < 0.5	–2 < error < –1	% of FSR

TABLE V. Offset and Gain Errors With and Without External Resistors.
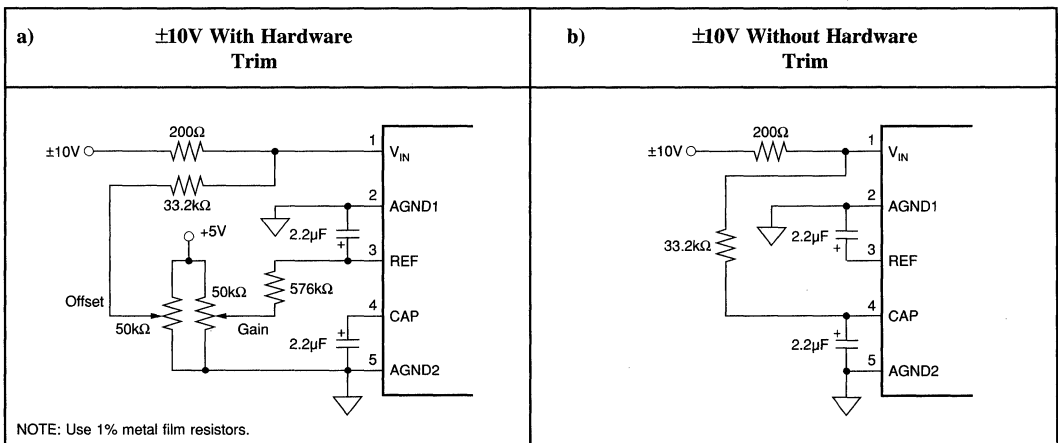
| a) | ±10V With Hardware Trim | b) | ±10V Without Hardware Trim |

NOTE: Use 1% metal film resistors.
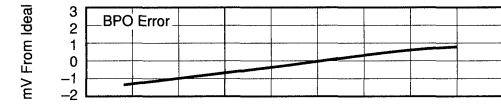
FIGURE 6. Circuit Diagram With and Without External Resistors.
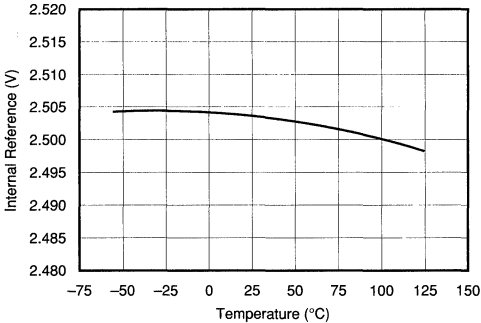
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A/D CONVERTERS, DATA ACQUISITION COMPONENTS
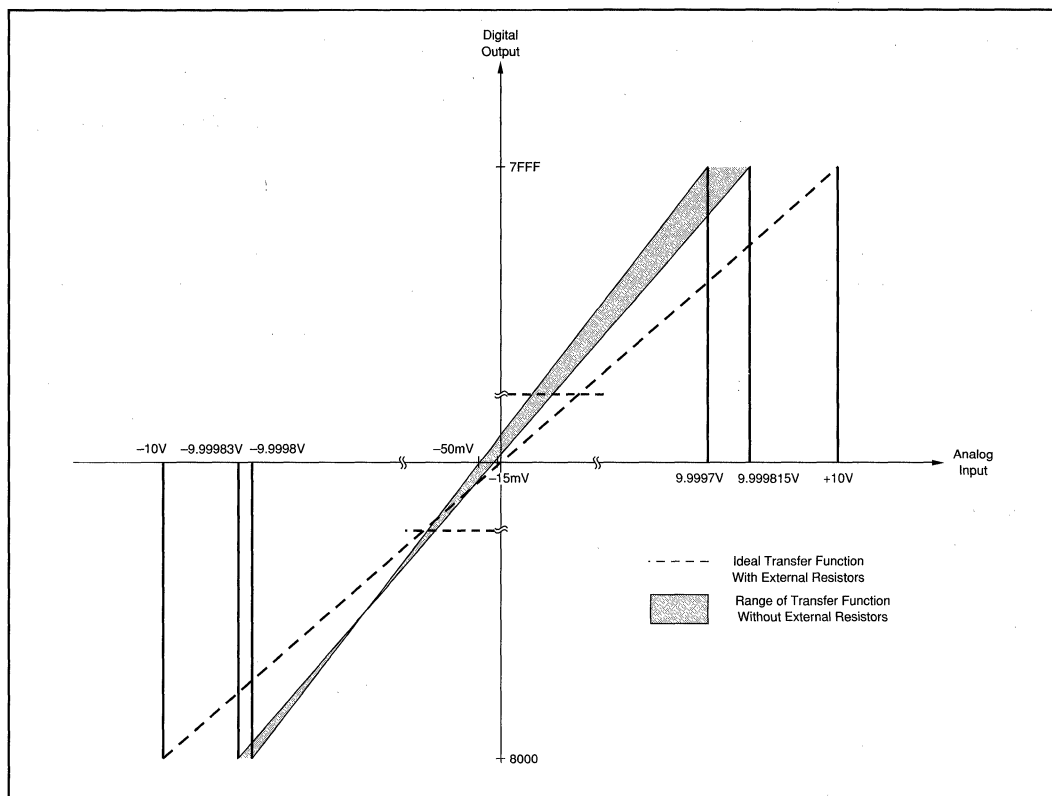
FIGURE 7. Full Scale Transfer Function.

REFERENCE

The ADS7805 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7805. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7805 uses 90% of its power for the analog circuitry. The ADS7805 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7805. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7805, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7805.

The resistive front end of the ADS7805 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7805 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7805 has an internal LSB size of 38μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

APPLICATIONS

Call factory for updated data sheet which includes standard DSP, microprocessor, and microcontroller interfaces.

ADS7805

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BURR - BROWN®

ADS7806

**DEMO BOARD
AVAILABLE**
See Appendix A for
more information.

Low-Power 12-Bit Sampling CMOS
ANALOG-to-DIGITAL CONVERTER

FEATURES

● **35mW max POWER DISSIPATION**

● **50µW POWER DOWN MODE**

● **25µs max ACQUISITION AND
   CONVERSION**

● **±1/2LSB max INL AND DNL**

● **72dB min SINAD WITH 1kHz INPUT**

● **±10V, 0V TO +5V, AND 0V TO +4V INPUT
   RANGES**

● **SINGLE +5V SUPPLY OPERATION**

● **PARALLEL AND SERIAL DATA OUTPUT**

● **PIN-COMPATIBLE WITH 16-BIT ADS7807**

● **USES INTERNAL OR EXTERNAL
   REFERENCE**

● **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7806 is a low-power 12-bit sampling A/D
using state-of-the-art CMOS structures. It contains a
complete 12-bit capacitor-based SAR A/D with S/H,
clock, reference, and microprocessor interface with
parallel and serial output drivers.

The ADS7806 can acquire and convert to full 12-bit
accuracy in 25µs max while consuming only 35mW
max. Laser-trimmed scaling resistors provide standard
industrial input ranges of ±10V and 0V to +5V. In
addition, a 0V to +4V range allows development of
complete single supply systems.

The 28-pin ADS7806 is available in a plastic 0.3" DIP
and in an SOIC, both fully specified for operation over
the industrial –40°C to +85°C temperature range.

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PDS-1158C

SPECIFICATIONS

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7806P, U MIN	TYP	MAX	ADS7806PB, UB MIN	TYP	MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table II)				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error			±0.15	±0.9		*	±0.45	LSB(1)
Differential Linearity Error			±0.15	±0.9		*	±0.45	LSB
No Missing Codes			Guaranteed			*		Bits
Transition Noise(2)			0.1			*		LSB
Full Scale Error(3,4)				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error(3,4)	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error(3)	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error(3)	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down(5)	2.2µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_S$)	+4.75V < V_S < +5.25V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V	80	90		*	*		dB(6)
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		−90	−80		*	*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V	70	73		72	*		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V	70	73		72	*		dB
Full-Power Bandwidth(7)			130			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		
Transient Response	FS Step			5			*	µs
Overvoltage Recovery(8)			750			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS								
Data Format			Parallel 12-bits in 2-bytes; Serial					
Data Coding			Binary Two's Complement or Straight Binary					
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*		*	V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

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Right margin: **ADS7806** · **2** · **A/D CONVERTERS, DATA ACQUISITION COMPONENTS**

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7806P, U			ADS7806PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	$R_L = 3.3k\Omega$, $C_L = 50pF$			83			*	ns
Bus Relinquish Time	$R_L = 3.3k\Omega$, $C_L = 10pF$			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{ANA}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6				*	mA
I_{ANA}			5.0				*	mA
Power Dissipation	$V_{ANA} = V_{DIG} = 5V$, $f_S = 40kHz$		28	35		*	*	mW
	REFD HIGH		23				*	mW
	PWRD and REFD HIGH		50				*	µW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	°C
Derated Performance		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7806 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 X FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$ .... ±25V
$R2_{IN}$ .... ±25V
CAP .... V_{ANA} +0.3V to AGND2 –0.3V
REF .... Indefinite Short to AGND2,
Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, and AGND2 .... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} .... +0.3V
V_{DIG} 7V
Digital Inputs .... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature .... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) .... +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO- (NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7806P	±0.9	70	–40°C to +85°C	Plastic DIP
ADS7806PB	±0.45	72	–40°C to +85°C	Plastic DIP
ADS7806U	±0.9	70	–40°C to +85°C	SOIC
ADS7806UB	±0.45	72	–40°C to +85°C	SOIC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7806P	Plastic DIP	246
ADS7806PB	Plastic DIP	246
ADS7806U	SOIC	217
ADS7806UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	R1$_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Ground.
3	R2$_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground.
7	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{INT}$	I	External/Internal data clock select.
9	D7	O	Data Bit 3 if BYTE is HIGH. Data bit 11 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
11	D5	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
12	D4	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
13	D3	O	LOW if BYTE is HIGH. Data bit 7 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D2	O	LOW if BYTE is HIGH. Data bit 6 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
16	D1	O	LOW if BYTE is HIGH. Data bit 5 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
17	D0	O	LOW if BYTE is HIGH. Data bit 4 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK.
20	TAG	I	Serial Input When Using an External Data Clock.
21	BYTE	I	Selects 8 most significant bits (LOW) or 4 least significant bits (HIGH).
22	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
23	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V$_{ANA}$		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V$_{DIG}$		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ V$_{ANA}$.

TABLE I. Pin Assignments.

PIN CONFIGURATION

R1$_{IN}$	1		28	V$_{DIG}$
AGND1	2		27	V$_{ANA}$
R2$_{IN}$	3		26	REFD
CAP	4		25	PWRD
REF	5		24	$\overline{BUSY}$
AGND2	6		23	$\overline{CS}$
SB/$\overline{BTC}$	7	ADS7806	22	R/$\overline{C}$
EXT/$\overline{INT}$	8		21	BYTE
D7	9		20	TAG
D6	10		19	SDATA
D5	11		18	DATACLK
D4	12		17	D0
D3	13		16	D1
DGND	14		15	D2

ANALOG INPUT RANGE	CONNECT R1$_{IN}$ VIA 200Ω TO	CONNECT R2$_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V$_{IN}$	CAP	45.7kΩ
0V to 5V	AGND	V$_{IN}$	20.0kΩ
0V to 4V	V$_{IN}$	V$_{IN}$	21.4kΩ

TABLE II. Input Range Connections. See also Figure 7.

ADS7806

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

TYPICAL PERFORMANCE CURVES

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)

FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)

SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)

SIGNAL-TO-(NOISE + DISTORTION) vs INPUT FREQUENCY
AND INPUT AMPLITUDE (T_A = +25°C)

SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

All Codes INL

All Codes DNL

POWER SUPPLY RIPPLE SENSITIVITY
INL/DNL DEGRADATION PER LSB OF P-P RIPPLE

ENDPOINT ERRORS (20V BIPOLAR RANGE)

BPO Error

+F_S Error

−F_S Error

ENDPOINT ERRORS (UNIPOLAR RANGES)

UPO Error

+F_S Error (4V Range)

+F_S Error (5V Range)

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE

CONVERSION TIME vs TEMPERATURE

ADS7806

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BASIC OPERATION

PARALLEL OUTPUT

Figure 1a shows a basic circuit to operate the ADS7806 with a ±10V input range and parallel output. Taking pin 22 LOW for 40ns (12μs max) will initiate a conversion. Pin 24 will go LOW and stay LOW until the conversion is completed and the output register is updated. If pin 21 is LOW, the 8 most significant bits will be valid when pin 24 rises; if pin 21 is HIGH, the 4 least significant bits will be valid when pin 24 rises. Data will be output in Binary Two's Complement format. Pin 24 going HIGH can be used to latch the data. After the first byte has been read, pin 21 can be toggled allowing the remaining byte to be read. All convert commands will be ignored while pin 24 is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25μs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

SERIAL OUTPUT

Figure 1b shows a basic circuit to operate the ADS7806 with a ±10V input range and serial output. Taking pin 22 LOW for 40ns (12μs max) will initiate a conversion and output valid data from the previous conversion on pin 19 synchronized to 12 clock pulses output on pin 18. Pin 24 will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. Pin 24 going HIGH can be used to latch the data. All convert commands will be ignored while pin 24 is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25μs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7806 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

FIGURE 1. Basic ±10V Operation, both Parallel and Serial Output.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables III and IV for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 6 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".

Table III. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion 'n', serial data from conversion 'n-1' will be output on SDATA (pin 19) following the start of conversion 'n'. See **Internal Data Clock** in the **Reading Data** section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

READING DATA

The ADS7806 outputs serial or parallel data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{BTC}$ (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table V for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
0	↓	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion "n" completed. Valid data from conversion "n" clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	↑	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	0	↑	X	X	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion "n-1".

Table IV. Control Functions When Using Serial Output.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
				BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	1.22mV	976µV				
+Full Scale (FS – 1LSB)	9.99512V	4.99878V	3.999024V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	2.5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	2.49878V	1.999024V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table V. Output Codes and Ideal Input Voltages.

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port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port. But data cannot be read through the serial port prior to reading the same data on the parallel port.

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{\text{INT}}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{\text{C}}$ (pin 22) is HIGH and $\overline{\text{CS}}$ (pin 23) is LOW. Any other combination of $\overline{\text{CS}}$ and R/$\overline{\text{C}}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17) . When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 4 least significant bits will be valid with the LSB on D4. BYTE can be toggled to read both bytes within one conversion cycle.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pin 9-13 and 15-17). $\overline{\text{BUSY}}$ going high can be used to latch the data. Refer to Table VI and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to read data from 12µs after the start of conversion 'n' until $\overline{\text{BUSY}}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table VI and Figures 2 and 3 for timing constraints.

FIGURE 2. Conversion Timing with Parallel Output ($\overline{\text{CS}}$ and DATACLK tied LOW, EXT/$\overline{\text{INT}}$ tied HIGH).

FIGURE 3. Using $\overline{\text{CS}}$ to Control Conversion and Read Timing with Parallel Outputs.

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_2	Data Valid Delay after R/$\overline{C}$ LOW		14.7	20	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			85	ns
t_4	$\overline{BUSY}$ LOW		14.7	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		14.7	20	µs
t_8	Acquisition Time			5	µs
t_9	Bus Relinquish Time	10		83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	20	60		ns
t_{11}	Previous Data Valid after Start of Conversion	12	14.7		µs
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{16}	Data Valid after DATACLK LOW Delay	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK LOW	40			ns
t_{19}	External DATACLK HIGH	50			ns
t_{20}	$\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time	25			ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{22}	Valid Data after DATACLK HIGH	25			ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE VI. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7806 will output 12 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 19), synchronized to 12 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7806, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 19) after conversion 'n' is completed or during conversion 'n + 1'.

Note! The number of control lines can be reduced by tying $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. From 12µs after the start of conversion 'n' until $\overline{BUSY}$ rises, the internal logic will shift conversion 'n' results into the output register. During this period of the conversion cycle, the external data clock must be LOW (when in read mode) or the ADS7806 must be taken out of the read mode (when using a continuous external data clock). Violating this condition may result in data loss.

NOTE: (1) If controlling with $\overline{CS}$, tie R/$\overline{C}$ LOW. Data bus pins will remain Hi-Z at all times.
If controlling with R/$\overline{C}$, tie $\overline{CS}$ LOW. Data bus pins will be active when R/C is HIGH, and should be left unconnected.

FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

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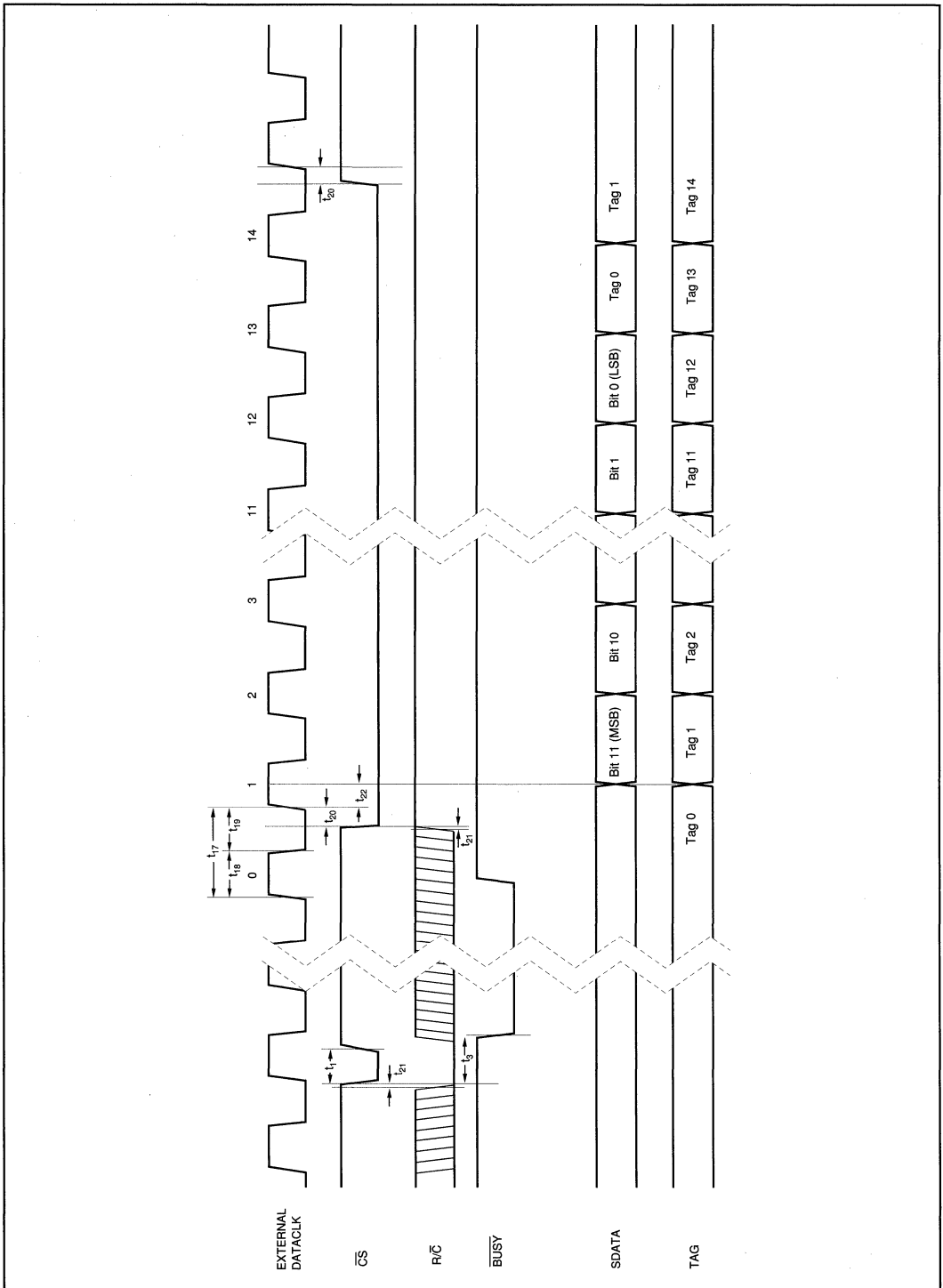
FIGURE 5. Conversion and Read Timing with External Clock (EXT/INT Tied HIGH) Read after Conversion.
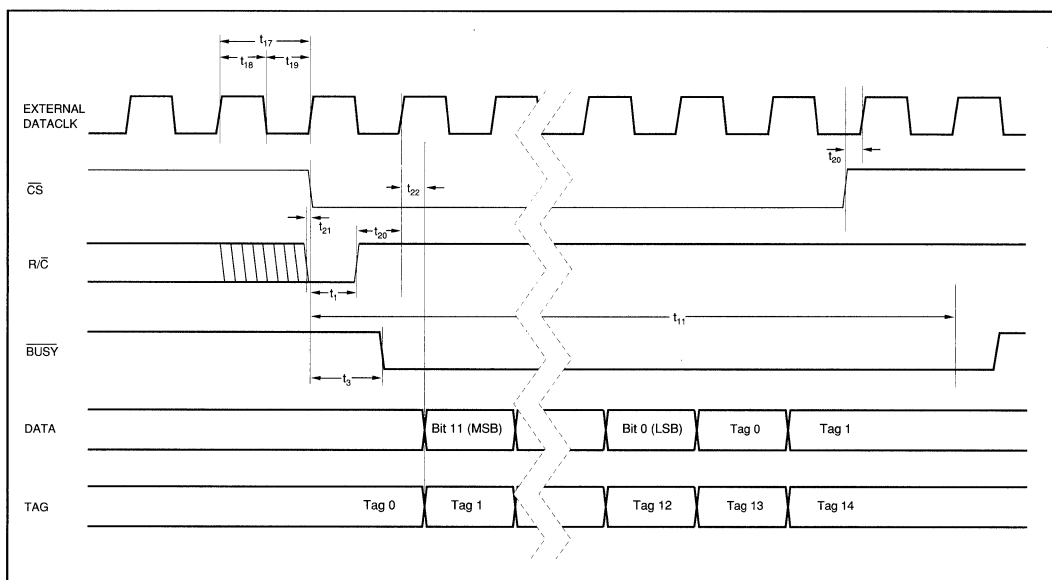
FIGURE 6. Conversion and Read Timing with External Clock (EXT/INT tied HIGH) Read During a Conversion.

EXTERNAL DATA CLOCK
(After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 12th falling edge and 13th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 13th falling edge and the 14th rising edge of DATACLK; the second input bit will be valid on the 14th falling edge and the 15th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table VI and Figure 5.

EXTERNAL DATA CLOCK
(During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to clock out data from 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

TAG FEATURE

TAG (Pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 12 bits of valid data have been output.

INPUT RANGES

The ADS7806 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 7a and 7b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error[1] specifications are tested and guaranteed with the fixed resistors shown in Figure 7b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

used for each input range. The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

The digital output will increase for an increasing analog input until digital full scale has been achieved (7FF for Binary Two's Complement); likewise for a decreasing analog signal (800 for Binary Two's Complement).

The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

CALIBRATION

The ADS7806 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7806, install the proper resistors and potentiometers as shown in Figure 7a. The calibration range is ±15mV for the offset and ±60mV for the gain.
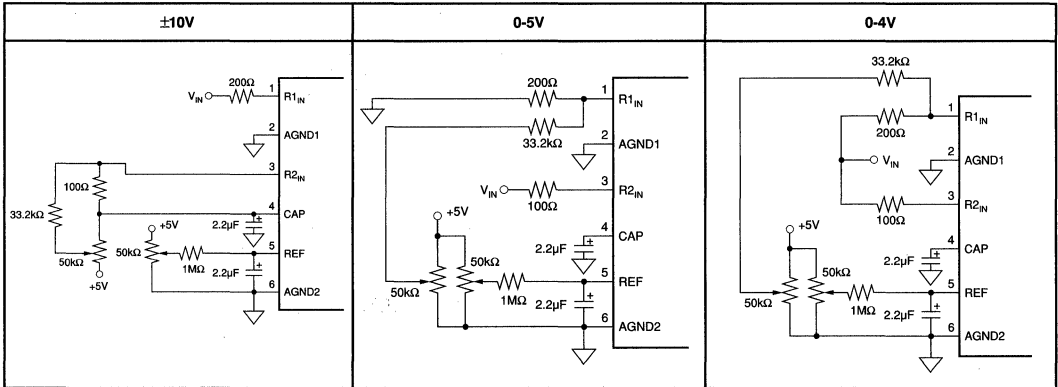
FIGURE 7a. Circuit Diagrams (With Hardware Trim).
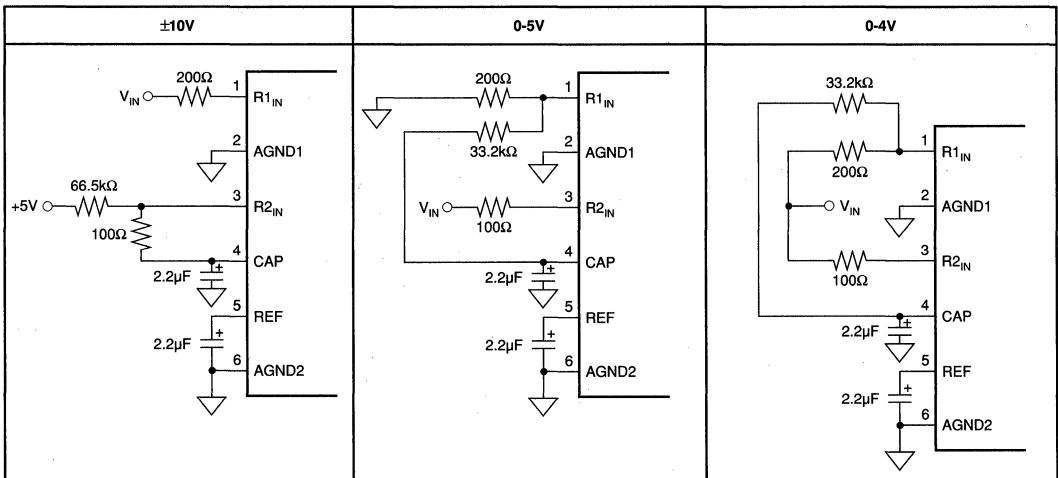
FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7806, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Tables VII and VIII for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPO	−10 < BPZ < 10 −2 ≤ BPZ ≤ 2	−45 < BPZ < 5 −10 ≤ BPZ ≤ 1	mV LSBs
Gain Error	−0.5 < error < 0.5 −0.25 < error < 0.25[1]	−0.6 < error < −0.55 −0.45 < error < −0.3[1]	% of FSR
NOTE: (1) High Grade.			

TABLE VII. Bipolar Offset and Gain Errors With and Without External Resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
UPO	−3 < BPZ < 3 −1 ≤ BPZ ≤ 1	−15 < BPZ < −3 −3 ≤ BPZ ≤ −1	mV LSBs
Gain Error	−0.5 < error < 0.5 −0.25 < error < 0.25[1]	−1.25 < error < −0.25 −1 < error < −0.50[1]	% of FSR
NOTE: (1) High Grade.			

TABLE VIII. Unipolar Offset and Gain Errors With and Without External Resistors.

NO CALIBRATION

See Figure 7b for circuit connections. The external resistors shown in Figure 7b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer functions, both bipolar and unipolar, will be bound by the shaded region seen in Figures 8 and 9 when the external resistors are not used. The typical bipolar offset will be −20mV with a typical gain error of −0.60%. The typical unipolar offset will be −9mV with a typical gain error of −0.75%. Refer to Tables VII and VIII for range of offset and gain errors with and without external resistors.

REFERENCE

The ADS7806 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed; REFD (pin 26) tied HIGH will power-down the internal reference reducing the overall power consumption of the ADS7806 by approximately 5mW.

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).
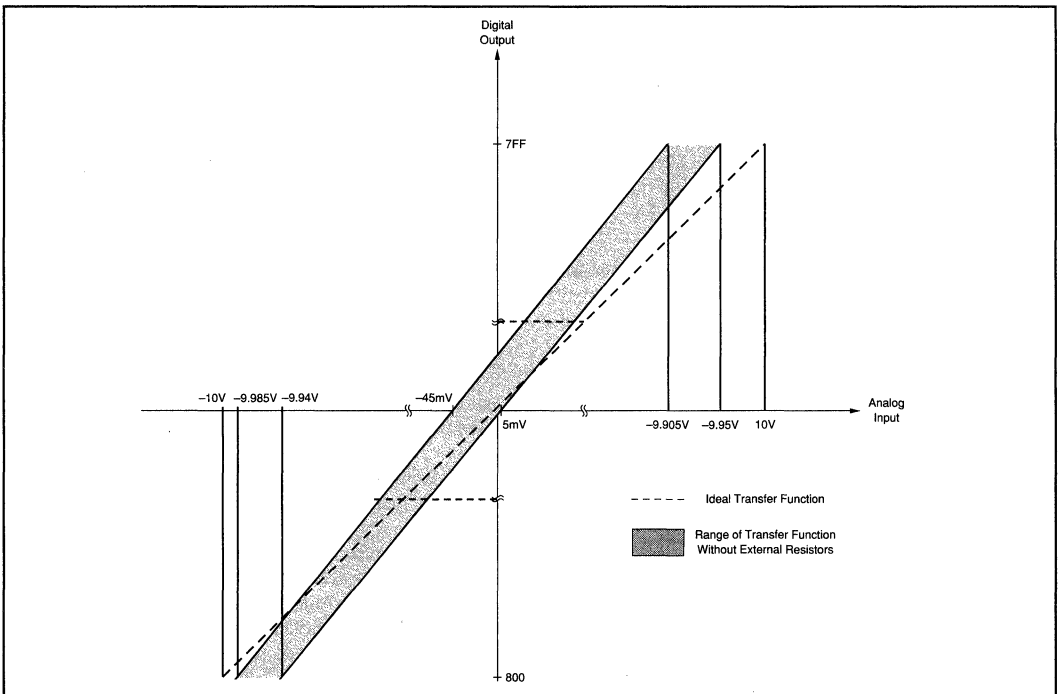
FIGURE 8. Bipolar Transfer Function.
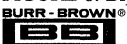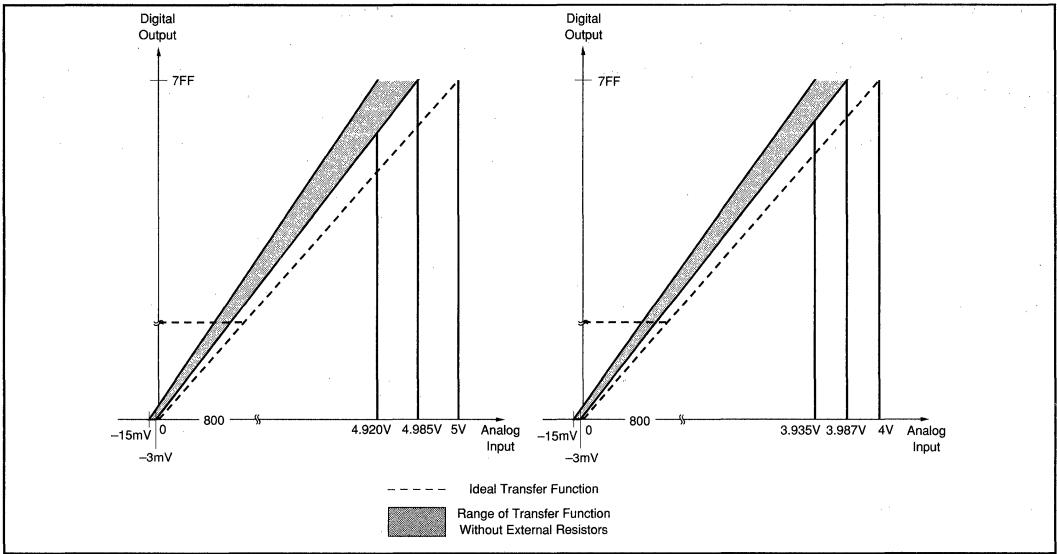
FIGURE 9. Unipolar Transfer Functions.

The ADS7806 also has an internal buffer for the reference voltage. See Figure 10 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

FIGURE 10. Characteristic Impedances of Internal Buffer.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

REFERENCE AND POWER DOWN

The ADS7806 has analog power down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26) respectively. PWRD and REFD HIGH will power down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms. With +5V applied to V_{DIG}, the digital circuitry of the ADS7806 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD HIGH will power down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

REFD

REFD HIGH will power down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

FIGURE 11. Power-Down to Power-Up. Time to rated accuracy vs capacitor value on CAP.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7806 uses 90% of its power for the analog circuitry. The ADS7806 should be considered as an analog component.

The +5V power for the ADS should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7806. D_{GND} is the digital supply ground. A_{GND2} is the analog supply ground. A_{GND1} is the ground which all analog signals internal to the A/D are referenced. A_{GND1} is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7806 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7806.

The resistive front end of the ADS7806 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7806 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7806 has an internal LSB size of 610μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7807 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of 38μV.

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APPLICATIONS INFORMATION

QSPI INTERFACING

Figure 12 shows a simple interface between the ADS7806 to any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7806 is the only serial peripheral.

Before enabling the QSPI interface, the microcontroller must monitor the slave select line. When a transition from LOW to HIGH occurs on Slave Select (SS) from $\overline{\text{BUSY}}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the and the A/D may be "out-of-sync."
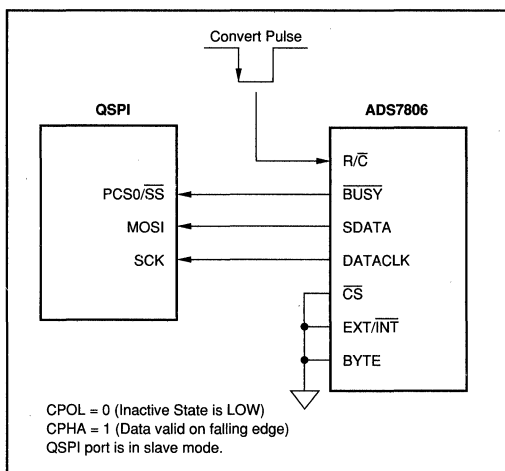
FIGURE 12. QSPI Interface to the ADS7806.

Figure 13 shows another interface between the ADS7806 and a QSPI equipped microcontroller. The interface allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7806 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated and prevent a conversion from taking place.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an eight bit transfer, causes PCS0 (R/$\overline{\text{C}}$) and PCS1 ($\overline{\text{CS}}$) to go LOW starting a conversion. The second, a twelve bit transfer, causes only PCS1 ($\overline{\text{CS}}$) to go LOW. This is when the valid data will be transferred.
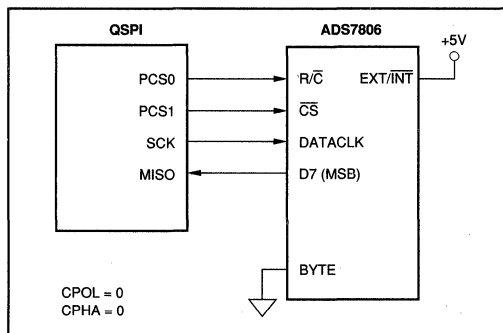
FIGURE 13. QSPI Interface to the ADS7806. Processor Initiates Conversions.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7806. This timing is thus locked to the crystal based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to two (4.19MHz SCK), DT set to ten, the first serial transfer set to eight bits, the second set to twelve bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first eight bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the eight bit transfer should be set to 20H and for the twelve bit transfer to 61H.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 12. The microcontroller will probably have to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 13 might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse itself.

DSP56000 INTERFACING

The DSP56000 serial interface has an SPI compatiblity mode with some enhancements. Figure 14 shows an interface between the ADS7806 and the DSP56000 which is very similar to the QSPI interface seen in Figure 12. As mentioned in the QSPI section, the DSP56000 must enable the interface when a LOW to HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 15. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to two). The prescale modulus should be set to five.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet suggests that the pulse width is (0.7)RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the **Starting A Conversion** section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is 35.6kHz. If a slower oscillator can be tolerated on the DSP56000, a conversion rate of 40kHz can be achieved by using a 19.2MHz clock and a prescale modulus of four.

FIGURE 14. DSP56000 Interface to the ADS7806.
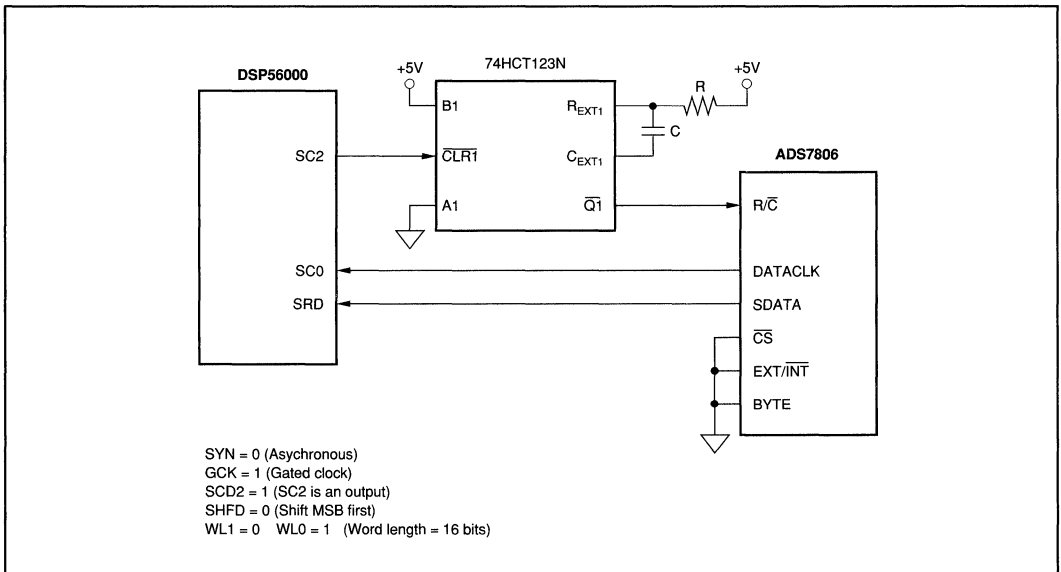
FIGURE 15. DSP56000 Interface to the ADS7806. Processor Initiates Conversions.

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BURR - BROWN®

BB
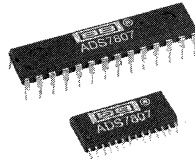
ADS7807

DEMO BOARD AVAILABLE
See Appendix A for more information.

Low-Power 16-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

● **35mW max POWER DISSIPATION**
● **50μW POWER DOWN MODE**
● **25μs max ACQUISITION AND CONVERSION**
● **±1.5LSB max INL**
● **DNL: 16-bits "No Missing Codes"**
● **86dB min SINAD WITH 1kHz INPUT**
● **±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES**
● **SINGLE +5V SUPPLY OPERATION**
● **PARALLEL AND SERIAL DATA OUTPUT**
● **PIN-COMPATIBLE WITH 12-BIT ADS7806**
● **USES INTERNAL OR EXTERNAL REFERENCE**
● **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7807 is a low-power, 16-bit, sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7807 can acquire and convert 16-bits to within ±1.5LSB in 25μs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7807 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.

PDS-1159C   **BURR - BROWN®** **BB**

SPECIFICATIONS

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U MIN	ADS7807P, U TYP	ADS7807P, U MAX	ADS7807PB, UB MIN	ADS7807PB, UB TYP	ADS7807PB, UB MAX	UNITS
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table II)				
Capacitance			35				*	pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, −2			+1.5, −1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			0.8			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error[3]	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error[3]	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down[5]	2.2µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_S$)	$+4.75V < V_S < +5.25V$			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 1kHz, ±10V$	90	100		96	*		dB[6]
Total Harmonic Distortion	$f_{IN} = 1kHz, ±10V$		−100	−90		*	−96	dB
Signal-to-(Noise+Distortion)	$f_{IN} = 1kHz, ±10V$	83	88		86	*		dB
	−60dB Input		30			32		dB
Signal-to-Noise	$f_{IN} = 1kHz, ±10V$	83	88		86	*		dB
Full-Power Bandwidth[7]			130			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		
Transient Response	FS Step			5			*	µs
Overvoltage Recovery[8]			750			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	$V_{IL} = 0V$			±10			*	µA
I_{IH}	$V_{IH} = 5V$			±10			*	µA
DIGITAL OUTPUTS								
Data Format			Parallel 16-bits in 2-bytes; Serial					
Data Coding			Binary Two's Complement or Straight Binary					
V_{OL}	$I_{SINK} = 1.6mA$			+0.4			*	V
V_{OH}	$I_{SOURCE} = 500µA$	+4			*			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 40kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U			ADS7807PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	$R_L = 3.3k\Omega$, $C_L = 50pF$			83			*	ns
Bus Relinquish Time	$R_L = 3.3k\Omega$, $C_L = 10pF$			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{ANA}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6			*		mA
I_{ANA}			5.0			*		mA
Power Dissipation	$V_{ANA} = V_{DIG} = 5V$, $f_S = 40kHz$		28	35		*	*	mW
	REFD HIGH		23			*		mW
	PWRD and REFD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 305µV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7807 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 X FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: R1$_{IN}$ .... ±25V
R2$_{IN}$ .... ±25V
CAP .... V_{ANA} +0.3V to AGND2 –0.3V
REF .... Indefinite Short to AGND2,
Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, and AGND2 .... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} .... +0.3V
V_{DIG} 7V
Digital Inputs .... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature .... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) .... +300°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	GUARANTEED NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7807P	±3	15	83	–40°C to +85°C	Plastic DIP
ADS7807PB	±1.5	16	86	–40°C to +85°C	Plastic DIP
ADS7807U	±3	15	83	–40°C to +85°C	SOIC
ADS7807UB	±1.5	16	86	–40°C to +85°C	SOIC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7807P	Plastic DIP	246
ADS7807PB	Plastic DIP	246
ADS7807U	SOIC	217
ADS7807UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	R1$_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Ground.
3	R2$_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground.
7	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{INT}$	I	External/Internal data clock select.
9	D7	O	Data Bit 7 if BYTE is HIGH. Data bit 15 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 6 if BYTE is HIGH. Data bit 14 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
11	D5	O	Data Bit 5 if BYTE is HIGH. Data bit 13 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
12	D4	O	Data Bit 4 if BYTE is HIGH. Data bit 12 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
13	D3	O	Data Bit 3 if BYTE is HIGH. Data bit 11 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D2	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
16	D1	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
17	D0	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK.
20	TAG	I	Serial Input When Using an External Data Clock.
21	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
22	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
23	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V$_{ANA}$		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V$_{DIG}$		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be $\leq$ V$_{ANA}$.

TABLE I. Pin Assignments.

PIN CONFIGURATION

	ADS7807	
R1$_{IN}$ 1		28 V$_{DIG}$
AGND1 2		27 V$_{ANA}$
R2$_{IN}$ 3		26 REFD
CAP 4		25 PWRD
REF 5		24 $\overline{BUSY}$
AGND2 6		23 $\overline{CS}$
SB/$\overline{BTC}$ 7		22 R/$\overline{C}$
EXT/$\overline{INT}$ 8		21 BYTE
D7 9		20 TAG
D6 10		19 SDATA
D5 11		18 DATACLK
D4 12		17 D0
D3 13		16 D1
DGND 14		15 D2

ANALOG INPUT RANGE	CONNECT R1$_{IN}$ VIA 200Ω TO	CONNECT R2$_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V$_{IN}$	CAP	45.7kΩ
0V to 5V	AGND	V$_{IN}$	20.0kΩ
0V to 4V	V$_{IN}$	V$_{IN}$	21.4kΩ

TABLE II. Input Range Connections. See also Figure 7.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

TYPICAL PERFORMANCE CURVES

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)

FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)

SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)

SIGNAL-TO-(NOISE + DISTORTION) vs INPUT FREQUENCY
AND INPUT AMPLITUDE (T_A = +25°C)

SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

ALL CODES INL

ALL CODES DNL

POWER SUPPLY RIPPLE SENSITIVITY
INL/DNL DEGRADATION PER LSB OF P-P RIPPLE

ENDPOINT ERRORS (20V BIPOLAR RANGE)

ENDPOINT ERRORS (UNIPOLAR RANGES)

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE

CONVERSION TIME vs TEMPERATURE

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

BASIC OPERATION

PARALLEL OUTPUT

Figure 1a shows a basic circuit to operate the ADS7807 with a ±10V input range and parallel output. Taking pin 22 LOW for a minimum of 40ns (12μs max) will initiate a conversion. Pin 24 will go LOW and stay LOW until the conversion is completed and the output register is updated. If pin 21 is LOW, the 8 most significant bits will be valid when pin 24 rises; if pin 21 is HIGH, the 8 least significant bits will be valid when pin 24 rises. Data will be output in Binary Two's Complement format. Pin 24 going HIGH can be used to latch the data. After the first byte has been read, pin 21 can be toggled allowing the remaining byte to be read. All convert commands will be ignored while pin 24 is LOW.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25μs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

SERIAL OUTPUT

Figure 1b shows a basic circuit to operate the ADS7807 with a ±10V input range and serial output. Taking pin 22 LOW for 40ns (12μs max) will initiate a conversion and output

valid data from the previous conversion on pin 19 synchronized to 16 clock pulses output on pin 18. Pin 24 will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. Pin 24 going HIGH can be used to latch the data. All convert commands will be ignored while pin 24 is LOW.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25μs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7807 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

FIGURE 1. Basic ±10V Operation, both Parallel and Serial Output.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables III and IV for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 6 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"[(1)]. Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".

Table III. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion 'n', serial data from conversion 'n-1' will be output on SDATA (pin 19) following the start of conversion 'n'. See **Internal Data Clock** in the **Reading Data** section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

READING DATA

The ADS7807 outputs serial or parallel data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{BTC}$ (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table V for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
0	↓	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion "n" completed. Valid data from conversion "n" clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	↑	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	0	↑	X	X	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion "n-1".

Table IV. Control Functions When Using Serial Output.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT				
				BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)		
Full-Scale Range	±10	0V to 5V	0V to 4V					
Least Significant Bit (LSB)	305µV	76µV	61µV		HEX			HEX
				BINARY CODE	CODE	BINARY CODE		CODE
+Full Scale (FS – 1LSB)	9.999695V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111		FFFF
Midscale	0V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000		8000
One LSB Below Midscale	–305µV	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111		7FFF
–Full Scale	–10V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000		0000

Table V. Output Codes and Ideal Input Voltages.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port. But data cannot be read through the serial port prior to reading the same data on the parallel port.

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{\text{INT}}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{\text{C}}$ (pin 22) is HIGH and $\overline{\text{CS}}$ (pin 23) is LOW. Any other combination of $\overline{\text{CS}}$ and R/$\overline{\text{C}}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17) . When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 8 least significant bits will be valid with the LSB on D0. BYTE can be toggled to read both bytes within one conversion cycle.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pin 9-13 and 15-17). $\overline{\text{BUSY}}$ going high can be used to latch the data. Refer to Table VI and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12μs after the start of conversion 'n'. Do not attempt to read data from 12μs after the start of conversion 'n' until $\overline{\text{BUSY}}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table VI and Figures 2 and 3 for timing constraints.

FIGURE 2. Conversion Timing with Parallel Output ($\overline{\text{CS}}$ and DATACLK tied LOW, EXT/$\overline{\text{INT}}$ tied HIGH).

FIGURE 3. Using $\overline{\text{CS}}$ to Control Conversion and Read Timing with Parallel Outputs.

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active. Refer to the **Applications Information** section for specific serial interfaces.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	μs
t_2	Data Valid Delay after R/$\overline{C}$ LOW		19	20	μs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			85	ns
t_4	$\overline{BUSY}$ LOW		19	20	μs
t_5	$\overline{BUSY}$ Delay after End of Conversion			90	ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		19	20	μs
t_8	Acquisition Time			5	μs
t_9	Bus Relinquish Time	10		83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	20	60		ns
t_{11}	Previous Data Valid after Start of Conversion	12	19		μs
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		μs
t_{14}	DATACLK Period		1.1		μs
t_{15}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{16}	Data Valid after DATACLK LOW Delay	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK LOW	40			ns
t_{19}	External DATACLK HIGH	50			ns
t_{20}	$\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time	25			ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{22}	Valid Data after DATACLK HIGH	25			ns
$t_7 + t_8$	Throughput Time			25	μs

TABLE VI. Conversion and Data Timing. $T_A = -40°C$ to +85°C.

INTERNAL DATA CLOCK (During Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7807 will output 16 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 19), synchronized to 16 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 16th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7807, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 19) after conversion 'n' is completed or during conversion 'n + 1'.

Note! The number of control lines can be reduced by tying $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. From 12μs after the start of conversion 'n' until $\overline{BUSY}$ rises, the internal logic will shift conversion 'n' results into the output register. During this period of the conversion cycle, the external data clock must be LOW (when in read mode) or the ADS7807 must be taken out of the read mode (when using a continuous external data clock). Violating this condition may result in data loss.

NOTE: (1) If controlling with $\overline{CS}$, tie R/$\overline{C}$ LOW. Data bus pins will remain Hi-Z at all times.
If controlling with R/$\overline{C}$, tie $\overline{CS}$ LOW. Data bus pins will be active when R/$\overline{C}$ is HIGH, and should be left unconnected.

FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

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FIGURE 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied HIGH) Read after Conversion.

FIGURE 6. Conversion and Read Timing with External Clock (EXT/$\overline{\text{INT}}$ tied HIGH) Read During a Conversion.

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EXTERNAL DATA CLOCK
(After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 24) will go HIGH. With $\overline{\text{CS}}$ LOW and R/$\overline{\text{C}}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 16th falling edge and 17th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 17th falling edge and the 18th rising edge of DATACLK; the second input bit will be valid on the 18th falling edge and the 19th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table VI and Figure 5.

EXTERNAL DATA CLOCK
(During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12μs after the start of conversion 'n'. Do not attempt to clock out data from 12μs after the start of conversion 'n' until $\overline{\text{BUSY}}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

TAG FEATURE

TAG (Pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 16 bits of valid data have been output.

INPUT RANGES

The ADS7807 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 7a and 7b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error[1] specifications are tested and guaranteed with the fixed resistors shown in Figure 7b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

used for each input range. The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

The digital output will increase for an increasing analog input until digital full scale has been achieved (7FFF for Binary Two's Complement); likewise for a decreasing analog signal (8000 for Binary Two's Complement).

The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

CALIBRATION

The ADS7807 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7807, install the proper resistors and potentiometers as shown in Figure 7a. The calibration range is ±15mV for the offset and ±60mV for the gain.

FIGURE 7a. Circuit Diagrams (With Hardware Trim).

FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7807, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Tables VII and VIII for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPO	−10 < BPZ < 10 −33 ≤ BPZ ≤ 33	−45 < BPZ < 5 −147 ≤ BPZ ≤ 16	mV LSBs
Gain Error	−0.5 < error < 0.5 −0.25 < error < 0.25[1]	−0.6 < error < −0.55 −0.45 < error < −0.3[1]	% of FSR
NOTE: (1) High Grade.			

TABLE VII. Bipolar Offset and Gain Errors With and Without External Resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
UPO	−3 < BPZ < 3 −10 ≤ BPZ ≤ 10	−15 < BPZ < −3 −49 ≤ BPZ ≤ −9	mV LSBs
Gain Error	−0.5 < error < 0.5 −0.25 < error < 0.25[1]	−1.25 < error < −0.25 −1 < error < −0.50[1]	% of FSR
NOTE: (1) High Grade.			

TABLE VIII. Unipolar Offset and Gain Errors With and Without External Resistors.

NO CALIBRATION

See Figure 7b for circuit connections. The external resistors shown in Figure 7b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer functions, both bipolar and unipolar will be bound by the shaded region seen in Figures 8 and 9 when the external resistors are not used. The typical bipolar offset will be −20mV with a typical gain error of −0.60%. The typical unipolar offset will be −9mV with a typical gain error of −0.75%. Refer to Tables VII and VIII for range of offset and gain errors with and without external resistors.

REFERENCE

The ADS7807 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed; REFD (pin 26) tied HIGH will power-down the internal reference reducing the overall power consumption of the ADS7807 by approximately 5mW.

The internal reference has approximately a 15 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).
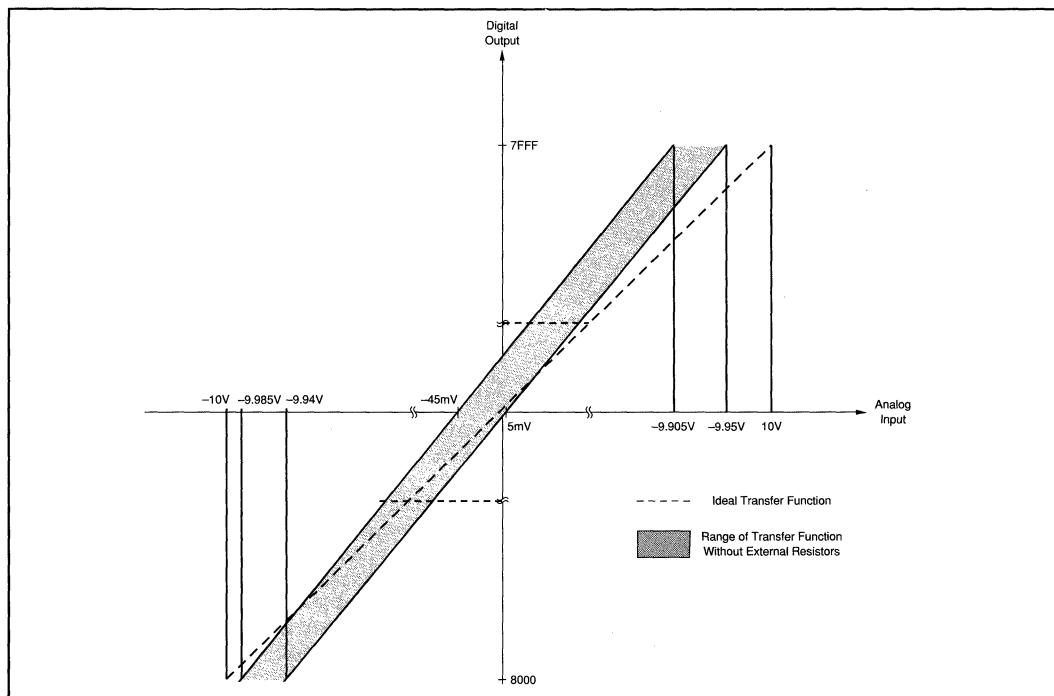
FIGURE 8. Bipolar Transfer Function.
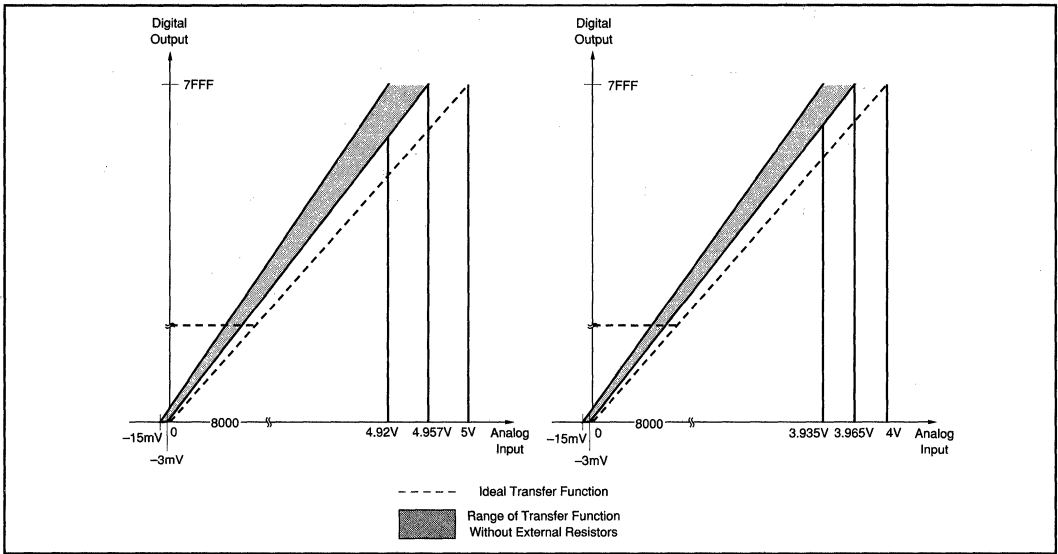
FIGURE 9. Unipolar Transfer Functions.

The ADS7807 also has an internal buffer for the reference voltage. See Figure 10 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

FIGURE 10. Characteristic Impedances of Internal Buffer.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

REFERENCE AND POWER DOWN

The ADS7807 has analog power down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26) respectively. PWRD and REFD HIGH will power down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms. With +5V applied to V_{DIG}, the digital circuitry of the ADS7807 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD HIGH will power down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

REFD

REFD HIGH will power down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

FIGURE 11. Power-Down to Power-Up Time to Rated Accuracy vs Capacitor Value on CAP.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7807 uses 90% of its power for the analog circuitry. The ADS7807 should be considered as an analog component.

The +5V power for the ADS should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7807. D_{GND} is the digital supply ground. A_{GND2} is the analog supply ground. A_{GND1} is the ground which all analog signals internal to the A/D are referenced. A_{GND1} is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADC should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7807 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7807.

The resistive front end of the ADS7807 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7807 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7807 has an internal LSB size of 38µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

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APPLICATIONS INFORMATION

TRANSITION NOISE

Apply a DC input to the ADS7807 and initiate 1000 conversions. The digital output of the converter will vary in output codes due to the internal noise of the ADS7807. This is true for all 16-bit SAR converters. The transition noise specification found in the electrical specifications section is a statistical figure which represents the one sigma limit or rms value of these output codes.

Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal output code for the input voltage value. The $\pm 1\sigma$, $\pm 2\sigma$, and $\pm 3\sigma$ distributions will represent 68.3%, 95.5%, and 99.7% of all codes. Multiplying TN by 6 will yield the $\pm 3\sigma$ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the 5 code distribution when executing 1000 conversions. The ADS7807 has a TN of 0.8 LSBs which yields 5 output codes for a $\pm 3\sigma$ distribution. See Figures 12 and 13 for 1000 and 10,000 conversion histogram results.

AVERAGING

The noise of the converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$ where n is the number of averages. For example, averaging four conversion results will reduce the TN by 1/2 to 0.4 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to lowpass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by two, the signal-to-noise ratio will improve 3dB.

FIGURE 13. Histogram of 10,000 Conversions with Input Grounded.

QSPI INTERFACING

Figure 14 shows a simple interface between the ADS7807 to any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7807 is the only serial peripheral.

Before enabling the QSPI interface, the microcontroller must monitor the slave select line. When a transition from LOW to HIGH occurs on Slave Select ($\overline{SS}$) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the A/D may be "out-of-sync".

FIGURE 12. Histogram of 1000 Conversions with Input Grounded.
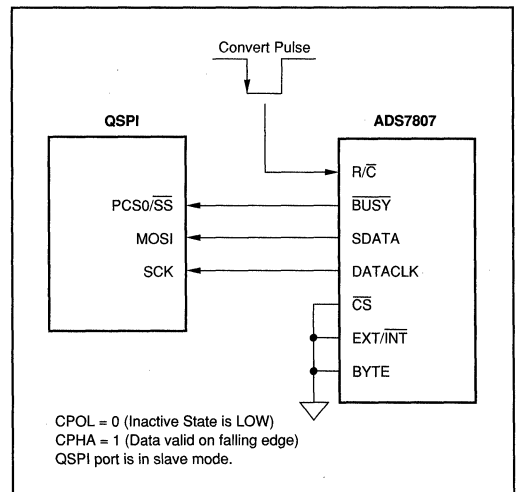
FIGURE 14. QSPI Interface to the ADS7807.

Figure 15 shows another interface between the ADS7807 and a QSPI equipped microcontroller which allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7807 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated.
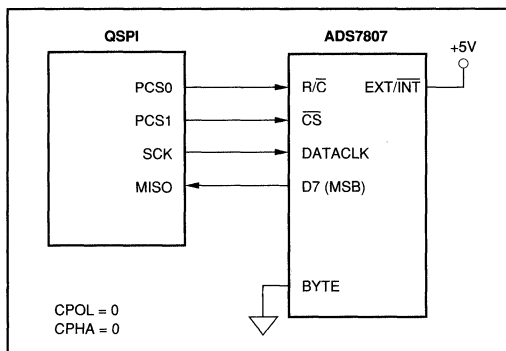
FIGURE 15. QSPI Interface to the ADS7807. Processor Initiates Conversions.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an eight bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go LOW starting a conversion. The second, a sixteen bit transfer, causes only PCS1 ($\overline{CS}$) to go LOW. This is when the valid data will be transferred.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7807. This timing is thus locked to the crystal based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to two (4.19MHz SCK), DT set to ten, the first serial transfer set to eight bits, the second set to 16 bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first eight bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the eight bit transfer should be set to 20H and for the sixteen bit transfer to 61H.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 14. The microcontroller will probably have to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 15 might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse itself.

DSP56000 INTERFACING

The DSP56000 serial interface has SPI compatibility mode with some enhancements. Figure 16 shows an interface between the ADS7807 and the DSP56000 which is very similar to the QSPI interface seen in Figure 14. As mentioned in the QSPI section, the DSP56000 must enable the interface when a LOW to HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).
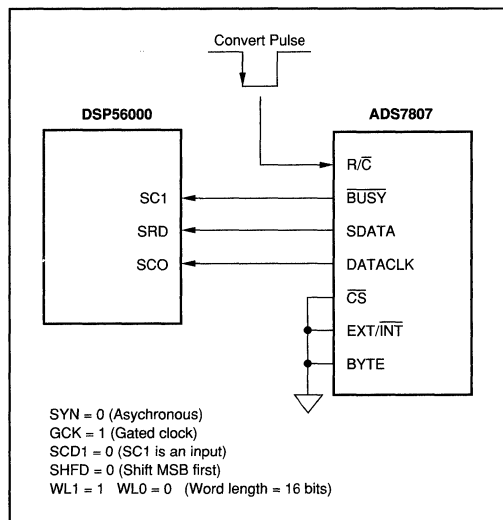
FIGURE 16. DSP56000 Interface to the ADS7807.

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 17. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit

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frame (frame rate divider set to two). The prescale modulus should be set to three.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet suggests that the pulse width is (0.7) RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the **Starting A Conversion** section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is exactly 40kHz. Note that this will not be the case for the ADS7806. See the ADS7806 data sheet for more information.
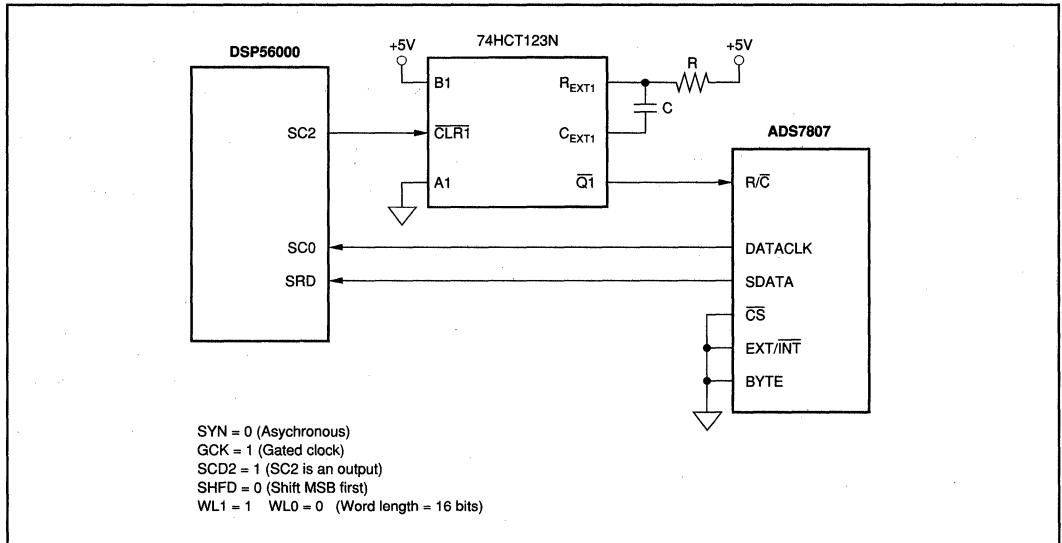
FIGURE 17. DSP56000 Interface to the ADS7807. Processor Initiates Conversions.

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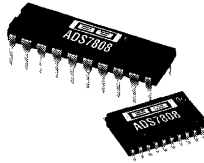
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DEMO BOARD AVAILABLE
See Appendix A for more information.

12-Bit 10μs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

● **100kHz SAMPLING RATE**
● **72dB SINAD WITH 45kHz INPUT**
● **±1/2 LSB INL AND DNL**
● **SIX SPECIFIED INPUT RANGES**
● **SERIAL OUTPUT**
● **SINGLE +5V SUPPLY OPERATION**
● **PIN-COMPATIBLE WITH 16-BIT ADS7809**
● **USES INTERNAL OR EXTERNAL REFERENCE**
● **100mW MAX POWER DISSIPATION**
● **20-PIN 0.3" PLASTIC DIP AND SOIC**
● **SIMPLE DSP INTERFACE**

DESCRIPTION

The ADS7808 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a 12-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7808 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7808 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7808 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

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ADS7808

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SPECIFICATIONS

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808P/U MIN	ADS7808P/U TYP	ADS7808P/U MAX	ADS7808PB/UB MIN	ADS7808PB/UB TYP	ADS7808PB/UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges				±10V, 0V to 5V, etc. (See Table I)				
Impedance				See Table I				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			5.7	8		*	*	μs
Complete Cycle	Acquire and Convert			10			*	μs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±0.9			±0.45	LSB[1]
Differential Linearity Error				±0.9			±0.45	LSB
No Missing Codes			Guaranteed			*		LSB
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10			*	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2			±2		ppm/°C
Unipolar Zero Error[3]	Unipolar Ranges			±3			*	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			*		ppm/°C
Recovery to Rated Accuracy after Power Down	1μF Capacitor to CAP		1			*		ms
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$)	$+4.75V < V_D < +5.25V$			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 45kHz$	80	90		*	*		dB[5]
Total Harmonic Distortion	$f_{IN} = 45kHz$		−90	−80		*	*	dB
Signal-to-(Noise+Distortion)	$f_{IN} = 45kHz$	70	73		72	*		dB
Signal-to-Noise	$f_{IN} = 45kHz$	70	73		72	*		dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		ns
Transient Response	FS Step			2			*	μs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		μA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	μA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	$V_{IL} = 0V$			±10			*	μA
I_{IH}	$V_{IH} = 5V$			±10			*	μA

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808P/U MIN	TYP	MAX	ADS7808PB/UB MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS								
Data Format			Serial 12-bits					
Data Coding			Binary Two's Complement or Straight Binary					
Pipeline Delay			Conversion results only available after completed conversion.					
Data Clock			Selectable for internal or external data clock					
Internal	$\overline{EXT/INT}$ LOW		2.3			*		MHz
(Output Only When Transmitting Data)								
External	$\overline{EXT/INT}$ HIGH	0.1		10	*		*	MHz
(Can Run Continually)								
V_{OL}	$I_{SINK} = 1.6mA$			+0.4			*	V
V_{OH}	$I_{SOURCE} = 500\mu A$	+4			*			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{ANA}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation: PWRD LOW	$V_{DIG} = V_{ANA} = 5V$, $f_S = 100kHz$			100			*	mW
PWRD HIGH			50			*		µW
TEMPERATURE RANGE								
Specified Performance		−40		+85	*		*	°C
Derated Performance		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°CW

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of −Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to (Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

```
Analog Inputs: R1_IN ........................................................ ±25V
               R2_IN ........................................................ ±25V
               R3_IN ........................................................ ±25V
               CAP ....................................... V_ANA+0.3V to AGND2 −0.3V
               REF ....................................... Indefinite Short to AGND2,
                                                          Momentary Short to V_ANA
Ground Voltage Differences: DGND, AGND2 ................................ ±0.3V
V_ANA ............................................................................. 7V
V_DIG to V_ANA .............................................................. +0.3
V_DIG ............................................................................. 7V
Digital Inputs ................................................. −0.3V to V_DIG +0.3V
Maximum Junction Temperature ..................................... +165°C
Internal Power Dissipation ......................................... 700mW
Lead Temperature (soldering, 10s) ............................... +300°C
```

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7808P	20-Pin Plastic DIP	222
ADS7808PB	20-Pin Plastic DIP	222
ADS7808U	20-Pin SOIC	221
ADS7808UB	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ODERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO- (NOISE + DISTORTION) RATIO(dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7808P	±0.9	70	−40°C to +85°C	20-Pin Plastic DIP
ADS7808PB	±0.45	72	−40°C to +85°C	20-Pin Plastic DIP
ADS7808U	±0.9	70	−40°C to +85°C	20-Pin SOIC
ADS7808UB	±0.45	72	−40°C to +85°C	20-Pin SOIC

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R1$_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	R2$_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
4	R3$_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2µF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 12 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 12 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 12-bits of data, the ADS7808 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3.) If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 12 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3.
15	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{CS}$	Chip Select. Internally OR'ed with R/$\overline{C}$.
17	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V$_{ANA}$	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
20	V$_{DIG}$	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V$_{ANA}$.

PIN CONFIGURATION

R1$_{IN}$	1		20	V$_{DIG}$
AGND1	2		19	V$_{ANA}$
R2$_{IN}$	3		18	PWRD
R3$_{IN}$	4		17	$\overline{BUSY}$
CAP	5	ADS7808	16	$\overline{CS}$
REF	6		15	R/$\overline{C}$
AGND2	7		14	TAG
SB/$\overline{BTC}$	8		13	DATA
EXT/$\overline{INT}$	9		12	DATACLK
DGND	10		11	SYNC

ANALOG INPUT RANGE	CONNECT R1$_{IN}$ VIA 200Ω TO	CONNECT R2$_{IN}$ VIA 100Ω TO	CONNECT R3$_{IN}$ TO	IMPEDANCE
±10V	V$_{IN}$	AGND	CAP	22.9kΩ
±5V	AGND	V$_{IN}$	CAP	13.3kΩ
±3.33	V$_{IN}$	V$_{IN}$	CAP	10.7kΩ
0V to 10V	AGND	V$_{IN}$	AGND	13.3kΩ
0V to 5V	AGND	AGND	V$_{IN}$	10.0kΩ
0V to 4V	V$_{IN}$	AGND	V$_{IN}$	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		4500	ns
t_2	$\overline{\text{BUSY}}$ Delay			65	ns
t_3	$\overline{\text{BUSY}}$ LOW			8	µs
t_4	$\overline{\text{BUSY}}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		5.7	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	R/$\overline{\text{C}}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK Period	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20		$t_{12} + 5$	ns
t_{16}	R/$\overline{\text{C}}$ to $\overline{\text{CS}}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15		35	ns
t_{18}	Data Valid Delay	25		55	ns
t_{19}	$\overline{\text{CS}}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{\text{CS}}$ LOW	4.5			µs

TABLE II. Conversion and Data Timing $T_A = -40°C$ to $+85°C$.

FIGURE 1. Basic Conversion Timing.

FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{\text{CS}}$, EXT/$\overline{\text{INT}}$ and TAG Tied LOW.)

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses ouput on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to externa DATACLK .[1] Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

Table III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS – 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	–2.44mV	–1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table IV. Output Codes and Ideal Input Voltages.

FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/$\overline{\text{INT}}$ Tied HIGH). Read After Conversion.

A/D CONVERTERS, DATA ACQUISITION COMPONENTS ADS7808

FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied HIGH.) Read During Conversion (Previous Conversion Results).

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Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

Burr-Brown IC Data Book—Data Conversion Products

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ADS7809

**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

16-Bit 10μs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

● **100kHz SAMPLING RATE**
● **86dB SINAD WITH 45kHz INPUT**
● **±1.5 LSB INL**
● **DNL: 16-Bits "No Missing Codes"**
● **SIX SPECIFIED INPUT RANGES**
● **SERIAL OUTPUT**
● **SINGLE +5V SUPPLY OPERATION**
● **PIN-COMPATIBLE WITH 12-BIT ADS7808**
● **USES INTERNAL OR EXTERNAL REFERENCE**
● **100mW MAX POWER DISSIPATION**
● **20-PIN 0.3" PLASTIC DIP AND SOIC**
● **SIMPLE DSP INTERFACE**

DESCRIPTION

The ADS7809 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7809 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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SPECIFICATIONS

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809P/U MIN	ADS7809P/U TYP	ADS7809P/U MAX	ADS7809PB/UB MIN	ADS7809PB/UB TYP	ADS7809PB/UB MAX	UNITS
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0V to 5V, etc. (See Table I)				
Impedance				See Table I				
Capacitance			35				*	pF
THROUGHPUT SPEED								
Conversion Time			7.6	8		*	*	µs
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, −2			+1.5, −1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10			*	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2			*		ppm/°C
Unipolar Zero Error[3]	Unipolar Ranges			±3			*	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			*		ppm/°C
Recovery to Rated Accuracy after Power Down	1µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 45kHz$	90	100		96	*		dB[5]
Total Harmonic Distortion	$f_{IN} = 45kHz$		−100	−90		*	−96	dB
Signal-to-(Noise+Distortion)	$f_{IN} = 45kHz$	83	88		86	*		dB
	−60dB Input		30			32		dB
Signal-to-Noise	$f_{IN} = 45kHz$	83	88		86	*		dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1		*	*		µA
External Reference Voltage Range For Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	$V_{IL} = 0V$			±10			*	µA
I_{IH}	$V_{IH} = 5V$			±10			*	µA

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = -40°C$ to $+85°C$, $f_S = 100kHz$, $V_{DIG} = V_{ANA} = +5V$, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809P/U MIN	TYP	MAX	ADS7809PB/UB MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS								
Data Format				Serial 16-bits				
Data Coding			Binary Two's Complement or Straight Binary					
Pipeline Delay			Conversion results only available after completed conversion.					
Data Clock			Selectable for internal or external data clock					
Internal	EXT/INT LOW		2.3			*		MHz
(Output Only When Transmitting Data)								
External	EXT/INT HIGH	0.1		10	*		*	MHz
(Can Run Continually)								
V_{OL}	$I_{SINK} = 1.6mA$			+0.4			*	V
V_{OH}	$I_{SOURCE} = 500\mu A$	+4			*		*	V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be $\leq V_{ANA}$	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation: PWRD LOW	$V_{ANA} = V_{DIG} = 5V$, $f_S = 100kHz$		100				*	mW
PWRD HIGH			50			*		µW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	°C
Derated Performance		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of −Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

```
Analog Inputs: R1_IN ........................................... ±25V
               R2_IN ........................................... ±25V
               R3_IN ........................................... ±25V
               CAP ................... V_ANA+0.3V to AGND2 −0.3V
               REF .......................... Indefinite Short to AGND2,
                                              Momentary Short to V_ANA
Ground Voltage Differences: DGND, AGND2 ................. ±0.3V
V_ANA ................................................................. 7V
V_DIG to V_ANA ............................................... +0.3
V_DIG ................................................................ 7V
Digital Inputs ............................... −0.3V to V_DIG +0.3V
Maximum Junction Temperature .............................. +165°C
Internal Power Dissipation ................................ 700mW
Lead Temperature (soldering, 10s) .......................... +300°C
```

⚡ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7809P	20-Pin Plastic DIP	222
ADS7809PB	20-Pin Plastic DIP	222
ADS7809U	20-Pin SOIC	221
ADS7809UB	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	GUARANTEED NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO- (NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7809P	±3	15	83	−40°C to +85°C	20-Pin Plastic DIP
ADS7809PB	±1.5	16	86	−40°C to +85°C	20-Pin Plastic DIP
ADS7809U	±3	15	83	−40°C to +85°C	20-Pin SOIC
ADS7809UB	±1.5	16	86	−40°C to +85°C	20-Pin SOIC

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R1$_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	R2$_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
4	R3$_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2µF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16-bits of data, the ADS7809 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3.) If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3.
15	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{CS}$	Chip Select. Internally OR'ed with R/$\overline{C}$.
17	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. CS or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V$_{ANA}$	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
20	V$_{DIG}$	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V$_{ANA}$.

PIN CONFIGURATION

		ADS7809		
R1$_{IN}$	1		20	V$_{DIG}$
AGND1	2		19	V$_{ANA}$
R2$_{IN}$	3		18	PWRD
R3$_{IN}$	4		17	$\overline{BUSY}$
CAP	5		16	$\overline{CS}$
REF	6		15	R/$\overline{C}$
AGND2	7		14	TAG
SB/$\overline{BTC}$	8		13	DATA
EXT/$\overline{INT}$	9		12	DATACLK
DGND	10		11	SYNC

ANALOG INPUT RANGE	CONNECT R1$_{IN}$ VIA 200Ω TO	CONNECT R2$_{IN}$ VIA 100Ω TO	CONNECT R3$_{IN}$ TO	IMPEDANCE
±10V	V$_{IN}$	AGND	CAP	22.9kΩ
±5V	AGND	V$_{IN}$	CAP	13.3kΩ
±3.33V	V$_{IN}$	V$_{IN}$	CAP	10.7kΩ
0V to 10V	AGND	V$_{IN}$	AGND	13.3kΩ
0V to 5V	AGND	AGND	V$_{IN}$	10.0kΩ
0V to 4V	V$_{IN}$	AGND	V$_{IN}$	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		6000	ns
t_2	$\overline{BUSY}$ Delay			65	ns
t_3	$\overline{BUSY}$ LOW			8	μs
t_4	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		7.6	8	μs
t_7	Acquisition Time			2	μs
$t_6 + t_7$	Throughput Time		9	10	μs
t_8	R/$\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20		t_{12} +5	ns
t_{16}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15		35	ns
t_{18}	Data Valid Delay	25		55	ns
t_{19}	$\overline{CS}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{CS}$ LOW	6			μs

TABLE II. Conversion and Data Timing. T_A = –40°C to +85°C.

FIGURE 1. Basic Conversion Timing.

FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{CS}$, EXT/$\overline{INT}$ and TAG Tied LOW.)

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFIC FUNCTION	C̄S̄	R/C̄	BUSY	EXT/INT	DATACLK	PWRD	SB/BTC	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 16 clock pulses ouput on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	C̄S̄ or R/C̄ must be HIGH or a new conversion will be initiated without time for acquisition.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

Table III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/B̄T̄C̄ LOW)		STRAIGHT BINARY (SB/B̄T̄C̄ HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305µV	153µV	102µV	153µV	76µV	61µV				
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

Table IV. Output Codes and Ideal Input Voltages.

FIGURE3a. Conversion and Read Timing with External Clock. (EXT/$\overline{\text{INT}}$ Tied HIGH.) Read After Conversion.

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FIGURE3b. Conversion and Read Timing with External Clock. (EXT/$\overline{\text{INT}}$ Tied HIGH.) Read During Conversion (Previous Conversion Results).

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FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

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**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

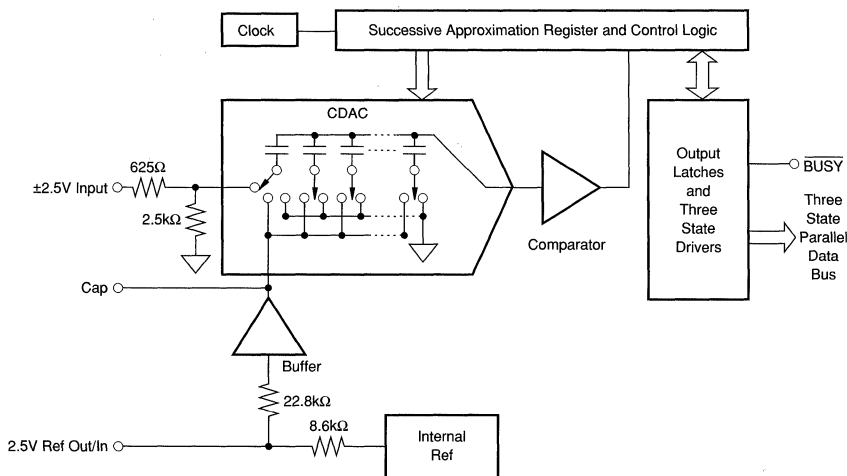# 12-Bit 800kHz Sampling CMOS
ANALOG-to-DIGITAL CONVERTER

FEATURES

- **1.25μs THROUGHPUT TIME**
- **STANDARD ±10V INPUT RANGE**
- **69dB min SINAD WITH 250kHz INPUT**
- **±3/4 LSB max INL AND ±1 LSB max DNL**
- **INTERNAL REFERENCE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **PARALLEL DATA w/LATCHES**
- **250mW max POWER DISSIPATION**
- **28-PIN 0.3" PDIP AND SOIC**

DESCRIPTION

The ADS7810 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7810 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide the industry-standard ±10V input range, while an innovative design allows operation from ±5V supplies, with power dissipation under 250mW.

The 28-pin ADS7810 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C, to +85°C, f_S = 800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $–V_{ANA}$ = –5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7810P, U MIN	ADS7810P, U TYP	ADS7810P, U MAX	ADS7810PB, UB MIN	ADS7810PB, UB TYP	ADS7810PB, UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±10				*	V
Impedance			3.1				*	kΩ
Capacitance			5				*	pF
THROUGHPUT SPEED								
Conversion Time			985				*	ns
Complete Cycle	Acquire & Convert			1240			*	ns
Throughput Rate		800			*			kHz
DC ACCURACY								
Integral Linearity Error				±1			±0.75	LSB[1]
Differential Linearity Error				±1			±1	LSB
No Missing Codes			Guaranteed			*		
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3, 4]				±0.5			±0.25	%
Full Scale Error Drift			±5			±3		ppm/°C
Full Scale Error[3, 4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2				*	ppm/°C
Bipolar Zero Error[3]				±8			±4	LSB
Bipolar Zero Error Drift			±1			±0.5		ppm/°C
Power Supply Sensitivity								
($+V_{DIG}$ = $+V_{ANA}$ = V_D)	+4.75V < V_D < +5.25V			±5			*	LSB
	–5.25V < $–V_{ANA}$ < –4.75V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 250kHz	74			77			dB[5]
Total Harmonic Distortion	f_{IN} = 250kHz			–74			–77	dB
Signal-to-(Noise+Distortion)	f_{IN} = 250kHz	67			69			dB
Signal-to-Noise	f_{IN} = 250kHz	68			70			dB
Full-Power Bandwidth[6]			1.5			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			20			*		ns
Aperture Jitter		Sufficient to Meet AC Specs			*			
Transient Response	FS Step		100			*		ns
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			100			*		nA
(Must use external buffer)								
Internal Reference Drift			8					ppm/°C
External Reference Voltage Range		2.3	2.5	2.7	*	*	*	V
For Specified Linearity								
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		V_D + 0.3	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS								
Data Format			Parallel 12-bits					
Data Coding			Binary Two's Complement					
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+2.8			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

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SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C, to +85°C, f_S = 800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $–V_{ANA}$ = –5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7810P, U			ADS7810PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
$+V_{DIG}$ = $+V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$–V_{ANA}$		–5.25	–5	–4.75	*	*	*	V
$+I_{DIG}$			+16			*		mA
$+I_{ANA}$			+16			*		mA
$–I_{ANA}$			–13			*		mA
Derated Performance								
$+V_{DIG}$ = $+V_{ANA}$		+4.5	+5	+5.5	*	*	*	V
$–V_{ANA}$		–5.5	–5	–4.5	*	*	*	V
Power Dissipation	f_S = 800kHz			250			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125				°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7810, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} .... ±25V
    CAP .... $+V_{ANA}$ +0.3V to AGND2 –0.3V
    REF .... Indefinite Short to AGND2
                                     Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2 .... ±0.3V
$+V_{ANA}$ .... +7V
$+V_{DIG}$ to $+V_{ANA}$ .... +0.3V
$+V_{DIG}$ 7V
$–V_{ANA}$ .... –7V
Digital Inputs .... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature .... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) .... +300°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION(1)

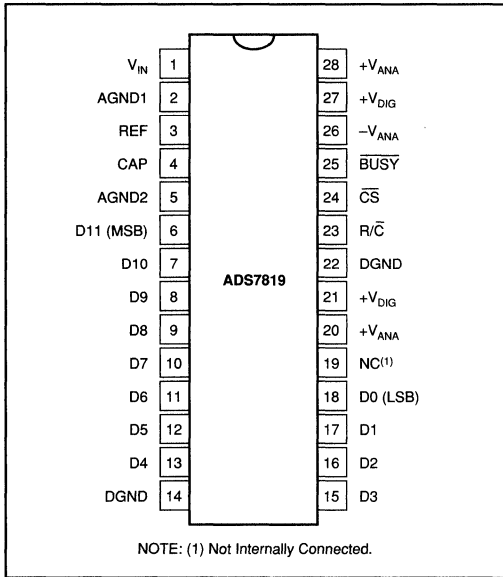| MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7810P	28-Pin Plastic DIP	246
ADS7810PB	28-Pin Plastic DIP	246
ADS7810U	28-Pin SOIC	217
ADS7810UB	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7810P	±1	67	–40°C to +85°C	Plastic DIP
ADS7810PB	±0.75	69	–40°C to +85°C	Plastic DIP
ADS7810U	±1	67	–40°C to +85°C	SOIC
ADS7810UB	±0.75	69	–40°C to +85°C	SOIC

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN CONFIGURATION

V_IN	1	28	+V_ANA
AGND1	2	27	+V_DIG
REF	3	26	−V_ANA
CAP	4	25	$\overline{BUSY}$
AGND2	5	24	$\overline{CS}$
D11 (MSB)	6	23	R/$\overline{C}$
D10	7	22	DGND
D9	8	21	+V_DIG
D8	9	20	+V_ANA
D7	10	19	NC(1)
D6	11	18	D0 (LSB)
D5	12	17	D1
D4	13	16	D2
DGND	14	15	D3

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NOTE: (1) Not Internally Connected.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	Data Valid Delay After R/$\overline{C}$ LOW		1030	1150	ns
t_3	$\overline{BUSY}$ Delay From R/$\overline{C}$ LOW		85	125	ns
t_4	$\overline{BUSY}$ LOW		1000	1115	ns
t_5	$\overline{BUSY}$ Delay After End of Conversion		80		ns
t_6	Aperture Delay		20		ns
t_7	Conversion Time		985	1090	ns
t_8	Acquisition Time		100	150	ns
t_7 & t_8	Throughput Time		1085	1240	ns
t_9	Bus Relinquish Time	20	50	83	ns
t_{10}	$\overline{BUSY}$ Delay After Data Valid	20	55	90	ns
t_{11}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	5			ns
t_{12}	Time Between Conversions	1250			ns
t_{13}	Bus Access Time	10	35	83	ns

TABLE I. Timing Specifications (T_{MIN} to T_{MAX}).

PIN ASSIGNMENTS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_IN		Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±10V.
2	AGND1		Analog Ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum to ground.
5	AGND2		Analog Ground.
6	D11 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
7	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
8	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
9	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
10	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
11	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
12	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
13	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
14	DGND		Digital Ground.
15	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
16	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
17	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
18	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
19			Not internally connected.
20	+V_ANA		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
21	+V_DIG		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28.
22	DGND		Digital ground.
23	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits.
24	$\overline{CS}$	I	Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits.
25	$\overline{BUSY}$	O	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to read the data.
26	−V_ANA		Analog Negative Supply Input. Nominally −5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
27	+V_DIG		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28.
28	+V_ANA		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27.

BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7810 with a full parallel data output. Taking R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7810 in the hold state and starts a conversion. BUSY (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 3 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	BUSY	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus enabled when conversion is completed.
0	↑	0	Conversion in progress. Databus enabled when conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register, but outputs are still tri-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table II. Control Line Functions for 'read' and 'convert'.

		DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
DESCRIPTION	ANALOG INPUT	BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	4.88mV		
+Full Scale (10V – 1LSB)	9.995V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–4.88mV	1111 1111 1111	FFF
–Full Scale	–10V	1000 0000 0000	800

TABLE III. Ideal Input Voltages and Output Codes.

FIGURE 1. Basic Operation

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 5ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the Reading Data section and refer to Table II for control line functions for 'read' and 'convert' modes.

READING DATA

The ADS7810 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on pins 6-13 and pins 15-18. Refer to Table III for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table I and Figures 2 and 3.

Note! For the best possible performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

INPUT RANGES

The ADS7810 offers a standard ±10V input range. Figure 4 shows the necessary circuit connections for the ADS7810 with and without external trim. Offset and full scale error[1] specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4. This external resistor makes it possible to trim the offset ±50mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain are negligible or they will be trimmed in software. See the Calibration section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and external 50Ω resistor. The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor used for the external offset adjustment circuitry does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

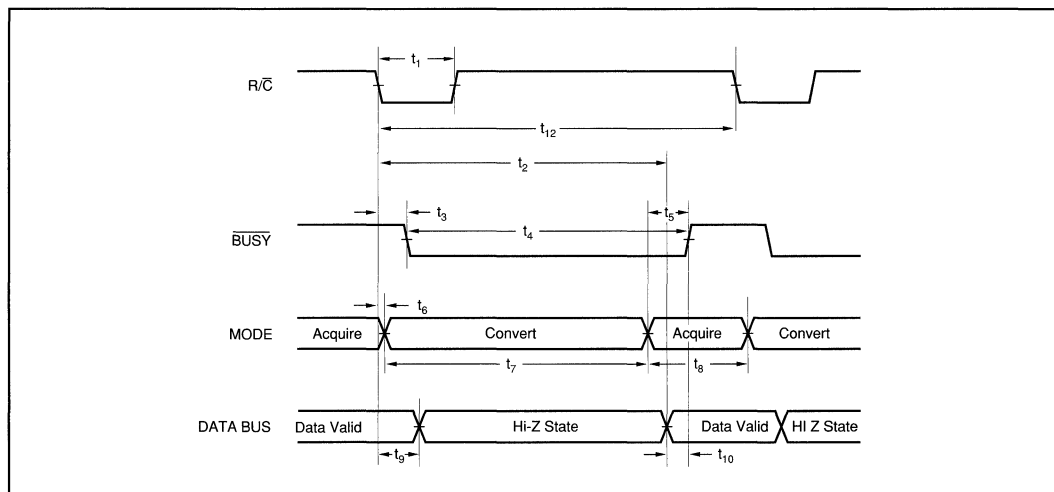NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

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FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

±10V With Hardware Trim	±10V Without Hardware Trim
NOTE: Use 1% metal film resistors. Trim offset at 0V first, then trim gain at 10V.	

FIGURE 4. Circuit Diagram With and Without External Resistors.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

CALIBRATION

The ADS7810 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

Hardware Calibration

To calibrate the offset and gain of the ADS7810, install the proper resistors and potentiometers as shown in Figure 4. The calibration range is ±50mV for the offset and ±135mV for the gain.

Software Calibration

To calibrate the offset and gain of the ADS7810, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistor. Refer to Table IV for range of gain errors with and without external 50Ω resistor.

No Calibration

See Figure 4 for circuit connections. The 50Ω external resistor shown in Figure 4 may not be necessary in some applications. This resistor provides trim capability for the gain of the ADS7810. The nominal transfer function of the ADS7810 will be bound by the shaded region seen in Figure 5 with a typical offset of 0mV and a typical gain error of –1.6%. Refer to Table IV for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPO	–40 < BPO < 40	–40 < BPO < 40	mV
	–8 < BPO < 8	–8 < BPO < 8	LSBs
Gain Error	–0.5 < error < 0.5	–2.5 < error < –1	% of FSR

TABLE IV. Offset and Gain Errors With and Without External Resistors.

REFERENCE

The ADS7810 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output of the buffer accessible on CAP (pin 4).

The internal reference has a 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 0.1μF capacitor should be connected as close to the REF pin as possible. The capacitor
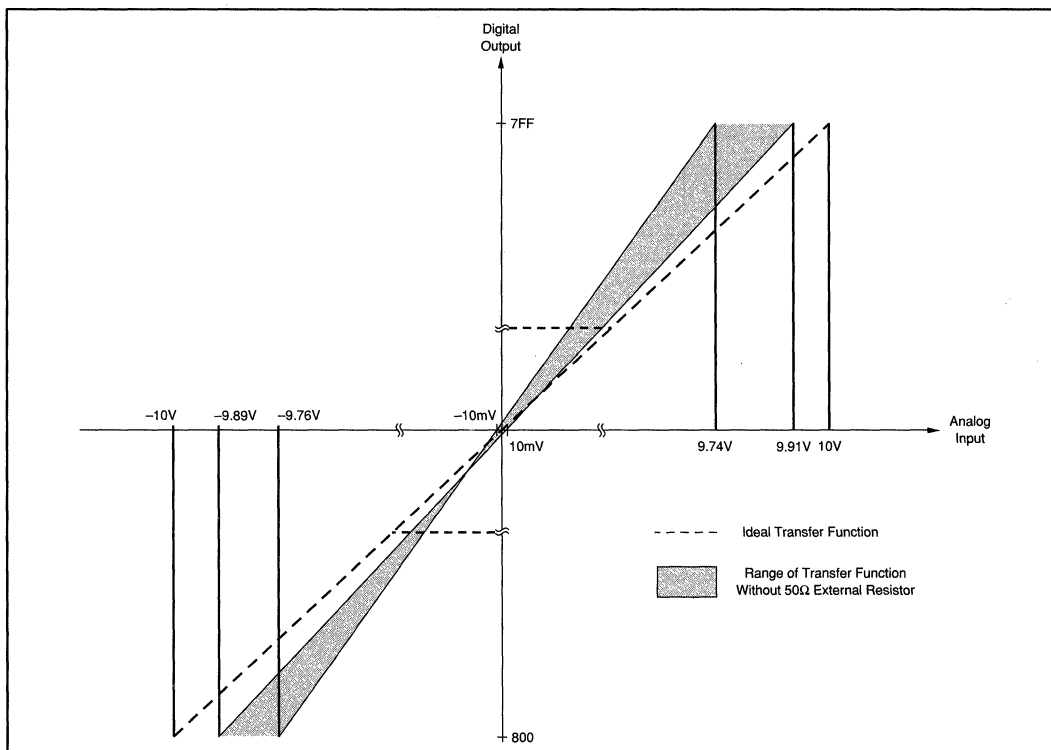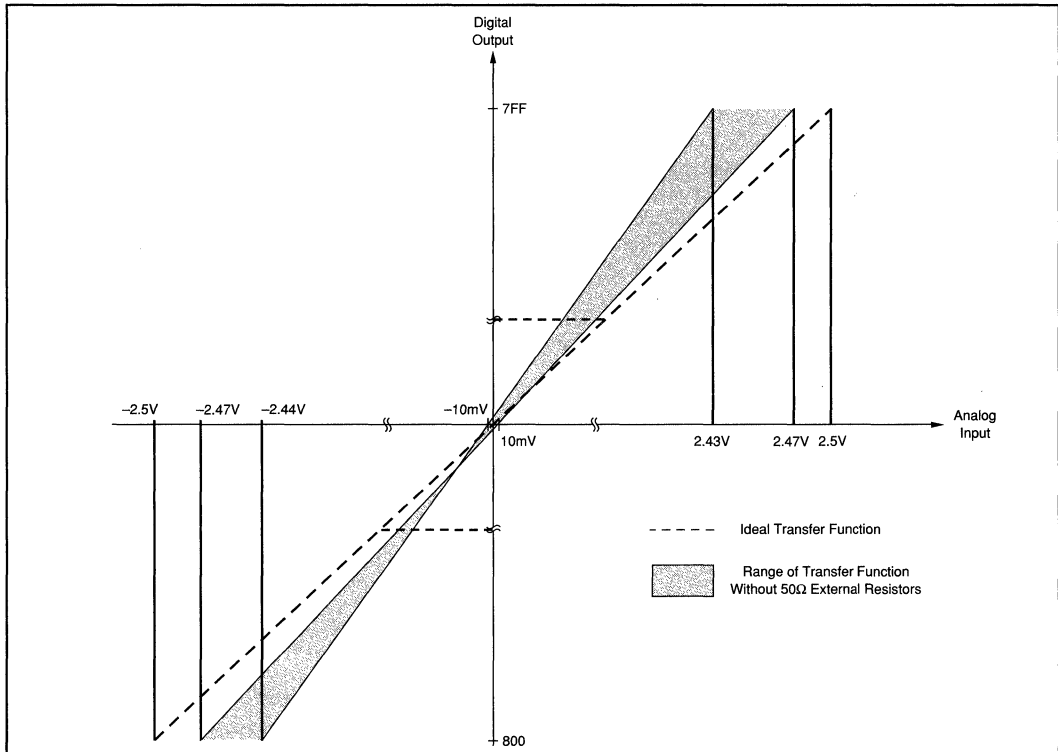

FIGURE 5. Bipolar Transfer Function Without External Resistors.

and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. The ADS7810 uses the majority of its power for analog and static circuitry. The ADS7810 should be considered as an analog component.

The +5V power for the ADS should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 21 and 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, simple +5V and –5V regulators can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, the V_{DIG} and V_{ANA} pins should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7810. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground, as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7810, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7810.

The resistive front end of the ADS7810 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7810 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7810 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

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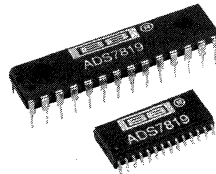
ADS7819

**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

12-Bit 800kHz Sampling CMOS
ANALOG-to-DIGITAL CONVERTER

FEATURES

- **1.25µs THROUGHPUT TIME**
- **STANDARD ±2.5V INPUT RANGE**
- **69dB min SINAD WITH 250kHz INPUT**
- **±3/4 LSB max INL AND ±1 LSB max DNL**
- **INTERNAL REFERENCE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **PARALLEL DATA w/LATCHES**
- **250mW max POWER DISSIPATION**
- **28-PIN 0.3" PDIP AND SOIC**

DESCRIPTION

The ADS7819 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7819 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a ±2.5V input range, while an innovative design allows operation from ±5V supplies, with power dissipation under 250mW.

The 28-pin ADS7819 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

PDS-1193B

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SPECIFICATIONS

ELECTRICAL

At $T_A = -40°C$, to $+85°C$, $f_S = 800kHz$, $+V_{DIG} = +V_{ANA} = +5V$, $-V_{ANA} = -5V$, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7819P, U MIN	ADS7819P, U TYP	ADS7819P, U MAX	ADS7819PB, UB MIN	ADS7819PB, UB TYP	ADS7819PB, UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±2.5			*		V
Impedance			3.1			*		kΩ
Capacitance			5			*		pF
THROUGHPUT SPEED								
Conversion Time			985			*		ns
Complete Cycle	Acquire & Convert			1240			*	ns
Throughput Rate		800			*			kHz
DC ACCURACY								
Integral Linearity Error				±1			±0.75	LSB[1]
Differential Linearity Error				±1			±1	LSB
No Missing Codes			Guaranteed		*			LSB
Transition Noise[2]			0.1		*			LSB
Full Scale Error[3, 4]				±0.5			±0.25	%
Full Scale Error Drift			±5			±3		ppm/°C
Full Scale Error[3, 4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±8			±4	LSB
Bipolar Zero Error Drift			±1			±0.5		ppm/°C
Power Supply Sensitivity								
($+V_{DIG} = +V_{ANA} = V_D$)	$+4.75V < V_D < +5.25V$			±5			*	LSB
	$-5.25V < -V_{ANA} < -4.75V$			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	$f_{IN} = 250kHz$	74			77			dB[5]
Total Harmonic Distortion	$f_{IN} = 250kHz$			−74			−77	dB
Signal-to-(Noise+Distortion)	$f_{IN} = 250kHz$	67			69			dB
Signal-to-Noise	$f_{IN} = 250kHz$	68			70			dB
Full-Power Bandwidth[6]			1.5			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			20			*		ns
Aperture Jitter		Sufficient to Meet AC Specs			*			
Transient Response	FS Step		100			*		ns
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			100		*			nA
(Must use external buffer)								
Internal Reference Drift			8					ppm/°C
External Reference Voltage Range		2.3	2.5	2.7	*	*	*	V
For Specified Linearity								
External Reference Current Drain	Ext. 2.5000V Ref			100			*	μA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		−0.3		+0.8	*		*	V
V_{IH}		+2.4		$V_D + 0.3$	*		*	V
I_{IL}	$V_{IL} = 0V$			±10			*	μA
I_{IH}	$V_{IH} = 5V$			±10			*	μA
DIGITAL OUTPUTS								
Data Format			Parallel 12-bits					
Data Coding			Binary Two's Complement					
V_{OL}	$I_{SINK} = 1.6mA$			+0.4			*	V
V_{OH}	$I_{SOURCE} = 500μA$	+2.8			*		*	V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_{DIG}			±5			*	μA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = -40°C$, to $+85°C$, $f_S = 800kHz$, $+V_{DIG} = +V_{ANA} = +5V$, $-V_{ANA} = -5V$, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7819P, U			ADS7819PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
$+V_{DIG} = +V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$-V_{ANA}$		-5.25	-5	-4.75	*	*	*	V
$+I_{DIG}$			+16				*	mA
$+I_{ANA}$			+16				*	mA
$-I_{ANA}$			-13				*	mA
Derated Performance								
$+V_{DIG} = +V_{ANA}$		+4.5	+5	+5.5	*	*	*	V
$-V_{ANA}$		-5.5	-5	-4.5	*	*	*	V
Power Dissipation	$f_S = 800kHz$			250			*	mW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	°C
Derated Performance		-55		+125				°C
Storage		-65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±2.5V input ADS7819, one LSB is 1.22mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±2.5V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	±25V
CAP	$+V_{ANA}$ +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2
	Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
$+V_{ANA}$	+7V
$+V_{DIG}$ to $+V_{ANA}$	+0.3V
$+V_{DIG}$	7V
$-V_{ANA}$	–7V
Digital Inputs	–0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7819P	28-Pin Plastic DIP	246
ADS7819PB	28-Pin Plastic DIP	246
ADS7819U	28-Pin SOIC	217
ADS7819UB	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7819P	±1	67	–40°C to +85°C	Plastic DIP
ADS7819PB	±0.75	69	–40°C to +85°C	Plastic DIP
ADS7819U	±1	67	–40°C to +85°C	SOIC
ADS7819UB	±0.75	69	–40°C to +85°C	SOIC

PIN CONFIGURATION


```
        V_IN    1          28   +V_ANA
       AGND1    2          27   +V_DIG
         REF    3          26   -V_ANA
         CAP    4          25   BUSY
       AGND2    5          24   CS
    D11 (MSB)   6          23   R/C
         D10    7    ADS7819  22   DGND
          D9    8          21   +V_DIG
          D8    9          20   +V_ANA
          D7   10          19   NC(1)
          D6   11          18   D0 (LSB)
          D5   12          17   D1
          D4   13          16   D2
        DGND   14          15   D3
```

NOTE: (1) Not Internally Connected.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	Data Valid Delay After R/C LOW		1030	1150	ns
t_3	BUSY Delay From R/C LOW		85	125	ns
t_4	BUSY LOW		1000	1115	ns
t_5	BUSY Delay After End of Conversion		80		ns
t_6	Aperture Delay		20		ns
t_7	Conversion Time		985	1090	ns
t_8	Acquisition Time		100	150	ns
t_7 & t_8	Throughput Time		1085	1240	ns
t_9	Bus Relinquish Time	20	50	83	ns
t_{10}	BUSY Delay After Data Valid	20	55	90	ns
t_{11}	R/C to CS Setup Time	5			ns
t_{12}	Time Between Conversions	1250			ns
t_{13}	Bus Access Time	10	35	83	ns

TABLE I. Timing Specifications (T_{MIN} to T_{MAX}).

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN ASSIGNMENTS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_IN		Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V.
2	AGND1		Analog Ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1μF ceramic capacitor.
4	CAP		Reference Buffer Capacitor. 2.2μF tantalum to ground.
5	AGND2		Analog Ground.
6	D11 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
7	D10	O	Data Bit 10. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
8	D9	O	Data Bit 9. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
9	D8	O	Data Bit 8. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
10	D7	O	Data Bit 7. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
11	D6	O	Data Bit 6. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
12	D5	O	Data Bit 5. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
13	D4	O	Data Bit 4. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
14	DGND		Digital Ground.
15	D3	O	Data Bit 3. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
16	D2	O	Data Bit 2. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
17	D1	O	Data Bit 1. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
18	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when CS is HIGH, or when R/C is LOW, or when a conversion is in progress.
19			Not internally connected.
20	+V_ANA		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28, and decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.
21	+V_DIG		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28.
22	DGND		Digital ground.
23	R/C	I	Read/Convert Input. With CS LOW, a falling edge on R/C puts the internal sample/hold into the hold state and starts a conversion. With CS LOW and no conversion in progress, a rising edge on R/C enables the output data bits.
24	CS	I	Chip Select. Internally OR'd with R/C. With R/C LOW, a falling edge on CS will initiate a conversion. With R/C HIGH and no conversion in progress, a falling edge on CS will enable the output data bits.
25	BUSY	O	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With CS LOW and R/C HIGH, output data will be valid when BUSY rises, so that the rising edge can be used to read the data.
26	-V_ANA		Analog Negative Supply Input. Nominally -5V. Decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.
27	+V_DIG		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28.
28	+V_ANA		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27.

BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7819 with a full parallel data output. Taking R/C̄ (pin 23) LOW for 40ns will initiate a conversion. BUSY (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. BUSY going HIGH can be used to latch the data. All convert commands will be ignored while BUSY is LOW.

C̄S̄	R/C̄	BUSY	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus enabled when the conversion is completed.
0	↑	0	Conversion in progress. Databus enabled when the conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register, but outputs are still tri-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table II. Control Line Functions for 'read' and 'convert'.

The ADS7819 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of C̄S̄ (pin 24) and R/C̄ (pin 23) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7819 in the hold state and starts a conversion. BUSY (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during BUSY LOW will be ignored.

The ADS7819 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of C̄S̄, R/C̄, and BUSY states and Figures 2 and 3 for timing parameters.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Range	±2.5V		
Least Significant Bit (LSB)	1.22mV		
+Full Scale (10V − 1LSB)	2.499V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	−1.22mV	1111 1111 1111	FFF
−Full Scale	−2.5V	1000 0000 0000	800

TABLE III. Ideal Input Voltages and Output Codes.

FIGURE 1. Basic Operation

CS and R/C are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that CS or R/C initiate the conversion, be sure the less critical input is LOW at least 5ns prior to the initiating input.

To reduce the number of control pins, CS can be tied LOW using R/C to control the read and convert modes. Note that the parallel output will be active whenever R/C is HIGH and no conversion is in progress. See the Reading Data section and refer to Table II for control line functions for 'read' and 'convert' modes.

READING DATA

The ADS7819 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when R/C (pin 23) is HIGH, and CS (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on pins 6-13 and pins 15-18. Refer to Table III for ideal output codes.

After the conversion is completed and the output registers have been updated, BUSY (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). BUSY going HIGH can be used to latch the data. Refer to Table I and Figures 2 and 3.

Note! For the best possible performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feed through degrading the converter's performance.

The number of control lines can be reduced by tieing CS LOW while using R/C to initiate conversions and activate the output mode of the converter. See Figure 2.

INPUT RANGES

The ADS7819 offers a ±2.5V input range. Figure 4 shows the necessary circuit connections for the ADS7819 with and without external trim. Offset and full scale error[1] specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4. This external resistor makes it possible to trim the offset ±13mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain are negligible or they will be trimmed in software. See the Calibration section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and external 50Ω resistor. The input resistor divider network provides inherent over-voltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor used for the external offset adjustment circuitry does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

FIGURE 2. Conversion Timing with Outputs Enabled After Conversion (CS Tied Low).

FIGURE 3. Using $\overline{\text{CS}}$ to Control Conversion and Read Timing.

FIGURE 4. Circuit Diagram With and Without External Resistors.

CALIBRATION

The ADS7819 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

Hardware Calibration

To calibrate the offset and gain of the ADS7819, install the proper resistors and potentiometers as shown in Figure 4. The calibration range is ±13mV for the offset and ±34mV for the gain.

Software Calibration

To calibrate the offset and gain of the ADS7819, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistor. Refer to Table IV for range of gain errors with and without the external 50Ω resistor.

No Calibration

See Figure 4 for circuit connections. The 50Ω external resistor shown in Figure 4 may not be necessary in some applications. This resistor provides trim capability for the gain of the ADS7819. The nominal transfer function of the ADS7819 will be bound by the shaded region seen in Figure 5 with a typical offset of 0mV and a typical gain error of −1.6%. Refer to Table IV for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPO	−10 < BPO < 10 −8 < BPO < 8	−10 < BPO < 10 −8 < BPO < 8	mV LSBs
Gain Error	−0.5 < error < 0.5	−2.5 < error < −1	% of FSR

TABLE IV. Offset and Gain Errors With and Without External Resistors.

REFERENCE

The ADS7819 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally and output on CAP (pin 4).

The internal reference has a 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 0.1µF capacitor should be connected as close to the REF pin as possible. The capacitor

FIGURE 5. Circuit Diagram With and Without External Resistors.

and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. The ADS7819 uses the majority of its power for analog and static circuitry. The ADS7819 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting VDIG (pin 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7819. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7819, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7819.

The resistive front end of the ADS7819 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7819 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7819 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

BURR - BROWN®

ADS7833

3-Channel Simultaneous Sampling
12-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES
● **3 SIMULTANEOUS SAMPLE/HOLD AND 12-BIT ADCs**
● **10μs THROUGHPUT RATE**
● **FULL DIFFERENTIAL MUX INPUTS**
● **±2.5V INPUT RANGE**
● **±5V POWER SUPPLIES**
● **SERIAL DIGITAL INPUT/OUTPUTS**

APPLICATIONS
● **AC MOTOR SPEED CONTROLS**
● **THREE PHASE POWER CONTROL**
● **UNINTERRUPTED POWER SUPPLIES**

DESCRIPTION
The basic functions of the ADS7833 consist of three 12-bit analog-to-digital converters preceded by three simultaneously operating sample-hold amplifiers. The ADCs have simultaneous serial outputs and are preceded by programmable gain amplifiers each with four gains.

The inputs to each of the three channels are full differential input multiplexers. Two of the channels have three differential inputs and the third channel has four differential inputs.

The desired input selection and gain configuration is determined by a user-supplied serial input control word. The 13-bit input control word for the next conversion is clocked into the input setup register at the same time the ADC serial outputs for the present conversions are clock out.

The part also contains an 8-bit digital-to-analog converter whose digital input is supplied as part of the input control word.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

SPECIFICATIONS

ELECTRICAL

$V_{ANA+} = +5V$, $V_{ANA-} = -5V$, $V_{DIG+} = +5V$, $V_{DIG-} = -5V$, $T_A = +25°C$, using internal reference, $f_{CLOCK} = 1.4MHz$.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

		ADS7833			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESOLUTION		12			Bit
ANALOG INPUT					
Full Scale Voltage, Differential	G = 1.0V/V		±2.5		V
	G = 1.25V/V		±2.0		V
	G = 2.0V/V		±1.25		V
	G = 5.0V/V		±0.5		V
Common Mode Voltage		±0.5	±1.0		V
Impedance			10^{12}		Ω
Capacitance			10		pF
THROUGHPUT SPEED	$f_{CLOCK} = 1.4MHz$				
Conversion Time				9.5	μs
Complete Cycle	Acquire and Convert			10	μs
Throughput Rate		100			kHz
SAMPLING DYNAMICS					
S/H Droop Rate			0.1		μV/μs
S/H Acquisition Time			0.5		μs
S/H Aperture Delay			50		ns
S/H Aperture Jitter			50		ps
Sampling Skew, Channel-to-Channel			3		ns
DC ACCURACY					
Integral Linearity				±0.75	LSB
Differential Linearity				±0.75	LSB
No Missing Codes		12			Bits
Full Scale Error	G = 1.0V/V		±0.05	±0.5	%
	G = 5.0V/V		±0.05	±0.5	%
Full Scale Error Drift	G = 1.0V/V,		±10	±100	ppm/°C
	With Internal Reference				
	G = 5.0V/V,		±10	±100	ppm/°C
Zero Error	With Internal Reference				
	G = 1.0V/V		±0.5	±10	LSB
	G = 5.0V/V		±0.5	±10	LSB
Zero Error Drift	G = 1.0V/V		±0.5	±5	ppm/°C
	G = 5.0V/V		±0.5	±5	ppm°C
AC ACCURACY	$F_{IN} = 1kHz$		92		
Total Harmonic Distortion	$F_{IN} = 1MHz$		72		dB
CMR	$V_{CM} = 1V$, $F_{CM} = 1MHz$		40		dB
REFERENCE					
Internal Reference Voltage			2.5		V
Internal Reference Accuracy			±0.25		%
Internal Reference Drift			±10	±100	ppm/°C
Internal Reference Source Current			10		μA
External Reference Voltage Range		2.25	2.5	2.75	V
for Specified Linearity					
External Reference Current Drain			10		μA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		0		1.5	V
V_{IH}		+3.5		+5	V
I_{IL}				±10	μA
I_{IH}				±10	μA
Input Capacitance	At All Digital Input Pins			15	pF
DIGITAL OUTPUTS					
Data Format			12-Bit Serial		
Data Coding			BTC		
V_{OL}	$I_{SINK} = 1.6mA$	0		0.4	V
V_{OH}	$I_{SOURCE} = 500μA$	4.2		5	V
Leakage Current				±5	μA
Output Capacitance	At All Digital Output Pins			15	pF

SPECIFICATIONS (CONT)

ELECTRICAL

V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, T_A = +25°C, using internal reference, f_{CLOCK} = 1.4MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

| PARAMETER | CONDITIONS | ADS7833 | | | UNITS |
		MIN	TYP	MAX	
POWER SUPPLIES	Specified Performance				
V_{ANA+}		+4.75	+5.0	+5.25	V
V_{ANA-}		–4.75	–5.0	–5.25	V
V_{DIG+}		+4.75	+5.0	+5.25	V
V_{DIG-}		–4.75	–5.0	–5.25	V
I_{ANA+}			15		mA
I_{ANA-}			8		mA
I_{DIG+}			3		mA
I_{DIG-}			1		mA
Power Dissipation				200	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Derated Performance		–55		+125	°C
Storage					
Thermal Resistance					

DIGITAL-TO-ANALOG CONVERTER

| PARAMETER | CONDITIONS | ADS7833 | | | UNITS |
		MIN	TYP	MAX	
RESOLUTION		8-Bits			
Offset Error			±1	±7	mV
Full Scale Error				±1	%

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltages:
  Analog Input Currents .... ±25V
  Ground Voltage Difference: AGND and DGND .... ±0.3V
Power Supply Voltages:
  V_{ANA+} .... +7V
  V_{ANA-} .... –7V
  V_{DIG+} .... +7V
  V_{DIG-} .... –7V
Maximum Junction Temperature .... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) .... +300°C

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN DEFINITIONS

PIN NO	NAME	TYPE(1)	DESCRIPTION	PIN NO	NAME	TYPE(1)	DESCRIPTION
1	V3–4N	OI	Voltage Input, Channel 4,Mux I/P 4, Negative Side	35	S_{OUT1}	DO	Serial Digital Output, Channel 1
				36	CLK	DI	Clock for A/D Converters
2	V3–4P	OI	Voltage Input, Channel 3, Mux IP 4, Positive Side	37	CONV	DI	Start A/D Converters. When CONV goes to "0" (low) the next rising edge of CLK starts the conversion.
3	V3–3N	OI	Voltage Input, Channel 3, Mux I/P 3, Negative Side				
4	V3–3P	OI	Voltage Input, Channel 3, Mux I/P 3, Positive Side	38	ASH	DI	Digital Control for Asynchronous Sample Hold. If signal is "1" (high), signals are sampled.
5	V3–2N	OI	Voltage Input, Channel 3, Mux I/P 2, Negative Side	39	SER_{IN}	DI	Serial Digital Input for Input Control Word
				40	BUSY	DO	A/D Converters Busy. Busy if signal is "0" (low).
6	V3–2P	OI	Voltage Input, Channel 3, Mux I/P 2, Positive Side	41	DCLOCK	DO	A Delayed and Truncated Version of the CLK Signals. It is Delayed 50ns from the CLK Signal and Stays Low after 13 DCLOCK Cycles.
7	NC	—	Make No Connection				
8	V2–1N	OI	Voltage Input, Channel 2, Mux I/P 1, Negative Side				
9	V2–1P	OI	Voltage Input, Channel 2, Mux I/P 1, Positive Side	42	NC	—	Make No Connection
				43	NC	—	Make No Connection
				44	NC	—	Make No Connection
10	NC	—	Make No Connection	45	NC	—	Make No Connection
11	V2–1N	OI	Voltage Input, Channel 2, Mux I/P 1, Negative Side	46	NC	—	Make No Connection
				47	NC	—	Make No Connection
12	V2–1P	OI	Voltage Input, Channel 2, Mux I/P 1, Positive Side	48	NC	—	Make No Connection
				49	NC	—	Make No Connection
13	NC	—	Make No Connection	50	NC	—	Make No Connection
14	V2–2N	OI	Voltage Input, Channel 2, Mux I/P 2, Negative Side	51	NC	—	Make No Connection
				52	V1–3P	OI	Voltage Input, Channel 1, Mux I/P 3, Positive Side
15	V2–2P	OI	Voltage Input, Channel 2, Mux I/P 2, Positive Side	53	V1–3N	OI	Voltage Input, Channel 1, Mux I/P 3, Negative Side
16	NC	—	Make No Connection	54	NC	—	Make No Connection
17	V2–3N	OI	Voltage Input, Channel 2, Mux I/P 3, Negative Side.	55	V1–2P	OI	Voltage Input, Channel 1, Mux I/P 2, Positive Side
18	V2–3P	OI	Voltage Input, Channel 2, Mux I/P 3, Positive Side	56	V1–2N	OI	Voltage Input, Channel 1, Mux I/P 2, Negative Side
19	NC	—	Make No Connection	57	NC	—	Make No Connection
20	NC	—	Make No Connection	58	V1–1P	OI	Voltage Input, Channel 1, Mux I/P 1, Positive Side
21	NC	—	Make No Connection				
22	NC	—	Make No Connection	59	V1–1N	OI	Voltage Input, Channel 1, Mux I/P 1, Negative Side
23	NC	—	Make No Connection				
24	NC	—	Make No Connection				
25	NC	—	Make No Connection	60	NC	—	Make No Connection
26	NC	—	Make No Connection	61	NC	—	Make No Connection
27	TP1	—	Test Point 1, Make No Connection	62	A_{OUT}	AO	Output of DAC
28	TP2	—	Test Point 2, Make No Connection	63	REF_{OUT}	AO	Output Voltage from Internal Reference
29	V_{DIG+}	P	Digital Supply Voltage, +5V	64	REF_{IN}	AI	Input Pin for External Reference
30	DGND	P	Digital Supply Voltage, Ground	65	REF_{GND}	P	Ground Pin for External Reference
31	V_{DIG-}	P	Digital Supply Voltage, –5V	66	V_{ANA-}	P	Analog Supply Voltage, –5V
32	NC	—	Make No Connection	67	AGND	P	Analog Supply Voltage, Ground
33	S_{OUT2}	DO	Serial Digital Output, Channel 2	68	V_{ANA+}	P	Analog Supply Voltage, +5V
34	S_{OUT3}	DO	Serial Digital Output, Channel 3				

NOTE: (1) AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, P is Power Supply Connection.

FUNCTIONAL DESCRIPTION

(See Figure 1)

ADCs AND PGAs

The ADS7833 contains three signal channels each with a 12-bit analog-to-digital converter output. The ADCs operate synchronously and their serial outputs occur simultaneously. (Table VI gives the analog input/digital output relation-ships). The ADCs are preceded by programmable gain amplifiers. (Table II gives gain select information). For channels one and two, the PGAs are effective for all three analog inputs. For the third channel, only the V_{3-1} input is gain changed by the PGA. Inputs V_{3-2}, V_{3-3}, and V_{3-4} are connected to ADC_3 at a fixed gain of 1V/V regardless of the Gain Select value.

FIGURE 1. Functional Diagram.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS
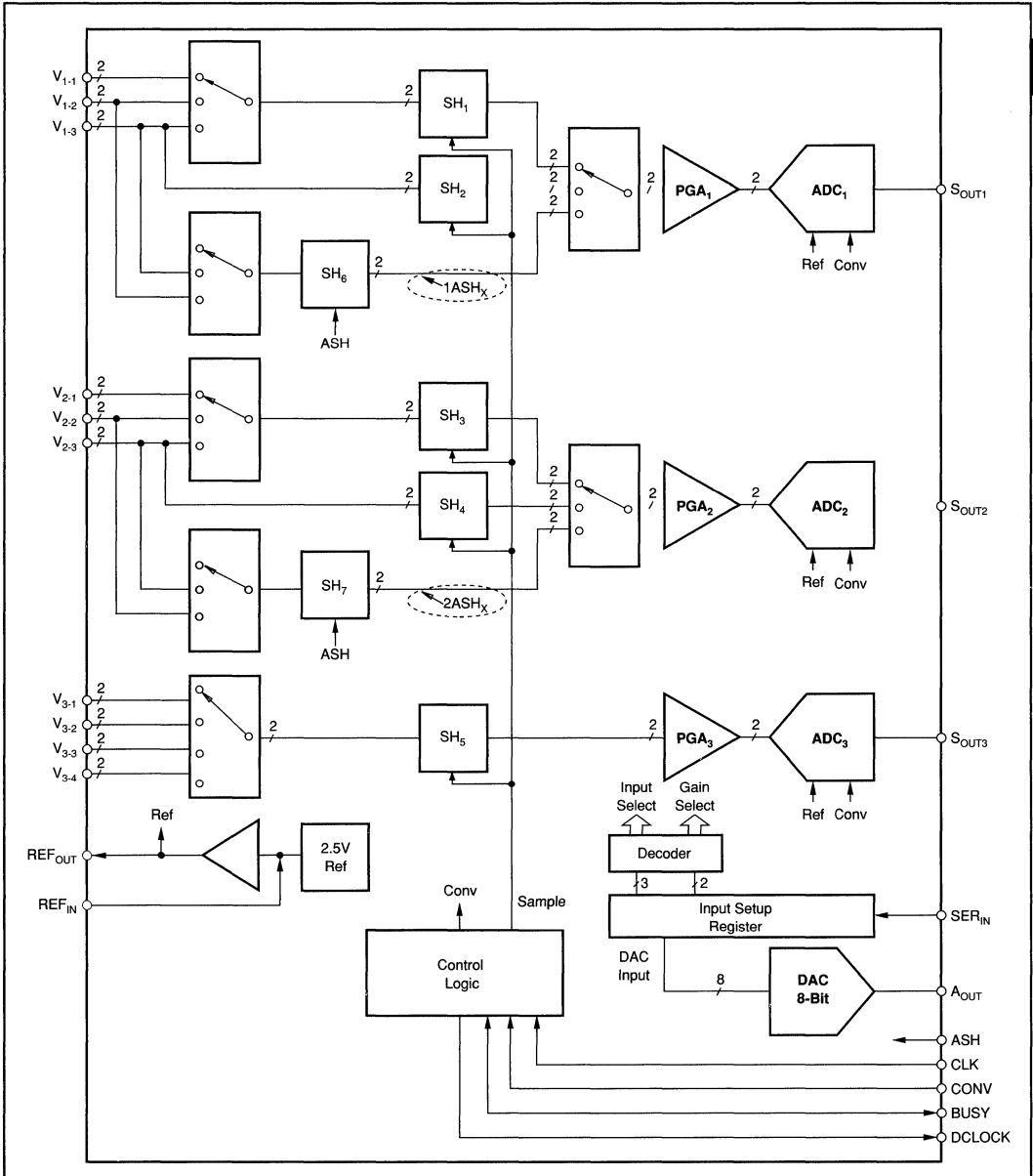
SAMPLE HOLDS

The ADS7833 contains seven sample holds. Five of them (SH_1 through SH_5) sample simultaneously and have their sample/hold timing internally synchronized. (The timing is shown in Figure 2).

Three of the sample holds (SH_1, SH_3, and SH_5) are connected to the input multiplexers so that they can provide simultaneous sampling for all of their channels inputs. In addition, SH_2 and SH_4 simultaneously sample the third input of their channels (V_{1-3} and V_{2-3}, respectively). This is useful in motor control applications where V_{1-2} and V_{1-3} are the quadrature inputs for one position sensor, and V_{2-2} and V_{2-3} are the quadrature inputs for a second position sensor (see Figure 7). In that application, it is desirable to sample the quadrature inputs of a given position sensor at the same time (even though they are converted on successive conversion cycles) (see Table III), so that their values are captured at the same shaft position.

The ADS7833 also has the capability for limited asynchronous sampling. The sampling of SH_6 and SH_7 is controlled asynchronously by the control signal ASH (see Table III). This allows two inputs each on channel 1 and channel 2 (see Table IV) to be sampled asynchronously from the timing of the other sample holds (see Figure 1). This can be useful in motor control applications where the two inputs for each channel come from a position sensor and it is desired to sample based on position sensor timing rather than system clock timing.

MULTIPLEXERS

The ADS7833 also contains several multiplexers that are used to select the desired analog inputs and connect the proper sample hold outputs to the PGAs and ADCs. The muxs are driven by a decoder which receives its inputs from the Input Setup Register. (See Table III for information on input channel selection). The input multiplexers can take full differential input signals (see Figure 3 and Table VII). The analog signals stay differential through the sample holds and the PGAs all the way to the inputs of the ADSs. This is done to provide the best possible high frequency noise rejection.

INPUT SETUP

As the ADCs are converting and outputting their serial digital data for one conversion cycle, a setup word is being inputted to be used for the next conversion cycle. The 13-bit word is supplied at the SER_{IN} pin (see Figure 1), and is stored in the buffered Input Setup Register. The Input Select and Gain Select portions of the word are decoded and determine the state of the multiplexers and PGAs (see CONFIGURABLE PARAMETERS section).

DIGITAL-TO-ANALOG CONVERTER

An 8-bit DAC provides 256 output voltage levels from 0V to 2.5V (see Table V for input/output relationships). The DAC is controlled by the DAC Input portion of the input setup word. The DAC Input portion of the word is strobed into the DAC at the end of the conversion cycle (14th CLK pulse in Figure 2).
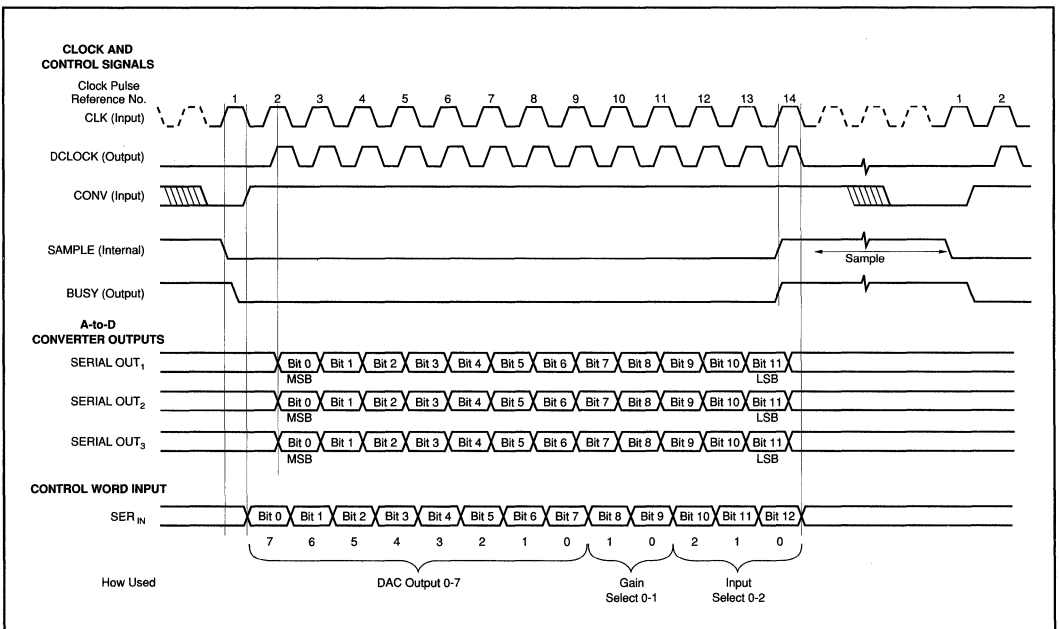
FIGURE 2. Timing Diagram.

VOLTAGE REFERENCE

The ADS7833 contains an internal 2.5V voltage reference. It is available externally through an output buffer amplifier. If it is desired to use an external reference, one may be connected at the REF_{IN} pins. This then overrides the internal 2.5V reference, is connected to the ADCs and is available buffered at the REF_{OUT} pin.

OTHER DIGITAL INPUTS AND OUTPUTS

Sampling and conversion is controlled by the CONV input (see Figure 2). The ADS7833 is designed to operate from an external clock supplied at the CLK input. This allows the conversion to be done synchronously with system timing so that transient noise effects can be minimized. The CLK signal may run continuously or may be supplied only during convert sequences. The BUSY and DCLOCK signals are internally generated and are supplied to make easier interfaces with microprocessors (see Figures 2, 4, and 5).

CONFIGURABLE PARAMETERS

Configurable parameters are:
- PGA Gain
- Input multiplexer and sample/hold selection
- DAC output voltage

Configuration information for these parameters is contained in the SER_{IN} word (See Figure 2). As one conversion is taking place, the configuration for the next conversion is being loaded into the buffered Input Setup Register via the SER_{IN} word. Table I shows information regarding these parameters.

CLOCK POSITIONS[1]	DESCRIPTION	FUNCTIONS
2-9	DAC Input$_{0-7}$	Sets DAC Output Voltage
10-11	Gain Select$_{0-1}$	Sets PGA Gains
12-14	Input Select$_{0-2}$	Determines Multiplexers Conditions

NOTE: (1) See Figure 2. "Clock Pulse Reference No."

TABLE I. Description of Configurable Parameters.

PGA GAIN

The PGA gain is determined by the Gain Select portion (bits 8 and 9) in the SER_{IN} word (see Figure 2). There is one gain input that sets the same gain for all three PGAs. The gain values and allowable full scale inputs are shown in Table II.

GAIN SELECT$_{0-1}$	GAIN SETTING	FULL SCALE INPUT
0_H	5.0V/V	±0.5V
1_H	2.5V/V	±1.0V
2_H	1.25V/V	±2.0V
3_H	1.0V/V	±2.5V

TABLE II. Gain Select Information.

For channels one and two the PGAs set the gain for all three analog inputs. For the third channel, only the V_{3-1} input is gain changed by the PGA. Inputs V_{3-2}, V_{3-3} and V_{3-4} are connected to ADC_3 at a fixed gain of 1V/V regardless of the Gain Select value.

INPUT MULTIPLEXER AND SAMPLE HOLD SELECTION

The Input Select portion of the SER_{IN} word (bits 10, 11 and 12) (see Figure 2) are decoded and determine the open/closed condition of the multiplexer switches. This in turn determines which input signals are connected to the sample holds and which sample holds are connected to the PGAs/ADCs.

INPUT SIGNALS FOR PGAs/ADCs

Table III shows the relationships between the value of Input Select$_{0-2}$ and the signals that are converted.

INPUT SELECT$_{0-2}$		ANALOG SIGNAL CONNECTED TO PGA$_X$/ADC$_X$		
HEX CODE	BINARY CODE	PGA$_1$/ADC$_1$	PGA$_2$/ADC$_2$	PGA$_3$/ADC$_2$
0_H	000	Undefined	Undefined	V_{3-4}
1_H	001	1ASH$_X$[1]	2ASH$_X$	V_{3-4}
2_H	010	V_{1-3} via SH$_1$	V_{2-3} via SH$_3$	V_{3-3}
3_H	011	V_{1-3} via SH$_2$	V_{2-3} via SH$_4$	V_{3-3}
4_H	100	V_{1-2}	V_{2-2}	V_{3-2}
5_H	101	V_{1-2}	V_{2-2}	V_{3-2}
6_H	110	V_{1-2}	V_{2-2}	V_{3-2}
7_H	111	V_{1-1}	V_{2-1}	V_{3-1}

NOTE: (1) This is a signal internal to the ADS7833 (see Figure 1). 1ASH$_X$ is the output of asynchronous sample hold, SH$_6$. The "1" indicates a channel 1 input. The "X" term is either 2 or 3 (i.e., signal V_{1-2} or V_{1-3}. See Table IV regarding how this selection is made.

TABLE III. Input Controls for Asynchronous Sample Holds.

Input Select = 7_H—Synchronously sample and convert input signals V_{1-1}, V_{2-1}, and V_{3-1}.

Input Select = 4_H, 5_H, 6_H—Synchronously sample and convert input signals V_{1-2}, V_{2-2}, and V_{3-2}. These codes also cause SH$_2$ and SH$_4$ to sample their inputs. Values 4_H, 5_H, 6_H have different effects on the inputs to SH$_6$ and SH$_7$ (see Table IV).

Input Select = 3_H—Convert V_{1-3} via SH$_2$, V_{2-3} via SH$_4$, and V_{3-3} (V_{1-3} and V_{2-3} are from the value sampled in a preceding conversion cycle with Input Select = 4_H, 5_H or 6_H).

Input Select = 2_H—Convert V_{1-3} via SH$_1$, V_{2-3} via SH$_3$, and V_{3-3} (V_{1-3} is sampled on SH$_2$ in this conversion cycle).

Input Select = 1_H—Input V_{3-4} is converted by PGA$_3$/ADC$_3$. The output of the asynchronous sample holds, SH$_6$ and SH$_7$, are converted by PGA$_1$/ADC$_1$ and PGA$_2$/ADC$_2$, respectively. Note that the inputs to SH$_6$ and SH$_7$ are determined by other Input Select values (see Table IV). Thus, to properly convert the output of one of the asynchronous sample holds it is first necessary to choose its input with a previous conversion cycle. Also, the output of SH$_6$ or SH$_7$ will only be converted if ASH goes low before the CONV command is received.

Input Select = 0_H—V_{3-4} is converted by PGA_3/ADC_3. The inputs to PGA_1/ADC_1 and PGA_2/ADC_2 are undefined.

CONVERSIONS FROM THE ASYNCHRONOUS SAMPLE HOLDS

Decoding the Input Select value also determines which inputs are applied to the two asynchronously controlled sample holds SH_6 and SH_7. (See Table IV.) One of the three possible inputs is selected by the Input Select value being 4, 5, or 6.

The "No Effect" states indicate that these values of Input Select have no effect on the multiplexers at the input of SH_6 and SH_7. When one of the "No Effect" values of Input Select is presented, the multiplexers will not be changed (i.e., their condition is determined by the last 4, 5, or 6 value of Input Select that existed prior to the "No Effect" state).

Note that Input Select = 1_H presents the output of SH_6 and SH_7 ($1ASH_X$ and $2ASH_X$) to PGA_1/ADC_1 and PGA_2/ADC_2, respectively (see Table III). Therefore, in order to properly convert the asynchronous sampled signals, it is first necessary to choose an input signal (Input Select equal 5 or 6 in Table IV) with one load/convert cycle and then convert the sample hold output (Input Select = 4 in Table III) in a following conversion cycle.

INPUT SELECT 0-2		ANALOG SIGNAL CONNECTED TO SH_6/SH_7	
HEX CODE	BINARY CODE	SH_6	SH_7
0_H	000	No Effect	No Effect
1_H	001	No Effect	No Effect
2_H	010	No Effect	No Effect
3_H	011	No Effect	No Effect
4_H	100	Open	Open
5_H	101	V_{1-2}	V_{2-2}
6_H	110	V_{1-3}	V_{2-3}
7_H	111	No Effect	No Effect

TABLE IV. Input Controls for Asynchronous Sample Holds.

DAC OUTPUT VOLTAGE

The value of the DAC output voltage is determined by the DAC Input portion of the SER_{IN} word (bits 0 through 7) (see Figure 2). The 8-bit DAC has 256 possible output voltages from 0V to +2.49V. The value of 1 LSB is 0.0098V.

DIGITAL INPUT DAC INPUT$_{0-7}$		ANALOG OUTPUT
HEX CODE	BINARY CODE	
00_H	0000 0000	0V
01_H	0000 0001	+0.0098V
•	•	•
•	•	•
•	•	•
FF_H	1111 1111	+2.499

TABLE V. DAC Input/Output Relationships.

ANALOG-TO-DIGITAL CONVERTERS

ARCHITECTURE

The ADCs are 12-bit, successive approximation types implemented with a switched capacitor circuitry.

SPEED

The clock for the ADC conversion is supplied externally at the CLK pin. Maximum clock frequency for specified accuracy is 1.4MHz. This results in a complete conversion cycle (S/H acquisition and A/D conversion) of 10µs.

INPUT/OUTPUT

The ADS7833 is designed for bipolar input voltages and uses a binary two's complement digital output code. A programmable gain function is associated with each ADC. This changes the full scale analog input range and the analog resolution of the converter. Details are shown in Table VI.

DIFFERENTIAL AND COMMON-MODE INPUT VOLTAGES

The ADS7833 is designed with full differential signal paths all the way from the multiplexer inputs through to the input of the ADCs. This was done to provide superior high frequency noise rejection.

As is common with most differential input semiconductor devices, there are compound restrictions on the combination of differential and common-mode input voltages. This matter is made slightly more complicated by the fact that most

DESCRIPTION	ANALOG INPUT					
GAIN SELECT CODE	0	1	2	3		
GAIN	5V/V	2.5V/V	1.25V/V	1.0V/V	DIGITAL OUTPUT	
FULL SCALE RANGE	±0.5V	±1.0V	±2.0V	±2.5V	HEX CODE	BINARY CODE
+Full Scale (FS −1LSB)	+0.49976	+0.9995V	+1.999V	+2.499	$7FF_H$	0111 1111 1111
One Bit above Mid-Scale	+0.244mV	+0.488mV	+0.976mV	+1.22mV		0000 0000 0001
Mid-Scale	0V	0V	0V	0V	000_H	0000 0000 0000
One Bit Below Mid-Scale	−0.244V	−0.488mV	−0.976mV	−1.22mV	FFF_H	1111 1111 1111
−Full Scale	−0.500V	−1.000V	−2.000V	−2.500V	800_H	1000 0000 0000

NOTE: The programmable gain function applies to all three input channels for ADC$_1$ and ADC$_2$. However, the programmable gain function only applies to the first input (V$_{3-1}$) for ADC$_3$. The other three inputs (V$_{3-2}$, V$_{3-3}$, and V$_{3-4}$) are not affected by the GAIN SEL input. They operate at a fixed gain of 1V/V and thus have a fixed ±2.5V full scale input range.

TABLE VI. Analog Input - Digital Output Relationships.

of the analog inputs are capable of being affected by the programmable gain function. The possible differential and single ended configurations are shown in Figures 3a and 3b.

The maximum differential and common mode restrictions are shown in Table VII.

GAIN SELECT CODE	0	1	2	3
Gain	5V/V	2.5V/V	1.25V/V	1.0V/V
Full Scale Range (V_D with V_{CM} = 0)	±0.5V	±1.0V	±2.0V	±2.5V
Largest Positive Common Mode Voltage, $V_{CM}+$	+2.7V	+2.4V	+1.9V	+1.6V
Largest Negative Common Mode Voltage, $V_{CM}-$	–2.7V	–2.4V	–1.9V	–1.6V

TABLE VII. Differential and Common Mode Voltage Restrictions.

MICROPROCESSOR INTERFACE

The internal logic of the ADS7833 is designed for easy control and data interface with microprocessors. Figure 4 shows the interface for loading the input control word from the microprocessor data bus into the serial input of the ADS7833. Figure 5 shows the interface for loading the serial ADC output into the parallel data bus and memory of the microprocessor.

TYPICAL ISOLATED ANALOG INPUT

Figure 6 shows an ISO130 used to isolate the current measurement in a motor speed control application. This amplifier is well suited for this application because of its high transient immunity (l0kV/μs). Its differential output feature is well suited to the differential input of the ADS7833. Keeping the signal transmission differential helps to preserve the high frequency noise rejection of the system.

A unique characteristic of the ISO130 is that it has a common mode output voltage of approximately 2.5V. To accept this level of CMV, the ADS7833 must be operated at a gain of 5V/V (±0.5V full scale differential input). (See Figure 3 and Table VII). Since the ISO130 has a gain of 8V/V, the maximum value of V_{SENSE} is 62.5mV. Thus, the value of R_{SENSE} is chosen to scale V_{SENSE} to this maximum value.

POWER-UP INITIALIZATION

When power is applied to the ADS7833, two conversion cycles are required for initialization and valid digital data is outpulled on the third cycle.

The first conversion after power is applied is performed with indeterminate configuration values in the double buffer output of the Input Setup Register. The second conversion cycle loads the desired values into the register. The third conversion uses those values to perform proper conversions and output valid digital data from each of the ADCs.

FIGURE 3. (a) Differential Signal Source, and (b) Single Ended Signal Source.
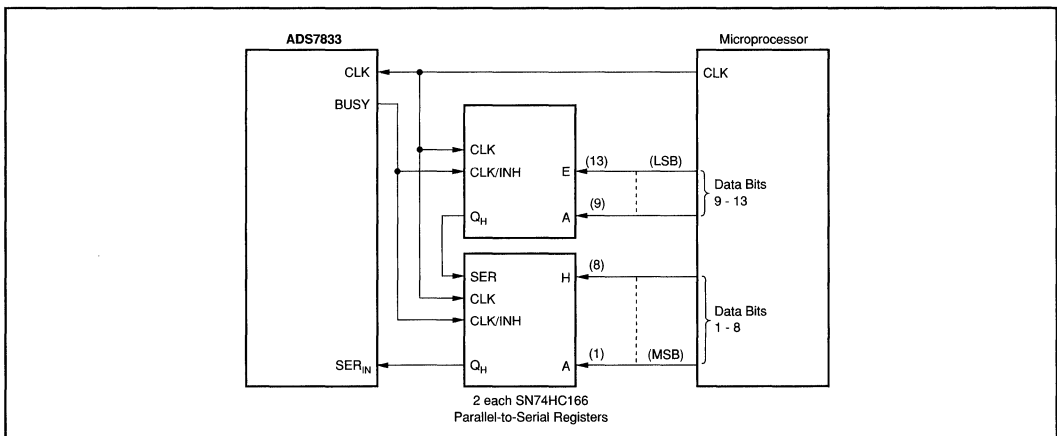
FIGURE 4. Typical Microprocessor Interface for Loading Input Control Word.
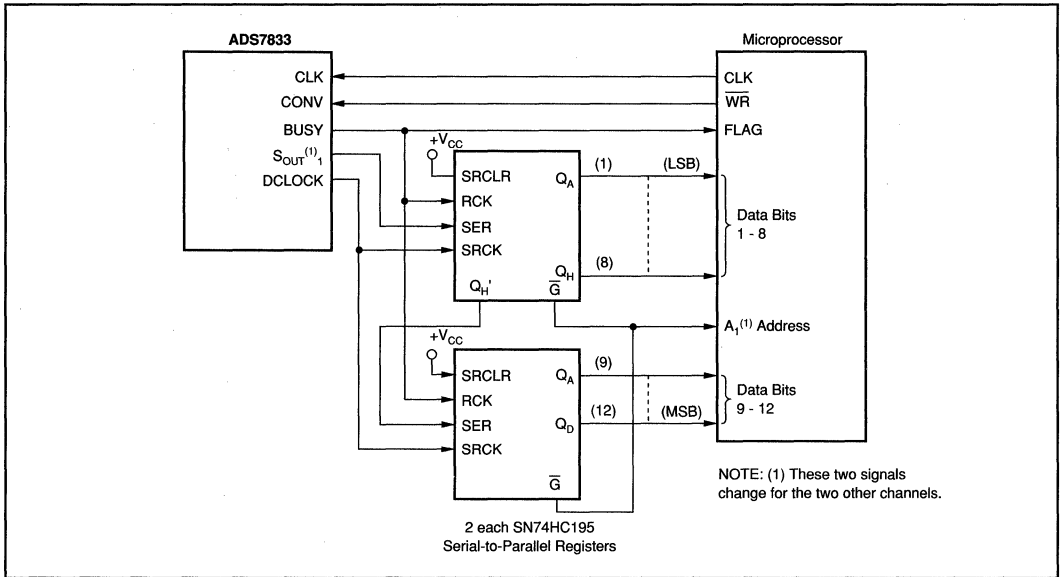
FIGURE 5. Typical Microprocessor Interface for A/D Serial Output.
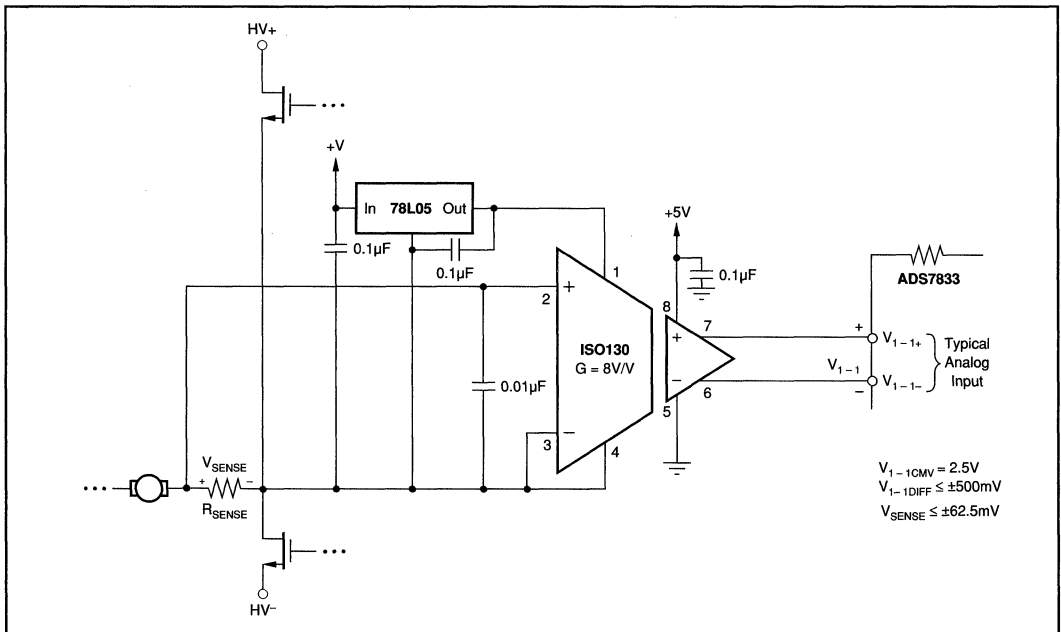
FIGURE 6. Typical Isolated Differential Analog Input.
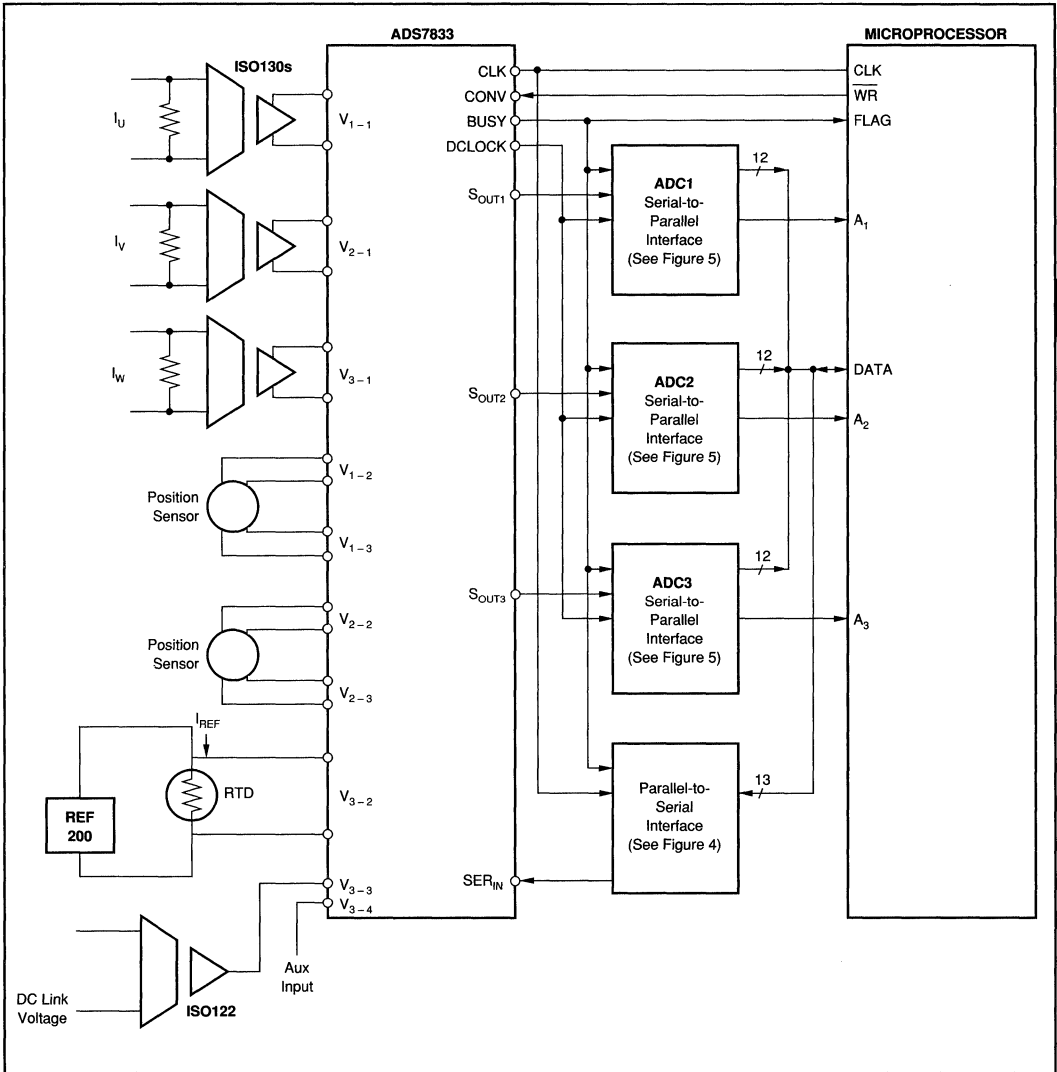
FIGURE 7. Motor Control Application Using Position Sensors.

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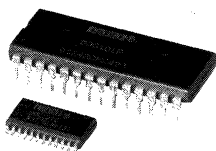
DDC101

20-BIT ANALOG-TO-DIGITAL CONVERTER

FEATURES
● **MONOLITHIC CHARGE INPUT ADC**
● **DIGITAL FILTER NOISE REDUCTION:**
  0.9ppm, rms
● **DIGITAL ERROR CORRECTION: CDS**
● **CONVERSION RATE: Up to 15kHz**
● **USER FRIENDLY EVALUATION FIXTURE**

APPLICATIONS
● **DIRECT PHOTOSENSOR DIGITIZATION**
● **PRECISION INSTRUMENTATION**
● **INFRARED PYROMETRY**
● **PRECISION PROCESS CONTROL**
● **CT SCANNER DAS**
● **CHEMICAL ANALYZERS**

DESCRIPTION

The DDC101 is a precision, wide dynamic range, charge digitizing A/D converter with 20-bit resolution. Low level current output devices, such as photosensors, can be directly connected to its input. The most stringent accuracy requirements of many unipolar output sensor applications occur at low signal levels. To meet this requirement, Burr-Brown developed the adaptive delta modulation architecture of the DDC101 to provide linearly improving noise and linearity errors as the input signal level decreases. The DDC101 combines the functions of current-to-voltage conversion, integration, input programmable gain amplification, A/D conversion, and digital filtering to produce precision, wide dynamic range results. The input signal can be a low level current connected directly into the unit or a voltage connected through a user selected resistor. Although the DDC101 is optimized for unipolar signals, it can also accurately digitize bipolar input signals. The patented delta modula-

tion topology combines charge integration and digitization functions. Oversampling and digital filtering reduce system noise dramatically. Correlated Double Sampling (CDS) captures and eliminates steady state and conversion cycle dependent offset and switching errors that are not eliminated with conventional analog circuits.

The DDC101 block diagram is shown below. During conversion, the input signal is collected on the internal integration capacitance for a user determined integration period. A high precision, autozeroed comparator samples the analog input node. Tracking logic updates the internal high resolution D/A converter at a 2MHz rate to maintain the analog input at virtual ground. A user programmable digital filter oversamples the tracking logic's output. The digital filter passes a low noise, high resolution digital output to the serial I/O register. The serial outputs of multiple DDC101 units can be easily connected together in series or parallel if desired to minimize interconnections.

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TABLE OF CONTENTS

SECTION 1
BASIC THEORY OF OPERATION

The basic function of the DDC101 is illustrated in the Simplified Equivalent Circuit shown in Figure 1. The operation is equivalent to the functions performed by a very high quality, low bias current switched integrator followed by a precision floating point programmable gain amplifier and ending with a high resolution A/D converter.

The second block diagram, Figure 2, shows the DDC101 circuit architecture which implements these functions monolithically. During each conversion, the input signal current is collected on the internal integration capacitance, C_{INT}, as charge for a user determined integration period, T_{INT}. As the integration capacitor collects input charge, the tracking logic updates the internal high resolution D/A converter at a 2MHz rate to maintain the analog input node at virtual ground.

The digital filter oversamples the tracking logic's output at the beginning and end of each integration period to produce two oversampled data points. The DDC101 measures the charge accumulated in the integration and performs correlated double sampling (CDS) by subtracting these two data points. CDS eliminates integration cycle dependent errors such as charge injection, offset voltage, and reset noise since these errors are measured with the signal at each of the two data points. The number of oversamples, and thus the frequency response of the digital filter, is user programmable.

The digital filter passes a low noise, high resolution digital output to the serial I/O register. Since the timing control of the serial I/O register is independent of the DDC101 conversion process, the outputs of multiple DDC101 units can be connected together in series or parallel to minimize interconnections.

FIGURE 1. Simplified Equivalent Circuit of DDC101 to Illustrate Function.
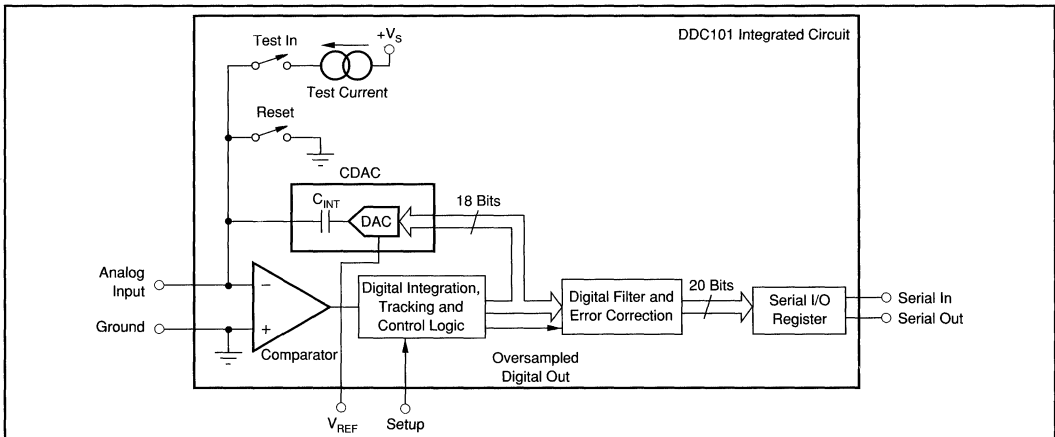
FIGURE 2. DDC101 Block Diagram.

An internal test current source is provided for basic functionality testing and diagnostics. This approximately 100nA current source is pin activated and sums with the external input current.

Figure 3 shows a more detailed circuit configuration of the DDC101. The single integration capacitor, C_{INT}, and the D/A converter have been replaced with a high resolution Capacitor Digital-to-Analog Converter (CDAC). By switching between ground and V_{REF} the binary weighted capacitor array of the CDAC accumulates the input signal's charge to keep the comparator input at virtual ground.
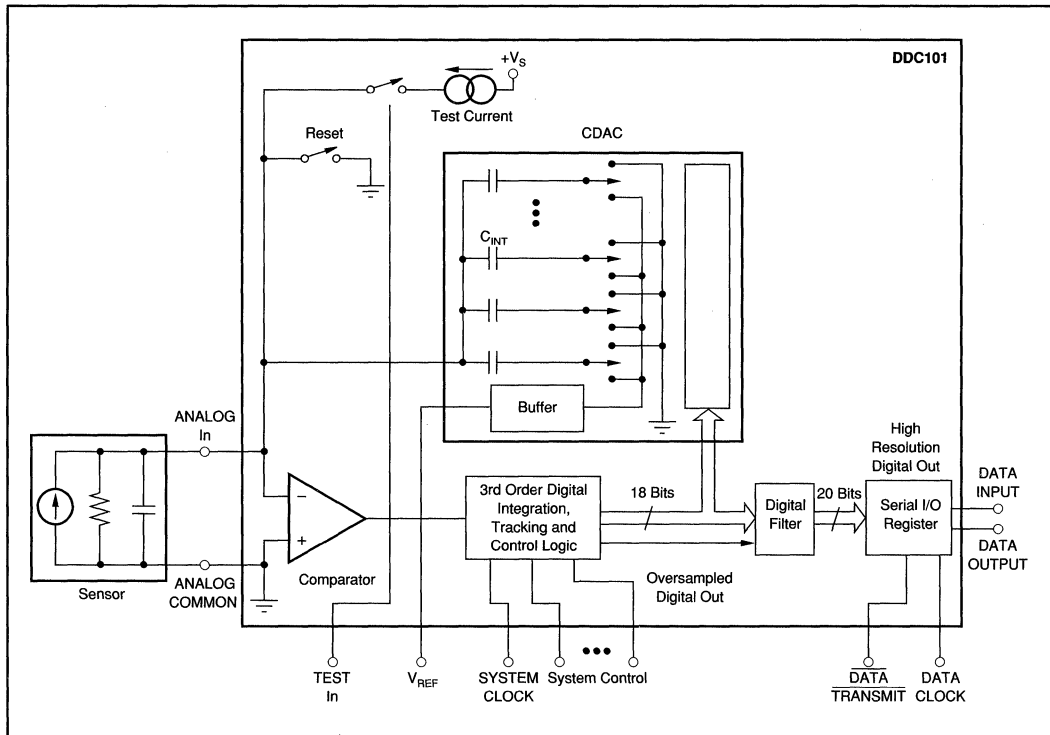
FIGURE 3. DDC101 Detailed Circuit Diagram.

SECTION 2
SPECIFICATIONS

ELECTRICAL

All specifications with unipolar current input range, $T_{INT} = 1ms$, correlated double sampling enabled, System Clock = 2MHz, $V_{REF} = -2.5V$, $T_A = +25°C$ and $V_S = \pm5VDC$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS					
Charge Input[6]					
Unipolar Input Range	BTC Output Code	–1.95		500	pC/Integration
Bipolar Input Range	BTC Output Code	–251.95		250	pC/Integration
Input Current	Unipolar or Bipolar Range			7.8	µA
Current Input Range Examples[10]					
Unipolar Input Range	$T_{INT} = 100µs$	–0.0195		5	µA
Unipolar Input Range	$T_{INT} = 1ms$	–1.95		500	nA
Bipolar Input Range	$T_{INT} = 100µs$	–2.5195		2.5	µA
Bipolar Input Range	$T_{INT} = 1ms$	–251.95		250	nA
Voltage Input Examples[10]					
Unipolar Input Range[2]	$R_{IN} = 10MΩ, T_{INT} = 1ms$	–0.0195		5	V
Bipolar Input Range[2]	$R_{IN} = 10MΩ, T_{INT} = 1ms$	–2.5195		2.5	V
DYNAMIC CHARACTERISTICS					
Conversion Time		64		256×10^6	µs
Integration Time		64		10^6	µs
System Clock Input		0.5		2	MHz
ACCURACY					
Unipolar Mode Noise					
Noise, Low Level Current Input[1]	$C_{SENSOR} = 0pF, L = 8$		0.9		ppm of FSR, rms[3]
Noise, Low Level Current Input[1]	$C_{SENSOR} = 0pF, L = 1$		1.6		ppm of FSR, rms
Noise, Low Level Current Input[1]	$C_{SENSOR} = 100pF, L = 1$		2.1	3	ppm of FSR, rms
Noise, Low Level Current Input[1]	$C_{SENSOR} = 500pF, L = 1$		4.2		ppm of FSR, rms
Noise, Voltage Input[1, 2]	$R_{IN} \geq 20MΩ$		1.9		ppm of FSR, rms
Differential Linearity Error					
Unipolar Input Range	Entire Range			±0.005% Reading ±0.5ppm FSR, max	
	0.1% FSR Input			±0.00006	% of FSR
	1% FSR Input			±0.00010	% of FSR
	10% FSR Input			±0.00055	% of FSR
Unipolar or Bipolar Input Range				±0.0015	% of FSR
Integral Linearity Error					
Unipolar Input Range[11]	Entire Range			±0.0244% Reading ±2.5ppm FSR, max	
	0.1% FSR Input			±0.00028	% of FSR
	1% FSR Input			±0.00050	% of FSR
	10% FSR Input			±0.0027	% of FSR
Unipolar or Bipolar Input Range[11]				±0.003	% of FSR
No Missing Codes					
Unipolar Input Range			18		Bits
Bipolar Input Range			16		Bits
Input Bias Current	$T_A = +25°C$		3	10	pA
DC Gain Error			±0.5	±2	% of FSR
Output Offset Error[8]			±0.5		ppm of FSR
Input Offset Voltage[8]			±0.5	±2	mV
External Voltage Reference, V_{REF}			–2.5		VDC
Internal Test Signal			100		nA
Internal Test Signal Accuracy			±20		nA
Gain Sensitivity to V_{REF}	$V_{REF} = 2.5V \pm0.1V$		1:1		
PSRR		80	90		dB
PERFORMANCE OVER TEMPERATURE					
Output Offset Drift[8]	not including bias current drift		0		µV/°C
Input Offset Voltage Drift[8]			1		µV/°C
Input Bias Current Drift	+25°C to +45°C		0.1	0.5	pA/°C
Input Bias Current	$T_A = +85°C$		8	40	pA
Gain Drift[4]			±15		ppm/°C
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	$I_{IH} = +5µA$	+2.0		$+V_{CC}$	V
V_{IL}	$I_{IL} = +5µA$	–0.3		+0.8	V
V_{OH}	$I_{OH} = 2$ TTL Loads	+2.4		$+V_{CC}$	V
V_{OL}	$I_{OL} = 2$ TTL Loads	0.0		0.4	V
Data Clock					
Data I/O				8	MHz
SETUP Code I/O[9]				4	MHz
Data Format					
Straight Binary	Unipolar or Bipolar Range		20		Bits
Two's Complement	Unipolar or Bipolar Range		21		Bits

DDC101

2

A/D CONVERTERS, DATA ACQUISTION COMPONENTS

SPECIFICATIONS (CONT)

ELECTRICAL

All specifications with unipolar current input range, T_{INT} = 1ms, correlated double sampling enabled, System Clock = 2MHz, V_{REF} = –2.5V, T_A = +25°C and V_S = ±5VDC unless otherwise noted.

		DDC101			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Operation[5]		±4.75	±5	±5.25	VDC
Quiescent Current, Positive Supply	V_S+ = +5VDC, V_{DD}+ = +5VDC		15.6	19.5	mA
Analog, V_S+			8.9		mA
Digital, V_{DD}+			6.7		mA
Quiescent Current, Negative Supply	V_S– = –5VDC		18.0	22.5	mA
Operating Power			170		mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Input = low level (less than 1% of Full Scale); Full Scale I_{IN} = 500nA; T_{INT} = 1ms; Unipolar Input Range; Acquisition Time = 16 clock cycles, Oversampling = 128. (2) Voltage input is converted through user provided input resistor, R_{IN}. (3) FSR is Full Scale Range. (4) Gain Drift does not include the drift of the external reference. (5) V_{DD}+ must be less than or equal to V_S+. See Section 7 for recommended connections. (6) Straight Binary output code has slightly different Charge Range. See Section 6. (8) Input offset voltage is nulled by autozero circuitry and causes no output error. See Section 6 (Internal Error Correction). (9) This is the maximum clock frequency at which SETUP codes can be written to and read from the DDC101. (10) For other input current and voltage configurations, see Discussion of Specifications and Detailed Theory of Operation sections. (11) A best-fit straight line method is used to determine linearity. Two different best-fit straight lines are used for the two unipolar integral linearity specifications. Acquisition Time = 16 clock cycles, Oversampling = 128.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DDC101P	28-Pin DIP	215
DDC101U	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

```
Analog Inputs
  Input Current ............................................. 100mA, momentary
  Input Current ................................................. 10mA, continuous
  Input Voltage ..................................... $V_S$+ +0.5V to $V_S$– –0.5V
Power Supply
  $V_S$+ ............................................................................. + 7V
  $V_S$– ............................................................................. –7V
  $V_{DD}$+ ............................................................ must be ≤ $V_S$+
Maximum Junction Temperature ................................................. +165°C
```

ORDERING INFORMATION

MODEL	PACKAGE	THERMAL RESISTANCE (θ_{JA}) (°C/W)
DDC101P	28-Pin DW DIP	100
DDC101U	24-Pin SOIC	100

⚡ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View   **28-Pin DIP**

Pin	Name	Pin	Name
1	V_S–, ANALOG	28	REFERENCE BUFFER BYPASS
2	ANALOG COMMON	27	V_{REF}
3	ANALOG In	26	TEST In
4	ANALOG COMMON	25	RESET SETUP In
5	V_S+, ANALOG	24	SETUP In
6	V_S+, ANALOG	23	READ DATA/SETUP
7	NC	22	NC
8	NC	21	NC
9	RESET SYSTEM In	20	DATA TRANSMIT In
10	FDS (Final Data Point Start) In	19	OVERFLOW + Out
11	SYSTEM CLOCK	18	OVERFLOW – Out
12	DATA CLOCK	17	DATA VALID Out
13	DATA INPUT	16	DATA OUTPUT
14	V_{DD}+, DIGITAL	15	DIGITAL GROUND

PIN CONFIGURATION

Top View   24-Pin SOIC

V_S–, ANALOG	1	24 REFERENCE BUFFER BYPASS
ANALOG COMMON	2	23 V_{REF}
ANALOG In	3	22 TEST In
ANALOG COMMON	4	21 $\overline{\text{RESET SETUP}}$ In
V_S+, ANALOG	5	20 SETUP
V_S+, ANALOG	6	19 READ DATA/$\overline{\text{SETUP}}$
$\overline{\text{RESET SYSTEM}}$ In	7	18 $\overline{\text{DATA TRANSMIT}}$ In
$\overline{\text{FDS}}$ (Final Data Point Start) In	8	17 $\overline{\text{OVERFLOW}}$ + Out
SYSTEM CLOCK	9	16 $\overline{\text{OVERFLOW}}$ – Out
DATA CLOCK	10	15 DATA VALID Out
DATA INPUT	11	14 DATA OUTPUT
V_{DD}+, DIGITAL	12	13 DIGITAL GROUND
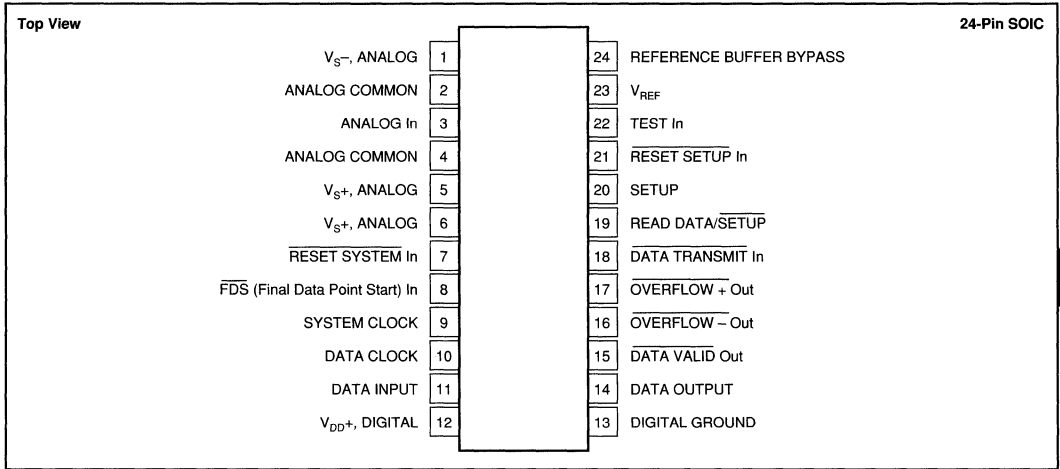
SECTION 3
PIN DESCRIPTIONS

SOIC PIN NUMBER	DIP PIN NUMBER	NAME	DESCRIPTION
1	1	V_S–, ANALOG	Negative analog power supply voltage, –5VDC.
2	2	ANALOG COMMON	Analog ground point.
3	3	ANALOG INPUT	Input for low level current signal. Photosensor can be directly connected to this input. With a resistor in series, DDC101 will convert a voltage input.
4	4	ANALOG COMMON	Analog ground point.
5	5	V_S+, ANALOG	Positive analog power supply voltage, +5VDC. Hardwire to pin 6.
6	6	V_S+, ANALOG	Positive analog power supply voltage, +5VDC. Hardwire to pin 5.
7	9	$\overline{\text{RESET SYSTEM}}$ In	This input resets DDC101, but does not reset the SETUP register. The DDC101 system is reset when this pin is active; reset action is removed when the pin is inactive.
8	10	$\overline{\text{FDS}}$ In	This is Final Data point Start input. This input is the basic user control of the integration and conversion timing. When it becomes active, the DDC101 starts collection of the M, final data point samples. The beginning of the next integration time is exactly M system clock periods after the Final Data point Start command when operating in the continuous mode.
9	11	SYSTEM CLOCK	This clock input sets the basic sampling rate of the DDC101. The DDC101 is specified with a clock speed of 2MHz. The clock speed can be 0.5MHz to 2.0MHz.
10	12	DATA CLOCK	This clock input controls the data transfer rate for the serial DATA INPUT and DATA OUTPUT ports. The DATA CLOCK is independent of the SYSTEM CLOCK. This allows the DATA CLOCK to be operated at higher or lower speeds than the SYSTEM CLOCK. For best noise performance, data should not be transmitted and the DATA CLOCK should not be active during the initial and final data point collection. If data is being transmitted during the initial and final data point collection periods, the DATA CLOCK should be synchronized to the SYSTEM CLOCK, to minimize added noise. DATA CLOCK can be connected to SYSTEM CLOCK, so that the same clock is used for both; however, for best noise performance, the DATA CLOCK input should be active only when data is transmitted.
11	13	DATA INPUT	This input can be used to "daisy chain" the output of several DDC101s together to minimize wiring. The output register of the DDC101 acts as a shift register to pass through the output of previously connected DDC101 units. In this way, multiple DDC101 units can convert simultaneously then sequence the data out serially on the same data line with one common control line and one common data line for all DDC101 units.
12	14	V_{DD}+, DIGITAL	Digital power supply, +5VDC. V_{DD}+ must be less than or equal to V_S+.
13	15	DIGITAL GROUND	Digital ground point.
14	16	DATA OUTPUT	This output provides serial digital data clocked out at user controlled DATA CLOCK rate. Output data format is a 21-bit binary two's complement word or a 20-bit straight binary word. The data word is transmitted MSB first. When $\overline{\text{DATA TRANSMIT}}$ is not active DATA OUTPUT tri-states.
15	17	DATA VALID	This output is activated when conversion is complete and remains active until the $\overline{\text{DATA TRANSMIT}}$ input is activated.
16	18	$\overline{\text{OVERFLOW}}$–	The $\overline{\text{OVERFLOW}}$ output signals each provide an open collector output so that the overflow outputs from several DDC101s can easily be connected (wire ORed) together to a common pull-up resistor. They are activated when the input is beyond the acceptable range during conversion. Specifically, they are activated when the internal D/A converter input or digital filter exceeds full scale. They are Cleared at the end of conversion 1/2 clock cycle after $\overline{\text{DATA VALID}}$ high. DATA VALID can be used to capture $\overline{\text{OVERFLOW}}$ data into an external register.
17	19	OVERFLOW+	

PIN DESCRIPTIONS (CONT)

SOIC PIN NUMBER	DIP PIN NUMBER	NAME	DESCRIPTION
18	20	DATA TRANSMIT In	This input controls the transmission of data from the serial I/O register of the DDC101. It can be activated anytime after DATA VALID out becomes active. It must remain active until all data has been collected from the serial I/O register(s) of all DDC101s in the data path.
19	23	READ DATA/ SETUP In	This input can be used to read back the current SETUP data. When this input is held high, the output from DATA OUTPUT is the data collected by the DDC101. When this input is pulled low, an internal shift register is loaded with the current SETUP data on the rising edge of DATA CLOCK. This SETUP data shift register is logically connected between DATA INPUT and DATA OUTPUT pins and can be read in the same way that the data output is read. SETUP data read back does not invalidate data already stored in the DDC101's serial I/O register or data being collected by the DDC101, although digital noise concerns should be considered as discussed in DATA CLOCK.
20	24	SETUP In	This input pin controls the DDC101 SETUP. A 12-bit digital word transmitted into this pin controls Acquisition Time, K, Oversampling, M, Multiple Integrations, L, Input Range and Output Data Format. The DDC101 reads the SETUP code at this pin after the RESET SETUP input transitions from active to inactive. The SETUP code is read into the SETUP register on the 12 positive data clock transitions following that transition.
21	25	RESET SETUP	Resets SETUP register only, does not reset balance of DDC101. The DDC101 reads SETUP input data after this input transitions from active (reset) to inactive.
22	26	TEST In	This is a digital input that controls the connection of an internal DC current source to the DDC101's input. TEST In exercises the DDC101 and is intended to test for functionality only. The typical test input current is 100nA ±20nA. The quiescent current of the DDC101 increases by approximately 1mA when TEST In is active. When TEST is HIGH, the internal current source is ON and current is flowing into the DDC101 input. When TEST is LOW, the current source is disconnected from the input.
23	27	V_{REF}	An external –2.5V reference must be connected to the REFERENCE In pin. Use of an external reference allows multiple DDC101s to use the same system reference for optimum channel matching. The external reference should be filtered to minimize noise contribution (see Figure 24).
24	28	REFERENCE BUFFER BYPASS	An external capacitor of 10µF should be connected to this node to provide proper operation of the internal D/A converter. The REFERENCE In pin is connected to an internal reference buffer amplifier. The internal reference buffer drives the internal CDAC. This buffer output is not intended for external use.
—	7	NC	No connection in 28-pin DIP.
—	8	NC	No connection in 28-pin DIP.
—	21	NC	No connection in 28-pin DIP.
—	22	NC	No connection in 28-pin DIP.

SECTION 4
TIMING CHARACTERISTICS

All specifications with Unipolar input range, T_{INT} = 1ms, Current Input, Correlated Double Sampling enabled, Sys Clock = 2MHz, V_{REF} = –2.5V, T_A = +25°C and V_S = ±5VDC unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	FDS Setup	30			ns
t_2	FDS width, Continuous Conversion	50		(M–1) Clocks+t_1+100ns	ns
t_3	FDS width, Asynchronous Conversion	M Clocks+t_1			ns
t_4	FDS HIGH to start of next integration, Asynchronous Conversion		50		ns
t_5	Setup time for RESET SETUP HIGH to DATA CLOCK HIGH	60			ns
t_6	Setup time for Setup Codes data valid before rising edge of DATA Clock	30			ns
t_7	Hold time for Setup Codes data valid after rising edge of DATA Clock	30			ns
t_8	Propagation delay from rising edge of SYSTEM CLOCK to DATA VALID LOW		50		ns
t_9	Propagation delay from DATA TRANSMIT LOW to DATA VALID HIGH		35		ns
t_{10}	Setup time for DATA CLOCK LOW to DATA TRANSMIT LOW	30			ns
t_{11}	Propagation delay from DATA TRANSMIT LOW to valid data out		30		ns
t_{12}	Hold time that Data output is valid after falling edge of DATA CLOCK	10			ns
t_{13}	Propagation delay from DATA TRANSMIT HIGH to Data Output tri-stated			40	ns
t_{14}	Propagation delay from falling edge of SYSTEM CLOCK to OVERFLOW+ and OVERFLOW– cleared	25			ns
t_{15}	SYSTEM CLOCK pulse width HIGH	240			ns
t_{16}	SYSTEM CLOCK pulse width LOW	240			ns
t_{17}	DATA VALID LOW to DATA TRANSMIT LOW, Single DDC101	30		(LxN–21) Clocks	ns

DDC101 **2** **A/D CONVERTERS, DATA ACQUISITION COMPONENTS**

Continuous Integration Timing

SYSTEM CLOCK

$\overline{\text{FDS}}$ In should be coincident with negative clock.

$\overline{\text{FDS}}$ In

Internal Oversampling Interval — $\overline{\text{FDS}}$ initiates oversampling period.

M Clock Periods

Internal Reset

End of oversample period initiates reset for next integration.

Next integration begins when 1 clock period wide Internal Reset ends.

DATA VALID Out

Non-Continuous Integration Timing

SYSTEM CLOCK

$\overline{\text{FDS}}$ In should be coincident with negative clock.

$\overline{\text{FDS}}$ In

Internal Oversampling Interval — $\overline{\text{FDS}}$ initiates oversampling period.

End of $\overline{\text{FDS}}$ In initiates end of Internal Reset.

End of oversample period initiates reset.

Internal Reset

DATA VALID Out

When Internal Reset period ends, next integration begins.

FIGURE 4. Conversion Timing Diagrams.

$\overline{\text{RESET SETUP}}$ In

DATA CLOCK (4MHz, max for setup)

Read   Read   Read   Read

$\overline{\text{SETUP}}$ In ACQ_{MSB} ACQ_{LSB} Input Range Output Format
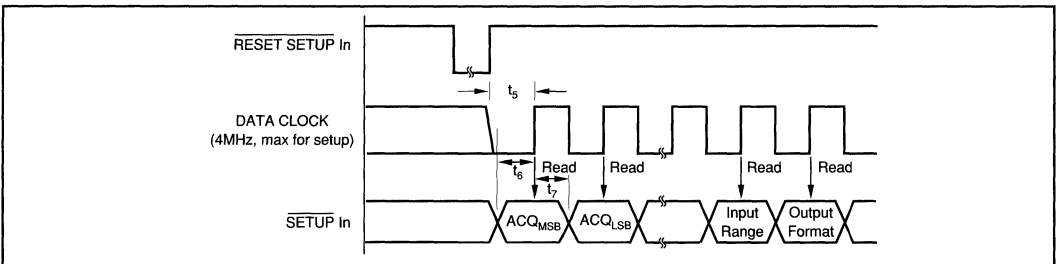
FIGURE 5. Input/Output Timing Diagram—SETUP Timing Diagram.

SYSTEM CLOCK

$\overline{\text{DATA VALID}}$ Out

$\overline{\text{DATA TRANSMIT}}$ In resets $\overline{\text{DATA VALID}}$ Out.

$\overline{\text{DATA TRANSMIT}}$ In

Data can be read on rising or falling edge of Data Clock

DATA CLOCK (8MHz, max for data)

DATA OUTPUT   Output Disabled   DDC(1) Bit 1, MSB   DDC(n) Bit 21, LSB   DDC (n+1) Bit 1   Output Disabled

Output Enabled

Last DDC Bit 21
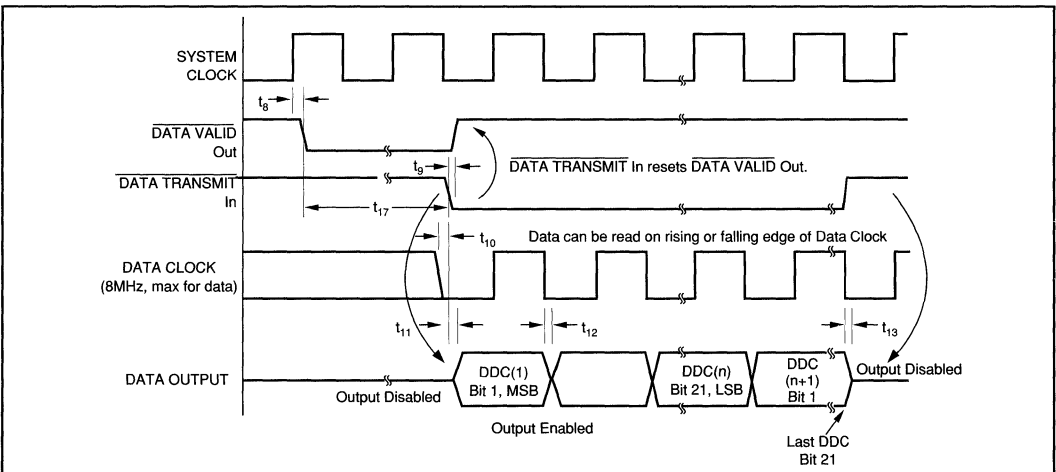
FIGURE 6. DATA TRANSMIT Timing Diagram.

TIMING DIAGRAMS (CONT)
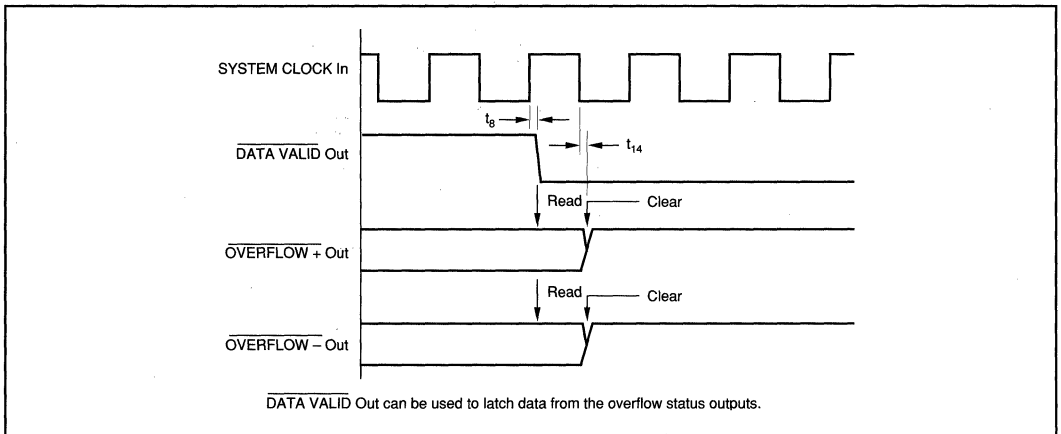
FIGURE 7. $\overline{\text{OVERFLOW}}$ Out Monitoring Timing Diagram.

FIGURE 8. System Clock Timing.

TYPICAL PERFORMANCE CURVES

ELECTRICAL

System Clock = 2MHz, V_S = ±5VDC, V_{REF} = −2.5V, L = 1 Integration/Conversion, and T_A = +25°C unless otherwise noted.

SINAD AT 10kHz CONVERSION, UNIPOLAR INPUT

100μs Integration Time
K = 16 Acquisition Clocks
M = 32 Oversamples

−60dB

0dB

THD + N (dB)

Input Frequency (Hz)

SINAD AT 1kHz CONVERSION, UNIPOLAR INPUT

1ms Integration Time
K = 16 Acquisition Clocks
M = 128 Oversamples

−60dB

0dB

THD + N (dB)

Input Frequency (Hz)

NOISE vs INPUT LEVEL (UNIPOLAR) WITH CDS

1ms Integration Time
K = 16 Acquisition Clocks
M = 128 Oversamples

C_{IN} = 500pF

C_{IN} = 100pF

C_{IN} = 0pF

Noise (ppm, rms)

Input Level of FS

NOISE vs INPUT LEVEL (UNIPOLAR) WITHOUT CDS

C_{IN} = 500pF

C_{IN} = 100pF

C_{IN} = 0pF

1ms Integration Time
M = 128 Oversamples

Noise (ppm, rms)

Input Level of FS

NOISE vs RESISTOR VALUE

Low Level, Unipolar Input
K = 16 Acquisition Clocks

1ms Int., M = 128 O/S

100μs Int., M = 16 O/S

Noise (ppm, rms)

R_{IN} (MΩ)

CHARGE INJECTION vs INPUT CAPACITANCE

No CDS

CDS On, K = 16

Charge Injection (ppm)

C_{IN} (pF)

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

TYPICAL PERFORMANCE CURVES (CONT)

ELECTRICAL

System Clock = 2MHz, $V_S = \pm5VDC$, $V_{REF} = -2.5V$, L = 1 Integration/Conversion, and $T_A = +25°C$ unless otherwise noted.

NOISE vs INPUT CAPACITANCE, UNIPOLAR INPUT

1ms Integration Time
M = 128 Oversamples

No CDS

CDS On, K = 16

NOISE vs OVERSAMPLING, UNIPOLAR INPUT

1ms Integration Time
K = 16 Acquisition Clocks
C_{IN} = 0pF

L = 1 Integration/Conversion

L = 128   L = 64
L = 256   L = 32   L = 16   L = 8   L = 4   L = 2

CHANGE IN I_B vs TEMPERATURE

NOISE vs TEMPERATURE, UNIPOLAR INPUT

1ms Integration Time
K = 16 Acquisition Clocks
M = 128 Oversamples

NOISE vs INTEGRATION TIME, UNIPOLAR INPUT

K = 16 Acquisition Clocks
C_{IN} = 0pF   M = 16 O/S

M = 64 O/S

M = 256 O/S

INPUT OFFSET VOLTAGE vs INPUT CAPACITANCE

TYPICAL PERFORMANCE CURVES (CONT)

ELECTRICAL

System Clock = 2MHz, V_S = ±5VDC, V_{REF} = −2.5V, L = 1 Integration/Conversion, and T_A = +25°C unless otherwise noted.

NEGATIVE PSRR vs FREQUENCY

1ms Integration Time
K = 16 Acquisition Clocks
M = 128 Oversamples

POSITIVE PSRR vs FREQUENCY

1ms Integration Time
K = 16 Acquisition Clocks
M = 128 Oversamples

NEGATIVE PSRR vs FREQUENCY

100µs Integration Time
K = 16 Acquisition Clocks
M = 32 Oversamples

POSITIVE PSRR vs FREQUENCY

100µs Integration Time
K = 16 Acquisition Clocks
M = 32 Oversamples

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A/D CONVERTERS, DATA ACQUISTION COMPONENTS

SECTION 5

DISCUSSION OF SPECIFICATIONS

INPUT

The DDC101 is a charge digitizing A/D converter. Low level current output sources, such as a photosensors, can be directly connected to its input. The input signal can also be a voltage connected through a user selected resistor.

CHARGE INPUT

The maximum charge that can be captured in one integration by the DDC101 is 500pC. In the unipolar input range mode, the maximum positive charge that can be collected in one integration is 500pC. The DDC101 has a small negative range in the unipolar mode of −1.95pC. This small negative underrange is included to allow for a small amount of leakage current from the user's PC board and sensor. In the bipolar input range, the maximum positive charge that can be collected is +250pC. The maximum negative charge that can be collected is −251.95pC.

In addition to the normal mode of one integration per conversion, DDC101 can be configured by the user for 1 to 256 integrations per conversion. When the multiple integrations per conversion mode is chosen, the DDC101 DSP circuitry internally averages multiple integration cycles to provide one conversion result. This result has lower noise because it is the average of multiple integrations. In this mode, the maximum total charge that can be captured by the DDC101 in 256 integrations is 128,000pC.

TEST CURRENT INPUT

An internal DC test current can be connected under user control to the DDC101's input. The test current is nominally 100nA and will be summed with any applied external input signal. It is derived by a resistive network from the positive power supply. The test current is intended to test for functionality only. The TEST In pin of the DDC101 controls the current. When TEST is HIGH, the internal current source is ON and current is flowing into the DDC101 input. When TEST is LOW, the current source is disconnected from the input. With TEST active, positive power supply current increases by approximately 1mA.

FULL SCALE RANGE

The full scale range (FSR), which is referenced in the specification table, is the difference between the positive full scale charge and the negative full scale charge for the DDC101 in one integration cycle. Specifications such as noise and linearity, which are specified in percent or ppm of FSR, are referring to a value of 500pC for both unipolar and bipolar input ranges.

The full scale input current for a given integration time will result in a full scale input charge. As an example for unipolar input range, an input current of 0.5μA integrated for 1ms will result in the full scale charge of 500pC. For voltage inputs, the input resistor is chosen to achieve the proper full scale input current. As an example, for a 5V full scale input, a 10MΩ input resistor is selected to achieve a full scale input current of 0.5μA (1ms integration time).

Noise of 1.6ppm of FSR is equal to 1.6ppm x 500pC = 0.8fC or 1.6ppm x 0.5μA = 0.8pA or 1.6ppm x 5V = 8μV. Thus, in this instance, noise is 1.6pA or 8μV.

For the unipolar input range, the following table shows the full scale input current required for different integration times to collect 500pC of charge and the equivalent current values for 2 and 5ppm of FSR.

T_{INT}	I_{FS}	2ppm	5ppm
50ms	10nA	0.02pA	0.5pA
5ms	100nA	0.2pA	1pA
1ms	500nA	1pA	2.5pA
500μs	1μA	2pA	5pA
100μs	5μA	10pA	25pA

TABLE I. Integration Time (T_{INT}) and Full Scale Current (I_{FS}) for Full Scale 500pC Integration.

CURRENT INPUT

The maximum average input current that can be captured by the DDC101 is ±7.8μA. This current will result in an integration time of 64μs for unipolar input range and 32μs for bipolar input range. For longer integration times, the average input current must be less.

The maximum input current is limited by the slew and update rate of the internal tracking logic and CDAC. The largest input current that the DDC101 can accurately track is 7.8μA. Input currents larger than 7.8μA and high speed current input pulses can be accurately captured and digitized by the DDC101 with an external input or sensor capacitance on the DDC101 input. The average current during a complete integration cycle cannot exceed 7.8μA. Likewise, the total charge input must not exceed 500pC unipolar, 250pC bipolar during the integration time.

An external user provided input capacitance, C_S, as shown in Figure 9a, will capture the input signal charge if the input current limit is temporarily exceeded during the integration cycle. The DDC101 will then transfer the charge completely to C_{INT} based upon conservation of charge. An additional
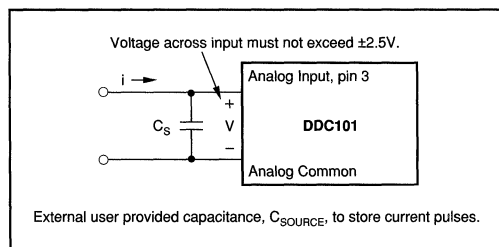
FIGURE 9a. Current Pulse Input Capture.

constraint is, the voltage that appears at the DDC101 input, must not exceed 2.5V. If this voltage is exceeded, charge may be lost and the integration result may be invalid. The input voltage can be calculated:

$$i(t) = C_S \frac{dv}{dt}$$

or

$$V = \frac{1}{C_S} \int i(t)dt$$

therefore,

$$V = i \frac{t}{C_S}.$$

As an example, with a user supplied input capacitance of 100pF, a current pulse of 100μA for 2μs could be stored without exceeding 2.5V applied to the input:

$$V = (100\mu A) \bullet \frac{2\mu s}{100pF} = 2V.$$

The current pulse must occur completely during part of one DDC101 integration time, and the DDC101 must still have time to discharge the input capacitance to ground at a maximum rate of 7.8μA before the DDC101 is triggered (through the FDS input) to end the integration. In addition, the total charge integrated must be 500pC or less for the unipolar range. A current pulse of 100μA for 2μs creates 200pC of charge.

VOLTAGE INPUT SPECIFICATIONS

The DDC101 is a charge digitizing device. With a user provided input resistor, the DDC101 can digitize voltage inputs. All of the general charge/current input specifications apply to the voltage input situation. The specification table shows the typical noise of the DDC101 including the effects of a 20MΩ input resistor, R_{IN}.

The input of the DDC101 is a virtual ground. A voltage input causes a current, i, to flow into the input through R_{IN} as shown in Figure 9b. The maximum input current is deter-

mined by the integration time selected. Table II shows the maximum input voltage based upon several selections of input current and input resistor for unipolar input range. The accuracy of the input resistor will add directly to the DC Gain Error of the DDC101; the drift of the input resistor will add directly to the Gain Drift of the DDC101.
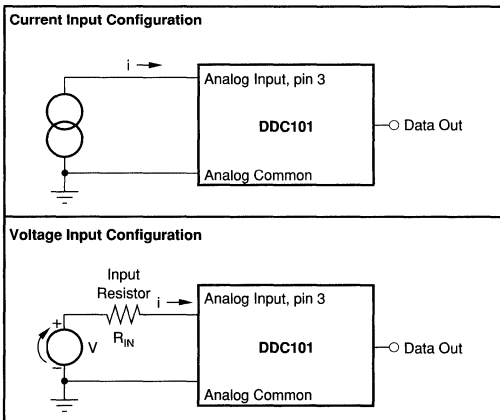
Note that the DDC101 output noise decreases as R_{IN} increases. This is because the DDC101 noise gain decreases and the input resistance current noise decreases as R_{IN} increases. This effect is shown in the "Noise vs Resistor Value" typical performance curve.

INTEGRATION TIME	INPUT RESISTOR, R_{IN}		
	1ms	500μs	100μs
Full Scale Input Current	0.5μA	1μA	5μA
Full Scale Voltage			
50mV	100kΩ	50kΩ	10kΩ
500mV	1MΩ	500kΩ	100kΩ
5V	10MΩ	5MΩ	1MΩ
50V	100MΩ	50MΩ	10MΩ

TABLE II. Example of Input Resistor Values Unipolar Input Range.

UNIPOLAR LINEARITY ERRORS

Due to innovative design techniques, the absolute level of linearity error of the DDC101 improves as the input signal level decreases when used in the unipolar input mode. Therefore, in unipolar input mode, the integral linearity of the DDC101 is specified as a small base error plus a percentage of reading error or as a percentage of full scale range. A best-fit straight line method is used to determine integral linearity. Two different best-fit straight lines are used for the two unipolar integral linearity specifications. For bipolar input mode, linearity is specified only as a percentage of full scale range.

To illustrate the improvement in unipolar mode linearity error, the graph below shows the maximum unipolar integral linearity error (ILE) of the DDC101 as a function of the input signal level. The maximum integral linearity error is ±0.0244% of reading ±2.5ppm of FSR. Thus, the maximum ILE for an input level of 1% of FSR is 0.0005%FSR.

Current Input Configuration

Voltage Input Configuration

FIGURE 9b. DDC101 Input Configurations.
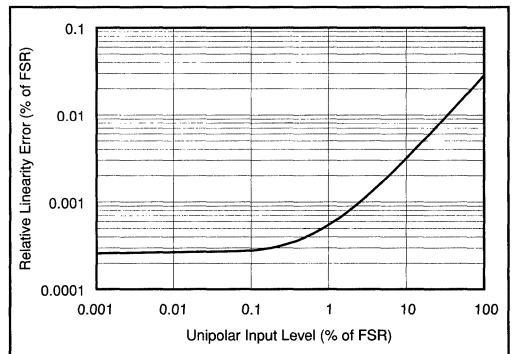
FIGURE 10. Maximum Unipolar Integral Linearity Error When Specified As a % of Reading.

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A/D CONVERTERS, DATA ACQUISITION COMPONENTS

NOISE

The noise of the DDC101 improves as the input signal level decreases, thus very low level signals can be resolved. Noise is shown in the specification table for low level inputs. For unipolar input range, the DDC101 noise at low level inputs is dominated by comparator noise gained to the output; at full scale inputs, the noise is dominated by D/A converter noise. The noise at low low level inputs is a function of input capacitance; the noise at full scale is relatively independent of input capacitance. For bipolar input operation, the noise is dominated by D/A converter noise and is higher than the full scale unipolar noise.

BIPOLAR INPUT ACCURACY

Linearity—As a bipolar input device, the linearity of the DDC101 is specified as a percentage of full scale range that does not improve with lower input signal levels. Performance is generally limited by the linearity of the unit when operated in the bipolar input mode.

Noise—In general, noise is not as important as linearity when determining total error. The output noise of the DDC101 in the bipolar mode peaks at midscale (zero input signal level). Output noise is lower for inputs above and below zero.

RESET CHARGE ERROR

The reset charge error (typically less than 250fC) is an offset error that could result from offset voltage, charge injection and kT/C errors. The DDC101 eliminates the effects of reset charge errors with correlated double sampling.

DC BIAS VOLTAGE

The DDC101 generates a small bias voltage (typically 500µV) at the input. This voltage is impressed on any sensor that is connected to the input. The DC bias voltage is the actual virtual ground voltage of the DDC101. The DDC101 input comparator circuitry includes an autozero circuit which eliminates this offset internally so that it does not produce an output error.

GAIN SENSITIVITY TO V_{REF}

The DDC101 gain is dependent upon the external reference voltage, V_{REF}. A change in the value of V_{REF} will be seen as a directly proportional change in the gain of the DDC101.

FREQUENCY RESPONSE

The DDC101 is a sampling system whose transfer function has three separate frequency components. These components are multiplied together to make the total frequency characteristic of the DDC101. The three components are:

1. Basic Integration
   This is the characteristic sin(x)/x response of the basic integration function. This response is controlled by the integration time of the DDC101.

2. Oversampling
   This is the low pass filter characteristic of the digital filter's oversampling. This response reduces the broadband noise in the input signal and the DDC101. Broadband noise decreases as the number of oversamples increases.

3. Multiple Integrations
   This is the low pass filter characteristic that results when the digital filter is used to average multiple integrations. This will determine the primary response of the DDC101 if two or more integrations are internally averaged.

See Section 6 for more details.

SECTION 6
DETAILED THEORY
OF OPERATION

INTEGRATION CYCLE

An integration cycle, as illustrated in Figure 11, includes the Acquisition Time, Initial Data Point Sampling, Tracking Interval, and Final Data Point Sampling. The Acquisition Time is K clock periods. The first clock cycle of the Acquisition Time is used to reset the integrating capacitor, C_{INT}, to zero from the previous integration. The balance of the Acquisition Time insures that the DDC101 system is accurately tracking the input signal prior to initial data point acquisition. Close-ups of the Reset and Acquisition time are shown in Figures 12 and 13.

The Initial Data Point is then sampled M times. The Integration cycle time consists primarily of the Tracking Interval during which time the DDC101 "tracks" the integration of the input signal. The Tracking Interval is followed by the measurement of the Final Data Point with the same user selected number of samples, M. M and K are user selectable. The entire integration cycle consists of N clock periods as controlled by the user.

The DDC101 operates in continuous and non-continuous integration modes. In the continuous mode, one integration follows another with no delay from the end of one integration to the beginning of the next conversion. In the non-continuous mode, each new integration is started separately under user control.

The Final Data point Start (FDS) input is the primary user control of the integration cycle. The FDS input controls the end of one integration cycle and the start of the next integration cycle in both the continuous and non-continuous integration modes. Measurement of the M final data point samples begins when the FDS input is activated.

CONTINUOUS INTEGRATION MODE

In the continuous integration mode, the "Final Data Point Start" command (using the FDS pin) initiates the measurement of the M final data point samples. The next integration cycle begins immediately after the final data point sampling
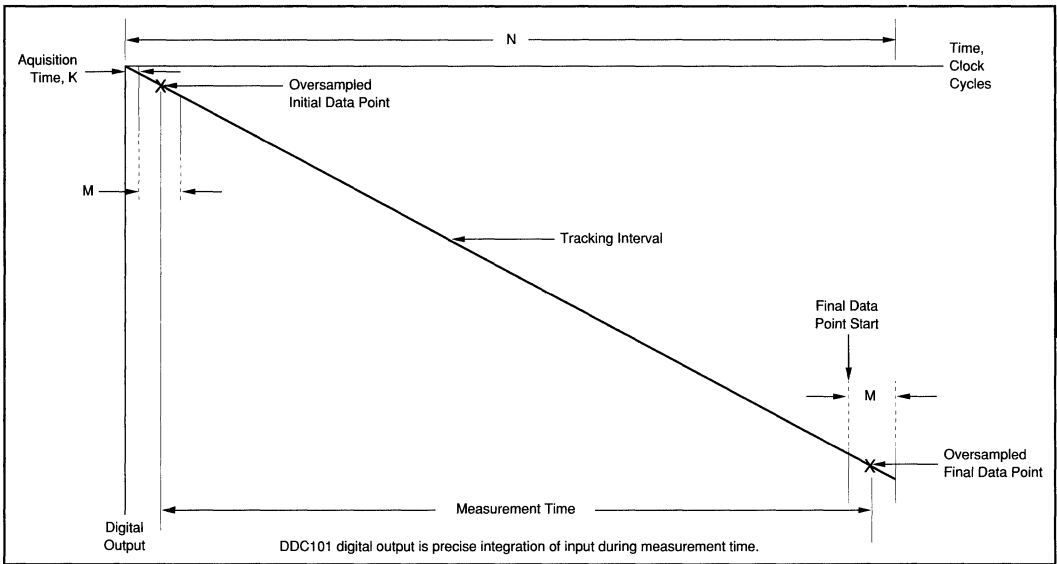
FIGURE 11. Equivalent Integrator Output for Single Integration.
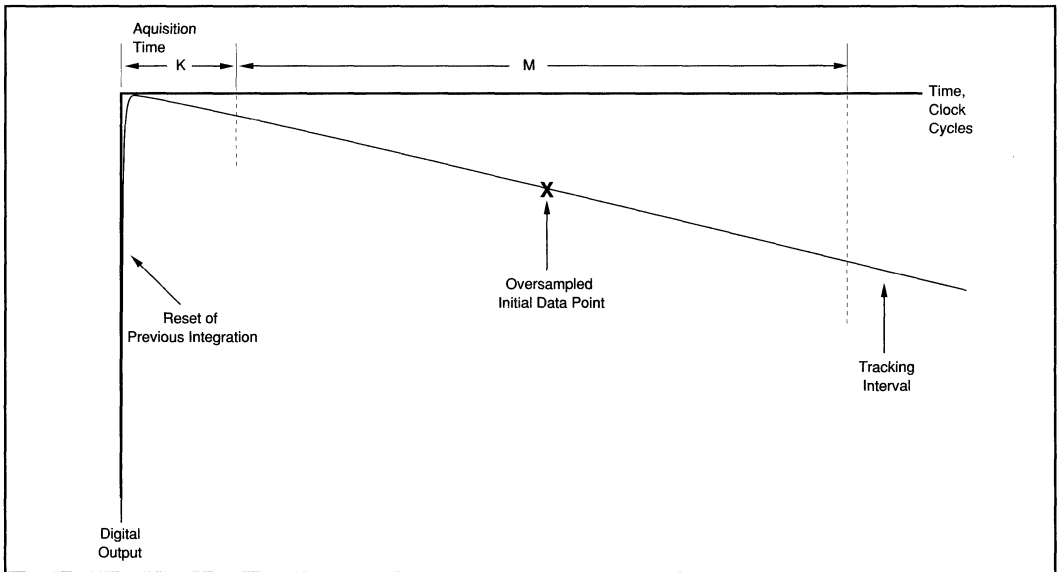
FIGURE 12. Close-up of Initial Oversampled Data Point for DDC101.

has been completed; this occurs M clock periods after the FDS transition to "ON". Acquisition, Initial Data Point and Tracking for the next integration follow automatically. The DDC101 continues in the Tracking mode until the next FDS command initiates the measurement of the M final data point samples. An FDS command is needed for each integration cycle. In the continuous integration mode, the FDS pulse width must be less than M clock periods. If the FDS pulse is held low past this time of M clock periods, the DDC101 will reset as for non-continuous mode (see also Figure 4).

In the continuous mode of operation, the tracking logic of the DDC101 "remembers" the integration rate of the previous integration and begins the next integration at the rate of the previous integration. This allows faster acquisition of the signal for the next integration.

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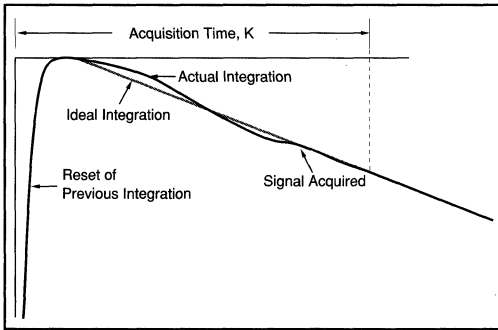
FIGURE 13. Close-up of Reset and Acquisition Time for DDC101.
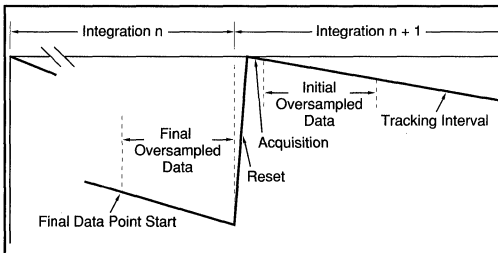
FIGURE 14. Close-up of End of One Integration Cycle and Beginning of Next.

NON-CONTINUOUS INTEGRATION MODE

For the non-continuous integration mode, FDS controls the start of the M final data point samples and the end of integration as discussed above. In this mode, however, FDS is also used to control the start of a new integration cycle asynchronously with the end of the previous integration. When FDS transitions to "ON", the collection of the M final data point samples begins. At the end of each integration, the DDC101 automatically resets the integration capacitance. If FDS remains "ON" past the end of integration, the DDC101 will stay in the integration reset state until FDS transitions to "OFF". Holding FDS "ON" past the end of integration will also reset the DDC101's tracking logic to zero integration rate.

In non-continuous integration mode, the initial data point measurement may be less accurate since the DDC101's internal tracking logic is reset at the beginning of the integration and tracking may not be accurate for the initial data point measurement. In this situation, Correlated Double Sampling (CDS) operation may not be advantageous.

INTERNAL ERROR CORRECTION

The DDC101 uses CDS techniques to gain optimum performance. CDS removes internal DDC101 errors which occur for a given integration cycle such as, charge injection, kT/C, and DDC101 offset errors. Correlated Double Sampling is user selectable. It is recommended for most continuous measurement applications.

Correlated Double Sampling is implemented in the DDC101 by subtracting the Initial Data Point from the Final Data Point. Thus, the error correction is updated automatically for each integration. When operating in the unipolar input range, CDS functions with either output data format—straight binary or binary two's complement. When operating in the bipolar input range, CDS functions with binary two's complement output data format only.

The errors that CDS removes are charge injection, kT/C and DDC101 input voltage offset. These errors are very difficult to eliminate in equivalent analog circuits. Charge injection errors result from charge that is transferred through the reset switch into the integration capacitor. kT/C errors are switching errors due to the noise of the resistance of the reset switch. DDC101 voltage offset errors are due to input offset of the input comparator. Both initial offset and offset drift with time and temperature are corrected since the correction is performed each integration cycle.

SINGLE CYCLE INTEGRATION

The DDC101 acquires charge (q) by integrating input current (i) for a specific time (T). That is,

$$q = \int_0^T i \, dt$$

The DDC101 acquires up to 500pC of full scale charge per integration cycle in the unipolar input range, and approximately ±250pC of full scale charge in the bipolar input range. Therefore, for the DDC101, maximum values can be calculated.

Unipolar Input Range	Bipolar Input Range
$500pC = I_{FS} \times T_{INT}$	$\pm250pC = \pm I_{FS} \times T_{INT}$

Where I_{FS} is the full scale input current and T_{INT} is the integration time of the DDC101. Examples of I_{FS} and T_{INT} that equal 500pC and ±250pC are shown in the following tables.

The maximum average input current that the DDC101 can integrate is 7.8µA. This results in a minimum integration time of 64µs for unipolar inputs and 32µs for bipolar inputs. Further flexibility is possible with multiple integration cycles per conversion as described in the following text.

INPUT RANGE

Unipolar Input Range

For the unipolar input range, the range of charge for each integration cycle is from positive full scale of +500pC to a slightly negative charge of –1/256 (approximately –0.4%) of the positive full scale charge. This is +500pC to –1.95pC. The negative charge measurement capability allows for low level PC board parasitic leakages.

Bipolar Input Range

For the bipolar input range, the range of charge for each integration cycle is from positive full scale of +250pC to negative full scale of –251.95pC.

I_{FS}	T_{INT}
1nA	500ms
10nA	50ms
100nA	5ms
1μA	500μs
5μA	100μs
7.8μA	64μs

TABLE III. Input Current vs Integration Time Examples for Maximum Charge. Unipolar input range maximum charge = 500pC.

$\pm I_{FS}$	T_{INT}
1nA	250ms
10nA	25ms
100nA	2.5ms
1μA	250μs
2.5μA	100μs
7.8μA	32μs

TABLE IV. Input Current vs Integration Time Examples for Maximum Charge. Bipolar input range maximum charge = ±250pC.

MULTIPLE INTEGRATIONS PER CONVERSION CYCLE

If more than 500pC, unipolar (or ±250pC, bipolar) of charge must be integrated in one conversion cycle, the DDC101 can be user programmed for multiple integrations per conversion cycle. This feature can be used to provide for longer conversion periods for a specific input current other than shown in the previous table. The integration cycles forming a conversion cycle may be continuous or non-continuous. The number of integrations per conversion cycle, L, can be 1, 2, 4, 8, 16, 32, 64, 128, or 256. The multiple integrations are automatically averaged in the DDC101 so that one conversion result is output per total conversion cycle.

FINAL DATA POINT CONFIGURATION LIMITS

In each conversion cycle, the maximum number of final data points which can be collected is 256. This means that at the extremes, the DDC101 can be setup to perform one integration cycle with 256 oversamples, or the DDC101 can be setup to perform 256 integration cycles with one sample per integration cycle. The total number of integrations, L, multiplied by the number of samples per final data point, must be 256 or less. As an example, if 16 integration cycles, L, are used, the number of samples per final data point must be 16 or less.

NOTE: When CDS is used, the initial data points impose no additional conversion sampling limitations.

FREQUENCY RESPONSE

The DDC101 charge digitizing A/D Converter is a sampled system whose frequency response has three separate components. These components are multiplied together to make the total frequency characteristic of the DDC101. The three frequency response components are shown below. Each individual component has a sinc (sinx/x) frequency response function.
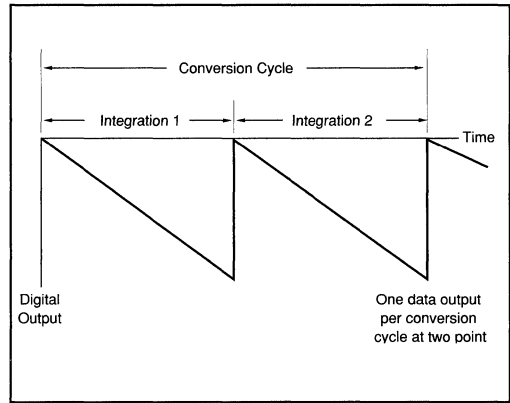
FIGURE 15. Conversion Cycle with Two Integrations.

INTEGRATIONS PER CONVERSION	I_{FS}	CONVERSION TIME	TOTAL CHARGE
1	10nA	50ms	500pC
2	10nA	100ms	1000pC
4	10nA	200ms	2000pC
8	10nA	400ms	4000pC
16	10nA	800ms	8000pC
32	10nA	1.6s	16000pC
64	10nA	3.2s	32000pC
128	10nA	6.4s	64000pC
256	10nA	12.8s	128000pC

TABLE V. Integrations/Conversion vs Conversion Time. Example for multiple integrations with unipolar input range.

1. Basic Integration
   This is the characteristic sin(x)/x response of the basic integration function. This response is controlled by the measurement time of the DDC101, T_{MEAS}; see Figure 16.

2. Oversampling
   This is the low pass filter characteristic of the digital filter's oversampling. This response reduces the broadband noise in the input signal of the DDC101. Broadband noise decreases as the number of oversamples increases. This response is controlled by the number of oversamples, M; see Figure 17.

3. Multiple Integrations
   This is the low pass filter characteristic that results when the digital filter is used to average multiple integrations. This will determine the primary response of the DDC101 if two or more integrations are internally averaged. This response is controlled by the total conversion time of the DDC101; see Figure 18.

Input frequencies are multiplied by the DDC101 frequency response. The Nyquist frequency is $f_{CONV}/2$, where f_{CONV} is the DDC101 conversion rate. The highest frequency that can be reconstructed from the output data is $f_{CONV}/2$. Input frequencies above Nyquist are multiplied by the DDC101 frequency response and are then aliased into DC to $f_{CONV}/2$.

DDC101

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A/D CONVERTERS, DATA ACQUISTION COMPONENTS

Basic Integration Frequency Response

The sin(x)/x basic integration characteristic is controlled by the digital filter's measurement time (T_{MEAS}). The measurement frequency, f_{MEAS} is $1/T_{MEAS}$. The input frequency response of the DDC101 is down –3dB at $f_{MEAS}/2.26$ with a null at f_{MEAS}. Subsequent nulls are at harmonics $2f_{MEAS}$, $3f_{MEAS}$, $4f_{MEAS}$, etc. as shown in the frequency response curve below. This characteristic is often used to eliminate known interference by setting f_{MEAS} or a harmonic to exactly the frequency of the interference. Table VI illustrates the frequency characteristics of the DDC101 integration function for various measurement times. As an example, for N = 2272, K = 16, and M = 256: T_{MEAS} = (N-M-K)/f_{CLK} = (2272-256-16)/2MHz = 1ms and f_{MEAS} = 1kHz. T_{INT} = 2272/2MHz = 1.14ms; f_{CONV} = $1/T_{INT}$ = 880Hz.

FIGURE 16. Basic Integration Frequency Response.

MEASUREMENT TIME	–3dB FREQUENCY	f_{MEAS}
100µs	4.42kHz	10kHz
1ms	442Hz	1kHz
10ms	44.2Hz	100Hz
16.66ms	26.5Hz	60Hz
20ms	22.1Hz	50Hz

TABLE VI. Basic Integration Frequency Response Examples.

Oversampling Frequency Response

The M oversamples of the initial and the final data points create an oversampling sin(x)/x type of low pass filter response. The oversampling function reduces broadband noise of the input signal and the DDC101. Broadband noise is reduced approximately in proportion to the square root of the number of oversamples, M. As an example, a conversion with 128 oversamples will have approximately 1/2 the noise of a conversion with 32 oversamples ($\sqrt{32/128} = \sqrt{1/4}$ = 1/2) The oversampling low pass filter response creates a null

at $f_{OS} = 1/T_{OS}$. The oversample time, T_{OS}, is M/f_{CLK}. For M = 256 and f_{CLK} = 2MHz, f_{OS} is approximately 7.8kHz. Subsequent nulls are at harmonics $2f_{OS}$, $3f_{OS}$, $4f_{OS}$, etc. The –3dB point is at $f_{OS}/2.26$. Table VII illustrates the DDC101 oversampling frequency characteristics with approximate values for f_{OS} and the –3dB frequency. An oversampling frequency response graph is shown below in Figure 17. This figure shows the frequency response for M = 256 oversamples with an f_{CLK} of 2MHz . The slope of the attenuation curve decreases at approximately 20dB/decade.

OVERSAMPLES (M)	–3dB FREQUENCY	f_{OS}
256	3.5kHz	7.8kHz
128	6.9kHz	15.6kHz
64	13.9kHz	31.2kHz
16	55kHz	125kHz

TABLE VII. Oversample Frequency Response Examples.

Normalized DDC101 Frequency Response

The normalized frequency response, H(f), of the DDC101 that is applied to the input signal consists of the product of the three frequency response components:

$$H(f) = \underbrace{\frac{\sin\left(\pi f(N-M-K)/f_{CLK}\right)}{\pi f(N-M-K)/f_{CLK}}}_{\text{Basic Integration}} \bullet \underbrace{\frac{\sin\left(\pi fM/f_{CLK}\right)}{M\sin\left(\pi f/f_{CLK}\right)}}_{\text{Oversampling}} \bullet \underbrace{\frac{\sin\left(\pi fLN/f_{CLK}\right)}{L\sin\left(\pi fN/f_{CLK}\right)}}_{\text{Multiple Integrations}} \bullet \underbrace{e^{-j\pi f(LN-K-1)/f_{CLK}}}_{\text{Linear Phase}}$$

Where:

f	is the signal frequency
f_{CLK}	is the system clock frequency, typically 2MHz
N	is the total number of clock periods in each integration time, T_{INT} = N/f_{CLK}, T_{INT} is the DDC101 CDAC's integration time
M	is the number of oversamples in one oversampled data point
K	is the number of clocks used in the acquisition time
(N-M-K)/f_{CLK}	is the digital filters measurement time, T_{MEAS}, (T_{MEAS} = T_{INT} –(M+K)/f_{CLK})
M/f_{CLK}	is the oversample time, T_{OS}
LN/f_{CLK}	is the total conversion time for multiple integrations, T_{CONV}

The DDC101's transfer response has a linear phase characteristic as indicated by the exponential term.
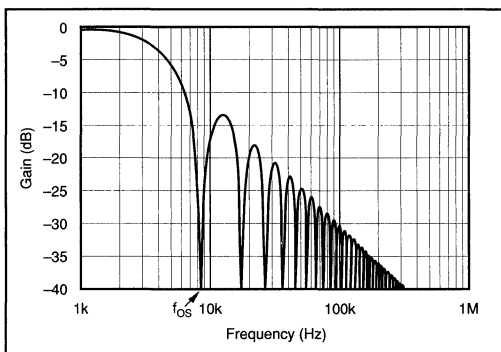
FIGURE 17. Oversampling Frequency Response for M = 256 (f_{CLK} = 2MHz).
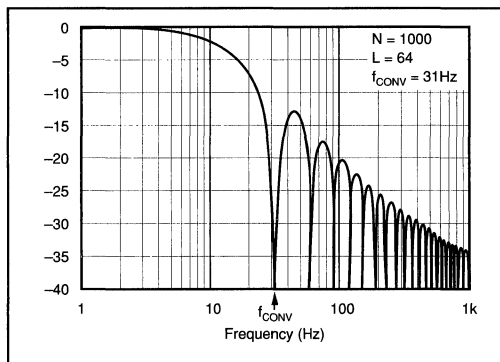
Multiple Integration Frequency Response

If the DDC101 is operated in the multiple integrations per conversion mode of operation, an additional sin(x)/x type low pass filter is created. The filter creates an initial null frequency at the conversion frequency, f_{CONV} of the DDC101 and at multiples of f_{CONV}. The –3dB point for this filter is also at $f_{CONV}/2.26$. The conversion time, T_{CONV}, is the sum of the integration times for multiple integrations that are averaged together by the DDC101. $T_{CONV} = LN/f_{CLK}$. $f_{CONV} = 1/T_{CONV}$. If multiple integrations per conversion are used, this filter will be the dominant low frequency filter of the DDC101. Table VIII shows examples of the conversion time and frequency for different parameter selections. Figure 18 shows an example of the frequency response due to Multiple Integrations. In the case of Figure 18, the integration time is 500μs (N = 1000 clock periods) and L = 64 integrations per conversion.

INTEGRATION TIME	L	CONVERSION TIME	–3dB FREQUENCY	f_{CONV}
1ms	2	2ms	221Hz	500Hz
1ms	8	8ms	55Hz	125Hz
1ms	16	16ms	27.5Hz	62.5Hz
1ms	64	64ms	6.9Hz	15.6Hz
1ms	256	256ms	1.73Hz	3.91Hz
10ms	2	20ms	22.1Hz	50.0Hz
10ms	8	80ms	5.5Hz	12.5Hz
10ms	16	160ms	2.75Hz	6.25Hz
10ms	64	640ms	0.69Hz	1.56Hz
10ms	256	2560ms	0.173Hz	0.39Hz

TABLE VIII. Multiple Integration Time Examples.

System Noise implications

The noise at the digital output of the DDC101 consists of system noise that is included in the analog input signal and noise from the DDC101.

DDC101 Noise—The noise of the DDC101 includes low frequency and broadband noise. The low frequency noise is reduced by the integrating function and the CDS function of the DDC101. This is reflected in the basic integration frequency response and in the multiple integration frequency response. The broadband electronic noise is reduced primarily by the oversampling function of the DDC101

FIGURE 18. A Multiple Integration Frequency Response Example.

Signal Noise—The noise of the input signal is filtered and reduced in a manner similar to the DDC101 noise reduction through the integrating and oversampling functions of the DDC101.

Figures 19 and 20 show the frequency response of the DDC101 for the product of the basic integration and oversampling frequency response for two different values of M. In both examples, the integration time is 1ms, the only difference is in the number of oversamples, M; for Figure 19, M = 256 oversamples was used; for Figure 20, M = 32 oversamples was used. The first null frequency is f_{MEAS} and subsequent nulls are at multiples of f_{MEAS}. The first example with the larger number of oversamples (M = 256) clearly reduces high frequency noise more than the second example with M = 32.

For M = 256, f_{OS} is 7.8kHz, f_{MEAS} is 1.16kHz, and the –3dB frequency is 507Hz. For M = 32, f_{OS} is 62.4kHz, f_{MEAS} is 1.02kHz and the –3dB frequency is 453Hz.
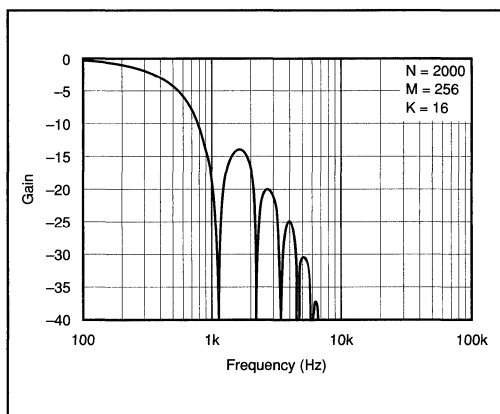
FIGURE 19. Product of Frequency Response of Basic Integration and Oversampling: 1ms Integration Time, 256 Oversamples.

DDC101

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A/D CONVERTERS, DATA ACQUISTION COMPONENTS
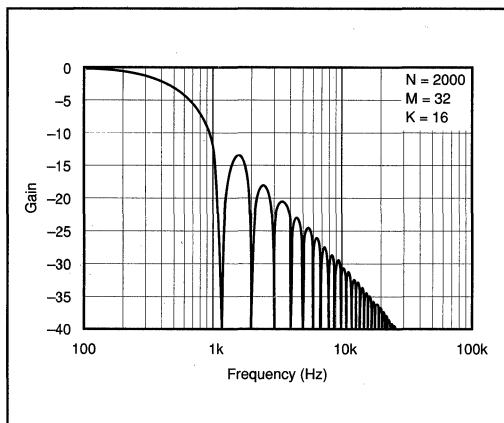
FIGURE 20. Product of Frequency Response of Basic Integration and Oversampling; 1ms Integration Time, 32 Oversamples.

Figure 21 shows the frequency response of the DDC101 and an ideal integrator with the same integration time. In this comparison, the DDC101 has greater bandwidth to the first null, but it also has greater out of band attenuation which reduces broadband noise significantly. If desired, the frequency response of the ideal integrator can be produced by passing the DDC101 output through an external digital filtering function which has the frequency response from DC to Nyquist of

$$\frac{\sin(\pi f T_{INT})}{\pi f T_{INT}} \cdot \frac{\pi f T_{MEAS}}{\sin(\pi f T_{MEAS})} \cdot \frac{M \sin(\pi f / f_{CLK})}{\sin(\pi f M / f_{CLK})} \ .$$

This has the effect of further attenuating undesired signals (noise) outside the "passband", further increasing the signal-to-noise ratio of the DDC101 and closely emulating the ideal integrator's signal accumulation characteristics.
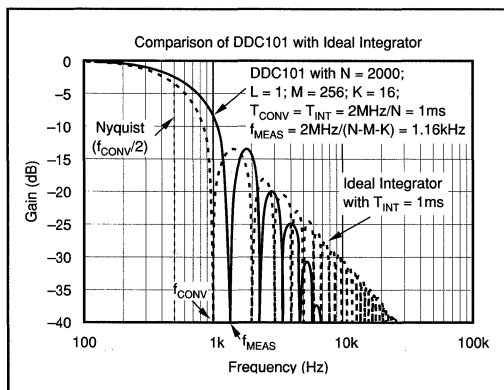
FIGURE 21. Comparison of DDC101 with Ideal Integrator.

SYSTEM SETUP

After power up, the Reset System and FDS signal inputs should be held low (active), while the SETUP register is loaded by the user. After the SETUP register is loaded, the Reset System input should transition to inactive while the FDS input remains active. The FDS should transition to inactive at the start of operation. Thereafter, Reset System should stay inactive and the FDS should be used to control each integration cycle.

SETUP INPUT

Software Control

Many of the options of the DDC101 are set through a serial bit stream transmitted by the user into the SETUP Input pin. The 12-bit word transmitted into the SETUP Input is used to set the following four options, in sequence:

1. Acquisition Time Control, K	2 bits	
2. Oversampling Control Samples/Integration, M	4 bits	
3. Multiple Integration Control Integrations/Conversion, L	4 bits	
4. Unipolar or Bipolar Input Range	1 bit	
5. Output Format	1 bit	
Total for SETUP	12 bits	

See Figure 5: SETUP Timing Diagram.

Acquisition Time Control, K

This signal sets the acquisition time (K clock periods) and controls the use of Correlated Double Sampling. The acquisition time occurs at the start of each new integration. The acquisition time control can be set to four options: "no CDS", 1, 16 or 32 clock periods. For typical continuous integration applications, K = 16 is recommended. The acquisition time always begins with one clock period for reset. This reset clock period is followed by 0, 15 or 31 clock periods for signal acquisition. Correlated Double Sampling is activated if the initial acquisition time is set to 1, 16 or 32 clock periods. Correlated Double Sampling is disabled and the Initial Data Point is not acquired if "no CDS" is selected.

K	RESET CLOCKS	ACQUISITION CLOCKS	CDS
"No CDS"	1	0	Disabled
1	1	0	Enabled
16	1	15	Enabled
32	1	31	Enabled

TABLE IX. Acquisition Time Control, K.

When Correlated Double Sampling is activated, the DDC101 acquires the initial data point for error correction as part of each conversion. At the end of the conversion cycle, the initial data point is subtracted from the final data point. The errors that are corrected with CDS are charge injection, kT/C noise, and DDC101 voltage offset. When Correlated Double Sampling is deactivated, the initial data point is not taken.

When operating in the unipolar input range, CDS functions with either output data format—straight binary or binary two's complement. When operating in the bipolar input range, CDS functions correctly only with binary two's complement output data format.

Oversampling Control
Samples/Integration, M

This control sets the number of samples, M, used by the DDC101 to oversample the initial and final data points. M can be set for these values: 1, 2, 4, 8, 16, 32, 64, 128, 256. Broadband noise in the conversion is reduced roughly in proportion to the square root of M. Therefore, a conversion with 128 oversamples will have 1/2 the broadband noise of a conversion with 32 oversamples. See the previous frequency response discussion.

Multiple Integration Control, L

This control sets the number of integrations per conversion cycle, L. It is used to reduce the data rate, increase the magnitude of the input signal range, and/or reduce the noise. The product of L and M must be 256 or less.

Output Format

Two output formats are available for either the unipolar or bipolar input ranges:

Binary Two's Complement (BTC) and Straight Binary.

UNIPOLAR INPUT RANGE

For Binary Two's Complement, output data format, the output word is a 21-bit Two's Complement word. The first bit is the sign bit followed by the Most Significant Bit (MSB), etc. The output range is +100%FS to –0.4%FS, where FS is 500pC.

CODE	INPUT SIGNAL	
0 1111 1111 1111 1111 1111	+100%FS	+500pC
0 1111 1111 1111 1111 1110	+100%FS –1LSB	
0 0000 0000 0000 0000 0001	+1SLB	
0 0000 0000 0000 0000 0000	Zero	0pC
1 1111 1111 1111 1111 1111	–1LSB	
1 1111 1111 0000 0000 0000	–0.4%FS	–1.95pC

TABLE X. BTC Code Table—Unipolar Input Range.

For Straight Binary output data format, the output is a 20-bit straight binary word. The first bit is the Most Significant Bit (MSB), etc. The output range is +99.6%FS to –0.4%FS in which +99.6%FS represents positive full scale and –0.4%FS represents the minimum input.

CODE	INPUT SIGNAL	
1111 1111 1111 1111 1111	+99.6%FS	498.05pC
1111 1111 1111 1111 1110	+99.6%FS –1LSB	
0000 0001 0000 0000 0001	+1LSB	
0000 0001 0000 0000 0000	Zero	
0000 0000 0000 0000 0000	–0.4%FS	–1.95pC

TABLE XI. Straight Binary Code Table — Unipolar Input Range.

BIPOLAR INPUT RANGE

For Binary Two's Complement, output data format, the output word is a 21-bit Two's Complement word. The first bit is the sign bit followed by the Most Significant Bit (MSB), etc. The output range is +100%FS to –100.8%FS, where FS is 250pC. For the bipolar input range, the output code table changes with the use of Correlated Double Sampling (CDS). (There is no difference with or without CDS in the output code table when using the unipolar input range.)

CODE	INPUT SIGNAL	
0 1111 1111 1111 1111 1111	+100%FS	+250pC
0 1111 1111 1111 1111 1110	+100%FS –1LSB	
0 1000 0000 0000 0000 0001	+1LSB	
0 1000 0000 0000 0000 0000	Zero	0pC
0 0111 1111 1111 1111 1111	–1LSB	
0 0000 0000 0000 0000 0001	–100%FS + 1SLB	
0 0000 0000 0000 0000 0000	–100%FS	–250pC
1 1111 1111 0000 0000 0000	–100.8%FS	–251.95pC

TABLE XII. BTC Code Table — Bipolar Input Range without CDS.

CODE	INPUT SIGNAL	
0 0111 1111 1111 1111 1111	+100%FS	+250pC
0 0111 1111 1111 1111 1110	+100%FS – 1LSB	
0 0000 0000 0000 0000 0001	+1LSB	
0 0000 0000 0000 0000 0000	Zero	0pC
1 1111 1111 1111 1111 1111	–1LSB	
1 1000 0000 0000 0000 0001	–100%FS + 1LSB	
1 1000 0000 0000 0000 0000	–100%FS	–250pC
1 0111 1111 0000 0000 0000	–100.8%FS	–251.95pC

TABLE XIII. BTC Code Table — Bipolar Input Range with CDS.

For Straight Binary output data format with the bipolar input range, the output is a 20-bit straight binary word. The first bit is the Most Significant Bit (MSB), etc. The output range is +100%FS to –100%FS in which +100%FS represents positive full scale and –100%FS represents the negative full scale. *When using the straight binary output data format in bipolar input range, do not use CDS. This will cause a negative overflow to occur.*

CODE	INPUT SIGNAL	
1111 1111 1111 1111 1111	+100%FS	+250pC
1111 1111 1111 1111 1110	+100%FS – 1LSB	
1000 0000 0000 0000 0001	+1LSB	
1000 0000 0000 0000 0000	Zero	0pC
0111 1111 1111 1111 1111	–1LSB	
0000 0000 0000 0000 0000	–100%FS	–250pC

TABLE XIV. Straight Binary Code Table — Bipolar Input Range without CDS.

SETUP INPUT CODE
Acquisition Time Control—K - 2 bits

CODE	RESULT
00	1 Reset clock period, 0 clock period Acquisition Time, CDS disabled, no initial data point,
01	1 Reset clock period, 0 clock period Acquisition Time
10[1]	1 Reset clock period, 15 clock period Acquisition Time
11	1 Reset clock period, 31 clock period Acquisition Time

NOTE: (1) Recommended for continuous integration mode.

Right margin: DDC101 — 2 — A/D CONVERTERS, DATA ACQUISTION COMPONENTS

Oversampling Control
Samples/Integration—M - 4 bits

CODE	SAMPLES PER INTEGRATION
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1XXX	256

Multiple Integration Control
Integrations/Conversion—L - 4 bits

CODE	INTEGRATIONS PER CONVERSION
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1XXX	256

Input Range - 1 bit

CODE	INPUT RANGE
0	Unipolar
1	Bipolar

Output Format - 1 bit

CODE	OUTPUT FORMAT
1	Binary Two's Complement
0	Straight Binary

SECTION 7
APPLICATIONS INFORMATION

BASIC PRINTED CIRCUIT BOARD LAYOUT

As with any precision circuit, careful printed circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pin. Digital signals should be kept as far from the analog input signals as possible on the PC board.

Leakage currents between PC board traces can exceed the input bias current of the DDC101 if care is not taken. A circuit board "guard" pattern for the analog input pin and for the PC board trace that connects to the analog input pin is recommended. The guard pattern reduces leakage effects by surrounding the analog input pin and trace with a low impedance analog ground. Leakage currents from other portions of the circuit will flow harmlessly to the low impedance analog ground rather than into the analog input of the DDC101. Analog ground pins are placed on either side of the analog input pin in the DDC101 package to allow convenient layout of guard patterns. Figure 22 illustrates the use of guard patterns to protect the analog input.
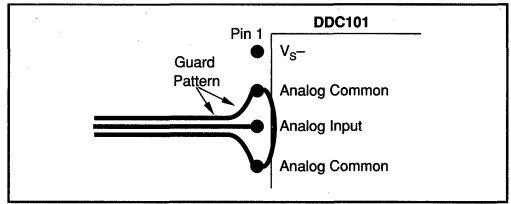
FIGURE 22. PC Board Layout Showing "Guard" Traces Surrounding Analog Input Pin and Traces.

Power Supplies

The ±5VDC supplies of the DDC101 should be bypassed with 10μF solid tantalum capacitors and 0.1μF ceramic capacitors. The supplies should each have a 10μF solid tantalum capacitor at a central point on the PC board. Each of the DDC101 power supply lines (V_S+, V_S-, $V_{DD}+$) should have a separate 0.1μF ceramic capacitor placed as close to the DDC101 package as possible.

The digital power supply voltage, $V_{DD}+$ must be equal to or less than the analog power supply voltage, V_S+. The analog power supply, V_S+, is connected to pins 5 and 6, these pins should be hardwired together on the printed circuit board at the pins for best performance.

$V_{DD}+$ should be as quiet as possible with minimal noise coupling. It is particularly important to eliminate noise from $V_{DD}+$ that is non-synchronous with DDC101 operation. Figure 23 illustrates two acceptable ways to supply $V_{DD}+$ power to the DDC101. The first case shows two separate +5VDC supplies for $V_{DD}+$ and V_S+. The second case shows the $V_{DD}+$ power supply derived from the V_S+ supply as used on the DDC101 Evaluation Fixture Device Under Test (DUT) board.
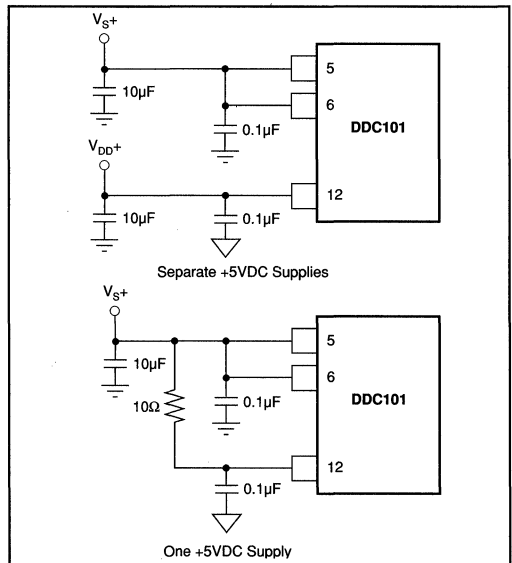
FIGURE 23. Positive Supply Connection Options.
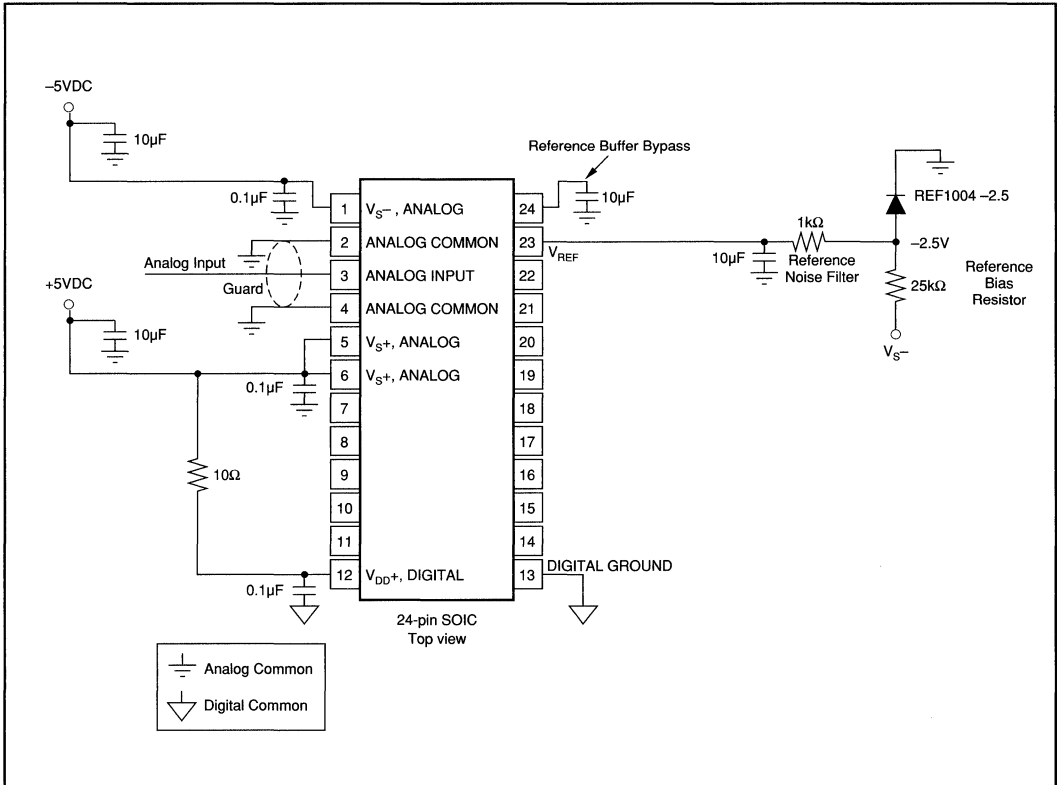
FIGURE 24. Example of Basic DDC101 Circuit Connections, SOIC Package.

Reading Data Output

Data from the previous conversion can be read any time after the $\overline{\text{DATA VALID}}$ output is activated and before the end of the next conversion. Data is held in an internal serial shift register until the end of the next conversion. The data must be completely read before the end of the next conversion or it will be overwritten with new data.

Recommended Setup

The following Setup parameters are recommended, in general, for use with the DDC101 with integration times of 1ms or longer. Multiple integrations per conversion, where practical, will provide lowest noise as illustrated in the typical performance curves.

Measurement Time Calculation

FUNCTION	RECOMMENDED
Acquisition Clocks, K	16
Oversamples, M	128
CDS	Enabled

A Continuous Integration Cycle consists of the Acquisition Time, Initial Data Point Collection, Tracking Interval, and Final Data Point Collection. The user can select these functions as illustrated in Table XV.

The time between "Final Data point Start" commands is the Integration Time, T_{INT}. The Measurement Time, T_{MEAS}, is the Integration time reduced by the Acquisition Time and by the Oversampling Time, T_{OS}.

$$T_{MEAS} = T_{INT} - T_{ACQ} - T_{OS}.$$

When CDS is used; T_{OS}, the oversampling time, is the time required to collect a data point (M clock periods). Each group of samples is averaged with the result at the midpoint of each sample group. Therefore, with CDS, $T_{OS} = M$ clock periods. This is shown in Figure 25.

Two calculations of the Measurement Time are shown

FUNCTION	CLOCK CYCLES	USER CONTROLLED
Acquisition Time, K	1, 16, 32	Yes
Initial Data Point Samples, M[1]	1, 2, 4, 8, 16, 32, 64, 128, 256	Yes
Tracking Interval	Variable	Yes
Final Data Point Samples, M[1]	1, 2, 4, 8, 16, 32, 64, 128, 256	Yes

NOTE: (1) Will be the same in CDS mode, initial Data Point Samples = 0 in non-CDS mode.

TABLE XV. Components of Integration Cycle.

DDC101

2

A/D CONVERTERS, DATA ACQUISTION COMPONENTS
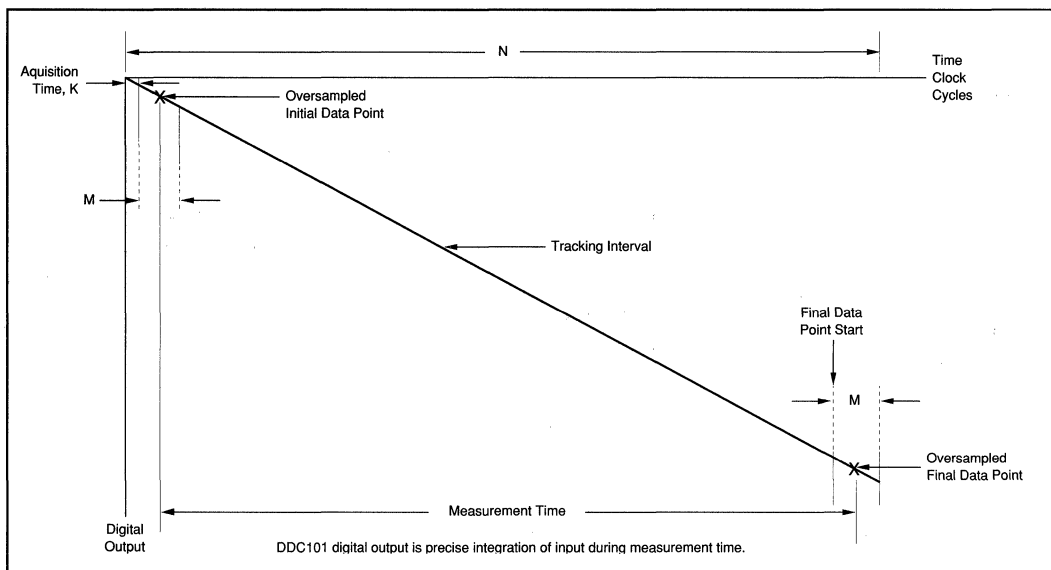
FIGURE 25. DDC101 Equivalent Integrator Output for Single Integration with CDS.

FUNCTION	USER SETTING (Clock Cycles)	TIME	MEASUREMENT (Calculated)
Integration Time (T_{INT})		1ms	
Acquisition Time K (T_{ACQ})	16	8µs	
Initial Data Point Samples, M	128	64µs	
Measurement Time			928µs
Final Data Point Samples, M	128	64µs	

TABLE XVI. Measurement Time with CDS.

FUNCTION	USER SETTING (Clock Cycles)	TIME	MEASUREMENT (Calculated)
Integration Time (T_{INT})		1ms	
Acquisition Time, K (T_{ACQ}) "No CDS"	1	0.5µs	
Initial Data Point Samples	None	0µs	
Measurement Time			967.5µs
Final Data Point Samples, M	128	64µs	

TABLE XVII. Measurement Time without CDS.

below: one with Correlated Double Sampling (CDS) and the other without CDS. Each example assumes that the recommended system clock frequency of 2MHz is used and that the time between "Final Data point Start" commands, (the integration time, T_{INT}) is 1ms.

Example with CDS. The Measurement Time with CDS is calculated as the Integration Time (T_{INT}) of 1ms less T_{ACQ} and T_{OS}. T_{OS}, the oversampling time, is 1/2 of the Initial Data Point time plus 1/2 the Final Data Point time since each group of samples is averaged with the result at the midpoint of each sample group.

Therefore, the Measurement Time = 1ms –(8 + 32 + 32)µs
= 928µs.

Example without CDS. The Measurement Time without CDS is calculated as the Total Integration Time (T_{INT}) of 1ms less T_{ACQ} and T_{OS}. T_{OS}, the oversampling time, is 1/2 of the Final Data Point time since this group of samples is averaged with the result at the midpoint of the sample group.

Therefore, the Measurement Time = 1ms –(0.5 + 32)µs
= 967.5µs.

Input Current Calculation

The following formula calculates the input current from the actual DDC output:

With CDS:
$$i = \frac{500pC \cdot \left[\dfrac{DDC\,output}{2^{20}}\right]}{T_{MEAS}}$$

$$i = \frac{500pC \cdot \left[\dfrac{DDC\,output}{2^{20}}\right]}{T_{INT} - K \text{ clock periods} - M \text{ clock periods}}$$

Without CDS:
$$i = \frac{500pC \cdot \left[\dfrac{DDC\,output}{2^{20}}\right]}{T_{MEAS}}$$

$$i = \frac{500pC \cdot \left[\dfrac{DDC\,output}{2^{20}}\right]}{T_{INT} - K \text{ clock periods} - M/2 \text{ clock periods}}$$
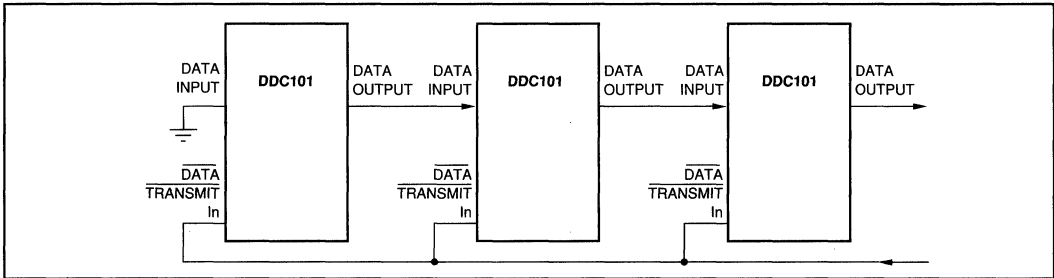
FIGURE 26. Daisy Chained DDC101s.
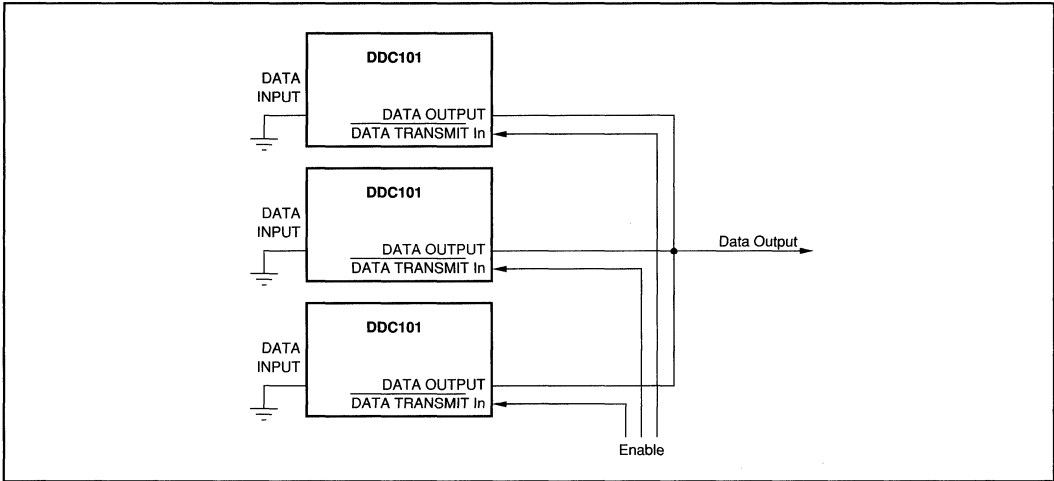
FIGURE 27. DDC101 Parallel Operation.

MULTIPLE DDC101 OPERATION

Multiple DDC101 units can be connected in serial or parallel configuration as illustrated in Figures 26 and 27.

DATA OUTPUT can be used with DATA INPUT to "daisy chain" the output of several DDC101 units together to minimize wiring; in this mode of operation, the serial data output is shifted through multiple DDC101s (Figure 26).

DATA OUTPUT is in a high impedance state until $\overline{\text{DATA TRANSMIT}}$ In is active. In this way, several DDC101 units can be connected in parallel to be enabled by the $\overline{\text{DATA TRANSMIT}}$ In line (Figure 27).

DDC101 EVALUATION FIXTURE

The DEM-DDC101P-C Evaluation Fixture is highly recommended for initial evaluation of the DDC101. It is designed for ease of use. The only additional equipment required to do a complete evaluation of the performance of the DDC101 is an IBM compatible PC with EGA or VGA graphics, a parallel interface port, a laser printer (optional), a ±5VDC power supply, and a signal source.

The DEM-DDC101P-C software is mouse compatible and retrieves data from up to 32 DDC101s in an easy to read, graphical format on the screen. The DEM-DDC101P-C Evaluation Fixture includes a PC Interface Board (with necessary parts), a DDC101 Board, a 25-pin ribbon connector and a 34-pin ribbon connector. The PC Interface Board makes timing commands and access to and from the DDC101 test board possible through the provided PC software. Data sheet, LI-439, provides complete information describing the evaluation fixture.

DDC101

2

A/D CONVERTERS, DATA ACQUISTION COMPONENTS
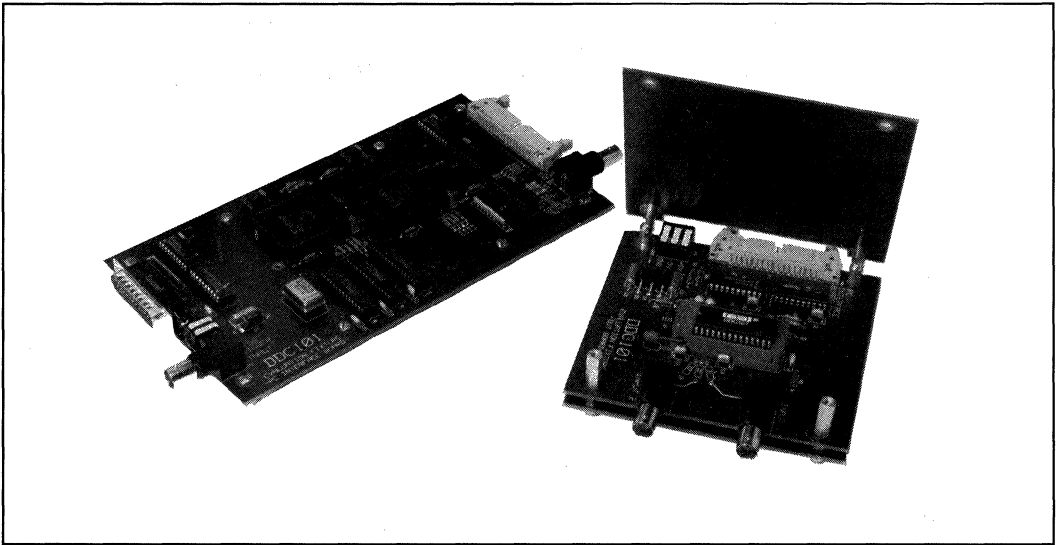
FIGURE 28. Photo of DEM-DDC101P-C Evaluation Fixture.
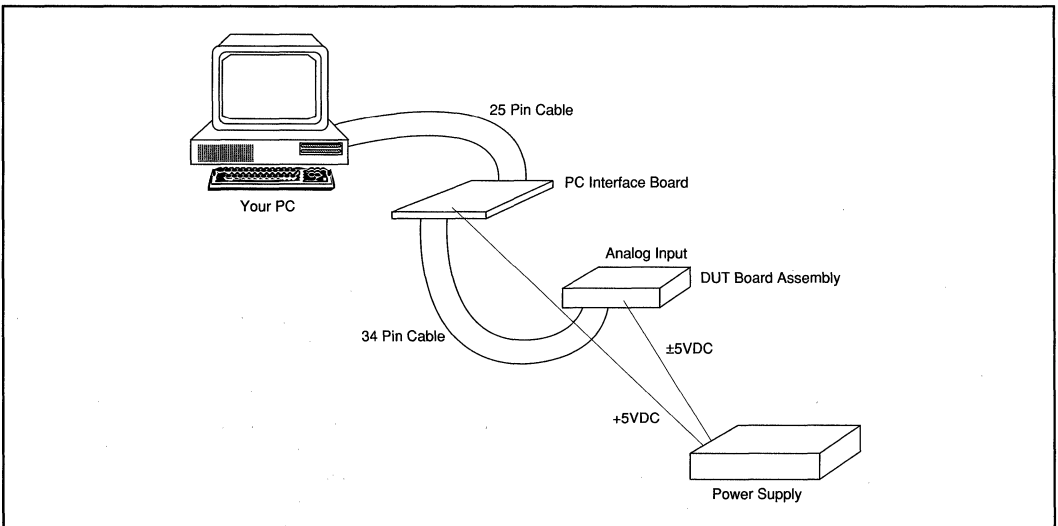
FIGURE 29. DEM-DDC101P-C Evaluation Fixture Connection Diagram.

BURR - BROWN®
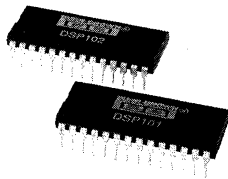
DSP101

DSP102

DSP101/102

2

DSP-Compatible Sampling Single/Dual
ANALOG-TO-DIGITAL CONVERTERS

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

FEATURES

- **ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI**
- **SINGLE CHANNEL: DSP101**
- **DUAL CHANNEL: DSP102**
  Two Serial Outputs or Cascade to Single 32-Bit Word
- **SAMPLING RATE TO 200kHz**
- **DYNAMIC SPECIFICATIONS:**
  Signal/(Noise + Distortion) = 88dB;
  Spurious-Free Dynamic Range = 94dB;
  THD = –91dB
- **SERIAL OUTPUT DATA COMPATIBLE WITH 16-, 24-, AND 32-BIT DSP IC FORMATS**

DESCRIPTION

The DSP101 and DSP102 are high performance sampling analog-to-digital converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide full sampling and conversion at rates up to 200kHz.

The DSP101 offers a single conversion channel, with 18 bits of serial data output, allowing the user to drive 16-bit, 24-bit, or 32-bit DSP ports. The DSP102 offers two complete conversion channels, with either two full 18-bit output ports, or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

Both the DSP101 and DSP102 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.

Convert
Command

Control
Logic

Analog
Input
Channel A

18-Bit Sampling ADC

Reference

Select Sync Format

Channel A User Tag In

Channel A Data/
Cascaded Data

Sync

Bit Clock

Analog
Input
Channel B

18-Bit Sampling ADC

Channel B Data

Channel B User Tag In

Cascade

Channel B on DSP102 Only

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

$T_A = 0°C$ to $70°C$, $\pm2.75V$ input signal, sampling frequency $(f_S) = 200kHz$, $V_A+ = V_D = +5V$, $V_A- = -5V$, 16MHz external clock on OSC1, CLKOUT tied to CLKIN, 8MHz data transfer clock on XCLK, data analysis band-limited to 20kHz, unless otherwise specified.

PARAMETER	CONDITIONS	DSP101JP DSP102JP MIN	TYP	MAX	DSP101KP DSP102KP MIN	TYP	MAX	UNITS
RESOLUTION				18			*	Bits
ANALOG INPUT								
Voltage Range			$\pm2.75V$			*		V
Impedance			1			*		$k\Omega$
Capacitance			20			*		pF
THROUGHPUT SPEED								
Complete Cycle	Acquisition + Conversion			5			*	μs
Throughput Rate		200			*			kHz
AC ACCURACY [1]								
Signal to (Noise + Distortion) Ratio	$f_{IN} = 1kHz$	83	86		86	88		dB[2]
	$f_{IN} = 1kHz$ (–60dB)		32			*		dB
	$f_{IN} = 25kHz$		82			*		dB
Total Harmonic Distortion	$f_{IN} = 1kHz$		–90	–86		–91	–89	dB
Spurious-Free Dynamic Range	$f_{IN} = 1kHz$	89	92		92	94		dB
Signal to Noise Ratio (SNR)	$f_{IN} = 1kHz$	84	88		87	89		dB
DC ACCURACY								
Gain Error				±5			*	%
Gain Error Mismatch	DSP102 Channels			±2			*	%
Integral Linearity	$\pm2.75V$ Input Range		Sufficient to meet AC Accuracy Specifications					
Differential Linearity	$\pm2.75V$ Input Range		Sufficient to meet AC Accuracy Specifications					
Integral Linearity Error	$\pm0.7V$ Input Range		±0.003			*		%
Differential Linearity Error	$\pm0.7V$ Input Range		±0.002			*		%
No Missing Codes	$\pm0.7V$ Input Range		14			*		Bits
Bipolar Zero Error [3]			±2					mV
Bipolar Zero Mismatch [3]	DSP102 Channels		±2					mV
Power Supply Sensitivity	$-5.25V < V_A- < -4.75V$		–60			*		dB
	$+4.75V < V_A+, V_D+ < +5.25V$		–60			*		dB
SAMPLING DYNAMICS								
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps,rms
Transient Response			1			*		μs
Overvoltage Recovery			5			*		μs
DIGITAL INPUTS								
Logic Levels (Except OSC1)								
V_{IL}	$I_L = \pm10\mu A$	0		+0.8	*		*	V
V_{IH}	$I_H = \pm10\mu A$	+2.4		+5	*		*	V
OSC1 Clock			74HC Compatible					
Frequency				16				MHz
Data Transfer Clock (XCLK)								
Frequency		0.1		12	*		*	MHz
Duty Cycle		40	50	60	*		*	%
Conversion Clock (CLKIN)								
Frequency		0.5		5.33	*		*	MHz
Duty Cycle		25	33	55	*	*	*	%
DIGITAL OUTPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded 32-bit Mode					
Coding			Binary Two's Complement					
Logic Levels (Except OSC2)								
V_{OL}	$I_{SINK} = 4mA$	0		+0.4	*		*	V
V_{OH}	$I_{SOURCE} = 4mA$	+2.4		+5	*		*	V
OSC2			Can only be used to drive crystal oscillator.					
Conversion Clock (CLKOUT)								
Drive Capability		$\pm2mA$			*			mA
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25	*	*	*	V
V_A-		–5.25	–5	–4.75	*	*	*	V
V_D		+4.75	+5	+5.25	*	*	*	V
Power Consumption	XCLK = OSC1 = 12MHz		250	425		*	*	mW
Supply Current	XCLK = OSC1 = 12MHz							
I_A+			30	45		*	*	mA
I_A-			–18	–25		*	*	mA
I_D			5	15		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		–65		+125	*		*	°C

NOTES: (1) All dynamic specifications are based on 2048-point FFTs, using four-term Blackman-Harris window. (2) All specifications in dB are referred to a full-scale input, $\pm2.75Vp$-p. (3) Adjustable to zero with external potentiometer.

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_A+ = V_D+ = +5V, V_A– = V_D– = –5V, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = 80f_S = 16MHz, XCLK = 40f_S = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

SINAD means Signal-to-(Noise + Distortion) Ratio.
SNR means Signal-to-Noise Ratio excluding harmonics thru the 8th.

THD means Total Harmonic Distortion thru 8th harmonic.
SFDR means Spurious Free Dynamic Range, including harmonics.

FREQUENCY SPECTRUM of ±2.75V, 1kHz INPUT
(Average of 12 FFTs, No Window Used)

FREQUENCY SPECTRUM of ±2.75V, 20kHz INPUT
(Using Four-Term Blackman-Harris Window)

FREQUENCY SPECTRUM of ±2.75V, 451kHz INPUT
(Using Four-Term Blackman-Harris Window)

Undersampling

INTERMODULATION DISTORTION WITH 1kHz AND 3kHz INPUTS
(Using Four-Term Blackman-Harris Window)

DSP102 CHANNEL SEPARATION ON CHANNEL B WITH
±2.75V, 1kHz INPUT ON CHANNEL A

DYNAMIC PERFORMANCE vs TEMPERATURE

f_{IN} = 1kHz, ±2.75V

SINAD
THD
SNR
SFDR

DSP101/102

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_A+ = V_D+ = +5V, V_A- = V_D- = −5V, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = 80f_S = 16MHz, XCLK = 40f_S = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

DYNAMIC PERFORMANCE vs TEMPERATURE
(f_S = 180kHz Asychronous to 12.288MHz
Crystal Between OSC1 and OSC2)
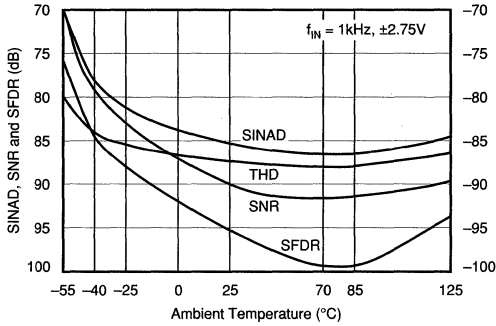
DYNAMIC PERFORMANCE vs TEMPERATURE
(Data Analysis Over Full 0 to 100kHz Band)
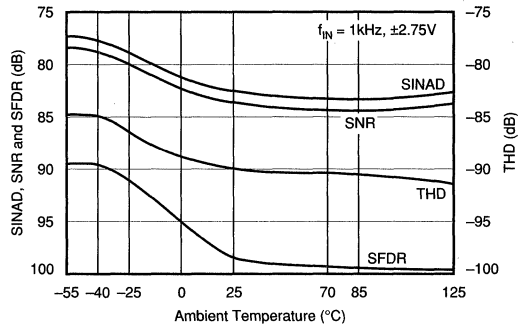
HISTOGRAM OF 5k CONVERSION RESULTS ON DSP102
(Both Inputs Grounded)
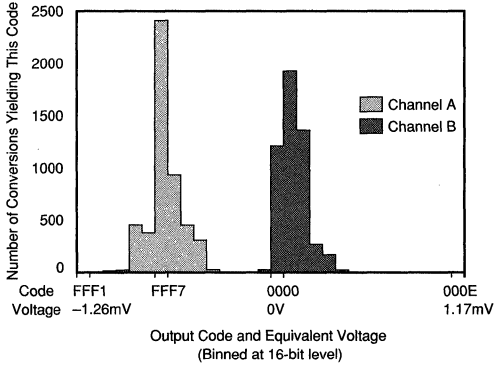
DYNAMIC PERFORMANCE vs CONVERSION RATE
(Data Analysis over Full 0 to f_S/2 Band,
OSC1 = 12.288MHz, XCLK = 3.072MHz)
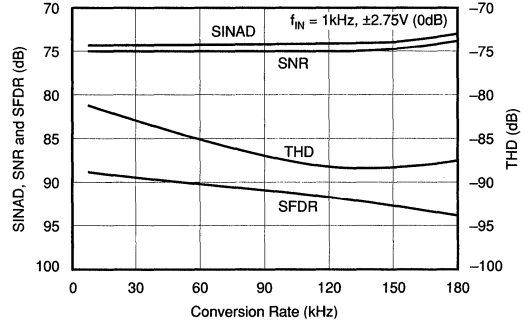
SINAD vs INPUT FREQUENCY
(Data Analysis over Full 0 to 100kHz Band)

TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY

BURR-BROWN®
BB

TYPICAL DSP102 FFT SETUP
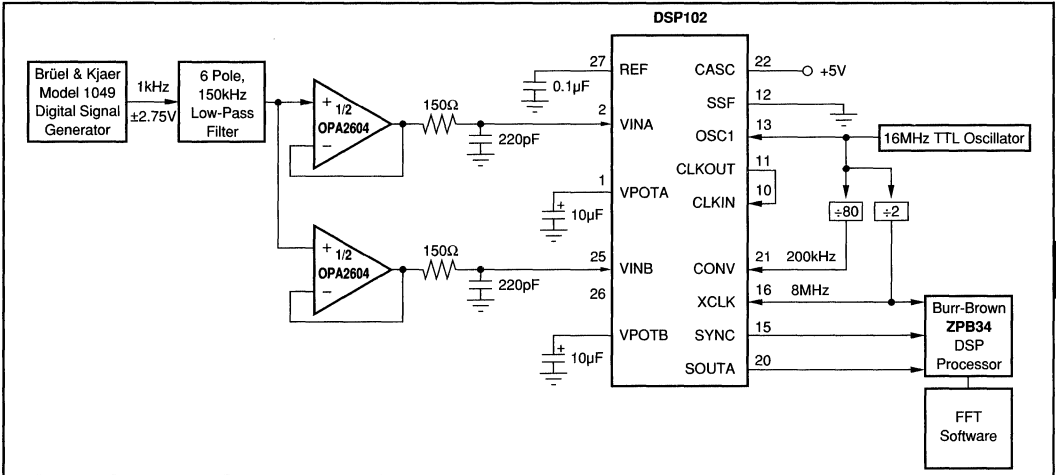
ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A- to Analog Common	−7V
V_D to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	−0.5 to V_D + 0.5V
Analog Input Voltage	±5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}, Plastic DIP	50°C/W

DSP101 PIN CONFIGURATION

Top View   **DIP**

VPOT	1		28	AGND
VIN	2		27	REF
MSB	3		26	CAP
VOS	4		25	
V_A-	5		24	
V_A+	6		23	
DGND	7	DSP101	22	DGND
DGND	8		21	CONV
V_D	9		20	SOUT
CLKIN	10		19	
CLKOUT	11		18	TAG
SSF	12		17	
OSC1	13		16	XCLK
OSC2	14		15	SYNC
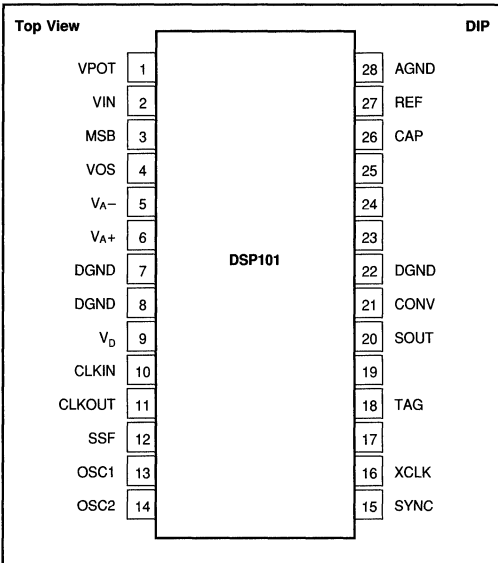
DSP101 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOT	Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V.
2	VIN	Analog In.
3	MSB	MSB Adjust In.
4	VOS	VOS Adjust In.
5	V_A-	−5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input/External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17		No Internal Connection.
18	TAG	User Tag In. Data clocked into this pin is appended to the conversion results on SOUT. See timing diagram (Figure 1).
19		No Internal Connection.
20	SOUT	Serial Data Out. MSB first, Binary Two's Complement format.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	DGND	Digital Ground.
23		No Internal Connection.
24		No Internal Connection.
25		No Internal Connection.
26	CAP	Bypass Capacitor. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.7V.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND. Voltage on this pin is approximately 3.8V.
28	AGND	Analog Ground.

DSP102 PIN CONFIGURATION

Top View   DIP

VPOTA	1		28	AGND
VINA	2		27	REF
MSBA	3		26	VPOTB
VOSA	4		25	VINB
V_A-	5		24	MSBB
V_A+	6		23	VOSB
DGND	7	**DSP102**	22	CASC
DGND	8		21	CONV
V_D	9		20	SOUTA
CLKIN	10		19	TAGB
CLKOUT	11		18	TAGA
SSF	12		17	SOUTB
OSC1	13		16	XCLK
OSC2	14		15	SYNC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DSP101JP	28-Pin Plastic DIP	215
DSP101KP	28-Pin Plastic DIP	215
DSP102JP	28-Pin Plastic DIP	215
DSP102KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	NUMBER OF CHANNELS	SIGNAL-TO-(NOISE + DIST.) RATIO dB min
DSP101JP	1	83
DSP101KP	1	86
DSP102JP	2	83
DSP102KP	2	86

DSP102 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOTA	Channel A Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V.
2	VINA	Channel A Analog In.
3	MSBA	Channel A MSB Adjust In.
4	VOSA	Channel A VOS Adjust In.
5	V_A-	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input / External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17	SOUTB	Channel B Serial Data Out. MSB first, Binary Two's Complement format.
18	TAGA	Channel A User Tag In. Data clocked into this pin is appended to the conversion results of SOUTA. See timing diagram (Figure 1).
19	TAGB	Channel B User Tag In. Data clocked into this pin is appended to the conversion results of SOUTB. See timing diagram (Figure 1).
20	SOUTA	Channel A Serial Data Out. MSB first, Binary Two's Complement format. If CASC is HIGH, 32 bits of data output, with first 16 bits being Channel A data.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	CASC	Select Cascade Mode In. If HIGH, DSP102 transmits a 32-bit word on SOUTA, with the first 16 bits being data on Channel A. If LOW, DSP102 transmits data for both channels simultaneously.
23	VOSB	Channel B VOS Adjust In.
24	MSBB	Channel B MSB Adjust In.
25	VINB	Channel B Analog In.
26	VPOTB	Channel B Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND. Voltage on this pin is approximately 3.8V.
28	AGND	Analog Ground.

DSP102 Cascade Mode (CASC = HIGH)

Conversion Clock Timing [2]

SYMBOL	DESCRIPTION (C_L = 50pF)	MIN	MAX	UNITS
t_1	XCLK period. Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP102)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP102)	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising		15	ns
t_8	SOUTA/B Data Valid Delay from XCLK Rising		15	ns
t_9	SOUTA/B Data Valid After from XCLK Rising	10		ns
t_{10}	TAGA/B Data Setup before XCLK Rising	20		ns
t_{11}	TAGA/B Data Hold after XCLK Rising		0	ns
t_{12}	OSC1 Period.[2] Duty Cycle 50% ± 10%	62	667	ns
t_{13}	CLKOUT Period. Duty Cycle 33% ± 10%		3 t_{12}	ns
t_{14}	CLKIN Period. Duty Cycle 33% ± 20%	186	2000	ns
t_{15}	CLKIN HIGH	62	1050	ns
t_{16}	CLKIN LOW	84	1340	ns

NOTES: (1) When using a DSP IC in a 16-bit mode, these data bits will be ignored by the processor. (2) f_{OSC1} must be at least 72 times faster than the conversion rate. (t_3, $t_4 \geq 72\ t_{12}$).

THEORY OF OPERATION

The DSP101 and DSP102 are sampling analog-to-digital converters optimized for handling dynamic signals. They have complete logic interface circuitry for ease of use with standard digital signal processing ICs, and transmit data words in a serial stream. The successive approximation conversion architecture is combined with an inherently sampling switched capacitor array to provide maximum user flexibility over sampling and conversion timing.

The DSP101 and DSP102 are pipelined internally. When the user gives a convert command at time (t), two actions are initiated. First, the internal sample/holds are switched to the hold state, and a conversion cycle is initiated. At the same time, the DSP101 or DSP102 transmits a synchronization pulse and starts shifting out the conversion results from the previous convert command at (t-1) using the system bit clock. The data from the conversion at time (t) is shifted out of the converter after the next convert command is received.

Both the DSP101 and the DSP102 are 18-bit A/Ds internally. When the DSP IC is programmed to accept 16-bit word lengths, the processor will ignore the last two data bits transmitted from the DSP101 or DSP102. A Cascade Mode on the DSP102 can be invoked to transmit data for both conversion channels over a single serial line as a 32-bit word. In this mode, the first 16 bits of data transmitted after the Sync pulse contain data from channel A, followed by 16 bits of information from channel B, allowing a single 32-bit word to contain data for both channels.

A unique Tag feature allows additional digital data to be appended to the conversion results, so that a single data word contains conversion results plus other signal information, such as gain settings or multiplexer channel settings in front of the converter.

The DSP101 and DSP102 are high-resolution A/D converters complete with sampling capability and on-board references. They can acquire and convert analog signals at up to a 200kHz sampling rate. Both operate from ±5V supplies, and have full-scale analog input ranges of ±2.75V.

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the DSP101. The falling edge of a convert command on pin 21 puts the internal sampling capacitor array into the hold state. The falling edge on pin 21 also starts the process to initiate a conversion and transmit data from the previous conversion, synchronizing both appropriately to the 10MHz clock input on pin 13. Figure 1 shows the timing relationship between the convert command, the output data, and the synchronization pulse.

In this basic system, the 10MHz clock is used both to generate a 3.33MHz conversion clock and as the data transfer bit clock for outputting data. Per Figure 1, there must be at least 72 clock pulses on pin 13 between convert commands, so that this circuit can sample and convert at up to 138kHz.
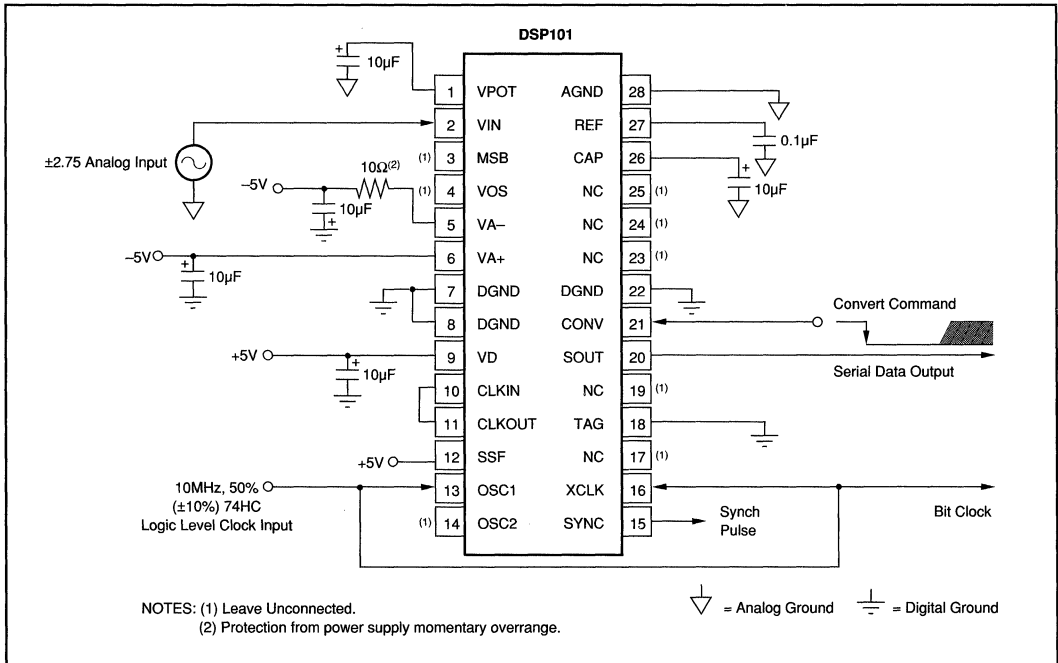
FIGURE 2. DSP101 Basic Operation.

The convert command at pin 21 causes a Sync pulse to be output on pin 15, followed by the data from the previous conversion output on pin 20. The Sync pulse will be HIGH for one bit clock cycle, since pin 12 is tied HIGH. (A LOW Sync pulse will be output on pin 15 if pin 12 is tied LOW.) Data is serially transmitted in an MSB-first data stream, in Binary Two's Complement format. Both the Sync pulse (pin 15) and the data stream (pin 20) are synchronized to the bit clock (at pins 13 and 16), with the timing relationships shown in Figure 1.

After the 18 bits of data from the previous conversion have been transmitted, pin 20 will continue to clock out LOWs until a new convert command restarts the process, since pin 18 (the Tag input) is grounded. If pin 18 is tied HIGH, pin 20 will clock out HIGHs between conversion cycles.

CONVERSION

A falling edge on pin 21 (CONV) puts the internal sampling capacitors in the hold state with minimum aperture jitter, initiates a conversion synchronized to the conversion clock, and outputs the data from the previous conversion with an appropriate Sync pulse. On the DSP102, a single convert command simultaneously samples both channels. The timing relationship between the convert command, Sync and the output data is shown in Figure 1. Both Sync and the output data are synchronized to XCLK, the system bit clock. Following a convert command falling edge, pin 21 must be held LOW at least 50ns.

Convert commands can be sent to the DSP101 and DSP102 completely asynchronous to other clocks in the system. This allows external events to be used to trigger conversions.

From Figure 1, it can be seen that two different clocking conditions must be considered in determining the minimum acceptable time between convert commands. First, there need to be a minimum of 24 XCLK periods between convert commands, to allow internal synchronization and transmission of Sync and the data. (In the Cascade Mode on the DSP102, there need to be at least 40 XCLK periods between convert commands, to allow transmission of the 32-bit data words.) When used with DSP processors programmed for data words longer than 16-bits, the transmission time to the processor may determine the minimum time between convert commands.

The second limitation on convert commands is the requirement that the internal analog-to-digital converter be given enough time to complete a conversion, shift the data to the output register, and acquire a new sample. This condition is met by having a minimum of 24 CLKIN periods between convert commands, or a minimum of 72 clock cycles on OSC1, if it is used to generate the conversion clock (CLKOUT driving CLKIN).

SIGNAL ACQUISITION

After a conversion is completed, the DSP101 or DSP102 will switch back to the sampling mode. With at least 24 CLKIN periods between convert commands, the A/D will have had sufficient time to acquire a new input sample to full rated accuracy.

DATA FORMAT AND INPUT LEVELS

The DSP101 and DSP102 output serial data, MSB first, in Binary Two's Complement format. In the Cascade Mode on the DSP102, the serial data will first contain 16 bits of data for channel A, MSB-first, followed by channel B data, again MSB-first. The analog input levels that generate specific output codes are shown in Table I.

As with all standard A/Ds, the first output transition will occur at an analog input voltage 1/2 LSB above negative full scale (–2.75V + 1/2 LSB) and the last transition will occur 3/2 LSB below positive full scale (+2.75V – 3/2 LSB.) See Figure 3.
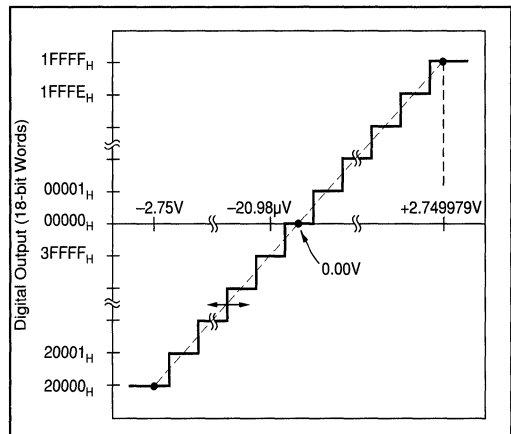
FIGURE 3. Analog Input to Digital Output Diagram.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT (BINARY TWO'S COMPLEMENT)		
		BINARY CODE	16-BIT WORDS (HEX)	18-BIT WORDS (HEX)
Least Significant Bit (LSB = $\frac{5.5V}{2^n}$)				
16-bit Words	84µV			
18-bit Words	21µV			
Input Range	±2.75V			
+ Full Scale (2.75V–1LSB)	+2.749916V +2.749979V	011...111	7FFF	1FFFF
Bipolar Zero (Midscale)	0V	000...000	0000	00000
One LSB below Bipolar Zero	–84µV –21µV	111...111	FFFF	3FFFF
– Full Scale	–2.75V	100...000	8000	20000

TABLE I. Ideal Input Voltage vs Output Code.
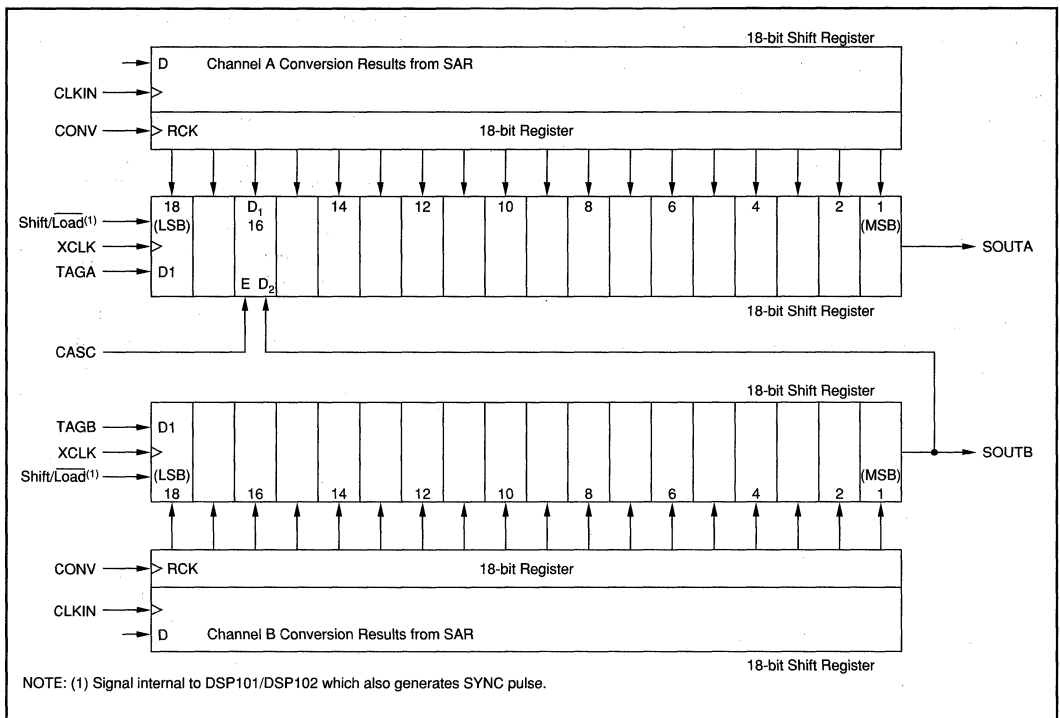
FIGURE 4. Output Structure of DSP102.

DATA TRANSFER

The internal A/Ds generate 18 bits of data, transmitting the data MSB first. When read by a DSP IC programmed to accept 16 bits of data, the first 16 MSB bits of data from the DSP101, or each channel of the DSP102, will be shifted into the processor's input shift register, and the last two least significant bits of data from the A/D will be ignored, although they will still be present on the serial data line. When the DSP processor is programmed to accept words of more than 16-bit length (typically 24-bit or 32-bit), the DSP101 and DSP102 will transmit the full 18-bit conversion results, after which the information input on the TAG input (or TAGA and TAGB on the DSP102) will be appended to the output word. (See Tag Feature below.)

In the Cascade Mode, the DSP102 will first transmit the 16 MSBs from channel A, followed by the full 18-bits from channel B, although DSP processors programmed to accept 32 bits of data will ignore the final two bits of information on Channel B. See the DSP102 Cascade Mode section below for details of the Cascade mode.

DATA SYNCHRONIZATION

A convert command both initiates a conversion and starts the process for transmitting data from the previous conversion. Convert commands can come at any time, completely asynchronous to the conversion clock or the bit clock, and

the conversion clock may also be independent of the bit clock. The DSP101 and DSP102 internally synchronize the output data, Sync pulse, and Tag inputs to the bit clock.

While the convert command, conversion clock and bit clock can be asynchronous, system performance is usually enhanced by synchronizing all of them to a system master clock, whenever the application permits. This minimizes changes in digital loads and currents when the critical S/H transition and A/D bit decisions are occurring. Within the DSP101 and DSP102 themselves, running asynchronous convert commands, conversion clocks and bit clocks typically degrades performance only several dB, as shown in the various typical performance curves, but the system board design can easily have more effect.

When a convert command is received, the internal logic generates an appropriate Sync pulse, synchronized to XCLK, as shown in Figure 1. The output Sync pulse will be active High or active Low depending on whether a HIGH or a LOW, respectively, is input at SSF (pin 12).

The convert command also causes the conversion results from the previous conversion to be loaded into the output shift register, synchronous to XCLK. Figure 4 shows the operation of the internal data shift registers on the DSP102. The DSP101 is basically similar, but includes only the top of the figure, showing the SOUTA path.

During the internal successive approximation conversion process, the conversion results are shifted into the input shift registers of the output stage on the DSP102. A new convert command latches that data into the 18-bit parallel latches shown. The internal signal that also generates the Sync pulse, labeled "Shift/Load" in Figure 4, synchronously loads the conversion data into the output shift register on the rising edge of XCLK. The conversion results are then clocked out of the shift register on subsequent rising edges of XCLK.

DATA TRANSFER CLOCK

XCLK is the data transfer clock, or bit clock, for the system, and is an input for the DSP101 or DSP102. This input is TTL- and 74HC-level compatible. The serial data and SYNC outputs are synchronized internally to this clock, with data valid on the rising edge of XCLK, per the timing shown in Figure 1. Data input on pin 18 (TAG) on the DSP101, or on pins 18 and 19 on the DSP102 (TAGA and TAGB), will be clocked into the output shift register on the rising edge of XCLK, as discussed in the Tag Feature section.

CONVERSION CLOCK

The analog-to-digital converter sections in the DSP101 and DSP102 were designed to provide accurate conversions under worst case conditions of supplies, temperatures, etc. In order to achieve a full 200kHz sampling capability, they were designed to use a 33% duty cycle conversion clock (CLKIN on pin 10) as shown in Figure 1. The clock is LOW

long enough for internal analog circuitry to settle sufficiently between bit decisions to insure rated accuracy. Bit decisions in the A/D are then made on the rising edge of CLKIN.
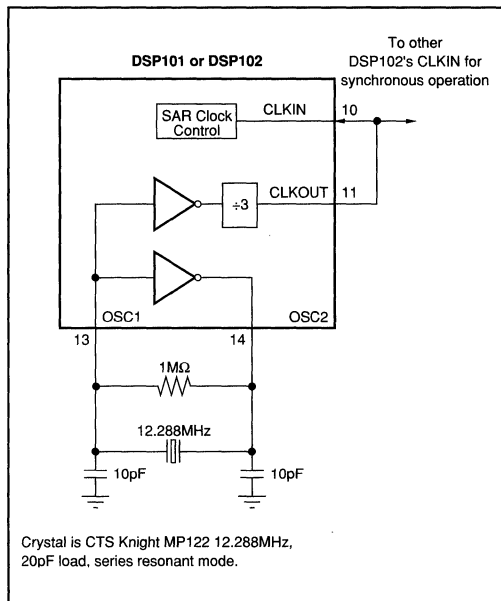
FIGURE 5. DSP101 or DSP102 Conversion Clock Circuit.
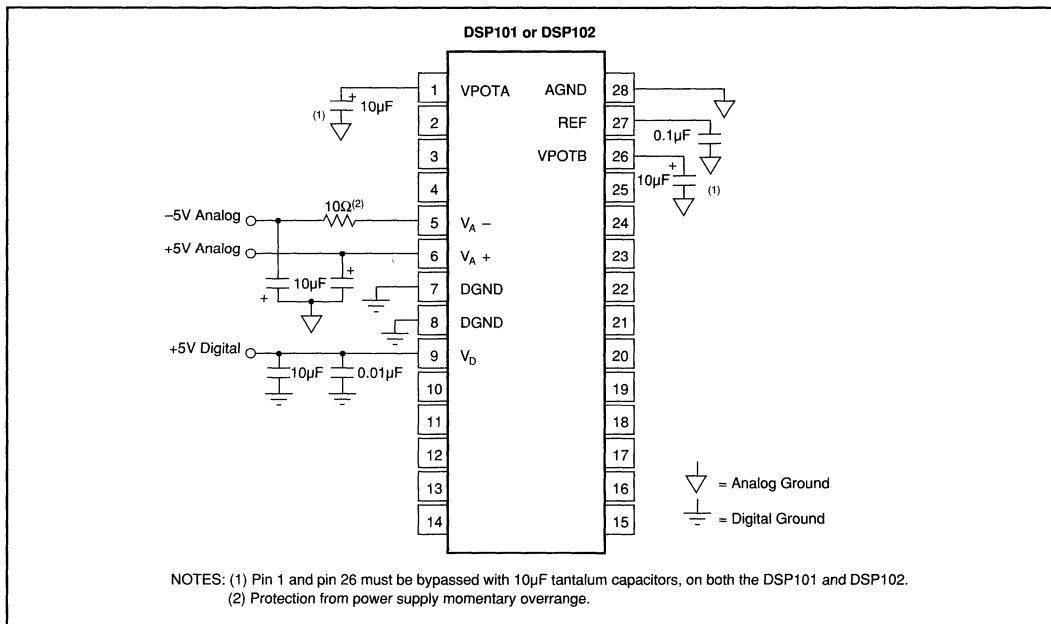
FIGURE 6. DSP101 or DSP102 Power Supply Connections.

DSP101/102

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

When a convert command is received, the DSP101 or DSP102 immediately switches the sampling capacitors to the hold state, and then internally gates the conversion clock to the A/D appropriately. Allowing a minimum of 24 CLKIN pulses between conversions insures that there is sufficient time for complete, accurate conversions, and allows the input sampling capacitor to fully acquire the next sample, regardless of the timing between the convert command and CLKIN.

In most applications, CLKIN (pin 10) can be driven from a 50% duty cycle clock without performance degradation. During characterization of the DSP101 and DSP102, the performance of a number of parts was measured under various conditions with a 4.8MHz, 50% duty cycle input to CLKIN at a full 200kHz conversion rate without noticeable degradation.

OSCILLATOR INPUTS AND CLKOUT

The DSP101 or DSP102 can generate a 33% duty cycle conversion clock output on CLKOUT (pin 11). This is accomplished by dividing by three a clock from either an external 74HC-level clock or from a crystal oscillator. CLKOUT can deliver ±2mA, and can be used to drive multiple DSP101 or DSP102 CLKINs. See Figure 1 for the timing relationship between OSC1 and CLKOUT.

To use an external 74HC-level clock, drive the clock into OSC1 (pin 13), and leave OSC2 (pin 14) unconnected.

To use a crystal oscillator to generate the conversion clock, refer to Figure 5. Connect the oscillator between OSC1 and OSC2. OSC2 provides the drive for the crystal oscillator. This pin cannot be used elsewhere in the system.

If CLKOUT is not used, both it and OSC2 should be left unconnected, and OSC1 should be grounded.

TAG FEATURE

Figure 4 shows the implementation of the TAG feature on the DSP101 and DSP102. When a convert command is received, the internal Shift/Load signal loads conversion result data into the output shift register synchronous to XCLK. Between convert commands, the information input on TAG (on the DSP101) or on TAGA and TAGB (on the DSP102) will be clocked into the output shift register on the rising edges of XCLK. Since this is an 18-bit shift register, the data input on the Tag lines will be output on SOUT (DSP101) or SOUTA and SOUTB (DSP102) delayed by 18 bit clocks.

The Tag Feature can be used in various ways. The Tag inputs can be tied HIGH or LOW to differentiate between two converters in a system. As discussed in the Applications section below, the Tag feature can be used to append to the serial output data word information on multiplexer channel address, or other digital data related to the input signal (such as the setting on a programmable gain amplifier.) Another option would be to daisy-chain multiple DSP101 or DSP102 converters, linking the serial output of one to the Tag input of the next. This can simplify the transmission of data from multiple A/Ds over a single optical isolation channel.

DSP102 CASCADE MODE

If pin 22 (CASC) is tied HIGH, the DSP102 will be in the Cascade Mode. In this mode, when a convert command is received, the DSP102 will transmit a 32-bit data word on pin
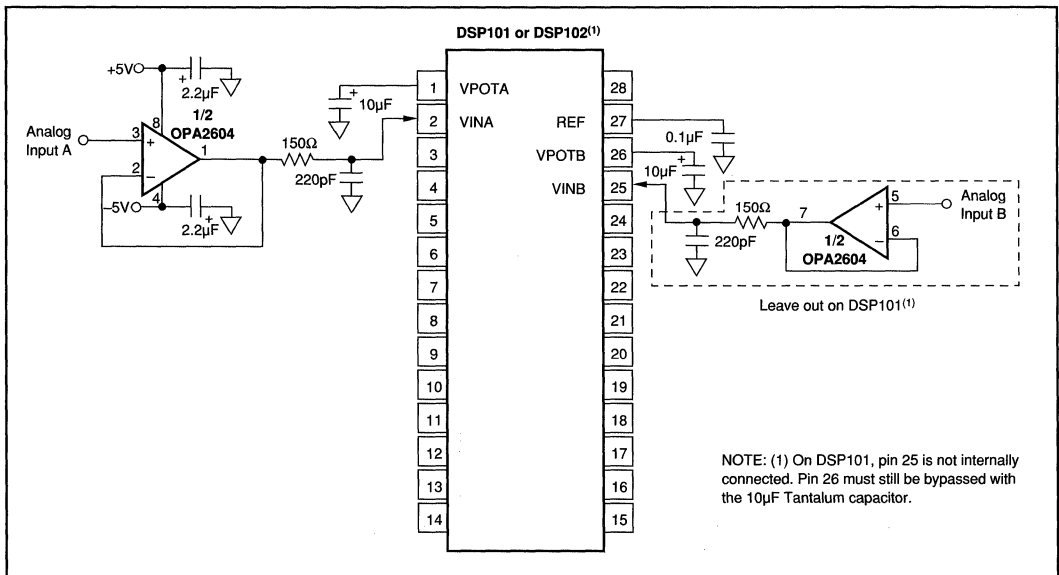
FIGURE 7. DSP101 or DSP102 Input Buffering.

20 (SOUTA) containing data for both input channels in two 16-bit words. Referring to Figure 1, the first 16 bits of data will be the results for channel A, followed by 16 bits of information for channel B. The data will be transferred MSB first. A convert command at time (t) will initiate the transmission of the results of the conversion initiated at time (t – 1).

From the descriptions above of the internal shift registers shown in Figure 4, it can be seen that the DSP102 in the Cascade Mode actually continues to shift out data after the 32nd bit of the data word. The next two bits clocked out will be the last two data bits from the full 18-bit conversion on channel B, after which the information output on SOUTA will be the information clocked into TAGB 35 bit clock cycles earlier.

In the Cascade mode on the DSP102, SOUTB will still output channel B conversion data and tag data as usual.

ANALOG PERFORMANCE

LINEARITY

The DSP101 and DSP102 are optimized for signal processing applications with wide dynamic range requirements. Linearity is trimmed for best performance in the range around 0V, which is critical for handling low amplitude signals. The DSP101 and DSP102 typically have integral and differential non-linearity below ±0.003% in the input range of ±0.7V, with there being no missing codes at the 14-bit level in this range. Over the full ±2.75V input range, the largest non-linearities are centered around the bit #2 transition points at +1.375V and –1.375V levels.

NOISE AND BIPOLAR ZERO ERROR

The equivalent input noise and bipolar zero error of the DSP101 and DSP102 is shown in the typical performance section for both channels on a DSP102. The inputs to both channels were grounded, and the results of 5,000 conversions was recorded. The data shown is binned at the 16-bit level. The noise results from all sources in the circuit, including clocks, reference noise, etc.

In a theoretically ideal converter with no offset and no noise, the results of all 5,000 conversion for each channel would lie in the bin corresponding to bipolar zero, code 0000. The typical DSP101 or DSP102 will have offset errors in the range of 1 to 2mV, and the two channels on the DSP102 will be matched closer than 2mV. The DSP102 shown in the typical performance section has the worst offset, –0.8mV, on channel A, with channel B being less than 1mV different, and the three sigma noise on either channel being less than 250µV.

INPUT BANDWIDTH

From the typical performance curves, it can be seen that there is very little degradation in Signal-to-(Noise + Distortion) for input signals up to 100kHz. The wideband sampling input typically maintains a 60dB Signal-to-(Noise + Distortion) Ratio undersampling 500kHz input signals.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP101 and DSP102, system design problems such as ground path resistance, contact resistance and power supply quality become very important.
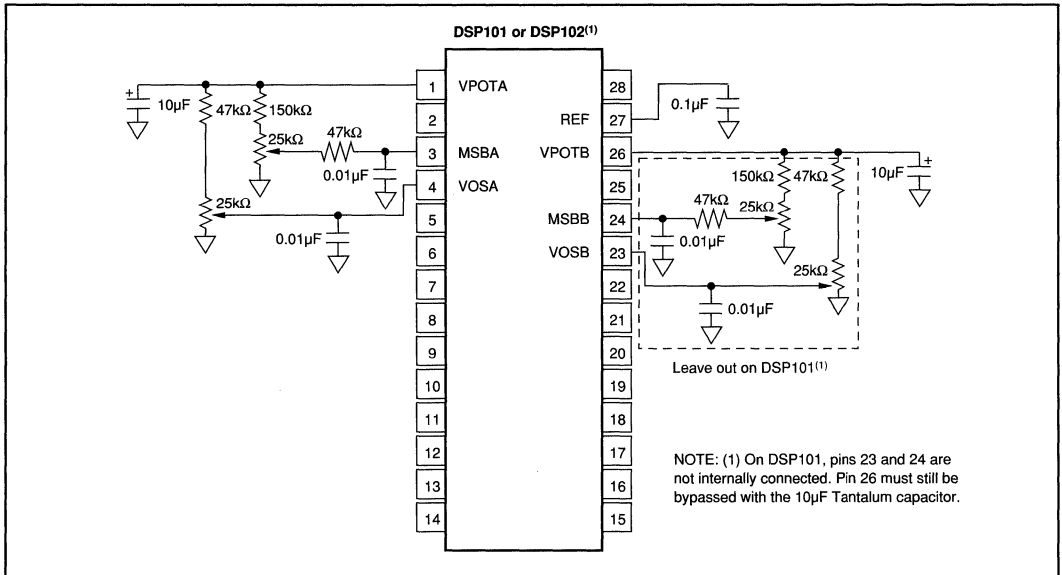
FIGURE 8. DSP101 or DSP102 Optional MSB and Offset Adjust.

Optimal dynamic performance is achieved by soldering the parts directly into boards, to keep the A/Ds as close as possible to ground. The use of sockets will often degrade AC performance. Zero-Insertion-Force sockets are particularly poor because longer lead lengths create inductance.

Short traces on the board, and bypass capacitors as close as possible to the A/D, will further improve dynamic performance.

GROUNDS

To achieve the maximum performance from the DSP101 or DSP102, care should be taken to minimize the effect of changes in current flowing in the system grounds, particularly while bit decisions are being made in the successive approximation converter's comparator. Pin 28 (AGND) on both the DSP101 and the DSP102 is the most critical, and care should be taken to make this pin as close as possible to the same potential as the system analog ground.

Whenever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 84µV at the 16-bit level, and one-quarter of that at the 18-bit level, the currents switched in a typical DSP system can easily corrupt the accuracy of the A/Ds unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figure 6. For optimum performance of any high resolution A/D, all of the supplies should be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-on.

INPUT SIGNAL CONDITIONING

To avoid introducing distortion, the DSP101 and DSP102 analog inputs must be driven by a source with low impedance over the input bandwidth needed in the application. Op amps such as the NE5532 or Burr-Brown's OPA2604 work well over audio bandwidths. Figure 7 shows an appropriate input driver circuit. The 150Ω and 220pF shown on the input help reduce the dynamic load on the input signal conditioning amp in front of the A/D, since all switched capacitor array architectures exhibit fast changes in input current load as the input sampling switch is opened and closed. These dynamic changes in the load can affect any signal conditioning circuit at the input. Other R and C combinations can be
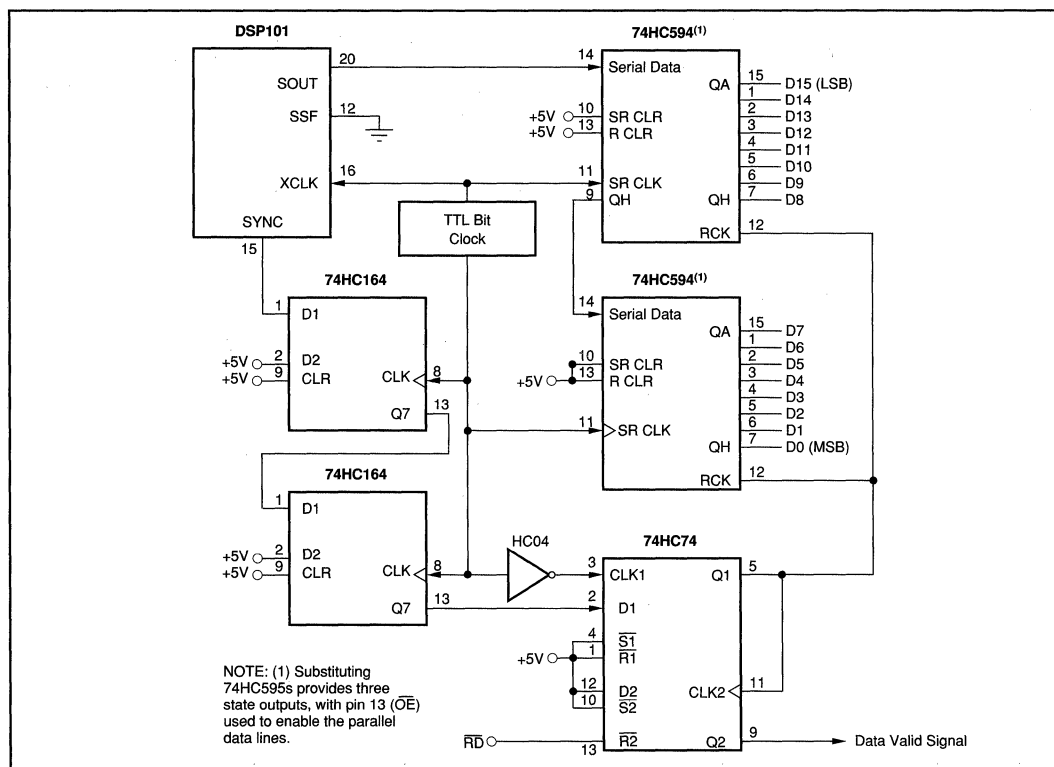
FIGURE 9. Driving a 16-bit Parallel Port from the DSP101.

used, but the resistor should not exceed 200Ω, or the output settling time of the signal conditioning amplifier may be too long.

EXTERNAL ADJUSTMENTS

All of the specifications for the DSP101 and DSP102, plus the typical performance curves, are based on the performance of these A/Ds without external trims. In most applications, external trims are not required.

OFFSET ADJUST

Where required by specific applications, offsets can be adjusted using the circuit of Figure 8. When not adjusted, VOS (pin 4) on the DSP101, and VOSA (pin 4) and VOSB (pin 23) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01μF capacitors, as close as possible to the A/D.

To trim offset, one alternative is to ground the analog input while converting continually. Then adjust the trimpot (on VOS for the DSP101, on VOSA and VOSB for the DSP102) until the output code is toggling between the codes FFFF and 0000 (Hex) at the 16-bit level (3FFFF and 00000 at the

18-bit level.) This will center the offset at 1/2 LSB below 0V, which is respectively –42μV or –10μV at the 16- and 18-bit levels.

The offset can also be adjusted by providing a sine wave to the A/D input. Using FFT, or even simple averaging of several thousand conversion results at a time, the trimpots can be adjusted until there is no DC offset of the signal.

Grounding the input, or providing the sine wave, as far in front of the A/D as possible allows offset from intervening signal conditioning components to be also corrected by this procedure.

MSB ADJUST

In most applications, adjustment of the Most Significant Bit weight will not be required. When not adjusted, MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01μF capacitors, as close as possible to the A/D.

MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, are internally connected to a resistor divider network that is used to laser-trim the weight
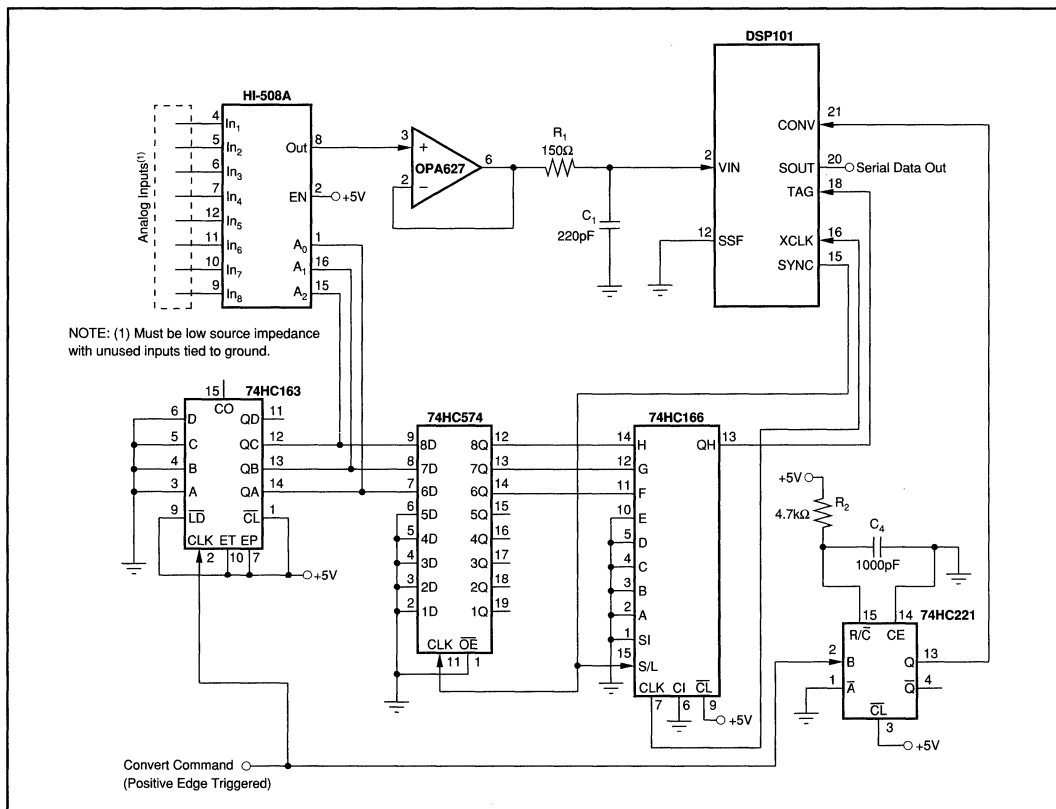
FIGURE 10. A Complete Eight-Channel Analog Input System Using the DSP202 and the HI-508A.

of the MSB capacitor in the CDAC. These pins are nominally at +100mV after laser-trimming during manufacturing. They can handle external inputs up to about one diode drop below ground (–0.6V) before internal clamping circuitry is triggered.

Figure 8 shows an appropriate circuit for adjusting the weight of the most significant bit to minimize differential non-linearity at the critical major-carry transition. To adjust, provide a small amplitude sine wave to the selected A/D input pin while converting continually, and adjust for maximum Signal-to-(Noise + Distortion) ratio, using appropriate signal analysis software.

GAIN ADJUST

If circuit gain needs to be adjusted in hardware, rather than in system software, appropriate trimpots should be included in the analog signal conditioning section in front of the DSP101 or DSP102. No specific gain adjust circuitry is included in the parts.

APPLICATIONS

INTERFACING DSP101 TO PARALLEL PORTS

Figure 9 shows a circuit for converting the serial output data from the DSP101 into 16 bits of parallel data, within the timing constraints of the serial bit-stream from the DSP101. In many applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

This circuit adds an additional pipeline delay to the conversion data, so that the parallel data from a conversion at time

(t) is valid one conversion cycle plus 17 XCLK clocks later (at t+1 plus 17 times XCLK). A convert command at time (t+1) generates a Sync and begins transmitting serial data from SOUT. The serial data is shifted into the 74HC594 shift registers, and Sync is shifted through the 74HC164 shift registers. The Q1 output of the 74HC74 dual D-type flip-flops clocks the conversion data into the output register of the 74HC594s, and triggers a data valid signal on its Q2 output. The user can then read the data at any time before the next conversion is started, and the Read signal will reset the data valid output from Q2.

In many systems, galvanic isolation of signals is required. Using opto-couplers on the serial data lines in Figure 9 allows a fully isolated system to be built using a DSP101 and only three couplers across the barrier (for serial data, XCLK and SYNC.)

MULTIPLEXING INPUTS TO THE DSP101

Figure 10 shows a complete circuit for sequentially scanning eight analog input channels with a single DSP101, and using the Tag feature on the DSP101 to append the multiplexer channel address to the serial output conversion results.

The circuit in Figure 10 includes the required digital logic and timing logic. The 74HC163 counter provides the scan sequence to the Burr-Brown HI-508A analog multiplexer. In order to allow the HI-508A enough time to switch to the next channel and settle before the DSP101 begins a conversion, a 74HC221 one-shot introduces a 3µs delay for the DSP101 convert command input.

The Burr-Brown OPA627 provides a low impedance source for the DSP101, buffering it from the output impedance of

DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	SSF[2]	SWL[3]
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

(1) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.
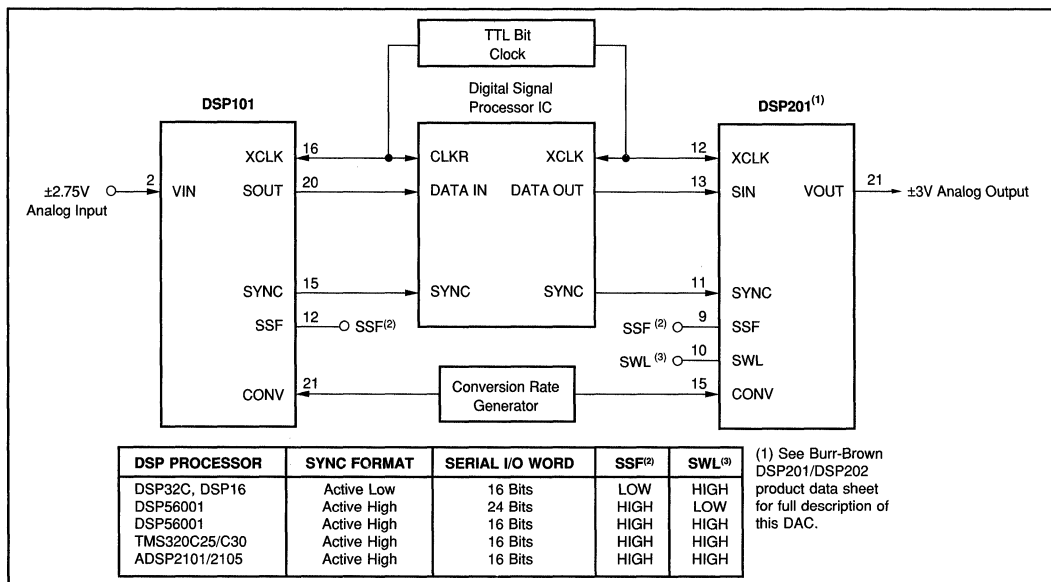
FIGURE 11. Analog Input and Analog Output System.

the multiplexer. This unity-gain buffer minimizes distortion, taking full advantage of the resolution and bandwidth of the DSP101.

The 74HC574D register delays the multiplexer address data by one conversion before appending the channel data to the serial conversion results from the DSP101. This attaches the channel address to the correct conversion results. Since the channel scanning shown in Figure 10 is sequential, this delay latch could be left out and software could recognize that the time (t) conversion results have the MUX address from the time (t-1) conversion appended. However, for systems using non-sequential scan lists, this delay latch is essential to maintain the conversion data and channel address integrity.

The 74HC166 synchronous loading shift register loads the channel address tag data into the shift register on the rising edge of the bit clock, in conjunction with the Sync output of the DSP101. The channel address tag data is then clocked into the DSP101 Tag input (pin 18) by the bit clock, while the conversion data is clocked out the other end of the

DSP101 shift register (discussed in another section of this data sheet.)

Figure 10 was developed and tested using a Burr-Brown ZPB34 DSP board, which contains an AT&T DSP32C, so that the SYNC output is programmed to be active LOW. The circuit needs to be modified for DSP processors from ADI, TI, and Motorola, which use active HIGH Sync pulses. For these processors, tie SSF (pin 12) on the DSP101 HIGH, and use a 74HC04 hex inverter to invert the Sync signal to the 74HC574 and 74HC166.

The same basic circuit can be duplicated to drive two channels in a DSP102, or can be easily modified for more or less than eight channels of analog input.

USING DSP101 AND DSP102 WITH TEXAS INSTRUMENTS DSP ICS

Figures 11 thru 17 show various ways to use the DSP101 and DSP102 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are
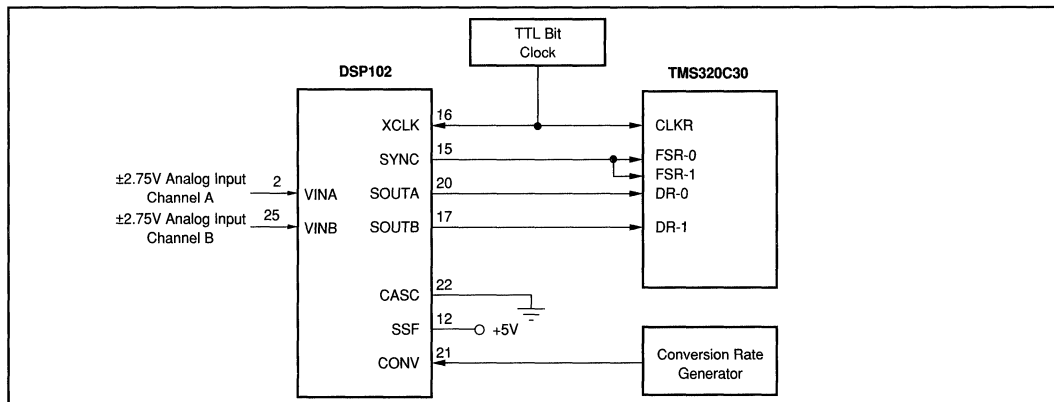
FIGURE 12. Using DSP102 with TMS320C30.
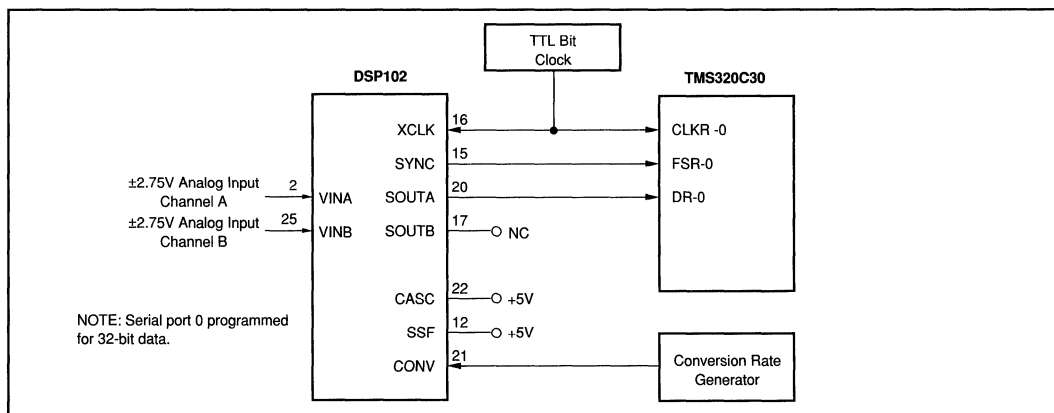
FIGURE 13. Using DSP102 with TMS320C30 in Cascade Mode.

based on using the TME320Cxx in the mode where SSF (Select Synch Format, pin 12) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP101 or DSP102 after receiving a convert command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing the basic operation of the A/Ds.

In all cases, the DSP101 and DSP102 will transmit data MSB-first, and the TMS320Cxx needs to be programmed for this.

Figure 11 shows a circuit for using the TMS320C25 or TMS320C30 in a complete analog input and analog output system using the DSP101 along with the Burr-Brown DSP201 D/A.

NOTES: (1) Sample rate on DSP102 and DSP202 may differ. (2) Analog Devices ADSP2101 may be used. SPORT1 and SPORT2 are used for serial MSB first communication. (3) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.
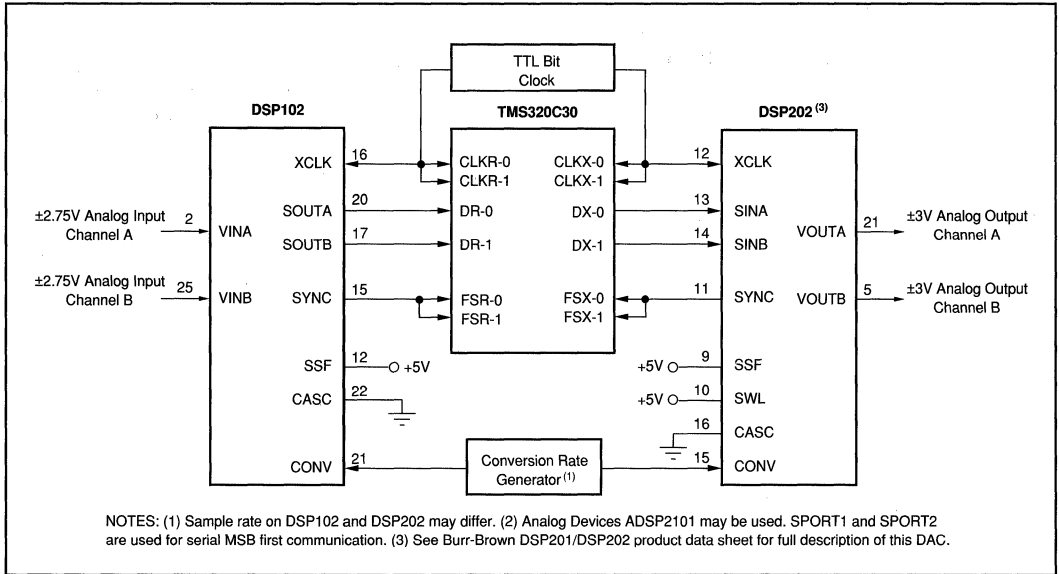
FIGURE 14. Two-Channel Analog Input and Output System with TMS320C30.

NOTES: (1) Program TMS320C30 for 32-bit mode. (2) Sample rate on DSP102 and DSP202 may differ. (3) DSP32C may be used in this mode. (4) See Burr-Brown DSP201/202 product data sheet for full description of this DAC.
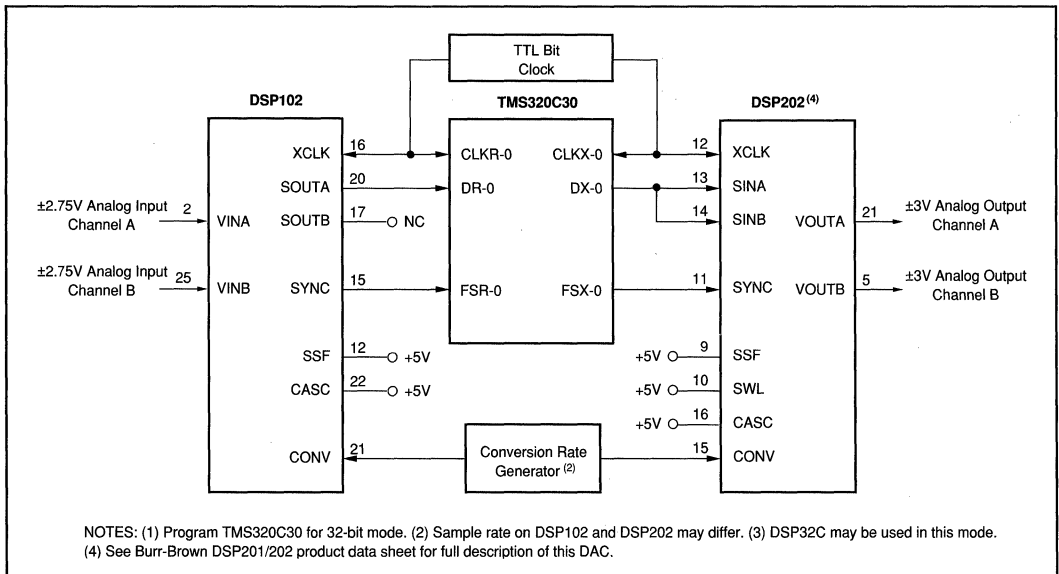
FIGURE 15. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

USING TMS320C31 TO GENERATE ALL CONTROL SIGNALS

Figure 17 shows a circuit for using the TMS320C31 with a DSP102 and a Burr-Brown DSP202 D/A to provide a two channel analog I/O system. The flexibility of the TMS320C31 allows it to generate the data transfer clock (XCLK) and the Convert Command, minimizing additional circuitry and synchronizing the timing signals to the processor's master clock. In this circuit, the DSP102 and DSP202 are used in their Cascade modes, transmitting and receiving two channels of data in a single 32-bit word. (See the Cascade Mode section above.)

Table II shows how to set up the circuit in Figure 17 for a 44.1kHz conversion rate for both channels of the DSP102 A/D and both channels of the DSP202 D/A. Both inputs and outputs will be simultaneously converted.

NOTES: (1) TMS320C25 FSR external, 16-bit data.
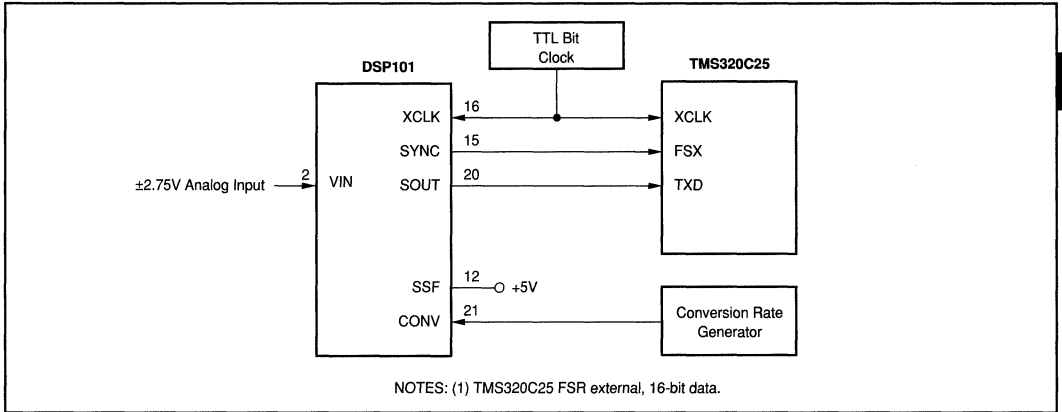
FIGURE 16. Using DSP101 with TMS320C25.
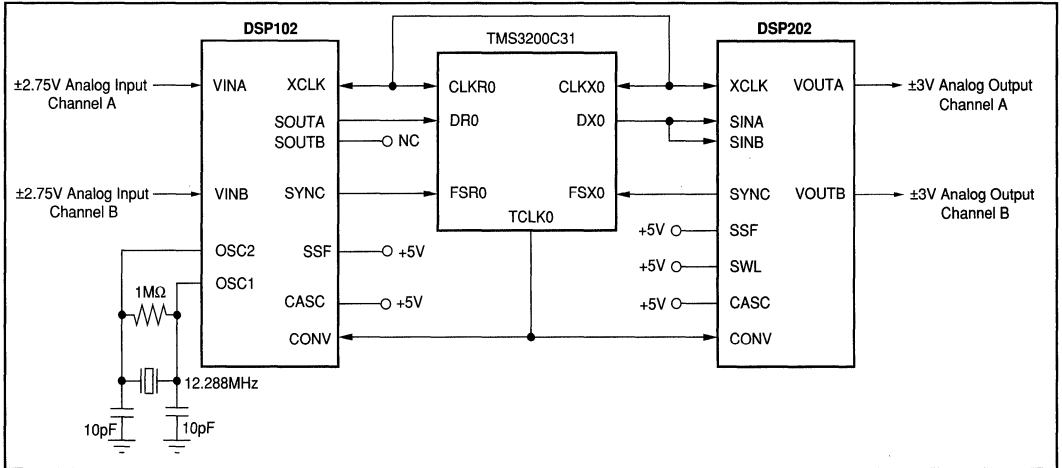
FIGURE 17. Two Channel Analog I/O Using TMS320C31.

SERIAL PORT	
Port Global Control Register	0x0EBC040
FSX/DX/CLKX Port Control Register	0x00000111
FSR/DR/CLKR Port Control Register	0x00000111
Receive/Transmit Timer Control Register	0x0000000F
TIMER	
Timer Global Control Register	0x000002C1
Timer Period Register	0x000000B5
NOTE: Assumes TMS320C31 has 32MHz Master Clock.	

TABLE II. TMS320C31 Register Settings for 44.1kHz Conversion Rate in Figure 17.

DSP101/102

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

USING DSP101 AND DSP102 WITH MOTOROLA DSP ICS

Figure 18 shows how to use the DSP101 with a Motorola DSP56001. Using the DSP102 requires using two DSP56001s. The DSP56001 needs to be programmed to receive data MSB-first with SYNC in the Bit Mode.

SSF (pin 12) needs to be tied HIGH for using either the DSP101 or the DSP102 with DSP56001s. This will cause the DSP101 or the DSP102 to transmit an appropriate active High synchronization pulse on SYNC (pin 15) after a convert command is received by the A/D. Timing is shown in Figure 1.

USING DSP101 AND DSP102 WITH AT&T DSP ICS

Figures 11, 19, 20, and 21 show how to use the DSP101 and DSP102 with the DSP16 and DSP32C in different modes. The AT&T processors need to be programmed to accept data MSB-first, and the DSP101 or DSP102 needs to have SSF (pin 12) tied LOW, so that an appropriate active Low synchronization pulse will be transmitted by the A/D after a convert command is received.

Figures 19 and 20 show the DSP32C and DSP16 respectively used with the DSP101 to handle a single analog input channel.

Figure 21 shows how to transmit to a single DSP32C conversion results from both DSP102 channels in a single 32-bit word, using the Cascade mode on the A/D.

Figure 11 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP101 and a Burr-Brown DSP201 D/A.
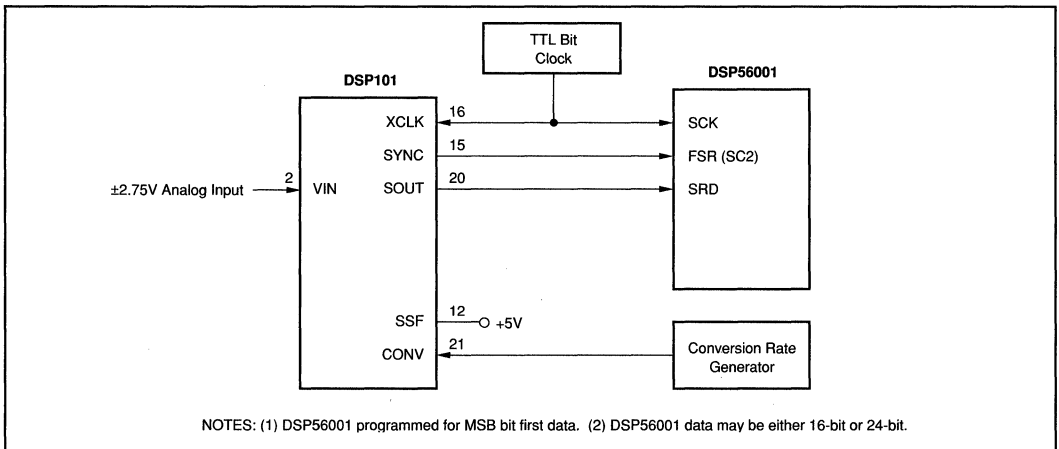
FIGURE 18. Using DSP101 with DSP56001.
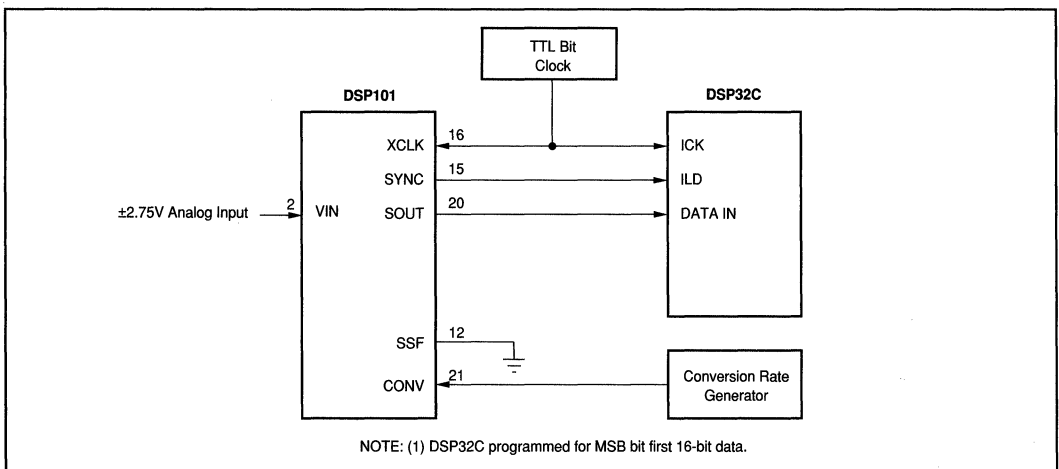
FIGURE 19. Using DSP101 with DSP32C.

USING DSP101 AND DSP102 WITH ADI DSP ICS

When using the DSP101 or DSP102 with the fixed-point ADSP21xx series, the processors need to be programmed to receive data MSB-first.

Figure 22 shows how to use the DSP102 with an ADSP2101 to provide a two-channel simultaneous sampling system.

Figure 23 shows the connections required to generate an analog input channel using an ADSP2105 with the DSP101.

The same basic circuit can be used to connect a DSP101 to the ADSP2101.

Figure 11 indicates how to build a complete analog I/O system using either the ADSP2101 or the ADSP2105 with a DSP101 and a Burr-Brown DSP201 D/A.

The two serial ports on the ADSP2101 can also be used with the DSP102 and the Burr-Brown DSP202 D/A to make two complete analog I/O channels, as indicated in footnote 2 of Figure 14.
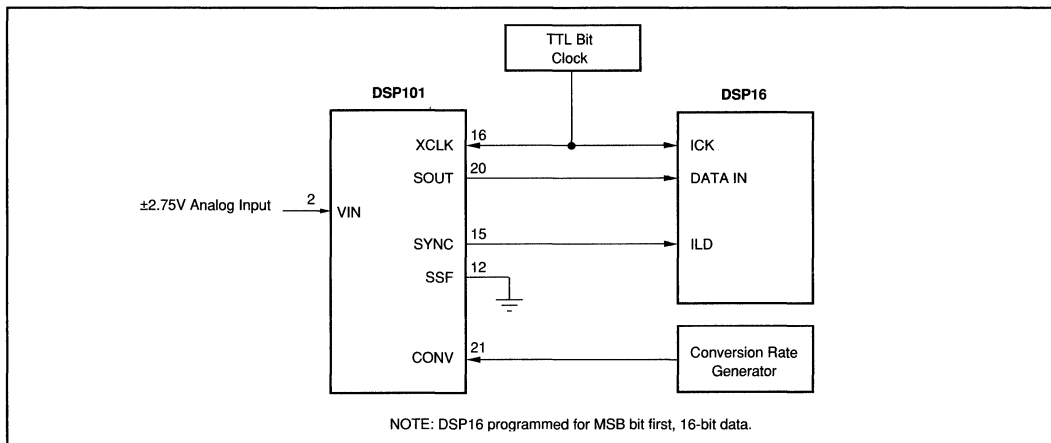
FIGURE 20. Using DSP101 with DSP16.
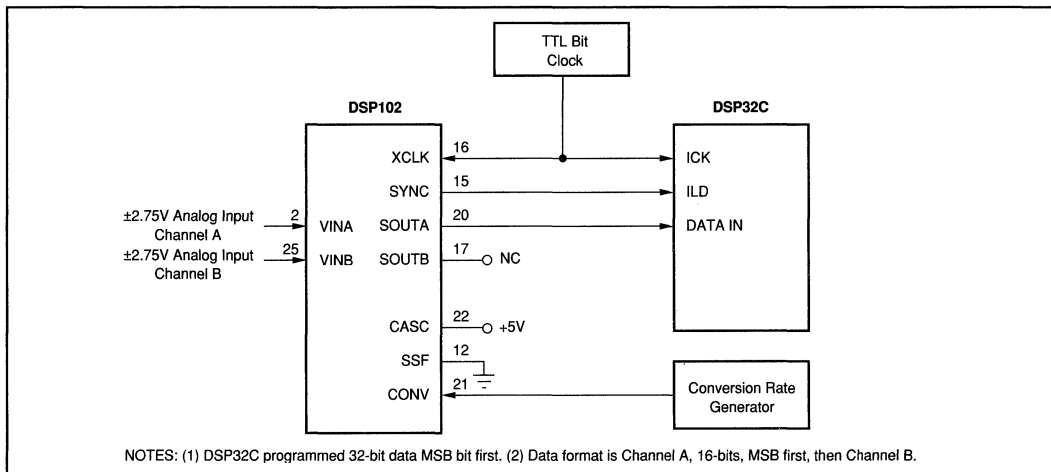
FIGURE 21. Using DSP102 with DSP32C in Cascade Mode.
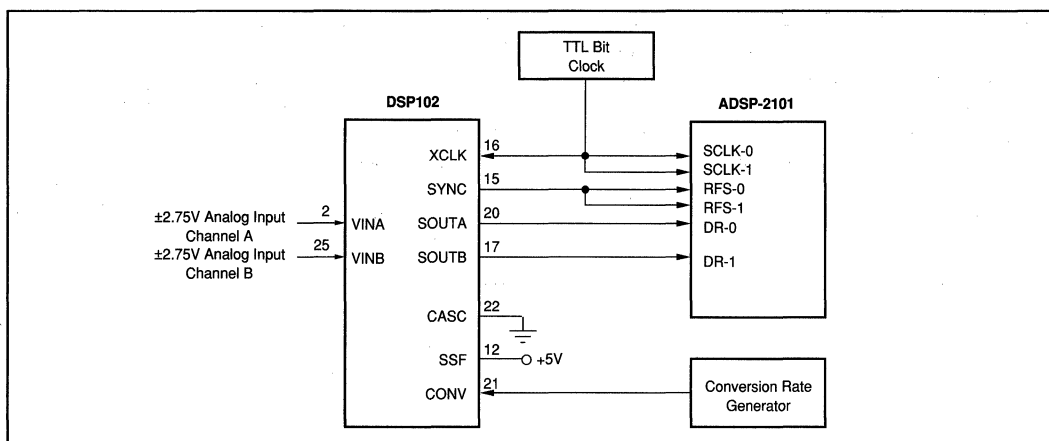
FIGURE 22. Using DSP102 with ADSP-2101.
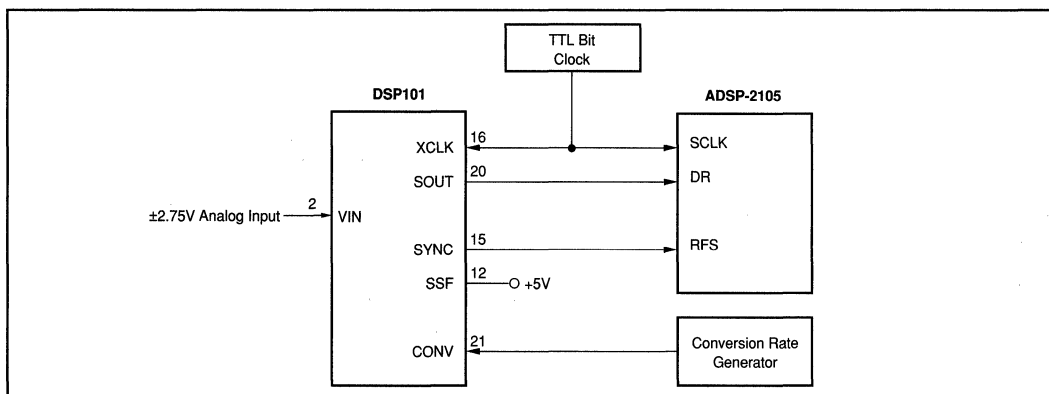
FIGURE 23. Using DSP101 with ADSP-2105.

DEM-DSP102/202 EVALUATION BOARD

An evaluation fixture, the DEM-DSP102/202, is available to simplify evaluation of the DSP101 and DSP102, and the companion digital-to-analog converters, the single DSP201 and dual DSP202. The DEM-DSP102/202 comes complete with a socketed DSP102 and DSP202, a breadboard area, TTL I/O headers and differential line drivers for data trans-fer options, a complete clocking circuit for the conversion clock and bit clock, and analog filter modules. The board makes it easy to go from design concept to working proto-type of a DSP-based system, offering two complete analog I/O channels.

Contact your local Burr-Brown representative for a full data sheet on the DEM-DSP102/202.

BURR - BROWN®
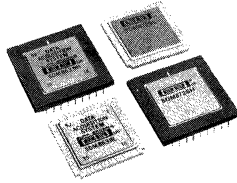
SDM862

SDM863

SDM872

SDM873

SDM862/3/872/3

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

16 Single Ended/8 Differential Input
12-BIT DATA ACQUISITION SYSTEMS

FEATURES

● COMPLETE 12-BIT DATA ACQUISITION
  SYSTEM IN A MINIATURE PACKAGE

● INPUT RANGES SELECTABLE FOR
  UNIPOLAR OR BIPOLAR OPERATION

● THROUGHPUT RATES: 862/3   872/3
   8-BIT ACCURACY: 45kHz   67kHz
  12-BIT ACCURACY: 33kHz   50kHz

● SELECTABLE GAINS OF 1, 10, AND 100

● FULL MICROPROCESSOR COMPATIBLE
  INTERFACE

● GUARANTEED NO MISSING CODES OVER
  TEMPERATURE

● SURFACE-MOUNT OR PIN GRID ARRAY
  PACKAGE OPTIONS

● HIGH RELIABILITY SCREENED VERSIONS
  AVAILABLE

● FULL SPECIFICATION OVER THREE
  TEMPERATURE RANGES:
  0 to +70°C, –25 to +85°C, –55 to +125°C

● EVERY UNIT SUPPLIED WITH
  ELECTRICAL TEST DATA

APPLICATIONS

● INDUSTRIAL PROCESS MONITORING

● AIRBORNE SYSTEMS MONITORING

● ENGINE MONITORING

● POWER PLANT MONITORING

● SECURITY SYSTEMS MONITORING

● AUTOMATIC TEST EQUIPMENT

DESCRIPTION

16 Single-Ended Inputs:	SDM862	SDM872
8 Differential Inputs:	SDM863	SDM873
33kHz Throughput Rate:	SDM862	SDM863
50kHz Throughput Rate:	SDM872	SDM873

The SDM components are complete, pin-compatible, data acquisition systems housed in a hermetically sealed 1"-square leadless chip carrier or a 1.1"-square pin grid array. The small package outlines and low power consumption provide an ideal data acquisition solution when space is at a premium.

The devices comprise of an input multiplexer, instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and three-state buffers.

The SDM family will accept unipolar or bipolar voltage inputs in the range 0 to +10V, ±5V and ±10V. For low-level signals, jumper-selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. System integration is simplified by the microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter.

ANALOG   DIGITAL

8 CH

16 CH   MUX   INA   S/H   ADC   12 Bits

8 CH

862/872   863/873

BURR - BROWN®

SDM862, SDM872 or SDM863, SDM873

CH0 | CH0 +
CH7 | CH0 -
CH15 | CH7

Input Channel Select — Enable

16 Single-Ended or 8 Differential Input Multiplexer

Output MUX* — Input Amp — Gain Select — Reference — Sense

Inst Amp — Amp Output — S/H Input

S/H Amp — S/H Output — Hold Capacitor — S/H Output

S/H Control — S/H Common

Input Range — Bipolar Offset — Reference In — Reference Out

12-Bit A/D Converter — Digital Data Outputs

Data Mode — Byte Select — Chip Select — Chip Enable — Read/Convert — Status

*(Output MUX Minus) Only on SDM863/873

SPECIFICATIONS

ELECTRICAL

At +25°C, $V_{CC} = \pm 15V$, $V_{DD} = 5V$, external sample/hold capacitor of 4700pF. **All grades are burned-in at +125°C for 48 hours min.**

PARAMETER	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Bipolar			±5, ±10				V
Unipolar			0-10				V
Input Impedance: On Channel		10^{10}			*		Ω
Off Channel		10^{10}			*		Ω
Input Capacitance: On Channel		20			*		pF
Off Channel		20			*		pF
CMRR (20VDC to 1kHz)	80	85		*	*		dB
Crosstalk (20Vp-p, 1kHz) [1]		−85	−80	*	*	*	dB
Feedthrough (at 1kHz) [1]		−85	−80	*	*	*	dB
Offset (channel to channel) G = 1 [2]		30	100	*	*	*	µV
Input Bias Current/Channel		1	5	*	*	*	nA
Input Voltage Range [3]	+10	+11		*	*		V
	−10	−15		*	*		V
DIGITAL [7, 8]							
MUX Input Channel Select: Logic '1'		5	30	*	*		µA
Logic '0'		5	30	*	*		µA
MUX Input: Logic High	4.0			*			V
Logic Low			0.8			*	V
S/H Command: Logic '1'		0.2			*		nA
Logic '0'		5	30	*		*	µA
ADC Section: Logic '1'			10			*	µA
Logic '0'			10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Integral Linearity [4]			±0.024			±0.012	%FSR
Differential Linearity [4]			±0.024			*	%FSR
No Missing Codes	Over Operating Temperature Range						
Gain Error [5]: G = 1			0.5			*	%
G = 100		0.9			*		%
Unipolar Offset Error [5]		16			*		mV
Bipolar Offset Error [5]			50			*	mV
Noise Error							
(Measured at S/H Output) G = 1		0.5	1		*	*	mVp-p
Droop Rate		50	500		*	*	µV/ms
Temperature Coefficients:							
Unipolar Offset		20				15	ppm of FSR/°C
Bipolar Offset		30				25	ppm of FSR/°C
Full-Scale Calibration		60				35	ppm of FSR/°C

SPECIFICATIONS

ELECTRICAL

At +25°C, $V_{CC} = \pm15V$, $V_{DD} = 5V$, external sample/hold capacitor of 4700pF.

PARAMETERS	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM TIMINGS							
ADC Conversion Time: SDM862/SDM863	9	20	25	*	*	*	μs
SDM872/SDM873	9	12	15	*	*	*	μs
S/H Aperture Delay		50			*		ns
S/H Aperture Uncertainty		2			*		ns
TIMING							
Throughput (Serial Mode)							
SDM862/SDM863			22			*	kHz
SDM872/SDM873			28			*	kHz
(Overlap Mode):							
SDM862/SDM863			33			*	kHz
SDM872/SDM873			50			*	kHz
MULTIPLEXER [6]							
Switching Time (between channels)		+1.5			*		μs
Settling Time (10V step to 0.02%)		2.5			*		μs
Enable Time 'ON'		1	2		*	*	μs
'OFF'		0.25	0.5		*	*	μs
INSTRUMENTATION AMPLIFIER [6]							
Settling Time (20V step to 0.01%)							
G = 1		5	12.5		*	*	μs
G = 10		3	7.5		*	*	μs
G = 100		4	7.5		*	*	μs
Slew Rate	12	17		*	*		V/μs
S/H AMPLIFIER [6]							
Acquisition (10V step to 0.01%)		5			*		μs
Aperture Delay		50			*		ns
Hold Mode Settling Time		1.5			*		μs
Slew Rate		10			*		V/μs
OUTPUT							
DIGITAL DATA							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (Sink = 1.6mA)			+0.4			*	V
Logic 1 (Source = 500μA)	+2.4			*			V
Leakage (Data Bits Only), High-Z State	−5	0.1	+5	*	*	*	μA
POWER SUPPLY REQUIREMENTS							
Rated Voltage: Analog ($\pm V_{CC}$)	14.25	15	15.75	*	*	*	VDC
Digital (V_{DD})	4.5	5	5.5	*	*	*	VDC
Supply Drain: +15V		13	22		*	*	mA
−15V		22	30		*	*	mA
+5V		11	15		*	*	mA
Power Dissipation		580	855		*	*	mW
TEMPERATURE RANGE							
Operating Temperature Range							
JH, KH/JL, KL	0		70	*		*	°C
AH, BH/AL, BL	−25		+85	*		*	°C
RH, SH/RL, SL	−55		+125	*		*	°C
Storage Temperature Range	−65		+150	*		*	°C

* Specification same as SDM862/863/872/873J, A, R grades.
NOTES: (1) Measured at the same and hold output. (2) Measured with all input channels grounded. (3) The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed. (4) Applicable over full operating temperature range. NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE. (5) Adjustable to zero using external potentiometer or select-on-test resistor. (6) Specifications are at +25°C and measured at 50% level of transition. (7) When using TTL drivers a 1kΩ pull-up resistor should be used. (8) Muxes operate in a break-before-make manner.

Side margin: SDM862/3/872/3 2 A/D CONVERTERS, DATA ACQUISITION COMPONENTS

DIGITAL TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tdsc	Status Delay from CE		100	200	ns
thec	CE Pulse Width	50	30		ns
tssc	$\overline{CS}$ to CE Setup	50	20		ns
thsc	$\overline{CS}$ Low During CE High	50	20		ns
tsrc	R/$\overline{C}$ to CE Setup	50	0		ns
thrc	R/$\overline{C}$ Low During CE High	50	20		ns
tsac	Byte Select to CE Setup	0	0		ns
thac	Byte Selected Valid During CE High	50	20		ns
tc 86X	Conversion Time: 12 Bit Cycle	9	20	25	µs
	8 Bit Cycle	6	13	17	µs
tc 87X	Conversion Time: 12 Bit Cycle	9	12	15	µs
	8 Bit Cycle	6	8	10	µs
READ MODE					
tdd	Access Time from CE		75	150	ns
thd	Data Valid after CE Low	25	35		ns
thl	Output Float Delay		100	150	ns
tssr	$\overline{CS}$ to CE Setup	50	0		ns
tsrr	R/$\overline{C}$ to CE Setup	0	0		ns
tsar	Byte Select to CE Setup	50	25		ns
thsr	$\overline{CS}$ Valid after CE Low	0	0		ns
thrr	R/$\overline{C}$ High after CE Low	0	0		ns
thar	Byte Select Valid after CE Low	50	25		ns
ths 86X	Status Delay after Data Valid	100	500	1000	ns
ths 87X	Status Delay after Data Valid	100	300	600	ns

ABSOLUTE MAXIMUM RATINGS[1]

+V_{CC} to ACOM .... −0.5V to +16V
−V_{CC} to ACOM .... +0.5 to −16V
+V_{DD} to DCOM .... −0.5V to +7.0V
Analog Input Signal Range .... +V_{CC} +20V to −V_{CC} −20V
Digital Input Signal .... −0.5V to +V_{DD}
ACOM to DCOM .... ±1V

NOTE: (1) Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functions operation under any of these conditions is not necessarily implied.

/QM HIGH RELIABILITY SCREENING

High Power Internal
  Visual Inspection .... Burr-Brown Spec. QC2010
Stabilization Bake .... 24Hr at +150°C
Temperature Cycling .... 10 Cycles −65°C to +150°C
Constant Acceleration .... 30kG, Y1 axis
Hermeticity Fine Leak .... Helium 5 x 10⁻⁸cc/s
Hermeticity Gross Leak .... Fluorocarbon
Burn-In .... 160Hr at +125°C

CONVERSION CYCLE TIMING
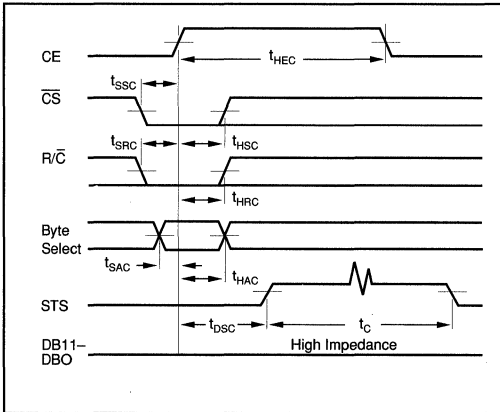
READ CYCLE TIMING
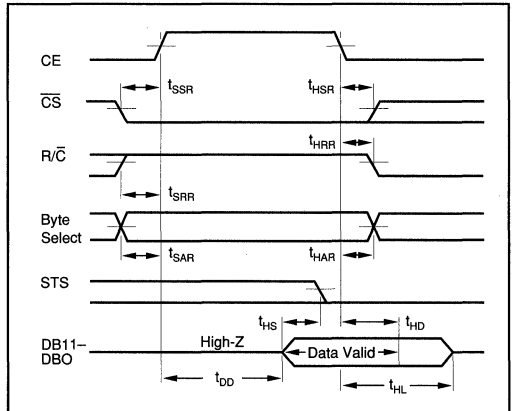
ORDERING INFORMATION [1]

Model	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)	Model	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)
SDM862J	16SE	L,H	±0.024	33kHz	0 to +70	SDM863J	8DIF	L, H	±0.024	33kHz	0 to +70
SDM862K	16SE	L,H	±0.012	33kHz	0 to +70	SDM863K	8DIF	L, H	±0.012	33kHz	0 to +70
SDM862A	16SE	L,H	±0.024	33kHz	−25 to +85	SDM863A	8DIF	L, H	±0.024	33kHz	−25 to +85
SDM862B	16SE	L,H	±0.012	33kHz	−25 to +85	SDM863B	8DIF	L, H	±0.012	33kHz	−25 to +85
SDM862R	16SE	L,H	±0.024	33kHz	−55 to +125	SDM863R	8DIF	L, H	±0.024	33kHz	−55 to +125
SDM862S	16SE	L,H	±0.012	33kHz	−55 to +125	SDM863S	8DIF	L, H	±0.012	33kHz	−55 to +125
SDM872J	16SE	L,H	±0.024	50kHz	0 to +70	SDM873J	8DIF	L,H	±0.024	50kHz	0 to +70
SDM872K	16SE	L,H	±0.012	50kHz	0 to +70	SDM873K	8DIF	L,H	±0.012	50kHz	0 to +70
SDM872A	16SE	L,H	±0.024	50kHz	−25 to +85	SDM873A	8DIF	L,H	±0.024	50kHz	−25 to +85
SDM872B	16SE	L,H	±0.012	50kHz	−25 to +85	SDM873B	8DIF	L,H	±0.012	50kHz	−25 to +85
SDM872R	16SE	L,H	±0.024	50kHz	−55 to +125	SDM873R	8DIF	L,H	±0.024	50kHz	−55 to +125
SDM872S	16SE	L,H	±0.012	50kHz	−55 to +125	SDM873S	8DIF	L,H	±0.012	50kHz	−55 to +125

NOTE: (1) 16 single-ended inputs, LCC package, with accuracy of 0.24% FSR. Temp Range of 0°C to +70°C and throughput of 33kHz = SDM862JL.

PACKAGE INFORMATION[1]

MODEL	DESCRIPTION	PACKAGE DRAWING NUMBER
PC862/863-1	LCC (Socketed) Evaluation PCB[2]	907
PC862/863-2	PGA Evaluation PCB	906

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) Socket is MC0068-1.

SDM862/3/872/3

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PIN CONFIGURATIONS

TOP VIEW

SDM862/SDM872

TOP VIEW

SDM863/SDM873

BURR-BROWN®

BB
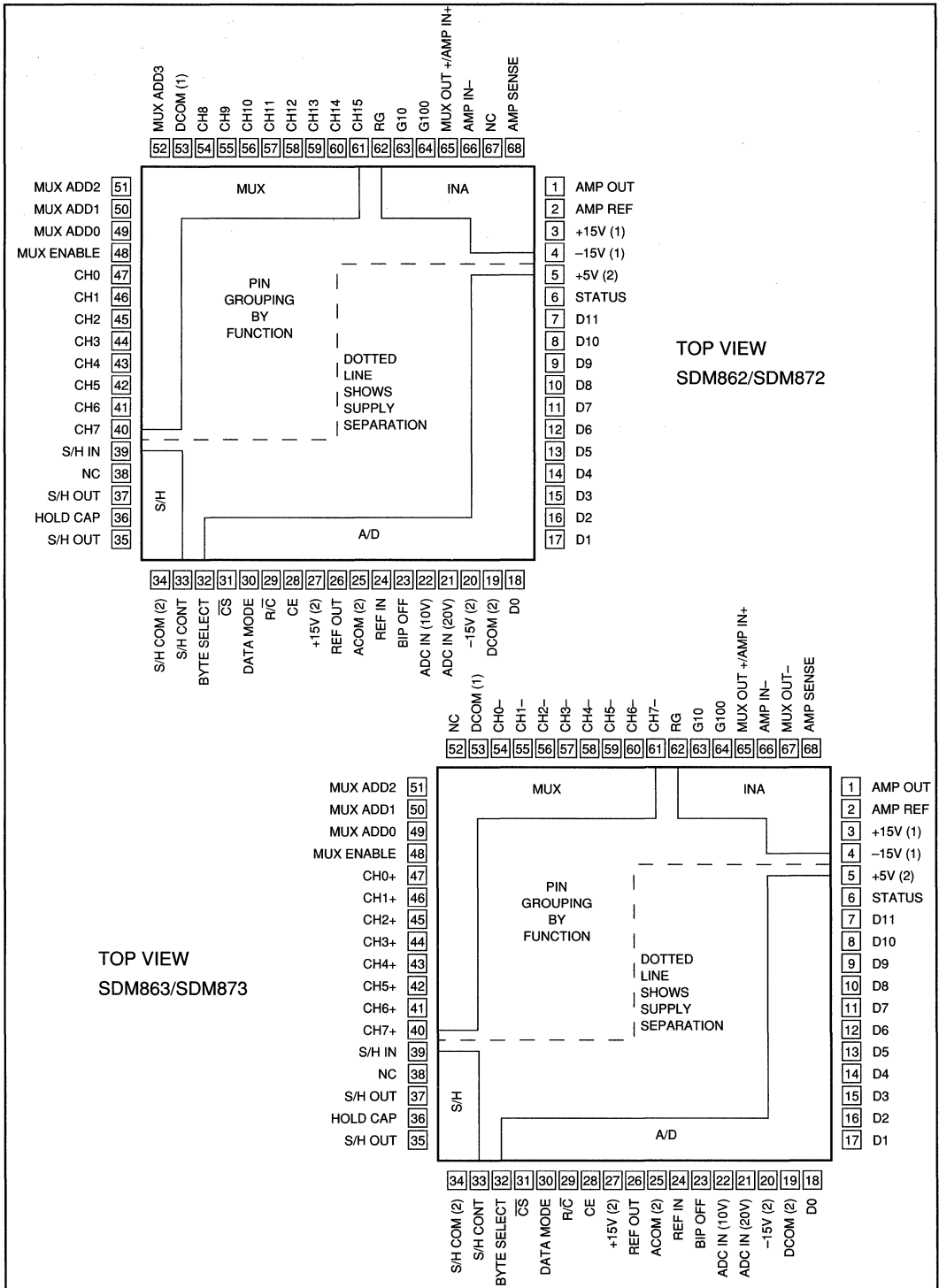
PIN DESIGNATION	DEFINITION	COMMENTS SDM8X2 = SDM862 OR SDM872
CH0 to CH15 CH0 to CH7 (+, −) (PINS 40 to 47, 54 to 61)	Channel Inputs	Analog Inputs (Total 16) for single-ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT+/AMP IN+ (PIN 65)	MULTIPLEXER "HI" OUTPUT	On the SDM8X2 this is the multiplexer output. On the SDM8X3 it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUXOUT (Pin 67)	MULTIPLEXER "LO" OUTPUT	This pin is used on the SDM8X3 only. It should be connected to the negative input of the instrumentation amplifier.
AMP IN (Pin 66)	Negative input of instrumentation amplifier	On the SDM8X2 this should be connected to analog common. On the SDM8X3 it should be connected to Muxout—(Pin 67).
AMP OUT (Pin 1)	Output of instrumentation amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE (Pin 68)	Output sense line of instrumentation amplifier	This pin will normally be connected direct to AMP OUT (Pin 1).
AMP REF (Pin 2)	Reference for amplifier output	This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to optimize system accuracy.
S/H OUT (Pins 35/37)	Output of sample/hold amplifier	Two pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.
HOLD CAP (Pin 36)	Connection for hold capacitor on S/H amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using Pins 35 and 37.
ADC IN (20V); ADC IN (10V) (Pins 21, 22)	Inputs to A/D converter	Connect to S/H amplifier output. Use appropriate pin for desired range.
RG, G10, G100 (Pins 62, 63, 64)	Gain settling pins on instrumentation amplifier	For Gain = 1, no connections. For Gain = 10, connect G10 to RG. For Gain = 100, connect G100 to RG.
REF OUT (PIN 26)	10V Reference voltage	This is the reference voltage for the A/D converter.
REF IN, BIP OFF (Pins 24, 23)	Reference input and offset input to A/D converter	Connect trim potentiometers (or select-on-test resistors) to these pins for unipolar or bipolar operation as shown in Figures 12, 13.
S/H IN (Pin 39)	Input to sample/hold amplifier	Connect to amp out (Pin 1).
MUX ENABLE (Pin 48)	Multiplex enable/disable	Logic '1' on this pin will enable a selected channel on the internal multiplexer. Logic '0' de-selects all channels.
MUX ADD0 to MUX ADD3 (Pins 49 to 52)	Address inputs for channel selection	These address lines select a particular channel as specified in Figure 24.
S/H CONT (Pin 33)	Track/Hold control on S/H amplifier	Logic '1' holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.
S/H COM (Pin 34)	Reference for S/H logic control	Connect to digital common.
D0 to D11 (Pins 7 to 18)	3-state digital outputs	The 12- or 8-bit result of a conversion is available as output on these pins (D0-LSB, D11-MSB).
STATUS (Pin 6)	Status of A/D conversion	This output is at logic '1' while the internal A/D converter is carrying out a conversion. This pin may be used to directly control the S/H amplifier.
CE (Pin 28)	Chip enable	This input must be at logic '1' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
$\overline{CS}$ (Pin 31)	Chip select	This input must be at logic '0' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
R/$\overline{C}$ (Pin 29)	Read/convert	Data can be read when this pin is logic '1' or a conversion can be initiated when this pin is logic '0'. This pin is typically connected to the R/$\overline{W}$ control line of a microprocessor-based system (see Figures 10, 17, 18, 19, 20).
DATA MODE (Pin 30)	Select 12 or 8 Bit Data	When data mode is at logic '1' all 12 output data bits are enabled simultaneously. When data mode is at logic '0' MSBs and LSBs are controlled by byte select (Pin 32).
BYTE SELECT (Pin 32)	Byte address, short cycle	When reading output data, byte select at logic '0' enables the 8 MSBs. Byte select at logic '1' enables the 4 LSBs. The 4 LSBs can therefore be connected to four of the MSB lines for inter-connection to an 8-bit bus. In start convert mode, logic '0' enables a 12-bit conversion while logic '1' will short cycle the conversion to 8 bits (see Figure 10).
+15V(1), +15V(2)(Pins 3, 27)	Power Supply	Connect to +15V supply using decoupling as indicated in Figures 15, 16.
−15V(1), −15V(2)(Pins 4, 20)	Power Supply	Connect to −15V supply using decoupling as indicated in Figures 15, 16.
ACOM(2) (Pin 25)	Analog Common	Analog common connection. Note that a common (including digital common) should be connected together at one point close to the device.
DCOM (1) (Pin 53)	Reference for MUX logic control.	Connect to digital common.
+5V (Pin 5)	Logic power supply	Connect to +5V digital supply line with decoupling as in Figures 15, 16.
DCOM(2) (Pin 19)	Reference for A/D converter control lines	Connect to S/H common at one point close to device.
NC (Pin 38)	No internal connection	

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SYSTEM DESCRIPTION

The SDM comprises four circuit elements—an input-protected multiplexer, an instrumentation amplifier, a sample/hold amplifier, and an analog-to-digital converter.

INSTALLATION

MULTIPLEXER

The SDM family has a choice of input multiplexers (MUX).

   SDM862 and SDM872:   16 single-ended inputs
   SDM863 and SDM873:   8 differential inputs

On all models, the analog inputs may be expanded using the enable control. See Figure 1. When the enable is at a logic "0," the internal MUX is disabled, allowing additional multiplexers to be connected in parallel. The limiting factor for the number of additional multiplexers is the cumulative effect of leakage current flowing in the signal source impedance, causing offset errors.

Differential inputs will generally eliminate the noise associated with common system grounds, but care must be taken to ensure that neither of the differential inputs exceed the maximum input range. Otherwise, signal distortion will result. A return path for the input bias currents must always be provided. This prevents the charging of stray capacitances in applications using floating sources, such as transformers and thermocouples. Multiplexer inputs are protected from overvoltage, as indicated in the electrical specifications, and should be current limited to 20mA.

Where high-speed operation is required and channels require rapid sampling, then it is important to buffer the inputs against the effect of current sharing between the MUX output capacitance and the input filter capacitance. See Figure 2.

FIGURE 2. Filter and MUX Capacitance.

All data acquisition systems using a MUX require consideration of the errors that may be introduced by MUX output capacitance. The applications information explains this more fully in the input filtering section.

Shown in Figure 3 is an application that demonstrates the flexibility of signal conditioning and gives the opportunity to use a higher bandwidth filter. Diodes shown are low leakage types (1na). The low output impedance of the amplifiers reduces the time taken to charge MUX capacitance C_M.

INSTRUMENT AMPLIFIER

The instrument amplifier (INA) presents a very high input impedance to the signal source, eliminating gain errors introduced by voltage divider action between the source output impedance and SDM input impedance. Where the differential models are used, the INA performs the differential to single-ended conversion required to drive the sample/hold amplifier. Gains may be set by using external jumpers, to values of 1 (no jumper), 10 and 100. For gains other than these presets, the following formula may be used to find an external resistor value to add in series with the G = 10 or G = 100 jumpers.

$$R_{ext} = \frac{40k\Omega}{G-1} - Ri \qquad \begin{array}{l}\text{Where Ri} = 4444\Omega, \text{G} = 10 \text{ input.}\\ 404\Omega, \text{G} = 100 \text{ input.}\end{array}$$

It should be noted that the internal gain set resistors have a ±20% tolerance and ±20ppm/°C drift.

FIGURE 1. External Multiplexer Connections for Differential and Single-Ended Operation.
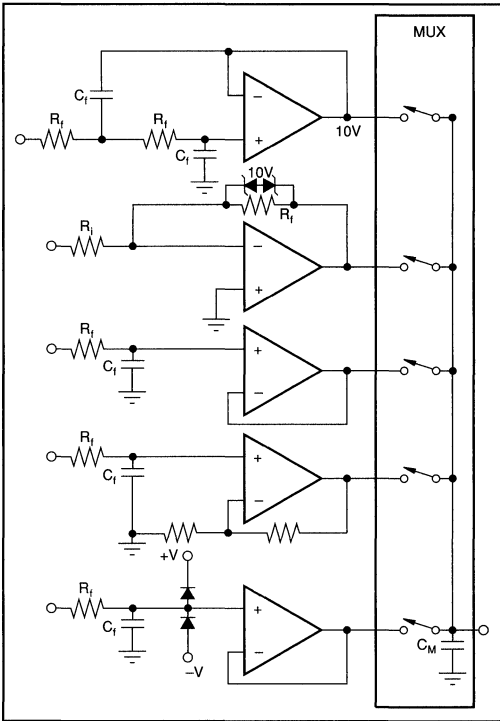
FIGURE 3. Example Application Illustrating Flexible Signal Conditioning.
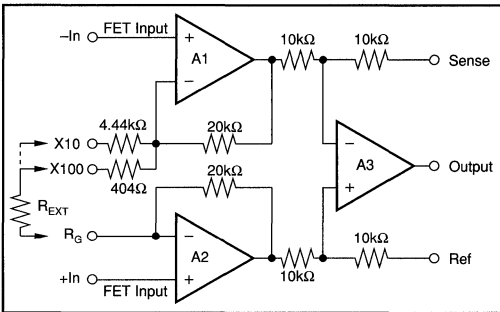
FIGURE 4. Use External Gain Set Resistor.

Where it is necessary to keep the input amplifiers from saturating or increasing the overall gain, then the gain of the output amplifier can be increased from unity by using the circuit in Figure 5.

The values of the resistors in Figure 5 are in the following table.

O/P GAIN	R_1 and R_3 Ω	R_2 Ω
2	1200	2740
5	1000	511
10	1500	340
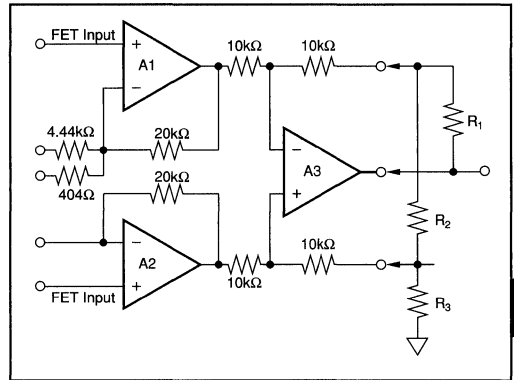
FIGURE 5. Increasing Output Amplifier Gain.

Matching of R_1 and R_3 is required to maintain high common-mode rejection (CMR), R_2 sets the gain and may be varied without effect on CMR.

To ensure that the effects of temperature are minimized when altering the gain with external components, it is very important to use low tempco resistors. When connecting the output sense, ensure that series resistance is minimized because resistance present will degrade CMR.
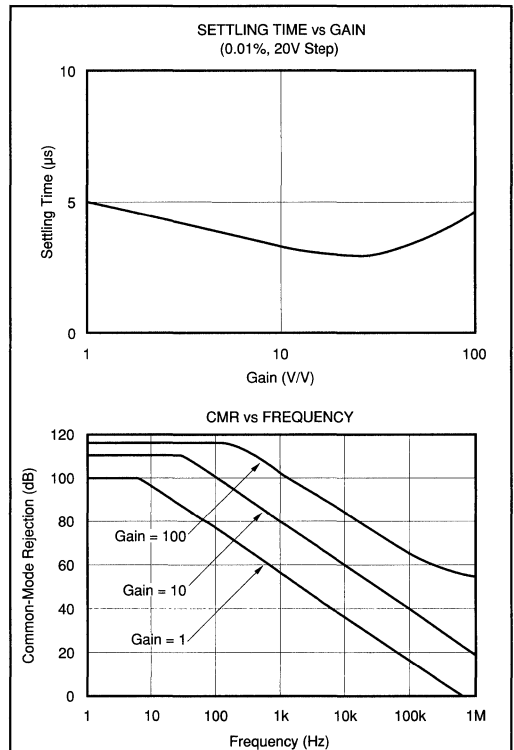
FIGURE 6. Typical INA Settling Time and CMR.

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Some applications may require programmable gains. This may be realized with Figure 7.
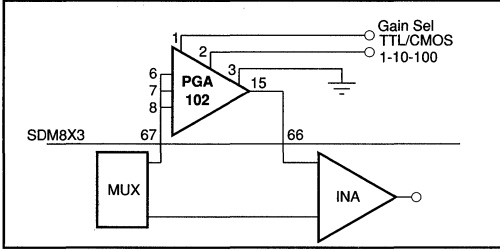
FIGURE 7. Setting Programmable Gains.

SAMPLE/HOLD AMPLIFIER

The Sample/Hold amplifier (S/H) is used to track the incoming signal and "hold" the required instantaneous value so that it does not change while the ADC is carrying out its conversion. Timing for the S/H may be derived from the STATUS output of the ADC, with care being taken to comply with the SDM timing considerations.

Capacitors with high insulation resistance and low dielectric absorption such as Teflon™, polystyrene or polypropylene should be used as storage elements. (Polystyrene should not be used above +80°C.) Teflon™ is recommended for high temperature operation. Care should be taken in the printed circuit layout to minimize stray capacitance and leakage currents from the capacitor to minimize charge offset and droop errors. The use of a guard ring driven by the S/H output around the pin connecting to the hold capacitor is recommended. (Refer to the application board layout for an example of this.)

The value of the external hold capacitor determines the droop rate, charge offset and acquisition time of the S/H, Figure 8. Droop rate for the SDM is specified with a hold capacitor value of 4700pf. There is a trade-off between
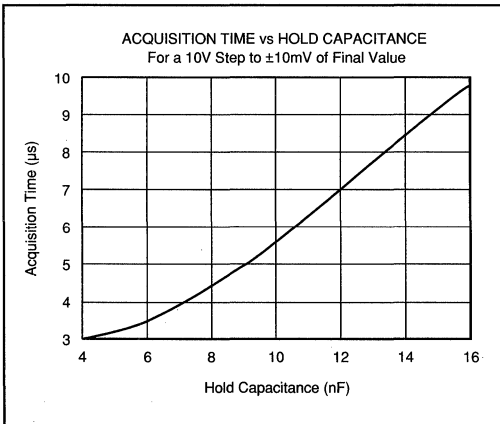
acquisition time and droop rate, as the hold capacitor is increased in value it takes longer to charge, and hence there is a corresponding increase in acquisition time and reduction in droop rate. The droop rate is determined by the amount of leakage present in the SDM, board leakage and the dielectric absorption of the hold capacitance. The hold capacitor is also a compensation element for the S/H and should not be reduced below 2nf for good stability. The offset error in sample mode is not affected by the hold capacitor. However, during the transition to hold mode there is approximately 5pC of charge injected into the hold capacitor, causing an offset error that has been nulled for use with a 5nf hold capacitor. Any other value for the hold capacitor will cause a minor but fixed hold mode offset to be introduced, and is proportional to the change in value from 5nf. Therefore, the SDM should be offset nulled with the S/H in hold mode.

ANALOG-TO-DIGITAL CONVERTER

This circuit element converts the analog voltage presented by the sample/hold amplifier to a digital number in binary format under control of the digital signals detailed in Figure 9. The converter can convert unipolar and bipolar signals in the range 10V and 20V. It can be calibrated to remove gain and offset errors from the entire system. The converter contains its own clock, voltage reference, and microprocessor interface with 3-state outputs. The converter will normally be used to digitize signals to 12-bit resolution, but it can be short-cycled to provide 8-bit resolution at higher speed. The digital output is compatible with 8- or 16-bit data buses, the data format being selected by control signals as detailed in Figure 9.

CE	$\overline{CS}$	R/$\overline{C}$	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
◊	0	0	X	0	Initiate 12-bit conversion
◊	0	0	X	1	Initiate 8-bit conversion
1	∨	0	X	0	Initiate 12-bit conversion
1	∨	0	X	1	Initiate 8-bit conversion
1	0	∨	X	0	Initiate 12-bit conversion
1	0	∨	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

FIGURE 9. Control Input Truth Table.

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure). Thus, with the SDM connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV

FIGURE 8. Acquisition Time vs Hold Capacitance for a 10V Step Settling to ±10mV of Final Value.

below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Figure 13).

NO MISSING CODES
(DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

The SDM is guaranteed to have no missing codes to 12-bit resolution over it's respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An SDM connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The SDM specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition 7FFH to 800H.

Bipolar offset error for the SDM is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

OPERATING INSTRUCTIONS
OPERATING MODES

The SDM can operate in one of two modes, namely serial and overlap, as shown in Figure 10. In serial mode, control of the device is such that a multiplexer channel X is first selected, time is then allowed for the instrumentation amplifier to settle, the sample/hold amplifier is set to HOLD mode and finally a conversion is carried out. This procedure is then repeated for channel Y. Faster throughput can be obtained using overlap mode. While a conversion is being
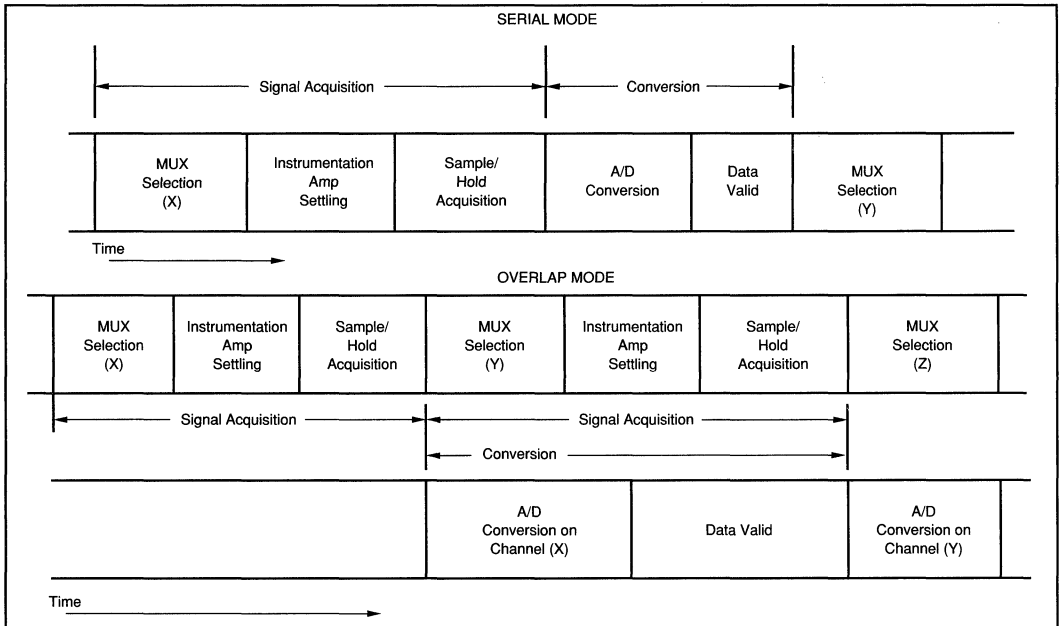
FIGURE 10. Serial and Overlap Modes of Operation.

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carried out by the ADC on a voltage from channel X held on the sample/hold, channel Y is selected and the multiplexer and instrumentation amplifier allowed to settle. In this way, the total throughput time is limited only by the sum of the sample/hold acquisition time and the ADC conversion time.

CALIBRATION – UNIPOLAR

If adjustment of unipolar offset and gain are not required, then the gain set potentiometer in Figure 11 (Unipolar operation) may be replaced with a 50Ω, 1% metal film resistor, and the offset network replaced with a connection from pin 23 to ground.
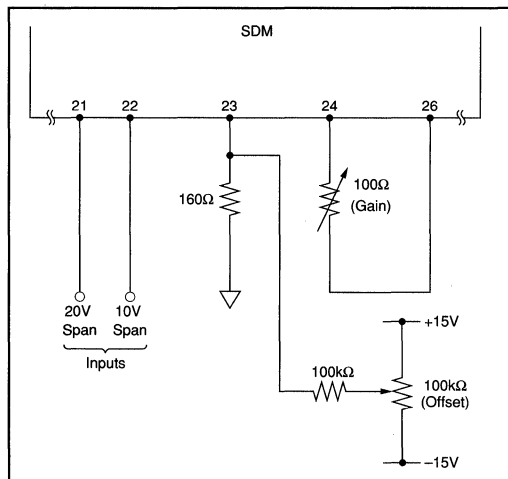
FIGURE 11. Unipolar Calibration.

CALIBRATION - BIPOLAR

If adjustment of bipolar offset and gain are not required then the gain set and offset potentiometers in Figure 12 (Bipolar operation) may both be replaced with 50Ω, 1% metal film resistors.
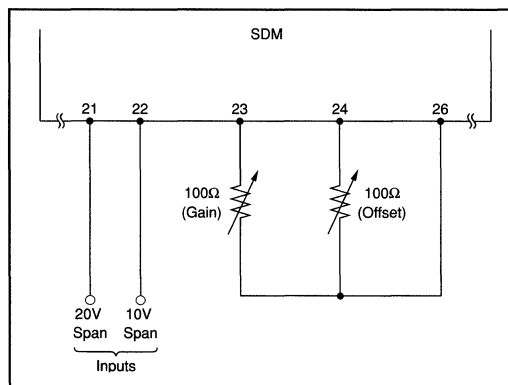
FIGURE 12. Bipolar Calibration.

CALIBRATION - GENERAL

The input voltage ranges of the ADC are 0-10V, ±5V and ±10V. Calibration in all ranges is achieved by adjusting the offset and gain potentiometers (indicated in Figures 11 and 12) such that the 000 to 001 code transition takes place at +1/2LSB from full-scale negative (–FS) and the FFE to FFF transition takes place at –3/2LSB from full-scale positive (+FS). The procedure is therefore to select the required range from Figure 13, apply the specified (–FS+1/2LSB) voltage to any selected input channel and adjust the offset potentiometer for the 000 to 001 transition. The (+FS–3/2LSB) voltage should then be applied to the same channel and the gain potentiometer adjusted for the FFE to FFF transition. The offset should always be made before the gain adjustment.

FULL-SCALE RANGE	000 TO 001 TRANSITION VOLT.	FFE TO FFF TRANSITION VOLT.	1LSB EQUALS
0–10V	+0.0012V	+9.9963V	2.44mV
±5V	–4.9988V	+4.9963V	2.44mV
±10V	–9.9976V	+9.9927V	4.88mV

FIGURE 13. Code Transition Ranges.
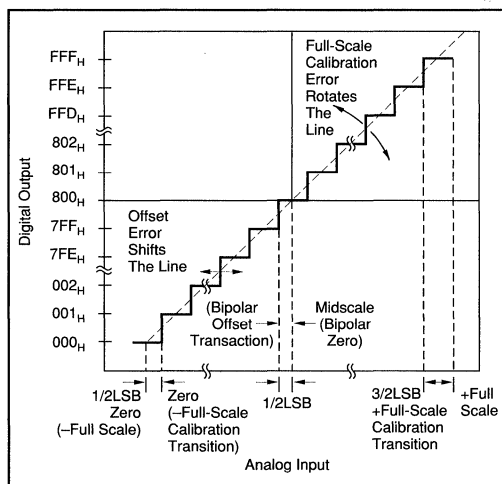
FIGURE 14. SDM Transfer Characteristic Terminology.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

It should be noted that the multiplexer/instrumentation amplifier section and sample/hold plus ADC section of the SDM have separate power connections. This is to enable more flexible grounding techniques to be implemented, Figures 15, 16. It also facilitates the use of independent decoupling of the analog front-end power supply, and the ADC plus associated digital circuitry power supply if desired. In this way, a separately decoupled analog front-end can be made to be substantially more immune to power supply noise generated by the ADC circuitry than if the

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power supplies to the two sections were directly connected. This feature is important where low-level signals are in use or high input signal noise immunity is desired.

The output section has three grounds:

Pin 25 Analog Common, A/D Converter
Pin 34 S/H Amp Digital Input Reference
Pin 19 Digital Common, A/D Converter

The input section has one ground:

Pin 53 Common for digital MUX-inputs and power supply decoupling.

All grounds have to be interconnected externally to the SDM, and it is recommended that all grounds are connected

via one track to a single point as close as possible to the SDM. To check that the grounding structure is correct, the ground tracking should be sketched and a grounding "tree" should result whereby all grounds route to a central point.

In general, layout should be such that analog and digital tracks are separated as much as possible with coupling between analog and digital lines minimized by careful layout. For instance, if the lines must cross they should do so at right angles to each other. Parallel analog and digital lines should be separated from each other by a pattern connected to common.
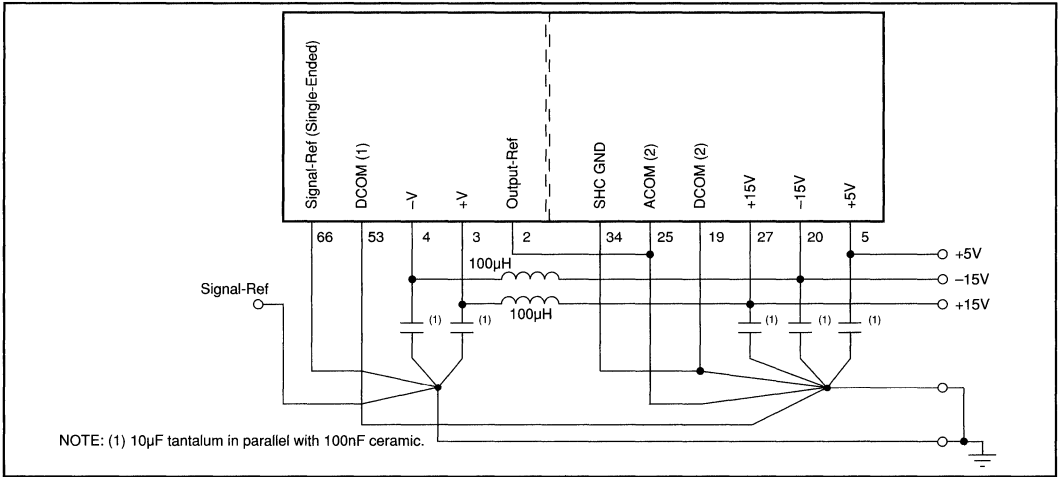
FIGURE 15. Recommended Decoupling of Power Supplies.
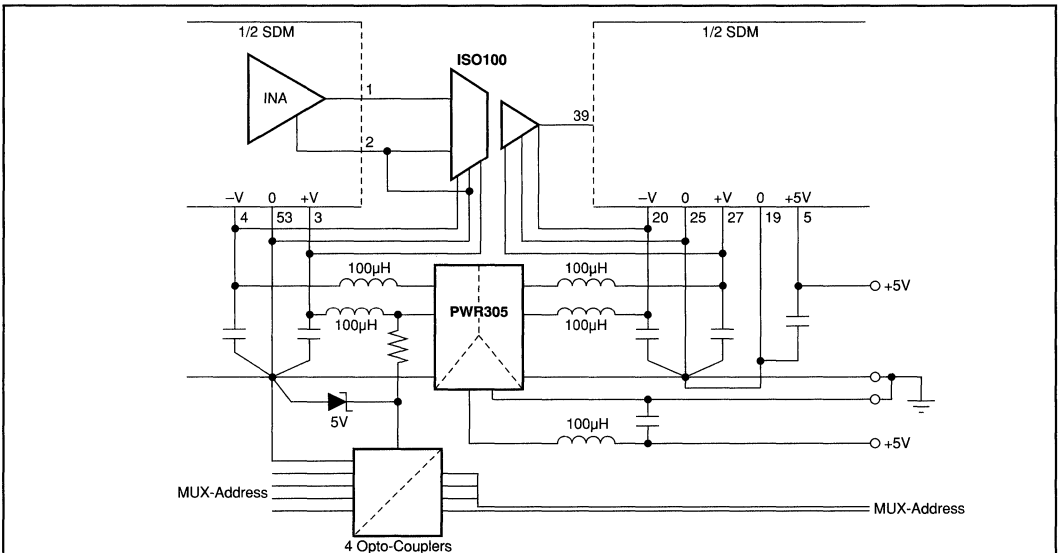
FIGURE 16. Galvanic Isolation Between Analog and Digital Signals.

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For Immediate Assistance, Contact Your Local Salesperson
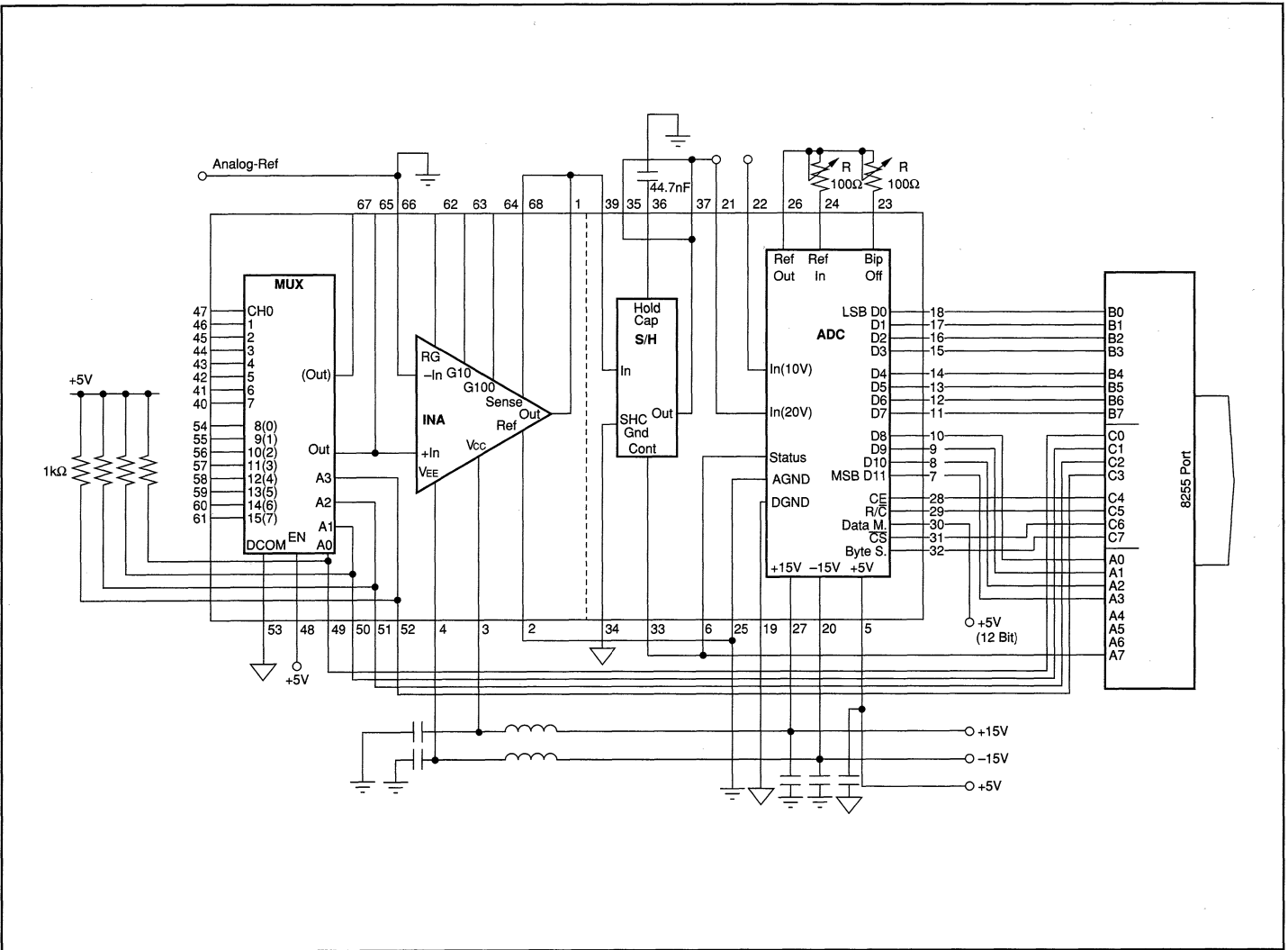
FIGURE 17. The SDM Connected to an Input/Output Port.
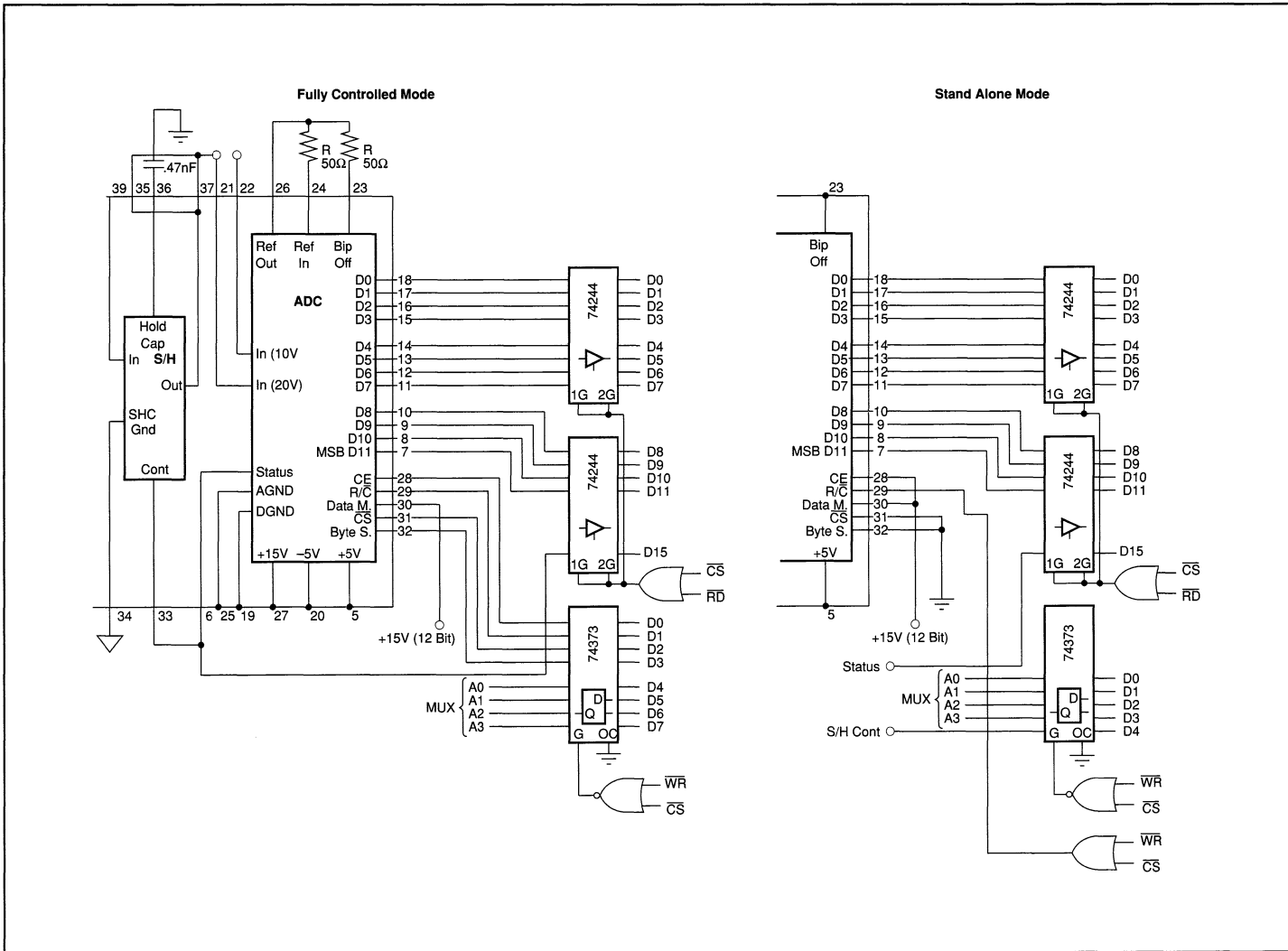
FIGURE 18. The SDM Connected to a 16-Bit-BUS.
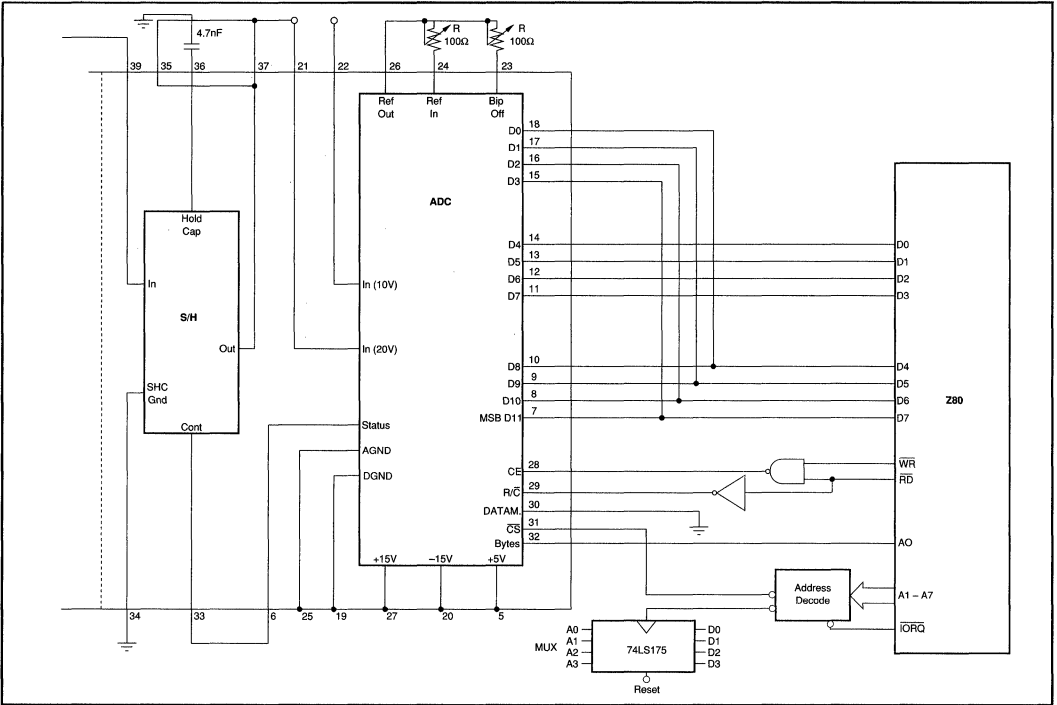
FIGURE 19A. SDM on the Z80 Interface.
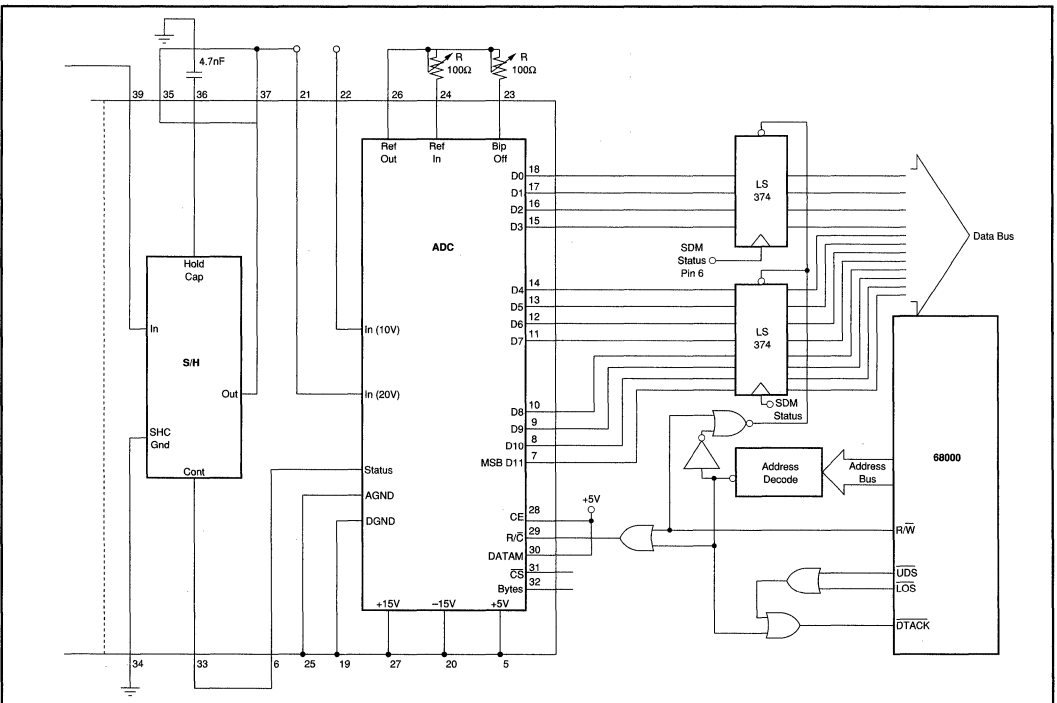
FIGURE 19B. 68000/SDM Interface.

Burr-Brown IC Data Book—Data Conversion Products
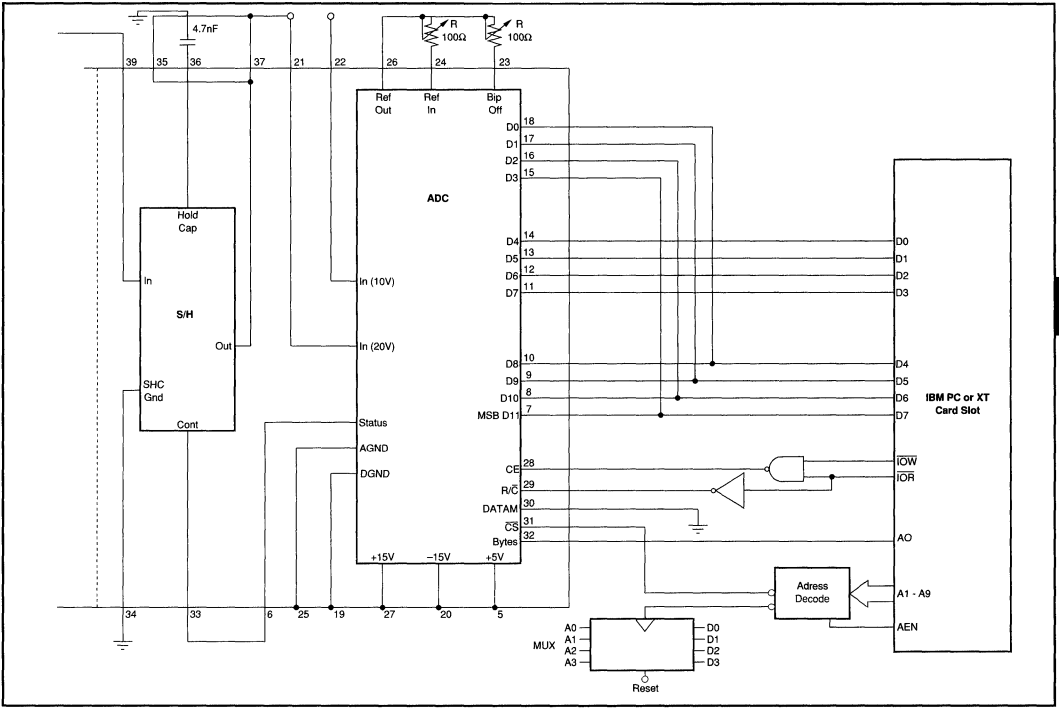
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FIGURE 19C. IBM PC SDM Interface.
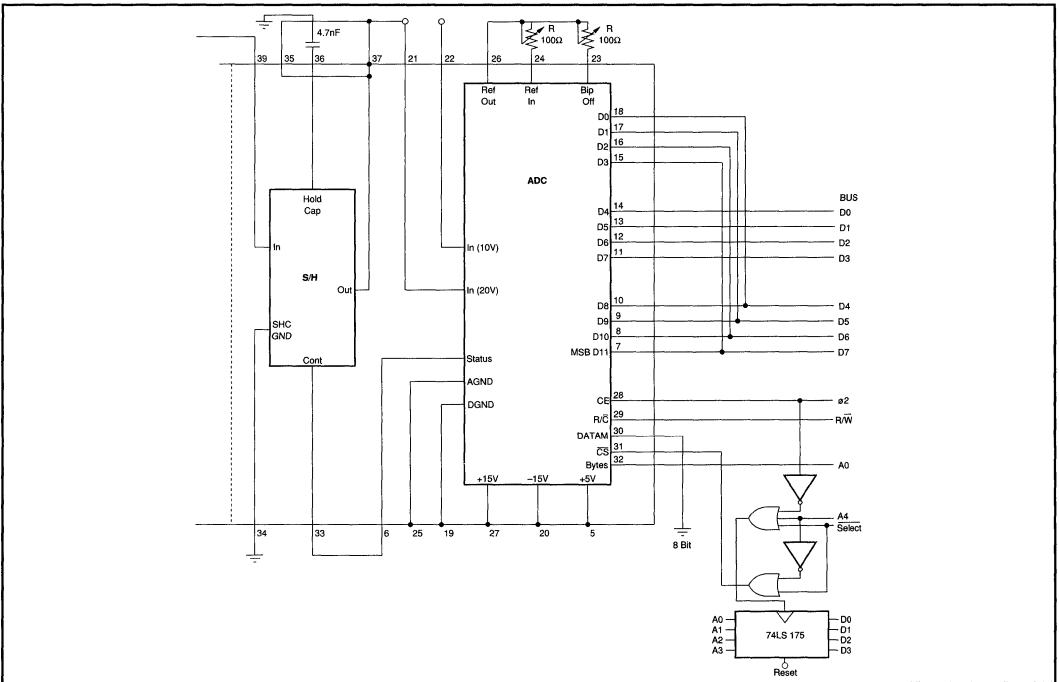
FIGURE 20. SDM on the 6502 BUS.

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CONTROLLING THE SDM

The Burr-Brown SDM family can be easily interfaced to most microprocessor systems, as shown in Figures 17-20. The microprocessor may control each conversion, or the converter may operate in a stand-alone mode controlled only by the R/C input.

STAND-ALONE OPERATION

The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Control of the converter is accomplished by a single control line connected to R/C. In this mode CS and BYTE SELECT are connected to LOW and CE and DATA MODE are connected to HIGH. The output data are presented as 12-bit words.

Conversion is initiated by a High-to-Low transition of R/C. The three-state data output buffers are enabled when R/C is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In each case the R/C pulse must remain low for a minimum of 50ns.

Figure 21 illustrates timing when conversion is initiated by an R/C pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/C and are enabled for external access of the data after completion of the conversion. Figure 22 illustrates the timing when conversion is initiated by a positive R/C pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/C. A new conversion is started on the falling edge of R/C, and the three-state outputs return to the high impedance state until the next occurrence of a high R/C pulse. Table I lists timing specifications for stand-alone operation.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the BYTE SELECT input, which is latched upon receipt of a conversion start transition. BYTE SELECT is latched because it is also involved in enabling the output buffers. No other control inputs are latched. If BYTE SELECT is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if BYTE SELECT is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	50			ns
t_{DS}	STS Delay from R/C			200	ns
t_{HDR}	Data Valid After R/C Low	25			ns
t_{HS} 86X	STS Delay After Data Valid	300	500	1000	ns
t_{HS} 87X		100	300	600	ns
t_{HRH}	High R/C Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE I. Stand-Alone Mode Timing.
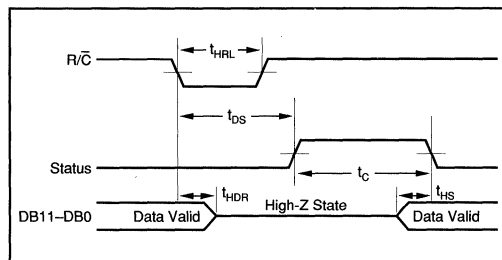
FIGURE 21. R/C Pulse Low—Outputs Enabled After Conversion.
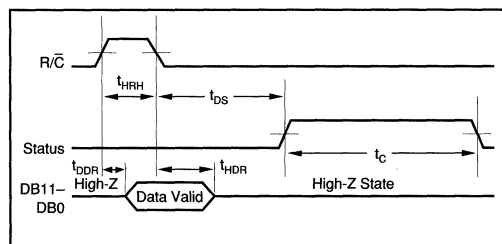
FIGURE 22. R/C Pulse High—Outputs Enabled Only Where R/C is High.

Conversion Start

A conversion is initiated by a transition on any of three logic inputs (CE, CS, and R/C)—refer to Figure 9. The last of the three to reach the required state start the conversion and thus all three may be dynamically controlled. If necessary, they may change state simultaneously, and the nominal delay time is independent of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Conversion Cycle Timing of the Digital Specifications.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SDM	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 23. 12-Bit Data Format for 8-Bit Systems (connected as Figures 18 and 19).

The STATUS output indicates the state of the converter by being high only during a conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore, data is not valid. During this period additional transitions of the three control inputs will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if BYTE SELECT changes state after the beginning of conversion, any additional start conversion transition will latch the new state of BYTE SELECT, possibly resulting in an incorrect conversion length (8 bit versus 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four conditions are met: R/C high, STATUS low, CE high, and CS low. In this condition the data lines are enabled according to the state of the inputs DATA MODE and BYTE SELECT. See Read Cycle Timing for timing relationships and specification.

In most applications the DATA MODE input will be hardwired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When DATA MODE is high, all 12 outputs lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus and the state of the BYTE SELECT is ignored.

When DATA MODE is low, the data is presented in the form of two 8-bit bytes, with selection of each byte by the state of BYTE SELECT during the read cycle.

The BYTE SELECT input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When BYTE SELECT is low, the byte addressed contains the 8MSBs. When BYTE SELECT is high, the byte addressed contains the 4LSBs from the conversion followed by four zeros that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 23. The design of the SDM guarantees that the BYTE SELECT input may be toggled at any time without damage to the output buffers occurring.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the status output has gone low. In those situations requiring the fastest possible access to the data, the read may be started as much as (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Read Cycle Timing for these timing relationships.

APPLICATIONS INFORMATION
ASSEMBLY OF SURFACE MOUNT PACKAGES

There are several assembly methods for the LCC versions of the SDM8XX. The associated advantages and disadvantages of three methods are outlined below.

1. DIRECT SURFACE MOUNT ONTO PCB

ADVANTAGES	DISADVANTAGES
Ease of assembly	Difficult to inspect solder joints
Low cost	Difficult to clean
Low weight	Choice of board material important in
Small footprint size	wide temperature range applications

In wide temperature applications it is important to match the coefficients of thermal expansion of the board and the SDM8XXL. Below is a list of materials and their approximate coefficients of linear thermal expansion.

MATERIAL	(ppm/°C)
Alumina (96%) - SDM Package	6-7
Copper-clad-Invar (50% Cu)	9
(30% Cu)	6
(10% Cu)	3
Epoxy-Kevlar (60% Kevlar)	6
Polyimide-Kevlar (40% Kevlar)	6
Beryllia	5
Polyimide-glass (x-axis)	12
(y-axis)	14

Kevlar™ E.I. du Pont de Nemours & Co.

2. ATTACHMENT OF SURFACE MOUNT EDGE CLIPS

ADVANTAGES	DISADVANTAGES
Ease of Inspection	Extra cost
Easy cleaning	Extra assembly
Thermal expansion taken up by the flexing of the edge clips	

ASSEMBLY

The edge clips are attached to the edges of the SDM8XXL as in Figure 24 before the device is mounted on to the board.
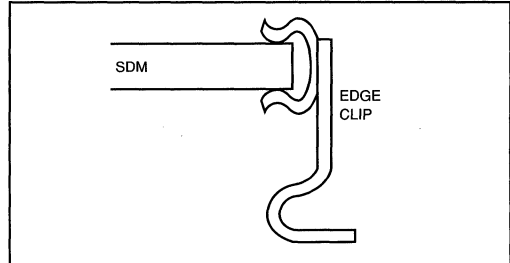
FIGURE 24. Edge Clip Assembly.

SUPPLIERS OF EDGE CLIPS

USA	USA
DIE-TECH INC., R.D. 1, Sipe Road, York Haven, PA 17370 USA PHONE: (717) 938-6771	NAS Electronics, 381 Park St., Hackensack, NJ 07602 USA PHONE: (201) 343-3156
EUROPE	EUROPE
SEMI-DICE (UK) Ltd, Buckingham House, Mineral Lane, Chesham, Bucks. HP5 2AU UK PHONE: 0494 771275	NASBRIT Ltd, Wester Goudi Ind. Est. Dundee DD2 4UX UK PHONE: 0382 622222

SDM862/3/872/3

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

3. SURFACE MOUNT SOCKET

ADVANTAGES	DISADVANTAGES
Board thermal expansion not so critical Ease of component replacement	Cost Extra height (if critical)

Below is the name and address of a supplier of a 68-pin surface mountable socket.

The part number is: Socket   212-068-012

Spring cover   CCS-004

USA	EUROPE
Methode Electronics INC, Interconnect Products Div. 1700 Hick Road, Rolling Meadows, TX 75050 USA PHONE: (312) 392-3500	Lucas Methode Connectors Ltd, Halifax Road Ingrow Bridge, Keighley, Yorkshire BD21 5HR UK PHONE: 0535 603282

General Comments

The advantages and disadvantages of all the methods mentioned above are for general use of surface mount components. Every user will find that the importance of these factors will depend on his application and situation.

EVALUATION BOARD

For the engineer who wishes to evaluate the SDM family, Burr-Brown has designed printed circuit boards on a single 'Eurocard' (shown here for LCC only). These boards enable the design engineer to experiment with various accuracy improvement techniques which are described below. Special consideration has been given to the grounding and circuit layout techniques required when dealing with 12-bit analog signals.

The printed circuit board has been designed so that the solutions to several of the problems likely to be encountered by the user can be examined.

It should not be thought that every user is required to adopt all of the techniques used on the circuit board. In many applications very few external components will be required.

However, in following the application guidelines illustrated by the circuitry and accompanying notes, the designer will be able to select and adapt the solutions most suited to their won particular application or problem area.

Provisions for the following are made on the LCC PC board:

—68 pin LCC socket (Burr-Brown Part No. MC0068).
—8 differential or 16 single-ended inputs.
—Input filtering with overvoltage protection for each channel.
—Socket for quad D-type flip-flop 74175 (MUX address latches).
—7 additional I.C. sockets for easy interfacing to various BUS systems (connection by wire wrap techniques).
—2 voltage regulators (15V).
—LC power supply decoupling.

The layout pays particular attention to the requirements when operating with precision analog signals. This requires strict separation of the analog and digital areas. Analog and digital commons are totally separated and connected together only at the commons of the supply voltage. All common lines are low resistance and low inductance.

SUPPLY VOLTAGES

In order to avoid coupling between the external supply voltage 15V supplies, 2 voltage regulators (78M15, 79L15) are provided on the PC board. The unregulated supply voltage may vary from ±17V to ±25V.

The MUX/INA section and SHC/ADC section of the SDM have separate supply lines which can be inductively decoupled. This is recommended in order to suppress the high frequency noise which comes from the ADC during conversion.

The power supply rejection of the instrumentation amplifier reduces with increasing frequency. If high frequency noise on the supplies is not decoupled it will be injected into the signal path and cause errors. This effect can be particularly pronounced when using the 'overlap' mode since the instru-

SDM862/872						SDM863/873				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8					–
H	L	L	H	H	9					–
H	L	H	L	H	10					–
H	L	H	H	H	11					–
H	H	L	L	H	12					–
H	H	L	H	H	13					–
H	H	H	L	H	14					–
H	H	H	H	H	15					–

FIGURE 25. Channel Select Truth Table.

mentation amplifier is settling to a new analog value while the ADC is still carrying out the previous conversion.

The digital supply voltage is +5V and is also LC-filtered.

All supply lines are bypassed with a 10μF tantalum and a 100nF ceramic capacitor situated **as close as possible** to the package.

If the voltage regulators for the ±15V are not used, small inductors for decoupling of the supply voltages are recommended. If inductors are not fitted a dynamic ground loop will be created from supply lines via bypass capacitors to analog common.

INPUT PROTECTION

The multiplexer is protected up to an input voltage which can exceed the supply voltage by a maximum of 20V. This means, that with ±15V supply voltage, the input voltage can be ±35V without damage. This is also the case when the supply voltages are switched off (0V). The maximum input voltage can then be ±20V. For higher overvoltage protection a series resistor has to be used. The current via the multiplexer should be limited to 20mA absolute maximum, 1mA is preferred. For example, a 10kΩ series resistor would give an additional 10V overprotection.

For much higher overvoltages (e.g. 100V), high value series resistors cannot be used as offset errors would result. In practice, a combination of series resistors and diodes is used. The diodes are connected to ±15V and will conduct whenever the input voltage exceeds the ±15V supply voltage. The diodes are selected by signal source impedance, as well as filter resistance, as the diode leakage current across the series resistor can cause offset and linearity errors. In this circuit, IN4148 together with 10kΩ are used.

INPUT FILTER

Processor noise can be induced in the analog ground. Input filtering is therefore recommended for analog data acquisition. Such high frequency noise signals can cause dynamic overload of the instrumentation amplifier resulting in non-linear behavior. This leads directly to digitizing errors.

The design of the filter takes into account the characteristics of the SDM and of the signal source.

The following points have to be considered:

—The stray capacitance, output capacitance of the multiplexer and input capacitance of the instrument amplifier (up to 80pf in some cases) has to be discharged in order to minimize errors caused by 'charge sharing.'

—The series resistor limits the current in the protection diodes, but it also has to be selected for the required filter time constant.

—The noise rejection of the filter has to be >80db in order to satisfy a 12-bit A/D conversion.

As well as considering the above, different calculations have to be carried out for single and differential input signals.
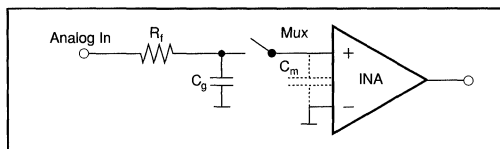
FIGURE 26.

Single-Ended Measurement

R_f limits the maximum input current through the protection diodes. In this case, R_f has been chosen as 10kΩ and together with the capacitor C_g, forms the input filter time constant (C_g = 0.47μF). The time constant must be chosen according to the requirements of the input signal bandwidth and noise rejection. The multiplexer capacitance (C_m) is discharged mainly by C_g. This means C_g has to be sufficiently large compared with C_m or charged via R_f prior to re-sampling of the signal.
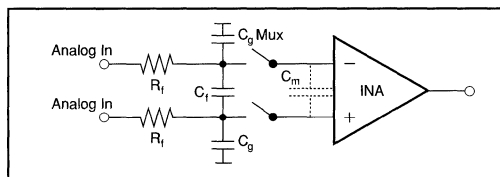
FIGURE 27.

Differential Measurement

Capacitor C_f, is used for limiting the input signal frequency. The bandwidth is calculated as follows:

$$F_f = \frac{1}{4\pi\,R_f C_f} \quad \text{IF } C_f >> C_g$$

When selecting the value of C_f, it should be noted that C_m has to be discharged when switching the multiplexer channels. This means that the voltage error of C_f (induced by 'charge sharing' with C_m) has to be smaller than 1LSB. Therefore, C_f should have a minimum value of a 0.47μF. The resistors R_f, together with the source impedance, have to be sufficiently small in order to recharge C_f prior to signal sampling. This prevents errors in the signal value caused by the charge stored on C_m by the previously selected channel.

The 2 capacitors C_g form together with R_f a common-mode filter. This filter greatly improves accuracy in a noisy environment (decrease of common-mode rejection of instrumentation amplifier with increasing frequency).

For good common-mode filter operation, both time constants R_f and C_g should match each other within 2%. Additional errors will be induced by a mismatch.

Selected values are: C_f = 0.47μF, C_g = 10nF, R_f = 10kΩ. The filter reduces the signal slew rate so that the instrumentation amplifier can follow the voltage variation of the signal with the noise component eliminated.

In general, all measurements which require more than a gain of 10 should be done in differential mode. Single ended

measurements should be limited to applications where current sources are measured via shunts or where signal voltages in the range of some volts are available.

Bus-Interface

As the outputs of the SDM are BUS compatible, only a few ICs are necessary to interface to various BUS systems. For such interfacing, 20-pin IC sockets are provided. Wiring is by wire wrap to the BUS connector.

Setting of Various Modes

Circuit Board positions are provided for the connection of 'jumpers' as follows:

J1, J2—ADC analog input volt age settings.

J3—Set for differential (SDM8X3) or single ended (SMD8X2) operation.

J4—Instrumentation amplifier gain settings.

(a) 16 input channels, single ended:
—Use SDM8X2
—Consider single-ended filtering

—Connect J3 (pin 66) to common

(b) Differential inputs
—Use SDM8X3
—Consider differential filtering
—Connect J3 (pin 66) to pin 67

(c) Analog input

$\pm10V$	Connect J1 to pin 21
	Connect J2 to pot P2 (100Ω)
$\pm5V$	Connect J1 to pin 22
	Connect J2 to pot P2 (100Ω)
0 to +10V:	Connect J1 to pin 22
	Connect J2 to junction of R_1/R_2

(d) Gain of instrumentation amplifier

G = 1	Jumper J4 open
G = 10	Jumper J4 to pin 63
G = 100	Jumper J4 to pin 64

Other gains: use additional resistor between pin 62 and pin 63 (see section on Instrumentation Amplifier) as low tempco resistor is recommended in order to minimize gain drift.

INPUT FILTER AND PROTECTION CIRCUITRY

SINGLE-ENDED

DIFFERENTIAL

Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common
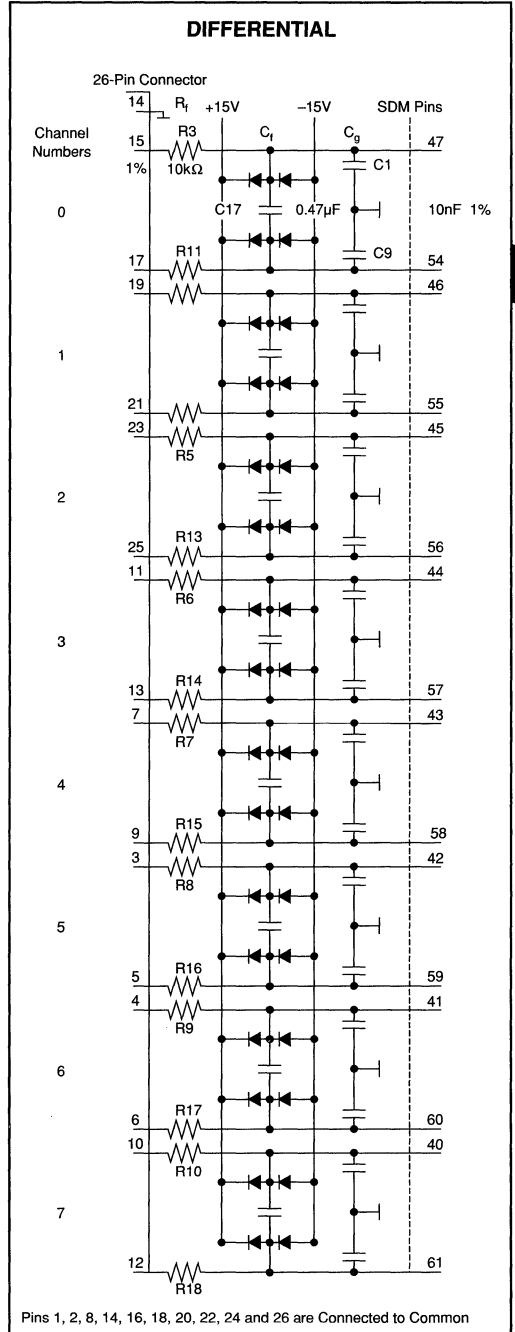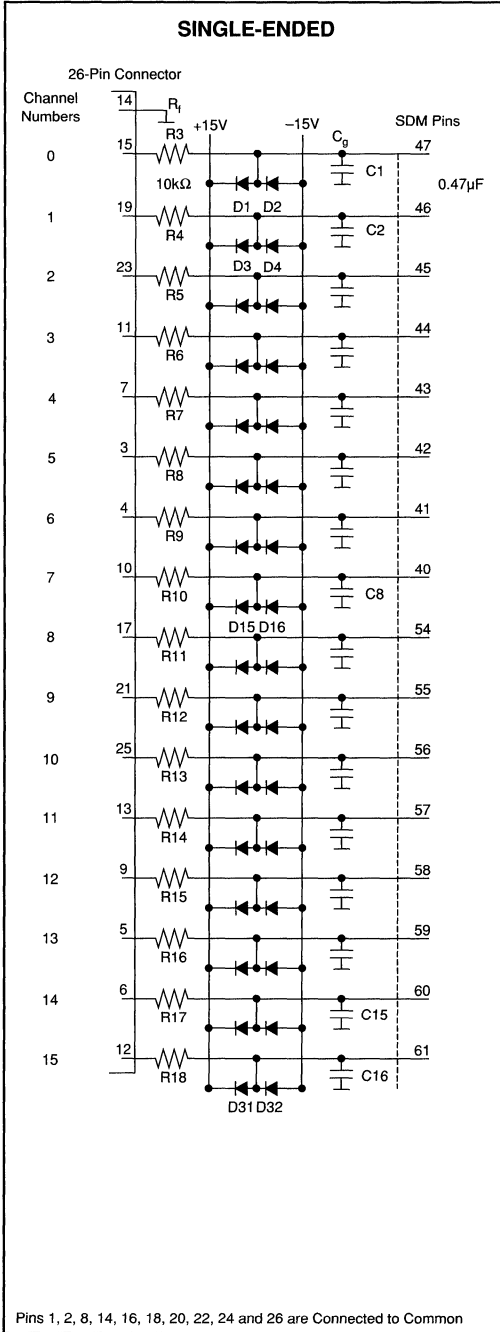
SDM862/3/872/3

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PCB COMPONENT LAYOUT
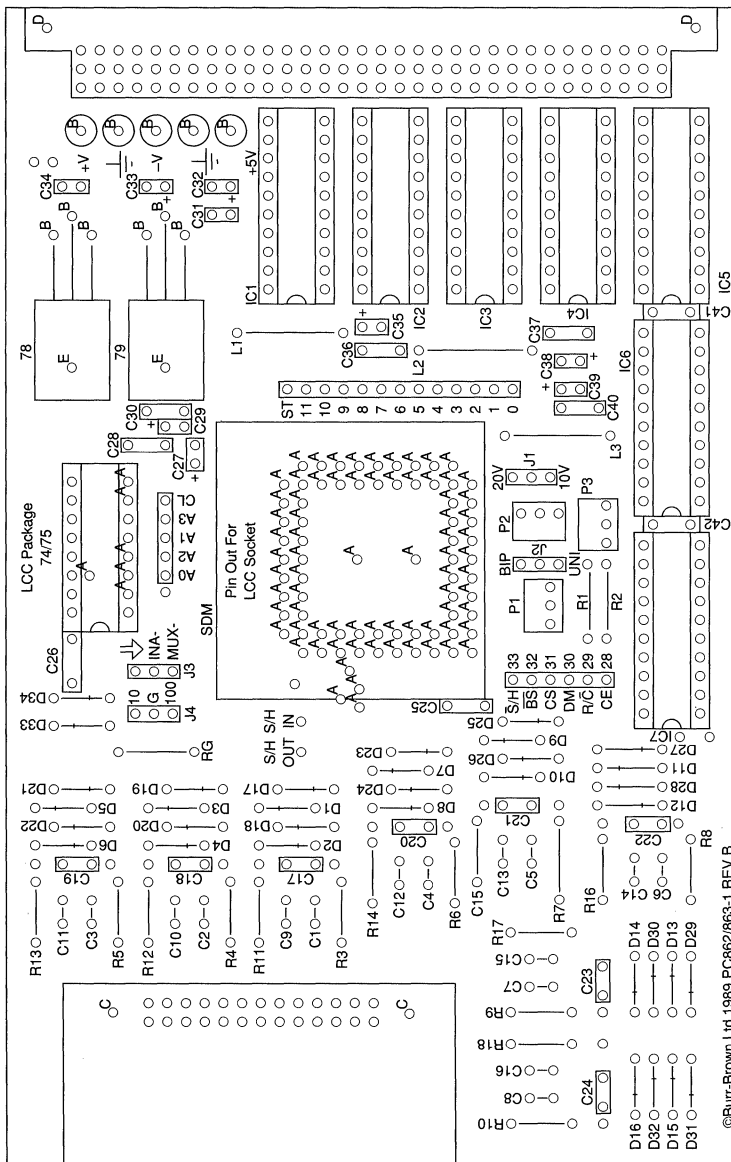
NOTE: (1) NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2
(2) NOT DRAWN TO SCALE

P.C.B. LAYOUT
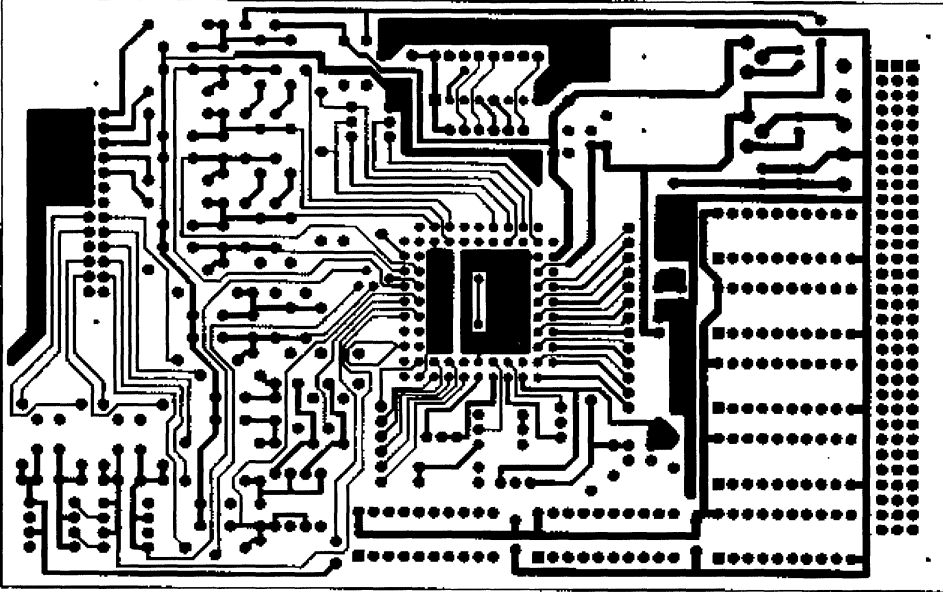
NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2
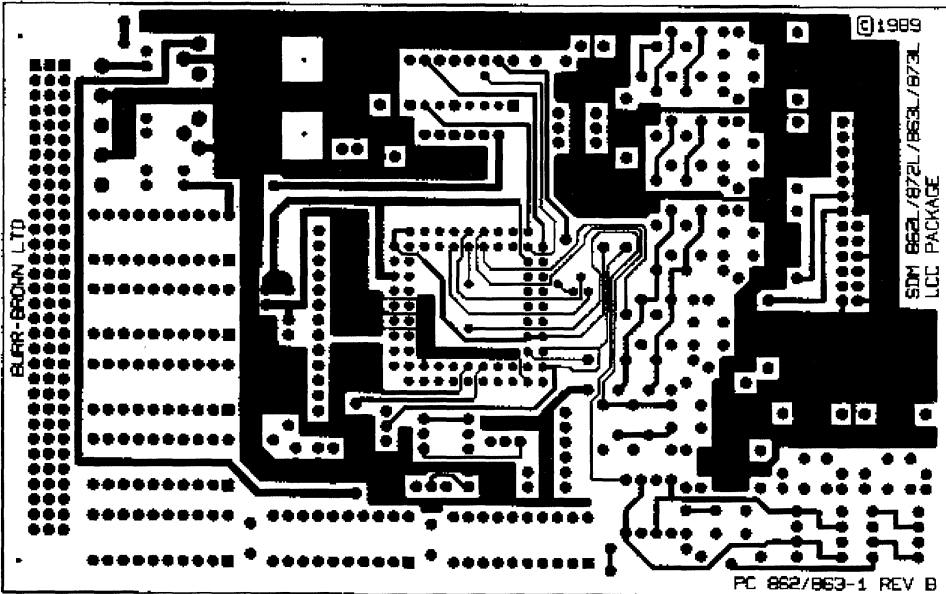
NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2

SDM862/3/872/3

2

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

PC 862/863-1 REV B

CIRCUIT DIAGRAM—SDM PC BOARD
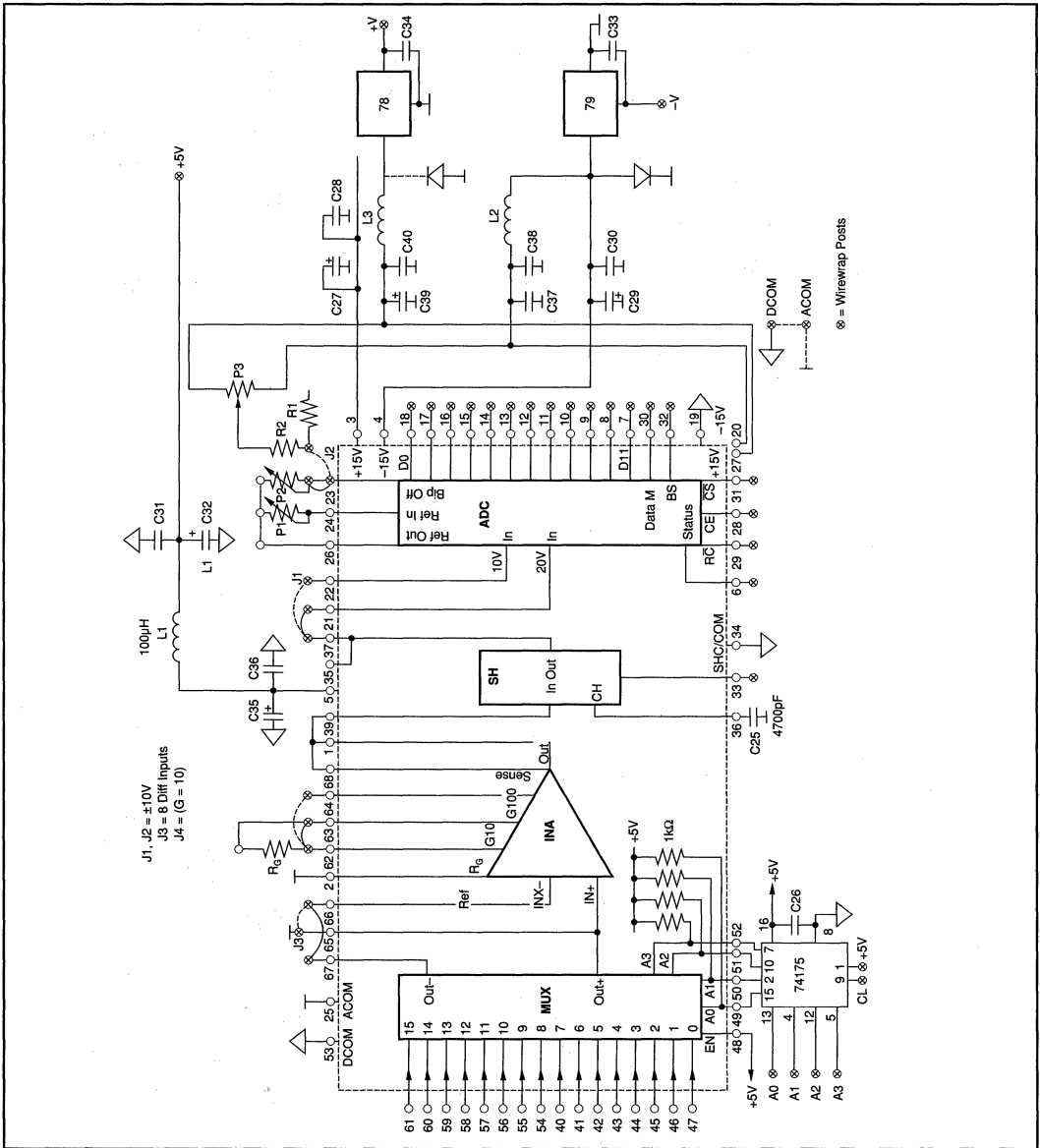
P.C.B. COMPONENTS PARTS LIST

R1	100Ω } For 0–10V Settling	C26	10nF Ceramic	P3	100kΩ **0–10V Range Only**
R2	100kΩ	C27, C29, C35 } 10µF Tantalum (Decoupling)		L1...L3	100µH (Decoupling)
R3...R18	10kΩ 1%	C32, C38, C39		D1...D32	1N4148 (Input Protection Diodes)
C1...C16	0.47µF—Single Ended Input Mode	C28, C30, C31 } 100nF Ceramic (Decoupling)		D33, D34	1N4007
	10nF 1%—Differential Input Mode	C36, C37, C40		78	MC78M15CG
C17...C24	0.47µF—Differential Input Mode	C33, C34	0.33µF Tantalum	79	MC79L15CG
C25	4.700pF (Polypropylene, Polystyrene or Teflon™)	P1	100Ω	**74175**	74LS175
		P2	100Ω ±5V, **±10V Range Only**	LCC Socket	MC0068

UNLESS OTHERWISE MARKED—RESISTORS ARE 1/4W, 5%, CAPACITORS ARE 10%

Teflon™ E.I. du Pont de Nemours & Co.

3 Digital-to-Analog Converters

Burr-Brown offers a wide range of Digital-to-Analog (D/A) converters designed to meet critical requirements for industrial, audio and waveform-generation applications.

Industrial instrumentation D/As with 12-, 16-, and 18-bit resolutions are available in industry standard pinouts. There are also new smaller size, lower-power D/As specified over the extended industrial temperature range, –40°C to +85°C which are introduced in this data book. Dual and Quad D/As are also available in the product line.

Audio D/A Converters

Burr-Brown continues to be the industry performance leader in audio DACs, with new entries such as dual 18-bit PCM67/69A and 20-bit PCM1702. These DACs take advantage of Burr-Brown's laser-trimming abilities to make the industry's leading audio converters in terms of THD, Noise, and Sound Quality.

High Speed D/A Converters

Burr-Brown's DAC600, DAC650 and the new DAC601 and DAC602 offer excellent price-to-performance ratios for applications such as Direct Digital Synthesis (DDS) and Arbitrary Waveform Generation (ARB). Both parts have guaranteed dynamic specifications, as well as extensive characterization plots for many different combinations of update rates and output frequencies. DAC600 and DAC650 are the best choice for high-speed 12-bit applications.

DIGITAL SIGNAL PROCESSING DIGITAL-TO-ANALOG CONVERTERS   **Boldface = NEW**

Model	Reso-lution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range	Signal-to-Noise + Distortion Ratio (dB)	Total Harmonic Distortion (dB)	Temp Range[1]	Pkg[2]	Page No.
DSP-Compatible Digital Interface (Single—DSP201, Dual—DSP202):									
DSP201	18	±0.006	—	±3V	86, f_{OUT} = 2kHz	–90	Ind	DDIP	3.245
DSP202	18	±0.006	—	±3V	86, f_{OUT} = 2kHz	–90	Ind	DDIP	3.245

NOTES: (1) Com = 0°C to +70°C, Ind = (–25°C to +85°C). (2) DDIP = 0.6" wide DIP.

VERY HIGH SPEED DIGITAL-TO-ANALOG CONVERTERS   **Boldface = NEW**

Model	Resolution (Bits)	Max Update Rate	SFDR (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package	Max Power Dissipation (mW)	Page No.
DAC600	12	256MHz	74dB SFDR	–1V, –20mA	Parallel	–5.2	68 PLCC	1.3W	3.17
DAC601	12	256MHz	76dB SFDR	0 to –1V, –20mA	Parallel	–5.46	DIP, SOIC	480W	3.29
DAC602	12	100MHz	78dB SFDR	0 to –1V, –20mA	Parallel	±5.0	DIP, SOIC	490W	3.32
DAC650	12	500MHz	–70dB SFDR	±1V, ±20mA	Parallel	±15, ±5	68 LEAD	2.0W	3.35

3

DIGITAL-TO-ANALOG CONVERTERS

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS   Boldface = NEW

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (μs)	Output Range	Temp Range[1]	Pkg[2]	Page No.
Very High Resolution	DAC729	18	±0.00075	5	±1mA, −2mA; +5V, +10V, ±5V, ±10V	Com	DDIP	3.103
General	DAC700	16	±0.0015	1	−2mA	Com, Ind, Mil	DDIP	3.55
Purpose	DAC701	16	±0.0015	8	+10V	Com, Ind, Mil	DDIP	3.55
	DAC702	16	±0.0015	1	±1mA	Com, Ind, Mil	DDIP	3.55
	DAC703	16	±0.0015	8	±10V	Com, Ind, Mil	DDIP, SO	3.55
Lowest Cost	DAC1600	16	±0.003	8 typ	±10V	Com	DDIP	A
Bus Interface:								
16-Bit Parallel	DAC712	16	±0.003	12	±10V	Ext	DIP, SO	3.77
8-Bit Port Interface	**DAC713**	**16**	**±0.003**	**10**	**±10V**	**Ext**	**DIP**	**3.88**
Serial Interface	**DAC714**	**16**	**±0.003**	**10**	**±10V**	**Ext**	**DIP**	**3.92**
16-Bit Parallel	DAC707	16	±0.003	8	±10V	Com, Ind, Mil	DDIP	3.65
Serial/8-bit Parallel	DAC708	16	±0.003	1	±1mA, −2mA	Com, Ind, Mil	DDIP	3.65
Serial/8-bit Parallel	DAC709	16	±0.003	8	±5V, ±10V, +10V	Com, Ind, Mil	DDIP	3.65
Dual,Ser./8-bit Par.	DAC725	16	±0.003	8	±10V	Com, Ind	DDIP	3.96
Industry Standard	DAC7541A	12	±0.012	1	0 to 1mA	Com, Ind, Mil	DIP, SO	3.210
Ind. Std. w/Latch	DAC7545	12	±0.012	2	0 to 1mA	Com, Ind, Mil	DIP, SO	3.218
Dual w/Bus Interface:								
Octal, Serial Interface	DAC7800	12	±0.012	0.8	0 to 1mA	Ext	DIP, SO	3.225
8-bit Port Interface	DAC7801	12	±0.012	0.8	0 to 1mA	Ext	DIP, SO	3.225
12-bit Port Interface	DAC7802	12	±0.012	0.8	0 to 1mA	Ext	DIP, SO	3.225
Single w/Bus	DAC8043	12	±0.012	0.25 typ	0 to 1mA	Ind, Com	DIP, SO, Die	3.238
Flexible Bus Interface:								
Industry Standard Pinout	DAC667	12	±0.006	4	±2.5V, ±5V, ±10V +5V, +10V	Com, Ind, Mil	DIP	3.46
	DAC811	12	±0.006	4	±5V, ±10V, +10V	Com, Ind, Mil	DDIP, SO	3.114
Small, Low Cost	DAC813	12	±0.006	4	±5V, ±10V, +10V	Com, Ext, Mil	DIP, SO	3.123
Lowest Cost	DAC1201	12	±0.018	4 typ	±5V, ±10V, +10V	Com	DDIP	A
Serial Input	DAC56	16	±0.012	1.5 typ	±3V	Com	DIP, SO	3.3
Quad, Serial	**DAC1204**	**12**	**±0.012**	**0.5**	**±1mA**	**Com**	**SO**	**3.134**
Quad, Serial	**DAC1214**	**12**	**±0.012**	**0.5**	**±1mA**	**Com**	**SO**	**3.134**
Industry Standard, General Purpose	DAC80	12	±0.012	0.3, 3 typ	±1mA, −2mA; +5V +10V, ±5V, ±10V	Com	DDIP	3.8
Dual, 12-bit Port	DAC2813	12	±0.006	6	±10, 0 to 10	Ext	DDIP	3.141
Dual, Multiplying Serial Port	DAC2814	12	±0.012	10	+V_S, −1.4V −V_S, +1.4V	Ext	DDIP	3.150
Dual Multiplying 8-bit Port	DAC2815	12	±0.012	10	+V_S, −1.4V −V_S, +1.4V	Ext	DDIP	3.161
QUAD, 12-bit Port	DAC4813	12	±0.012	6	±10	Ext	DDIP	3.172
QUAD, Multiplying Serial Port	DAC4814	12	±0.012	10	+V_S, −1.4V −V_S, +1.4V	Ext	DDIP	3.180
Dual Multiplying 8-bit Port	DAC4815	12	±0.012	10	+V_S, −1.4V −V_S, +1.4V	Ext	DDIP	3.192
Dual Multiplying DAC	DAC7528	8	±0.012	0.18	0 to 1mA	Ind, Com	DIP, SO, Die	3.202

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = −25°C to +85°C, Ext = −40°C to +85°C, Mil = −55°C to +125°C. (2) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, SO = small outline surface mount.
"A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

STILL AVAILABLE BUT NOT IN DATA BOOK

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (μs)	Output Range	Temp Range	Pkg	Page No.
Industry Standard,	DAC85H	12	±0.012	3 typ	+10V, ±5V, ±10V	Ind	DDIP	A
General Purpose	DAC87H	12	±0.012	3 typ	+10V, ±5V, ±10V	Mil	DDIP	A

NOTES: "A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

BURR - BROWN®
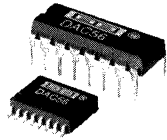
DAC56

Monolithic 16-Bit Resolution
DIGITAL-TO-ANALOG CONVERTER

DAC56

3

DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **COMPLETE D/A CONVERTER:**
  Internal Voltage Reference
  ±3V Output Operational Amplifier
  Pinout Allows I_{OUT} (±1.0mA) Option
  No external components required

● **0.012% LINEARITY ERROR MAX**

● **12-BIT MONOTONICITY GUARANTEED OVER 0°C TO +70°C**

● **±5V TO ±12V POWER SUPPLY**

● **SETTLING TIME: V_{OUT} = 1.5µs;**
  I_{OUT} = 350ns

● **SERIAL DATA INPUT: Binary Two's Complement**

● **16-PIN PLASTIC DIP AND SOIC**

APPLICATIONS

● **PROCESS CONTROL**

● **ATE PIN ELECTRONICS LEVEL SETTING**

● **CLOSED-LOOP SERVO-CONTROL**

● **AUTO-CALIBRATION CIRCUIT FOR A/D BOARDS**

● **UP-GRADE REPLACEMENT FOR MULTIPLYING D/A**

● **X-Y PLOTTER**

● **DSP PROCESSOR BOARDS**

DESCRIPTION

The DAC56 is a complete 16-bit monolithic D/A converter. Completely self-contained with a stable, low noise, internal zener voltage reference; high-speed current switches; a resistor ladder network; and a low noise output operational amplifier all on a single monolithic chip. The DAC56 operates over a wide power supply range from ±5V to ±12V.

Differential linearity error (DLE) is guaranteed to meet specifications without external adjustment. However, provisions for an externally adjustable circuit controlling the MSB error, the differential linearity error at bipolar zero, makes the DLE at BPZ essentially zero and provides for high system performance. The I/V amplifier stage includes an output current limiting circuit to protect both amplifier and load from excessive current. This assures the user of high system reliability.

A high-speed interface is capable of clocking in data at a rate of 10MHz max, and its interface logic contains a serial data clock (input), serial data (input) and latch-enable (input). Serial data is clocked MSB first into a 16-bit register and then latched into a 16-bit parallel register.

The DAC56 is packaged in a 16-pin plastic DIP and 16-pin SOIC.

BURR - BROWN®
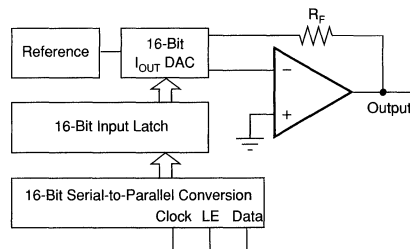
SPECIFICATIONS

ELECTRICAL

All specifications at +25°C, and power supply voltage of ±5V unless otherwise noted.

PARAMETER	CONDITIONS	DAC56 MIN	DAC56 TYP	DAC56 MAX	UNITS
DIGITAL INPUT					
Resolution			16		Bits
Digital Input Level: [1] V_{IH}		+2.4		$+V_L$	V
V_{IL}		0		+0.8	V
$I_{IH} \cdot V_I = +2.7V$				+1	μA
$I_{IL} \cdot V_I = +0.4V$				−50	μA
Input Clock Frequency		10			MHz
ACCURACY					
Integral Linearity Error				±0.012	% of FSR[3]
Differential Linearity Error				±0.024	% of FSR
Gain Error				±1.5	% of FSR
Bipolar Zero Error				±0.5	% of FSR
Monotonicity	0°C to +70°C			12	Bits
TEMPERATURE DRIFT	0°C to +70°C				
Gain Drift			±60		ppm of FSR/°C
Bipolar Zero Drift			±20		ppm of FSR/°C
Linearity Drift				±0.012	% of FSR
Differential Linearity Drift				±0.024	% of FSR
POWER SUPPLY SENSITIVITY	$\pm V_S = \pm V_L = \pm 5VDC$				
Gain			±0.0045		% of FSR/%V
Bipolar Zero			±0.0015		% of FSR/%V
SETTLING TIME	to ±0.006% of FSR				
Voltage Output					
6V Step			1.5		μs
1LSB			1		μs
Current Output					
1mA Step	10 to 100Ω Load		350		ns
	1kΩ Load[3]		350		ns
Slew Rate			12		V/μs
ANALOG OUTPUT					
Voltage Output Configuration					
Bipolar Range		±2.66	±3.0	±3.34	V
Output Current		±8			mA
Output Impedance			0.1		Ω
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Range			±1		mA
Output Impedance			1.2		kΩ
WARMUP TIME		1			min
POWER SUPPLY REQUIREMENTS[4]					
Supply Voltage					
$+V_S$ and $+V_L$		+4.75	+5.00	+13.2	V
$-V_S$ and $-V_L$		−4.75	−5.00	−13.2	V
Supply Drain (No Load)					
+V ($+V_S$ and $+V_L = +5V$)			+10	+17	mA
−V ($-V_S$ and $-V_L = -5V$)			−25	−35	mA
+V ($+V_S$ and $+V_L = +12V$)			+12		mA
−V ($-V_S$ and $-V_L = -12V$)			−27		mA
Power Dissipation					
V_S and $V_L = \pm 5V$			175	260	mW
V_S and $V_L = \pm 12V$			468		mW
TEMPERATURE RANGE					
Specification		0		70	°C
Storage		−60		100	°C

NOTES: (1) Logic input levels are TTL-/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for DAC56 in the V_{OUT} mode. (3) Measured with an active clamp to provide a low impedance for approximately 200ns. (4) All specifications assume $+V_S$ connected to $+V_L$ and $-V_S$ connected to $-V_L$. If supplies are connected separately, $-V_L$ must not be more negative than $-V_S$ to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

PIN CONFIGURATION

DAC56

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DIGITAL-TO-ANALOG CONVERTERS
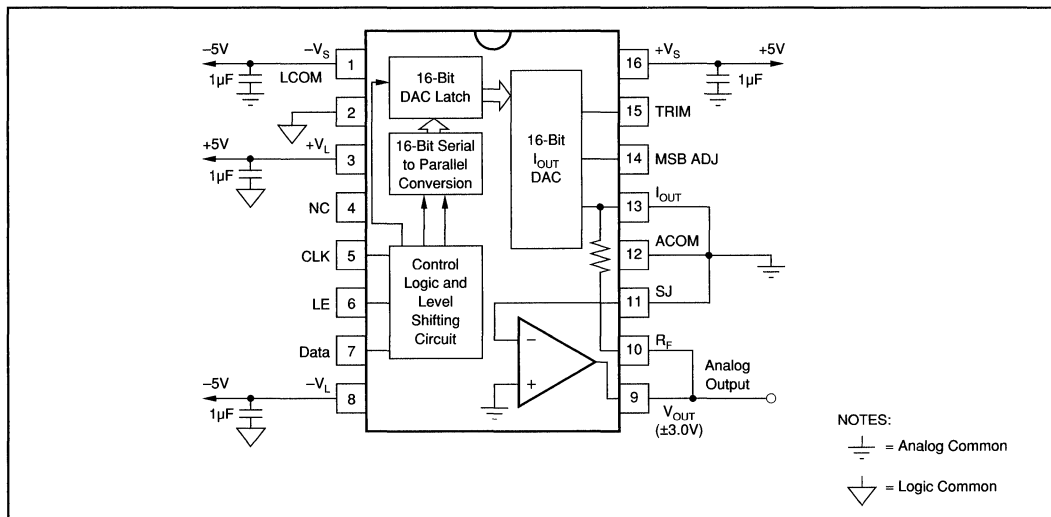
PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	$-V_S$	Analog Negative Supply
2	LCOM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	ACOM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

PACKAGE AND ORDERING INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC56P	16-Pin Plastic DIP	802
DAC56U	16-Pin SOIC	803

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage .... ±15VDC
Input Logic Voltage .... −1V to $+V_S/+V_L$
Power Dissipation 850mW
Operating Temperature .... −25°C to +70°C
Storage Temperature .... −80°C to +100°C
Lead Temperature (soldering, 10s) .... +300°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

OPERATING INSTRUCTIONS

The accuracy of a D/A converter is described by the transfer function as shown in Figure 1. Digital input to analog output converter relationships are shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift is due to the drift of the internal reference zener diode with temperature or time.

The converter is designed so that these drifts are in opposite directions. This way the bipolar zero voltage is virtually unaffected by variations in the reference voltage.

FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

TABLE I. Digital Input to Analog Output Relationship.
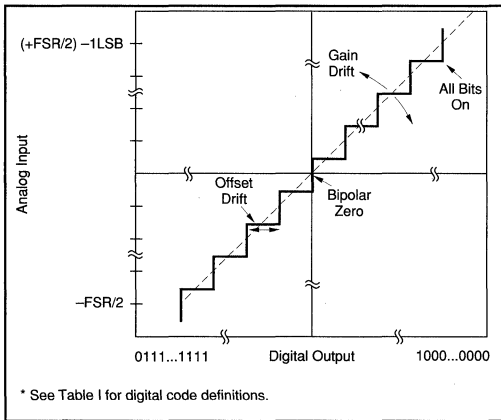
DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
$7FFF_H$	+ Full Scale	+2.999908	–0.999970
8000_H	– Full Scale	–3.000000	+1.000000
0000_H	Bipolar Zero	0.000000	0.000000
$FFFF_H$	Zero –1LSB	–0.000092	+0.030500µA

DIGITAL INPUT CODES

The DAC56 accepts serial input data (MSB first) in Binary Two's Complement form—Refer to Table I for input/output relationships.

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added as shown in the Connection Diagram (Figure 2), for optimum performance and noise rejection.

These capacitors (1µF tantalum recommended) should be connected as close as possible to the converter.
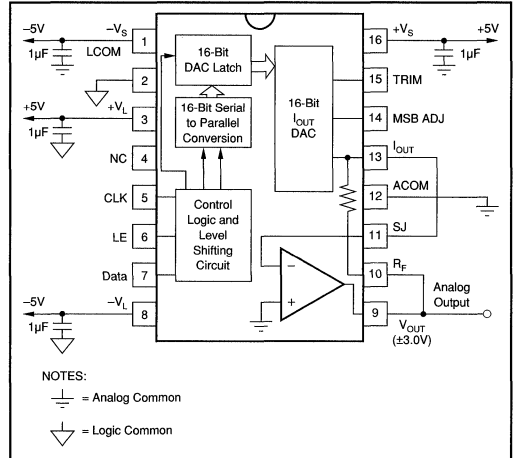
FIGURE 2. Connection Diagram.

MSB ERROR ADJUSTMENT (OPTIONAL)

Differential linearity error at all codes of the DAC56 is guaranteed to meet specifications without an external adjustment. However, if adjustment of the differential linearity error at bipolar zero is desired, it can be trimmed essentially to zero using the circuit as shown in Figure 3.
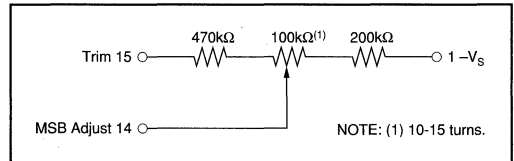
FIGURE 3. MSB Adjustment Circuit.

After allowing ample warm-up time (5 to 10 minutes) to assure stable operation, select the input code $FFFF_H$. Measure the output voltage using a 6-1/2 digit voltmeter and record the measurement. Change the digital input code to 0000_H. Adjust the 100kΩ potentiometer (TCR of 100ppm per °C or less is recommended) to make the output voltage read 1LSB more than the voltage reading of the previous code (ex. 1LSB = 92µV at FSR = 6V).

If the MSB adjustment circuit is not used, pins 14 and 15 should be left open.

NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 4. Input Timing Diagram.
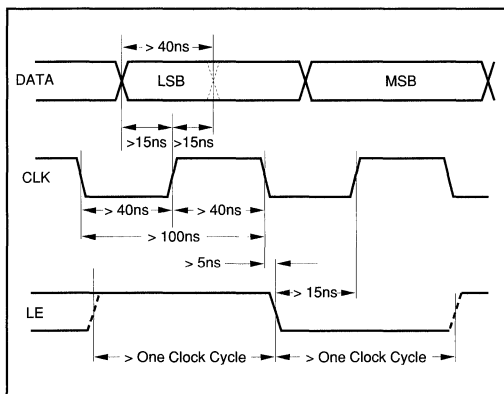
FIGURE 5. Input Timing Relationships.

INPUT TIMING CONSIDERATIONS

Figures 4 and 5 refer to the input timing required to interface the inputs of DAC56 to a serial input data stream. Serial data is accepted in Binary Two's Complement with the MSB being loaded first. Data is clocked in on positive going clock (CLK, pin 5) edges and is latched into the DAC input register on negative going latch enable (LE, pin 6) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are those that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

Figure 4 gives the general input format required for the DAC56. Figure 5 shows the specific relationships between the various signals and their timing constraints.

DAC56

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DIGITAL-TO-ANALOG CONVERTERS

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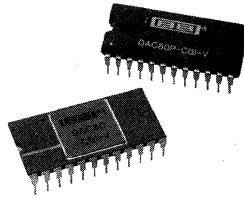
DAC80
DAC80P

Monolithic 12-Bit
DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **INDUSTRY STANDARD PINOUT**

● **FULL ±10V SWING WITH V_{cc} = ±12VDC**

● **DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE**

● **GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES**

● **±1/2LSB MAXIMUM NONLINEARITY: 0°C to +70°C**

● **SETTLING TIME: 4µs max to ±0.01% of Full Scale**

● **GUARANTEED MONOTONICITY: 0°C to +70°C**

● **TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic**

resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with voltage output only.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H.

DESCRIPTION

This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80 first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback

PDS-643E

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and ±V_CC = 12V or 15V unless otherwise noted.

PARAMETER	DAC80			UNITS
	MIN	TYP	MAX	
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (0°C to +70°C)[1]:				
V_{IH} (Logic "1")	+2		+16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	μA
I_{IL} (V_{IN} = +0.4V)			−180	μA
ACCURACY (at +25°C)				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
DRIFT (0°C to +70°C)[4]				
Total Bipolar Drift (includes gain, offset, and linearity drifts)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C[5]				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.06	±0.12	% of FSR
Gain: Including Internal Reference		±10	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	±3/4	LSB
Linearity Error 0°C to +70°C		±1/4	±1/2	LSB
Monotonicity Guaranteed	0		+70	°C
CONVERSION SPEED, V_{OUT} Models				
Settling Time to ±0.01% of FSR				
For FSR Change (2kΩ ‖ 500pF Load)				
with 10kΩ Feedback		3	4	μs
with 5kΩ Feedback		2	3	μs
For 1LSB Change		1		μs
Slew Rate	10			V/μs
CONVERSION SPEED, I_{OUT} Models				
Settling Time to ±0.01% of FSR				
For FSR change: 10Ω to 100Ω Load		300		ns
1kΩ Load		1		μs
ANALOG OUTPUT, V_{OUT} Models				
Ranges		±2.5, ±5, ±10, +5, +10		V
Output Current[6]	±5			mA
Output Impedance (DC)				Ω
Short Circuit to Common, Duration[7]		Indefinite		
ANALOG OUTPUT, I_{OUT} Models				
Ranges: Bipolar	±0.96	±1.0	±1.04	mA
Unipolar	−1.96	−2.0	−2.04	mA
Output Impendance: Bipolar	2.6	3.2	3.7	kΩ
Unipolar	4.6	6.6	8.6	kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
External Current (constant load)			2.5	mA
Drift vs Temperature		±10	±20	ppm/°C
Output Impedance		1		Ω
POWER SUPPLY SENSITIVITY				
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS				
±V_{CC}	±11.4		±16.5	VDC
Supply Drain (no load): +V_{CC}		8	12	mA
−V_{CC}		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480	mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C
Storage: Plastic DIP	−60		+100	°C
Ceramic DIP	−65		+150	°C

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For +V_{CC} less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire ±V_{CC} range. (7) Short circuit current is 40mA, max.

DAC80/80P

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DIGITAL-TO-ANALOG CONVERTERS

FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS

Voltage Models

(MSB) Bit 1	1		24	6.3V Ref Out
Bit 2	2		23	Gain Adjust
Bit 3	3		22	+V_{CC}
Bit 4	4		21	Common
Bit 5	5		20	Summing Junction
Bit 6	6		19	20V Range
Bit 7	7		18	10V Range
Bit 8	8		17	Bipolar Offset
Bit 9	9		16	Ref Input
Bit 10	10		15	V_{OUT}
Bit 11	11		14	$-V_{CC}$
(LSB) Bit 12	12		13	NC[1]

Current Models

(MSB) Bit 1	1		24	6.3V Ref Out
Bit 2	2		23	Gain Adjust
Bit 3	3		22	+V_{CC}
Bit 4	4		21	Common
Bit 5	5		20	Scaling Network
Bit 6	6		19	Scaling Network
Bit 7	7		18	Scaling Network
Bit 8	8		17	Bipolar Offset
Bit 9	9		16	Ref Input
Bit 10	10		15	I_{OUT}
Bit 11	11		14	$-V_{CC}$
(LSB) Bit 12	12		13	NC[1]

NOTE: (1) Logic supply applied to this pin has no effect.

ABSOLUTE MAXIMUM RATINGS

+V_{CC} to Common	0V to +18V
$-V_{CC}$ to Common	0V to –18
Digital Data Inputs to Common	–1V to +18V
Reference Output to Common	±V_{CC}
Reference Input to Common	±V_{CC}
Bipolar Offset to Common	±V_{CC}
10V Range R to Common	±V_{CC}
20V Range R to Common	±V_{CC}
External Voltage to DAC Output	–5V to +5V
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	100°C/W
Ceramic DIP	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	OUTPUT
DAC80-CBI-I	Ceramic DIP	Current
DAC80Z-CBI-I	Ceramic DIP	Current
DAC80-CBI-V	Ceramic DIP	Voltage
DAC80Z-CBI-V	Ceramic DIP	Voltage
DAC80P-CBI-V	Plastic DIP	Voltage

BURN-IN SCREENING OPTION		
MODEL	PACKAGE	BURN-IN TEMP. (160h)[1]
DAC80-CBI-V-BI	Ceramic DIP	+125°C
DAC80P-CBI-V-BI	Plastic DIP	+125°C

NOTE: (1) Or equivalent combination. See text.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC80P	24-Pin Plastic DIP	167
DAC80	24-Pin Ceramic DIP	125

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "–BI" to the base model number.

DICE INFORMATION

DAC80KD-V DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB)	15	$-V_{CC}$
2	Bit 2	16	V_{OUT}
3	Bit 3	17	Ref In
4	Bit 4	18	Bipolar Offset
5	Bit 5	19	Scale 10V FSR
6	Bit 6	20	Scale 20V FSR
7	Bit 7	21	NC
8	Bit 8	22	Sum Junct
9	Bit 9	23	COM
10	Bit 10	24	COM
11	Bit 11	25	$+V_{CC}$
12	Bit 12 (LSB)	26	Gain Adjust
13	NC	27	6.3V Ref Out
14	NC		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	118 x 121 ± 5	3.0 x 3.07 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum
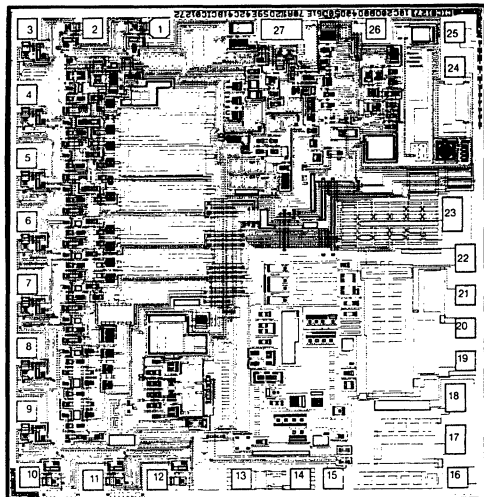
DAC80KD-I DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB)	15	$-V_{CC}$
2	Bit 2	16	I_{OUT}
3	Bit 3	17	Ref In
4	Bit 4	18	Bipolar Offset
5	Bit 5	19	Scale 10V FSR
6	Bit 6	20	Scale 20V FSR
7	Bit 7	21	Scale
8	Bit 8	22	NC
9	Bit 9	23	COM
10	Bit 10	24	COM
11	Bit 11	25	$+V_{CC}$
12	Bit 12 (LSB)	26	Gain Adjust
13	NC	27	6.3V Ref Out
14	NC		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	118 x 121 ± 5	3.0 x 3.07 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DAC80/80P

3

DIGITAL-TO-ANALOG CONVERTERS

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

DIGITAL INPUT		ANALOG OUTPUT		
		CSB Complementary Straight Binary	COB Complementary Offset Binary	CTC(1) Complementary Two's Complement
MSB ↓	LSB ↓			
000000000000		+Full Scale	+Full Scale	−1LSB
011111111111		+1/2 Full Scale	Zero	−Full Scale
100000000000		1/2 Full Scale −1LSB	−1LSB	−Full Scale
111111111111		Zero	−Full Scale	Zero

NOTE: (1) Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE I. Digital Input Codes.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C, and +70°C; 2) calculating the gain error with respect to the 25°C value, and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C, and 70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).
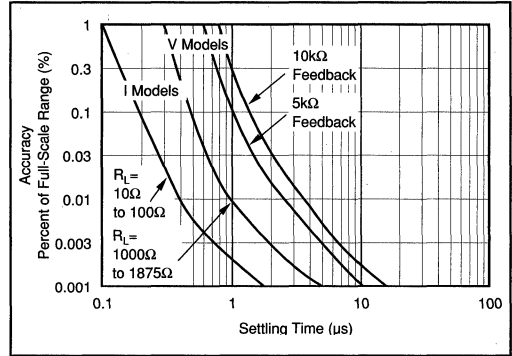
FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V (see Figures 11 and 12).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage range of ±1V and 0 to −2V (see Figures 11 and 12).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input
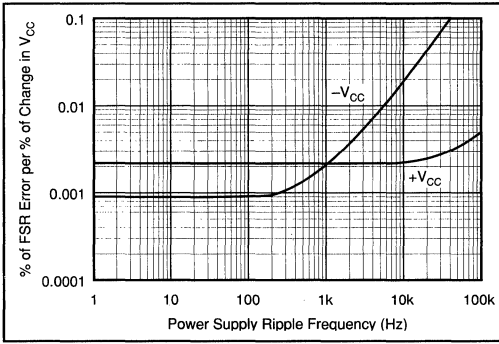
FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

(pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC80 digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC80 directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1µF tantalum) should be located close to the DAC80.

±12V OPERATION

All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, minimum, over the entire V_{CC} range.

No bleed resistor is needed from +V_{CC} to pin 24, as was needed with prior hybrid Z versions of DAC80. Existing ±12V applications that are being converted to the monolithic DAC80 must omit the resistor to pin 24 to insure proper operation.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.
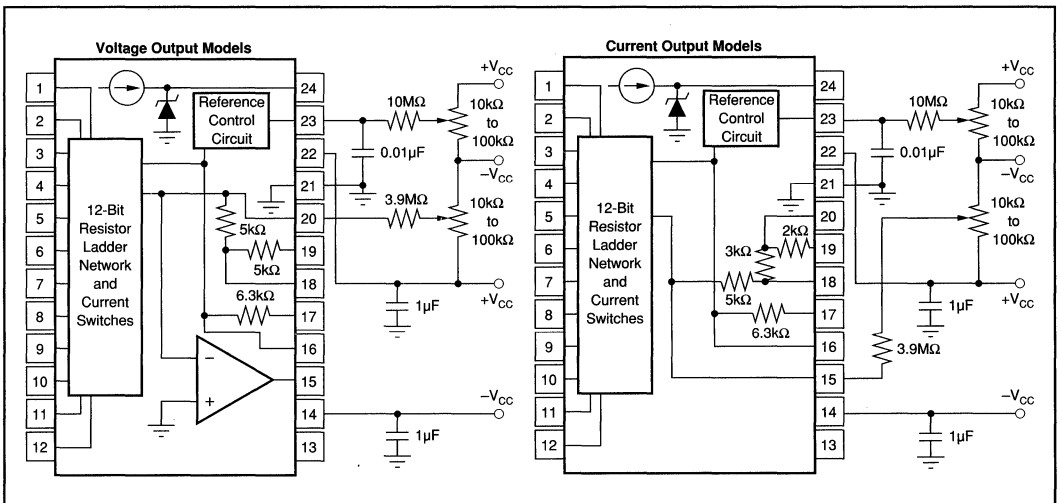
FIGURE 3. Power Supply and External Adjustment Connection Diagrams.
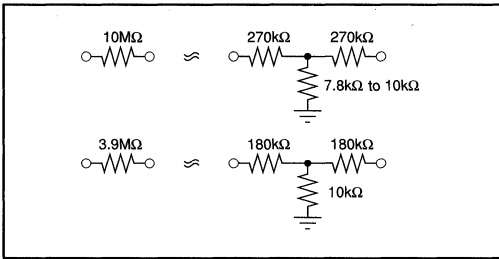
FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC80 must change the gain trim resistor on pin 23 from 33MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001µ1F to 0.01µF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.
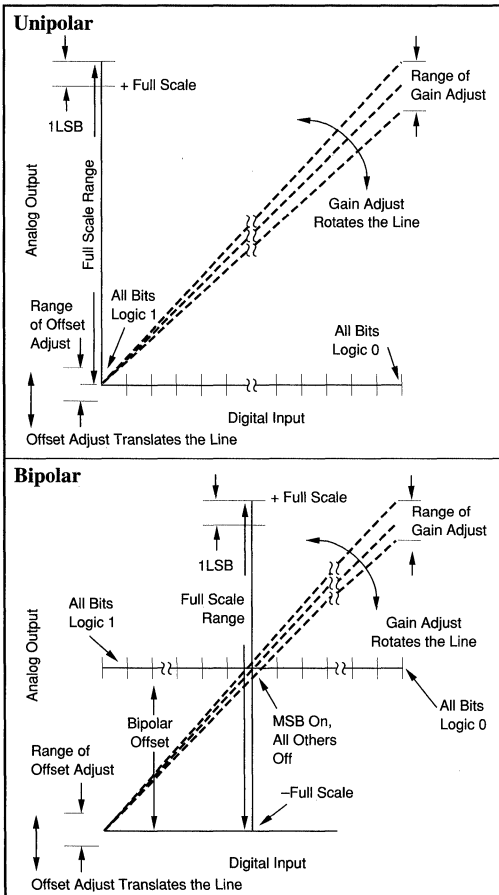
FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is –10V. See Table II for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

| DIGITAL INPUT | ANALOG OUTPUT | | | |
	VOLTAGE[1]		CURRENT	
MSB ⁻ LSB ↓ ↓	0 to +10V	±10V	0 to –2mA	±1mA
000000000000	+9.9976V	+9.9951V	–1.9995mA	–0.9995mA
011111111111	+5.0000V	0.0000V	–1.0000mA	0.0000mA
100000000000	+4.9976V	–0.0049V	–0.9995mA	+0.0005mA
111111111111	0.0000V	–10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488µA	0.488µA

NOTE: (1) To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE II. Digital Input/Analog Output.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V, ±5V, or ±2.5V; or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.
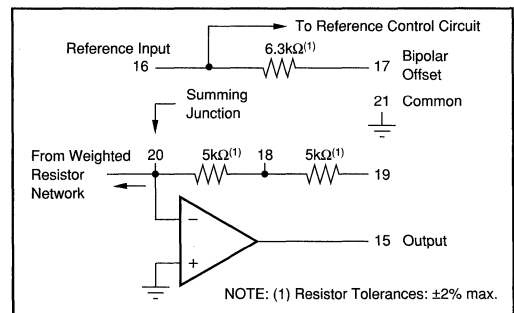
FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4µs for the 20V range and 3µs for the 10V range.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

TABLE III. Output Voltage Range Connections for Voltage Models.

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.
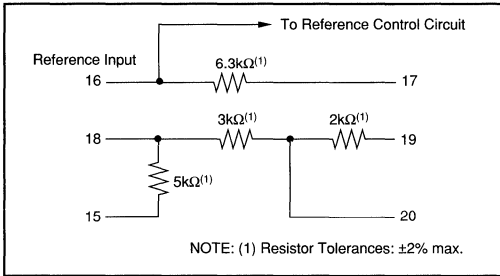
FIGURE 7. Internal Scaling Resistors.
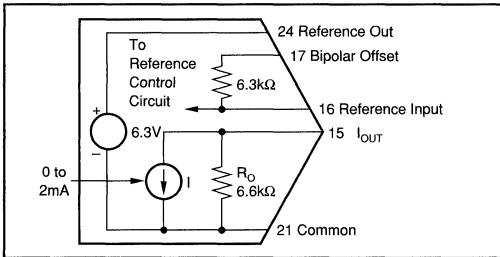
FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of
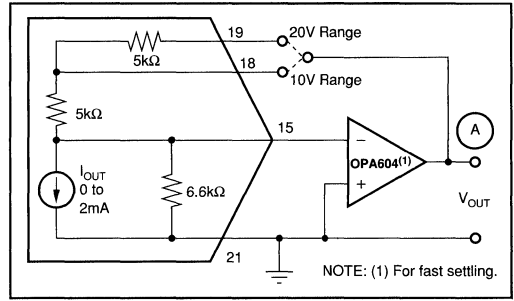
FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

the current output model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

TABLE IV. Voltage Range of Current Output.

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} value of ±1mA for bipolar voltage ranges and –2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.
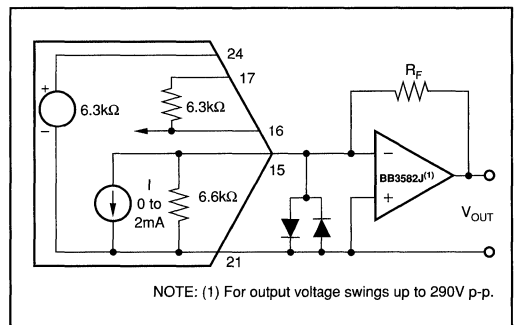
FIGURE 10. External Op-Amp—Using External Feedback Resistors.

DAC80/80P

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DIGITAL-TO-ANALOG CONVERTERS

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \; [(R_L \times R_O) \div (R_L + R_O)]$$
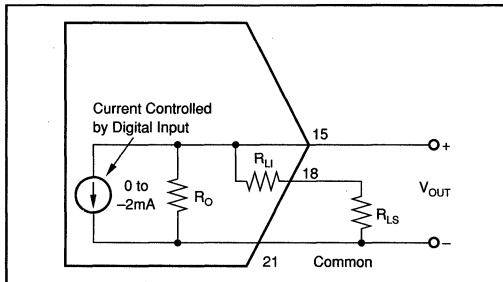
FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to 20 and pin 18 to 19). By choosing R_{LS} = 210Ω, R_L = 1178Ω. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to –2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \; [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (± 1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ in parallel with 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing R_{LS} = 225Ω, R_L = 1455Ω. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ± 1V. As indicated above, trimming may be necessary.
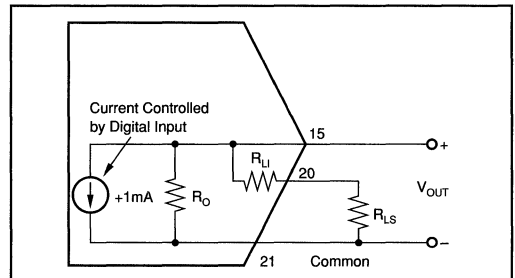
FIGURE 12. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

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DAC600

DEMO BOARD
AVAILABLE
See Appendix A for
more information

DAC600

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DIGITAL-TO-ANALOG CONVERTERS

12-Bit 256MHz Monolithic
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **12-BIT RESOLUTION**
● **256MHz UPDATE RATE**
● **−73dB HARMONIC DISTORTION AT 10MHz**
● **LASER TRIMMED ACCURACY: 1/2LSB**
● **−5.2V SINGLE POWER SUPPLY**
● **EDGE-TRIGGERED LATCH**
● **LOW GLITCH: 5.6pVs**
● **WIDEBAND MULTIPLYING REFERENCE INPUT**
● **50Ω OUTPUT IMPEDANCE**

APPLICATIONS

● **DIRECT DIGITAL SYNTHESIS**
● **ARBITRARY WAVEFORM GENERATION**
● **HIGH RESOLUTION GRAPHICS**
● **COMMUNICATIONS LOCAL OSCILLATORS**
   Spread Spectrum/Frequency Hopping
   Base Stations
   Digitally Tuned Receivers

DESCRIPTION

The DAC600 is a monolithic, high performance digi-tal-to-analog converter for high frequency waveform generation. The internal segmentation and latching minimize output glitch energy and maximizes AC performance. Resistor laser trimming provides for excellent DC linearity.

The ECL compatibility provides for low digital noise at high update rates. The complementary 50Ω outputs and low output capacitance simplifies transmission line design and filtering at the output.

The DAC600 combines precision thin film and bipolar technology to create a high performance, cost effec-tive solution for modern waveform synthesis.

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SPECIFICATIONS

ELECTRICAL

At +25°C V_{REF} = +1.0V, V_{EEA} = V_{EED} = −5.2V, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	DAC600AN MIN	DAC600AN TYP	DAC600AN MAX	DAC600BN MIN	DAC600BN TYP	DAC600BN MAX	UNITS
DIGITAL INPUTS									
Logic	12 Parallel Input Lines, ECL								
Resolution					12			*	Bits
ECL Logic Input Levels: V_{IL}	Logic "0"	Full	−1.48	−1.95	−2	*	*	*	V
I_{IL}		Full			2			*	µA
V_{IH}	Logic "1"	Full	−1.1	−0.75	0	*	*	*	V
I_{IH}		Full			200			*	µA
DIGITAL TIMING									
Input Data Rate		Full	DC		256	*		*	MHz
CLK Pulse Width High or Low		Full	1.95			*			ns
Set-up Time		Full	1.5	1.0		*	*		ps
Hold Time (Referred to CLK)		Full	1.9	1.7		*	*		ns
Propagation Delay		Full		2			*		ns
ANALOG OUTPUT									
Bipolar Output Current	R_L = 0Ω	Full	19	20	21	*	*	*	mA
Output Resistance		Full	47.5	50	52.5	49	*	51	Ω
Output Capacitance		Full		15			*		pF
CONTROL AMPLIFIER									
Input Resistance		Full		800			*		Ω
Full Power Bandwidth	−3dB	Full		10			*		MHz
Offset		+25°C		0	±1		0	±0.5	mV
Input Reference Range		Full	100mV		±1.25	*		*	V
TRANSFER CHARACTERISTICS									
Integral Linearity Error[1]: $V_{OUT\ NOT}$	Best Fit Straight Line	+25°C		±0.012	±0.024		±0.006	±0.012	%FSR
$V_{OUT\ NOT}$		Full		±0.024	±0.036		±0.012	±0.024	%FSR
V_{OUT}		+25°C			±0.1			±0.1	%FSR
Differential Linearity Error[1]: $V_{OUT\ NOT}$		+25°C			±0.024			±0.012	%FSR
$V_{OUT\ NOT}$		Full			±0.036			±0.024	%FSR
V_{OUT}		+25°C			±0.1%			±0.1%	%FSR
12-Bit Monotonicity		+25°C		Guaranteed			Guaranteed		
		Full		Typical			Guaranteed		
Output Offset Current: $V_{OUT\ NOT}$	Bits 1-12 HIGH	+25°C		75	150		50	100	µA
$V_{OUT\ NOT}$		Full		57	150		50	100	µA
Gain Error[2]		+25°C		±0.5	±1.5		±0.5	±1.0	%
		Full		±1.3	±2.0		±1.1	±2.0	%
Output Leakage Current	V_{REF} = 0V, Bits 1-12 LOW, $V_{OUT\ NOT}$	+25°C		10	75		5	50	µA
TIME DOMAIN PERFORMANCE									
Glitch Energy	Major Carry	+25°C		5.6			*		pVs
Fall Time	90% to 10%	+25°C		510			*		ps
Rise Time	10% to 90%	+25°C		770			*		ps
Settling Time[3]									
±0.1% FSR	Major Carry, 1 LSB Change	Full		4			*		ns
±0.024% FSR		Full		15			*		ns
DYNAMIC PERFORMANCE									
Spurious Free Dynamic Range [4]									
f_O = 1MHz	f_{CLOCK} = 50MHz	+25°C		74		70	77		dBFS[3]
f_O = 10MHz	f_{CLOCK} = 50MHz	+25°C		71		65	73		dBFS
f_O = 1MHz	f_{CLOCK} = 100MHz	+25°C		72		70	75		dBFS
f_O = 10MHz	f_{CLOCK} = 100MHz	+25°C		71		66	70		dBFS
f_O = 20MHz	f_{CLOCK} = 100MHz	+25°C		63		59	62		dBFS
f_O = 10MHz	f_{CLOCK} = 200MHz	+25°C		66		66	70		dBFS
f_O = 20MHz	f_{CLOCK} = 200MHz	+25°C		58		64	67		dBFS
f_O = 50MHz	f_{CLOCK} = 200MHz	+25°C		52		50	55		dBFS
Output Noise	Bits 1-12 HIGH	+25°C		10.6			*		nV/√Hz
POWER SUPPLIES									
Supply Voltages: V_{EE}		Full	−4.5	−5.2	−5.5	*	*	*	V
Supply Currents: I_{EEA}	Pins 33 and 34	Full	30	46	60	*	*	*	mA
I_{EED}	Pins 5 and 55	Full	110	150	190	*	*	*	mA
Power Consumption	Operating	Full		900mW	1.3		*	*	W
TEMPERATURE RANGE									
Specification: DAC600AN, BN	Ambient	Full	−40		+85	*		*	°C
θ_{JA}				30			*		°C/W

NOTES: (1) Linearity tests are measured into a virtual ground (op amp). (2) Gain error in % is calculated by: GE (%) = $\dfrac{V_{MEASURED}\ (FS) - V_{IDEAL}\ (FS) \times 100}{V_{IDEAL}\ (FS)}$

(3) Settling time is influenced by the load due to fast edge speeds. Use good transmission line techniques for best results. (4) Spurious free dynamic range is measured from the fundamental frequency to any harmonic or non-harmonic spurs within the bandwidth $f_{CLK}/2_C$, unless otherwise specified.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE (AMBIENT)
DAC600AN, BN	68-Pin Plastic QUAD	−40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

V_{EEA}	0.3 to −7
V_{EED}	0.3 to −7
Logic Inputs	0 to −5.5V
Reference Input Voltage	0 to +1.25V
Reference Input Current	0 to 1.56mA
Case Temperature	−40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	−55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC600AN, BN	68-Pin Plastic QUAD	312-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION	PIN NO	DESIGNATION	DESCRIPTION
1	BYPASS	Disables Latching of Data	35	V_{REF2}	Analog Reference Voltage Center Tap
2	CLK	CLOCK	36	NC	
3	CLKNOT	CLOCKNOT	37	NC	
4	DGND	Digital Ground	38	V_{REF}	Analog Reference Voltage
5	DV_{EE}[1]	−5.2V Supply	39	V_{REF}	Analog Reference Voltage
6	Bit 9		40	NC	
7	Bit 10		41	NC	
8	Bit 11		42	R_{OFFSET}	Offset Compensation
9	Bit 12	LSB	43	NC	
10	NC		44	BYPASS	0.1µF Bypass to Ground
11	NC		45	NC	
12	NC		46	NC	
13	V_{OUT}	DAC Output	47	ALTCOMPC	Control Amp PTAT Reference Compensation[2]
14	V_{OUT}	DAC Output	48	AGND	Analog Signal Ground
15	LGND	Ladder Ground	49	NC	
16	LGND	Ladder Ground	50	LBIAS	Ladder Bias Alternate Compensation[2]
17	V_{OUTNOT}	DAC Output Complement	51	NC	
18	V_{OUTNOT}	DAC Output Complement	52	NC	
19	NC		53	NC	
20	AGND	Analog Ground	54	Bit 1	MSB
21	NC		55	DV_{EE}	Digital −5.2V Supply
22	NC		56	DGND	Digital Signal Ground
23	NC		57	DGND	Digital Signal Ground
24	NC		58	Bit 2	
25	NC		59	Bit 3	
26	BYPASS	0.1µF Bypass to Ground	60	Bit 4	
27	NC		61	NC	
28	ALTCOMPIB	PTAT-IB Reference Compensation[2]	62	Bit 5	
29	AGND	Analog Ground	63	DGND	Digital Ground
30	AGND	Analog Ground	64	Bit 6	
31	NC		65	Bit 7	
32	LOOPCRNT	DAC Reference Alt. Loop Current (Connect to AGND)	66	DGND	Digital Ground
33	V_{EE}[1]	−5.2V Supply	67	Bit 8	
34	V_{EE}[1]	−5.2V Supply	68	NC	

NC: no connect
NOTE: (1) Pins 5 and 55 typically draw 150mA of current. Pins 33 and 34 combined typically draw 46mA. (2) Connect bypass capacitor to V_{EE}.

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DICE INFORMATION

DAC600 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bypass	36	NC
2	CLK	37	V_{REF}
3	CLKNOT	38	V_{REF}
4	DGND	39	NC
5	DV_{EE}	40	NC
6	Bit 9	41	R_{OFFSET}
7	NC	42	NC
8	Bit 10	43	NC
9	Bit 11	44	NC
10	Bit 12	45	NC
11	V_{OUT}	46	ALTCOMPC
12	V_{OUT}	47	AGND
13	LGND	48	NC
14	LGND	49	LBIAS
15	V_{OUTNOT}	50	NC
16	V_{OUTNOT}	51	NC
17	NC	52	NC
18	AGND	53	Bit 1 (MSB)
19	NC	54	DV_{EE}
20	NC	55	DGND
21	NC	56	DGND
22	NC	57	Bit 2
23	NC	58	Bit 3
24	NC	59	Bit 4
25	NC	60	NC
26	NC	61	NC
27	ALTCOMPIB	62	NC
28	AGND	63	Bit 5
29	AGND	64	DGND
30	NC	65	Bit 6
31	LOOPCRNT	66	Bit 7
32	AV_{EE}	67	DGND
33	AV_{EE}	68	Bit 8
34	V_{REF2}	69	NC
35	NC		

Substrate Bias: Negative Supply $-V_{CC}$.
NC = Do not connect.
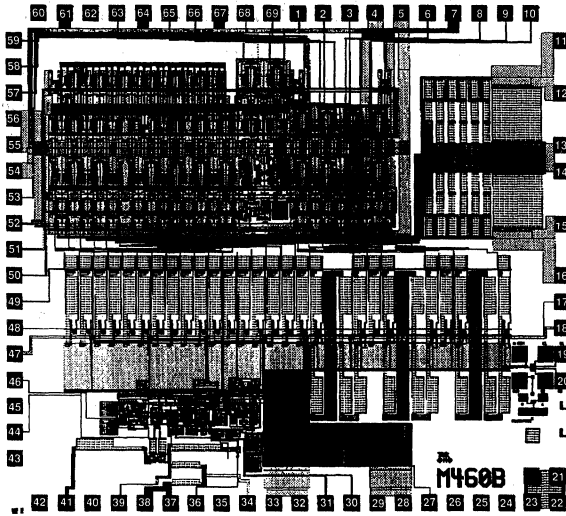
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	160 x 140 ±5	4.06 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	
Metallization	Gold	

TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

DIFFERENTIAL NON-LINEARITY (+25°C)

DIFFERENTIAL NON-LINEARITY (+85°C)

DIFFERENTIAL NON-LINEARITY (–40°C)

INTEGRAL NON-LINEARITY (+85°C)

INTEGRAL NON-LINEARITY (+25°C)

INTEGRAL NON-LINEARITY (–40°C)

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TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\,NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_O = 11MHz

OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_O = 21.9MHz

OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_{OUT} = 41.5MHz

OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 33.8MHz

OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 55.3MHz

OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 83.1MHz

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TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\,NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY

SPURIOUS FREE DYNAMIC RANGE vs
CLOCK FREQUENCY ($f_{OUT} \approx 1/16\ f_{CLOCK}$)

HARMONIC DISTORTION vs CLOCK FREQUENCY
($f_{OUT} \approx 1/3\ f_{CLOCK}$)

3RD HARMONIC vs CLOCK FREQUENCY
($f_{OUT} \approx 1/4\ f_{CLOCK}$)

SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY

SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY

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TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25°C$, $V_{REF} = +1.0V$, measured at $V_{OUT\,NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE

SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE

REFERENCE VOLTAGE vs DISTORTION
($f_{CLK} = 128MHz$, $f_{OUT} = 21.9MHz$)

HARMONIC DISTORTION vs REFERENCE VOLTAGE
($f_{OUT} \approx 1/4 \; f_{CLOCK}$)

REFERENCE CONTROL AMPLIFIER
FREQUENCY RESPONSE

SPURIOUS FREE DYNAMIC RANGE
vs REFERENCE FREQUENCY

V_{REF} Amplitude +0.75V DC 100mVp-p AC
(All Bits on, 47pF Pin 35)

V_{REF} Amplitude +0.75V DC 100mVp-p AC
(All Bits on, 47pF Pin 35)

THEORY OF OPERATION

The DAC600 employs a familiar architecture where input bits switch on the appropriate current sources (Figure 1.) Bits 1-4 are decoded into 15 segments after the first set of latches. The edge triggered master-slave latches are driven by an internal clock buffer. Current sources for bits 5 and 6 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 7-12 are properly scaled and fed to the laser trimmed R-2R ladder.

Decoding of bits 1-4 into 15 segments and synchronizing the data with a master/slave register reduces glitching. If the BYPASS input is low, data is transferred to the output on the positive going edge of the clock. If BYPASS is high, data is transferred to the output regardless of clock state. All digital inputs are ECL compatible.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder. With all of the current sources off, the output voltage is at 0V. With all current sources on (-20mA), the output voltage is at -1V. Transfer function information is given in Tables I and II.
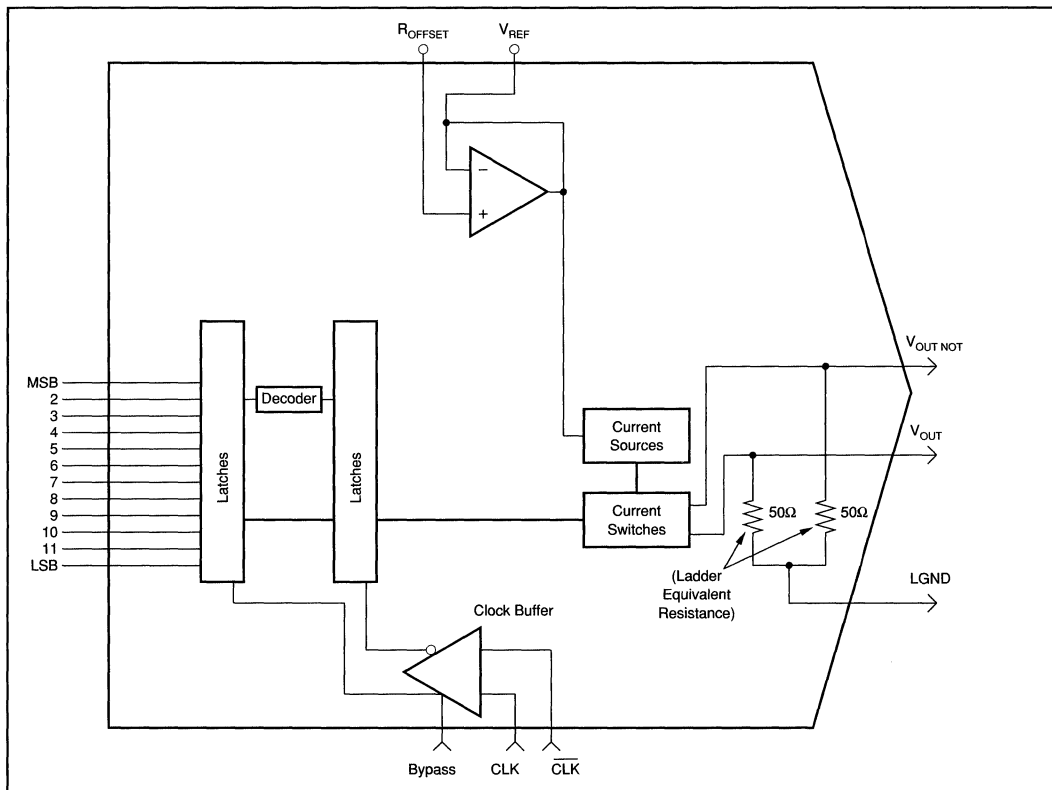
FIGURE 1. Basic DAC600 Architecture.

INPUT BITS		OUTPUT VOLTAGES	
1 2 3 4 5 6 7 8 9 10 11 12		V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0		0V	-0.999756V
0 0 0 0 0 0 0 0 0 0 0 1		-244μV	0.999512V
•		•	
•		•	
•		•	
•		•	
1 0 0 0 0 0 0 0 0 0 0 0		-0.5	-0.499756
1 1 1 1 1 1 1 1 1 1 1 1		-0.999756V	0

TABLE I. Input Code vs Output Voltage Relationships.

BIT	VOLTAGE (No External Load, V_{OUT})
1	-0.5
2	-0.25
3	-0.125
4	-62.5mV
5	-31.25mV
6	-15.625mV
7	-7.8125mV
8	-3.9063mV
9	-1.9531mV
10	-976μV
11	-488μV
12 (LSB)	-244μV

TABLE II. Nominal Bit Weight Values.

DAC600

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DIGITAL-TO-ANALOG CONVERTERS

There is also a complementary $V_{OUT\ NOT}$ output that allows for a differential output signal. The full scale complementary outputs (V_{OUT} and $V_{OUT\ NOT}$) can be simply modeled as –20mA in parallel with 50Ω. This gives an output swing of 0.5Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

The V_{REF} pin should be supplied by a +1.0V reference that is capable of supplying a nominal current of 1.25mA. An alternative would be the use of a 1.25mA current source. A low drift reference will minimize gain drift. A recommended reference circuit is given in Figure 2 as shown in the Typical Performance Curves, lowering the reference voltage to +0.8V will typically improve the Spurious Free Dynamic Range by a few dB.

NOTE: (1) 50 to 100 ppm/°C resistors.
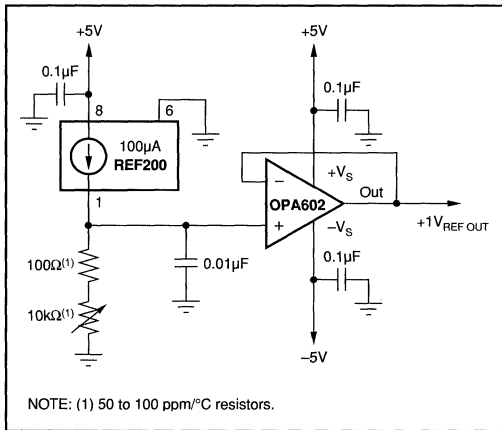
FIGURE 2. A Low Drift External Reference Circuit.

A low-cost alternative reference circuit is shown in Figure 3. This circuit uses the Burr-Brown REF1004-2.5 micropower voltage reference. Gain drift is dependent upon the temperature coefficient of the 1.2kΩ resistor. A TC of < 10ppm/°C is recommended.
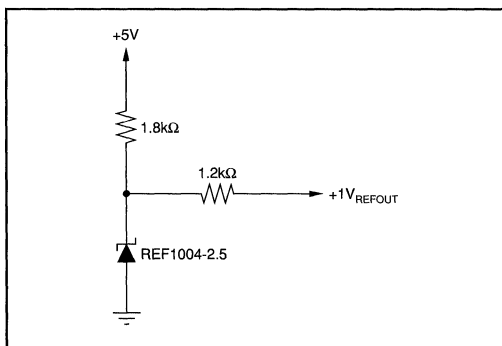
FIGURE 3. Low Cost External Reference Circuit.

The DAC600 can also accept a wideband multiplying reference input. The full power bandwidth of this reference is approximately 30MHz. Care must be taken not to exceed the minimum and maximum input reference voltage levels which are 100mV and +1.25V respectively (refer to the absolute maximum ratings section). In the multiplying reference mode, the 0.4µF bypass capacitor on LBIAS and the 0.1µF on pin 35 need to be removed. A 47pF capacitor to ground needs to be connected to pin 35 (Figure 4.)
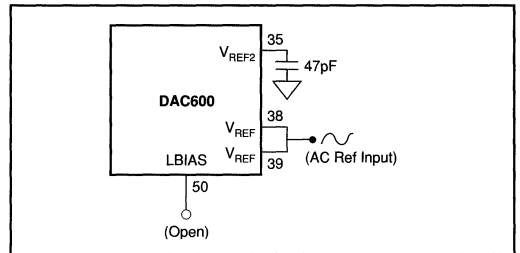
FIGURE 4. Connections for a Multiplying Reference Input.

TIMING

The DAC600 has an internal latch that is triggered on the rising edge of the clock when the BYPASS pin is set LOW. This master-slave mode of operation will assure that the 12 bits will arrive at the current sources with a minimum of data skew. Therefore, this mode is recommended for the vast majority of applications. Observing the minimum set-up and hold time recommendations will ensure proper data latching, refer to Figure 5 for complete timing specifications.

When BYPASS is set HIGH, the DAC600 will operate in the transparent mode. In this mode, both the master and slave registers are transparent and changes in input data ripple directly to the output. Since the four MSBs have a decoder delay, these bits arrive at the output approximately 600 picoseconds later than the lower 8 LSBs. Because this data skew causes glitch, this mode is not recommended for optimum AC performance.

The DAC600 has a differential ECL clock input. This clock input can also be driven by a single ended clock if desired by trying the CLKNOT input to an external voltage of –1.3V. Using a differential clock provides much improved digital feedthrough immunity, however.

DRIVING THE DAC600

The DAC600 inputs will most likely be driven by high speed ECL gate outputs. These outputs should be terminated using standard high speed transmission line techniques. Consult an ECL handbook for proper methods of termination.

Termination resistors should not be connected to the analog ground plane close to the DAC600. The fast changing digital bit currents will cause noise in the analog ground plane under this layout scheme. These fast changing digital currents should be steered away from the sensitive DAC600

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		2		ns
t_{SU}	Setup time DATA must remain stable before CLK.	1.5	1.0		ps
t_H	Hold time DATA must remain stable after CLK.	1.9	1.7		ns
t_{PWL}	CLK pulse width low (50% to 50%).	1.95			ns
t_{PWH}	CLK pulse width high (50% to 50%).	1.95			ns
t_{PMSB}	Propagation delay, MSBs, transparent mode only.		2.1		ns
t_{PLSB}	Propagation delay, LSBs, transparent mode only.		1.5		ns

FIGURE 5. Timing Diagram.

analog ground plane. For speeds of up to 256MHz, series termination with 47Ω resistors will be adequate (Figure 6). This termination technique will greatly lessen the issue of termination currents coupling into the analog ground plane. This is shown in the typical DAC600 connection diagram (Figure 7.)
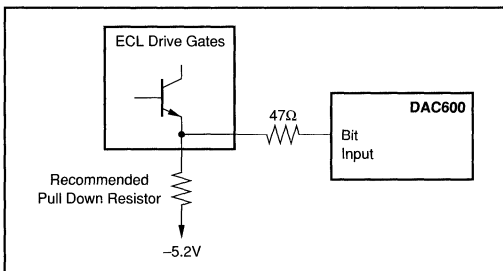
FIGURE 6. Series Bit Termination.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. All of the ground pins (both analog and digital) should be connected directly to the analog ground plane at the DAC600.

Wide busses for the power paths are recommended as good general practice. External bypassing is recommended. A 10µF ceramic capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

ALTCOMPB and ALTCOMPC should be bypassed with 0.1µF capacitors connected to V_{EEA}. When not used in the multiplying mode LBIAS should be bypassed with a 0.4µF capacitor connected to V_{EEA}. The heat spreader (pins 26 and 44) should be bypassed with a 0.1µF capacitor.

MAXIMIZING PERFORMANCE

In addition to optimizing the layout and ground of the DAC600, there are other important issues to consider when optimizing the performance of this DAC in various AC applications.

The DAC600 includes an internal 50Ω output impedance to simplify output interfacing to a 50Ω load. Because some loads may be a complex impedance, care must be taken to match the output impedance with the load. Mismatching of impedances can cause reflections which will affect the measured AC performance parameters such as settling time, harmonic distortion, rise/fall times, etc. Often complex impedances can be matched by placing a variable 3 to 10pF capacitor at the output of the DAC to ground. Also, probing the output of the DAC can present a complex impedance.

The typical performance curves of Spurious Free Dynamic Range vs various combinations of clock rate and/or input frequency should give a general idea of the spectral performance of the DAC under system specific clock and output frequencies. For variable frequency DDS and ARB applications, having a programmable frequency bandpass (smart) filter at the output of the DAC can greatly improve system

spur and noise performance by filtering out unwanted spur and noise spectra. Even with a programmable bandpass filter, care should be taken to update the DAC at greater than 4 times per cycle to (1) minimize the 2nd and 3rd harmonic magnitudes by having the output slew excessively between any successive clock and (3) to keep the 2nd harmonic and other even order harmonics from folding back close to the fundamental under the condition $f_{OUT} = 1/3 \, f_{CLK}$ and (3) to keep the 3rd harmonic and other harmonics from folding back close to the fundamental under the condition

$f_{OUT} = 1/4 \, f_{CLK}$. The making use of the high update rate of the DAC600 helps to lessen the problems of large harmonics "folding back" into the passband.

For DDS applications, often the DAC itself is the limit in Spurious Free Dynamic Range (SFDR) performance. However, due to the high linearity of the DAC600, low frequency spurious performance may be limited by the digital truncation error of the phase accumulator/ROM combination. Most vendors supplying a combination of phase accumulator and ROM specify the SFDR of their digital algorithm.
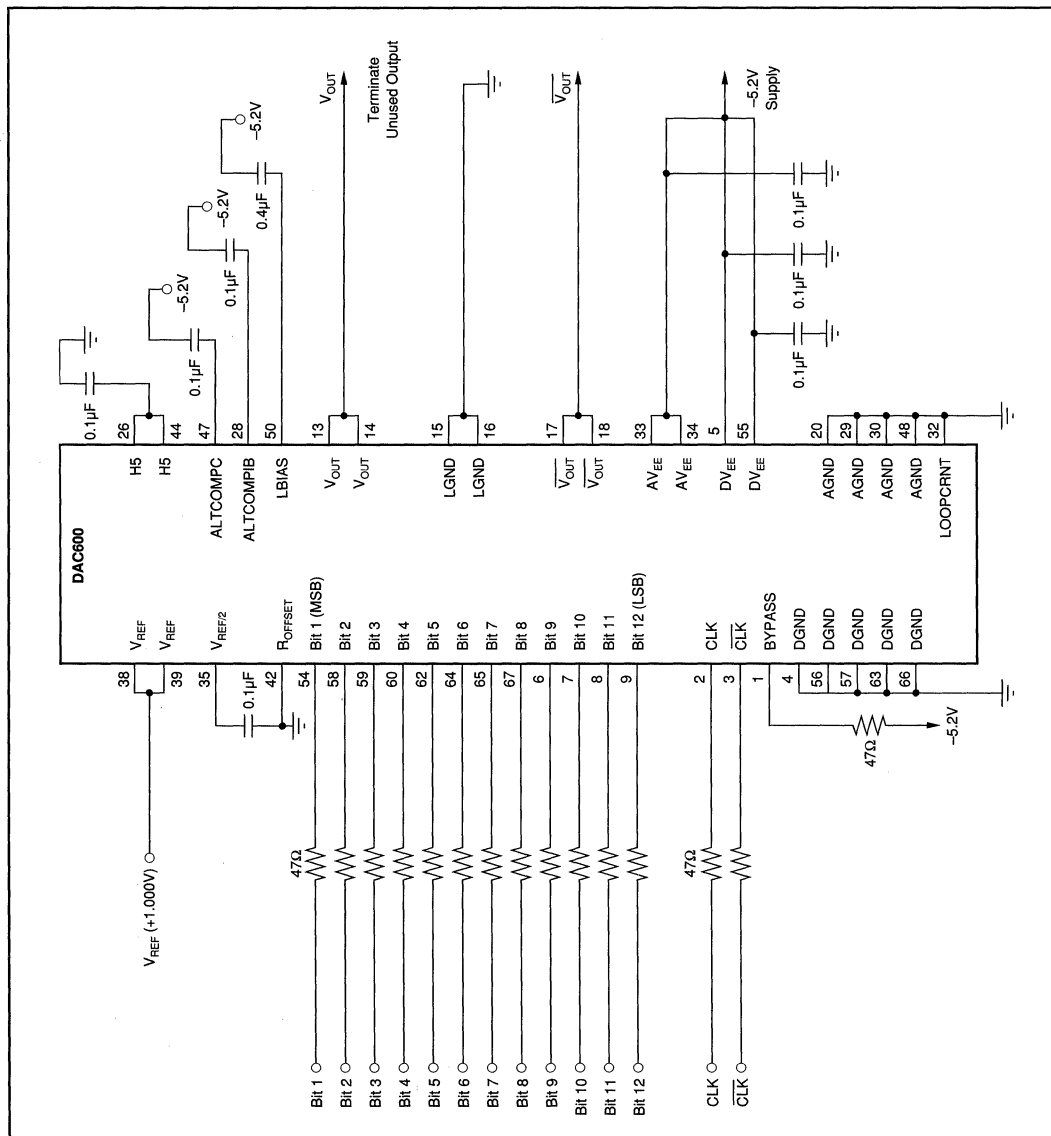
FIGURE 7. Typical DAC600 Connection Diagram.

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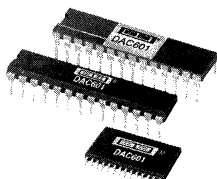
DAC601

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

12-Bit 250MHz Latched ECL
DIGITAL-TO-ANALOG CONVERTER

DAC601

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DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **LOW HARMONICS: 72dB AT 10MHz**
● **LOW SETUP AND HOLD TIMES**
● **LOW POWER: 480mW**
● **LOW REFERENCE DRIFT: ±20ppm/°C**
● **LOW GLITCH**
● **STREAMLINED PINOUT:**
  28-Pin 0.3" DIP or SOIC Package

APPLICATIONS

● **TELECOMMUNICATIONS:**
  Local Oscillator Generation
  Modulated Baseband Generation
● **FUNCTION GENERATORS**
● **ARBITRARY WAVEFORM GENERATORS**
● **TEST EQUIPMENT**

DESCRIPTION

The DAC601 is a high speed, high performance digital-to-analog converter capable of 256MHz data rates. It is complete with a low-drift reference and internal latches.

The user-friendly dual master/slave latches require minimal setup and hold times, thus reducing the speed and cost requirements of the driving

memory. These optimized latches are also designed to suppress digital feedthrough. Segmented DAC current sources further minimize the output glitch.

The DAC601 has been optimized for excellent spurious-free dynamic performance while dissipating only 480mW. This high performance device is available in streamlined (0.3" wide) 28-pin DIP and SOIC packages. A mil temp range DIP is also available.

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SPECIFICATIONS

$T_A = +25°C$, $-V_S = 5.2V$, using internal reference unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	DAC601P, U, HSQ MIN	TYP	MAX	DAC601PB, UB MIN	TYP	MAX	UNITS
TEMPERATURE RANGE									
Specification: P, PB, U, UB Grades	Tambient		−40		+85	*		*	°C
HSQ Grade			−55		+125	*		*	°C
Thermal Resistance: H Package	Junction-to-Ambient			75			*		°C/W
P Package				75			*		°C/W
U Package				75			*		°C/W
DIGITAL INPUTS									
Logic Inputs				ECL Compatible		*			
Resolution					12			*	Bits
ECL Logic Input Levels: V_{IL}	Logic "0"	Full	−1.48	−1.95	−2	*	*	*	V
I_{IL}		Full			10			*	μA
V_{IH}	Logic "1"	Full	−1.1	−0.75	0	*	*	*	V
I_{IH}		Full			10			*	μA
DIGITAL TIMING									
Input Data Rate		Full	DC		256	*		*	MHz
Clock Pulse Width High or Low		Full		1.25			*		ns
Set-up Time		Full		500			*		ps
Hold Time (Referred to Clock)		Full		500			*		ps
Propagation Delay		Full		2			*		ns
ANALOG OUTPUT									
Analog Output Format				Complementary, Unipolar		*			
Full Scale Output Current, Both Outputs	All Bits High, $R_L = 0Ω$	Full		−19.995			*		mA
Low Output Current, Both Outputs	All Bits Low, $R_L = 0Ω$			0			*		mA
Output Resistance[1]	No External Termination	Full	632	744	856	*	*	*	Ω
Output Capacitance		Full		3			*		pF
REFERENCE CHARACTERISTICS									
REFIN	Reference Input			−2.5			*		V
Input Range			0		−2.7	*		*	V
Input Resistance				2			*		kΩ
Full Power Bandwidth				500			*		kHz
REFOUT	Internal Reference								
Accuracy		+25°C	−2.49	−2.5	−2.51	*	*	*	V
Drift		Full		20			*		ppm/°C
TRANSFER CHARACTERISTICS									
Monotonicity		Full		Guaranteed			Guaranteed		
Differential Linearity Error	Worst Case Code	+25°C		0.5	1.0		0.3	0.5	LSB
		Full			2.0		0.35	0.5	LSB
Integral Linearity Error		+25°C		0.5	1.0		0.5	0.75	LSB
		Full			2.0		0.6	1.0	LSB
Gain Error		Full		0.3	0.7		0.2	0.5	%FSR
Output Offset		Full		0.4	0.7		0.2	0.5	%FSR
Power Supply Rejection	$\Delta -V_S = \pm10\%$	Full		±0.03	±0.07		*	*	%FSR/%
TIME DOMAIN PERFORMANCE									
Rise Time		+25°C		770			*		ps
Fall Time		+25°C		510			*		ps
Settling Time									
±0.1%	Major Carry, 1LSB Change	Full		4			*		ns
±.024%		Full		15			*		ns
Glitch Energy		Full		1.5			*		pVs
DYNAMIC PERFORMANCE									
Spurious Free Dynamic Range (SFDR)									
$f_O = 1MHz$	$f_{CLOCK} = 50MHz$	+25°C		76			*		dBFS
$f_O = 5MHz$	$f_{CLOCK} = 50MHz$	+25°C		74			*		dBFS
$f_O = 10MHz$	$f_{CLOCK} = 50MHz$	+25°C		72			*		dBFS
$f_O = 5MHz$	$f_{CLOCK} = 100MHz$	+25°C		73			*		dBFS
$f_O = 10MHz$	$f_{CLOCK} = 100MHz$	+25°C		72			*		dBFS
$f_O = 20MHz$	$f_{CLOCK} = 100MHz$	+25°C		62			*		dBFS
$f_O = 50MHz$	$f_{CLOCK} = 256MHz$	+25°C		78			*		dBFS
$f_O = 80MHz$	$f_{CLOCK} = 256MHz$	+25°C		72			*		dBFS
Differential Gain Error	NTSC	+25°C		TBD			*		%
Differential Phase Error	NTSC	+25°C		TBD			*		°
Output Noise	Bits 1-12 High	+25°C		10.6			*		nV√Hz
POWER SUPPLY REQUIREMENTS									
Supply Voltage: $-V_S$	Operating	Full	−5.46	−5.2	−4.94	*	*	*	V
Supply Current: $-I_S$	Operating	Full		92	105		*	*	mA
Power Consumption		Full		478	546		*	*	W

NOTE: (1) The DAC601 output may be externally terminated with a 53.6Ω resistor to ground for an equivalent 50Ω nominal output impedance and 0V to −1V output swing.

ORDERING INFORMATION

```
                    DAC601   ( )      ( )      ( )
Basic Model Number ─────────┘         │        │
Package Code ───────────────────────────┘      │
  P
  U
  H
Performance Grade Code ────────────────────────┘
  No letter or "B" = –40°C to +85°C
  S = –55°C TO +125°C
Reliability Screening ──────────────────────────┘
  Q-Screened (HS Model Only)
```

ABSOLUTE MAXIMUM RATINGS

–V_S	0.3V to –7V
Logic Inputs	0V to –5.5V
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC, 3s)	+260°C

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC601H, HSQ	28-Pin, 0.3" Wide Hermetic Sidebraze	247
DAC601P, PB	28-Pin, 0.3" Wide Plastic DIP	246
DAC601U, UB	28-Pin, 0.3" Wide SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION
1	B_1	Bit 1, Most Significant Bit
2	B_2	
3	B_3	
4	B_4	
5	B_5	
6	B_6	
7	B_7	
8	B_8	
9	B_9	
10	B_10	
11	B_11	
12	B_12	Bit 12, Least Significant Bit
13	Clock	Data Clocking Input
14	NCLOCK	Complement of Clock Input
15	GND	Ground
16	–V_S	Voltage Supply Input (–5.2V)
17	DIVGND	Divider Ground
18	BYP	Bypass DAC
19	LM	Latch Mode[1]
20	NIC	No Internal Connection
21	–V_S	Voltage Supply Input (–5.2V)
22	NOUT	Complementary Output
23	OUT	Output
24	REFIN	Reference Input
25	REFOUT	Reference Output
26	GND	Ground
27	–V_S	Negative Supply Input (–5.2V)
28	GND	Ground

NOTE: (1) If LM is left floating, the input latches will be in the latch mode. If LM is grounded, the input latches will be in the transparent mode.

TIMING DIAGRAM

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagaton delay. 50% of CLK to 50%V_OUT Time not including one pipeline delay		2		ns
t_SU	Setup time DATA must be stable before CLK		500		ps
t_H	Hold time DATA must remain stable after CLK		500		ps
t_PWL	CLK pulse width low (50% to 50%)		1.25		ns
t_PWH	CLK pulse width high (50% to 50%)		1.25		ns
t_r	Data update period	4			ns

NOTE: Timing is specified in the mode with the LATCH mode floating.

DAC601

DIGITAL-TO-ANALOG CONVERTERS

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BB

DAC602

12-Bit 100MHz Latched TTL
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **LOW HARMONICS: 72dB AT 10MHz**
● **LOW SETUP AND HOLD TIMES**
● **LOW POWER: 490mW**
● **LOW REFERENCE DRIFT: ±20ppm/°C**
● **LOW GLITCH**
● **STREAMLINED PINOUT:**
  28-Pin 0.3" DIP or SOIC Package

APPLICATIONS

● **TELECOMMUNICATIONS:**
  Local Oscillator Generation
  Modulated Baseband Generation
● **FUNCTION GENERATORS**
● **ARBITRARY WAVEFORM GENERATORS**
● **TEST EQUIPMENT**

DESCRIPTION

The DAC602 is a high speed, high performance digital-to-analog converter capable of 100MHz data rates. It is complete with a low-drift reference and internal latches.

The user-friendly dual master/slave latches require minimal setup and hold times, thus reducing the speed and cost requirements of the driving

memory. These optimized latches are also designed to suppress digital feedthrough. Segmented DAC current sources further minimize the output glitch.

The DAC602 has been optimized for excellent spurious-free dynamic performance while dissipating only 490mW. This high performance device is available in streamlined (0.3" wide) 28-pin DIP and SOIC packages. A mil temp range DIP is also available.

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SPECIFICATIONS

TA = +25°C, +V$_S$ = +5V, −V$_S$ = 5.2V, using internal reference unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	DAC602P, U, HSQ MIN	TYP	MAX	DAC602PB, UB MIN	TYP	MAX	UNITS
TEMPERATURE RANGE									
Specification: P, PB, U, UB Grades	Tambient		−40		+85	*		*	°C
HSQ Grade			−55		+125				°C
Thermal Resistance: H Package	Junction-to-Ambient			75			*		°C/W
P Package				75			*		°C/W
U Package				75			*		°C/W
DIGITAL INPUTS									
Logic Inputs				TTL/HCT Compatible		*			
Resolution					12			*	Bits
TTL Logic Input Levels: V$_{IL}$	Logic "0"	Full			0.8			*	V
I$_{IL}$		Full			+10			*	µA
V$_{IH}$	Logic "1"	Full	+2			*			V
I$_{IH}$		Full			+10			*	µA
DIGITAL TIMING									
Input Data Rate		Full	DC		100	*		*	MHz
Clock Pulse Width High or Low		Full		2.5			*		ns
Data Set-up Time	Referred to Clock	Full		500			*		ps
Hold Time	Referred to Clock	Full		500			*		ps
Propagation Delay		Full		2			*		ns
ANALOG OUTPUT									
Analog Output				Complementary, Unipolar		*			
Full Scale Output Current V$_{OUT}$	All Bits High, R$_L$= 0Ω	Full		−19.995			*		mA
Low Output Current, V$_{OUT}$	All Bits Low, R$_L$ = 0Ω	Full		0			*		mA
Output Resistance[1]	No External Termination	Full	632	744	856	*	*	*	W
Output Capacitance		Full		3			*		pF
REFERENCE CHARACTERISTICS									
REFIN	Standard Reference Voltage	Full		−2.5			*		V
Input Range		Full	0		−2.7	*		*	V
Input Resistance				2			*		kΩ
Full Power Bandwidth				500			*		kHz
REFOUT	Internal Reference								
Accuracy		+25°C	−2.49	−2.5	−2.51	*	*	*	ppm
Drift		Full		20			*		ppm/°C
TRANSFER CHARACTERISTICS									
Monotonicity		Full		Guaranteed			Guaranteed		
Differential Linearity Error	Worst Case Code	+25°C		0.5	1.0		0.3	0.5	LSB
		Full		0.6	2.0		0.35	0.5	LSB
Integral Linearity Error		+25°C		0.5	1.0		0.5	0.75	LSB
		Full		0.75	2.0		0.6	1.0	LSB
Gain Error		Full		0.3	0.7		0.2	0.5	%FSR
Output Offset		Full		0.4	0.7		0.2	0.5	%FSR
Power Supply Rejection	Δ −V$_S$ = ±10%	Full		±0.03	±0.07		*	*	%FSR/%
	Δ +V$_S$ = ±5%	Full		±0.01	±0.07		*	*	%FSR/%
TIME DOMAIN PERFORMANCE									
Rise Time		+25°C		770			*		ps
Fall Time		+25°C		510			*		ps
Settling Time									
±0.1%	Major Carry, 1LSB Change	Full		4			*		ns
±.024%		Full		15			*		ns
Glitch Energy		Full		1.5			*		pV$_S$
DYNAMIC PERFORMANCE									
Spurious Free Dynamic Range (SFDR)									
f$_O$ = 1MHz	f$_{CLOCK}$ = 20MHz	+25°C		78			*		dBFS
f$_O$ = 5MHz	f$_{CLOCK}$ = 20MHz	+25°C		72			*		dBFS
f$_O$ = 1MHz	f$_{CLOCK}$ = 50MHz	+25°C		76			*		dBFS
f$_O$ = 5MHz	f$_{CLOCK}$ = 50MHz	+25°C		74			*		dBFS
f$_O$ = 10MHz	f$_{CLOCK}$ = 50MHz	+25°C		72			*		dBFS
f$_O$ = 5MHz	f$_{CLOCK}$ = 100MHz	+25°C		73			*		dBFS
f$_O$ = 10MHz	f$_{CLOCK}$ = 100MHz	+25°C		72			*		dBFS
f$_O$ = 20MHz	f$_{CLOCK}$ = 100MHz	+25°C		62			*		dBFS
Differential Gain Error	NTSC, PAL	+25°C		TBD			*		%
Differential Phase Error	NTSC, PAL	+25°C		TBD			*		°
Output Noise	Bits 1-12 High	+25°C		10.6			*		nV √Hz
POWER SUPPLY REQUIREMENTS									
Supply Voltages: +V$_S$	Operating	Full	+4.75	+5.0	+5.25	*	*	*	V
−V$_S$		Full	−5.46	−5.2	−4.94	*	*	*	V
Supply Currents: +I$_S$	Operating	Full		2	2.3		*	*	mA
−I$_S$		Full		92	105		*	*	mA
Power Consumption		Full		488	560		*	*	mW

NOTE: (1) The DAC602 output may be externally terminated with a 53.6Ω resistor to ground for an equivalent 50Ω output impedance and 0V to −1V output swing.

DAC602

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DIGITAL-TO-ANALOG CONVERTERS

ORDERING INFORMATION

DAC602 ( ) ( ) ( )

Basic Model Number
Package Code
  P
  U
  H
Performance Grade Code
  No letter or "B" = –40°C to +85C
  S = –55°C to +125°C
Reliability Screening
  Q-Screened (HS Model Only)

ABSOLUTE MAXIMUM RATINGS

$+V_S$ .... +6V
$-V_S$ .... 0.3V to –7V
Logic Inputs .... 0V to –5.5V
Junction Temperature .... +165°C
Storage Temperature .... –65°C to +165°C
Lead Temperature (soldering, 10s) .... +300°C
                 (soldering, SOIC, 3s) .... +260°C
Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC602H, HSQ	28-Pin, 0.3" Wide Hermetic DIP	247
DAC602P, PB	28-Pin, 0.3" Wide Plastic DIP	246
DAC602U, UB	28-Pin, 0.3" Wide SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION
1	B_1	Bit 1, Most Significant Bit
2	B_2	
3	B_3	
4	B_4	
5	B_5	
6	B_6	
7	B_7	
8	B_8	
9	B_9	
10	B_{10}	
11	B_{11}	
12	B_{12}	Bit 12, Least Significant Bit
13	Clock	Data Clocking Input
14	$+V_S$	Positive Supply Input (+5V)
15	GND	Ground
16	$-V_S$	Negative Supply Input (–5.2V)
17	DIVGND	Divider Ground
18	BYP	Bypass DAC
19	LM	Latch Mode[1]
20	NC	No Internal Connection
21	$-V_S$	Negative Supply Input (–5.2V)
22	NOUT	Complementary Output
23	OUT	Output
24	REFIN	Reference Input
25	REFOUT	Reference Output
26	GND	Ground
27	$-V_S$	Negative Supply Input (–5.2V)
28	GND	Ground

NOTE: (1) If LM is left floating, the input latches will be in the latch mode. If LM is grounded, the input latches will be in the transparent mode.

TIMING DIAGRAM

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagaton delay. 50% of CLK to 50%V_{OUT}. Time not including one pipeline delay.		2		ns
t_{SU}	Setup time DATA must be stable before CLK.		500		ps
t_H	Hold time DATA must remain stable after CLK.		500		ps
t_{PWL}	CLK pulse width low (50% to 50%).		2.5		ns
t_{PWH}	CLK pulse width high (50% to 50%).		2.5		ns
t_R		10			ns

NOTE: Timing is specified in the mode with the LATCH mode floating.

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DAC650

DEMO BOARD
AVAILABLE
See Appendix A
for more information.

DAC650

12-Bit 500MHz
DIGITAL-TO-ANALOG CONVERTER

DIGITAL-TO-ANALOG CONVERTERS

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FEATURES

● **12-BIT RESOLUTION**
● **500MHz UPDATE RATE**
● **GUARANTEED SPURIOUS PERFORMANCE**
● **LOW GLITCH**
● **FAST SETTLING**
● **INTERNAL EDGE-TRIGGERED LATCH**
● **LASER TRIMMED ACCURACY**
● **INTERNAL REFERENCE**
● **CLEAN LOW-NOISE OUTPUT**

APPLICATIONS

● **DIRECT DIGITAL SYNTHESIS**
● **ARBITRARY WAVEFORM GENERATION**
● **HIGH RESOLUTION GRAPHICS**
● **COMMUNICATIONS LOCAL OSCILLATORS**
   Spread Spectrum
   Base Stations
   Digitally Tuned Receivers
● **HIGH-SPEED MODEMS**

DESCRIPTION

The DAC650 is a high performance 12-bit digital to analog converter for high frequency waveform generation. It is complete with an internal low drift reference and edge-triggered data latch. The internal segmentation and latching provide for minimal output glitch energy.

The ECL compatibility provides for low digital noise at high update rates. The 50Ω output resistance and low output capacitance simplify transmission line design and filtering at the output. Complementary outputs are offered for increased performance while driving transformers or differential amplifiers.

The DAC650 combines precision thin film and bipolar technology with high speed gallium arsenide to create a high performance, cost effective solution for modern waveform synthesis systems.

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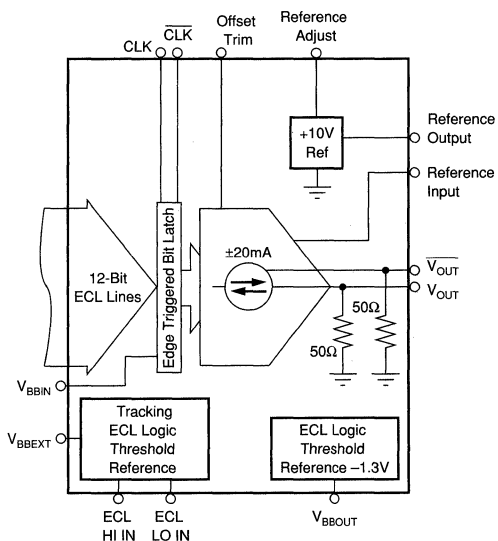
SPECIFICATIONS

ELECTRICAL

Over full specified temperature range, using the internal +10V reference and rated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	DAC650JL MIN	DAC650JL TYP	DAC650JL MAX	DAC650KL MIN	DAC650KL TYP	DAC650KL MAX	UNITS
TEMPERATURE RANGE								
Specification: DAC650JL, KL[1]	Ambient	0		+70	*		*	°C
θ_{CA}			27			*		°C/W
θ_{JC}			13			*		°C/W
DIGITAL INPUTS								
Logic	12 Parallel Input Lines			ECL Compatible				
Resolution			12		*	*	*	Bits
ECL Logic Input Levels[2]: V_{IL}	Logic "0"	−1.475	−1.8	−2	*	*	*	V
I_{IL}			1.0	10		*	*	µA
V_{IH}	Logic "1"	−1.115	−0.8	−0.6	*	*	*	V
I_{IH}			1.0	10		*	*	µA
Logic Threshold Voltage		−1.2	−1.3	−1.4	*	*	*	V
DIGITAL TIMING								
Input Data Rate		DC		500	*		*	MHz
CLK Pulse Width Low		1.0			*			ns
Set-Up Time		2.0	1.8		*	*		ns
Hold Time (Referred to CLK)		−500	−600		*	*		ps
Propagation Delay			1.5			*		ns
ANALOG OUTPUT								
Bipolar Output Current	$R_L = 0\Omega$		±20			*		mA
Bipolar Output Voltage	$R_L = \infty$		±1.0			*		V
Output Resistance	$V_{OUT}, \overline{V_{OUT}}$ to Ground	49	50	51	*	*	*	Ω
Output Resistance Drift			50			*		ppm/°C
Output Capacitance			5			*		pF
TRANSFER CHARACTERISTICS								
Integral Linearity Error	Best Fit Straight Line		±0.018	±0.036		±0.012	±0.024	%FSR
Differential Linearity Error	+25°C		±0.018	±0.036		±0.08	±0.024	%FSR
	Over Temperature		±0.018	±0.036		±0.012	±0.024	%FSR
Monotonicity			Typical			Guaranteed		
Bipolar Gain Error	Output Voltage, $R_L = \infty$		±0.5	±1.0		±0.5	±1.0	%FSR
Bipolar Offset Error	Output Voltage, $R_L = \infty$		±0.5	±1.0		±0.25	±0.5	%FSR
TIME DOMAIN PERFORMANCE								
Glitch Energy	Major Carry		20			*		pV-s
Output Rise Time	10% to 90%		300			*		ps
Output Fall Time	90% to 10%		350			*		ps
Settling Time[3]: ±0.1%FSR	Major Carry, 1LSB Change		2.0			*		ns
REFERENCES								
V_{BB} Input Range (Pin 1)		−1.4	−1.3	−1.2	*	*	*	V
$V_{BB\,INT}$ Reference (Pin 68)		−1.4	−1.3	−1.2	*	*	*	V
$V_{BB\,EXT}$ Tracking Reference (Pin 67)	$ECL_{HI\,IN} = -0.8V, ECL_{LO\,IN} = -1.8V$	−1.4	−1.3	−1.2	*	*	*	V
Internal Reference Voltage (Ref Out)		9.95	10	10.05	*	*	*	V
Ref in Resistance			4950			*		Ω
Ref in Operating Voltage Range		4.5	10.0	11.0	*	*	*	V
DYNAMIC PERFORMANCE								
Spurious Free Dynamic Range[4]								
$f_O = 1MHz, f_{CLK} = 100MHz$	+25°C, Span = DC to $f_{CLK}/2$	65	68		68	70		dBc[5]
$f_O = 10MHz, f_{CLK} = 100MHz$	+25°C, Span = DC to $f_{CLK}/2$	59	63		62	65		dBc
$f_O = 30MHz, f_{CLK} = 200MHz$	+25°C, Span = DC to $f_{CLK}/2$	50	52		53	56		dBc
$f_O = 80MHz, f_{CLK} = 200MHz$	+25°C, Span = DC to $f_{CLK}/2$	47	50		50	52		dBc
$f_O = 80MHz, f_{CLK} = 500MHz$	+25°C, Span = DC to 150MHz	49	55		52	58		dBc
$f_O = 100MHz, f_{CLK} = 500MHz$	+25°C, Span = 50MHz to 150MHz	51	56		54	59		dBc
Output Noise	Full Scale Sine Wave Output		1.0			*		$\mu V/\sqrt{Hz}$
POWER SUPPLIES								
Supply Voltages: $+V_{CC}$	Operating, T_{MIN} to T_{MAX}	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−15.75	−15	−14.25	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD2}$		−5.46	−5.2	−4.94	*	*	*	V
Power Supply Rejection	All Supplies, ±5% Change		0.05	0.08		*	*	%/%
Supply Currents: $+I_{CC}$	Operating		10	13		*	*	mA
$-I_{CC}$			−47	−50		*	*	mA
$+I_{DD1}$			53	57		*	*	mA
$-I_{DD2}$			−191	−245		*	*	mA
Power Consumption	Operating		2.0	2.6		*	*	W

NOTE: (1) Extended temperature range devices are available, inquire. (2) V_{BBIN} (Pin 1) connected to $V_{BB\,INT}$ (Pin 68). (3) Settling time is influenced by load due to fast edge speeds. Use good transmission line techniques for best results. (4) Spurious Free Dynamic Range includes both harmonic and non-harmonic related spurs in the bandwidth indicated. (5) dBc is "dB referred to the fundamental amplitude."

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE (AMBIENT)
DAC650JL, KL	68-Pin Ceramic, Gullwing Leads	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$ .... $\pm 18V$
Logic Input .... +0.5V to −5.5V
Case Temperature .... −40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature .... −55°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC650JL, KL	68-Pin Ceramic Gullwing	256

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION	PIN NO	DESIGNATION	DESCRIPTION
1	V_{BB}	Sets Logic Threshold for Bits 1-12	35	AGND	Ground for Analog Output Current
2	Bit 1	MSB	36	AGND	
3	Bit 2		37	AGND	
4	Bit 3		38	AGND	
5	Bit 4		39	$\overline{V_{OUT}}$	Complementary Output Voltage
6	Bit 5		40	$\overline{V_{OUT}}$	
7	Bit 6		41	$\overline{V_{OUT}}$	
8	Bit 7		42	AGND	
9	Bit 8		43	AGND	
10	Bit 9		44	AGND	
11	Bit 10		45	V_{OUT}	Output Voltage
12	Bit 11		46	V_{OUT}	
13	Bit 12	LSB	47	V_{OUT}	
14	V_{EE}	Logic Power (−5.2V Nominal)[1]	48	AGND	
15	V_{EE}		49	AGND	
16	CLK	Clock	50	AGND	
17	CLK_{NOT}	Not Clock	51	AGND	
18	DNC	Do Not Connect	52	−15V	−15V Supply
19	V_{EE}		53	−15V	
20	V_{EE}		54	PWR GND	Ground for Analog Supplies
21	V_{EE}		55	+5V	+5V Supply
22	V_{EE}		56	+5V	+5V Supply
23	V_{EE}		57	V_{OS} ADJ	Offset Adjust
24	V_{EE}		58	PWR GND	Ground for Analog Supplies
25	V_{EE}		59	Ref_{ADJ}	Reference Out Adjust
26	V_{EE}		60	Ref_{OUT}	Reference Out (+10V, Buffered)
27	DGND	Ground for Logic	61	Ref_{IN}	Reference In (4.950kΩ)
28	DGND		62	+15V	+15V Supply
29	DGND		63	PWR GND	Ground for Analog Supplies
30	DGND		64	−5.2V Analog	Analog Power (−5.2V Nominal)[1]
31	DGND		65	ECL LO_{IN}	External ECL LOW input (optional)
32	DGND		66	ECL HI_{IN}	External ECL HI input (optional)
33	DGND		67	V_{BBEXT}	The buffered mean of LO_{EXT} and HI_{EXT}
34	DGND		68	V_{BBINT}	Internally generated −1.3V reference

NOTE: (1) Both the −5.2V Logic and −5.2V analog pins should be powered from a common supply.

DAC650

DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

OUTPUT SPECTRUM

f_O = 1.0MHz
f_{CLK} = 100MHz
Amplitude = +3.6dBm
Resolution BW = 150Hz

OUTPUT SPECTRUM

f_O = 1.0MHz
f_{CLK} = 100MHz
Amplitude = +3.58dBm
Resolution BW = 290Hz

OUTPUT SPECTRUM

f_O = 9.98MHz
f_{CLK} = 100MHz
Amplitude = +3.4dBm
Resolution BW = 580Hz

OUTPUT SPECTRUM

f_O = 9.96MHz
f_{CLK} = 100MHz
Amplitude = +3.35dBm
Resolution BW = 580Hz

OUTPUT SPECTRUM

f_O = 29.93MHz
f_{CLK} = 200MHz
Amplitude = +3.13dBm
Resolution BW = 290Hz

OUTPUT SPECTRUM

f_O = 29.32MHz
f_{CLK} = 200MHz
Amplitude = +3.1dBm
Resolution BW = 1.2kHz

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BB

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

OUTPUT SPECTRUM

f_O = 49.88MHz
f_{CLK} = 500MHz
Amplitude = +3.3dBm
Resolution BW = 1.2kHz

Amplitude (dBm) vs Frequency (MHz)

OUTPUT SPECTRUM

f_O = 79.92MHz
f_{CLK} = 500MHz
Amplitude = +3.0dBm
Resolution BW = 4.6kHz

Amplitude (dBm) vs Frequency (MHz)

OUTPUT SPECTRUM

f_O = 79.88MHz
f_{CLK} = 200MHz
Amplitude = +0.93dBm
Resolution BW = 1.2kHz

Amplitude (dBm) vs Frequency (MHz)

OUTPUT SPECTRUM

f_O = 79.27MHz
f_{CLK} = 200MHz
Amplitude = +0.93dBm
Resolution BW = 9.1kHz

Amplitude (dBm) vs Frequency (MHz)

OUTPUT SPECTRUM

f_O = 99.75MHz
f_{CLK} = 500MHz
Amplitude = +2.7dBm
Resolution BW = 2.3kHz

Amplitude (dBm) vs Frequency (MHz)

DAC650

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DIGITAL-TO-ANALOG CONVERTERS

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY
(Span = DC to $f_{CLK}/2$)

SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY
(Span = DC to 200MHz)

SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY
(Span = DC to $f_{CLK}/2$)

SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY
(Span = DC to 200MHz)

TECHNOLOGY OVERVIEW

The DAC650 uses a unique design approach to achieve very fast settling time and high resolution. This mixed-technology design uses two active chips: one gallium arsenide and the other silicon.

The GaAs MESFET die is used for those circuits which determine speed. This includes the latches, data decoders, and current switches. A silicon die with thin film is used for those circuits which determine accuracy, such as the precision references and current sources. The precision R-2R resistor ladders are laser trimmed to further increase the accuracy of the DAC650. A block diagram of the DAC650 is shown in Figure 1.

THEORY OF OPERATION

The DAC650 employs a familiar architecture where input bits switch on the appropriate current sources. Bits 1-3 are decoded into 7 segments before the first set of latches. A similar delay is given for the 9 least significant bits to minimize data skew. The edge triggered master-slave latches are driven by an internal clock buffer. This buffer placement has matched the clock lines to each of the 32 latches, thus minimizing output glitch energy.

There are 7 current sources for bits 1 to 3. Current sources for bits 4-8 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 9-12 are fed to the laser trimmed R-2R ladder for proper scale-down. The segmentation further minimizes output glitch which can cause spectral degradation.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder (100Ω) in parallel with 100Ω (Figure 1). With all of the current sources off, the output voltage is at +1V. With all current sources on (–40mA), the output voltage is at –1V. There is also a complementary $\overline{V_{OUT}}$ output that allows for a differential output signals. The full scale complementary outputs (V_{OUT} and $\overline{V_{OUT}}$) can be simply modeled as ±20mA in parallel with 50Ω. This gives an output swing of 1Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

A precision +10V reference is included in the DAC650. A 50Ω resistor should be connected between REF$_{IN}$ and REF$_{OUT}$ for the specified unadjusted gain. This internal reference has been laser trimmed to minimize offset and gain drift. Alternatively, an external reference may be used. Multiple DACs may be run from one master reference by connecting a 50Ω resistor from each REF$_{IN}$ to the master REF$_{OUT}$. A 100Ω potentiometer may be used in place of the 50Ω resistor in order to provide a ±1% gain adjustment range (Figure 2).

A wider adjustment range of ±20% may be achieved by connecting a 10kΩ potentiometer from REF$_{OUT}$ to ground, with the wiper connected to the REF$_{ADJ}$ pin. Adjusting the output to more than 40mA full scale may degrade high

frequency performance and reliability due to higher current densities and operating temperature. Alternatively, lower full scale currents will affect operation because there is less current available to charge internal and external capacitances.

It should be noted that the gain adjust techniques mentioned above affect the current output and thus the voltage output from the DAC650. The voltage output will also be affected by an external load acting in parallel with the 50Ω output impedance.

OFFSET ADJUST

The offset may be adjusted by connecting a potentiometer between the +5V supply and ground with the wiper connected to the offset adjust pin. The voltage on this pin with no connection is about 2V, with an equivalent impedance of 1.6kΩ. A 10kΩ potentiometer will give the necessary adjustment range. The full scale range of the DAC output may be offset so it is not symmetrical around zero, but the full scale range must also be adjusted so that the output swing does not exceed ±1V. Connecting the offset adjust pin to ground gives a unipolar output of 0 to –2V (with no load) or 0 to –1V (with a 50Ω load). This also reduces the current requirements for the +5V supply by 20mA.

DIGITAL INPUTS, LOGIC THRESHOLDS, and TERMINATION

The input logic levels and clock levels are ECL compatible. The data inputs are single ended ECL and the clock input is differential.

The internal impedance of the data and clock inputs is a high impedance (FET gate), and is clamped to the digital supply and ground to protect against ESD damage. ESD precautions should still be used when handling the DAC650.

The inputs will most likely be driven by high-speed ECL gate outputs. These outputs should be terminated using standard high-speed transmission line techniques. Consult an ECL handbook for proper methods of termination.

Termination resistors should not be connected to the analog ground plane close to the DAC650. The fast changing digital bit currents will cause noise in the analog ground plane under this layout scheme. These fast changing digital currents should be steered away from the sensitive DAC650 analog ground plane. For speeds of up to 256MHz, series termination with 47Ω resistors will be adequate (Figure 3). This termination technique will greatly lessen the issue of termination currents coupling into the analog ground plane. Above 256MHz, parallel termination of the transmission line at the package pin may be required for clean digital input.

The input data threshold level is set by connecting the appropriate voltage (–1.2V to –1.4V) to pin 1. The actual level may be provided 3 ways:

(1) The user connects the DAC650's internal –1.3V threshold reference directly to pin 1. This simple connection provides excellent noise margins for ECL levels.
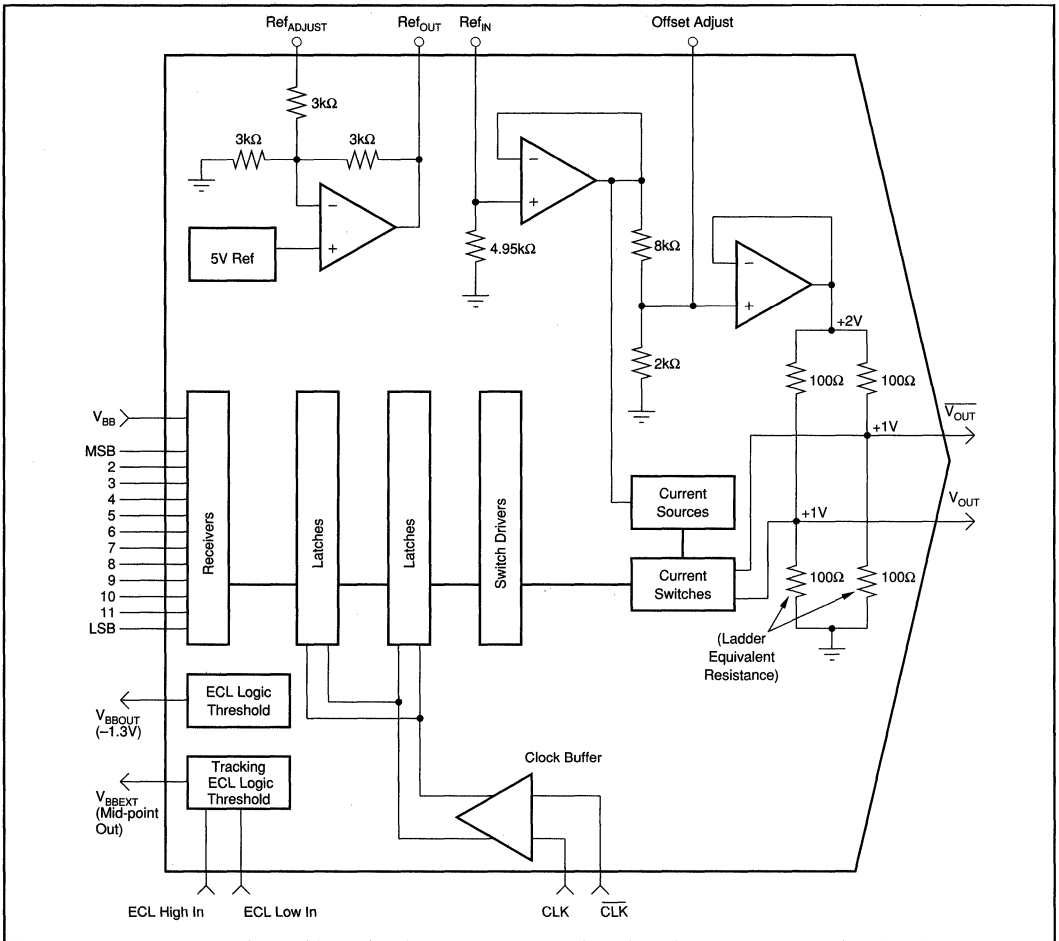
FIGURE 1. Functional Block Diagram of the DAC650.
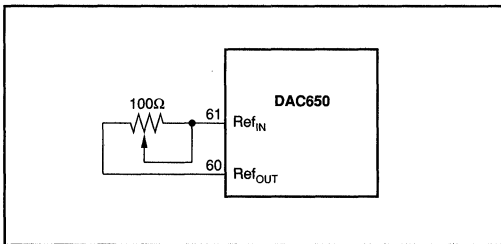
FIGURE 2. Using a Potentiometer for ±1% Gain Adjust.
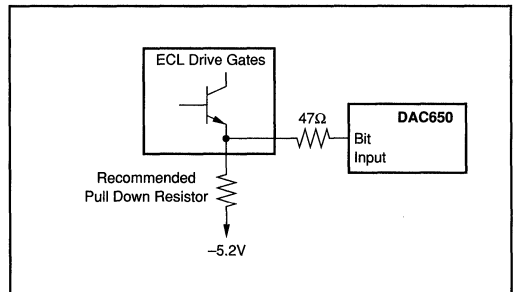
FIGURE 3. Series Bit Termination.

(2) An external V_{BB} system reference is applied to pin 1. This technique may allow data threshold levels to track the system over supply and temperature variations.

(3) The internal tracking ECL threshold reference (pin 67) is applied to pin 1. The output of the tracking ECL threshold reference is simply the average of two externally applied levels. These levels are a system logic low (pin 65) and system logic high (pin 66). This technique may provide increased noise margin for systems with levels slightly different from ECL. Leave pins 65-67 open if this option is not used.

TIMING

The DAC650 has an internal edge triggered latch. The output changes on the positive edge of CLK. This master-slave latching will assure that the 12 bits will arrive at the bit switches with a minimum of data skew. Data must have adequate setup and hold time for proper operation (refer to Figure 4). Note that the Hold time is negative. Therefore the data may change before the rising edge of clock and still be valid.

The DAC650 has a differential ECL clock input. This clock input can also be driven by a single-ended clock if desired by tying the $\overline{CLK}$ input to an external voltage of –1.3V. Using a true differential clock provides much improved digital feedthrough immunity, however.

DATA IN/VOUT CORRESPONDENCE

The each full scale output of the DAC650 may be modeled as either ±20mA current source in parallel with 50Ω or a ±1V voltage source in series with 50Ω. The nominal current and voltage bit weights are given in Table I and the input code vs output voltage relationships are given in Table II.

Transmission line techniques at the output are also recommended to minimize ringing and glitching. Ideally, both of the outputs should see the same termination, including any delay between the DAC650 and the load.

Since the outputs V_{OUT} and $\overline{V_{OUT}}$ are equal in magnitude but opposite in sign, they are ideal for driving RF transformers (Figures 5). The primary may be connected between the two outputs. The secondary may be floating or referenced to ground. This results in a 2X signal power and some cancellation of clock feedthrough, glitching, and distortion. Figures 6 and 7 give recommended output amplifiers.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		1.5		ns
t_{SU}	Setup time DATA must remain stable before CLK.	2.0	1.8		ns
t_H	Hold time DATA must remain stable after CLK.	–500	–600		ps
t_{PWL}	CLK pulse width low (50% to 50%).	1.0			ns
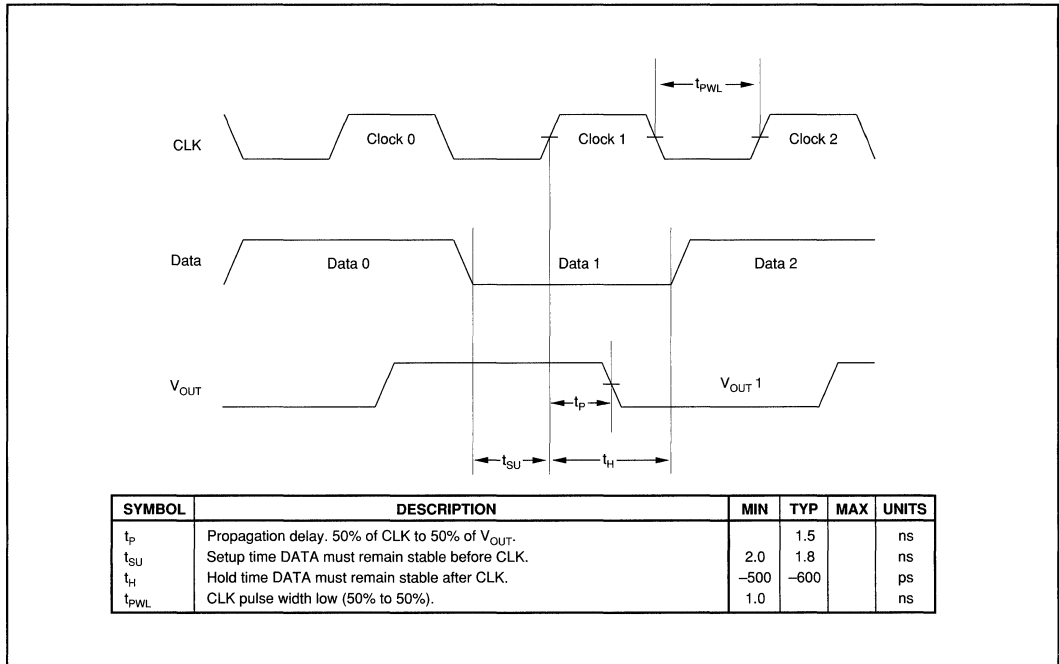
FIGURE 4. Timing Diagram for the DAC650.

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If only one output is used, the unused output should be terminated identically. If the terminations cannot be identical and the unused output must be unterminated, the termination for the used output should be as close as possible to the DAC650.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. An example of a typical circuit configuration is given in Figures 8. The DAC650 has multiple ground pins to minimize pin impedances. All of the ground pins (analog and digital both) should be connected directly to the analog ground plane at the DAC650.

Wide busses for the power paths are recommended as good general practice. There are several internal power supply bypass capacitors, but external bypassing is still recom-

BIT	VOLTAGE (No External Load)	CURRENT
1	1V	20mA
2	.5V	10mA
3	0.25V	5mA
4	0.125V	2.5mA
5	62.5mV	1.25mA
6	31.25mV	625µA
7	15.625mV	312.5µA
8	7.8125mV	156.25µA
9	3.9063mV	78.125µA
10	1.9531mV	39.06µA
11	976µV	19.53µA
12 (LSB)	488µV	9.76µA

TABLE I. Nominal Bit Weight Values.

INPUT BITS		OUTPUT VOLTAGES	
1 2 3 4 5 6 7 8 9 10 11 12		V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0		+1.000	−1 + 488µV
0 0 0 0 0 0 0 0 0 0 0 1		+1 − 488µV	−1 + 976µV
0 0 0 0 0 0 0 0 0 0 1 0		+1 − 976µV	−1 + 1.464mV
•			
•			
•			
0 1 0 0 0 0 0 0 0 0 0 0		0.50	−0.50 + 488µV
1 0 0 0 0 0 0 0 0 0 0 0		0.000	+488µV
1 1 1 1 1 1 1 1 1 1 1 1		−1 + 488µV	+1.000

TABLE II. Input Code vs Output Voltage Relationships.
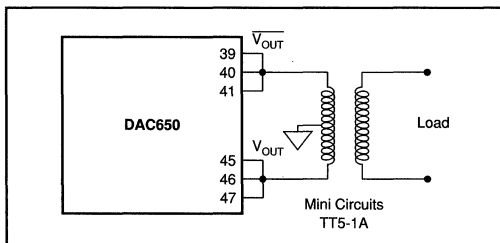
FIGURE 5. Using an RF Transformer at the Output of the DAC650. Filtering the Outputs Before the Transformer Improves the Performance in Some Applications.

mended. A 10µF tantalum capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

Pin 64, Analog V_{EE}, should be connected to the same supply as the digital V_{EE} pins (–5.2V).

MAXIMIZING PERFORMANCE

The DAC650 has been designed to give a very clean analog output with minimal noise, overshoot, and ringing. In addition to optimizing the layout and ground of the DAC650, there are other important issues to consider when optimizing the performance of this DAC in various AC applications.

The DAC650 includes an internal 50Ω output impedance to simplify output interfacing to a 50Ω load. Because some loads may be a complex impedance, care must be taken to match the output impedance with the load. Mismatching of impedances can cause reflections which will affect the measured AC performance parameters such as settling time, harmonic distortion, rise/fall times, etc. Often complex impedances can be matched by placing a variable 3 to 10pF capacitor at the output of the DAC to ground. Also, probing the output can present a complex impedance.

The typical performance curves of Spurious Free Dynamic Range vs various combinations of clock rate and/or input frequency should give a general idea of the spectral performance of the DAC under system specific clock and output frequencies. We have defined Spurious Free Dynamic Range as any harmonic or non-harmonic spurs in the indicated bandwidth . In phase lock loop applications, the harmonics often fall outside the loop bandwidth of the PLL. In these cases, as well as cases where the output is filtered, Spurious

FIGURE 6. A High Speed Single Ended Amplifier at the Output. The Gain is $-R_F/50\Omega$.
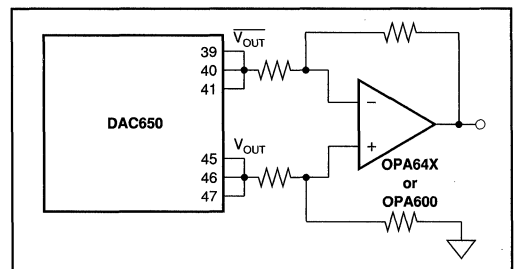
FIGURE 7. A High Speed Differential Amplifier at the Output.

Free Dynamic Range will generally be much better due to the harmonics falling outside the passband. Even with a bandpass filter, updating the DAC at greater than 4 times per cycle will (1) minimize the 2nd and 3rd harmonic magnitudes by having the output slew excessively between any successive clock and (2) will keep the $(f_{CLK} - 2f_O)$ spur and other even order spurs from folding back close to the fundamental under the condition $f_{OUT} = 1/3f_{CLK}$ and (3) will keep the $(f_{CLK} - 3f_O)$ spur and other spurs from folding back close to the fundamental under the condition $f_{OUT} = 1/4f_{CLK}$. Making use of the high update rate of the DAC650 helps to lessen the problems of harmonics "folding back" into the passband.

EVALUATION BOARD

The high frequency signals used in operating the DAC650 can cause difficult layout problems. It is especially difficult to build a high-performance prototype board using the DAC650. It is recommended that an evaluation fixture be used for prototyping. An evaluation fixture includes a DAC650 soldered to the PC board. Both grades are available for the evaluation fixture.

ORDERING INFORMATION

MODEL	DESCRIPTION
DEM-DAC650J-E	Evaluation Board with DAC650JL Attatched
DEM-DAC650K-E	Evaluation Board with DAC650KL Attatched
DEM-DAC650 PDS	Data Sheet for DAC650 Evaluation Board
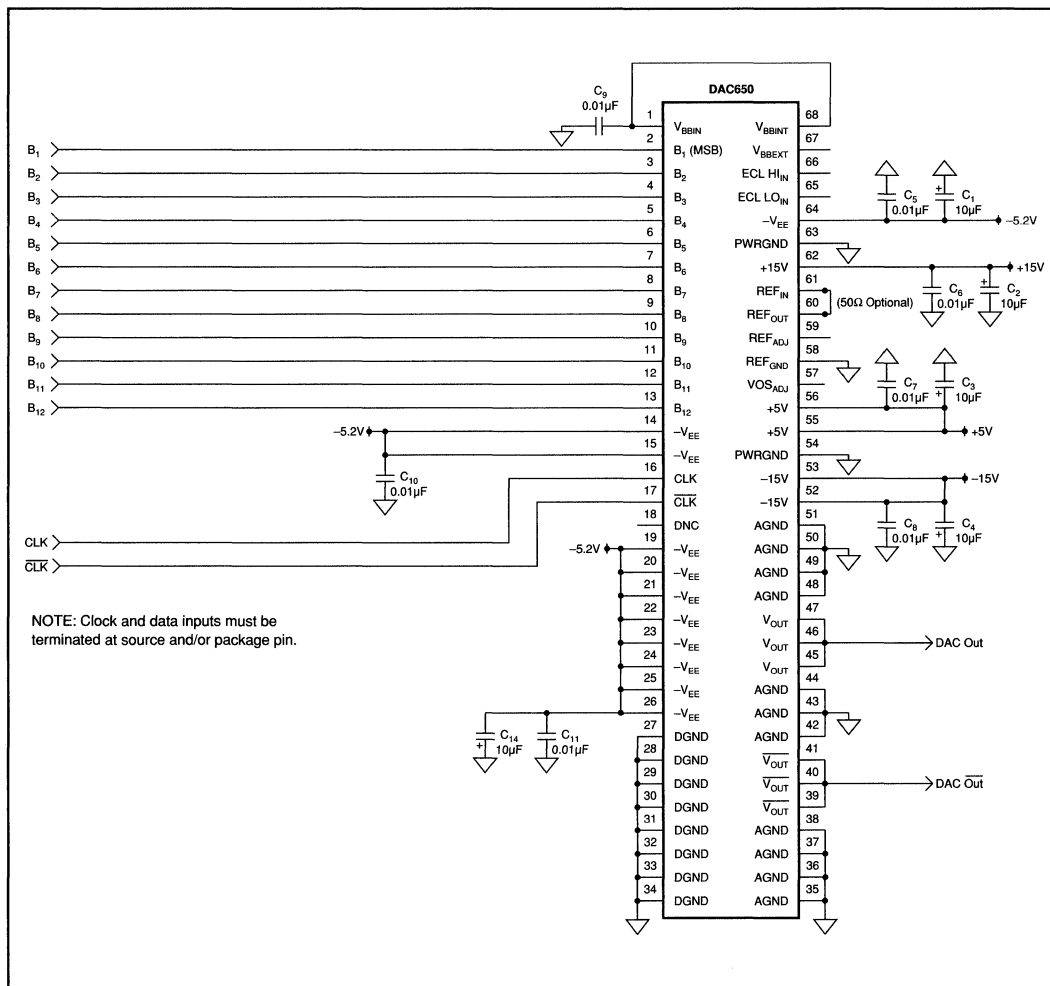
FIGURE 8. Typical DAC650 Connection Diagram.

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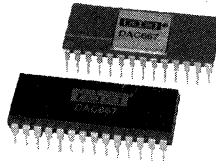
DAC667

Microprocessor-Compatible
12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

● ±1/2LSB MAX NONLINEARITY OVER TEMPERATURE

● MONOTONICITY GUARANTEED OVER TEMPERATURE

● MICROCOMPUTER INTERFACE: Double-Buffered Latch

● VOLTAGE OUTPUT: ±10V, ±5V, +10V With ±12V to ±15V Supplies

● LOW POWER DISSIPATION: 345mW typ

● PIN COMPATIBLE WITH AD667

DESCRIPTION

The DAC667 is a complete monolithic integrated circuit microprocessor-compatible 12-bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

A double-buffered latch facilitates microcomputer interfacing to 4-, 8-, 12-, or 16-bit data buses. The input buffer latch holds the 12-bit data until it is transferred to an internal 12-bit D/A converter latch, giving precise timing control over an analog output change.

The DAC667 is specified to ±1/4LSB maximum linearity error (B and K grades) at +25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range. The DAC667 is available in two performance grades and in 28-pin, 0.6" wide plastic and ceramic DIP package types.

PDS-1091B

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SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $\pm12V$. $\pm15V$ power supplies unless otherwise noted.

PARAMETER	DAC667JP MIN	TYP	MAX	DAC667KP MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	0		+0.8	*		*	V
I_{IH} ($VI_H = 5.5V$)		3	10		*	*	µA
I_{IL} ($V_{IL} = 0.8V$)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
$T_A = T_{MIN}$ to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
$T_A = T_{MIN}$ to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), $T_A = +25°C$ to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, $T_A = +25°C$ to T_{MIN} or T_{MAX}		±1	±3		*		ppm of FSR/°C
Bipolar Zero, $T_A = +25°C$ to T_{MIN} or T_{MAX}		±5	±10		*		ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ ‖ 500pF Load, $C_F = 0$)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT							
	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
$V_{CC} = +11.4$ to +16.5VDC		5	10		*	*	ppm of FS/%
$V_{EE} = -11.4$ to -16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
-11.4 to -16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating	-40		+85	*		*	°C
Storage	-65		+125	*		*	°C

* Same as specification for DAC667JP.

<div style="float:right">**DAC667** **3** **DIGITAL-TO-ANALOG CONVERTERS**</div>

ABSOLUTE MAXIMUM RATINGS

```
V_CC to Power Ground ............................................. 0V to +18V
V_EE to Power Ground ............................................. 0V to -18V
Digital Inputs (Pins 11-15, 17-28) to Power Ground ............ -1V to +7V
Ref In to Reference Ground ........................................ ±12V
Bipolar Offset to Reference Ground ................................ ±12V
10V Span Resistor to Reference Ground ........................... ±12V
20V Span Resistor to Reference Ground ........................... ±24V
Ref Out, V_OUT (Pins 6, 9) ................. Indefinite Short to Power Ground,
                                             Momentary Short To V_CC
Power Dissipation ..................................................... 1000mW
```

TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

All models, $T_A = +25°C$, $V_{CC} = +12V$ or +15V, $V_{EE} = -12V$ or -15V.

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ELECTRICAL (CONT)

T_A = +25°C, ±12V, ±15V power supplies unless otherwise noted.

PARAMETER	DAC667AH			DAC667BH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	+0		+0.8	*		*	V
I_{IH} (V_{IH} = 5.5V)		3	10		*	*	μA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	μA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}	Monotonicity Guaranteed			*			LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3		*	*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10		*	*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load)							
With 10kΩ Feedback		3	4		*	*	μs
With 5kΩ Feedback		2	3		*	*	μs
For LSB Change		2			*		μs
Slew Rate	8			*			V/μs
ANALOG OUTPUT							
Ranges[4]	±2.5, ±5, ±10, +5, +10			*			V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT							
	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = −11.4 to −16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
−11.4 to −16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Operating	−40		+85	*		*	°C
Storage	−65		+150	*		*	°C

* Same as specification for DAC667AH.

NOTES: (1) The digital input specifications are 100% tested at +25°C and over the full temperature range. (2) Adjustable to zero. (3) FSR means full scale range and is 20V for ±10V range and 10V for the ±5V range. (4) ±10V full scale output can be achieved using ±11.4 supplies.

TIMING DIAGRAMS
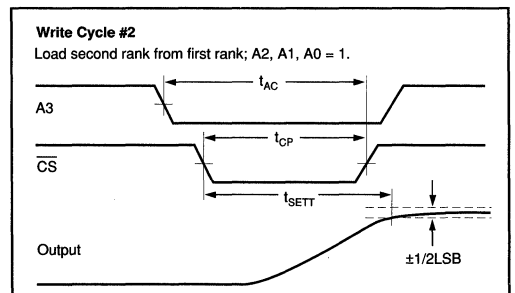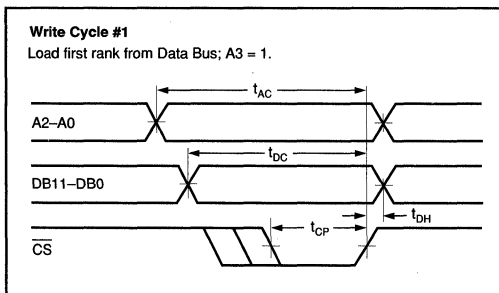
Write Cycle #1
Load first rank from Data Bus; A3 = 1.

A2–A0, t_{AC}, t_{DC}, DB11–DB0, t_{DH}, t_{CP}, $\overline{CS}$

Write Cycle #2
Load second rank from first rank; A2, A1, A0 = 1.

A3, t_{AC}, $\overline{CS}$, t_{CP}, t_{SETT}, Output, ±1/2LSB

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC667JP	28-Pin Plastic DIP	215
DAC667KP	28-Pin Plastic DIP	215
DAC667AH	28LD Side-Brazed Ceramic DIP	149
DAC667BH	28LD Side-Brazed Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE (°C)	LINEARITY ERROR, max at 25°C	GAIN TC, max (ppm/°C)
DAC667JP	Plastic DIP	0 to +70	±1/2LSB	±30
DAC667KP	Plastic DIP	0 to +70	±1/4LSB	±15
DAC667AH	Ceramic DIP	−25 to +85	±1/2LSB	±30
DAC667BH	Ceramic DIP	−25 to +85	±1/4LSB	±15

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all ones and all zeros). DAC667 linearity error is specified at ±1/4LSB max at +25°C for B and K grades, and ±1/2LSB max for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than −1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. All grades of the DAC667 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Gain drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar offset drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar offset drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

Bipolar zero drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar zero drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for FSR output changes of 20V (10kΩ feedback) and 10V (5kΩ feedback), and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

OPERATION

DAC667 is a monolithic integrated-circuit 12-bit D/A converter. It is complete with 12-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface as shown in the front-page diagram.

INTERFACE LOGIC

The bus interface logic of the DAC667 consists of four independently addressable latches in two ranks. The first rank consists of three four-bit input latches which can be loaded directly from a 4-, 8-, 12- or 16-bit microprocessor/microcontroller bus. These latches hold data temporarily while a complete 12-bit word is assembled before loading it into the second rank of latches. This double buffered organization prevents the generation of spurious analog output values while the complete word is being assembled.

DAC667

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DIGITAL-TO-ANALOG CONVERTERS

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When the control signals return to logic 1, the data is latched. A truth table for the control signals is presented in Table I.

$\overline{CS}$	A3	A2	A1	A0	OPERATION
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable Four LSBs of First Rank
0	1	1	0	1	Enable Four Middle Bits of First Rank
0	1	0	1	1	Enable Four MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent
X = Don't care.					

TABLE I. DAC667 Truth Table.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the timing specifications on page 2 are met.

LOGIC INPUT COMPATIBILITY

The DAC667 digital inputs are TTL compatible (1.4V switching level) with a low leakage, high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.
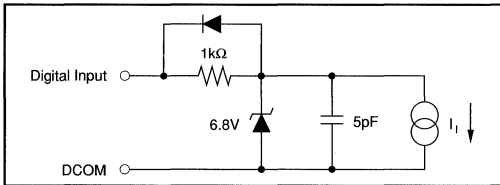
FIGURE 1. Equivalent Digital Input Circuit.

DAC667 data inputs will float to logic 1 and control inputs will float to logic 0 if left open. It is recommended that any unused inputs be connected to power common to improve noise immunity.

INPUT CODING

The DAC667 accepts positive-true binary input codes.

Input coding for unipolar analog output is straight binary (USB), where all zeros (000_{HEX}) on the data inputs gives a zero analog output and all ones (FFF_{HEX}) gives an analog output 1LSB below full scale.

Input coding for bipolar analog outputs is bipolar offset binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

The DAC667 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

INTERNAL/EXTERNAL REFERENCE USE

DAC667 contains a +10V reference which is trimmed to typically ±0.2% and tested and guaranteed to ±1%. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 50Ω. A trim potentiometer with a nominal value of 100Ω can be used to provide adjustment to zero gain error. If an external 10.000V reference is used, it may be necessary to increase the trim range slightly.

The reference output may be used to drive external loads, sourcing up to 5mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the converter will vary.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. The DAC667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range, a CMOS multiplying D/A is a better choice.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of offset and gain adjustments to a unipolar- and a bipolar-connected DAC667. Offset should be adjusted first to avoid interaction of adjustments.

Offset Adjustment

For unipolar (USB) operation, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) operation, apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. See Table II for calibration values and codes.
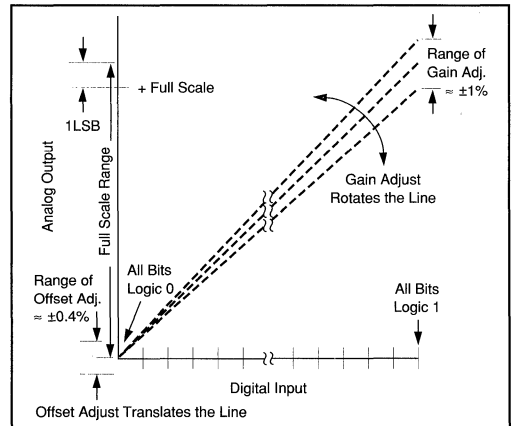
FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.
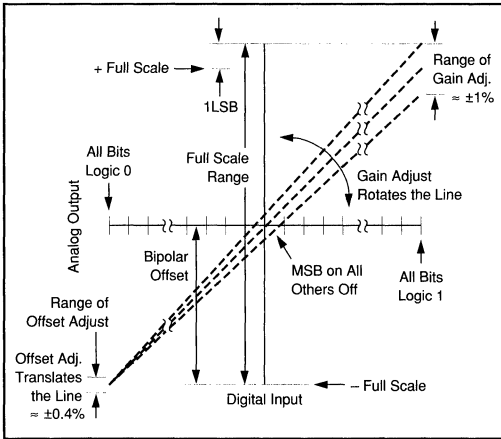
FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Gain Adjustment

For either unipolar or bipolar operation, apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for calibration values.

DIGITAL INPUT	ANALOG OUTPUT				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FFF$_{HEX}$	+4.9987V	+9.9976V	+2.4987V	+4.9976V	+9.9951V
800$_{HEX}$	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
7FF$_{HEX}$	+2.4987V	+4.9976V	−0.0013V	−0.0024V	−0.0049V
000$_{HEX}$	0.0000V	0.0000V	−2.5000V	−5.0000V	−10.0000V
1LSB	1.22mV	2.44mV	1.22mV	2.44mV	4.88mV

TABLE II. Calibration Values.

SETTLING TIME PERFORMANCE

The switches, reference and output amplifier of the DAC667 are designed for optimum settling time performance (Figure 4). Figure 4a shows the full scale range step response, V_{OUT} −10V to +10V to −10V, for data input 000$_{HEX}$ to FFF$_{HEX}$ to 000$_{HEX}$. Figure 4b shows the settling time response at plus full scale (+10V) for an output transition from −10V to +10V. Figure 4c shows the settling time response at minus full scale (−10V) for an output transition from +10V to −10V. Figure 4d shows the major carry glitch response for input code transitions 7FF$_{HEX}$ to 800$_{HEX}$ and for 800$_{HEX}$ to 7FF$_{HEX}$.

Unlike the Analog Devices AD667, the Burr-Brown DAC667 does not require an external capacitor (C_f = 20pF) across R_{SPAN} to eliminate overshoot. Using the 20pF with the Burr-
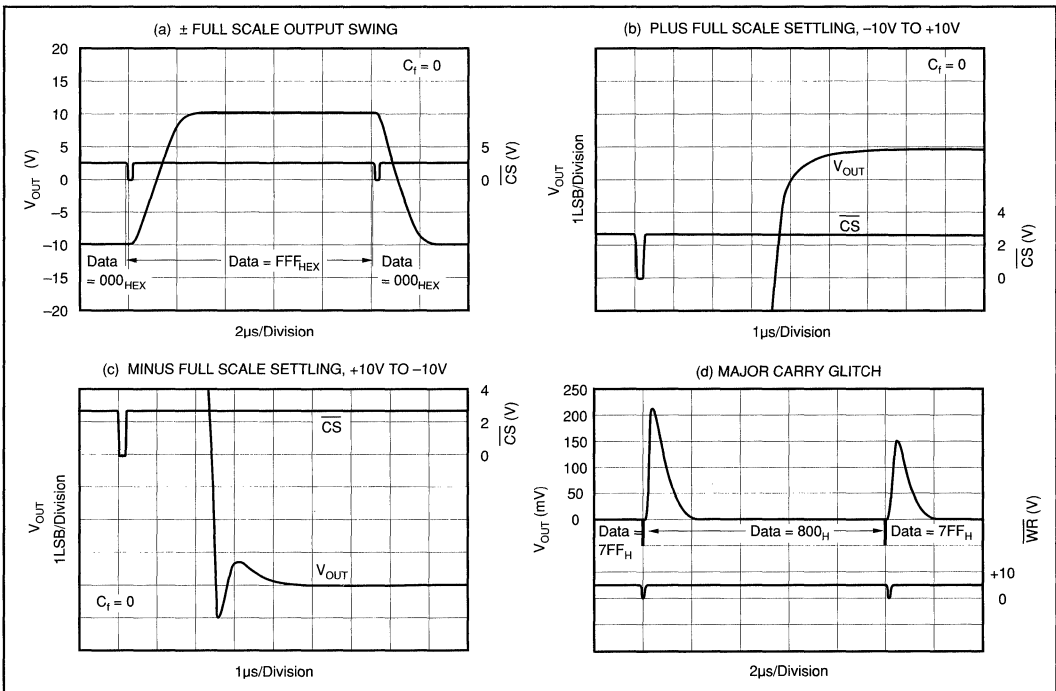
FIGURE 4. Settling Time Performance, Z_{LOAD} = 2kΩ ‖ 500pF.

DAC667

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DIGITAL-TO-ANALOG CONVERTERS
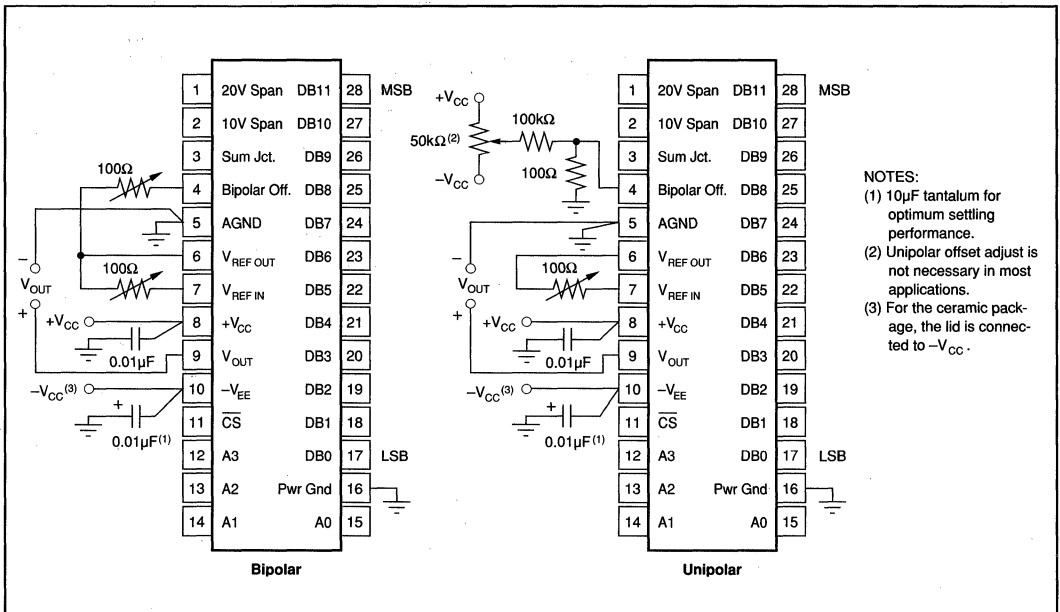
FIGURE 5. Power Supply, Gain and Offset Connections.

Brown DAC667 increases the settling time about one microsecond. The DAC667 settling time is specified at 7µs maximum. The AD667 is specified at 4µs maximum.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the metal lid of the ceramic-packaged DAC667 is connected to $-V_{EE}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Best settling performance occurs using a 1µF to 10µF tantalum capacitor at $-V_{EE}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{EE}$ as well as at $+V_{CC}$. The capacitors should be located close to the DAC667 package.

DAC667 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both power ground (pin 16) and analog ground (AGND, pin 5) be connected directly to a ground plane under the package. If a ground plane is not used, connect the AGND and power ground pins together close to the package. Since the reference point for V_{OUT} and $V_{REF OUT}$ is the AGND pin, it is also important to connect the load directly to the AGND pin.

The change in current in the AGND pin due to an input data word change from 000_{HEX} to FFF_{HEX} is only 1mA.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

The DAC667 output amplifier can provide ±10V output swing while operating on ±11.4V supplies. The Analog Devices AD667 requires a minimum of ±12.5V to achieve an output swing of ±10V.

Internal scaling resistors provided in the DAC667 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. Refer to Figures 6, 7 and 8. Connections for various output ranges are shown in Table III.

The internal feedback resistors (5kΩ) and the bipolar offset resistor (9.95kΩ) are trimmed to an absolute tolerance of about ±10%.
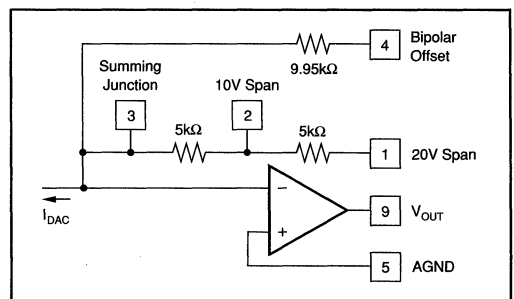
FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 9 TO	CONNECT PIN 1 TO	CONNECT PIN 2 TO	CONNECT PIN 4 TO
±10V	Offset Binary	1	9	NC	6 (Through 50Ω fixed or 100Ω trim resistor.)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (Through 50Ω fixed or 100Ω trim resistor.)
±2.5V	Offset Binary	2	3	9	6 (Through 50Ω fixed or 100Ω trim resistor.)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (Or optional trim. See Figure 7.)
0 to +5V	Straight Binary	2	3	9	5 (Or optional trim. See Figure 7.)

TABLE III. Output Voltage Range Connections.
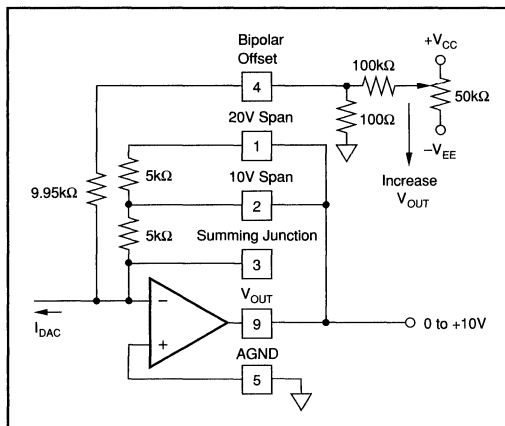
FIGURE 7. 0 to +10V Unipolar Voltage Output.
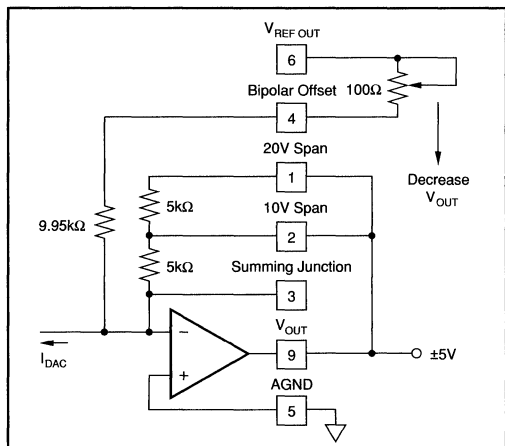
FIGURE 8. ±5V Bipolar Voltage Output.

MICROCOMPUTER BUS INTERFACING

8-BIT BUS INTERFACE

The DAC667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats. Data formats for 8-bit buses are illustrated in Figure 9.
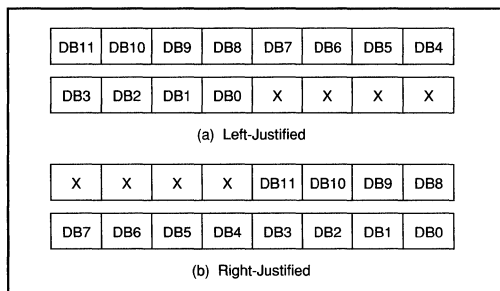
FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

Whenever a 12-bit D/A is loaded from an 8-bit bus, two bytes are required. If the software program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the four most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

Figure 10 shows an addressing scheme for use with a DAC-667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the DAC667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

Right-justified data can also be accommodated as shown in Figure 11. The DAC667 still occupies two adjacent locations in the processor's memory map. Location X01 loads the eight LSBs and location X10 loads the four MSBs and updates the output.

12- AND 16-BIT BUS INTERFACES

For operation with 12- and 16-bit buses, all four address lines (A0 through A3) are connected to logic 0, and the latch is enabled by $\overline{CS}$ asserted low. The DAC667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the DAC667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering. See Figure 12.

DAC667

DIGITAL-TO-ANALOG CONVERTERS
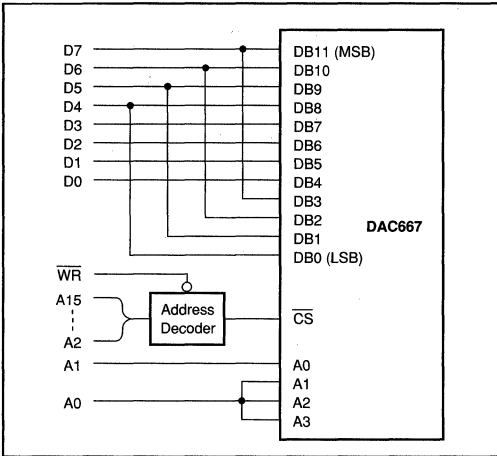
FIGURE 10. Left-Justified 8-Bit Bus Interface.
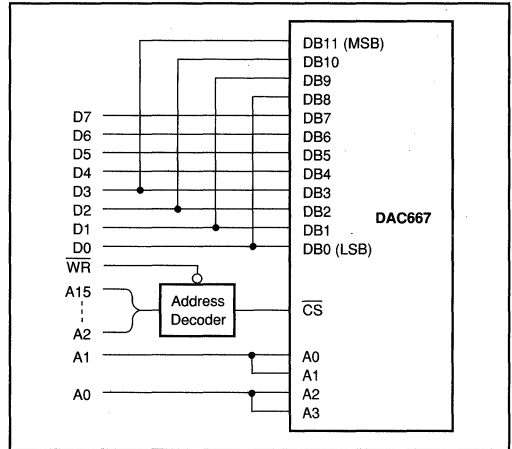
FIGURE 11. Right-Justified 8-Bit Bus Interface.
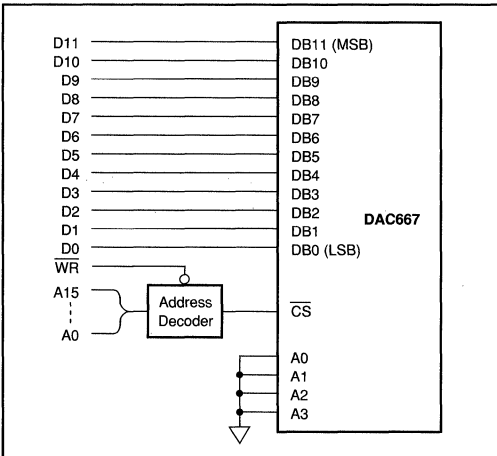
FIGURE 12. Connections for 12- and 16-Bit Bus Interface.

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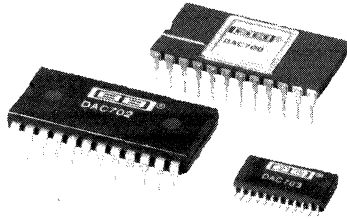
DAC700/702
DAC701/703

Monolithic 16-Bit
DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● V_{OUT} AND I_{OUT} MODELS
● HIGH ACCURACY:
 Linearity Error ±0.0015% of FSR max
 Differential Linearity Error ±0.003% of FSR
 max
● MONOTONIC (at 15 bits) OVER FULL
 SPECIFICATION TEMPERATURE RANGE

● PIN-COMPATIBLE WITH DAC70, DAC71,
 DAC72
● DUAL-IN-LINE PLASTIC AND HERMETIC
 CERAMIC AND SOIC

DESCRIPTION

The DAC70X family comprise of complete 16-bit digital-to-analog converters that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range, but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to –2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC700 and DAC702 are also pin-compatible with the DAC70 model family. In addition, the DAC703 is offered in a 24-pin SOIC package for surface mount applications.

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3.55

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	DAC702/703J, D			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT													
DIGITAL INPUT													
Resolution			16			*			*			*	Bits
Digital Inputs [1]													
V_{IH}	+2.4		+V_{CC}	*		*	*		*	*		*	V
V_{IL}	−1.0		+0.8	*		*	*		*			*	V
I_{IH}, V_I = +2.7V			+40			*			*			*	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5	*		*			*		*	*	mA
TRANSFER CHARACTERISTICS													
ACCURACY [2]													
Linearity Error [4]		±0.0015	±0.006		*	±0.003		*	*		±0.00075	±0.0015	% of FSR [3]
Differential Linearity Error [4]		±0.003	±0.012		*	±0.006		*	*		±0.0015	±0.003	% of FSR
Differential Linearity Error at Bipolar Zero (DAC702/703) [4]					±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR
Gain Error [5]		±0.07	±0.30		*	±0.15		±0.05	±0.10		*	*	%
Zero Error [5, 6]		±0.05	±0.10		*	*					*	*	% of FSR
Monotonicity Over Spec. Temp Range	13			14			*			15			Bits
DRIFT (over specification temperature range)													
Total Error Over Temperature Range (all models) [7]		±0.08			*	±0.15		±0.05	±0.10		*	*	% of FSR
Total Full Scale Drift:													
DAC700/701		±10			*	±30		±8.5	±18		±6	±13	ppm of FSR/°C
DAC702/703		±10			*	±25		±7	±15		*	*	ppm of FSR/°C
Gain Drift (all models)		±10	±30		*	±25		±7	±15		±5	±10	ppm/°C
Zero Drift:													
DAC700/701					±2.5	±5		±1.5	±3		*	*	ppm of FSR/°C
DAC702/703		±5	±15		*	±12		±4	±10		±2.5	±5	ppm of FSR/°C
Differential Linearity Over Temp. [4]			±0.012			+0.009, −0.006			*			+0.006, −0.003	% of FSR
Linearity Error Over Temp. [4]			±0.012			±0.006			*			±0.003	% of FSR
SETTLING TIME (to ±0.003% of FSR) [8]													
DAC701/703 (V_{OUT} Models)													
Full Scale Step, 2kΩ Load		4			*	8		*	*		*	*	µs
1LSB Step at Worst-Case Code [9]		2.5			*			*			*		µs
Slew Rate		10			*			*			*		V/µs
DAC700/702 (I_{OUT} Models)													
Full Scale Step (2mA),													
10 to 100Ω Load		350			*	1000		*	*		*	*	ns
1kΩ Load		1			*	3		*	*		*	*	µs
OUTPUT													
VOLTAGE OUTPUT MODELS													
DAC701 (CSB Code)					0 to +10			*			*		V
DAC703 (COB Code)		±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance		0.15			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		
CURRENT OUTPUT MODELS													
DAC700 (CSB Code) [10]					0 to −2			*			*		mA
Output Impedance [10]					4			*			*		kΩ
DAC702 (COB Code) [10]		±1			*			*			*		mA
Output Impedance [10]		2.45			*			*			*		kΩ
Compliance Voltage		±2.5			*			*			*		V

ELECTRICAL (CONT)

MODEL	DAC702/703J, D			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE													
Voltage		+6.3		+6.0	+6.3	+6.6	+6.24	+6.3	+6.36	*	*	*	V
Source Current Available													
for External Loads		+2.5		+1.5	*		*	*		*	*		mA
Temperature Coefficient		±10				±25			±15		*	*	ppm/°C
Short Circuit to Common													
Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: +V_{CC}	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
–V_{CC}	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+16.5	*	*	*	*	*	*	*	*	*	V
Current (No Load):													
DAC700/702													
(I_{OUT} Models)													
+V_{CC}		+10	+25		*	*		*	*		*	*	mA
–V_{CC}		–13	–25		*	*		*	*		*	*	mA
V_{DD}		+4	+8		*	*		*	*		*	*	mA
DAC701/703													
(V_{OUT} Models)													
+V_{CC}		+16	+30		*	*		*	*		*	*	mA
–V_{CC}		–18	–30		*	*		*	*		*	*	mA
V_{DD}		+4	+8		*	*		*	*		*	*	mA
Power Dissipation:													
(V_{DD} = +5.0V)(11)													
DAC700/702		365				790			630		*	*	mW
DAC701/703		530				940			780		*	*	mW
Power Supply Rejection:													
+V_{CC}		±0.0015	±0.006		*	*			±0.003		*	*	% of FSR/%V_{CC}
–V_{CC}		±0.0015	±0.006		*	*			±0.003		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*			*		*	*	% of FSR/%V_{DD}
TEMPERATURE RANGE													
Specification:													
B, C Grades							–25		+85	*		*	°C
S Grades							–55		+125				°C
J, K, L Grades	0		+70	*		*				0		+70	°C
Storage: Ceramic				–60		+150	*		*	*		*	°C
Plastic, SOIC	–60		+100	*		*							°C

* Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.0015% of FSR for the LH and CH grades, ±0.003% of FSR for the BH grade and ±0.006% of FSR for the KG grade. (2) DAC700 and DAC702 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC702) and the 0 to +2mA range (DAC700). (4) ±0.0015% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 14-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 13-bit resolution. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code FFFF$_H$ for DAC700 and DAC701, 7FFF$_H$ for DAC702 and DAC703. (7) With gain and zero errors adjusted to zero at +25°C. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, 7FFF$_H$ to 8000$_H$ and 8000$_H$ to 7FFF$_H$. (10) Tolerance on output impedance and output current is ±30%. (11) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.
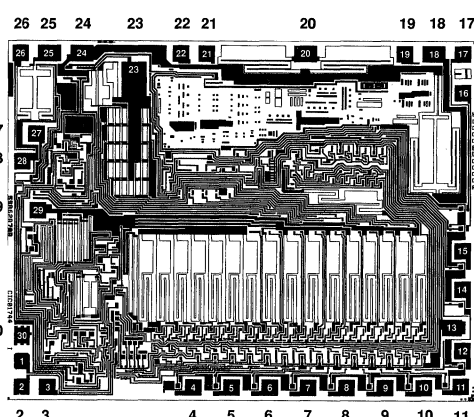
ABSOLUTE MAXIMUM RATINGS

+V_{CC} to Common .... 0V, +18V	V_{OUT} (DAC701/703) .... Indefinite Short to Common
–V_{CC} to Common .... 0V, –18V	Power Dissipation 1W
V_{DD} to Common .... 0V, +18V	Storage Temperature .... –60°C to +150°C
Digital Data Inputs to Common .... –1V, +18V	Lead Temperature (soldering, 10s) .... 300°C
Reference Out to Common .... Indefinite Short to Common	
External Voltage Applied to R_F (DAC700/702) .... ±18V	NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
External Voltage Applied to D/A Output (DAC701/703) .... –5V to +5V	

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DAC700/01/02/03

3

DIGITAL-TO-ANALOG CONVERTERS

DICE INFORMATION

DAC702KD DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} −10kΩ
4	Bit 4 Input	19	No Connection
5	Bit 5 Input	20	R_{FB} −10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	−15V Supply	28	Reference Output
14	Bit 13 Input	29	−15V Supply
15	Bit 14 Input	30	Zener Test Point
			Do Not Use

Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	153 x 120	3.89 x 3.05
Die Thickness	20 Mils	0.5
Min. Pad Size	4 x 4	0.1 x 0.1
Metalization		Aluminum

DAC703KD DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} −10kΩ
4	Bit 4 Input	19	Voltage Output
5	Bit 5 Input	20	R_{FB} −10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	−15V Supply	28	Reference Output
14	Bit 13 Input	29	−15V Supply
15	Bit 14 Input	30	Zener Test Point
			Do Not Use

Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	153 x 120	3.89 x 3.05
Die Thickness	20 Mils	0.5
Min. Pad Size	4 x 4	0.1 x 0.1
Metalization		Aluminum

CONNECTION DIAGRAMS

NOTES: (1) Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply. (2) Decoupling capacitors are 0.1μF to 1.0μF. (3) Potentiometers are 10kΩ to 100kΩ. (4) 5kΩ (DAC700/701), 10kΩ (DAC702/703).

DAC700/01/02/03

DIGITAL-TO-ANALOG CONVERTERS
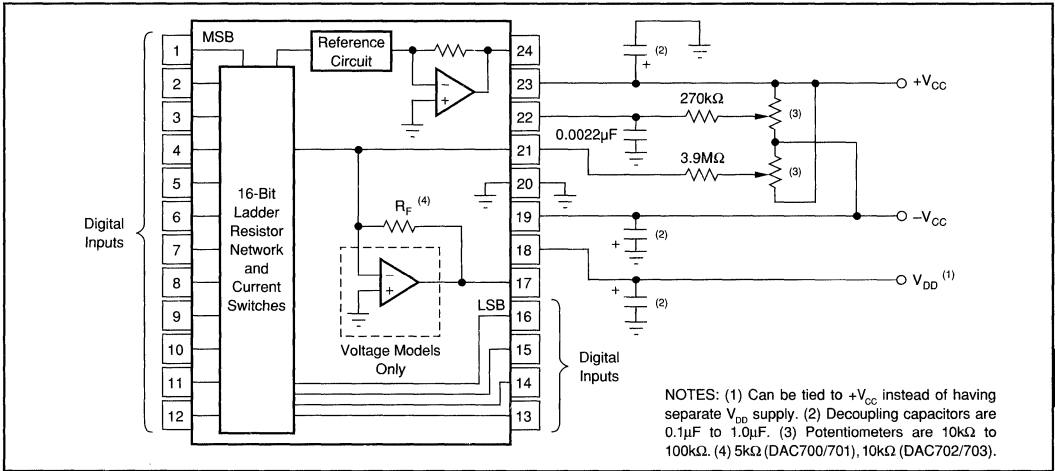
PIN ASSIGNMENTS

	ALL PACKAGES	
PIN #	**DAC700/702**	**DAC701/703**
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Reference Output	+6.3V Reference Output

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC702JP	24-Pin Plastic DIP	167
DAC703JP	24-Pin Plastic DIP	167
DAC702KP	24-Pin Plastic DIP	167
DAC703KP	24-Pin Plastic DIP	167
DAC700KH	24-Pin Ceramic DIP	165
DAC701KH	24-Pin Ceramic DIP	165
DAC702KH	24-Pin Ceramic DIP	165
DAC703KH	24-Pin Ceramic DIP	165
DAC700BH	24-Pin Ceramic DIP	165
DAC701BH	24-Pin Ceramic DIP	165
DAC702BH	24-Pin Ceramic DIP	165
DAC703BH	24-Pin Ceramic DIP	165
DAC700LH	24-Pin Ceramic DIP	165
DAC701LH	24-Pin Ceramic DIP	165
DAC702LH	24-Pin Ceramic DIP	165
DAC703LH	24-Pin Ceramic DIP	165
DAC700CH	24-Pin Ceramic DIP	165
DAC701CH	24-Pin Ceramic DIP	165
DAC702CH	24-Pin Ceramic DIP	165
DAC703CH	24-Pin Ceramic DIP	165
DAC702SH	24-Pin Ceramic DIP	165
DAC703SH	24-Pin Ceramic DIP	165
DAC703JU	24-Pin SOIC	239
DAC703KU	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	OUTPUT CONFIGURATION	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (% of FSR)	GAIN DRIFT MAX (ppm/°C)
DAC702JP, DAC703JP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.006	±30
DAC702KP, DAC703KP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700KH, DAC701KH	Ceramic DIP	0 to −2mA, 0 to +10V	0°C to +70°C	±0.003	±25
DAC702KH, DAC703KH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700BH, DAC701BH	Ceramic DIP	0 to −2mA, 0 to +10V	−25°C to +85°C	±0.003	±15
DAC702BH, DAC703BH	Ceramic DIP	±1mA, ±10V	−25°C to +85°C	±0.003	±15
DAC700LH, DAC701LH	Ceramic DIP	0 to −2mA, 0 to +10V	0°C to +70°C	±0.0015	±10
DAC700CH, DAC701CH	Ceramic DIP	0 to −2mA, 0 to +10V	−25°C to +85°C	±0.0015	±10
DAC700SH, DAC701SH	Ceramic DIP	0 to −2mA, 0 to +10V	−55°C to +125°C	±0.003	±15
DAC702LH, DAC703LH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.0015	±10
DAC702CH, DAC703CH	Ceramic DIP	±1mA, ±10V	−25°C to +85°C	±0.0015	±10
DAC702SH, DAC703SH	Ceramic DIP	±1mA, ±10V	−55°C to +125°C	±0.003	±15
DAC703JU	Plastic SOIC	±10V	0°C to +70°C	±0.006	±30
DAC703KU	Plastic SOIC	±10V	0°C to +70°C	±0.003	±25

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC700/701/702/703 accept complementary digital input codes in either binary format (CSB, unipolar or COB, bipolar). The COB models DAC702/703 may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

DIGITAL INPUT CODES	ANALOG OUTPUT		
	DAC700/701 Complementary Straight Binary (CSB)	DAC702/703 Complementary Offset Binary (COB)	DAC702/703 Complementary Two's Complement (CTC)*
0000$_H$	+ Full Scale	+ Full Scale	−1LSB
7FFF$_H$	+1/2 Full Scale	Bipolar Zero	− Full Scale
8000$_H$	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
FFFF$_H$	Zero	− Full Scale	Bipolar Zero
* Invert the MSB of the COB code with an external inverter to obtain CTC code.			

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential linearity error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC700/701/702/703 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with FFFF$_H$ (DAC700 and DAC701) applied to the digital inputs over the specified temperature range. For the bipolar models, zero is measured at 7FFF$_H$ (bipolar zero) applied to the digital inputs. This code corresponds to zero volts (DAC703) or zero milliamps (DAC702) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (DAC703) or 10V (DAC701) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.
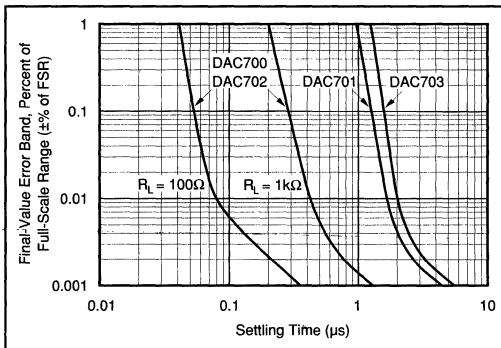
FIGURE 1. Final-Value Error Band vs Full-Scale Range Settling Time.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply (+V_{CC}), negative supply (–V_{CC}) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

FIGURE 2. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage, available to the user, has a tolerance of ±5% (KH models) and ±1% (BH models). A minimum of 1.5mA is available for external loads. Since the output impedance of the reference output is typically 1W, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001µF to 0.01µF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.
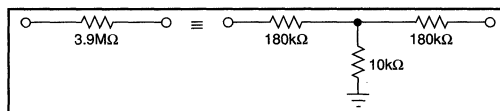
FIGURE 3. Equivalent Resistances.
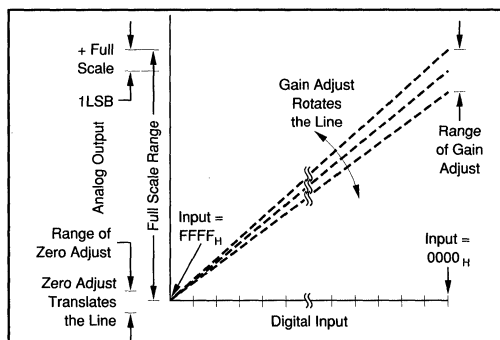
FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC700 and DAC701.

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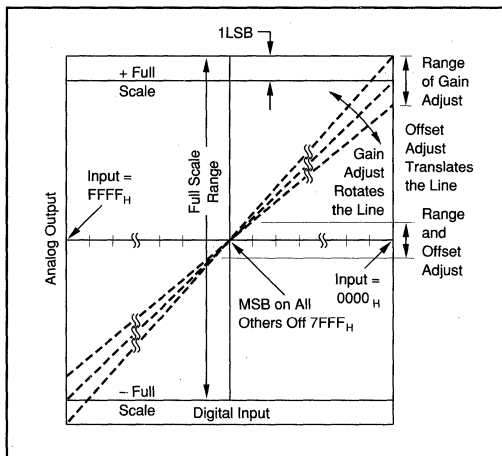
FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC702 and DAC703.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single $1k\Omega$ resistor.

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a 10V full-scale range, 1LSB is $153\mu V$. With a load current of 5mA, series wiring and connector resistance of only $30m\Omega$ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about $0.021\Omega/ft$. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{L\,MIN}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\,MIN}$ is $5k\Omega$, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC700 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under $20\mu A$ (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models (DAC700 or DAC702) with external precision output op amps. By sensing the output voltage at the load resistor (ie, by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.
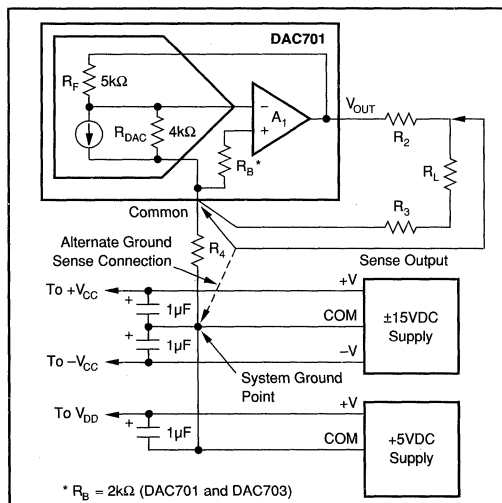
FIGURE 6. Output Circuit for Voltage Models.

VOLTAGE OUTPUT MODELS						
	ANALOG OUTPUT					
	DAC701 UNIPOLAR			DAC703 BIPOLAR		
DIGITAL INPUT CODE	16-BIT	15-BIT	14-BIT	16-BIT	15-BIT	14-BIT
1LSB (µV)	153	305	610	305	610	1224
0000_H (V)	+9.99985	+9.99969	+9.99939	+9.99960	+9.99939	+9.99878
FFFF_H (V)	0	0	0	−10.0000	−10.0000	−10.0000
ANALOG OUTPUT MODELS						
	ANALOG OUTPUT					
	DAC700 UNIPOLAR			DAC702 BIPOLAR		
DIGITAL INPUT CODE	16-BIT	15-BIT	14-BIT	16-BIT	15-BIT	14-BIT
1LSB (µA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H (mA)	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988
FFFF_H (mA)	0	0	0	+1.00000	+1.00000	+1.00000

TABLE II. Digital Input and Analog Output Relationships.

If the output cannot be sensed at Common or the sytem ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

	R_B	R_F	R_{DAC}
DAC702	2.45kΩ	10kΩ	2.45kΩ
DAC700	4kΩ	5kΩ	4kΩ

‡ R_B should be equal to the output impedance at the current output to compensate for the bias current drift of A_1. Use standard 10%, 1/4W carbon composition or equivalent resistors.
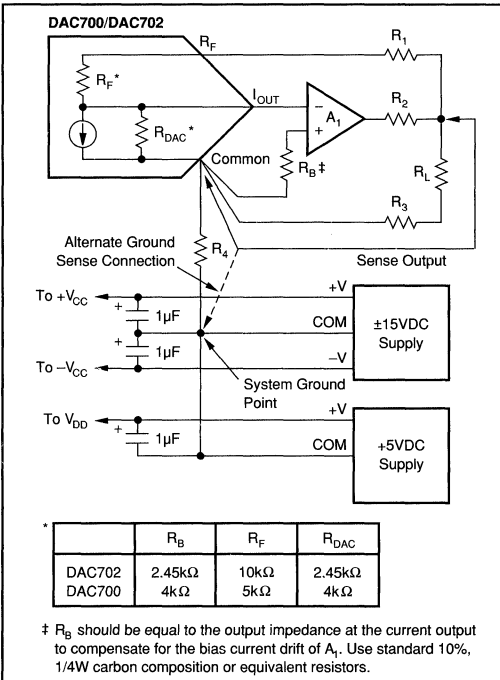
FIGURE 7. Preferred External Op Amp Configuration.

	R_F	R_{DAC}
DAC702	10kΩ	2.45kΩ
DAC700	5kΩ	4kΩ

$R_5 + R_7 = R_F + R_1$
$R_6 = R_{DAC}$
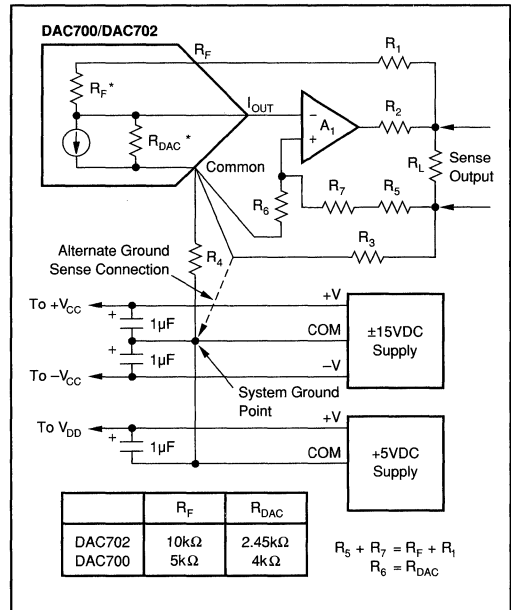
FIGURE 8. Differential Sensing Output Op Amp Configuration.

DAC700/01/02/03

DIGITAL-TO-ANALOG CONVERTERS

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/AS

DAC700 and DAC702 are current output devices and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

DAC700 or DAC702 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the

DAC700 and DAC702 ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and – 2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.
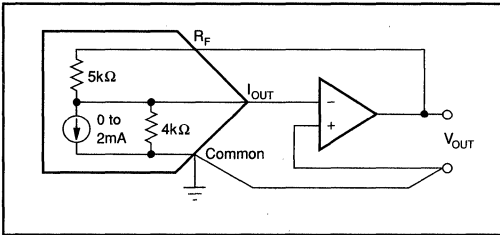
FIGURE 9. External Op Amp Using Internal Feedback Resistors.
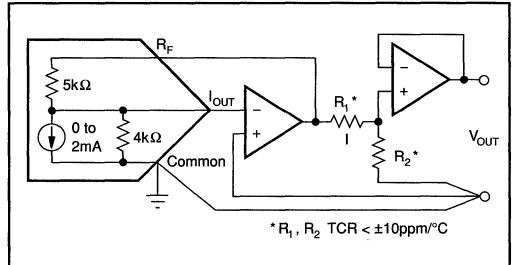
FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.
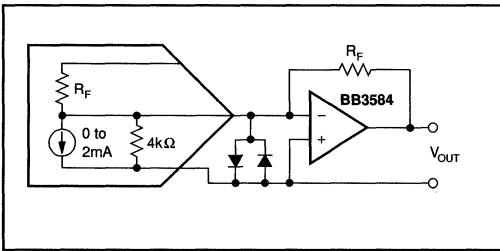
FIGURE 11. External Op Amp Using External Feedback Resistors.

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DAC707
DAC708/709

DAC707/08/09

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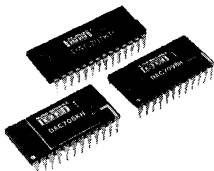
DIGITAL-TO-ANALOG CONVERTERS

Microprocessor-Compatible
16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **TWO-CHIP CONSTRUCTION**

● **HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES**

● **DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION**

● V_{OUT} **AND** I_{OUT} **MODELS**

● **HIGH ACCURACY:**
Linearity Error ±0.003% of FSR max
Differential Linearity Error ±0.006% of FSR max

● **MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE**

● **HERMETICALLY SEALED**

● **LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)**

DESCRIPTION

The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first).

The DAC707 is designed to interface to a 16-bit bus.

Data is written into a 16-bit latch and subsequently the D/A latch. The DAC707 has bipolar voltage output and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and for the DAC707, and DAC709, a voltage output amplifier. All models are available with an optional burn-in screening.

DAC707/708/709 Block Diagram

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP MIN	TYP	MAX	DAC707/708/709KH, DAC707KP MIN	TYP	MAX	DAC707/708/ 709BH, SH MIN	TYP	MAX	UNITS
INPUT										
DIGITAL INPUT										
Resolution			16			*			*	Bits
Bipolar Input Code (all models)		Binary Two's Complement			*			*		
Unipolar Input Code[1] (DAC708/709 only)		Unipolar Straight Binary						*		
Logic Levels[2]: V_{IH}	+2.0		+5.5	*		*	*		*	V
V_{IL}	−1.0		+0.8	*		*	*		*	V
I_{IH} (V_I = +2.7V)			1			*			*	μA
I_{IL} (V_I = +0.4V)			1			*			*	μA
TRANSFER CHARACTERISTICS										
ACCURACY[3]										
Linearity Error		±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.0045	±0.012		±0.003	±0.006		*	*	% of FSR
at Bipolar Zero[5, 6]					±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.30		*	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		*	*		*	*	% of FSR
Monotonicity Over Spec Temp Range	13			14			14			Bits
Power Supply Sensitivity: +V_{CC}, −V_{CC}		±0.0015	±0.006		*	*		*	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*	% of FSR/%V_{DD}
DRIFT (Over Spec Temp Range)[3]										
Total Error Over Temp Range[8]		±0.08			*	±0.15		*	±0.10	% of FSR
Total Full Scale Drift		±10			*	±25		*	±15	ppm of FSR/°C
Gain Drift		±10	±30		*	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)					±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±15		*	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			±0.012			+0.009, −0.006		*		% of FSR
Linearity Error Over Temp[5]			±0.012			±0.006		*		% of FSR
SETTLING TIME (to ±0.003% of FSR)[9]										
Voltage Output Models										
Full Scale Step (2kΩ load)		4			*	8		*	8	μs
1LSB Step at Worst Case Code[10]		2.5			*	4		*	4	μs
Slew Rate		10			*			*		V/μs
Current Output Models										
Full Scale Step (2mA): 10 to 100Ω Load					350			*		ns
1kΩ Load					1			*		μs
OUTPUT										
VOLTAGE OUTPUT MODELS										
Output Voltage Range										
DAC709: Unipolar (USB Code)					0 to +10			*		V
Bipolar (BTC Code)					±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*			*		V
Output Current	±5			*			*			mA
Output Impedance		0.15			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*		
CURRENT OUTPUT MODELS										
Output Current Range (±30% typ)										
DAC708: Unipolar (USB Code)					0 to −2			*		mA
Bipolar (BTC Code)					±1			*		mA
Unipolar Output Impedance (±30% typ)					4.0			*		kΩ
Bipolar Output Impedance (±30% typ)					2.45			*		kΩ
Compliance Voltage					±2.5			*		V

ELECTRICAL (CONT)

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP			DAC707/708/709KH, DAC707KP			DAC707/708/ 709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS										
Voltage (all models): +V_{CC}	+13.5	+15	+16.5	*	*	*	*	*	*	V
−V_{CC}	−13.5	−15	−16.5	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	V
Current (No Load, +15V Supplies)										
Current Output Models: +V_{CC}					+10	+25		*	*	mA
−V_{CC}					−13	−25		*	*	mA
V_{DD}					+5	+10		*	*	mA
Voltage Output Models: +V_{CC}		+16	+30		*	*		*	*	mA
−V_{CC}		−18	−30		*	*		*	*	mA
V_{DD}		+5	+10		*	*		*	*	mA
Power Dissipation (±15V supplies)										
Current Output Models					370	800		*	*	mW
Voltage Output Models		535			*	950		*	*	mW
TEMPERATURE RANGE										
Specification: BH Grades							−25		+85	°C
JP, KP, KH Grades	0		+70	*		*				°C
SH Grades							−55		+125	°C
Storage: Ceramic				−65		+150	−65		+150	°C
Plastic	−60		+100	*		*				°C

*Specification same as for models in column to the left.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution, ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) With gain and zero errors adjusted to zero at +25°C. (9) Maximum represents the 3σ limit. Not 100% tested for this parameter. (10) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

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BB

DAC707/08/09

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DIGITAL-TO-ANALOG CONVERTERS

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC707JP	28-Pin Plastic DBL Wide DIP	215
DAC707KP	28-Pin Plastic DBL Wide DIP	215
DAC707BH	28LD Side Brazed Hermetic Dip	144
DAC707KH	28LD Side Brazed Hermetic DIP	144
DAC707SH	28LD Side Brazed Hermetic DIP	144
DAC708BH	24LD Side Brazed Hermetic DIP	165
DAC708KH	24LD Side Brazed Hermetic DIP	165
DAC708SH	24LD Side Brazed Hermetic DIP	165
DAC709BH	24LD Side Brazed Hermetic DIP	165
DAC709KH	24LD Side Brazed Hermetic DIP	165
DAC709SH	24LD Side Brazed Hermetic DIP	165

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V, +15V
$+V_{CC}$ to COMMON	0V, +18V
$-V_{CC}$ to COMMON	0V, −18V
Digital Data Inputs to COMMON	−0.5V, V_{DD} +0.5
DC Current any input	±10mA
Reference Out to COMMON	Indefinite Short to COMMON
V_{OUT} (DAC707, DAC709)	Indefinite Short to COMMON
External Voltage Applied to R_F (pin 13 or 14, DAC708)	±18V
External Voltage Applied to D/A Output (pin 1, DAC707; pin 14, DAC709)	±5V
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	INPUT CONFIG	OUTPUT CONFIG
DAC707JP	0°C to +70°C	16-bit port	±10V output
DAC707JP-BI[1]	0°C to +70°C	16-bit port	±10V output
DAC707KP	0°C to +70°C	16-bit port	±10V output
DAC707KP-BI[1]	0°C to +70°C	16-bit port	±10V output
DAC707KH	0°C to +70°C	16-bit port	±10V output
DAC707KH-BI[1]	0°C to +70°C	16-bit port	±10V output
DAC707BH	−25°C to +85°C	16-bit port	±10V output
DAC707BH-BI[1]	−25°C to +85°C	16-bit port	±10V output
DAC707SH	−55°C to +125°C	16-bit port	±10V output
DAC707SH-BI[1]	−55°C to +125°C	16-bit port	±10V output
DAC708KH	0°C to +70°C	8-bit port	±1mA output
DAC708BH	−25°C to +85°C	8-bit port	±1mA output
DAC708SH	−55°C to +125°C	8-bit port	±1mA output
DAC709KH	0°C to +70°C	8-bit port	±10V output
DAC709BH	−25°C to +85°C	8-bit port	±10V output
DAC709SH	−55°C to +125°C	8-bit port	±10V output

NOTE: (1) 25 piece minimum order.

DESCRIPTION OF PIN FUNCTIONS

DAC707		Pin	DAC708/709	
DESIGNATOR	DESCRIPTION	#	DESIGNATOR	DESCRIPTION
V_{OUT}	Voltage output for DAC707 (±10V)	1	A_2	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	A_0	Latch enable for "low byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital common	3	A_1	Latch enable for "high byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ	Summing junction of the internal output op amp for the DAC707. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (−15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
$\overline{CLR}$	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
$\overline{WR}$	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
$\overline{A_1}$	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
$\overline{A_0}$	Enable for input latch (Active low)	12	DCOM	Digital common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (−15V)
D7	Data bit 7	21	$\overline{CLR}$	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

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DIGITAL-TO-ANALOG CONVERTERS

CONNECTION DIAGRAMS

DAC708/709

NOTES: (1) Potentiometer is 10kΩ to 100kΩ. (2) Decoupling capacitors are 0.1µF to 1.0µF.

Connect for bipolar operation.
Connect for 10V range.
Leave pin 13 open for 20V range.

DAC707

NOTES: (1) Potentiometers are 10kΩ to 100kΩ.
(2) Decoupling capacitors are 0.1µF to 1.0µF.
(3) Bypass, 0.0022µF to 0.01µF.
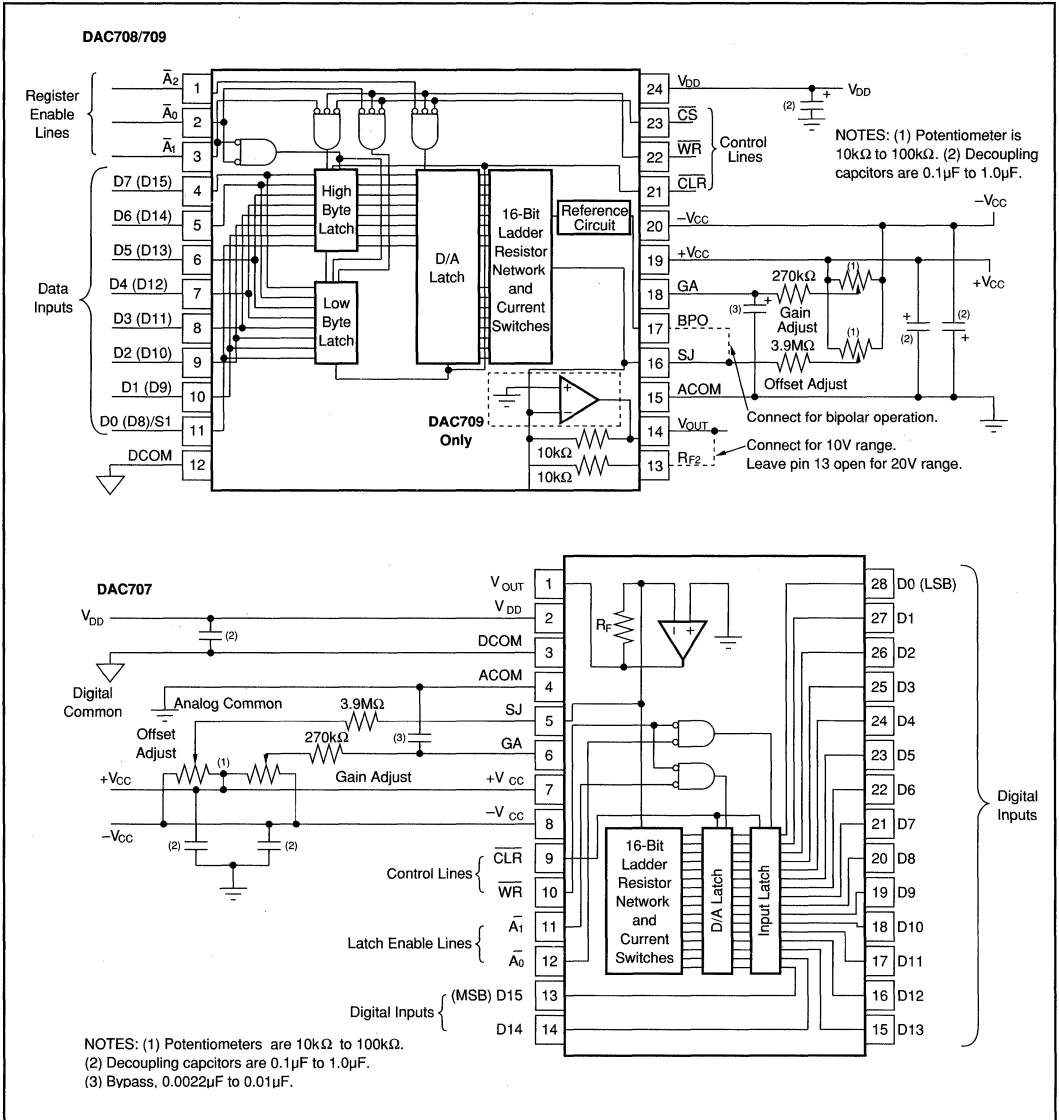
DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

Digital Input Codes	ANALOG OUTPUT	
	Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale −1LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	−1LSB
8000_H	+1/2 Full Scale	−Full Scale

NOTES: (1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (−Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of −1LSB maximum (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain Drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero Drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted). This code corresponds to zero volts (DAC707 and DAC709) or zero milliamps (DAC708) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.
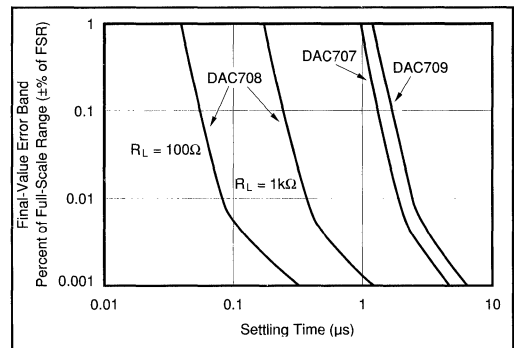
FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter

output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.
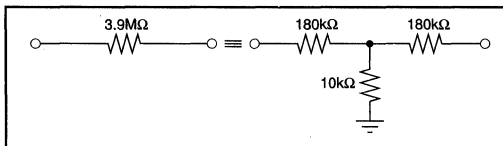
FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustments circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.
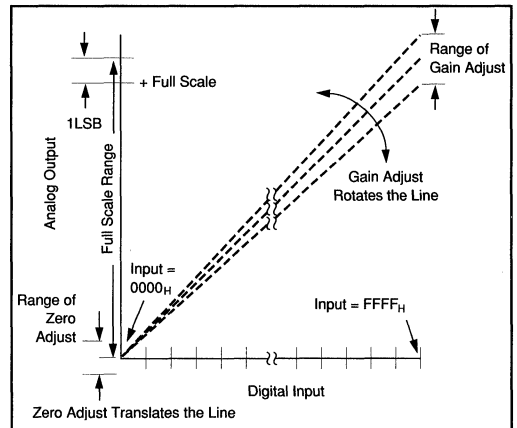
FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.
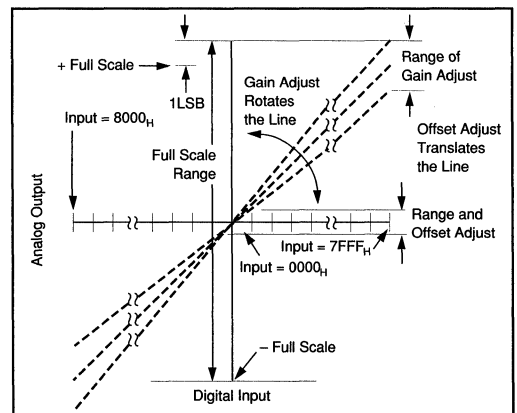
FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC707 and DAC708/709

VOLTAGE OUTPUT MODELS

Digital Input Code	Analog Output				Digital Input Code	Analog Output						
	Unipolar, 0 to +10V[1]			Units		Bipolar, ±10V			Bipolar, ±5V			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	µV	One LSB	305	610	1224	153	305	610	µV
FFFF$_H$	+9.99985	+9.99969	+9.99939	V	7FFFH	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000$_H$	0	0	0	V	8000H	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V

CURRENT OUTPUT MODELS

Digital Input Code	Analog Output				Digital Input Code	Analog Output			
	Unipolar, 0 to −2mA[1]			Units		Bipolar, ±1mA			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0.031	0.061	0.122	µA	One LSB	0.031	0.061	0.122	µA
FFFF$_H$	−1.99997	−1.99994	−1.99988	mA	7FFF$_H$	−0.99997	−0.99994	−0.99988	mA
0000$_H$	0	0	0	mA	8000$_H$	+1.00000	+1.00000	+1.00000	mA

NOTE: (1) MSB assumed to be inverted externally.

TABLE II. Digital Input and Analog Output Voltage/Current Relationships.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A}_0$, $\overline{A}_1$, and $\overline{A}_2$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A}_0$ and $\overline{A}_1$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A}_2$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A}_2$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 0000$_H$. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

DAC707

The DAC707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A}_0$. The

LOGIC TIMING - Parallel or Serial Data Input Over Temperature

		ns, min	ns, max
T_{DW}	Data valid to end of $\overline{WR}$		80
T_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$		80
T_{AW}	$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ valid to end of $\overline{WR}$		80
T_{WP}	Write pulse width		80
T_{DH}	Data hold after end of $\overline{WR}$		0
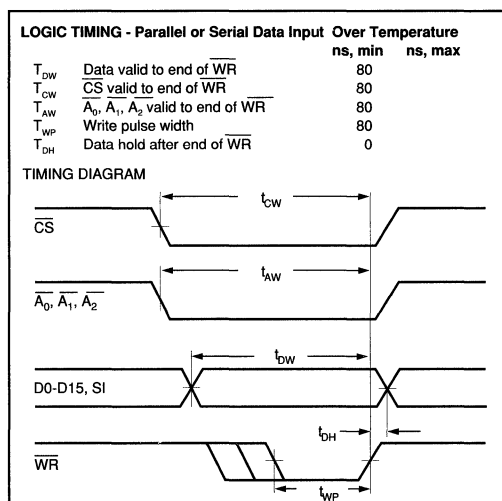
TIMING DIAGRAM

FIGURE 6. Logic Timing Diagram.

D/A latch is enabled by $\overline{A}_1$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

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DIGITAL-TO-ANALOG CONVERTERS

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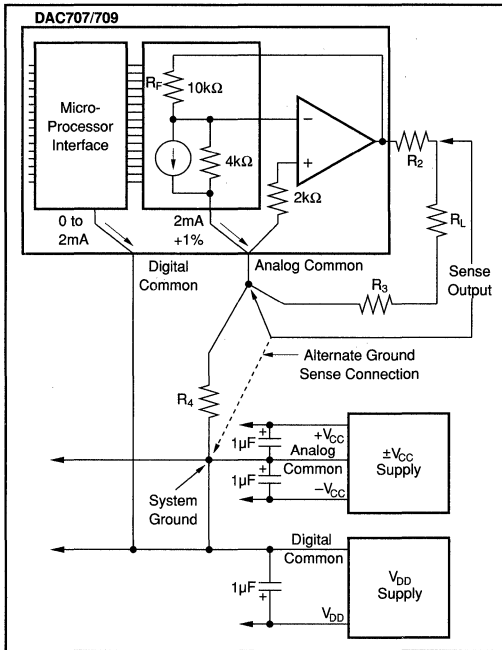
FIGURE 7. DAC707/709 Bipolar Output Circuit (Voltage Out).
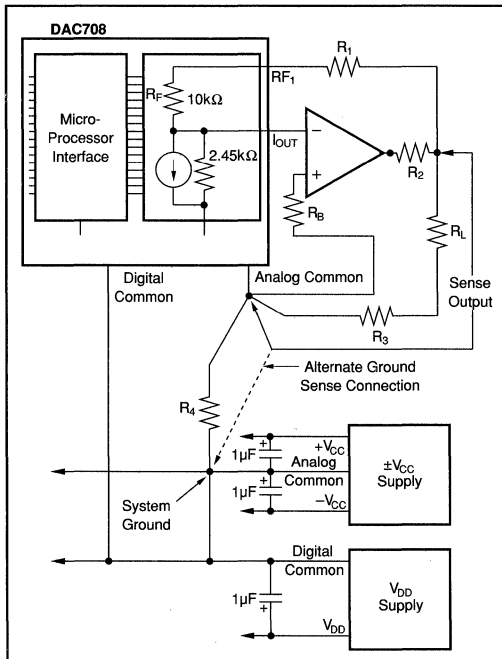
FIGURE 8. DAC708 Bipolar Output Circuit (with External Op Amp).

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

Figures 8 and 9 show two methods of connecting the current output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

In many applications it is impractical to sense the output voltage at ANALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10μA to 20μA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.
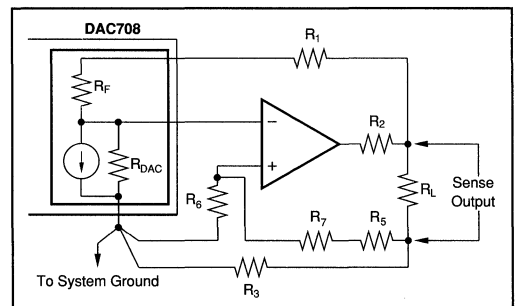
FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

BURN-IN SCREENING

Burn-in screening is an option available for the DAC707. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Model	Temp. Range	Burn-In Screening
DAC707JP-BI	0°C to 70°C	100°C
DAC707KP-BI	0°C to 70°C	100°C
DAC707KH-BI	–25°C to +85°C	125°C
DAC707BH-BI	–25°C to +85°C	125°C
DAC707SH-BI	–55°C to +125°C	125°C

All units are tested after burn-in to ensure that grade specifications are met.

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The $\overline{WR}$ input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 $\overline{WR}$ pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

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DIGITAL-TO-ANALOG CONVERTERS
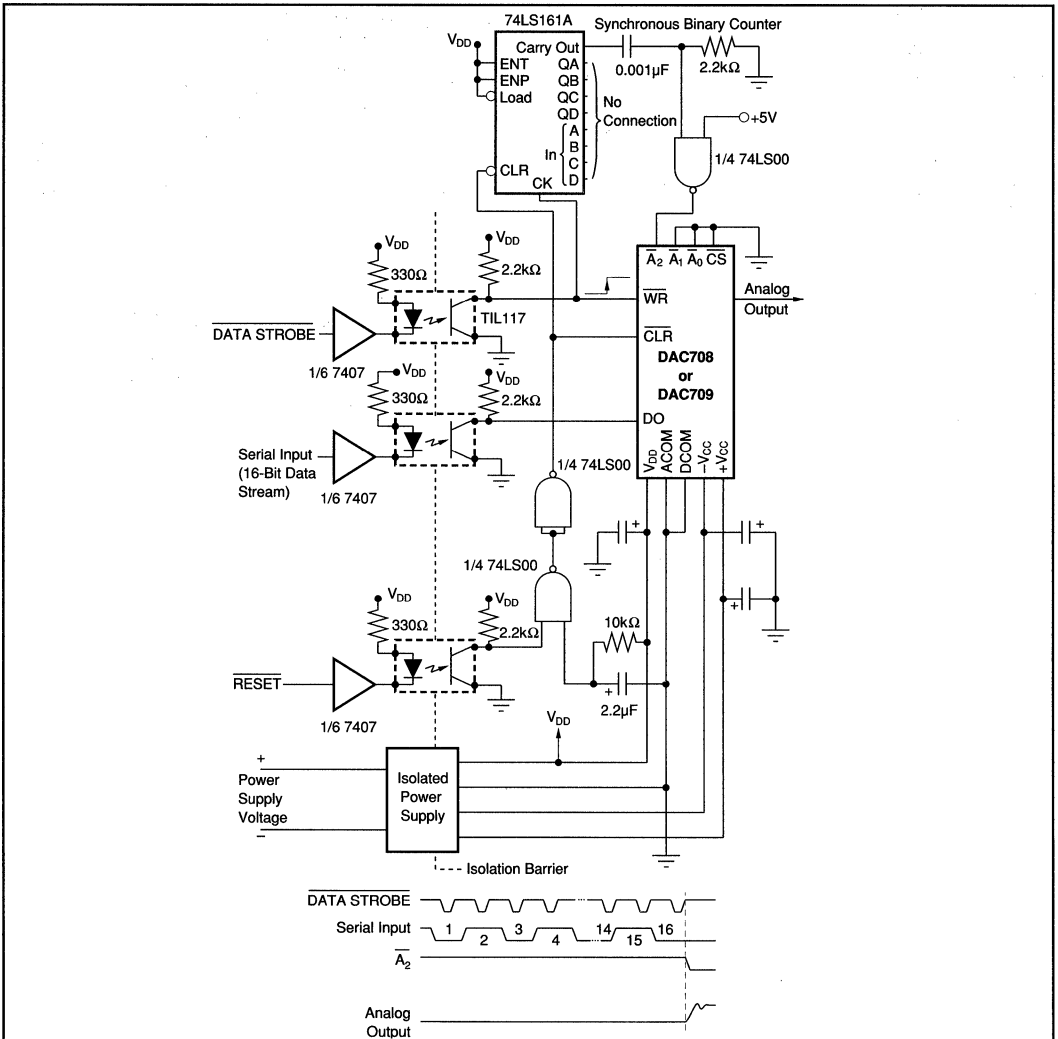
FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.
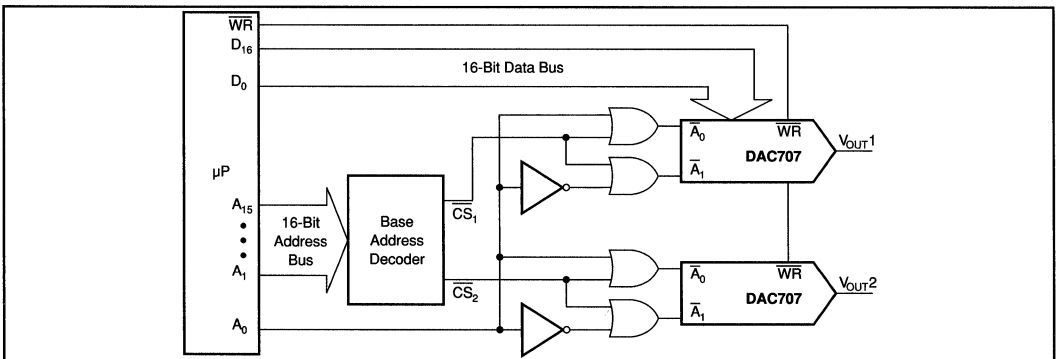
FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

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BB
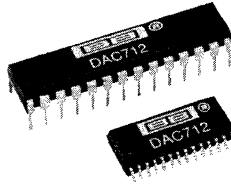
DAC712

16-BIT DIGITAL-TO-ANALOG CONVERTER WITH 16-BIT BUS INTERFACE

FEATURES

● **HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE**
● **VOLTAGE OUTPUT: ±10V**
● **13-, 14-BIT LINEARITY GRADES**
● **14-BIT MONOTONIC OVER TEMPERATURE (B GRADE)**
● **POWER DISSIPATION: 600mW max**
● **GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters**
● **SPECIFIED OVER –40°C to +85°C**
● **28-LEAD DIP AND SOIC PACKAGES**

DESCRIPTION

DAC712 is a complete 16-bit resolution D/A converter.

DAC712 has a precision +10V temperature compensated voltage reference, ±10V output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to bipolar zero.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC712 is available in two linearity error performance grades: ±4LSB DAC712P and U, ±2LSB DAC712PB or UB. DAC712 is specified at power supply voltages of ±12V and ±15V.

DAC712 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. DAC712 is specified over –40°C to +85°C.

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SPECIFICATIONS

ELECTRICAL

At $T_A = 25°C$, $+V_{CC} = +12V$ and $+15V$, $-V_{CC} = -12V$ and $-15V$ unless otherwise noted.

PARAMETER	DAC712P, U MIN	DAC712P, U TYP	DAC712P, U MAX	DAC712PB, UB MIN	DAC712PB, UB TYP	DAC712PB, UB MAX	UNITS
INPUT							
RESOLUTION			16			*	Bits
DIGITAL INPUTS							
Input Code	Binary Two's Complement			*			
Logic Levels[1]							
V_{IH}	+2.0		$+V_{CC}$	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} ($V_I = +2.7V$)			±10			*	µA
I_{IL} ($V_I = +0.4V$)			±10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Differential Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Monotonicity Over Temp	13			14			Bits
Gain Error[3]			±0.1			±0.1	%
T_{MIN} to T_{MAX}			±0.2			±0.15	%
Bipolar Zero Error[3]			±0.1			*	% FSR[2]
			±20			*	mV
T_{MIN} to T_{MAX}			±0.2			±0.15	% FSR
			±40			±30	mV
Power Supply Sensitivity Of Full Scale:			±0.003			*	% FSR/% V_{CC}
			±30			*	ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ ‖ 500pF Load)[4]							
20V Output Step		6			*	10	µs
1 LSB Output Step[5]		4			*		µs
Output Slew Rate		10			*		V/µs
Total Harmonic Distortion + Noise							
0dB, 1001Hz, $f_S = 100kHz$		0.005			*		%
–20dB, 1001Hz, $f_S = 100kHz$		0.03			*		%
–60dB, 1001Hz, $f_S = 100kHz$		3.0			*		%
SINAD							
1001Hz, $f_S = 100kHz$		87			*		dB
Digital Feedthrough[5]		2			*		nV-s
Digital-to-Analog Glitch Impulse[5]		15			*		nV-s
Output Noise Voltage (Includes Reference)		120			*		nV/$\sqrt{Hz}$
ANALOG OUTPUT							
Output Voltage Range							
$+V_{CC}$, $-V_{CC} = ±11.4V$	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM							
Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM, Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
$+V_{CC}$		13	15		*	*	mA
$-V_{CC}$		22	25		*	*	mA
Power Dissipation[6]		525	600		*	*	mW
TEMPERATURE RANGES							
Specification							
All Grades	–40		+85	*		*	°C
Storage	–60		+150	*		*	°C
Thermal Coefficient θ_{JA}							
DIP Package		75			*		°C/W
SOIC Package		75			*		°C/W

*Specifications are the same as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: FFFF$_{HEX}$ to 0000$_{HEX}$ and 0000$_{HEX}$ to FFFF$_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

ABSOLUTE MAXIMUM RATINGS

```
+V_CC to COMMON ........................................................ 0V, +17V
–V_CC to COMMON ........................................................ 0V, –17V
+V_CC to –V_CC ................................................................. 34V
Digital Inputs to COMMON ...................................... –1V to +V_CC
External Voltage Applied to BPO and Range Resistors .................... ±V_CC
V_REF OUT ...................................... Indefinite Short to COMMON
V_OUT ............................................. Indefinite Short to COMMON
Power Dissipation ............................................................. 750mW
Storage Temperature ...................................... –60°C to +150°C
Lead Temperature (soldering, 10s) .............................. +300°C
```

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC712P	Plastic DIP	246
DAC712U	Plastic SOIC	217
DAC712PB	Plastic DIP	246
DAC712UB	Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX at +25°C
DAC712P	Plastic DIP	–40°C to +85°C	±4LSB
DAC712U	Plastic SOIC	–40°C to +85°C	±4LSB
DAC712PB	Plastic DIP	–40°C to +85°C	±2LSB
DAC712UB	Plastic SOIC	–40°C to +85°C	±2LSB

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

TIMING DIAGRAM

TIMING SPECIFICATIONS

$T_A = –40°C$ to $+85°C$, $+V_{CC} = +12V$ or $+15V$, $–V_{CC} = –12V$ or $–15V$.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	80		ns
t_{AW}	$\overline{A_0}, \overline{A_1}$ Valid to End of $\overline{WR}$	80		ns
t_{AH}	$\overline{A_0}, \overline{A_1}$ Hold after End of $\overline{WR}$	10		ns
t_{DH}	Data Hold after end of $\overline{WR}$	10		ns
t_{WP}[1,2]	Write Pulse Width	60		ns
t_{CP}	CLEAR Pulse Width	150		ns

NOTES: (1) There is a timing interaction between $\overline{A_X}$ and $\overline{WR}$ when the edges (rising or falling) of $\overline{A_X}$ get close to the edges of $\overline{WR}$. In the limit, where either edge of $\overline{A_X}$ coincides with an edge of $\overline{WR}$, t_{WP} (min) increases to 80ns. For example as t_{AH} approaches 0ns, t_{WP} (min) increases to 80ns. (2) For single-buffered operation, t_{WP} is 80ns min. Refer to page 10.

TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	$1 \rightarrow 0 \rightarrow 1$	1	Load Input Latch
1	0	$1 \rightarrow 0 \rightarrow 1$	1	Load D/A Latch
1	1	$1 \rightarrow 0 \rightarrow 1$	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

DAC712

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DIGITAL-TO-ANALOG CONVERTERS

PIN CONFIGURATION

DCOM	1		28	LSB D0
ACOM	2		27	D1
V_{OUT}	3		26	D2
Offset Adjust	4		25	D3
$V_{REF\ OUT}$	5		24	D4
Gain Adjust	6		23	D5
$+V_{CC}$	7	DAC712	22	D6
$-V_{CC}$	8		21	D7
$\overline{CLR}$	9		20	D8
$\overline{WR}$	10		19	D9
$\overline{A_1}$	11		18	D10
$\overline{A_0}$	12		17	D11
D15 MSB	13		16	D12
D14	14		15	D13
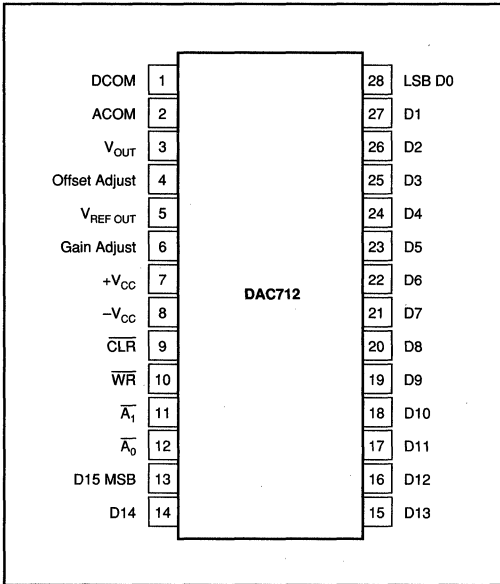
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Power Supply return for digital currents.
2	ACOM	Analog Supply Return.
3	V_{OUT}	±10V D/A Output.
4	Off Adj	Offset Adjust (Bipolar).
5	$V_{REF\ OUT}$	Voltage Reference Output.
6	Gain Adj	Gain Adjust.
7	$+V_{CC}$	+12V to +15V Supply.
8	$-V_{CC}$	−12V to −15V Supply.
9	$\overline{CLR}$	CLEAR. Sets D/A output to BIPOLAR ZERO (Active Low).
10	$\overline{WR}$	Write (Active Low).
11	$\overline{A_1}$	Enable for D/A latch (Active Low).
12	$\overline{A_0}$	Enable for Input latch (Active Low).
13	D15	Data Bit 15 (Most Significant Bit).
14	D14	Data Bit 14.
15	D13	Data Bit 13.
16	D12	Data Bit 12.
17	D11	Data Bit 11.
18	D10	Data Bit 10.
19	D9	Data Bit 9.
20	D8	Data Bit 8.
21	D7	Data Bit 7.
22	D6	Data Bit 6.
23	D5	Data Bit 5.
24	D4	Data Bit 4.
25	D3	Data Bit 3.
26	D2	Data Bit 2.
27	D1	Data Bit 1.
28	D0	Data Bit 0 (Least Significant Bit).

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

POWER SUPPLY REJECTION vs POWER SUPPLY RIPPLE FREQUENCY

LOGIC vs V LEVEL

± FULL SCALE OUTPUT SWING

Time (10μs/div)

SETTLING TIME, +10V TO −10V

Time (1μs/div)

SETTLING TIME, −10V TO +10V

Time (1μs/div)

Spectral Noise Density

Frequency (Hz)

DAC712

DIGITAL-TO-ANALOG CONVERTERS

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DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC712 is guaranteed over the specification temperature range to 13-, and 14-bits for performance grades DAC712P/U and DAC712PB/UB, respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_{HEX}$ to 0000_{HEX}, and 0000_{HEX} to $FFFF_{HEX}$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from $7FFF_{HEX}$ to 8000_{HEX}.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC712 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

DAC712 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a bipolar zero output (8000_{HEX} internally).

LOGIC INPUT COMPATIBILITY

DAC712 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic "0" and control inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC712 is designed to accept positive-true binary two's complement (BTC) input codes which are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of $7FFF_{HEX}$ gives a plus full scale output, 8000_{HEX} gives a minus full scale output, and 0000_{HEX} gives bipolar zero output.

INTERNAL REFERENCE

DAC712 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.
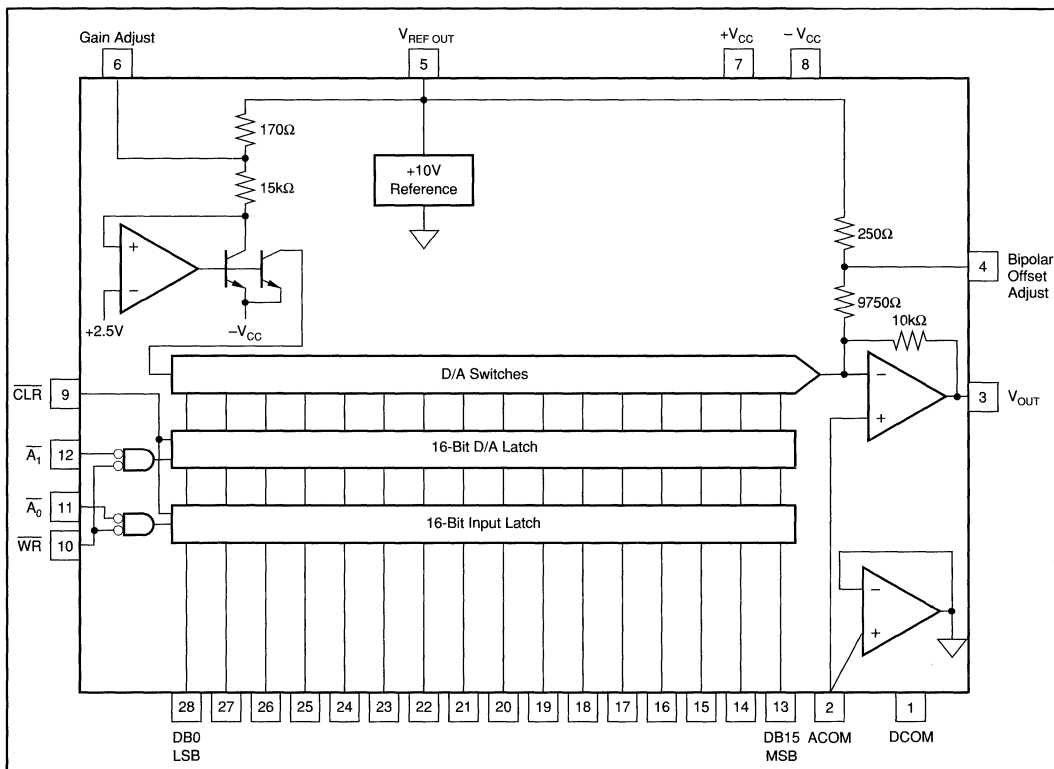
FIGURE 1. DAC712 Block Diagram.
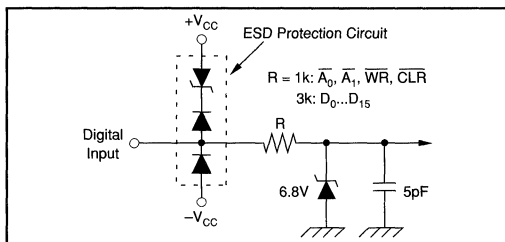
FIGURE 2. Equivalent Circuit of Digital Inputs.

FIGURE 3. Relationship of Offset and Gain Adjustments.

OUTPUT VOLTAGE SWING

The output amplifier of DAC712 is committed to a ±10V output range. DAC712 will provide a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.
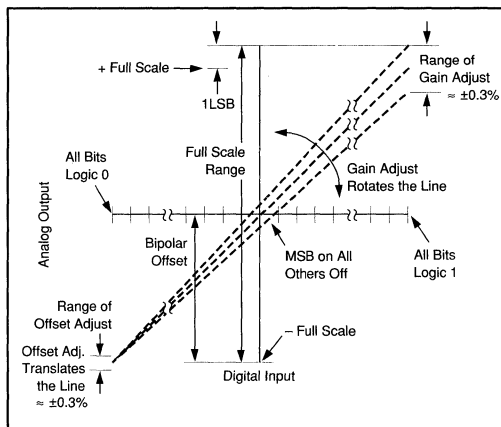
Offset Adjustment

Apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for –10V.

DAC712 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 305µV		
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V)	DESCRIPTION
$7FFF_H$	+9.999695	+ Full Scale –1LSB
4000_H	+5.000000	3/4 Scale
0001_H	+0.000305	BPZ + 1LSB
0000_H	0.000000	Bipolar Zero (BPZ)
$FFFF_H$	–0.000305	BPZ – 1LSB
$C000_H$	–5.000000	1/4 Scale
8000_H	–10.00000	Minus Full Scale

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milliinch wide printed circuit conductor 60 milliinches long will result in a voltage drop of 150µV.

The analog output of DAC712 has an LSB size of 305µV (–96dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC712's noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less

critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.
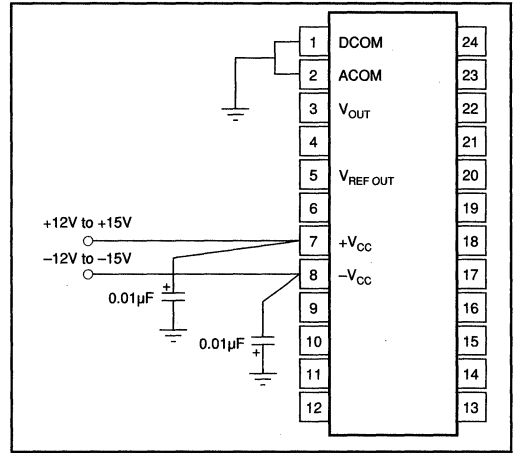
FIGURE 4. Power Supply Connections.

DAC712 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC712s are used or if DAC712 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because

there is no change in DAC712 ACOM current, provided that R₃ is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST
Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC712 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30μV to 50μV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC712 output amplifier is connected internally for the ±10V bipolar (20V) output range. That is, the bipolar offset resistor is connected to an internal reference voltage and the 20V range resistor is connected internally to V_{OUT}. DAC712 cannot be connected by the user for unipolar operation.

DIGITAL INTERFACE

BUS INTERFACE

DAC712 has 16-bit double-buffered data bus interface with control lines for easy interface to interface to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.
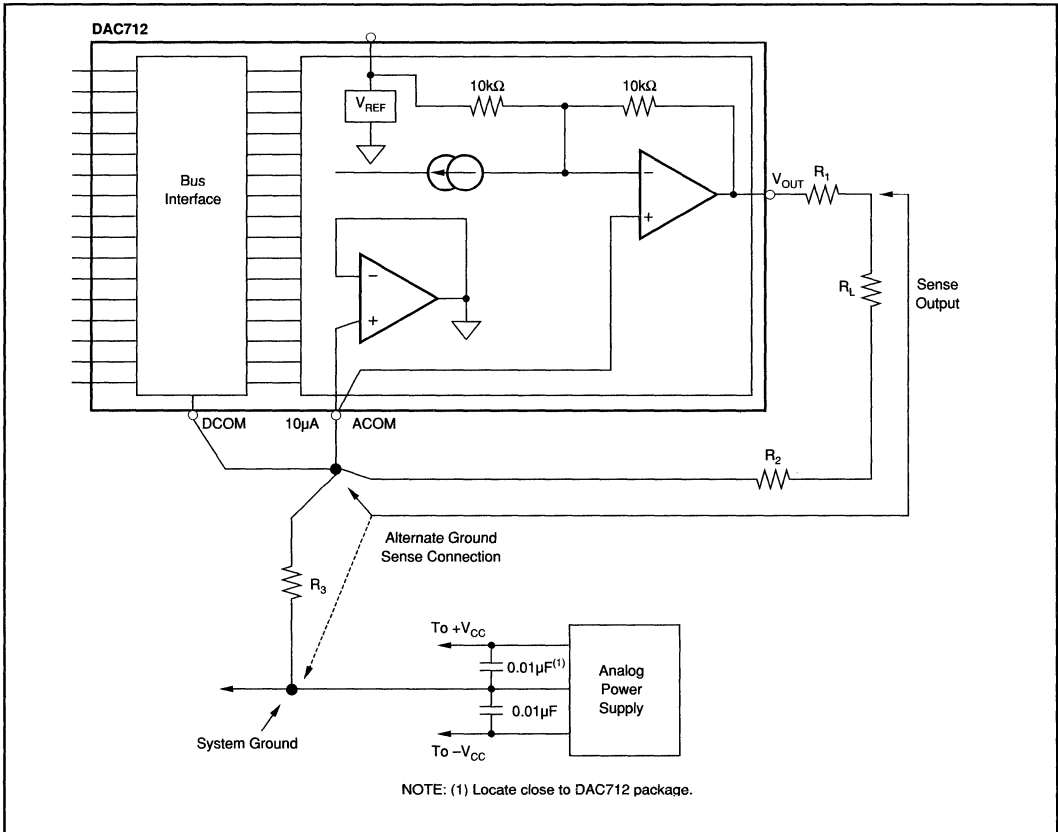
FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

$\overline{A_0}$ is the enable control for the DATA INPUT LATCH. $\overline{A_1}$ is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by $\overline{A_0}$, and $\overline{A_1}$. Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

$\overline{CLR}$ sets the INPUT DATA LATCH to all zero and the D/A LATCH to a code that gives bipolar 0V at the D/A output.

SINGLE-BUFFERED OPERATION

To operate the DAC712 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting $\overline{A_0}$ to DCOM. If $\overline{A_1}$ is not used to enable the

D/A, it should be connected to DCOM also. For this mode of operation, the width of $\overline{WR}$ will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

TRANSPARENT INTERFACE

The digital interface of the DAC712 can be made transparent by asserting $\overline{A_0}$, $\overline{A_1}$, and $\overline{WR}$ LOW, and asserting $\overline{CLR}$ HIGH.
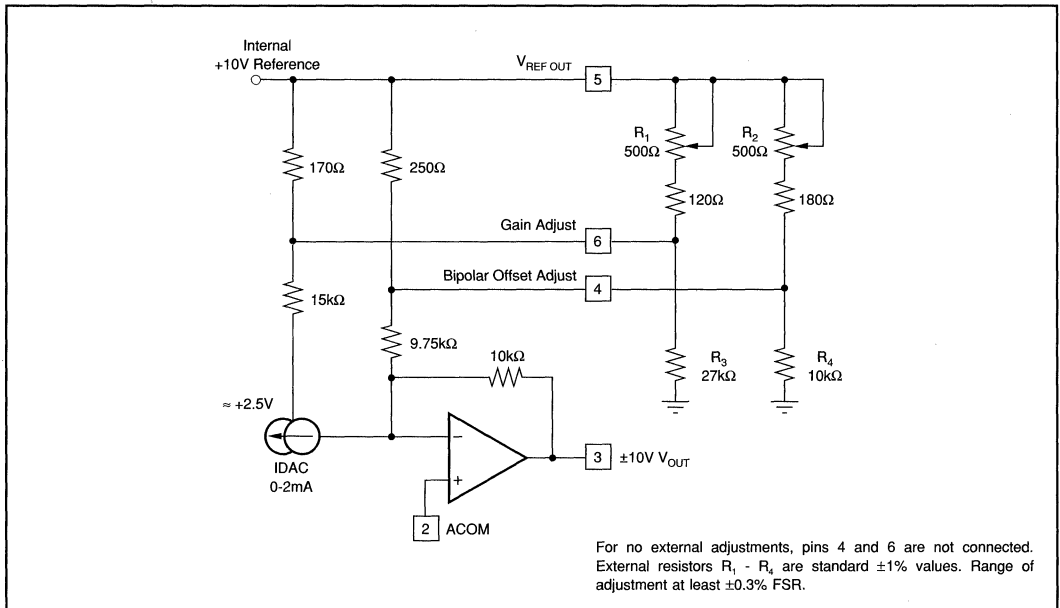
FIGURE 6. Manual Offset and Gain Adjust Circuits.
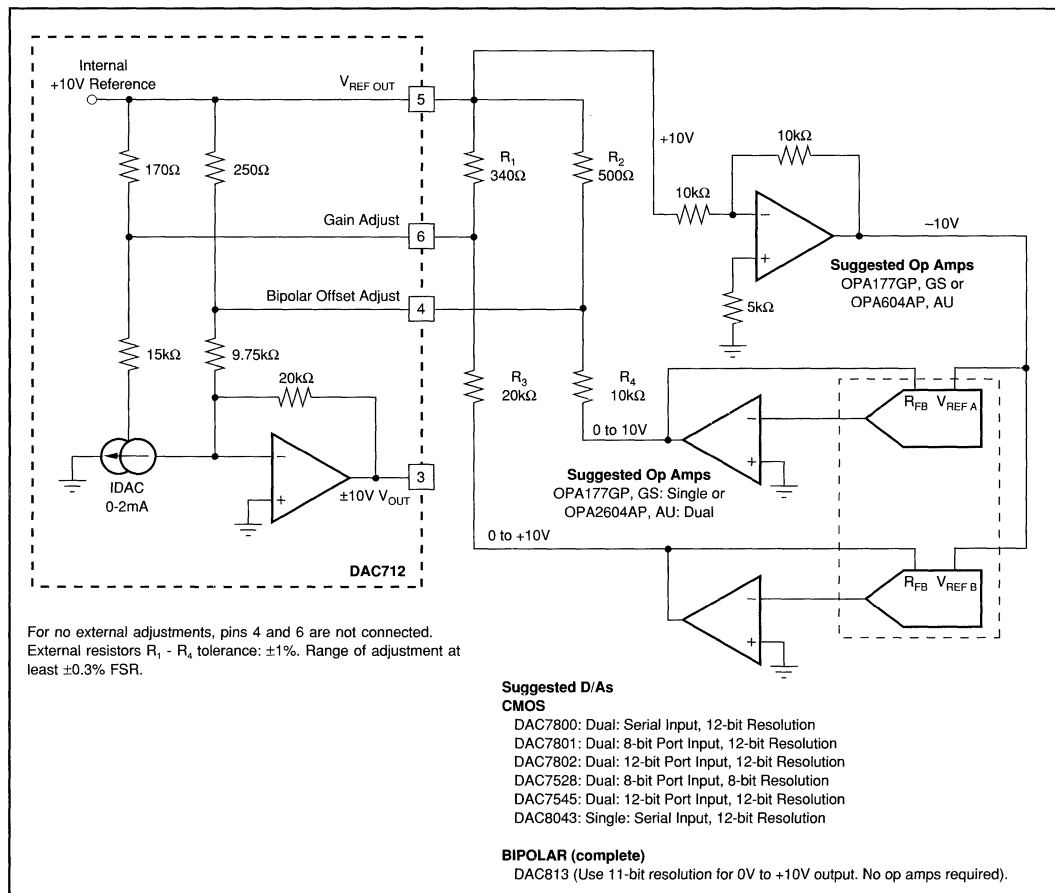
FIGURE 7. Gain and Offset Adjustment Using D/A Converters.

For no external adjustments, pins 4 and 6 are not connected.
External resistors R_1 - R_4 tolerance: ±1%. Range of adjustment at
least ±0.3% FSR.
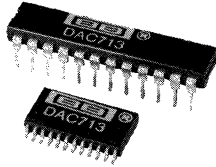
Suggested D/As
CMOS
　DAC7800: Dual: Serial Input, 12-bit Resolution
　DAC7801: Dual: 8-bit Port Input, 12-bit Resolution
　DAC7802: Dual: 12-bit Port Input, 12-bit Resolution
　DAC7528: Dual: 8-bit Port Input, 8-bit Resolution
　DAC7545: Dual: 12-bit Port Input, 12-bit Resolution
　DAC8043: Single: Serial Input, 12-bit Resolution

BIPOLAR (complete)
　DAC813 (Use 11-bit resolution for 0V to +10V output. No op amps required).

DAC712

3

DIGITAL-TO-ANALOG CONVERTERS

BURR - BROWN®

DAC713

16-Bit DIGITAL-TO-ANALOG CONVERTER
With 8-Bit Double-Buffered Bus Interface

FEATURES

● **HIGH-SPEED 8-BIT PARALLEL DOUBLE-BUFFERED INTERFACE**

● **VOLTAGE OUTPUT: ±10V, ±5V, 0 to +10V**

● **13-, 14-BIT LINEARITY GRADES**

● **14-BIT MONOTONIC OVER TEMPERATURE (B GRADE)**

● **GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters**

● **SPECIFIED OVER –40°C TO +85°C**

● **24-LEAD SKINNY DIP AND SOIC PACKAGES**

DESCRIPTION

DAC713 is a complete 16-bit resolution monolithic digital-to-analog converter.

DAC713 has precision temperature compensated voltage reference, voltage output amplifier and 8-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a RESET function.

GAIN and BIPOLAR OFFSET adjustment are arranged so that they can be set by external digital-to-analog converters as well as by potentiometers.

DAC713 is available in two linearity error grades: ±4LSB DAC713P and U, ±2LSB DAC713PB and UB, and are specified at power supply voltages of ±12V and ±15V.

DAC713 is packaged in a 24-pin plastic skinny-DIP and in a wide-body 24-lead plastic SOIC. DAC713 is specified over –40°C to +85°C.

PDS-1251

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = −12V and −15V unless otherwise noted.

PARAMETER	DAC713P, U MIN	TYP	MAX	DAC713PB, UB MIN	TYP	MAX	UNITS
INPUT							
RESOLUTION	16			*			Bits
DIGITAL INPUTS							
Input Code	Binary Two's Complement			*			
Logic Levels[1]							
V_{IH}	+2.0		$+V_{CC}$	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_i = +2.7V)			±10			*	µA
I_{IL} (V_i = +0.4V)			±10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Differential Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Monotonicity Over							
T_{MIN} to T_{MAX}	13			14			Bits
Gain Error[3]			±0.1			*	%
T_{MIN} to T_{MAX}			±0.25			±0.02	%
Unipolar/Bipolar Zero Error[3]			±0.1			*	% of FSR[2]
T_{MIN} to T_{MAX}			±0.2			±0.15	% of FSR
Power Supply Sensitivity of Gain			±0.003			*	%FSR/%+V_{CC}
			±30			*	ppm FSR/%V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ ‖ 500pF Load)[4]							
20V Output Step		6			*	10	µs
1LSB Output Step[5]		4			*		µs
Output Slew Rate		10			*		V/µs
Total Harmonic Distortion							
0dB, 1001Hz, f_S = 100kHz		0.005			*		%
−20dB, 1001Hz, f_S = 100kHz		0.03			*		%
−60dB, 1001Hz, f_S = 100kHz		3.0			*		%
SINAD: 1001Hz, f_S = 100kHz		87			*		dB
Digital Feedthrough[5]		2			*		nV–s
Digital-to-Analog Glitch Impulse[5]		15			*		
Output Noise Voltage (includes reference)		120			*		nV/√Hz
ANALOG OUTPUT							
Output Voltage Range							
$+V_{CC}$, $-V_{CC}$ = ±11.4V	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage							
$+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	−11.4	−15	−16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
$+V_{CC}$		15	TBD		*	*	mA
$-V_{CC}$		24	TBD		*	*	mA
Power Dissipation[6]			TBD			*	W
TEMPERATURE RANGES							
Specification	−40		+85	*		*	°C
Storage	−60		+150	*		*	°C
Thermal Coefficient, θ_{JA}							
Plastic DIP		75			*		°C/W
Plastic SOIC		75			*		°C/W

*Same specification as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst-case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. (6) Typical supply voltages times maximum currents.

DAC713

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DIGITAL-TO-ANALOG CONVERTERS

PIN CONFIGURATION

Top View   **DIP AND SOIC**

$\overline{A2}$	1		24	$\overline{CS}$
$\overline{A0}$	2		23	$\overline{WR}$
$\overline{A1}$	3		22	$\overline{CLR}$
D7/D15	4		21	$-V_{CC}$
D6/D14	5		20	$+V_{CC}$
D5/D13	6	**DAC713**	19	Gain Adjust
D4/D12	7		18	$V_{REF\ OUT}$
D3/D11	8		17	Offset Adjust
D2/D10	9		16	R_{BPO}
D1/D9	10		15	R_{FB2}
D0/D8	11		14	V_{OUT}
DCOM	12		13	ACOM

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V to +17V
$-V_{CC}$ to COMMON	0V to –17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	–1V to $+V_{CC}$
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR max at +25°C	TEMPERATURE RANGE
DAC713P	Plastic DIP	±4	–40°C to +85°C
DAC713U	Plastic SOIC	±4	–40°C to +85°C
DAC713PB	Plastic DIP	±2	–40°C to +85°C
DAC713UB	Plastic SOIC	±2	–40°C to +85°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC713P	Plastic DIP	243
DAC713U	Plastic SOIC	239
DAC713PB	Plastic DIP	243
DAC713UB	Plastic SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TIMING SPECIFICATIONS

$T_A = -40°C$ to $+85°C$, $+V_{CC} = +12V$ or $+15V$, $-V_{CC} = -12V$ or $-15V$

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	80		ns
t_{CS}	$\overline{CS}$ Valid to End of $\overline{WR}$	80		ns
t_{AW}	$\overline{A0}, \overline{A1}, \overline{A2}$: Valid to End of $\overline{WR}$	80		ns
t_{DH}	Data Hold After End of $\overline{WR}$	10		ns
t_{AH}	$\overline{A0}, \overline{A1}, \overline{A2}$ HOLD after End of $\overline{WR}$	10		ns
t_{WP}	Write Pulse Width	80		ns
t_{CP}	CLEAR Pulse Width	150		ns

TIMING DIAGRAM

$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{WR}$	$\overline{CS}$	$\overline{CLR}$	DESCRIPTION
0	1	1	1→0→1	0	1	Load LOW Byte
1	0	1	1→0→1	0	1	Load HIGH Byte
1	1	0	1→0→1	0	1	Load D/A Latch
X	X	X	X	1	1	No Change
X	X	X	1	X	1	No Change
X	X	X	X	X	0	RESET D/A Latch

NOTE: X = Don't Care.

TIMING DIAGRAM
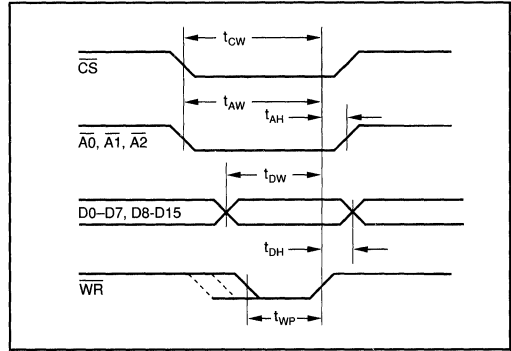
DAC713

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DIGITAL-TO-ANALOG CONVERTERS

BURR - BROWN®
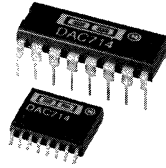
DAC714

16-Bit DIGITAL-TO-ANALOG CONVERTER
With Serial Data Interface

FEATURES:

- **SERIAL DIGITAL INTERFACE**
- **VOLTAGE OUTPUT: ±10V, ±5V, 0 to +10V**
- **POWER DISSIPATION: 600mW max**
- **13-, 14-BIT LINEARITY GRADES**
- **14-BIT MONOTONIC OVER TEMPERATURE (B GRADE)**
- **GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters**
- **SPECIFIED OVER –40°C TO +85°C**
- **16-LEAD SKINNY DIP AND WIDE BODY SOIC PACKAGES**

DESCRIPTION

DAC714 is a complete monolithic D/A converter. A precision +10V temperature compensated voltage reference, ±10V voltage output amplifier and serial interface.

The serial digital interface is fast, 60ns max minimum write pulse width, and has a RESET function.

GAIN and BIPOLAR OFFSET adjustment are arranged so that they can be set by external D/A converters as well as by potentiometers.

DAC714 is available in two linearity error performance grades: ±4LSB DAC714P and U, ±2LSB DAC714PB and UB, and are specified at power supply voltages of ±12V and ±15V.

DAC714 is packaged in a 16-pin plastic skinny-DIP and in a 16-lead wide-body plastic SOIC. DAC714 is specified over –40°C to +85°C.

PDS-1252

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, +V_{CC} = +12V and +15V, −V_{CC} = −12V and −15V unless otherwise noted.

PARAMETER	DAC714P, U MIN	DAC714P, U TYP	DAC714P, U MAX	DAC714PB, UB MIN	DAC714PB, UB TYP	DAC714PB, UB MAX	UNITS
INPUT							
RESOLUTION		16			*		Bits
DIGITAL INPUTS							
Serial Data Input Code		Binary Two's Complement			*		
Logic Levels[(1)]							
V_{IH}	+2.0		+V_{CC}	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	μA
I_{IL} (V_I = +0.4V)			±10			*	μA
DIGITAL OUTPUT							
Serial Data							
V_{OL} (I_{SINK} = 1.6mA)	0		+0.4	*		*	V
V_{OH} (I_{SOURCE} = 500μA)	+2.4		+5	*		*	V
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Differential Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Monotonicity Over Spec Temp Range	13			14			Bits
Gain Error[(3)]			±0.1			*	%
T_{MIN} to T_{MAX}			±0.25			±0.2	%
Unipolar/Bipolar Zero Error[(3)]			±0.1			±0.1	% of FSR[(2)]
T_{MIN} to T_{MAX}			±0.2			±0.15	% of FSR
Power Supply Sensitivity of Gain			±0.003			*	%FSR/%+V_{CC}
			±30			*	ppm FSR/%V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ ‖ 500pF Load)[(4)]							
20V Output Step		6			*	10	μs
1LSB Output Step[(5)]		4			*		μs
Output Slew Rate		10			*		V/μs
Total Harmonic Distortion							
0dB, 1001Hz, f_S = 100kHz		0.005			*		%
−20dB, 1001Hz, f_S = 100kHz		0.03			*		%
−60dB, 1001Hz, f_S = 100kHz		3.0			*		%
SINAD: 1001Hz, f_S = 100kHz		87			*		dB
Digital Feedthrough[(5)]		2			*		nV−s
Digital-to-Analog Glitch Impulse[(5)]		15			*		nV−s
Output Noise Voltage (includes reference)		120			*		nV/√Hz
ANALOG OUTPUT							
Output Voltage Range							
+V_{CC}, −V_{CC} = ±11.4V	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage							
+V_{CC}	+11.4	+15	+16.5	*	*	*	V
−V_{CC}	−11.4	−15	−16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
+V_{CC}		13	TBD		*	*	mA
−V_{CC}		22	TBD		*	*	mA
Power Dissipation[(6)]			TBD			*	W
TEMPERATURE RANGES							
Specification							
All Grades	−40		+85	*		*	°C
Storage	−60		+150	*		*	°C
Thermal Coefficient, θ_{JA}		75			*		°C/W

*Same specification as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst-case Binary Two's Complement code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. (6) Typical (i.e. rated) supply voltages times maximum currents.

DAC714

DIGITAL-TO-ANALOG CONVERTERS

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PIN CONFIGURATION

Top View

		DAC714		
$\overline{CLK}$	1		16	$\overline{CLR}$
$\overline{A_0}$	2		15	$-V_{CC}$
$\overline{A_1}$	3		14	Gain Adjust
SDI	4		13	Offset Adjust
SDO	5		12	$V_{REF\ OUT}$
DCOM	6		11	R_{BPO}
$+V_{CC}$	7		10	R_{FB2}
ACOM	8		9	V_{OUT}

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V to +17V
$-V_{CC}$ to COMMON	0V to –17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	–1V to $+V_{CC}$
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR max at +25°C	TEMPERATURE RANGE
DAC714P	Plastic DIP	±4	–40°C to +85°C
DAC714U	Plastic SOIC	±4	–40°C to +85°C
DAC714PB	Plastic DIP	±2	–40°C to +85°C
DAC714UB	Plastic SOIC	±2	–40°C to +85°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC714P	Plastic DIP	180
DAC714U	Plastic SOIC	211
DAC714PB	Plastic DIP	180
DAC714UB	Plastic SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TIMING SPECIFICATIONS

$T_A = -40°C$ to $+85°C$, $+V_{CC} = +12V$ or $+15V$, $-V_{CC} = -12V$ or $-15V$.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{CLK}	Data Clock Period	120		ns
t_{CL}	Clock LOW	60		ns
t_{CH}	Clock HIGH	60		ns
t_{A0S}	Setup Time for $\overline{A_0}$	60		ns
t_{A1S}	Setup Time for $\overline{A_1}$	60		ns
t_{A1H}	Hold Time for $\overline{A_1}$	0		ns
t_{DS}	Setup Time for DATA	60		ns
t_{DH}	Hold Time for DATA	10		ns
t_{A0H}	Hold Time for $\overline{A_0}$	0		ns
t_{DSOP}	Output Propogation Delay	140		ns

TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{CLK}$	$\overline{CLR}$	DESCRIPTION
0	1	$1 \rightarrow 0 \rightarrow 1$	1	Shift Serial Data into SDI
1	0	$1 \rightarrow 0 \rightarrow 1$	1	Load D/A Latch
1	1	$1 \rightarrow 0 \rightarrow 1$	1	No Change
0	0	$1 \rightarrow 0 \rightarrow 1$	1	Two Wire Operation[1]
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

NOTES: X = Don't Care. (1) All digital input change will appear at the output.

TIMING DIAGRAMS
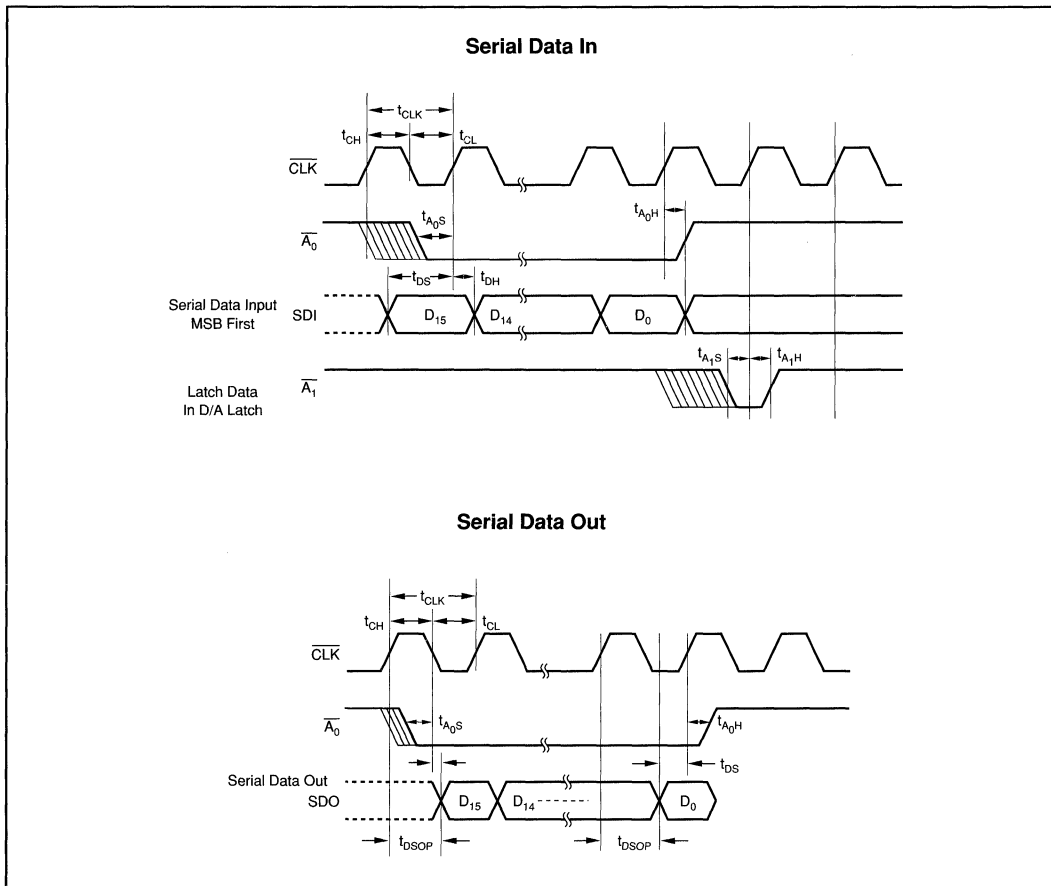
Serial Data In

Serial Data Out

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BB
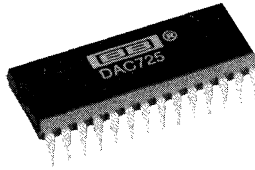
DAC725

Dual 16-Bit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **COMPLETE DUAL V_{OUT} DAC**
● **DOUBLE-BUFFERED INPUT REGISTER**
● **HIGH-SPEED DATA INPUT:**
  Serial or Parallel
● **HIGH ACCURACY: ±0.003% Linearity Error**
● **14-BIT MONOTONICITY OVER**
  TEMPERATURE
● **PLASTIC PACKAGE**
● **CLEAR INPUT TO SET ZERO OUTPUT**

DESCRIPTION

The DAC725 is a dual 16-bit DAC, complete with internal reference and output op amps. The DAC725 is designed to interface to an 8-bit microprocessor bus, but can also be interfaced to wider buses. The hybrid construction minimizes the digital feedthrough typically associated with products that combine the digital bus interface circuitry with high-accuracy analog circuitry.

The 16-bit data word is loaded into either of the DACs in two 8-bit bytes per 16-bit word. The versatility of the control lines allows the data word to be directed to either DAC, in any order. The voltage-out DACs are dedicated to a bipolar output voltage of ±10V. The output is immediately set to 0V when the Clear command is given. This feature, combined with the bus interfacing and complete DAC circuitry, makes the DAC725 ideal for automatic test equipment, power control, servo systems, and robotics applications.

PDS-757D

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, and after a 10-minute warm-up unless otherwise noted.

PARAMETER	DAC725JP MIN	DAC725JP TYP	DAC725JP MAX	DAC725KP MIN	DAC725KP TYP	DAC725KP MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Bipolar Input Code		Binary Twos Complement			*		
Logic Levels[1]: V_{IH}	+2		+5.5	*		*	V
V_{IL}	−1		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			1			*	µA
I_{IL} (V_I = +0.4V)			1			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.003	±0.006		±0.0015	±0.003	% of FSR[2]
Differential Linearity Error[3]		±0.0045	±0.012		0.003	±0.006	% of FSR
At Bipolar Zero: KP[3, 4]					±0.003	±0.006	% of FSR
Gain Error[5]		±0.07	±0.2		*	±0.15	%
Bipolar Zero Error[5]		±0.05	±0.1		*	*	% of FSR
Montonicity Over Specified Temp. Range	13			14			Bits
Power Supply Sensitivity: +V_{CC}, −V_{CC}		±0.0015	±0.006		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*	% of FSR/%V_{DD}
DRIFT (Over Specified Temperature Range)							
Gain Drift		±10			*	±25	ppm/°C
Bipolar Zero Drift		±5			*	±12	ppm of FSR/°C
Differential Linearity Over Temperature[3]		±0.0045	±0.012		±0.003	±0.006	% of FSR
Linearity Error Over Temperature[3]			±0.012			±0.006	% of FSR
SETTLING TIME (to ±0.003% of FSR)[6]							
20V Step (2kΩ load)		4			*	8	µs
1LSB Step at Worst-Case Code[7]		2.5			*	4	µs
Slew Rate		10			*		V/µs
OUTPUT							
Output Voltage Range[8]	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: +V_{CC}	+11.4	+15	+16.5	*	*	*	V
−V_{CC}	−11.4	−15	−16.5	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Current (No load, ±15V supplies): +V_{CC}		+29	+35		*	*	mA
−V_{CC}		−35	−40		*	*	mA
V_{DD}		+6	+10		*	*	mA
Power Dissipation (±15V supplies)		920	1175		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Storage	−60		+150	*		*	°C

*Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74HC and 54/74HTC compatible over the specification temperature range. (2) FSR means Full-Scale Range. For example, for ±10V output, FSR = 20V. (3) ±0.0015% of FSR is equal to 1LSB in 16-bit resolution. ±0.003% of FSR is equal to 1LSB in 15-bit resolution. ±0.006% of FSR is equal to 1LSB in 14-bit resolution. (4) Error at input code 0000_H (BTC). (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (6) Maximum represents the 3σ limit. Not tested for this parameter. (7) The bipolar worst-case code change is $FFFF_H$ to 0000_H (BTC). (8) Minimum supply voltage for ±10V output swing is approximately ±13V. Output swing for ±12V supplies is at least ±9V.

DAC725

DIGITAL-TO-ANALOG CONVERTERS

3

CONNECTION DIAGRAM
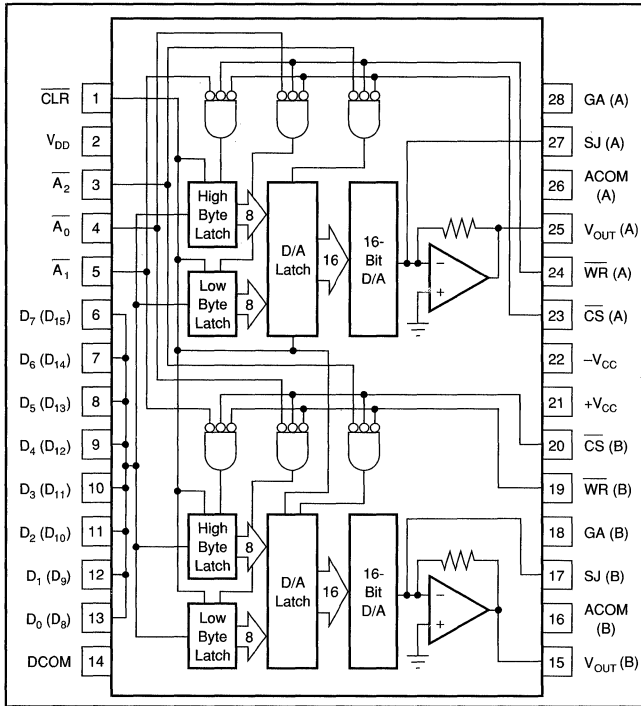
PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	CLR	Clear line. Sets the D/A register to 0000_{HEX}, which gives bipolar zero on the D/A output.
2	V_{DD}	Logic supply (+5V).
3	$\overline{A_2}$	Latch enable for D/A latch (active low).
4	$\overline{A_0}$	Latch enable for "low byte" input (active low).
5	$\overline{A_1}$	Latch enable for "high byte" input (active low).
6	D_7 (D_{15}) (MSB)	Input for data bit 7 if enabling low byte (LB) latch, or data bit 15 if enabling the high byte (HB) latch.
7	D_6 (D_{14})	Input for data bit 6 if enabling LB latch, or data bit 14 if enabling HB latch.
8	D_5 (D_{13})	Data bit 5 (LB) or data bit 13 (HB).
9	D_4 (D_{12})	Data bit 4 (LB) or data bit 12 (HB).
10	D_3 (D_{11})	Data bit 3 (LB) or data bit 11 (HB).
11	D_2 (D_{10})	Data bit 2 (LB) or data bit 10 (HB).
12	D_1 (D_9)	Data bit 1 (LB) or data bit 9 (HB).
13	D_0 (D_8)	Data bit 0 (LB) or data bit 8 (HB).
14	DCOM	Digital common.
15	V_{OUT} (B)	Voltage output for DAC B.
16	ACOM (B)	Analog common for DAC B.
17	SJ (B)	Summing junction of the internal op amp for DAC B.
18	GA (B)	Gain adjust pin for DAC B.
19	$\overline{WR}$ (B)	Write control line for DAC B.
20	$\overline{CS}$ (B)	Chip select control line for DAC B.
21	$+V_{CC}$	Positive supply voltage (+15V).
22	$-V_{CC}$	Negative supply voltage (−15V).
23	$\overline{CS}$ (A)	Chip select control line for DAC A.
24	$\overline{WR}$ (A)	Write control line for DAC A.
25	V_{OUT} (A)	Voltage output for DAC A.
26	ACOM (A)	Analog common for DAC A.
27	SJ (A)	Summing junction of the internal op amp for DAC A.
28	GA (A)	Gain adjust pin for DAC A.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V, +15V
$+V_{CC}$ to COMMON	0V, +18V
$-V_{CC}$ to COMMON	0V, −18V
Digital Data Inputs to COMMON	−0.5V, V_{DD} + 0.5
DC Current any Input	±10mA
Reference Out to COMMON	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
External Voltage Applied to R_F	±18V
External Voltage Applied to D/A Output	±5V
Power Dissipation	2000mW
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC725JP	28-Pin Plastic DIP	215
DAC725KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
DAC725JP	±0.012	0°C to +70°C
DAC725KP	±0.006	0°C to +70°C

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC725 accepts positive-true binary twos complement input code, as shown in Table I. The data is loaded into either DAC, 8 bits at a time. The data may also be clocked into the device in a serial format.

DIGITAL INPUT CODES	ANALOG OUTPUT (Binary Two's Complement, Bipolar Operation, All Models)
7FFF$_H$	+ Full Scale
0000$_H$	Zero
FFFF$_H$	– 1LSB
8000$_H$	– Full Scale

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (minus full-scale point and plus full-scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of –1LSB maximum (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC725 is specified to be monotonic to 14 bits over the entire specification range.

DRIFT

Gain Drift

Gain drift is a measure of the change in full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by:

(1) testing the end point differences at t_{MIN}, +25°C and t_{MAX},

(2) calculating the gain error with respect to the +25°C value, and

(3) dividing by the temperature change.

The DAC725 is specified for Maximum Gain and Offset values at temperature. This tells the system designer the maximum that can be expected over temperature, regardless of room temperature values.

Zero Drift

Zero drift is a measure of change in the output with 0000$_H$ applied to the D/A converter inputs over the specified temperature range. This code corresponds to 0V analog output.

The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.
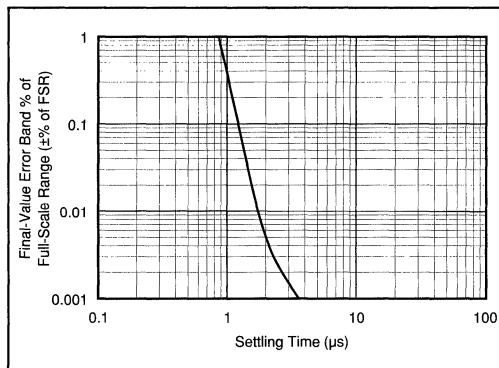
FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V), and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. This is the worst-case point since all of the input bits change when going from one code to the next.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply (+V_{CC}), negative supply (–V_{CC}) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

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FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF to 10µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001µF to 0.01µF low-leakage film capacitor should be connected from Gain Adjust to Analog Common to prevent noise pickup. Refer to Figure 4 for relationship of Offset and Gain adjustments.
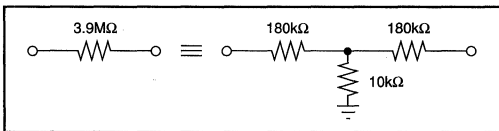
FIGURE 3. Equivalent Resistances.

Zero Adjustment

By loading the code 0000_H, the DAC will force 0V. Offset is adjusted by using the circuit of Figure 5. An alternate method would be to use the $\overline{CLR}$ control to set the DAC to 0V. Zero calibration should be made before gain calibration.

Gain Adjustment

To adjust the gain of the DAC725, set the DAC to $7FFF_H$ for both DACs. Adjust the gain of each DAC to obtain the full scale voltage of +9.99969V as shown in Table II.

DIGITAL INPUT CODE	BIPOLAR OUTPUT, ±10V			UNITS
	16 Bits	15 Bits	14 Bits	
One LSB	305	610	1224	µV
$7FFF_H$	+9.99969	+9.99939	+9.99878	V
8000_H	−10	−10	−10	V

TABLE II. Digital Input Codes.

INTERFACE LOGIC AND TIMING

The control logic functions are chip select ($\overline{CS}_A$ or $\overline{CS}_B$), write ($\overline{WR}_A$ or $\overline{WR}_B$), latch enable (A_0, A_1, A_2), and clear ($\overline{CLR}$). These pins provide the control functions for the microprocessor interface. There is a write and a chip select for both DAC_A and for DAC_B channels. This allows the 8-bit data word to be latched from the data bus to the input latch or from the input latch to the DAC latch, of DAC_A, DAC_B, or both.

A_0	A_1	A_2	$\overline{WR}$ (A)	$\overline{CS}$ (A)	DESCRIPTION
1	1	0	0	0	DAC latch enabled, Channel A
1	0	1	0	0	Input latch high byte enabled, Channel A
1	0	0	0	0	High byte flows through to DAC, Channel A
0	1	1	0	0	Low byte latched from data bus, Channel A
0	1	0	0	0	Low byte flows through to DAC, Channel A
0	0	1	1	1	Serial input mode for byte latches
X	X	X	1	0	No data is latched
X	X	X	0	1	No data is latched

"1" or "0" indicates TTL Logic Level Channel A shown.

TABLE III. Truth Table of Data Transfers.
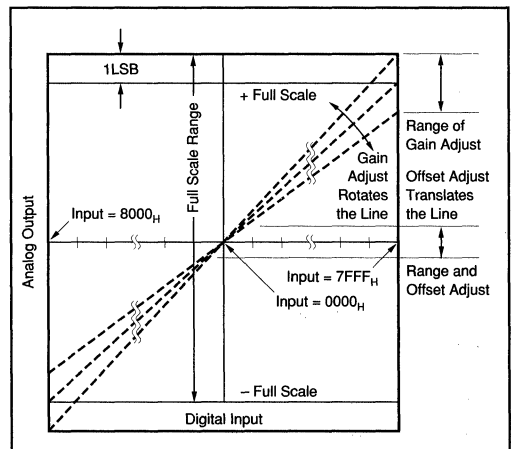
FIGURE 4. Relationship of Zero and Gain Adjustments for the DAC725.

The latch enable lines control which latch is being loaded. Line $\overline{A}_1$ in combination with $\overline{WR}$ and $\overline{CS}$ enables the high byte of the DAC channel to be latched through the byte latch. The $\overline{A}_0$ line, in conjunction with the $\overline{WR}$ and $\overline{CS}$, latches the data for the low byte. When $\overline{A}_2$, $\overline{CS}$, and $\overline{WR}$ are low at the same time, the data is latched through the D/A latch and the DAC changes output voltage. Each latch may be made transparent by maintaining its enable signal at logic "0".

The serial data mode is activated when both $\overline{A}_0$ and $\overline{A}_1$ are at logic low simultaneously. The data (MSB first) is clocked in to pin 13 with clock pulses on the $\overline{WR}$ pin. The data is then latched through to the DAC as a complete 16-bit word selected by $\overline{A}_2$.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the DAC latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the DAC.

The maximum clock rate of the latches is 10MHz. The minimum time between the write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode, the maximum rate at which data can be clocked into the input shift register is 10MHz. The timing of the control signals is given in Figure 6.

INTERVAL	DESCRIPTION	OVER TEMP.	
		ns, min	ns, max
t_{DW}	Data valid to end of $\overline{WR}$	80	
t_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
t_{AW}	$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ valid to end of $\overline{WR}$	80	
t_{WP}	Write pulse width	80	
t_{DH}	Data hold after end of $\overline{WR}$	0	
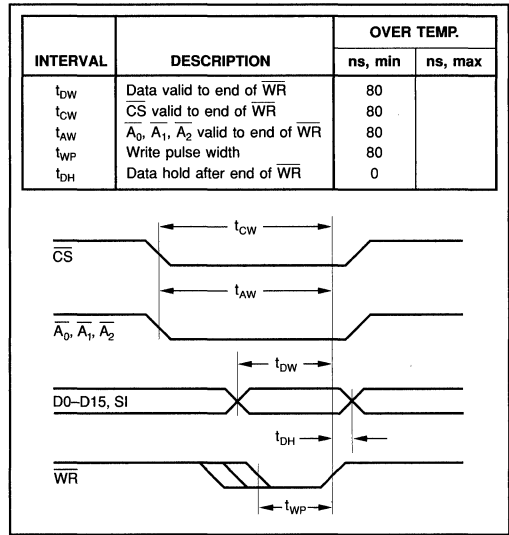
FIGURE 6. Logic Timing Diagram.
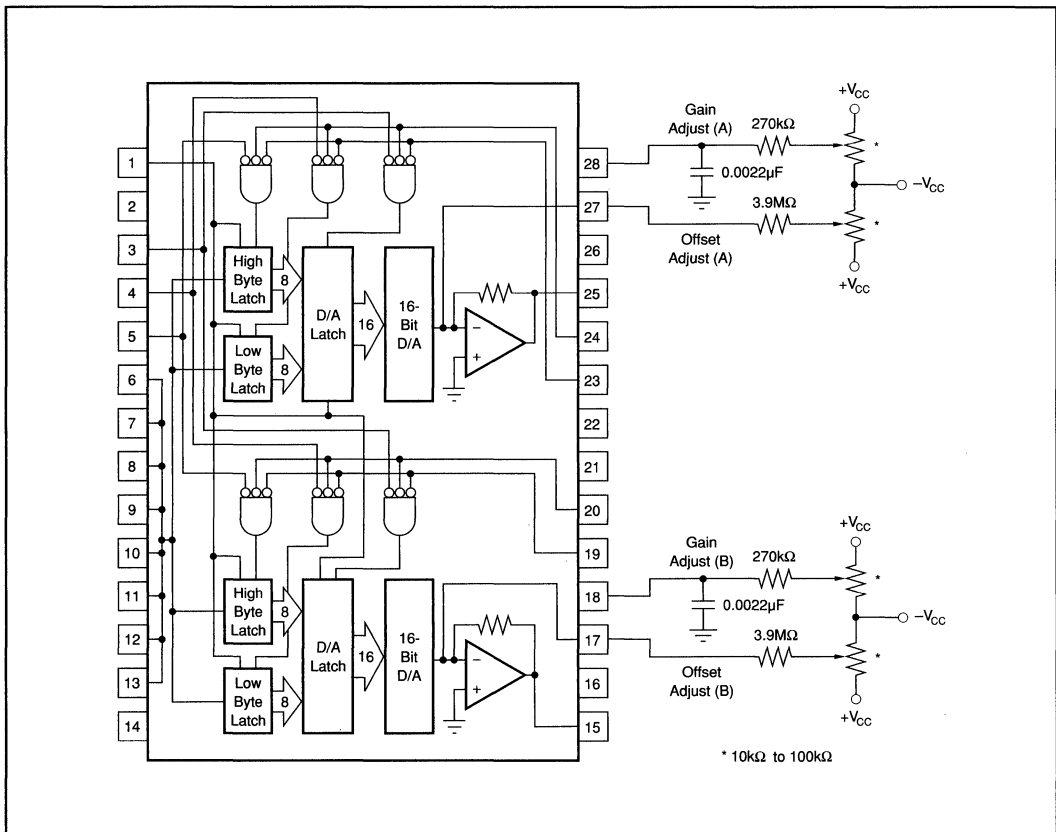
FIGURE 5. Connections for Gain and Offset Adjust.

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INSTALLATION

Because of the extremely high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1oz copper-clad printed circuit board material is approximately 1/2mΩ per square mil. In the example above, a 10mil-wide conductor 60mil long would cause a 1LSB error in R_2 and R_3 of Figure 7.

In Figure 7, lead and contact resistances are represented as R_2 through R_6. As long as the load resistance (R_L) remains constant, the resistances of R_2 and R_3 will appear as gain errors when the output is sensed across the load. If the output is sensed at the DAC725 output terminal and the system analog common, R_2 and R_3 appear in series with R_L. R_4 has a current through it that varies by only 1% of the nominal 2mA current for all code combinations. This IR drop causes an offset error, and is calibrated out as an offset error.

The current through the digital common varies directly with the digital code that is loaded into the DAC. The current is not the same for each code. If this IR drop is allowed to modulate the analog common, there may be code-dependent errors in the analog output.

The IR drop across R_6 may cause accuracy problems if the analog commons of several circuits are "daisy chained" along the power supply analog common. All analog sense lines should be referenced to the system analog common.

APPLICATIONS

WAVEFORM GENERATION

The DAC725 has attributes that make it ideal for very low distortion waveform synthesis. Due to special design techniques, the feedthrough energy is much lower than that found in other D/A converters available today. In addition to the low feedthrough glitch energy, the input logic will operate with data rates of 10MHz. This makes the DAC725 ideal for waveform synthesis.

PROGRAMMABLE POWER SUPPLIES

The DAC725 is an excellent choice for programmable power supply applications. The DAC outputs may be programmed to track or oppose each other. If the load is floating, and can be driven differentially, the dynamic range will be 17 bits, because the full-scale range doubles for the same sized LSB. The clear line ($\overline{CLR}$) sets both DAC outputs to zero, and would be used at power-up to bring the system up in a safe state. The $\overline{CLR}$ line could also be used if an over-power state is sensed.

ISOLATION

The DAC725 can accept serial input data, which means that only six optoisolators are needed for two DACs. The data is clocked into the input latch using the $\overline{WR}$ pin. The 16-bit data word is latched into the DAC selected by $\overline{A_2}$. When $\overline{A_0}$ and $\overline{A_1}$ are simultaneously low, the serial mode is enabled.
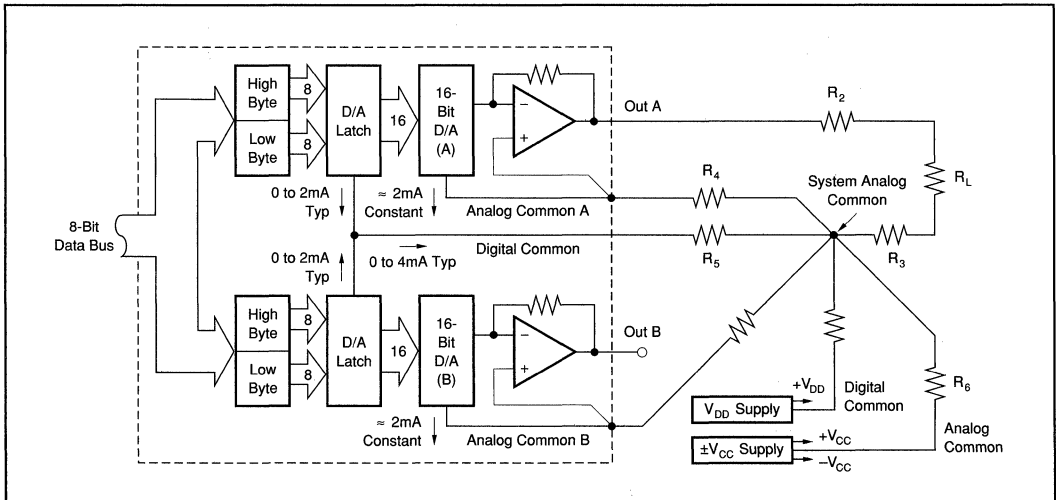
FIGURE 7. System Wiring Example.

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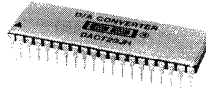
DAC729

Ultra-High Resolution
18-BIT DIGITAL-TO-ANALOG CONVERTER

DAC729

DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **16-BIT LINEARITY GUARANTEED (K Grade)**

● **USER ADJUSTABLE TO 18-BIT LINEARITY**

● **PRECISION INTERNAL REFERENCE**

● **FAST SETTLING, LOW NOISE INTERNAL OP AMP**

● **LOW DRIFT**

● **HERMETIC 40-PIN CERAMIC PACKAGE**

● **I_{OUT} OR V_{OUT} OPERATION**

DESCRIPTION

The DAC729 sets the standard in very high accuracy digital-to-analog conversion. It is supplied from the factory at a guaranteed linearity of 16 bits, and is user-adjustable to 18-bit linearity (1LSB = FSR/262144).

To attain this high level of accuracy, the design takes advantage of Burr-Brown's thin-film monolithic DAC process, dielectric op amp process, hybrid capabilities, and advanced test and laser-trim techniques.

The DAC729 hybrid layout is specifically partitioned to minimize the effects of external load-current-induced thermal errors. The op amp design consists of a fast settling precision op amp with a current buffer within the feedback loop. This buffer isolates the load from the precision op amp, which results in a fast settling (8μs to 16 bits) output. The standard 40-pin package offers full hermeticity, contributing to the excellent reliability of the DAC729.

18-Bit I_{OUT} DAC

Precision 10V Reference

Servo-Loop Amplifier

5kΩ · 5kΩ · 5kΩ · 5kΩ

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $V_{CC} = ±15V$, $V_{DD} = +5V$, using internal reference op amp, unless otherwise noted. COB = ±10V FSR, CSB = 0V to +10V FSR.

PARAMETER	DAC729JH MIN	DAC729JH TYP	DAC729JH MAX	DAC729KH MIN	DAC729KH TYP	DAC729KH MAX	UNITS
DIGITAL INPUT							
Resolution		18			*		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH}, $V_{IN} = +2.7V$			+5			*	µA
I_{IL}, $V_{IN} = +0.4V$			−300			*	µA
TRANSFER CHARACTERISTICS[2]							
ACCURACY							
Linearity Error[3]			±0.0015			±0.00076	% of FSR[4]
Differential Linearity Error			±0.003			±0.0015	% of FSR
Gain Error[5]		±0.05	±0.10		*	*	%
Offset Error:[5]Voltage, COB[6]		±5	±10		*	*	mV
CSB[6]		±3	±5	*		*	mV
Current, COB			±5			*	µA
CSB			±1			*	µA
Power Supply Sensitivity, Unipolar: ±15VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Bipolar Offset: ±15VDC		±0.0004	±0.0015		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Bipolar Gain: ±15VDC		±0.0005	±0.0015		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Output Noise (10Hz to 100kHz), Voltage: Bipolar Offset		29			*		µVrms
Bipolar Gain		37			*		µVrms
Current: Bipolar Offset		2.9			*		nArms
Bipolar Gain		3			*		nArms
Monotonicity (0°C to +70°C)	15	16		16	17		Bits
Differential Linearity Adjustment Resolution[7]		18			*		Bits
DRIFT (Over Specification Temperature Range)							
Gain Drift (Excluding Reference Drift)		±3	±5		*	*	ppm/°C
Offset Drift (Excluding Reference Drift): COB (Bipolar)		±2	±5		*	*	ppm of FSR/°C
CSB (Unipolar)		±2	±3		*	*	ppm of FSR/°C
Linearity Error (at 0°C and +70°C)		±0.3	±1		±0.3	±0.5	ppm of FSR/°C
Differential Linearity Error (at 0°C and +70°C)		±0.5	±2		±0.5	±1	ppm of FSR/°C
STABILITY, LONG TERM (at +25°C)							
Gain (Exclusive of Reference)		±5			±5		ppm/1000hr
Offset: COB (Exclusive of Reference)		±5			±5		ppm of FSR/1000hr
CSB		±5			±5		ppm of FSR/1000hr
Linearity		±2			±2		ppm of FSR/1000hr
Reference		±5			±5		ppm/1000hr
OUTPUT							
VOLTAGE OUTPUT MODE							
Ranges: COB		±2.5, ±5, ±10			*		V
CSB		0 to +10, 0 to +5			*		V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
CURRENT OUTPUT MODE							
COB Ranges		±1			*		mA
Output Impedance		2.86			*		kΩ
CSB Ranges		0 to −2			*		mA
Output Impedance		4.0			*		kΩ
Output Current Tolerance			±0.1			*	% of FSR
Compliance Voltage		−1 to +5			*		V
SETTLING TIME (To ±0.00076% of FSR)[8]							
Voltage (Load = 2kΩ ‖ 100pF): Full-Scale Step		5	8		*	*	µs
1LSB Step (Major Carry)[9]		4	7		*	*	µs
Slew Rate		20			*		V/µs
Switching Transient Peak		500			*		mV
Switching Transient Energy		0.45			*		V-µs
Current Full-Scale Step (2mA X 10Ω ‖ 1pF)		300			*		ns

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, using internal reference op amp, unless otherwise noted. COB = ±10V FSR, CSB = 0V to +10V FSR.

PARAMETER	DAC729JH			DAC729KH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE							
Output (pin 32) :Voltage	+9.990	+10.000	+10.010	*	*	*	V
Source Current[10]			+4			*	mA
Temperature Coefficient		±2	±4		*		ppm/°C
Short-Circuit Duration	Indefinite to Common			Indefinite to Common			
Power Supply Sensitivity		0.00025	0.003		*	*	%/V
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$	−16.5	−15	−13.5	*	*	*	V
V_{DD}	+4.75	+5	+5.25	*	*	*	V
Current: $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−45	−60		*	*	mA
V_{DD}		+18	+25		*	*	mA
Power Dissipation (Rated Supplies)		1.22	1.63		*	*	W
ENVIRONMENTAL SPECIFICATIONS							
Temperature Range: Specification	0		+70	*		*	°C
Storage	−60		+150	*		*	°C

* Specifications same as DAC729JH.

NOTES: (1) TTL- and CMOS-compatible. (2) Specified for V_{OUT} mode using the internal op amp. (3) ±0.00076% of full-scale range is 1/2LSB for 16-bit resolution. (4) FSR means full-scale range, 20V for ±10V range, etc. (5) Adjustable to zero error with an external potentiometer. (6) COB is complementary offset binary (bipolar); CSB is complementary straight binary (unipolar). (7) Using the MSB adjustment circuit, the user may improve the DAC linearity to 1/2LSB of this specification with gain and offset errors adjusted to zero at 25°C. (8) Maximum represents 3σ limit, not 100% production tested. (9) At the major carry; 20000 to 1FFFF$_{HEX}$ and from 1FFFF to 20000$_{HEX}$. (10) Maximum with no degradation in specifications. External loads must be constant.

PIN CONNECTIONS

Top View			DIP
(MSB) Bit 1	1	40	V_{POT}
Bit 2	2	39	Bit 1 Adjust
Bit 3	3	38	Bit 2 Adjust
Bit 4	4	37	Bit 3 Adjust
Bit 5	5	36	Bit 4 Adjust
Bit 6	6	35	Reference Adjust
Bit 7	7	34	Gain Adjust
Bit 8	8	33	Reference Common
Bit 9	9	32	Reference Out
Bit 10	10	31	Reference In
Bit 11	11	30	Analog Common
Bit 12	12	29	I_{OUT}
Bit 13	13	28	5kΩ Feedback
Bit 14	14	27	5kΩ Feedback
Bit 15	15	26	10kΩ Feedback
Bit 16	16	25	10kΩ Feedback
Bit 17	17	24	Summing Junction
(LSB) Bit 18	18	23	V_{OUT}
V_{DD} (5V)	19	22	$+V_{CC}$ (15V)
Digital Common	20	21	$-V_{CC}$ (15V)

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to Common .... 0V to +7V
$+V_{CC}$ to Common .... 0V to +18V
$-V_{CC}$ to Common .... 0V to −18V
Digital Data Inputs (pins 1-18) to Common .... −0.5V to V_{DD}
Reference Voltage In (pin 31) .... +9V to +11V
Reference Out (pin 32) to Common .... Indefinite Short to Common
External Voltage Applied to D/A Output (pin 29) .... −5V to +5V
External Voltage Applied to Feedback Resistors
 (pins 25, 26, 27, 28) .... −15V to +15V
V_{OUT} (pin 23) .... Indefinite Short to Common
Power Dissipation 3000mW
Storage Temperature .... −60°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
DAC729JH	40-Pin Hermetic DIP	0°C to +70°C
DAC729KH	40-Pin Hermetic DIP	0°C to +70°C
DAC729KH-BI	40-Pin Hermetic DIP	0°C to +70°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC729JH	40-Pin Hermetic DIP	214
DAC729KH	40-Pin Hermetic DIP	214
DAC729KH-BI	40-Pin Hermetic DIP	214

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURN-IN SCREENING

Burn-in screening is an option available for the DAC729 family of products. Burn-in duration is 160 hours at 100°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met.

THEORY OF OPERATION

The DAC729 is an 18-bit digital-to-analog converter system, including a precision reference, low noise, fast settling operational amplifier, and an 18-bit current source/DAC chip contained in a hermetic 40-pin ceramic dual-in-line package. Refer to Figure 11 for a schematic diagram of the DAC729.

THE INTERNAL REFERENCE

The reference consists of a very low temperature coefficient closed-loop reference zener circuit that has been temperature-drift-compensated by laser-trimming a zener current to achieve less than 1ppm/°C temperature drift of V_{REF}.

By strapping pin 32 (Reference Out) to pin 31 (Reference In), the DAC will be properly biased from the internal reference. The internal reference may be fine adjusted using pin 35 as shown in Figure 7. The reference has an output buffer that will supply 4mA for use external to the DAC729. This load must remain constant because changing load on the reference may change the reference current to the DAC.

In systems where several components need to track the same system reference, the DAC729 may be used with an external 10V reference, however, the internal reference has lower noise (6µVp-p) and better stability than other references available.

THE OPERATIONAL AMPLIFIER

To support a DAC of this accuracy, the operational amplifier must have a maximum gain-induced error of less than 1/3LSB, independent of output swing (the op amp must be linear!) To support 15 bits (1/2-bit linearity), the op amp must have a gain of 130,000V/V. For 18 bits, the minimum

gain is well over 500,000V/V. Since thermal feedback is the major limitation of gain for mono op amps, the amplifier was designed as a high gain, fast settling mono op amp, followed by a monolithic, unity-gain current buffer to isolate the thermal effects of external loads from the input stage gain transistors. The op amp and buffer are separated from the DAC chip, minimizing thermally-induced linearity errors in the DAC circuit. The op amp, like the reference, is not dedicated to the DAC729. The user may want to add a network, or select a different amplifier. The DAC729 internal op amp is intended to be the best choice for accuracy, settling time, and noise.

THE DAC CHIP

The heart of the DAC729 is a monolithic current source and switch integrated circuit. The absolute linearity, differential linearity, and the temperature performance of the DAC729 are the result of the design, which utilizes the excellent element matching of the current sources and switch transistors to each other, and the tracking of the current setting resistors to the feed back resistors. Older discrete designs cannot achieve the performance of this monolithic DAC design.

The two most significant bits are binarily weighted interdigitated current sources. The currents for bits 3 through 18 are scaled with both current source weighting and an R-2R ladder. The circuit design is optimized for low noise and low superposition error, with the current sources arranged to minimize both code-dependent thermal errors and IR drop errors. As a result, the superposition errors are typically less than 20µV.

The DAC chip is biased from a servo amplifier feeding into the base line of the current sources. This servo amplifier sets the collector current to be mirrored and scaled in the DAC chip current sources, as shown in Figure 11. The reference current for the servo is established by the reference voltage applied to pin 31 feeding an internal resistor (20kΩ) to the virtual ground of the servo amplifier.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC729 accepts complementary digital input codes in either binary format (CSB for Unipolar or COB for Bipolar; see Table I).

DIGITAL INPUT	DAC ANALOG OUTPUT			
	COB	20V FSR	CSB	10V FSR
00 0000 0000 0000 0000	+ Full Scale	9.999924V	+ Full Scale	9.999962V
11 1111 1111 1111 1111	– Full Scale	–10V	– Full Scale	0V

TABLE I. Digital Input Coding.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2 LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than –1LSB (–0.0015% for 16-bit resolution) insures monotonicity to 16 bits.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC729KH is specified to be monotonic to 16 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is measured by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C, and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $3FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full-scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Settling time includes the slew time of the op amp.

Voltage Output

Settling times are specified to ±0.00076% of FSR scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.00076% of FSR for a full-scale range change with an output load resistance of 10Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to the current output mode of operation. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified linearity.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter full-scale output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$), or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 1). It is specified for DC or low frequency changes. The typical performance curve in Figure 1 shows the effect of high frequency changes in power supply voltages using internal reference, DAC, and op amp.
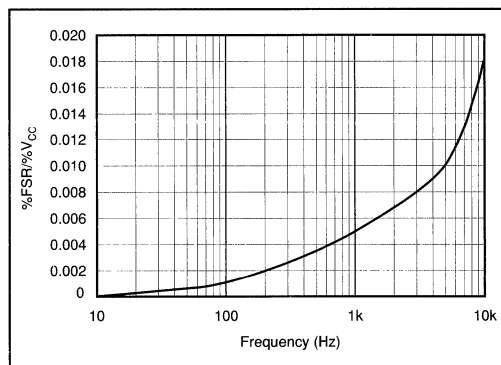
FIGURE 1. Power Supply Sensitivity vs Frequency Using Internal Reference and Op Amp.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in Figure 2. These capacitors (1µF to 10µF tantalum recommended) should be located at the DAC729.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC729 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001µF to 0.01µF capacitor should be connected from Gain Adjust (pin 34) to

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common to shunt noise pickup. This capacitor should be a low leakage film type (such as Mylar™ or Teflon™).

Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. See Table II for corresponding codes and Figures 2 and 3 for offset adjustment connections. Offset adjust should be made prior to gain adjust.

Mylar™, Teflon™ E.I. du Pont de Nemours & Co.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and Figure 3 for gain adjustment connections.

OUTPUT RANGE	CODE	CONNECT PIN 23	CONNECT PIN 31	CONNECT PIN 24	GAIN ADJUST 16-BITS	GAIN ADJUST 18-BITS
±10V	COB	to Pin 25	to Pin 26	to Pin 29	9.9969V	9.99992V
±5V	COB	to Pin 27	to Pin 26	to Pin 29	4.9998V	9.99996V
±2.5V	COB	to Pin 27	to Pin 26	to Pins 29 & 25	2.4992V	2.49998V
0 to 10V	CSB	to Pins 25 & 26	N/C	to Pin 29	9.9998V	9.99996V
0 to 5V	CSB	to Pins 27 & 28	N/C	to Pin 29	4.9999V	4.99998V

TABLE II. Output Range Connections and Gain Adjust Voltage.
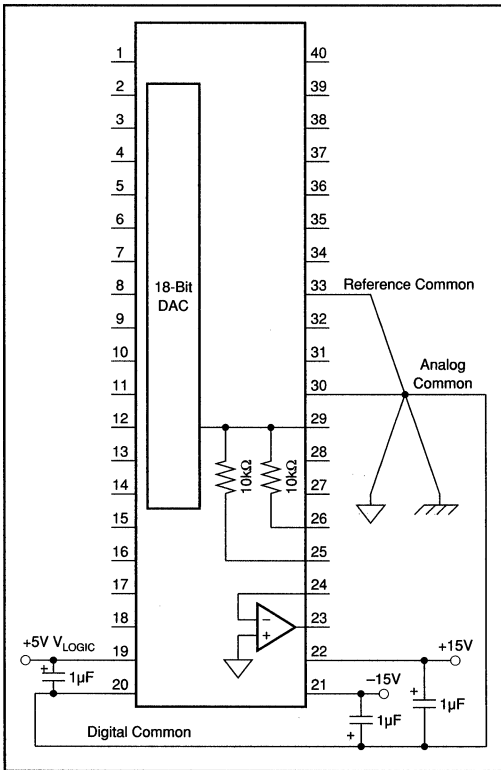
FIGURE 2. Ground Connections and Supply Bypass.

NOTE: (1) Mylar™ or Teflon™ Film.
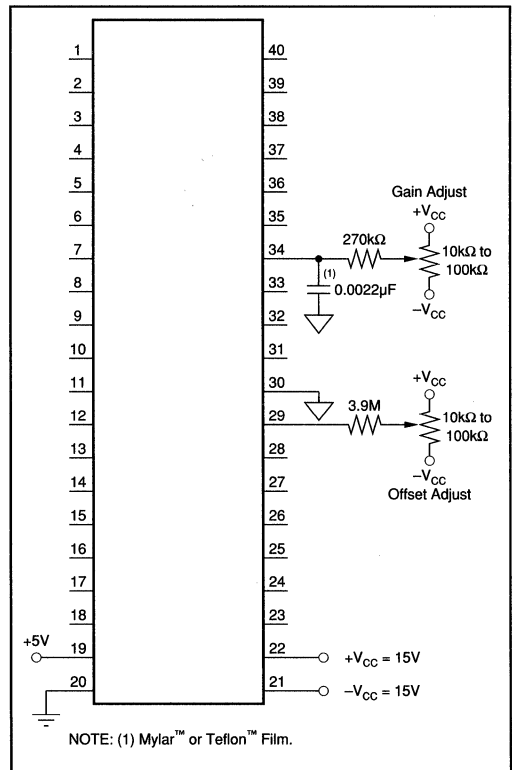
FIGURE 3. Gain and Offset Adjust Hook-Up.
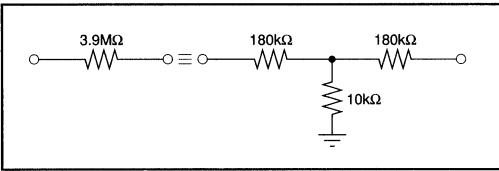
FIGURE 4. Equivalent Resistances.
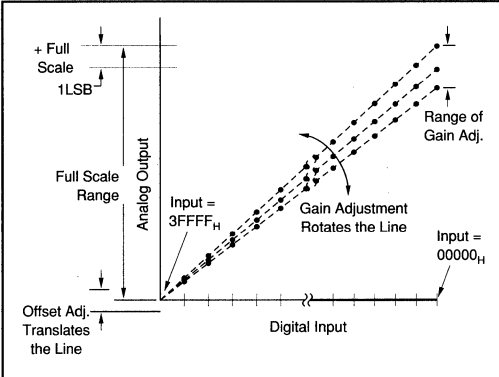
FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.
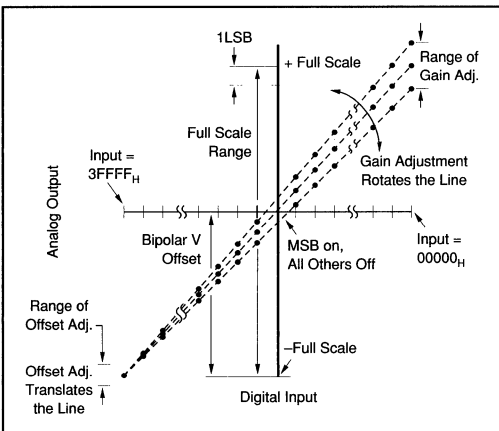
FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

REFERENCE ADJUSTMENT

The internal reference may be fine adjusted using pin 35 as shown in Figure 7. Adjusting the reference has a similar effect on the DAC as gain adjust, except the transfer characteristic rotates around bipolar zero for a bipolar connection as shown in Figure 8.

LAYOUT/APPLICATIONS SUGGESTIONS

Obviously, the management of IR drops, power supply noise, thermal stability, and environmental noise becomes much more critical as the accuracy of the system increases. The DAC729 has been designed to minimize these applications problems to a large degree. The basics of "Kelvin sensing" and "holy point" grounding will be the most important considerations in optimizing the absolute accuracy of the system. Figure 9 shows the proper connection of the DAC with the holy-point ground and the Kelvin-sensed-output connection at the load.

The DAC729 has three separate supply common (ground) pins. Reference common (pin 33) carries the return current from the internal reference and the output I/V converter common. The current in pin 33 is stable and independent of code or load. Digital common (pin 20) carries the variable currents of the biasing circuits. Analog common (pin 30) is the termination of the R-2R ladder and also carries the "waste current" from the off side of the current switches. These three ground pins must be star connected to system ground for the DAC to bias properly and accurately. Good ground connections are essential, because an IR drop of just 39μV completely swamps out a 10V FSR 18-bit LSB.

When the application is such that the DAC must control loads of greater than ±5mA with rated accuracy, it is recommended that an external op amp or op amp buffer combination be used to dissipate the variable power external to the DAC729. This minimizes the temperature variations on the precision D/A converter. Figure 10 illustrates a method of connecting the external amplifier for ±10V operation, while using an external reference.

When driving loads to greater than ±10V, care must be taken that the internal resistors are never exposed to greater than ±10V, and that the summing junction is clamped to insure that the voltage never exceeds ±5V. Clamping the summing junction with diodes (parallel opposing connection) to ground will give the best transient response and settling times.

TRUE 18-BIT PERFORMANCE
(Differential Linearity Adjustment)

To take full advantage of the DAC729's accuracy, the four MSBs have adjustment capabilities. A simplified schematic (Figure 11) shows the internal structure of the DAC current source and the adjustment input terminal. The suggested network for adjusting the linearity is shown in Figure 12. This circuit has nearly twice the range that is required for the DAC729JH. The range is intentionally narrow so as to minimize the effect of temperature drift or stability problems in the potentiometers. The potentiometers are biased in an identical fashion to the internal DAC current sources to minimize power supply sensitivity and drift over temperature. Low leakage capacitors such as Mylar or Teflon film are essential.

The linearity adjustment requires a digital voltmeter with 7 digits of resolution on the 10V range (1μV resolution) and excellent linearity. For the DAC, 1LSB of the 0V to 10V scale (10 FSR) is 38μV. To be 1/2LSB linear, the measurement must resolve 19μV. The meter must be properly calibrated and linear to 1ppm of range.

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DIGITAL-TO-ANALOG CONVERTERS
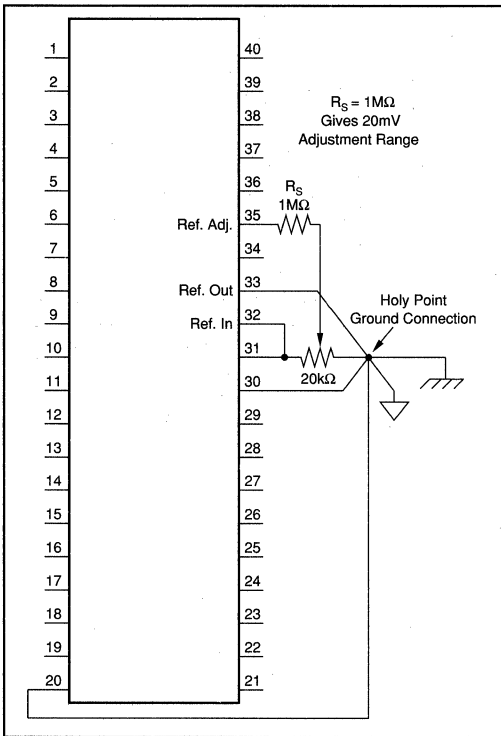
FIGURE 7. V_{REF} Adjust.

FIGURE 8. Effect of V_{REF} Adjust on a COB Connected DAC729.

FIGURE 9. Typical Hook-Up Diagram with "Holy Point" Ground and Kelvin Sense Load, Using Internal Op Amp and Reference.

With the DAC connected for 0 to 10V output (Figure 13), the adjustment procedure is to set the DAC code and measure as follows:

FOURTH MSB ADJUSTMENT (Pin 36)

1. Set Code = 11 1100 0000 0000 0000

2. Measure V_{OUT}

3. Set Code = 11 1011 1111 1111 1111

4. Measure V_{OUT} and record the difference.

5. Adjust 4th MSB potentiometer to make difference +38μV.

6. Repeat steps 1 through 5 to confirm.

THIRD MSB ADJUSTMENT (Pin 37)

1. Set Code = 11 1000 0000 0000 0000

2. Measure V_{OUT}

3. Set Code = 11 0111 1111 1111 1111

4. Measure V_{OUT} and record the difference.

5. Adjust 3rd MSB potentiometer to make difference +38μV.

6. Repeat steps 1 through 5 to confirm.
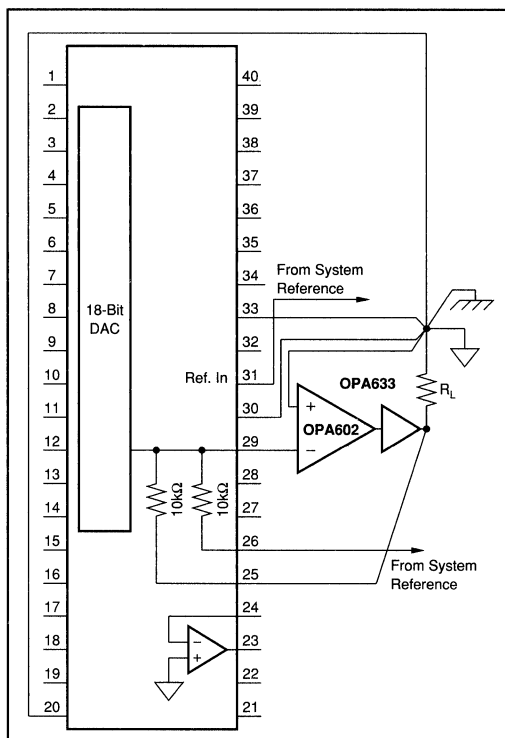
FIGURE 10. Using an External Op Amp with Buffer and External Reference for ±10V Output.

SECOND MSB ADJUSTMENT (Pin 38)

1. Set Code = 11 0000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 10 1111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 2nd MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

MSB ADJUSTMENT (Pin 39)

1. Set Code = 10 0000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 01 1111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust the MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

APPLICATIONS

The DAC729 is the DAC of choice for applications requiring very high resolution, accuracy, and wide dynamic range.

DIGITAL AUDIO

The excellent linearity and differential linearity are ideal for PCM professional audio and waveform generation applications.

DAC729

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DIGITAL-TO-ANALOG CONVERTERS
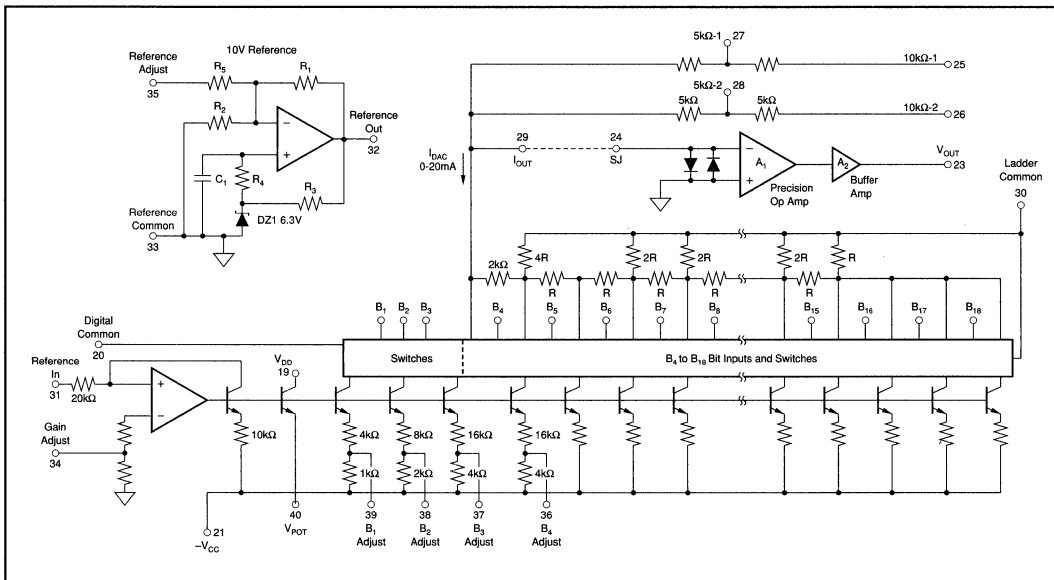
FIGURE 11. DAC729 Simplified Schematic.
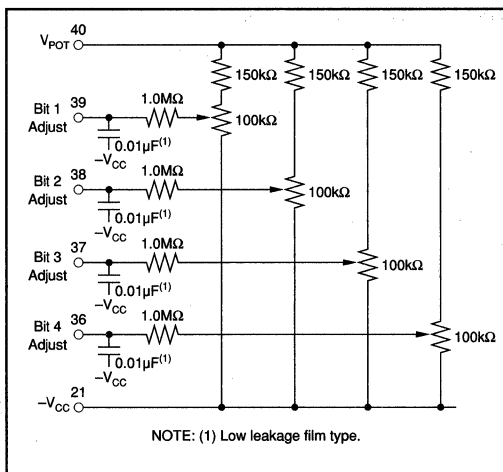
FIGURE 12. Differential Linearity Adjustment Circuit for the 4MSBs.

The DAC729 offers superb dynamic range. Dynamic range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range, usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6dB per bit. For the DAC729 the theoretical range is 108dB! The actual dynamic range is limited by noise (signal-to-noise) and linearity errors. The DAC729's 6µV typical noise floor, fast settling op amp, and adjustable 18-bit linearity minimize the limitation.

Total harmonic distortion (THD) is the measure of the magnitude and distribution of the linearity error, differential linearity error, noise, and quantization error. The THD is defined as the ratio of the square root of the sum of the squares of the harmonics to the values of the input fundamental frequency. The rms value of a DAC error can be shown to be

$$\varepsilon_{RMS} = \sqrt{\frac{1}{n} \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2}$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the DAC729 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\varepsilon_{RMS}}{E_{RMS}} = \frac{\sqrt{\frac{1}{n} \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2}}{E_{RMS}} \quad X \times 100\% \quad (2)$$

where E rms is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.
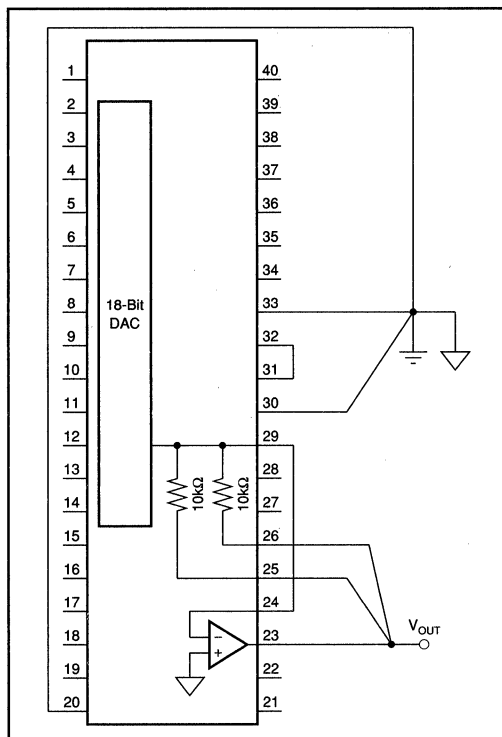
FIGURE 13. 0 to 10V FSR.

The DAC729 has demonstrated THD of 0.0009% at full scale (at 1kHz). This is the level of distortion that is desired to test other professional audio products, making the DAC729 ideal for professional audio test equipment.

The ability to adjust the linearity of the 4MSBs, the 18-bit resolution, fast settling and low noise give the DAC729 unmatched performance.

AUTOMATIC TEST EQUIPMENT

The pin functions of the DAC729 are convenient for use in automatic test equipment systems. The ability to use internal or external reference and internal or external op amp means versatility for the system designer. For example, in automatic test systems with several DACs and ADCs, it is desirable to operate all of the high accuracy converters from the same reference, improving the tracking characteristics of those components to one another. The reference in the DAC729 is a very stable precision reference, and is suitable for use as the system reference.

Test systems, and other large systems are the ideal application for a DAC of this accuracy, because the DAC will be calibrated in the environment in which it will be used. Since the environment is very stable, the manual calibration (Figure 12) may be adequate. However, highly automated systems will go to an automatic calibration routine. Replacing

the potentiometers in Figure 12 with V_{OUT} DACs, and using sample and difference measurements, the major carry bit weights can be measured, and external DACs used to adjust the differential linearity of the DAC729. A successive approximation routine yields the fastest calibration. The output voltage of the external DACs will have to be level shifted, as the bit adjustment potentiometer must be able to achieve $-V_{CC}$ to give the full adjust range.

Because the DAC729 feedback resistors have a tolerance of ±0.1%, the output range can be rescaled slightly with small-value fixed external resistors to give convenient ranges. A popular range is 0V to +10.24V which gives even 5mV steps at 11 bits. In this case, the LSB size is 39.06µV. Figure 14 shows how to connect two 240Ω resistors in series with the internal 10kΩ resistors to give a 0V to 10.24V full-scale range. Another convenient range might be 0V to +10.48576V which gives an even 40µV LSB step size.

THE HEART OF AN 18-BIT ADC

The DAC729 makes a good building block in ADC applications. The key to ADC accuracy is differential linearity of the DAC. The ability to adjust to 18-bit linearity, coupled with the fast settling time of the DAC729 makes the design cycle for an 18-bit successive approximation ADC much faster, and the production more consistent. Figure 15 shows the DAC as the heart of a successive approximation ADC. The clock and successive approximation register could be implemented in 7400 series TTL, as a simple gate-array or standard cell, or part of a local processor.

With the DAC out of the way, the comparator is the toughest part of the ADC design. To resolve an 18-bit LSB, and interface to a TTL-logic device, the comparator must have a gain of 500kV/V (5X actual) as well as low hysteresis, low noise, and low thermally induced offsets. With this much gain, a slow comparator may be desired to reduce the risk of instability.

The feedback resistors of the DAC are the input scaling resistors of the ADC. An OPA602 and an OPA633 make an excellent buffer for the input signal, giving a very high input impedance to the signal (minimizing IR drop) while maintaining the linearity.
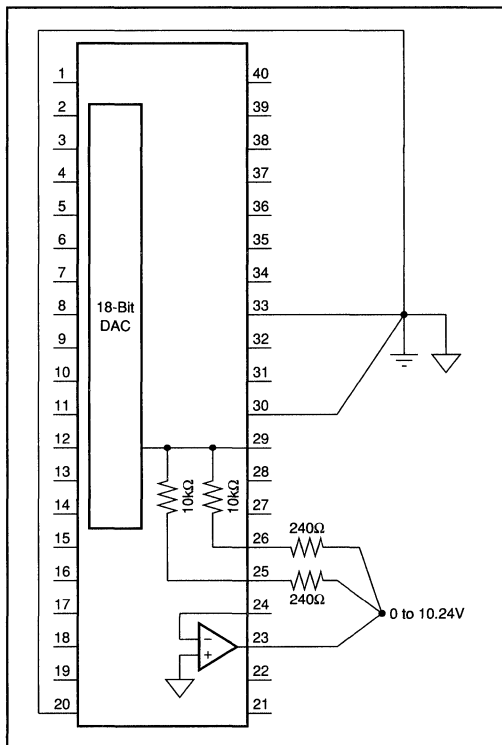
FIGURE 14. 0V to 10.24V Using Internal Op Amp and Internal Reference.
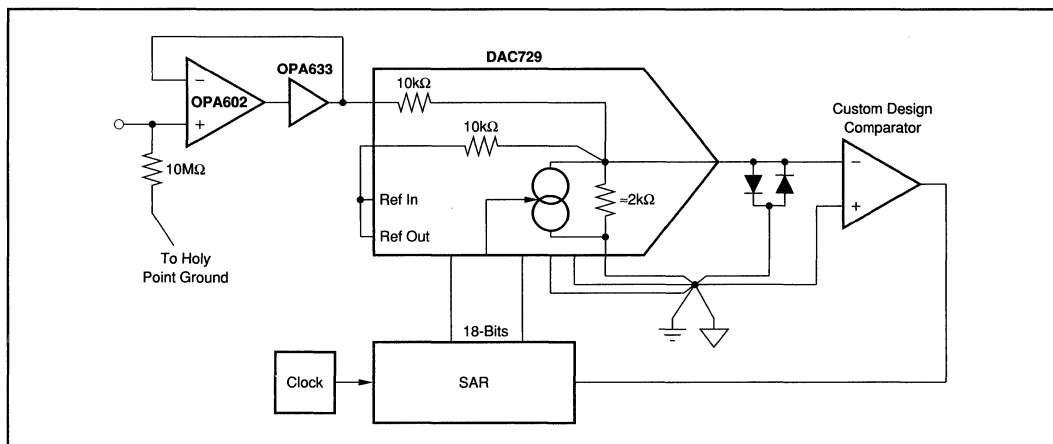
FIGURE 15. Block Diagram of an 18-Bit Resolution ±10V_{IN} ADC.

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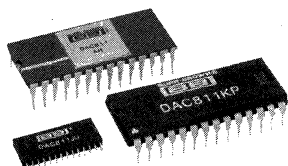
DAC811

Microprocessor-Compatible
12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **SINGLE INTEGRATED CIRCUIT CHIP**
● **MICROCOMPUTER INTERFACE:**
   DOUBLE-BUFFERED LATCH
● **VOLTAGE OUTPUT: ±10V, ±5V, +10V**
● **MONOTONICITY GUARANTEED OVER**
   TEMPERATURE
● **±1/2LSB MAXIMUM NONLINEARITY OVER**
   TEMPERATURE
● **GUARANTEED SPECIFICATIONS AT ±12V**
   AND ±15V SUPPLIES
● **TTL/5V CMOS-COMPATIBLE LOGIC**
   INPUTS

DESCRIPTION

The DAC811 is a complete, single-chip integrated-circuit, microprocessor-compatible, 12-bit digital-to-analog converter. The chip combines a precision voltage reference, microcomputer interface logic, and double-buffered latch, in a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nibbles to permit interfacing to 4-, 8-, 12-, or 16-bit buses and to handle right-or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nibble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B, K, and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in six performance grades and three package types. DAC811J and K are specified over the temperature ranges of 0°C to +70°C; DAC811A and B are specified over –25°C to +85°C; DAC811R and S are specified over –55°C to +125°C. DAC811J and K are packaged in a reliable 28-pin plastic DIP or plastic SOIC package, while DAC811A, B, R and S are available in a 28-pin 0.6" wide dual-inline hermetically sealed ceramic side-brazed package (H package).

PDS-503H

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C. $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

PARAMETER	DAC811AH, JP, JU, D MIN	TYP	MAX	DAC811BH, KP, KU MIN	TYP	MAX	DAC811RH MIN	TYP	MAX	DAC811SH MIN	TYP	MAX	UNITS
DIGITAL INPUT													
Resolution			12			*			*			*	Bits
Codes[1]		USB, BOB			*			*			*		
Digital Inputs Over Temperature Range[2]													
V_{IH}	+2		+15	*		*	*		*	*		*	VDC
V_{IL}	0		+0.8	*		*	*		*	*		*	VDC
I_{IH}, V_I = +2.7V			+10			*			*			*	µA
I_{IL}, V_I = +0.4V			±20			*			*			*	µA
Digital Interface Timing Over Temperature Range													
t_{WP}, $\overline{WR}$ Pulse Width	50			*			*			*			ns
$t_{AW}1$, N_X and $\overline{LDAC}$ Valid to End of $\overline{WR}$	50			*			*			*			ns
t_{DW}, Data Valid to End of $\overline{WR}$	80			*			*			*			ns
t_{DH}, Data Valid Hold Time	0			*			+10			*			ns
ACCURACY													
Linearity Error		±1/4	±1/2	±1/8	±1/4		±1/4	±1/2		±1/8	±1/4		LSB
Differential Linearity Error		±1/2	±3/4	±1/4	±1/2		±1/2	±3/4		±1/4	±1/2		LSB
Gain Error[3]		±0.1	±0.2	*	*		*	*		*	*		%
Offset Error[3, 4]		±0.05	±0.15	*	*		*	*		*	*		% of FSR[5]
Monotonicity		Guaranteed		*			*			*			
Power Supply Sensitivity: +V_{CC}		±0.001	±0.003	*	*		*	*		*	*		% of FSR/%V_{CC}
−V_{CC}		±0.002	±0.006	*	*		*	*		*	*		% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015	*	*		*	*		*	*		% of FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)													
Gain		±10	±30	±10	±20		±15	±30		±15	±30		ppm/°C
Unipolar Offset		±5	±10	±5	±7		±5	±10		±5	±7		ppm of FSR/°C
Bipolar Zero		±5	±10	±5	±7		±5	±10		±5	±7		ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4	±1/4	±1/2		±1/2	±3/4		±1/4	±1/2		LSB
Monotonicity Over Temperature Range		Guaranteed		*			*			*			
SETTLING TIME[6] (to within ±0.01% of FSR of Final Value; 2kΩ load)													
For Full Scale Range Change, 20V Range		3	4	*	*		*	*		*	*		µs
10V Range		3	4	*	*		*	*		*	*		µs
For 1LSB Change at Major Carry[7]		1		*			*			*			µs
Slew Rate[6]	8	12		*	*		*	*		*	*		V/µs
ANALOG OUTPUT													
Voltage Range ($\pm V_{CC}$ = 15V)[8]: Unipolar		0 to +10		*			*			*			V
Bipolar		±5, ±10		*			*			*			V
Output Current	±5			*			*			*			mA
Output Impedance (at DC)		0.2		*			*			*			Ω
Short Circuit to Common Duration		Indefinite		*			*			*			
REFERENCE VOLTAGE													
Voltage	+6.2	+6.3	+6.4	*	*	*	*	*	*	*	*	*	V
Source Current Available for External Loads	+2			*			*			*			mA
Temperature Coefficient		±10	±30	±10	±20		±10	±30		±10	±20		ppm/°C
Short Circuit to Common Duration		Indefinite		*			*			*			
POWER SUPPLY REQUIREMENTS													
Voltage: +V_{CC}	+11.4	+15	+16.5	*	*	*	*	*	*	*	*	*	VDC
−V_{CC}	−11.4	−15	−16.5	*	*	*	*	*	*	*	*	*	VDC
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	*	*	*	VDC
Current (no load): +V_{CC}		+16	+25	*	*		*	*		*	*		mA
−V_{CC}		−23	−35	*	*		*	*		*	*		mA
V_{DD}		+8	+15	*	*		*	*		*	*		mA
Potential at DCOM with Respect to ACOM[9]		±0.5		*			*			*			V
Power Dissipation		625	800	*	*		*	*		*	*		mW
TEMPERATURE RANGE													
Specification: J, K, D	0		+70	*		*	*		*	*		*	°C
A, B	−25		+85	*		*	*		*	*		*	°C
R, S	−65		+150	*		*	*		*	*		*	°C
							−55		+125	*		*	°C
Storage: J, K	−60		+100	*		*	*		*	*		*	°C
A, B, R, S	−65		+150	*		*	*		*	*		*	°C

* Specification same as model to immediate left.
NOTES: (1) USB = unipolar straight binary; BOB = bipolar offset binary. (2) TTL, LSTTL and 54/74 HC compatible. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means full scale range and is 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

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BB *Burr-Brown IC Data Book—Data Conversion Products*

DAC811

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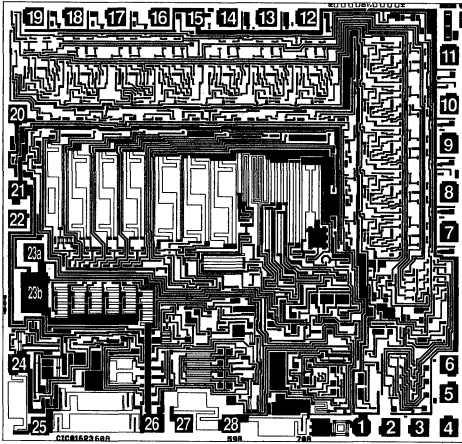
DAC811 DIE TOPOGRAPHY

MECHANICAL INFORMATION

	MILS (0.001")
Die Size	134 x 128
Min. Pad Size	4 x 4

Backside Bias: $-V_{CC}$

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	$+V_{DD}$	Logic supply, +5V.
2	$\overline{WR}$	Write, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	Load D/A converter, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	Nibble A, enables $\overline{WR}$ to load input latch A (the most significant nibble). Logic low enables.
5	$\overline{N_B}$	Nibble B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	Nibble C, enables $\overline{WR}$ to load input latch C (the least significant nibble). Logic low enables.
7	D_{11}	Data bit 12, MSB, positive true.
8	D_{10}	Data bit 11.
9	D_9	Data bit 10.
10	D_8	Data bit 9.
11	D_7	Data bit 8.
12	D_6	Data bit 7.
13	D_5	Data bit 6.
14	D_4	Data bit 5.
15	DCOM	Digital common, V_{DD} supply return.
16	D_0	Data bit 1, LSB.
17	D_1	Data bit 2.
18	D_2	Data bit 3.
19	D3	Data bit 4.
20	$+V_{CC}$	Analog supply input, +15V or +12V.
21	$-V_{CC}$	Analog supply input, −15V or −12V.
22	Gain Adj	To externally adjust gain.
23	ACOM	Analog common, $\pm V_{cc}$ supply return.
24	V_{OUT}	D/A converter voltage output.
25	10V Range	Connect to pin 24 for 10V range.
26	SJ	Summing junction of output amplifier.
27	BPO	Bipolar offset. Connect to pin 26 for bipolar operation.
28	Ref Out	6.3V reference output.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ .... 0 to +18V
$-V_{CC}$ to ACOM .... 0 to −18V
V_{DD} to DCOM .... 0 to +7V
V_{DD} to ACOM .... ±7V
ACOM to DCOM .... ±7V
Digital Inputs (Pins 2–14, 16–19) to DCOM .... −0.4V to +18V
External Voltage Applied to 10V Range Resistor .... ±12V
Ref Out .... Indefinite Short to ACOM
External Voltage Applied to DAC Output .... −5V to +5V
Power Dissipation 1000mW
Lead Temperature (soldering, 10s) .... +300°C
Max Junction Temperature .... +165°C
Thermal Resistance, $\theta_{J\text{-}A}$: Plastic DIP and SOIC .... 100°C/W
Ceramic DIP .... 65°C/W

NOTE: Stresses above those listed above may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE (°C)	LINEARITY ERROR, MAX AT +25°C	GAIN DRIFT (ppm/°C)
DAC811JP	Plastic DIP	0 to +70	±1/2LSB	30
DAC811JU	Plastic SOIC	0 to +70	±1/2LSB	30
DAC811KP	Plastic DIP	0 to +70	±1/4LSB	15
DAC811KU	Plastic SOIC	0 to +70	±1/4LSB	15
DAC811AH	Ceramic DIP	−25 to +85	±1/2LSB	30
DAC811BH	Ceramic DIP	−25 to +85	±1/4LSB	15
DAC811RH	Ceramic DIP	−55 to +125	±1/2LSB	30
DAC811SH	Ceramic DIP	−55 to +125	±1/4LSB	20

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC811AH	28-Pin Side-Brazed DIP	149
DAC811BH	28-Pin Side-Brazed DIP	149
DAC811RH	28-Pin Side-Brazed DIP	149
DAC811SH	28-Pin Side-Brazed DIP	149
DAC811JP	28-Pin Plastic DIP	215
DAC811KP	28-Pin Plastic DIP	215
DAC811JU	28-Pin SOIC	217
DAC811KU	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TIMING DIAGRAMS

Write Cycle #1
Load first rank from Data Bus: $\overline{LDAC} = 1$

Write Cycle #2
Load second rank from first rank: $\overline{N_A}, \overline{N_B}, \overline{N_C} = 1$
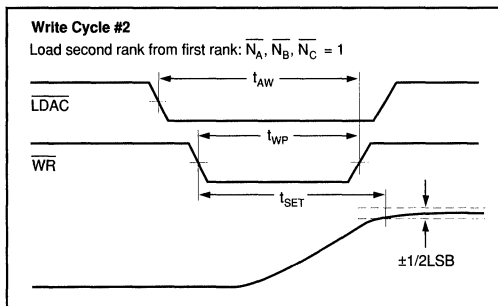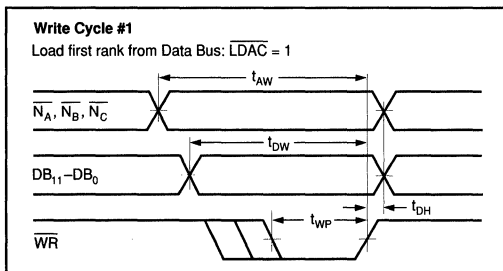
DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive-true binary input codes. DAC811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB ↓ ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111	+ Full Scale	+ Full Scale	–1LSB
100000000000	+ 1/2 Full Scale	Zero	– Full Scale
011111111111	+ 1/2 Full Scale – 1LSB	–1LSB	+ Full Scale
000000000000	Zero	– Full Scale	Zero
* Invert MSB of the BOB code with external inverter to obtain BTC code.			

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all 1s and all 0s). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A, J, and R grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC811 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full scale range value (e.g., +FS minus –FS) at high temperature, +25°C, and low temperature, calculating the error with respect to the +25°C value, and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0s on the input over the specification temperature range. Offst is measured at high temperature, +25°C, and low temperature. The offset drift is the maximum change in offset referred to the +25°C value, divided by the temperature change. It is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.1V. The reference output may be used to drive external loads, sourcing at least 2mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

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DIGITAL-TO-ANALOG CONVERTERS
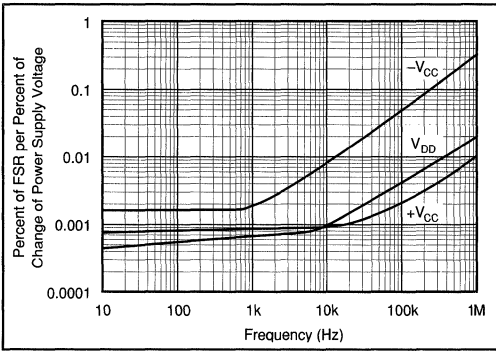
FIGURE 1. Power Supply Rejection vs Power Supply Ripple Frequency.

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$, and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic 0. When either $\overline{N_A}$, ($\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic 1, the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic 0.

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic 0. When either $\overline{LDAC}$ or $\overline{WR}$ are at logic 1, the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic 0.

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When any one of the control signals returns to logic 1, the data is latched. Table II is a truth table for all latches.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No operation
0	0	1	1	1	Enables input latch 4MSBs
0	1	0	1	1	Enables input latch 4 middle bits
0	1	1	0	1	Enables input latch 4LSBs
0	1	1	1	0	Loads D/A latch from input latches
0	0	0	0	0	Makes all latches transparent

"X" = Don't care.

TABLE II. DAC813 Interface Logic Truth Table.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output, and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.
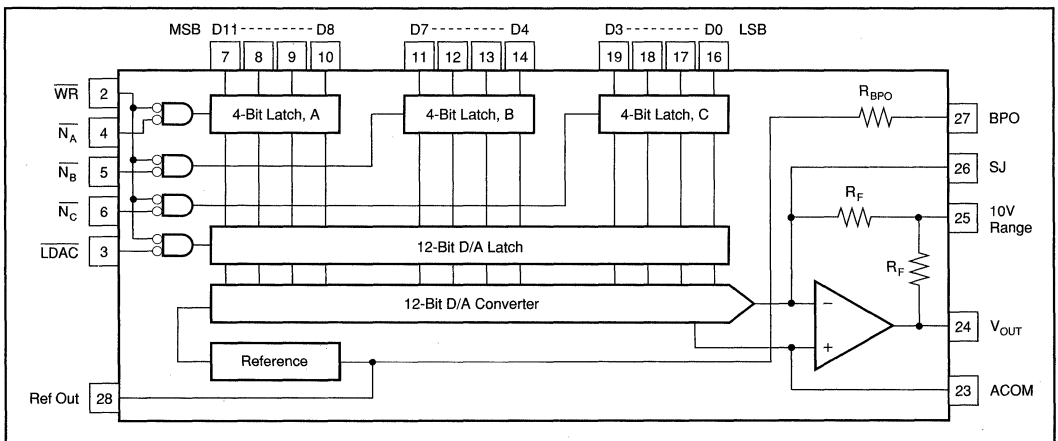
FIGURE 2. DAC811 Block Diagram.

FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT		
	0 to +10V	±5V	±10V
MSB LSB			
↓ ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5V	0V	0V
011111111111	+4.9976V	–0.0024V	–0.0049V
000000000000	0V	–5V	–10V
LSB	2.4mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12VB supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TLL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B and 54/74C CMOS devices.

Resistors of 47kΩ should be placed in series with D0 through D11, $\overline{WR}$, N_A, N_B, N_C and $\overline{LDAC}$ if edges are <10ns or if the logic input is driven below ground by undershoot.

INSTALLATION

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in Figure 5.

These capacitors (1µF tantalum recommended) should be located close to the DAC811.
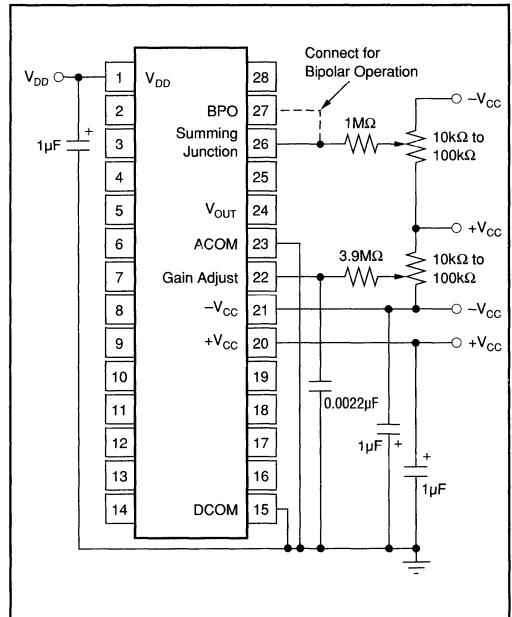
FIGURE 5. Power Supply, Gain, and Offset Potentiometer Connections.

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DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The analog common (pin 23) and digital common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiomters should be 100ppm/°C or less. The 1MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001µF to 0.01µF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment. Excessive capacitance on the Gain Adjust or Offset Adjust pin may affect slew rate and settling time.
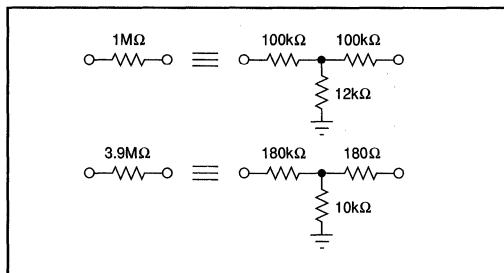
FIGURE 6. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or a unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.
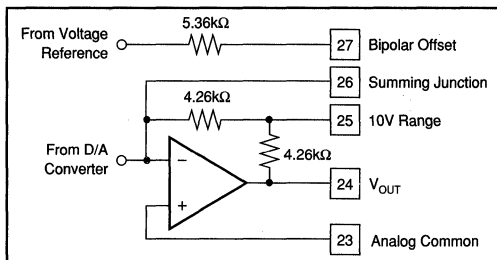
FIGURE 7. Output Amplifier Voltage Range Scaling Circuit.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 25 TO	CONNECT PIN 27 TO
0 to +10V	USB	24	23
±5	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

TABLE IV. Output Range Connections.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface to microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether. For instance, if half the memory space is unused, address line A15 of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each DAC811 occupies four address locations. A 74LS139 provides the two-to-four decoder and selects it with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. An 8205 decoder is an alternative to the 74LS139.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right-justified data formats, as illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 10 and 11 show an addressing scheme for right-justified and left-justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right-justified case, $X10_{16}$ loads the 8LSBs, and $X01_{16}$ loads the 4MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

Left-justified data is handled in a similar manner, shown in Figure 11. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.
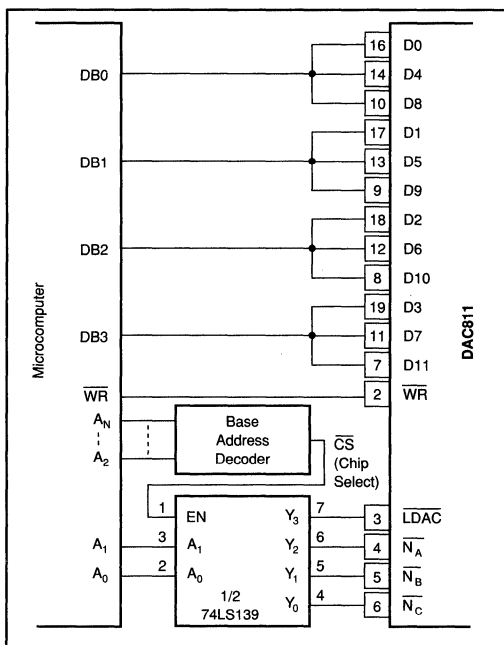
FIGURE 8. Addressing and Control for 4-Bit Microcomputer Interface.

a. Right-Justified
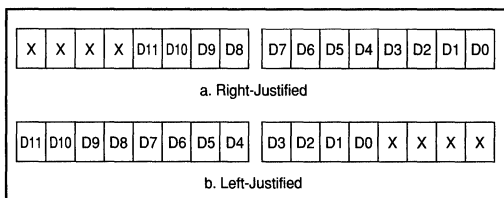
b. Left-Justified

FIGURE 9. 12-Bit Data Format for 8-Bit Systems.
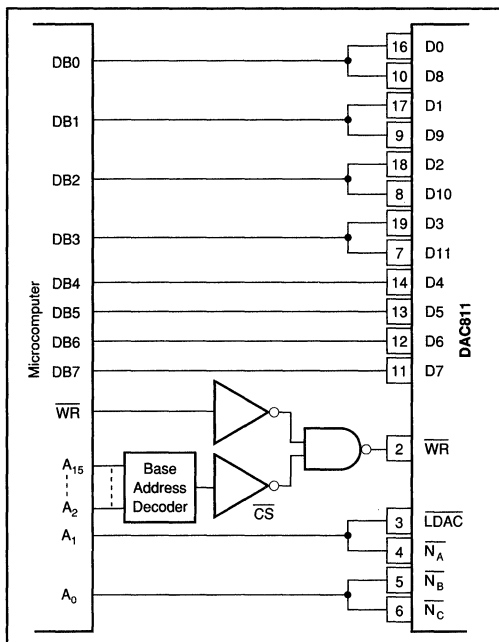
FIGURE 10. Right-Justified Data Bus Interface.
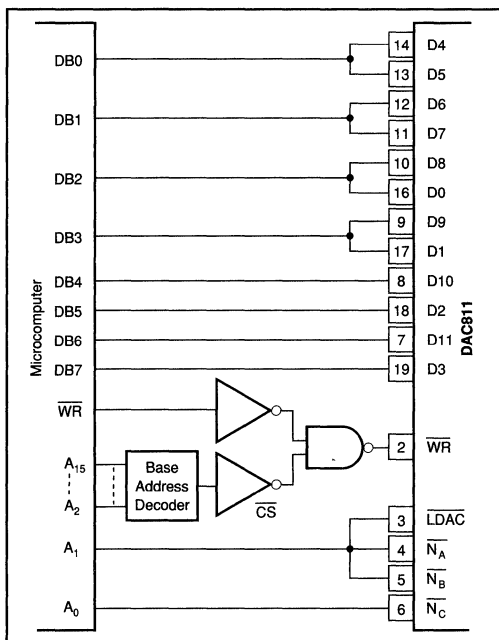
FIGURE 11. Left-Justified Data Bus Interface.

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DIGITAL-TO-ANALOG CONVERTERS

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INTERFACING MULTIPLE DAC811s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 12 uses a 74LS138 decoder to decode a set of eight adjacent addresses, to load the input latches of four DAC811s. The example shows a right-justified data format.

A ninth address using A_3 causes all DAC811s to be updated simultaneously. If a particular DAC811 is always loaded last—for instance, D/A #4—A_3 is not needed, thus saving eight address spaces for other uses. Incorporate A_3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application, the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$ and $\overline{N_C}$ are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC811, is selected by the address decoder and strobed by $\overline{WR}$.

ADDRESS BUS				
A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 MSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 MSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 MSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 12. Interfacing Multiple DAC811s to an 8-Bit Bus.

BURR - BROWN®

DAC813

Microprocessor-Compatible
12-BIT DIGITAL-TO-ANALOG CONVERTER

DAC813

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DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

DESCRIPTION

The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A con-

verter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to ±1/2LSB maximum linearity error (J, A grades) and ±1/4LSB (K, B grades). It is packaged in a 28-pin 0.3" wide ceramic DIP (–40°C to +85°C specification temperature range), 28-pin 0.3" wide plastic DIP and 28-lead plastic SO (0°C to +70°C).

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = $\pm12V$ or $\pm15V$ and load on V_{OUT} = 5kΩ || 500µF to common unless otherwise noted.

PARAMETER	CONDITIONS	DAC813AH, JP, JU, AU, D			DAC813BH, KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution				12			*	Bits
Codes[1]			USB, BOB			*		
Digital Inputs Over Temperature Range[2]								
V_{IH}[3]		+2		+5.5	*		*	VDC
V_{IL}		0		+0.8	*		*	VDC
DATA Bits, $\overline{WR}$, $\overline{Reset}$, $\overline{LDAC}$, $\overline{LMSB}$, $\overline{LLSB}$				±10			*	µA
I_{IH}	V_{IN} = +2.7V			±10			*	µA
I_{IL}	V_{IN} = +0.4V							
ACCURACY								
Linearity Error			±1/4	±1/2	±1/8	±1/4		LSB
Differential Linearity Error			±1/2	±3/4	±1/4	±1/2		LSB
Gain Error[4]			±0.05	±0.2	*		*	%
Unipolar Offset Error[5]			±0.01	±0.02	*		*	% of FSR[7]
Bipolar Zero Error[6]			±0.02	±0.2	*		*	% of FSR
Monotonicity			Guaranteed		*			
Power Supply Sensitivity: $+V_{CC}$	20V Range		5	10	*		*	ppm of FSR/%
$-V_{CC}$			1	10	*		*	ppm of FSR/%
DRIFT	Over Specification							
Gain	Temperature Range		±5	±30	*		±15	ppm/°C
Unipolar Offset			±1	±3	*		±3	ppm of FSR/°C
Bipolar Zero			±3	±10	*		±5	ppm of FSR/°C
Linearity Error Over Temperature Range			±1/2	±3/4	±1/4		±1/2	LSB
Monotonicity Over Temperature Range			Guaranteed		*			
SETTLING TIME[8] (To Within ±0.01% of FSR of Final Value; 5kΩ || 500pF load)								
For Full Scale Range Change	20V Range		4.5	6	*		*	µs
	10V Range		3.3	5	*		*	µs
For 1LSB Change at Major Carry[9]			2		*			µs
Slew Rate			10		*			V/µs
ANALOG OUTPUT								
Voltage Range: Unipolar	$\pm V_{CC} > \pm11.4V$		0 to +10			*		V
Bipolar	$\pm V_{CC} > \pm11.4V$		±5, ±10			*		V
Output Current		±5			*			mA
Output Impedance	At DC		0.2			*		Ω
Short Circuit to Common Duration			Indefinite			*		mA
REFERENCE VOLTAGE								
Voltage		+9.95	+10	+10.05	*	*	*	V
Source Current Available for External Loads		5			*			mA
Impedance			2			*		Ω
Temperature Coefficient			±5	±25	*		*	ppm/°C
Short Circuit to Common Duration			Indefinite		*			mA
POWER SUPPLY REQUIREMENTS								
Voltage: $+V_{CC}$		+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$		−11.4	−15	−16.5	*	*	*	VDC
Current: $+V_{CC} + V_L$	No Load		13	15	*	*	*	mA
$-V_{CC}$	No Load		−5	−7	*	*	*	mA
Potential at DCOM with Respect to ACOM[10]		−3		+3	*		*	V
Power Dissipation			270	330	*		*	mW
TEMPERATURE RANGE								
Specification: J, K, D		0		+70	*		*	°C
A, B		−40		+85	*		*	°C
Operating: J, K, D		−40		+85	*		*	°C
A, B		−55		+125	*		*	°C
Storage: J, K, D		−60		+100	*		*	°C
A, B		−65		+150	*		*	°C

*Same as specification for DAC813AH, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (5) Error at input code 000_{HEX} for unipolar mode, FSR = 10V. (6) Error at input code 800_{HEX} for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (7) FSR means Full Scale Range and is 20V for the ±10V range. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

DAC813

DIGITAL-TO-ANALOG CONVERTERS

MINIMUM TIMING DIAGRAMS

WRITE CYCLE #1

(Load first rank from Data Bus: $\overline{LDAC}$ = 1)

$\overline{LLSB}$, $\overline{LMSB}$ — > 50ns —

DB11–DB0 — > 50ns —

>5ns

$\overline{WR}$ — > 50ns —

WRITE CYCLE #2

(Load second rank from first rank: $\overline{LLSB}$, $\overline{LMSB}$ = 1)

$\overline{LDAC}$ — > 50ns —

$\overline{WR}$ — > 50ns —

$t_{SETTLING}$

±1/2LSB

RESET COMMAND (Bipolar Mode)

$\overline{LLSB}$, $\overline{LMSB}$, $\overline{LDAC}$, $\overline{WR}$ = Don't Care

$\overline{Reset}$

+10V — > 50ns — $t_{SETTLING}$

V_{OUT} 0V

±1/2LSB

–10V

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	+V$_L$	Positive supply pin for logic circuits. Connect to +V$_{CC}$.
2, 3	20V Range	Connect Pin 2 or Pin 3 to Pin 9 (V$_{OUT}$) for a 20V FSR. Connect both to Pin 9 for a 10V FSR.
4	BPO	Bipolar offset. Connect to Pin 6 (V$_{REF\ OUT}$) through 100Ω resistor or 200Ω potentiometer for bipolar operation.
5	ACOM	Analog common, ±V$_{CC}$ supply return.
6	V$_{REF\ OUT}$	+10V reference output referred to ACOM.
7	V$_{REF\ IN}$	Connected to V$_{REF\ OUT}$ through a 1kΩ gain adjustment potentiometer or a 500Ω resistor.
8	+V$_{CC}$	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V$_{OUT}$	D/A converter voltage output.
10	–V$_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
11	$\overline{WR}$	Master enable for $\overline{LDAC}$, $\overline{LLSB}$, and $\overline{LMSB}$. Must be low for data transfer to any latch.
12	$\overline{LDAC}$	Load DAC. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	$\overline{Reset}$	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	$\overline{LMSB}$	Enable for 4-bit input latch of D$_8$-D$_{11}$ data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path.
15	$\overline{LLSB}$	Enable for 8-bit input latch of D$_0$-D$_7$ data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

ABSOLUTE MAXIMUM RATINGS

+V$_{CC}$ to ACOM .... 0 to +18V
–V$_{CC}$ to ACOM .... 0 to –18V
+V$_{CC}$ to –V$_{CC}$ .... 0 to +36V
DCOM with respect to ACOM .... ±4V
Digital Inputs (Pins 11–15, 17–28) to DCOM .... –0.5V to +V$_{CC}$
External Voltage Applied to BPO Span Resistor .... ±V$_{CC}$
V$_{REF\ OUT}$ .... Indefinite Short to ACOM
V$_{OUT}$ .... Indefinite Short to ACOM
Power Dissipation 750mW
Lead Temperature (soldering, 10s) .... +300°C
Max Junction Temperature .... +165°C
Thermal Resistance, θ_{J-A}: Plastic DIP and SOIC ...... 130°C/W
          Ceramic DIP .... 85°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.
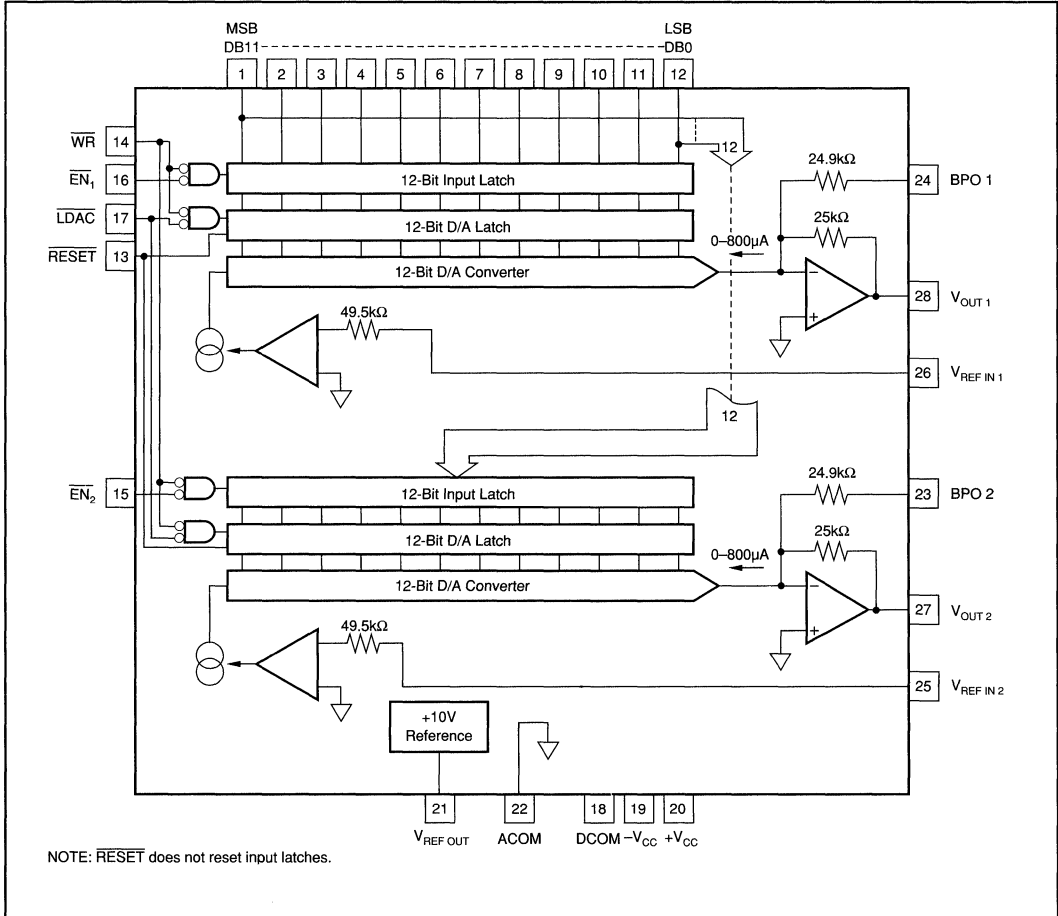
DICE INFORMATION

DAC813 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	$+V_L$	15	$\overline{LLSB}$
2	20V Range	16	DCOM
3	20V Range	17	DB0 (LSB)
4	BPO	18	DB1
5	ACOM	19	DB2
6	$V_{REF\,OUT}$	20	DB3
7	$V_{REF\,IN}$	21	DB4
8	$+V_{CC}$	22	DB5
9	V_{OUT}	23	DB6
10	$-V_{CC}$	24	DB7
11	$\overline{WR}$	25	DB8
12	$\overline{LDAC}$	26	DB9
13	$\overline{Reset}$	27	DB10
14	$\overline{LMSB}$	28	DB11 (MSB)

Substrate Bias: $-V_{CC}$
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	204 x 140 ±5	5.18 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C	GAIN DRIFT (ppm/°C)
DAC813AU	Plastic SOIC	–40°C to +85°C	±1/2LSB	±30
DAC813JP	Plastic DIP	0°C to +70°C	±1/2LSB	±30
DAC813JU	Plastic SOIC	0°C to +70°C	±1/2LSB	±30
DAC813KP	Plastic DIP	0°C to +70°C	±1/4LSB	±15
DAC813KU	Plastic SOIC	0°C to +70°C	±1/4LSB	±15
DAC813AH	Ceramic DIP	–40°C to +85°C	±1/2LSB	±30
DAC813BH	Ceramic DIP	–40°C to +85°C	±1/4LSB	±15

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC813AH	28-Pin Hermetic Side-Brazed DIP	247
DAC813BH	28-Pin Hermetic Side-Brazed DIP	247
DAC813AP	28-Pin Plastic DIP	246
DAC813KP	28-Pin Plastic DIP	246
DAC813AU	28-Pin Plastic SOIC	217
DAC813JU	28-Pin Plastic SOIC	217
DAC813KU	28-Pin Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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BB

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY

DIGITAL INPUT CURRENT
vs INPUT VOLTAGE

CHANGE OF GAIN AND OFFSET ERROR
vs TEMPERATURE

INTEGRAL LINEARITY ERROR

± FULL SCALE OUTPUT SWING

MAJOR CARRY GLITCH

DAC813

DIGITAL-TO-ANALOG CONVERTERS

3

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

SETTLING TIME, +10V TO –10V

SETTLING TIME, –10V TO +10V

DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
MSB to LSB			
FFF_{HEX}	+ Full Scale	+ Full Scale	Zero – 1LSB
800_{HEX}	+ 1/2 Full Scale	Zero	– Full Scale
$7FF_{HEX}$	+ 1/2 Full Scale – 1LSB	Zero – 1LSB	+ Full Scale
000_{HEX}	Zero	– Full Scale	Zero
* Invert MSB of BOB code with external inverter to obtain BTC code.			

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar Offset Drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.012% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of ±50mV. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 500Ω. The connection can be made through an optional 1kΩ trim resistor to provide adjustment to zero

gain error. The reference output may be used to drive external loads, sourcing at least 5mA. This current should be constant, otherwise the gain of the converter will vary.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a ppm of FSR output change per percent of change in either $+V_{CC}$ or $-V_{CC}$ about the nominal voltages expressed in ppm of FSR/%. The first performance curve on page 5 shows typical power supply rejection versus power supply ripple frequency.

OPERATION

DAC813 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

INTERFACE LOGIC

Input latches hold data temporarily while a complete 12-bit word is assembled before loading into the D/A latch. This double-buffered organization prevents the generation of spurious analog output values. Each latch is independently addressable.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for the control signals is presented in Table II.

$\overline{WR}$	$\overline{LLSB}$	$\overline{LMSB}$	$\overline{LDAC}$	$\overline{RESET}$	OPERATION
1	X	X	X	1	No operation
X	X	X	X	0	D/A latch set to 800_{HEX}
0	1	0	1	1	Enables 4 MSBs input latch
0	0	1	1	1	Enables 8 LSBs input latch
0	1	1	0	1	Loads D/A latch from input latches
0	0	0	0	1	Makes all latches transparent

"X" = Don't Care

TABLE II. DAC813 Interface Logic Truth Table.

CAUTION: DAC813 was designed to use $\overline{WR}$ as the fast strobe. $\overline{WR}$ has a much faster logic path than $\overline{EN}_X$ (or $\overline{LDAC}$). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_X$ to strobe data into the latches, the DATA HOLD time will be long, approximately 15ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

LOGIC INPUT COMPATIBILITY

The DAC813 digital inputs are TTL, 5V CMOS compatible over the operating range of $+V_{CC}$. The input switching threshold remains at the TTL threshold over the supply range. An equivalent circuit of a digital input is shown in Figure 2.

The logic input current over temperature is low enough to permit driving the DAC813 directly from the outputs of 5V CMOS devices.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition,
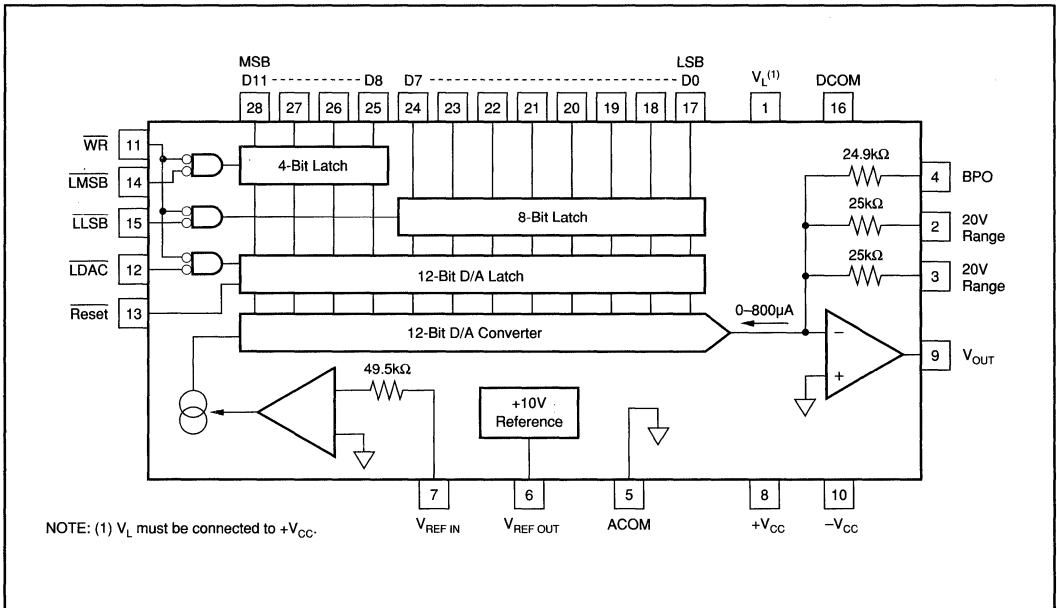
FIGURE 1. DAC813 Block Diagram.

NOTE: (1) V_L must be connected to $+V_{CC}$.

DAC813 · **3** · **DIGITAL-TO-ANALOG CONVERTERS**
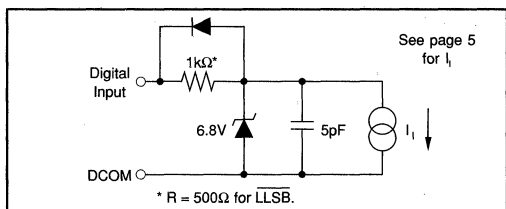
FIGURE 2. Equivalent Input Circuit for Digital Inputs.

the speed of the interface will be slower. A digital output driving a DATA input line of the DAC813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

RESET FUNCTION

When asserted low (<0.8V), $\overline{\text{RESET}}$ (Pin 13) forces the D/A latch to 800_{HEX} regardless of any other input logic condition. If the analog output is connected for bipolar operation (either ±10V or ±5V), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If $\overline{\text{RESET}}$ is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available $\overline{\text{Reset}}$ can be connected to $+V_{CC}$ through a 100kΩ to 1MΩ resistor to limit the input current.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB,

BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	0 to +10V	±5V	±10V
FFF_{HEX}	+9.9976V	+4.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V	0.0000V
7FF_{HEX}	+4.9976V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	–5.0000V	–10.0000V
1LSB	2.44mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to $-V_{CC}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Optimum settling performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$ and at least a 0.01µF ceramic capacitor at $+V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well. The 0.01µF capacitors should be located close to the DAC813.

Pin 1 supplies internal logic and **must** be connected to $+V_{CC}$.
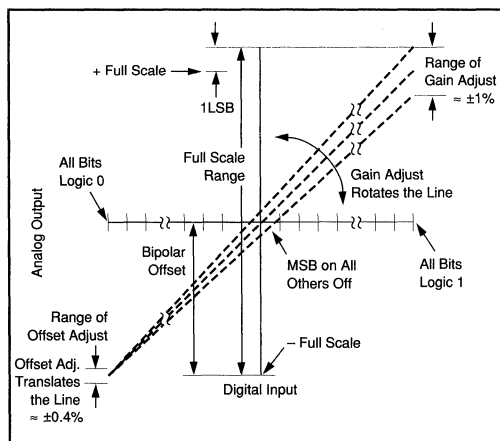
FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DAC813

DIGITAL-TO-ANALOG CONVERTERS

(1) 10µF tantalum for optimum settling performance.
(2) Unipolar offset is not necessary in most applications and can lead to noise pickup.
(3) Note that for the ceramic package the lid is connected to –V_{CC}.
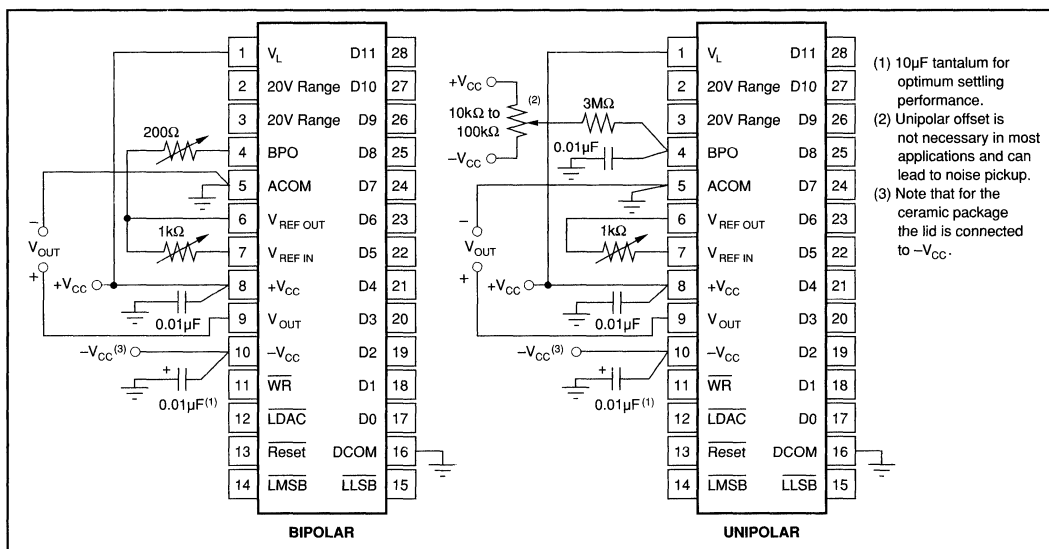
FIGURE 5. Power Supply, Gain, and Offset Connections.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 16) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from 000_{HEX} to FFF_{HEX} is only 800µA.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.

The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a 600Ω resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A 7.98kΩ resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A resistors.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{LMSB}$, $\overline{LLSB}$, and $\overline{LDAC}$ determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

8-BIT INTERFACE

The control logic of DAC813 permits interfacing to right-justified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. $X10_{HEX}$ loads the 8 LSBs and $X01_{HEX}$ loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{HEX}$ and $X11_{HEX}$ are not used.

INTERFACING MULTIPLE
DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address

spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common $\overline{\text{LDAC}}$ line to $\overline{\text{LLSB}}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{\text{LMSB}}$ and $\overline{\text{LLSB}}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by $\overline{\text{WR}}$.

Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.
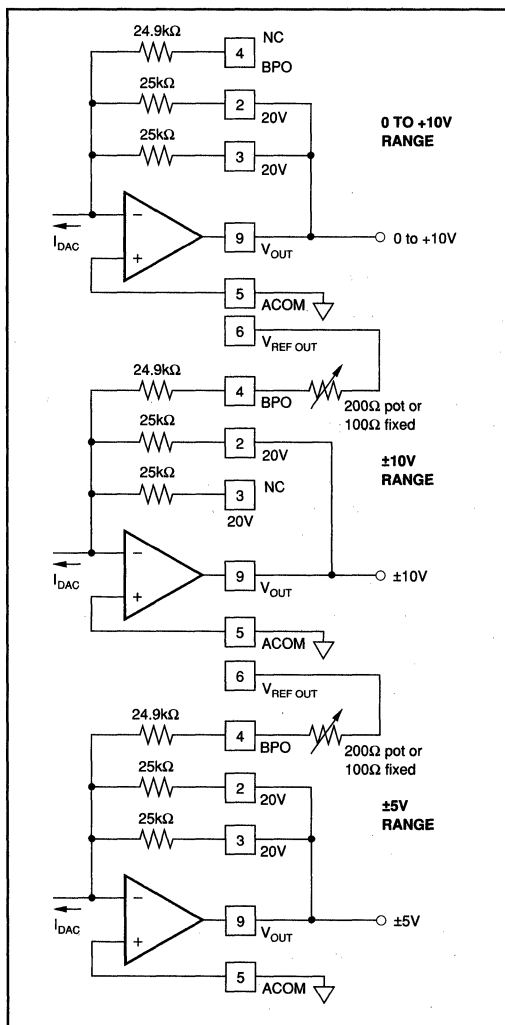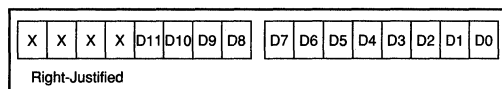
FIGURE 7. 12-Bit Data Format for 8-Bit Systems.
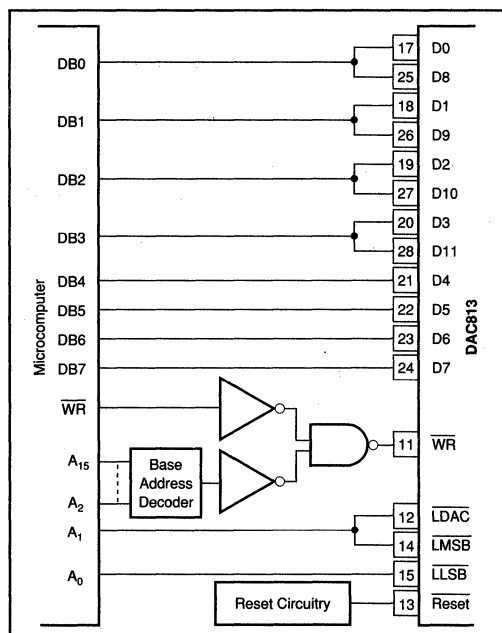
FIGURE 8. Right-Justified Data Bus Interface.

FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

ADDRESS BUS				OPERATION
A3	A2	A1	A0	
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 LSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 LSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 LSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A
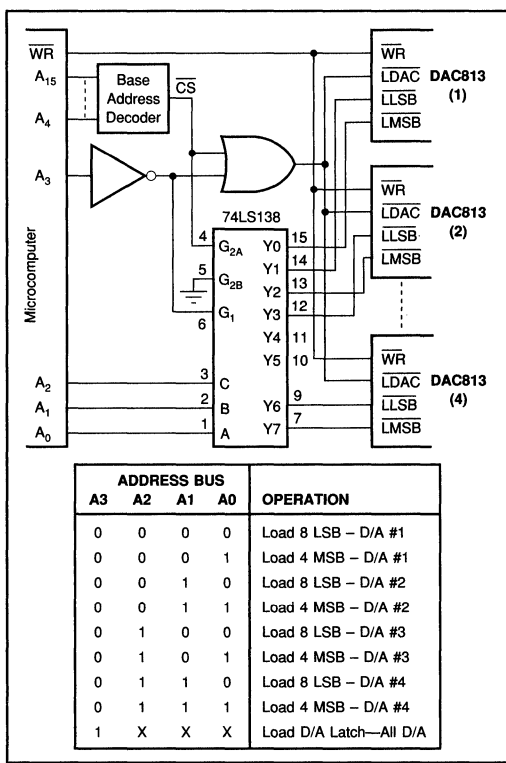
FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.

DIGITAL-TO-ANALOG CONVERTERS   DAC813

3

BURR - BROWN®

DAC1204/1214

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

QUAD Monolithic 12-Bit
DIGITAL-TO-ANALOG CONVERTER
(Serial Interface)

FEATURES

● **QUAD MONOLITHIC 12-BIT DAC**
  Current Output: 1mA Span
  Minimal External Components Required;
  One Op Amp Only
  Internal Feedback Resistor (R_{FB}) for
  External I/V Amp Trimmed at Wafer Level;
    DAC1204: V_{OUT} = ±10V
    DAC1214: V_{OUT} = ±5V, 0 to 10V
  Internal High Stability Voltage Reference
● **HIGH SPEED SERIAL INTERFACE:**
  10MHz Clock
● **FOUR DACs SIMULTANEOUS UPDATE**
  FUNCTION:
  Available Individual Updating
● **PROGRAMMABLE FUNCTION FOR**
  BIPOLAR/UNIPOLAR OUTPUT SELECT
● **CLEAR FUNCTION FOR RESET TO**
  OUTPUT ZERO
● **SINGLE +5V SUPPLY**
● **28-PIN SOIC**

APPLICATIONS

● **MOTOR CONTROL**
● **ATE PIN-ELECTRONICS LEVEL SETTING**
● **PROCESS CONTROL**
● **AUTO CALIBRATION CIRCUIT**
● **DSP PROCESSOR BOARD**
● **UPGRADE REPLACEMENT FOR**
  MULTIPLYING DAC

DESCRIPTION

The DAC1204 and DAC1214 are serial interface, quad 12-bit current output digital-to-analog convert-ers. These DACs consist of four separate DACs with high stability feedback resistors, a high-stability bandgap reference and a 16-bit serial-to-parallel reg-ister which is followed by four separate double-buff-ered registers on a single monolithic chip. The opti-mum performance is achieved from a combination of state-of-the art Bi CMOS process and advanced laser trimming technology.

The current output stage of the DAC1204 and DAC1214 has a pair of feedback resistors which are trimmed at wafer level. The feedback resistors of the DAC1204 are specified for ±10V output range, while the later is specified for ±5V (or 0 to 10V) output range. Thus the external I/V converter is possible with only one op amp for both bipolar and unipolar output range.

The DAC1204 and DAC1214 have a high speed serial interface capable of clocking in data at a rate of 10MHz. The serial data is a 16-bit word including channel address bits, output mode select (bipolar or unipolar mode) bits and actual DAC data. Serial data is clocked into the 16-bit shift register (MSB first) then latched into the DAC's first register. All DAC analog outputs can be simultaneously updated using asynchronous load (LOAD) signal. Also, DAC regis-ters can be updated independently. These DACs have an asynchronous clear (CLR) control for reset to bipolar zero or unipolar zero depending on the output mode selected. This feature is useful for power-on-reset or system calibration.

All digital pins are CMOS/TTL compatible. Power supply voltage is +5VDC. The DAC1204 and DAC1214 are available in 28 pin plastic SOIC pack-age.

PDS-1273

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

$T_A = 25°C$, $V_{CC} = V_{DD} = 5.0V$, V_{REF} = internal or external 2.500V, with external I/V amp using internal feedback resistor and suitable op-amp unless otherwise noted.

PARAMETER	DAC1204U, DAC1214U			DAC1204UB, DAC1214UB			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT							
Resolution		12			*		Bits
Digital Input Voltage							
V_{IH}	2.0		5.0	*		*	V
V_{IL}	0		0.8	*		*	V
Digital Input Current							
I_{IH} at V_{IH} = 5V			10			*	µA
I_{IL} at V_{IL} = 0V			100			*	µA
Maximum Input Clock Frequency	10			*			MHz
Input Pulse Width							
T_{WH}[(1)]	40			*			ns
T_{WL}[(1)]	40			*			ns
Input Set-up Time[(1)]			20			*	ns
Input Hold Time[(1)]			20			*	ns
TRANSFER CHARACTERISTICS							
DC ACCURACY							
Integral Linearity Error	−1.0		+1.0	−0.5		+0.5	LSB
Differential Linearity Error	−1.0		+1.0	−0.5		+0.5	LSB
Gain Error[(2)]	−8.0		+8.0	−4.0		+4.0	LSB
Bipolar Zero Error[(2)]	−4.0		+4.0	−2.0		+2.0	LSB
Unipolar Zero Error[(2)] (DAC1214 Only)	−2.0		+2.0	−1.0		+1.0	LSB
Monotonicity (0 to 70°C)		Guaranteed			Guaranteed		
MISMATCH AMONG CHANNELS							
Integral Linearity Error		1.0	TBD		0.5	TBD	LSB
Differential Linearity Error		1.0	TBD		0.5	TBD	LSB
Gain Error[(2)]		8.0	TBD		4.0	TBD	LSB
Bipolar Zero Error[(2)]		4.0	TBD		2.0	TBD	LSB
Unipolar Zero Error[(2)] (DAC1214 Only)		2.0	TBD		1.0	TBD	LSB
DRIFT (0 to 70°C)							
Gain Drift[(2)] with External V_{REF}		±10	TBD		*	TBD	ppm/°C
Gain Drift[(2)] with Internal V_{REF}		±25	TBD		*	TBD	ppm/°C
Bipolar Zero Drift[(2)] with External/Internal V_{REF}		±5	TBD		*	TBD	ppm FSR/°C
Unipolar Zero Drift[(2)] with External/Internal V_{REF} (DAC1214 Only)		±5	TBD		*	TBD	ppm FSR/°C
AC PERFORMANCE							
Settling Time; (to 0.012% of FSR, Load to I_{OUT})		500			*		ns
Glitch Energy[(3)]		20			*		nV-s
Crosstalk;[(3)]							
Digital-to-Analog		20			*		nV-s
Channel-to-Channel		−78			*		dB
REFERENCE							
External Reference Voltage Range	2.45	2.50	2.55	*	*	*	V
External Reference Current Drain at V_{REF} = 2.500V		±10	±50		*	*	µA
ANALOG OUTPUT							
Voltage Output Configuration							
Bipolar Range							
DAC1204		±10			*		V
DAC1214		±5			*		V
Unipolar Range							
DAC1214		0 to +10			*		V
Output Impedance at Output to Ground		1.0			*		kΩ
Short Circuit Duration		Indefinite to Ground			*		
POWER SUPPLY REQUIREMENTS							
Supply Voltage							
V_{CC}, V_{DD}	4.75	5.00	5.25	*	*	*	V
Supply Current (No Load)							
$I_{CC} + I_{DD}$ ($V_{CC} = V_{DD}$ = 5.0V)		20	TBD		*	*	mA
Power Dissipation		100	TBD		*	*	mW
Power Supply Rejection Ratio[(2)]		±0.001			*		% of FSR/% V_{CC}
TEMPERATURE RANGE							
Specification	0		70	*		*	°C
Operating	−40		+85	*		*	°C
Storage	−55		+125	*		*	°C

NOTES: (1) See serial interface timing for details. (2) Offset, linearity and CMRR of external Op-Amp influence each performance. (3) Specified condition (Clock/Signal frequency. Op-Amp, Band-Width, etc.) should be determined.

DAC1204/1214

DIGITAL-TO-ANALOG CONVERTERS

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BLOCK DIAGRAM
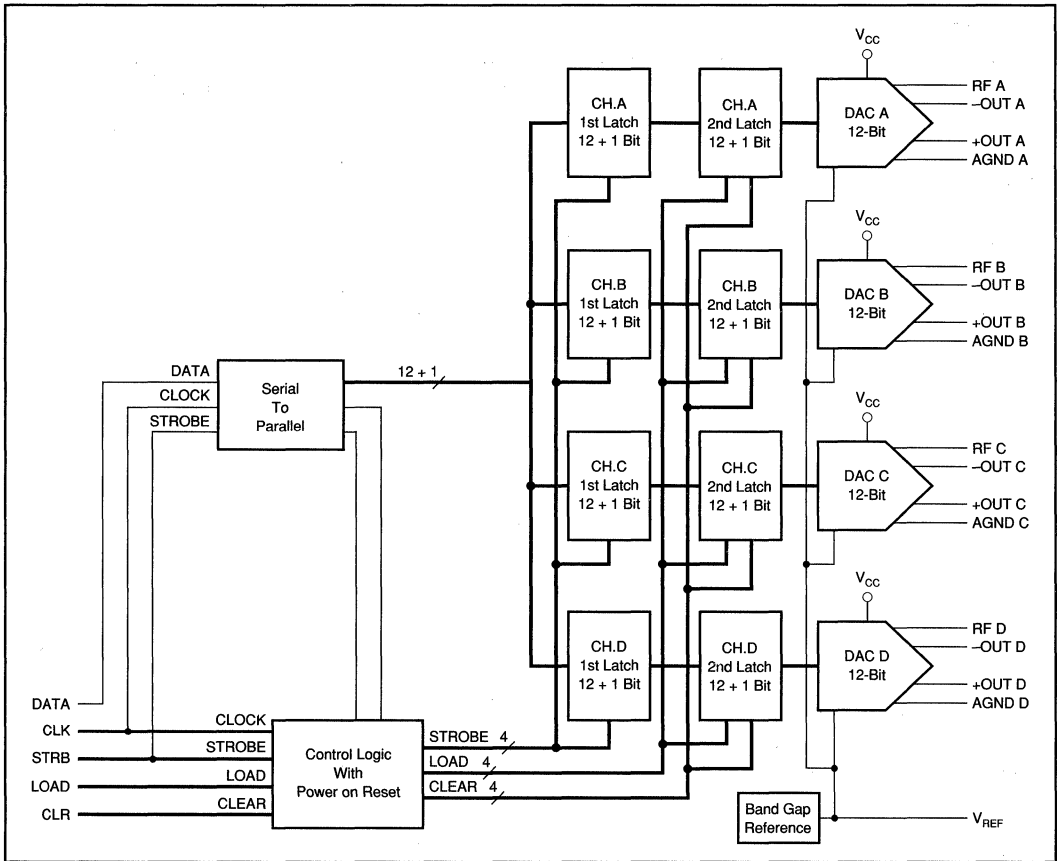
ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .... 0 to +6V
V_{CC} to AGND .... 0 to +6V
AGND to DGND .... ±0.3V
Digital Input to DGND .... −0.3V to +V_{DD} +0.3V
External Voltage applied to;
Internal Feed-back Resistor .... ±25V
$V_{REF\ IN}$ .... −0.3V to V_{CC} +0.3V
−Out/+Out .... −0.3V to V_{CC} +0.3V
Lead Temperature; (soldering, 5s) .... +260°C
(reflow, 10s) .... +235°C
Max Junction Temperature .... +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	OUTPUT RANGE	LINEARITY ERR	PACKAGE
DAC1204U	±10V	±1LSB	28-Pin SOIC
DAC1204UB	±10V	±0.5LSB	28-Pin SOIC
DAC1214U	±5V, 0 to 10V	±1LSB	28-Pin SOIC
DAC1214UB	±5V, 0 to 10V	±0.5LSB	28-Pin SOIC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC1204U, UB	28-Pin SOIC	809
DAC1204UB	28-Pin SOIC	809
DAC1214U	28-Pin SOIC	809
DAC1214UB	28-Pin SOIC	809

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	−OUTA	DAC A Current Output.
2	+OUTA	DAC A Common Current Output.
3	AGNDA	DAC A Analog Ground.
4	RFA	DAC A Feed-back Resistor.
5	STRB	1st Latch Register Update. Data is latched in on negative edge.
6	DATA	Serial Data Input. Data is clocked in on positive edge of the CLK.
7	CLK	Serial Clock Input.
8	LOAD	Load DAC Input (active low) - 2nd Latch Register Update.
9	CLR	Reset to DAC Output zero (active low).
10	RFB	DAC B Feed-back Resistor.
11	AGNDB	DAC B Analog Ground.
12	+OUTB	DAC B Common Current Output.
13	−OUTB	DAC B Current Output.
14	DGND	Digital Ground.
15	V_{DD}	Digital Power Supply, +5V typ.
16	−OUTC	DAC C Current Output.
17	+OUTC	DAC C Common Current Output.
18	AGNDC	DAC C Analog Ground.
19	RFC	DAC C Feed-back Resistor.
20	V_{REF}	Reference Voltage Input.
21	V_{CC}	Analog Power Supply, +5V typ.
22	V_{CC}	Analog Power Supply, +5V typ.
23	AGND	Analog Power Ground.
24	AGND	Analog Power Ground.
25	RFD	DAC D Feed-back Resistor.
26	AGNDD	DAC D Analog Ground.
27	+OUTD	DAC D Common Current Output.
28	−OUTD	DAC D Current Output.

PIN CONNECTIONS
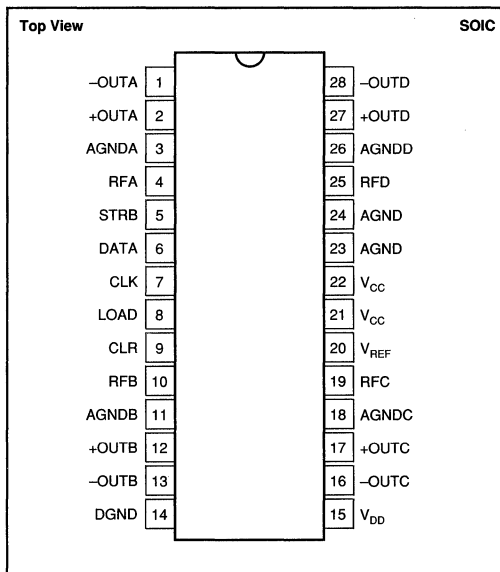
Top View   SOIC

−OUTA	1		28	−OUTD
+OUTA	2		27	+OUTD
AGNDA	3		26	AGNDD
RFA	4		25	RFD
STRB	5		24	AGND
DATA	6		23	AGND
CLK	7		22	V_{CC}
LOAD	8		21	V_{CC}
CLR	9		20	V_{REF}
RFB	10		19	RFC
AGNDB	11		18	AGNDC
+OUTB	12		17	+OUTC
−OUTB	13		16	−OUTC
DGND	14		15	V_{DD}

DAC1204/1214

DIGITAL-TO-ANALOG CONVERTERS

3

DIGITAL INPUTS DESCRIPTION

INPUT CODES

All digital inputs are TTL and CMOS compatible. For bipolar output range, input codes for the DAC1204 and DAC1214 are Binary Two's Compliment (BTC) code. For unipolar output range, input codes are Unipolar Straight Binary (USB) code. The input/output relationship is shown in Table Ia and Ib.

DIGITAL INPUT CODE (BTC)	ANALOG OUTPUT (BIPOLAR)
7FF$_{HEX}$	+FS
000$_{HEX}$	BPZ
FFF$_{HEX}$	BPZ –1LSB
800$_{HEX}$	–FS

TABLE Ia. Digital Input/Bipolar Output Relationships.

DIGITAL INPUT CODE (USB)	ANALOG OUTPUT (UNIPOLAR)
FFF$_{HEX}$	FS
800$_{HEX}$	FS/2
7FF$_{HEX}$	FS/2 –1LSB
000$_{HEX}$	ZERO

TABLE Ib. Digital Input/Unipolar Output Relationships.

SERIAL INPUT DATA FORMAT

Serial data is a 16-bit word per channel and is clocked in on the raising edge of clock (CLK) into the internal 16-bit shift register with MSB first format. Figure 1 shows the serial data input format. The 16-bit serial input format comprises two DAC address bits (A1, A0), two output mode select bits (M1, M0) and twelve bits of DAC data (D11...D00). A1 and A0 shown in Table IIa set the DAC address, and M1 and M0 shown in Table IIb select the output range of bipolar or unipolar.

A1	A0	SELECTED DAC
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

TABLE IIa. DAC Address.

M1	M0	DAC OUTPUT MODE
0	0	Bipolar Output
0	1	Unipolar Output
1	X	Reserved

NOTES: 0 = logical "Low", 1 = logical "High", X = Don't Care.

TABLE IIb. DAC Output Mode Select.

DIGITAL INTERFACE TIMING

Interface logic signals of the DAC1204 and DAC1214 consist of the serial data clock (CLK), serial data (DATA), strobe (STRB), load (LOAD) and clear (CLR) controls. Figure 2 shows a typical interface timing diagram. The serial data is clocked in on positive edge of CLK into the shift register until all 16 bits of data are entered and then is transferred into the addressed DAC first latch register from the shift register on negative edge of STRB. The DAC data is allowed to stay in each first register until each first latch register is updated by next STRB signal. Also the STRB signal and DAC address bits (A0, A1) on serial data frame with LOAD signal allow DAC update; independently or simultaneously. The STRB signal must be "High" for at least one clock cycle before going "Low" and must be held "Low" for at least one cycle after the signal is changed from "High" to "Low" as shown in Figure 2.

DB15	DB14	DB13	DB12	DB11	DB10	DB09	DB08	DB07	DB06	DB05	DB04	DB03	DB02	DB01	DB00
A1	A0	M1	M0	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

DAC INPUT DATA: BTC code for Bipolar Output
USB code for Unipolar Output
NOTE: D11 = MSB, D00 = LSB

OUTPUT MODE: M1 M0 DAC OUTPUT MODE
0 0   Bipolar
0 1   Unipolar
1 X   RESERVED

DAC ADDRESS: A1 A0 DAC ADDRESS
0 0   DAC A
0 1   DAC B
1 0   DAC C
1 1   DAC D
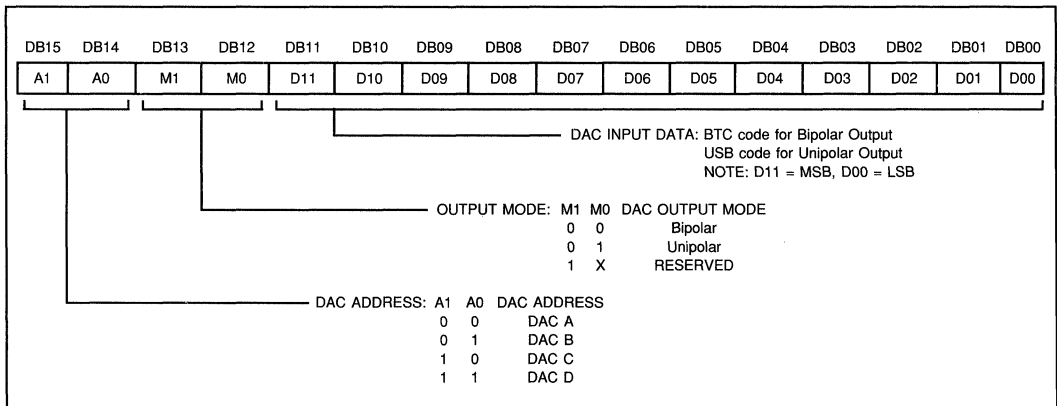
FIGURE 1. Serial Input Data Format.

LOAD signal is asynchronous with respect to DATA, CLK and STRB signals and can simultaneously update all four DAC second latch registers. When LOAD signal is changed "High" to "Low", the data on all first latch registers are loaded into corresponding second latch registers and DAC's outputs are updated simultaneously. This mode is a Latch Mode. In this case, if the LOAD signal become "Low" within two clocks from the negative edge of STRB signal, the previous data of first latch register is loaded into the second latch register. If LOAD signal is fixed "Low", the data on the first latch register addressed by A1, A0 is loaded into corresponding second latch register on second negative edge of CLK after STRB goes "Low", and in this case, DAC's output can be updated independently. This is a Transparent Mode.

CLR signal, also, is asynchronous with respect to DATA, CLK, STRB signals and can simultaneously reset to bipolar zero or unipolar zero depending on the output mode selected (M_0, M_1) when the CLR is "Low".

CIRCUIT CONNECTION

Figure 3 shows a typical connection diagram for the DAC1204 and DAC1214. The output stage of the DAC1204 and DAC1214 is current output mode.

For optimum performance and noise rejection, the DACs and I/V op amp should be located close to each other and power supply decoupling capacitors should be located close to the DACs.
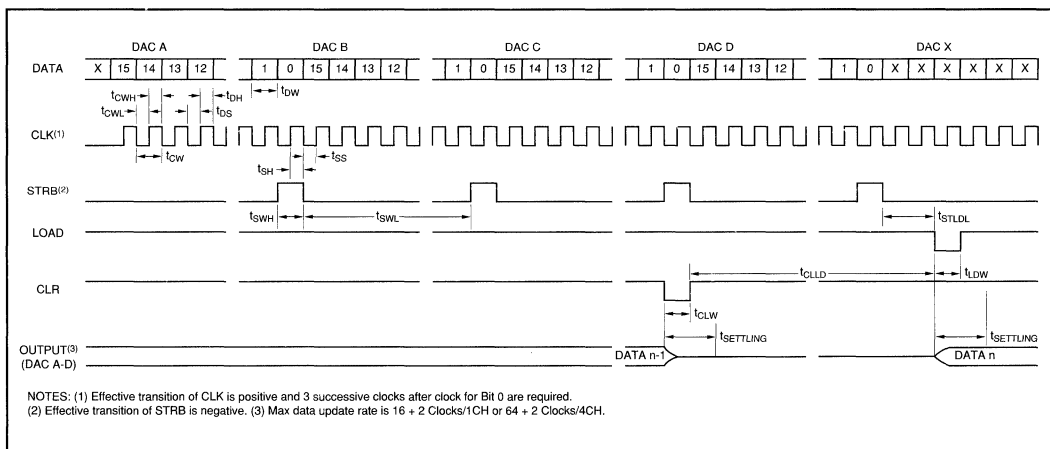
FIGURE 2a. Serial Interface Timing Diagram (Latch Mode).
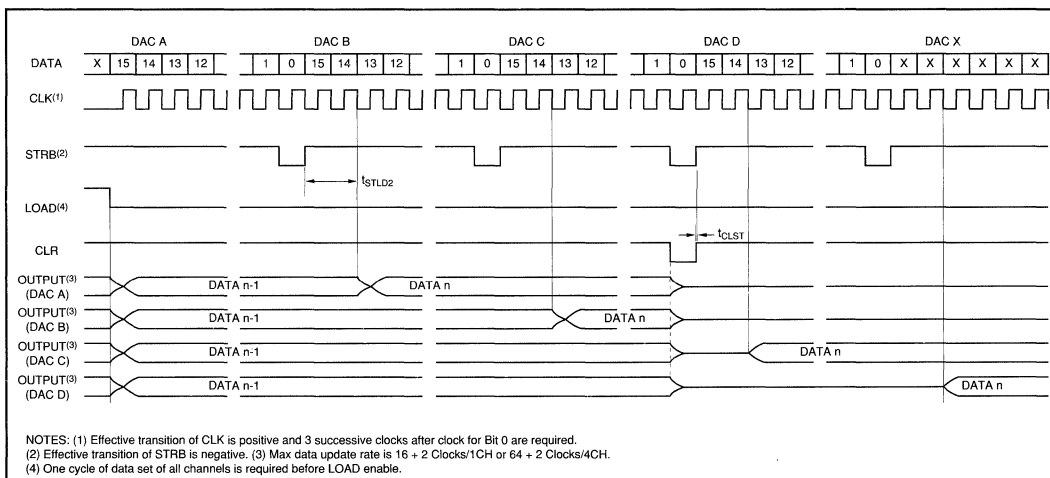
FIGURE 2b. Serial Interface Timing Diagram (Transparent Mode).

TIMING SPECIFICATION

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CW}	CLOCK (CLK) width	100			ns
t_{CWL}	CLOCK (CLK) low width	40			ns
t_{CWH}	CLOCK (CLK) high width	40			ns
t_{SWL}	STROBE (STRB) low width	1			CLOCK
t_{SWH}	STROBE (STRB) high width	1			CLOCK
t_{DW}	DATA (DATA) width	100			ns
t_{LDW}	LOAD (LOAD) low width	40			ns
t_{CLW}	CLEAR (CLR) low width	40			ns
t_{DS}	DATA (DATA) to CLOCK (CLK) set-up time	20			ns
t_{DH}	DATA (DATA) to CLOCK (CLK) hold time	20			ns
t_{SS}	STROBE (STRB) to CLOCK (CLK) set-up time	20			ns
t_{SH}	STROBE (STRB) to CLOCK (CLK) hold time	20			ns
t_{STLD1}	STROBE (STRB) to LOAD (LOAD) delay time for latch mode	2.5			CLOCK
t_{STLD2}	STROBE (STRB) to LOAD (LOAD) delay time for transparent mode			2.5	CLOCK
t_{CLLD}	CLEAR (CLR) to LOAD (LOAD) delay time	100			ns
t_{CLST}	CLEAR (CLR) to STROBE (STRB) delay time	0			ns
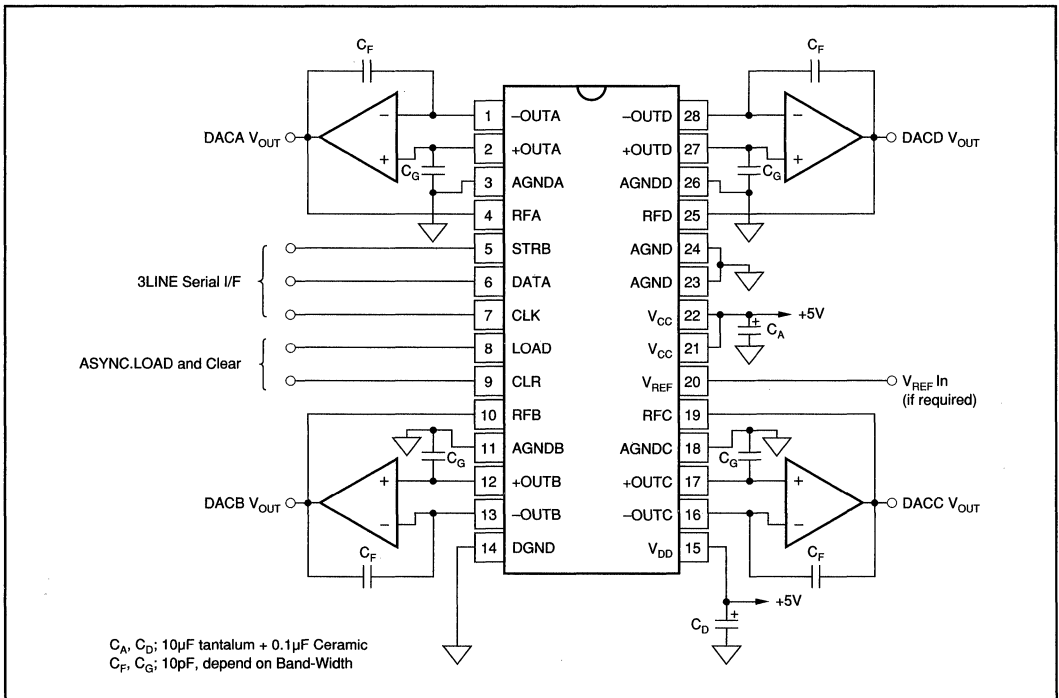
FIGURE 3. Typical I/V Amp Connection.

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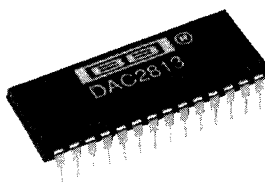
DAC2813

DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

DAC2813

3

DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS**

● **12-BIT PORT INTERFACE**

● **ANALOG OUTPUT RANGE: ±10V**

● **MONOTONICITY GUARANTEED OVER TEMPERATURE**

● **INTEGRAL LINEARITY ERROR: ±1/2LSB max**

● **±12V to ±15V SUPPLIES**

● **28-PIN PLASTIC DIP PACKAGE**

DESCRIPTION

DAC2813 is a complete dual 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC2813 output range resistors are internally connected for 20V full scale range. A 0 to 10V range can be connected using the bipolar offset resistor. Gain and bipolar offset of each D/A are adjustable with external trim potentiometers.

DAC2813 is available in one performance grade with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C.

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, +V_{CC} = +12V or +15V, −V_{CC} = −12V or −15V unless otherwise noted.

PARAMETER	CONDITIONS	DAC2813AP			UNITS
		MIN	TYP	MAX	
INPUTS					
DIGITAL INPUTS	Over Temperature				
Input Code [1]	Range		Bipolar Offset Binary		
Logic Levels [2]					
V_{IH}		+2		+5.5[3]	V
V_{IL}		0		+0.8	V
Logic Input Currents					
DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$, $\overline{EN}_X$					
I_{IH}	V_I = +2.7V			±20	μA
I_{IL}	V_I = +0.4V			±20	μA
TRANSFER CHARACTERISTICS					
ACCURACY					
Linearity Error			±1/4	±1/2	LSB
Differential Linearity Error			±1/2	±1	LSB
Gain Error [5,6]			±0.05	±0.2	%
Bipolar Zero Error [5,7]			±0.05	±0.2	%FSR[4]
Power Supply Sensitivity					
Of Full Scale +V_{CC}			±5	±20	ppmFSR/%+V_{CC}
−V_{CC}			±1	±10	ppmFSR/%−V_{CC}
DRIFT	Over Specification				
	Temperature Range				
Gain			±5	±30	ppm/°C
Bipolar Zero Drift			±5	±15	ppmFSR/°C
Linearity Error over Temperature			±1/2	±3/4	LSB
Monotonicity			Guaranteed		
DYNAMIC CHARACTERISTICS					
SETTLING TIME [8]	To within ±0.012%FSR				
	of Final Value				
	5kΩ ‖ 500pF Load				
Full Scale Range Change	20V Range		4.5	6	μs
1LSB Output Step [9] At Major Carry			2		μs
Slew Rate			10		V/μs
Crosstalk [10]	5kΩ Loads		0.1		LSB
OUTPUT					
Output Voltage Range	±V_{CC} ≥ ±11.4V			±10	V
Output Current		±5			mA
Output Impedance			0.2		Ω
Short Circuit to ACOM Duration			Indefinite		
REFERENCE VOLTAGE					
Voltage		+9.95	+10.00	+10.05	V
Source Current Available					
for External Loads		2			mA
Impedance			0.2		Ω
Temperature Coefficient			±5	±25	ppm/°C
Short Circuit to Common Duration			Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: +V_{CC}		+11.4	+15	+16.5	V
−V_{CC}		−11.4	−15	−16.5	V
Current:	No Load				
	±V_{CC} = ±15V				
+V_{CC}			24	30	mA
−V_{CC}			12	14	mA
Power Dissipation			540	660	mW
Potential at DCOM with					
Respect to ACOM [11]		−3		+3	V
TEMPERATURE RANGES					
Specification		−40		+85	°C
Storage		−60		+100	°C
Thermal Resistance, θ_{JA}, Plastic DIP			30		°C/W

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Adjustable to zero with external trim potentiometer. (6) Specified with 500Ω connected between $V_{REF\,OUT}$ and $V_{REF\,IN}$. (7) Error at input code 800$_{HEX}$. DAC2813 specified with 100Ω connected between $V_{REF\,OUT}$ and $V_{REF\,IN}$; and with 500Ω connected between $V_{REF\,OUT}$ and BPO. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) For the worst-case code change: 7FF$_{HEX}$ to 800$_{HEX}$ and 800$_{HEX}$ to 7FF$_{HEX}$. (10) Crosstalk is defined as the change in any output as a result of any other output being driven from −10V to +10V at rated output current. (11) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

ABSOLUTE MAXIMUM RATINGS

```
+V_CC to ACOM ............................................................ 0 to +18V
−V_CC to ACOM ............................................................ 0 to −18V
+V_CC to −V_CC ............................................................ 0 to +36V
ACOM to DCOM .................................................................. ±4V
Digital Inputs to DCOM ............................................. −1V to +V_CC
External Voltage applied to BPO Resistor ........................................ ±18V
V_REF OUT ....................................................... Indefinite short to ACOM
V_OUT ..................................................................... Momentary to ±18V
Lead Temperature, soldering 10s ................................................. +300°C
Max Junction Temperature ............................................ 165°C
```

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
DAC2813AP	28-Pin DBL Wide DIP	−40°C to +85°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC2813AP	28-Pin DBL Wide DIP	167

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DAC2813

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DIGITAL-TO-ANALOG CONVERTERS

BLOCK DIAGRAM

NOTE: RESET does not reset input latches.

TIMING DIAGRAMS

WRITE CYCLE #1

(Load first rank from Data Bus: $\overline{LDAC}$ = 1)

WRITE CYCLE #2

(Load second rank from first rank: $\overline{EN}_X$ = 1)
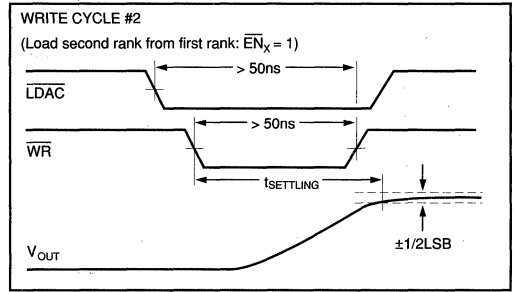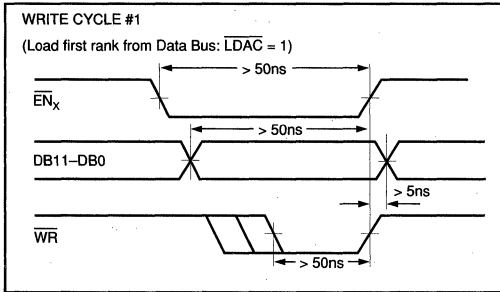
TRUTH TABLE

WR	EN1	EN2	LDAC	RESET	OPERATION
X	X	X	X	0	Reset both D/A Latches. Does not reset input latches.
1	X	X	X	1	No Operation
X	1	1	1	1	No Operation
0	1	0	1	1	Load Data into First Rank for D/A 2
0	0	1	1	1	Load Data into First Rank for D/A 1
0	1	1	0	1	Load Second Rank from First Rank, both D/As
0	0	0	0	1	All Latches Transparent

"X" = Don't Care

RESET COMMAND (Bipolar Mode)

$\overline{EN}_X$, $\overline{LDAC}$, $\overline{WR}$ = Don't Care

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	DB11	DATA, MSB, positive true.
2	DB10	DATA
3	DB9	DATA
4	DB8	DATA
5	DB7	DATA
6	DB6	DATA
7	DB5	DATA
8	DB4	DATA
9	DB3	DATA
10	DB2	DATA
11	DB1	DATA
12	DB0	DATA, LSB.
13	$\overline{RESET}$	Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten an $\overline{LDAC}$-$\overline{WR}$ command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state.
14	$\overline{WR}$	Write strobe. Must be low for data transfer to any latch (except RESET).
15	$\overline{EN2}$	Enable for 12-bit input data latch of D/A 2. NOTE: This logic path is slower than the WR\ path.
16	$\overline{EN1}$	Enable for 12-bit input data latch of D/A 1. NOTE: This logic path is slower than the WR\ path.
17	$\overline{LDAC}$	Load DAC enable. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of both D/A converters.
18	DCOM	Digital common, logic currents return.
19	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
20	$+V_{CC}$	Analog supply input, nominally +12V or +15V referred to ACOM.
21	$V_{REF\ OUT}$	+10V reference output.
22	ACOM	Analog common, $+V_{CC}$, $-V_{CC}$ supply return.
23	BPO2	Bipolar offset. Connect to pin 21 ($V_{REF\ OUT}$) through a 100Ω resistor or through a 200 potentiometer for Bipolar Offset Adjust for D/A 2.
24	BPO1	Bipolar offset. Connect to pin 21 ($V_{REF\ OUT}$) through a 100Ω resistor or through a 200 potentiometer for Bipolar Offset Adjust or D/A 1.
25	$V_{REF\ IN\ 2}$	Connect to $V_{REF\ OUT}$ through 500Ω fixed resistor or through a 1kΩ gain adjustment potentiometer for D/A 2.
26	$V_{REF\ IN\ 1}$	Connect to $V_{REF\ OUT}$ through 500Ω fixed resistor or through a 1kΩ gain adjustment potentiometer for D/A 1.
27	$V_{OUT\ 2}$	D/A 2 analog output.
28	$V_{OUT\ 1}$	D/A 1 analog output.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY

DIGITAL INPUT CURRENT vs INPUT VOLTAGE

CHANGE OF GAIN AND OFFSET ERROR
vs TEMPERATURE

INTEGRAL LINEARITY ERROR

± FULL SCALE OUTPUT SWING

MAJOR CARRY GLITCH

DAC2813

DIGITAL-TO-ANALOG CONVERTERS

3

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{cc} = ±15V unless otherwise noted.

SETTLING TIME, +10V TO −10V

SETTLING TIME, +10V TO −10V

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all "1s" and all "0s"). DAC2813 linearity error is ±1/2LSB max at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word If the DLE is more positive than −1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. DAC2813 is monotonic over their specification temperature range −40°C to +85°C.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Settling times are specified to ±0.01% of Full Scale Range (FSR) for two conditions: one for a FSR output change of 20V (25kΩ feedback) and one for a 1LSB change. The 1LSB change is measured at the Major Carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input code transition at which worst-case settling time occurs.

OPERATION

INTERFACE LOGIC

The bus interface logic of the DAC2813 consists of two independently addressable latches in two ranks for each D/A converter. The first rank consists of one 12-bit input latch which can be loaded directly from a 12- or 16-bit microprocessor/microcontroller bus. The input latch holds data temporarily before it is loaded into the second latch, the D/A latch. This double buffered organization permits simultaneous update of all D/As.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When the control signals return to logic "1", the data is latched.

CAUTION: DAC2813 was designed to use $\overline{WR}$ as the fast strobe. WR/ has a much faster logic path than $\overline{EN}_X$ (or LDAC). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_X$ to strobe data into the latches,

the DATA HOLD time will be long, approximately 20ns to 30ns and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

RESET FUNCTION

The Reset function resets only the D/A latch. Therefore, after a RESET, good data must be written to **all** the input latches before an $\overline{LDAC} - \overline{WR}$ command is issued. Otherwise, old data or unknown data is present in the input latches and will be transferred to the D/A latch producing an analog output value that may be unwanted.

LOGIC INPUT COMPATIBILITY

DAC2813 digital inputs are TTL compatible (1.4V switching level) over the operating range of $+V_{CC}$. Each input has low leakage and high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC2813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition, the speed of the interface will be slower. A digital output driving a DATA input line of the DAC2813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

Unused CONTROL inputs should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available, the control inputs can be connected to $+V_{CC}$ through a 100kΩ resistor to limit the input current.

DIGITAL INPUT	DAC2813 RΩ
Data, $\overline{LDAC}$, $\overline{WR}$, RESET	500
$\overline{EN}_X$	330
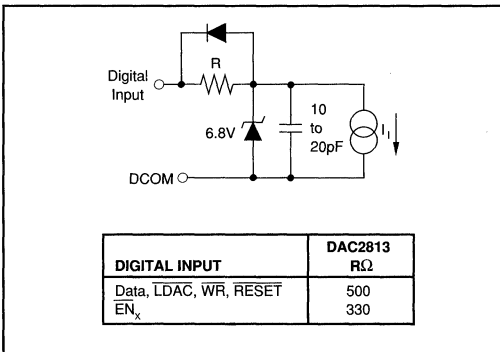
FIGURE 1. Equivalent Digital Input Circuit.

INPUT CODING

DAC2813 accepts positive-true binary input codes.

Input coding for bipolar analog outputs is Bipolar Offset Binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

DAC2813 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

DAC2813 can be connected for 0 to +10V unipolar operation by using the BPO resistors, plus a 100Ω series resistor, in parallel with the internal feedback resistor. In this case, an input code of 000_{HEX} gives zero volt output, an input of FFF_{HEX} gives an output 1LSB below positive full scale.

INTERNAL/EXTERNAL REFERENCE USE

DAC2813 contains a +10V ±50mV voltage reference, $V_{REF OUT}$. $V_{REF OUT}$ is available to drive external loads sourcing up to 2mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the D/A converters will vary.

For DAC2813 $V_{REF OUT}$ must be connected to $V_{REF IN 1}$ and $V_{REF IN 2}$ through gain adjust resistors with a nominal value of 500 Ω. Trim potentiometers with a nominal value of 1000Ω can be used to provide adjustment to zero gain error.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. However, DAC2813 is optimized for fixed-reference applications. If the reference voltage is expected to time-vary over a wide range, a CMOS multiplying D/A is a better choice.
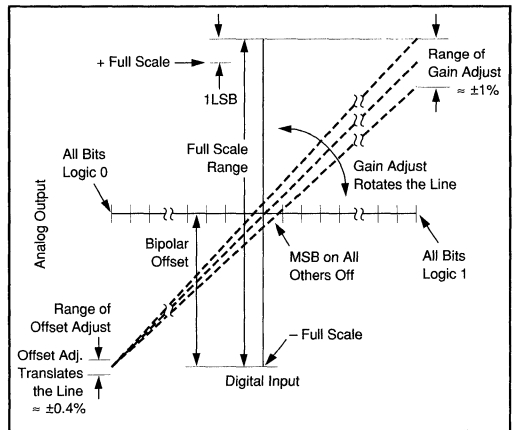
FIGURE 2. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT	
	UNIPOLAR 0 TO +10V	BIPOLAR ±10V
FFF_{HEX}	+9.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V
$7FF_{HEX}$	+4.9976V	–0.0049V
000_{HEX}	0.0000V	–10.0000V
1LSB	2.44mV	4.88mV

TABLE III. Analog Output Calibration Values.

GAIN AND OFFSET ADJUSTMENTS

Figure 2 illustrates the relationship of offset and gain adjustments to a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments.

Offset Adjustment

For bipolar analog output operation, apply digital input code 000_{HEX} to produce the maximum negative output and adjust the offset potentiometer for –10.000V. See Table III for calibration values and codes.

Gain Adjustment

For either unipolar or bipolar operation, apply digital input code FFF_{HEX} gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for calibration values.

INSTALLATION

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best settling time performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

DAC2813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both DIGI-TAL COMMON (DCOM) and ANALOG COMMON (ACOM) be connected directly to a ground plane under the package. If a ground place is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. The change in current in the ACOM pin due to an input date word change from 000_{HEX} to FFF_{HEX} is only 1mA for each D/A converter.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

DAC2813 output amplifiers provide a ±10V output swing while operating on supplies as low as ±12V ±5%.

DAC2813 is internally connected to provide ±10V output when the bipolar offset pins BPO1 and/or BPO2 are connected, through 100Ω resistors, to $V_{REF\ OUT}$. For a unipolar 0 to +10V output, the BPO resisitor, in series with a 100Ω external resistor, may be paralleled with the internal feedback resistor to provide the correct scaling. The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of ±2%.

12- AND 16-BIT BUS INTERFACES

DAC2813 data is latched into the input latches of each D/A by asserting low each ENx individually and transferring the data from the bus to each input latch by asserting WR low. All D/A outputs in each package are then updated simultaneously by asserting LDAC and WR low. Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.
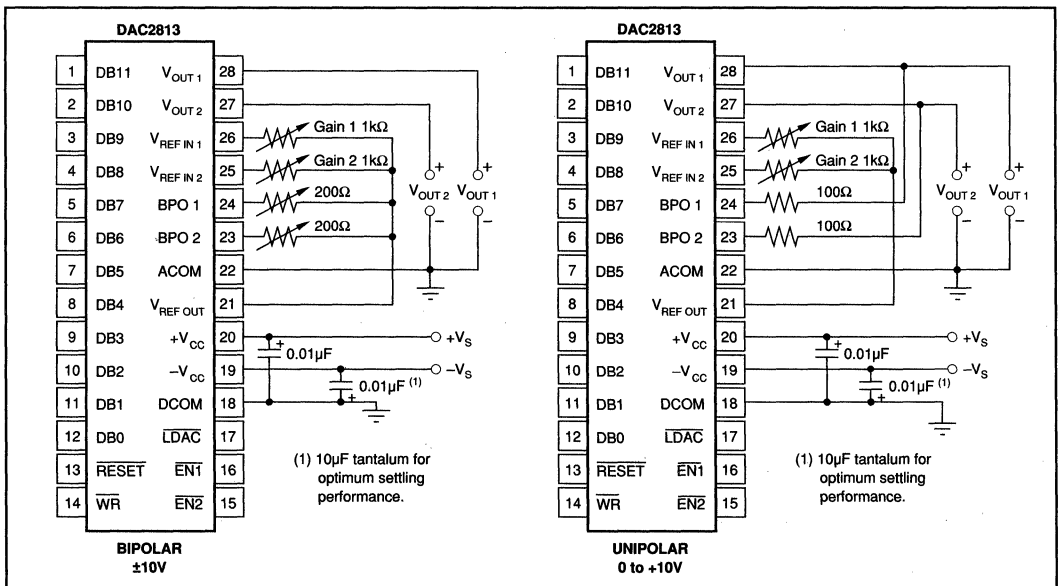
FIGURE 3. DAC2813 Power Supply, Output Range, Gain and Offset Adjust Connections. Unipolar output connected DAC2813s have Gain Adjust only.
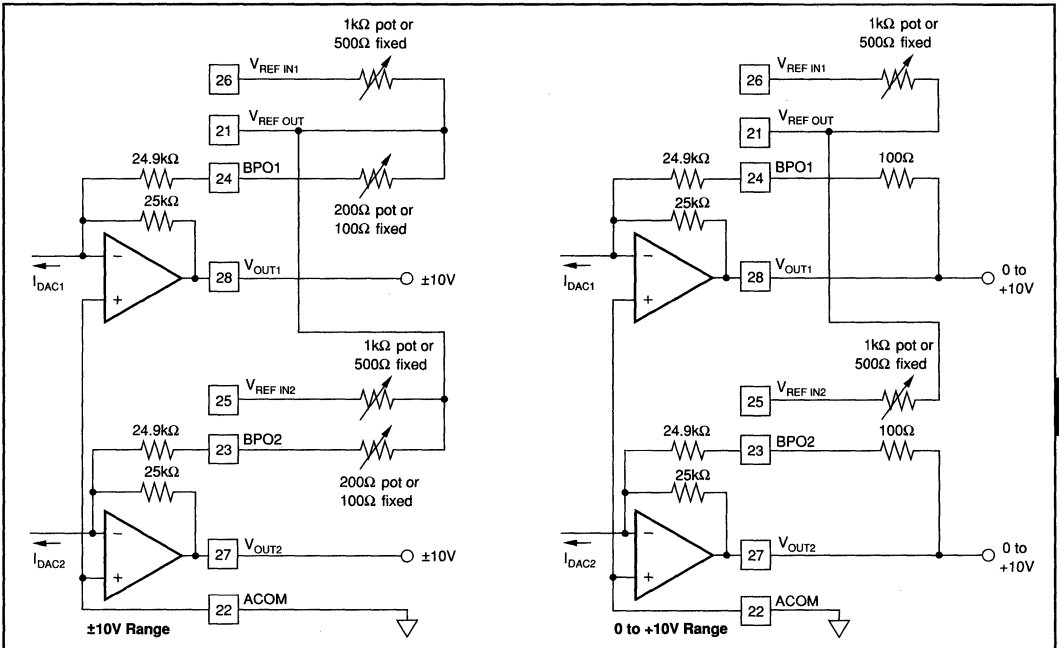
FIGURE 4. DAC2813 Output Amplifier Range Connnections.

DAC2813

DIGITAL-TO-ANALOG CONVERTERS 3

BURR - BROWN®

DAC2814

DUAL 12-BIT DIGITAL-TO-ANALOG
CONVERTER (Serial Interface)

FEATURES

- **COMPLETE DUAL DAC —**
  INCLUDES INTERNAL REFERENCES AND
  OUTPUT AMPLIFIERS
- **GUARANTEED SPECIFICATIONS OVER**
  TEMPERATURE
- **GUARANTEED MONOTONIC OVER**
  TEMPERATURE

- **HIGH-SPEED SERIAL INTERFACE**
  (10MHz CLOCK)
- **LOW POWER: 300mW (150mW/DAC)**
- **LOW GAIN DRIFT: 5ppm/°C**
- **LOW NONLINEARITY: ±1/2 LSB max**
- **UNIPOLAR OR BIPOLAR OUTPUT**
- **CLEAR/RESET TO UNIPOLAR OR**
  BIPOLAR ZERO

DESCRIPTION

The DAC2814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC2814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC B MSB first into a 24-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2814 is packaged in a 24-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.

PDS-1103B

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SPECIFICATIONS, Guaranteed over $T_A = -40°C$ to $+85°C$ unless otherwise specified.

ELECTRICAL

Specifications as shown for $V_S = ±12V$ or $±15V$, $V_L = +5V$, and $R_L = 2kΩ$ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2814AP MIN	DAC2814AP TYP	DAC2814AP MAX	DAC2814BP MIN	DAC2814BP TYP	DAC2814BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		+2		+5	*		*	V
V_{IL} (Input Low Voltage)		0		+0.8	*		*	V
I_{IN} (Input Current)	$T_A = 25°C$			±1			*	µA
	$T_A = -40°C$ to $+85°C$			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
DIGITAL OUTPUT								
Data Out V_{OL}	$I_{SINK} = 1.6mA$	0		+0.4	*		*	V
V_{OH}	$I_{SOURCE} = 500µA$	+2.4		+5	*		*	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	$T_A = 25°C$			±1			*	LSB
	$T_A = -40°C$ to $+85°C$		+1.5/-1				±1	LSB
Unipolar Offset Error	$T_A = +25°C$			±1			±0.5	mV
	$T_A = -40°C$ TO $+85°C$			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	$V_S = ±11.4V$ to $±18V$			30			*	ppmFSR/V
	$V_L = +4.5V$ to $+5.5V$							
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	$T_A = 25°C$	+10/-5			*			mA
	$T_A = -40°C$ to $+85°C$	+6.5/-5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
INVERTER								
-10V Reference[4], Inverter Output		-10.020	-10	-9.980	-10.015	*	-9.985	V
-10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$-V_S + 1.4$		$+V_S - 1.4$	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	$C_L = 100pF$							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±2			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	$C_L = 100pF$							
D/A GLITCH IMPULSE			30			*		nV-s

DAC2814

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DIGITAL-TO-ANALOG CONVERTERS

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2814AP			DAC2814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
+V_S and –V_S		±11.4	±15	±18	*	*	*	V
+V_L		4.5	5	5.5	*	*	*	V
+I_S			+10	+13.5		*	*	mA
–I_S			–10	–13.5		*	*	mA
+I_L	Digital Inputs = 0V or +V_L		0.2	1		*	*	mA
+I_L	Digital Inputs = V_{IL} or V_{IH}			5			*	mA
Total Power, All DACs			300	410		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to +V_{REF}. (5) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

+V_L to AGND	0V, +7V
+V_L to DGND	0V, +7V
+V_S to AGND	0V, +18V
–V_S to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, +V_L +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or ±V_S
Reference Short Circuit	Continuous to common or +V_S

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC2814AP	24-Pin Plastic DIP	167
DAC2814BP	24-Pin Plastic DIP	167

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	DGND	Digital common	24	CS	Chip select enable, DAC A and DAC B
2	LATCH B	Latch data update, logic input, DAC B	23	Data In	Serial data input
3	CLR	Asychronous input reset to zero	22	LATCH A	Latch data update, logic input, DAC A
4	MODE	Selection input for unipolar or bipolar reset to zero	21	CLK	Clock input
5	Data Out	Serial data output	20	NC	No internal connection
6	+V$_L$	Positive logic power supply, +5V input	19	BPO A	Bipolar offset input, DAC A
7	−V$_S$	Negative analog power supply, −15V input	18	BPO B	Bipolar offset input, DAC B
8	AGND	Analog common	17	V$_{OUT}$ B	Analog output voltage, DAC B
9	NC	No internal connection	16	+V$_{REF}$ Out	Reference voltage, +10V output
10	+V$_S$	Positive analog power supply, +15V input	15	Inv In	Inverter (A3) input
11	V$_{REF}$ In	± Reference voltage input	14	V$_{OUT}$ A	Analog output voltage, DAC A
12	Inv Out	Inverter (A3) output	13	NC	No internal connection

PIN CONFIGURATIONS

Top View

DGND	1		24	CS
LATCH B	2		23	Data In
CLR	3		22	LATCH A
MODE	4		21	CLK
Data Out	5		20	NC
+V$_L$	6	DAC2814	19	BPO A
−V$_S$	7		18	BPO B
AGND	8		17	V$_{OUT}$ B
NC	9		16	+V$_{REF}$ Out
+V$_S$	10		15	Inv In
V$_{REF}$ In	11		14	V$_{OUT}$ A
Inv Out	12		13	NC

NC = No Internal Connection

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

PSRR vs FREQUENCY (Bipolar Mode)

NOISE vs BANDWIDTH (Bipolar Mode)

DAC2814

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DIGITAL-TO-ANALOG CONVERTERS

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = ±12V$ or $±15V$, $V_L = +5V$ unless otherwise noted.

CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR
vs TEMPERATURE

POWER SUPPLY CURRENT vs TEMPERATURE

OUTPUT VOLTAGE SWING vs RESISTOR LOAD

CROSSTALK (Bipolar Mode)

NOTE: Crosstalk is dominated by digital crosstalk/
feedthrough of the $\overline{\text{LATCH}}$ signal.

FULL-SCALE OUTPUT SWING
BIPOLAR (20V Step)

FULL-SCALE OUTPUT SWING
UNIPOLAR (10V Step)

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)

Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)

Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)

Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)

Time (1µs/div)

MAJOR CARRY GLITCH

Time (1µs/div)
NOTE: Data transition 800$_{HEX}$ to 7FF$_{HEX}$.

DIGITAL FEEDTHROUGH

Time (500ns/div)
DAC output noise due to activity on digital inputs with latch disabled.

DAC2814

DIGITAL-TO-ANALOG CONVERTERS

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BB

TIMING CHARACTERISTICS

V_L = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$ or $\overline{LATCH\ B}$	15ns
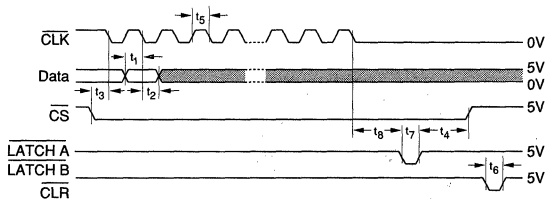
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V • t_R = t_F = 5ns.
(2) Timing measurement reference level is $\dfrac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	FUNCTION
X	1	↓	0	X	X	Data Clocked In
X	1	X	1	X	X	No Data Transfer
X	1	X	0	0	1	DAC A Register Updated
X	1	X	0	1	0	DAC B Register Updated
X	1	X	0	0	0	DAC A and DAC B Updated Together
0	0	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	Shift Registers Cleared = 000_{HEX}, DAC Registers = 800_{HEX}

NOTE: X = Don't care   ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM , DAC2814 — Dual, 12-bit DAC, Serial Port
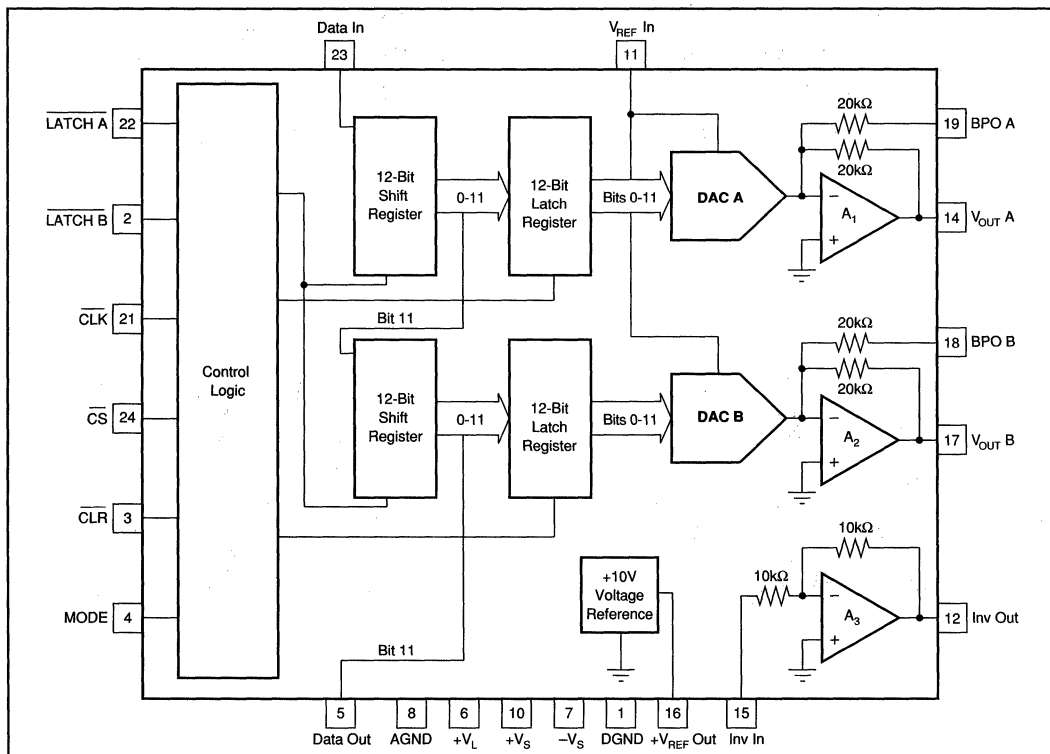
DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2814 are TTL and 5V CMOS compatible. Input codes for the DAC2814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 24-bit shift register. DAC B MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. Both $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream.

By using separate signals for $\overline{\text{LATCH A}}$ and $\overline{\text{LATCH B}}$, it is possible to update either one of the two DACs every 12 clock cycles.

When $\overline{\text{CLR}}$ is brought low, the input shift registers are cleared to 000_{HEX}, while the DAC registers = 800_{HEX}. If $\overline{\text{LATCH}}$ is brought low after $\overline{\text{CLR}}$, the DACs are updated with 000_{HEX} resulting in –10V (Bipolar) or 0V (Unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

FIGURE 1. Simplified Circuit Diagram of DAC Cell.

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FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2814 is specified for operation with power supplies of $V_L = +5V$ and $V_S =$ either $\pm 12V$ or $\pm 15V$. Even with the V_S supplies at $\pm 11.4V$ the DACs can swing a full $\pm 10V$. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = $-1.0V/V$) is provided to invert the +10V reference. Connect +V_{REF} Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC2814s can be connected to the same $\overline{CLK}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC2814s can be cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 24N $\overline{CLK}$ cycles may be required to update any given DAC, where N = number of DAC2814s.

Parallel Bus Connection

Several DAC2814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 24 $\overline{CLK}$ cycles.

FIGURE 3. Analog Connections for ±10V DAC Output.

FIGURE 4. Analog Connections for 0 to +10V DAC Output.

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FIGURE 5. Analog Connections for 0 to –10V DAC Output.

FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC packages.

FIGURE 7. Parallel Bus Connection for Multiple DAC packages.

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DAC2815

DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (8-Bit Port Interface)

FEATURES

- **COMPLETE DUAL DAC —** INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- **GUARANTEED SPECIFICATIONS OVER TEMPERATURE**
- **GUARANTEED MONOTONIC OVER TEMPERATURE**

- **HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE**
- **LOW POWER: 300mW (150mW/DAC)**
- **LOW GAIN DRIFT: 5ppm/°C**
- **LOW NONLINEARITY: ±1/2 LSB max**
- **UNIPOLAR OR BIPOLAR OUTPUT**
- **CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO**

DESCRIPTION

The DAC2815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC2815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.

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SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP MIN	TYP	MAX	DAC2815BP MIN	TYP	MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		2		5	*		*	V
V_{IL} (Input Low Voltage)		0		0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	μA
	T_A = –40°C to +85°C			±10			*	μA
C_{IN} (Input Capacitance)			0.8			*		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C TO +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V, V_L = +4.5V to +5.5V			30			*	ppmFSR/V
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+6.5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30		*	±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		–V_S + 1.4		+V_S – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	μs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	μs
Slew Rate			10			*		V/μs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±2			*		mA
DIGITAL CROSSTALK	Full Scale Transition C_L= 100pF		3			*		nV-s
D/A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP			DAC2815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
+V_S and –V_S		±11.4	±15	±18	*	*	*	V
+V_L		4.5	5	5.5	*	*	*	V
+I_S			+10	+13.5		*	*	mA
–I_S			–10	–13.5		*	*	mA
+I_L	Digital Inputs = 0V or +V_L		0.2	1		*	*	mA
+I_L	Digital Inputs = V_{IL} or V_{IH}			5			*	mA
Total Power, All DACs			300	410		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to +V_{REF}. (5) Guaranteed but not tested.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC2815AP	28-Pin Plastic DIP	215
DAC2815BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

+V_L to AGND	0V, +7V
+V_L to DGND	0V, +7V
+V_S to AGND	0V, +18V
–V_S to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, +V_L +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or ±V_S
Reference Short Circuit	Continuous to common or +V_S

ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC2815AP	±1
DAC2815BP	±1/2

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PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	D_6	Data bit 6 input	28	DGND	Digital common
2	D_7	Data bit 7 input	27	D_5	Data bit 5 input
3	A_0	Address 0 input	26	D_4	Data bit 4 input
4	A_1	Address 1 input	25	D_3	Data bit 3 input
5	$\overline{CLR}$	Asychronous input reset to zero	24	D_2	Data bit 2 input
6	MODE	Selection input for unipolar or bipolar reset to zero	23	D_1	Data bit 1 input
7	$\overline{CS}$	Chip select enable, DAC A and DAC B	22	D_0	Data bit 0 input
8	$-V_S$	Negative analog power supply, $-15V$ input	21	$\overline{WR}$	Write input, DAC A and DAC B
9	$\overline{LE}$	Latch data enable, DAC A and DAC B	20	BPO A	Bipolar offset input, DAC A
10	$+V_L$	Positive logic power supply, +5V input	19	BPO B	Bipolar offset input, DAC B
11	AGND	Analog common	18	Inv In	Inverter (A3) input
12	$+V_S$	Positive analog power supply, +15V input	17	$+V_{REF}$ Out	Reference voltage, +10V output
13	V_{REF} In	$\pm$ Reference voltage input	16	V_{OUT} A	Analog output voltage, DAC A
14	Inv Out	Inverter (A_3) output	15	V_{OUT} B	Analog output voltage, DAC B

PIN CONFIGURATION

Top View — DIP — DAC2815

D_6 — 1	28 — DGND
D_7 — 2	27 — D_5
A_0 — 3	26 — D_4
A_1 — 4	25 — D_3
$\overline{CLR}$ — 5	24 — D_2
MODE — 6	23 — D_1
$\overline{CS}$ — 7	22 — D_0
$-V_S$ — 8	21 — $\overline{WR}$
$\overline{LE}$ — 9	20 — BPO A
$+V_L$ — 10	19 — BPO B
AGND — 11	18 — Inv In
$+V_S$ — 12	17 — $+V_{REF}$ Out
V_{REF} In — 13	16 — V_{OUT} A
Inv Out — 14	15 — V_{OUT} B

TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm 12V$ or $\pm 15V$, $V_L = +5V$ unless otherwise noted.

PSRR vs FREQUENCY (Bipolar Mode)

NOISE vs BANDWIDTH (Bipolar Mode)

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR
vs TEMPERATURE
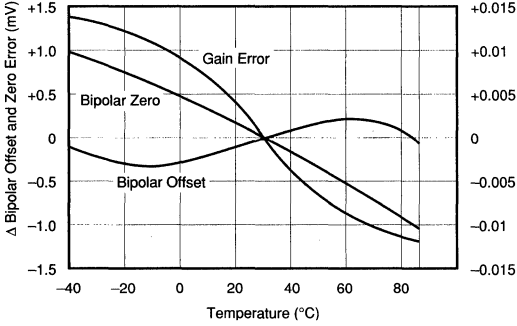
POWER SUPPLY CURRENT vs TEMPERATURE

OUTPUT VOLTAGE SWING vs RESISTOR LOAD

CROSSTALK (Bipolar Mode)

NOTE: Crosstalk is dominated by digital crosstalk/feedthrough of the $\overline{LE}$ signal.

FULL-SCALE OUTPUT SWING
BIPOLAR (20V Step)

FULL-SCALE OUTPUT SWING
UNIPOLAR (10V Step)

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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_S = ±12V$ or $±15V$, $V_L = +5V$ unless otherwise noted.

SETTLING TIME
BIPOLAR (−10V to +10V)

ΔV Around +10V (2mV/div)

Time (1μs/div)

SETTLING TIME
BIPOLAR (+10V to −10V Step)

ΔV Around −10V (2mV/div)

Time (2μs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)

ΔV Around −10V (1mV/div)

Time (1μs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)

ΔV Around +10V (1mV/div)

Time (1μs/div)

MAJOR CARRY GLITCH

V_{OUT} (20mV/div)

Time (1μs/div)
NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH

V_{OUT} (5mV/div)

Time (500ns/div)
DAC output noise due to activity on digital inputs
with latch disabled.

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TIMING CHARACTERISTICS

$+V_L = +5V$, $T_A = -40°C$ to $+85°C$.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	10ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{\text{LE}}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{\text{LE}}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns

NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F = 5$ns.

(2) Timing measurement reference level is $\dfrac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{\text{CLR}}$	$\overline{\text{LE}}$	$\overline{\text{CS}}$	$\overline{\text{WR}}$	A_1	A_0	FUNCTION
X	1	1	0	0	0	0	DAC A LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	0	1	DAC A MS Input Register Loaded with D3-(MSB)-D0
X	1	1	0	0	1	0	DAC B LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	1	1	DAC B MS Input Register Loaded with D3-(MSB)-D0
X	1	0	0	1	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
X	1	0	0	0	X	X	DAC A, DAC B Registers are Transparent
X	1	X	1	X	X	X	No Data Transfer
X	1	1	X	1	X	X	No Data Transfer
0	0	X	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	X	Input Registers Cleared = 000$_{\text{HEX}}$, DAC Registers = 800$_{\text{HEX}}$

NOTE: X = Don't care.

FUNCTIONAL BLOCK DIAGRAM, DAC2815 — Dual 12-bit DAC, 8-bit Port
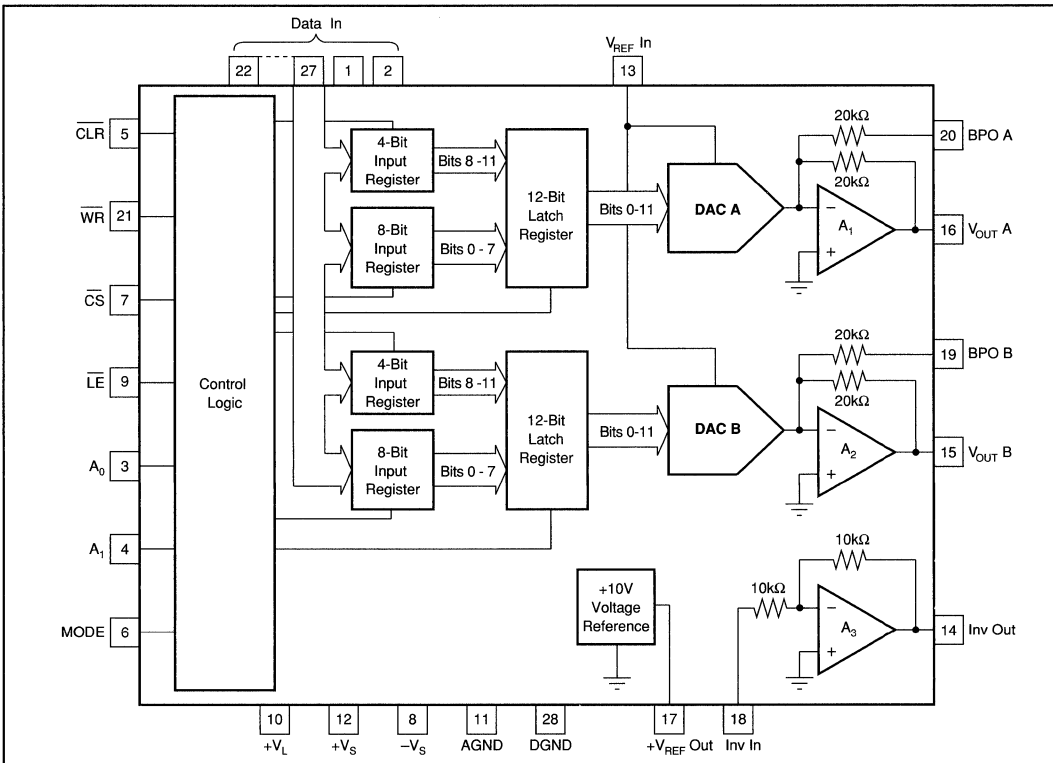
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DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2815 are TTL and 5V CMOS compatible. Input codes for the DAC2815 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in the unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. This data is latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bring $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. Both DACs are updated simultaneously.

When $\overline{CLR}$ is brought low, the input registers are cleared to 000_{HEX} (–10V), while the DAC registers = 800_{HEX}. If $\overline{LE}$ is brought low, the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of

FIGURE 1. Simplified Circuit Diagram of DAC Cell.
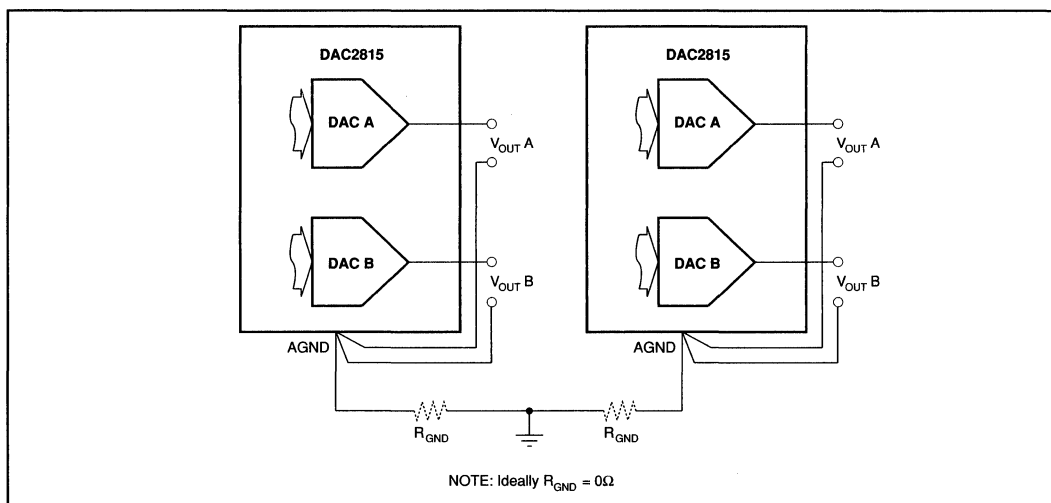
FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2815 is specified for operation with power supplies of $V_L = +5V$ and $V_S =$ either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1μF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect +V_{REF} Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2815 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2815 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2815 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

DAC2815s can easily be connected to a μprocessor bus. Decode your address lines to derive the control signals shown in Figure 6. Only one $\overline{LATCH}$ signal is required for a system where all DAC2815s are updated simultaneously. If you want to update DAC2815s independently, use separate $\overline{LATCH}$ signals. The $\overline{LATCH}$ and $\overline{WRITE}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

FIGURE 3. Analog Connections for ±10V DAC Output.
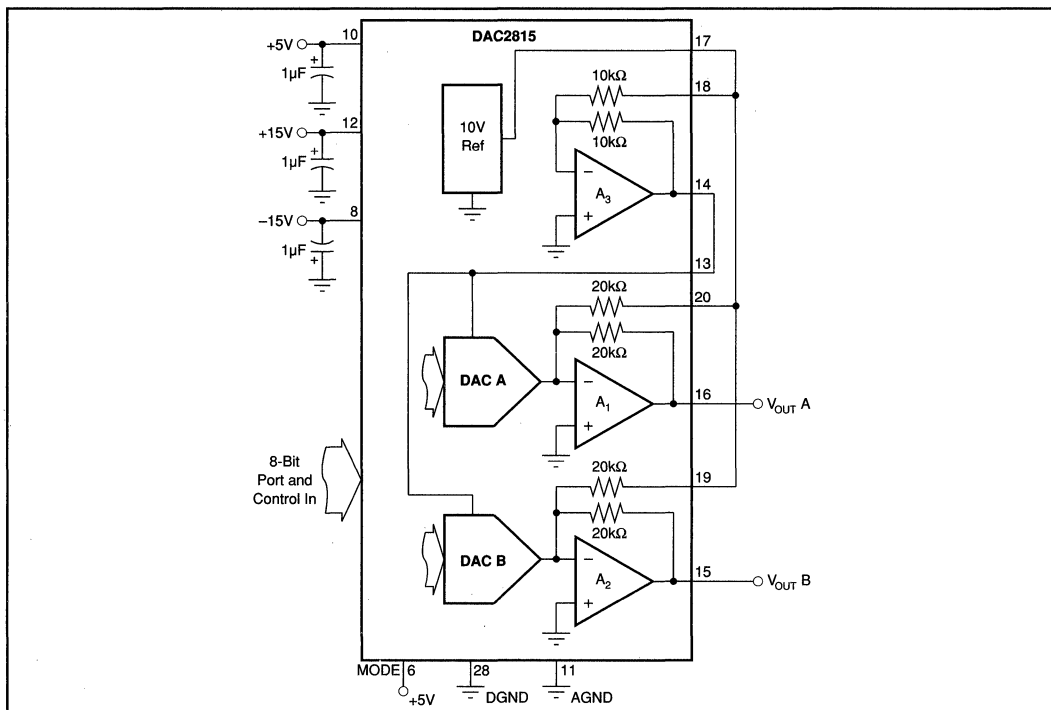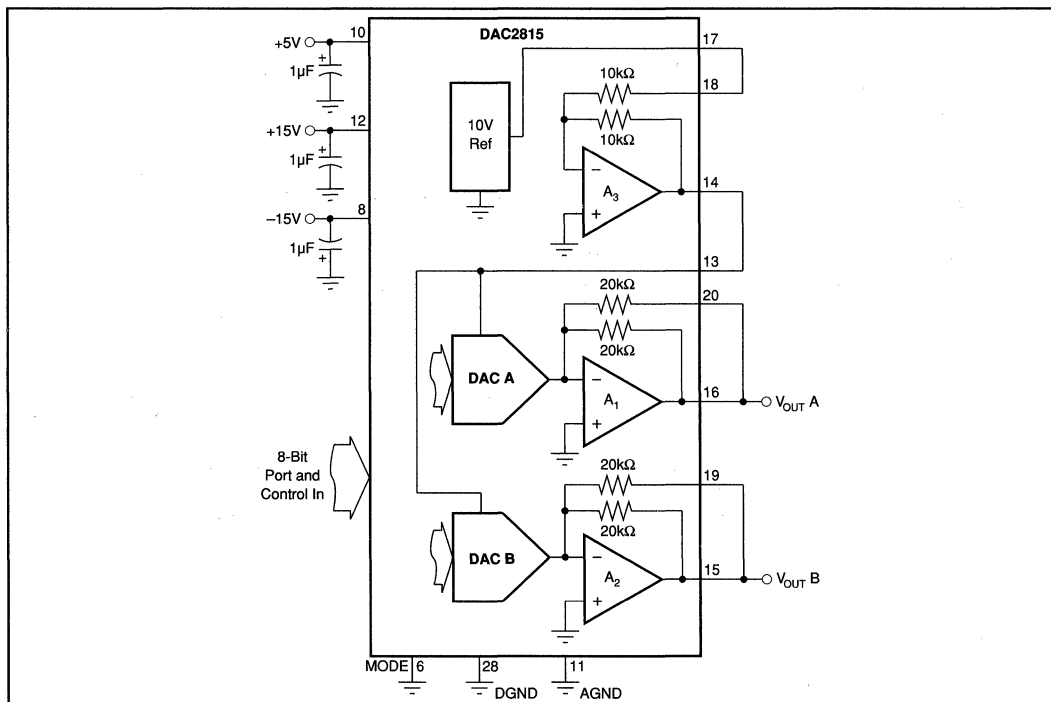
FIGURE 4. Analog Connections for 0 to +10V DAC Output.
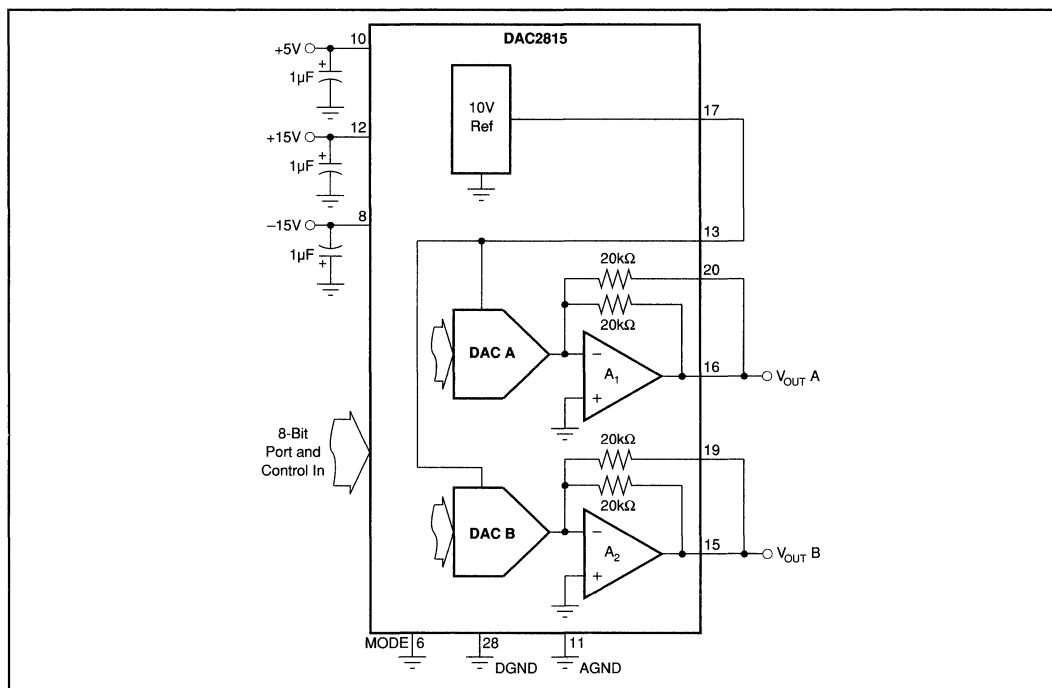
FIGURE 5. Analog Connections for 0 to –10V DAC Output.
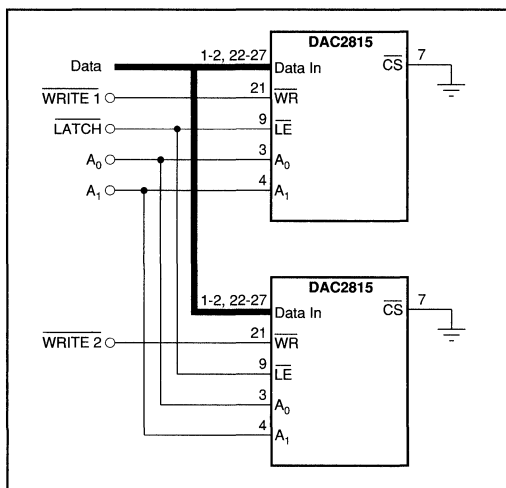
FIGURE 6. Logic Connection for Multiple DAC2815 Packages.

DAC2815

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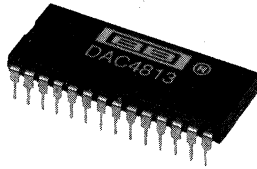
DAC4813

QUAD 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

FEATURES

● **COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS**
● **12-BIT PORT INTERFACE**
● **ANALOG OUTPUT RANGE: ±10V**

● **MONOTONICITY GUARANTEED OVER TEMPERATURE**
● **INTEGRAL LINEARITY ERROR: ±1/2LSB max**
● **±12V to ±15V SUPPLIES**
● **28-PIN PLASTIC DIP PACKAGE**

DESCRIPTION

DAC4813 is a complete quad 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asyn-

chronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC4813 D/A converters are committed to the ±10V output range only. Gain and offset are not externally adjustable.

DAC4813AP is available in one performance grade with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C.

PDS-1148B

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, +V_{CC} = +12V or +15V, −V_{CC} = −12V or −15V unless otherwise noted.

PARAMETER	CONDITIONS	DAC4813			UNITS
		MIN	TYP	MAX	
INPUTS					
DIGITAL INPUTS	Over Temperature				
Input Code [1]	Range		Bipolar Offset Binary		
Logic Levels [2]					
V_{IH} [3]		+2		+5.5	V
V_{IL}		0		+0.8	V
Logic Input Currents					
DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$, EN_x					
I_{IH}	V_I = +2.7V			±40	μA
I_{IL}	V_I = +0.4V			±40	μA
TRANSFER CHARACTERISTICS					
ACCURACY					
Linearity Error			±1/4	±1/2	LSB
Differential Linearity Error			±1/2	±1	LSB
Gain Error			±0.05	±0.2	%
Bipolar Zero Error [5]			±0.05	±0.2	%FSR [4]
Power Supply Sensitivity					
Of Full Scale +V_{CC}			±5	±20	ppmFSR/%+V_{CC}
−V_{CC}			±1	±10	ppmFSR/%−V_{CC}
DRIFT	Over Specification Temperature Range				
Gain			±5	±30	ppm/°C
Bipolar Zero Drift			±5	±15	ppmFSR/°C
Linearity Error over Temperature			±1/2	±3/4	LSB
Monotonicity			Guaranteed		
DYNAMIC CHARACTERISTICS					
SETTLING TIME [6]	To within ±0.012%FSR of Final Value 5kΩ ‖ 500pF Load				
Full Scale Range Change	20V Range		4.5	6	μs
1LSB Output Step [7] At Major Carry		2			μs
Slew Rate			10		V/μs
Crosstalk [8]	5kΩ Loads		0.2		LSB
OUTPUT					
Output Voltage Range	±V_{CC} ≥ ±11.4V			±10	V
Output Current		±5			mA
Output Impedance			0.2		Ω
Short Circuit to ACOM Duration	at DC		Indefinite		
REFERENCE VOLTAGE					
Voltage		+9.95	+10.00	+10.05	V
Source Current Available					
for External Loads		2			mA
Impedance			0.2		Ω
Temperature Coefficient			±5	±25	ppm/°C
Short Circuit to Common Duration	at DC		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: +V_{CC}		+11.4	+15	+16.5	V
−V_{CC}		−11.4	−15	−16.5	V
Current:	No Load ±V_{CC} = ±15V				
+V_{CC}			48	60	mA
−V_{CC}			24	28	mA
Power Dissipation			1080	1320	mW
Potential at DCOM with					
Respect to ACOM [9]		−3		+3	V
TEMPERATURE RANGES					
Specification		−40		+85	°C
Storage		−60		+100	°C
Thermal Resistance, θ_{JA}, Plastic DIP			30		°C/W

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Error at input code 800$_{HEX}$. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) For the worst-case code change: 7FF$_{HEX}$ to 800$_{HEX}$ and 800$_{HEX}$ to 7FF$_{HEX}$. (8) Crosstalk is defined as the change in any output as a result of any other output being driven from −10V to +10V at rated output current. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

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ABSOLUTE MAXIMUM RATINGS

```
+V_CC to ACOM ........................................................................ 0 to +18V
–V_CC to ACOM ........................................................................ 0 to –18V
+V_CC to –V_CC ........................................................................ 0 to +36V
ACOM to DCOM ................................................................................ ±4V
Digital Inputs to DCOM ........................................................ –1V to +V_CC
External Voltage applied to BPO Resistor ........................................ ±18V
V_REF OUT .............................................................. Indefinite short to ACOM
V_OUT ............................................................................ Momentary to ±18V
Lead Temperature, soldering 10s ................................................. +300°C
Max Junction Temperature ............................................................. 165°C
```

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
DAC4813AP	Plastic DIP	–40°C to +85°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC4813AP	28-Pin Plastic DBL Wide DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TIMING DIAGRAMS

WRITE CYCLE #1
(Load first rank from Data Bus: $\overline{LDAC}$ = 1)

WRITE CYCLE #2
(Load second rank from first rank: $\overline{EN}_X$ = 1)

TIMING DIAGRAMS (CONT)

RESET COMMAND (Bipolar Mode)
$\overline{EN}_X$, $\overline{LDAC}$, $\overline{WR}$ = Don't Care

TRUTH TABLE

$\overline{WR}$	$\overline{EN1}$	$\overline{EN2}$	$\overline{EN3}$	$\overline{EN4}$	$\overline{LDAC}$	RESET	OPERATION
X	X	X	X	X	X	0	Reset all D/A Latches
1	X	X	X	X	X	1	No Operation
X	1	1	1	1	1	1	No Operation
0	1	1	1	0	1	1	Load Data into First Rank for D/A 4
0	1	1	0	1	1	1	Load Data into First Rank for D/A 3
0	1	0	1	1	1	1	Load Data into First Rank for D/A 2
0	0	1	1	1	1	1	Load Data into First Rank for D/A 1
0	1	1	1	1	0	1	Load Second Rank from First Rank, All D/As
0	0	0	0	0	0	1	All Latches Transparent

"X" = Don't Care

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	DB11	DATA, MSB, positive true.
2	DB10	DATA
3	DB9	DATA
4	DB8	DATA
5	DB7	DATA
6	DB6	DATA
7	DB5	DATA
8	DB4	DATA
9	DB3	DATA
10	DB2	DATA
11	DB1	DATA
12	DB0	DATA, LSB.
13	$\overline{\text{RESET}}$	Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten by a $\overline{\text{LDAC}}$-$\overline{\text{WR}}$ command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state.
14	$\overline{\text{WR}}$	Write strobe. Must be low for data transfer to any latch (except RESET).
15	$\overline{\text{EN1}}$	Enable for 12-bit input data latch of D/A1. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
16	$\overline{\text{EN2}}$	Enable for 12-bit input data latch of D/A2. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
17	$\overline{\text{EN3}}$	Enable for 12-bit input data latch of D/A3. NOTE: This logic path is slower than the $\overline{\text{WR}}$ /path.
18	$\overline{\text{EN4}}$	Enable for 12-bit input data latch of D/A4. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
19	$\overline{\text{LDAC}}$	Load DAC enable. Must be low with $\overline{\text{WR}}$ for data transfer to the D/A latch and simultaneous update of all D/A converters.
20	DCOM	Digital common, logic currents return.
21	$-V_{CC}$	Analog supply input, nominally −12V or −15V referred to ACOM.
22	ACOM	Analog common, $+V_{CC}$, $-V_{CC}$ supply return.
23	$+V_{CC}$	Analog supply input, nominally +12V or +15V referred to ACOM.
24	$V_{OUT\,4}$	D/A 4 analog output.
25	$V_{OUT\,3}$	D/A 3 analog output.
26	$V_{OUT\,2}$	D/A 2 analog output.
27	$V_{OUT\,1}$	D/A 1 analog output.
28	$V_{REF\,OUT}$	+10V reference output.

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DIGITAL-TO-ANALOG CONVERTERS

BLOCK DIAGRAM

NOTE: $\overline{\text{RESET}}$ does not reset input latches.

TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = ±15V$ unless otherwise noted.

POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY

DIGITAL INPUT CURRENT vs INPUT VOLTAGE

CHANGE OF GAIN AND OFFSET ERROR
vs TEMPERATURE

INTEGRAL LINEARITY ERROR

± FULL SCALE OUTPUT SWING

MAJOR CARRY GLITCH

DAC4813

DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

SETTLING TIME, +10V TO –10V

SETTLING TIME, –10V TO +10V

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all "1s" and all "0s"). DAC4813 linearity error is ±1/2LSB max at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. DAC4813 is monotonic over their specification temperature range –40°C to +85°C.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Settling times are specified to ±0.01% of Full Scale Range (FSR) for two conditions: one for a FSR output change of 20V (25kΩ feedback) and one for a 1LSB change. The 1LSB change is measured at the Major Carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input code transition at which worst-case settling time occurs.

OPERATION

INTERFACE LOGIC

The bus interface logic of the DAC4813 consists of two independently addressable latches in two ranks for each D/A converter. The first rank consists of one 12-bit input latch which can be loaded directly from a 12- or 16-bit microprocessor/microcontroller bus. The input latch holds data temporarily before it is loaded into the second latch, the D/A latch. This double buffered organization permits simultaneous update of all D/As.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When the control signals return to logic "1", the data is latched.

CAUTION: DAC4813 was designed to use $\overline{WR}$ as the fast strobe. $\overline{WR}$ has a much faster logic path than $\overline{EN}_x$ (or $\overline{LDAC}$). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_x$ to strobe data into the latches, the DATA HOLD time will be long, approximately 20ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

RESET FUNCTION

The Reset function resets only the D/A latch. Therefore, after a RESET, good data must be written to **all** the input latches before an $\overline{LDAC} - \overline{WR}$ command is issued. Otherwise, old data or unknown data is present in the input latches and will be transferred to the D/A latch producing an analog output value that may be unwanted.

LOGIC INPUT COMPATIBILITY

DAC4813 digital inputs are TTL compatible (1.4V switching level) over the operating range of $+V_{CC}$. Each input has low leakage and high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC4813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition, the speed of the interface will be slower. A digital output driving a DATA input line of the DAC4813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

Unused control inputs should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available, the control inputs can be connected to $+V_{CC}$ through a 100kΩ resistor to limit the input current.

DIGITAL INPUT	DAC4813 RΩ
Data, $\overline{LDAC}$, $\overline{WR}$, $\overline{RESET}$	250
$\overline{EN}_x$	330
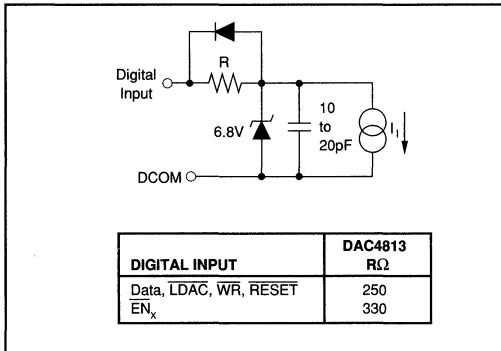
FIGURE 1. Equivalent Digital Input Circuit.

INPUT CODING

DAC4813 accepts positive-true binary input codes.

Input coding for bipolar analog outputs is Bipolar Offset Binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

DAC4813 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

INTERNAL/EXTERNAL REFERENCE USE

DAC4813 contains a +10V ±50mV voltage reference, $V_{REF\,OUT}$. $V_{REF\,OUT}$ is available to drive external loads sourcing up to 2mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the D/A converters will vary.

Because of the lack of additional pins required for external reference inputs, $V_{REF\,OUT}$ is connected internally to all 4 D/A converters. $V_{REF\,OUT}$ is available for external use on pin 28.

GAIN AND OFFSET ADJUSTMENTS

DAC4813 has no Gain and Offset Adjustment option.

INSTALLATION

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added. Best settling time performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be ale to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

DAC4813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both DIGITAL COMMON (DCOM) and ANALOG COMMON (ACOM) be connected directly to a ground plane under the package. If a ground place is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\,OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. The change in current in the ACOM pin due to an input date word change from 000_{HEX} to FFF_{HEX} is only 1mA for each D/A converter.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

DAC4813 output amplifiers provide a ±10V output swing while operating on supplies as low as ±12V ±5%.

DAC4813 is fully committed to ±10V output ranges. Optional ranges are not pin programmable.

12- AND 16-BIT BUS INTERFACES

DAC4813 data is latched into the input latches of each D/A by asserting low each $\overline{EN}x$ individually and transferring the data from the bus to each input latch by asserting $\overline{WR}$ low. All D/A outputs in each package are then updated simultaneously by asserting $\overline{LDAC}$ and $\overline{WR}$ low.

Be sure to read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

DAC4813

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DIGITAL-TO-ANALOG CONVERTERS

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DAC4814

Quad 12-Bit Digital-to-Analog Converter
(Serial Interface)

FEATURES

● **COMPLETE QUAD DAC —**
  INCLUDES INTERNAL REFERENCES AND
  OUTPUT AMPLIFIERS
● **GUARANTEED SPECIFICATIONS**
  OVER TEMPERATURE
● **GUARANTEED MONOTONIC OVER**
  TEMPERATURE
● **HIGH-SPEED SERIAL INTERFACE**
  (10MHz CLOCK)
● **LOW POWER: 600mW (150mW/DAC)**
● **LOW GAIN DRIFT: 5ppm/°C**
● **LOW NONLINEARITY: ±1/2 LSB max**
● **UNIPOLAR OR BIPOLAR OUTPUT**
● **CLEAR/RESET TO UNIPOLAR OR**
  BIPOLAR ZERO

DESCRIPTION

The DAC4814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC4814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC4814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC D MSB first into a 48-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC4814 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.

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SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP MIN	DAC4814AP TYP	DAC4814AP MAX	DAC4814BP MIN	DAC4814BP TYP	DAC4814BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		+2		+5	*		*	V
V_{IL} (Input Low Voltage)		0		+0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
DIGITAL OUTPUT								
Data Out V_{OL}	I_{SINK} = 1.6mA	0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5	*		*	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C to +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			*	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5				*		mA
	T_A = –40°C to +85°C	+6.5/–5				*		mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(Δ V_{OUT} vs Δ I_{LOAD})								
Supply Regulation				±5			*	ppm/V
(Δ V_{OUT} vs Δ V_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7				*		mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$-V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5				*		mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	C_L = 100pF							
D/A GLITCH IMPULSE			30			*		nV-s

DAC4814

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DIGITAL-TO-ANALOG CONVERTERS

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP			DAC4814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
+V_S and –V_S		±11.4	±15	±18	*	*	*	V
+V_L		4.5	5	5.5	*	*	*	V
+I_S			+20	+24		*	*	mA
–I_S			–20	–25.5		*	*	mA
+I_L	Digital Inputs = 0V or +V_L		0.4	2		*	*	mA
+I_L	Digital Inputs = V_{IL} or V_{IH}			10		*	*	mA
Total Power, All DACs			600	753		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to +V_{REF}. (5) Guaranteed to but not tested.

ABSOLUTE MAXIMUM RATINGS

```
+V_L to AGND ........................................................... 0V, +7V
+V_L to DGND ........................................................... 0V, +7V
+V_S to AGND ......................................................... 0V, +18V
–V_S to AGND ......................................................... 0V, –18V
AGND to DGND ........................................................... ±0.3V
Any digital input to DGND ............................... –0.3V, +V_L +0.3V
Ref In to AGND ............................................................ ±25V
Ref In to DGND ............................................................ ±25V
Storage Temperature Range ......................... –55°C to +125°C
Operating Temperature Range ........................ –40°C to +85°C
Lead Temperature (soldering, 10s) .............................. +300°C
Junction Temperature ................................................... +155°C
Output Short Circuit .................................. Continuous to common or ±V_S
Reference Short Circuit ............................. Continuous to common or +V_S
```

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC4814AP	28-Pin Plastic DBL Wide DIP	215
DAC4814BP	28-Pin Plastic DBL Wide DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	$+V_L$	Positive logic power supply, +5V input
2	V_{OUT} A	Analog output voltage, DAC A	27	$\overline{\text{LATCH A}}$	Latch data update, logic input, DAC A
3	Inv In	Inverter (A_5) input	26	$\overline{\text{LATCH B}}$	Latch data update, logic input, DAC B
4	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	25	MODE	Selection input for unipolar or bipolar reset to zero
5	BPO B	Biplolar offset input, DAC B	24	$\overline{\text{CLR}}$	Asynchronous input reset to zero
6	BPO A	Bipolar offset input, DAC A	23	$\overline{\text{CS}}$	Chip select enable, DAC A, B, C, and D
7	$-V_S$	Negative analog power supply , −15V input	22	Data In	Serial data input
8	BPO D	Bipolar offset input, DAC D	21	$\overline{\text{LATCH C}}$	Latch data update, logic input, DAC C
9	BPO C	Bipolar offset input, DAC C	20	$\overline{\text{LATCH D}}$	Latch data update, logic input, DAC D
10	V_{REF} In	± Reference voltage input	19	$\overline{\text{CLK}}$	Clock input
11	Inv Out	Inverter (A_5) output	18	Data Out	Serial data output
12	AGND	Analog common	17	DGND	Digital common
13	V_{OUT} D	Analog output voltage, DAC D	16	NC	No internal connection
14	V_{OUT} C	Analog output voltage, DAC C	15	$+V_S$	Positive analog power supply, +15V input

PIN CONFIGURATION

TOP VIEW

		DAC4814		
V_{OUT} B	1		28	$+V_L$
V_{OUT} A	2		27	$\overline{\text{LATCH A}}$
Inv In	3		26	$\overline{\text{LATCH B}}$
$+V_{REF}$ Out	4		25	MODE
BPO B	5		24	$\overline{\text{CLR}}$
BPO A	6		23	$\overline{\text{CS}}$
$-V_S$	7		22	Data In
BPO D	8		21	$\overline{\text{LATCH C}}$
BPO C	9		20	$\overline{\text{LATCH D}}$
V_{REF} In	10		19	$\overline{\text{CLK}}$
Inv Out	11		18	Data Out
AGND	12		17	DGND
V_{OUT} D	13		16	NC
V_{OUT} C	14		15	$+V_S$

NC = No Internal Connection

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

PSRR vs FREQUENCY (Bipolar Mode)

NOISE vs BANDWIDTH (Bipolar Mode)

DAC4814

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DIGITAL-TO-ANALOG CONVERTERS

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE

POWER SUPPLY CURRENT vs TEMPERATURE

OUTPUT VOLTAGE SWING vs RESISTOR LOAD

CROSSTALK (Bipolar Mode)

NOTE: Crosstalk is dominated by digital crosstalk/feedthrough of the LATCH signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (−10V to +10V)

ΔV Around +10V (2mV/div)

Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to −10V Step)

ΔV Around −10V (2mV/div)

Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)

ΔV Around 0V (1mV/div)

Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)

ΔV Around +10V (1mV/div)

Time (1µs/div)

MAJOR CARRY GLITCH

V_{OUT} (20mV/div)

Time (1µs/div)
NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH

V_{OUT} (5mV/div)

Time (500ns/div)
DAC output noise due to activity on digital inputs
with latch disabled.

DAC4814

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DIGITAL-TO-ANALOG CONVERTERS

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TIMING CHARACTERISTICS

$V_S = \pm 15V$, $V_L = +5V$, $T_A = -40°C$ to $+85°C$.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold Time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$, $\overline{LATCH\ B}$, $\overline{LATCH\ C}$, or $\overline{LATCH\ D}$	15ns
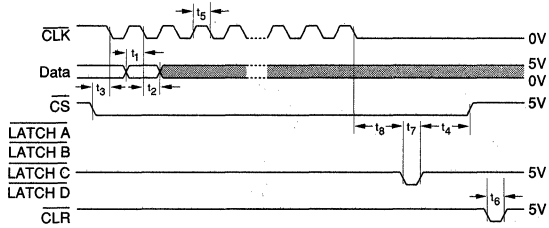
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V • $t_R = t_F = 5ns$.
(2) Timing measurement reference level is $\dfrac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	$\overline{LATCH\ C}$	$\overline{LATCH\ D}$	FUNCTION
X	1	↓	0	X	X	X	X	Data clocked in
X	1	X	1	X	X	X	X	No data transfer
X	1	X	0	0	1	1	1	DAC A register updated
X	1	X	0	1	0	1	1	DAC B register updated
X	1	X	0	1	1	0	1	DAC C register updated
X	1	X	0	1	1	1	0	DAC D register updated
X	1	X	0	0	0	0	0	All DAC registers updated simultaneously
0	0	X	X	X	X	X	X	All registers cleared
1	0	X	X	X	X	X	X	Shift registers cleared = 000_{HEX}, DAC registers = 800_{HEX}

Note: X = Don't Care.   ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM, DAC4814 — Quad 12-bit DAC, Serial Port
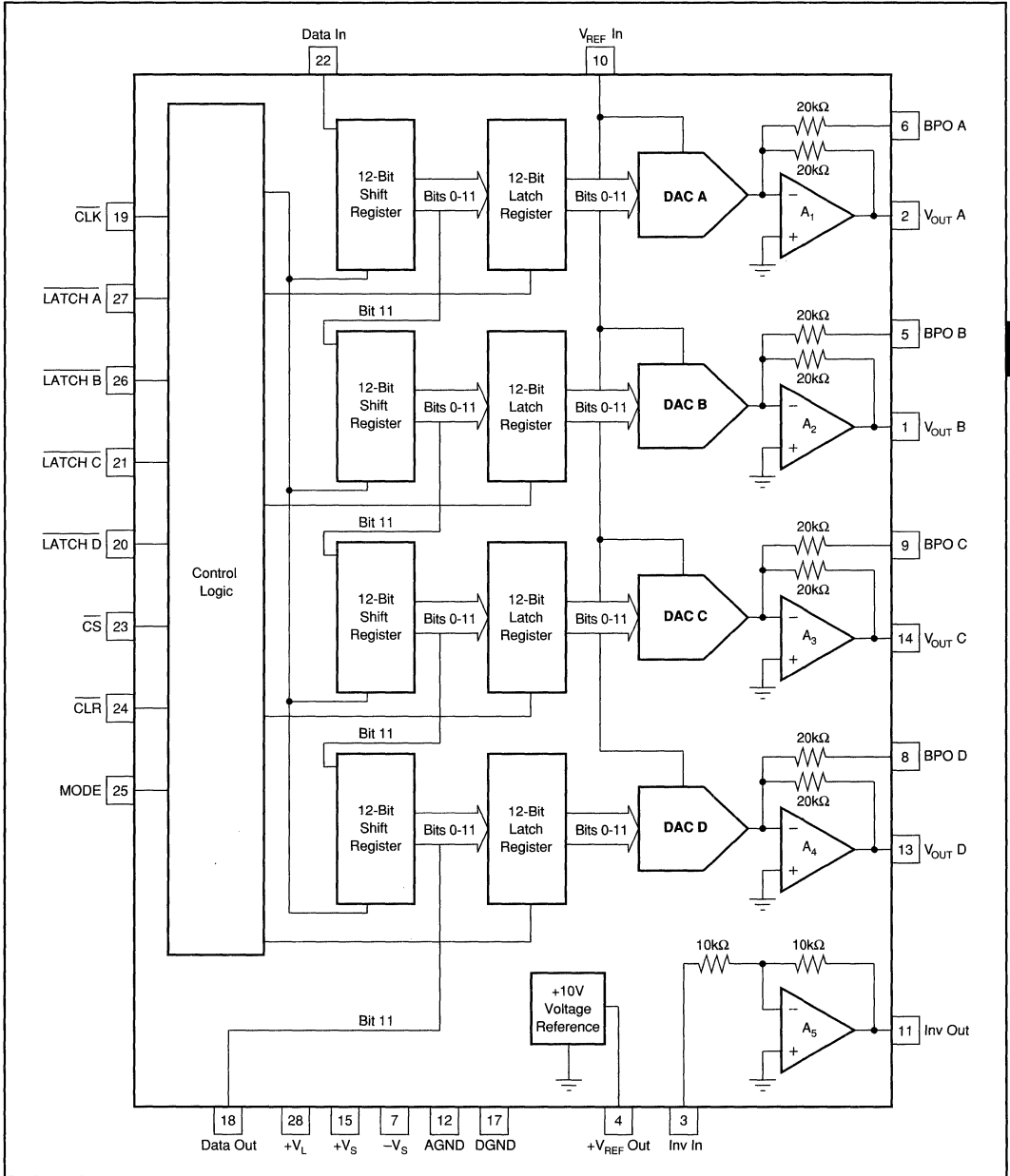
DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4814 are TTL and 5V CMOS compatible. Input codes for the DAC4814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 48-bit shift register. DAC D MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. All $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream. By using separate signals for $\overline{\text{LATCH A}}$, $\overline{\text{LATCH B}}$, $\overline{\text{LATCH C}}$, and $\overline{\text{LATCH D}}$ it is possible to update one of the four DACs every 12 clock cycles.

When $\overline{\text{CLR}}$ is brought low, the input shift registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX}. If $\overline{\text{LATCH}}$ is brought low after $\overline{\text{CLR}}$, the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

FIGURE 1. Simplified Circuit Diagram of DAC Cell.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC4814 is specified for operation with power supplies of $V_L = +5V$ and $V_S =$ either $\pm 12V$ or $\pm 15V$. Even with the V_S supplies at $\pm 11.4V$ the DACs can swing a full $\pm 10V$. Power supply decoupling capacitors (1μF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system

reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect +V_{REF} Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS
±10V Output Range

For a ±10V bipolar output connect the DAC4814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC4814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

DAC4814

DIGITAL-TO-ANALOG CONVERTERS

FIGURE 3. Analog Connections for ±10V DAC Output.
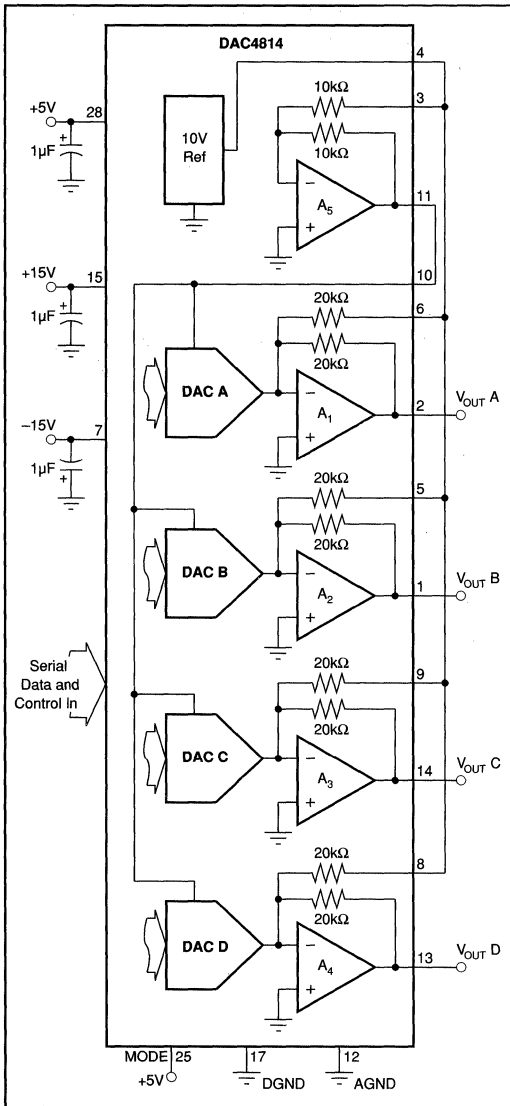
FIGURE 4. Analog Connections for 0 to +10V DAC Output.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC4814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC4814s can be connected to the same $\overline{\text{CLK}}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC4814s can be
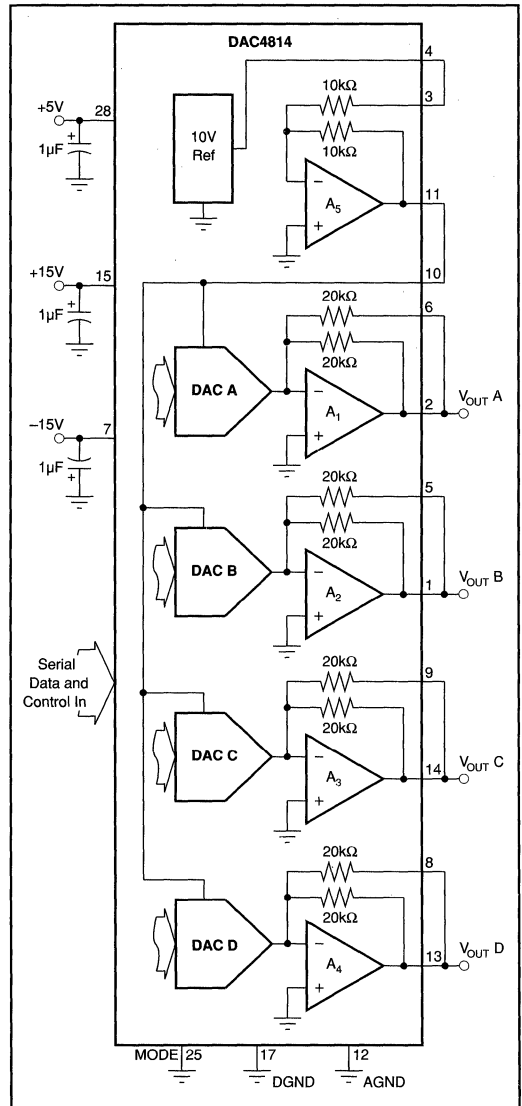
cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 48N $\overline{\text{CLK}}$ cycles may be required to update any given DAC, where N = number of DAC4814s.

Parallel Bus Connection

Several DAC4814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 48 $\overline{\text{CLK}}$ cycles.
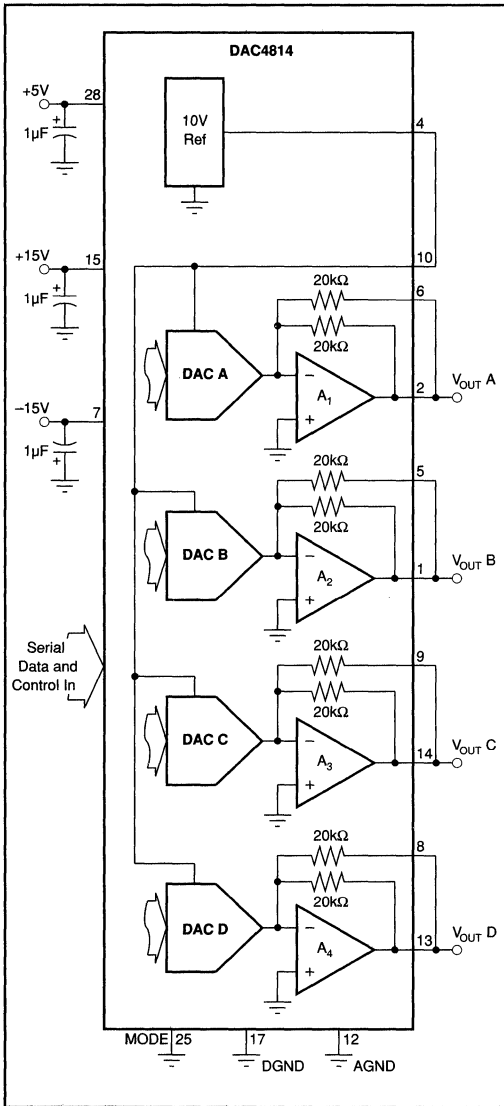
FIGURE 5. Analog Connections for 0 to –10V DAC Output.
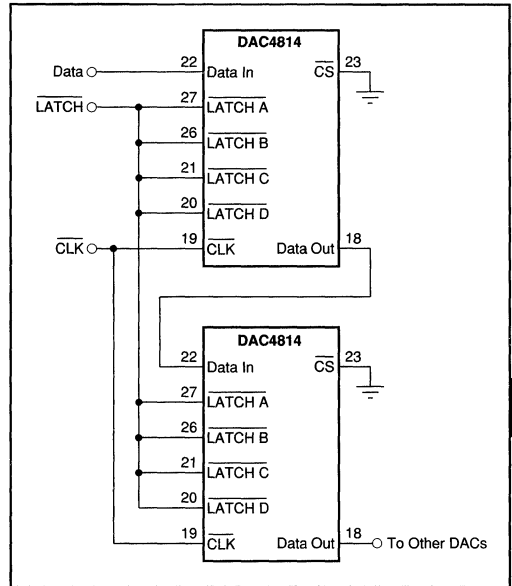
FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC Packages.
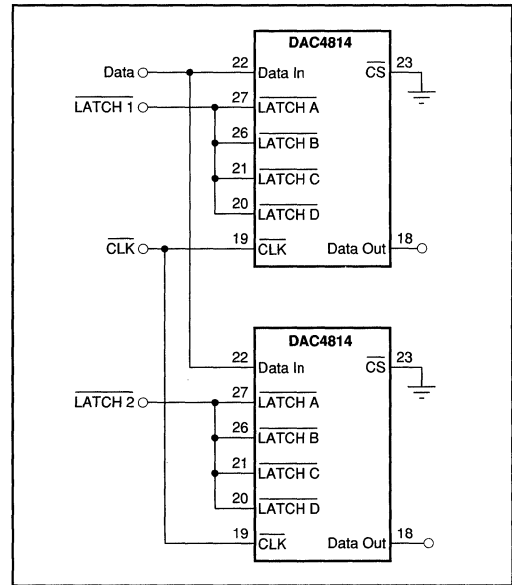
FIGURE 7. Parallel Bus Connection for Multiple DAC Packages.

DAC4814

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DIGITAL-TO-ANALOG CONVERTERS

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DAC4815

DAC4815

Quad 12-Bit Digital-to-Analog Converter
(8-Bit Port Interface)

FEATURES

- **COMPLETE QUAD DAC —**
  INCLUDES INTERNAL REFERENCES AND
  OUTPUT AMPLIFIERS
- **GUARANTEED SPECIFICATIONS**
  OVER TEMPERATURE
- **GUARANTEED MONOTONIC OVER**
  TEMPERATURE
- **HIGH-SPEED 8 + 4-BIT PARALLEL**
  INTERFACE
- **LOW POWER, 600mW (150mW/DAC)**
- **LOW GAIN DRIFT, 5ppm/°C**
- **LOW NONLINEARITY: ±1/2 LSB max**
- **BIPOLAR OUTPUT**
- **CLEAR/RESET TO BIPOLAR ZERO**

DESCRIPTION

The DAC4815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC4815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for bipolar ±10V output range.

The DAC4815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to bipolar zero. This feature is useful for power-on reset or system calibration. The DAC4815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.

PDS-1112B

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SPECIFICATIONS, Guaranteed over T$_A$ = –40°C to +85°C unless otherwise specified.

ELECTRICAL
Specifications as shown for V$_S$ = ±12V or ±15V, V$_L$ = +5V, and R$_L$ = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP MIN	TYP	MAX	DAC4815BP MIN	TYP	MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V$_{IH}$ (Input High Voltage)		2		5	*		*	V
V$_{IL}$ (Input Low Voltage)		0		0.8	*		*	V
I$_{IN}$ (Input Current)	T$_A$ = 25°C			±1			*	µA
	T$_A$ = –40°C to +85°C			±10			*	µA
C$_{IN}$ (Input Capacitance)			0.8			*		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T$_A$ = 25°C			±1			*	LSB
	TA = –40°C to +85°C	±1.5/–1					±1	LSB
Bipolar Zero Error			±20					mV
Gain Error	With Internal or External 10.0V Ref			±0.2		±10	±0.15	%
Power Supply Sensitivity[3]	V$_S$ = ±11.4V to ±18V			30			*	ppmFSR/V
	V$_L$ = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift			±5	±30		*	±20	ppm/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T$_A$ = 25°C	+10/–5			*			mA
	T$_A$ = –40°C to +85°C	+5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(Δ V$_{OUT}$ vs Δ I$_{LOAD}$)								
Supply Regulation				±5			*	ppm/V
(Δ V$_{OUT}$ vs Δ V$_S$)								
–REFERENCE OUTPUT, Inverter								
–10V Reference		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		3.5	5		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		–V$_S$ + 1.4		+V$_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V$_{OUT}$		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[4]	C$_L$ = 100pF							
Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	C$_L$ = 100pF							
DIGITAL-TO-ANALOG								
GLITCH IMPULSE			30			*		nV-s
POWER SUPPLY								
+V$_S$ and –V$_S$		±11.4	±15	±18	*	*	*	V
+V$_L$		4.5	5	5.5	*	*	*	V
+I$_S$			+20	+24		*	*	mA
–I$_S$			–20	–25.5		*	*	mA
+I$_L$	Digital Inputs = 0V or +V$_L$		0.4	2		*	*	mA
+I$_L$	Digital Inputs = V$_{IL}$ or V$_{IH}$			10		*	*	mA
Total Power, All DACs			600	753		*	*	mW

DAC4815

DIGITAL-TO-ANALOG CONVERTERS

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SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes effect of voltage output DAC, voltage references. (4) Guaranteed but not tested.

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	A_2	Address line 2 input
2	V_{OUT} A	Analog output voltage, DAC A	27	A_1	Address line 1 input
3	$-V_{REF}$ Out	Negative reference voltage output (–10V output)	26	A_0	Address line 0 input
4	V_{REF} In	± Reference voltage input	25	D_7	Data bit 7 input
5	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	24	D_6	Data bit 6 input
6	BPO	Bipolar offset input, DAC A, B, C, and D	23	D_5	Data bit 5 input
7	$-V_S$	Negative analog power supply, –15V input	22	D_4	Data bit 4 input
8	$+V_S$	Positive analog power supply, +15V input	21	D_3	Data bit 3 input
9	AGND	Analog common	20	D_2	Data bit 2 input
10	DGND	Digital common	19	D_1	Data bit 1 input
11	$+V_L$	Positive logic power supply, +5V input	18	D_0	Data bit 0 input
12	V_{OUT} D	Analog output voltage, DAC D	17	$\overline{LE}$	Latch data enable, DAC A, B, C, and D
13	V_{OUT} C	Analog output voltage, DAC C	16	$\overline{CS}$	Chip select enable, DAC A, B, C, and D
14	$\overline{CLR}$	Asynchronous input reset to zero	15	$\overline{WR}$	Write input, DAC A, B, C, and D

PIN CONFIGURATIONS

Top View

		DAC4815		
V_{OUT} B	1		28	A_2
V_{OUT} A	2		27	A_1
$-V_{REF}$ Out	3		26	A_0
V_{REF} In	4		25	D_7
$+V_{REF}$ Out	5		24	D_6
BPO	6		23	D_5
$-V_S$	7		22	D_4
$+V_S$	8		21	D_3
AGND	9		20	D_2
DGND	10		19	D_1
$+V_L$	11		18	D_0
V_{OUT} D	12		17	$\overline{LE}$
V_{OUT} C	13		16	$\overline{CS}$
$\overline{CLR}$	14		15	$\overline{WR}$

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND .... 0V, +7V
$+V_L$ to DGND .... 0V, +7V
$+V_S$ to AGND .... 0V, +18V
$-V_S$ to AGND 0V,–18V
AGND to DGND .... ±0.3V
Any digital input to GND .... –0.3V, $+V_L$ +0.3V
Ref In to AGND .... ±25V
Ref In to DGND .... ±25V
Storage Temperature Range .... –55°C to +125°C
Operating Temperature Range .... –40°C to +85°C
Lead Temperature (soldering, 10s) .... +300°C
Junction Temperature .... +155°C
Output Short Circuit .... Continuous to common or ±V_S
Reference Short Circuit .... Continuous to common or +V_S

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC4815AP	±1
DAC4815BP	±1/2

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC4815AP	28-Pin Plastic DIP	215
DAC4815BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

PSRR vs FREQUENCY (Bipolar Mode)

V_{OUT} = 0V

V_{OUT} = +10V

NOISE vs BANDWIDTH (Bipolar Mode)

V_{OUT} = +10V
FFF_{HEX}

V_{OUT} = 0V
800_{HEX}

CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE

Gain Error

Bipolar Zero

Bipolar Offset

POWER SUPPLY CURRENT vs TEMPERATURE

$+I_L$ (All Logic Inputs = 2V)

I_S

$+I_L$ (All Logic Inputs = 0V or V_L)

OUTPUT VOLTAGE SWING vs RESISTOR LOAD

V_S = ±15V
V_L = 5V

10V REF

CROSSTALK (Bipolar Mode)

0V

+5V

0V

V_{OUT} B

V_{OUT} A

$\overline{LE}$

Time (500ns/div)
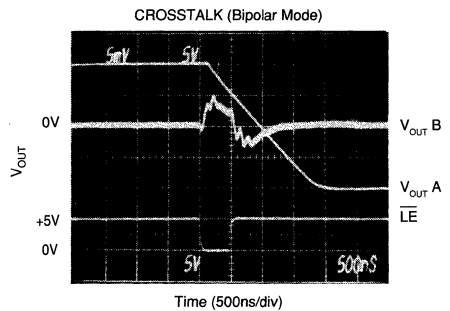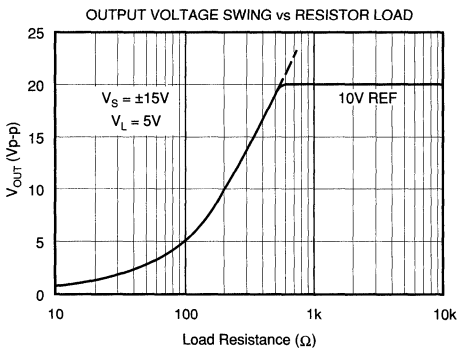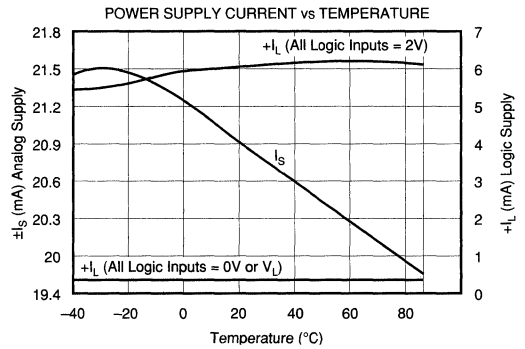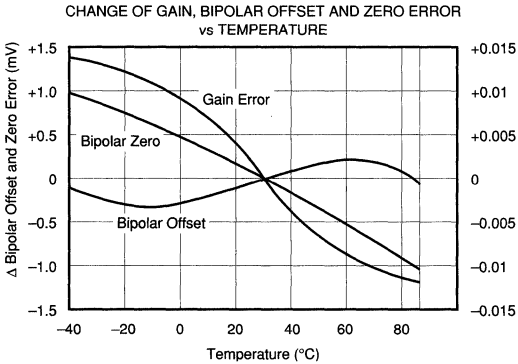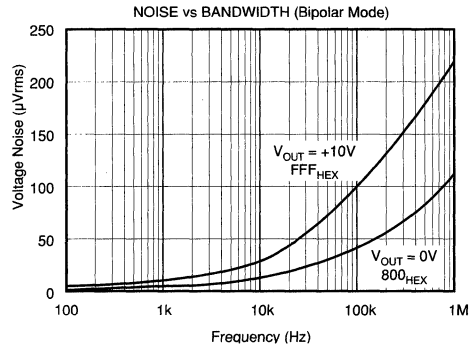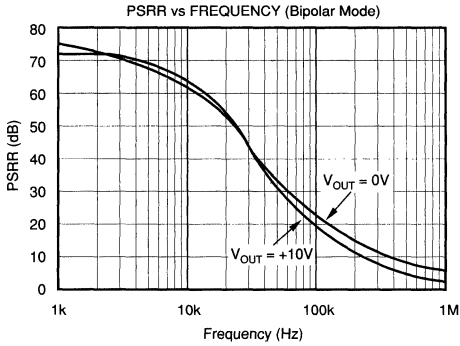
NOTE: Crosstalk is dominated by digital crosstalk/feedthrough of $\overline{LE}$ signal.

DAC4815

3

DIGITAL-TO-ANALOG CONVERTERS

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

FULL-SCALE OUTPUT SWING
BIPOLAR (20V Step)

Time (2µs/div)

SETTLING TIME
BIPOLAR (–10V to +10V)

Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)

Time (2µs/div)

MAJOR CARRY GLITCH

Time (1µs/div)

NOTE: Data transition 800$_{HEX}$ to 7FF$_{HEX}$.

DIGITAL FEEDTHROUGH

Time (500ns/div)

DAC output noise due to activity on digital inputs
with latch disabled.

BURR - BROWN®
BB

FUNCTIONAL BLOCK DIAGRAM, DAC4815 — Quad 12-bit DAC, 8-bit Port

TIMING CHARACTERISTICS

$+V_L = +5V$, $T_A = -40°C$ to $+85°C$.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	20ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns

NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F = 5ns$.

(2) Timing measurement reference level is $\dfrac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_2	A_1	A_0	FUNCTION
1	1	0	0	0	0	0	DAC A LS input register loaded with D7-D0(LSB)
1	1	0	0	0	0	1	DAC A MS input register loaded wtih D3(MSB)-D0
1	1	0	0	0	1	0	DAC B LS input register loaded with D7-D0(LSB)
1	1	0	0	0	1	1	DAC B MS input register loaded with D3(MSB)-D0
1	1	0	0	1	0	0	DAC C LS input register loaded with D7-D0(LSB)
1	1	0	0	1	0	1	DAC C MS input register loaded with D3(MSB)-D0
1	1	0	0	1	1	0	DAC D LS input register loaded with D7-D0(LSB)
1	1	0	0	1	1	1	DAC D MS input register loaded with D3(MSB)-D0
1	0	0	1	X	X	X	All DAC registers updated simultaneously from input registers
1	0	0	0	X	X	X	All DAC registers are transparent
1	X	1	X	X	X	X	No data transfer
1	1	X	1	X	X	X	No data transfer
0	X	X	X	X	X	X	Input registers cleared = 000_{HEX}, DAC registers = 800_{HEX}

NOTE: X = Don't care.

DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4815 are TTL and 5V CMOS compatible. Input codes for the DAC4815 are BOB (Bipolar Offset Binary). See Figure 3 for ±10V bipolar connection.

BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	BIPOLAR (BOB)
FFF_{HEX}	+Full Scale
800_{HEX}	Zero
$7FF_{HEX}$	Zero – 1 LSB
000_{HEX}	–Full Scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX}.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. The data are latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bringing $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. All DACs are updated simultaneously.

When $\overline{CLR}$ is brought low, the input registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX}. If $\overline{LE}$ is brought low after $\overline{CLR}$ the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or OV (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a –10V reference are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

FIGURE 1. Simplified Circuit Diagram of DAC Cell.

POWER SUPPLY CONNECTIONS

The DAC4815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

±10V OUTPUT RANGE CONNECTION

For a ±10V bipolar output connect the DAC4815 as shown in Figure 3.

CONNECTION TO DIGITAL BUS

DAC4815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 4. Only one $\overline{LATCH}$ signal is required for a system where all DAC4815s are updated simultaneously. If your want to update DAC4815s independently, use separate $\overline{LATCH}$ signals. The $\overline{LATCH}$ and $\overline{WRITE}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

DAC4815

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DIGITAL-TO-ANALOG CONVERTERS
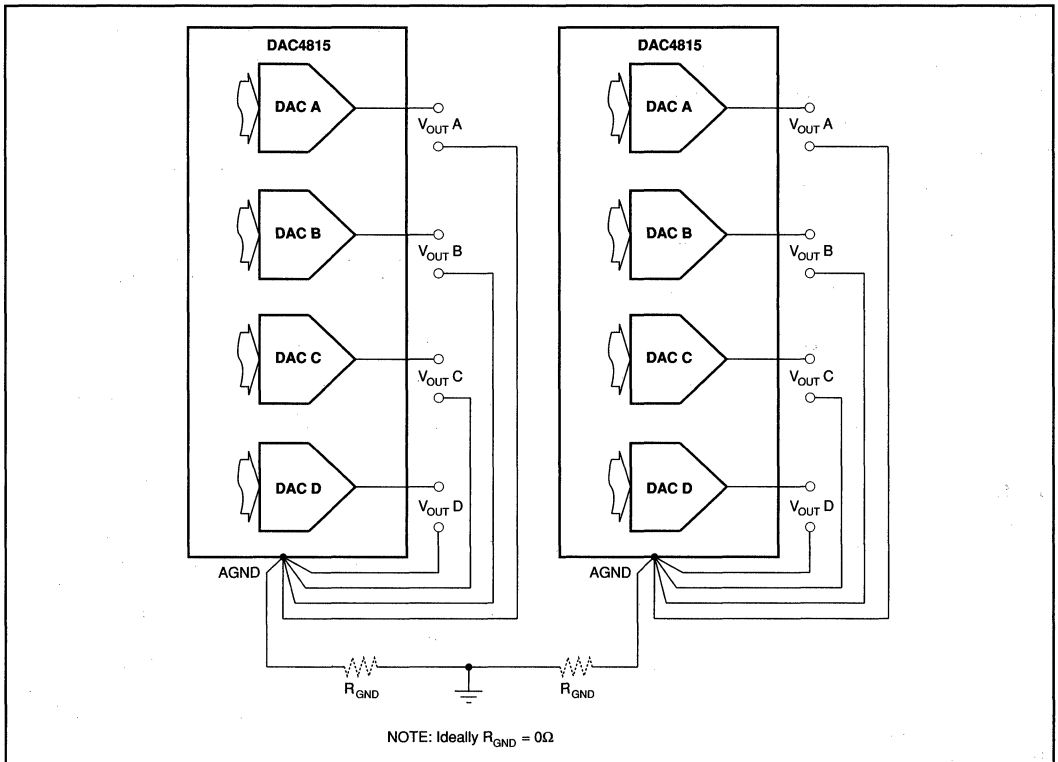
FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.
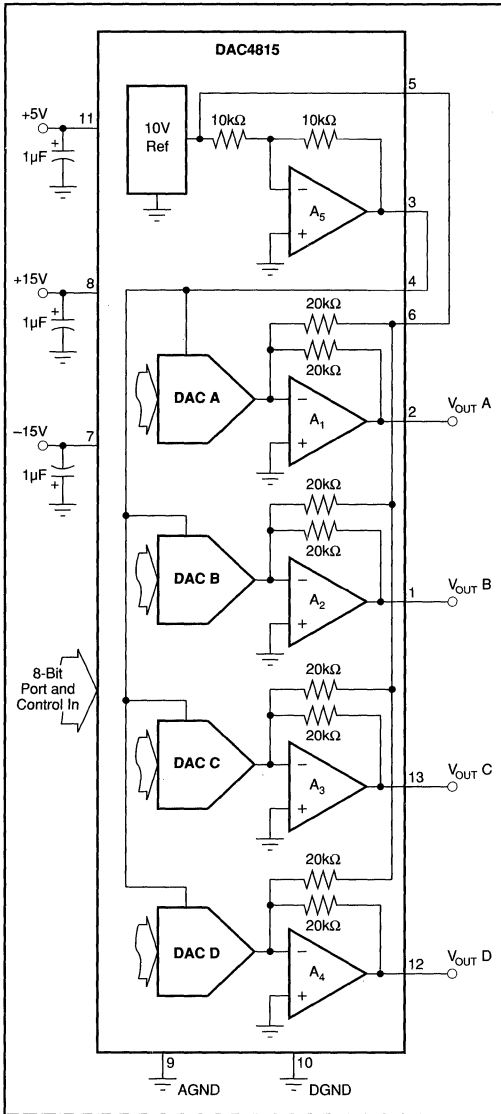
FIGURE 3. Analog Connections for ±10V DAC Output.
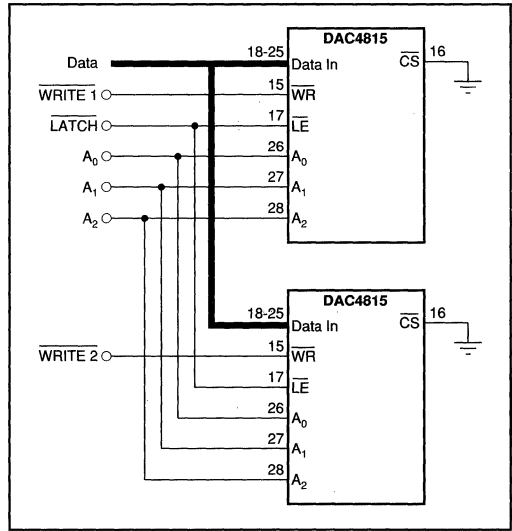
FIGURE 4. Logic Connections for Multiple DAC4815 Packages.

DAC4815

DIGITAL-TO-ANALOG CONVERTERS

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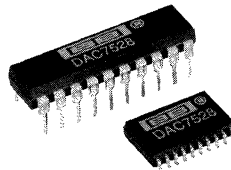
DAC7528

CMOS Dual 8-Bit Buffered Multiplying
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **DOUBLE BUFFERED DATA LATCHES**
● **SINGLE 5V SUPPLY OPERATION**
● **±1/2 LSB LINEARITY**
● **FOUR-QUADRANT MULTIPLICATION**
● **DACs MATCHED TO 1%**

APPLICATIONS

● **DIGITALLY CONTROLLED FILTERS**
● **DISK DRIVES**
● **AUTO CALIBRATION**
● **MOTOR CONTROL SYSTEMS**
● **PROGRAMMABLE GAIN/ATTENUATION**
● **X-Y GRAPHICS**

DESCRIPTION

The DAC7528 contains two, 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors.

Each DAC operates independently with separate reference input pins and internal feedback resistors. Excellent converter-to-converter matching is maintained.

The DAC7528 operates from a single +5V power supply. The inputs are TTL-compatible. Package options include 20-pin plastic DIP and SOIC.

PDS-1219A

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SPECIFICATIONS

ELECTRICAL

At $V_{DD} = +5V$; $V_{REFA, B} = +10V$; $I_{OUT} = GND = 0V$; T = Full Temperature Range specification under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC7528P, U MIN	DAC7528P, U TYP	DAC7528P, U MAX	DAC7528PB, UB MIN	DAC7528PB, UB TYP	DAC7528PB, UB MAX	UNITS
DC ACCURACY [1]									
Resolution	N		8			8			Bits
Relative Accuracy	INL				±1			±1/2	LSB
Differential Nonlinearity	DNL	Guaranteed Monolithic Over Temp			±1			±1/2	LSB
FS Gain Error [2]		$T_A = +25°C$			±2			±1	LSB
		$T_A = T_{MIN}$ to T_{MAX}			±4			±2	LSB
Gain Tempco [2][3]				±2	±35		−	−	ppm/°C
Supply Rejection	PSR	$\Delta V_{DD} = ±5\%$, $T_A = +25°C$		0.001	0.01		−	−	%FSR/%
		$T_A = T_{MIN}$ to T_{MAX}		0.001	0.01		−	−	%FSR/%
Output Leakage Current (OUTA)		$DACA = 00_{16}$, $T_A = +25°C$			±50			−	nA
		$T_A = T_{MIN}$ to T_{MAX}			±200			−	nA
Output Leakage Current (OUTB)		$DACB = 00_{16}$, $T_A = +25°C$			±50			−	nA
		$T_A = T_{MIN}$ to T_{MAX}			±200			−	nA
REFERENCE INPUT									
Input Resistance		(V_{REFA}, V_{REFB})	8	10	15	−	−	−	kΩ
Input Resistance Match		(V_{REFA}, V_{REFB})			±1			−	%
DYNAMIC PERFORMANCE [4]									
Output Current Settling Time to 1/2 LSB		Enable Pins Low $T_A = +25°C$			180			−	ns
		Load = 100Ω/13pF, $T_A = T_{MIN}$ to T_{MAX}			200			−	ns
Digital-to-Analog Propagation Delay		Enable Pins Low $T_A = +25°C$			80			−	ns
to 90% of Output		Load = 100Ω/13pF, $T_A = T_{MIN}$ to T_{MAX}			100			−	ns
Digital-to-Analog Impulse				125			−		nVs
AC Feedthrough		$V_{REFA} = 20Vpp$ Sinewave, $T_A = +25°C$			−70				dB
(V_{REFA} to OUTA)		100kHz, $V_{REFB} = 0V$, $T_A = T_{MIN}$ to T_{MAX}			−65				dB
AC Feedthrough		$V_{REFB} = 20Vpp$ Sinewave, $T_A = +25°C$			−70				dB
(V_{REFB} to OUTB)		100kHz, $V_{REFB} = 0V$, $T_A = T_{MIN}$ to T_{MAX}			−65				dB
Channel-to-Channel Isolation		$V_{REFA} = 20Vpp$ Sinewave, 100kHz,		−90			−		dB
(V_{REFA} to OUTB)		$V_{REFB} = 0V$, Both DACs = FF_{16}							
Channel-to-Channel Isolation		$V_{REFB} = 20Vpp$ Sinewave 100kHz,		−90			−		dB
(V_{REFB} to OUTA)		$V_{REFA} = 0V$, Both DACs = FF_{16}							
Digital Crosstalk		Measured With Code Transition 00_{16} to FF_{16}		30			−		nVs
Harmonic Distortion	THD	$V_{IN} = 6Vrms$ at 1kHz		−85			−		dB
ANALOG OUTPUTS [4]									
OUTA capacitance	C_{OUTA}	$DAC = 00_{16}$			50			−	pF
		$DAC = FF_{16}$			120			−	pF
OUTB capacitance	C_{OUTB}	$DAC = 00_{16}$			50			−	pF
		$DAC = FF_{16}$			120			−	pF
DIGITAL INPUTS									
Input High Voltage	V_{IH}		2.4			−			V
Input Low Voltage	V_{IL}				0.8			−	V
Input Current	I_{IN}	$T_A = +25°C$			±1			−	μA
		$T_A = T_{MIN}$ to T_{MAX}			±10			−	μA
Input Capacitance [4]	C_{IN}	All Digital Inputs			10			−	pF
POWER REQUIREMENTS									
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}, $T_A = +25°C$			1			−	mA
		$T_A = T_{MIN}$ to T_{MAX}			1			−	mA
		Digital Inputs = 0V or V_{DD}, $T_A = +25°C$			100			−	μA
		$T_A = T_{MIN}$ to T_{MAX}			500			−	μA
SWITCHING CHARACTERISTICS (100% tested) See Timing Diagram									
Chip Select To Write Setup Time	t_{CS}	$T_A = +25°C$	200			−			ns
		$T_A = T_{MIN}$ to T_{MAX}	230			−			ns
Chip Select To Write Hold Time	t_{CH}	$T_A = +25°C$	20			−			ns
		$T_A = T_{MIN}$ to T_{MAX}	30			−			ns
DAC Select To Write Setup Time	t_{AS}	$T_A = +25°C$	200			−			ns
		$T_A = T_{MIN}$ to T_{MAX}	230			−			ns
DAC Select To Write Hold Time	t_{AH}	$T_A = +25°C$	20			−			ns
		$T_A = T_{MIN}$ to T_{MAX}	30			−			ns
Write Pulse Width	t_{WR}	$T_A = +25°C$	180			−			ns
		$T_A = T_{MIN}$ to T_{MAX}	200			−			ns
Data Setup Time	t_{DS}	$T_A = +25°C$	110			−			ns
		$T_A = T_{MIN}$ to T_{MAX}	130			−			ns
Data Hold Time	t_{DH}	$T_A = +25°C$	0			−			ns

NOTES: (1) Specifications apply to both DACs. (2) Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}. (3) Guaranteed, but not tested. (4) These characteristics are for design guidance only and are not subject to test.

DAC7528

DIGITAL-TO-ANALOG CONVERTERS

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DICE INFORMATION
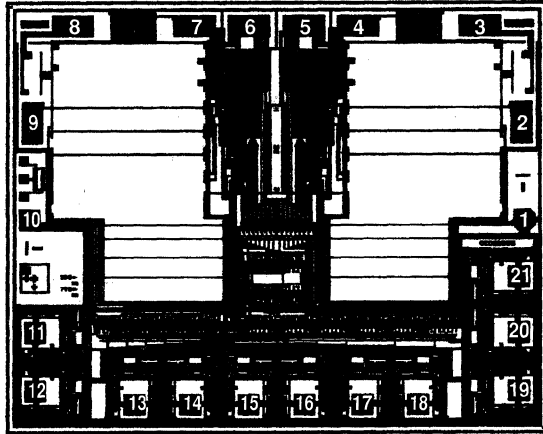
DAC7528 TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION	PAD	FUNCTION
1	V_{DD}	8	$R_{FB\ A}$	15	DB4
2	$V_{REF\ B}$	9	$V_{REF\ B}$	16	DB3
3	$R_{FB\ B}$	10	DGND	17	DB2
4	OUTB	11	$\overline{DAC\ A}/DAC\ B$	18	DB1
5	AGNDB	12	DB7	19	DB0
6	AGNDA	13	DB6	20	$\overline{CS}$
7	OUTA	14	DB5	21	$\overline{WR}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	104 x 124	2.6 x 3.1
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10

ELECTRICAL, (DICE)

At V_{DD} = +5V; $V_{REFA,\ B}$ = +10V; I_{OUT} = GND = 0V: T = Full Temperature Range specification under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC7528AD MIN	DAC7528AD TYP	DAC7528AD MAX	UNITS
DC ACCURACY [1]						
Resolution	N		8			Bits
Relative Accuracy	INL				±1	LSB
Differential Nonlinearity	DNL	Guaranteed Monolithic Over Temp			±1	LSB
FS Gain Error [2]		T_A = +25°C			±2	LSB
		$T_A = T_{MIN}$ to T_{MAX}			±4	LSB
Gain Tempco [2, 3]				±2	±35	ppm/°C
Supply Rejection	PSR	ΔV_{DD} = ±5%, T_A = +25°C		0.001	0.01	%FSR/%
		$T_A = T_{MIN}$ to T_{MAX}		0.001	0.01	%FSR/%
Output Leakage Current (OUTA)		DACA = 00_{16} T_A = +25°C			±50	nA
		$T_A = T_{MIN}$ to T_{MAX}			±200	nA
Output Leakage Current (OUTB)		DACB = 00_{16} T_A = +25°C			±50	nA
		$T_A = T_{MIN}$ to T_{MAX}			±200	nA
REFERENCE INPUT						
Input Resistance		$(V_{REF\ A},\ V_{REF\ B})$	8	10	15	kΩ
Input Resistance Match		$(V_{REF\ A},\ V_{REF\ B})$			±1	%

NOTES: (1) Specifications apply to both DACs. (2) Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}. (3) Guaranteed, but not tested. (4) These characteristics are for design guidance only and are not subject to test.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC7528P	20-Pin Plastic DIP	222
DAC7528PB	20-Pin Plastic DIP	222
DAC7528U	20-Pin SOIC	221
DAC7528UB	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.
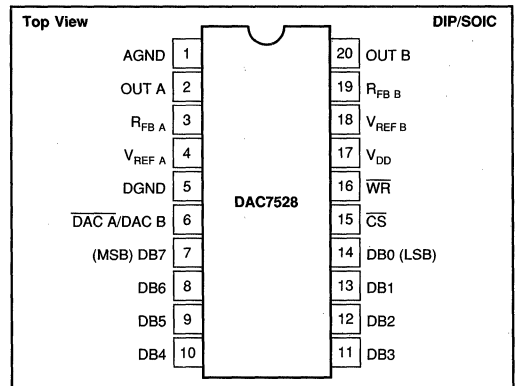
ORDERING INFORMATION

MODEL	INL	PACKAGE	TEMPERATURE RANGE
DAC7528P	±1LSB	20-Pin Plastic DIP	−40°C to +85°C
DAC7528PB	±1/2LSB	20-Pin Plastic DIP	−40°C to +85°C
DAC7528U	±1LSB	20-Pin SOIC	−40°C to +85°C
DAC7528UB	±1/2LSB	20-Pin SOIC	−40°C to +85°C

PIN CONFIGURATION

Top View
DIP/SOIC

AGND	1	20	OUT B
OUT A	2	19	$R_{FB\ B}$
$R_{FB\ A}$	3	18	$V_{REF\ B}$
$V_{REF\ A}$	4	17	V_{DD}
DGND	5	16	$\overline{WR}$
$\overline{DAC\ A}/DAC\ B$	6	15	$\overline{CS}$
(MSB) DB7	7	14	DB0 (LSB)
DB6	8	13	DB1
DB5	9	12	DB2
DB4	10	11	DB3

DAC7528

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... 0V, +7V
$V_{REFA, B}$ to GND .... ±25V
$R_{FA,B}$ to GND .... ±25V
Digital Input Voltage Range .... −0.3V to V_{DD}
Output Voltage (pins 2, 20) .... −0.3V to V_{DD}
Operating Temperature Range U,P .... −40°C to +85°C
                                          DICE .... 0°C to +70°C
Junction Temperature .... +150°C
Storage Temperature .... −60°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
θ_{JA} U package .... 105°C/W
       P package .... 85°C/W
θ_{JC} U package .... 60°C/W
       P package .... 35°C/W

NOTES: θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for PDIP package.
CAUTION: (1) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except $V_{REFA, B}$ (pins 4 and 18) and $R_{FBA, B}$ (pins 3 and 19). (2) The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. (3) Use proper anti-static handling procedures. (4) Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

WRITE CYCLE TIMING DIAGRAM
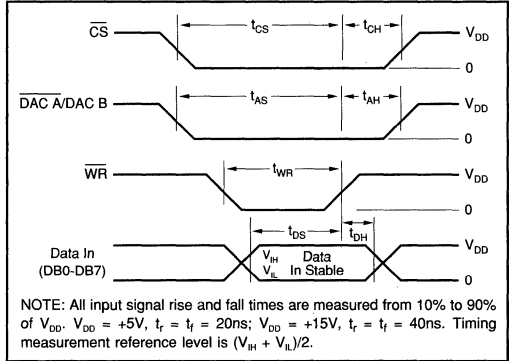
NOTE: All input signal rise and fall times are measured from 10% to 90% of V_{DD}. V_{DD} = +5V, t_r = t_f = 20ns; V_{DD} = +15V, t_r = t_f = 40ns. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

MODE SELECTION TABLE

DAC A/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Digital Inputs: All digital inputs of the DAC7528 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. $R_{FB A}$, $V_{REF A}$, $R_{FB B}$, and $V_{REF B}$ show some sensitivity.

TYPICAL PERFORMANCE CURVES

At V_{DD} = +5V; $V_{REFA,B}$ = +10V; I_{OUT} = GND = 0V: T = Full Temperature Range Specification under Absolute Maximum Ratings unless otherwise noted.

DAC7528

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DIGITAL-TO-ANALOG CONVERTERS

DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC7528 is $-(255/256)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figure 4.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT A}$ and $I_{OUT B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT A}$ or $I_{OUT B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

AC FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within $\pm 0.195\%$ of final value for a full scale step.

DIGITAL-TO-ANALOG IMPULSE

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC7528. The current from the $V_{REF A}$ pin is switched between $I_{OUT A}$ and AGND by 8 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at $V_{REF A}$ is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to $\pm 20V$.
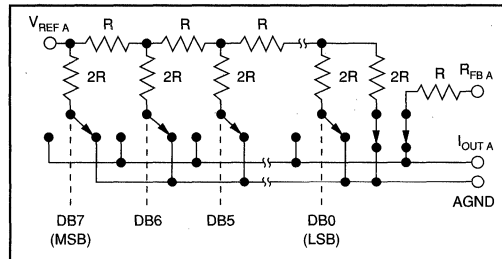
FIGURE 1. Equivalent Circuit for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.
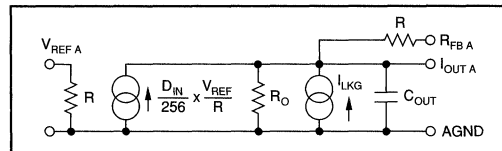
FIGURE 2. Simplified Circuit Diagram for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC7528 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC7528 is designed to operate on $V_{DD} = +5V \pm 10\%$. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the D/A. AGND and DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pin of the DAC7528 as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC7528 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC7528 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The non-linearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is non-linear with code, and the largest steps in R_O occur at major code transitions where the worst differential non-linearity is also likely to be experienced. The non-linearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good non-linearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC7528 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.
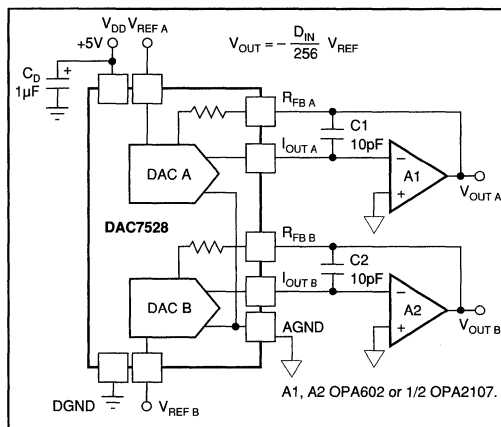
FIGURE 3. Unipolar Configuration 2 Quadrant Multiplication.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC7528 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R1–R3 and R4–R6 should be ratio-matched to 0.195% to ensure the specified gain error performance.

DAC7528

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DIGITAL-TO-ANALOG CONVERTERS

APPLICATION INFORMATION
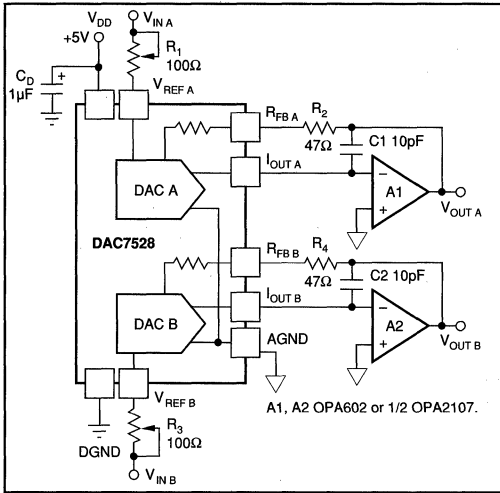
FIGURE 4. Unipolar Configuration with Gain Trim.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (255/256) = $-1/2V_{REF}$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	0V

TABLE I. Unipolar Output Code.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111	$+V_{REF}$ (127/128)
1000 0001	$+V_{REF}$ (1/128)
1000 0000	0V
0111 1111	$-V_{REF}$ (1/128)
0000 0000	$-V_{REF}$ (127/128)

TABLE II. Bipolar Output Code.
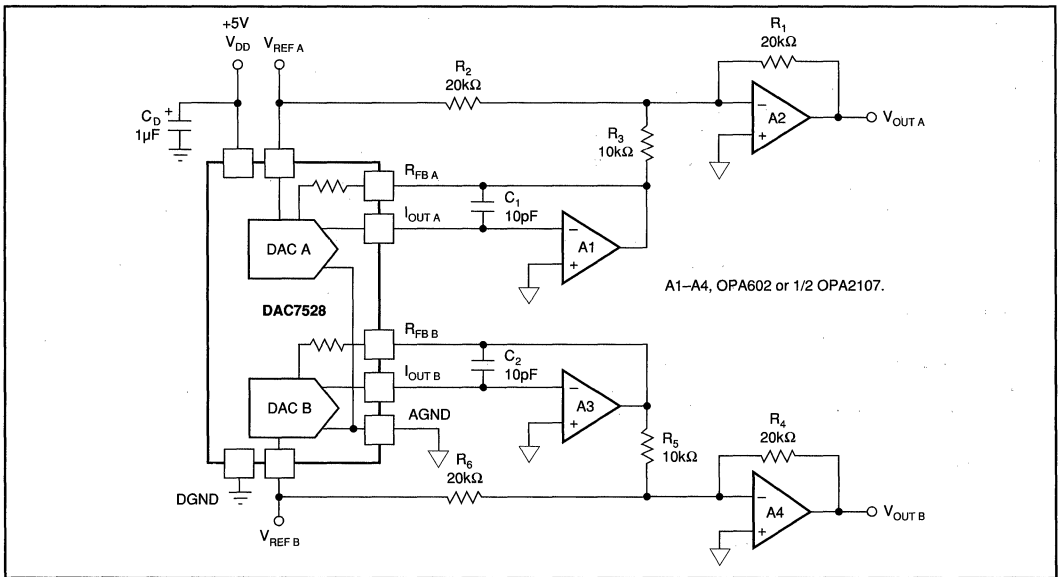
FIGURE 5. Bipolar Configuration 4 Quadrant Multiplication.

APPLICATIONS CIRCUIT: 8-BIT PLUS SIGN DAC
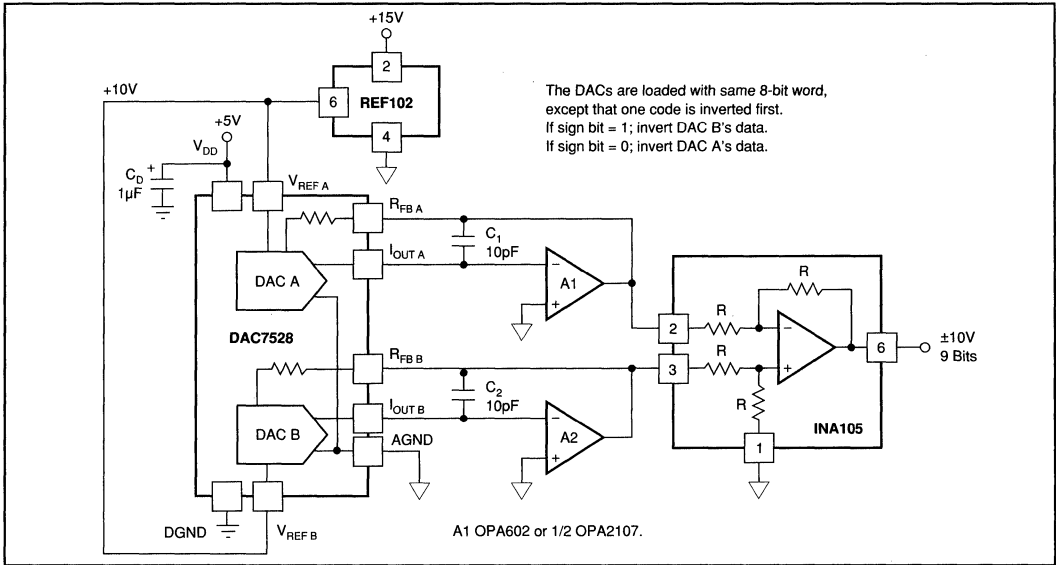
The DACs are loaded with same 8-bit word, except that one code is inverted first.
If sign bit = 1; invert DAC B's data.
If sign bit = 0; invert DAC A's data.

A1 OPA602 or 1/2 OPA2107.

DAC7528

DIGITAL-TO-ANALOG CONVERTERS

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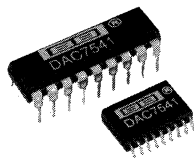
DAC7541A

Low Cost 12-Bit CMOS
Four-Quadrant Multiplying
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **FULL FOUR-QUADRANT MULTIPLICATION**
● **12-BIT END-POINT LINEARITY**
● **DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE**
● **MONOTONICITY GUARANTEED OVER TEMPERATURE**
● **TTL-/CMOS-COMPATIBLE**
● **SINGLE +5V TO +15V SUPPLY**
● **LATCH-UP RESISTANT**
● **7521/7541/7541A REPLACEMENT**
● **PACKAGES: Plastic DIP, Plastic SOIC**
● **LOW COST**

DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature range.

DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to a standard 18-pin plastic package, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.
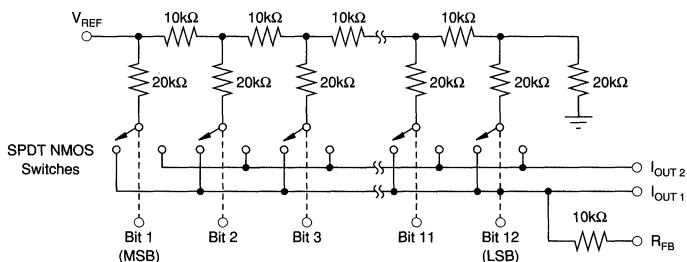
Digital Inputs (DTL-/TTL-/CMOS-compatible)
Logic: A switch is closed to $I_{OUT\,1}$ for its digital input in a "HIGH" state.

Switches shown for digital inputs "HIGH".

PDS-639C

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SPECIFICATIONS

ELECTRICAL

At +25°C, $+V_{DD}$ = +12V or +15V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V, unless otherwise specified.

PARAMETER	GRADE	T_A = +25°C	$T_A = T_{MAX}, T_{MIN}$[(1)]	UNITS	TEST CONDITIONS/COMMENTS
			DAC7541A		
ACCURACY					
Resolution	All	12	12	Bits	±1LSB = ±0.024% of FSR.
Relative Accuracy	J	±1	±1	LSB max	±1/2LSB = ±0.012% of FSR.
	K	±1/2	±1/2	LSB max	
Differenctial Non-linearity	J	±1	±1	LSB max	All grades guaranteed monotonic to 12 bits,
	K	±1/2	±1/2	LSB max	T_{MIN} to T_{MAX}.
Gain Error	J	±6	±8	LSB max	Measured using internal R_{FB} and includes effect
	K	±1	±3	LSB max	of leakage current and gain T.C.
					Gain error can be trimmed to zero.
Gain Temperature Coefficient					
(ΔGain/ΔTemperature)	ALL		5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current: Out₁ (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
Out₂ (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
REFERENCE INPUT					
Voltage (Pin 17 to GND)	All	−10/+10	−10/+10	V min/max	
Input Resistance (Pin 17 to GND)	All	7-18	7-18	kΩ min/max	
					Typical input resistance = 11kΩ.
					Typical input resitance temperature coefficient is
					−50ppm/°C.
DIGITAL INPUTS					
V_{IN} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic inputs are MOS gates.
					I_{IN} typ (25°C) = 1nA
C_{IN} (Input Capacitance)[(2)]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
ΔGain/ΔV_{DD}	All	±0.01	±0.02	% per % max	V_{DD} = +11.4V to +16V
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min to	Accuracy is not guaranteed over this range.
				V max	
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IN}.
	All	100	500	μA max	All digital inputs 0V or V_{DD}.

NOTES: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions. (2) Guaranteed by design but not production tested.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not production tested.
V_{DD} = +15V, V_{REF} = +10V except where stated, V_{PIN1} = V_{PIN2} = 0V, output amp is OPA606 except where stated.

PARAMETER	GRADE	T_A = +25°C	$T_A = T_{MAX}, T_{MIN}$[(1)]	UNITS	TEST CONDITIONS/COMMENTS
			DAC7541A		
PROPAGATION DELAY					
(from Digital Input change to 90% of					Out₁ Load = 100Ω, C_{EXT} = 13pF.
final Analog Output)	All	100	—	ns typ	Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL-TO-ANALOG GLITCH					V_{REF} = 0V, all digital inputs 0V to V_{DD} or V_{DD} to
IMPULSE	All	1000	—	nV-s typ	0V. Measured using OPA606 as output amplifier.
MULTIPLYING FEEDTHROUGH					
ERROR					
(V_{REF} to Out₁)	All	1.0	—	mVp-p max	V_{REF} = ±10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME					
	All	0.6	—	μs typ	To 0.01% of Full Scale Range.
	All	1.0	—	μs max	Out₁ Load = 100Ω, C_{EXT} = 13pF.
					Digital Inputs: 0V to V_{DD} or V_{DD} to 0V.
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	100	100	pF max	Digital Inputs = V_{IH}
C_{OUT2} (Pin 2)	All	60	60	pF max	Digital Inputs = V_{IH}
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs = V_{IL}
C_{OUT2} (Pin 2)	All	100	100	pF max	Digital Inputs = V_{IL}

NOTE: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions.

DAC7541A

DIGITAL-TO-ANALOG CONVERTERS

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ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} (Pin 16) to Ground .... +17V
V_{REF} (Pin 17) to Ground .... +25V
V_{RPB} (Pin 18) to Ground .... ±25V
Digital Input Voltage (pins 4-15) to Ground .... –0.4V, V_{DD}
$V_{PIN 1}$, $V_{PIN 2}$ to Ground .... –0.4V, V_{DD}
Power Dissipation (any Package):
   To +75°C 450mW
   Derates above +75°C .... –6mW/°C
Lead Temperature (soldering, 10s) .... +300°C
Storage Temperature: Plastic Package .... +125°C

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

BURN-IN SCREENING

Burn-in screening is an option available for the models in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

PIN CONNECTIONS

Top View   DIP/SOIC

$I_{OUT 1}$	1	18	R_{FB}
$I_{OUT 2}$	2	17	V_{REF}
GND	3	16	+V_{DD}
Bit 1 (MSB)	4	15	Bit 12 (LSB)
Bit 2	5	14	Bit 11
Bit 3	6	13	Bit 10
Bit 4	7	12	Bit 9
Bit 5	8	11	Bit 8
Bit 6	9	10	Bit 7

DAC7541A

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC7541JP	Plastic DIP	218
DAC7541KP	Plastic DIP	218
DAC7541JU	Plastic SOIC	219
DAC7541KU	Plastic SOIC	219
DAC7541JP-BI	Plastic DIP	218
DAC7541KP-BI	Plastic DIP	218

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB)
DAC7541AJP	Plastic DIP	0°C to +70°C	±1	±6
DAC7541AKP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7541AJU	Plastic SOIC	0°C to +70°C	±1	±6
DAC7541AKU	Plastic SOIC	0°C to +70°C	±1/2	±1

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	BURN-IN TEMP. (160 Hours)[1]
DAC7541AJP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC7541AKP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C
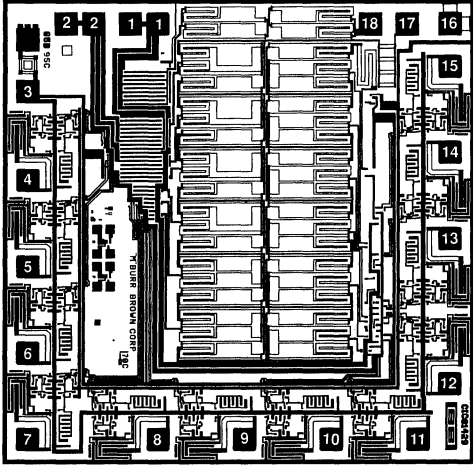
DIE TOPOLOGY DAC7541A

PAD	FUNCTION	PAD	FUNCTION
1	I_{OUT1}	10	Bit 7
2	I_{OUT2}	11	Bit 8
3	GND	12	Bit 9
4	Bit 1 (MSB)	13	Bit 10
5	Bit 2	14	Bit 11
6	Bit 3	15	Bit 12 (LSB)
7	Bit 4	16	$+V_{DD}$
8	Bit 5	17	V_{REF}
9	Bit 6	18	$R_{FEEDBACK}$

Substrate Bias: Isolated.
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	104 x 105 ±5	2.64 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DAC7541A

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DIGITAL-TO-ANALOG CONVERTERS

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V, unless otherwise noted.

GAIN ERROR vs SUPPLY VOLTAGE

FEEDTHROUGH ERROR vs FREQUENCY

LINEARITY vs SUPPLY VOLTAGE

SUPPLY CURRENT vs SUPPLY VOLTAGE

V_{IH} = +2.4V

V_{IH} = V_{DD}
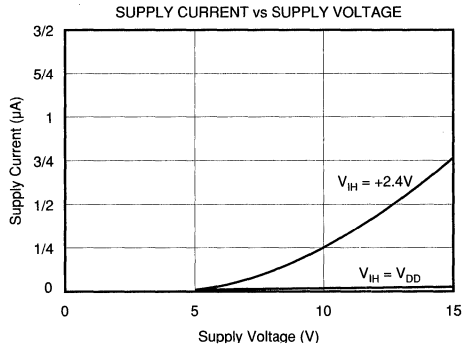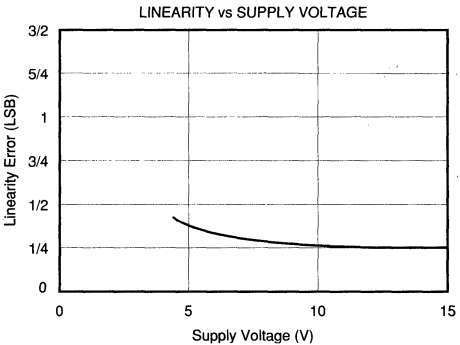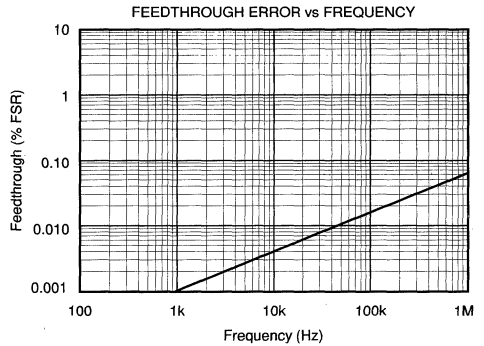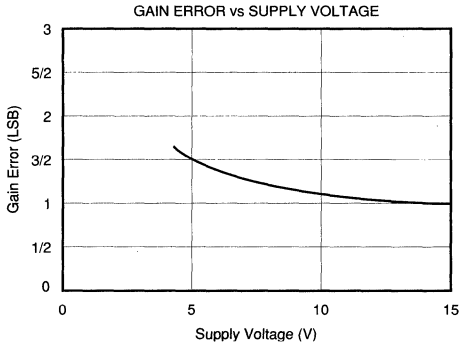
DISCUSSION
OF SPECIFICATIONS

RELATIVE ACCURACY

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line between zero and full scale.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, from one adjacent output state to the next. A differential nonlinearity specification of ±1.0LSB guarantees monotonicity.

GAIN ERROR

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7541A is $-(4095/4096)$ X (V_{REF}). Gain error may be adjusted to zero using external trims.

OUTPUT LEAKAGE CURRENT

The measure of current which appears at Out_1 with the DAC loaded with all zeros, or at Out_2 with the DAC loaded with all ones.

MULTIPLYING FEEDTHROUGH ERROR

This is the AC error output due to capacitive feedthrough from V_{REF} to Out_1 with the DAC loaded with all zeros. This test is performed at 10kHz.

OUTPUT CURRENT SETTLING TIME

This is the time required for the output to settle to a tolerance of ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

PROPAGATION DELAY

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the measure of the area of the glitch energy measured in nV-seconds. Key contributions to glitch energy are digital word-bit timing differences, internal circuitry timing differences, and charge injected from digital logic.

MONOTONICITY

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7541A is guaranteed monotonic to 12 bits.

POWER SUPPLY REJECTION

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

The DAC7541A is a 12-bit multiplying D/A converter consisting of a highly stable thin-film R-2R ladder network and 12 pairs of current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the DAC7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity.
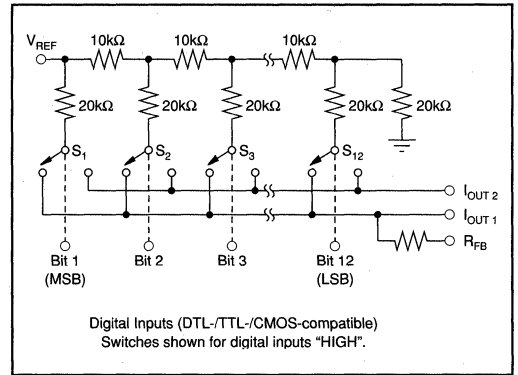
FIGURE 1. Simplified DAC Circuit.

EQUIVALENT CIRCUIT ANALYSIS

Figures 2 and 3 show the equivalent circuits for all digital inputs low and high, respectively. The reference current is switched to $I_{OUT\,2}$ when all inputs are low and $I_{OUT\,1}$ when inputs are high. The I_L current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant one-bit current drain through the ladder terminal.

DYNAMIC PERFORMANCE
Output Impedance

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\,1}$ terminal may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output
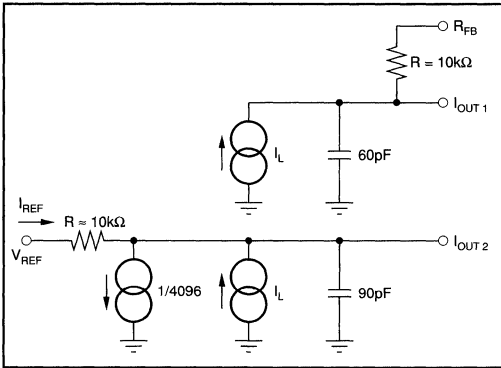
FIGURE 2. DAC7541A Equivalent Circuit (All inputs LOW).
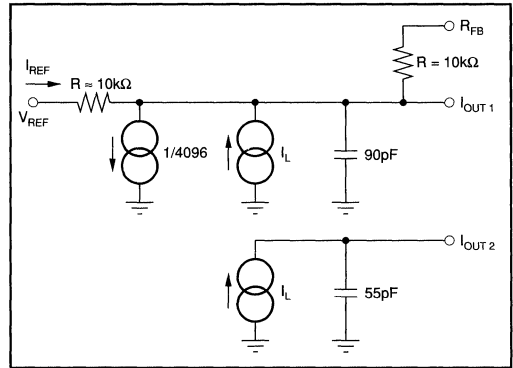
FIGURE 3. DAC7541A Equivalent Circuit (All inputs HIGH).

amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically dampen the output. See Figures 4 and 6.

APPLICATIONS

OP AMP CONSIDERATIONS
The input bias current of the op amp flows through the feedback resistor, creating an error voltage at the output of the op amp. This will show up as an offset through all codes of the transfer characteristics. A low bias current op amp such as the OPA606 is recommended.

Low offset voltage and V_{OS} drift are also important. The output impedance of the DAC is modulated with the digital code. This impedance change (approximately $10k\Omega$ to $30k\Omega$) is a change in closed-loop gain to the op amp. The result is that V_{OS} will be multiplied by a factor of one to two depending on the code. This shows up as a linearity error. Offset can be adjusted out using Figure 4. Gain may be adjusted using Figure 5.

UNIPOLAR BINARY OPERATION
(Two-Quadrant Multiplication)
Figure 4 shows the analog circuit connections required for unipolar binary (two-quadrant multiplication) operation. With a DC reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an AC reference voltage or current, the circuit provides two-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I.

BINARY INPUT	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0V

TABLE I. Unipolar Codes.

C_1 phase compensation (10 to 25pF) in Figure 4 may be required for stability when using high speed amplifiers. C_1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at Out_1.

R_1 in Figure 5 provides full scale trim capability—load the DAC register to 1111 1111 1111, adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096). Alternatively, full scale can be adjusted by omitting R_1 and R_2 and trimming the reference voltage magnitude.

BIPOLAR FOUR-QUADRANT OPERATION
Figure 6 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

BINARY INPUT	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Codes.

DAC7541A

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DIGITAL-TO-ANALOG CONVERTERS

$$V_{OUT} = -V_{REF} \left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \cdots + \frac{B_{12}}{4096} \right)$$

$$-10V \le V_{REF} \le +10V$$

$$0 \le V_{OUT} \le -\frac{4095}{4096} V_{REF}$$

Where: $B_N = 1$ if the B_N digital input is HIGH.
$B_N = 0$ if the B_N digital input is LOW.
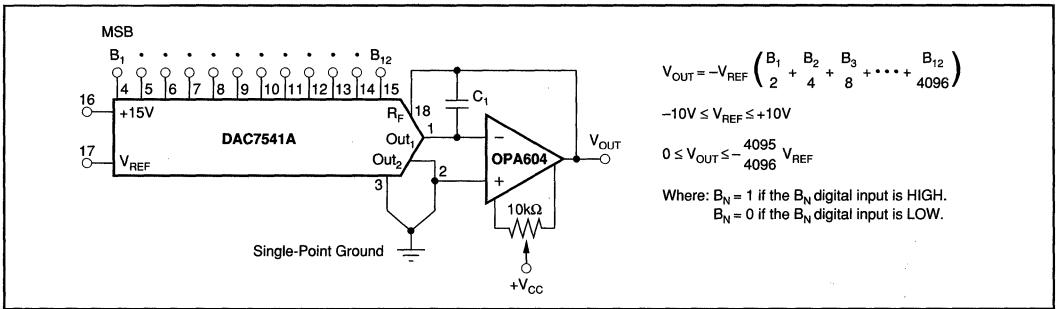
FIGURE 4. Basic Connection With Op Amp V_{OS} Adjust: Unipolar (two-quadrant) Multiplying Configuration.
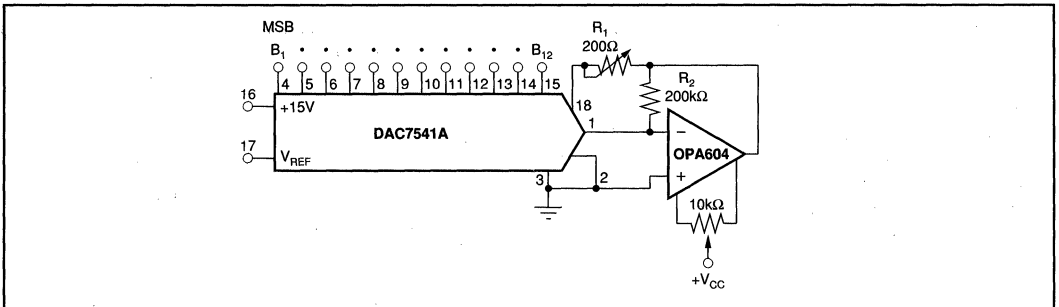
FIGURE 5. Basic Connection With Gain Adjust (allows adjustment up or down).

$$V_{OUT} = +V_{REF} \left(\frac{B_1}{1} + \frac{B_2}{2} + \frac{B_3}{4} + \cdots + \frac{B_{12}}{2048} - 1 \right)$$
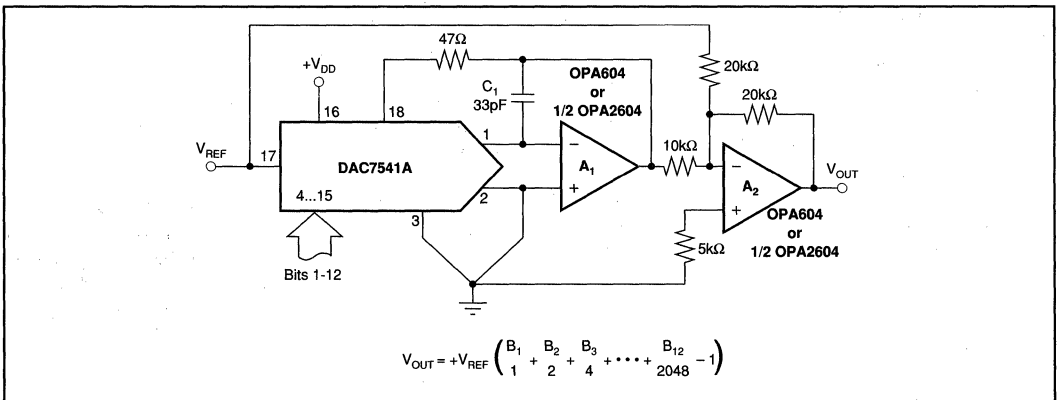
FIGURE 6. Bipolar Four-Quadrant Multiplier.

DIGITALLY CONTROLLED GAIN BLOCK

The DAC7541A may be used in a digitally controlled gain block as shown in Figure 7. This circuit gives a range of gain from one (all bits = one) to 4096 (LSB = one). The transfer function is:

$$V_{OUT} = \frac{-V_{IN}}{\left(\dfrac{B_1}{2} + \dfrac{B_2}{4} + \dfrac{B_3}{8} + \bullet \bullet \bullet + \dfrac{B_{12}}{4096} \right)}$$

All bits off is an illegal state, as division by zero is impossible (no op amp feedback). Also, errors increase as gain increases, and errors are minimized at major carries (only one bit on at a time).
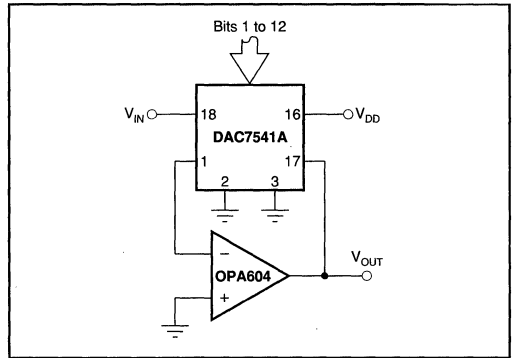
FIGURE 7. Digitally Programmable Gain Block.

DAC7541A

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DIGITAL-TO-ANALOG CONVERTERS

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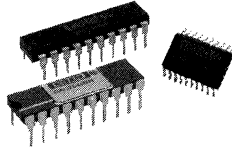
DAC7545

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER Microprocessor Compatible

FEATURES

● **FOUR-QUADRANT MULTIPLICATION**

● **LOW GAIN TC: 2ppm/°C typ**

● **MONOTONICITY GUARANTEED OVER TEMPERATURE**

● **SINGLE 5V TO 15V SUPPLY**

● **TTL/CMOS LOGIC COMPATIBLE**

● **LOW OUTPUT LEAKAGE: 10nA max**

● **LOW OUTPUT CAPACITANCE: 70pF max**

● **DIRECT REPLACEMENT FOR AD7545, PM-7545**

DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin plastic DIP or 20-lead plastic SOIC packages. Devices are specified over the commercial, industrial, and military temperature ranges.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and V_{DD} = +5V.

R_{FB} [20]

V_{REF} [19] — 12-Bit Multiplying DAC — [1] OUT 1 / [2] AGND

$\overline{WR}$ [17] / $\overline{CS}$ [16] — Input Data Latches — [18] V_{DD} / [3] DGND

DB_{11}-DB_0 (Pins 4-15)

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SPECIFICATIONS

ELECTRICAL

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM, unless otherwise specified.

PARAMETER	GRADE	DAC7545 V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{MAX}-T_{MIN}[1]	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{MAX}-T_{MIN}[1]	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Accuracy	D, J, A, S	±2	±2	±2	±2	LSB	
	K, B, T	±1	±1	±1	±1	LSB	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB	
Differential Nonlinearity	D, J, A, S	±4	±4	±4	±4	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	K, B, T	±1	±1	±1	±1	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	L, C, U	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
	GL, GC, GU	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
Gain Error (with internal R_{FB})[2]	D, J, A, S	±20	±20	±25	±25	LSB	D/A register loaded with FFF$_H$.
	K, B, T	±10	±10	±15	±15	LSB	Gain error is adjustable using
	L, C, U	±5	±6	±10	±10	LSB	the circuits in Figures 2 and 3.
	GL, GC, GU	±1	±2	±6	±7	LSB	
Gain Temperature Coefficient[3]							
(ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C	Typical value is 2ppm/°C
						for V_{DD} = +5	
DC Supply Rejection[3]							
(ΔGain/ΔV_{DD})	All	0.015	0.03	0.01	0.02	%/%	ΔV_{DD} ±5%
Output Leakage Current at Out 1	D, J, K, L, GL	10	50	10	50	nA	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA	
	S, T, U, GU	10	200	10	200	nA	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	µs	To 1/2LSB. Out, Load = 100Ω DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V
Propagation Delay[3] (from digital input change to 90% of final analog output)	All	300		250		ns	Out, Load ≈ 100Ω. C_{EXT} = 13pF[4]
Glitch Energy	All	400		250		nV-s[5]	V_{REF} = ACOM
AC Feedback at I_{OUT} 1	All	5	5	5	5	mVp-p[5]	V_{REF} = ±10V, 10kHz Sine Wave
REFERENCE INPUT							
Input Resistance (pin 19 to AGND)	All	7	7	7	7	kΩ[6]	Input resistance TC = 300ppm/°C[5]
		25	25	25	25	kΩ	
AC OUTPUTS							
Output Capacitance[3] $C_{OUT\,1}$	All	70	70	70	70	pF	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
$C_{OUT\,2}$	All	200	200	200	200	pF	DB_0-DB_{11} = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	13.5	13.5	V[6]	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	1.5	1.5	V	
I_{IN} (Input Current)[7]	All	±1	±10	±1	±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[3]: DB_0-DB_{11}	All	5	5	5	5	pF	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF	V_{IN} = 0V
SWITCHING CHARACTERISTICS[6]							
Chip Select to Write Setup Time, t_{CS}	All	280	380	180	200	ns[6]	See Timing Diagram
		200	270	120	150	ns[5]	
Chip Select to Write Hold Time, t_{CH}	All	0	0	0	0	ns[6]	
Write Pulse Width, t_{WR}	All	250	400	160	240	ns[6]	t_{CS} ≥ t_{WR}, t_{CH} ≥ 0
		175	280	100	170	ns[5]	
Data Setup Time, t_{DS}	All	140	210	90	120	ns[6]	
		100	150	60	80	ns[5]	
Data Hold Time, t_{DH}	All	10	10	10	10	ns[6]	
POWER SUPPLY, I_{DD}							
	All	2	2	2	2	mA	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	µA	All Digital Inputs 0V or V_{DD}
	All	10	10	10	10	µA[5]	All Digital Inputs 0V or V_{DD}

NOTES: (1) Temperature ranges—J, K, L, GL: 0°C to +70°C. A, B, C, GC: –25°C to +85°C. S, T, U, GU: –55°C to +125°C. (2) This includes the effect of 5ppm max, gain TC. (3) Guaranteed but not tested. (4) DB_0-DB_{11} = 0V to V_{DD} or V_{DD} to 0V. (5) Typical. (6) Minimum. (7) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA. (8) Sample tested at +25°C to ensure compliance.

DAC7545

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DIGITAL-TO-ANALOG CONVERTERS

ABSOLUTE MAXIMUM RATINGS[(1)]

$T_A = +25°C$, unless otherwise noted.

V_{DD} to DGND .... −0.3V, +17	
Digital Input to DGND .... −0.3V, V_{DD}	
V_{RFB}, V_{REF}, to DGND .... ±25V	
$V_{PIN 1}$ to DGND .... −0.3V, V_{DD}	
AGND to DGND .... −0.3V, V_{DD}	
Power Dissipation: Any Package to +75°C 450mW	
Derates above +75°C by .... 6mW/°C	
Operating Temperature:	
Commercial J, K, L, GL .... 0°C to +70°C	
Industrial A, B, C, GC .... −25°C to +85°C	
Military S, T, U, GU .... −55°C to +125°C	
Storage Temperature .... −65°C to +150°C	
Lead Temperature (soldering, 10s) .... +300°C	

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONNECTIONS

Top View DIP/SOIC

OUT 1	1	20	R_{FB}
AGND	2	19	V_{REF}
DGND	3	18	V_{DD}
(MSB) DB_{11}	4	17	$\overline{WR}$
DB_{10}	5	16	$\overline{CS}$
DB_9	6	15	DB_0 (LSB)
DB_8	7	14	DB_1
DB_7	8	13	DB_2
DB_6	9	12	DB_3
DB_5	10	11	DB_4

DAC7545

PACKAGE INFORMATION[(1)]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC7545AP	20-Pin PDIP	222
DAC7545BP	20-Pin PDIP	222
DAC7545JP	20-Pin PDIP	222
DAC7545KP	20-Pin PDIP	222
DAC7545GLP	20-Pin PDIP	222
DAC7545JU	20-Pin SOIC	221
DAC7545KU	20-Pin SOIC	221
DAC7545LU	20-Pin SOIC	221
DAC7545GLU	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB) V_{DD} = +5V
DAC7545JP	Plastic DIP	0°C to +70°C	±2	±20
DAC7545KP	Plastic DIP	0°C to +70°C	±1	±10
DAC7545LP	Plastic DIP	0°C to +70°C	±1/2	±5
DAC7545GLP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7545JU	Plastic SOIC	0°C to +70°C	±2	±20
DAC7545KU	Plastic SOIC	0°C to +70°C	±1	±10
DAC7545LU	Plastic SOIC	0°C to +70°C	±1/2	±5
DAC7545GLU	Plastic SOIC	0°C to +70°C	±1/2	±1

WRITE CYCLE TIMING DIAGRAM

Mode Selection	
Write Mode	**Hold Mode**
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to Data Bus (DB_0-DB_{11}) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB_0-DB_{11}) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES: V_{DD} = +5V, $t_R = t_F$ = 20ns. V_{DD} = +15V, $t_R = t_F$ = 40ns. All inputs signal rise and fall times measured from 10% to 90% of V_{DD}. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.
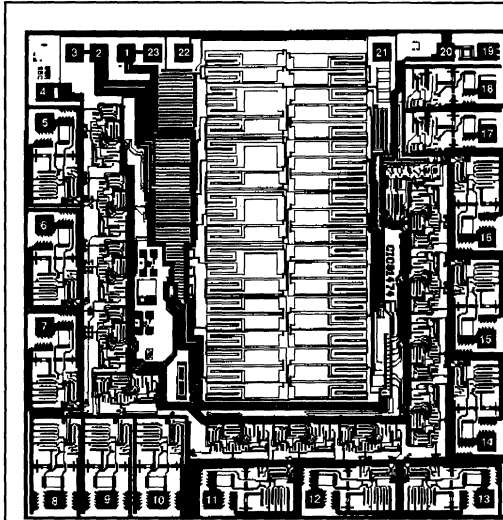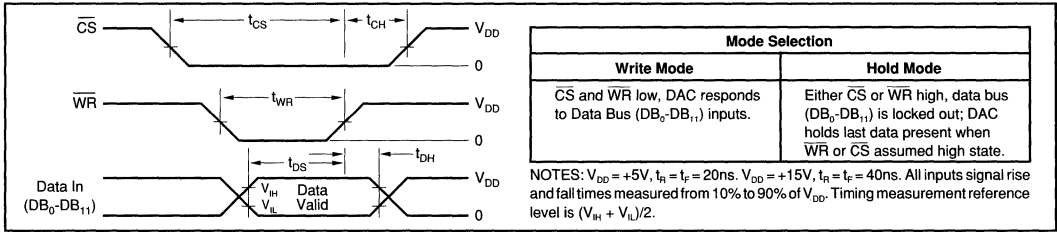
DAC7545 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	OUT 1	13	DB_3
2	AGND	14	DB_2
3	AGND	15	DB_1 (LSB)
4	DGND	16	DB_0
5	DB11	17	$\overline{CS}$
6	DB10	18	$\overline{WR}$
7	DB9	19	$\overline{XYR}$
8	DB8	20	V_{DD}
9	DB7	21	V_{REF}
10	DB6	22	R_{FB}
11	DB_5	23	OUT_1
12	DB_4		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	136 x 134 ±5	3.45 x 3.40 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DISCUSSION OF SPECIFICATIONS

Relative Accuracy
This term (also known as end point linearity) describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale have been adjusted.

Differential Nonlinearity
Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Gain Error
Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7545 is $-(4095/4096)(V_{REF})$. Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current
The current which appears at OUT 1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error
The AC output error due to capacitive feedthrough from V_{REF} to OUT 1 with the DAC loaded with all zeros. This test is performed using a 10kHz sine wave.

Output Current Settling Time
The time required for the output to settle within ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

DIGITAL-TO-ANALOG CONVERTERS 3 **DAC7545**

Propagation Delay

The delay of the internal circuitry is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-to-Analog Glitch Impulse

The area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND and an OPA600 as the output op amp and G_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7545 is guaranteed monotonic to 12 bits, except the J, A, S grades are specified to be 10-bit monotonic.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of the digital-to-analog converter portion of the DAC7545. The current from the V_{REF} pin is switched from OUT 1 to AGND by the FET switch. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.
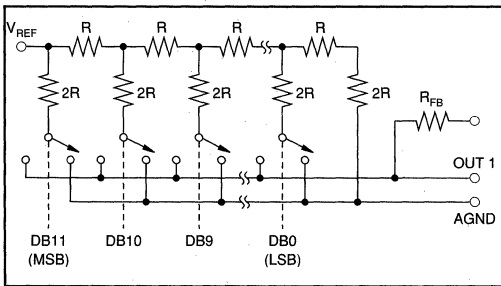
FIGURE 1. Simplified DAC Circuit of the DAC7545.

The output capacitance of the DAC7545 is code dependent and varies from a minimum value (70pF) at code 000H to a maximum (200pF) at code FFFH.

The input buffers are CMOS inverters, designed so that when the DAC7545 is operated from a 5V supply (V_{DD}), the logic threshold is TTL-compatible. Being simple CMOS inverters, there is a range of operation where the inverters operate in the linear region and thus draw more supply

current than normal. Minimizing this transition time through the linear region and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

UNIPOLAR OPERATION

Figure 2 shows the DAC7545 connected for unipolar operation. The high-grade DAC7545 is specified for a 1LSB gain error, so gain adjust is typically not needed. However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC7545JP, the gain error is specified to be ±25LSB. A range of adjustment of ±37LSB will be adequate. The equation below results in a value of 458Ω for the potentiometer (use 500Ω).

$$R_1 = \frac{R_{LADDER}}{4096} (3 \times \text{Gain Error})$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 2 may be used with input voltages up to ±20V as long as the output amplifier is biased to handle the excursions. Table I represents the analog output for four codes into the DAC for Figure 2.
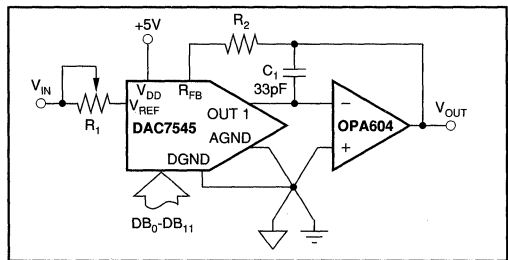
FIGURE 2. Unipolar Binary Operation.

BINARY CODE	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 V

TABLE I. Unipolar Codes.
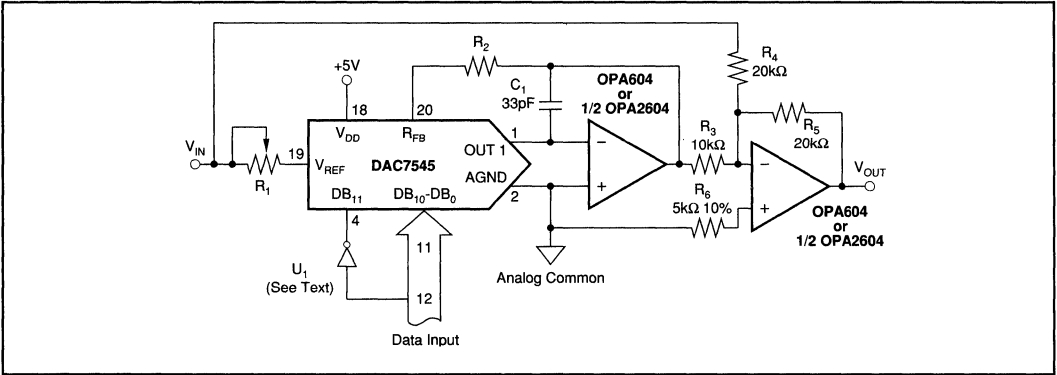
FIGURE 3. Bipolar Operation (Two's Complement Code).

BIPOLAR OPERATION

Figure 3 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter, U_1, on the MSB line converts two's complement input code to offset binary code. If the inversion is done in software, U_1 may be omitted.

R_3, R_4, and R_5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R_3 value to R_4 causes both offset and full-scale error. Mismatch of R_5 to R_4 and R_3 causes full-scale error.

DATA INPUT	ANALOG OUTPUT
MSB LSB	
0111 1111 1111	$+V_{IN}$ (2047/2048)
0000 0000 0001	$+V_{IN}$ (1/2048)
0000 0000 0000	0 V
1111 1111 1111	$-V_{IN}$ (1/2048)
1000 0000 0000	$-V_{IN}$ (2048/2048)

TABLE II. Two's Complement Code Table for Circuit of Figure 3.

DIGITALLY CONTROLLED GAIN BLOCK

Figure 4 shows a circuit for digitally controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC7545. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback, and a saturated op amp output.

APPLICATIONS HINTS

CMOS DACs, such as the DAC7545, exhibit a code-dependent out resistance. The effect of this is a code-dependent differential nonlinearity at the amplifier output which depends on the offset voltage, V_{OS}, of the amplifier. Thus linearity depends upon the potential of OUT 1 and AGND being exactly equal to each other. Usually the DAC is
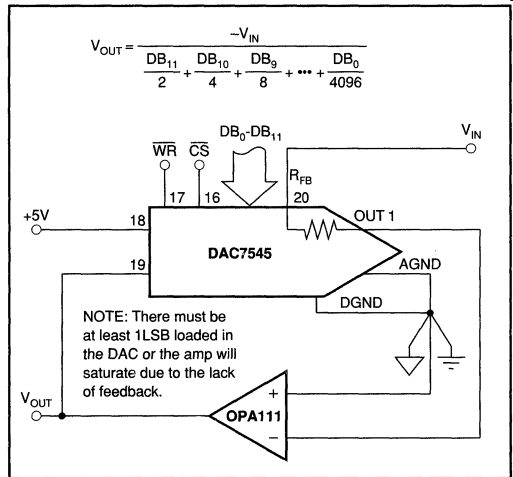
FIGURE 4. Digitally Controlled Gain Block.

connected to an external op amp with its noninverting input connected to AGND. The op amp selected should have a low input bias current and low V_{OS} and V_{OS} drift over temperature. The op amp offset voltage should be less than $(25 \times 10^{-6})(V_{REF})$ over operating conditions. Suitable op amps are the Burr-Brown OPA37 and the OPA627 for fixed reference applications and low bandwidth requirement. The OPA37 has low V_{OS} and will not require an offset trim. For wide bandwidth, high slew rate, or fast settling applications, the Burr-Brown OPA604 or 1/2 OPA2604 are recommended.

Unused digital inputs should be connected to V_{DD} or to DGND. This prevents noise form triggering the high imped-ance digital input. It is suggested that the unused digital inputs also be given a path to ground or V_{DD} through a 1MΩ resistor to prevent the accumulation of static charge if the PC card is unplugged from the system. In addition, in systems where the AGND to DGND connection is on a backplane, it is recommended that two diodes be connected in inverse parallel between AGND and DGND.

INTERFACING
TO MICROPROCESSORS

The DAC7545 can be directly interfaced to either an 8- or 16-bit microprocessor through its 12-bit wide data latch using the $\overline{CS}$ and $\overline{WR}$ controls.

An 8-bit processor interface is shown in Figure 5. It uses two memory addresses, one for the lower 8 bits and one for the upper 4 bits of data into the DAC via the latch.

NOTES: (1) $\overline{Q_0}$ = Decoded Address for DAC.
(2) $\overline{Q_1}$ = Decoded Address for Latch.
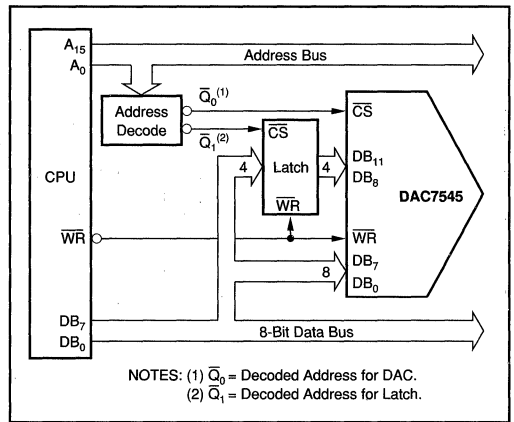
FIGURE 5. 8-Bit Processor Interface.

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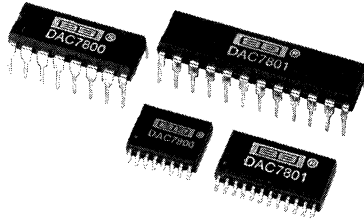
DAC7800
DAC7801
DAC7802

DAC7800/01/02

Dual Monolithic CMOS 12-Bit Multiplying
DIGITAL-TO-ANALOG CONVERTERS

DIGITAL-TO-ANALOG CONVERTERS

3

FEATURES

● TWO D/As IN A 0.3" WIDE PACKAGE
● SINGLE +5V SUPPLY
● HIGH SPEED DIGITAL INTERFACE:
  Serial—DAC7800
  8 + 4-Bit Parallel—DAC7801
  12-Bit Parallel—DAC7802
● MONOTONIC OVER TEMPERATURE
● LOW CROSSTALK: –94dB min
● FULLY SPECIFIED OVER –40°C TO +85°C

APPLICATIONS

● PROCESS CONTROL OUTPUTS
● ATE PIN ELECTRONICS LEVEL SETTING
● PROGRAMMABLE FILTERS
● PROGRAMMABLE GAIN CIRCUITS
● AUTO-CALIBRATION CIRCUITS

DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of –40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each D/A separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single D/A register for each D/A. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.

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SPECIFICATIONS

ELECTRICAL

At V_{DD} = +5VDC, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = −40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7800/7801/7802K, D			DAC7800/7801/7802L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Resolution		12			*			Bits
Relative Accuracy				±1			±1/2	LSB
Differential Nonlinearity				±1			*	LSB
Gain Error	Measured Using $R_{FB\,A}$ and $R_{FB\,B}$.			±3			±1	LSB
	All Registers Loaded with All 1s.							
Gain Temperature Coefficient[1]	T_A = +25°C		2	5		*	*	ppm/°C
Output Leakage Current	T_A = +25°C		0.005	10		*	*	nA
	T_A = −40°C to +85°C		3	150		*	*	nA
REFERENCE INPUT								
Input Resistance		6	10	14	*	*	*	kΩ
Input Resistance Match			0.5	3		*	2	%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)		2			*			V
V_{IL} (Input Low Voltage)				0.8			*	V
I_{IN} (Input Current)	T_A = +25°C			±1			*	µA
	T_A = −40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8	10		*	*	pF
POWER SUPPLY								
V_{DD}		4.5		5.5	*		*	V
I_{DD}			0.2	2		*	*	mA
Power Supply Rejection	V_{DD} from 4.5V to 5.5V			0.002			*	%/%

* Same specification as for DAC7800/7801/7802K.

AC PERFORMANCE

OUTPUT OP AMP IS OPA602.

At V_{DD} = +5VDC, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = +25°C unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7800/7801/7802K, D			DAC7800/7801/7802L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CURRENT SETTLING TIME	To 0.01% of Full Scale R_L = 100Ω, C_L = 13pF		0.4	0.8		*	*	µs
DIGITAL-TO-ANALOG GLITCH IMPULSE	$V_{REF\,A}$ = $V_{REF\,B}$ = 0V R_L = 100Ω, C_L = 13pF		0.9			*		nV-s
AC FEEDTHROUGH	f_{VREF} = 10kHz		−75	−72		*	*	dB
OUTPUT CAPACITANCE	DAC Loaded with All 0s		30	50		*	*	pF
	DAC Loaded with All 1s		70	100		*	*	pF
CHANNEL-TO-CHANNEL ISOLATION								
$V_{REF\,A}$ to $I_{OUT\,B}$	$f_{VREF\,A}$ = 10kHz $V_{REF\,B}$ = 0V, Both DACs Loaded with 1s	−90	−94		*	*		dB
$V_{REF\,B}$ to $I_{OUT\,A}$	$f_{VREF\,B}$ = 10kHz $V_{REF\,A}$ = 0V, Both DACs Loaded with 1s	−90	−101		*	*		dB
DIGITAL CROSSTALK	Full Scale Transition R_L = 100Ω, C_L = 13pF		0.9			*		nV-s

NOTE: (1) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

At T_A = +25°C unless otherwise noted.

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	–0.3, V_{DD}
Digital Input to DGND	–0.3, V_{DD} + 0.3
$V_{REF\,A}$, $V_{REF\,B}$ to AGND	±25V
$V_{REF\,A}$, $V_{REF\,B}$ to DGND	±25V
$I_{OUT\,A}$, $I_{OUT\,B}$ to AGND	–0.3, V_{DD}
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure.

Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

Digital Inputs: All digital inputs of the DAC780X family incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. AGND, I_{OUT}, and R_{FB} show some sensitivity. Failure to observe ESD handling procedures could result in catastrophic device failure.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC7800KP	16-Pin PDIP	180
DAC7800LP	16-Pin PDIP	180
DAC7800KU	16-Pin SOIC	211
DAC7800LU	16-Pin SOIC	211
DAC7801KP	24-Pin DIP	243
DAC7801LP	24-Pin DIP	243
DAC7801KU	24-Pin SOIC	239
DAC7801LU	24-Pin SOIC	239
DAC7802KP	24-Pin DIP	243
DAC7802LP	24-Pin DIP	243
DAC7802KU	24-Pin SOIC	239
DAC7802LU	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	RELATIVE ACCURACY	GAIN ERROR	PACKAGE
DAC7800KP	±1LSB	±3LSB	16-Pin DIP
DAC7800KU[1]			16-Lead SO
DAC7800LP	±1/2LSB	±1LSB	16-Pin DIP
DAC7800LU			16-Lead SO
DAC7801KP	±1LSB	±3LSB	24-Pin DIP
DAC7801KU			24-Lead SO
DAC7801LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7801LU			24-Lead SO
DAC7802KP	±1LSB	±3LSB	24-Pin DIP
DAC7802KU[1]			24-Lead SO
DAC7802LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7802LU			24-Lead SO

NOTE: (1) Available with Tape and Reel. Add "-TR" to basic model number.

DAC7800/01/02

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DIGITAL-TO-ANALOG CONVERTERS
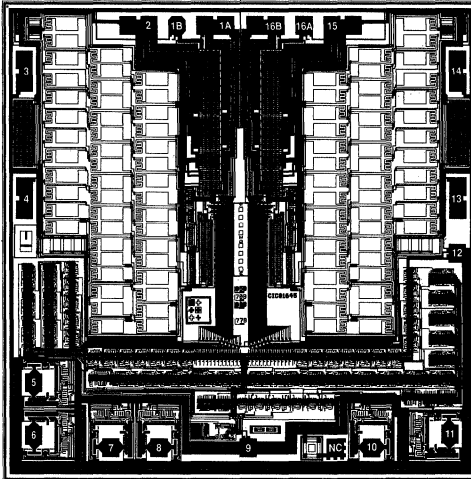
DICE INFORMATION

DAC7800 DIE TOPOGRAPHY
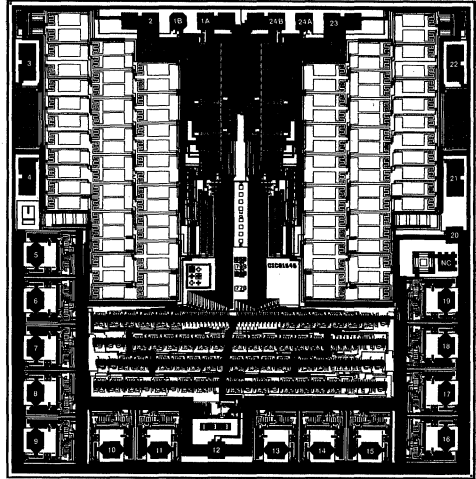
DAC7801 DIE TOPOGRAPHY
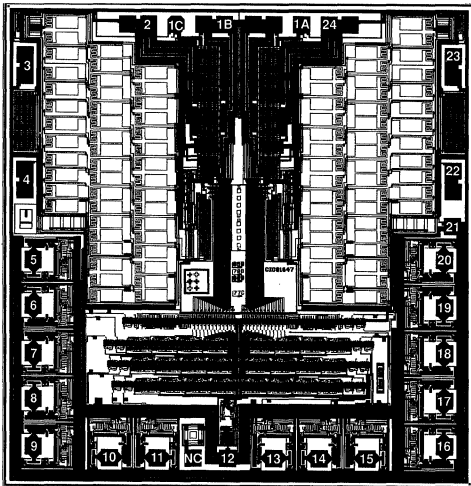
DAC7802 DIE TOPOGRAPHY

MECHANICAL INFORMATION

DAC7800	MILS (0.001")	MILLIMETERS
Die Size	131 x 136 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

Substrate Bias: $+V_{DD}$

DAC7801	MILS (0.001")	MILLIMETERS
Die Size	131 x 134 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

Substrate Bias: $+V_{DD}$

DAC7802	MILS (0.001")	MILLIMETERS
Die Size	131 x 121 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

Substrate Bias: $+V_{DD}$

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DAC7800

BLOCK DIAGRAM

PIN CONFIGURATION

DAC7800
Top View
DIP

AGND A	1	16	AGND B
$I_{OUT\,A}$	2	15	$I_{OUT\,B}$
$R_{FB\,A}$	3	14	$R_{FB\,B}$
$V_{REF\,A}$	4	13	$V_{REF\,B}$
CLK	5	12	V_{DD}
$\overline{UPD\,A}$	6	11	$\overline{CLR}$
Data In	7	10	$\overline{UPD\,B}$
$\overline{CS}$	8	9	DGND
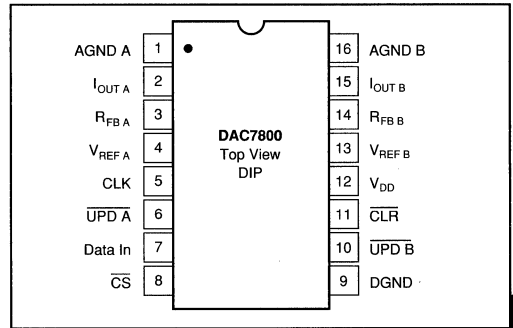
LOGIC TRUTH TABLE

CLK	$\overline{UPD\,A}$	$\overline{UPD\,B}$	$\overline{CS}$	$\overline{CLR}$	FUNCTION
X	X	X	X	0	All register contents set to 0's (asynchronous).
X	X	X	1	X	No data transfer.
⌐	X	X	0	1	Input data is clocked into input register (location Bit 23) and previous data shifts.
X	0	1	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A.
X	1	0	0	1	Input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.
X	0	0	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A, and input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.

X = Don't care. ⌐ means falling edge triggered.

DATA INPUT FORMAT

DAC7800 Digital Interface Block Diagram

DAC7800 Data Input Sequence
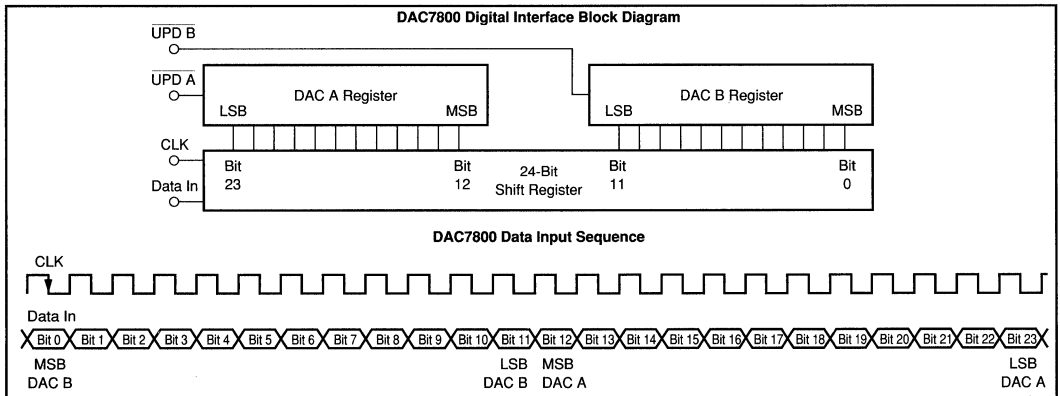
DAC7800 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1 — Data Setup Time	15ns
t_2 — Data Hold Time	15ns
t_3 — Chip Select to CLK, Update, Data Setup Time	15ns
t_4 — Chip Select to CLK, Update, Data Hold Time	40ns
t_5 — CLK Pulse Width	40ns
t_6 — Clear Pulse Width	40ns
t_7 — Update Pulse Width	40ns
t_8 — CLK Edge to $\overline{UPD\,A}$ or $\overline{UPD\,B}$	15ns

NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. t_R = t_F = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.
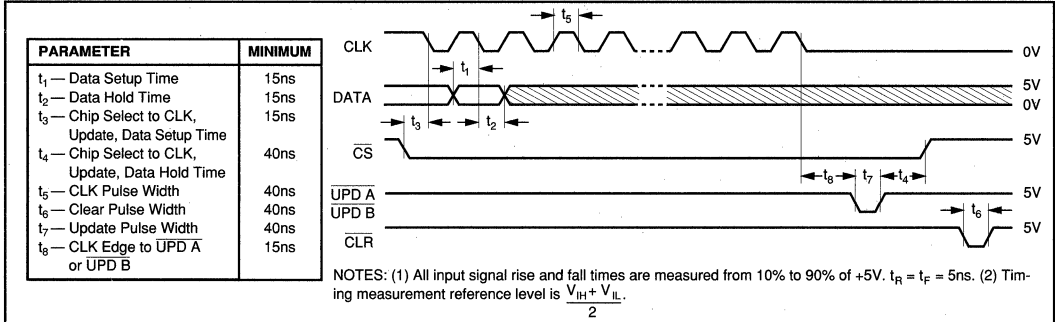
DAC7801

BLOCK DIAGRAM
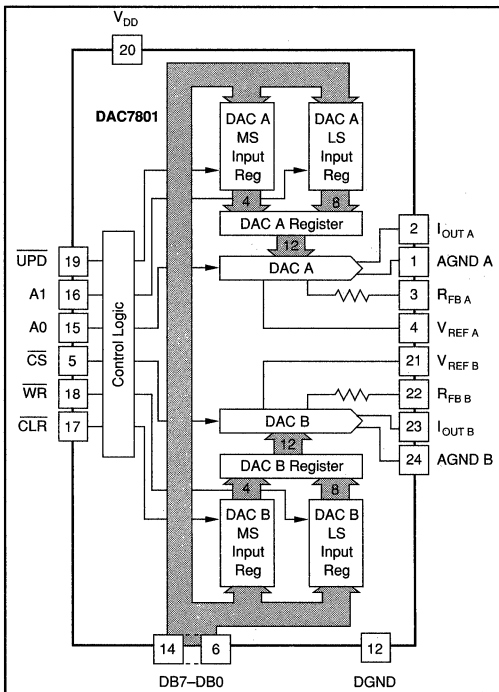
PIN CONFIGURATION
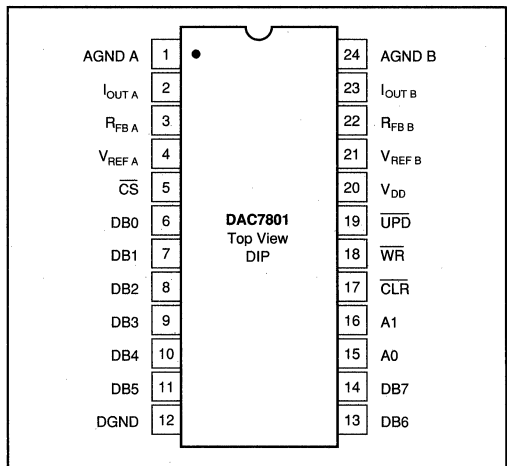
LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)–DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)–DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent
X = Don't care.						

DAC7801 (CONT)

TIMING CHARACTERISTICS

$V_{DD} = +5V$, $V_{REF\,A} = V_{REF\,B} = +10V$, $T_A = -40°C$ to $+85°C$.

PARAMETER	MINIMUM
t_1 — Address Valid to Write Setup Time	10ns
t_2 — Address Valid to Write Hold Time	10ns
t_3 — Data Setup Time	30ns
t_4 — Data Hold Time	10ns
t_5 — Chip Select or Update to Write Setup Time	0ns
t_6 — Chip Select or Update to Write Hold Time	0ns
t_7 — Write Pulse Width	40ns
t_8 — Clear Pulse Width	40ns
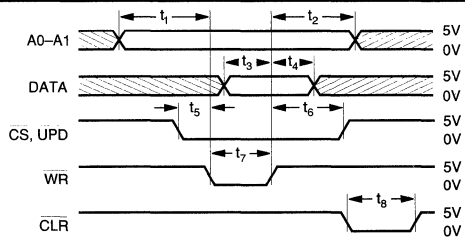
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F = 5ns$. (2) Timing measurement reference level is $\dfrac{V_{IH} + V_{IL}}{2}$.

DAC7802

BLOCK DIAGRAM

PIN CONFIGURATION

		DAC7802 Top View DIP		
AGND	1	●	24	$I_{OUT\,B}$
$I_{OUT\,A}$	2		23	$R_{FB\,B}$
$R_{FB\,A}$	3		22	$V_{REF\,B}$
$V_{REF\,A}$	4		21	V_{DD}
$\overline{CS\,A}$	5		20	$\overline{CS\,B}$
(LSB) DB0	6		19	$\overline{WR}$
DB1	7		18	DB11 (MSB)
DB2	8		17	DB10
DB3	9		16	DB9
DB4	10		15	DB8
DB5	11		14	DB7
DGND	12		13	DB6

LOGIC TRUTH TABLE

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
⌐	⌐	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC
0	1	⌐	DAC A Register Loaded from Data Bus
1	0	⌐	DAC B Register Loaded from Data Bus
0	0	⌐	DAC A and DAC B Registers Loaded from Data Bus

X = Don't care. ⌐ means rising edge triggered.

TIMING CHARACTERISTICS

At $V_{DD} = +5V$, and $T_A = -40°C$ to $+85°C$.

PARAMETER	MINIMUM
t_1 - Data Setup Time	20ns
t_2 - Data Hold Time	15ns
t_3 - Chip Select to Write Setup Time	30ns
t_4 - Chip Select to Write Hold Time	0ns
t_5 - Write Pulse Width	30ns

NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F = 5ns$. (2) Timing measurement reference level is $\dfrac{V_{IH} + V_{IL}}{2}$.

DAC7800/01/02

DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL PERFORMANCE CURVES

OUTPUT OP AMP IS OPA602.
$T_A = +25°C$, $V_{DD} = +5V$.

OUTPUT LEAKAGE CURRENT
vs TEMPERATURE

THD + NOISE vs FREQUENCY

CHANNEL-TO-CHANNEL ISOLATION
vs FREQUENCY

FEEDTHROUGH vs FREQUENCY

FREQUENCY RESPONSE

PSRR vs FREQUENCY

DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC780X is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figures 5 and 7.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT A}$ and $I_{OUT B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT A}$ or $I_{OUT B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within $\pm 0.01\%$ of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC780X. The current from the $V_{REF A}$ pin is switched between $I_{OUT A}$ and AGND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to $\pm 20V$.
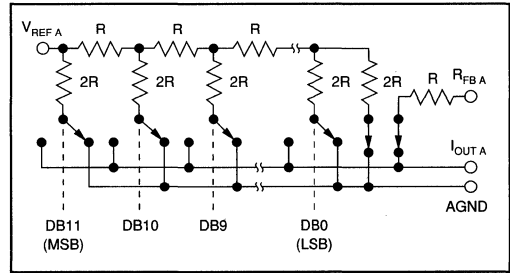
FIGURE 1. Simplified Circuit Diagram for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.
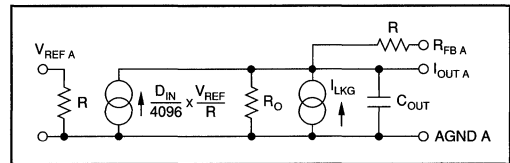
FIGURE 2. Equivalent Circuit for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC780X incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC780X are designed to operate on $V_{DD} = +5V \pm 10\%$. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1μF tantalum recommended) should be located close to the D/A. AGND and

DAC7800/01/02

DIGITAL-TO-ANALOG CONVERTERS

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DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pins of the DAC780X as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC780X directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC780X should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The non-linearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is non-linear with code, and the largest steps in R_O occur at major code transitions where the worst differential non-linearity is also likely to be experienced. The non-linearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good non-linearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC780X in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC780X in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table III.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE II. Unipolar Output Code.
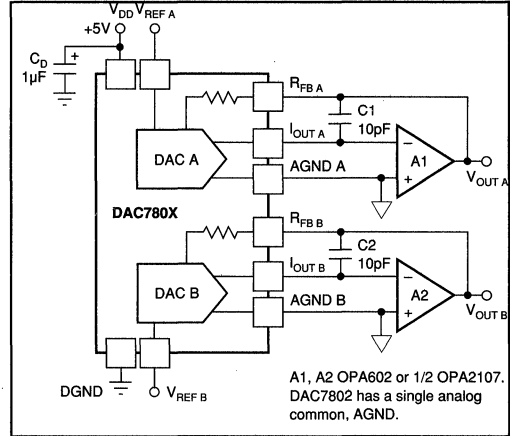
FIGURE 3. Unipolar Configuration.
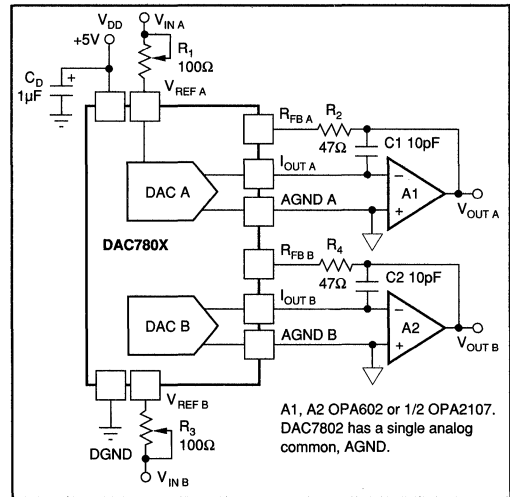
FIGURE 4. Unipolar Configuration with Gain Trim.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R5–R7 and R8–R10 should be ratio-matched to 0.01% to ensure the specified gain error performance.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 6 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE III. Bipolar Output Code.
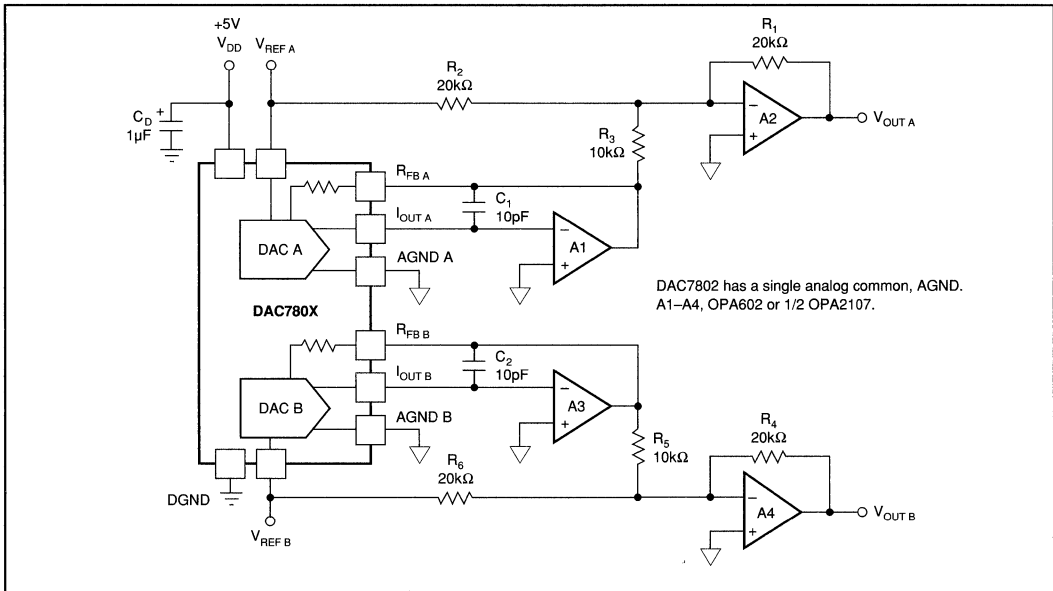
FIGURE 5. Bipolar Configuration.

APPLICATIONS

12-BIT PLUS SIGN DACS

For a bipolar DAC with 13 bits of resolution, two solutions are possible. As shown in Figure 7, the addition of a precision difference amplifier and a high speed JFET switch provides a 12-bit plus sign voltage-output DAC. When the switch selects the op amp output, the difference amplifier serves as a non-inverting output buffer. If the analog ground side of the switch is selected, the output of the difference amplifier is inverted.

Another option, shown in Figure 8, also produces a 12-bit plus sign output without the additional switch and digital control line.

DIGITALLY PROGRAMMABLE ACTIVE FILTER

DAC780X are shown in Figure 9 in a digitally programmable active filter application. The design is based on the state-variable filter, Burr-Brown UAF42, an active filter topology that offers stable and repeatable filter characteristics.

DAC1 and DAC2 can be updated in parallel with a single word to set the center frequency of the filter. DAC 4, which makes use of the uncommitted op amp in UAF42, sets the Q of the filter. DAC3 sets the gain of the filter transfer function without changing the Q of the filter. The reverse is also true.

The center frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance of the D/A (typical value, $10k\Omega$) and C the internal capacitor value (1000pF) of the UAF42. External capacitors can be added to lower the center frequency of the filter. But the highest center frequency for this circuit will be about 16kHz because the effective series resistance of the D/A cannot be less than $10k\Omega$.

Note that the ladder resistance of the D/A may vary from device to device. Thus, for best tracking, DAC2 and DAC3 should be in the same package. Some calibration may be necessary from one filter to another.

DAC7800/01/02

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DIGITAL-TO-ANALOG CONVERTERS
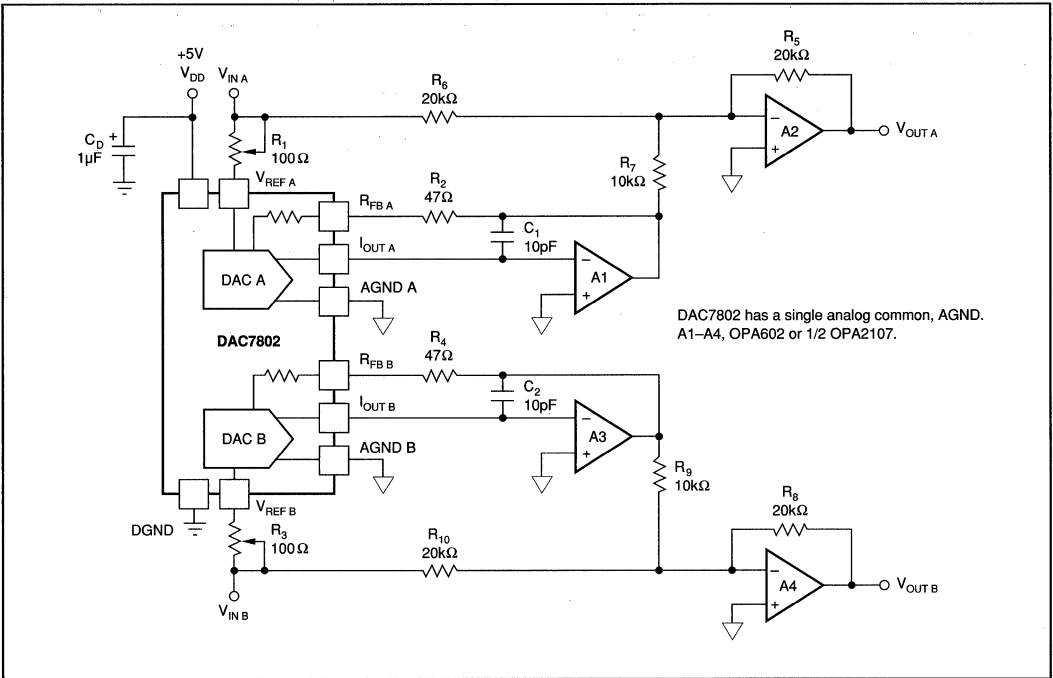
FIGURE 6. Bipolar Configuration with Gain Trim.
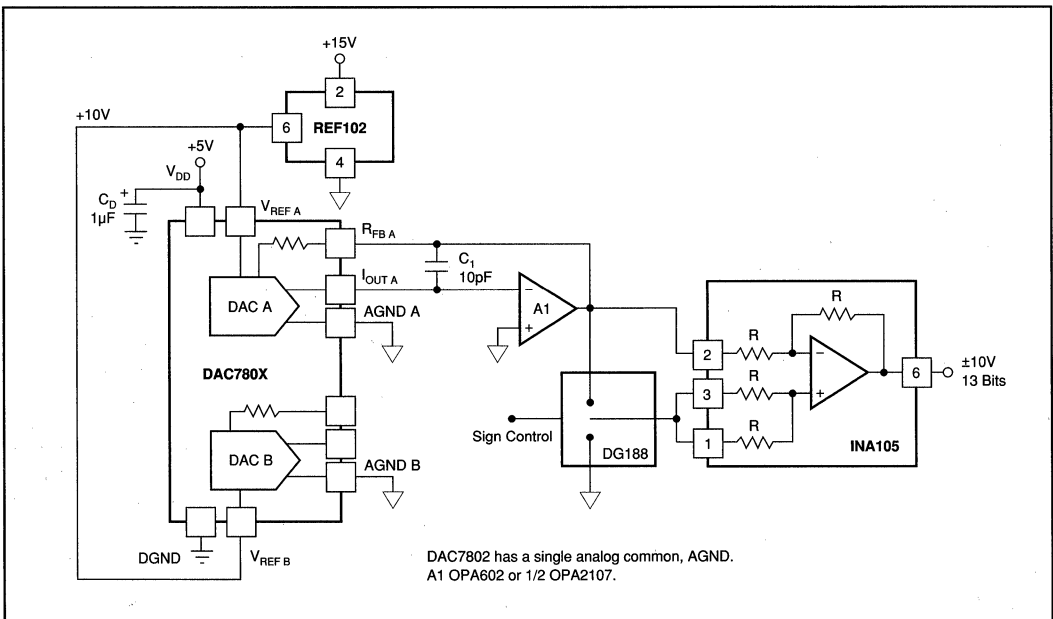
FIGURE 7. 12-Bit Plus Sign DAC.
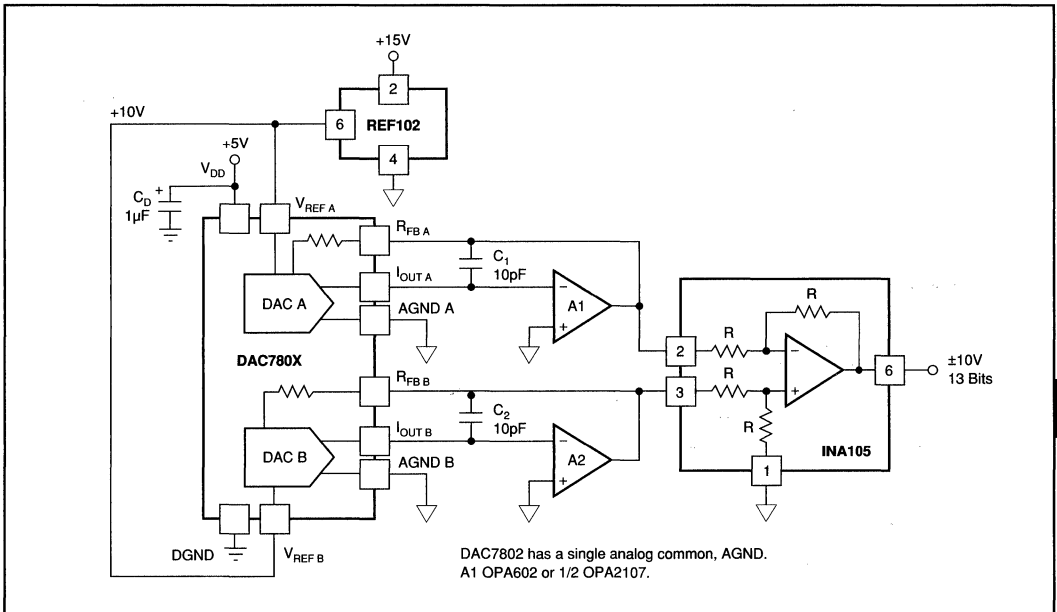
FIGURE 8. 13-Bit Bipolar DAC.

DAC7800 has a single analog common, AGND.
A1 OPA602 or 1/2 OPA2107.
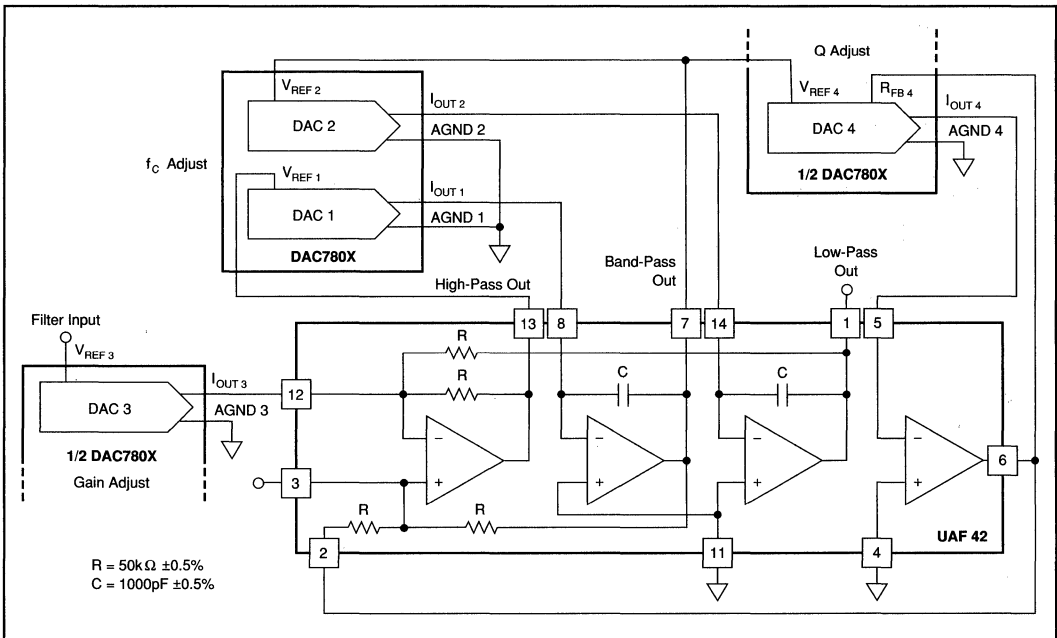
FIGURE 9. Digitally Programmable Universal Active Filter.

$R = 50k\Omega \pm 0.5\%$
$C = 1000pF \pm 0.5\%$

DAC7800/01/02

DIGITAL-TO-ANALOG CONVERTERS

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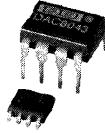
DAC8043

CMOS 12-Bit Mulitplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **12-BIT ACCURACY IN 8-PIN MINI-DIP AND 8-PIN SOIC**
● **FAST 3-WIRE SERIAL INTERFACE**
● **LOW INL AND DNL: ±1/2 LSB max**
● **GAIN ACCURACY TO ±1LSB max**
● **LOW GAIN TEMPCO: 5ppm/°C max**
● **OPERATES WITH +5V SUPPLY**
● **TTL/CMOS COMPATIBLE**
● **ESD PROTECTED**

APPLICATIONS

● **AUTOMATIC CALIBRATION**
● **MOTION CONTROL**
● **MICROPROCESSOR CONTROL SYSTEMS**
● **PROGRAMMABLE AMPLIFIER/ ATTENUATORS**
● **DIGITALLY CONTROLLED FILTERS**

DESCRIPTION

The DAC8043 is a 12-bit current output multiplying digital-to-analog converter (DAC) that is packaged in a space saving surface mount 8-pin SOIC and an 8-pin Mini-DIP. Its 3-wire serial interface saves additional circuit board space which results in low power dissipation. When used with microprocessors having a serial port, the DAC8043 minimizes the digital noise feedthrough from its input to output. The serial port can be used as a dedicated analog bus and kept inactive while the DAC8043 is in use. Serial interfacing reduces the complexity of opto or transformer isolation applications.

The DAC8043 contains a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial input (SRI) data is clocked into the input register on the rising edge of the clock (CLK) pulse. When the new data word had been clocked in, it is loaded into the DAC register by taking the $\overline{LD}$ input low. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043 operates from a single +5V power supply which makes the DAC8043 an ideal low power, small size, high performance solution for several applications.

PDS-1197A **BURR - BROWN** ®

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8043P, U MIN	DAC8043P, U TYP	DAC8043P, U MAX	DAC8043PC, UC MIN	DAC8043PC, UC TYP	DAC8043PC, UC MAX	UNITS
STATIC PERFORMANCE									
Resolution	N		12			12			Bits
Nonlinearity[1]	INL				±1			±1/2	LSB
Differential Nonlinearity[2]	DNL				±1			±1/2	LSB
Gain Error[3]	FSE	T_A = +25°C			±2			±1	LSB
		T_A = Full Temp Range			±2			±2	LSB
Gain Tempco[5]	TC_{FSE}				±5			±5	ppm/°C
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		±0.0006	±0.002		±0.0006	±0.002	%/%
Output Leakage Current[4]	I_{LKG}	T_A = +25°C			±5			±5	nA
		T_A = Full Temp Range			±100			±25	nA
Zero Scale Error[7, 12]	I_{ZSE}	T_A = +25°C			0.03			0.03	LSB
		T_A = Full Temp Range			0.60			0.15	LSB
Input Resistance[8]	R_{IN}		7	11	15	7	11	15	kΩ
AC PERFORMANCE									
Output Current Settling Time[5, 6]	t_S	T_A = +25°C		0.25	1		0.25	1	μs
Digital-to-Analog Glitch		V_{REF} = 0V		2	20		2	20	nVs
Energy[5, 10]	Q	I_{OUT} = Load = 100Ω							
		C_{EXT} = 13pF							
		DAC Register Loaded Alternately with all 0s and all 1s							
Feedthrough Error[5, 11]	FT	V_{REF} = 20Vp-p at f = 10kHz		0.7	1		0.7	1	mVp-p
(V_{REF} to I_{OUT})		Digital Input = 0000 0000 0000							
		T_A = +25°C							
Total Harmonic Distortion[5]	THD	V_{REF} = 6V$_{RMS}$ at 1kHz		−85			−85		dB
		DAC Register Loaded with all 1s							
Output Noise Voltage Density[5, 13]	e_N	10Hz to 100kHz		17			17		nV/√Hz
		Between R_{FB} and I_{OUT}							
DIGITAL INPUTS									
Digital Input High	V_{IH}		2.4			2.4			V
Digital Input Low	V_{IL}				0.8			0.8	V
Input Leakage Current[9]	I_{IL}	V_{IN} = 0V to +5V			±1			±1	μA
Input Capacitance[5, 11]	C_{IN}	V_{IN} = 0V			8			8	pF
ANALOG OUTPUTS									
Output Capacitance[5]	C_{OUT}	Digital Inputs = V_{IH}			110			110	pF
		Digital Inputs = V_{IL}			80			80	pF
TIMING CHARACTERISTICS[5, 14]									
Data Setup Time	t_{DS}	T_A = Full Temperature Range	40			40			ns
Data Hold Time	t_{DH}	T_A = Full Temperature Range	80			80			ns
Clock Pulse Width High	t_{CH}	T_A = Full Temperature Range	90			90			ns
Clock Pulse Width Low	t_{CL}	T_A = Full Temperature Range	120			120			ns
Load Pulse Width	t_{LD}	T_A = Full Temperature Range	120			120			ns
LSB Clock into Input Register to Load DAC Register Time	t_{ASB}	T_A = Full Temperature Range	0			0			ns
POWER SUPPLY									
Supply Voltage	V_{DD}		4.75	5	5.25	4.75	5	5.25	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}			500			500	μA
		Digital Inputs = 0V or V_{DD}			100			100	μA

NOTES: (1) ±1/2 LSB = ±0.012% of Full Scale. (2) All grades are monotonic to 12-bits over temperature. (3) Using internal feedback resistor. (4) Applies to I_{OUT}; All digital inputs = 0V. (5) Guaranteed by design and not tested. (6) I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_S = propagation delay (t_{PD}) + 9τ where τ = measured time constant of the final RC decay. (7) V_{REF} = +10V, all digital inputs = 0V. (8) Absolute temperature coefficient is less than ±50ppm/°C. (9) Digital inputs are CMOS gates: I_{IN} is typically 1nA at +25°C. (10) V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V. (11) All digital inputs = 0V. (12) Calculated from worst case R_{REF}; I_{ZSE} (in LSBs) = (R_{REF} X I_{LKG} X 4096)/V_{REF}. (13) Calculations from en = $\sqrt{4K\ TRB}$ where: K = Boltzmann constant, J/°K, R = resistance, Ω. T = Resistor temperature, °K, B = bandwidth, Hz. (14) Tested at V_{IN} = 0V or V_{DD}.

DAC8043

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DIGITAL-TO-ANALOG CONVERTERS

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... 0V, +7V
V_{REF} to GND .... ±25V
V_{RFB} to GND .... ±25V
Digital Input Voltage Range .... −0.3V to V_{DD}
Output Voltage (Pin 3) .... −0.3 V to V_{DD}
Operating Temperature Range
    AD .... 0°C to +70°C
    P, PC, U, UC .... −40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature .... −65°C to + 150°C
Lead Temperature (soldering, 10s) .... +300° C
$\theta_{JA}^{(1)}$
    U Package .... +100°C/W
    P Package .... +96°C/W
θ_{JC}
    U Package .... +42°C/W
    P Package .... +37°C/W

NOTE: (1) θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for PDIP packages.

CAUTION: 1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2). 2. The digital control inputs are ESD protected: however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. 3. Use proper anti-static handling procedures. 4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ORDERING INFORMATION

MODEL	INL	TEMPERATURE RANGE	PACKAGE
DAC8043P	1LSB	−40°C to +85°C	8-pin Plastic DIP
DAC8043PC	1/2LSB	−40°C to +85°C	8-pin Plastic DIP
DAC8043U	1LSB	−40°C to +85°C	8-pin SOIC
DAC8043UC	1/2LSB	−40°C to +85°C	8-pin SOIC

PACKAGING INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC8043P	8-Pin PDIP	006
DAC8043PC	8-Pin PDIP	006
DAC8043U	8-Pin SOIC	182
DAC8043UC	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION

Top View   8-Pin Plastic DIP
                                           8-Pin SOIC

V_{REF}	1	8 V_{DD}
R_{FB}	2	7 CLK
I_{OUT}	3	6 SRI
GND	4	5 $\overline{LD}$

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Digital Inputs: All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. V_{REF} and R_{FB} show some sensitivity.

WRITE CYCLE TIMING DIAGRAM

DICE INFORMATION

DAC8043 DIE TOPOGRAPHY

PAD	FUNCTION
1	V_{DD}
2	V_{REF}
3	R_{FB}
4	I_{OUT}
5	AGND
6	DGND
7	$\overline{LD}$
8	SRI
9	CLK

Substrate Bias: $+V_{DD}$.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	70x 110 ±5	1.78 x 2.79 ±0.13
Die Thickness	14 ±3	0.35 ±3
Min. Pad Size	4 x 4	0.1 x 0.1
Metallization		Aluminum
Backing		Chrome Silver

WAFER TEST LIMITS

At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	LIMIT	DAC8043 UNITS
STATIC ACCURACY				
Resolution	N		12	Bits min
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Gain Error	G_{FSE}	Using Internal Feedback Resistor	±2	LSB max
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% max
Output Leakage Current (I_{OUT})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA max
REFERENCE INPUT				
Input Resistance	R_{IN}		7/15	kΩ min/max
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V min
Digital Input LOW	V_{IL}		0.8	V max
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	µA max
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	500	µA max
		Digital Inputs = 0V to V_{DD}	100	µA max

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

DAC8043

DIGITAL-TO-ANALOG CONVERTERS

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TYPICAL PERFORMANCE CURVES

At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

LINEARITY ERROR vs REFERENCE VOLTAGE

GAIN vs FREQUENCY

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

TOTAL HARMONIC DISTORTION vs FREQUENCY
(Multiplying Mode)

LINEARITY ERROR vs DIGITAL CODE

DNL ERROR vs REFERENCE VOLTAGE

DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC8043 is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figure 4.

OUTPUT LEAKAGE CURRENT

The current which appears at I_{OUT} with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from I_{OUT} to GND.

FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within $\pm0.01\%$ of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of a DAC8043. The current from the V_{REF} pin is switched between I_{OUT} and GND by 12 single-pole double-throw CMOS switches. This main-

tains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to $\pm20V$.
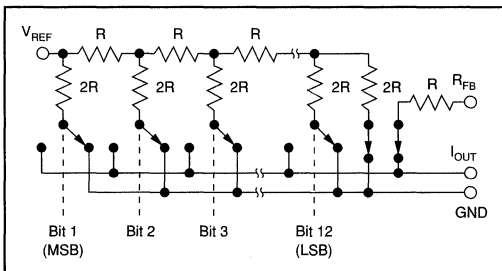
A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, R_{FB}, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for the DAC. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 80pF to 110pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.
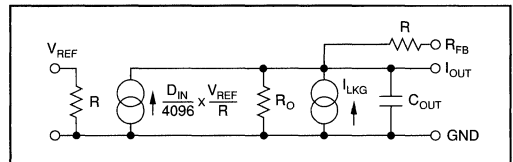
FIGURE 2. Equivalent Circuit for the DAC.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC8043 is designed to operate on $V_{DD} = +5V \pm5\%$. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1μF tantalum recommended) should be located close to the D/A. Output op amp analog common (+ input) should be connected as near to the GND pins of the DAC8043 as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Coupling from any of the digital control or data lines might degrade the glitch performance. Solder the DAC8043 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

FIGURE 1. Simplified Circuit Diagram for the DAC.

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC8043 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The non-linearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is non-linear with code, and the largest steps in R_O occur at major code transitions where the worst differential non-linearity is also likely to be experienced. The non-linearity seen at the amplifier output is

$$2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3.$$

Thus, to maintain good non-linearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC8043 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistor R2 induces a positive gain error greater than worst-case initial negative gain error. Trim resistor R1 provides a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC8043 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602 or a dual amplifier such as the OPA2107. C1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R1–R2 should be ratio-matched to 0.01% to ensure the specified gain error performance.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE I. Unipolar Output Code.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Output Code.

FIGURE 3. Unipolar Configuration.
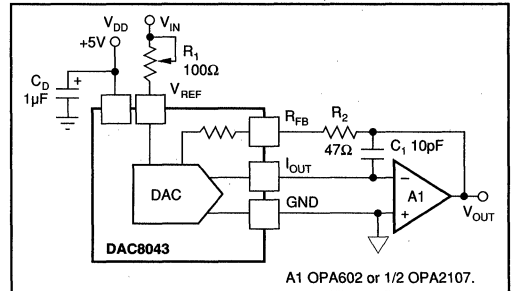
FIGURE 4. Unipolar Configuration with Gain Trim.

FIGURE 5. Bipolar Configuration.

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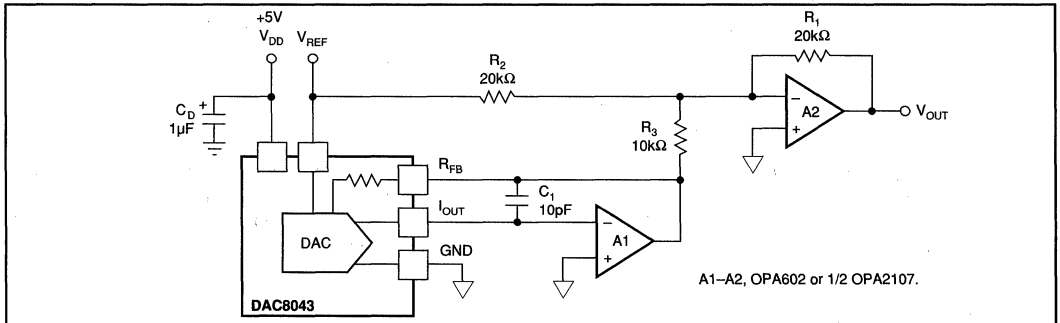
DSP201

DSP202

DSP201/202

DSP-Compatible Single/Dual
DIGITAL-TO-ANALOG CONVERTERS

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DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **ZERO-CHIP INTERFACE TO DSP ICs:**
  AD, AT&T, MOTOROLA, TI
● **SINGLE CHANNEL: DSP201**
● **DUAL CHANNEL: DSP202**
  Two Serial Inputs or Cascade from Single
  32-Bit Word
● **UPDATE RATE TO 500kHz**
● **DYNAMIC SPECIFICATIONS:**
  Signal/(Noise + Distortion) = 90dB;
  THD = –92dB
● **USER SELECTABLE 16-BIT OR 18-BIT**
  DATA WORDS

DESCRIPTION

The DSP201 and DSP202 are high performance digital-to-analog converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide analog output voltages updated at up to 500kHz.

The DSP201 offers a single complete voltage output channel, accepting either 16 bits or 18 bits of input data, and can be driven by 16-bit, 24-bit, or 32-bit serial ports. The DSP202 offers two complete voltage output channels, with either two separate input ports, or a mode to drive both output channels from a single 32-bit word.

Both the DSP201 and DSP202 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.

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SPECIFICATIONS

ELECTRICAL

T_A = 0°C to 70°C, Output Update Frequency, f_S, = 400kHz, V_A+ = V_D+ = +5V, V_A- = V_D- = −5V, unless otherwise specified.

PARAMETER	CONDITIONS	DSP201JP DSP202JP MIN	TYP	MAX	DSP201KP DSP202KP MIN	TYP	MAX	UNITS
RESOLUTION				18			*	Bits
DYNAMIC RANGE			108			*		dB
ANALOG OUTPUT								
Voltage Range	R_L = 375Ω		±3		*			V
Impedance			0.1			*		Ω
Current	R_L = 375Ω		±8			*		mA
Slew Rate	R_L = 1.5kΩ, C_L = 100pF		15			*		V/μs
Settling Time to 0.006%	R_L = 1.5kΩ, C_L = 100pF		2.5			*		μs
for Full-Scale Step								
THROUGHPUT SPEED [1]								
Update Rate	CASC = LOW on DSP202	500			*			kHz
DSP202 in Cascade Mode	CASC = HIGH	300						kHz
AC ACCURACY [2, 3]								
Signal to (Noise + Distortion) Ratio	f_{OUT} = 1kHz	82	86		88	90		dB[4]
	f_{OUT} = 1kHz (−60dB)		30			32		dB
	f_{OUT} = 10kHz	80	86		86	90		dB
Total Harmonic Distortion	f_{OUT} = 1kHz		−90	−85		−92	−88	dB
Channel Separation	f_{OUT} = 1kHz to 100kHz		105			*		dB
on DSP202								
DC ACCURACY								
Integral Nonlinearity Error			±0.006			±0.004		%
Differential Nonlinearity Error			±0.006			±0.004		%
Bipolar Zero Error [5]			±10			*		mV
Bipolar Zero Error Drift			20			*		ppm FSR/°C
Bipolar Zero Mismatch [5]	DSP202 Channels		5			*		mV
Gain Error			1	3		*	*	%
Gain Error Drift			100			*		ppm/°C
Gain Error Mismatch	DSP202 Channels		1	3		*	*	%
Digital Feedthrough	ENABLE = HIGH		−105			*		dB
Power Supply Sensitivity	−5.1 < V_A-, V_D- < −4.9		−60			*		dB
	+4.9 < V_A+, V_D+ < +5.1		−60			*		dB
DIGITAL INPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded					
Coding			Binary Twos Complement					
Logic Levels								
V_{IL}	I_{IL} = ±10μA	0		+0.8	*		*	V
V_{IH}	I_{IH} = ±10μA	+2.4		+5	*		*	V
Data Transfer Clock								
Frequency				12	*		*	MHz
Duty Cycle		40	50	60	*	*	*	%
DIGITAL OUTPUTS								
V_{OL}	I_{OL} = 4mA	0		+0.4	*		*	V
V_{OH}	I_{OH} = 4mA	+2.4		+5	*		*	V
POWER SUPPLIES								
Rated Voltage								
V_A+		+4.75	+5	+5.25	*	*	*	V
V_A-		−5.25	−5	−4.75	*	*	*	V
V_D+		+4.75	+5	+5.25	*	*	*	V
V_D-		−5.25	−5	−4.75	*	*	*	V
Current								
I_A+			18			*		mA
I_A-			17			*		mA
I_D+			13			*		mA
I_D-			25			*		mA
Power Consumption			365	450		*	*	mW
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		−40		+125	*		*	°C

NOTES: (1) The data transfer clock must be at least 24 times the update rate for the standard mode, and 40 times the update rate in the DSP202 Cascade Mode. (2) All dynamic specifications are based on 2048-point FFTs. (3) Data for the 1kHz test is bandlimited to 0 to 20kHz. Data for the 10kHz test is bandlimited to 0 to 40kHz. (4) All specifications in dB are referred to a full-scale output, ±3Vp-p. (5) Adjustable to zero with external potentiometer.

TYPICAL PERFORMANCE CURVES

T_A = +25°C; Update Frequency, f_S = 400kHz; V_A+ = V_D+ = +5V; V_A– = V_D– = 5V; SWL = HIGH; CASC = LOW; Output Bandwidth Limited to 20kHz; unless otherwise noted.

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DYNAMIC PERFORMANCE vs TEMPERATURE

f_{OUT} = 1kHz, ±3Vp-p

Signal-to-(Noise + Distortion) (SINAD)

Signal-to-Noise Ratio (SNR)

Total Harmonic Distortion (THD)

Spurious Free Dynamic Range (SFDR)

SINAD, SNR and SFDR (dB)

THD (dB)

Ambient Temperature (°C)

SIGNAL-TO-(NOISE + DISTORTION) RATIO vs TEMPERATURE AND AMPLITUDE

f_{OUT} = 1kHz, 0dB

f_{OUT} = 1kHz, –20dB

f_{OUT} = 1kHz, –60dB

Signal-to-(Noise + Distortion) Ratio (dB)

Ambient Temperature (°C)

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

f_{OUT} = 0dB
Output not band-limited.

Total Harmonic Distortion (dB)

Output Frequency (kHz)

SIGNAL-TO-(NOISE + DISTORTION) vs OUTPUT UPDATE RATE

f_{OUT} = 0dB
Output not band-limited.

Signal-to-(Noise + Distortion) Ratio (dB)

Output Update Rate (kHz)

INTEGRAL AND DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE (For Worst-Case Codes.)

Differential Non-Linearity

Integral Non-Linearity

Absolute Value of Error (%)

Ambient Temperature (°C)

BIPOLAR ZERO ERROR AND GAIN ERROR vs TEMPERATURE

Gain Error

Bipolar Zero Error

Bipolar Zero Error (mV)

Gain Error (% of 6V Full Scale Range)

Ambient Temperature (°C)

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; Update Frequency, f_S = 400kHz; V_A+ = V_D+ = +5V; V_A– = V_D– = 5V; SWL = HIGH; CASC = LOW;
Output Bandwidth Limited to 20kHz; unless otherwise noted.

OUTPUT VOLTAGE SETTLING TIME

POWER SUPPLY REJECTION vs
SUPPLY RIPPLE FREQUENCY

INTERMODULATION DISTORTION vs TEMPERATURE
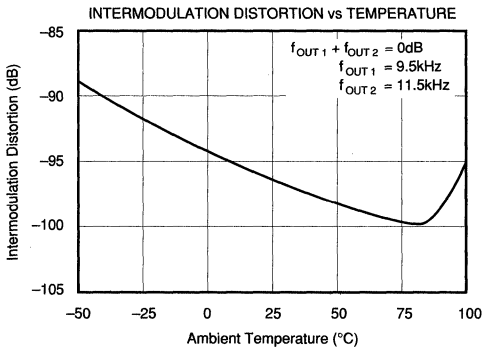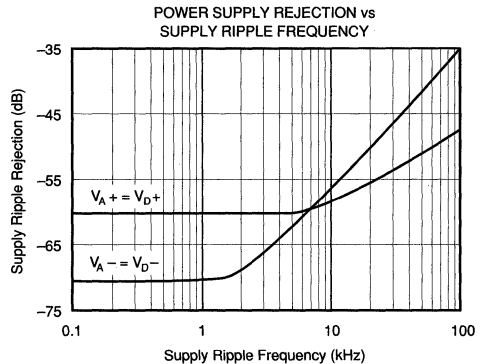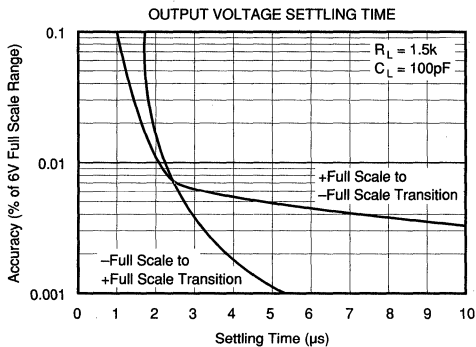
⚡ ELECTROSTATIC DISCHARGE SENSITIVITY

The DSP201 and DSP202 are ESD (electrostatic discharge) sensitive devices, and normal standard precautions should be taken. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DSP201JP	28-Pin Plastic DIP	215
DSP201KP	28-Pin Plastic DIP	215
DSP202JP	28-Pin Plastic DIP	215
DSP202KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A– to Analog Common	–7V
V_D+ to Digital Common	+7V
V_D– to Digital Common	–7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	50°C/W

ORDERING INFORMATION

MODEL	NUMBER OF CHANNELS	SIGNAL-TO- (NOISE + DIST.) RATIO, dB min
DSP201JP	1	82
DSP201KP	1	88
DSP202JP	2	82
DSP202KP	2	88

DSP201 PIN CONFIGURATION

```
              ┌──────⌒──────┐
    VA–   │ 1        28 │  AGND
          │ 2        27 │  DGND
          │ 3        26 │  VA+
    AGND  │ 4        25 │  VPOT
          │ 5        24 │  MSB
    VD+   │ 6        23 │  VOS
    VD+   │ 7  DSP201 22 │  AGND
    RESET │ 8        21 │  VOUT
    SSF   │ 9        20 │  VD–
    SWL   │ 10       19 │  DGND
    SYNC  │ 11       18 │  DGND
    XCLK  │ 12       17 │  ENABLE
    SIN   │ 13       16 │  DGND
          │ 14       15 │  CONV
              └─────────────┘
```

DSP201 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2		No Internal Connection.
3		No Internal Connection.
4	AGND	Analog Ground.
5		No Internal Connection.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	RESET	Reset. If LOW, DAC output will be 0V after two convert commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two convert commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP201 accepts first 16 bits of data. If LOW, DSP201 accepts first 18 bits of data.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SIN	Serial Data In. MSB first, Binary Two's Complement format.
14		No Internal Connection.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	DGND	Digital Ground.
17	ENABLE	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUT	Voltage Out.
22	AGND	Analog Ground.
23	VOS	VOS Adjust In.
24	MSB	MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustment.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

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DIGITAL-TO-ANALOG CONVERTERS

DSP202 PIN CONFIGURATION

V_A-	1		28	AGND
MSBB	2		27	DGND
VOSB	3		26	V_A+
AGNDB	4		25	VPOT
VOUTB	5		24	MSBA
V_D+	6		23	VOSA
V_D+	7	DSP202	22	AGNDA
$\overline{RESET}$	8		21	VOUTA
SSF	9		20	V_D-
SWL	10		19	DGND
SYNC	11		18	DGND
XCLK	12		17	$\overline{ENABLE}$
SINA	13		16	CASC
SINB	14		15	$\overline{CONV}$

DSP202 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2	MSBB	Channel B MSB Adjust In.
3	VOSB	Channel B VOS Adjust In.
4	AGNDB	Channel B Analog Ground.
5	VOUTB	Channel B Voltage Out.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{RESET}$	Reset. If LOW, DAC output will be 0V after two Convert Commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two Convert Commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP202 accepts first 16 bits of data. If LOW, DSP202 accepts first 18 bits of data. Must be HIGH if CASC is HIGH.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SINA	Channel A Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINB and to DSP IC output.
14	SINB	Channel B Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINA and to DSP IC output.
15	$\overline{CONV}$	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	CASC	Select Cascade Mode In. If HIGH, DSP202 accepts a 32-bit word, and uses the first 16 bits to update channel A, and the second 16 bits to update channel B. In Cascade Mode, SINA and SINB are connected together. If CASC is LOW, data is strobed into both channels on each clock cycle.
17	$\overline{ENABLE}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUTA	Channel A Voltage Out.
22	AGNDA	Channel A Analog Ground.
23	VOSA	Channel A VOS Adjust In.
24	MSBA	Channel A MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustments.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

THEORY OF OPERATION

The DSP201 and DSP202 are basic voltage output digital-to-analog converters with complete logic interface circuitry for ease of use with standard digital signal processing ICs. Data words are transmitted from the DSP IC on its serial port, leaving the DSP IC parallel ports free for digital communication.

The DSP201 and DSP202 are pipelined internally. When the user gives a convert command at time t, two actions are initiated. First, the data stored in the internal shift registers following the previous convert command (at t – 1) is used to update the output D/A converters immediately. Second, the DSP201 or DSP202 transmits a synchronization pulse to the DSP IC and starts clocking new data into the shift register using the system Bit Clock. This data is then used to update the D/As when the t + 1 convert command is received.

Both the DSP201 and DSP202 are 18-bit D/As internally. On-chip logic can be programmed to use 18-bits of data to update the D/A outputs, or can be programmed to update the D/A based on 16-bit data words. Additionally, the logic in the DSP202 can accept a 32-bit data word (the Cascade Mode), and update both D/A channels simultaneously with 16 bits each. All of these modes can be hard-wired or logic-controlled externally, so that no extra overhead on the part of the DSP IC is required.

In the 16-bit modes, the DSP201 and DSP202 will append zeros to the 16-bits transferred to each of the internal D/As, which are full 18-bit converters. The 18-bit word-length mode can be used with DSP ICs programmed for either 24-bit or 32-bit output words, in which case the DSP201 or DSP202 will clock in the first 18-bits of data after the synchronization pulse, and ignore additional information on the serial line. When programmed to accept 16-bit words, the DSP201 and DSP202 can be used with DSP ICs programmed to output 16-, 24-, or 32-bit words, and will ignore additional information after the first 16 bits on the serial line.

The DSP201 and DSP202 are complete voltage output D/A converters, with on-chip references and output amplifiers to drive ±3V into 375Ω loads. State-of-the-art bipolar technologies are used in the D/A section to maximize the output update rate, to maximize dynamic performance, and to eliminate glitch problems. Advanced plastic packaging methods makes this performance attainable economically.

BASIC OPERATION

DATA FORMAT AND OUTPUT LEVELS

The DSP201 and DSP202 accept serial data, MSB first, in standard Binary Two's Complement format. The length of the data words can be selected as shown below, and the D/A output level generated by a specific input code is shown in Table I.

As with all standard D/As, the output ranges from negative full scale (–3V) to 1 LSB below positive full scale (+3V – 1LSB). The bipolar output amplifiers are designed to drive 375Ω loads at full speed and accuracy.

UPDATING THE OUTPUT

With $\overline{\text{ENABLE}}$ (pin 17) LOW, the falling edge of a Convert Command arriving on CONV (pin 15) will immediately update the D/A outputs with the data stored in the internal shift registers following the previous Convert Command. The Convert Command can be asynchronous to any other signals or clocks without reducing accuracy, although system accuracy is often enhanced by synchronizing digital signals.

For a full-scale change in the input code, the output will typically settle to within ±0.006% of its final level within 2.5μs. The slew rate of the output amplifier is typically 15V/μs, for a full power bandwidth close to 800kHz. All of the specifications and typical performance curves are achieved with a full 400kHz update rate, unless otherwise specified. The DSP201 and DSP202 are guaranteed operational to a full 500kHz update rate, which exceeds the maximum Bit Clock rate for most standard DSP ICs.

DATA TRANSFER

Data is transmitted serially to the DSP201 or DSP202, and is clocked into the internal shift registers on the rising edge of the external Data Transfer Clock or Bit Clock (XCLK input on pin 12.) This clock can be as fast as 12MHz. The Data Transfer Clock can tolerate duty cycles from 40% to 60%.

As indicated in the timing diagrams in Figure 1, either 16- or 18-bits of data will be clocked into the DSP201 or DSP202, or 32-bits will be clocked into the DSP202 in the

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DIGITAL-TO-ANALOG CONVERTERS

INPUT CODE			OUTPUT VOLTAGE	
BINARY	16-BIT MODE AND DSP202 CASCADE MODE	HEX 18-BIT MODE	16-BIT MODE AND DSP202 CASCADE MODE	18-BIT MODE
0111...1111	7FFF	1FFFF	+2.999908V	2.999977V
0000...0000	0000	00000	0V	0V
1111...1111	FFFF	3FFFF	–92μV	–23μV
1000...0000	8000	20000	–3.000000V	–3.000000V
Theoretical LSB Size			91.6μV	22.9μV

TABLE I. Output Voltage vs Input Code.

DSP202 Cascade Mode (CASC = HIGH)
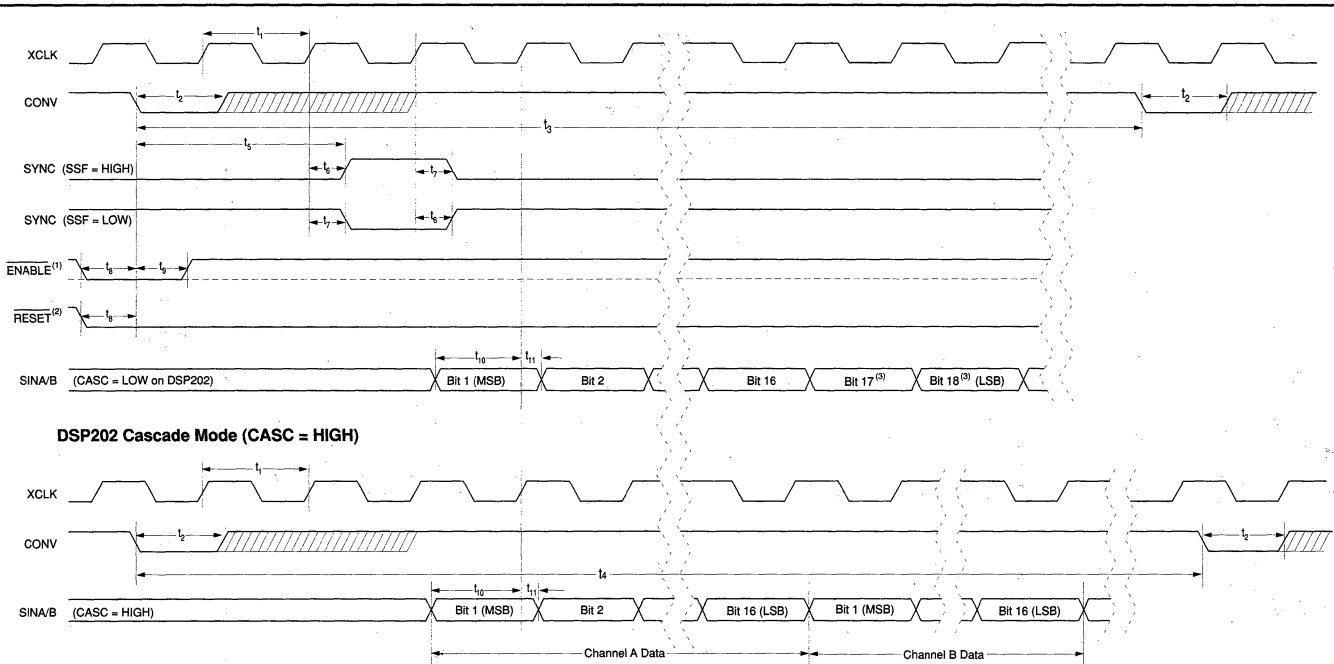
INTERVAL	DESCRIPTION	MIN	MAX	UNITS
t_1	XCLK period; Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP202)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP202	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge)	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising; C_L = 50pF		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising; C_L = 50pF		15	ns
t_8	ENABLE Setup before Convert Falling Edge[1]	50		ns
t_9	ENABLE Hold after Convert Falling Edge[1]	50		ns
t_8	RESET Setup before Convert Falling Edge	50		ns
t_{10}	SINA/B Data Setup before XCLK Rising	20		ns
t_{11}	SINA/B Data Hold after XCLK Rising		0	ns

NOTES: (1) Normally tied LOW so that previously transmitted data is used to update DAC output on falling edge of CONV. ENABLE HIGH prevents the DAC from being updated. (2) RESET must be held LOW for two complete Convert Command cycles, and ENABLE must be LOW. (3) Optional data bits. Clocked into DAC register only if SWL is LOW.

Cascade Mode, but internal digital overhead requires additional Data Transfer Clock cycles before a new Convert Command can be sent. The minimum time between Convert Commands is 24 times the Data Transfer Clock period for either the DSP201 or the DSP202 in standard modes, and 40 times the Data Transfer clock period for the DSP202 in the Cascade Mode. There is no maximum time between Convert Commands.

These additional clock cycles are used to set up the internal shift registers and logic, and are included in the specifications for maximum update rate. This means a 12MHz Bit Clock can achieve the maximum specified update rate of 500kHz.

DATA SYNCHRONIZATION

The DSP201 and DSP202 have internal logic to generate a synchronization pulse (SYNC on pin 11) to signal the host processor to transmit data. The synchronization pulse is sent when a Convert Command is received, and the SYNC output changes on the rising edge of XCLK. Timing is shown in Figure 1.

The synchronization pulse can be programmed to be either active High or active Low, depending on the logic level input on SSF (Select Sync Format on pin 9.) If SSF is LOW, SYNC will be normally HIGH, and will transmit a LOW pulse after a Convert Command is received. If SSF is HIGH, SYNC will be normally LOW, and will transmit a HIGH pulse after a Convert Command is received. The SYNC pulse will be as wide as one clock cycle on the Data Transfer Clock input on XCLK (pin 12.)

SELECTING WORD LENGTH

If the Select Word Length input (SWL, pin 10) is HIGH, the DSP201 or DSP202 will accept 16 bits of data after a Convert Command, with the timing shown in Figure 1. After these 16 bits, additional data on SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) will be ignored. Transparent to the user, the internal shift register will append two zeroes to the 16-bit data words before updating the D/As on the next Convert Command.

If SWL is LOW, the DSP201 or DSP202 will clock 18 bits of data into the internal shift register after a Convert Command, with the timing shown in Figure 1. Subsequent data on SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) will be ignored.

In the 16-bit mode, an increment of 1 LSB will change the D/A output by approximately 91.6µV (the 6V full scale range divided by 2^{16}), while an LSB in the 18-bit mode will change the output approximately 22.9µV ($6V/2^{18}$).

The DSP201 and DSP202 analog performance is tested in production using the 16-bit mode (with SWL HIGH), and the typical performance curves were generated using the 16-bit mode. Verification is made during final test that the 18-bit mode functions, but the extra resolution of these last two bits is not used when testing the analog performance.

DSP202 CASCADE MODE

If CASC on the DSP202 (pin 16) is HIGH, the Cascade Mode is implemented. In this mode, SINA (pin 13) and SINB (pin 14) are strapped together and connected to the serial output port of an appropriate DSP IC or other data word source. A Convert Command initiates the transfer of a 32-bit word to the DSP202.

In the Cascade Mode, care must be taken to make sure SWL (pin 10) is HIGH.

LATCH ENABLE

If ENABLE (pin 17) is LOW, the D/A outputs will be latched with new data on the falling edge of the Convert Command. Taking ENABLE HIGH causes the DSP201 or DSP202 to ignore Convert Commands. With ENABLE HIGH when a Convert Command arrives at time t, data latched in the internal shift register after the Convert Command at t − 1 is not latched to the D/As, but a new synchronization pulse is still generated and the data in the shift register is overwritten. This feature allows multiple DSP201s or DSP202s to share a single DSP IC and still be independently updated.

RESET

Taking RESET (pin 8) LOW will cause the D/As to output 0V after two Convert Commands are received. The two Convert Commands clear out the internal shift registers, and data input on the serial input lines will be ignored while RESET is low. This facilitates designing an analog output system that goes into a known, benign state either at power-up, after fault conditions or during a calibration cycle. ENABLE (pin 17) must be LOW when resetting the DSP201 or DSP202 outputs to 0V.

After RESET is taken HIGH, two Convert Commands are required before the output will relate to the input data. Also, ENABLE must be LOW for the data to be latched to the D/As. The first Convert Command again latches the outputs at 0V, and the second Convert Command drives the output to the level determined by the data clocked in after the first Convert Command.

A RESET command after power up is not required for proper operation of the DSP201 or DSP202.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP201 and DSP202, system design problems such as ground path resistance, contact resistance and power supply quality become very important.

GROUNDS

To achieve the maximum performance from the DSP201 or DSP202, care should be taken to minimize the effect of current flows in the system grounds that may corrupt the output voltages generated by the D/As. Pin 22 on the DSP201 and pins 4 and 22 on the DSP202 are the most

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DIGITAL-TO-ANALOG CONVERTERS

critical internal grounds, and care should be taken especially at these points to make them as close as possible to the same potential as the system analog ground. The design of the DSP201 and DSP202 insures that these pins will have minimal current flowing through them.

Internally, power currents are directed to the digital grounds (pins 18, 19, and 27) for internal digital currents, which are primarily switching currents, and to the analog grounds (pin 28, plus pin 4 on the DSP201) for analog currents, which are primarily from the internal current switches and the output amplifier. Pin 16 on the DSP201 is used internally as a logic level, and injects essentially no current into the ground.

Wherever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 92µV in 16-bit modes, and one quarter of that in 18-bit modes, the currents switched in a typical DSP system (processor, memory, etc.) can easily corrupt the output accuracy of the D/A's unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figures 2 and 3. For optimum performance of any high resolution D/A, all of the supplies need to be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-on.

Separate –5V analog and digital supplies are not needed. These pins are kept separate internally to minimize coupling. Drive pin 20 from the –5V analog supply, and make sure that the decoupling shown in Figure 2 or 3 are placed as close as possible to the D/As.

CALIBRATION AND ADJUSTMENT
OPTIONAL EXTERNAL OFFSET AND MSB TRIMS

All of the specifications for the DSP201 and DSP202, plus the typical performance curves, are based on the performance of these D/As without external trims. In most applications, external trims are not required.

If external trims are not used, pins 23, 24, and 25 on the DSP201 should be left open, as should pins 2, 3, 23, 24 and 25 on the DSP202. These pins should not be decoupled with capacitors or tied to any specific potential, or the noise on the D/A outputs may increase.

ADJUSTING OFFSET

Where required by specific applications, offsets can be trimmed using the circuits in Figure 2 (DSP201) or Figure 3 (DSP202.) As with all standard D/As, offset on the DSP201 and DSP202 means the difference of the output from the ideal negative full scale value. The DSP201 and DSP202 use a current switching D/A architecture, and the current from this is internally amplified to produce a ±3V output range. Negative full scale output thus results from having all of the internal current switches turned off. Offset on the DSP201 and DSP202 should not be confused with the delta from 0V with an input code of 0000...0000 (0000 hex for 16-bit Modes, 00000 hex for 18-bit Modes). This is often described as bipolar zero error, and includes the effects of both offset and gain error.

To trim the offsets, first latch the D/As with 1000...0000 (8000 hex or 20000 hex). Then adjust the offset adjustment pots to produce an output of –3.000000V.

ADJUSTING THE MSB WEIGHT

The MSB adjustment circuitry shown in Figure 2 for the DSP201 and in Figure 4 for the DSP202 basically change the weight of the MSB by adding to or subtracting from the current controlled by the internal MSB switch.

Depending on the application, the MSB adjustments can be made in one of three different ways to optimize the system performance using the DSP201 or DSP202. For dynamic performance, the MSB can be adjusted to minimize distortion of either a full-scale or low level sine-wave output. For applications stressing differential linearity, the 0000...0000 (0000 hex or 00000 hex) to 1000...0000 (FFFF hex or 3FFFF hex) transition can be trimmed to change the output of the D/As precisely 1 LSB (92µV in the 16-bit Mode or 23µV in the 18-bit Mode.)

To adjust for minimum distortion of full-scale sinewaves, strobe the inputs to the DSP201 or DSP202 with codes representing ideal full scale sine waves, then trim the MSB adjustment circuit to minimize distortion, as measured by either a distortion analyzer or by digitizing the output with an appropriate A/D and running FFT analyses.

In many audio applications, it is more appropriate to adjust for minimum distortion with low level sinewave outputs. This minimizes zero-crossover error, which can be a concern in high-end audio systems. To do this, strobe the inputs to the DSP201 or DSP202 with codes representing ideal low-level sine waves (–60dB from full scale works well), and then trim the MSB adjustment circuit to minimize distortion, again using a distortion analyzer or FFT analyses to check the results of the trims.

The MSB adjustment circuits can also be used to trim the D/A outputs directly for the transition from 0000...0000 (0000 hex or 00000 hex) to 1111...1111 (FFFF hex or 3FFFF hex), eliminating differential linearity error at the major carry. Ideally, this transition of the digital input code should cause the D/A outputs to change 92µV in the 16-bit Mode or 23µV in the 18-bit Mode. A simple way to make this adjustment is to continually load alternately the codes 1111...1111 (FFFF hex or 3FFFF hex) and 0000...0000 (0000 hex or 00000 hex) into the DSP201 or DSP202. An amplifier with sufficient gain can then drive an oscilloscope input, and the transition output step can be adjusted.

An alternative for calibrating on a bench is to tie SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) HIGH, and provide a Bit Clock and periodic Convert Commands. This loads 1111...1111 (FFFF$_{HEX}$ or 3FFFF$_{HEX}$), driving the output to 1LSB below 0V. Then periodically bring $\overline{RESET}$ (pin 8) LOW for at least two Convert Commands, which is the equivalent of loading all 0s, so the output is 0V. Now the output can be adjusted for an ideal transition step.

ADJUSTING BIPOLAR ZERO ERROR

If it is important in a specific application to adjust bipolar zero error, the user should first adjust the MSB trim circuits, and then use the offset adjust circuits to adjust the outputs to 0V with input codes of all 0s (0000...0000; 0000 hex or 00000 hex.) In this case, it is not possible to also trim offset at −Full Scale, as described above.

GAIN ERROR

Gain error on the DSP201 or DSP202 cannot be directly adjusted. If required in a specific application, gain can be trimmed out at the system level by adjusting the gain used in an output amplifier stage, such as would be used in any active output filter. In this case, the bipolar zero error should be adjusted first as discussed above. Then, the gain on the output amplifier should be adjusted to minimize the deviation from ideal for −Full Scale (1000...000; 8000 hex or 20000 hex) and +Full Scale (0111...1111; 7FFF hex or 1FFFF hex.)
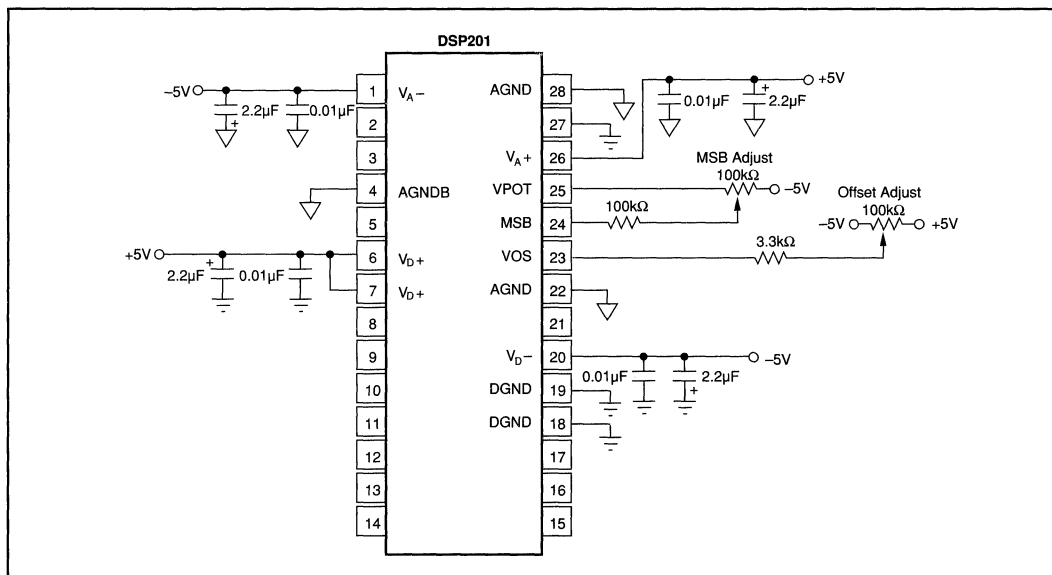
FIGURE 2. DSP201 Power Supply Connections and Optional Adjust Circuits.

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DIGITAL-TO-ANALOG CONVERTERS
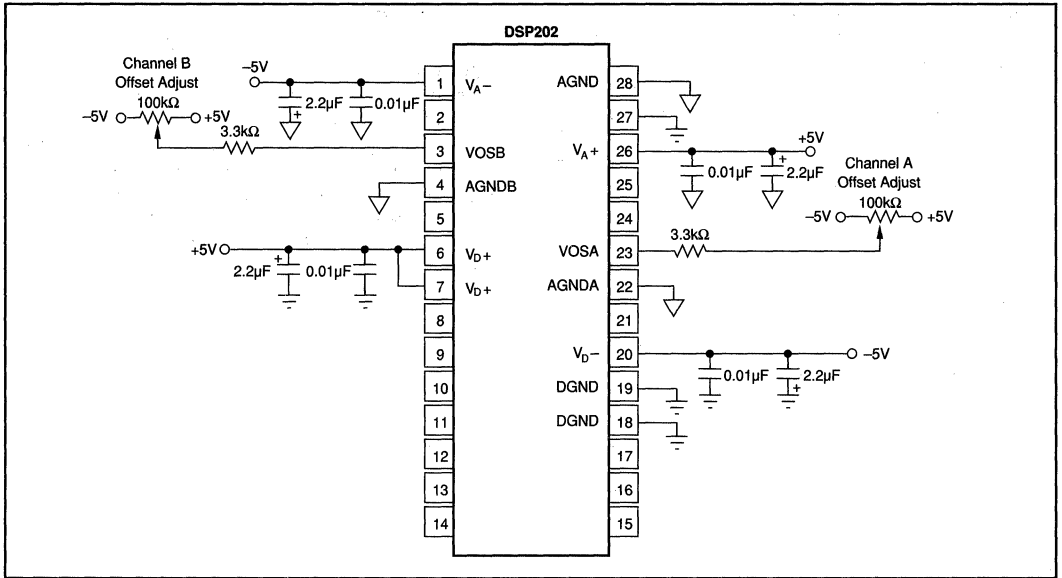
FIGURE 3. DSP202 Power Supply Connections and Optional Offset Voltage Adjustment.
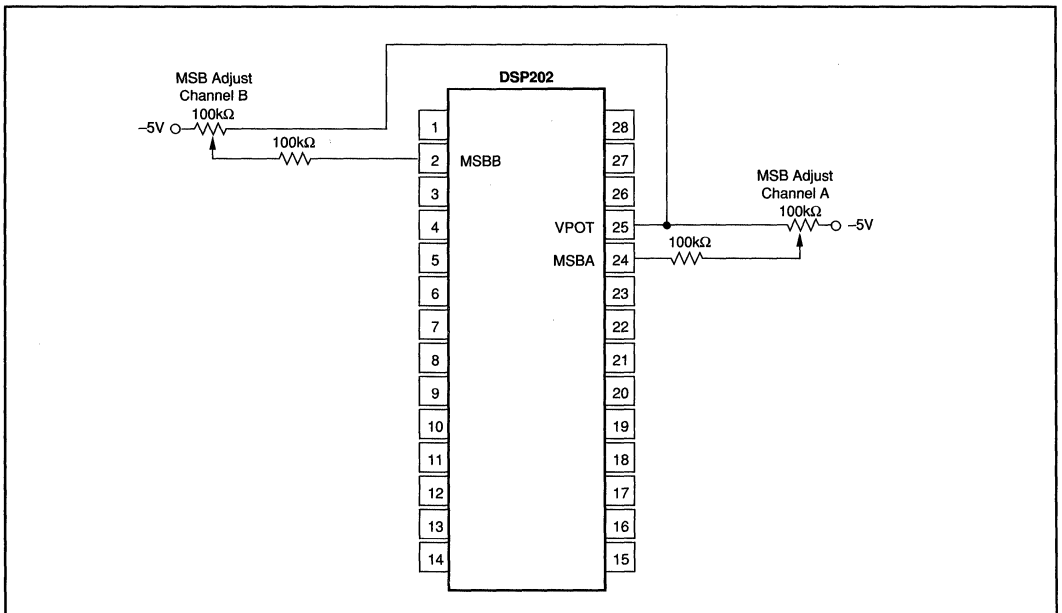
FIGURE 4. DSP202 Optional MSB Adjust Circuit.

APPLICATIONS

USING PARALLEL PORTS WITH THE DSP201 OR DSP202

Figure 5 shows a circuit for converting parallel outputs into the serial data stream required by the DSP201, and meets the requirements for timing signals. Doubling this circuit allows the DSP202 to be driven from a 32-bit parallel port. In most applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

DEGLITCHING

Particularly in high resolution D/A converters, changing input codes may cause glitching on the output that excessively corrupts the dynamic purity of an output signal. The DSP201 and DSP202 are designed to minimize output glitching, and all of the performance specifications and typical performance curves are based on tests with no extra deglitching circuitry. In particular, the guaranteed Signal-to-(Noise + Distortion) performance would be impossible to attain with any significant glitching.

COMPLETE ANALOG INPUT/OUTPUT SYSTEM

The DSP201 or DSP202 can be paired with the Burr-Brown DSP101 or DSP102 analog-to-digital converter to provide both analog input and analog output for a complete digital signal processing system. The DSP101 and DSP102 are respectively single and dual channel 200kHz sampling A/Ds with easy to use interfacing logic that complement the DSP201 and DSP202. Figure 6 shows a single channel analog input and output system based on a DSP201 and a DSP101, and the minimal connections required to interface to a DSP IC. A pair of channels can be implemented using a single DSP202 and a single DSP102, either with two separate DSP ICs, with a single DSP IC with dual serial input and output channels, or a single DSP IC capable of 32-bit words in the Cascade Mode.

For maximum flexibility in system design, the DSP201 or DSP202 D/As can be updated at a different rate than the conversion rate used on the DSP101 or DSP102 A/Ds, and either or both of these rates can be asynchronous to the clocks used with the DSP IC.
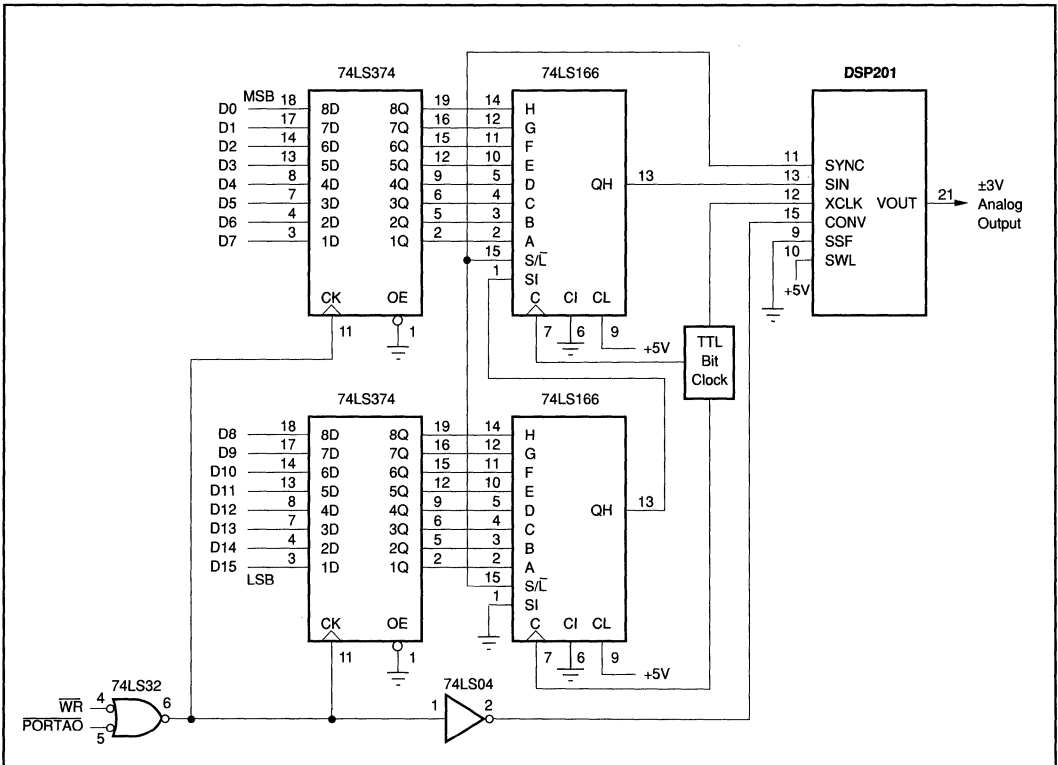
FIGURE 5. Driving the DSP201 from a 16-Bit Parallel Port.

DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	*SSF	**SWL
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

*See Burr-Brown DSP101/102 product data sheet for full description of this ADC.
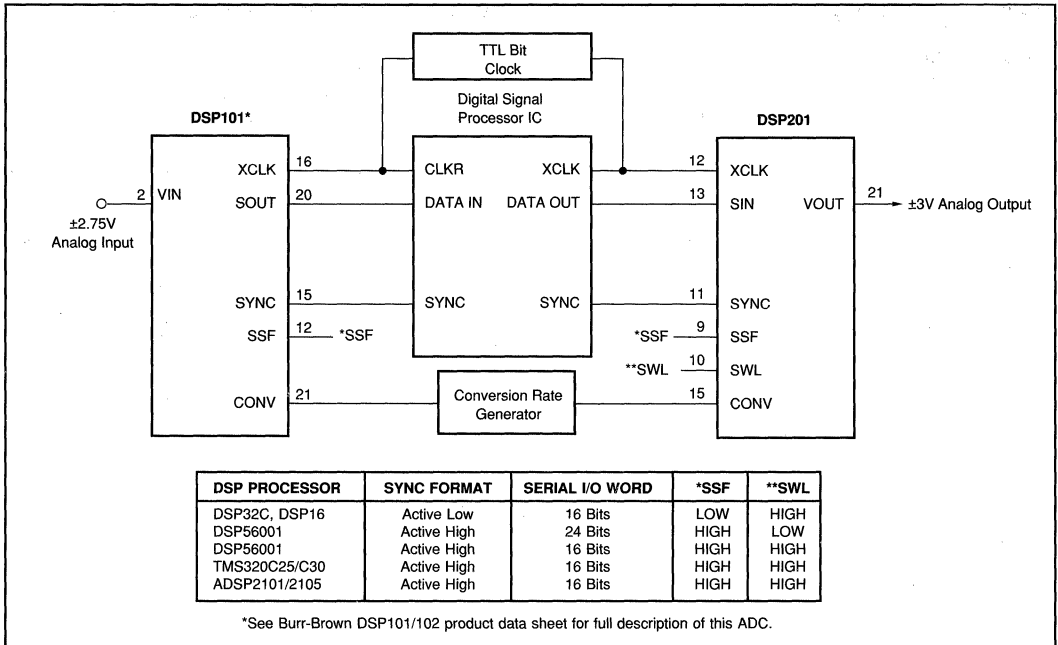
FIGURE 6. Analog Input and Analog Output System.

DIGITAL SIGNAL PROCESSOR	SYNC FORMAT	DATA LENGTH
DSP32C	Logic 0	16-Bit, Logic 1
DSP16	Logic 1	16-Bit, Logic 1
DSP56001 in 16-bit Mode	Logic 1	16-Bit, Logic 1
DSP56001 in 24-bit Mode		24-Bit, Logic 0
TMS320C25	Logic 1	16-Bit, Logic 1
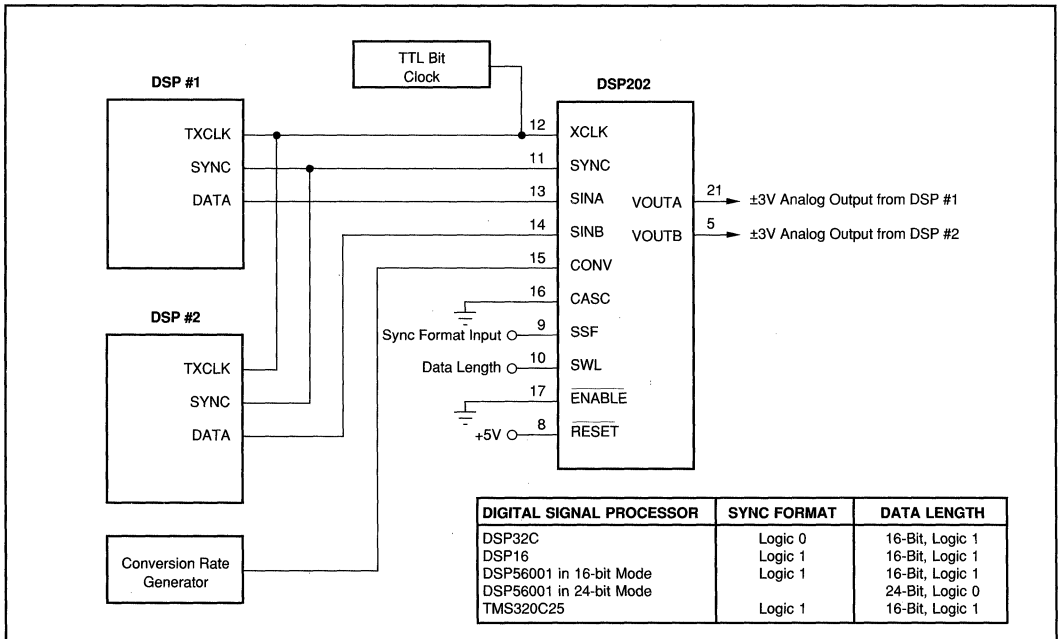
FIGURE 7. DSP202 with Dual DSP ICs.

USING DSP201 AND DSP202
WITH TEXAS INSTRUMENTS DSP ICS

Figures 6 thru 12 show various ways to use the DSP201 and DSP202 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are based on using the TMS320Cxx in the mode where SSF (Select Synch Format, pin 9) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP201 or DSP202 after receiving a Convert Command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing basic operation of the D/As. The timing for either synchronization mode is shown in Figure 1.

In all cases, the DSP201 and DSP202 expect to receive the data with the MSB first, and the TMS320Cxx needs to be programmed for this.

Figure 6 shows a circuit for using the TMS320C25 to generate a complete analog input and analog output system using the DSP201 plus the Burr-Brown DSP101 A/D.

Figure 7 shows how to use two TMS320C25 chips to drive the two channels of the DSP202.

The TMS320C30 has dual serial I/O ports, which can be used to drive the dual inputs on the DSP202, as shown in Figure 8. This circuit can maximize the update rate for the channels. Since the TMS320C30 can also output 32-bit words, both channels of the DSP202 can be updated from a single serial output port on the TMS320C30, using the cascade mode as shown in Figure 9.

Figures 10 and 11 show complete two-channel analog input and analog output systems consisting of three basic chips, the TMS320C30 plus a DSP202 dual D/A and a Burr-Brown DSP102 dual A/D. Figure 10 makes use of the dual serial I/O ports on the TMS320C30, and is shown with the DSP202 in the 16-bit Mode, which maximizes the possible throughput rate on the system. Figure 11 makes use of the 32-bit word length mode in the TMS320C30 and the Cascade Mode on both the DSP202 and the DSP102 to provide two full analog I/O channels over a single serial I/O port on the TMS320C30. Thus, up to four complete, separate analog I/O channels could be operated using a single TMS320C30, by making use of the second serial port.

Figure 12 shows how to use a TMS320C25 to update the analog output of the DSP201.

USING DSP201 AND DSP202
WITH MOTOROLA DSP ICS

Figure 13 shows how to use the DSP201 with a Motorola DSP56001. Using the DSP202 requires using two DSP56001s, as indicated in Figure 7.

The DSP56001 needs to be programmed for transmission of the MSB bit first with SYNC in the Bit Mode. If the DSP56001 is programmed for 16-bit data words, SWL (pin 10) on the DSP201 or DSP202 needs to be tied HIGH to select the 16-bit Mode. In the DSP56001 24-bit mode, the DSP201 or DSP202 can be programmed to accept data lengths of 16-bits (with SWL HIGH) or 18-bits (with SWL LOW), and will ignore the trailing bits on the serial line.

For use with the Motorola DSP56001, SSF (pin 9) on the DSP201 or DSP202 needs to be tied HIGH. This will cause the DSP201 or DSP202 to transmit an appropriate active High synchronization pulse on SYNC (pin 11) after a Convert Command is received by the DSP201 or DSP202. Timing is shown in Figure 1.

Even though the DSP201 or DSP202 require a minimum of 24 Bit Clock pulses between convert commands, the maximum update rate for the D/As using a 5MHz Bit Clock will still be over 200kHz (5MHz / 24 = 208.3kHz.)

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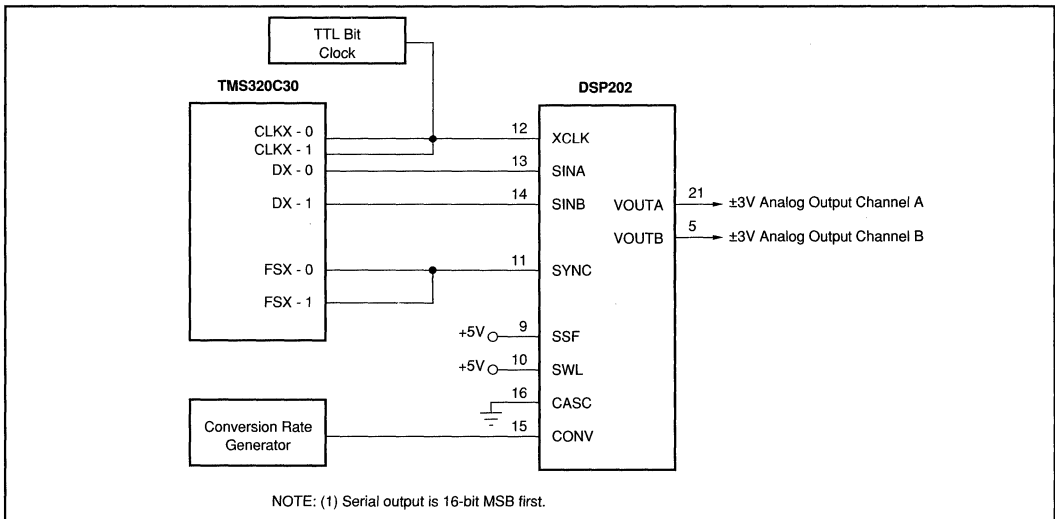
FIGURE 8. Using DSP202 with TMS320C30's Dual SIO.
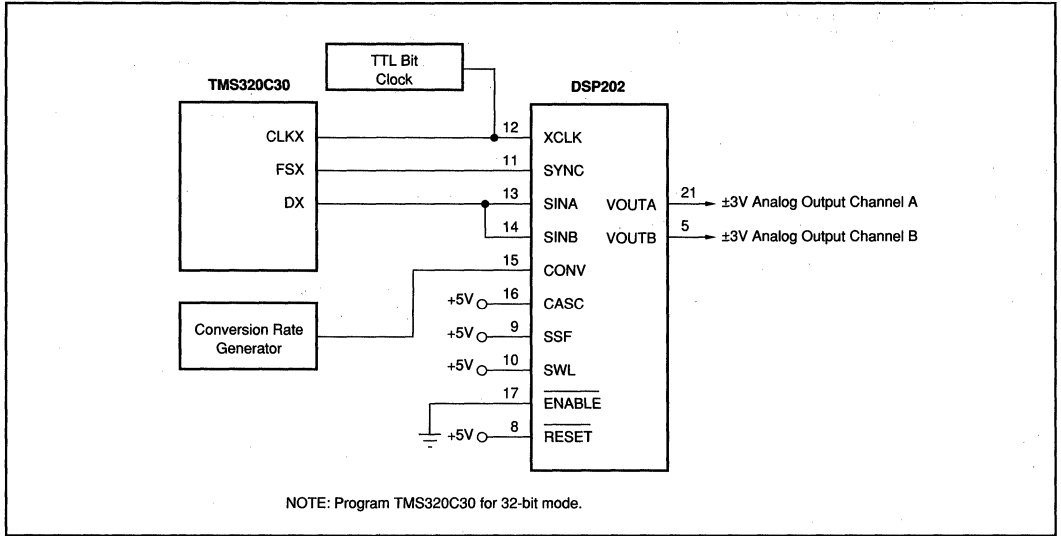
FIGURE 9. Using DSP202 with TMS320C30 in Cascade Mode.
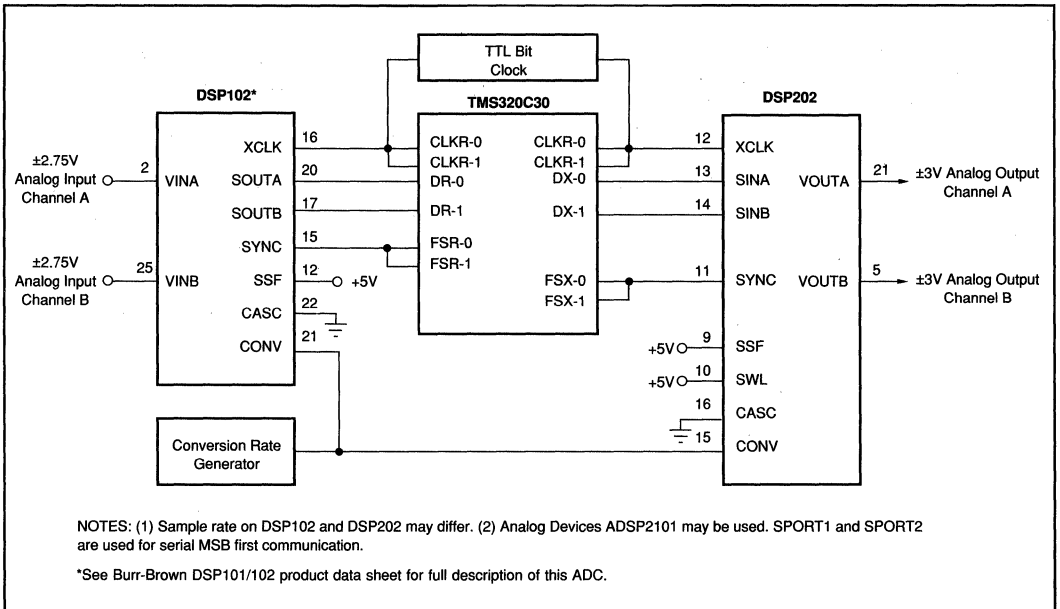
FIGURE 10. Two-Channel Analog Input and Output System with TMS320C30.

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DIGITAL-TO-ANALOG CONVERTERS

NOTES: (1) Program TMS320C30 for 32-bit mode. (2) Sample rate on DSP102 and DSP202 may differ. (3) DSP32C may also be used in this mode, with SSF pins tied LOW. *See Burr-Brown DSP101/DSP102 product data sheet for full description of this ADC.
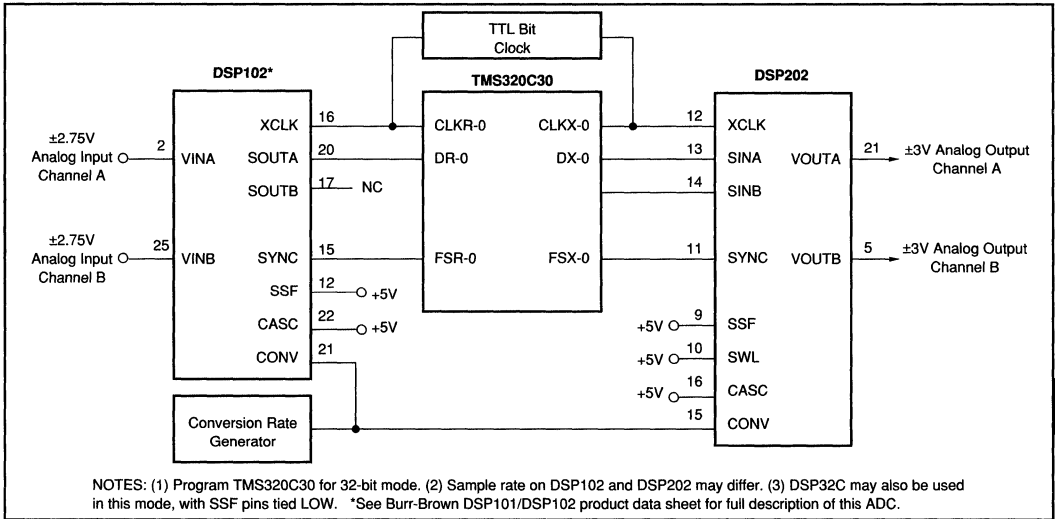
FIGURE 11. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

NOTE: FSX is programmed for external mode.
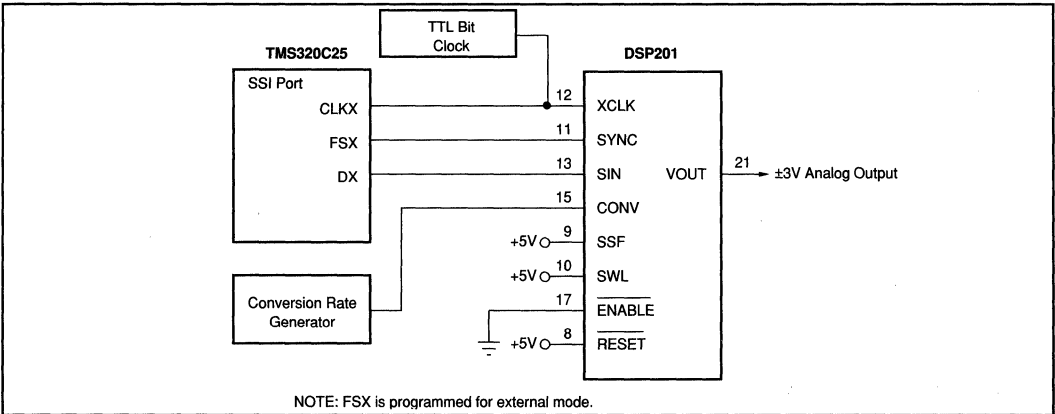
FIGURE 12. Using DSP201 with TMS320C25.

NOTES: (1) DSP56001 programmed for MSB bit first. (2) For 16-bit data connect SWL to Logic 1; For 24-bit data connect SWL to Logic 0.
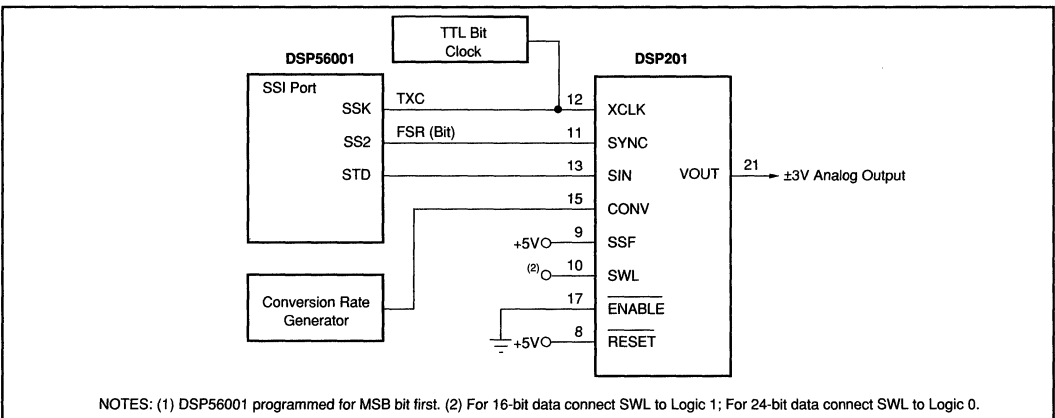
FIGURE 13. Using DSP201 with DSP56001.
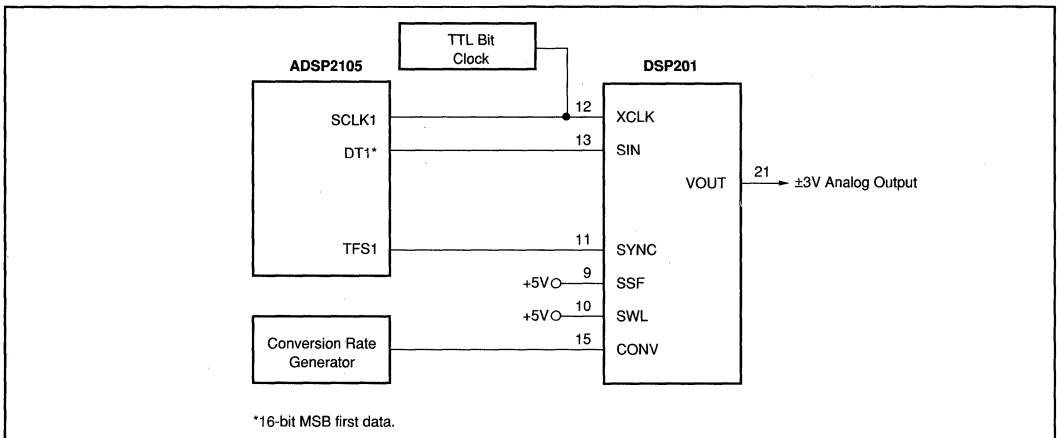
FIGURE 14. Using DSP201 with ADSP-2105.

USING DSP201 AND DSP202 WITH ADI DSP ICS

When using the DSP201 or DSP202 with the ADSP2101 or ADSP2105, the processors need to be programmed to transmit the data with the MSB first.

Figure 14 shows the connections required to generate an analog output channel using an ADSP2105 with the DSP201. The same basic circuit can also be used to connect a DSP201 to the ADSP2101.

Figure 6 indicates how to build a complete analog input and analog output system using either the ADSP2101 or ADSP2105 with a DSP201 and a Burr-Brown DSP101 A/D.

The two serial ports on the ADSP2101 can also be used with the DSP202 to make two complete analog output channels as noted in footnote 2 of Figure 10.

USING DSP201 AND DSP202 WITH AT&T DSP ICS

Figures 15, 16 and 17 show how to use the DSP201 and DSP202 with the DSP16 and DSP32C in different modes. The DSP IC needs to be programmed to transmit data with the MSB first, and the DSP201 or DSP202 needs to have SSF (Select Sync Format on pin 9) tied LOW so that the

D/As will output an appropriate active Low synchronization pulse after a Convert Command is received.

Figures 15 and 17 show the DSP32C and DSP16 respectively used with the DSP201 in the 16-bit Mode to generate a single analog output channel. With a 12MHz Bit Clock and the 24 Bit Clock cycles required by the DSP201 and DSP202 between Convert Commands, the output of Figure 15 can be updated at a full 500kHz (12MHz/24 = 500kHz.)

Figure 16 shows how to drive two analog output channels from a single 32-bit serial port on the DSP32C, using the Cascade Mode on the DSP202. With a 12MHz Bit Clock and the 40 Bit Clock cycles required between Convert Commands by the DSP for internal logic overhead, this circuit can update two separate analog outputs at 300kHz each from a single serial port (12MHz/40 = 300kHz.)

Figure 6 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP201 and a Burr-Brown DSP101 A/D.

Figure 7 shows a two channel analog output system using a single DSP202 with two DSP32Cs or two DSP16s.

NOTES: DSP32C programmed for MSB bit first. Data length 16 bit. External OCK, ILD.
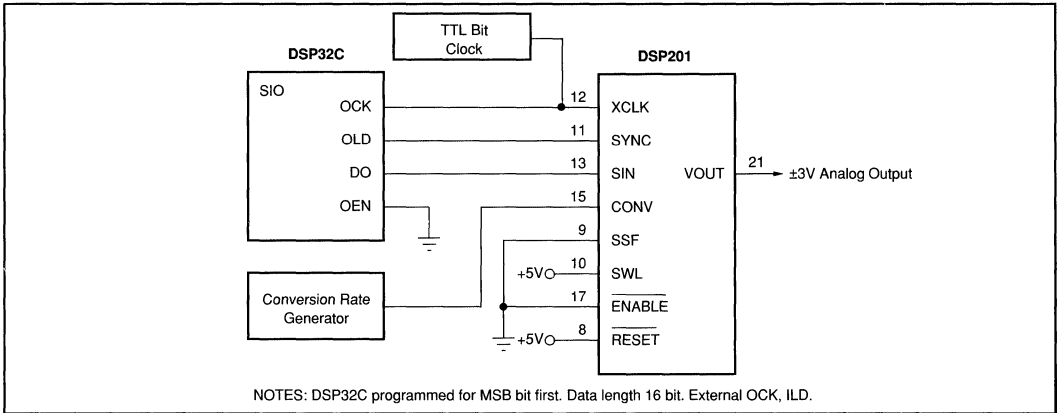
FIGURE 15. Using DSP201 with DSP32C with 16-Bit Data Words.

NOTE: (1) DSP16 programmed for MSB bit first 16-bit data.
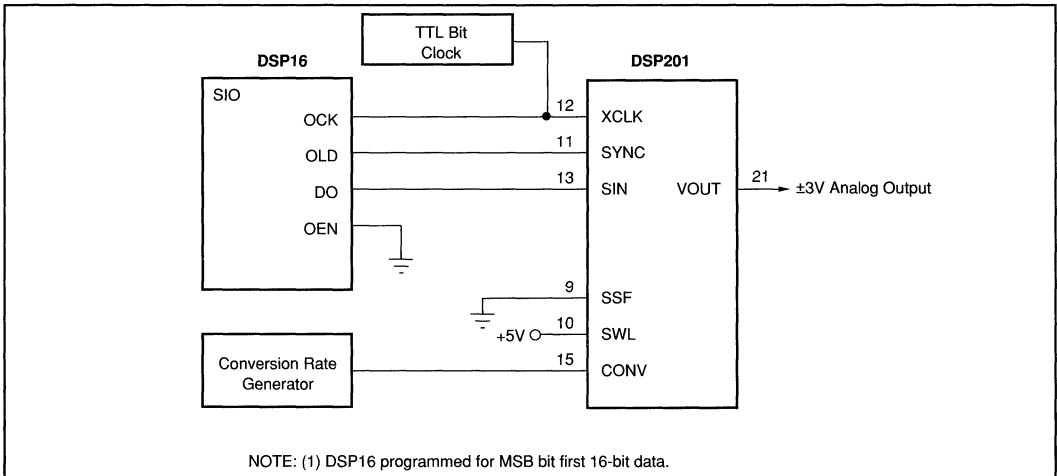
FIGURE 16. Using DSP202 with DSP32C in Cascade Mode.

NOTE: (1) DSP16 programmed for MSB bit first 16-bit data.
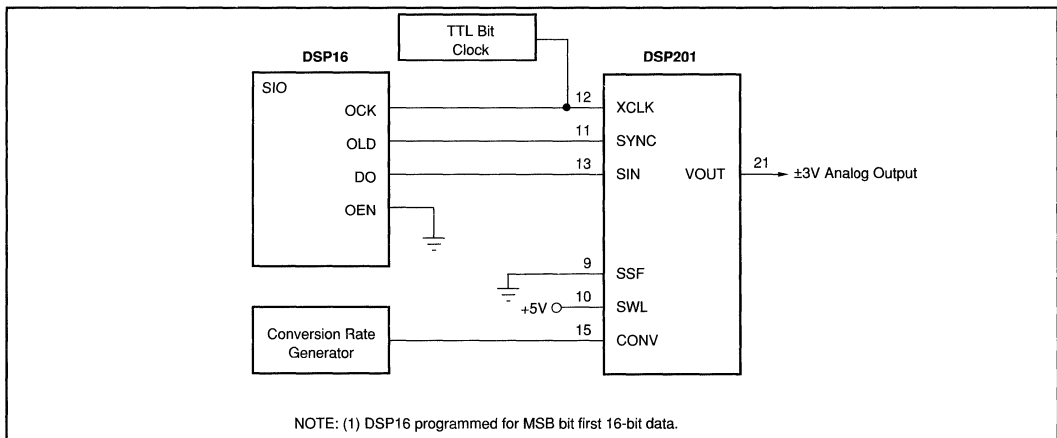
FIGURE 17. Using DSP201 with DSP16.

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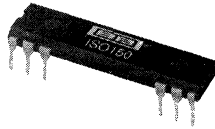
ISO150

Dual, Isolated, Bi-Directional
DIGITAL COUPLER

FEATURES

● REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
● DATA RATE: 80M Baud, typ
● LOW POWER CONSUMPTION: 25mW Per Channel, max
● TWO CHANNELS, EACH BI-DIRECTIONAL, PROGRAMMABLE BY USER
● PARTIAL DISCHARGE TESTED: 2400Vrms
● CREEPAGE DISTANCE OF 16.5mm (DIP)
● LOW COST PER CHANNEL
● PLASTIC DIP AND SOIC PACKAGES

APPLICATIONS

● DIGITAL ISOLATION FOR A/D, D/A CONVERSION
● ISOLATED UART INTERFACE
● MULTIPLEXED DATA TRANSMISSION
● ISOLATED PARALLEL TO SERIAL INTERFACE
● TEST EQUIPMENT
● MICROPROCESSOR SYSTEM INTERFACE
● ISOLATED LINE RECEIVER
● GROUND LOOP ELIMINATION

DESCRIPTION

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80MBaud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/µs.

ISO150 avoids the problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

ISO150 is available in a 24-pin DIP package and in a 28-lead SOIC. Both are specified for operation from –40°C to 85°C.

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SPECIFICATIONS

$T_A = +25°C$, $V_S = +5V$ unless otherwise noted.

PARAMETER	CONDITION	ISO150AP, AU MIN	TYP	MAX	UNITS
ISOLATION PARAMETERS					
Rated Voltage, Continuous	60Hz	1500			Vrms
Partial Discharge, 100% Test[1]	1s, 5pC	2400			Vrms
Creepage Distance (External)					
DIP—"P" Package			16		mm
SOIC—"U" Package			7.2		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity[2]			1.6		kV/µs
Barrier Impedance			>10^{14} || 7		Ω || pF
Leakage Current	240Vrms, 60Hz		0.6		µArms
DC PARAMETERS					
Logic Output Voltage, High, V_{OH}	$I_{OH} = 6mA$	V_S-1		V_S	V
Low, V_{OL}	$I_{OL} = 6mA$	0		0.4	V
Logic Output Short-Circuit Current	Source or Sink		30		mA
Logic Input Voltage, High[3]		2		V_S	V
Low[3]		0		0.8	V
Logic Input Capacitance			5		pF
Logic Input Current			<1		nA
Power Supply Voltage Range[3]		3	5	5.5	V
Power Supply Current[4]					
Transmit Mode	DC		0.001	100	µA
	50MBaud		14		mA
Receive Mode	DC		7.2	10	mA
	50MBaud		16		mA
AC PARAMETERS					
Data Rate, Maximum[5]	$C_L = 50pF$	50	80		MBaud
Data Rate, Minimum		DC			
Propagation Time[6]	$C_L = 50pF$	20	27	40	ns
Propagation Delay Skew[7]	$C_L = 50pF$		0.5	2	ns
Pulse Width Distortion[8]	$C_L = 50pF$		1.5	6	ns
Output Rise/Fall Time, 10% to 90%	$C_L = 50pF$		9	14	ns
Mode Switching Time					
Receive-to-Transmit			13		ns
Transmit-to-Receive			75		ns
TEMPERATURE RANGE					
Operating Range		−40		85	°C
Storage		−40		125	°C
Thermal Resistance, θ_{JA}			75		°C/W

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥5 pulses of ≥5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 0.4V hystersis—see text. (4) Supply current measured with both tranceivers set for the indicated mode. Supply current varies with data rate—see typical curves. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from $V_{IN} = 1.5V$ to $V_O = 2.5V$. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between progagation time of a rising edge and a falling edge.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... –40°C to +125°C
Supply Voltages, V_S .... –0.5 to 6V
Transmitter Input Voltage, V_I .... –0.5 to V_S + 0.5V
Receiver Output Voltage, V_O .... –0.5 to V_S + 0.5V
$R/\overline{T}_X$ Inputs .... –0.5 to V_S + 0.5V
Isolation Voltage dV/dt, V_{ISO} 500kV/μs
D_X Short to Ground .... Continuous
Junction Temperature, T_J .... 175°C
Lead Temperature (soldering, 10s) .... 260°C
1.6mm below seating plane (DIP package) .... 300°C

PIN CONFIGURATION

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO150AP	24-Pin Single-Wide DIP	243-1
ISO150AU	28-Lead SOIC	217-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.
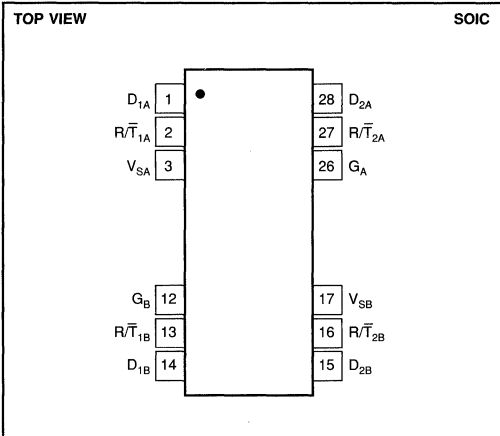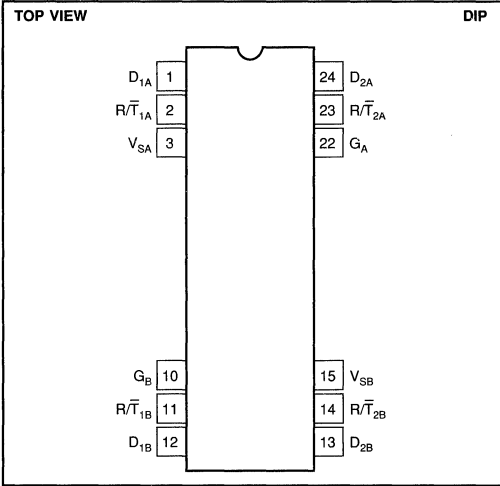
PIN DESCRIPTIONS

NAME	FUNCTION
D_{1A}	Data in or data out for transceiver 1A. $R/\overline{T}_{1A}$ held low makes D_{1A} an input pin.
$R/\overline{T}_{1A}$	Receive/Transmit switch controlling transceiver 1A.
V_{SA}	+5V supply pin for side A which powers transceivers 1A and 2A.
G_B	Ground pin for transceivers 1B and 2B.
$R/\overline{T}_{1B}$	Receive/Transmit switch controlling transceiver 1B.
D_{1B}	Data in or data out for transceiver 1B. $R/\overline{T}_{1B}$ held low makes D_{1B} an input pin.
D_{2B}	Data in or data out for transceiver 2B. $R/\overline{T}_{2B}$ held low makes D_{2B} an input pin.
$R/\overline{T}_{2B}$	Receive/Transmit switch controlling D_{2B}.
V_{SB}	+5V supply pin for side B which powers transceivers 1B and 2B.
G_A	Ground pin for transceivers 1A and 2A.
$R/\overline{T}_{2A}$	Receive/Transmit switch controlling transceiver 2A.
D_{2A}	Data in or data out for transceiver 2A. $R/\overline{T}_{2A}$ held low makes D_{2A} in input pin.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ISO150

4

DIGITAL INTERFACE PRODUCTS

TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = +5V$ unless otherwise noted.

SUPPLY CURRENT PER CHANNEL
vs SUPPLY VOLTAGE

POWER CONSUMPTION PER CHANNEL vs FREQUENCY

SUPPLY CURRENT PER CHANNEL
vs TEMPERATURE

TYPICAL RISE AND FALL TIMES vs CAPACITIVE LOAD
vs SUPPLY VOLTAGE

NORMALIZED RISE/FALL TIME vs TEMPERATURE

PROPAGATION DELAY vs SUPPLY VOLTAGE

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = +5V unless otherwise noted.

PROPAGATION DELAY vs TEMPERATURE

PULSE WIDTH DISTORTION vs TEMPERATURE

LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

OUTPUT VOLTAGE vs LOGIC INPUT VOLTAGE

ISOLATION LEAKAGE CURRENT vs FREQUENCY

ISOLATION VOLTAGE vs FREQUENCY

ISO150

4

DIGITAL INTERFACE PRODUCTS

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = +5V unless otherwise noted.

TYPICAL INSULATION RESISTANCE vs TEMPERATURE

[Graph: Isolation Resistance (Ω) on y-axis from 10^{10} to 10^{16}, Temperature (°C) on x-axis from 0 to 180]
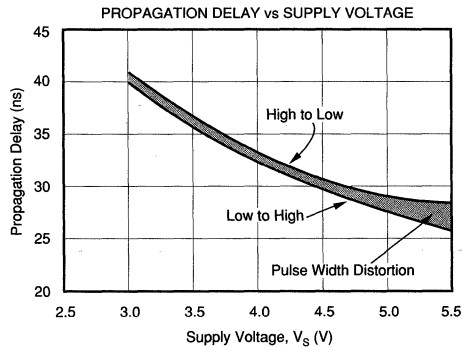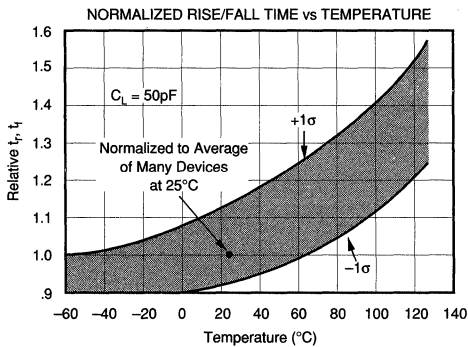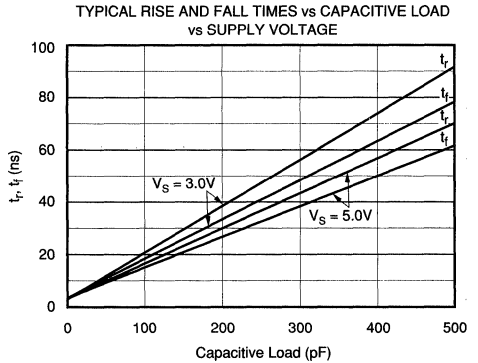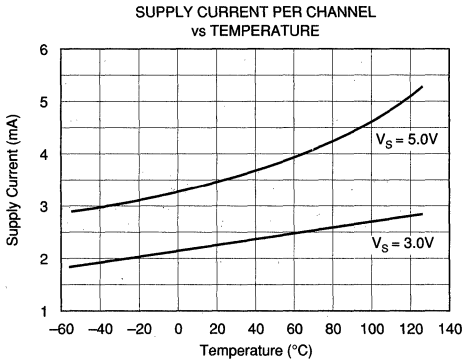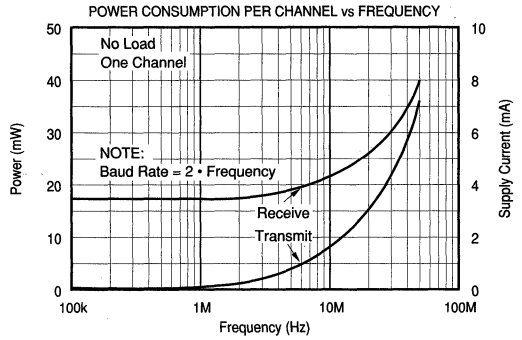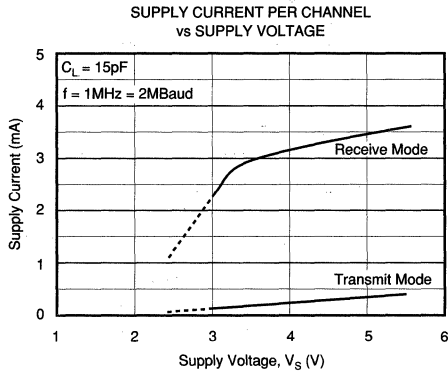
ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO150 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO150 is verified by partial discharge testing. 2400Vrms, 60Hz, is applied across the barrier for one second while measuring any tiny discharge currents that may flow through the barrier. These current pulses are produced by localized ionization within the barrier. This is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATIONS INFORMATION

Figure 1 shows the ISO150 connected for basic operation. Channel 1 is configured to transmit data from side B to A. Channel 2 is set for transmission from side A to B. The R/$\overline{\text{T}}$ pins for each of the four transceivers are shown connected to the required logic level for the transmission direction shown. The transmission direction can be controlled by logic signals applied to the R/$\overline{\text{T}}$ pins. Channel 1 and 2 can be independently controlled for the desired transmission direction.
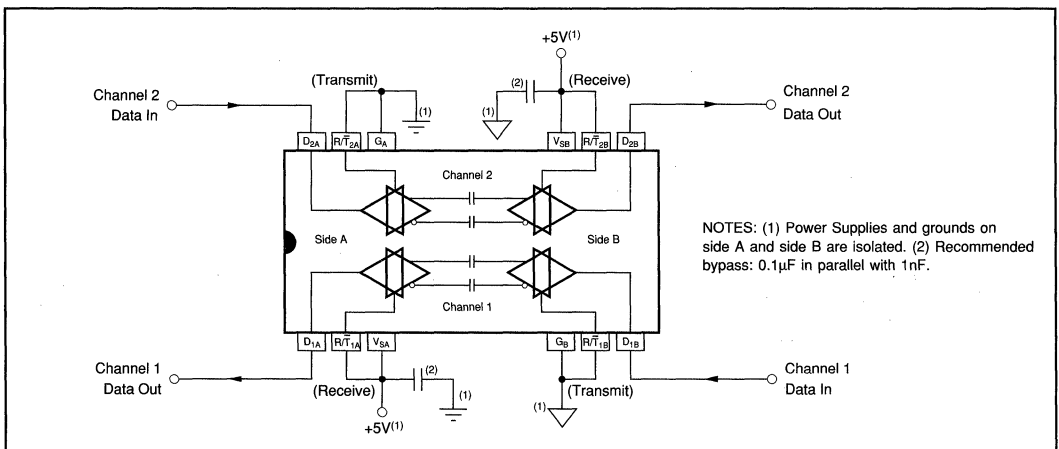
FIGURE 1. Basic Operation Diagram.

NOTES: (1) Power Supplies and grounds on side A and side B are isolated. (2) Recommended bypass: 0.1µF in parallel with 1nF.

LOGIC LEVELS

A single pin serves as a data input or output, depending on the mode selected. Logic inputs are CMOS with thresholds set for TTL compatibility. The logic threshold is approximately 1.3V with 5V supplies and with approximately 400mV of hysteresis. Input logic thresholds vary with the power supply voltage. Drive the logic inputs with signals that swing the full logic voltage swing. The ISO150 will use somewhat greater quiescent current if logic inputs do not swing within 0.5V of the power supply rails.

In receive mode, the data output can drive 15 standard LS-TTL loads. It will also drive CMOS loads. The output drive circuits are CMOS.

POWER SUPPLY

Separate, isolated power supplies must be connected to side A and side B to provide galvanic isolation. Nominal rated supply voltage is 5V. Operation extends from 3V to 5.5V. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier.

The V_S pin for each side powers the transceivers for both channel 1 and 2. The specified supply current is the total of both transceivers on one side, both operating in the indicated mode. Supply current for one transceiver in transmit mode and one in receive mode can be estimated by averaging the specifications for transmit and receive operation. Supply current varies with the data transmission rate—see typical curves.

POWER-UP STATE

The ISO150 transmits information across the barrier only when the input-side data changes logic state. When a transceiver is first programmed for receive mode, or is powered-up in receive mode, its output is initialized "high". Subsequent changes of data applied to the input side will cause the output to properly reflect the input side data.

SIGNAL LOSS

The ISO150's differential-mode signal transmission and careful receiver design make it highly immune to voltage across the isolation barrier (isolation-mode voltage). Rapidly changing isolation-mode voltage can cause data errors. As the rate of change of isolation voltage is increased, there is a very sudden increase in data errors. Approximately 50% of ISO150s will begin to produce data errors with isolation-mode transients of 1.6kV/μs. This may occur as low as 500V/μs in some devices. In comparison, a 1000Vrms, 60Hz isolation-mode voltage has a rate of change of approximately 0.5V/μs.

Still, some applications with large, noisy isolation-mode voltage can produce data errors by causing the receiver output to change states. After a data error, subsequent changes in input data will produce correct output data.

PROPAGATION DELAY AND SKEW

Logic transitions are delayed approximately 27ns through the ISO150. Some applications are sensitive to data skew— the difference in propagation delay between channel 1 and channel 2. Skew is less than 2ns between channel 1 and channel 2. Applications using more than one ISO150 must allow for somewhat greater skew from device to device. Since all devices are tested for delay times of 20ns min to 40ns max, 20ns is the largest device-to-device data skew.

MODE CHANGES

The transmission direction of a channel can be changed "on the fly" by reversing the logic levels at the channel's R/$\overline{T}$ pins on both side A and side B. Approximately 75ns after the transceiver is programmed to receive mode its output is initialized "high", and will respond to subsequent input-side changes in data.

STANDBY MODE

Quiescent current of each transceiver circuit is very low in transmit mode when input data is not changing (1nA typical). To conserve power when data transmission is not required, program both side A and B transceivers for transmit mode. Input data applied to either transceiver is ignored by the other side. High speed data applied to either transceiver will increase quiescent current.

CIRCUIT LAYOUT

The high speed of the ISO150 and its isolation barrier require careful circuit layout. Use good high speed logic layout techniques for the input and output data lines. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier. Use low inductance connections. Ground planes are recommended.

Maintain spacing between side 1 and side 2 circuitry equal or greater than the spacing between the missing pins of the ISO150 (approximately 16mm for the DIP version). Sockets are not recommended.
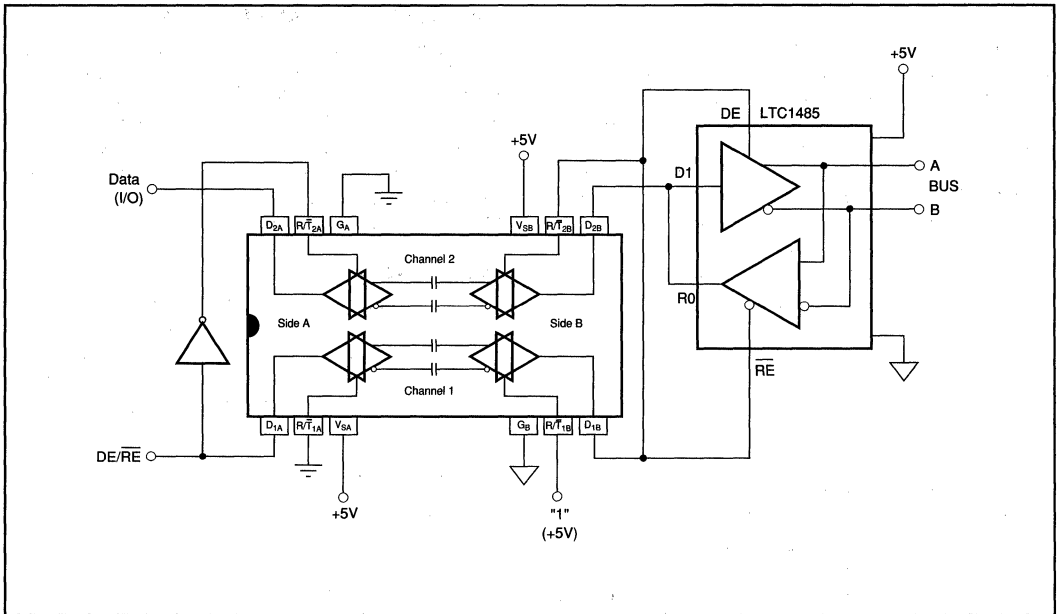
FIGURE 2. Isolated RS-485 Interface.
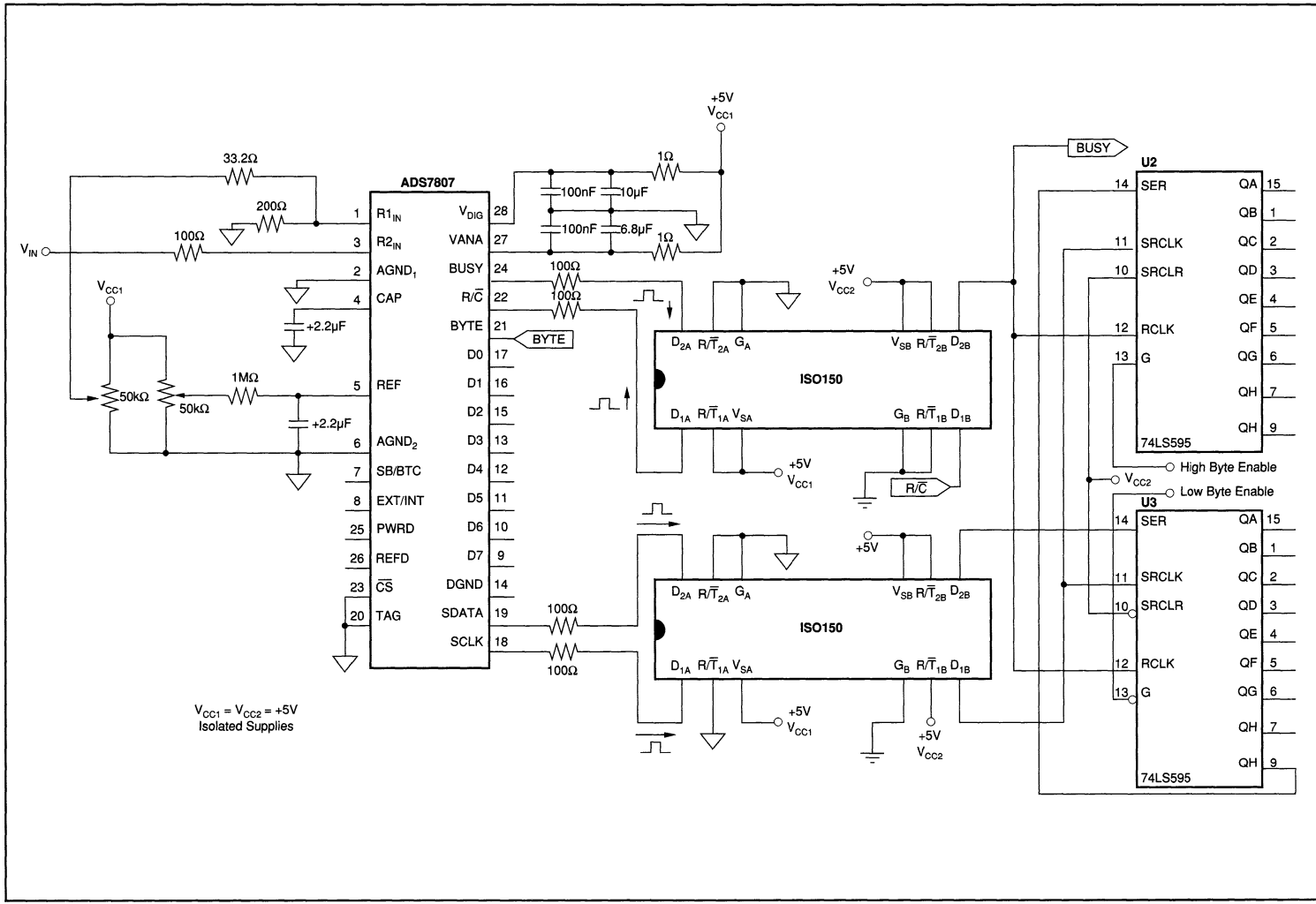
FIGURE 3. ISO150 and ADS7807 is Used to Reduce Circuit Noise in a Mixed Signal Application.

DIGITAL INTERFACE PRODUCTS 4 **ISO150**

5 Multiplexers

Burr-Brown analog multiplexers provide one of the most cost effective methods of achieving multiple-channel signal distribution. Single-ended and differential channel versions are available in both ceramic and plastic packages.

These high speed multiplexers are input protected and can withstand voltages of 70Vp-p without damaging the device. Full ±15V input range is provided on all devices.

MPC506	16 to 1 mux	single-ended
MPC507	8 to 1 mux	differential
MPC508	8 to 1 mux	single-ended
MPC509	4 to 1 mux	differential

ANALOG MULTIPLEXERS   **Boldface = NEW**

Description	Model	Channels	Input Range (V)	On Resistance max (Ω)	Settling Time (to 0.01%)	Temp Range[1]	Pkg[2]	Page No.
Protected Inputs	MPC506AP	16-channel single ended	±15	1.8k	3.5µs	Com	28-p PDIP	5.48
	MPC506AG	16-channel single ended	±15	1.8k	3.5µs	Ext	28-p CDIP	5.48
	MPC506AU	16-channel differential	±15	1.8k	3.5µs	Com	29-p SOIC	5.48
	MPC507AP	8-channel differential	±15	1.8k	3.5µs	Com	28-p PDIP	5.48
	MPC507AG	8-channel differential	±15	1.8k	3.5µs	Ext	28-p CDIP	5.48
	MPC507AU	8-channel differential	±15	1.8k	3.5µs	Com	28-p SOIC	5.48
	MPC508AP	8-channel single ended	±15	1.8k	3.5µs	Com	16-p PDIP	5.59
	MPC508AG	8-channel single ended	±15	1.8k	3.5µs	Ext	16-p CDIP	5.59
	MPC508AU	8-channel single ended	±15	1.8k	3.5µs	Com	16-p SOIC	5.59
	MPC509AP	4-channel differential	±15	1.8k	3.5µs	Com	16-p PDIP	5.59
	MPC509AG	4-channel differential	±15	1.8k	3.5µs	Ext	16-p CDIP	5.59
	MPC509AU	4-channel differential	±15	1.8k	3.5µs	Com	16-p SOIC	5.59
High Speed	MPC800KG	16 single or 8 differential	±15	750	800ns	Com	CDIP	5.69
	MPC800SG	16 single or 8 differential	±15	750	800ns	Mil	CDIP	5.69
	MPC801KG	8 single or 4 differential	±15	750	800ns	Com	CDIP	5.77
	MPC801SG	8 single or 4 differential	±15	750	800ns	Mil	CDIP	5.77

Description	Model	Channels	Input Range (V)	Input Impedance	Bandwidth	Temp Range[1]	Pkg[2]	Page No.
Buffered 4 x 1	MPC100AP	4-channel single ended	±4.2	0.88MΩ	450MHz	Ext	14-p PDIP	5.2
	MPC100AU	4-channel single ended	±4.2	0.88MΩ	450MHz	Ext	14-p SOIC	5.2
Buffered Dual 2 x 1	MPC102AP	dual 2-channel single ended	±3.6	0.88MΩ	370MHz	Ext	14-p PDIP	5.18
	MPC102AU	dual 2-channel single ended	±3.6	0.88MΩ	370MHz	Ext	14-p SOIC	5.18
	MPC104AP	**2-channel single-ended**	**±3.6**	**0.88MΩ**	**370MHz**	**Ext**	**8-p PDIP**	**5.33**
	MPC104AU	**2-channel single-ended**	**±3.6**	**0.88MΩ**	**370MHz**	**Ext**	**8-p SOIC**	**5.33**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ext = –40°C to +85°C, Mil = –55°C to +125°C. (2) CDIP = Ceramic DIP, PDIP = Plastic DIP.

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MULTIPLEXERS

BURR - BROWN®
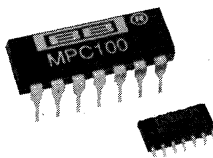
MPC100

Wide Bandwidth
4 x 1 VIDEO MULTIPLEXER

FEATURES

● **BANDWIDTH: 250MHz (1.4Vp-p)**

● **LOW INTERCHANNEL CROSSTALK:**
  ≤60dB (30MHz, DIP); ≤70dB (30MHz, SO)

● **LOW SWITCHING TRANSIENTS:**
  +2.5/−1.2mV

● **LOW DIFFERENTIAL GAIN/PHASE**
  ERRORS: 0.05%, 0.01°

● **LOW QUIESCENT CURRENT:**
  One Channel Selected: ±4.6mA
  No Channel Selected: ±230μA

APPLICATIONS

● **VIDEO ROUTING AND MULTIPLEXING**
  (CROSSPOINTS)

● **RADAR SYSTEMS**

● **DATA ACQUISITION**

● **INFORMATION TERMINALS**

● **SATELLITE OR RADIO LINK IF ROUTING**

DESCRIPTION

The MPC100 is a very wide bandwidth 4 to 1 channel
Video Signal Multiplexer, which can be used in a wide
variety of applications.

It was designed for wide-bandwidth systems, includ-
ing high-definition television and broadcast equip-
ment. Although it is primarily used to route video
signals, the harmonic and dynamic attributes of the
MPC100 make it appropriate for other analog signal
routing applications such as radar, communications,
computer graphics, and data acquisition systems.

The MPC100 consists of four identical monolithic
integrated open-loop buffer amplifiers, which are con-

nected together internally at the output. The unidirec-
tional transmission path consists of bipolar comple-
mentary buffers, which offer extremely high output-
to-input isolation. The MPC100 multiplexer enables
the user to connect any one of the four input channels
(IN_1 - IN_4) to the output. The output of the multiplexer
is in a high-impedance state when no channel is
selected. When one channel is selected with a digital
"1" at the corresponding SEL-input, the component
acts as a buffer with high input impedance and low
output impedance.

The wide bandwidth of over 250MHz at 1.4Vp-p
signal level, high linearity and low distortion, and low
input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint
switch suitable for RF and video applications. All
performance is specified with ±5V supply voltage,
which reduces power consumption in comparison with
±15V designs. The multiplexer is available in a space-
saving 14-pin SO and cost-saving DIP packages. Both
are designed and specified for operation over the
industrial temperature range (−40°C to +85°C.)
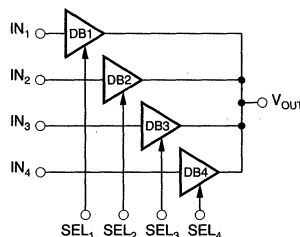
TRUTH TABLE

SEL₁	SEL₂	SEL₃	SEL₄	V_OUT
0	0	0	0	HI-Z
1	0	0	0	IN₁
0	1	0	0	IN₂
0	0	1	0	IN₃
0	0	0	1	IN₄

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm5VDC$, $R_L = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

| PARAMETER | CONDITIONS | MPC100AP/AU | | | UNITS |
		MIN	TYP	MAX	
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE					
Initial			±3	±30	mV
vs Temperature			30		µV/°C
vs Supply (Tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$	−40	−80		dB
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		−50		dB
vs Supply (Non-tracking)	$V_{CC} = −4.5V$ to $−5.5V$		−50		dB
Initial Matching	Between the Four Channels		1.5	4.5	mV
INPUT BIAS CURRENT					
Initial			+3	8	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$		±380		nA/V
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		+1.0		µA/V
vs Supply (Non-tracking)	$V_{CC} = −4.5V$ to $−5.5V$		−11.0		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	$f_{OUT} = 20kHz$ to $10MHz$		4.0		nV/$\sqrt{Hz}$
Signal-to-Noise Ratio	S/N = 0.7/V_N • $\sqrt{5MHz}$		−98		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±4.2		V
TRANSFER CHARACTERISTICS	Voltage Gain				
	$R_L = 1k\Omega$, $V_{IN} = \pm2V$		0.982		V/V
	$R_L = 10k\Omega$, $V_{IN} = \pm2.8V$	0.98	0.992		V/V
RATED OUTPUT					
Voltage	$G \geq 0.97$, $R_L = 5k\Omega$	±2.8	±3.8		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6		mA
	No Channel Selected		±230	±350	µA
Rejection Ratio			−80		dB

MPC100

5

MULTIPLEXERS

CONNECTION DIAGRAM

Top View   SOIC/DIP

IN₁ 1 — DB1 — 14 SEL₁
GND 2 — 13 SEL₂
IN₂ 3 — DB2 — 12 −V_CC
GND 4 — 11 V_OUT
IN₃ 5 — DB3 — 10 +V_CC
GND 6 — 9 SEL₃
IN₄ 7 — DB4 — 8 SEL₄

MPC100

FUNCTIONAL DESCRIPTION

IN₁-IN₄	Four analog input channels
GND	Analog input shielding grounds, not internally connected
SEL₁-SEL₄	Channel selection inputs
V_OUT	Analog output; tracks selected channel
−V_CC	Negative supply voltage; typical −5VDC
+V_CC	Positive supply voltage; typical +5VDC

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP/AU MIN	MPC100AP/AU TYP	MPC100AP/AU MAX	UNITS
AC CHARACTERISTICS					
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH (–3dB)	$V_O = 5.0Vp$-p, $C_{OUT} = 1pF$		70		MHz
	$V_O = 2.8Vp$-p, $C_{OUT} = 1pF$		140		MHz
	$V_O = 1.4Vp$-p, $C_{OUT} = 1pF$		250		MHz
SMALL SIGNAL BANDWIDTH	$V_O = 0.2Vp$-p, $C_{OUT} = 1pF$		450		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	$f = 4.43MHz$, $V_{IN} = 0.3Vp$-p				
	VDC = 0 to 0.7V		0.05		%
	VDC = 0 to 1.4V		0.06		%
DIFFERENTIAL PHASE	$f = 4.43MHz$, $V_{IN} = 0.3Vp$-p				
	VDC = 0 to 0.7V		0.01		Degrees
	VDC = 0 to 1.4V		0.02		Degrees
GAIN FLATNESS PEAKING	$V_O = 0.2Vp$-p, DC to 30MHz		0.04		dB
	$V_O = 0.2Vp$-p, DC to 100MHz		0.05		dB
HARMONIC DISTORTION	$f = 30MHz$, $V_O = 1.4Vp$-p, $R_L = 1k\Omega$				
Second Harmonic			–53		dBc
Third Harmonic			–67		dBc
CROSSTALK	$V_I = 1.4Vp$-p, Figures 4 and 8				
MPC100AP All Hostile	$f = 5MHz$,		–82		dB
	$f = 30MHz$,		–60		dB
Off Isolation	$f = 5MHz$,		–70		dB
	$f = 30MHz$,		–71		dB
MPC100AU All Hostile	$f = 5MHz$,		–78		dB
	$f = 30MHz$,		–70		dB
Off Isolation	$f = 5MHz$,		–75		dB
	$f = 30MHz$		–76		dB
TIME DOMAIN					
RISE TIME	$V_O = 1.4Vp$-p, Step 10% to 90%				
	$C_{OUT} = 1pF$, $R_{OUT} = 22\Omega$		3.3		ns
SLEW RATE	$V_O = 2Vp$-p				
	$C_{OUT} = 1pF$		650		V/µs
	$C_{OUT} = 22pF$		460		V/µs
	$C_{OUT} = 47pF$		320		V/µs

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE –40°C to +85°C)

At $V_{CC} = \pm 5VDC$, $R_L = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP/AU MIN	MPC100AP/AU TYP	MPC100AP/AU MAX	UNITS
OFFSET VOLTAGE			±5	±35	mV
TRANSFER CHARACTERISTICS	Voltage Gain				
	$R_L = 10k\Omega$	0.95	0.992	0.997	V/V
INPUT BIAS CURRENT			+3	±10	µA
RATED OUTPUT					
Voltage Output	$G \geq 0.90$, $R_L = 10k\Omega$	±2.8	±3.8	±4	V
POWER SUPPLY					
Quiescent Current	One Channel Selected		±4.6	±5.5	mA
	No Channel Selected		±230	±320	µA

CHANNEL SELECTION

PARAMETER	CONDITIONS	MPC100AP/AU			UNITS
		MIN	TYP	MAX	
SELECTION INPUTS					
Logic 1 Voltage		+2.0		V_{CC} +0.6	V
Logic 0 Voltage		0		+0.8	V
Logic 1 Current	V_{SEL} = 5.0V	+75	+100	+125	μA
Logic 0 Current	V_{SEL} = 0.8V	0	0.002	+5	μA
SWITCHING CHARACTERISTICS	V_I = −0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_O = 1Vp-p		0.25		μs
SEL to Channel OFF Time	10% Point of V_O = 1Vp-p		0.25		μs
Switching Transient, Positive	Measured While Switching		+2.5		mV
Switching Transient, Negative	Between Two Grounded Channels		−1.2		mV

DICE INFORMATION
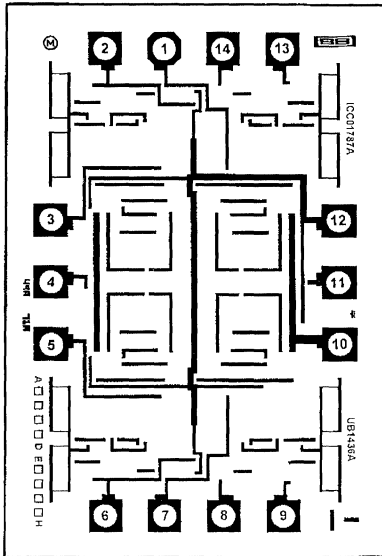
MPC100 DIE TOPOGRAPHY

PAD	FUNCTION
1	Input 1
2	Ground
3	Input 2
4	Ground
5	Input 3
6	Ground
7	Input 4
8	Select 4
9	Select 3
10	+5V Supply
11	Output
12	−5V Supply
13	Select 2
14	Select 1

Substrate Bias: Negative Supply
NC: No Connection
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	51 x 76, ±5	1.295 x 1.93, ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, −0.0	0.0005 +0.0013, −0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (±V_{CC}) .... ±6VDC
Analog Input Voltage (IN₁ through IN₄)[1] .... ±V_{CC}, ±0.7V
Operating Temperature .... −40°C to +85°C
Storage Temperature .... −40°C to +125°C
Output Current .... ±6mA
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
Digital Input Voltages (SEL₁ through SEL₄)[1] .... −0.5V to +V_{CC} +0.7V

NOTE: (1) Inputs are internally diode-clamped to ±V_{CC}.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC100AP	14-Pin Plastic DIP	010
MPC100AU	14-Pin SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC100AP	14-Pin Plastic DIP	−40°C to +85°C
MPC100AU	14-Pin SOIC	−40°C to +85°C

MULTIPLEXERS **MPC100**

5

TYPICAL PERFORMANCE CURVES

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

OFFSET VOLTAGE vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT IMPEDANCE vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

TOTAL QUIESCENT CURRENT vs TEMPERATURE

One Channel Selected

TOTAL QUIESCENT CURRENT vs TEMPERATURE

No Channel Selected

TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

TRANSFER FUNCTION

GAIN ERROR vs INPUT VOLTAGE

INPUT VOLTAGE NOISE SPECTRAL DENSITY

SWITCHING ENVELOPE (Video Signal)

Time (μs)

SWITCHING TRANSIENTS (Channel To Channel)

Without bandwidth
limiting lowpass filter.

SWITCHING TRANSIENTS (Channel To Channel)

36MHz Low pass filter acc.
Eureka Rec. EU95-PG03
in the signal path.

MPC100

5

MULTIPLEXERS
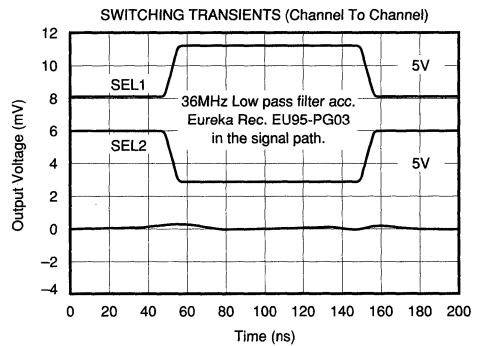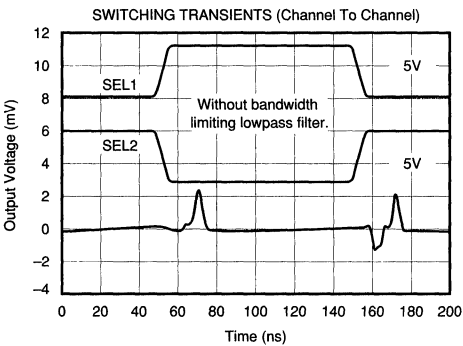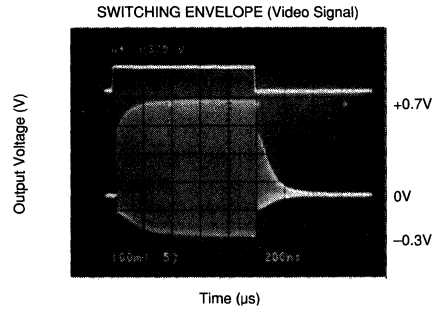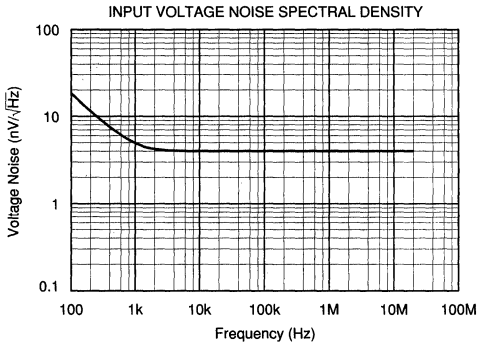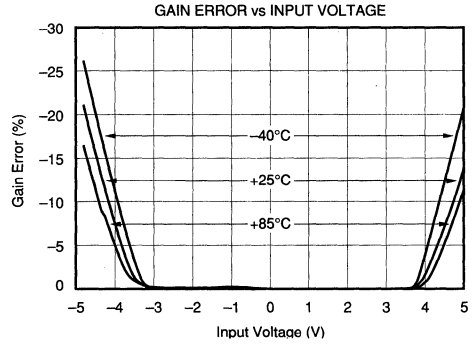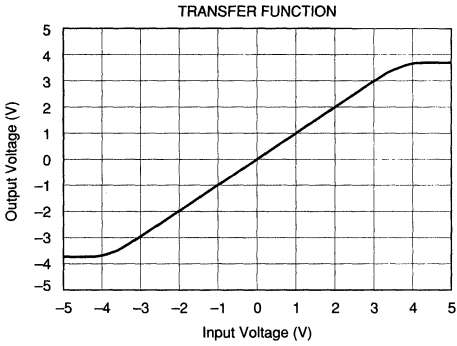
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE

Time (ns)
C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

SMALL SIGNAL PULSE RESPONSE
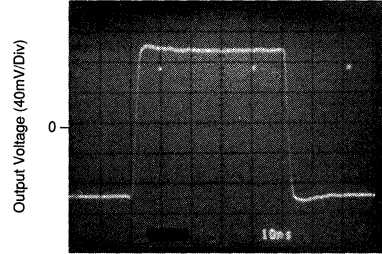
Time (ns)
C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

LARGE SIGNAL PULSE RESPONSE

Time (ns)
C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

LARGE SIGNAL PULSE RESPONSE

Time (ns)
C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

GROUP DELAY TIME vs FREQUENCY

BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}

C_{OUT}	R_{OUT}	f_{-3dB}
1p	0Ω	500MHz
10p	22Ω	340MHz
22p	15Ω	250MHz
33p	12Ω	215MHz
47p	10Ω	130MHz

TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm5VDC$, $R_{LOAD} = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

GAIN FLATNESS

$R_{IN} = 150\Omega$, $R_{O1} = 1k\Omega$
$C_{OUT} = 22pF$, $R_{OUT} = 15\Omega$

0.2Vp-p

Output (dB) vs Frequency (Hz)

BANDWIDTH vs OUTPUT VOLTAGE

$C_{OUT} = 1pF$, $R_{OUT} = 0\Omega$
$R_{IN} = 150\Omega$

5Vp-p
2.8Vp-p
1.4Vp-p
0.6Vp-p
0.2Vp-p

Output Voltage (Vp-p) vs Frequency (Hz)

BANDWIDTH vs R_{LOAD}

2.8Vp-p

$C_{OUT} = 22pF$, $R_{OUT} = 15\Omega$, $V_O = 2.8Vp-p$
$R_L = 500\Omega = 1k\Omega = 10k\Omega$

Gain (dB) vs Frequency (Hz)

BANDWIDTH MATCHING (DB1...DB4)

2.8Vp-p

$C_{OUT} = 22pF$, $R_{OUT} = 15\Omega$

Gain (dB) vs Frequency (Hz)

30MHz HARMONIC DISTORTION

Frequency (Hz)
$V_{OUT} = 2.8Vp-p$, $R_L = 1k\Omega$, $C_{OUT} = 1pF$

Harmonic Distortion (dB)
10dB/Div

30MHz HARMONIC DISTORTION

Frequency (Hz)
$V_{OUT} = 2.8Vp-p$, $R_L = 10k\Omega$, $C_{OUT} = 1pF$

Harmonic Distortion (dB)
10dB/Div

MPC100

5

MULTIPLEXERS

APPLICATIONS INFORMATION

The MPC100 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

All pins on the MPC100 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision buffer amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC100.

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC100 incorporates on-chip ESD protection diodes as shown in Figure 1. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.
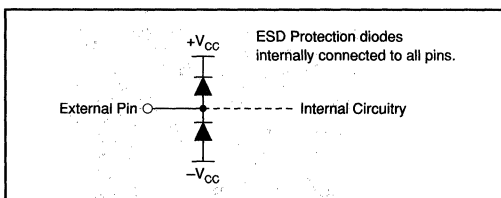
FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC100 video multiplexer allows the user to connect any one of four analog input channels (IN_1-IN_4) to the output of the component and to switch between channels within less than 0.5µs. It consists of four identical unity-gain buffer amplifiers, which are connected together internally at the output. The open loop buffers consisting of complementary emitter followers applies no feedback, so their low frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements the bipolar complementary buffers form an unidirectional transmission path and thus provide high output-to-input isolation. Switching stages compatible to TTL level digital signals are provided for each buffer to select the input channel. When no channel is selected, the output of the device is a high-impedance and allows the user to wire more MPC100s together to form switch multi-channel matrices.

If one channel is selected with a digital "1" at the corresponding SEL-input, the MPC100 acts as a buffer amplifier with high input impedance and low output impedance. The truth table on the front page describes the relationship between the digital inputs (SEL_1 to SEL_4) and the analog inputs (IN_1 to IN_4), and which signal is selected at the output.

The 2-4 address decoder and chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the 1 of 4 multiplexer, in effect, a quad switchable high-speed buffer. They require DC coupling and termination resistors when directly driven from a low impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 250MHz at an output voltage of 1.4Vp-p allows the design of large crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.05%) and phase (0.01°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the brightness (luminance) signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC100 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short

time, but it hardly interferes with the input signals. The transient peaks remain less than +2.5mV and −1.2mV. Subsequent equipment might interpret large negative output glitches as synchronization pulses. To remove this problem, the output must be clamped during the switching dead time. With the MPC100, the generated output transients are extremely small and clamping is unnecessary. The switching time between two channels is less than 0.5µs. This short time period allows easy switching during the vertical blanking time. The signal envelope during the transition from one channel to another rises and falls symmetrically and shows less overshooting or DC settling transients.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffers are always in off-state. One important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±230µA in off-state and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC100 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

• Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.

• PC board traces for signal and power lines should be wide to reduce impedance or inductance.

• Make short and low inductance traces. The entire physical circuit should be as small as possible.

• Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection. Refer to the suggested layout shown in Figure 9.

• Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.

• Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.

• Use low-inductance and surface-mounted components. Circuits using all surface mount components with the MPC100AU will offer the best AC-performance.

• A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.

• Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the MPC100AU to speed prototyping. This board allows easy and fast performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. The complete AC characterization was performed with the same type. Figure 10 shows the schematic and Figure 9 the silk screen and the double-sided layout. Request DEM-MPC100-1GC.
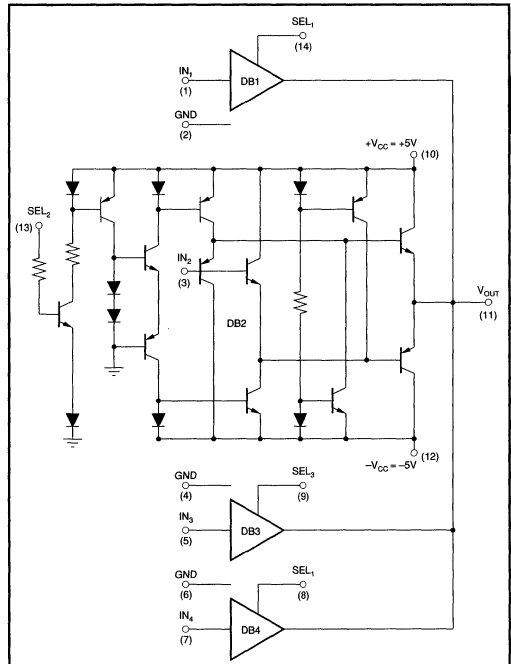
FIGURE 2. Simplified Circuit Diagram.

CROSSTALK
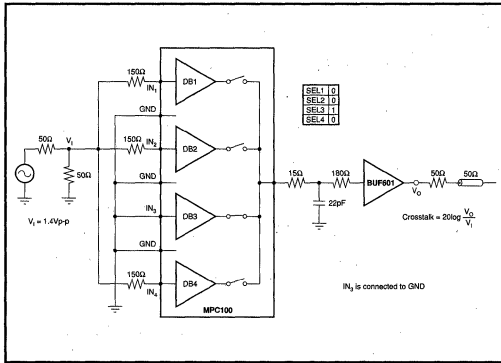
FIGURE 3. All Hostile Crosstalk Test Circuit 1.
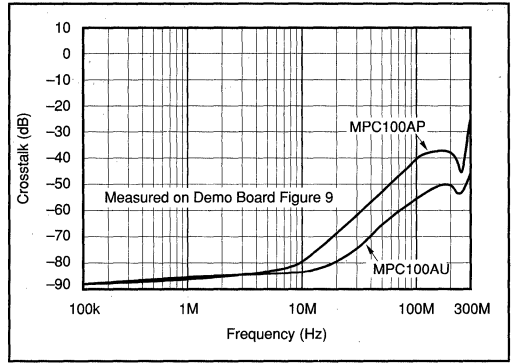
FIGURE 4. All Hostile Crosstalk.[1]
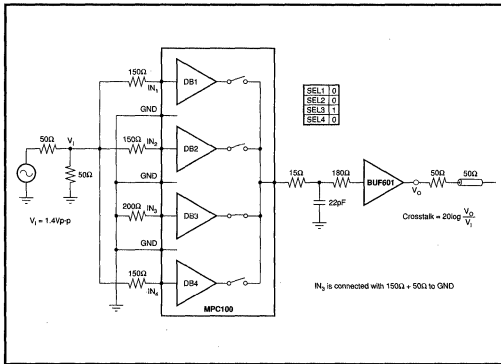
FIGURE 5. All Hostile Crosstalk Test Circuit 2.
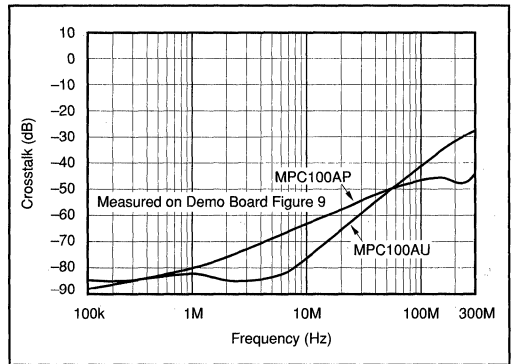
FIGURE 6. All Hostile Crosstalk.[1]
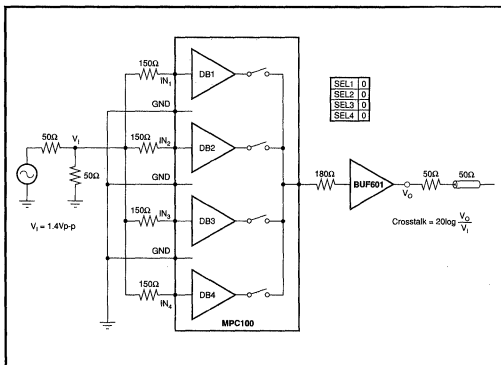
FIGURE 7. Off Isolation Crosstalk Test Circuit.
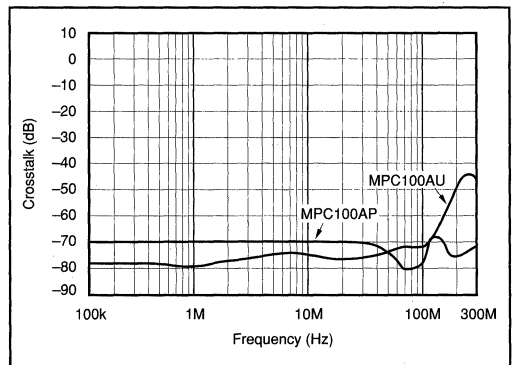
FIGURE 8. Off Isolation Crosstalk.

NOTE: (1) An optimized multilayer board layout makes it possible to achieve a crosstalk performance at 30MHz better than –70dB.
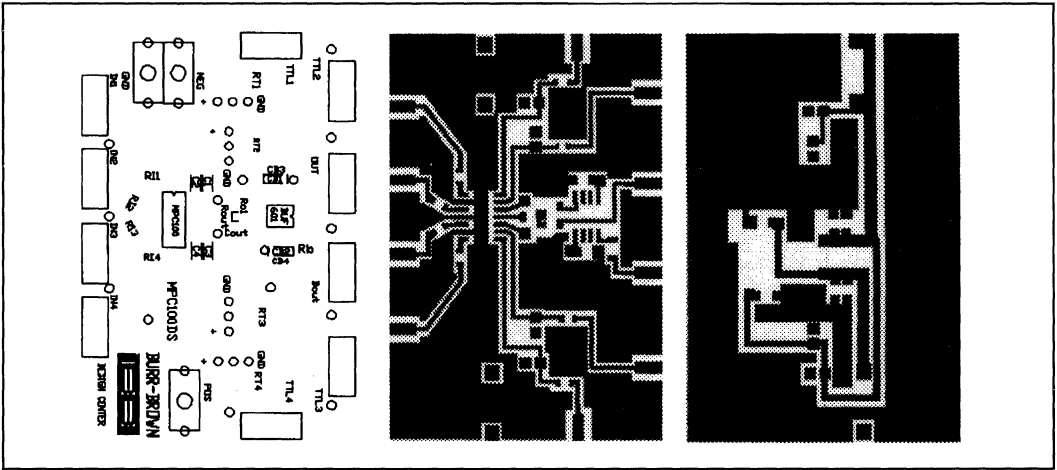
FIGURE 9. Silk Screen and Board Layout of DEM-MPC100-1GC.

MPC100

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MULTIPLEXERS
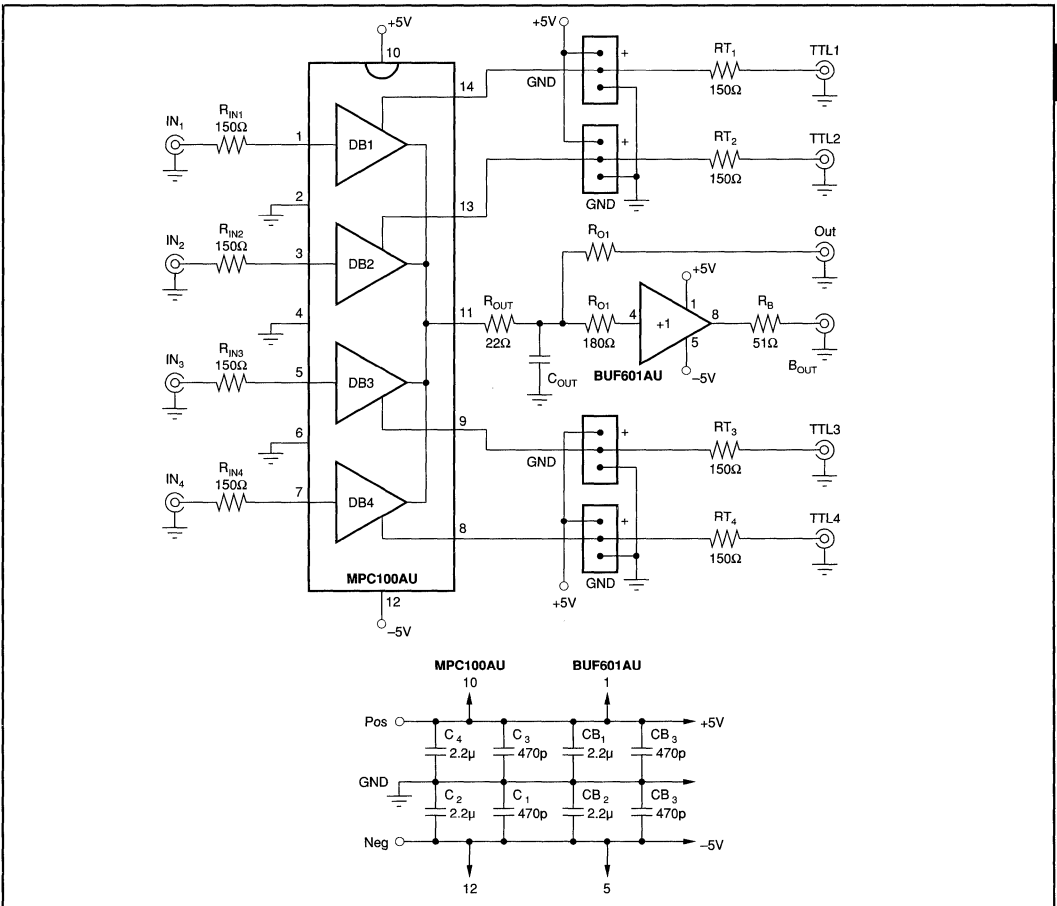
FIGURE 10. Circuit Schematic DEM-MPC100-1GC.

APPLICATIONS INFORMATION
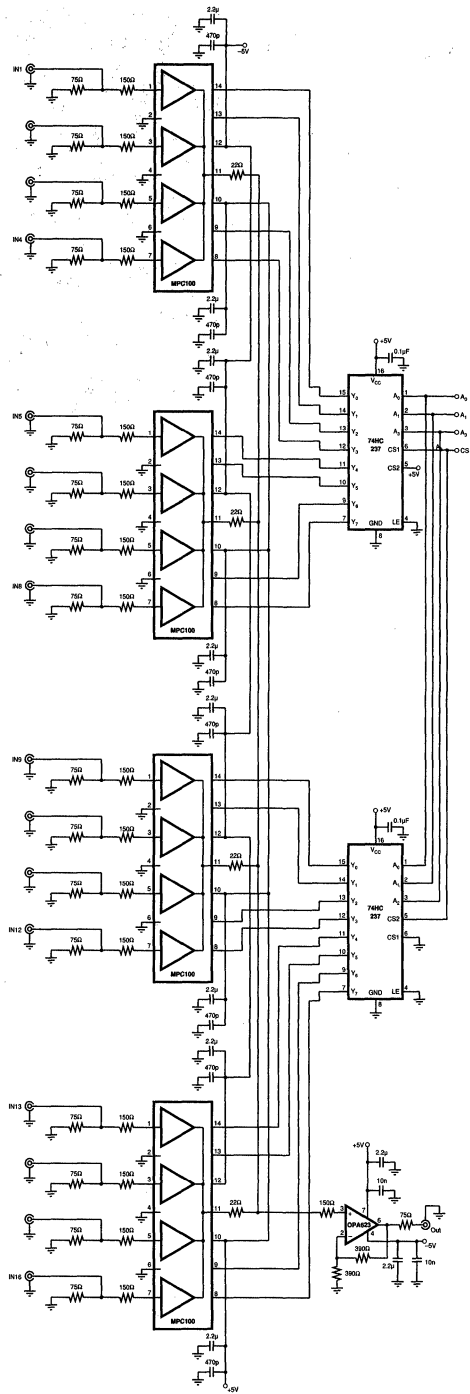
FIGURE 11. Video Distribution Field.
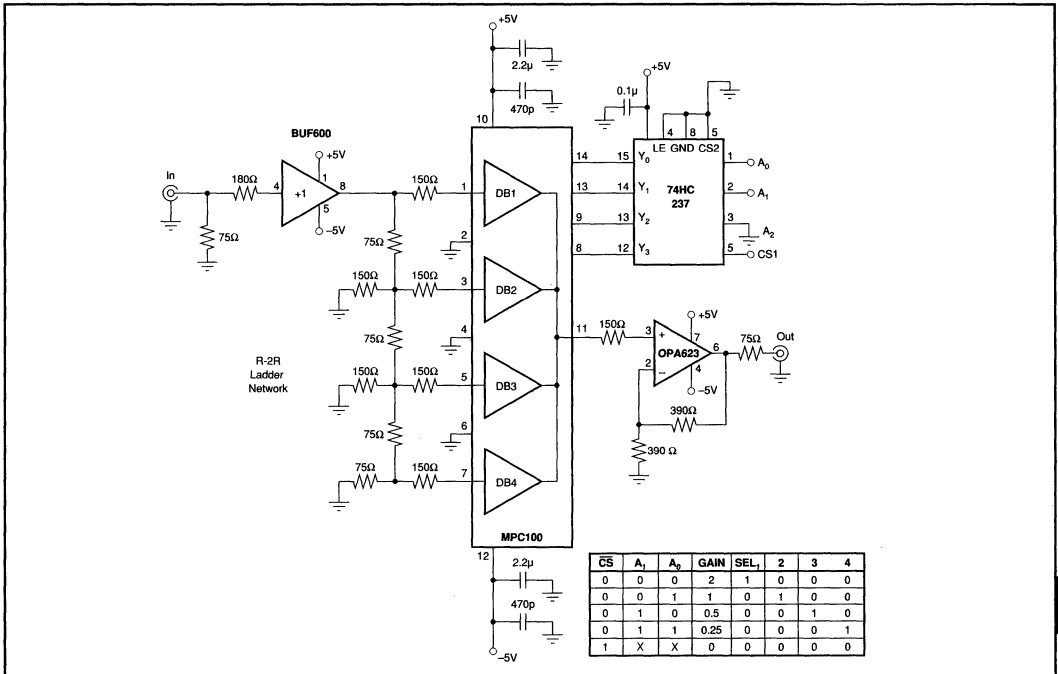
FIGURE 12. Digital Gain Control.
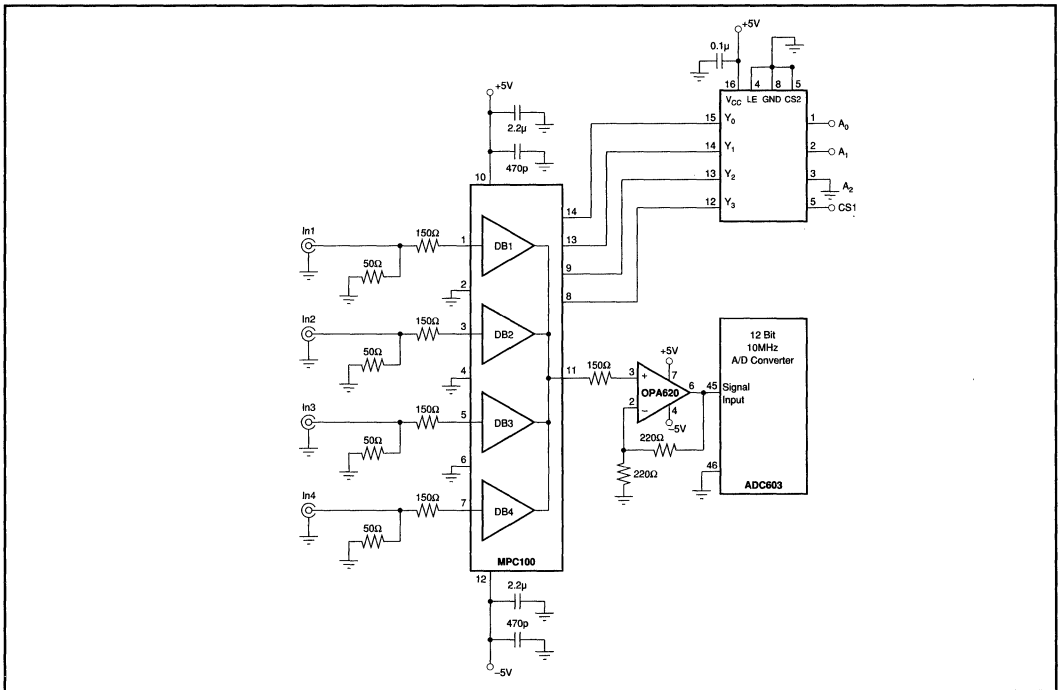
FIGURE 13. High Speed Data Acquisition System.

MPC100

MULTIPLEXERS

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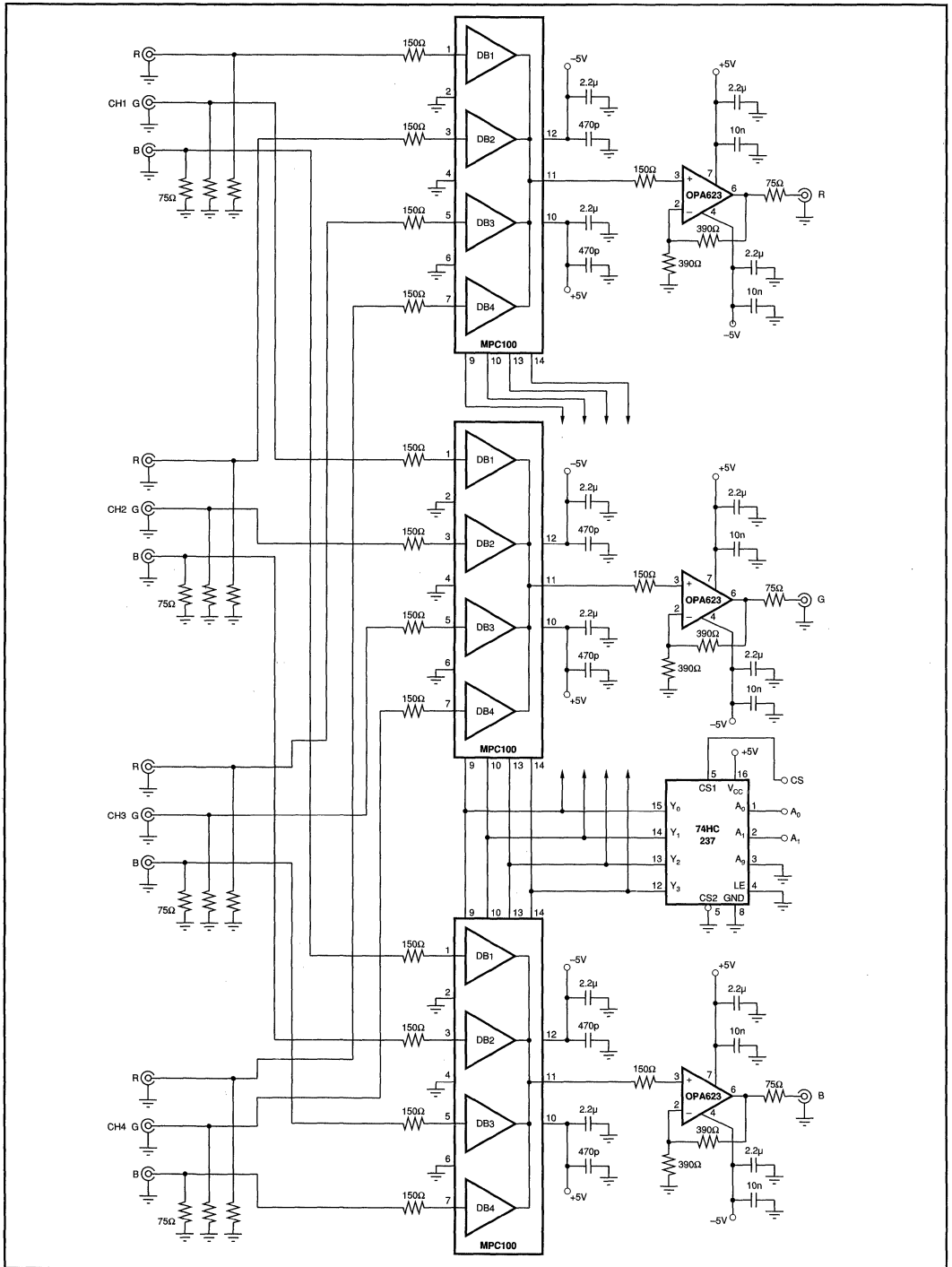
FIGURE 14. Distribution Field for High Resolution Graphic Cards, Cameras.
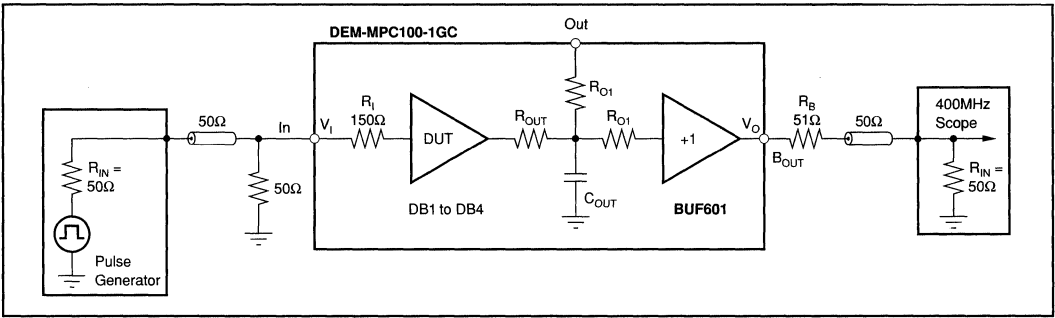
FIGURE 15. Test Circuit Pulse Response.
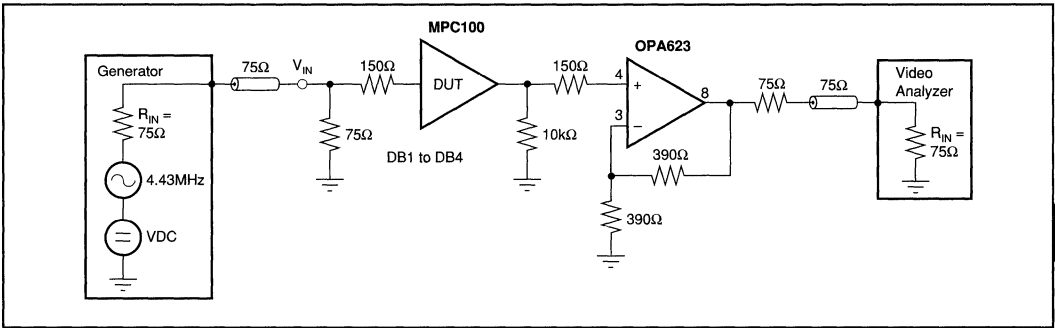
FIGURE 16. Test Circuit Differential Gain and Phase.
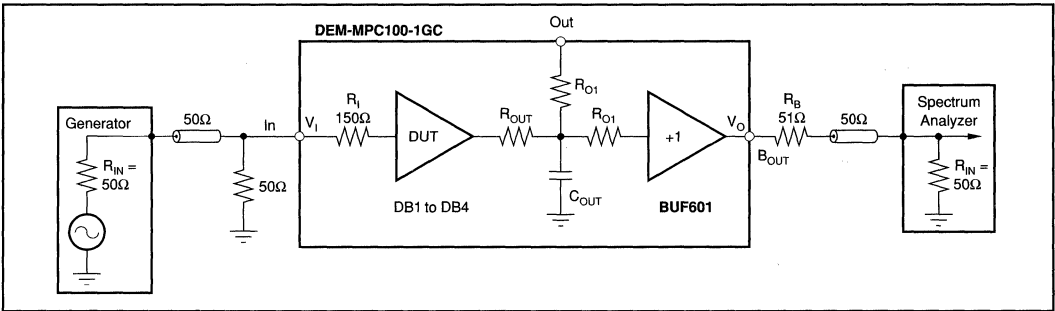
FIGURE 17. Test Circuit Frequency Response.
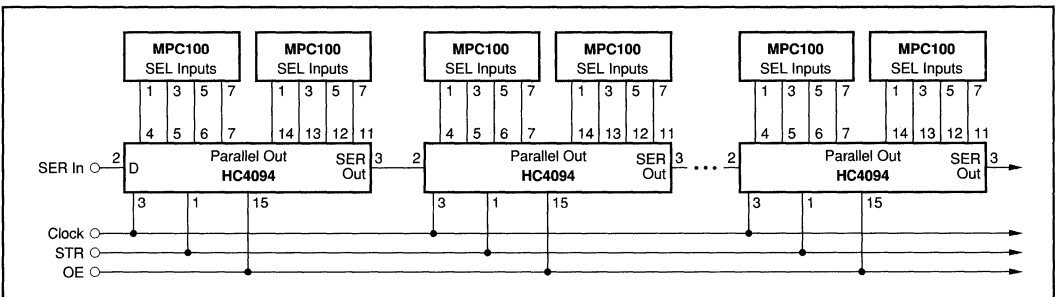
FIGURE 18. Serial Bus-Controlled Distribution Field.

MPC100

MULTIPLEXERS

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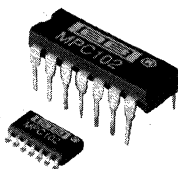
MPC102

Wide-Bandwidth
DUAL 2 x 1 VIDEO MULTIPLEXER

FEATURES

● **BANDWIDTH: 210MHz (1.4Vp-p)**

● **LOW INTERCHANNEL CROSSTALK:**
  −68dB (30MHz, SO); −58dB (30MHz, DIP)

● **LOW SWITCHING TRANSIENTS:**
  +6mV/−8mV

● **LOW DIFFERENTIAL GAIN/PHASE**
  ERRORS: 0.02%, 0.02°

● **LOW QUIESCENT CURRENT:**
  One Channel Selected: ±4.6mA
  No Channel Selected: ±250μA

APPLICATIONS

● **VIDEO ROUTING AND MULTIPLEXING**
  (CROSSPOINTS)

● **RADAR SYSTEMS**

● **DATA ACQUISITION**

● **INFORMATION TERMINALS**

● **SATELLITE OR RADIO LINK IF ROUTING**

DESCRIPTION

The MPC102 is dual, wide-bandwidth, 2-to-1 channel video signal multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC102 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC102 consists of four identical monolithic, integrated, open-loop buffer amplifiers. Two buffer outputs are each connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC102 multiplexer enables the user to connect one of two input signals to the corresponding output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 14-pin SO and DIP packages. Both are designed and specified for operation over the industrial temperature range (−40°C to +85°C.)
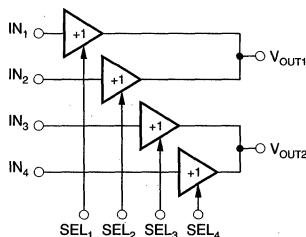
TRUTH TABLE

SEL$_1$	SEL$_2$	SEL$_3$	SEL$_4$	V$_{OUT1}$	V$_{OUT2}$
0	0	0	0	HI-Z	HI-Z
1	0	0	0	IN$_1$	HI-Z
0	1	0	0	IN$_2$	HI-Z
0	0	1	0	HI-Z	IN$_3$
0	0	0	1	HI-Z	IN$_4$

PDS-1202B

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm5VDC$, $R_L = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP/AU			UNITS
		MIN	TYP	MAX	
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE					
Initial			14	±30	mV
vs Temperature			60		µV/°C
vs Supply (Tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$	−40	−80		dB
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		−50		dB
vs Supply (Non-tracking)	$V_{CC} = −4.5V$ to $−5.5V$		−50		dB
Initial Matching	All Four Buffers		3		mV
INPUT BIAS CURRENT					
Initial			4	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	$V_{CC} = \pm4.5V$ to $\pm5.5V$		±710		nA/V
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		0.26		µA/V
vs Supply (Non-tracking)	$V_{CC} = −4.5V$ to $−5.5V$		1.7		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	$f_{OUT} = 20kHz$ to $10MHz$		4.0		nV/√Hz
Signal-to-Noise Ratio	$S/N = 0.7/V_N \cdot \sqrt{5MHz}$		−98		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±3.6		V
TRANSFER CHARACTERISTICS	Voltage Gain				
	$R_L = 1k\Omega$, $V_{IN} = \pm2V$		0.982		V/V
	$R_L = 10k\Omega$, $V_{IN} = \pm2V$	0.98	0.992		V/V
RATED OUTPUT					
Voltage	$G \geq 0.97$, $R_L = 10k\Omega$	±2.8	3.0		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6		mA
	No Channel Selected		±250	±350	µA
Rejection Ratio			−80		dB

CONNECTION DIAGRAM

Top View　　　　　　　　　　　　　　SO/DIP

IN_1	1	+1	14	SEL_1
GND	2		13	SEL_2
IN_2	3	+1	12	V_{OUT1}
$+V_{CC}$	4		11	$−V_{CC}$
IN_3	5	+1	10	V_{OUT2}
GND	6		9	SEL_3
IN_4	7	+1	8	SEL_4

MPC102

PIN DESCRIPTION

PIN	DESCRIPTION
IN_1, IN_2	Analog Inputs Channel 1 and 2
IN_3, IN_4	Analog Inputs Channel 3 and 4
GND	Analog Shielding—Grounds Not Internally Connected
SEL_1, SEL_2	Channel Selection Inputs
V_{OUT1}	Analog Output 1
V_{OUT2}	Analog Output 2
$−V_{CC}$	Negative Supply Voltage; typical −5VDC
$+V_{CC}$	Positive Supply Voltage; typical +5VDC

SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = \pm5VDC$, $R_L = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.
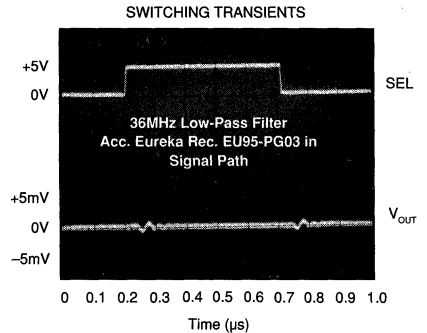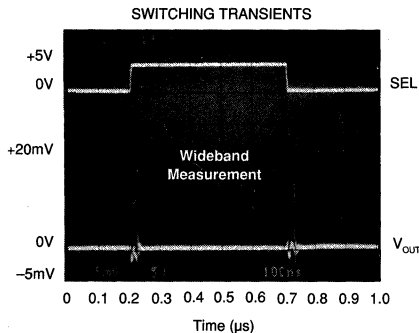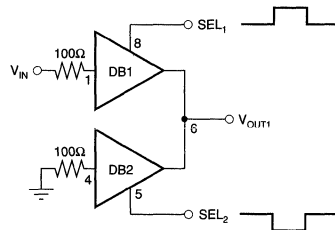
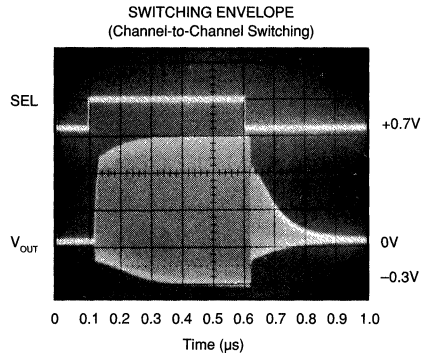| PARAMETER	CONDITIONS	MPC102AP/AU			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS					
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH (–3dB)	$V_{OUT} = 5.0Vp\text{-}p$, $C_{OUT} = 1pF$		55		MHz
	$V_{OUT} = 2.8Vp\text{-}p$, $C_{OUT} = 1pF$		100		MHz
	$V_{OUT} = 1.4Vp\text{-}p$, $C_{OUT} = 1pF$		210		MHz
SMALL SIGNAL BANDWIDTH	$V_{OUT} = 0.2Vp\text{-}p$, $C_{OUT} = 1pF$		370		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	$f = 4.43MHz$, $V_{IN} = 0.3Vp\text{-}p$				
	VDC = 0 to 0.7V		0.02		%
DIFFERENTIAL PHASE	$f = 4.43MHz$, $V_{IN} = 0.3Vp\text{-}p$				
	VDC = 0 to 0.7V		0.02		Degrees
GAIN FLATNESS PEAKING	$V_{OUT} = 0.2Vp\text{-}p$, DC to 30MHz		0.04		dB
	$V_{OUT} = 0.2Vp\text{-}p$, DC to 100MHz		0.05		dB
HARMONIC DISTORTION	$f = 30MHz$, $V_{OUT} = 1.4Vp\text{-}p$, $R_L = 350\Omega$				
Second Harmonic			–64		dBc
Third Harmonic			–66		dBc
CROSSTALK	$V_{IN} = 1.4Vp\text{-}p$				
MPC102AP All Hostile	f = 5MHz,		–75		dB
	f = 30MHz,		–58		dB
Off Isolation	f = 5MHz,		–70		dB
	f = 30MHz,		–71		dB
MPC102AU All Hostile	f = 5MHz,		–78		dB
	f = 30MHz,		–68		dB
Off Isolation	f = 5MHz,		–75		dB
	f = 30MHz		–76		dB
TIME DOMAIN					
RISE/FALL TIME	$V_{OUT} = 1.4Vp\text{-}p$, Step 10% to 90%				
	$C_{OUT} = 1pF$, $R_{OUT} = 22\Omega$		2.5		ns
SLEW RATE	$V_{OUT} = 1.4Vp\text{-}p$				
	$C_{OUT} = 1pF$		500		V/µs
	$C_{OUT} = 22pF$		360		V/µs
	$C_{OUT} = 47pF$		260		V/µs

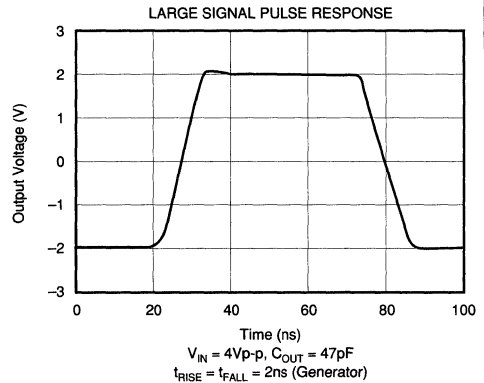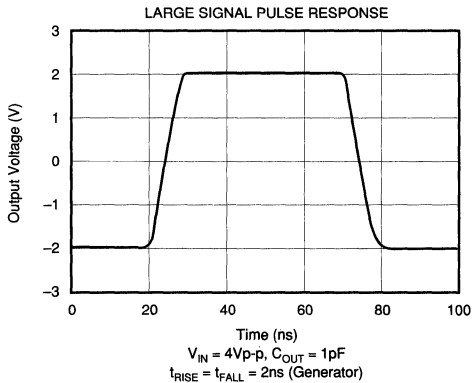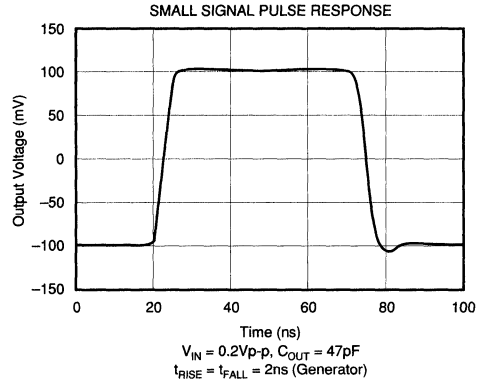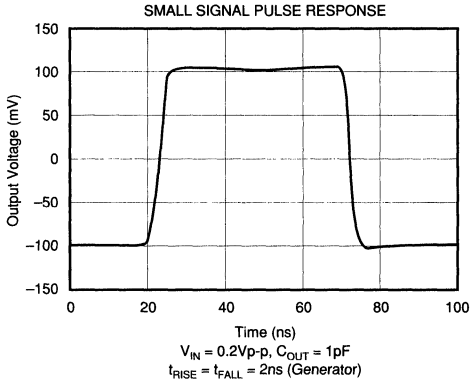# SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE –40°C TO +85°C)

At $V_{CC} = \pm5VDC$, $R_L = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP/AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE			14	±35	mV
TRANSFER CHARACTERISTICS	Voltage Gain				
	$R_L = 10k\Omega$	0.95	0.992	0.997	V/V
INPUT BIAS CURRENT			+4	±10	µA
RATED OUTPUT					
Voltage Output	$G \geq 0.90$, $R_L = 10k\Omega$	±2.8	±3.8	±4	V
POWER SUPPLY					
Quiescent Current	One Channel Selected		±4.6	±5.5	mA
	No Channel Selected		±250	±350	µA

CHANNEL SELECTION

PARAMETER	CONDITIONS	MPC102AP/AU			UNITS
		MIN	TYP	MAX	
SELECTION INPUTS					
Logic 1 Voltage				V_{CC} +0.6	V
Logic 0 Voltage		+2		+0.8	V
Logic 1 Current	V_{SEL} = 5.0V	75	100	125	μA
Logic 0 Current	V_{SEL} = 0.8V		0.002	5	μA
SWITCHING CHARACTERISTICS	V_{IN} = −0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_{OUT} = 1Vp-p		0.25		μs
SEL to Channel OFF Time	10% Point of V_{OUT} = 1Vp-p		0.25		μs
Switching Transient, Positive	Measured While Switching		6		mV
Switching Transient, Negative	Between Two Grounded Channels		−8		mV

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (±V_{CC}) .... ±6VDC
Analog Input Voltage (IN_1 through IN_4) .... ±V_{CC}, ±0.7V
Operating Temperature .... −40°C to +85°C
Storage Temperature .... −40°C to +125°C
Output Current .... ±6mA
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
Digital Input Voltages (SEL_1 through SEL_4) .... −0.5V to +V_{CC} +0.7V

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC102AP	14-Pin DIP	010
MPC102AU	14-Pin SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC102AP	14-Pin Plastic DIP	−40°C to +85°C
MPC102AU	14-Pin SOIC	−40°C to +85°C

DICE INFORMATION

MPC102AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Input 1
2	Ground
3	Input 2
4	+5V Supply
5	Input 3
6	Ground
7	Input 4
8	Select 4
9	Select 3
10	Output 2
11	−5V Supply
12	Output 1
13	Select 2
14	Select 1

Substrate Bias: Negative Supply.
NC: No Connection.
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	51 x 76 ±5	1.295 x 1.93 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, −0.0	0.0005, +0.0013, −0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

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TYPICAL PERFORMANCE CURVES

At $V_{CC} = \pm5VDC$, $R_{LOAD} = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.
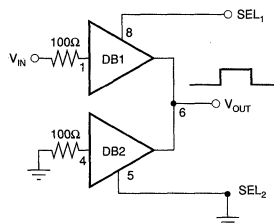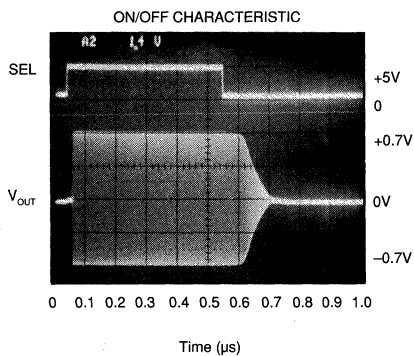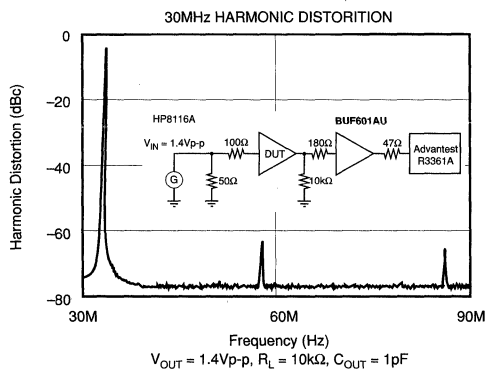
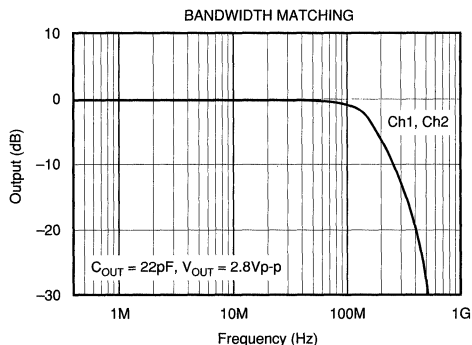INPUT OFFSET VOLTAGE vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT IMPEDANCE vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

TOTAL POSITIVE QUIESCENT CURRENT
vs TEMPERATURE

TOTAL POSITIVE QUIESCENT CURRENT
vs TEMPERATURE

TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm5VDC$, $R_{LOAD} = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

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TRANSFER FUNCTION

GAIN ERROR vs INPUT VOLTAGE

INPUT VOLTAGE NOISE SPECTRAL DENSITY

SWITCHING ENVELOPE
(Channel-to-Channel Switching)

SWITCHING TRANSIENTS
(Channel-to-Channel)

SWITCHING TRANSIENTS
(Channel-to-Channel)

TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE

C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 2ns
(Generator), V_{IN} = 0.2Vp-p

SMALL SIGNAL PULSE RESPONSE

C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator), V_{IN} = 0.2Vp-p

LARGE SIGNAL PULSE RESPONSE

C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator), V_{IN} = 5Vp-p

LARGE SIGNAL PULSE RESPONSE

C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator), V_{IN} = 5Vp-p

GROUP DELAY TIME vs FREQUENCY

BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}

C_{OUT}	R_{OUT}	f_{-3dB}
1pF	0Ω	410MHz
10pF	30Ω	310MHz
22pF	22Ω	220MHz
33pF	13Ω	155MHz
47pF	11Ω	140MHz

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TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

GAIN FLATNESS

V_{IN} = 0.2Vp-p

BANDWIDTH vs OUTPUT VOLTAGE

5Vp-p
2.8Vp-p
1.4Vp-p
0.2Vp-p

BANDWIDTH vs R_{LOAD}

R_L = 10kΩ
R_L = 500Ω

V_{IN} = 2.8Vp-p, C_{OUT} = 22pF

BANDWIDTH MATCHING (DB1...DB4)

C_{OUT} = 22pF, R_{OUT} = 15Ω, V_{OUT} = 2.8Vp-p

30MHz HARMONIC DISTORTION

Δ MKR
30.00 MHz
-65.59 dB

Frequency (Hz)
V_{OUT} = 1.4Vp-p, R_L = 350Ω, C_{OUT} = 1pF

ON/OFF CHARACTERISTIC

SEL_1
+0.7V

0V

-0.7V

SEL_1

150Ω
V_{IN} — DB1

V_{OUT1}

150Ω
DB2

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MULTIPLEXERS

APPLICATIONS INFORMATION

The MPC102 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

As shown below, all pins on the MPC102 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the characteristics of the buffer amplifier input without necessarily destroying the device. In precision buffer amplifiers, such damage may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC102.

Static damage has been well-recognized as a problem for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC102 incorporates on-chip ESD protection diodes as shown in Figure 1. Thus the user does not need to add external protection diodes, which can add capacitance and degrade AC performance.
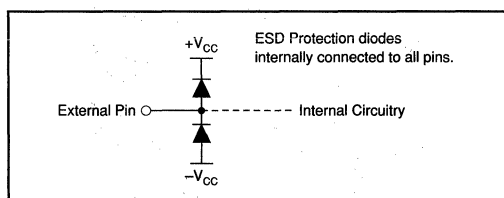
FIGURE 1. Internal ESD Protection.

DISCUSSION
OF PERFORMANCE

The MPC102 is a dual, 2 x 1, wide-band analog signal multiplexer. It allows the user to connect one of the two inputs (IN_1/IN_2 or IN_3/IN_4) to the corresponding output. The switching speed between two input channels is typically less than 300ns.

However, in contrast to signal switches using CMOS or DMOS transistors, the switching transients were kept very low at +6mV and –8mV. The MPC102 consists of four identical unity-gain buffer amplifiers, respectively. Two of the four amplifiers are connected together internally at the output. The open-loop buffer amps, which consist of complementary emitter followers, apply no feedback so their low-frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form a unidirectional transmission path, thus providing high output-to-input isolation. Switching stages compatible to TTL-level digital signals are provided for each buffer to select the input channel. When no channel is selected, the outputs of the device are high-impedance and allow the user to wire several MPC102s together to create multichannel switch matrices.

Chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. The buffers require DC coupling and termination resistors when driven directly from a low-impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated, high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 210MHz at an output voltage of 1.4Vp-p allows the design of multi-channel crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz, or in quality for high resolution graphic and imaging systems with 200MHz system bandwidth. The buffer amplifiers also offer low differential gain (0.02%) and phase (0.02°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the luminance signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC102 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short

time, but it hardly interferes with the input signals. The transient peaks remain less than +6mV and –8mV. The generated output transients are extremely small, so DC clamping during switching between channels is unnecessary. DC clamping during the switching dead time is required to avoid synchronization by large negative output glitches in subsequent equipment.

The SEL-to-channel-ON time is typically 25ns and always shorter than the typical SEL-to-channel-OFF time of 250ns. In the worst case, an ON/OFF margin of 150ns ensures safe switching even for timing spreads in the digital control latches. The short interchannel switching time of 300ns allows channel change during the vertical blanking time, even in high-resolution graphic or broadcast systems. As shown in the typical performance curves, the signal envelope during transition from one channel to another rises and falls symmetrically and shows less overshooting and DC settling effects.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffer amplifiers are in the off-state. One important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±250µA when no channel is selected and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC102 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

• Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.

• PC board traces for signal and power lines should be wide to reduce impedance or inductance.

• Make short and low inductance traces. The entire physical circuit should be as small as possible.

• Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection.

• Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.

• Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.

• Use low-inductance and surface-mounted components. Circuits using all surface mount components with the MPC102 will offer the best AC-performance.

• A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.

• Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the MPC102 to speed prototyping. This board allows easy and fast performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. The demo board is available as DEM-MPC102-1GC. Please contact your local sales office to receive more information.
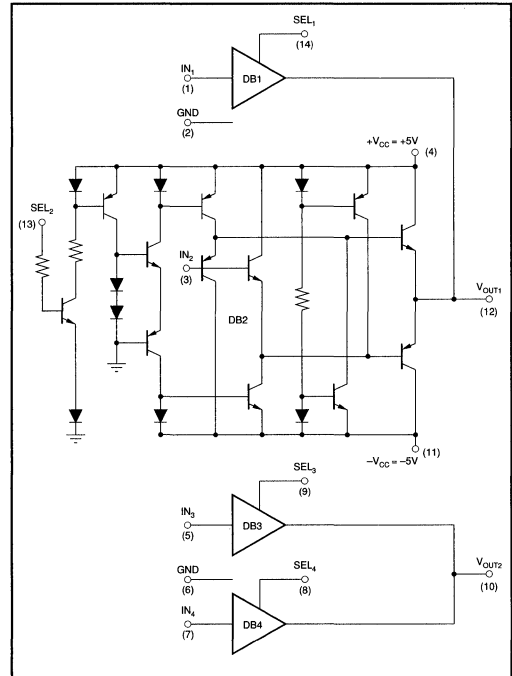
FIGURE 2. Simplified Circuit Diagram.

FIGURE 3. All Hostile Crosstalk Test Circuit 1.

CHANNEL	SEL $_1$	SEL $_2$	SEL $_3$	SEL $_4$	IN$_1$	IN$_2$	IN$_3$	IN$_4$	R$_{IN1}$	R$_{IN2}$	R$_{IN3}$	R$_{IN4}$	V$_{OUT}$
DB1	1	0	0	0	GND	V$_{IN}$	GND	GND	200Ω	150Ω	150Ω	150Ω	1
DB2	0	1	0	0	V$_{IN}$	GND	GND	GND	150Ω	200Ω	150Ω	150Ω	1
DB3	0	0	1	0	GND	GND	GND	V$_{IN}$	150Ω	150Ω	200Ω	150Ω	2
DB4	0	0	0	1	GND	GND	V$_{IN}$	GND	150Ω	150Ω	150Ω	200Ω	2
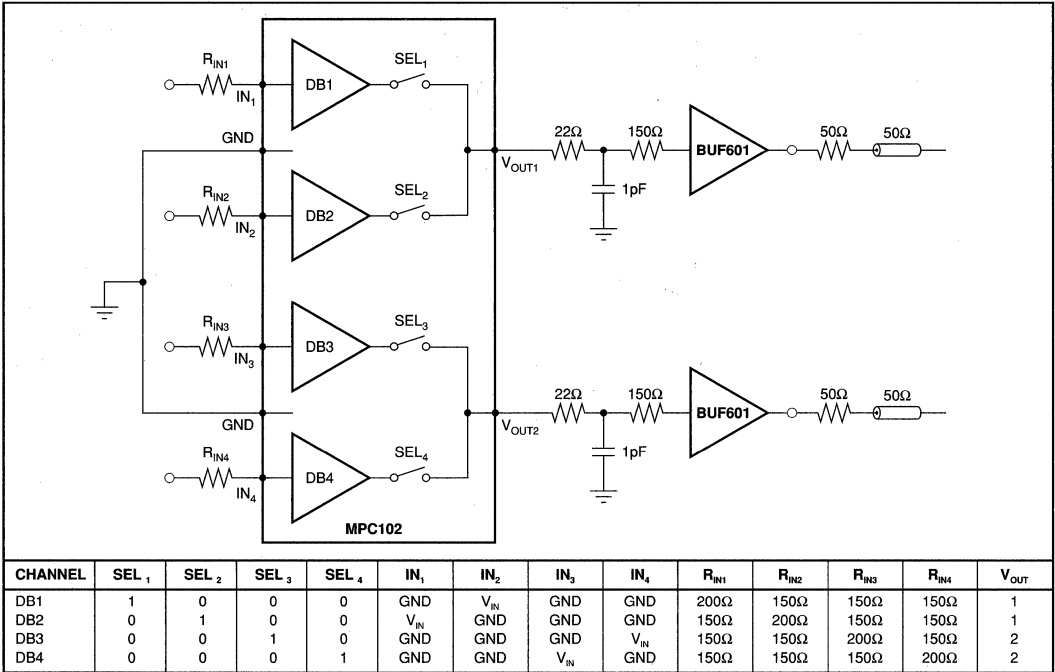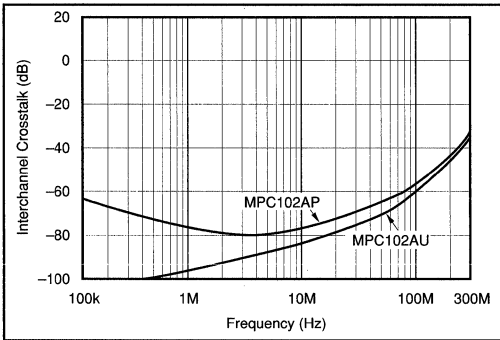
FIGURE 4. Interchannel Crosstalk.
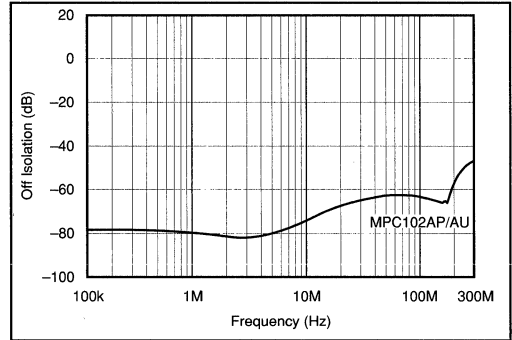
FIGURE 6. Off Isolation Crosstalk.
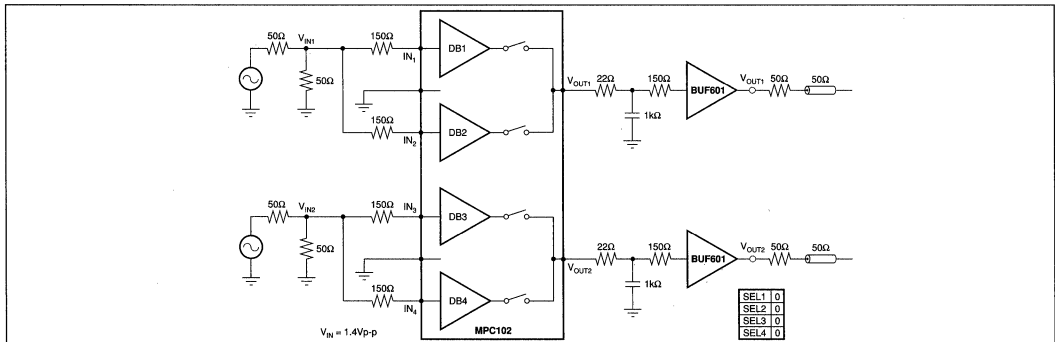
FIGURE 5. Off Isolation Crosstalk Test Circuit 2.

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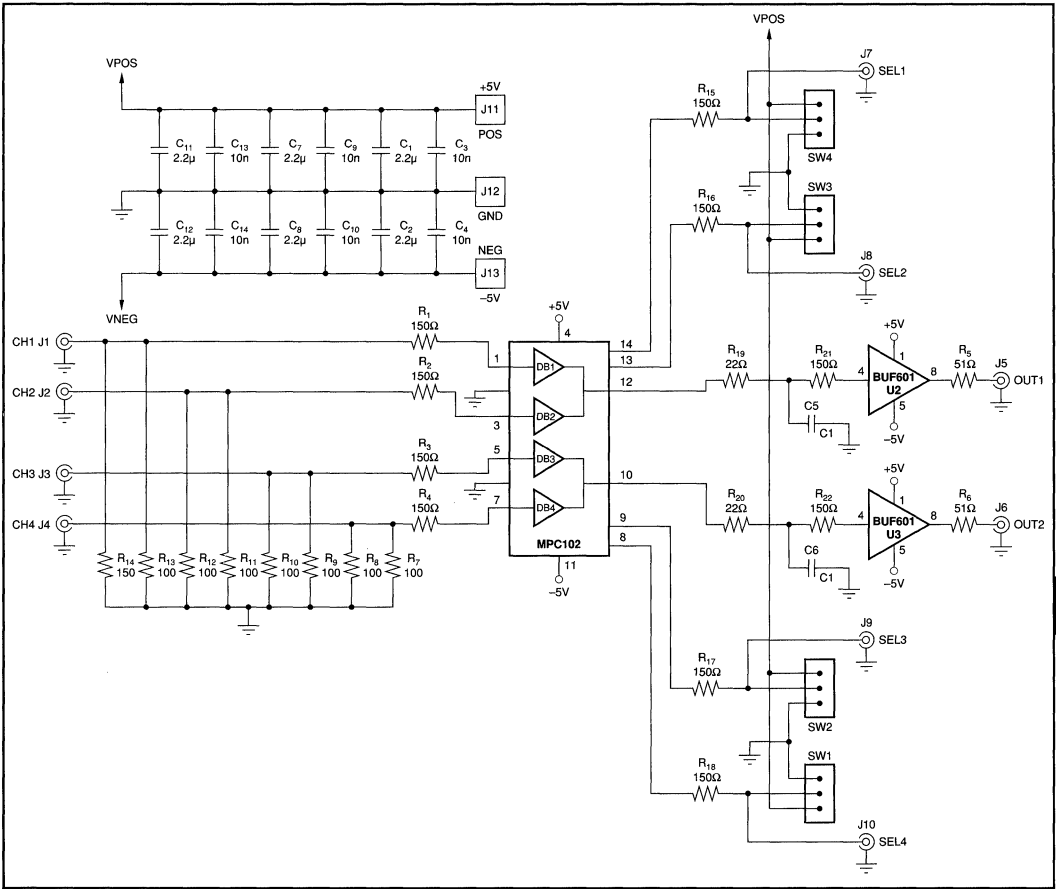
FIGURE 7. Circuit Schematic DEM-MPC102-1GC.

| Component Side | Silk Screen | Solder Side |
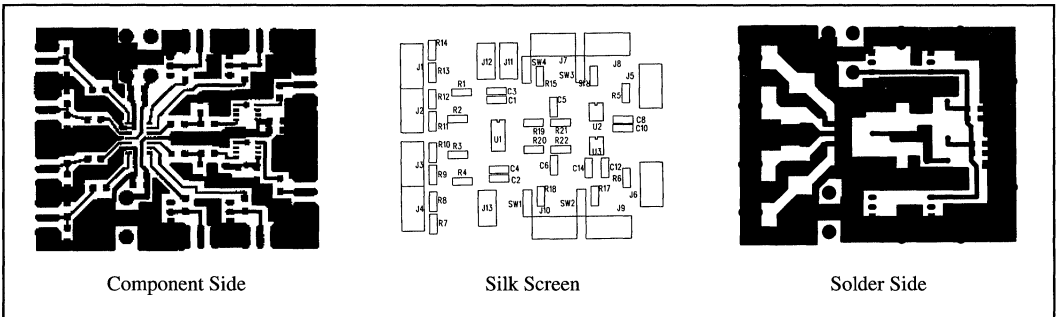
FIGURE 8. Silk Screen and Board Layout of DEM-MPC102-1GC.

MPC102

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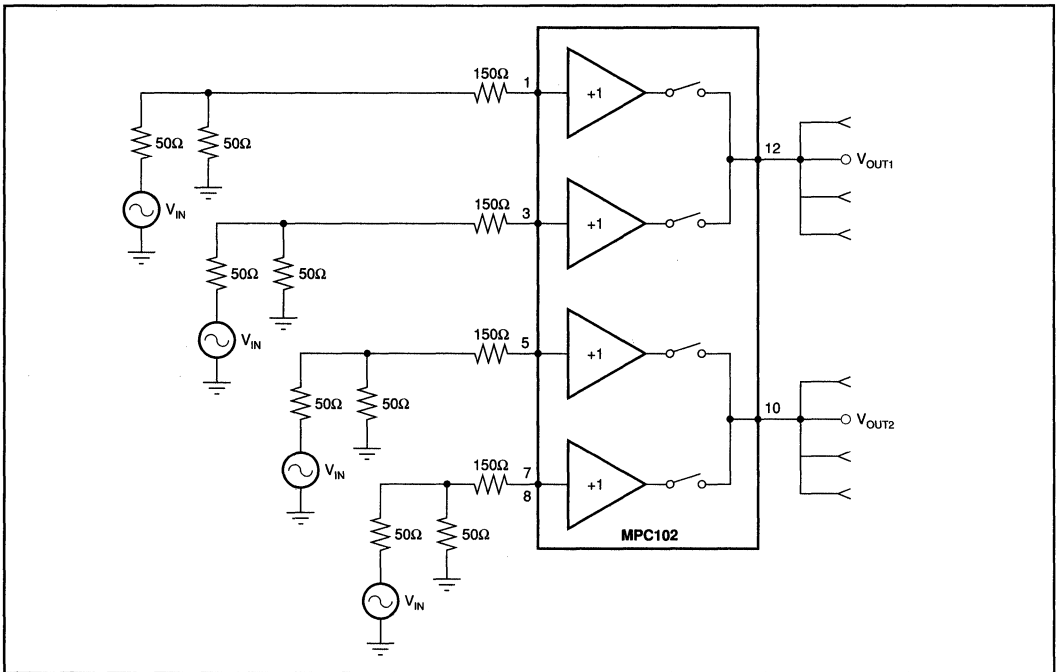
MULTIPLEXERS

FIGURE 9. Dual 2 x 1 Video Multiplexer.
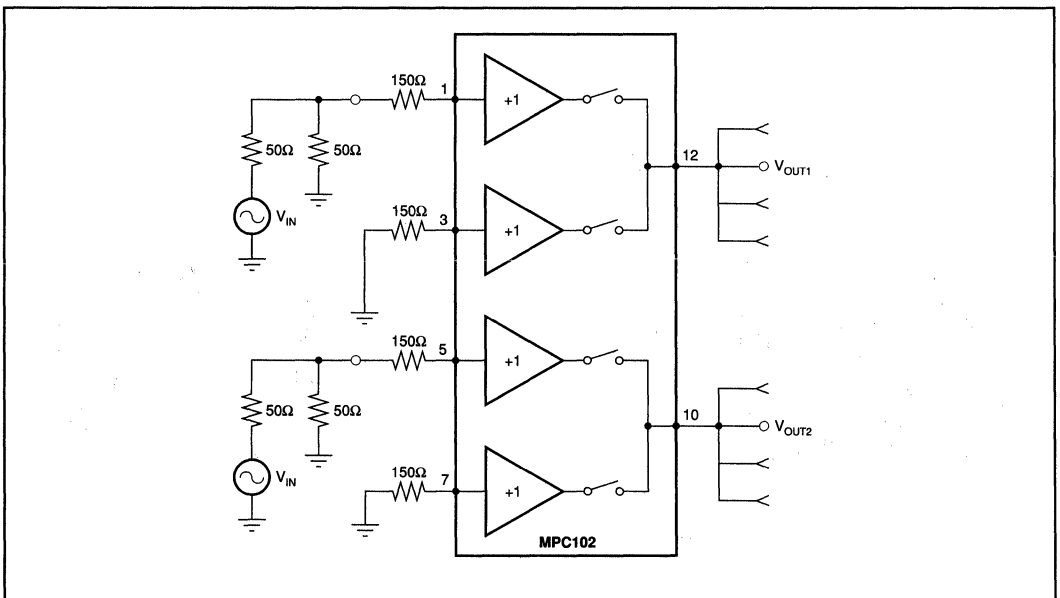
FIGURE 10. Signal Source to GND Switch.
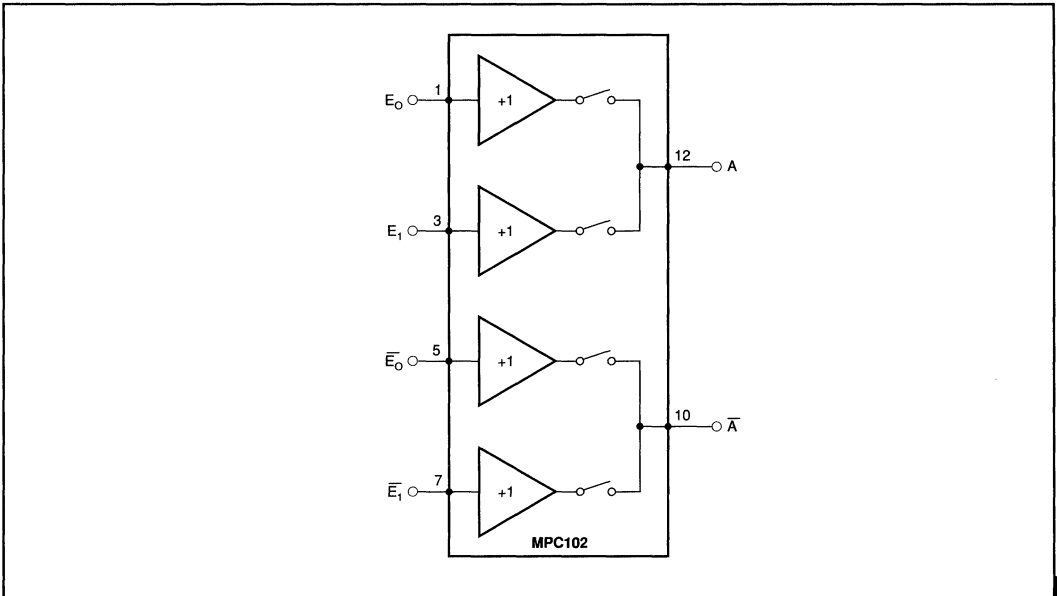
FIGURE 11. 2 x 1 Multiplexer for Differential Analog and Digital ECL Data.
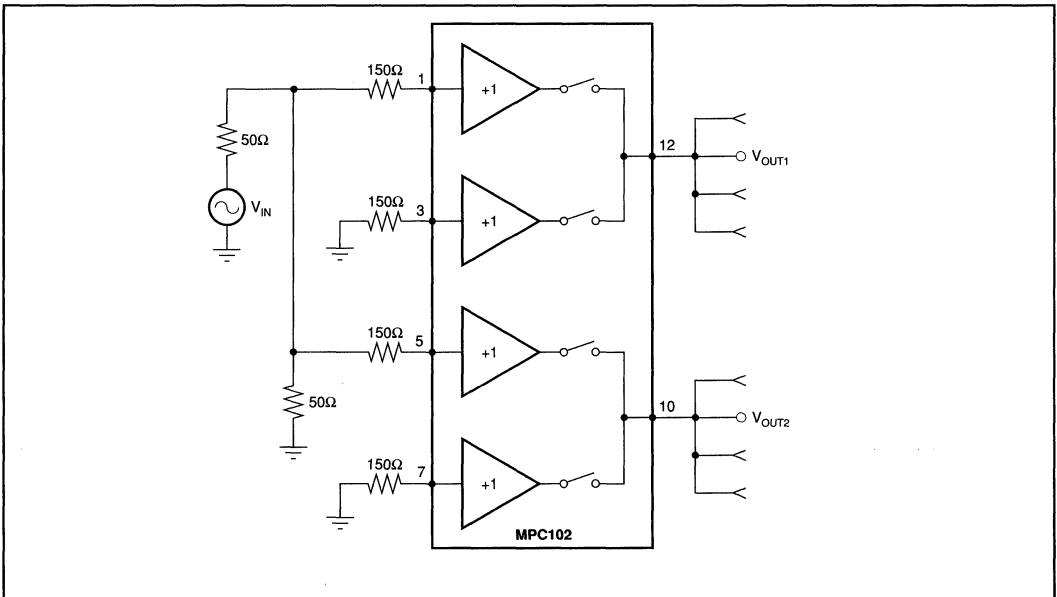
FIGURE 12. 1 x 2 Demultiplexer.

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MULTIPLEXERS
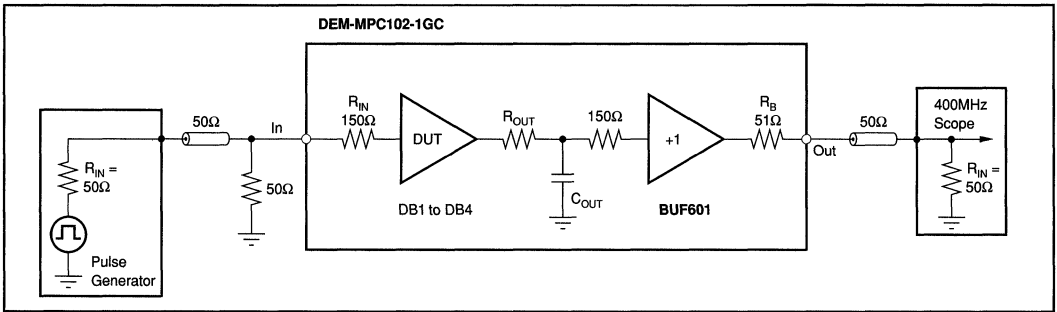
FIGURE 13. Test Circuit Pulse Response.
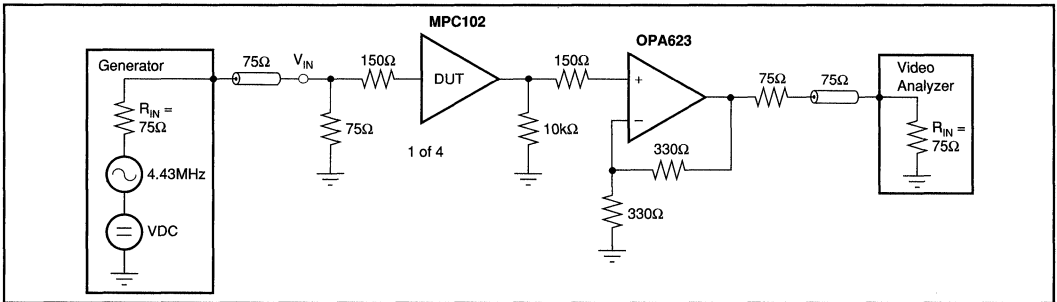
FIGURE 14. Test Circuit Differential Gain and Phase.
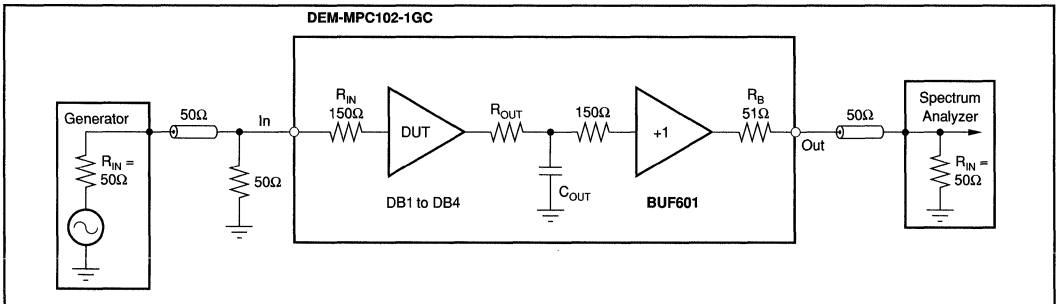
FIGURE 15. Test Circuit Frequency Response.
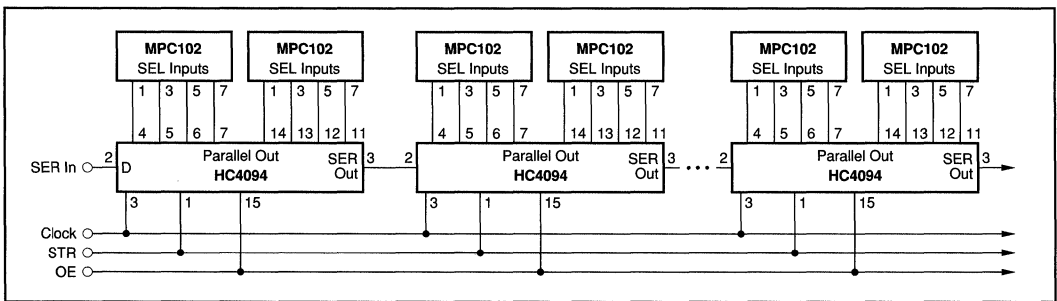
FIGURE 16. Serial Bus-Controlled Distribution Field.

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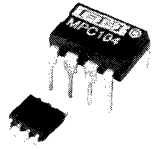
MPC104

Wide-Bandwidth
2 x 1 VIDEO MULTIPLEXER

FEATURES
- **BANDWIDTH: 210MHz (1.4Vp-p)**
- **LOW INTERCHANNEL CROSSTALK:**
  –79dB (30MHz, SO); –77dB (30MHz, DIP)
- **LOW SWITCHING TRANSIENTS:**
  +13mV/–4mV
- **LOW DIFFERENTIAL GAIN/PHASE**
  ERRORS: 0.03%, 0.01°
- **LOW QUIESCENT CURRENT:**
  One Channel Selected: ±4.6mA
  No Channel Selected: ±120µA

APPLICATIONS
- **VIDEO ROUTING AND MULTIPLEXING**
  (CROSSPOINTS)
- **RADAR SYSTEMS**
- **DATA ACQUISITION**
- **INFORMATION TERMINALS**
- **SATELLITE OR RADIO LINK IF ROUTING**

DESCRIPTION
The MPC104 is a wide-bandwidth, 2-to-1 channel video signal multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC104 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC104 consists of two identical monolithic, integrated, open-loop buffer amplifiers, which are connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC104 multiplexer enables the user to connect one of two input signals to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $5nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 8-pin SO and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)
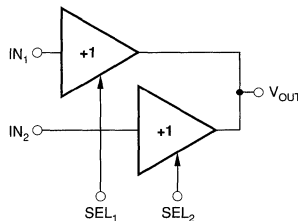
TRUTH TABLE

SEL$_1$	SEL$_2$	V$_{OUT}$
0	0	HI-Z
1	0	IN$_1$
0	1	IN$_2$

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SPECIFICATIONS–DC CHARACTERISTICS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 10k\Omega$, $R_{IN} = 100\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	MPC104AP, AU MIN	MPC104AP, AU TYP	MPC104AP, AU MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial			14	±30	mV
vs Temperature			60		µV/°C
vs Supply (Tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$	−40	−80		dB
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		−50		dB
vs Supply (Non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$		−50		dB
Initial Matching	All Buffers		3		mV
INPUT BIAS CURRENT					
Initial			5	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$		±710		nA/V
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		0.26		µA/V
vs Supply (Non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$		1.7		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	$f_{OUT} = 20kHz$ to $10MHz$		5		nV/√Hz
Signal-to-Noise Ratio	$S/N = 0.7/V_N \cdot \sqrt{5MHz}$		−96		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±3.6		V
TRANSFER CHARACTERISTICS					
Voltage Gain	$R_L = 1k\Omega$, $V_{IN} = \pm 2V$		0.982		V/V
	$R_L = 10k\Omega$, $V_{IN} = \pm 2.8V$	0.98	0.992		V/V
RATED OUTPUT					
Voltage	$V_{IN} = \pm 3V$	±2.8	±2.97		V
Resistance	One Channel Selected		12.5		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.2		pF
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2		$V_{CC} +0.6$	V
Logic 0 Voltage				+0.8	V
Logic 1 Current	$V_{SEL} = 5.0V$	75	100	125	µA
Logic 0 Current	$V_{SEL} = 0.8V$		0.002	5	µA
SWITCHING CHARACTERISTICS	$V_I = -0.3V$ to $+0.7V$, $f = 5MHz$				
SEL to Channel ON Time	90% Point of $V_{OUT} = 1Vp-p$		0.13		µs
SEL to Channel OFF Time	10% Point of $V_{OUT} = 1Vp-p$		0.17		µs
Switching Transient, Positive	(Measured While Switching		+13		mV
Switching Transient, Negative	Between Two Grounded Channels)		−4		mV
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected, Over Temperature		±4.6	±5.3	mA
	No Channel Selected, Over Temperature		±120	±175	µA
Rejection Ratio			−80		dB

SPECIFICATIONS– AC CHARACTERISTICS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 10k\Omega$, $R_{IN} = 100\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	MPC104AP, AU			UNITS
		MIN	TYP	MAX	
LARGE SIGNAL BANDWIDTH (–3dB)	$V_{OUT} = 5.0Vp\text{-}p$, $C_{OUT} = 1pF$		55		MHz
	$V_{OUT} = 2.8Vp\text{-}p$, $C_{OUT} = 1pF$		101		MHz
	$V_{OUT} = 1.4Vp\text{-}p$, $C_{OUT} = 1pF$		210		MHz
SMALL SIGNAL BANDWIDTH	$V_{OUT} = 0.2Vp\text{-}p$, $C_{OUT} = 1pF$		590		MHz
GROUP DELAY TIME			550		ps
DIFFERENTIAL GAIN	$f = 4.43MHz$, $V_{IN} = 0.3Vp\text{-}p$				
	VDC = 0 to 0.7V		0.03		%
DIFFERENTIAL PHASE	$f = 4.43MHz$, $V_{IN} = 0.3Vp\text{-}p$				
	VDC = 0 to 0.7V		0.01		Degrees
GAIN FLATNESS PEAKING	$V_{OUT} = 0.2Vp\text{-}p$, DC to 30MHz		0.05		dB
	$V_{OUT} = 0.2Vp\text{-}p$, DC to 100MHz		0.07		dB
HARMONIC DISTORTION	$f = 30MHz$, $V_{OUT} = 1.4Vp\text{-}p$				
Second Harmonic			–63		dBc
Third Harmonic			–65		dBc
CROSSTALK	$V_{IN} = 1.4Vp\text{-}p$				
MPC104AP All Hostile	$f = 5MHz$,		–90		dB
	$f = 30MHz$,		–77		dB
Off Isolation	$f = 5MHz$,		–93		dB
	$f = 30MHz$,		–81		dB
MPC104AU All Hostile	$f = 5MHz$,		–95		dB
	$f = 30MHz$,		–79		dB
Off Isolation	$f = 5MHz$,		–93		dB
	$f = 30MHz$		–86		dB
RISE/FALL TIME	$V_{OUT} = 1.4Vp\text{-}p$, Step 10% to 90%				
	$C_{OUT} = 1pF$, $R_{OUT} = 22\Omega$		2.3		ns
SLEW RATE	$V_{OUT} = 1.4Vp\text{-}p$				
	$C_{OUT} = 1pF$		500		V/μs
	$C_{OUT} = 22pF$		360		V/μs
	$C_{OUT} = 47pF$		260		V/μs

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CONNECTION DIAGRAM

Top View   SO/DIP

```
       IN₁  │1        +1        8│  SEL₁
       GND  │2                  7│  −V_CC
      +V_CC │3                  6│  V_OUT
       IN₂  │4        +1        5│  SEL₂
```

PIN DESCRIPTION

PIN	DESCRIPTION
IN₁, IN₂	Analog Input Channels
GND	Analog Input Shielding Grounds, Not Internally Connected
SEL₁, SEL₂	Channel Selection Inputs
V_OUT	Analog Output; tracks selected channel
−V_CC	Negative Supply Voltage; typical −5VDC
+V_CC	Positive Supply Voltage; typical +5VDC

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$) .... $\pm$6VDC
Analog Input Voltage (IN₁ through IN₂) .... $\pm V_{CC}$, $\pm$0.7V
Operating Temperature .... −40°C to +85°C
Storage Temperature .... −40°C to +125°C
Output Current .... $\pm$6mA
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
Digital Input Voltages (SEL₁ through SEL₂) .... −0.5V to +V_CC +0.7V

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC104AP	8-Pin DIP	006
MPC104AU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC104AP	8-Pin Plastic DIP	−40°C to +85°C
MPC104AU	8-Pin SOIC	−40°C to +85°C

DICE INFORMATION

ICC02077R

PAD	FUNCTION
1	Input 1
2	Ground
3	+5V Supply
4	Input 2
5	Select 2
6	Output
7	−5V Supply
8	Select 1

Substrate Bias: Negative Supply.
NC: No Connection.
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	44 x 47 ±5	1.13 x 1.19 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, −0.0	0.0005, +0.0013, −0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

MPC104AD DIE TOPOGRAPHY

TYPICAL PERFORMANCE CURVES

At $V_{CC} = \pm5VDC$, $R_L = 10k\Omega$, $R_{IN} = 100\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

INPUT OFFSET VOLTAGE vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT IMPEDANCE vs FREQUENCY

OUTPUT IMPEDANCE vs FREQUENCY

TOTAL POSITIVE QUIESCENT CURRENT vs TEMPERATURE

One Channel Selected

TOTAL POSITIVE QUIESCENT CURRENT vs TEMPERATURE

No Channel Selected

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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm5VDC$, $R_L = 10k\Omega$, $R_{IN} = 100\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

TRANSFER FUNCTION

GAIN ERROR vs INPUT VOLTAGE

INPUT VOLTAGE NOISE SPECTRAL DENSITY

SWITCHING ENVELOPE
(Channel-to-Channel Switching)

SWITCHING TRANSIENTS

SWITCHING TRANSIENTS

TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 10k\Omega$, $R_{IN} = 100\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25°C$, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE

$V_{IN} = 0.2Vp\text{-}p$, $C_{OUT} = 1pF$
$t_{RISE} = t_{FALL} = 2ns$ (Generator)

SMALL SIGNAL PULSE RESPONSE

$V_{IN} = 0.2Vp\text{-}p$, $C_{OUT} = 47pF$
$t_{RISE} = t_{FALL} = 2ns$ (Generator)

LARGE SIGNAL PULSE RESPONSE

$V_{IN} = 4Vp\text{-}p$, $C_{OUT} = 1pF$
$t_{RISE} = t_{FALL} = 2ns$ (Generator)

LARGE SIGNAL PULSE RESPONSE

$V_{IN} = 4Vp\text{-}p$, $C_{OUT} = 47pF$
$t_{RISE} = t_{FALL} = 2ns$ (Generator)

GROUP DELAY TIME vs FREQUENCY

$V_{IN} = 1.4Vp\text{-}p$

BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}

C_{OUT}	R_{OUT}	f_{-3dB}
1pF	0Ω	571MHz
10pF	27Ω	364MHz
22pF	16Ω	279MHz
33pF	12Ω	231MHz
47pF	8Ω	188MHz

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TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

GAIN FLATNESS

BANDWIDTH vs OUTPUT VOLTAGE

BANDWIDTH vs R_{LOAD}

BANDWIDTH MATCHING

30MHz HARMONIC DISTORITION

V_{OUT} = 1.4Vp-p, R_L = 10kΩ, C_{OUT} = 1pF

ON/OFF CHARACTERISTIC

APPLICATIONS INFORMATION

The MPC104 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

As shown below, all pins on the MPC104 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the characteristics of the buffer amplifier input without necessarily destroying the device. In precision buffer amplifiers, such damage may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC104.

Static damage has been well-recognized as a problem for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC104 incorporates on-chip ESD protection diodes as shown in Figure 1. Thus the user does not need to add external protection diodes, which can add capacitance and degrade AC performance.
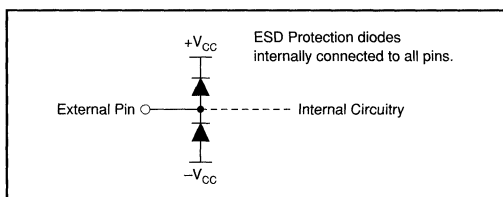
FIGURE 1. Internal ESD Protection.

DISCUSSION
OF PERFORMANCE

The MPC104 is a 2 x 1, wide-band analog signal multiplexer. It allows the user to connect one of the two inputs (IN_1/IN_2) to the output. The switching speed between two input channels is typically less than 300ns.

However, in contrast to signal switches using CMOS or DMOS transistors, the switching transients were kept very low at +13mV and –4mV. The MPC104 consists of two identical unity-gain buffer amplifiers, respectively connected together internally at the output. The open-loop buffer amps, which consist of complementary emitter followers, apply no feedback so their low-frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form a unidirectional transmission path, thus providing high output-to-input isolation. Switching stages compatible to TTL-level digital signals are provided for each buffer to select the input channel. When no channel is selected, the outputs of the device are high-impedance and allow the user to wire several MPC104s together to create multichannel switch matrices.

Chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. The buffers require DC coupling and termination resistors when driven directly from a low-impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated, high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 210MHz at an output voltage of 1.4Vp-p allows the design of multi-channel crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz, or in quality for high resolution graphic and imaging systems with 200MHz system bandwidth. The buffer amplifiers also offer low differential gain (0.03%) and phase (0.01°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the luminance signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.2pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC104 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short time, but it hardly interferes with the input signals. The transient peaks remain less than +13mV and –4mV. The generated output transients are extremely small, so DC clamping during switching between channels is unnecessary. DC clamping during the switching dead time is re-

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MULTIPLEXERS

quired to avoid synchronization by large negative output glitches in subsequent equipment.

The SEL-to-channel-ON time is typically 25ns and always shorter than the typical SEL-to-channel-OFF time of 250ns. In the worst case, an ON/OFF margin of 150ns ensures safe switching even for timing spreads in the digital control latches. The short interchannel switching time of 300ns allows channel change during the vertical blanking time, even in high-resolution graphic or broadcast systems. As shown in the typical performance curves, the signal envelope during transition from one channel to another rises and falls symmetrically and shows less overshooting and DC settling effects.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffer amplifiers are in the off-state. One important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of $\pm120\mu A$ when no channel is selected and $\pm4.6mA$ when one channel is selected, as well as the reduced $\pm5V$ supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC104 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

• Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately $2.2\mu F$), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.

• PC board traces for signal and power lines should be wide to reduce impedance or inductance.

• Make short and low inductance traces. The entire physical circuit should be as small as possible.

• Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection.

• Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.

• Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.

• Use low-inductance and surface-mounted components. Circuits using all surface mount components with the MPC104 will offer the best AC-performance.

• A resistor (100Ω to 150Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.

• Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

FIGURE 2. Simplified Circuit Diagram.

CHANNEL	SEL$_1$	SEL$_2$	IN$_1$	IN$_2$	R$_{IN1}$	R$_{IN2}$
DB1	1	0	GND	V$_{IN}$	200Ω	100Ω
DB2	0	1	V$_{IN}$	GND	100Ω	200Ω

FIGURE 3. All Hostile Crosstalk Test Circuit 1.

SEL$_1$	0
SEL$_2$	0
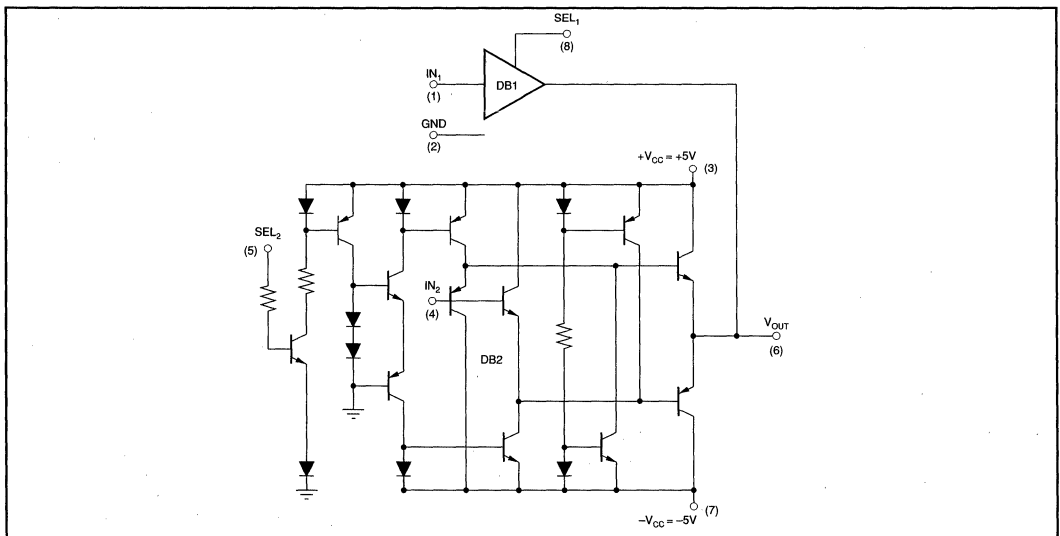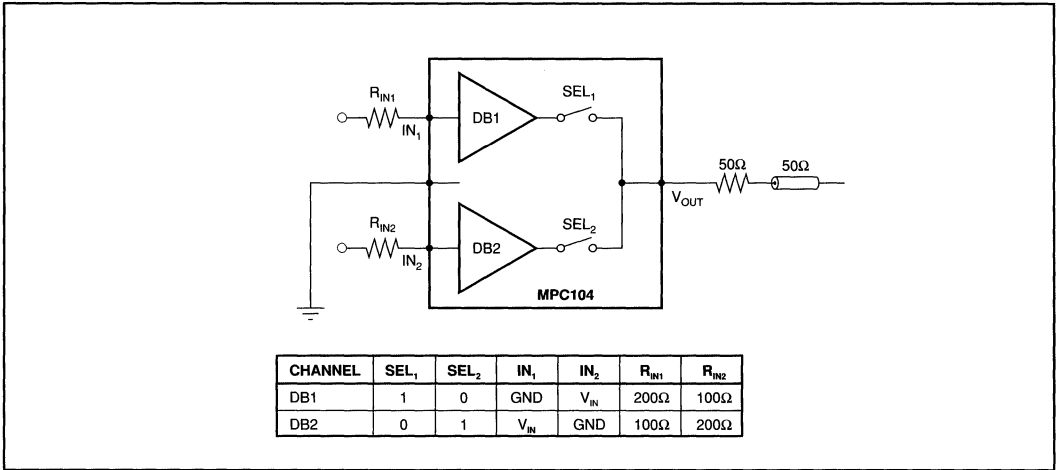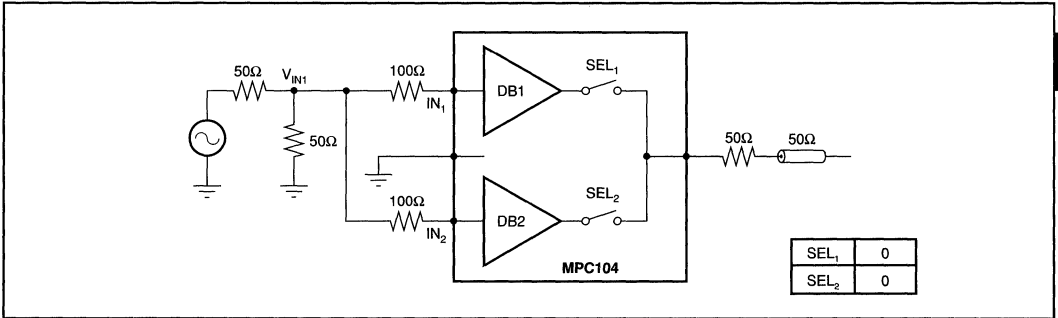
FIGURE 4. Off Isolation Crosstalk Test Circuit 2.
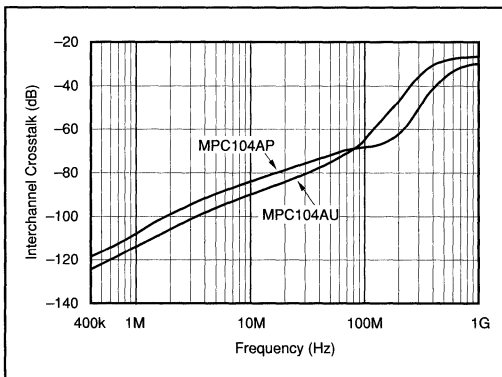
FIGURE 5. Interchannel Crosstalk.

FIGURE 6. Off Isolation Crosstalk.

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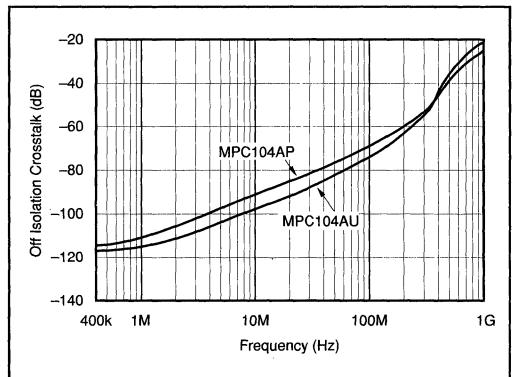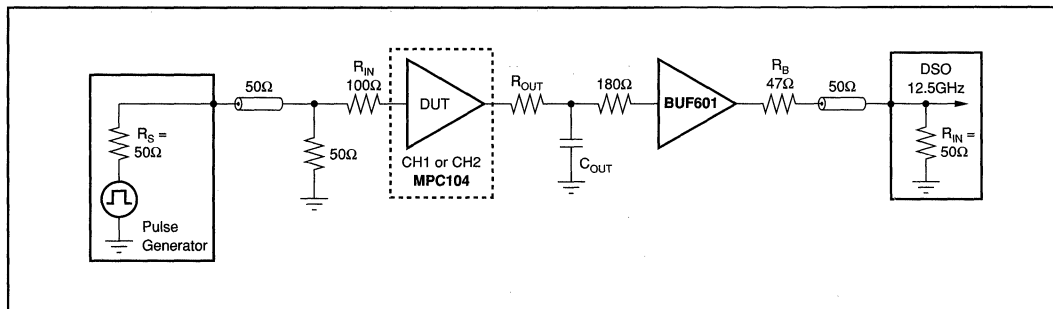
FIGURE 7. Test Circuit Pulse Response.
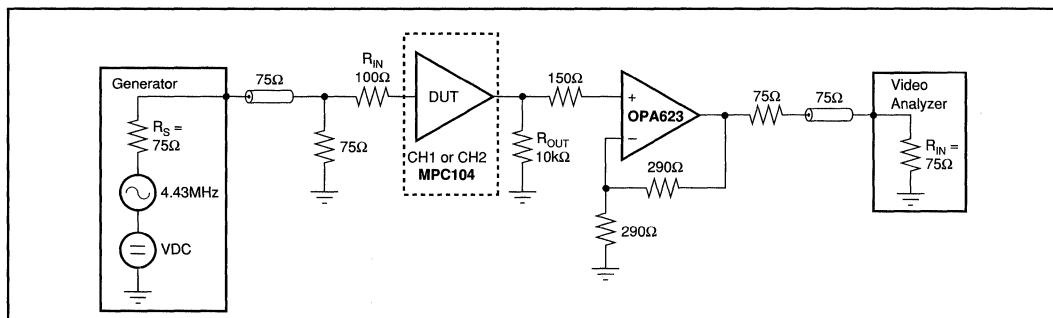
FIGURE 8. Test Circuit Differential Gain and Phase.
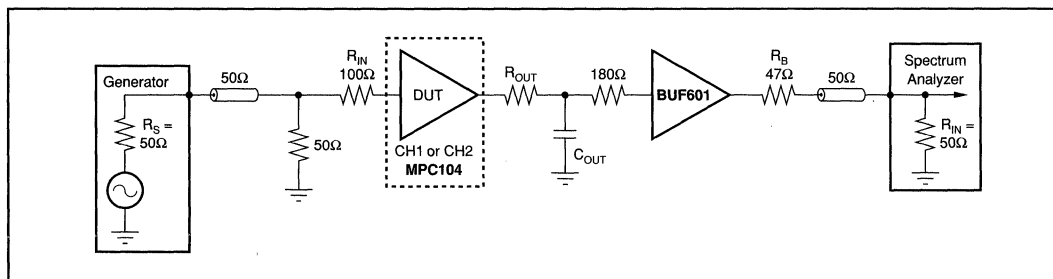
FIGURE 9. Test Circuit Frequency Response.
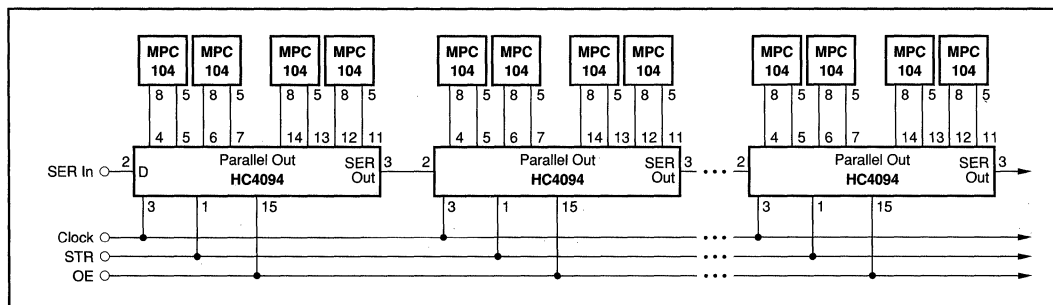
FIGURE 10. Serial Bus-Controlled Distribution Field.
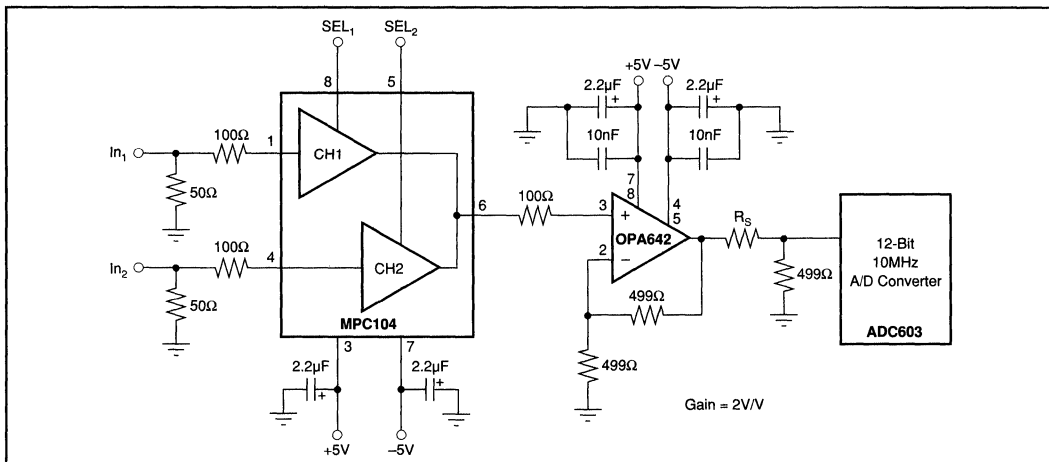
FIGURE 11. High-Speed Data Acquisition System.
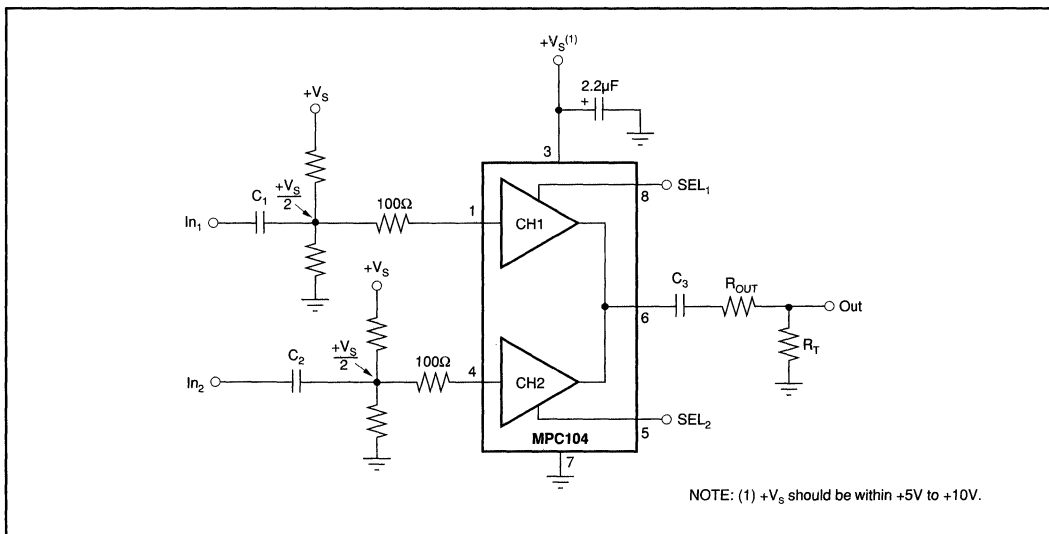
FIGURE 12. Single Supply Operation.

MPC104

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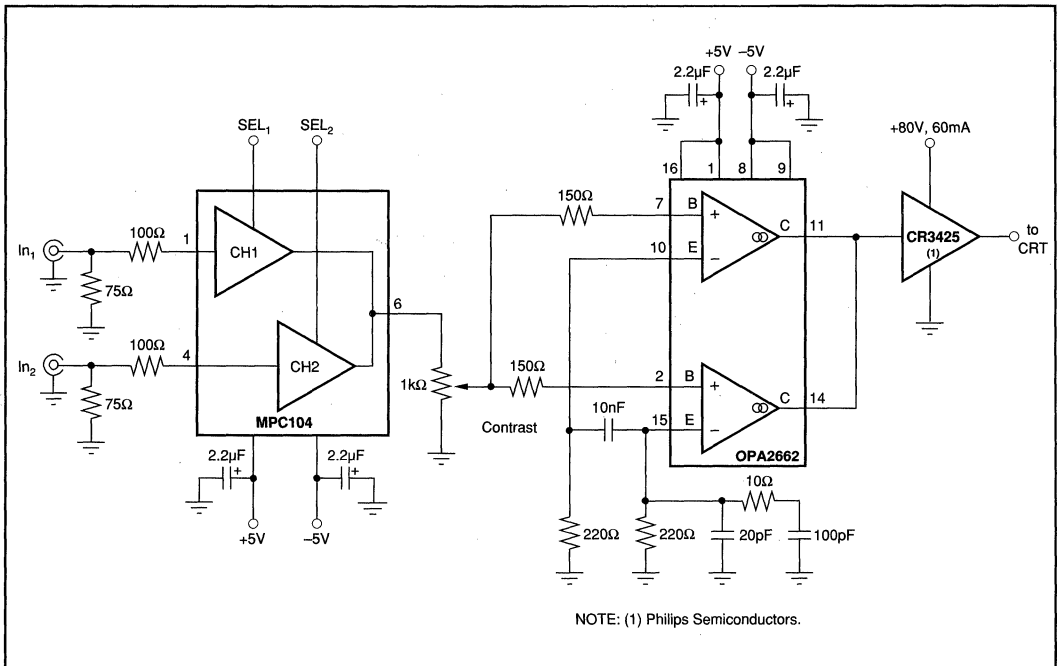
MULTIPLEXERS

FIGURE 13. Input Multiplexer for a CRT Output Stage.
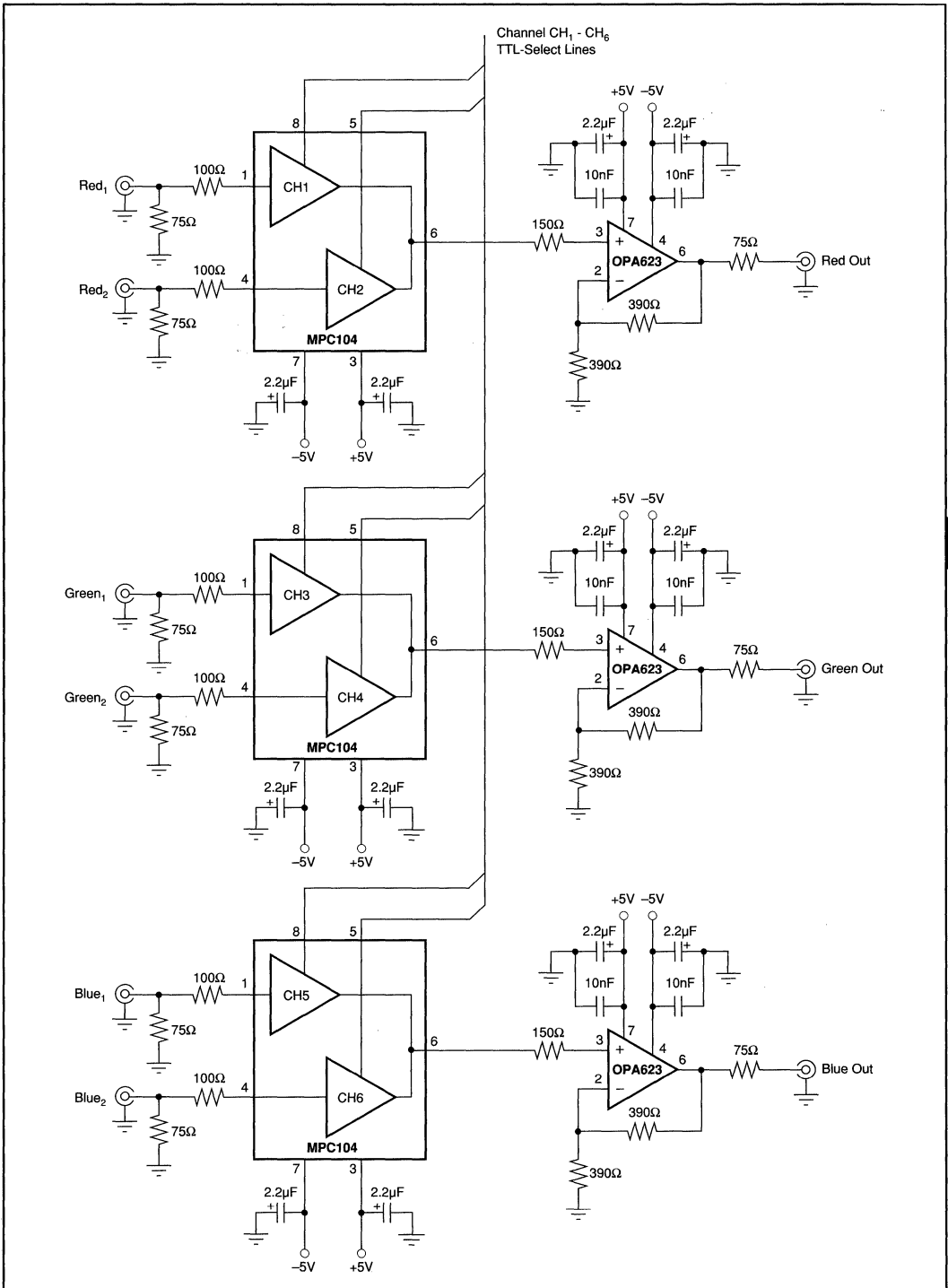
FIGURE 14. Input Multiplexer for RGB Video Signals.

BURR - BROWN ®
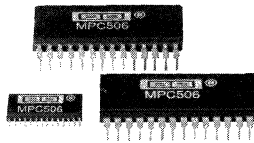
MPC506A
MPC507A

Single-Ended 16-Channel/Differential 8-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

● **ANALOG OVERVOLTAGE PROTECTION: 70Vp-p**
● **NO CHANNEL INTERACTION DURING OVERVOLTAGE**
● **BREAK-BEFORE-MAKE SWITCHING**
● **ANALOG SIGNAL RANGE: ±15V**
● **STANDBY POWER: 7.5mW typ**
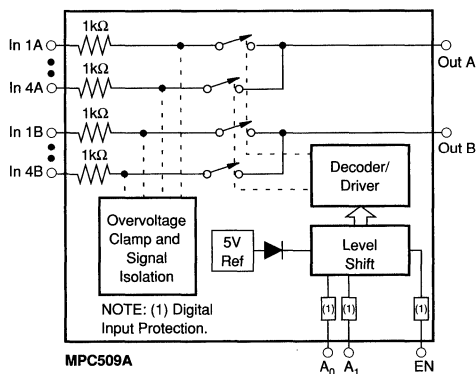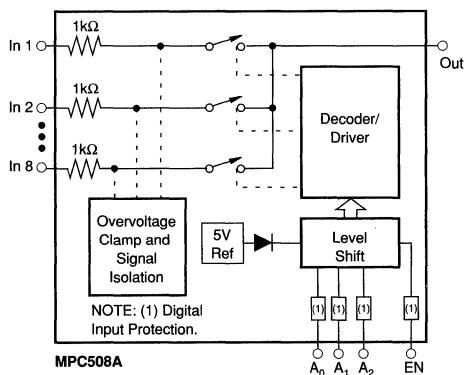● **TRUE SECOND SOURCE**

DESCRIPTION

The MPC506A is a 16-channel single-ended analog multiplexer, and the MPC507A is an 8-channel differential multiplexer.

The MPC506A and MPC507A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

These features make the MPC506A and MPC507A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC506A and MPC507A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic or plastic DIP and plastic SOIC packages. Temperature range is –40/+85°C.

FUNCTIONAL DIAGRAMS

MPC506A

MPC507A

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SPECIFICATIONS

ELECTRICAL

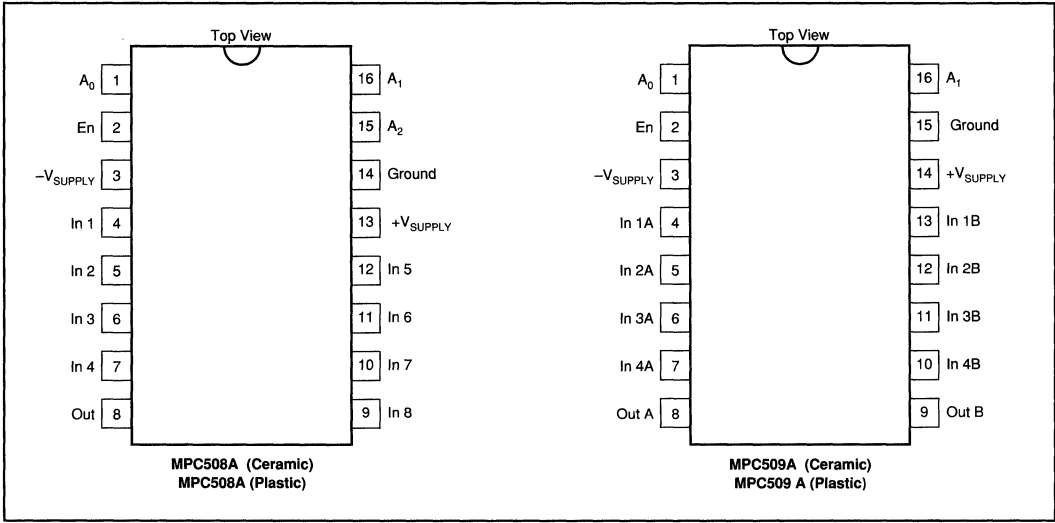Supplies = +15V, −15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V unless otherwise specified.

PARAMETER	TEMP	MPC506A/MPC507A			UNITS
		MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS					
V_S, Analog Signal Range	Full	−15		+15	V
R_{ON}, On Resistance[1]	+25°C		1.3	1.5	kΩ
	Full		1.5	1.8	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.5		nA
	Full			10	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.2		nA
MPC506A	Full			5	nA
MPC507A	Full			5	nA
I_D (OFF) with Input Overvoltage Applied[2]	+25°C		4.0		nA
	Full				μA
I_D (ON), On Channel Leakage Current	+25°C		2		nA
MPC506A	Full			10	nA
MPC507A	Full			10	nA
I_{DIFF} Differential Off Output Leakage Current					
(MPC507A Only)	Full			10	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold	Full			0.8	V
V_{AH}, Input High Threshold[3]	Full	4.0			V
V_{AL}, MOS Drive[4]	+25°C			0.8	V
V_{AH}, MOS Drive[4]	+25°C	6.0			V
I_A, Input Leakage Current (High or Low)[5]	Full			1.0	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.3		μs
	Full			0.6	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		200		ns
	Full			500	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		250		ns
	Full			500	ns
Settling Time (0.1%)	+25°C		1.2		μs
(0.01%)	+25°C		3.5		μs
"OFF Isolation"[6]	+25°C	50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5		pF
C_D (OFF), Channel Output Capacitance: MPC506A	+25°C		50		pF
MPC507A	+25°C		25		pF
C_A, Digital Input Capacitance	25°C		5		pF
C_{DS}, (OFF), Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
I+, Current Pin 1[7]	Full		0.7	1.5	mA
I−, Current Pin 27[7]	Full		5	20	μA

NOTES: (1) $V_{OUT} = \pm10V$, $I_{OUT} = -100\mu A$. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) $V_{REF} = +10V$. (5) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (6) $V_{EN} = 0.8V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 7Vrms$, f = 100kHz. Worst-case isolation occurs on channel 8 due to proximity of the output pins. (7) V_{EN}, $V_A = 0V$ or 4.0V.

MPC506/507

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MULTIPLEXERS

PIN CONFIGURATION

Top View

+V$_{SUPPLY}$	1		28	Out
NC	2		27	−V$_{SUPPLY}$
NC	3		26	In 8
In 16	4		25	In 7
In 15	5		24	In 6
In 14	6		23	In 5
In 13	7		22	In 4
In 12	8		21	In 3
In 11	9		20	In 2
In 10	10		19	In 1
In 9	11		18	Enable
Ground	12		17	Address A$_0$
V$_{REF}$	13		16	Address A$_1$
Address A$_3$	14		15	Address A$_2$

MPC506A (Ceramic)
MPC506A (Plastic)

Top View

+V$_{SUPPLY}$	1		28	Out A
Out B	2		27	−V$_{SUPPLY}$
NC	3		26	In 8A
In 8B	4		25	In 7A
In 7B	5		24	In 6A
In 6B	6		23	In 5A
In 5B	7		22	In 4A
In 4B	8		21	In 3A
In 3B	9		20	In 2A
In 2B	10		19	In 1A
In 1B	11		18	Enable
Ground	12		17	Address A$_0$
V$_{REF}$	13		16	Address A$_1$
NC	14		15	Address A$_2$

MPC507A (Ceramic)
MPC507A (Plastic)
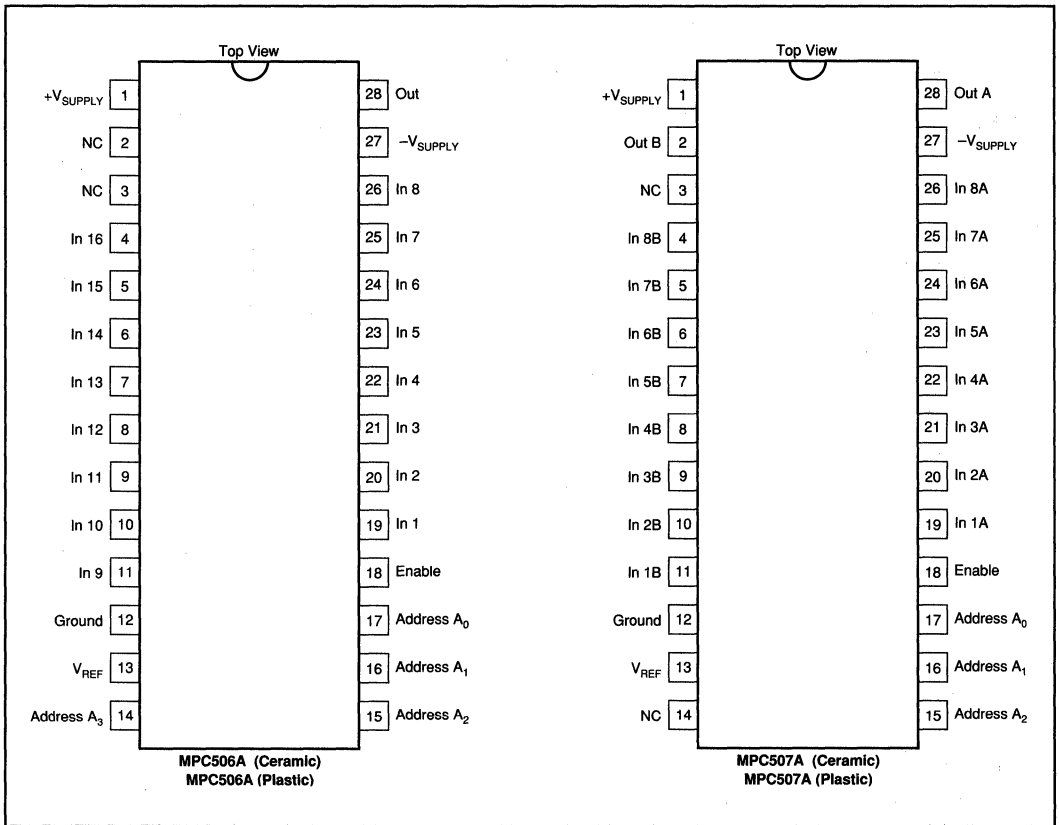
TRUTH TABLES

MPC506A

A$_3$	A$_2$	A$_1$	A$_0$	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

MPC507A

A$_2$	A$_1$	A$_0$	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC506AP	28-Pin Plastic	905
MPC506AG	28-Pin Ceramic	904
MPC506AU	28-Pin Plastic SOIC	217-1
MPC507AP	28-Pin Plastic	905
MPC507AG	28-Pin Ceramic	904
MPC507AU	28-Pin Plastic SOIC	217-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS(1)

Voltage between supply pins 44V
V_{REF} to ground, V+ to ground 22V
V– to ground 25V
Digital input overvoltage:
V_{EN}, V_A: V_{SUPPLY} (+) .... +4V
V_{SUPPLY} (–) .... –4V
or 20mA, whichever occurs first.
Analog input overvoltage:
V_S: V_{SUPPLY} (+) .... +20V
V_{SUPPLY} (–) .... –20V
Continuous current, S or D 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation* 2.0W
Operating temperature range .... –40°C to +85°C
Storage temperature range .... –65°C to +150°C

*Derate 20.0mW/°C above T_A = 70

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	DESCRIPTION
MPC506AP	28-Pin Plastic DIP	–40°C to +85°C	16-Channel Single-Ended
MPC506AG	28-Pin Ceramic DIP	–40°C to +85°C	16-Channel Single-Ended
MPC506AU	28-Pin Plastic SOIC	–40°C to +85°C	16-Channel Single-Ended
MPC507AP	28-Pin Plastic DIP	–40°C to +85°C	8-Channel Differential
MPC507AG	28-Pin Ceramic	–40°C to +85°C	8-Channel Differential
MPC507AU	28-Pin Plastic SOIC	–40°C to +85°C	8-Channel Differential

TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

SETTLING TIME vs
SOURCE RESISTANCE FOR 20V STEP CHANGE

CROSSTALK vs SIGNAL FREQUENCY

COMBINED CMR vs
FREQUENCY MPC507A AND INA110

MPC506/507

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MULTIPLEXERS

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DISCUSSION OF SPECIFICATIONS

DC CHARACTERISTICS

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedance of $10^8 \Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.

- *Use sources with impedances as low as possible.* A 1000Ω source resistance will present less than 0.001% loading error and $10k\Omega$ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1).

FIGURE 1. MPC506A Static Accuracy Equivalent Circuit.

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20µV if a 1kΩ source is used. In general, for the MPC506A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications.

FIGURE 2. MPC507A Static Accuracy Equivalent Circuit.

Load (Output Device) Characteristics

- *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.

- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.

- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.

- Keep source impedances as low as possible to minimize resistive loading errors.

- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC507A is used for multiplexing high-level signals of 1V to 10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\,(dV/dt)$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can

FIGURE 3. Settling Time Effects—MPC506A.

see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The trade-off for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\,dt$$

where $i = C\,(dV/dt)$ of the CMOS FET switches

$\quad C$ = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.
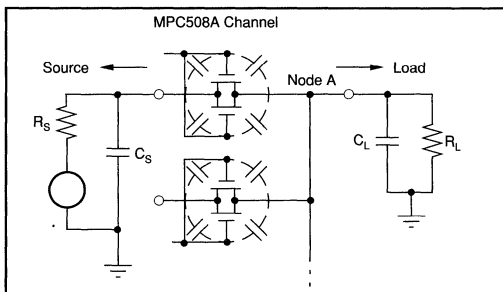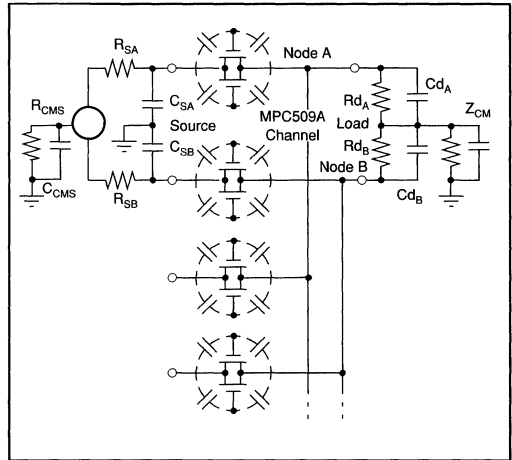

FIGURE 4. Settling and Common-Mode Effects— MPC507A

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the seven (MPC507A) or 15 (MPC506A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1000Hz sine wave applied to all off channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

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MULTIPLEXERS

Common-Mode Rejection (MPC507A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC507A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC507A and Burr-Brown's INA110 instrumentation amplifier (G = 100) is 110dB at DC to 10Hz with a 6dB/octave roll-off to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown INA110 instrumentation amplifier connected for gains of 500, 100, and 10.

Factors which will degrade multiplexer and system DC CMR are:

• Amplifier bias current and differential impedance mismatch
• Load impedance mismatch
• Multiplexer impedance and leakage current mismatch
• Load and source common-mode impedance

AC CMR roll-off is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.
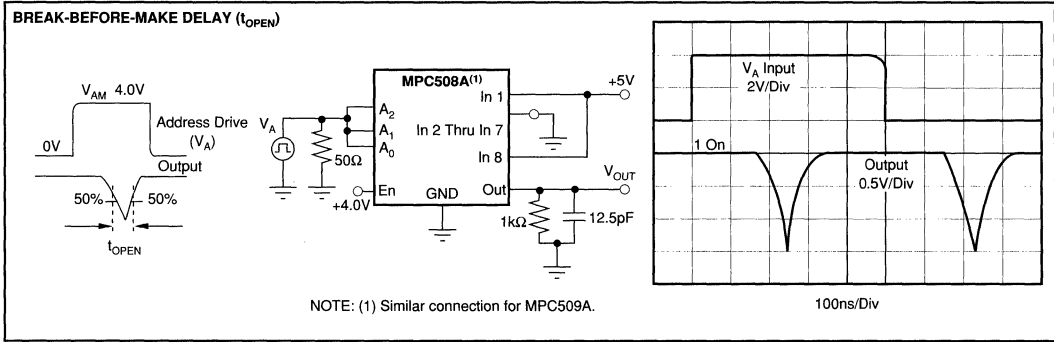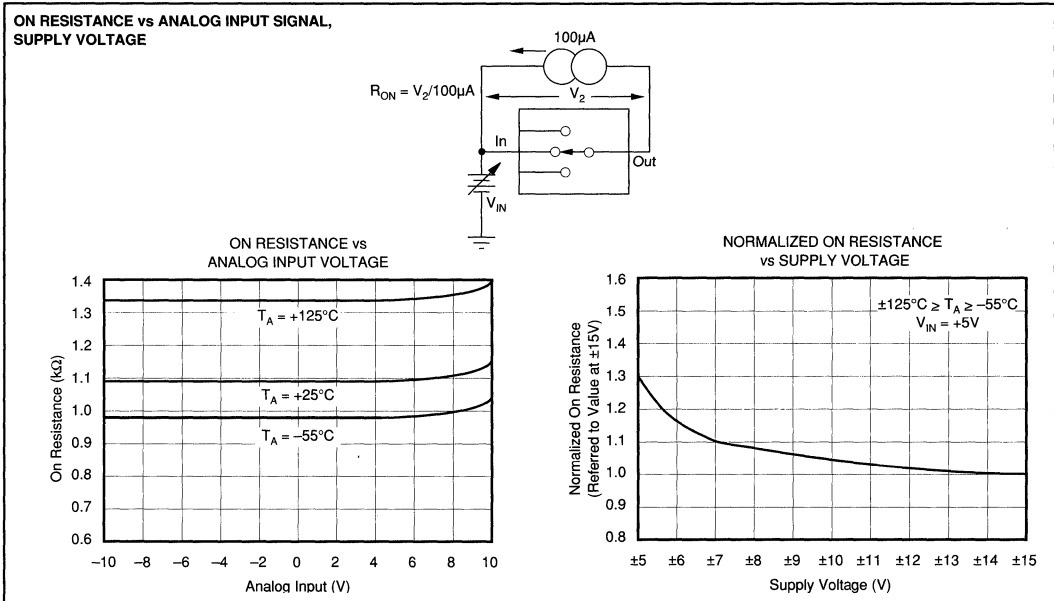
SWITCHING WAVEFORMS

Typical at +25°C, unless otherwise noted.

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

NOTE: (1) Similar connection for MPC507A.
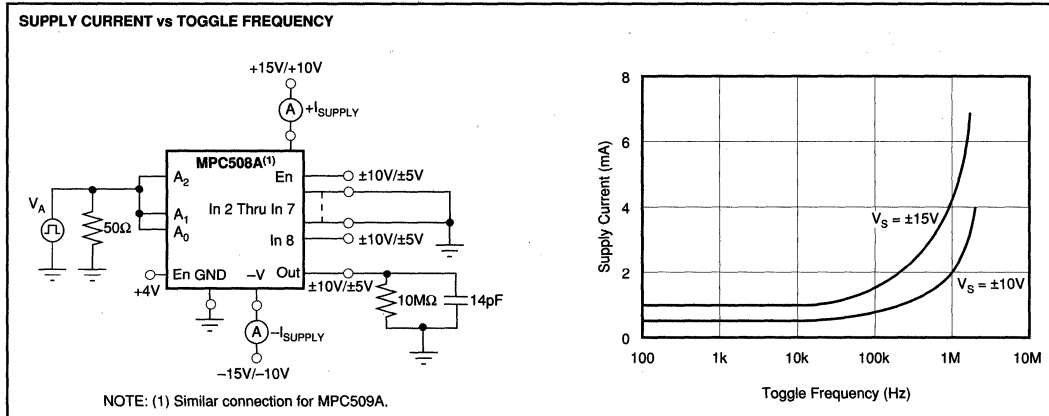

ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))

NOTE: (1) Similar connection for MPC507A.
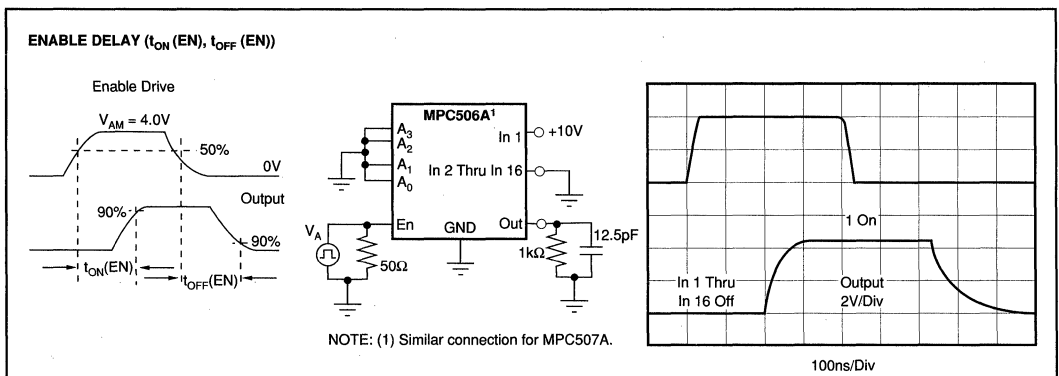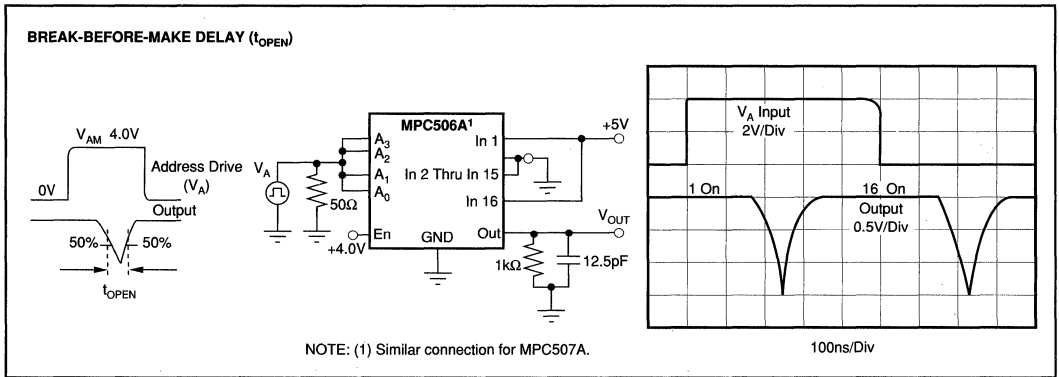
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

$T_A = +25°C$, $V_S = ±15V$, $V_{AM} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = $ Open, unless otherwise noted.

ON RESISTANCE vs INPUT SIGNAL, SUPPLY VOLTAGE
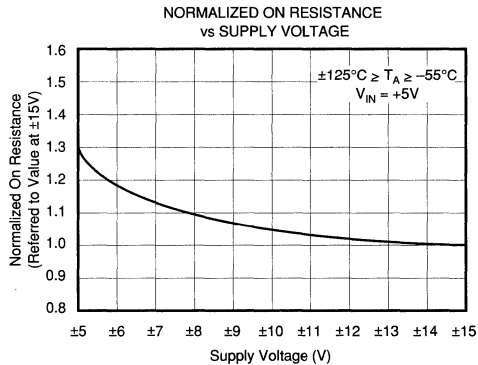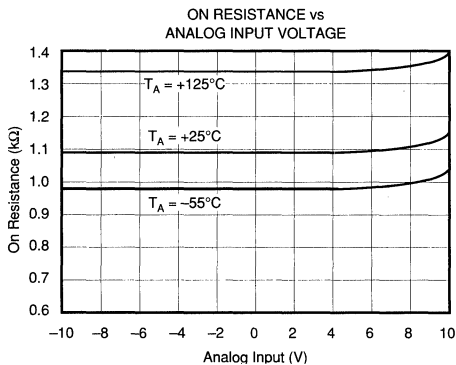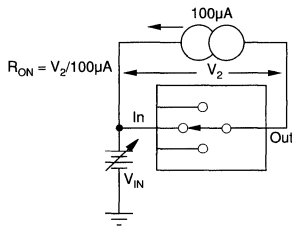
$R_{ON} = V_2/100\mu A$

ON RESISTANCE vs
ANALOG INPUT VOLTAGE

NORMALIZED ON RESISTANCE
vs SUPPLY VOLTAGE

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

MPC506/507

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MULTIPLEXERS

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

LEAKAGE CURRENT vs TEMPERATURE

NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V.
(Two measurements per device for I_D (Off): +10V/–10V and –10V/+10V).

ON-CHANNEL CURRENT vs VOLTAGE
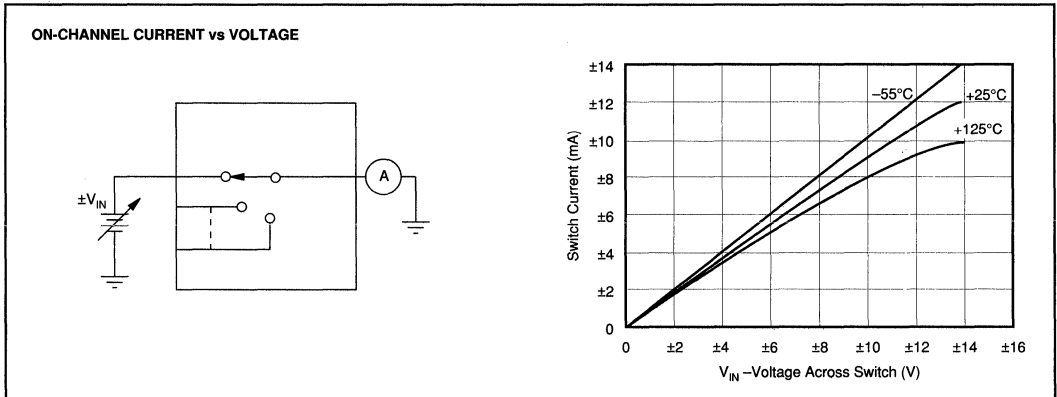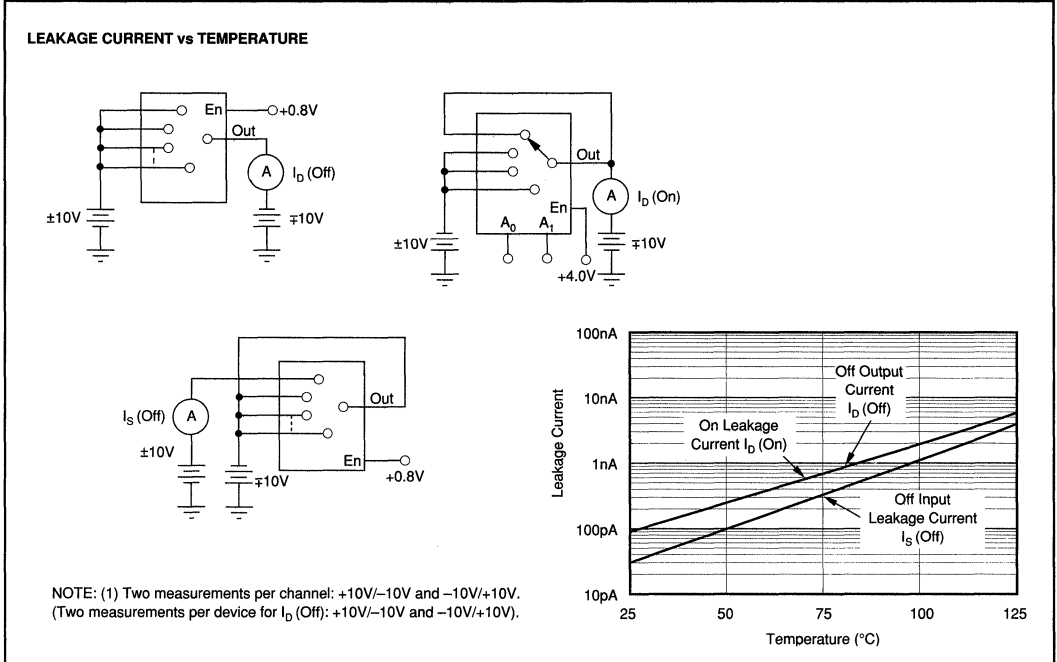
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

$T_A = +25°C$, $V_S = ±15V$, $V_{AM} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = $ Open, unless otherwise noted.

SUPPLY CURRENT vs TOGGLE FREQUENCY

NOTE: (1) Similar connection for MPC507A.

ACCESS TIME vs LOGIC LEVEL (High)

$V_{REF} = $ Open for logic high levels $\leq 6V$
$V_{REF} = $ Logic high for logic high levels $> 6V$[1]

NOTE: (1) Similar connection for MPC507A.

ACCESS TIME WAVEFORM

MPC506/507

MULTIPLEXERS

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INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 3-bit (MPC507A or 4-bit MPC506A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15V and/or −15V supply voltage is absent or shorted to ground, the MPC507A and MPC506A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull up resistors are recommended (see Typical Performance Curves, Access Time).

To preserve common-mode rejection of the MPC507A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.
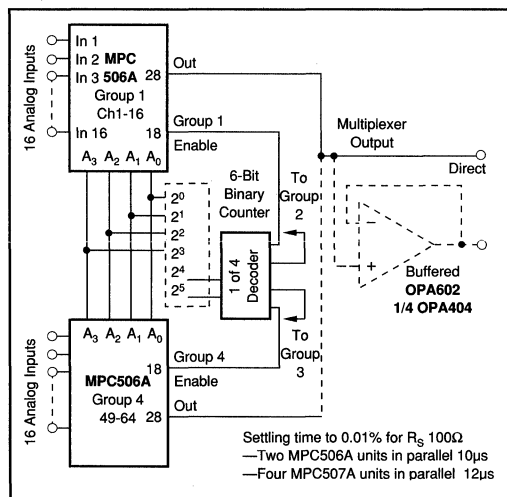
FIGURE 5. 64-Channel, Single-Tier Expansion.

CHANNEL EXPANSION

Single-Ended Multiplexer (MPC506A)

Up to 64 channels (four multiplexers) can be connected to a single node, or up to 256 channels using 17 MPC506A multiplexers on a two-tiered structure as shown in Figures 5 and 6.
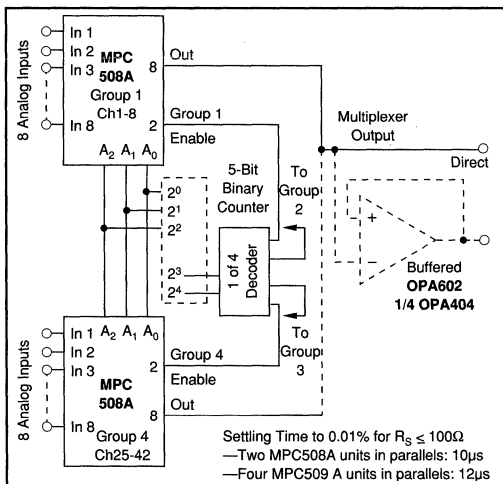
Differential Multiplexer (MPC507A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 X 1 or an 8X8 configuration.

Single-Node Expansion

The 64x1 configuration is simply eight (MPC507A) units tied to a single node. Programming is accomplished with a 6-bit counter, using the 3LSBs of the counter to control Channel Address inputs A_0, A_1, A_2 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC507A multiplexers.

Two-Tier Expansion

Using an 8x8 two-tier structure for expansion to 64 channels, the programming is simplified. The 6-bit counter output does not require a 1-of-8 decoder. The 3LSBs of the counter drive the A_0, A_1 and A_2 inputs of the eight first-tier multiplexers and the 3MSBs of the counter are applied to the A_0, A_1, and A_2 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multitiered configuration.

FIGURE 6. Channel Expansion up to 256 Channels Using 16x16 Two-Tiered Expansion

BURR - BROWN®
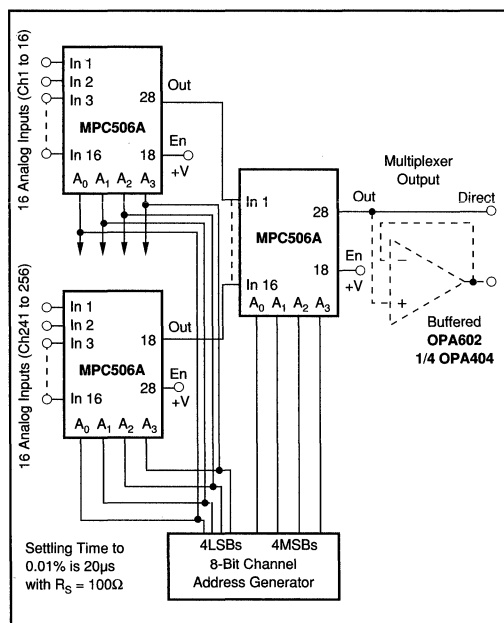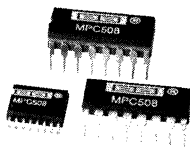
MPC508A

MPC509A

Single-Ended 8-Channel/Differential 4-Channel CMOS ANALOG MULTIPLEXERS

MPC508/509

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MULTIPLEXERS

FEATURES

● **ANALOG OVERVOLTAGE PROTECTION: 70Vp-p**
● **NO CHANNEL INTERACTION DURING OVERVOLTAGE**
● **BREAK-BEFORE-MAKE SWITCHING**
● **ANALOG SIGNAL RANGE: ±15V**
● **STANDBY POWER: 7.5mW typ**
● **TRUE SECOND SOURCE**

DESCRIPTION

The MPC508A is an 8-channel single-ended analog multiplexer and the MPC509A is a 4-channel differential multiplexer.

The MPC508A and MPC509A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

These features make the MPC508A and MPC509A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC508A and MPC509A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic or plastic DIP and plastic SOIC packages. Temperature range is –40°C to +85°C.

FUNCTIONAL DIAGRAMS

MPC508A

MPC509A

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

Supplies = +15V, −15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V, unless otherwise specified.

PARAMETER	TEMP	MPC508A/509A			UNITS
		MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS					
V_S, Analog Signal Range	Full	−15		+15	V
R_{ON}, On Resistance[1]	+25°C		1.3	1.5	kΩ
	Full		1.5	1.8	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.5		nA
	Full			10	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.2		nA
MPC508A	Full			5	nA
MPC509A	Full			5	nA
I_D (OFF) with Input Overvoltage Applied[2]	+25°C		4.0		nA
	Full				µA
I_D (ON), On Channel Leakage Current	+25°C		2		nA
MPC508A	Full			10	nA
MPC509A	Full			10	nA
I_{DIFF} Differential Off Output Leakage Current					
(MPC509A Only)	Full			10	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold Drive	Full			0.8	V
V_{AH}, Input High Threshold[3]	Full	4.0			V
I_A, Input Leakage Current (High or Low)[4]	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.5		µs
	Full			0.6	µs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		200		ns
	Full			500	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		250		ns
	Full			500	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.01%)	+25°C		3.5		µs
"OFF Isolation"[5]	+25°C	50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5		pF
C_D (OFF), Channel Output Capacitance: MPC508A	+25°C		25		pF
MPC509A	+25°C		12		pF
C_A, Digital Input Capacitance	25°C		5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
I+, Current Pin 1[6]	Full		0.7	1.5	mA
I−, Current Pin 27[6]	Full		5	20	µA

NOTES: (1) $V_{OUT} = \pm10V$, $I_{OUT} = -100\mu A$. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (5) $V_{EN} = 0.8V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 7Vrms$, f = 100kHz. Worst-case isolation occurs on channel 4 due to proximity of the output pins. (6) V_{EN}, $V_A = 0V$ or 4.0V.

PIN CONFIGURATIONS

Top View — MPC508A (Ceramic) / MPC508A (Plastic)

Pin	Signal		Pin	Signal
1	A_0		16	A_1
2	En		15	A_2
3	$-V_{SUPPLY}$		14	Ground
4	In 1		13	$+V_{SUPPLY}$
5	In 2		12	In 5
6	In 3		11	In 6
7	In 4		10	In 7
8	Out		9	In 8

Top View — MPC509A (Ceramic) / MPC509 A (Plastic)

Pin	Signal		Pin	Signal
1	A_0		16	A_1
2	En		15	Ground
3	$-V_{SUPPLY}$		14	$+V_{SUPPLY}$
4	In 1A		13	In 1B
5	In 2A		12	In 2B
6	In 3A		11	In 3B
7	In 4A		10	In 4B
8	Out A		9	Out B

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MULTIPLEXERS

TRUTH TABLES

MPC508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

MPC509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

ABSOLUTE MAXIMUM RATINGS[1]

Voltage between supply pins	44V
V+ to ground	22V
V– to ground	25V

Digital input overvoltage V_{EN}, V_A:
- V_{SUPPLY} (+) .... +4V
- V_{SUPPLY} (–) .... –4V
- or 20mA, whichever occurs first.

Analog input overvoltage V_S:
- V_{SUPPLY} (+) .... +20V
- V_{SUPPLY} (–) .... –20V

Continuous current, S or D	20mA
Peak current, S or D (pulsed at 1ms, 10% duty cycle max)	40mA
Power dissipation[2]	1.28W
Operating temperature range	–40°C to +85°C
Storage temperature range	–65°C to +150°C

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Derate 1.28mW/°C above T_A = +70°C.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	DESCRIPTION
MPC508AP	16-Pin Plastic DIP	–40°C to +85°C	8-Channel Single-Ended
MPC508AU	16-Pin Plastic SOIC	–40°C to +85°C	8-Channel Single-Ended
MPC508AG	16-Pin Ceramic DIP	–40°C to +85°C	8-Channel Single-Ended
MPC509AP	16-Pin Plastic DIP	–40°C to +85°C	4-Channel Differential
MPC509AU	16-Pin Plastic SOIC	–40°C to +85°C	4-Channel Differential
MPC509AG	16-Pin Ceramic	–40°C to +85°C	4-Channel Differential

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC508/509AP	16-Pin Plastic DIP	180
MPC508/509AU	16-Pin Plastic SOIC	211
MPC508/509AG	16-Pin Ceramic	129

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DISCUSSION OF PERFORMANCE

DC CHARACTERISTICS

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error;
Multiplexer ON resistance error;
and, DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

* *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$, or greater, will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.

* *Use sources with impedances as low as possible.* 1000Ω source resistance will present less than 0.001% loading error and $10k\Omega$ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1).

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
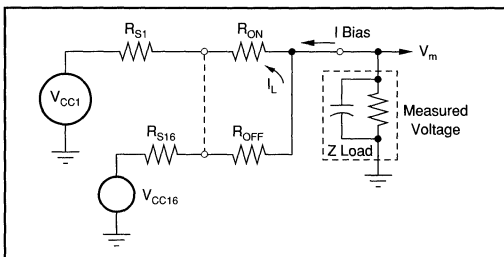R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20μV if a 1kΩ source is used. In general, for the MPC508A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications. Refer to Figure 2.
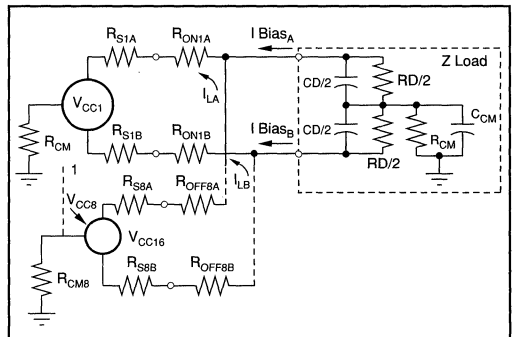
Load (Output Device) Characteristics

* *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.

* The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.

* Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.
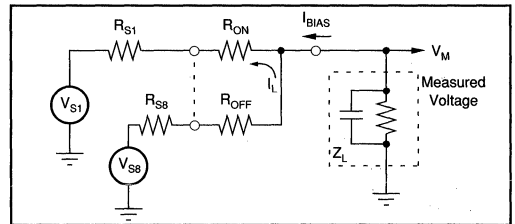
FIGURE 1. MPC508A DC Accuracy Equivalent Circuit.
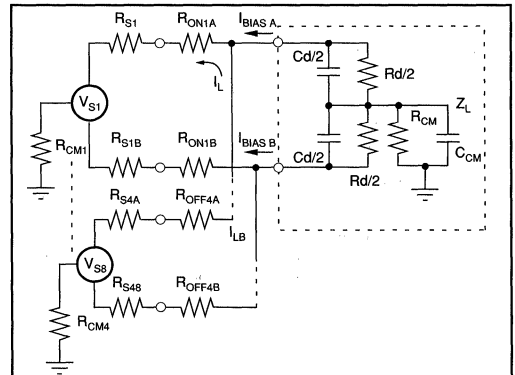
FIGURE 2. MPC509A DC Accuracy Equivalent Circuit.

Source Characteristics

- *The source impedance unbalance* will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- *Keep source impedances as low as possible* to minimize resistive loading errors.
- *Minimize ground loops.* If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC509A is used for multiplexing high-level signals of ±1V to ±10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation i = C (dV/dt), the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients, seen at the source and load, decrease proportionally as the capacitance of the load and source increase. The trade-off for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C) \, dt$$

where i = C (dV/dt) of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

FIGURE 3. Settling Time Effects—MPC508A

FIGURE 4. Settling and Common-Mode-Effects—MPC509A

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the three (MPC509A) or seven (MPC508A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_s impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1kHz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (MPC509A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC509A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC509A and Burr-Brown's INA110 instrumentation amplifier is 110dB at DC to 10Hz (G = 100) with a 6dB/octave roll off to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model INA110 instrumentation amplifier connected for gains of 10, 100, and 500.

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MULTIPLEXERS

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR roll off is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer-to-amplifier wiring must be minimized. Use twisted-shielded-pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.
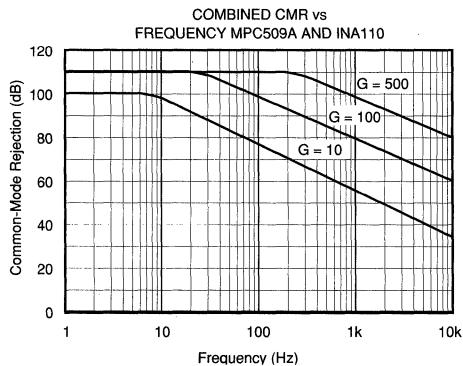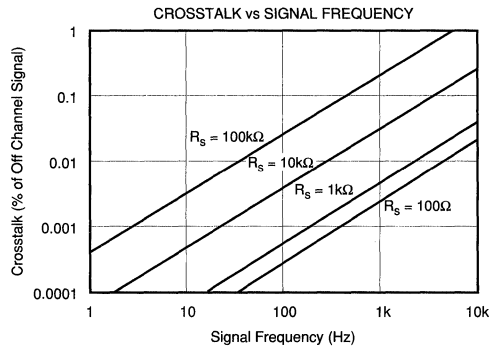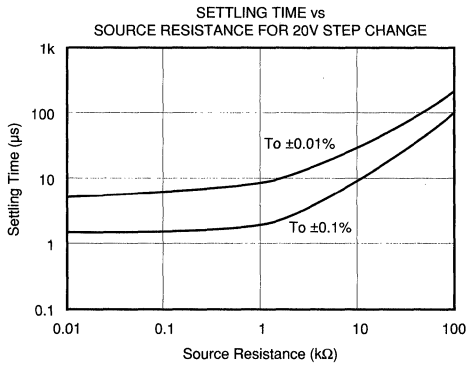
SETTLING TIME vs
SOURCE RESISTANCE FOR 20V STEP CHANGE

CROSSTALK vs SIGNAL FREQUENCY

COMBINED CMR vs
FREQUENCY MPC509A AND INA110

SWITCHING WAVEFORMS

TYPICAL AT +25°C UNLESS OTHERWISE NOTED.

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

NOTE: (1) Similar connection for MPC509A.

V_A Input
2V/Div

1 On

Output
0.5V/Div

100ns/Div

ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))

NOTE: (1) Similar connection for MPC509A.

Enable Drive
2V/Div

Output
2V/Div

100ns/Div
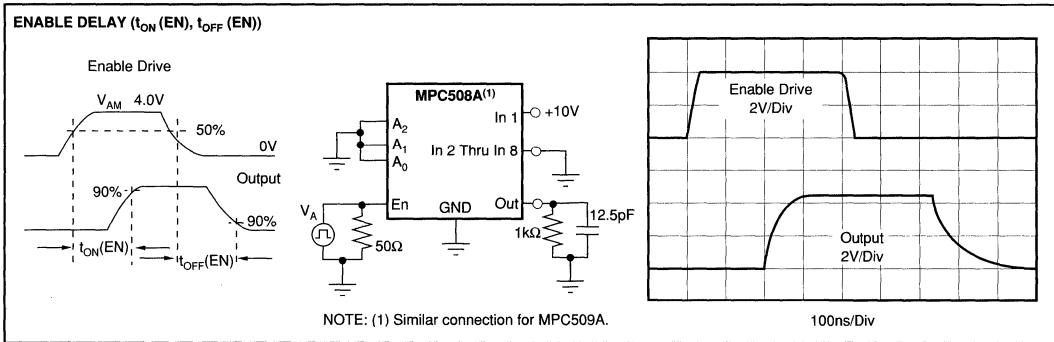
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless otherwise specified: T_A = +25, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V.

ON RESISTANCE vs ANALOG INPUT SIGNAL, SUPPLY VOLTAGE

$100\mu A$

$R_{ON} = V_2/100\mu A$

V_2

In   Out

V_{IN}

ON RESISTANCE vs
ANALOG INPUT VOLTAGE

T_A = +125°C

T_A = +25°C

T_A = –55°C

On Resistance (kΩ)

Analog Input (V)

NORMALIZED ON RESISTANCE
vs SUPPLY VOLTAGE

±125°C ≥ T_A ≥ –55°C
V_{IN} = +5V

Normalized On Resistance
(Referred to Value at ±15V)

Supply Voltage (V)

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PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

SUPPLY CURRENT vs TOGGLE FREQUENCY

NOTE: (1) Similar connection for MPC509A.

LEAKAGE CURRENT vs TEMPERATURE

NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V.
(Two measurements per device for I_D (Off): +10V/–10V and –10V/+10V).

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

ACCESS TIME vs LOGIC LEVEL (High)
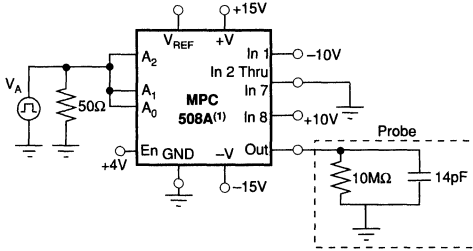
NOTE: (1) Similar connection for MPC509A.
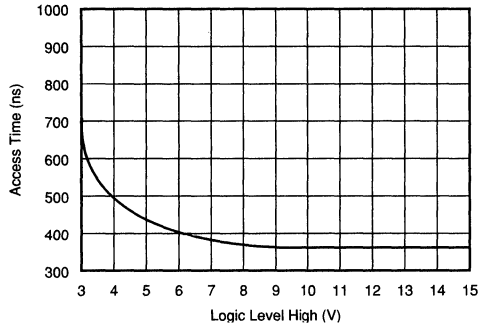
ACCESS TIME WAVEFORM
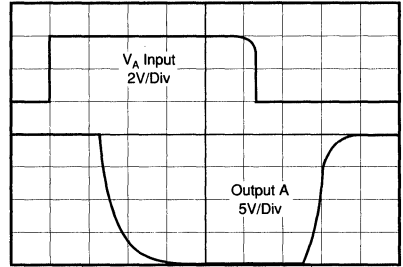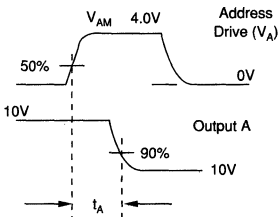
200ns/Div

ON-CHANNEL CURRENT vs VOLTAGE

MPC508/509

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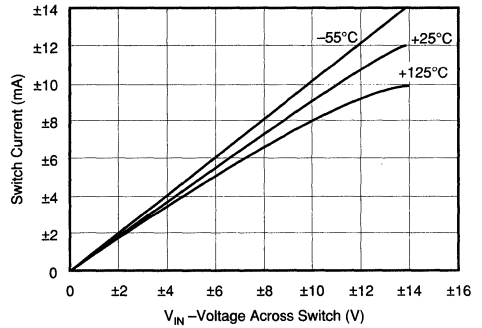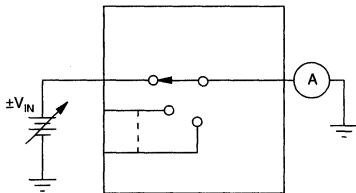
MULTIPLEXERS

INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 2-bit (MPC509A) or 3-bit (MPC508A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to $+V_{SUPPLY}$.

If the +15V and/or –15V supply voltage is absent or shorted to ground, the MPC509A and MPC508A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended

To preserve common-mode rejection of the MPC509A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

Single-Ended Multiplexer (MPC508A)

Up to 32 channels (four multiplexers) can be connected to a single node, or up to 64 channels using nine MPC508A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

FIGURE 5. 32-Channel, Single-Tier Expansion.
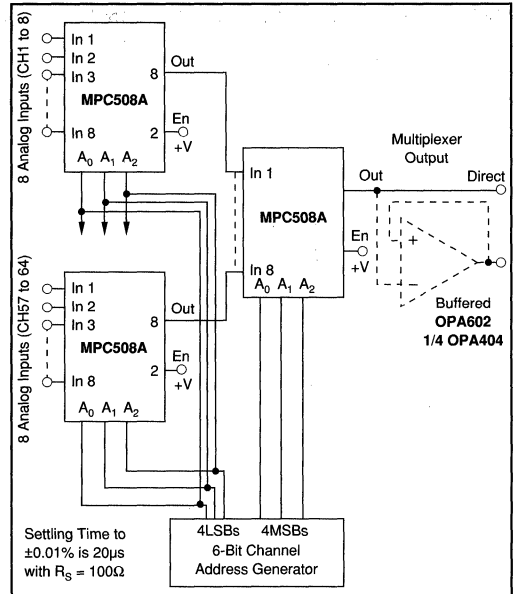
FIGURE 6. Channel Expansion Up to 64 Channels Using 8 x 8 Two-Tiered Expansion.

Differential Multiplexer (MPC509A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

Single-Node Expansion

The 32 x 1 configuration is simply eight (MPC509A) units tied to a single node. Programming is accomplished with a 5-bit counter, using the 2LSBs of the counter to control Channel Address inputs A_0 and A_1 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC509A multiplexers.

Two-Tier Expansion

Using a 4 x 4 two-tier structure for expansion to 16 channels, the programming is simplified. A 4-bit counter output does not require a 1-of-8 decoder. The 2LSBs of the counter drive the A_0 and A_1 inputs of the four first-tier multiplexers and the 2MSBs of the counter are applied to the A_0 and A_1 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.
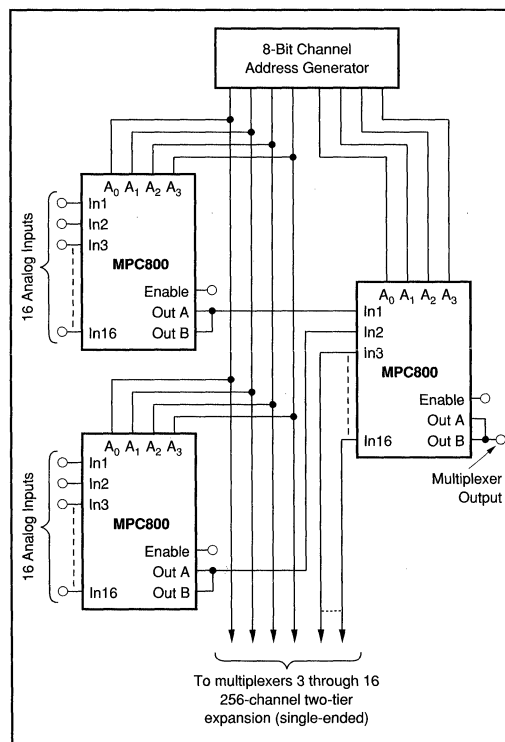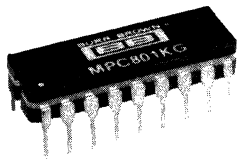
BURR - BROWN®
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MPC800

High Speed
CMOS ANALOG MULTIPLEXER

FEATURES

- **HIGH SPEED**
  100ns Access Time
  800ns Settling to 0.01%
  250ns Settling to 0.1%
- **USER-PROGRAMMABLE**
  16-Channel Single-Ended or
  8-Channel Differential

- **SELECTABLE TTL OR CMOS**
  COMPATIBILITY
- **WILL NOT SHORT SIGNAL SOURCES —**
  Break-Before-Make Switching
- **SELF-CONTAINED WITH INTERNAL**
  CHANNEL ADDRESS DECODER
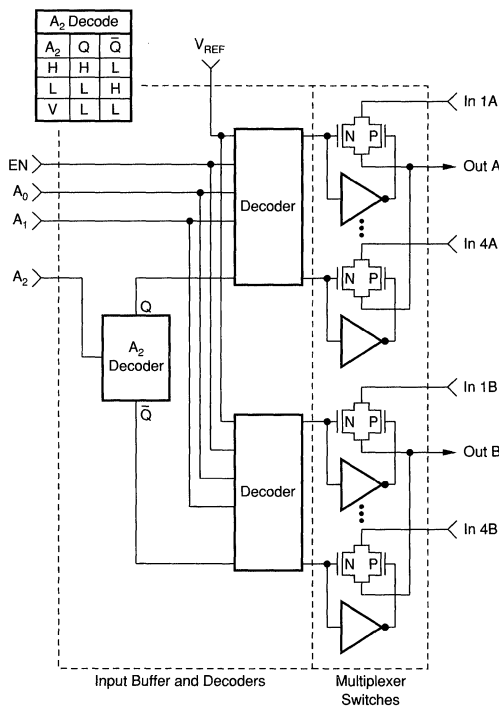- **28-PIN HERMETIC DUAL-IN-LINE**
  PACKAGE
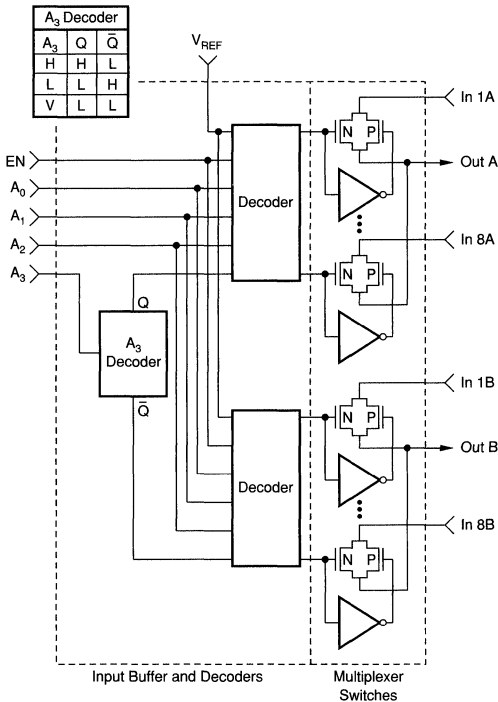
DESCRIPTION

The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C and the MPC800SG for operation from –55°C to +125°C.

A_3 Decoder		
A_3	Q	$\bar{Q}$
H	H	L
L	L	H
V	L	L

Input Buffer and Decoders   Multiplexer
                             Switches

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MPC800

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MULTIPLEXERS

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±V_{CC} = 15V, unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
		MPC800KG, MPC800SG		
ANALOG INPUTS				
Voltage Range	–15		+15	V
Maximum Overvoltage	–V_{CC} –2		+V_{CC} +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range[1]	6		10	V
ON Characteristics[2]				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature		See Typical Performance Curves		
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.04		nA
Over Temperature Range		0.6	100	nA
ON Channel Leakage Drift		See Typical Performance Curves		
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.01		nA
Over Temperature Range		0.38	50	nA
OFF Channel Input Leakage Drift		See Typical Performance Curves		
OFF Channel Output Leakage		0.035		nA
Over Temperature Range		0.48	100	nA
OFF Channel Output Leakage Drift		See Typical Performance Curves		
Output Leakage (All channels disabled)[3]		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
–16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL[4]				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	25	μA
TTL Input Overvoltage	–6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7V_{REF}			V
CMOS Input Overvoltage	–2		+V_{CC} +2	V
Address A_3 Overvoltage	–V_{CC} –2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select[5]				
Single-Ended		4-bit Binary Code One of 16		
Differential		3-bit Binary Code One of 8		
Enable		Logic "0" Inhibits All Channels		
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between				
Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation[6]			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, –39		mA
At 100kHz Switching Speed		+25, –29		mA

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = +25°C$ and $\pm V_{CC} = 15V$, unless otherwise noted.

PARAMETER	MPC800KG, MPC800SG			UNITS
	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk[7]		See Typical Performance Curves		
T_{OPEN} (Break-before-make delay)		20		ns
Access Time at +25°C		100	150	ns
Over Temperature Range		120	200	ns
Settling Time[8]				
to 0.1% (20mV)		250		ns
to 0.01% (2mV)		800		ns
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S		2.5		pF
OFF Channel Output Capacitance, C_O		18		pF
OFF Input to Output Capacitance, C_{DS}		0.02		pF
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	−65		+150	°C
MPC800SG				
Specification	−55		+125	°C
Storage	−65		+150	°C

NOTES: (1) Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility. (2) $V_{IN} = \pm 10V$, I_{OUT} = 100µA. (3) Single-ended mode. (4) Logic levels specified for V_{REF} (pin 13) open. (5) For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line. For differential operation connect A_3 to $-V_{CC}$. (6) Derate 8mW/°C above $T_A = +75°C$. (7) 10Vp-p sine wave on all unused channels. See Typical Performan Curves. (8) For 20V step input to ON channel, into 1kΩ load.

PIN CONFIGURATION

Top View

+V_{CC}	1	28	Out A
Out B	2	27	−V_{CC}
NC	3	26	IN8/8A
IN16/8B	4	25	IN7/7A
IN15/7B	5	24	IN6/6A
IN14/6B	6	23	IN5/5A
IN13/5B	7	22	IN4/4A
IN12/4B	8	21	IN3/3A
IN11/3B	9	20	IN2/2A
IN10/2B	10	19	IN1/1A
IN9/1B	11	18	ENABLE
GND	12	17	A_0
V_{REF}	13	16	A_1
A_3	14	15	A_2
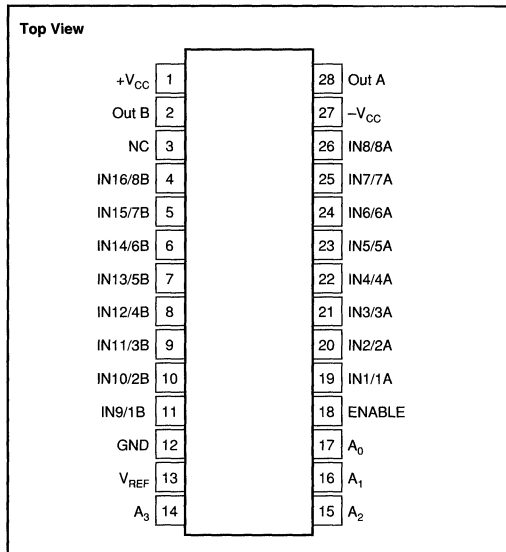
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPC800KG	Single-Wide Cerdip	−0°C to +75°C
MPC800SG	Single-Wide Cerdip	−55°C to +125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC800KG	28-Pin Single-Wide Cerdip	228
MPC800SG	28-Pin Single-Wide Cerdip	228

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

MPC800

5

MULTIPLEXERS

TYPICAL PERFORMANCE CURVES

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

CROSS TALK vs SIGNAL FREQUENCY

LEAKAGE CURRENTS vs TEMPERATURE

COMBINED CMR vs FREQUENCY
FOR MODEL 3630 AND MPC800

R_{ON} DRIFT vs TEMPERATURE

SETTLING TIME vs SOURCE RESISTANCE
(10V Step Change, R_L = 1kΩ)

DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and
  multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

• *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedance of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.

• *Use sources with impedances as low as possible.* A 1000Ω source resistance will present less than 0.002% loading error and $10k\Omega$ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\in (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where, $R_S = R_{SOURCE}$
  R_L = Load resistance
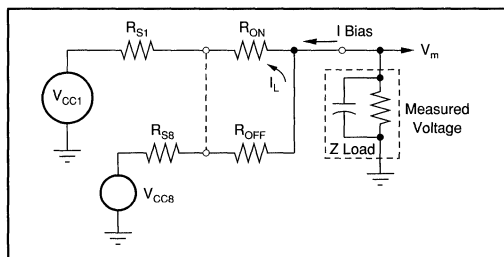 R_{OS} = Multiplexer ON resistance

FIGURE 1. MPC800 Static Accuracy Equavalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of $19\mu V$ if a 1000Ω source is used, and $118\mu V$ if a $10k\Omega$ source is used. In general, for the MPC800 the offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{SOURCE})$$

where:

I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.
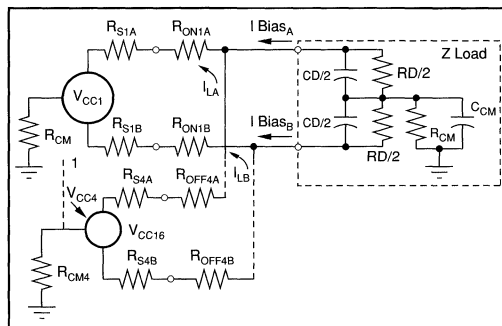

FIGURE 2. MPC800 Static Accuracy Equavalent Circuit (Differential Operation).

Load (Output Device) Characteristics

• *Use devices with very low bias current.* Generally FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine input offset.

• *The system DC common-mode rejection* (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.

• *Load impedances, differential and common-mode* should be $10^{10}\Omega$ or higher.

Source Characteristics

• *The source impedance unbalance* will produce offset, common-mode, and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.

• *Keep source impedances as low as possible* to minimize resistive loading errors.

• *Minimize ground loops.* If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC800 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should be taken, but the parameters are not as critical as for low level signal applications.
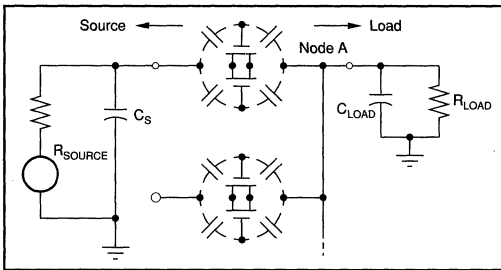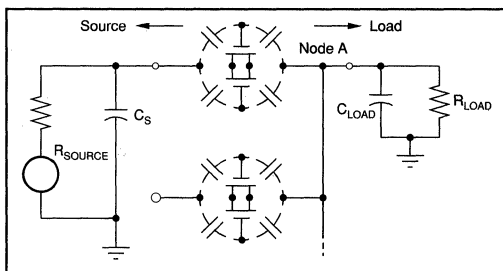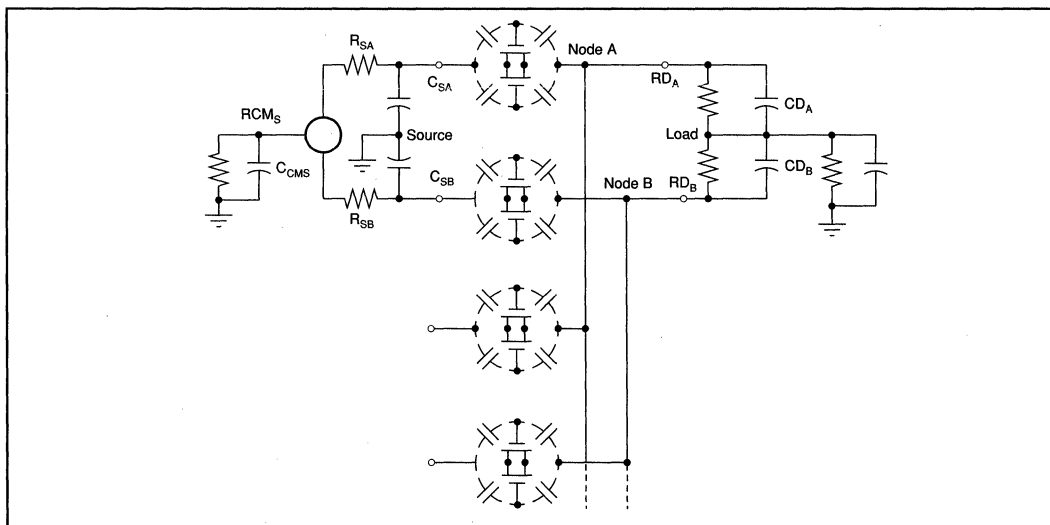

FIGURE 3. Settling Time Effect (Single-ended).
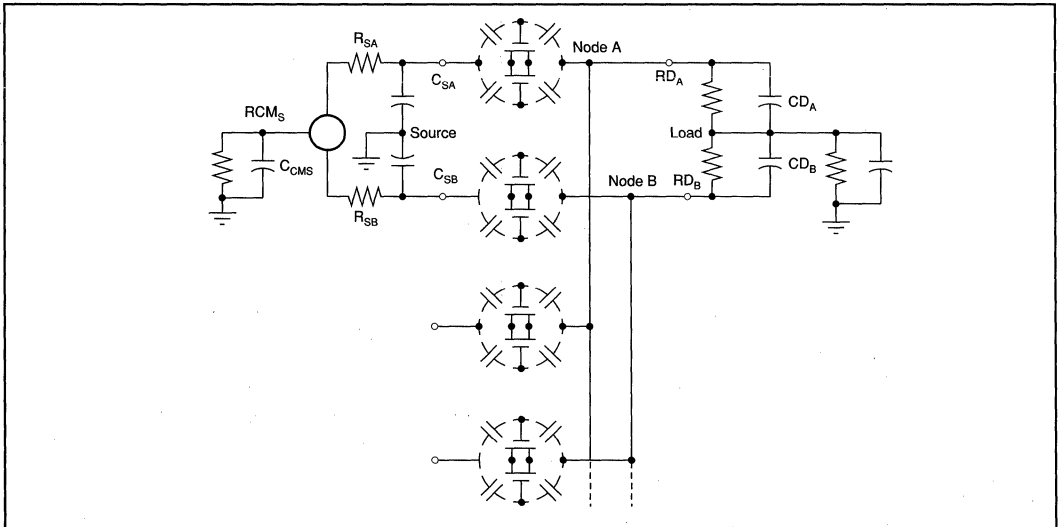
SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC800 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RCs. For the MPC800, the internal capacitance is approximately 20pF differential or 40pF single-ended. With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40ns. This means the source resistance should be kept to less than 2kΩ (assume high load resistance) to maintain fast settling times.

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 differential or 15 signal-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{SOURCE} impedance of the ON channel. Crosstalk is measured with a

FIGURE 4. Settling and Common-Mode Effects (Differential).

20Vp-p, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION
(Differential Mode Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC800 and Burr-Brown's model 3630 instrumentation amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a signal of 1000 and with source unbalance of 10kΩ. 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC800 use twisted-shielded pair wire for signal lines and inter-tier

connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 13) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC800 as a 16-channel single-ended multiplexer, output A (pin 28) is connected to output B (pin 2) to form a single output, then all four address lines (A_0, A_1, A_2 and A_3) are used to address the correct channel.

The MPC800 can also be used as a dual 8-channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC800 as an 8-channel differential multiplexer, connect address line A_3 to $-V_{CC}$, then use the remaining three address lines (A_0, A_1 and A_2) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC800 used as 16-channel single-ended multiplexer or 8-channel dual multiplexer.

	USE A_3 AS DIGITAL ADDRESS INPUT				"ON" CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

For 16-channel single-ended function, tie "out A" to "out B", for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

MPC800

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MULTIPLEXERS

MPC800 used as 8-channel differential multiplexer.

A₃ CONNECT TO −V_cc				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

CHANNEL EXPANSION

Single-Tier Expansion

Up to four MPC800s can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC800s can be connected to two nodes to form a 64-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1-of-4 decoder for 64-channel single-ended expansion (see Figure 5), and an 8-bit address and a 1-of-8 decoder for 64-channel differential expansion. The decoder drives the enable inputs of the MPC800, turning on only one multiplexer at a time.

Two-Tier Expansion

Up to seventeen MPC800s can be connected in a two-tier structure to form a 256-channel single-ended multiplexer (see Figure 6) or up to nine MPC800s can be connected in a two-tier structure to form a 64-channel differential multiplexer. Programming is accomplished with an 8-bit address.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (8 or 16) in the multitiered configuration.
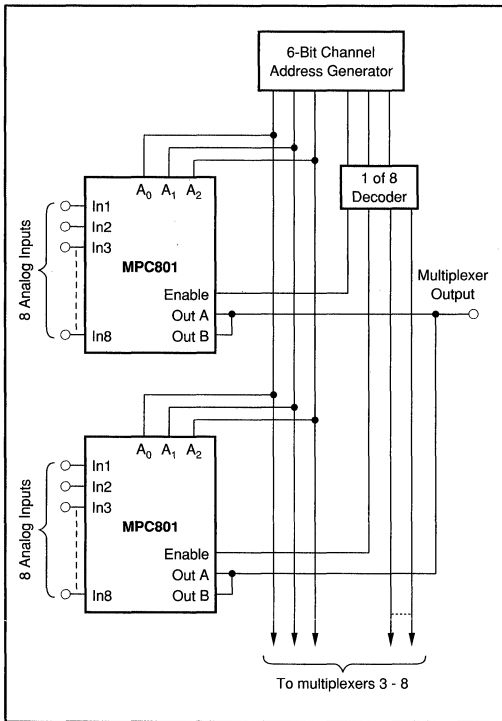

FIGURE 5. 32- to 64-Channel, Single-tier Expansion.

FIGURE 6. Channel Expansion up to 256 Channels Using 16 X 16 Two-tiered Expansion.

BURR - BROWN®

MPC801

High Speed
CMOS ANALOG MULTIPLEXER

FEATURES

● **HIGH SPEED**
  80ns Access Time
  800ns Settling to 0.01%
  250ns Settling to 0.1%
● **USER-PROGRAMMABLE**
  8-Channel Single-Ended or
  4-Channel Differential

● **SELECTABLE TTL OR CMOS**
  COMPATIBILITY
● **WILL NOT SHORT SIGNAL SOURCES —**
  Break-Before-Make Switching
● **SELF-CONTAINED WITH INTERNAL**
  CHANNEL ADDRESS DECODER
● **18-PIN HERMETIC DUAL-IN-LINE**
  PACKAGE

DESCRIPTION

The MPC801 is a high speed multiplexer that is user-programmable for 8-channel single-ended operation or 4-channel differential operation and for TTL or CMOS compatibility.

The MPC801 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC801KG for operation from 0°C to +75°C and the MPC801SG for operation from –55°C to +125°C.

A_2 Decode		
A_2	Q	$\bar{Q}$
H	H	L
L	L	H
V	L	L

Input Buffer and Decoders   Multiplexer Switches

MPC801

5

MULTIPLEXERS

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±V_{CC} = 15V, unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
		MPC801KG, MPC801SG		
ANALOG INPUTS				
Voltage Range	−15		+15	V
Maximum Overvoltage	−V_{CC} −2		+V_{CC} +2	V
Number of Input Channels				
Differential	4			
Single-Ended	8			
Reference Voltage Range[1]	6		10	V
ON Characteristics[2]				
ON Resistance (R_{ON}) at +25°C		500	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature		See Typical Performance Curves		
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.1		nA
Over Temperature Range		0.3	50	nA
ON Channel Leakage Drift		See Typical Performance Curves		
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.05		nA
Over Temperature Range		0.6	50	nA
OFF Channel Input Leakage Drift		See Typical Performance Curves		
OFF Channel Output Leakage		0.1		nA
Over Temperature Range		0.30	50	nA
OFF Channel Output Leakage Drift		See Typical Performance Curves		
Output Leakage				
(All channels disabled)[3]		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
−16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL[4]				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	20	μA
TTL Input Overvoltage	−6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7V_{REF}			V
CMOS Input Overvoltage	−2		+V_{CC} +2	V
Address A_2 Overvoltage	−V_{CC} −2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select[5]				
Single-Ended		3-bit Binary Code One of 8		
Differential		2-bit Binary Code One of 4		
Enable		Logic "0" Inhibits All Channels		
POWER REQUIREMENTS				
Over Temperature Range				
Rated Sypply Voltage		±15		V
Maximum Voltage Between				
Supply Pins			33	V
Total Power Dissipation		360		mW
Allowable Total Power Dissipation[6]			725	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+14, −12.5		mA
At 100kHz Switching Speed		+12.5, −12.5		mA

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C and ±V_{CC} = 15V, unless otherwise noted.

PARAMETER	MPC801KG, MPC801SG			UNITS
	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk[7]		See Typical Performance Curves		
T_{OPEN} (Break-before-make delay)		20		ns
Access Time at +25°C		80	125	ns
Over Temperature Range		110	150	ns
Settling Time[8]				
to 0.1% (20mV)		250		ns
to 0.01% (2mV)		800		ns
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S		1.9		pF
OFF Channel Output Capacitance, C_O		10		pF
OFF Input to Output Capacitance, C_{DS}		0.02		pF
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	−65		+150	°C
MPC800SG				
Specification	−55		+125	°C
Storage	−65		+150	°C

NOTES: (1) Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility. (2) V_{IN} = ±10V, I_{OUT} = 100µA. (3) Single-ended mode. (4) Logic levels specified for V_{REF} (pin 8) open. (5) For single-ended operation, connect output A (pin 18) to output B (pin 2) and use A_2 (pin 9) as an address line. For differential operation connect A_2 to −V_{CC}. (6) Derate 8mW/°C above T_A = +75°C. (7) 10Vp-p sine wave on all unused channels. See Typical Performance Curves. (8) For 20V step input to ON channel, into 1kΩ load.

PIN CONFIGURATION

Top View

+V_{CC}	1		18	Out A
Out B	2		17	−V_{CC}
IN8/4B	3		16	IN4/4A
IN7/3B	4		15	IN3/3A
IN6/2B	5		14	IN2/2A
IN5/1B	6		13	IN1/1A
GND	7		12	ENABLE
V_{REF}	8		11	A_0
A_2	9		10	A_1
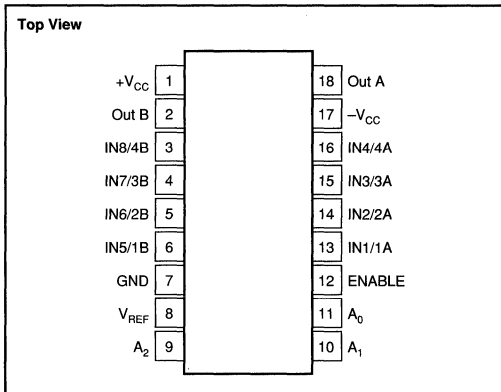
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPC801KG	Cerdip	0°C to +75°C
MPC801SG	Cerdip	−55°C to +125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC801KG	18-Pin Single-Wide Cerdip	266
MPC801SG	18-Pin Single-Wide Cerdip	266

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

MPC801

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MULTIPLEXERS

TYPICAL PERFORMANCE CURVES

At T_A = +25°C and ±V_{CC} = 15V, unless otherwise noted.

CROSS TALK vs SIGNAL FREQUENCY

Cross Talk (% of OFF Channel Signal) vs Signal Frequency (Hz)

LEAKAGE CURRENTS vs TEMPERATURE

Leakage Current (nA) vs Temperature (°C)

"ON" Channel

"OFF" Output

"OFF" Input

COMBINED CMR vs FREQUENCY FOR MODEL 3630 AND MPC800

CMR (dB) vs Frequency (Hz)

G = 1000

Balanced Source

Unbalanced = 1kΩ

Unbalanced = 10kΩ

SETTLING TIME vs SOURCE RESISTANCE
(20V Step Change, R_L = 1kΩ)

Settling Time (ns) vs Source Resistance (kΩ)

To 0.01%

To 0.1%

R_{ON} DRIFT vs TEMPERATURE

R_{ON} (Ω) vs Temperature (°C)

DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

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Multiplexer ON resistance error

DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

• *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedance of $10^8 \Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6 \Omega$ load impedance will increase source loading error to 0.2% or more.

• *Use sources with impedances as low as possible.* A 1000Ω source resistance will present less than 0.002% loading error and $10 k\Omega$ source resistance will increase source loading error 0.02% with a $10^8 \Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\in (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where, $R_S = R_{SOURCE}$

R_L = Load resistance

R_{OS} = Multiplexer ON resistance

FIGURE 1. MPC801 Static Accuracy Equivalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input offset voltage as a result of the voltage drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of 19µV if a 1000Ω source is used, and 118µV if a $10k\Omega$ source is used. In general, for the MPC801 the offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L) (R_{ON} + R_{SOURCE})$$

where:

I_B = Bias current of device multiplexer is driving

I_L = Multiplexer leakage current

R_{ON} = Multiplexer ON resistance

R_{SOURCE} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

FIGURE 2. MPC801 Static Accuracy Equivalent Circuit (Differential Operation).

Load (Output Device) Characteristics

• *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine input offset.

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MULTIPLEXERS

• *The system DC common-mode rejection* (CMR) can never be better than the combined CMR of multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.

• *Load impedances, differential and common-mode should* be $10^{10}\Omega$ or higher.

Source Characteristics

• *The source impedance unbalance* will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.

• *Keep source impedances as low as possible* to minimize resistive loading errors.

• *Minimize ground loops.* If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC801 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should be taken, but the parameters are not as critical as for low level signal applications.

FIGURE 3. Settling Time Effects (Single-ended).

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC801 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RCs. For the MPC801, the internal capacitance is approximately 10pF differential or 20pF single-ended. With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40ns. This means the source resistance should be kept to less than 4kΩ (assume high load resistance) to maintain fast settling times.

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 3 differential or 7 signal-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel. OFF resistance, and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with

FIGURE 4. Settling and Common-Mode Effects (Differential).

a 20Vp-p, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION
(Differential Mode Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC801 and Burr-Brown's model 3630 instrumentation amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 12, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC801, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 8) open, or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC801 as a 8-channel single-ended multiplexer, output A (pin 18) is connected to output B (pin 2) to form a single output, then all three address lines (A_0, A_1 and A_2) are used to address the correct channel.

The MPC801 can also be used as a dual channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC801 as an 4-channel differential multiplexer, connect address line A_2 to $-V_{CC}$ then use the remaining two address lines (A_0, and A_1) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC801 used as an 8-channel single-ended multiplexer or 4-channel dual multiplexer.

USE A_2 AS DIGITAL ADDRESS INPUT				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

For 8-channel single-ended function, tie "out A" to "out B", for dual 4-channel function use the A_2 address pin to select between MUX A and MUX B, where MUX A is selected with A_2 low.

MPC801 used as a 4-channel differential multiplexer.

A_2 CONNECT TO $-V_{CC}$			"ON" CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

MPC801

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MULTIPLEXERS

CHANNEL EXPANSION

Single-Tier Expansion

Up to eight MPC801s can be connected to a single node to form a 64-channel single-ended multiplexer, or up to eight MPC801s can be connected to two nodes to form a 32-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1-of-8 decoder (see Figure 5). The decoder drives the enable inputs of the MPC801 turning on only one multiplexer at a time.

Two-Tier Expansion

Up to nine MPC801s can be connected in a two-tier structure to form a 64-channel single-ended multiplexer (see Figure 6), or up to five MPC801s can be connected in a two-tier structure to form a 16-channel differential multiplexer. Programming is accomplished with a 6-bit address.

SINGLE VS MULTITIERED CHANNEL EXPANSION

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (4 or 8) in the multitiered configuration.

FIGURE 5. 64-channel, Single-tier, Single-ended Expansion.
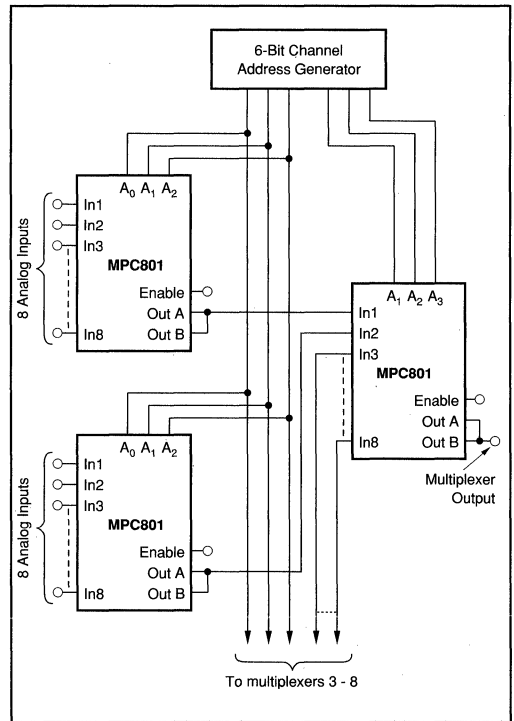
FIGURE 6. 64-channel, Two-tier, Single-ended Expansion.

6 Sample/Hold Amplifiers

Sample/hold amplifiers are a key part of an A/D conversion solution. While many new A/D converters have a self-contained sample/hold on the A/D chip, sample/hold amplifiers play a role in specialized applications such as multiple channel simultaneous sampling, and ultra-high speed sampling and multichannel output applications.

Burr-Brown products range from the industry standards SHC298 and SHC5320, now available in the SOIC package, to the high-speed SHC605 and the high-resolution SHC702.

Use of a sample/hold increases the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal to be converter is captured at a specific instant in time.

HIGH-SPEED SAMPLE/HOLD AMPLIFIERS Boldface = NEW

Description	Model	Gain Error (%)	Offset Error (mV)	Ampl BW –3dB, (MHz)	Acq Time (µs max)	Droop Rate (µV/µs)	Temp Range[1]	Input Range (Vp-p)	Pkg[2]	Q[3] Screen	Page No.
High Speed	SHC804	±0.1	±3	16	0.35	±5	Ind	20	HMD	Q	6.49
High Speed with Buffer	SHC803	±0.1	±3	16	0.35	±5	Ind	20	HMD	Q	6.49
Ultra-High Speed	SHC600	±0.1	±5	70	0.05	±180	Ind	2.5	CDIP	Q	A
Low Cost	SHC605	±0.1	±5	125	0.02[4]	±5000	Ext	4.0	16-p SOIC	—	6.15
High Linearity	SHC702	±0.1	±3	3	0.8	±2	Ind	20	24-p HMD	—	2.88

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C, Ext = –40°C to +85°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for the model. (4) Typical.

SAMPLE/HOLD AMPLIFIERS Boldface = NEW

Description	Model	Gain Error (%)	Offset Error (mV)	Charge Offset (mV)	Acq Time (µs max)	Droop Rate (µV/ms)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page No.
Fast, High Accuracy	SHC76	±0.02	±3	±6 typ	3	1	Ind, Com, Miil	HMD	—	6.2
Low Cost, Fast Industry Std	SHC5320	NA	±0.5	±1 typ	1.5	0.5	Com, Mil	HCD PDIP, SOIC, Die	BI	6.53
Lowest Cost Industry Std	SHC298	±0.01	±7	±25 max	10	100	Com, Ind	PDIP, MC, SOIC	BI	6.7
Wideband DC Restoration Circuit	SHC615	0.1[4]	8	1.5[4]	15µs[4]	160[4]	Xlind	PDIP, SOIC	—	6.30

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Xlind = –40°C to +85°C, Mil = –55°C to +125°C, Ext = –40°C to +85°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for the model. (5) With 27pF external hold capacitor.

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SAMPLE/HOLD AMPLIFIERS

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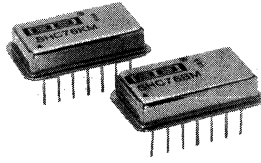
SHC76

SAMPLE/HOLD AMPLIFIER

FEATURES

● **FAST (6μs max) ACQUISITION TIME (14-bit)**

● **APERTURE JITTER 400ps**

● **POWER DISSIPATION: 300mW**

● **COMPATIBLE WITH HIGH RESOLUTION A/D CONVERTERS ADC76, PCM75, AND ADC71**

DESCRIPTION

The SHC76 is fast, high-accuracy hybrid sample/hold circuit suitable for use in high-resolution data acquisition systems.

The SHC76 is complete with internal hold capacitor and incorporates an internal compensation network which minimizes sample-to-hold charge offset. The SHC76 is configured as a unity-gain inverter.

High-resolution converters such as the ADC76 and ADC71 are compatible with SHC76 in forming complete, 14-bit accurate analog-to-digital conversion systems.

The SHC76 comes in a 14-pin single-wide hermetic metal DIP. Power supply requirements are specified from ±14.5V to ±15.5V with guaranteed operation from ±11.4V to ±18V. Input voltage range is ±10V. The SHC76 is available in two temperature ranges: KM, for 0°C to +70°C; and BM, for –25°C to +85°C operation.

PDS-641A

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C, and nominal power supply voltage of ±15V, unless otherwise noted.

PARAMETER	SHC76KM, BM			UNITS
	MIN	TYP	MAX	
ANALOG INPUTS				
Voltage Range	±10			V
Overvoltage, no damage			±15	V
Impedance		3000		Ω
DIGITAL INPUT				
(TTL-Compatible)				
Track Mode, Logic "1"	2		5.5	V
Hold Mode, Logic "0"	0		0.8	V
I_{IH}, V_{IH} = 2.4V			400	μA
I_{IL}, V_{IL} = 0.4V			1000	μA
ANALOG OUTPUT				
Voltage		±10		V
Current		5		mA
Short-Circuit Current		20		mA
Impedance		1		Ω
DC ACCURACY/STABILITY				
Gain		−1.00		V/V
Gain Error		±0.01	±0.02	%
Gain Nonlinearity				
(±10V Output Track)		±0.001		%
Gain Temperature Coefficient		1	5	ppm/°C
Offset Voltage[1]			±3	mV
Output Offset at T_{MIN}, T_{MAX} (Track)		±6		mV
TRACK MODE DYNAMICS				
Freqency Response				
Small Signal (−3dB)		1.5		MHz
Full Power Bandwidth		0.5		MHz
Slew Rate		30		V/μs
Noise in Track Mode				
(DC to 1.0MHz)		200		μVrms
TRACK-TO-HOLD SWITCHING				
Aperture Time		30		ns
Aperture Uncertainty (Jitter)		0.4		ns
Offset Step (Pedestal)		±2	±4	mV
Pedestal at Temperature				
KM Grade		±4		mV
BM Grade		±6		mV
Switching Transient				
Amplitude		200		mV
Settling to 1mV		0.5	2	μs
Settling to 0.3mV		1	3	μs
HOLD MODE DYNAMICS				
Droop Rate		0.1	1	μV/μs
Droop Rate at T_{MAX}			100	μV/μs
Feedthrough Rejection				
(10Vp-p, 20kHz)	74	86		dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
To ±0.01% of 20V		1.5	3	μs
To ±0.003% of 20V		4	6	μs
POWER REQUIREMENTS				
Nominal Voltages for Rated				
Performance	±14.5	±15	±15.5	V
Operating Range[2]	±11.4		±18	V
Power Supply Rejection		100		μV/V
Supply Current: $+V_S$		15	20	mA
$-V_S$		−4	−10	mA
Power Dissipation		300	500	mW
TEMPERATURE RANGE				
Operating: KM Grade	0		+70	°C
BM Grade	−25		+85	°C
Storage	−55		+125	°C

NOTES: (1) Adjustable to zero with external circuit. (2) Operating to derated performance with $V_{IN} < V_S$ −5V.

CONNECTION DIAGRAM
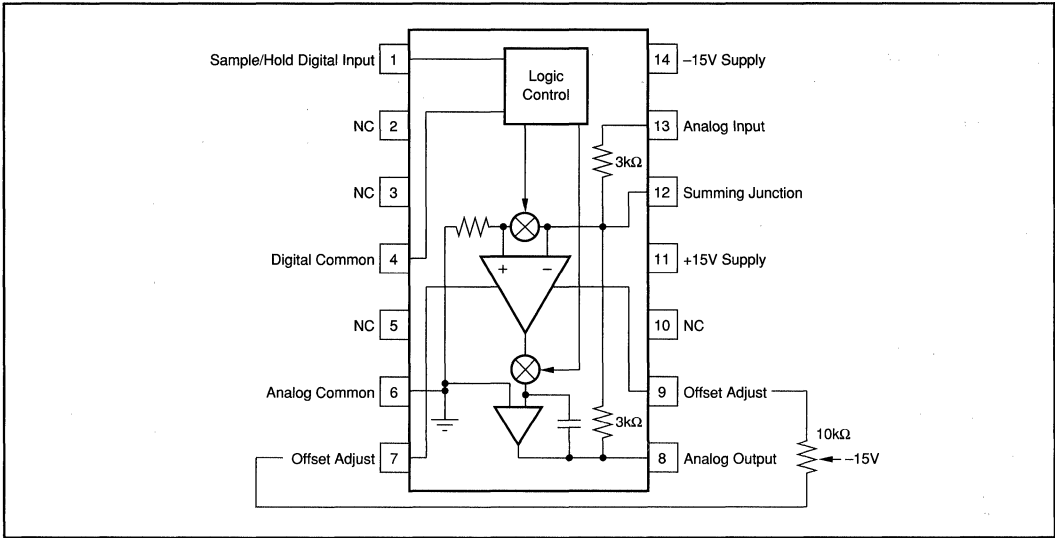
ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between +V_{CC} and –V_{CC} Terminals 40V
Input Voltage .... Actual Supply Voltage
Differential Input Voltage .... ±24V
Digital Input Voltage .... –0.5V to +5.5V
Output Current Continuous[2] .... ±20mA
Internal Power Dissipation 500mW
Storage Temperature Range .... –65°C < T_A < +150°C
Output Short-Circuit Duration[3] .... Momentary to Common
Lead Temperature (soldering, 10s) .... +300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
SHC76KM	14-Pin Single-Wide, Hermetic Metal DIP	0°C to +70°C
SHC76BM	14-Pin Single-Wide, Hermetic Metal DIP	–25°C to +85°C

PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Digital Input	8	Analog Output
2	No Connection	9	Offset Adjust
3	No Connection	10	No Connection
4	Digital Ground	11	+15V Supply
5	No Connection	12	Summing Junction
6	Analog Ground	13	Analog Input
7	Offset Adjust	14	–15V Supply

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC76KM	14-Pin Single-Wide, Hermetic Metal DIP	107
SHC76BM	14-Pin Single-Wide, Hermetic Metal DIP	107

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

This is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

GAIN ERROR

The difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

DROOP RATE

The voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

FEEDTHROUGH

The amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

APERTURE DELAY TIME

The time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

APERTURE UNCERTAINTY TIME

The nonrepeatibility of aperture delay time.

ACQUISITION TIME

The time required for the sample/hold output to settle within a given error band of its final value when the sample/hold is switched from Hold to Sample.

CHARGE OFFSET (PEDESTAL)

The output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.
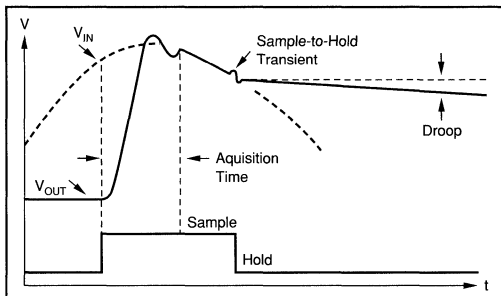
FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

SAMPLE-TO-HOLD SWITCHING TRANSIENT

The switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

SAMPLED DATA ACQUISITION SYSTEM CALCULATIONS

The rated accuracy of an A/D converter in combination with the aperture uncertainty of a sample/hold determine the maximum theoretical input slew rate (frequency) of a given sampled data system.

Sine Wave $f_{MAX} = (2^{-N} FSR) \div (2\pi A t)$
A = max Input Signal Amplitude (peak-to-peak)
FSR = Full-Scale Range of A/D Converter
t = Aperture Uncertainty of S/H (jitter)
N = Number of Bits Accuracy

Given below are the maximum input frequencies of two A/D converters in conjunction with the SHC76:

SHC76 13-bit Sine Wave $f_{MAX} =$
$(0.000122 \cdot 20V) \div (2 \cdot \pi \cdot 20V \cdot 0.4ns) = 48.6kHz$

SHC76 14-bit Sine Wave $f_{MAX} =$
$(0.000061 \cdot 20V) \div (2 \cdot \pi \cdot 20V \cdot 0.4ns) = 24.3kHz$

The maximum throughput rate is determined by adding all critical conversion process times together. Throughput rate cannot exceed the maximum input frequency determined by the accuracy and jitter specs without degrading system performance. Two samples per period of a sine wave are required to satisfy the Nyquist sampling theorem. A low-pass filter is required to cut off frequencies higher than the maximum throughput frequency to prevent aliasing errors from occurring.

Throughput f_{MAX} (2 samples) =
1 ÷ [2 (S/H acquisition time + S/H settling time + A/D conversion time)]

Table I is a listing of various A/D throughput rates using the SHC76 S/H amplifier (assuming two samples per period).

CONVERTER	ACCURACY (Bits)	CONVERSION SPEED (µs)	RESOLUTION (Bits)	THROUGHPUT F_{MAX} (kHz)
ADC76KG	14	17	16	19.2
	14	16	15	20.0
	14	15	14	20.8
ADC76JG	13	17	16	23.8
	13	16	15	25.0
	13	15	14	26.3
ADC71KG	14	57	16	7.58
	14	54	15	7.94
	14	50	14	8.47
ADC71JG	13	57	16	8.20
	13	54	15	8.62
	13	50	14	9.26

TABLE I. A/D Converter Throughput Rates.

SHC76

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SAMPLE/HOLD AMPLIFIERS

APPLICATIONS

Figures 2 and 3 show the SHC76 in combination with an ADC76 and ADC71 to provide 14-bit accurate A/D conversion systems.
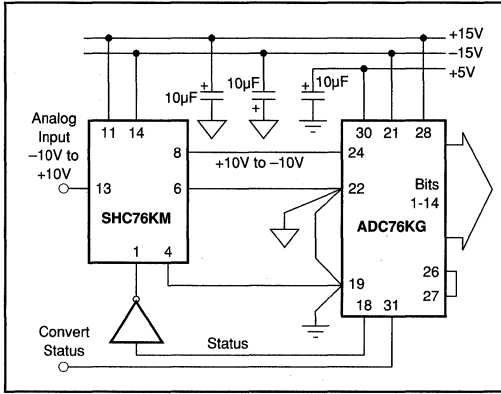
FIGURE 2. A 20kHz A/D Conversion System (14-bit accurate).
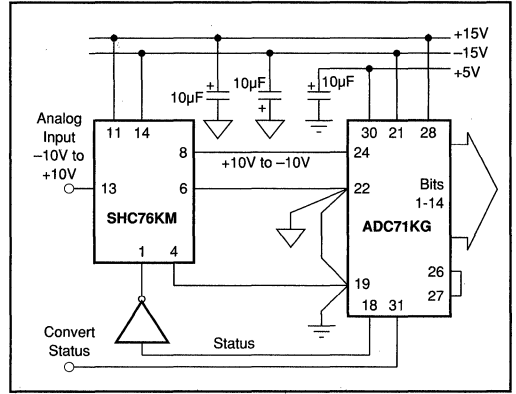
FIGURE 3. A 8.47kHz A/D Conversion System (14-bit accurate).

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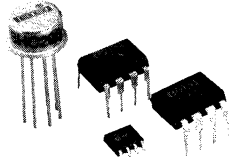
SHC298
SHC298A

Monolithic
SAMPLE/HOLD AMPLIFIER

FEATURES

● **12-BIT THROUGHPUT ACCURACY**
● **LESS THAN 10µs ACQUISITION TIME**
● **WIDEBAND NOISE LESS THAN 20µVrms**
● **RELIABLE MONOLITHIC CONSTRUCTION**
● **10^{10}Ω INPUT RESISTANCE**
● **TTL-CMOS-COMPATIBLE LOGIC INPUT**

DESCRIPTION

The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6µs acquisition time. Droop rates less than 5mV/min are possible with a 1µF holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from ±5V to ±18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample on the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from –25°C to +85°C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0°C to +70°C.

The SHC298AJP, specified over 0°C to +70°C, is available in an 8-pin plastic DIP. The SHC298A grade features improved gain and offset error, improved drift over temperature, and faster acquisition time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.

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SHC298/SHC298A

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SAMPLE/HOLD AMPLIFIERS

SPECIFICATIONS

ELECTRICAL

T_J = +25°C, ±15V supplies, 1000pF holding capacitor, –11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

PARAMETER	SHC298AM/JP/JU MIN	SHC298AM/JP/JU TYP	SHC298AM/JP/JU MAX	SHC298AJP MIN	SHC298AJP TYP	SHC298AJP MAX	UNITS
ANALOG INPUT							
Resistance		10^{10}			*		Ω
Bias Current[1]		10	50		*	25	nA
DIGITAL INPUT	Pin 7		Pin 8		Circuit State		
Mode Control Truth Table	0V		+2.4V		Sample (Track)		
	0V		+0.8V		Hold		
	+2.4V		+2.8V		Hold		
	+0.8V		+2.8V		Sample (Track)		
Mode Control and Mode Control Reference Input Current			10				µA
Differential Logic Threshold	0.8	1.4	2.4				V
TRANSFER CHARACTERISTICS							
ACCURACY (+25°C)							
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015		*	*	% of 20V
Gain		+1			*		V/V
Gain Error		±0.004	±0.010		±0.001	±0.005	%
Input Voltage Offset (adjust to zero)[1]		±2	±7		±1	±2	mV
Droop Rate[1]		±30	±200		*	±100	µV/ms
Charge Offset[2]		±15	±25		*	*	mV
Noise (rms) 10Hz to 100kHz		10	20		*	*	µV
Power Supply Rejection		±25	±100		*	*	µV/V
ACCURACY DRIFT							
Gain Drift		3	4		1	2	ppm/°C
Input Offset Drift		15	70		*	25	µV/°C
Charge Offset Drift, C = 1000pF		50	150		*	*	µV/°C
Charge Offset Drift, C = 10,000pF		20	50		*	*	µV/°C
Droop Rate at T_J = +85°C		1	10		*	*	mV/ms
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth, C = 1000pF	75	125		*	*		kHz
Full Power Bandwidth, C = 10,000pF	10	16		*	*		kHz
Output Slew Rate, C = 1000pF	7	10		*	*		V/µs
Output Slew Rate, C = 10,000pF	1.4	2		*	*		V/µs
Aperture Time : Negative Input Step		200	250		*	*	ns
Positive Input Step		150	200		*	*	ns
Acquisition Time (C = 1000pF): to ±0.01%, 10V Step		6	10		*	*	µs
to ±0.01%, 20V Step		8	12		*	*	µs
to ±0.1%, 10V Step		5	9		4	6	µs
to ±0.1%, 20V Step		7	11		*	*	µs
Sample/Hold Transient: Peak Amplitude		160			*		mV
Settling to 1mV		1	1.5		*	*	µs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015		±0.004	±0.0075	% of 20V
OUTPUT							
ANALOG OUTPUT							
Voltage Range	±11.5			*			V
Current Range	±2			*			mA
Impedance (in Hold Mode)	0.5	4		*	*		Ω
POWER SUPPLY							
Rate Voltage		15			*		VDC
Range	±5		±18	*		*	VDC
Current[1]		±4.5	±6.5		*	*	mA

* Same as specifications for SHC298AM/JP/JU.

NOTES: (1) These parameters guaranteed over a supply voltage range of ±5V to = ±18V. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

PIN CONFIGURATIONS

Top View   **TO-99**

Top View   **Plastic DIP/Small Outline**
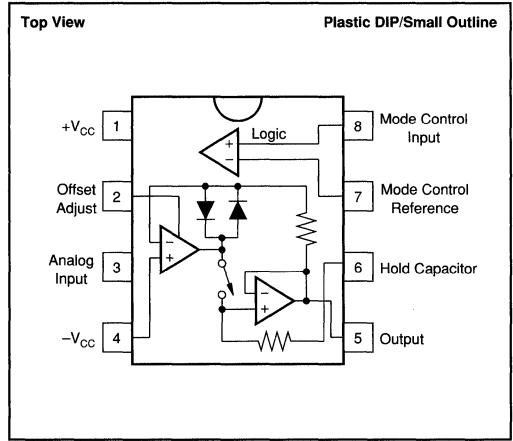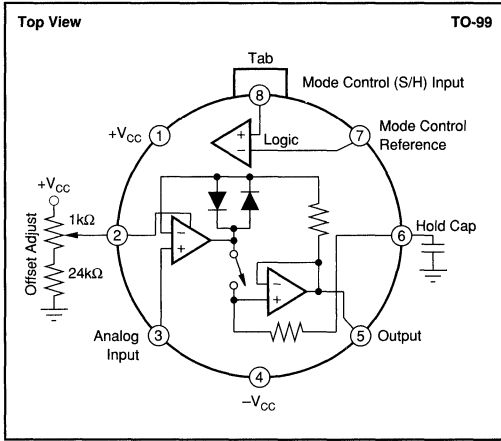
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Power Dissipation (Package Limitation) 500mV
Junction Temperature, $T_{J\,MAX}$
    AM .... 125°C
    JP, JU .... 100°C
Operating Temperature Range .... −25°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Input Voltage .... Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage[1] .... +7V, −30V
Output Short Circuit Duration .... Indefinite
Hold Capacitor Short Circuit Duration 10s
Lead Temperature (soldering, 10s) .... 300°C

NOTE: (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BURN-IN SCREENING

Burn-in screening is available for both plastic and TO-99 metal can packages. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

    Plastic "–BI" models: +85°C
    TO-99 "–BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "–BI" to the base model number.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
SHC298AM	TO-99	−25°C to +85°C
SHC298JP	8-pin DIP	0°C to +70°C
SHC298JU	8-lead SOIC	0°C to +70°C
SHC298AJP	8-pin DIP	0°C to +70°C

BURN-IN SCREENING OPTION		
See text for details.		

MODEL	PACKAGE	TEMPERATURE RANGE
SHC298AM-BI	TO-99	−25°C to +85°C
SHC298JP-BI	8-pin DIP	0°C to +70°C
SHC298JU-BI	8-lead SOIC	0°C to +70°C
SHC298AJP-BI	8-pin DIP	0°C to +70°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC298AM	TO-99	001
SHC298JP	8-Pin Plastic DIP	006
SHC298JU	8-Lead SOIC	182
SHC298AJP	8-Pin Plastic DIP	006
SHC298AM-BI	TO-99	001
SHC298JP-BI	8-Pin Plastic DIP	006
SHC298JU-BI	8-Lead SOIC	182
SHC298AJP-BI	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

SHC298/SHC298A

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SAMPLE/HOLD AMPLIFIERS

TYPICAL PERFORMANCE CURVES

T_J = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

APERTURE TIME

+V_{CC} = −V_{CC} = 15V
ΔV_{OUT} ≤ mV
ΔV_{IN} = 10V

Negative Input Step

Positive Input Step

Time (ns) vs Junction Temperature (°C)

CHARGE OFFSET

V_{IN} = 0V
T_J = 25°C

Hold Step (mV) vs Hold Capacitor (μF)

SAMPLE-TO-HOLD TRANSIENT SETTLING TIME

+V_{CC} = −V_{CC} = 15V
Settling to 1mV

Time (ns) vs Junction Temperature (°C)

OUTPUT DROOP RATE

T_J = 125°C
T_J = 70°C
T_J = 0°C
T_J = 25°C

$\Delta V/\Delta T$ (V) vs Hold Capacitor (μF)

ACQUISITION TIME

V_{IN} = 0V to ±10V
T_J = 25°C

0.1%
0.01%

Time (μs) vs Hold Capacitor (μF)

OUTPUT NOISE

"Hold" Mode
"Sample" Mode

Noise (nV/√Hz) vs Frequency (Hz)

TYPICAL PERFORMANCE CURVES (CONT)

T_J = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

DYNAMIC SAMPLING ERROR

+V_{CC} = −V_{CC} = 15V
T_J = 25°C

Hold Capacitor
0.01µF
1000pF
0.1µF
3000pF
1µF

Error (mV)

Input Slew Rate (V/ms)

GAIN ERROR

T_J = 25°C
R_L = 10kΩ
Sample Mode

Slope ≈ 0.0007%

Input-Output Voltage (mV)

Output Voltage (V)

CHARGE OFFSET

C_H = 0.01µF
T_J = 25°C

T_J = −55°C
T_J = 125°C
T_J = 25°C

Hold Step (mV)

Input Voltage (V)

POWER SUPPLY REJECTION

T_J = 25°C
+V_{CC} = −V_{CC} = 15V
V_{OUT} = 0V

Positive Supply
Negative Supply

Rejection Ratio (dB)

Frequency (Hz)

INPUT BIAS CURRENT

Current (nA)

Junction Temperature (°C)

FEEDTHROUGH REJECTION RATIO

+V_{CC} = −V_{CC} = 15V
V_{IN} = 10Vp-p
T_J = 25°C

C_H ≥ 0.1µF
C_H = 0.01µF
C_H = 1000pF

Rejection Ratio (dB)

Frequency (Hz)

SHC298/SHC298A

SAMPLE/HOLD AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

$T_J = +25°C$, $\pm15V$ supplies, 1000pF holding capacitor, $-11.5V \leq V_{IN} \leq +11.5$, $R_L = 10k\Omega$, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

PHASE AND GAIN
(Input to Output, Small Signal)

CHARGE OFFSET

DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1ms of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10μs acquisition time, and 1ms Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between input and output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.
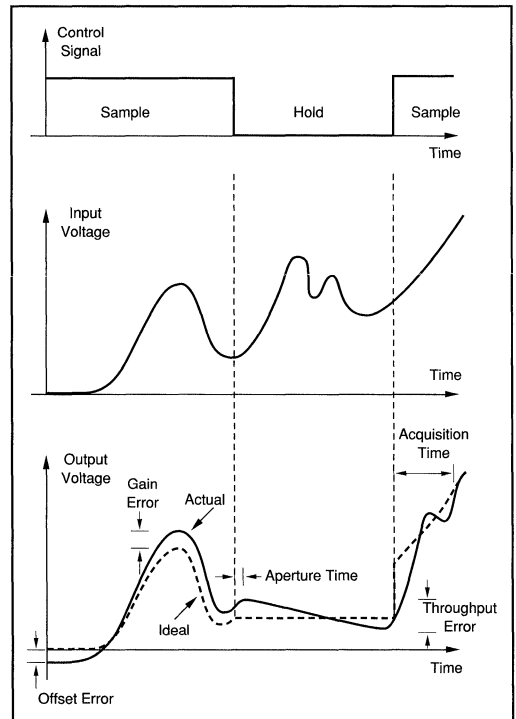
FIGURE 1. Sample/Hold Errors.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as Teflon®, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF, the droop will reduce to approximately 2.5μV/ms and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in the Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298 may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

DATA DISTRIBUTION

The SHC298 may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

TEST SYSTEMS

The SHC298 is also well suited for use in test systems to acquire and hold data transients for human operators or for the other parts of the test system such as comparators, digital voltmeters, etc.

®Teflon, DuPont de Nemours

With a 0.1μF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high-speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5). For low-level systems, and instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.
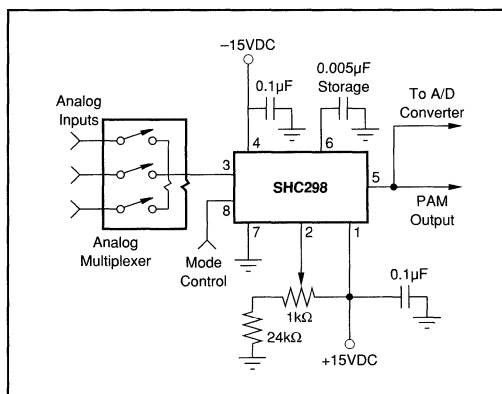
FIGURE 2. Data Acquisition.
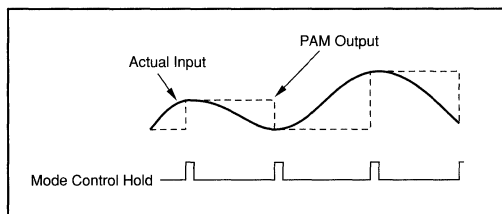
FIGURE 3. PAM Output.

SHC298/SHC298A

SAMPLE/HOLD AMPLIFIERS

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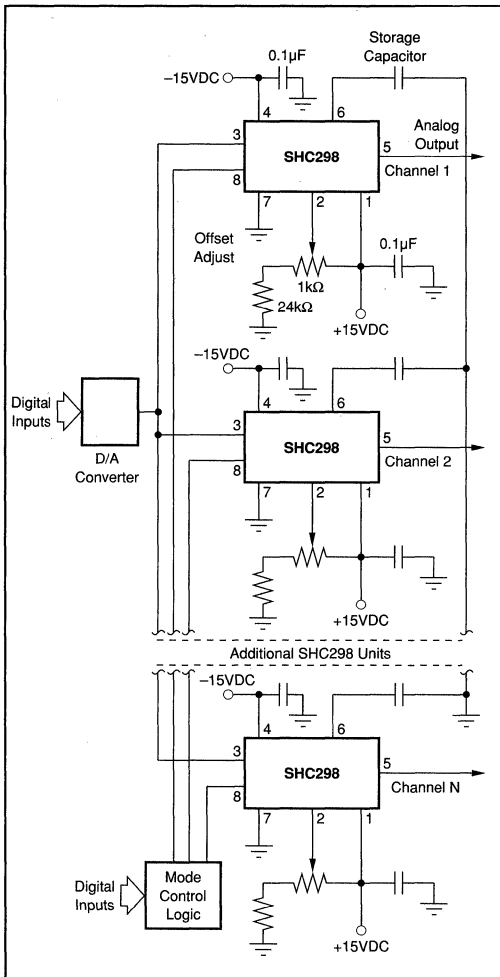
FIGURE 4. Data Distribution.
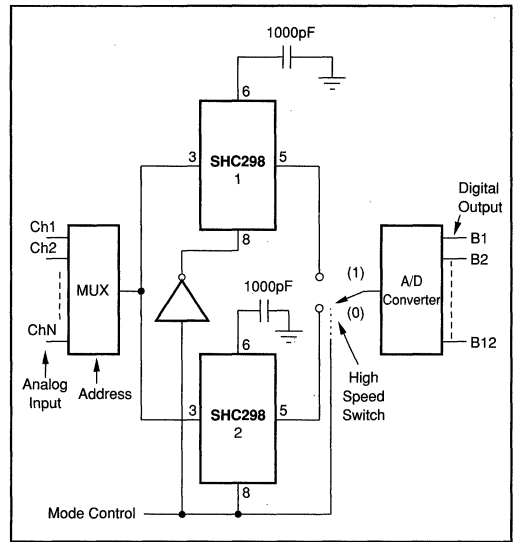
FIGURE 5. "Ping-Pong" Sample Holds.

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[BB]
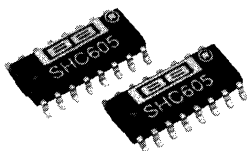
SHC605

DEMO BOARD
AVAILABLE
See Appendix A for
more information.

High-Speed Operational
TRACK-AND-HOLD AMPLIFIER

<div style="float:right">

SHC605

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SAMPLE/HOLD AMPLIFIERS

</div>

FEATURES

- **VERY GOOD SPURIOUS FREE DYNAMIC RANGE**
  90dB at 1MHz F_{IN} and 20MSPS
  86dB at 2MHz F_{IN} and 20MSPS
  77dB at 5MHz F_{IN} and 20MSPS
- **LOW ACQUISITION TIME: 30ns to 0.01%**
- **LOW DROOP RATE: 8mV/μs max T_{MIN} to T_{MAX}**
- **LOW POWER CONSUMPTION: 335mW**
- **EXTREMELY VERSATILE ARCHITECTURE: Noninverting, Inverting, and Differential Gains**
- **LOGIC FLEXIBILITY: TTL and ECL Compatible**
- **SMALL PACKAGE: 16-Lead SOIC**
- **EXTENDED TEMPERATURE SPECS: –40°C to +85°C**

APPLICATIONS

- **A/D CONVERTER FRONT ENDS**
- **MULTIPLE CHANNEL SIMULTANEOUS SAMPLING**
- **IMPROVING FLASH ADC PERFORMANCE**
- **PEAK DETECTORS**
- **DAC DEGLITCHING**

DESCRIPTION

The SHC605 is a monolithic high-speed, high accu-racy track-and-hold amplifier. It combines fast acqui-sition and low distortion to provide a complete solu-tion for a wide range of sampling applications. Its new proprietary closed-loop architecture provides a single-chip solution to many data acquisition problems for-merly requiring more than one device. Non-inverting, inverting, and differential gain configurations are easy to apply with the SHC605. An on-board logic refer-ence circuit makes the SHC605 compatible with both single-ended and differential ECL or TTL clock in-puts. An internal track-mode lockout circuit allows edge-triggered operation in data acquisition systems. The SHC605 is available in a 16-lead SOIC package specified for the –40C to +85C industrial temperature range.

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PDS-1165C

6.15

SPECIFICATIONS

ELECTRICAL

$T_A = +25°C$, $\pm V_S = \pm 5V$, $G = +1V/V$, $R_L = 100\Omega$, $C_L = 5pF$, ECL Hold/$\overline{Hold}$ Inputs unless otherwise noted.

PARAMETER	CONDITION	TEMP RANGE	SHC605AU			UNITS
			MIN	TYP	MAX	
DC INPUT PARAMETERS						
Offset Voltage		Full		±1	±7.5	mV
Power Supply Rejection	$V_S = \pm4.5$ to $\pm5.5V$	+25°C	60	85		dB
Input Bias Current	$V_{CM} = 0V$	Full		15	50	µA
Input Offset Current	$V_{CM} = 0V$	Full		±0.2	±5	µA
Common-mode Input Range		Full	±2.0	±2.5		V
Common-mode Rejection	$V_{CM} = \pm2VDC$	Full		80		dB
Differential Input Impedance		Full		13‖1		kΩ‖pF
Common-Mode Input Impedance		Full		2‖1		MΩ‖pF
Open-loop Voltage Gain	$V_O = \pm2V$, $R_L = 100\Omega$	+25°C		100		dB
OUTPUT						
Voltage Output	$R_L = 50\Omega$	Full	±2.0	±2.5		V
Current Output		+25°C	±40	±80		mA
		Full	±40	±60		mA
Short Circuit Current		Full		±140		mA
Output Resistance,						
Closed-Loop: Track-Mode	DC	Full		0.0001		Ω
Hold-Mode	DC	Full		0.01		Ω
DIGITAL INPUTS/OUTPUTS						
TTL Input Levels [1]	Hold Input Only					
V_{IL}	Logic "LO"	Full	0		+1.0	V
V_{IH}	Logic "HI"	Full	+2.0		+5.0	V
Single-Ended ECL Input Levels [2]	Hold/$\overline{Hold}$ and Lock/$\overline{Lock}$ Inputs					
V_{IL}	Logic "LO"	Full	−1.80		−1.45	V
V_{IH}	Logic "HI"	Full	−1.05		−0.80	V
Common-Mode Input Voltages	Hold/$\overline{Hold}$	Full	−3		+5	V
	Lock/$\overline{Lock}$	Full	$-V_S$		+3	V
Differential Input Voltages	Hold/$\overline{Hold}$ and Lock/$\overline{Lock}$ Inputs	Full	0.2		5.0	V
Digital Input Currents						
I_{IL}, Lock/$\overline{Lock}$ Inputs Only	ECL Logic "LO", $V_{IL} = -1.60V$	Full			5	µA
I_{IL}, Hold/$\overline{Hold}$ Inputs Only	ECL or TTL Logic "LO"	Full			−100	µA
I_{IH}, Lock/$\overline{Lock}$ Inputs Only	Logic "HI", $V_{IH} = -1.0V$	Full			50	µA
I_{IH}, Hold/$\overline{Hold}$ Inputs Only		Full			−10	µA
Threshold Voltage Output[3]						
TTL[4]		Full	1.1	1.5	1.9	V
ECL[5]	$-V_S = -5.2V$	Full	−1.40		−1.10	V
TRACK-MODE RESPONSE						
Closed-Loop Bandwidth	Gain = +1V/V	+25°C	100	200		MHz
	Gain = +2V/V	+25°C		75		MHz
	Gain = +5V/V	+25°C		20		MHz
	Gain = +10V/V	+25°C		10		MHz
Full Power Response	±1V Input, −3dB Output	Full		32		MHz
Slew Rate [6]	G = +1, 2V Step	+25°C	140	200		V/µs
		Full	120	200		V/µs
Acquisition Time to 1%[7]	2V Step	Full		15	25	ns
0.1%	2V Step	Full		23	35	ns
0.012%	2V Step	Full		30	45	ns
0.012%	4V Step	Full		40	60	ns
Input Voltage Noise	1MHz to 100MHz			2.5		nV/√Hz
Input Bias Current Noise	1MHz to 100MHz			2.5		pA/√Hz
Differential Gain	3.58MHz, $V_O = 0$ to 0.7Vp–p			0.005		%
Differential Phase	3.58MHz, $V_O = 0$ to 0.7Vp–p			0.005		degrees
Spurious Free Dynamic Range						
(5MHz)	$V_O = \pm1V$			83		dBc
(10MHz)	$V_O = \pm1V$			73		dBc

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is $10\mu V_{rms}$. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

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SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25°C$, $\pm V_S = \pm 5V$, $G = +1V/V$, $R_L = 100\Omega$, $C_L = 5pF$, ECL Hold/$\overline{Hold}$ Inputs unless otherwise noted.

PARAMETER	CONDITION	TEMP RANGE	SHC605AU MIN	SHC605AU TYP	SHC605AU MAX	UNITS
TRACK-TO-HOLD SWITCHING	$V_{IN} = 0V$					
Aperture Delay		Full		1.7		ns
Aperture Jitter		Full		2.4		ps rms
Pedestal Offset		+25°C		±5	±20	mV
over Temperature		Full		±5	±25	mV
Transient Amplitude		Full		±5		mV
Settling Time to 1mV		Full		8	15	ns
100μV		Full		15		ns
HOLD-MODE RESPONSE						
Spurious Free Dynamic Range						
(1MHz, 20MSPS)	$V_O = \pm 1V$	Full	78	90		dBc
(2MHz, 20MSPS)	$V_O = \pm 1V$	Full	74	86		dBc
(5MHz, 20MSPS)	$V_O = \pm 1V$	Full	65	77		dBc
(10MHz, 20MSPS)	$V_O = \pm 1V$	+25°C		60		dBc
(10MHz, 20MSPS)	$V_O = \pm 0.5$	+25°C		72		dBc
Hold Noise[8]				$400xt_H$		V/s rms
Droop Rate		Full		±1	±8	mV/μs
Hold Time[9]		Full			2	μs
Feedthrough Rejection (20MHz)		+25°C		85		dB
POWER SUPPLY						
Specified Operating Voltage		Full	±4.50	±5	±5.50	V
Positive Supply Current[10]		Full		34	39	mA
Negative Supply Current[10]		Full		33	39	mA
Total Power Dissipation		Full		335	390	mW
TEMPERATURE RANGE						
Specification	Ambient	Full	−40		+85	°C
Storage			−55		+150	°C
Thermal Resistance, θ_{JA}		Full		100		°C/W

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is $10\mu V_{rms}$. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Input Voltage Range	±5V
Differential Input Voltage	±5.5V (between +In and −In inputs)
Storage Temperature Range	−40°C to +125°C
Lead Temperature (soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_j)	+175°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC605AU	16-Pin SOIC	265

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
SHC605AU	16-Pin SOIC	−40°C to +85°C

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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SAMPLE/HOLD AMPLIFIERS

PIN CONFIGURATION

U Package　　　　　　**16-Pin SOIC**

+In	1		16	$-V_S$
$+V_S$	2		15	$-V_S$
$+V_S$	3		14	Lock
DGND	4		13	$\overline{\text{Lock}}$
AGND	5		12	Hold
AGND	6		11	Thresh/$\overline{\text{Hold}}$
AGND	7		10	Select
−In	8		9	V_{OUT}
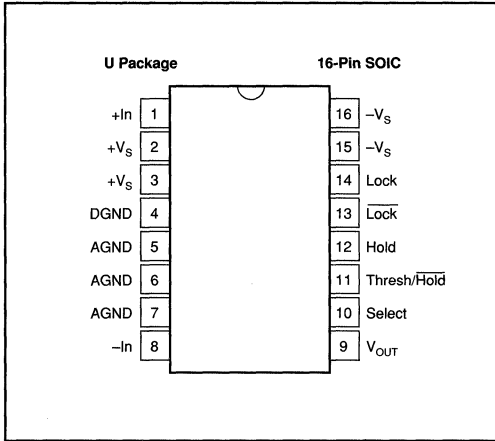
PIN DESCRIPTION

PIN #	SYMBOL	DESCRIPTION
1	+In	Non-Inverting Input
2	$+V_S$	+5V Supply
3	$+V_S$	+5V Supply
4	DGND	Digital Ground
5	AGND	Analog Ground
6	AGND	Analog Ground
7	AGND	Analog Ground
8	−In	Inverting Input
9	V_{OUT}	Output Voltage
10	Select	+5V Selects TTL; −5V Selects ECL
11	Thresh/$\overline{\text{Hold}}$	Logic threshold for single-ended operation or complement Hold input for differential operation
12	Hold	True Hold input
13	$\overline{\text{Lock}}$	Complement Lock Input
14	Lock	True Lock input; Locks SHC605 in Hold-mode regardless of Hold/$\overline{\text{Hold}}$ Inputs
15	$-V_S$	−5V Supply
16	$-V_S$	−5V Supply

DICE INFORMATION

SHC605 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	+In	10	Select
2	$+V_S$	11	$\overline{\text{Comp}}$
3	$+V_S$	12	Thresh/$\overline{\text{Hold}}$
4	DGND	13	Hold
5	AGND	14	$\overline{\text{Lock}}$
6	C_2	15	Lock
7	C_1	16	$-V_S$
8	−In	17	$-V_S$
9	V_{OUT}		

Substrate Bias: Negative supply ($-V_s$).

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	58 x 80	
Die Thickness	14 ±1	
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	
Metallization	Gold	

TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $\pm V_S = \pm 5V$, $G = +1V/V$, $R_L = 100\Omega$, $C_L = 5pF$, ECL Hold/$\overline{\text{Hold}}$ Inputs unless otherwise noted.
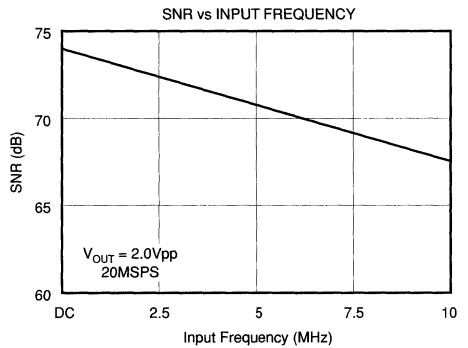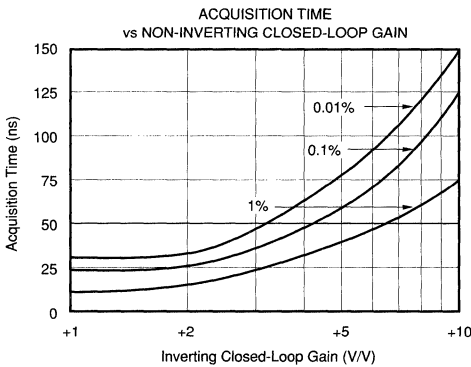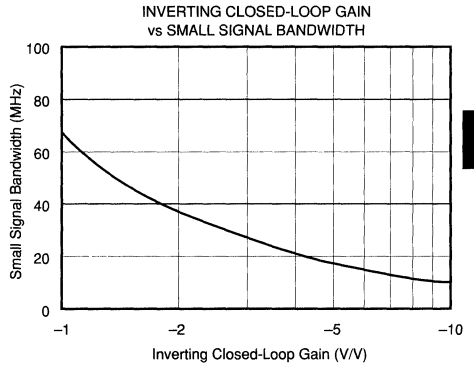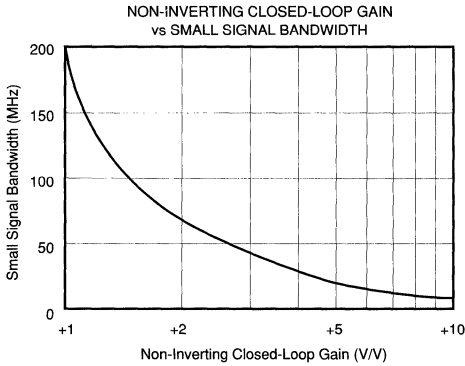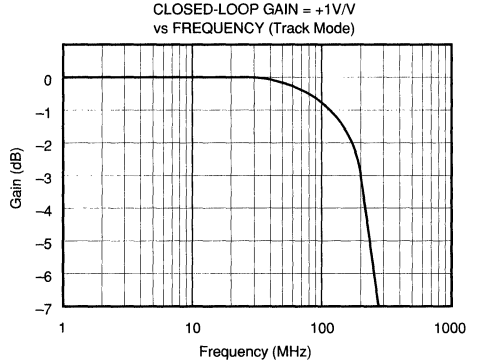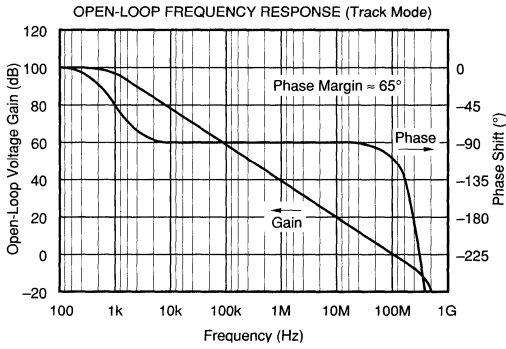
OPEN-LOOP FREQUENCY RESPONSE (Track Mode)

CLOSED-LOOP GAIN = +1V/V vs FREQUENCY (Track Mode)

NON-INVERTING CLOSED-LOOP GAIN vs SMALL SIGNAL BANDWIDTH

INVERTING CLOSED-LOOP GAIN vs SMALL SIGNAL BANDWIDTH

ACQUISITION TIME vs NON-INVERTING CLOSED-LOOP GAIN

SNR vs INPUT FREQUENCY

SHC605

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SAMPLE/HOLD AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $\pm V_S = \pm 5V$, $G = +1V/V$, $R_L = 100\Omega$, $C_L = 5pF$, ECL Hold/$\overline{Hold}$ Inputs unless otherwise noted.

LARGEST HARMONIC
vs INPUT FREQUENCY (Track Mode)

LARGEST HARMONIC
vs INPUT FREQUENCY (Hold Mode)

FEEDTHROUGH REJECTION
vs INPUT FREQUENCY

POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY (Track Mode)

DROOP RATE vs TEMPERATURE

PEDESTAL vs TEMPERATURE

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, ±V_S = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, ECL Hold/$\overline{\text{Hold}}$ Inputs unless otherwise noted.

HOLD-MODE DISTORTION
@ 20MSPS, V_{IN} = 2MHz

V_{OUT} = 2Vpp
R_L = 100Ω
V_{IN} = 2MHz
$f_{T/H}$ = 20MHz
t_{TRACK} = 35ns

HOLD-MODE DISTORTION
@ 20MSPS, V_{IN} = 5MHz

V_{OUT} = 2Vpp
R_L = 100Ω
V_{IN} = 5MHz
$f_{T/H}$ = 20MHz
t_{TRACK} = 35ns

HOLD-MODE DISTORTION
@ 20MSPS, V_{IN} = 10MHz

V_{OUT} = 1Vpp
R_L = 100Ω
V_{IN} = 10MHz
$f_{T/H}$ = 20MHz
t_{TRACK} = 35ns

HOLD-MODE DISTORTION
@ 20MSPS, V_{IN} = 10MHz

V_{OUT} = 2Vpp
R_L = 100Ω
V_{IN} = 10MHz
$f_{T/H}$ = 20MHz
t_{TRACK} = 35ns

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SAMPLE/HOLD AMPLIFIERS

TIMING DEFINITIONS

Acquisition Time is the time it takes to reacquire the input signal when switching from the hold to track mode. This time interval starts at 50% of the clock transition and ends when the input signal is reacquired to within a specified accuracy at the output. This specification does not include the track-to-hold settling time.

Aperture Delay is a measure of the track-to-hold switch delay time. It is the difference between the analog input amplifier's signal path delay and the digital track-to-hold switch delay. A positive delay indicates the digital switch delay is larger than the analog amplifier delay.

Aperture Jitter is random variation in the aperture delay. This specification is measured in ps-rms and results in phase noise on the held signal. A large aperture jitter value can manifest itself by degrading the SNR of a sampling ADC.

Droop Rate is the change of the held output voltage as a function of time. The measurement starts immediately after the device switches from the track to hold mode.

Feedthrough Rejection is a measure of the amount of the input signal that "feeds through" to the output while the device is in the hold mode. This specification is usually a function of frequency, with degradation at higher frequencies.

Hold-to-Track Delay is the time from the track command to the point when the output begins changing to acquire a new signal. This delay is included in the SHC605's specified acquisition time.

Pedestal Offset is the error voltage step incurred at the output when the device is switched from the track to hold mode.

Track-to-Hold Settling Time is the time for the track to hold transient to settle to within a specified accuracy.
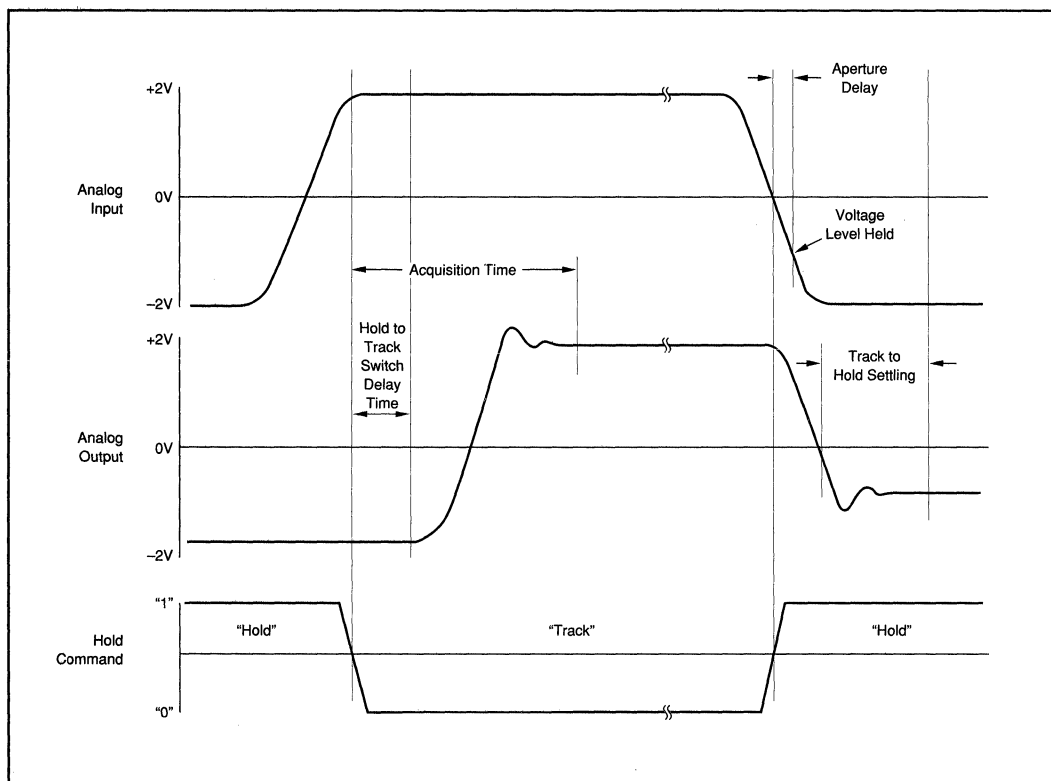
FIGURE 1. SHC605 Timing Diagram.

THEORY OF OPERATION

The SHC605 is a monolithic track-and-hold circuit fabricated on an extremely fast complementary bipolar process. Figure 2 provides a simplified circuit diagram of the SHC605. A conventional two-stage operational amplifier is shown with a standard differential phase compensation scheme sometimes referred to as "doublet compensation." Capacitors C_1 and C_2 compensate the amplifier in the track-mode and hold the analog output signal in the hold-mode. Switching from track to hold is achieved by turning off the amplifier's input stage and isolating C_1 and C_2 from the input signal.

The differential two-stage amplifier architecture of the SHC605 provides many performance advantages over traditional open-loop designs. The use of differential hold capacitors provides a first-order correction for many errors including distortion, pedestal, and droop. A dominant cause of distortion in high-speed amplifiers is the non-linear transistor junction capacitance connected to the hold capacitor(s). This parasitic capacitance varies as the voltage across it changes. Most open-loop track-and-hold circuits have a fixed gain of +1V/V, which means the hold capacitor(s) and parasitic junction capacitance sees the full output signal swing. In the SHC605 the second gain stage attenuates the signal across the capacitors and greatly reduces the nonlinear capacitance. The SHC605's second stage has a unity-gain bandwidth of approximately 250MHz and its open-loop gain rolls off at –20dB/decade. With a 2.5MHz signal, the voltage across the hold capacitors is 100 times less than the output signal, and therefore, the nonlinear capacitance is greatly reduced.

The SHC605's patented architecture provides users with an extremely accurate high-speed *operational* track-and-hold amplifier. All common operational amplifier transfer functions can be realized with the SHC605; i.e. unity-gain, non-inverting gain, inverting gain, and differential gain. These configurations are shown in Figures 3 through 6. In many instances, the SHC605 provides a superior single-chip solution to applications previously requiring two or more devices. As with any conventional voltage feedback op amp, it is important to consider tradeoffs between noise, bandwidth, and settling time for these applications. Refer to Discussion of Performance and Typical Performance Curves for more details.
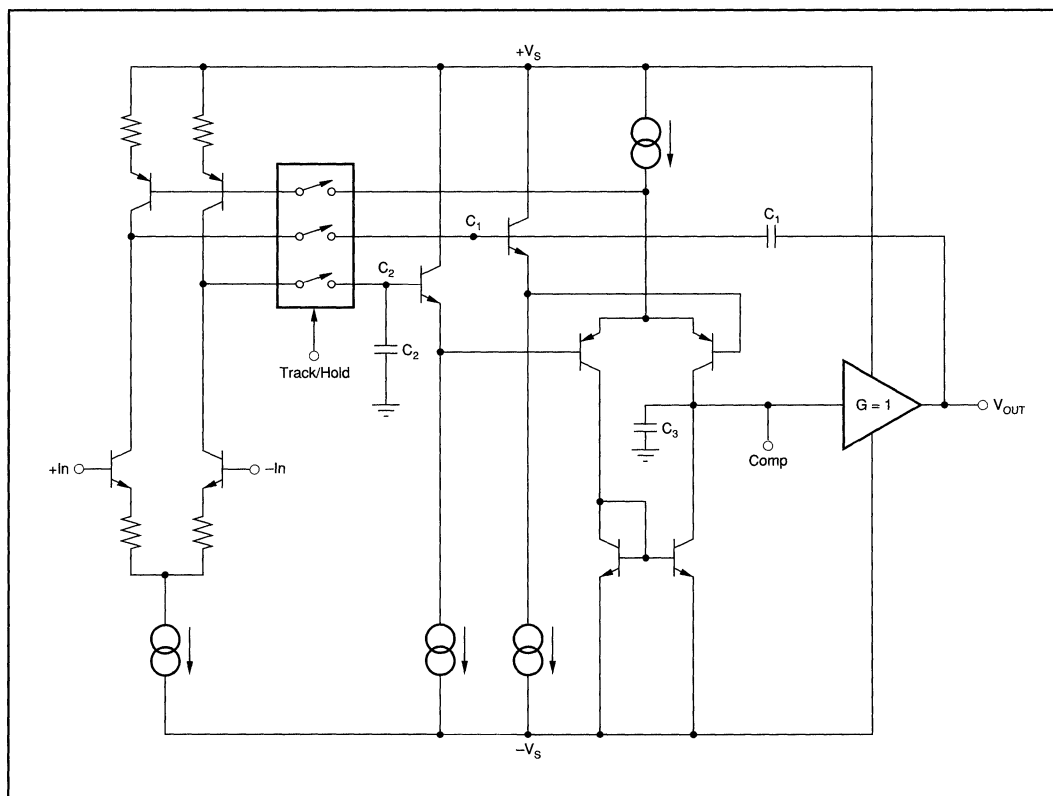
FIGURE 2. SHC605 Simplified Circuit Diagram.

DISCUSSION OF PERFORMANCE

DISTORTION

Hold-mode distortion is an important specification for a track-and-hold amplifier. This is a measure of the accuracy of the amplifier's held output while sampling a sinusoidal input signal. It includes errors from both the switching network and the amplifier's signal path. Hold-mode distortion depends on the input signal's amplitude and frequency as well as the sampling rate. The biggest cause of distortion in the SHC605 is slew-induced nonlinearity; the higher the amplitude of a high frequency input, the higher the distortion. Hold-mode distortion can also result from sampling too fast or not allowing enough acquisition time or track-to-hold settling time. The SHC605 has a typical 0.01% acquisition time of 30ns for a 2V step, and a typical 100µV track-to-hold settling time of 15ns. Thus, for 12-bit accuracy the clock rate should not exceed 22MHz (refer to Typical Performance Curves for details).

NOISE

The SHC605's noise performance is almost completely determined by track-mode noise. This is the noise sampled by the differential hold capacitors during track-mode, which is greater than the noise measured directly at the output. The input referred noise of the SHC605 is 2.5nV/$\sqrt{Hz}$. For unity-gain this corresponds to an output noise of approximately 35µVrms; which is much lower than the typical 150µVrms noise sampled by the hold capacitors. The track-mode noise sampled by the hold capacitors is independent of closed-loop gain, and therefore, the SHC605 can be used with higher closed-loop gain without degrading the overall noise performance.

The SHC605's noise performance is also affected by hold-mode noise and aperture jitter. Hold-mode noise is the result of current noise reacting with the hold capacitors. This noise accumulates on the capacitors at a rate which is proportional to the square root of the hold time. For sample rates above 1MHz this noise is usually insignificant. Aperture jitter describes the random variation in track-to-hold aperture delay, and causes increased hold-mode noise when high slew rate signals are sampled. A differential ECL clock input will provide lower aperture jitter than a single-ended ECL or TTL clock.

CHOOSING THE BEST ARCHITECTURE

The SHC605 is basically a high-speed operational amplifier which can hold its output on command. Unlike traditional high-speed track-and-hold amplifiers, which have fixed gains of +1V/V, the SHC605 can be used with non-inverting, inverting, or differential gains. In many applications, a single SHC605 can be used to solve a problem that previously required two or more devices.

Figures 3 through 6 show the SHC605 connected for non-inverting, inverting, and differential gains. As with any op amp, it is important to consider performance tradeoffs for all of these configurations. For gains less than ±10, the SHC605's track-to-hold settling, pedestal offset, droop, and total hold-mode noise remains constant. However, small-signal bandwidth and acquisition time will be compromised as the closed-loop gain is increased (refer to the Typical Performance Curves for details).
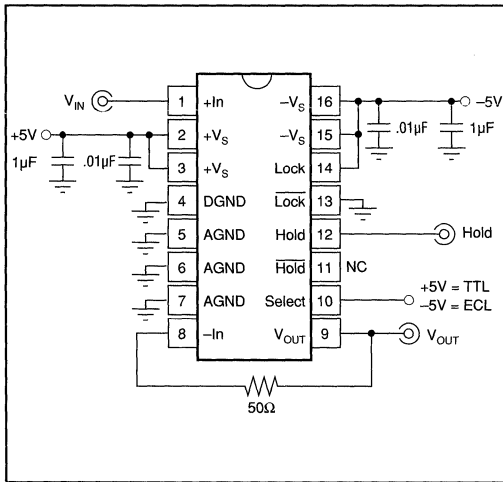
FIGURE 3. Gain of +1 Track-and-Hold Amplifier.
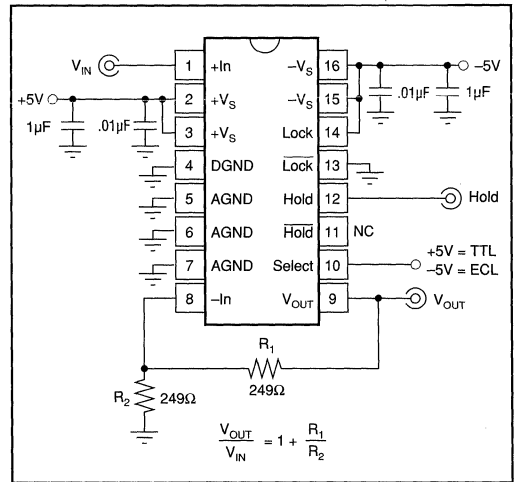
FIGURE 4. Gain of +2 Track-and-Hold Amplifier.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_1}{R_2}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_1}{R_2}$$
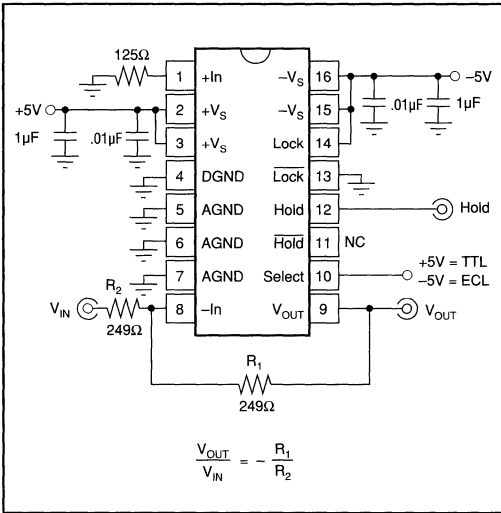
FIGURE 5. Gain of –1 Track-and-Hold Amplifier.

$$V_{OUT} = (V_{+IN} - V_{-IN})\frac{R_1}{R_2}$$
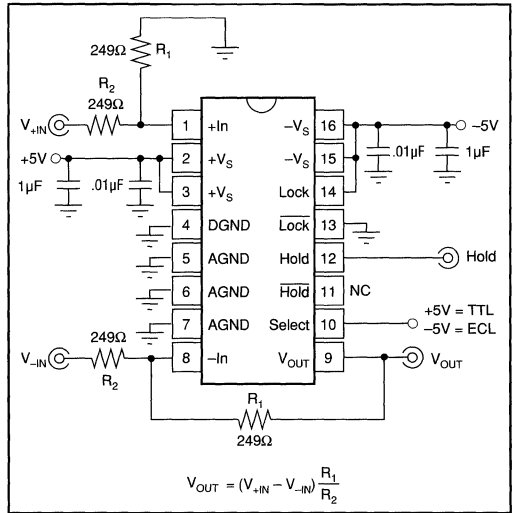
FIGURE 6. Differential Gain of 1 Track-and-Hold Amplifier.

APPLICATIONS INFORMATION

LOGIC COMPATIBILITY/TRACK-TO-HOLD SWITCHING

The SHC605 contains an internal reference circuit which produces either an ECL or TTL logic threshold voltage for single-ended track-to-hold switching. Differential ECL switching is also possible with the SHC605. Table I provides the proper pin connections for all of the possible switching options and the Performance Specifications Table gives the logic levels and input bias currents.

LOGIC TYPE	DGND (Pin 4)	SELECT (Pin 10)	THRESH/HOLD (Pin 11)	HOLD (Pin 12)
Single-ended TTL	GND	+5V	NC	Clock
Single-ended ECL	GND	–5V	NC	Clock
Differential ECL	NC	NC	$\overline{\text{Clock}}$	Clock

TABLE I. Track-to-Hold Switching Options.

LOCKOUT CIRCUITRY

The SHC605 includes additional logic circuitry which allows edge-triggered operation for sampling ADCs. The lockout comparator and Track/Hold comparator form a wired-or mode control circuit as shown in the block diagram on page one. When the Lock input, pin 14, is high with respect to the $\overline{\text{Lock}}$ input, pin 13, the SHC605 is in the Hold-mode regardless of the Hold/$\overline{\text{Hold}}$ inputs. This feature provides more flexibility in the convert command duty cycle and reduces noise resulting from aperture jitter.

Figure 7 shows how the SHC605 lockout circuit can be used with an ECL one-shot to provide an edge-triggered sampling ADC. An ECL threshold voltage is generated on Thresh/$\overline{\text{Hold}}$ (Pin 11), which is connected to $\overline{\text{Lock}}$ (Pin 13), to allow a single-ended lockout input on Lock (Pin 14). The ECL convert command is applied directly to the SHC605. The 10ns delay on the ADCs convert signal is to allow for SHC605 track-to-hold settling. The one-shot's duty cycle

HOLD	LOCK	MODE
0	0	Track
0	1	Hold
1	0	Hold
1	1	Hold
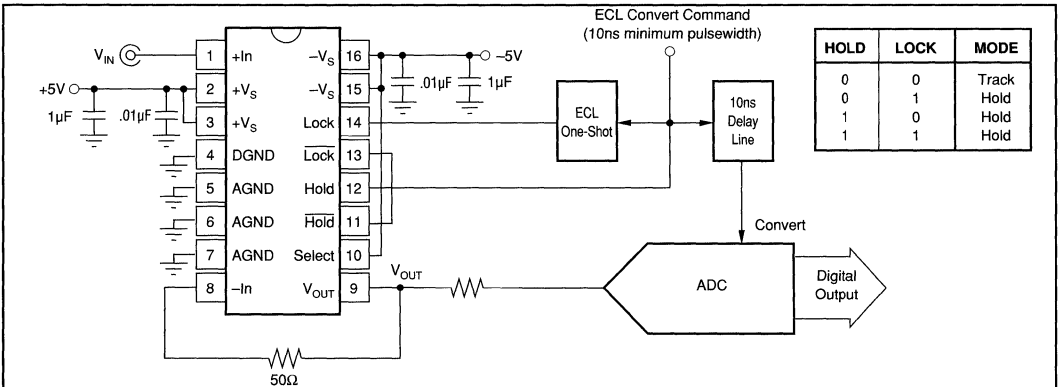
FIGURE 7. Edge-Triggered ADC.

SHC605

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SAMPLE/HOLD AMPLIFIERS

will depend on the ADC conversion time. In this application the one-shot is used to set the critical ADC timing which means the user has more freedom in selecting the convert command duty cycle. Since the convert command is applied directly to the SHC605—instead of after additional logic and clock conditioning—aperture jitter noise is minimized.

OFFSET VOLTAGE ADJUSTMENT

The SHC605's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 8 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input offset voltage errors due to the amplifier's input offset current, which is typically only 0.2µA.

Output Trim Range $\approx +V_{CC} \dfrac{R_2}{R_{TRIM}}$ to $-V_{CC} \dfrac{R_2}{R_{TRIM}}$

NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.
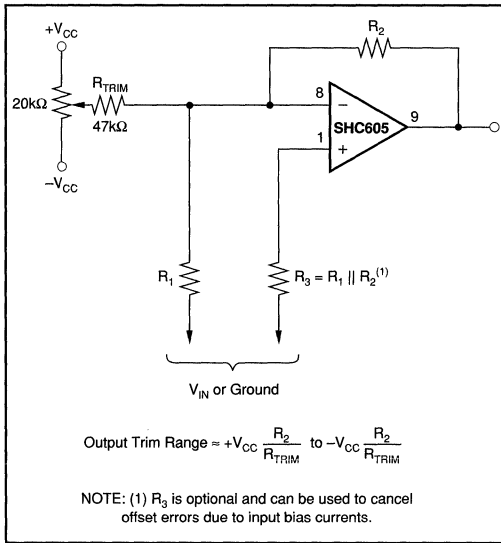
FIGURE 8. Offset Voltage Trim.

INPUT PROTECTION

The SHC605 incorporates on-chip ESD protection diodes as shown in Figure 9. All pins on the SHC605 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability diode current should be externally limited to 10mA or so whenever possible. Static

damage can cause subtle changes in SHC605 input characteristics without necessarily destroying the device. In precision track-and-hold amplifiers, this may cause a noticeable degradation in performance. Therefore, static protection is recommended when handling the SHC605.
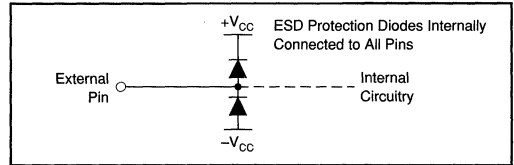
FIGURE 9. Internal ESD Protection.

LAYOUT AND BYPASSING

For best performance, good high speed design techniques must be applied. The component (top) side ground plane should be as large as possible and continuous (not fragmented). Two ounce copper cladding is recommended.

All traces should be as short as possible, especially the output. As much of the ground plane as possible should be removed from around the +In, –In, and V_{OUT} pins to reduce parasitic capacitance and minimize coupling onto the analog signal path.

Power supply decoupling capacitors must be used as shown in Figures 3 through 6. The 0.01µF capacitors should be low inductance surface mount devices and should be connected as close to the SHC605 ±Vs leads as possible (within 30 mils). The 1µF low frequency bypass capacitors should be tantalum capacitors (preferably surface mount) and should be located within one inch of the SHC605. Surface mount resistors are also recommended and should be placed as close to the SHC605 as possible to minimize inductance.

CAPACITIVE LOADS

The SHC605's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 20Ω to 50Ω, in series with the output as shown in
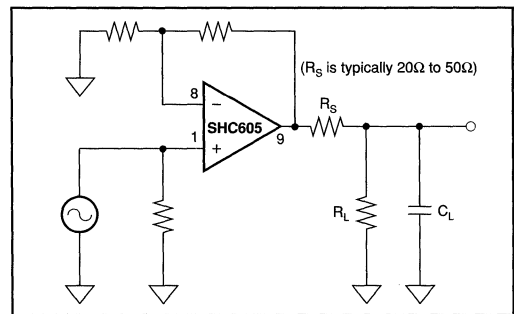
FIGURE 10. Driving Capacitance Load.

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BB

Figure 10. This is particularly important when driving high capacitance loads such as flash A/D converters.

The series resistor, R_S, should be connected as close to the SHC605 as possible. If R_S causes excessive output attenuation, add closed-loop gain to the SHC605 as shown in Figures 4 through 6.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coaxial cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

APPLICATIONS

The SHC605's combination of high speed and accuracy, small size, and low price makes it ideally suited for many data acquisition applications. Its versatile operational amplifier architecture and switching flexibility provides users with an extremely reliable single-chip solution to problems that previously required several components. Figures 11 through 16 show many application circuits using the SHC605. These include high-speed flash and sub-ranging ADC driving, multi-channel simultaneous sampling, DAC deglitching, and peak detecting.
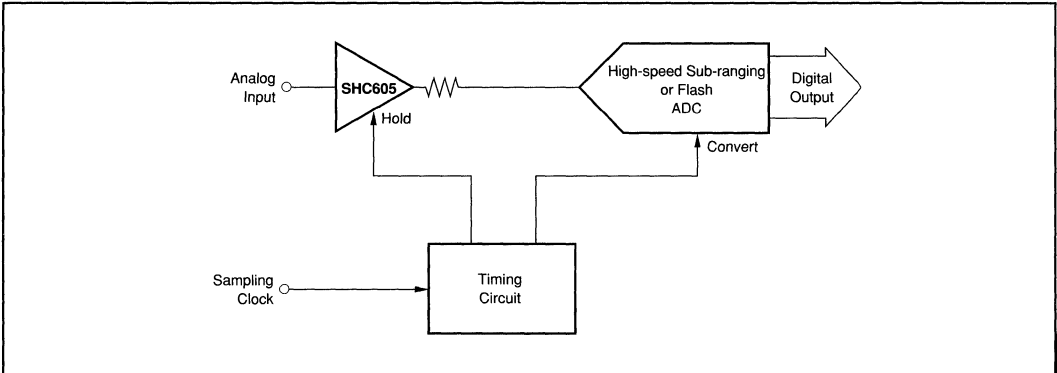
FIGURE 11. Sampling ADC.
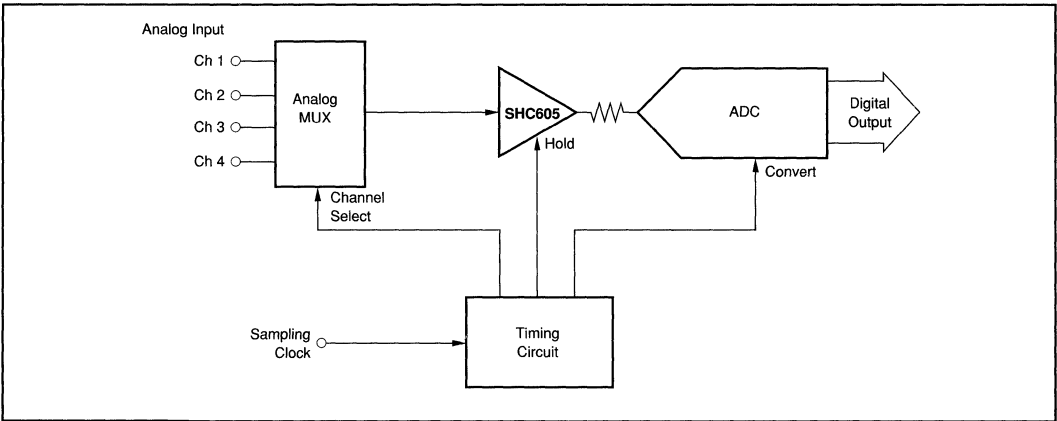
FIGURE 12. Traditional Data Acquisition System.

SHC605

SAMPLE/HOLD AMPLIFIERS

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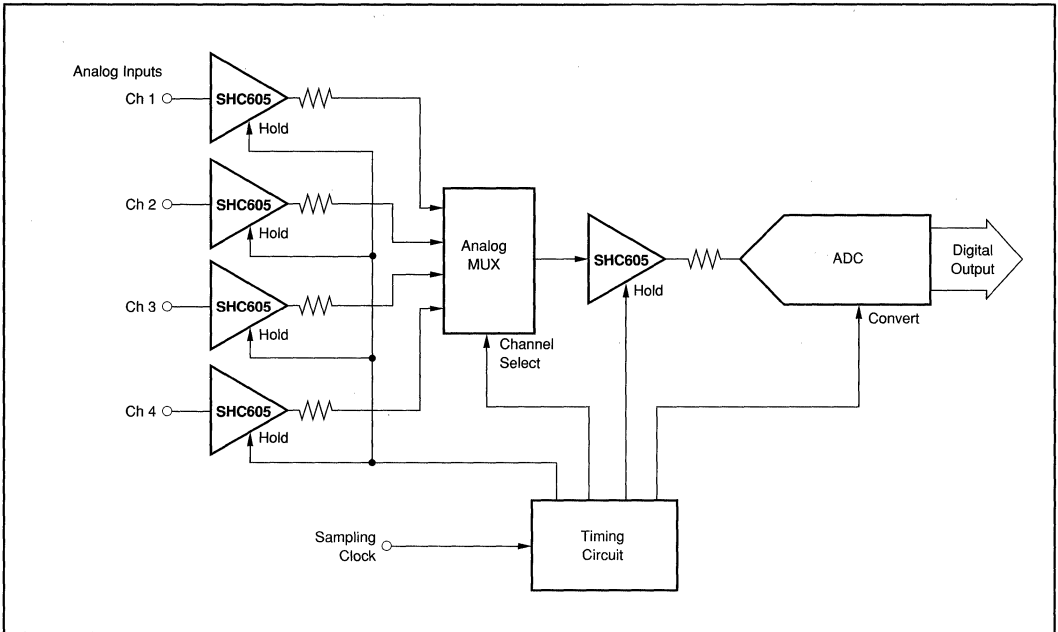
FIGURE 13. Multi-Channel Simultaneous Sampling System.
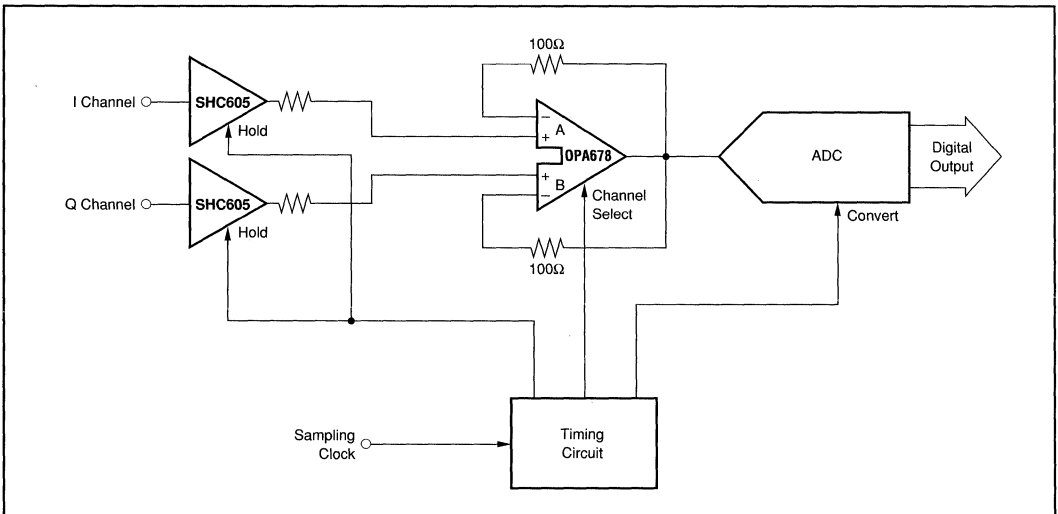
FIGURE 14. I/Q Channel Simultaneous Sampling.
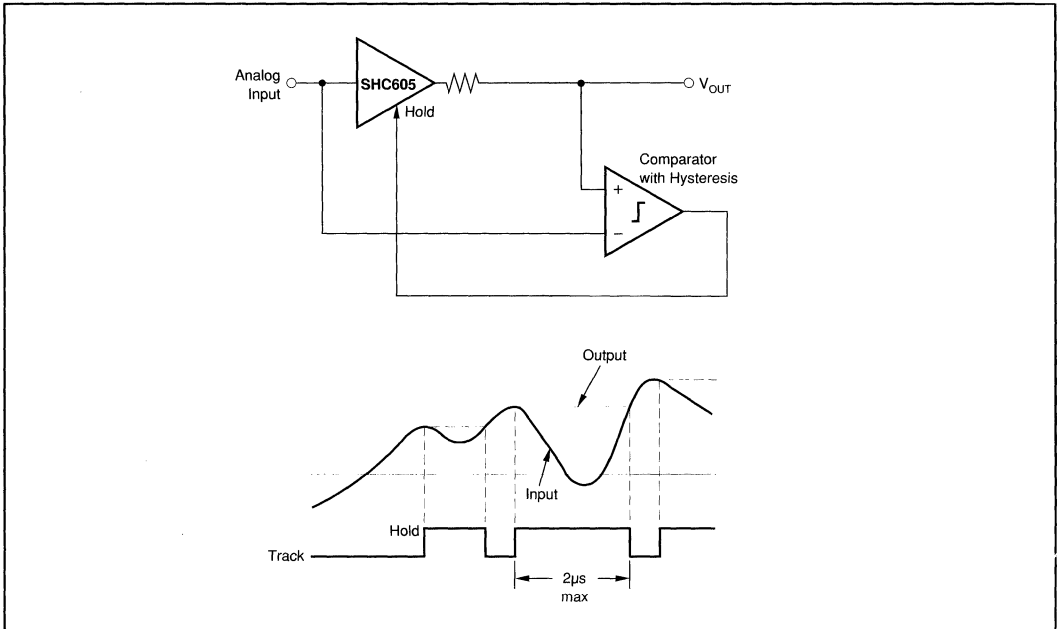
FIGURE 15. High-Speed Peak Detector.
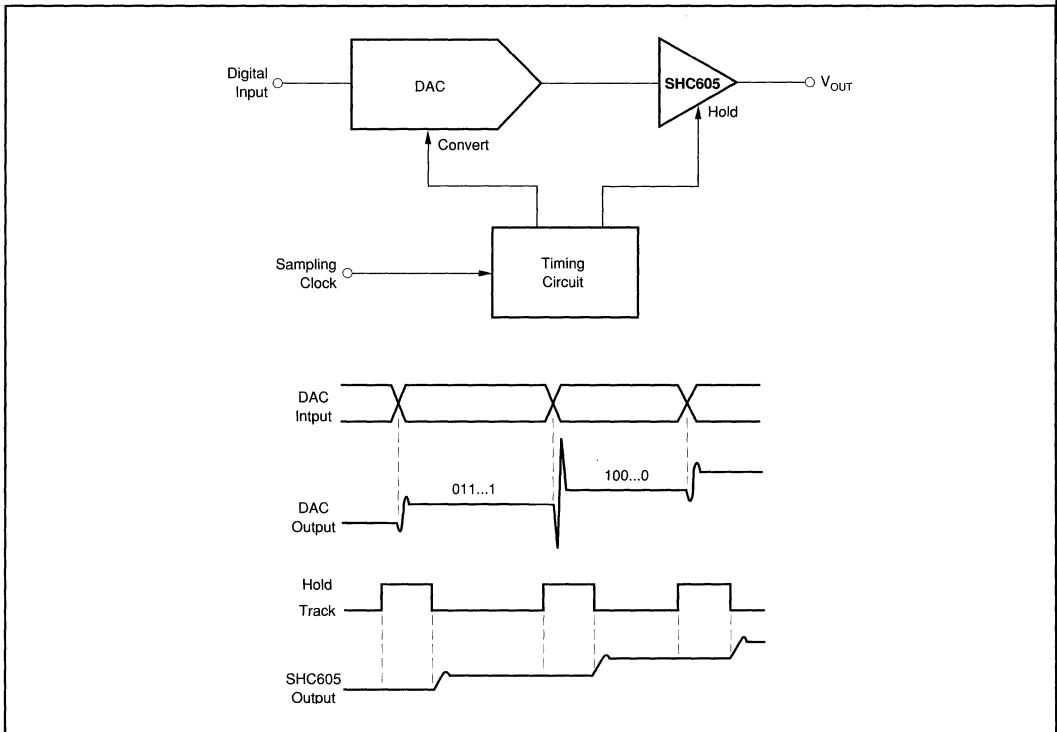
FIGURE 16. DAC Deglitcher.

SHC605

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SAMPLE/HOLD AMPLIFIERS

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SHC615

Wide-Bandwidth,
DC RESTORATION CIRCUIT

FEATURES

● **PROPAGATION DELAY: 2.2ns**
● **BANDWIDTH: OTA: 750MHz**
     Comparator: 280MHz
● **LOW INPUT BIAS CURRENT: –0.3μA**
● **SAMPLE/HOLD**
  SWITCHING TRANSIENTS:+1/–7mV
● **SAMPLE/HOLD**
  FEEDTHROUGH REJECTION: 100dB
● **CHARGE INJECTION: 40fC**
● **HOLD COMMAND DELAY TIME: 3.8ns**
● **TTL/CMOS HOLD CONTROL**

APPLICATIONS

● **BROADCAST/HDTV EQUIPMENT**
● **TELECOMMUNICATIONS EQUIPMENT**
● **HIGH-SPEED DATA ACQUISITION**
● **CAD MONITORS/CCD IMAGE**
  PROCESSING
● **NANO SECOND PULSE INTEGRATOR/PEAK**
  DETECTORS
● **PULSE CODE MODULATOR/**
  DEMODULATOR
● **COMPLETE VIDEO DC LEVEL**
  RESTORATION
● **SAMPLE/HOLD AMPLIFIER**

DESCRIPTION

The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low-frequency hum suppression of wideband amplifiers or buffers. Although it was designed to stabilize the performance of video signals, the circuit can also be used as a sample and hold amplifier, high-speed integrator, or peak detector for nano second pulses. A wide-band Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast and precise sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal volt-

age-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nano seconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is packaged in SO-14 surface mount packages and 14-pin plastic DIPs, and is specified over the extended temperature range of –40°C to +85°C.

PDS-1214A

BURR - BROWN®

DC SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$, $R_Q = 300\Omega$, $R_{IN} = 150\Omega$ and $T_A = +25°C$, unless otherwise specified.

| PARAMETER | CONDITIONS | SHC615AP, AU | | | UNITS |
		MIN	TYP	MAX	
OTA					
OFFSET VOLTAGE					
Initial			8	±40	mV
vs Temperature			40		µV/°C
vs Supply (tracking)	$V_{CC} = \pm 4.5V$ to ±5.5V	50	55		dB
B-INPUT BIAS CURRENT					
Initial			−0.3	±0.9	µA
vs Temperature			1		nA/°C
C-OUTPUT BIAS CURRENT					
Initial		−200	−77	+100	µA
B-INPUT IMPEDANCE			4.4		MΩ
INPUT NOISE					
Voltage Noise Density, B-to-E	$f_{OUT} = 100kHz$ to 100MHz		2.2		nV/$\sqrt{Hz}$
Voltage Noise Density, B-to-C	$f_{OUT} = 100kHz$ to 100MHz		4.5		nV/$\sqrt{Hz}$
INPUT VOLTAGE RANGE			±3.4		V
OUTPUT					
Output Voltage Compliance			±3.2		V
C-Current Output		±18	±20		mA
E-Current Output		±18	±20		mA
C-Output Impedance			0.5		MΩ
E-Output Impedance			12		Ω
Open-Loop Gain			96		dB
TRANSCONDUCTANCE	Small Signal, <200mV		70		mA/V

SHC615

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SAMPLE/HOLD AMPLIFIERS

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DC SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = \pm5VDC$, $R_{LOAD} = 1k\Omega$, $R_Q = 300\Omega$, and $T_A = +25°C$, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
COMPARATOR					
INPUT BIAS CURRENT					
Initial			1.0	±5	μA
vs Temperature			−2.3		nA/°C
C-OUTPUT BIAS CURRENT					
Initial			±4	±25	μA
vs Temperature			±13		nA/°C
INPUT IMPEDANCE					
Input Impedance			0.2		MΩ
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 100kHz to 100MHz		5		nV/√Hz
INPUT VOLTAGE RANGE					
Input Voltage Range			±3.0		V
Common-Mode Input Range			±4.0		V
OUTPUT					
Output Voltage Compliance			±3.5		V
C-Current Output		±3.5	±4.0		mA
C-Output Impedance			620 ‖ 2		kΩ ‖ pF
Open-Loop Gain			83		dB
TRANSCONDUCTANCE					
Transconductance			22		mA/V
HOLD CONTROL					
Logic 1 Voltage		+2		$+V_{CC}$ +0.6	V
Logic 0 Voltage		0		0.8	V
Logic 1 Current	V Hold Control = 5.0V		1		μA
Logic 0 Current	V Hold Control = 0.8V		0.05		μA
TRANSFER CHARACTERISTICS					
Charge Injection	Track-To-Hold		40		fC
Feedthrough Rejection	Hold Mode		−100		dB
COMPLETE SHC615					
POWER SUPPLY					
Rated Voltage			±5		VDC
Derated Performance		±4.5		±5.5	VDC
Quiescent Current	Programmable (Useful Range)	±3	±14	±36	mA
Rejection Rate			−70		dB
TEMPERATURE RANGE					
Operating		−40		+85	°C
Storage		−40		+125	°C

AC SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_Q = 300\Omega$, and $T_A = +25°C$, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
FREQUENCY DOMAIN					
OTA					
LARGE-SIGNAL BANDWIDTH	$V_{OUT} = 5.0Vp\text{-}p$		430		MHz
(–3dB), (B-to-E)	$V_{OUT} = 2.8Vp\text{-}p$		540		MHz
	$V_{OUT} = 1.4Vp\text{-}p$		620		MHz
SMALL-SIGNAL BANDWIDTH B-TO-E	$V_{OUT} = 0.2Vp\text{-}p$		520		MHz
DIFFERENTIAL GAIN (B-TO-E)	$f = 4.43MHz$, $V_{OUT} = 0.7Vp\text{-}p$,				
	$R_L = 150\Omega$		1.8		%
	$R_L = 500\Omega$		0.1		%
DIFFERENTIAL PHASE	$f = 4.43MHz$, $V_{OUT} = 0.7Vp\text{-}p$,				
	$R_L = 150\Omega$		0.07		°
(B-TO-E)	$R_L = 500\Omega$		0.01		°
HARMONIC DISTORTION (B-TO-E)	$f = 30MHz$, $V_{OUT} = 1.4Vp\text{-}p$				
Second Harmonic			–50		dBc
Third Harmonic			–46		dBc
LARGE SIGNAL BANDWIDTH	$V_{OUT} = 5.0Vp\text{-}p$		250		MHz
(–3dB), (B-to-C)	$V_{OUT} = 2.8Vp\text{-}p$		580		MHz
	$V_{OUT} = 1.4Vp\text{-}p$		750		MHz
SMALL SIGNAL BANDWIDTH					
B-to-C	$V_{OUT} = 0.2Vp\text{-}p$		680		MHz
COMPARATOR	Sample Mode				
BANDWIDTH	$I_{OUT} = 4mAp\text{-}p$		240		MHz
(–3dB)	$I_{OUT} = 2mAp\text{-}p$		270		MHz
	$I_{OUT} = 1mAp\text{-}p$		280		MHz
TIME DOMAIN					
OTA					
RISE TIME	2Vp-p Step, 10% to 90%				
	B-to-E		1.1		ns
	B-to-C		1.2		ns
SLEW RATE	2Vp-p, B-to-E		1800		V/μs
	B-to-C		1700		V/μs
	5Vp-p, B-to-E		3300		V/μs
	B-to-C		3000		V/μs
COMPARATOR					
RISE TIME	10% to 90%, $R_L = 50\Omega$, $I_{OUT} = \pm 2mA$				
(Sample Mode)	$C_{LOAD} = 1pF$		2.5		ns
SLEW RATE	10% to 90%, $R_L = 50\Omega$, $I_{OUT} = \pm 2mA$				
(Sample Mode)	$C_{LOAD} = 1pF$		0.95		mA/ns
DYNAMIC CHARACTERISTICS					
Propagation Delay Time	t_{PDH}, $V_{OD} = 200mV$		2.2		ns
Propagation Delay Time	t_{PDL}, $V_{OD} = 200mV$		2.15		ns
Delay Time	Sample-to-Hold		3.8		ns
	Hold-to-Sample		3.0		ns

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SAMPLE/HOLD AMPLIFIERS

DICE INFORMATION

SHC615 DIE TOPOGRAPHY

DIE PAD	FUNCTION
1	I_Q Adjust
2	OTA-Emitter
3	OTA-Base
4	C_{HOLD}
5	–5V Supply, Analog
6	–5V Supply, Digital
7	Hold Control
8	Ground
9	S/H In+
10	S/H In–
11	I_{OUT}, OTA-Collector
12	+5V Supply, Analog
13	+5V Supply, Digital

Substrate Bias: Negative Supply.
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	73 x 81, ±5	1.86 x 2.06, ±0.13
Die Thickness	14, ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (±V_{CC}) .... ±6VDC
Input Voltage[1] .... ±V_{CC} ±0.7V
Operating Temperature .... –40°C to +85°C
Storage Temperature .... –40°C to +125°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
Hold Control .... –0.5V to +V_{CC} +0.7V

NOTE: (1) Inputs are internally diode-clamped to ±V_{CC}.

PIN CONFIGURATION

Top View   **SO/DIP**

I_Q Adjust	1	14	NC
Emitter, E	2	13	+V_{CC}
Base, B	3	12	I_{OUT}, Collector, C
C_{HOLD}	4	11	S/H In–
–V_{CC}	5	10	S/H In+
NC	6	9	Ground
Hold Control	7	8	NC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC615AP	Plastic 14-Pin DIP	010
SHC615AU	SO 14-Pin Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.
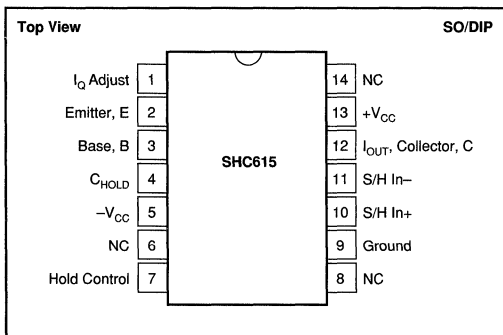
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
SHC615AP	Plastic 14-Pin DIP	–40°C to +85°C
SHC615AU	SO 14-Pin Surface Mount	–40°C to +85°C

BLOCK DIAGRAM

TYPICAL PERFORMANCE CURVES

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

SHC615 TOTAL QUIESCENT CURRENT vs R_Q

Total Quiescent Current, I_Q (mA)

R_Q (Ω)

TOTAL QUIESCENT CURRENT vs TEMPERATURE

Total Quiescent Current, I_Q (Normalized)

Temperature (C°)

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

OTA B-INPUT BIAS CURRENT vs TEMPERATURE

OTA-B Input Bias Current (µA)

Temperature (C°)

OTA-B INPUT OFFSET VOLTAGE vs TEMPERATURE

OTA-B Input Offset Voltage (mV)

$R_E = 100\Omega$

Temperature (C°)

OTA-B INPUT RESISTANCE vs TOTAL QUIESCENT CURRENT

OTA-B Input Resistance (MΩ)

Total Quiescent Current, I_Q (mA)

OTA-E OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT

OTA-E Output Resistance (Ω)

Total Quiescent Current, I_Q (mA)

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SAMPLE/HOLD AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

OTA-C OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT

OTA-C OUTPUT BIAS CURRENT vs TEMPERATURE

OTA TRANSFER CHARACTERISTICS vs INPUT VOLTAGE

OTA TRANSFER CHARACTERISTIC vs INPUT VOLTAGE

OTA TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT

OTA-TRANSCONDUCTANCE vs FREQUENCY

TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm 5V$ unless otherwise noted.

OTA-E VOLTAGE NOISE SPECTRAL DENSITY

2.2nV/√Hz

OTA-E FREQUENCY RESPONSE

5Vp-p
2.8Vp-p
1.4Vp-p
0.6Vp-p
0.2Vp-p

OTA-E SMALL SIGNAL PULSE RESPONSE

$R_{IN} = 150\Omega$, $R_L = 100\Omega$, $V_{IN} = 200mVp-p$,
$t_{RISE} = t_{FALL} = 1.5ns$ (Generator)

OTA-E LARGE SIGNAL PULSE RESPONSE

$R_{IN} = 150\Omega$, $R_L = 100\Omega$, $V_{IN} = 4Vp-p$,
$t_{RISE} = t_{FALL} = 1.5ns$ (Generator)

OTA-C VOLTAGE NOISE SPECTRAL DENSITY

4.5nV/√Hz

OTA-C FREQUENCY RESPONSE

5Vp-p
2.8Vp-p
1.4Vp-p
0.6Vp-p
0.2Vp-p

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SAMPLE/HOLD AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$R_O = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

OTA-C SMALL SIGNAL PULSE RESPONSE

$R_{IN} = 150\Omega$, $R_E = 100\Omega$, $R_C = 100\Omega$,
$V_{IN} = 200mVp-p$, $t_{RISE} = t_{FALL} = 1.5ns$ (Generator)

OTA-C LARGE SIGNAL PULSE RESPONSE

$R_{IN} = 150\Omega$, $R_E = 100\Omega$, $R_C = 100\Omega$,
$V_{IN} = 4Vp-p$, $t_{RISE} = t_{FALL} = 1.5ns$ (Generator)

OTA-E HARMONIC DISTORTION vs FREQUENCY

$R_E = 100\Omega$

2f

3f

OTA-C HARMONIC DISTORTION vs FREQUENCY

$V_{OUT} = 1.4Vp$
$R_E = R_C = 100\Omega$

2f

3f

SAMPLING COMPARATOR

INPUT BIAS CURRENT vs TEMPERATURE

S/H In+

S/H In–

OUTPUT BIAS CURRENT vs TEMPERATURE

TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

INPUT RESISTANCE vs TOTAL QUIESCENT CURRENT

TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT

TRANSFER CHARACTERISTICS

TRANSCONDUCTANCE vs INPUT VOLTAGE

COMMON MODE REJECTION vs FREQUENCY

PROPAGATION DELAY vs TOTAL QUIESCENT CURRENT

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SAMPLE/HOLD AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

PROPAGATION DELAY vs OVERDRIVE

PROPAGATION DELAY TIME vs TEMPERATURE

PROPAGATION DELAY vs LOAD CAPACITANCE

PROPAGATION DELAY vs SLEW RATE

COMPARATOR RESPONSE TO A 2ns ANALOG INPUT PULSE

COMPARATOR RESPONSE TO A 10ns ANALOG INPUT PULSE

TYPICAL PERFORMANCE CURVES (CONT)

$R_Q = 300\Omega$, $T_A = +25°C$, $V_{CC} = \pm5V$ unless otherwise noted.

SWITCHING TRANSIENTS

SWITCHING TRANSIENTS TEST CIRCUITS

FEEDTHROUGH REJECTION vs FREQUENCY
(Off-Isolation)

BANDWIDTH vs OUTPUT CURRENT SWING

SLEW RATE vs TOTAL QUIESCENT CURRENT

HOLD COMMAND DELAY TIME

SHC615

SAMPLE/HOLD AMPLIFIERS

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DISCUSSION OF PERFORMANCE

The SHC615, which contains a wide-band Operational Transconductance Amplifier and a fast sampling comparator, represents a complete subsystem for very fast and precise DC restoration, offset clamping and correction to GND or to an adjustable reference voltage, and low frequency hum suppression of wideband operational or buffer amplifiers.

Although the IC was designed to improve or stabilize the performance of complex, wide-band video signals, it can also be used as a sample and hold amplifier, high-speed integrator, peak detector for nanosecond pulses, or demodulator or modulator for pulse code transmission systems. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and a fast and precise sampling comparator set a new standard for high-speed sampling applications.

Both can be used as stand-alone circuits or combined to create more complex signal processing stages like sample and hold amplifiers. The SHC615 simplifies the design of input amplifiers with high hum suppression, clamping or DC-restoration stages in professional broadcast equipment, high-resolution CAD monitors and information terminals, signal processing stages for the energy and peak value of small and fast nanoseconds pulses, and eases the design of high-speed data acquisition systems behind a CCD sensor or in front of an analog-to-digital converter.

An external resistor, R_Q, allows the user to set the quiescent current. R_Q is connected from Pin 1 (I_Q adjust) to $-V_{CC}$. It determines the operating currents of both the OTA and comparator sections and controls the bandwidth and AC behavior as well as the transconductance of both sections. Besides the quiescent current setting feature, the Proportional-to-Absolute-Temperature (PTAT) supply increases the quiescent current vs temperature and keeps it constant over a wide range of input voltages. This variation holds the transconductance g_m of the OTA and comparator relatively constant vs temperature. The circuit parameters listed in the specification table are measured with R_Q set to 300Ω, giving a nominal quiescent current at ±14mA. The circuit can be totally switched-off with a current flowing into Pin 1.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

SECTION AND OVERVIEW

The symbol for the OTA section is similar to that of a bipolar transistor, and the self-based OTA can be viewed as a quasi-ideal transistor or as a voltage-controlled current source. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor, also, is a voltage-controlled current source. Like a transistor, it has three terminals: a high-impedance input (base) optimized for a low input bias current of 0.3µA, a low-impedance input/output (emitter), and the high-impedance current output (collector).

The OTA consists of a complementary buffer amplifier and a subsequent complementary current mirror. The buffer amplifier features a Darlington output stage and the current mirror has a cascoded output. The addition of this cascode circuitry increases the current source output resistance to 1MΩ and the open-loop gain to typical 96dB. Both features improve the OTAs linearity and drive capabilities. Any bipolar input voltage at the high impedance base has the same polarity and signal level at the low impedance buffer or emitter output. For the open-loop diagrams the emitter is connected to GND and then the collector current is determined by the product voltage between base and emitter times the transconductance. In application circuits (Figure 2b.), a resistor R_E between emitter and GND is used to set the OTA transfer characteristics. The following formulas describe the most important relationships. r_E is the output impedance of the buffer amplifier (emitter) or the reciprocal of the OTA transconductance. Above ±5mA, collector current, I_C, will be slightly less than indicated by the formula.

$$I_C = \frac{V_{IN}}{r_E + R_E} \qquad R_E = \frac{V_{IN}}{I_C} - r_E$$

The R_E resistor may be bypassed by a relatively large capacitor to maintain high AC gain. The parallel combination of R_E and this large capacitor form a high pass filter enhancing the high frequency gain. Other cases may require a RC compensation network parallel to R_E to optimize the high-frequency response. The full power bandwidth measured at the emitter achieves 620MHz. The frequency response of the collector is directly related to the resistor's value between collector and GND; it decreases with increasing resistor values, because it forms a low-pass network with the OTA C-output capacitance.

Figure 1 shows a simplified block and circuit diagram of the SHC615 OTA. Both the emitter and the collector outputs offer a drive capability of ±20mA for driving low impedance lines or inputs. Connecting the collector to the emitter in a direct-feedback buffer configuration increases the drive capability to ±40mA. The emitter output is not current-limited or-protected. Momentary shorts to GND should be avoided, but are unlikely to cause permanent damage.

While the OTA's function and labeling looks similar to that of transistors, it offers essential distinctive differences and improvements: 1) The collector current flows out of the C terminal for a positive B-to-E input voltage and into it for negative voltages; 2) A common emitter amplifier operates in non-inverting mode while the common base operates in inverting mode; 3) The OTA is far more linear than a bipolar transistor; 4) The transconductance can be adjusted with an external resistor; 5) Due to the PTAT biasing characteristic the quiescent current increases as shown in the typical performance curve vs temperature and keeps the AC performance constant; 6) The OTA is self-biased and bipolar; and, 7) The output current is zero for zero differential input voltages. AC inputs centered at zero produce an output current centered at zero.
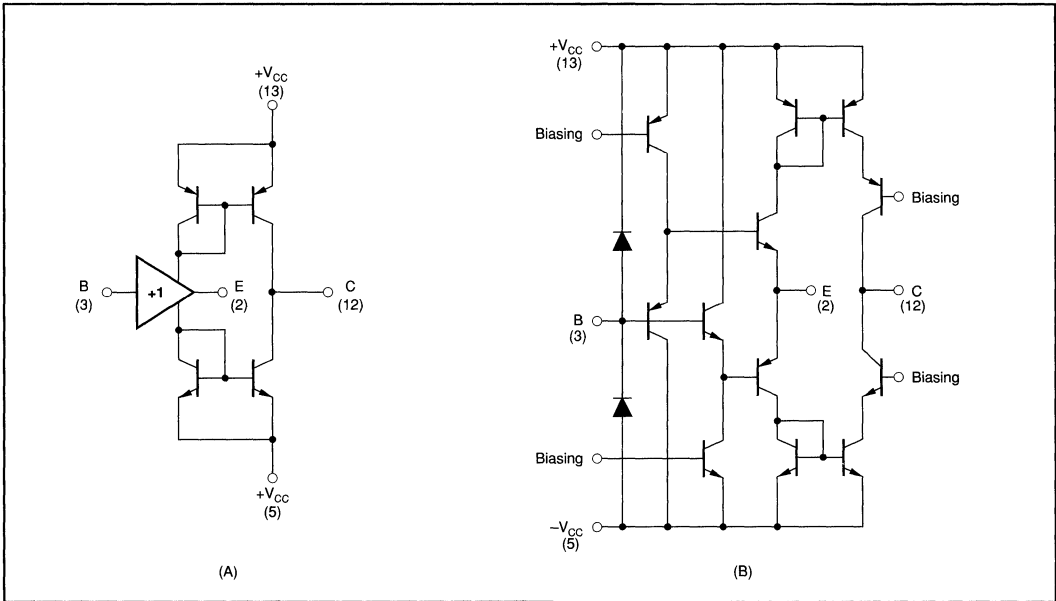
FIGURE 1. a) Simplified Block; and, b) Circuit Diagram of the OTA Section.
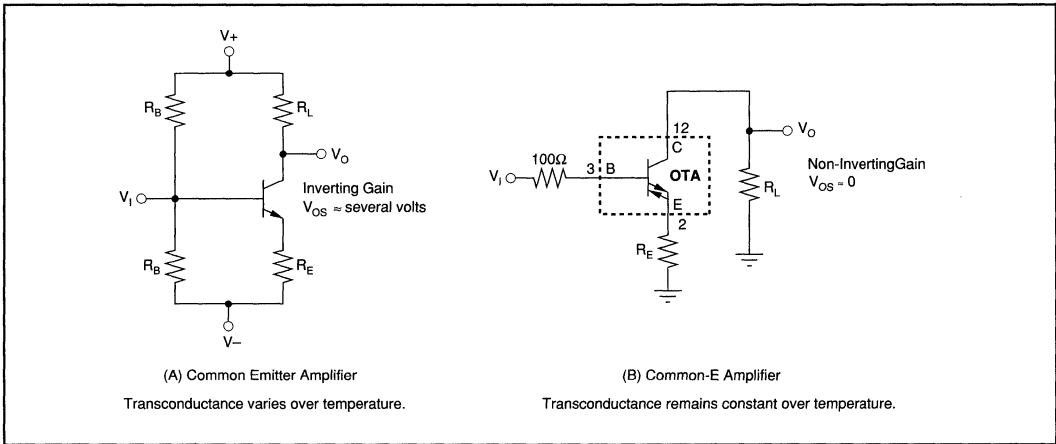
FIGURE 2. a) Common Emitter Amplifier Using a Discrete Transistor; b) Common-E Amplifier Using the OTA Portion of the SHC615.

BASIC APPLICATIONS CIRCUITS

Most application circuits for the OTA section consist of a few basic types which are best understood by analogy to discrete transistor circuits. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C (See Figures 2, 3 and 4). Figure 2 shows the OTA connected as

a Common-E amplifier which is equivalent to a common emitter transistor amplifier. Input and output can be ground referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting.

Figure 3 shows the common-B amplifier. This configuration produces an inverting gain, and the input is low-impedance. When a high impedance input is needed, it can be created by inserting a buffer amplifier like BUF600 in series.

SHC615

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SAMPLE/HOLD AMPLIFIERS
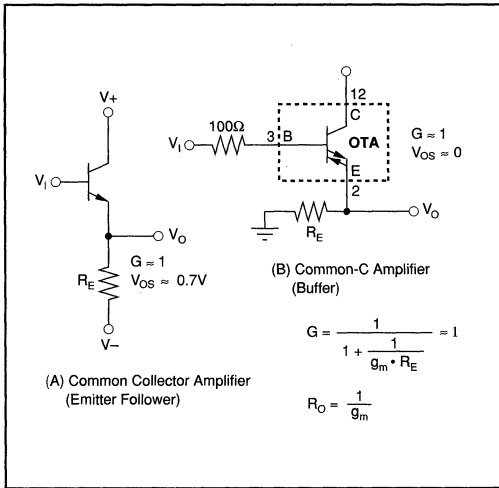
FIGURE 3. a) Common Collector Amplifier Using a Discrete Transistor; b) Common-C Amplifier Using the OTA Portion of the SHC615.

FIGURE 4. a) Common Base Amplifier Using a Discrete Transistor; b) Common-B Amplifier Using the OTA Portion of the SHC615.

SAMPLING COMPARATOR

The SHC615 sampling comparator features a very short 2.2ns propagation delay and utilizes a new switching circuit architecture to achieve new levels of high-speed precision.

It provides high impedance inverting and non-inverting inputs, a high-impedance current source output and a TTL-CMOS-compatible Hold Control Input.

The sampling comparator consists of an operational transconductance amplifier (OTA), a buffer amplifier, and a subsequent switching circuit. The OTA and buffer amplifier are directly tied together at the buffer outputs to provide the two identical high-impedance inputs and high open-loop transconductance. Even a small differential input voltage multiplied with the high transconductance results in an output current—positive or negative—depending upon the input polarity. This is similar to the low or high status of a convential comparator. The current source output features high output impedance, output bias compensation, and is optimized for charging a capacitor in DC restoration, ns-second integrators, peak detectors and S/H circuits. The typical comparator output current is ±4mA and the output bias current is minimized to typically 4µA in the sampling mode.

This innovative circuit achieves the slew rate representatives of an open-loop design. In addition, the acquisition slew current for a hold or storage capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

The switching circuits in the SHC615 use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, reduced power supply and analog switching noise. Sample-to-hold peak switching is 40fC.
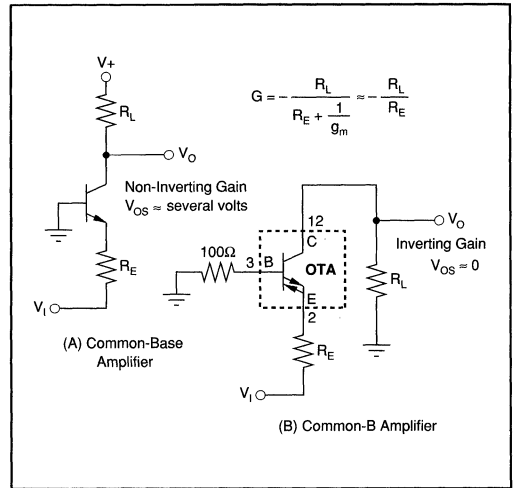
The additional offset voltage or switching transient induced on a capacitor at the current source output by the switching charge can be determined by the following formula:

$$\text{Offset(V)} = \frac{\text{Charge(pC)}}{C_H \text{ Total(pF)}}$$

The switching stage input is insensitive to the low slew rate performance of the hold control command and compatible with TTL/CMOS logic levels. With a TTL logic high, the comparator is active, compares the two input voltages with each other and varies the output current accordingly. With a TTL logic low, the comparator output is switched off.

APPLICATION INFORMATION

The SHC615 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the SHC615 are protected with internal diode clamps as shown in Figure 1. These protection diodes can safely conduct 10mA, continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V, the input signal current must be limited.

BASIC CONNECTIONS

Figure 6 shows the basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See "Circuit Layout" at the end of the applications discussion for further suggestions on layout.

If the high speed TTL-hold command signal goes negative due to reflections for AC-coupling, the hold control input must be protected by an external reverse bias diode to ground as shown in Figure 6.

CIRCUIT LAYOUT

The high-frequency performance of the SHC615 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute requirements. Oscillations, ringing, poor bandwidth, poor settling, and peaking are all typical problems that

plague high-speed components when they are used incorrectly.

• Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2μF); parallel 470pF and/or 10nF ceramic chip capacitors may be added if desired. Surface mount types are recommended because of their low lead inductance. Supply bypassing is extremely critical at high frequencies and when driving high current loads.

• PC board traces for power lines should be wide to reduce impedance or inductance.
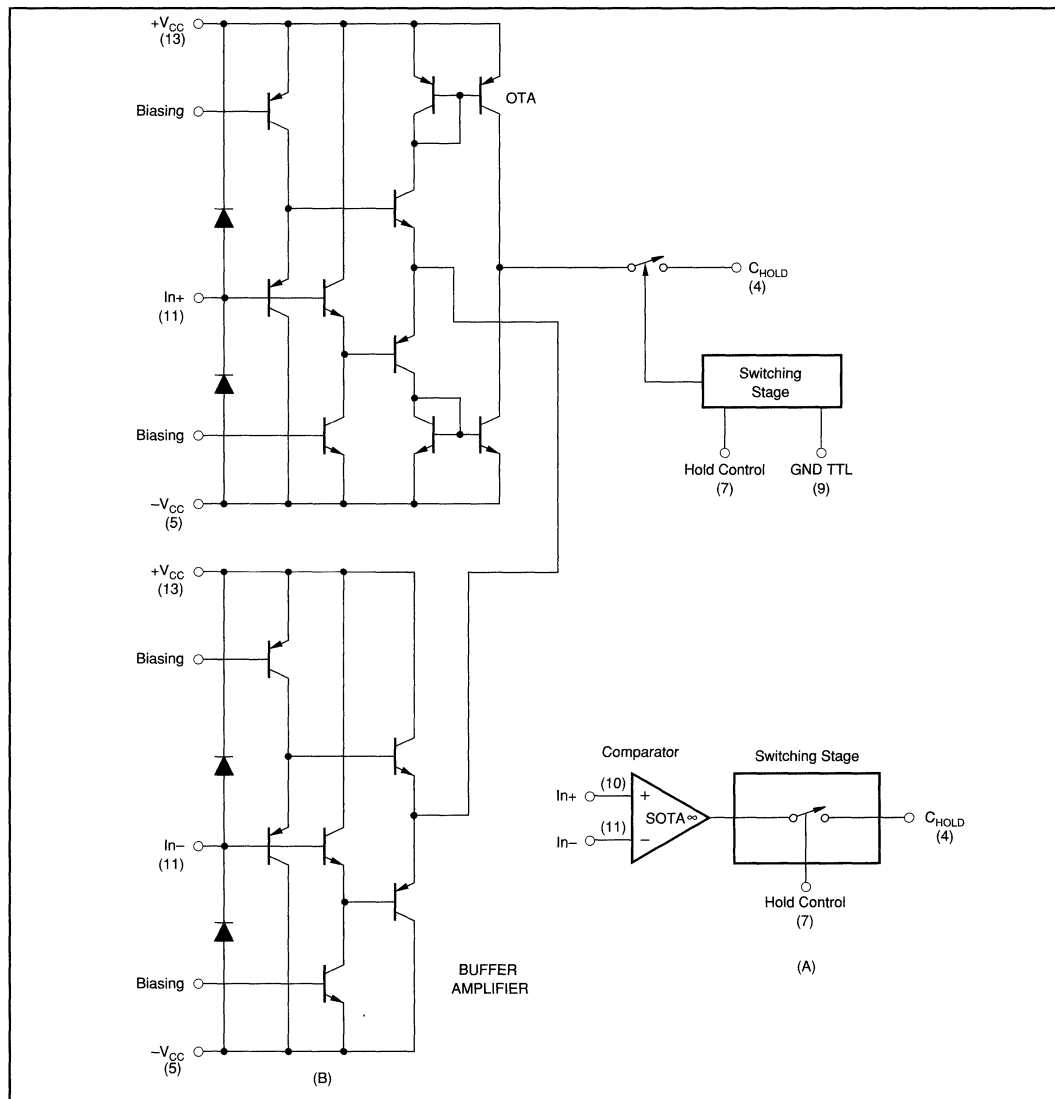
FIGURE 5. a) Simplified Block Diagram; and, b) Circuit Diagram of the Sampling Comparator which Includes the Sampling Operational Transconductance Amplifier (SOTA) and the Switching Stage.

- Make short, low-inductance traces. The entire physical circuit should be as small as possible.

- Use a low-impedance ground plane on the component side to ensure that a low-impedance ground is available throughout the layout.

- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input terminals.

- Sockets are not recommended since they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile sockets.

- Use low-inductance, surface-mount components. Circuits using all surface-mount components with the SHC615 will offer the best AC performance.

- A resistor of 100 to 250Ω in series with the high-impedance inputs is recommended to reduce peaking.

- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

- Terminate transmission line loads. Unterminated lines, such as box cables, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

- Protect the hold control input with an external diode if necessary.
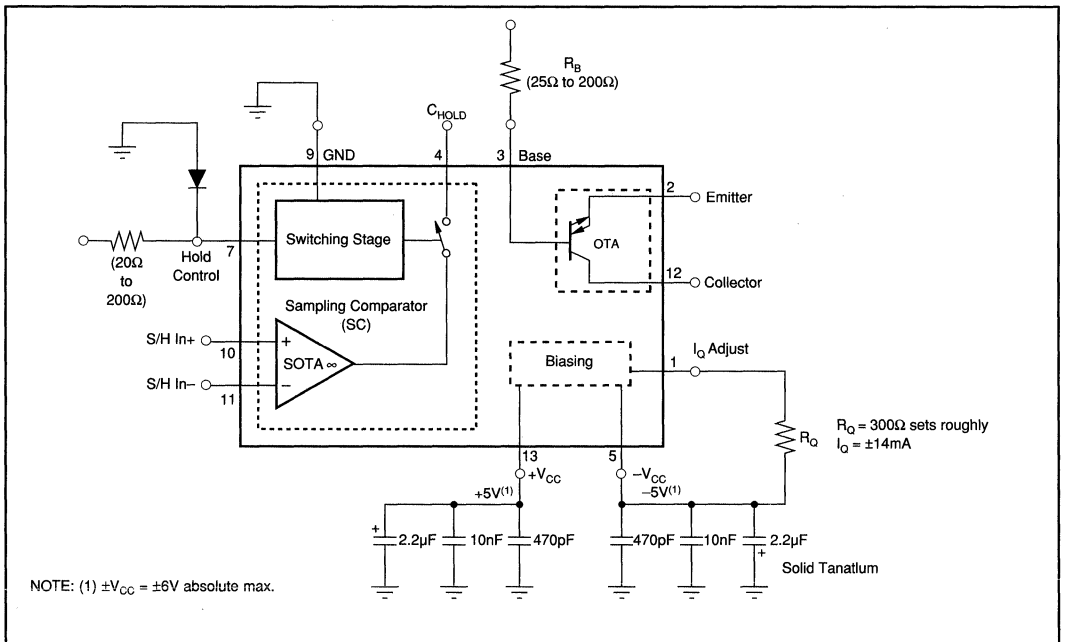
FIGURE 6. Basic Connections

TYPICAL APPLICATIONS
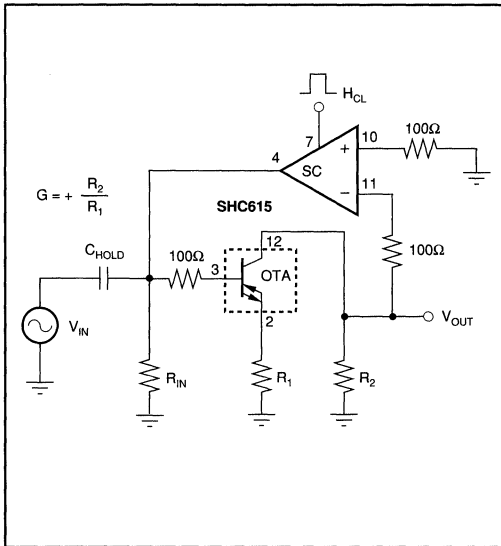
FIGURE 7. Complete DC Restoration System.
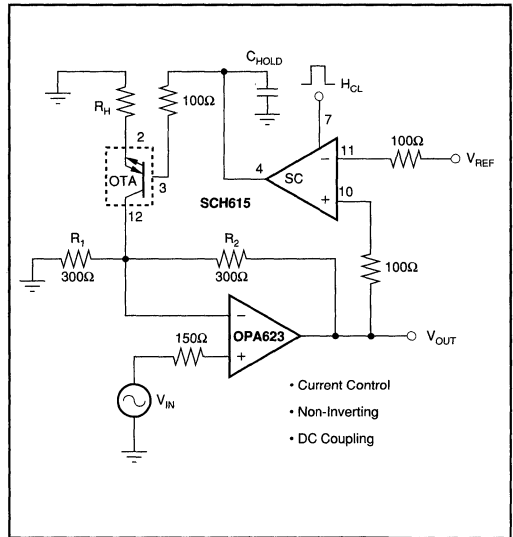
FIGURE 9. Clamped Video/RF Amplifier.
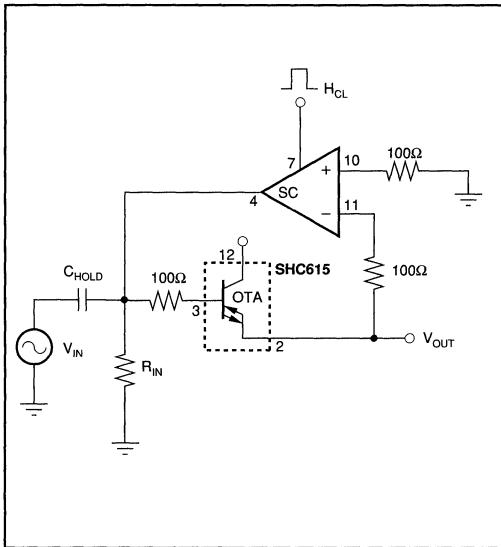
FIGURE 8. DC Resotration of a Buffer Amplifier.
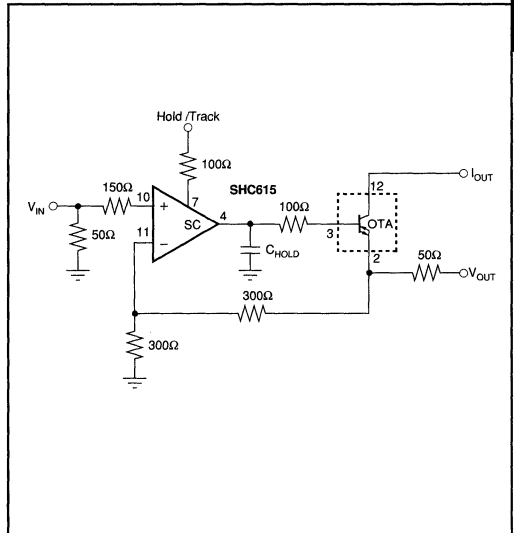
FIGURE 10. Sample/Hold Amplifier.

SHC615

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SAMPLE/HOLD AMPLIFIERS
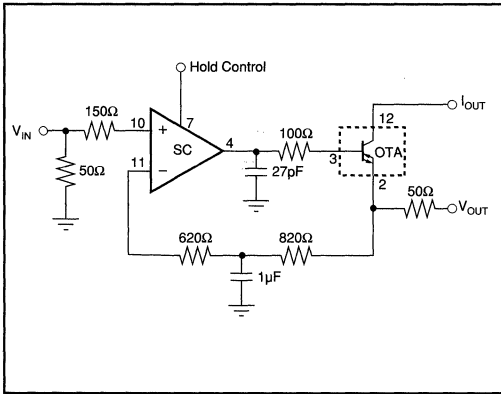
FIGURE 11. Integrator for ns-Pulses.

FIGURE 12. Fast Pulse Peak Detector.

FIGURE 13. CCD Analog Front-End.
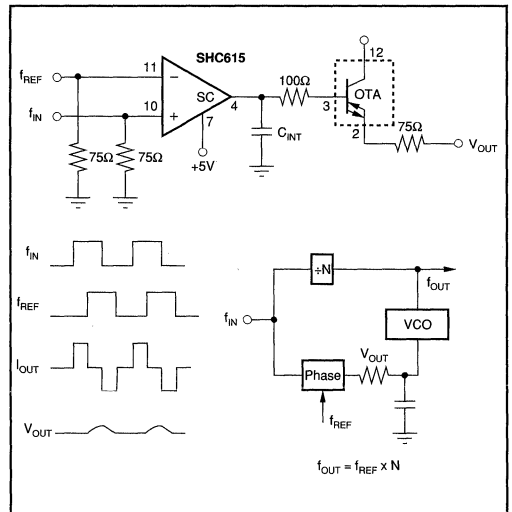
FIGURE 14. Phase Detector For Fast PLL-Systems.

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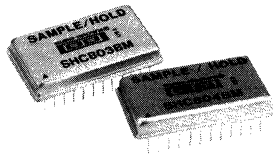
SHC803BM, CM
SHC804BM, CM

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-512

High Speed
SAMPLE/HOLD AMPLIFIER

SHC803/804BM, CM

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SAMPLE/HOLD AMPLIFIERS

FEATURES

● **350ns max ACQUISITION TIME**

● **±0.01% THROUGHPUT NONLINEARITY**

● **150ns max SAMPLE-TO-HOLD SETTLING TIME**

● **INPUT BUFFER (SHC803)**

● **24-PIN HERMETICALLY-SEALED METAL PACKAGE**

DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350ns to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the –25 to +85°C temperature range.

The ±25ps maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/µs. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is –25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.

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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM			SHC803/SHC804CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
SAMPLE/HOLD INPUTS (without Input Buffer)							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL (HOLD, $\overline{HOLD}$)							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	μA
I_{IL}, V_{IN} = +0.4V			−1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS (without Input Buffer)							
ACCURACY							
Sample Mode							
Gain		−1			*		V/V
Gain Error			±0.1		*	*	%
Temperature Coefficient		±3	±10	±1		±5	ppm/°C
Linearity Error		±0.001	±0.005	*		*	% of FSR[1]
Zero Offset		±1	±5	±0.5		±3	mV
Temperature Coefficient		±1	±2.5	±0.5		±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10	±1		±5	mV
Temperature Coefficient		±3	±10	±2		±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		*		μV/μs
+85°C			±0.5			±0.1	mV/μs
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity[2]: ±V_{CC}			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V Step)							
to within: ±0.1% (±10mV)		220		*			ns
±0.01% (±1mV)		250	350	*	*		ns
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150	*	*		ns
Sample-to-Hold Transient Amplitude		60	150	*	*		mV_{PEAK}
Aperture Delay Time[3]		15	25	*	*		ns
Aperture Uncertainty		±10	±25	*	*		ps
Sample Mode: Output Slew Rate		160		*			V/μs
Full Power Bandwidth		1		*			MHz
Small Signal Bandwidth		16		*			MHz
Hold Mode Feedthrough Rejection							
(10V Square Wave Input)	±0.03	±0.005		*			%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common		*			
Output Impedance (at DC)		0.01	0.1	*	*		Ω
INPUT BUFFER CHARACTERISTICS (SHC803 only)							
INPUT							
Offset Voltage		±1/2	±5	*	*		mV
vs Temperature		±1.5	±2.5	*	*		ppm of FSR/°C
Bias Current			±25			*	nA
Impedance		10⁸ ‖ 5		*			Ω ‖ pF
V_{IN} Range	±10.25	±11		*	*		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320		*			kHz
Slew Rate[4]		10		*			V/μs
Settling Time[4] to ±2mV for 10V Step		2.5		*			μs
OUTPUT							
V_{OUT} Range	±10.25			*			V
Output Current	±10.25			*			mA

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SPECIFICATIONS (CONT)

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM			SHC803/SHC804CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Rated Voltage: ±V_{CC}	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (No Load)							
SHC804: +V_{CC}		30	35		*	*	mA
−V_{CC}		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: +V_{CC}		33	40		*	*	mA
−V_{CC}		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+125	*		*	°C

* Specification same as SHC803/SHC804BM.
NOTES: (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804. (2) Sensitivity of offset plus charge offset. (3) With respect to HOLD. For $\overline{\text{HOLD}}$ add 5ns typical. (4) With buffer connected to the sample/hold amplifier.

SHC803/804BM, CM

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SAMPLE/HOLD AMPLIFIERS

CONNECTION DIAGRAMS

SHC803CM, BM

Pin	Name		Name	Pin
1	Analog Output	+V$_{CC}$		24
2	NC	V$_{CC}$ COM		23
3	NC	−V$_{CC}$		22
4	NC	COM		21
5	NC	NC		20
6	NC	NC		19
7	NC	NC		18
8	NC	Buffer In		17
9	V$_{DD}$	NC		16
10	DCOM	COM		15
11	Hold	Buffer Out		14
12	$\overline{Hold}$	S/H In		13

V$_{OUT}$ — 1μF, 1μF — +15V, COM, −15V Analog Power Supply

Digital Power Supply +5V COM

Signal Source

SHC804CM, BM

Pin	Name		Name	Pin
1	Analog Output	+V$_{CC}$		24
2	NC	V$_{CC}$ COM		23
3	NC	−V$_{CC}$		22
4	NC	COM		21
5	NC	NC		20
6	NC	NC		19
7	NC	NC		18
8	NC	NC		17
9	V$_{DD}$	NC		16
10	DCOM	COM		15
11	Hold	NC		14
12	$\overline{Hold}$	S/H In		13

V$_{OUT}$ — 1μF, 1μF — +15V, COM, −15V Analog Power Supply

Digital Power Supply +5V COM

Signal Source

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V$_{DD}$	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{HOLD}$	Logic "0" = HOLD
13	S/H In	SHC804 input; for SHC803 connect pin 13 to pin14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal common
22	−V$_{CC}$	−15V supply
23	V$_{CC}$ COM	Analog to power common, connected to case
24	+V$_{CC}$	+15V supply

ABSOLUTE MAXIMUM RATINGS

Input Overvoltage .... ±15V
+V$_{CC}$ to V$_{CC}$ COMMON .... 0 to +18V
−V$_{CC}$ to V$_{CC}$ COMMON .... 0 to −18V
Voltage on Digital Inputs (pins 11 and 12) .... −0.5V to +7V
Power Dissipation 1500mW
V$_{DD}$ to DCOM .... −0.5V
Analog Output .... Indefinite Short to V$_{CC}$ COM

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliablility.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC803BM	24-Pin	113
SHC803CM	24-Pin	113
SHC804BM	24-Pin	113
SHC804CM	24-Pin	113

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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SHC5320
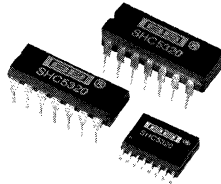
High Speed Bipolar Monolithic
SAMPLE/HOLD AMPLIFIER

FEATURES

● **ACQUISITION TIME TO 0.01%: 1.5µs max**
● **HOLD MODE SETTLING TIME: 350ns max**
● **DROOP RATE AT +25°C: 0.5µV/µs max**
● **TTL COMPATIBLE**
● **FULL DIFFERENTIAL INPUTS**
● **INTERNAL HOLDING CAPACITOR**
● **TWO TEMPERATURE RANGES:**
  –40°C to +85°C (KH, KP, KU, KD)
  –55°C to +125°C (SH)
● **PACKAGE OPTIONS: 14-pin Ceramic and Plastic DIP, 16-pin SOIC**

APPLICATIONS

● **PRECISION DATA ACQUISITION SYSTEMS**
● **DIGITAL-TO-ANALOG CONVERTER DEGLITCHER**
● **AUTO ZERO CIRCUITS**
● **PEAK DETECTORS**

DESCRIPTION

The SHC5320 is a bipolar monolithic sample/hold circuit designed for use in precision high-speed data acquisition applications.

The circuit employs an input transconductance amplifier capable of providing large amounts of charging current to the holding capacitor, thus enabling fast acquisition times. It also incorporates a low leakage analog switch and an output integrating amplifier with input bias current optimized to assure low droop rates. Since the analog switch always drives into a load at virtual ground, charge injection into the holding capacitor is constant over the entire input voltage range. As a result, the charge offset (pedestal voltage) resulting from this charge injection can be adjusted to zero by use of the offset adjustment capability. The device includes an internal holding capacitor to simplify ease of application; however, provision is also made to add additional external capacitance to improve the output voltage droop rate.

The SHC5320 is manufactured using a dielectric isolation process which minimizes stray capacitance (enabling higher-speed operation), and eliminates latch-up associated with substrate SCRs. The SHC5320KH, KP, KU, and KD feature fully specified operation over the extended industrial temperature range of –40°C to +85°C, while the SHC5320SH operates over the temperature range of –55°C to +125°C. The device requires ±15V supplies for operation, and is packaged in a reliable 14-pin ceramic or plastic dual-in-line package, as well as a 16-pin surface mount plastic package.

SHC5320

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SAMPLE/HOLD AMPLIFIERS

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

PARAMETERS	SHC5320KH, KP, KU			SHC5320SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS							
ANALOG							
Voltage Range	±10			*			V
Common-Mode Range	±10			*			V
Input Resistance	1	5		*	*		MΩ
Input Capacitance			3			*	pF
Bias Current		±100	±300		±70	±200	nA
Bias Current Over Temperature Range			±300			±200	nA
Offset Current		±30	±300		*	±100	nA
Offset Current Over Temperature Range			±300			±100	nA
DIGITAL (Over Temperature Range)							
V_{IH} (Logic "1")	2.0			*			V
V_{IL} (Logic "0")			0.8			*	V
I_{IH} (V_I = +5V)			0.1			*	μA
I_{IL} (V_I = 0V)			4			*	μA
Logic "0" = SAMPLE							
Logic "1" = HOLD							
OUTPUT CHARACTERISTICS							
Voltage Range	±10			*			V
Current	±10			*			mA
Output Impedance (Hold Mode)		1			*		Ω
Noise, DC to 10MHz: Sample Hold		125	200		*	*	μVrms
Hold Mode		125	200		*	*	μVrms
DC ACCURACY/STABILITY							
Gain, Open Loop, DC	3×10^5	2×10^6		10^6	*		V/V
Input Offset Voltage		±0.5			±0.2		mV
Input Offset Voltage Over Temperature Range			±1.5			±2	mV
Input Offset Voltage Drift		±5	±20		*	±15	μV/°C
CMRR[1]	72	90		80	*		dB
Power Supply Rejection[2]: $+V_{CC}$	80			*			dB
$-V_{CC}$	65			*			dB
HOLD-TO-SAMPLE MODE							
DYNAMIC CHARACTERISTICS							
Acquisition Time, A = −1, 10V Step[3]:							
to ±0.01%		1	1.5		*	*	μs
to ±0.1%		0.8	1.2		*	*	μs
SAMPLE MODE							
Gain-Bandwidth Product (Gain = +1)[4]:							
C_H = 100pF		2			*		MHz
C_H = 1000pF		180			*		kHz
Full Power Bandwidth[5]		600			*		kHz
Slew Rate[6]		45			*		V/μs
Rise Time[4]		100			*		ns
Overshoot[4]		15			*		%
SAMPLE-TO-HOLD MODE							
DYNAMIC CHARACTERISTICS							
Aperture Time[7]		25			*		ns
Effective Aperture Time	−50	−25	0	*	*	*	ns
Aperture Uncertainty (Aperture Jitter)		0.3			*		ns
Charge Offset (Pedestal)[8] (Adjustable to Zero)		1	5		*	*	mV
Charge Transfer[8]		0.1	0.5		*	*	pC
Sample-to-Hold Transient Settling Time							
to ±0.01% of FSR		165	350		*	*	ns
HOLD MODE							
Droop[9]		0.08	0.5		*	*	μV/μs
Droop at Maximum Temperature[9]		1.2	100		17	*	μV/μs
Drift Current[9]		8	50		*	*	pA
Drift Current at Maximum Temperature[9]		0.12	10		1.7	*	nA
Feedthrough, 10Vp-p, 100kHz Sinewave		2			*		mV

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

	SHC5320KH, KP, KU			SHC5320SH			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLIES							
$+V_{CC}$	+12	+15	+18	*	*	*	V
$-V_{CC}$	−12	−15	−18	*	*	*	V
$+I_{CC}$ ($+V_{CC}$ = 15V)[9]		11	13		*	*	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)[9]		−11	−13		*	*	mA
TEMPERATURE							
Specification	−40		+85	−55		+125	°C
Storage	−65		+150	*		*	°C
PACKAGE	Hermetic Ceramic, Plastic DIP, SOIC			Hermetic Ceramic			

*Specification same as grade to the left.
NOTES: (1) $V_{CM} = \pm5VDC$. (2) Based on a ±0.5V swing for each supply with all other supplies held constant. (3) V_O = 10V step, R_L = 2kΩ, C_L = 50pF. (4) V_O = 200mVp-p, R_L = 2kΩ, C_L = 50pF. (5) V_{IN} = 20Vp-p, R_L = 2kΩ, C_L = 50pF, unattenuated output. (6) V_O = 20V step, R_L = 2kΩ, C_L = 50pF. (7) Simulated only, not tested. (8) V_{IN} = 0V, V_{IH} = +3.5V, t_R < 20ns (V_{IL} to V_{IH}). (9) Specified for zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA average at 20V differential.

PIN CONNECTIONS
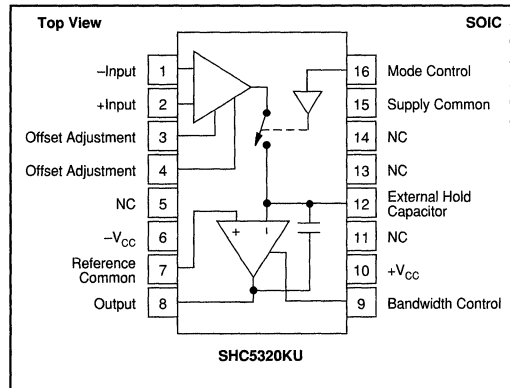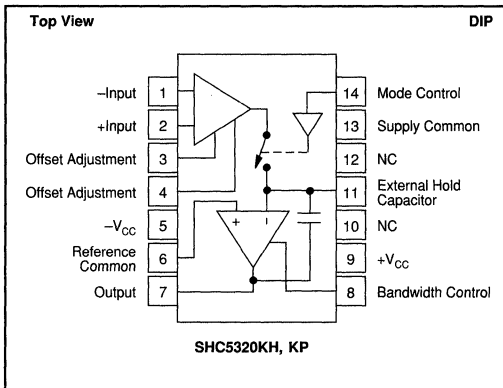
SHC5320KH, KP

SHC5320KU

ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals 40V
Input Voltage .... Actual Supply Voltage
Differential Input Voltage .... ±24V
Digital Input Voltage .... +15V, −1V
Output Current, continuous[2] .... ±20mA
Internal Power Dissipation 450mW
Storage Temperature Range .... −65°C < T_A < +150°C
Output Short-Circuit Duration[3] .... None
Lead Temperature (soldering, 10s) .... 300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Absolute maximum ratings apply to both dice and package parts, unless otherwise noted. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE
SHC5320KP	−40°C to +85°C	14-pin Plastic DIP
SHC5320KU	−40°C to +85°C	16-pin SOIC
SHC5320KH	−40°C to +85°C	14-pin Cerdip
SHC5320SH	−55°C to +125°C	14-pin Cerdip

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC5320KP	14-Pin Plastic DIP	010
SCH5320KU	16-Pin SOIC	211
SHC5320KH	14-Pin Cerdip	163
SHC5320SH	14-Pin Cerdip	163

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

SHC5320

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SAMPLE/HOLD AMPLIFIERS

DICE INFORMATION
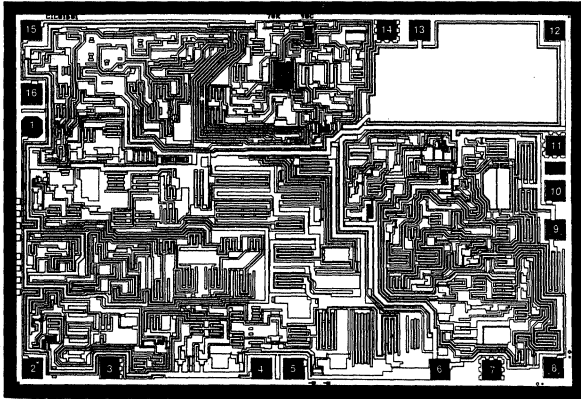
SHC5320 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	−Input	9	Output
2	+Input	10	Bandwidth Control
3	NC	11	NC
4	Offset Adjustment	12	+V$_{CC}$
5	Offset Adjustment	13	External Hold Cap.
6	−V$_{CC}$	14	NC
7	NC	15	Supply Common
8	Reference Common	16	Mode Control

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	140 x 95	3.56 x 2.41
Die Thickness	18 ±0.8	0.45 ±0.02
Min. Pad Size	5 x 5	0.127 x 0.127

ELECTRICAL (Dice)

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

PARAMETER	SHC5320KD			UNITS
	MIN	TYP	MAX	
INPUT VOLTAGE RANGE	±10			V
INPUT OFFSET VOLTAGE			1.5	mV
BIAS CURRENT			300	nA
INPUT OFFSET CURRENT			300	nA
COMMON-MODE RANGE	±10			V
COMMON-MODE REJECTION RATIO[1]	72			dB
OUTPUT VOLTAGE RANGE	±10			V
OUTPUT CURRENT	±10			mA
DIGITAL INPUT VOLTAGE "HIGH" (V$_{IH}$)	2.0			V
DIGITAL INPUT VOLTAGE "LOW" (V$_{IL}$)			0.8	V
POSITIVE SUPPLY CURRENT[2]			+13	mA
NEGATIVE SUPPLY CURRENT[2]			−13	mA
POWER SUPPLY REJECTION[3] +V$_{CC}$ −V$_{CC}$	80 65			dB dB

NOTES: (1) V$_{CM}$ = ±5VDC. (2) Specified for a zero differential input voltage between pins 1 and 2. Supply current will increase with differential input voltage (as may occur in the hold mode) to approximately ±28mA at V$_{DIFF}$ = 20V. (3) Based on a ±0.5V swing for each supply with all other supplies held constant.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE
SHC5320KP	−40°C to +85°C	14-pin Plastic DIP
SHC5320KU	−40°C to +85°C	16-pin SOIC
SHC5320KH	−40°C to +85°C	14-pin Cerdip
SHC5320SH	−55°C to +125°C	14-pin Cerdip

TYPICAL PERFORMANCE CURVES

$\pm V_{CC} = 15V$.

TYPICAL SAMPLE/HOLD PERFORMANCE
AS FUNCTION OF HOLDING CAPACITOR

Acquisition Time (µs)
for 10V Step to ±0.01%

Voltage Droop (mV/100ms)
during Hold Mode

Charge Offset
Error (mV)

C_H Value (pF)
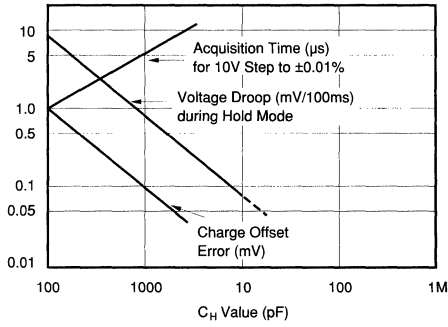
CHARGE OFFSET
vs MODE CONTROL (V_{IH}) VOLTAGE

Hold Step Voltage (mV)

$C_H = 100pF$

+75°C

+25°C

Logic Level High (V)
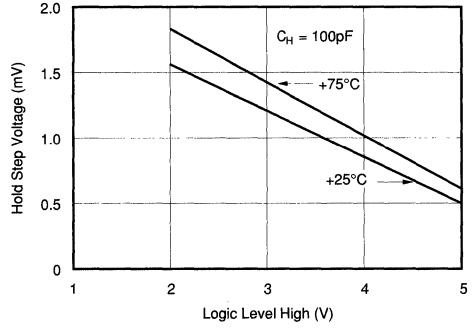
OPEN-LOOP GAIN
AND PHASE RESPONSE
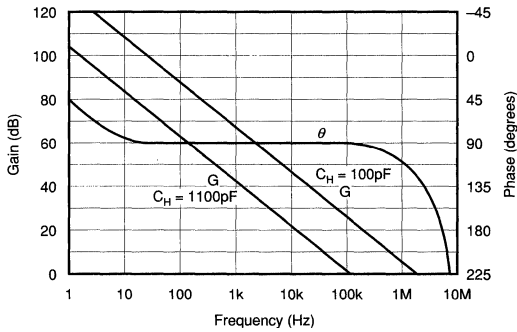
Gain (dB)

Phase (degrees)

θ

$C_H = 100pF$
G

$C_H = 1100pF$
G

Frequency (Hz)

DRIFT CURRENT
vs TEMPERATURE

I_{DRIFT} (pA)

$C_H = 100pF$

Temperature (°C)

SHC5320

SAMPLE/HOLD AMPLIFIERS

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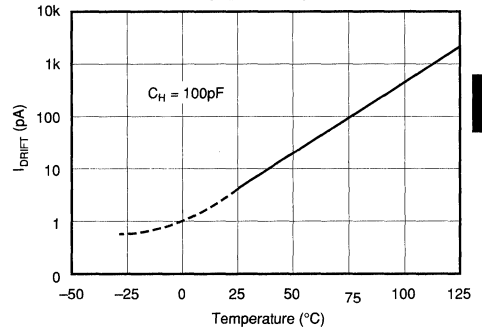
DISCUSSION OF SPECIFICATIONS

WHAT IS A SAMPLE/HOLD AMPLIFIER?

A sample/hold amplifier (also sometimes called a track-and-hold amplifier) is a circuit that captures and holds an analog voltage at a specific point in time under control of an external circuit, such as a microprocessor. This type of circuit has many applications; however, its primary use is in data acquisition systems which require that the voltage be captured and held during the analog-to-digital conversion process. Use of a sample/hold effectively increases the bandwidth of a data acquisition system by a significant amount. For further discussion of this capability, refer to "Signal Digitization" in the Applications section of this data sheet.

The ideal sample/hold amplifier in its simplest form contains four primary components as illustrated in Figure 1, although in actual practice they may not be internally connected exactly as shown. Amplifier A_1, the input buffer, provides a high impedance load to the source circuit and supplies charging current to the holding capacitor C_H. Switch S_1 opens and closes under external control to gate the buffered input signal to the holding circuit or to remove it so that the most recently sampled signal will be held. Amplifier A_2 serves to present a high impedance load to the holding capacitor and to provide a low impedance voltage source for external loads. A minimum of three terminals are provided for the user: input, output, and mode control (or sample/hold control). When S_1, is closed, the output signal follows the input signal, subject to errors imposed by amplifier bandwidth and other errors as discussed below. When S_1, is opened, the voltage stored on the holding capacitor will be held indefinitely (in the ideal case), and will appear at the output of the circuit until S_1, is again closed under command of the mode control signal.
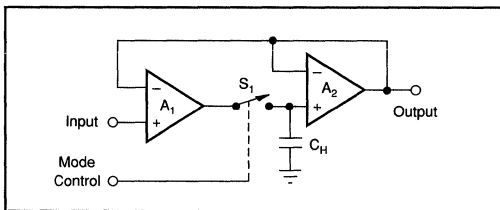
FIGURE 1. Ideal Sample/Hold Amplifier.

The following discussion of specifications covers the critical types of errors which may be experienced in applications of a sample/hold amplifier. These errors are depicted graphically in Figure 2, and in the Typical Performance Curves.

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value after the sample mode is initiated. Included in this time are effects of switch delay time, slew rate of the buffer amplifier, and settling time for a specified change in held voltage value. Slew rate limitations of the buffer amplifier will cause
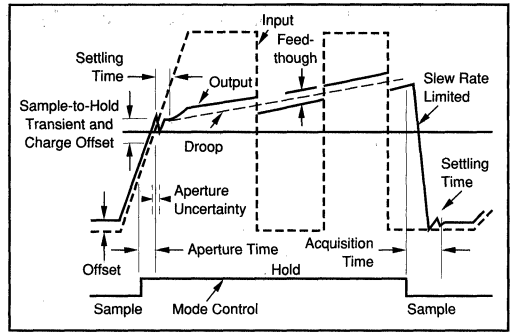
FIGURE 2. Illustration of Sample/Hold Specifications.

actual acquisition time to be highly dependent on the amplitude of the voltage to be acquired, relative to the value already held by the capacitor. Therefore, proper specification of sample/hold amplifier performance includes definition of both output value step size and required error band accuracy.

Aperture Time (or aperture delay time) is the time required for switch S_1, to open and remove the charging signal from the capacitor after the mode control signal has changed from "sample" to "hold." This time is measured from the 50% point of the Hold mode transition to the time at which the output stops tracking the input. This parameter is very important in applications for which the input signal is changing very rapidly when the Hold mode is initiated.

Effective Aperture Time is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to switch S_1. This time may be negative, zero, or positive. A negative value indicates that the mode control propagation delay is shorter than the analog propagation delay, with the result that the analog value present on the capacitor at the time the switch opens occurred earlier than the application of the mode control signal by the amount of the effective aperture delay time.

Aperture Uncertainty (or aperture jitter) is the variation observed in the aperture time over a large number of observations. This parameter is important when the analog input is a rapidly changing signal, as aperture uncertainty contributes to lack of knowledge (at the output) about the true value of the input at the precise time the Hold mode is initiated. The maximum input frequency for a given acceptable error contribution due to aperture uncertainty is

$$f_{MAX} = \text{Maximum Fractional Error}/2\pi t_U$$

where Maximum Fractional Error (MFE) is the ratio of the maximum allowable error voltage to peak voltage, and t_U is the aperture uncertainty time. For a bipolar $\pm10V$ signal and a maximum uncertainty error of 1/2LSB in a 12-bit system, the MFE is equal to $1/2LSB \div V_{PEAK} = 2.44mV \div 10V = 0.000244V/V$, since 1/2LSB = 2.44mV for a 20V full-scale range.

For the same system operating with a unipolar 0V to 10V signal, MFE would be 0.000122V/V.

Charge Offset (pedestal) is the output voltage change that results from charge transfer into the hold capacitor through stray capacitance when the Hold mode command is given. This charge appears as an offset voltage at the output, and in some sample/hold amplifiers may be a function of the input voltage.

Charge offset is specified for the SHC5320 using only the internal holding capacitor. When an external capacitor is added, charge offset is calculated as Charge Transfer (pC) divided by total hold capacitance. Charge Transfer is also specified for the SHC5320, and total hold capacitance is the sum of the internal hold capacitor value (100pF) and the external hold capacitor. Since charge transfer is not a function of analog input voltage for the SHC5320, this error may be removed by means of the offset adjustment capability of the amplifier.

Droop Rate is the change in output voltage over time during the Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier. Droop rate varies with temperature and the quality of the external holding capacitor, if used. Careful circuit layout is also required to minimize droop.

Drift Current is the net leakage current affecting the hold capacitor during the Hold mode. With knowledge of the drift current, droop can be calculated as:

$$\text{Droop (V/s)} = I_D(pA)/C_H(pF)$$

Hold Mode Feedthrough is the fraction of the input signal which appears at the output while in the Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.

Hold Mode Settling Time is the time required for the sample-to-hold transient to settle within a specified error band.

OPERATING INSTRUCTIONS

(Developed Around 14-Pin Package)

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold modes. The offset should then be adjusted to zero output for the periods when the amplifier is in the Hold mode. In this way, the effects of both amplifier offset and charge offset will be accounted for.

SAMPLE/HOLD CONTROL

A TTL logic "0" applied to pin 14 switches the SHC5320 into the Sample (track) mode. In this mode, the device acts as an amplifier which exhibits normal operational amplifier behavior, with the relationship of output to input signal depending upon the circuit configuration selected (see the Installation section below). Application of a logic "1" to pin 14 switches the SHC5320 into the Hold mode, with the output voltage held constant at the value present when the hold command is given. Pin 14 presents less than one LSTTL load to the driving circuit throughout the full operating temperature range.

Teflon® Du Pont Corporation

ADDITION OF AN EXTERNAL CAPACITOR

The SHC5320 contains an internal 100pF MOS holding capacitor, sufficient for most high-speed applications. If improved droop performance is desired (with increased acquisition time), additional capacitance may be added between pins 7 and 11. If an external holding capacitor C_H is used, then a noise-bandwidth capacitor with a value $0.1C_H$ should be connected from pin 8 to ground. The exact value and type of this bandwidth capacitor are not critical.

Capacitors with high insulation resistance and low dielectric absorption, *such as Teflon® or polystyrene units*, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with total hold capacitance from the values given in the specification table for the internal 100pF capacitor. The behavior of acquisition time versus total hold capacitance is shown in the Typical Performance Curves.

OUTPUT PROTECTION

In order to optimize high-frequency performance of this device, output protection is not included. This high frequency performance is mandatory for a good sample/hold, which must absorb high-frequency changes in load current when driving a successive-approximation A/D converter. Due to the lack of output protection, the output circuit will not tolerate an indefinite short to common, but a momentary short is permissible. The output should never be shorted to a supply.

INSTALLATION

(Developed Around 14-Pin Package)

LAYOUT PRECAUTIONS

Since the holding capacitor is connected to virtual ground at one end (pin 11) and to a low-impedance voltage source at the other (pin 7), the SHC5320 does not require the use of guard rings and other careful layout techniques which are required by many sample/hold circuits. However, normal good layout practice should be observed, minimizing the possibility of leakage paths across the holding capacitor. As in all digital-analog circuits, analog signal lines on the circuit board should cross digital signal paths at right angles whenever possible.

GROUNDING AND BYPASSING

Pin 6 (Reference Common) should be connected to the system analog signal common as close to the unit as possible. Likewise, pin 13 (Supply Common) should be connected to the system supply common. If the system design prevents running these two common lines separately, they should be connected together close to the unit, preferably to

SHC5320

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SAMPLE/HOLD AMPLIFIERS

a large ground plane surrounding the sample/hold. Bypass capacitors ($0.01\mu F$ to $0.1\mu F$ ceramic in parallel with $1\mu F$ to $10\mu F$ tantalum) should be connected from each power supply terminal of the device to pin 13 (Supply Common).

OFFSET ADJUSTMENT

Offset adjustment capability may be achieved by connecting a $10k\Omega$, 10-turn potentiometer as illustrated in Figure 3.
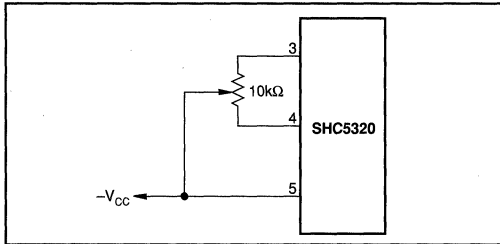
FIGURE 3. Connection of Offset Adjustment Potentiometer.

NONINVERTING MODE

The most common application of the SHC5320 will utilize the connection illustrated in Figure 4. In this mode of operation, the sample/hold will operate as a unity-gain noninverting amplifier when in the Sample mode, and the output signal will track the input. The high bandwidth of the SHC5320 and the large open-loop gain assure that gain error will be minimized.
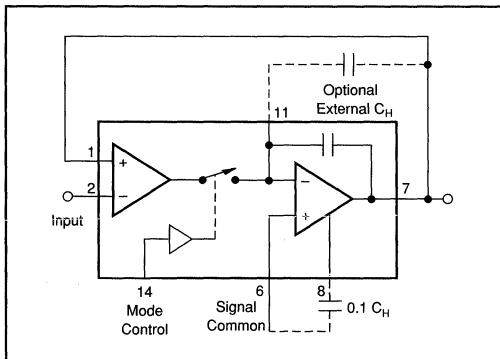
FIGURE 4. Noninverting Unity-Gain Connections.

When sampling lower-amplitude signals, the SHC5320 may also be connected as a noninverting amplifier with gain, as illustrated in Figure 5. In this circuit the gain of the amplifier is equal to $-R_2/R_1$ when sampling.

The Burr-Brown SHC5320 uses current sources to bias the internal amplifiers. This means that the bias of the amplifiers is not dependent on the common-mode voltage of the input signal. This makes the spurious free dynamic range in the non-inverting mode equal that of the inverting mode.
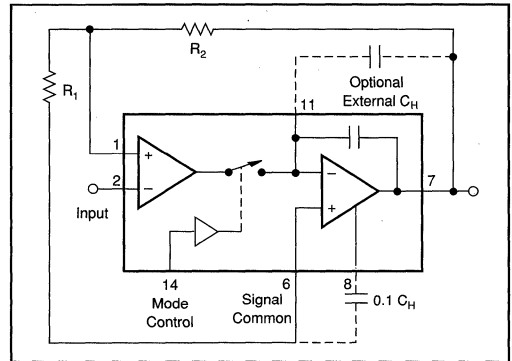
FIGURE 5. Noninverting Configuration with Gain = 1 + R_2/R_1.
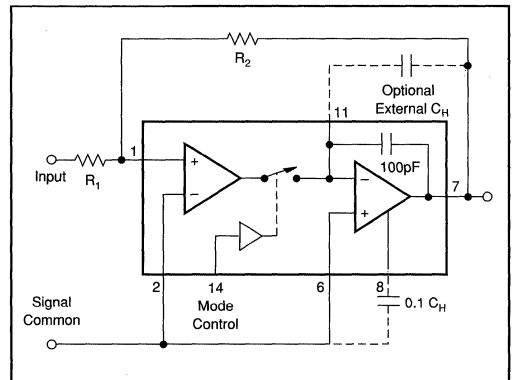
FIGURE 6. Inverting Configuration with Gain = $-(R_2/R_1)$.

INVERTING MODE

Unlike most sample/holds, the SHC5320 may also be connected to act as an inverting amplifier, as shown in Figure 6. For this configuration, the gain is equal to $-R_2/R_1$.

INPUT OVERLOAD PROTECTION

It is possible that the input transconductance amplifier of the SHC5320 will saturate when the unit is in the Hold mode, due to a non-zero differential signal appearing between pins 1 and 2. This differential signal may be the result of a rapidly changing input signal or application of a new channel from an input multiplexer. When the input buffer is saturated in this fashion, acquisition time may be degraded because of the time required for the buffer to recover from saturation. In addition, the input buffer, which is designed to provide large amounts of charging current to the output integrator, may draw large amounts of supply current which may exceed 40mA peak in some applications. For these reasons, it is desirable to limit the differential voltage which may appear at the summing junction of the input buffer. Figures 7 and 8 illustrate possible methods of providing this voltage limitation for the inverting and noninverting configurations. The

diodes may be Schottky diodes, which will provide the fastest clamping action and lowest clamping voltage, but fast signal diodes such as IN914 will also work in most applications. In each configuration the value of R_1 should be large enough to avoid excessive loading of the input signal source. Similarly, R_2 should have a value of $2k\Omega$ or greater to insure sufficient load current capability from the sample/hold. If the value of R_2 becomes too large, however, the added capacitance of the diodes may change the sample/hold phase response enough to cause oscillation.
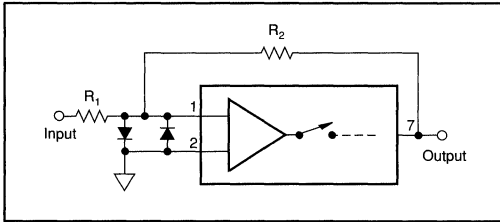
FIGURE 7. Input Overload Protection—Inverting Configuration.
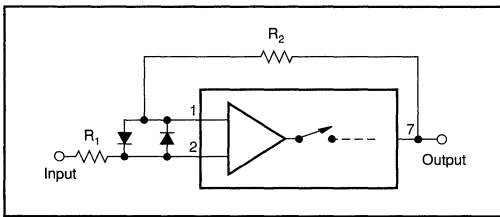
FIGURE 8. Input Overload Protection—Noninverting Configuration.

APPLICATIONS

(Developed Around 14-Pin Package)

SIGNAL DIGITIZATION

Sample/hold amplifiers are normally used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC80MAH-12 is a 12-bit successive-approximation converter with a 25μs conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during conversion.

The maximum rate of change of a sine wave of frequency, f, is dv/dt (max) = $2\pi Af(V/s)$. If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/25μs = 0.0976mV/μs. Thus the sampled sinusoidal signal frequency limit is

$$f = (0.0976 \times 10^3)/2\pi A = 15.5/A \text{ (Hz)},$$

where A is the peak amplitude of the sine wave. For a ±10V

sine wave, this corresponds to a frequency of 1.6Hz, hardly acceptable for the majority of sampled data systems.

However, a sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold it at any instant in time. There is a short delay (aperture delay) between the time the hold command is asserted and the time the circuit actually holds. The hold command signal can usually be advanced in time (or delayed, in the case of negative effective aperture delay) to cause the amplifier to hold the signal actually desired.

Aperture uncertainty (also called aperture jitter) is also a key consideration. For the SHC5320 there is a 300ps period during which the signal should not change more than the amount allowed for aperture uncertainty in the system error budget, perhaps 1/2LSB for a 12-bit system. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/0.3ns = 8.13mV/ns. The equivalent input sine wave frequency is

$$f = 8.13 \times 10^6/2\pi A = 1.29/A \text{ (MHz)},$$

a factor of almost 84,000 higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC80/SHC5320 combination is 26.5μs (25μs A/D) conversion time plus 1.5μs S/H acquisition time). Sampling a sine wave at the Nyquist rate, this permits a maximum input signal frequency of 37.7kHz. The above analysis assumes that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion. Both of these assumptions are valid for the SHC5320 in this application.

DATA ACQUISITION

The SHC5320 may be used to hold data for analog-to-digital conversion or may be used to provide pulse-amplitude modulation (PAM) data output (see Figures 9 and 10).
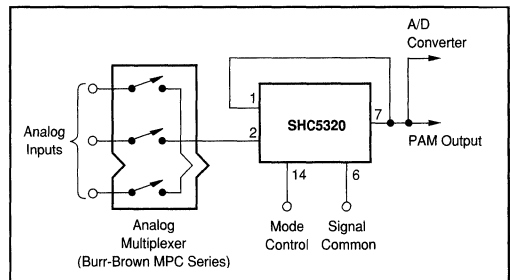
FIGURE 9. Typical Data Acquisition Configuration.
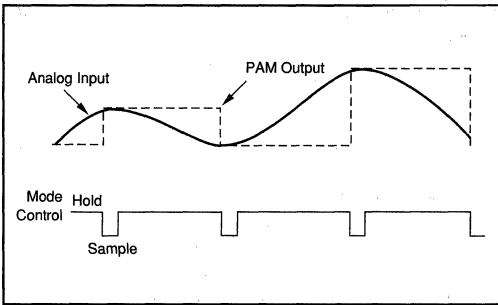
FIGURE 10. PAM Output.

DATA DISTRIBUTION

The SHC5320 may be used to hold the output of a digital-to-analog converter and distribute several different analog voltages to different loads (see Figure 11).

HIGH-SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the A/D converter. If two or more sample/holds are used with a multiplexer (such as the Burr-Brown MPC800 or MPC801) as shown in Figure 12, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched into the A/D converter, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this signal by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed. In low level systems an instrumentation amplifier (such as the Burr-Brown INA101) and a differential multiplexer (such as the Burr-Brown MPC509A or MPC507A) may be required in front of the sample/hold. The settling and acquisition times of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the total conversion time as before by operating in this overlapped mode with the sample/holds.
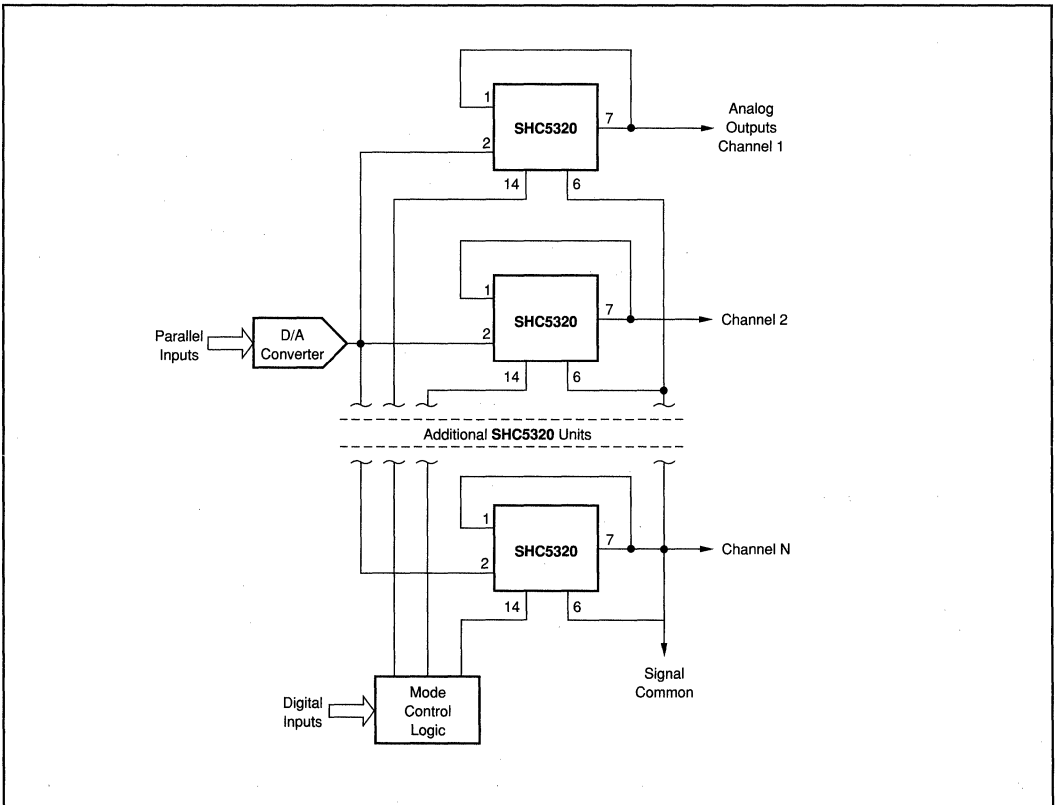
FIGURE 11. Typical Data Distribution Configuration.
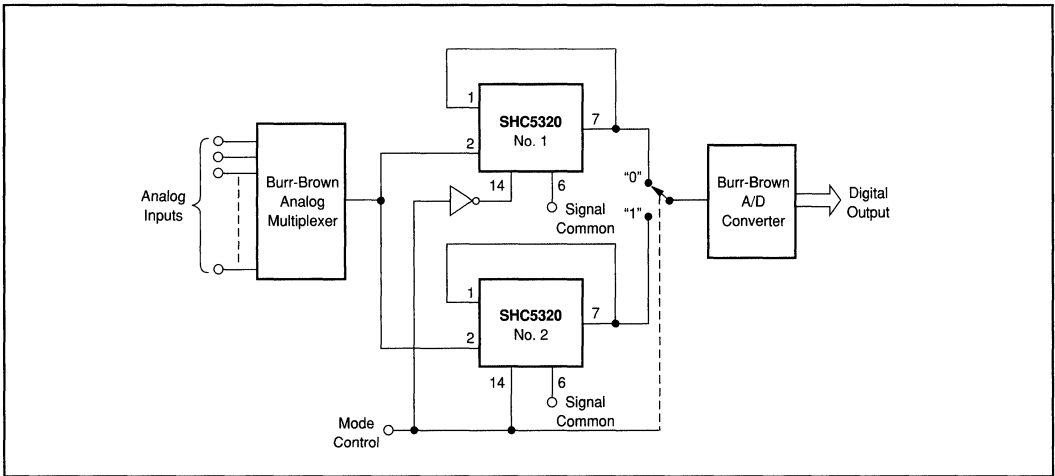
FIGURE 12. Typical Overlapped Sample/Hold Configuration.

SHC5320

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SAMPLE/HOLD AMPLIFIERS

7 Voltage-to-Frequency Converters

Voltage-to-frequency converters provide a simple, low-cost alternative to A/D converters. The frequency output is easily isolated, transmitted or recorded. It can be interfaced to many commonly used micro-controllers and processors through counter input ports or counter/timer peripheral ICs.

The voltage-to-frequency converters' integrating input properties make them ideal for high noise industrial environments. Connected in frequency-to-voltage mode, they are useful for tachometer and rate control circuitry, motor control and telemetry.

Choose from a variety of popular devices, including:

VFC32—Low cost V/F converter operates up to 500kHz.

VFC320—Operates up to 1MHz full-scale with improved accuracy for high performance A/D conversion.

VFC100, VFC101—Synchronized V/F converter up to 2MHz full-scale frequency is precisely determined by your system clock frequency. Excellent for A/D conversion.

VFC121—Operates from a single 4.5V to 36V power supply. Full-scale output frequency up to 1.5MHz.

VFC110—High performance V/F converter operates to 4MHz with low frequency jitter.

Other models provide special features and performance. Use our selection guide below to locate the V/F converter for your application.

VOLTAGE-TO-FREQUENCY CONVERTERS — Boldface = NEW — 7

Description	Model	Frequency Range (kHz)	V_IN Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[1]	Pkg	Page No.
Low-Cost Monolithic	VFC32	User-selected 500kHz, max	User-selected	±0.01 at 10kHz ±0.05 at 100kHz	75 typ ±100	Com Ind, Mil	DIP, SOIC TO-100,	7.2
Low-Cost Complete	VFC42 VFC52	0 to 10 0 to 100	0 to +10 0 to +10	±0.01 ±0.05	±100 ±150	Ind Ind	DIP DIP	A A
Precision Monolithic	VFC62 VFC320	User-selected 1MHz max	User-selected	±0.002 at 10kHz ±0.002 at 10kHz	±20 ±20	Ind Ind, Mil	DIP, TO-100 DIP, TO-100	A 7.50
Synochronized Monolithic	VFC100	Clock-Programmed 2MHz max	0 to +10	0.1 at 1MHz	±50	Ind, Mil	DIP	7.9
	VFC101	Clock-Programmed, 2MHz max	0 to +10, 0 to +5, 0 to +8, −5 to +5	±0.02 at 100kHz	±40	Ind	PLCC	7.24
High-Performance	VFC110	User-selected 4MHz max	0 to +10	±0.05 at 1MHz	±50	Ind	DIP	7.34
Single Supply, Low Power	VFC121	User-selected 1.5MHz max	User-selected	±0.03 at 100kHz	±40	Ind	DIP	7.42

NOTE: (1) Com = 0°C to +70°C, Ind = −25°C to +85°C.
"A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

VOLTAGE-TO-FREQUENCY CONVERTERS

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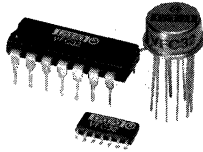
VFC32

Voltage-to-Frequency
and Frequency-to-Voltage
CONVERTER

FEATURES

● **OPERATION UP TO 500kHz**
● **EXCELLENT LINEARITY**
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
● **V/F OR F/V CONVERSION**
● **MONOTONIC**
● **VOLTAGE OR CURRENT INPUT**

APPLICATIONS

● **INTEGRATING A/D CONVERTER**
● **SERIAL FREQUENCY OUTPUT**
● **ISOLATED DATA TRANSMISSION**
● **FM ANALOG SIGNAL MOD/DEMOD**
● **MOTOR SPEED CONTROL**
● **TACHOMETER**

DESCRIPTION

The VFC32 voltage-to-frequency converter provides an output frequency accurately proportional to its input voltage. The digital open-collector frequency output is compatible with all common logic families. Its integrating input characteristics give the VFC32 excellent noise immunity and low nonlinearity.

Full-scale output frequency is determined by an external capacitor and resistor and can be scaled over a wide range. The VFC32 can also be configured as a frequency-to-voltage converter.

The VFC32 is available in 14-pin plastic DIP, SO-14 surface-mount, and metal TO-100 packages. Commercial, industrial, and military temperature range models are available.

PDS-372F

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SPECIFICATIONS

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	VFC32KP, KU MIN	TYP	MAX	VFC32BM MIN	TYP	MAX	VFC32SM MIN	TYP	MAX	UNITS
INPUT (V/F CONVERTER) $F_{OUT} = V_{IN}/7.5\,R_1\,C_1$											
Voltage Range(1)											
Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		−10	*		*	*		*	V
Current Range(1)		>0		+0.25	*		*	*		*	mA
Bias Current											
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage(2)			1	4		*	*		*	*	mV
Differential Impedance		300 || 10	650 || 10		*	*		*	*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		*	*		MΩ || pF
INPUT (F/V CONVERTER) $V_{OUT} = 7.5\,R_1\,C_1\,F_{IN}$											
Impedance		50 || 10	150 || 10		*	*		*	*		kΩ || pF
Logic "1"			+1.0		*		*	*		*	V
Logic "0"			−0.05		*		*	*		*	V
Pulse-width Range		0.1		150k/F_{MAX}	*		*	*		*	μs
ACCURACY											
Linearity Error(3)	0.01Hz ≤ Oper Freq ≤ 10kHz		±0.005	±0.010(4)		*	*		*	*	% of FSR(5)
	0.1Hz ≤ Oper Freq ≤ 100kHz		±0.025	±0.05		*	*		*	*	% of FSR
	0.5Hz ≤ Oper Freq ≤ 500kHz		±0.05			*			*		% of FSR
Offset Error Input											
Offset Voltage(2)			1	4		*	*		*	*	mV
Offset Drift(6)			±3			*			*		ppm of FSR/°C
Gain Error(2)			5			*			*		% of FSR
Gain Drift(6)	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift and gain drift)(6, 7)	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*		*	*	μA
Voltage, Logic "1"	External Pull-up Resistor Required (see Figure 4)			V_{PU}			*			*	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			*			*	s
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			*			*	ns
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	I_O ≤ 7mA	0 to +10			*			*			V
Current	V_O ≤ 7VDC	+10			*			*			mA
Impedance	Closed Loop			1			*			*	Ω
Capacitive Load	Without Oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500(8)	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	(V/F) to Specified Linearity for a Full Scale Input Step		(9)			*			*		
Overload Recovery	< 50% Overload		(9)			*			*		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					*		V
Quiescent Current			±5.5	±6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	−25		+85	−55		+125	°C
Operating		−25		+85	−55		+125	−55		+125	°C
Storage		−25		+85	−65		+150	−65		+150	°C

* Specification the same as VFC32KP.

NOTES: (1) A 25% duty cycle (0.25mA input current) is recommended for best linearity. (2) Adjustable to zero. See Offset and Gain Adjustment section. (3) Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C. (4) ±0.015% of FSR for negative inputs shown in Figure 5. Positive inputs are shown in Figure 1. (5) FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage). (6) Exclusive of external components' drift. (7) Positive drift is defined to be increasing frequency with increasing temperature. (8) For operations above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections. (9) One pulse of new frequency plus 1μs.

VFC32

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VOLTAGE-TO-FREQUENCY CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Output Sink Current (F_{OUT}) 50mA
Output Current (V_{OUT}) .... +20mA
Input Voltage, −Input .... ±Supply
Input Voltage, +Input .... ±Supply
Comparator Input .... ±Supply
Storage Temperature Range:
  VFC32BM, SM .... −65°C to +150°C
  VFC32KP, KU .... −25°C to +85°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC32KP	14-Pin Plastic DIP	010
VFC32BM	TO-100 Metal	007
VFC32SM	TO-100 Metal	007
VFC32KU	SO-14 SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC32KP	14-Pin Plastic DIP	0°C to 70°C
VFC32BM	TO-100 Metal	−25°C to +85°C
VFC32SM	TO-100 Metal	−55°C to +125°C
VFC32KU	SO-14 SOIC	0°C to +70°C

PIN CONFIGURATIONS

Top View

M Package (TO-100)

P Package / U Package (Epoxy Dual-in-line)

NC = no internal connection
External connection permitted.

TYPICAL PERFORMANCE CURVES

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

LINEARITY ERROR vs FULL SCALE FREQUENCY

LINEARITY ERROR vs OPERATING FREQUENCY

FULL SCALE DRIFT vs FULL SCALE FREQUENCY

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VOLTAGE-TO-FREQUENCY CONVERTERS

APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for frequency-to-voltage conversion. R_1 sets the input voltage range. For a 10V full-scale input, a 40kΩ input resistor is recommended. Other input voltage ranges can be achieved by changing the value of R_1.

$$R_1 = \frac{V_{FS}}{0.25 \text{mA}} \qquad (1)$$

R_1 should be a metal film type for good stability. Manufacturing tolerances can produce approximately ±10% variation in output frequency. Full-scale output frequency can be trimmed by adjusting the value of R_1—see Figure 3.

The full-scale output frequency is determined by C_1. Values shown in Figure 1 are for a full-scale output frequency of 10kHz. Values for other full-scale frequencies can be read from Figure 2. Any variation in C_1—tolerance, temperature drift, aging—directly affect the output frequency. Ceramic NPO or silver-mica types are a good choice.

For full-scale frequencies above 200kHz, use larger capacitor values as indicated in Figure 2, with $R_1 = 20$kΩ.

The value of the integrating capacitor, C_2, does not directly influence the output frequency, but its value must be chosen within certain bounds. Values chosen from Figure 2 produce approximately 2.5Vp-p integrator voltage waveform. If C_2's value is made too low, the integrator output voltage can exceed its linear output swing, resulting in a nonlinear response. Using C_2 values larger than shown in Figure 2 is acceptable.

Accuracy or temperature stability of C_2 is not critical because its value does not directly affect the output frequency. For best linearity, however, C_2 should have low leakage and low dielectric absorption. Polycarbonate and other film capacitors are generally excellent. Many ceramic types are adequate, but some low-voltage ceramic capacitor types may degrade nonlinearity. Electrolytic types are not recommended.

FREQUENCY OUTPUT PIN

The frequency output terminal is an open-collector logic output. A pull-up resistor is usually connected to a 5V logic supply to create standard logic-level pulses. It can, however, be connected to any power supply up to $+V_{CC}$. Output pulses have a constant duration and positive-going during the one-shot period. Current flowing in the open-collector output transistor returns through the Common terminal. This terminal should be connected to logic ground.
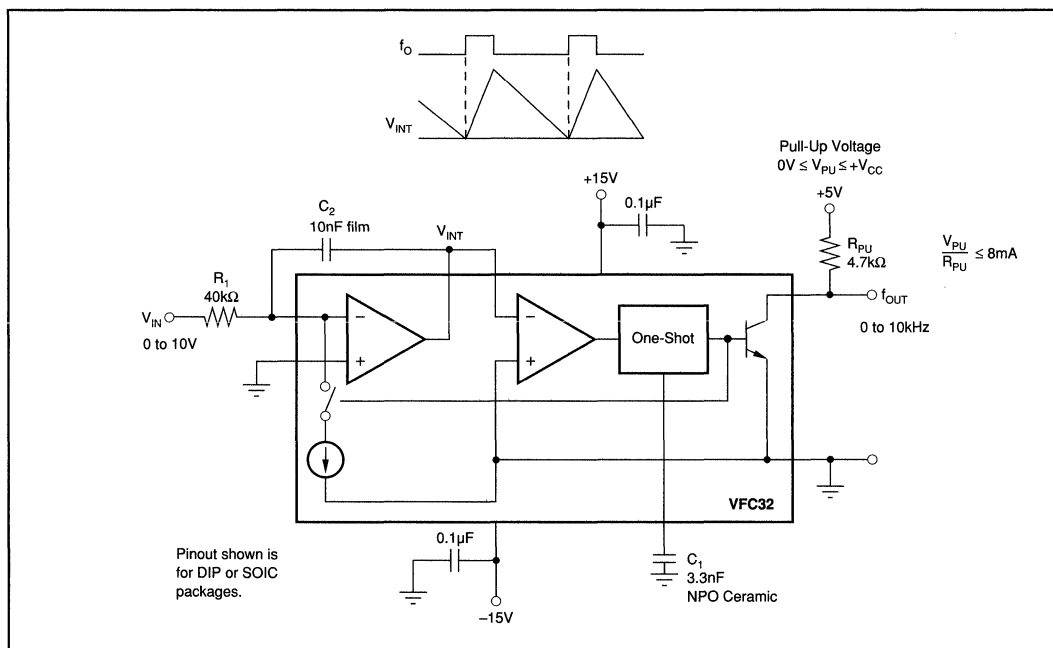
FIGURE 1. Voltage-to-Frequency Converter Circuit.

FREQUENCY-TO-VOLTAGE CONVERSION

Figure 4 shows the VFC32 connected as a frequency-to-voltage converter. The capacitive-coupled input network C_3, R_6 and R_7 allow standard 5V logic levels to trigger the comparator input. The comparator triggers the one-shot on the falling edge of the frequency input pulses. Threshold voltage of the comparator is approximately –0.7V. For frequency input waveforms less than 5V logic levels, the R_6/R_7 voltage divider can be adjusted to a lower voltage to assure that the comparator is triggered.

The value of C_1 is chosen from Figure 2 according to the full-scale input frequency. C_2 smooths the output voltage waveform. Larger values of C_2 reduce the ripple in the output voltage. Smaller values of C_2 allow the output voltage to settle faster in response to a change in input frequency. Resistor R_1 can be trimmed to achieve the desired output voltage at the full-scale input frequency.

PRINCIPLES OF OPERATION

The VFC32 operates on a principle of charge balance. The signal input current is equal to V_{IN}/R_1. This current is integrated by input op amp and C_2, producing a downward ramping integrator output voltage. When the integrator output ramps to the threshold of the comparator, the one-shot is triggered. The 1mA reference current is switched to the integrator input during the one-shot period, causing the integrator output ramp upward. After the one-shot period, the integrator again ramps downward.

The oscillation process forces a long-term balance of charge (or average current) between the input signal current and the reference current. The equation for charge balance is:

$$I_{IN} = I_{R(AVERAGE)} \qquad (2)$$

$$\frac{V_{IN}}{R_1} = f_O t_{OS}(1mA) \qquad (3)$$

Where:
 f_O is the output frequency
 t_{OS} is the one-shot period, equal to
 $t_{OS} = 7500\ C_1$ (Farads) $\qquad (4)$

The values suggested for R_1 and C_1 are chosen to produce a 25% duty cycle at full-scale frequency output. For full-scale frequencies above 200kHz, the recommended values produce a 50% duty cycle.

$$C_1 = \frac{33,000pF}{f_{FS\ (kHz)}} - 30pF$$
$$R_1 = 40k\Omega$$

Above 200kHz Full-Scale
$$C_1 = \frac{66,000pF}{f_{FS\ (kHz)}} - 30pF$$
$$R_1 = 20k\Omega$$

FIGURE 2. Capacitor Value Selection.
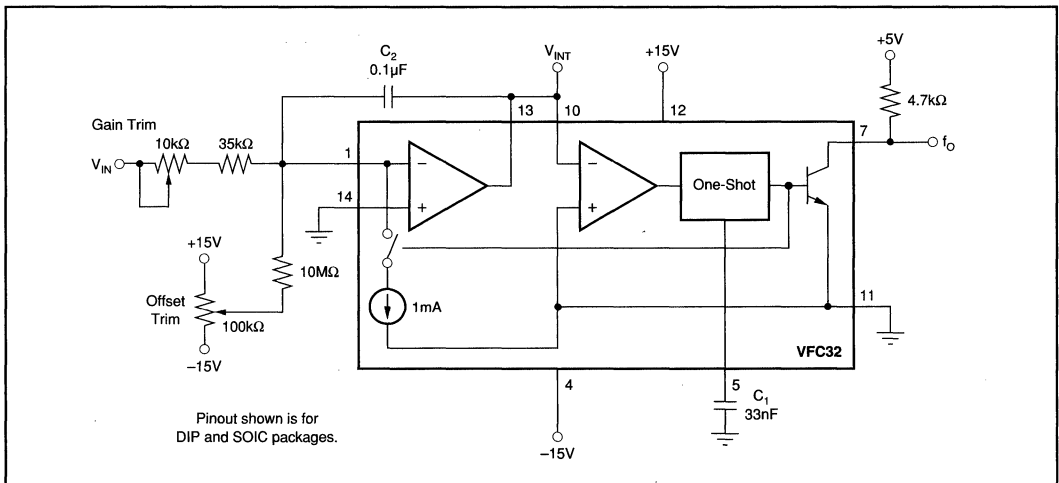
FIGURE 3. Gain and Offset Voltage Trim Circuit.

VFC32

VOLTAGE-TO-FREQUENCY CONVERTERS

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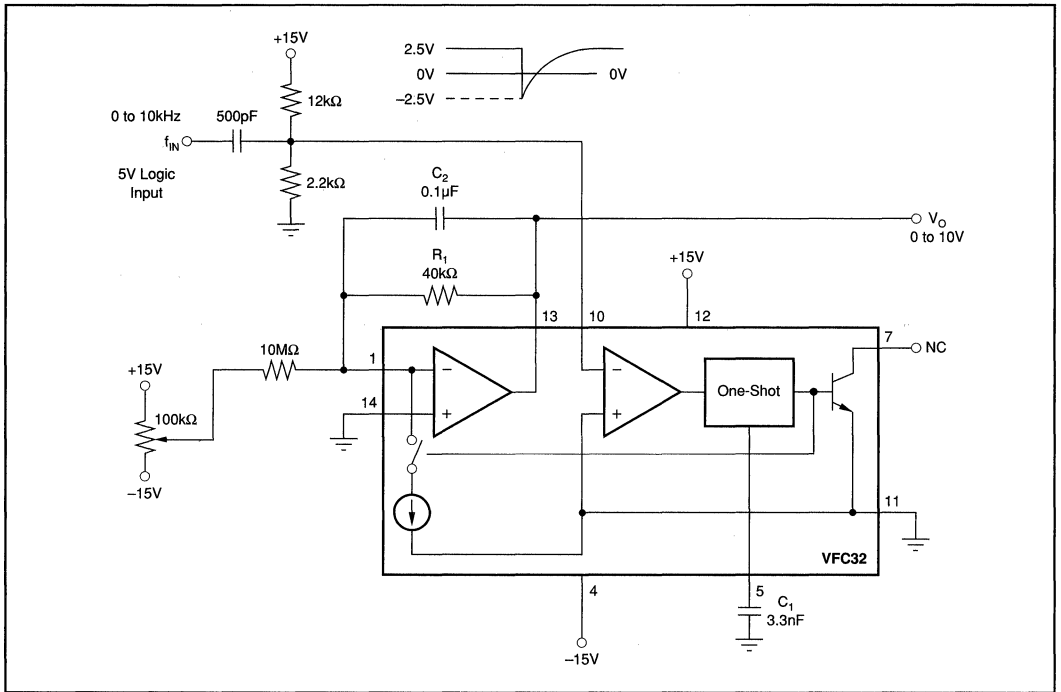
FIGURE 4. Frequency-to-Voltage Converter Circuit.
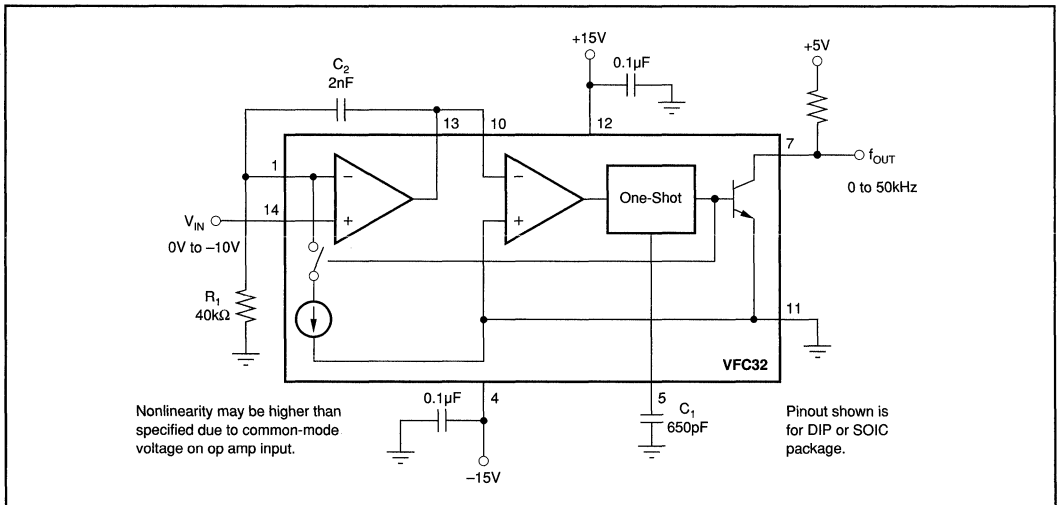
FIGURE 5. V/F Converter—Negative Input Voltage.

BURR - BROWN®
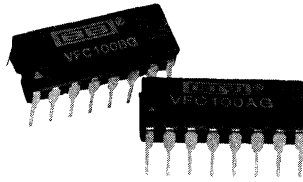
VFC100

Synchronized
VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

● **FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK; NO CRITICAL EXTERNAL COMPONENTS REQUIRED**

● **PRECISION 10V FULL-SCALE INPUT, 0.5% max GAIN ERROR**

● **ACCURATE 5V REFERENCE VOLTAGE**

● **EXCELLENT LINEARITY:**
  0.02% max at 100kHz FS
  0.1% max at 1MHz FS

● **VERY LOW GAIN DRIFT: 50ppm/°C**

APPLICATIONS

● **A/D CONVERSION**
● **PROCESS CONTROL**
● **DATA ACQUISITION**
● **VOLTAGE ISOLATION**

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used; however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly uesful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.

VFC100

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VOLTAGE-TO-FREQUENCY CONVERTERS

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG			VFC100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	f_{OUT} = f_{CLOCK} x (V_{IN}/20V)							
Gain Error[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	% of FSR[4]
Linearity Error	FSR = 100kHz, Over Temperature		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.015			*	±0.05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.025			*	±0.1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			±70	±100		±30	±50	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6.5	±25	μV/°C
Power Supply Rejection	Full Supply Range			0.01			*	%/V
Response Time	To Step Input Change	One Period of New Output Frequency Plus One Clock Period						
Current-to-Frequency Mode	f_{OUT} = f_{CLOCK} x (I_{IN}/1mA)							
Gain Error			±0.5	±1		±0.2	±0.5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	V_{OUT} = 20V x (f_{IN}/f_{CLOCK})							
Gain Accuracy[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	%
Linearity	FSR = 100kHz		±0.01	±0.025		*	±0.02	%
Input Resistor (R_{IN})								
Resistance		19.8	20	20.2	*	*	*	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	μV
V_{OS} Drift			±5			*		μV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dBV
CM Range		−7.5		+0.1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	−0.2		+12		*	*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Current (Operating)	−11V < $V_{COMPARATOR}$ < +V_{CC} − 2V			5			*	μA
CLOCK INPUT								
(Referred to Digital Common)								
Frequency (Maximum Operating)			4			*		MHz
Threshold Voltage			1.4			*		V
	Over Temperature	0.8		2	*		*	V
Voltage Range (Operating)		−V_{CC} + 2V		+V_{CC}	*		*	V
Input Current	−V_{CC} < V_{CLOCK} < +V_{CC}		0.5	5		*	*	μA
Rise Time				2			*	μs
OPEN COLLECTOR OUTPUT								
(Referred to Digital Common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (Off Leakage)	V_{OH} = 30V		0.01	10		*	*	μA
Delay Time, Positive Clock								
Edge to Output Pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT	Nominal PW_{OUT} = (5ns/pF) x C_{OS} − 90ns							
Pulse Width Out	C_{OS} = 300pF	1	1.4	2	*	*	*	μs
REFERENCE VOLTAGE								
Accuracy	No Load	4.9	5	5.1	4.95	*	5.05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	Sourcing Capability	10				*		mA
Power Supply Rejection				0.015			0.015	%/V
Output Impedance			0.5	2		*	*	Ω

ELECTRICAL (CONT)

At $T_A = +25°C$ and $±15VDC$ supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG			VFC100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range								
(See Figure 9)	$+V_{CC}$	+7.5		+28.5	*		*	V
	$-V_{CC}$	-7.5		-28.5	*		*	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	*		*	V
Digital Common		$-V_{CC} + 2$		$+V_{CC} - 4$	*		*	V
Quiescent Current: $+I_{CC}$	Over Temperature		10.6	15		*	*	mA
$-I_{CC}$			9.6	15		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-65		+150	*		*	°C
θ_{JA}			150			*		°C/W
θ_{JC}			100			*		°C/W

* Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (max. – min.) ÷ (FSR x ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements. (4) FSR = Full Scale Range.

DICE INFORMATION
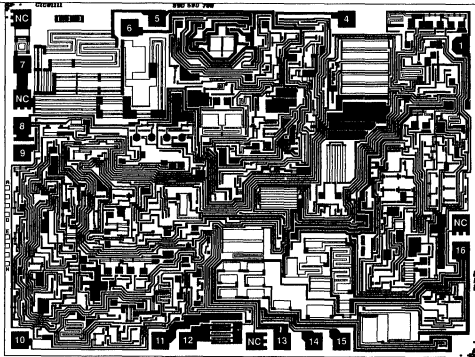
VFC100 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	$+V_{CC}$	9	C_{OS}
2	NC	10	Clock Input
3	NC	11	f_{OUT}
4	Integrator Out	12	Digital Common
5	C_{INT}	13	Analog Common
6	Noninverting In	14	–Comparator In
7	V_{IN}	15	+Comparator In
8	$-V_{CC}$	16	V_{REF}

NC: No Connection
Substrate Bias: Electrically connected to –V supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	141 x 107 ±5	3.58 x 2.72 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC100AG	16-Pin Ceramic DIP	129
VFC100BG	16-Pin Ceramic DIP	129

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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VOLTAGE-TO-FREQUENCY CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_{CC}$ to $-V_{CC}$) 36V
$+V_{CC}$ to Analog Common 28V
$-V_{CC}$ to Analog Common 28V
Integrator Out Short-Circuit to Ground .... Indefinite
Integrator Differential Input .... ±10V
Integrator Common-Mode Input .... $-V_{CC}$ +5V to +2V
V_{IN} (pin 7) .... ±V_{CC}
Clock Input .... ±V_{CC}
V_{REF} Out Short-Circuit to Ground .... Indefinite
Pin 9 (C_{OS}) .... 0 to +V_{CC}
f_{OUT} (referred to digital common) .... −0.5V to 36V
Digital Common .... ±V_{CC}
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (soldering, 10s) .... 300°C

PIN CONFIGURATION
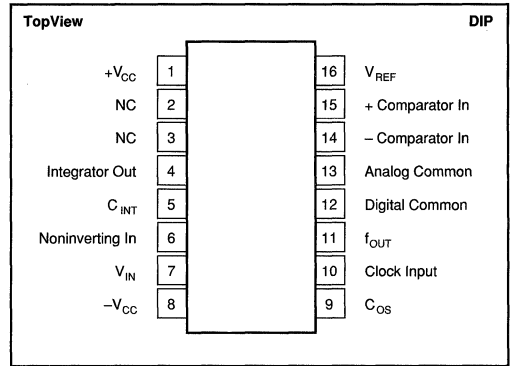
TopView   DIP

+V_{CC}	1	16	V_{REF}
NC	2	15	+ Comparator In
NC	3	14	− Comparator In
Integrator Out	4	13	Analog Common
C_{INT}	5	12	Digital Common
Noninverting In	6	11	f_{OUT}
V_{IN}	7	10	Clock Input
−V_{CC}	8	9	C_{OS}

TYPICAL PERFORMANCE CURVES

At +25°C, ±V_{CC} = 15VDC, and in circuit of Figure 1.

QUIESCENT CURRENT vs TEMPERATURE

REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT
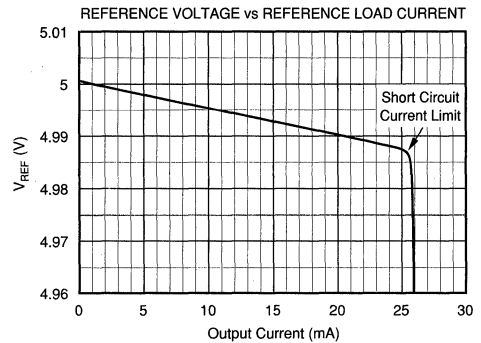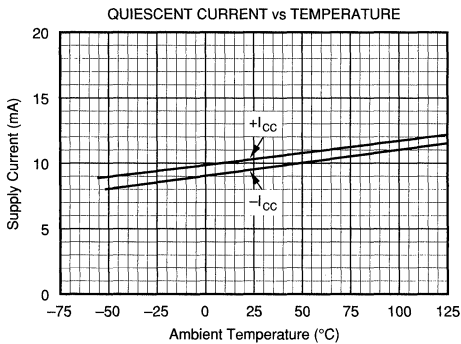
THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S_1 is closed

for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting
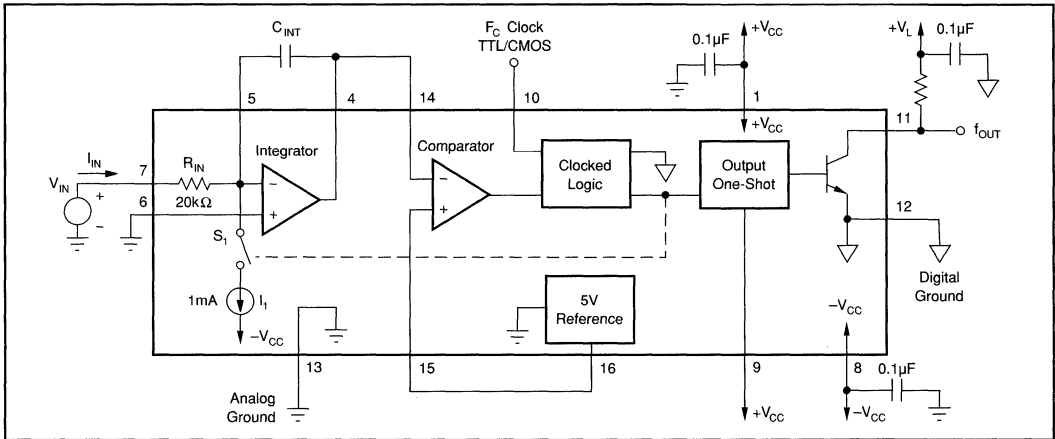
FIGURE 1. Circuit Diagram for Voltage-to-Frequency Mode.
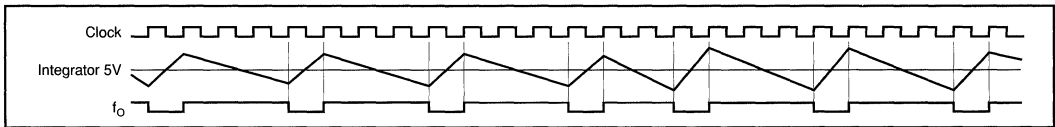
FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to half the clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V) f_{CLOCK}.$$

Figure 3 shows the transfer function graphically. Note that inputs above 10V (or 0.5mA) do not cause an increase in output frequency. This is an easily detectable indication of an overrange input. In the overrange condition, the integrator amplifier will ramp to its negative output swing limit.

When the input signal returns to within the linear range, the integrator amplifier will recover and begin ramping upward during the reset period.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate

FIGURE 3. Transfer Function for Voltage-to-Frequency Mode.

* This is the maximum swing of the integrator output voltage referred to the comparator noninverting input voltage.
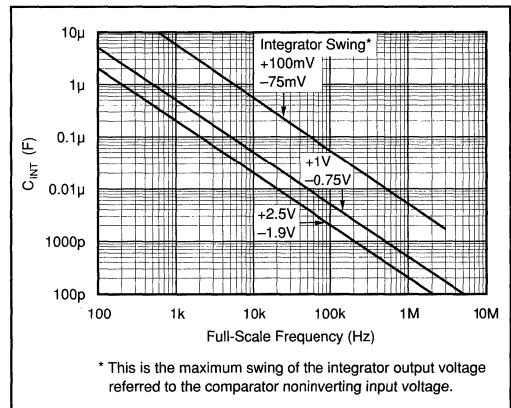
FIGURE 4. Integrator Capacitor Selection Graph.

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VOLTAGE-TO-FREQUENCY CONVERTERS

standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar®, polycarbonate, mica, polystyrene, Teflon® and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to –0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without integrator output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and $C_{INT} = 0.1\mu F$, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1Vp-p superimposed 60Hz noise.

The integrator output voltage should not be allowed to exceed +12V or –0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supply Considerations" for information on low voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 12). One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 12). The clock "high" input may be standard TLL or may be as high as $+V_{CC} - 2V$. A CMOS clock should be powered from a voltage source at least 2V below the VFC100's $+V_{CC}$ to prevent overdriving the clock input. Alternatively, a resistive voltage divider may be used to limit the clock voltage swing to $+V_{CC} - 2V$ maximum. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.8V to 2V must be less than 2µs for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the output transistor is on only during the reset integration period (see

"Shortened Output Pulses"). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse, where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC100 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels; the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This is normal. Experimentation with the input voltage and oscilloscope triggering generally allows a stable view of the output and provides an understanding of its nature.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 9 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100ns. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Excellent gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not required for this function). The reference is very useful for handling bipolar
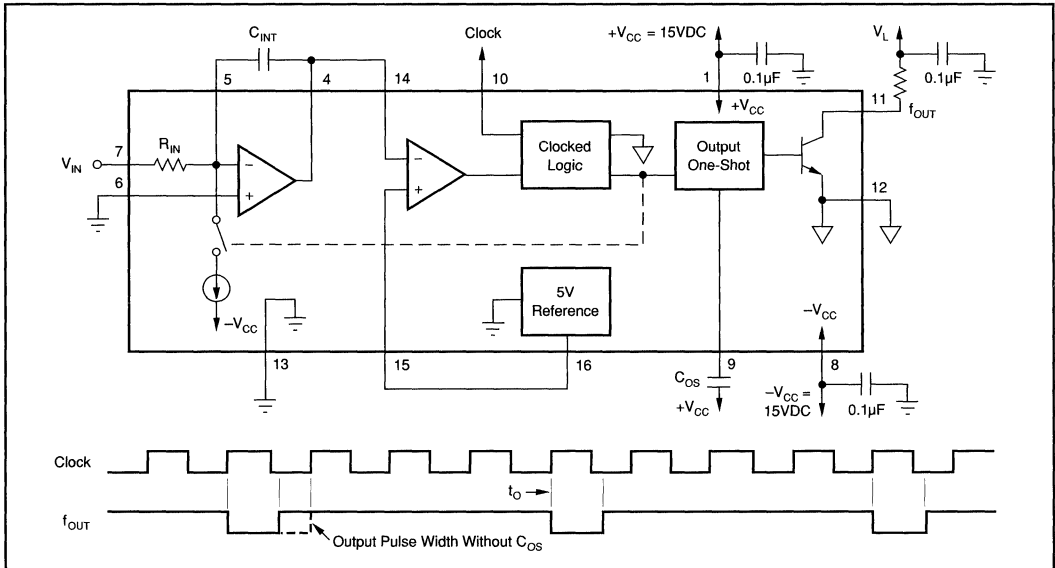
FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.
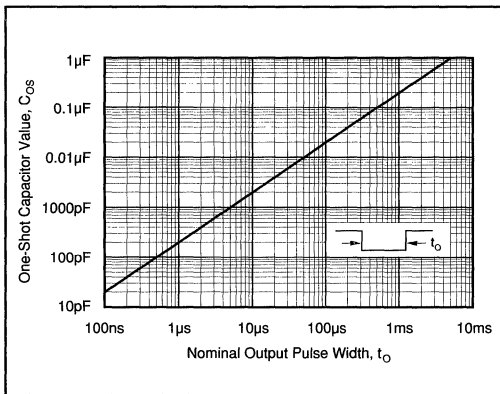
FIGURE 6. Output One-Shot Capacitor Selection.

input signals in many other applications, such as offsetting the input. It can source up to 10mA and sink 100μA. Heavy loading of the reference will change the gain of the VFC and affect the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

Figure 7 shows the reference used to offset the VFC transfer function, to convert a –5V to +5V input to 0–500kHz output. The circuit in Figure 8 uses the reference to excite a 300Ω bridge transducer. R_1 provides the majority of the current to the bridge while the V_{REF} output supplies the balance and accurately controls the bridge voltage. The VFC gain is inversely proportional to the reference voltage, V_{REF}. Since the bridge gain is directly proportional to its excitation voltage, the two equal and opposite effects cancel the effect of reference voltage drift on gain.

The reference output amplifier is specifically designed for excellent transient response, to provide precision in a noisy environment.

OTHER INPUT VOLTAGE RANGES

The internal input resistor, $R_{IN} = 20kΩ$, sets a full-scale input of 10V. Other input ranges can be created by using an external gain set resistor connected to pin 5. Since the excellent temperature drifts of the VFC100 are achieved by careful matching of internal temperature coefficients, use of an external gain set resistor will generally degrade this drift. Using an external resistor to set the gain, the resulting gain drift would be equal to the sum of the external resistor drift and the specified current gain drift of the VFC100. Different voltage input ranges are best implemented by using the internal input resistor, R_{IN}, in series or parallel with a high quality external resistor, thus maintaining as much of the precision temperature tracking as possible.

For best drift performance, the adjustment range of a fine gain trim should be made as narrow as practical. R_1 and R_2 in Figure 9 allow gain adjustments over a ±1% range (adequate to trim the 100kHz FS gain error to zero) and will not significantly affect the drift performance of the VFC100. R_3, R_4 and R_5 allow trimming of the integrator amplifier input offset voltage. The adjustment range is determined by the ratio of R_4 to R_5. Accurate end-point calibration would be performed by first adjusting the offset trim so that zero volts input just causes all output pulses to cease. The gain trim is then adjusted for the proper full-scale output frequency with an accurate full-scale input voltage.

A different input voltage range could also be made by using only a portion of the normal input range of the VFC. For instance, a 2V full-scale input could be created by using the

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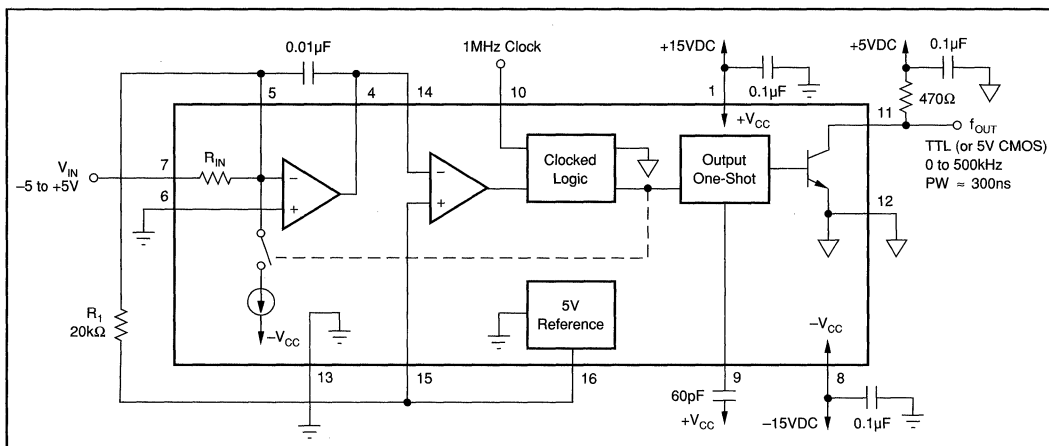
FIGURE 7. Circuit Diagram for Bipolar Input Voltages.
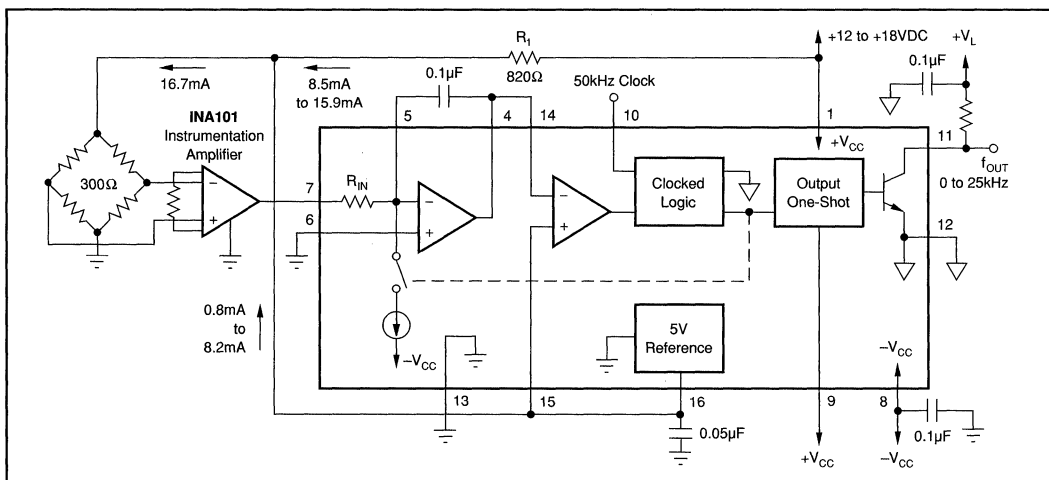
FIGURE 8. Circuit Diagram for Bridge Excitation Using V_{REF}.

internal input resistor and a clock frequency of 10 times the desired full-scale output frequency.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale end point measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating frequency as shown in Figure 10. Figure 11 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. A small integrator voltage swing typically leads to best linearity performance.

The best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC100 circuit is totally determined by the performance of the VFC100. Gain drift is specified at a full-scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly
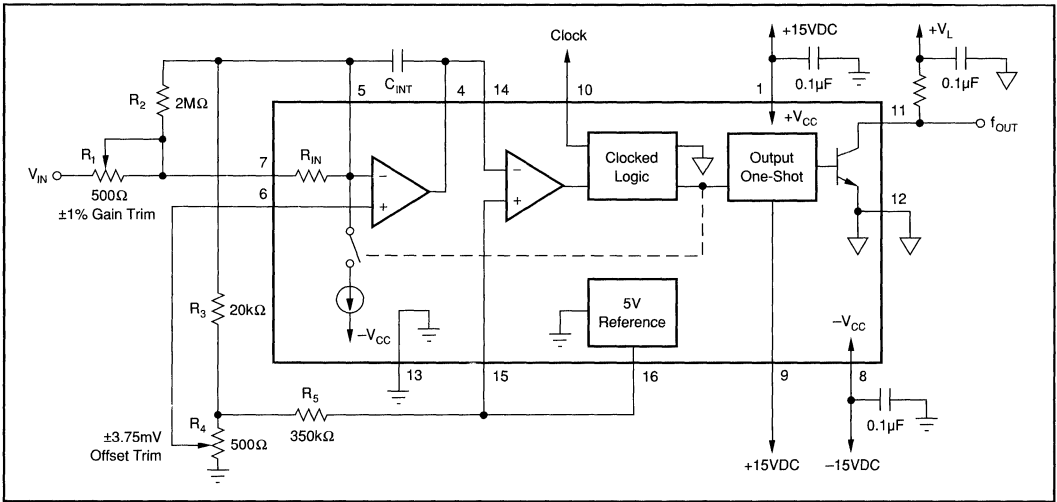
FIGURE 9. Circuit Diagram for Fine Offset and Gain Trim.
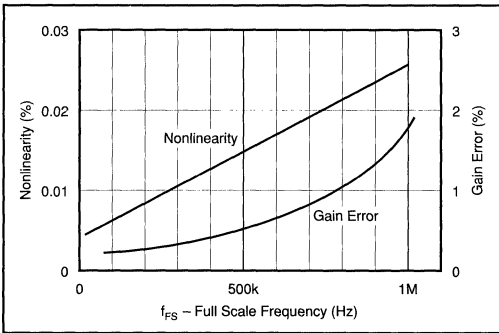
FIGURE 10. Typical Nonlinearity and Gain Error vs Full Scale Frequency.
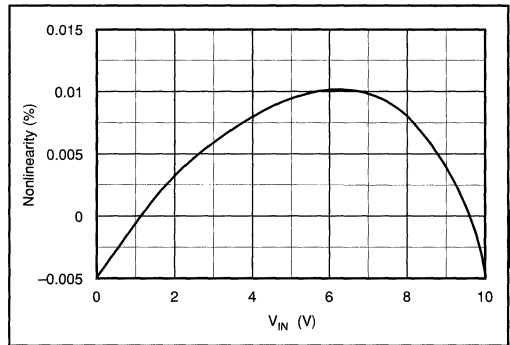
FIGURE 11. Typical Nonlinearity vs V_{IN}. ($f_{FS} = 0.1$MHz)

at higher operating frequency. The VFC100's gain drift remains excellent at higher operating frequency, typically remaining within specifications at $f_{FS} = 1$MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry, this drift can be cancelled (see "Counting the Output").

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC100 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V

V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of $0.1\mu F$ is adequate for most circuit layouts.

The VFC100 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too

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small, however, or the negative output limitation of the integrator (–0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see "Integrator Capacitor").

Figure 12 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to –75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationship of the allowable operating voltage ranges on important pins is show in Figure 13. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high frequency performance. It is this characteristic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

COUNTING THE OUTPUT

In evaluation and use of the VFC100, you may want to measure the output frequency with a frequency counter. Since synchronization of the VFC100 causes it to await a clock edge for any given output pulse, the output frequency is essentially quantized. The quantized steps are equal to one clock period of the counting gate period. The quantizing error can be made arbitrarily small by counting with long gate times. For instance, a one-second counter gate period with a 100kHz full-scale frequency has a resolution of one part in 100,000. Many of the more sophisticated laboratory frequency counters, however, use period measurement schemes to count the input frequency quickly. These instruments work equally well, but the gate period must be set appropriately to achieve the desired count resolution. Short gate periods will produce many digits of "accuracy" in the display, but the results may be very inaccurate.

Figure 14 is a typical system application showing a basic counting technique. A 0 to 10V input is converted to a 0 to 100kHz frequency output. The VFC's clock is divided by M = 4000 to produce a gate period for the counter circuit. The resulting VFC count, N, is insensitive to variations in the actual clock frequency. The input voltage represented by the resulting count is $V_{IN} = (N/M)\ 20V$.

Resolution is related to the number of counts at full scale, or half the number of clock pulses in the gate period.

The integrating nature of the VFC is important in achieving accurate conversions. The integrating period is equal to the counting period. This can be used to great advantage to reject unwanted signals of a known frequency. Figure 15 shows that response nulls occur at the inverse of the integration period and its multiples. If 60Hz is to be rejected, for instance, the counting period should be made equal to, or a multiple of, 1/60 of a second.
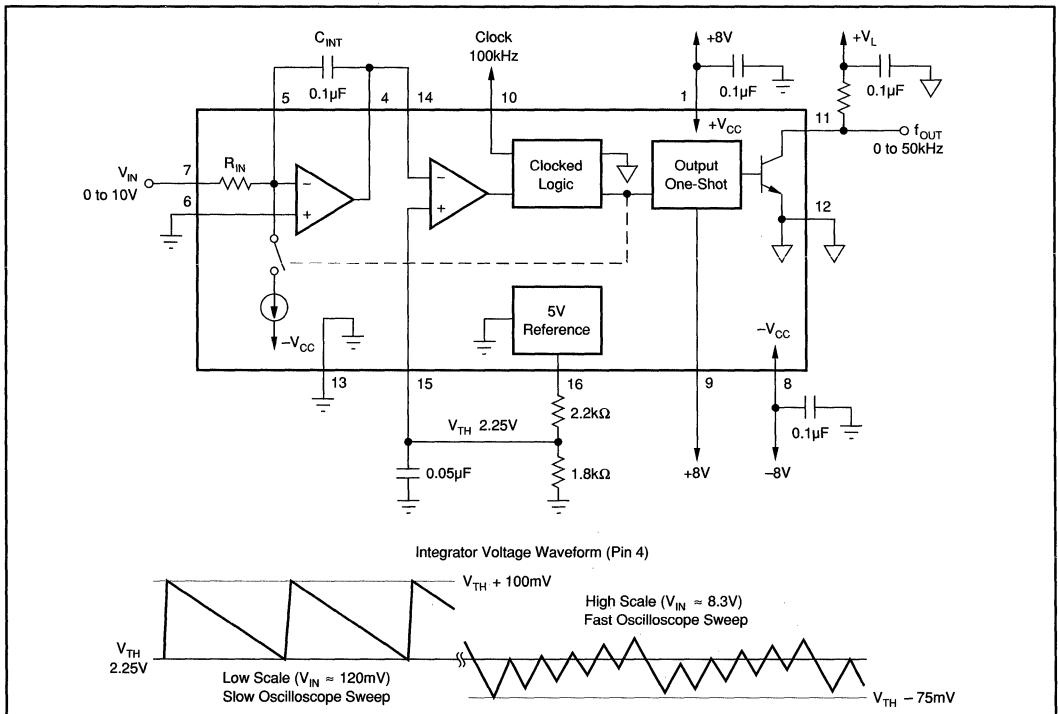
FIGURE 12. Circuit Diagram and Integrator Voltage Waveform Power Supply Voltage Operation.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by supplying an input frequency to the comparator input as shown in Figure 16. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is $V_{OUT} = (F_{IN}/f_{CLOCK})\ 20V$.

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 16. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200ns before a negative clock edge and rise no sooner
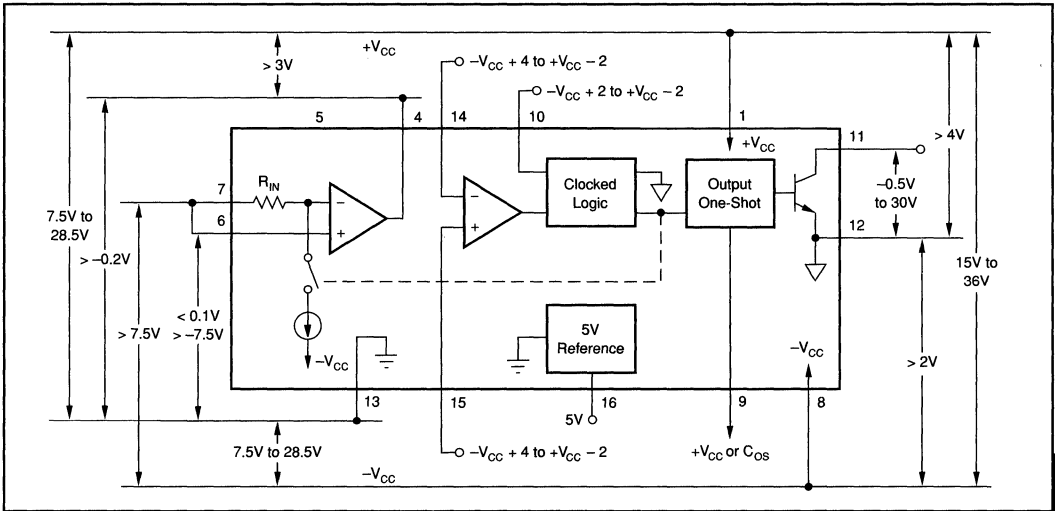
FIGURE 13. Relationships of Allowable Voltages.
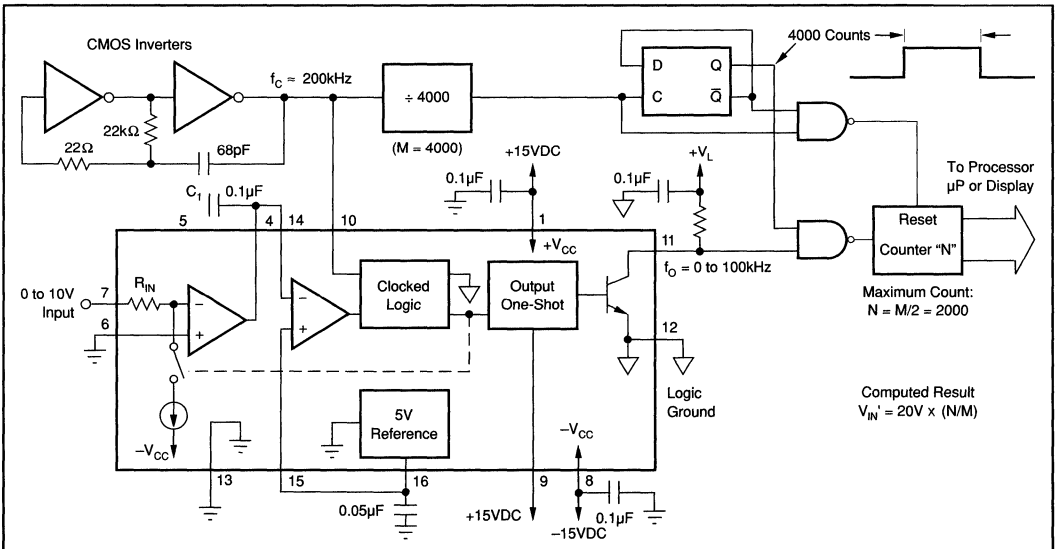
FIGURE 14. Diagram of a Voltage-to-Frequency Converter and Counter System.

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than 200ns after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 17 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.
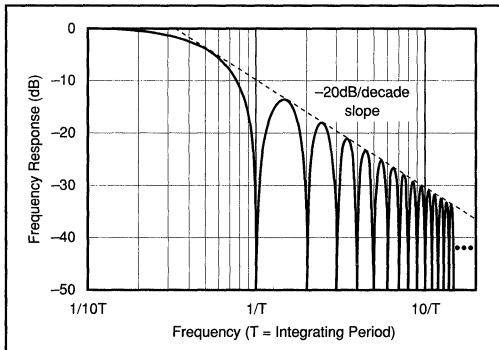
Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capaci-

tor. Figure 18 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

The system in Figure 20 makes use of both voltage-to-frequency and frequency-to-voltage modes to send a signal across an optically isolated barrier. This technique is useful not only for providing safety in the presence of high voltages, but also for creating high noise rejection in electrically noisy environments. The use of a common clock frequency causes the two devices to have complementary transfer functions, which minimizes errors.

Optical coupling is facilitated by use of the output one-shot feature. The output pulse is shortened (see "Shortened Output Pulses") to allow for the relatively slow turn-off time of the LED. The timing diagram in Figure 19 shows how the accumulated delay of both optical couplers could produce too long an input pulse for the frequency-to-voltage converter, VFC_2, of Figure 20.

An output filter is used to reduce the ripple in the output of VFC_2. In order to most effectively filter the output, both input and output VFCs are offset. By connecting R_1 to V_{REF},

FIGURE 15. Frequency Response of an Integrating Analog-to-Digital Converter.
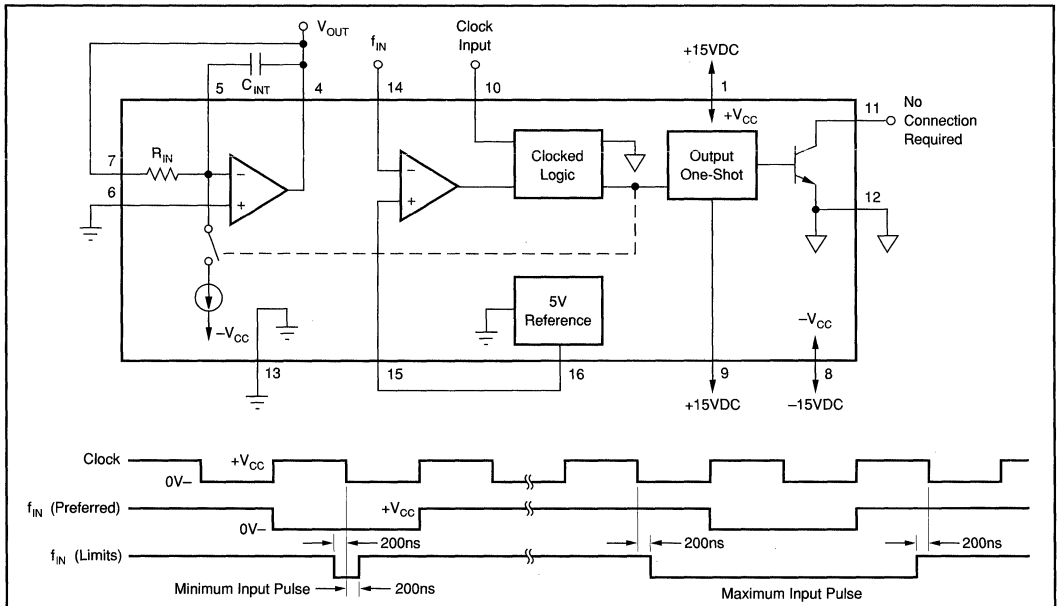
FIGURE 16. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.
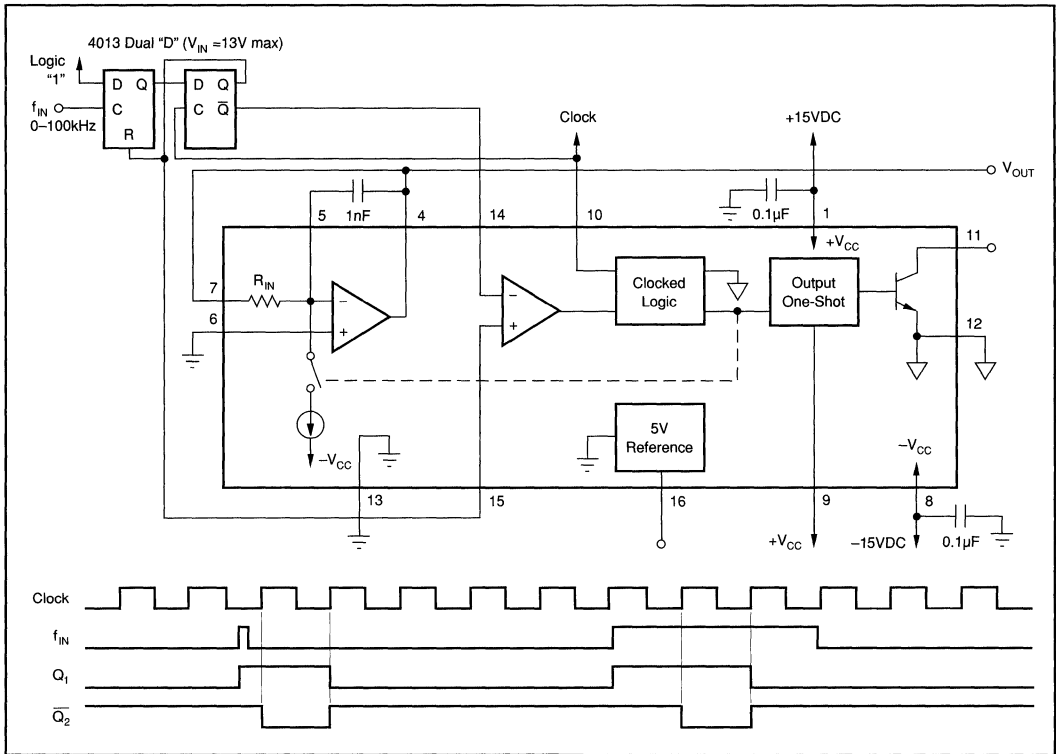
FIGURE 17. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.
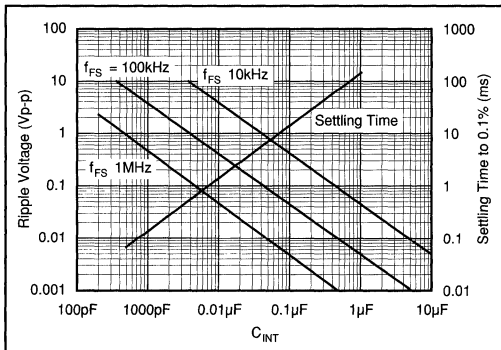
FIGURE 18. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

an accurate offset is created in the voltage-to-frequency function. Zero volts input now creates a 10kHz output. This offset is subtracted in the frequency-to-voltage conversion on the output side, by V_{REF} and R_5.

MORE PULSE POSITION RESOLUTION

Since output pulses must always align with clock edges, the instantaneous output frequency is quantized and appears to have phase jitter. This effect can be greatly reduced by using

a high speed clock so that available clock edges come more frequently. This would also create a high full-scale frequency, but the technique shown in Figure 21 offers an alternative. A high speed clock is used to produce high resolution of the output pulse position, but a low full-scale frequency can be programmed.

When an output pulse is generated, the next rising edge of the high frequency clock is delayed for a programmable number of clock counts. Since the integrator reset period (which sets the full-scale range) is determined by the time from rising edge to rising edge at the VFC's clock input once the comparator is tripped, the effective clock frequency is $f_{CLOCK}/16$. The circuit shown can be programmed for an N from 2 to 16. Since an output pulse must propagate through the VFC before the next rising edge of the clock arrives, maximum clock frequency is limited by the delay time shown in the timing diagram.

With output pulses now able to align with greater resolution, the output has lower phase jitter. Using this technique, the output is suitable for ratiometric (period measurement) type counting. This counting technique achieves the maximum possible resolution for short gate periods (see Burr-Brown Application Note AN-130).

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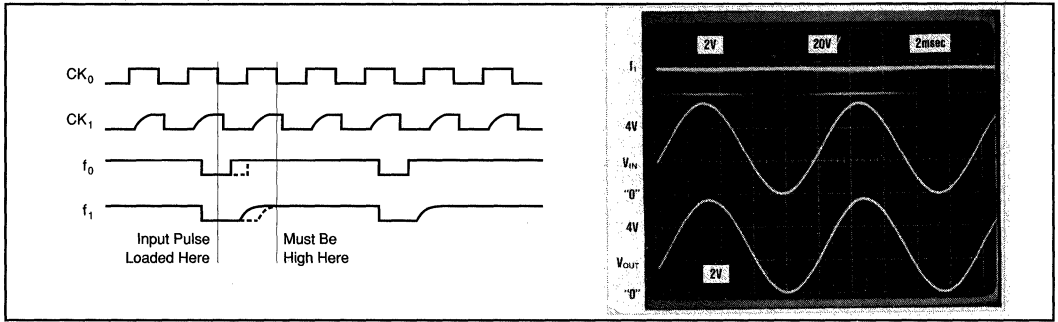
FIGURE 19. Timing Diagram and Oscilloscope Trace of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.
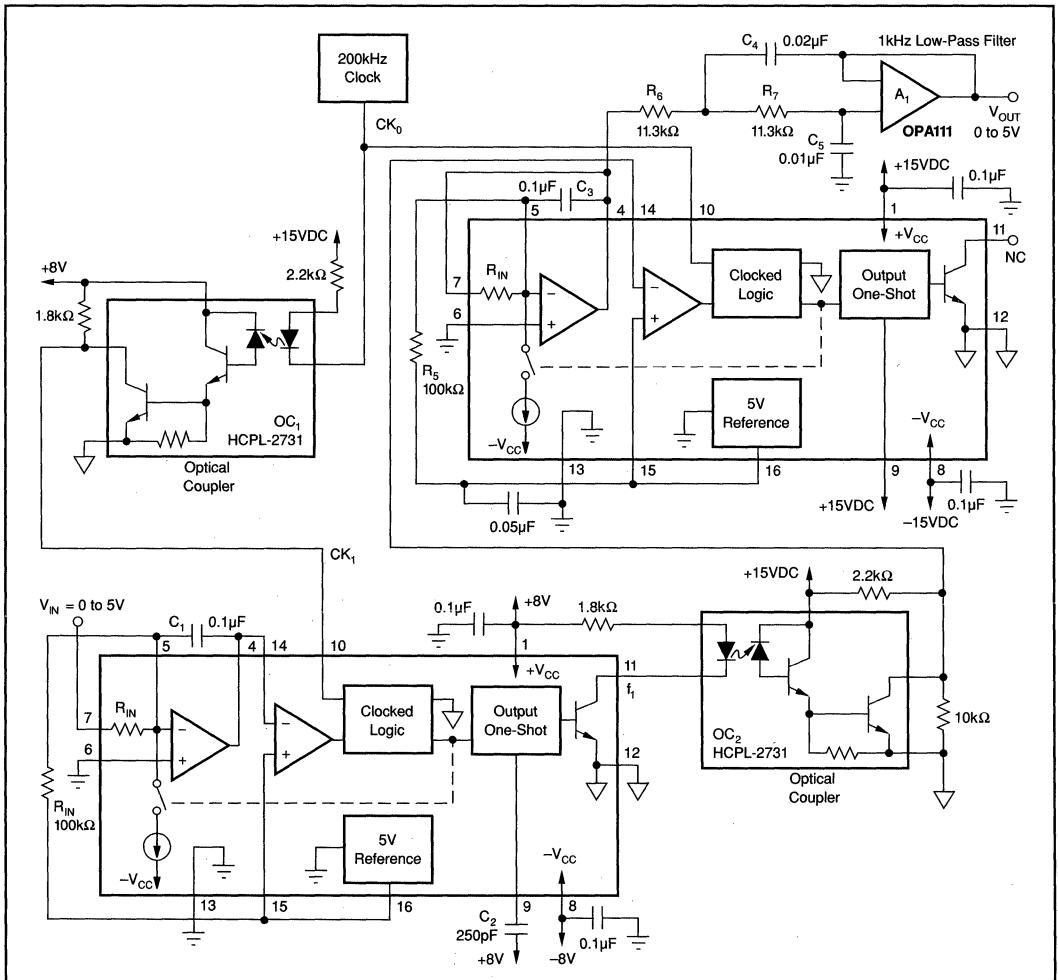
FIGURE 20. Circuit Diagram of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.
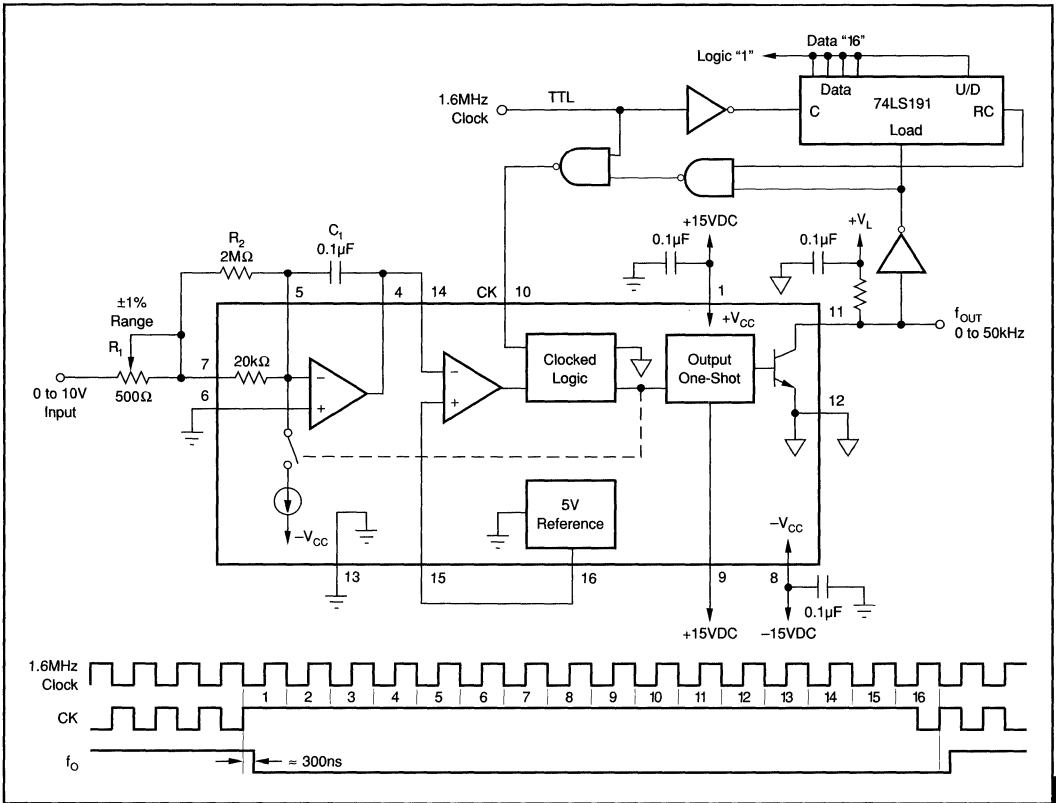
FIGURE 21. Circuit Diagram for Increased Pulse Position Resolution.

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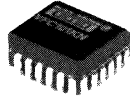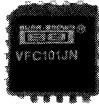
VFC101

Synchronized
VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

● **FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK**

● **MULTIPLE INPUT RANGES:**
   5V, 8V, 10V Full Scale

● **ACCURATE 5V REFERENCE VOLTAGE**

● **LOW NONLINEARITY:**
   0.02% max at 100kHz FS

● **LOW GAIN DRIFT: 40ppm/°C**

APPLICATIONS

● **INTEGRATING A/D CONVERTER**

● **MULTICHANNEL DATA ACQUISITION**

● **FREQUENCY-TO-VOLTAGE CONVERSION**

● **VOLTAGE ISOLATION**

DESCRIPTION

The VFC101 voltage-to-frequency converter uses the proven charge-balance technique with internal digital logic to control the critical reference integration period. Reference timing is derived from an external clock signal which accurately sets the full-scale frequency. This technique eliminates the errors and drift from external timing components which are required with other VFCs.

Internal resistors provide accurate full-scale input ranges of 5V, 8V or 10V inputs without external resistors or trimming. An accurate 5V reference voltage output is useful for bridge or sensor excitation. With simple pin interconnections, it can provide half-scale offset to allow bipolar input voltages.

The open-collector frequency output interfaces easily to CMOS or TTL circuitry. Output one-shot circuitry may be used to optimize the output pulse width for optical couplers or transformers.

The VFC101 is packaged in a surface-mount 20-pin PLCC (plastic leaded chip carrier) package.

PDS-779B

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC101JN			VFC101KN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK}(V_{IN}/2V_{FS})$							
Gain Error[1]	FSR[2] = 100kHz		±0.3	±0.5		*	*	% of FSR
Linearity Error	FSR = 100kHz, Over Temperature		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.02	±0.05		*	*	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.05	±0.1		*	*	% of FSR
Gain Drift[2]	FSR = 100kHz		±50	±80		±30	±40	ppm of FSR/°C
Referred to Internal V_{REF}			10	±25		*	±15	ppm of FSR/°C
Offset Referred to Input			±1	±3		*	±2	mV
Offset Drift			±12	±100		±6.5	±25	μV/°C
Power Supply Rejection	Full Supply Range			0.02			0.015	%/V
Response Time	To Step Input Change	One Period of New Output Frequency Plus One Clock Period						
Frequency-to-Voltage Mode	$V_{OUT} = 2V_{FS}(f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.3	±0.5		*	*	%
Linearity Error	FSR = 100kHz		±0.01	±0.025		*	±0.02	%
Input Resistors								
Resistance			±30			*		%
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	μV
V_{OS} Drift			±5	±25		*	±15	μV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dB
CM Range		−7.5		+0.1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	−0.2		+12	*		*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Bias Current (I_S)	$−V_{CC} + 4V < V_{IN} < +V_{CC}$			5			*	μA
CLOCK INPUT (Referenced to Digital Common)								
Frequency (maximum operating)			4			*		MHz
Threshold Voltage			1.4			*		V
	Over Temperature	0.8		2	*		*	V
Voltage Range		$−V_{CC} + 3$		$+V_{CC}$	*		*	V
Input Current			0.5	5		*	*	μA
Rise Time				2			*	μs
OPEN COLLECTOR OUTPUT (Referenced to Digital Common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (off leakage)	V_{OUT} = 30V		0.01	10		*	*	μA
Delay Time, Positive Clock								
Edge to Output Pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT								
Pulse Width Out	Nominal PW_{OUT} =	1	1.4	2	*	*	*	μs
	(5ns/pF) x C_{OS} − 90ns; C_{OS} = 300pF							
REFERENCE VOLTAGE								
Accuracy	No Load	4.9	5	5.1	4.95	*	5.05	V
Drift[2]			±60	±105		±40	±55	ppm/°C
Current Output (sourcing)		10			*			mA
Power Supply Rejection				0.015			*	%/V
Output Impedance			0.5	2		*	*	Ω
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range	$+V_{CC}$	+7.5		+28.5	*		*	V
	$−V_{CC}$	−7.5		−28.5	*		*	V
Total Supply	$+V_{CC} − (−V_{CC})$	15		36	*		*	V
Digital Common		$−V_{CC} + 2$		$+V_{CC} − 4$	*		*	V
Quiescent Current: $+I_{CC}$	Over Temperature		10.6	15		*	*	mA
$−I_{CC}$			9.6	15		*	*	mA

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SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC101JN MIN	VFC101JN TYP	VFC101JN MAX	VFC101KN MIN	VFC101KN TYP	VFC101KN MAX	UNITS
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		−65		+150	*		*	°C
θ_{JA}			90			*		°C/W
θ_{JC}			35			*		°C/W

* Specification same as JN grade.
NOTES: (1) Offset and gain error can be trimmed to zero. (2) Specified by the box method: (max − min) ÷ (Avg x ΔT).

PIN CONFIGURATION

Top View

20-Pin
PLCC
Package

Grade
Designation

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (+V_{CC} to −V_{CC}) 36V
+V_{CC} to Analog Common 28V
−V_{CC} to Analog Common 28V
Integrator Out Short-Circuit to Ground .... Indefinite
Integrator Differential Input .... ±10V
Integrator Common-Mode Input .... −V_{CC} +5V to +2V
V_{IN} (pins 7, 8, 9, 10) .... ±V_{CC}
Clock Input .... ±V_{CC}
V_{REF} Out Short-Circuit to Ground .... Indefinite
C_{OS} (Pin 12) .... 0 to +V_{CC}
f_{OUT} (referred to digital common) .... −0.5V to 36V
Digital Common .... ±V_{CC}
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC101JN	20-Pin PLCC	0°C to +70°C
VFC101KN	20-Pin PLCC	0°C to +70°C

PIN ASSIGNMENTS

PIN #	DESCRIPTION
1	NC
2	+V_{CC} Power Supply
3	NC
4	V_{OUT} Integrator Amp Output
5	C_{INT}, Integrator Inverting Input
6	+V_{IN}, Integrator Noninverting Input
7	V_{IN}, 5V FS
8	V_{IN}, 10V FS
9	V_{IN}, 8V FS
10	V_{IN}, 10V FS
11	−V_{CC} Power Supply
12	C_{OS}, Output One-Shot Capacitor
13	f_{CLOCK} Input
14	f_{OUT} Frequency Output
15	Digital Ground
16	Analog Ground
17	− Comparator Input
18	+ Comparator Input
19	NC
20	V_{REF} +5V Reference Output

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC101JN	20-Pin PLCC	181
VFC101KN	20-Pin PLCC	181

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

At +25°C, ±V$_{CC}$ = 15VDC, and in circuit of Figure 1, unless otherwise specified.

QUIESCENT CURRENT vs TEMPERATURE

REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT

NONLINEARITY AND GAIN ERROR
vs FULL-SCALE FREQUENCY

NONLINEARITY vs V$_{IN}$

VFC101

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VOLTAGE-TO-FREQUENCY CONVERTERS

THEORY OF OPERATION

The VFC101 voltage-to-frequency converter provides digital output pulses with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge-balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in C_{INT}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge. On the rising edge, switch SW_1 is closed for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC101 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full-scale input causes a nominal output frequency equal to one-half the clock frequency. The transfer function is $f_{OUT} = (V_{IN}/2V_{FS}) f_{CLOCK}$.

Input voltages greater than V_{FS} cause the output frequency to limit at half the clock frequency. Negative inputs cause all output pulses to cease. The full-scale input voltage, V_{FS}, is determined by the input pin used—see Figure 1.

One of the useful functions made possible by the VFC101's multiple input resistors is shown in Figure 2. By connecting one 10V input to the 5V V_{REF} output, the other 10V input pin functions as a bipolar input. A –5V to +5V input range causes a zero to $f_{CLOCK}/2$ output frequency range. Accurate ratio matching and temperature tracking of the input resistors provides improved stability of the half-scale offset.

INPUT Pin Number	FULL-SCALE VOLTAGE V_{RS}
8	10V
10	10V
9	8V
7	5V
7(1)	2.5V

NOTE: (1) Pin 8 connected to pin 5.
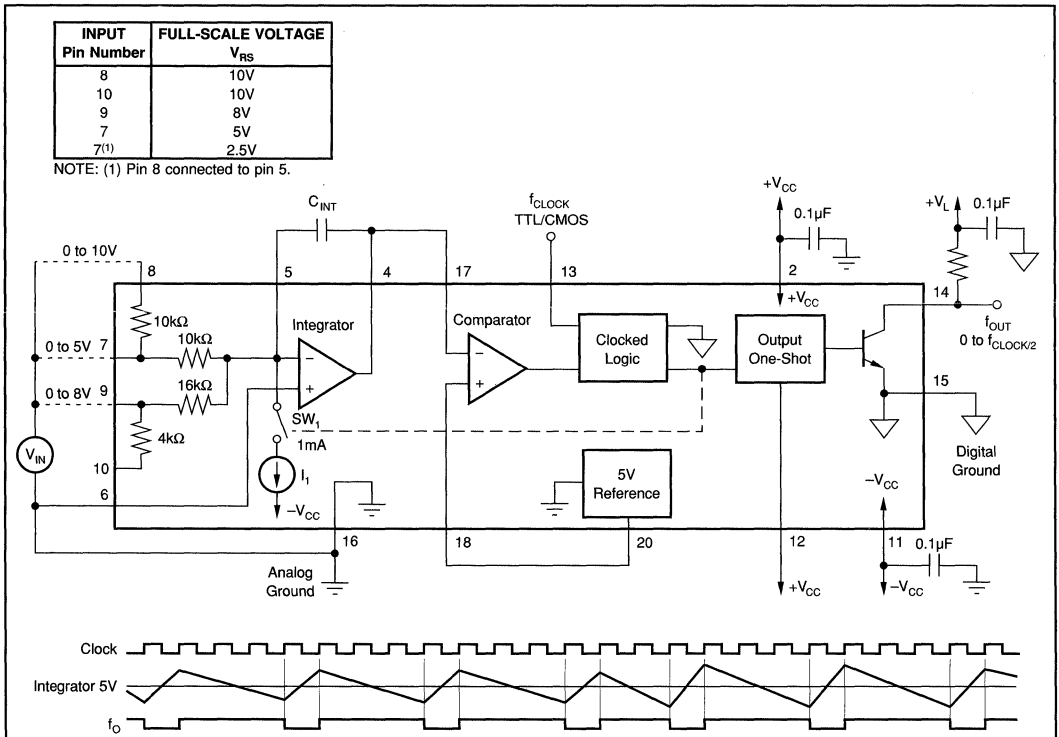
FIGURE 1. Basic Voltage-to-Frequency Operations.
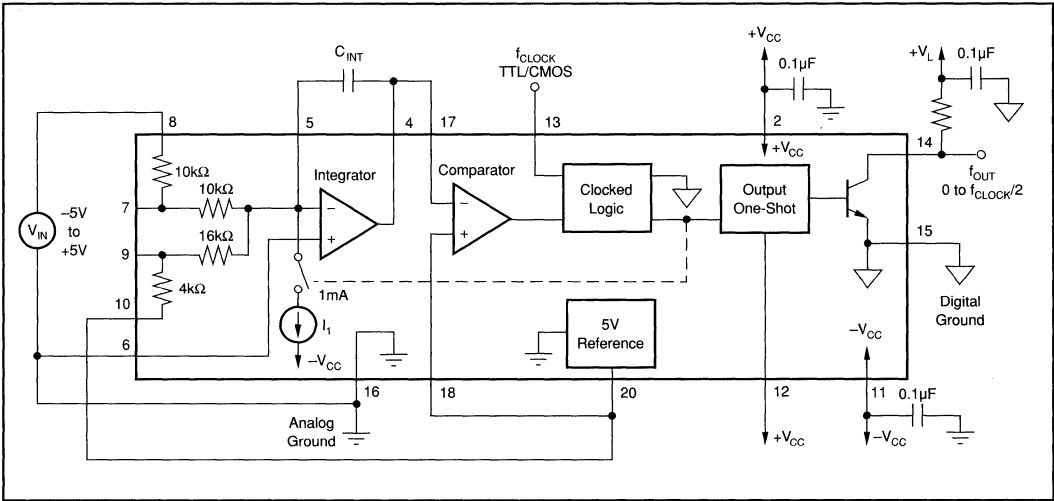
FIGURE 2. Offset for Bipolar Input Voltages.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. Figure 3 facilitates choosing an appropriate standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar™, polycarbonate, mica, polystyrene, Teflon™ and glass types are appropriate choices. Choice will depend on the particular value and size. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to –0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on

FIGURE 3. Integrator Capacitor Selection Graph.

NOTE: (1)This is the maximum swing of the integrator output voltage referred to the comparator noninverting input voltage.

VFC operation. It may be desirable to deviate from the suggested value. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without integrator output saturation and loss of accuracy.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 5.) One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL- and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 15). The clock "high" input may be standard TLL or may be as high as +V_{CC}. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.5V to 2V must be less than 2µs for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active-low during the reset integration period (see "Shortened Output Pulses".)

Interface to a logic circuit normally uses a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capaci-

Mylar™, Teflon™ E. I. du Pont de Nemours & Co.

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VOLTAGE-TO-FREQUENCY CONVERTERS
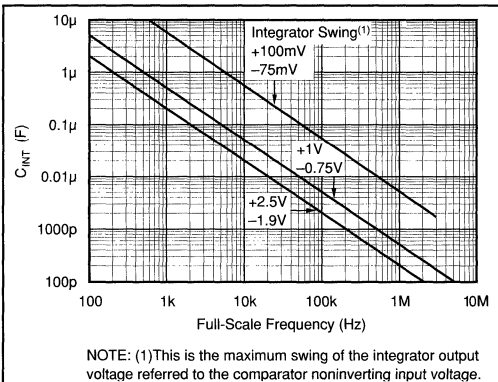
tance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance.

The synchronized nature of the VFC101 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels and the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This behavior amounts to a frequency or phase jitter in the output, making frequency detection with most phase-locked loop circuitry impractical. For the same reason, fast period measurement (ratiometric counting) will not provide a stable reading. The output frequency must be measured (averaged) for N counts of f_{CLOCK} to achieve a stable N counts of resolution.

SHORTENED OUTPUT PULSES

With pin 12 connected to $+V_{CC}$, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 4. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot,

causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100ns. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Low gain. drift is achieved with a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not required for this function). It is very useful in many other applications such as offsetting the input to accept bipolar input signals. It can source up to 10mA and sink 100μA. Heavy loading of the reference will change the gain of the VFC. A 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale end point measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested.

Linearity performance and gain error change with full-scale operating frequency as shown in the typical performance curves. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. A small integrator voltage swing typically leads to best linearity performance.

The best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses

FIGURE 4. Circuit and Timing Diagram for Shortened Output Pulses.

with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC101 circuit is totally determined by the performance of the VFC101. Gain drift is specified at a full-scale output frequency of 100kHz. Gain drift remains excellent at higher operating frequency, typically remaining within specifications at $f_{FS} = 1MHz$.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry, this drift can be cancelled.

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC101 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may even-

tually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1µF is adequate for most circuit layouts.

The VFC101 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V.) This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too small, however, or the negative output limitation of the integrator (–0.2V) may cause saturation. Also, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see Figure 3.)
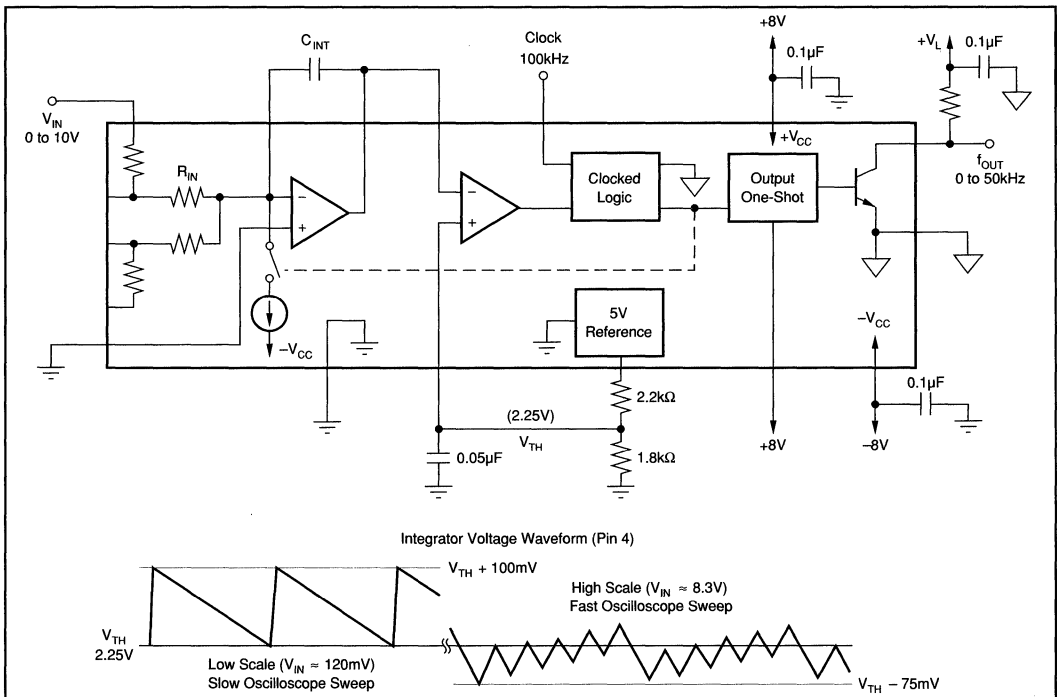
FIGURE 5. Circuit Diagram and Integrator Voltage Waveform for Low Power Supply Voltage Operation.

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VOLTAGE-TO-FREQUENCY CONVERTERS

The circuit in Figure 5 operates from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to –75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationship of the allowable operating voltage ranges on important pins is shown in Figure 6. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special design of this type optimizes high-frequency performance. It is this characteristic which requires offsetting the noninverting comparator input in voltage-to-frequency mode.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by supplying an input frequency to the comparator input as shown in Figure 7. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is:

$$V_{OUT} = (f_{OUT}/f_{CLOCK})\ 20V.$$

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 7. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200ns before a negative clock edge and rise no sooner than 200ns after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 8 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but with the tradeoff of slow settling time in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

NOTE: Several useful applications circuits may be found in the VFC100 product data sheet. These require only minor adaptation to the different pinout and input resistor configurations of the VFC101.
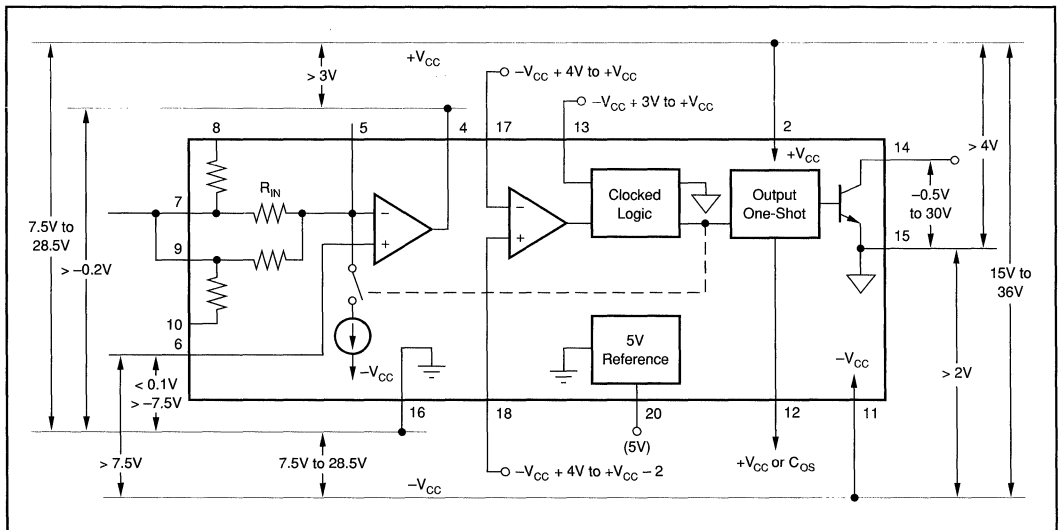
FIGURE 6. Relationships of Allowable Voltages.
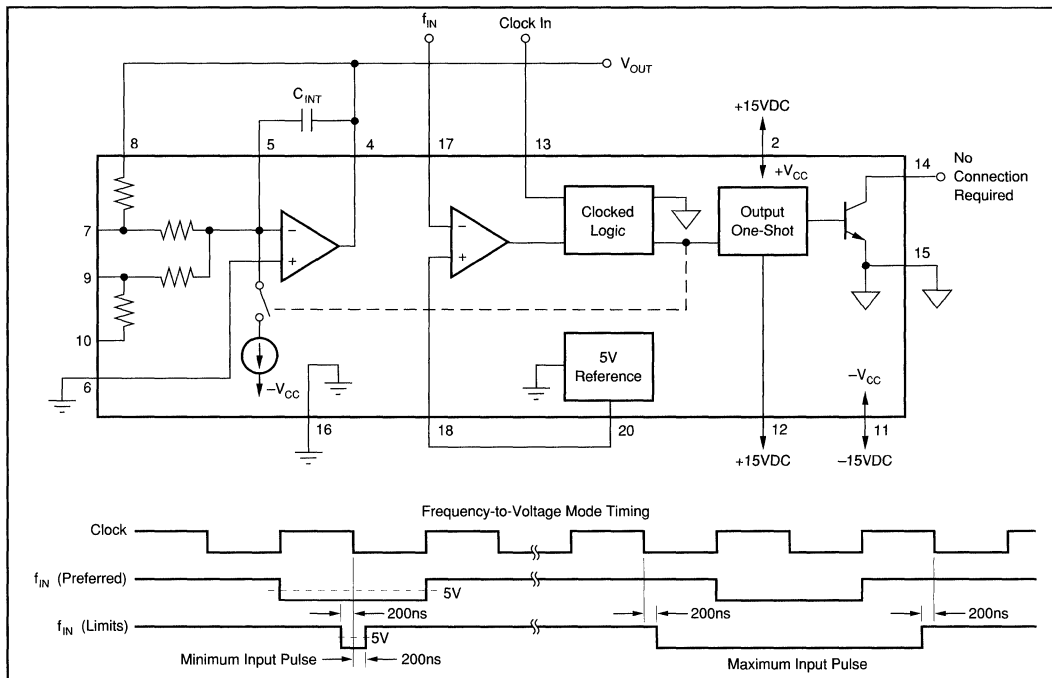
FIGURE 7. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.
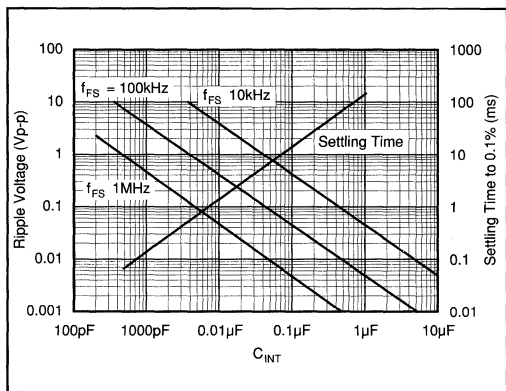
FIGURE 8. Frequency-to-Voltage Mode Output Ripple and
Settling Time vs Integrator Capacitance.

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VOLTAGE-TO-FREQUENCY CONVERTERS

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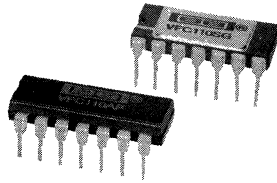
VFC110

High-Frequency
VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

● **HIGH-FREQUENCY OPERATION:**
  4MHz FS max
● **EXCELLENT LINEARITY:**
  ±0.02% typ at 2MHz
● **PRECISION 5V REFERENCE**
● **DISABLE PIN**
● **LOW JITTER**

APPLICATIONS

● **INTEGRATING A/D CONVERSION**
● **PROCESS CONTROL**
● **VOLTAGE ISOLATION**
● **VOLTAGE-CONTROLLED OSCILLATOR**
● **FM TELEMETRY**

DESCRIPTION

The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency

output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range gradeouts are available.

     PDS-861A

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SPECIFICATIONS

At T_A = +25°C and V_S = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	VFC110BG MIN	VFC110BG TYP	VFC110BG MAX	VFC110AG/SG/AP MIN	VFC110AG/SG/AP TYP	VFC110AG/SG/AP MAX	UNITS
VOLTAGE-TO-FREQUENCY OPERATION								
Nonlinearity[1]: f_{FS} = 100kHz	C_{OS} = 2.2nF, R_{IN} = 44kΩ		0.005	0.01		0.01	0.05	%FS
f_{FS} = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ		0.01	0.05			0.1	%FS
f_{FS} = 2MHz	C_{OS} = 56pF, R_{IN} = 34kΩ		0.02				*	%FS
f_{FS} = 4MHz	C_{OS} = (Int), R_{IN} = (Int)		1				*	%FS
Gain Error, f = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ			5			*	%
Gain Drift, f = 1MHz	Specified Temp Range			50			100	ppm/°C
Relative to V_{REF}	Specified Temp Range		50			100		ppm/°C
PSRR	V_S = ±8V to ±18V			0.05			0.1	%/V
INPUT								
Full Scale Input Current			250	500		*	*	µA
I_B– (Inverting Input)			15	60		20	100	nA
I_B+ (Non-Inverting Input)			250			*		nA
V_{OS}				3			3	mV
V_{OS} Drift	Specified Temp Range		35			*		µV/°C
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 2kΩ	–0.2		$+V_S$ – 4	*		*	V
Output Current Drive		5	20		*	*		mA
Capacitive Load	No Oscillations		10			10		nF
COMPARATOR INPUT								
I_B (Input Bias Current)			–5			*		µA
Trigger Voltage			±50			*		mV
Input Voltage Range		–5		$+V_S$	*		*	V
OPEN COLLECTOR OUTPUT								
V_O Low				0.4			*	V
$I_{LEAKAGE}$			0.1	1		*	*	µA
Fall Time			25			*		ns
Delay to Rise			25			*		ns
Settling Time	To Specified Linearity for a Full-Scale Input Step	One Pulse of New Frequency Plus 1µs						
REFERENCE VOLTAGE								
Voltage		4.97	5	5.03	*	*	*	V
Voltage Drift				20			50	ppm/°C
Load Regulation	I_O = 0 to 10mA		2	10		*	*	mV
PSRR	V_S = ±8V to ±18V		5			*		mV/V
Current Limit	Short Circuit	15	20			*		mA
ENABLE INPUT								
V_{HIGH} (f_{OUT} Enabled)	Specified Temp Range	2			*			V
V_{LOW} (f_{OUT} Disabled)	Specified Temp Range			0.4			*	V
I_{HIGH}			0.1			*		µA
I_{LOW}			1			*		µA
POWER SUPPLY								
Voltage, ±V_S		±8	±15	±18	*	*	*	V
Current			13	16		*	*	mA
TEMPERATURE RANGE								
Specified								
AG, BG, AP		–25		+85	*		*	°C
SG		–55		+125				°C
Storage								
AG, BG, SG		–65		+150	*		*	°C
AP		–40		+125	*		*	°C

* Same specifications as VFC110BG.
NOTE: (1) Nonlinearity measured from 1V to 10V input.

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VOLTAGE-TO-FREQUENCY CONVERTERS

PIN CONFIGURATION

Top View   DIP

I_{IN}	1		14	Input Common
V_{IN}	2		13	Analog Common
+5V_{REF} Out	3		12	V_{OUT}
$-V_S$	4		11	Comparator In
Enable	5		10	$+V_S$
C_{OS}	6		9	NC
Digital Ground	7		8	f_{OUT}

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages ($+V_s$ to $-V_s$) 40V
f_{OUT} Sink Current 50mA
Comparator In Voltage .... −5V to $+V_s$
Enable Input .... $+V_s$ to $-V_s$
Integrator Common-Mode Voltage .... −1.5V to +1.5V
Integrator Differential Input Voltage .... +0.5V to −0.5V
Integrator Out (short-circuit) .... Indefinite
V_{REF} Out (short-circuit) .... Indefinite
Operating Temperature Range
 G Package .... −55°C to +125°C
 P Package .... −40°C to +85°C
Storage Temperature
 G Package .... −60°C to +150°C
 P Package .... −40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC110AG	Ceramic DIP	−25°C to +85°C
VFC110BG	Ceramic DIP	−25°C to +85°C
VFC110SG	Ceramic DIP	−55°C to +125°C
VFC110AP	Plastic DIP	−25°C to +85°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC110AG	14-Pin Ceramic DIP	137
VFC110BG	14-Pin Ceramic DIP	137
VFC110SG	14-Pin Ceramic DIP	137
VFC110AP	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V unless otherwise noted.

FULL-SCALE FREQUENCY vs
EXTERNAL ONE-SHOT CAPACITOR

R_{IN} = 40kΩ

Full Scale Frequency (Hz)

External One-Shot Capacitor

QUIESCENT CURRENT vs TEMPERATURE

I_Q+

I_Q-

Quiescent Current (mA)

Temperature (°C)

REFERENCE VOLTAGE vs
REFERENCE LOAD CURRENT

Short Circuit
Current Limit

V_{REF} (V)

Output Current (mA)

TYPICAL FULL SCALE GAIN DRIFT
vs FULL SCALE FREQUENCY

A Grade,
S Grade   B Grade

Full Scale Frequency (ppm/°C)

Full Scale Frequency (Hz)

JITTER vs FULL SCALE FREQUENCY

Jitter (ppm)

Full Scale Frequency (Hz)

Jitter is the ratio of the 1σ value of the distribution of the period
($1/f_{OUT}$, max) to the mean of the period.

FREQUENCY COUNT REPEATABILITY
vs COUNTER GATE TIME

f_{FS} = 100kHz

f_{FS} = 1MHz

Frequency Repeatability (%)

Repeatability (Bits)
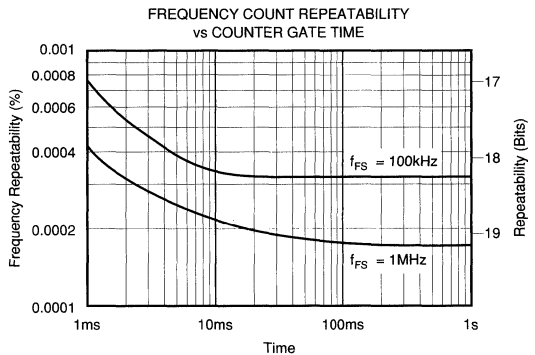
Time

This graph describes the low frequency stability of the VFC110:
the ratio of the 1σ point of the distribution of 100 runs (where
each mean frequency came from 1000 readings for each gate
time) to the overall mean frequency.

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VOLTAGE-TO-FREQUENCY CONVERTERS

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

NONLINEARITY vs INPUT VOLTAGE

NONLINEARITY vs FULL SCALE FREQUENCY
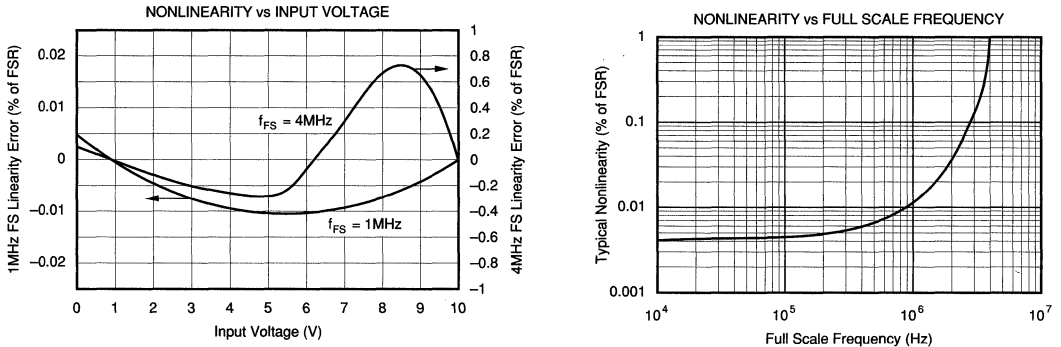
OPERATION

Figure 1 shows the connections required for operation at a full-scale output frequency of 4MHz. Only power supply bypass capacitors and an output pull-up resistor, R_{PU}, are required for this mode of operation. A 0V to 10V input voltage produces a 0Hz to 4MHz output frequency. The internal input resistor, one-shot and integrator capacitors set the full-scale output frequency. The input is applied to the summing junction of the integrator amplifier through the 25kΩ internal input resistor. Pin 14 (the non-inverting amplifier input) should be referred directly to the negative side of V_{IN}. The common-mode range of the integrating amplifier is limited to approximately –1V to +1V referred to analog ground. This allows the non-inverting input to Kelvin-sense the common connection of V_{IN}, easily accommodating any ground-drop errors. The input impedance loading V_{IN} is equal to the input resistor—approximately 25kΩ.

OPERATION AT LOWER FREQUENCIES

The VFC110 can be operated at lower frequencies simply by limiting the input voltage to less than the nominal 10V full-scale input. To maintain a 10V FS input and highest accuracy, however, external components are required (see Table I). Small adjustments may be required in the nominal values indicated. Integrator and one-shot capacitors are added in parallel to internal capacitors. Figure 2 shows the connections required for 100kHz full scale output. The one-shot capacitor, C_{OS}, should be connected to logic ground. The one-shot connection (pin 6) is not short-circuit protected. Short-circuits to ground may damage the device.
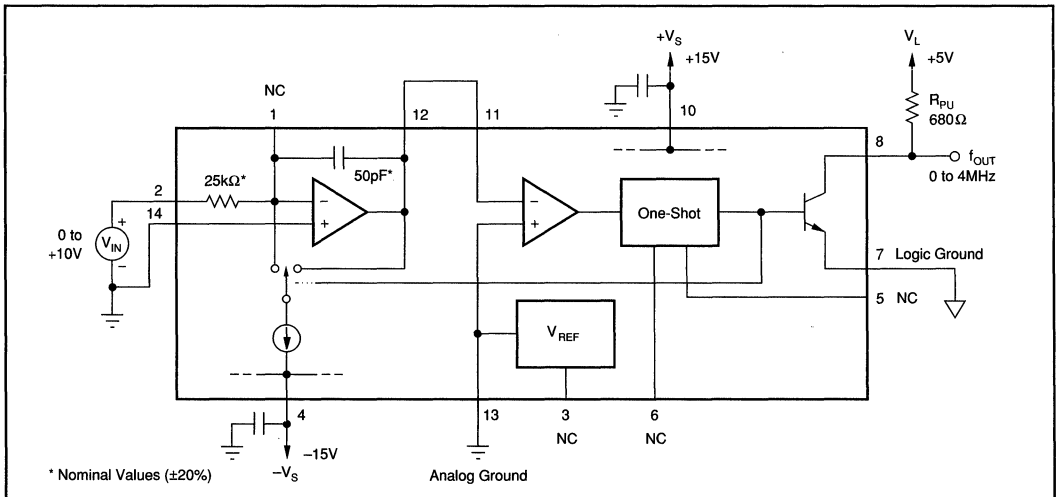
FIGURE 1. 4MHz Full-Scale Operation.

The integrator capacitor's value does not directly affect the output frequency, but determines the magnitude of the voltage swing on the integrator's output. Using a C_{INT} equal to C_{OS} provides an integrator output swing from 0V to approximately 1.5V.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of an external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor serves as a "charge bucket," where charge is accumulated from the input, V_{IN}, and that charge is drained during the one-shot period. While the size of the bucket (capacitor value) is not critical, it must not leak. Capacitor leakage or dielectric absorption can affect the

FULL-SCALE FREQUENCY, f_{FS}	EXTERNAL COMPONENTS		
	R_{IN}	C_{OS}	C_{INT}
4MHz	*	*	*
2MHz	34kΩ	56pF	*
1MHz	40kΩ	150pF	*
500kHz	58kΩ	330pF	2nF
100kHz	44kΩ	2.2nF	10nF
50kHz	88kΩ	2.2nF	0.1µF
10kHz	44kΩ	22nF	0.1µF

* Use internal component only.
The values given were determined empirically to give the optimal performance, taking into consideration tradeoffs between linearity and jitter for each given full scale frequency of operation. The capacitors listed were chosen from standard values of NPO ceramic type capacitors while the resistor values were rounded off. Larger C_{INT} values may improve linearity, but may also increase frequency noise.

TABLE I. Component Selection Table.

linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF. Use caution with higher value ceramic capacitors. High-k ceramic capacitors may have voltage nonlinearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for high values.

PULL-UP RESISTOR

The VFC110's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply voltage, $+V_L$. The output transistor is On during the one-shot period, causing the output to be a logic Low. The current flowing in this resistor should be limited to 8mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 8mA. The logic power supply can be any positive voltage up to $+V_S$.

ENABLE PIN

If left unconnected, the Enable input will assume a logic High level, enabling operation. Alternatively, the Enable input may be connected directly to $+V_S$. Since an internal pull-up current is included, the Enable input may be driven by an open-collector logic signal.

A logic Low at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp negatively and saturate at its most negative output swing of approximately –0.7V.

FIGURE 2. 100kHz Full-Scale Operation.

VFC110

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VOLTAGE-TO-FREQUENCY CONVERTERS

PRINCIPLE OF OPERATION

The VFC110 uses a charge-balance technique to achieve high accuracy. The heart of this technique is an analog integrator formed by the integrator op amp, feedback capacitor C_{INT}, and input resistor R_{IN}. The integrator's output voltage is proportional to the charge stored in C_{INT}. An input voltage develops an input current of V_{IN}/R_{IN}, which is forced to flow through C_{INT}. This current charges C_{INT}, causing the integrator output voltage to ramp negatively.

When the output of the integrator ramps to 0V, the comparator trips, triggering the one-shot. This connects the reference current, I_{REF}, to the integrator input during the one-shot period, T_{OS}. This switched current causes the integrator output to ramp positively until the one-shot period ends. Then the cycle starts again.

The oscillation is regulated by the balance of current (or charge) between the input current and the time-averaged
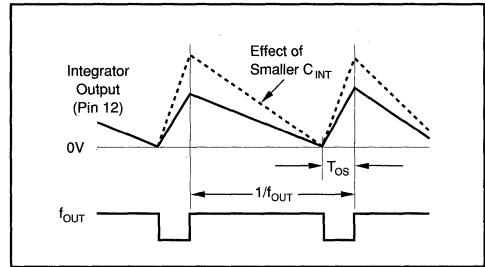
reset current. The equation of current balance is

$$I_{IN} = I_{REF} \bullet \text{Duty Cycle}$$

$$V_{IN}/R_{IN} = I_{REF} \bullet f_{OUT} \bullet T_O$$

where T_O is the one-shot period and f_{OUT} is the oscillation frequency.

When the Enable input receives a logic High (greater than +2V), a reset current cycle is initiated (causing f_{OUT} to go Low). The integrator ramps positively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, several VFCs' outputs can be connected to a single output line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the output line. Since the disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency as—or a multiple of—a nearby VFC. Coupling between the two may cause them to lock to the same or exact multiple frequency. It then takes a small incremental input voltage change to unlock them. Locking cannot occur when unneeded VFCs are disabled.

REFERENCE VOLTAGE

The V_{REF} output is useful for offsetting the transfer function and exciting sensors. Figure 3 shows V_{REF} used to offset the transfer function of the VFC110 to achieve a bipolar input voltage range. Sub-surface zener reference circuitry is used for low noise and excellent temperature drift. Output current is specified to 10mA and current-limited to approximately 20mA. Excessive or variable loads on V_{REF} can decrease frequency stability due to internal heating.

MEASURING THE OUTPUT FREQUENCY

To complete an integrating A/D conversion, the output frequency of the VFC110 must be counted. Simple frequency counting is accomplished by counting output pulses for a reference time (usually derived from a crystal oscilla-
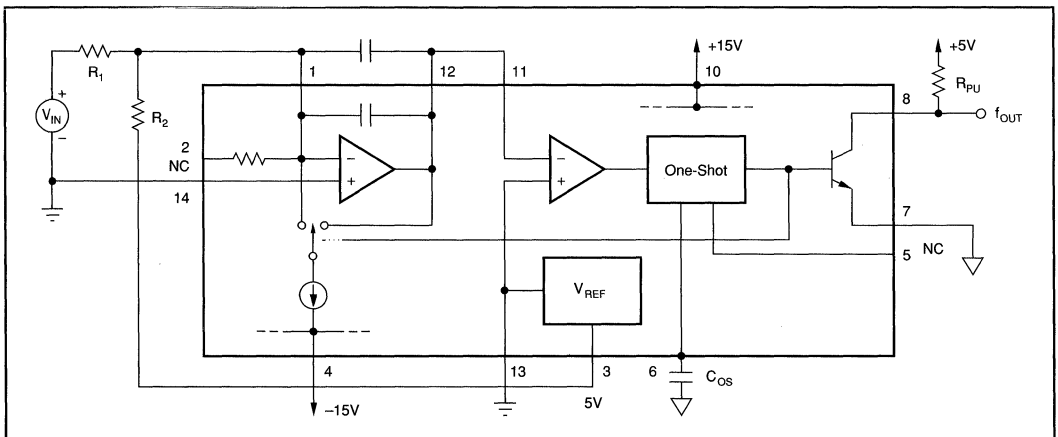
FIGURE 3. Offsetting the Frequency Output.

tor). This can be implemented with counter/timer peripheral chips available for many popular microprocessor families. Many micro-controllers have counter inputs that can be programmed for frequency measurement.

Since f_{OUT} is an open-collector device, the negative-going edge provides the fastest logic transition. Clocking the counter on the falling edge will provide the best results in noisy environments.

Frequency can also be measured by accurately timing the period of one or more cycles of the VFC's output. Frequency must then be computed since it is inversely proportional to the measured period. This measurement technique can provide higher measurement resolution in short conversion times. It is the method used in most high-performance laboratory frequency counters. It is usually necessary to offset the transfer function so 0V input causes a finite frequency out. Otherwise the output period (and therefore the conversion time) approaches infinity.

FREQUENCY NOISE

Frequency noise (small random variation in the output frequency) limits the useful resolution of fast frequency measurement techniques. Long measurement time averages the effect of frequency noise and achieves the maximum useful resolution. The VFC110 is designed to minimize frequency noise and allows improved useful resolution with short measurement times. The typical curve "Frequency Count Repeatability vs Counter Gate Time" shows the effect of noise as the counter gate time is varied. It shows the one

standard deviation (1σ) count variation (as a percentage of FS counts) versus counter gate time.

FREQUENCY-TO-VOLTAGE CONVERSION

The VFC110 can also be connected as a frequency-to-voltage converter (Figure 4). Input frequency pulses are applied to the comparator input. A negative-going pulse crossing 0V initiates a reference current pulse which is averaged by the integrator op amp. The values of the one-shot capacitor and feedback resistor (same as R_{IN}) are determined with Table I. The input frequency pulse must not remain negative for longer than the duration of the one-shot period. Figure 4 shows the required timing to assure this. If the negative-going input frequency pulses are longer in duration, the capacitive coupling circuit shown can be used. Level shift or capacitive coupling circuitry should not provide pulses which go lower than –5V or damage to the comparator input may occur.

This frequency-to-voltage converter operates by averaging (filtering) the reference current pulses triggered on every falling edge at the frequency input. Voltage ripple with a frequency equal to the input will be present in the output voltage. The magnitude of this ripple voltage is inversely proportional to the integrator capacitor. The ripple can be made arbitrarily small with a large capacitor, but at the sacrifice of settling time. The R-C time constant of C_{INT} and R_{IN} determine the settling behavior. A better compromise between output ripple and settling time can be achieved by adding a low-pass filter following the voltage output.

FIGURE 4. Frequency-to-Voltage Conversion.

VFC110

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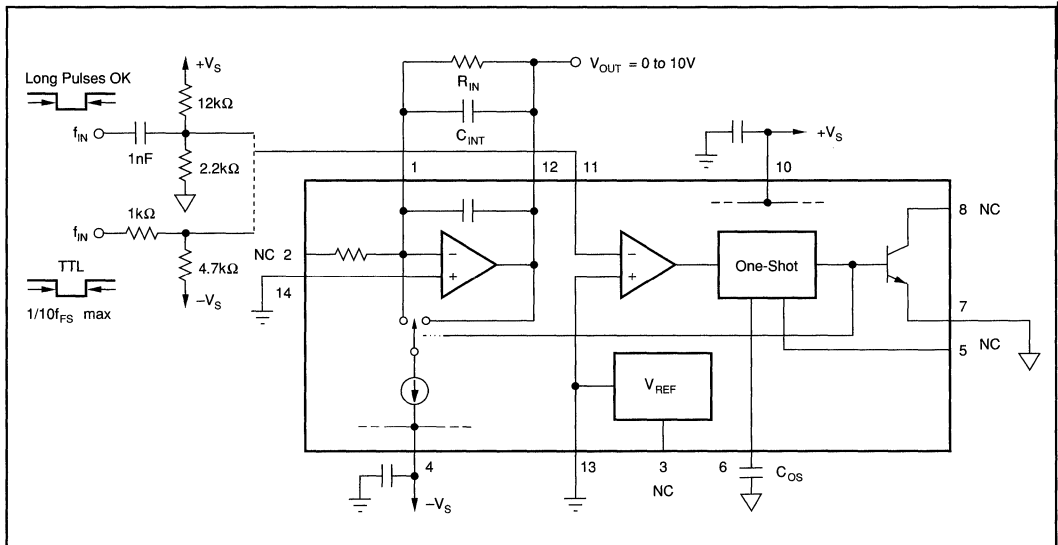
VOLTAGE-TO-FREQUENCY CONVERTERS

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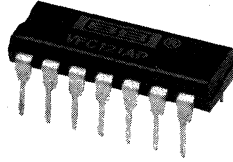
VFC121

Precision Single Power Supply
VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

● **SINGLE SUPPLY OPERATION:**
  +4.5V to +36V
● **f_O = 1.5MHz max**
● **LOW NONLINEARITY: 0.03% max at**
  100kHz, 0.1% max at 1MHz
● **HIGH INPUT IMPEDANCE**
● **VOLTAGE REFERENCE OUTPUT**
● **THERMOMETER OUTPUT: 1mV/°K**

APPLICATIONS

● **INTEGRATING A/D CONVERSION**
● **ANALOG SIGNAL TRANSMISSION**
● **PHASE-LOCKED LOOP VCO**
● **GALVANICALLY ISOLATED SYSTEMS**

DESCRIPTION

The VFC121 is a monolithic voltage-to-frequency converter consisting of an integrating amplifier, voltage reference, and one-shot charge pump circuitry. High-frequency complementary NPN/PNP circuitry is used to implement the charge-balance technique, achieving speed and accuracy far superior to previous single power supply VFCs.

The high-impedance input accepts signals from ground potential to V_S – 2.5V. Power supplies from 4.5V to

36V may be used. A 2.6V reference voltage output may be used to excite sensors or bias external circuitry. A thermometer output voltage proportional to absolute temperature (°K) may be used as a temperature sensor or for temperature compensation of applications circuits.

Frequency output is an open-collector transistor. A disable pin forces the output to the high impedance state, allowing multiple VFCs to share a common transmission path.

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

PARAMETER	CONDITIONS	VFC121AP MIN	VFC121AP TYP	VFC121AP MAX	VFC121BP MIN	VFC121BP TYP	VFC121BP MAX	UNITS
ACCURACY								
Nonlinearity: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			0.05			0.03	%FS
f_{FS} = 1MHz	C_{OS} 68pF, C_{INT} = 270pF		0.1				0.1	%FS
Gain Error: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			10			*	%FS
Gain Drift: f_{FS} = 100kHz	T_{MIN} to T_{MAX}			80			40	ppm/°C
Relative to V_{REF}	+V_S = +5V to +36V			100			40	ppm/°C
PSRR				0.025			*	%/V
INPUT								
Minimum Input Voltage				0			*	V
Maximum Input Voltage		V_S – 2.5	V_S – 2		*	*		V
Impedance		10	100		*	*		MΩ
I_{BIAS}			150	300		*	*	nA
V_{OS}			300	800		100	400	μV
V_{OS} Drift	T_{MIN} to T_{MAX}		10			*		μV/°C
OPEN COLLECTOR OUTPUT								
V_{SAT}	$I_{PULL\ UP}$ = 10mA			0.4			*	V
$I_{LEAKAGE}$	$V_{PULL\ UP}$ = 5V			1			*	μA
	$V_{PULL\ UP}$ ≈ 36V			10			*	μA
Fall Time				100			*	ns
Delay to Rise	$R_{PULL\ UP}$ = 470Ω			100			*	ns
Settling Time	To Specified Linearity for Full Scale Input Step	(1)						
REFERENCE VOLTAGE								
Voltage		2.59	2.6	2.61	*	*	*	V
Voltage Drift				100			50	ppm/°C
Load Regulation	I_O = 0 to 10mA			10			*	mV
PSRR	V_S = +5V to +36V			10			*	mV
Current Limit				Short Circuit Protected				
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 100kΩ	0.8		2.9	*		*	V
COMPARATOR INPUT								
I_{BIAS}			+1				*	μA
Trigger Voltage			2.6				*	V
Input Voltage Range		0		2.9	*		*	V
THERMOMETER								
V_T	T_A = +25°C		298			*		mV
V_T Slope	T_{MIN} to T_{MAX}		1			*		mV/°K
DISABLE INPUT								
V_{HIGH} (Disabled)		2			*			V
V_{LOW}				0.8			*	V
I_{HIGH} (Disabled)	V_{HIGH} = 2V		10			*		μA
I_{LOW}	V_{LOW} = 0.8V		10			*		μA
POWER SUPPLY								
Voltage		4.5	5	36	*	*	*	V
Current			7.5	10		*	*	mA
TEMPERATURE RANGE								
Specified		–25		+85	*		*	°C
Storage		–40		+125	*		*	°C

* Same specification as VFC121AP.
NOTE: (1) One pulse of new frequency plus 1μs.

VFC121

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VOLTAGE-TO-FREQUENCY CONVERTERS

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PIN CONFIGURATION

Top View

Pin		Pin	
NC	1	14	f_{OUT}
Disable	2	13	$+V_S$
V_T	3	12	$-V_{IN}$
Gnd Sense	4	11	$+V_{IN}$
C_{OS}	5	10	Int Out
V_{REF}	6	9	Comp In
NC	7	8	Gnd

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_S$) 40V
f_{OUT} Sink Current 20mA
Comparator In Voltage .... −0.5V to +3V
Enable Input .... −0.3V to $+V_S$
Integrator Common-Mode Voltage .... 0V to $+V_S$ − 2V
Integrator Differential Input Voltage .... −0.3V to +0.3V
V_{REF} Out (short-circuit) .... Indefinite
Operating Temperature Range .... −40°C to +85°C
Storage Temperature .... −40°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses above these ratings may permanently damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR, MAX (f_s = 100kHz)	TEMPERATURE RANGE
VFC121AP	Plastic DIP	0.05%	−25°C to +85°C
VFC121BP	Plastic DIP	0.03%	−25°C to +85°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC121AP	14-Pin Plastic DIP	010
VFC121BP	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION

PIN #	NAME	DESCRIPTION
1	NC	Not Connected
2	Disable	Input logic Low for normal operation. Input logic High to disable the VFC121. Has internal pull-down, for normal operation if not connected.
3	V_T	Temperature compensation voltage proportional to absolute temperature. Typically 298mV at room temperature (298°K), with a change of 1mV per °C (°K).
4	Gnd Sense	Defines ground for the internal voltage reference.
5	C_{OS}	One-shot capacitor is connected between here and ground to set full scale output frequency.
6	V_{REF}	Output from the internal band-gap voltage reference, typically 2.6V. Can be used externally to set levels or excite sensors.
7	NC	Not Connected
8	Gnd	Ground
9	Comp In	Comparator In
10	Int Out	Integrator Out
11	$+V_{IN}$	Non-inverting input of the integrating op amp. The input signal is applied here.
12	$-V_{IN}$	Inverting input of the integrating op amp. C_{INT} is connected between here and the integrator output (pin 10), and R_{IN} is connected between here and ground.
13	$+V_S$	Supply voltage connected here. Range is +4.5V to +36V.
14	f_{OUT}	Frequency output pin. This is the output of an open-collector transistor, and an external pull-up circuit should be used to generate the appropriate logic levels.

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

JITTER vs FULL SCALE FREQUENCY

FREQUENCY COUNT REPEATABILITY
vs COUNTER GATE TIME

FULL SCALE FREQUENCY
vs EXTERNAL ONE-SHOT CAPACITOR

NON-LINEARITY vs
FULL-SCALE FREQUENCY

NON-LINEARITY vs INPUT VOLTAGE

REFERENCE VOLTAGE vs
REFERENCE LOAD CURRENT

NOTE: The V_{REF} output is
short-circuit protected.

VFC121

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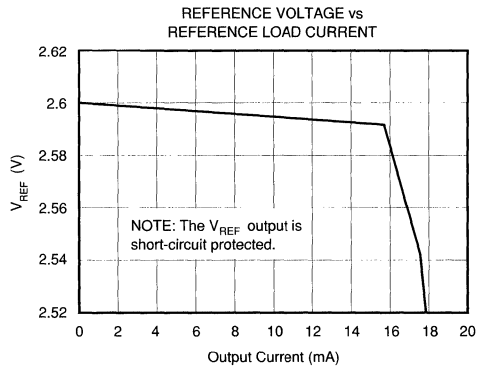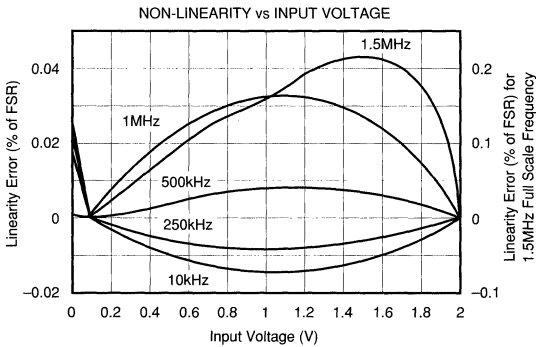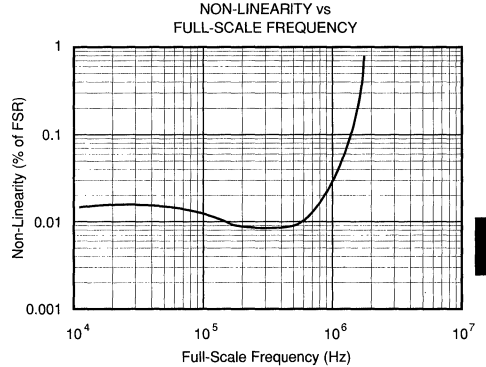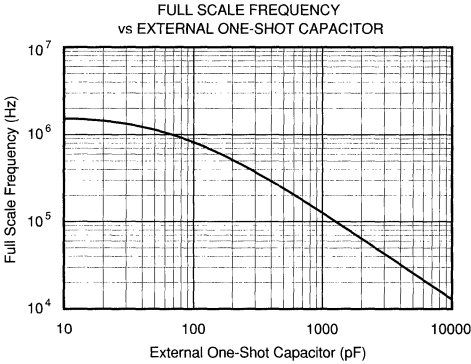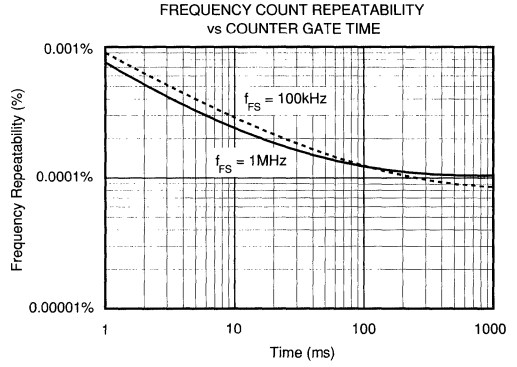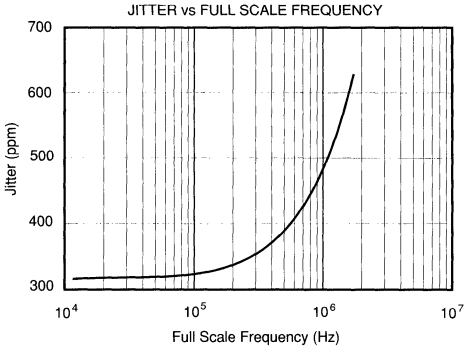
VOLTAGE-TO-FREQUENCY CONVERTERS

TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

FULL SCALE GAIN DRIFT vs TEMPERATURE

THEORY OF OPERATION

The VFC121 uses a charge-balance technique to achieve high accuracy. The basic architecture is shown in Figure 1. An analog integrator at the front end, consisting of a precision op amp and a feedback capacitor, C_{INT}, provides a true integrating approach for improved noise immunity. Use of the non-inverting input of the op amp for the analog input provides a high input impedance to the user.

The integrator's output is proportional to the charge stored on C_{INT} plus the analog input voltage. An input voltage, V_{IN}, forces a current through R_{IN} of V_{IN}/R_{IN}, which also flows through C_{INT}. This current through C_{INT} causes the integrator output to ramp positive. (Refer to the timing diagram in Figure 2.)

When the output of the integrator ramps to V_{REF}, the comparator trips, driving the output of the VFC121 Low, and triggering the one-shot. The tripping of the comparator also connects the reference current, I_{REF}, to the integrator input

for the duration of the one-shot period, T_{OS}. This switched current causes the output of the integrator to ramp negative.

When the one-shot times out, the output of the VFC121 is reset High, the one-shot is reset, and I_{REF} is switched to the output of the integrating op amp. (This causes the output of
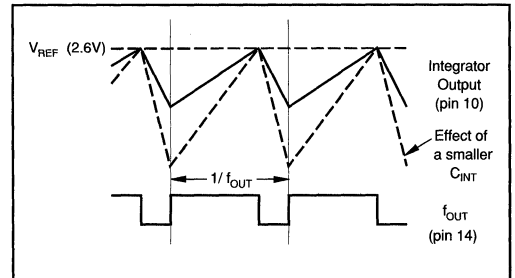
FIGURE 2. Timing Diagram.
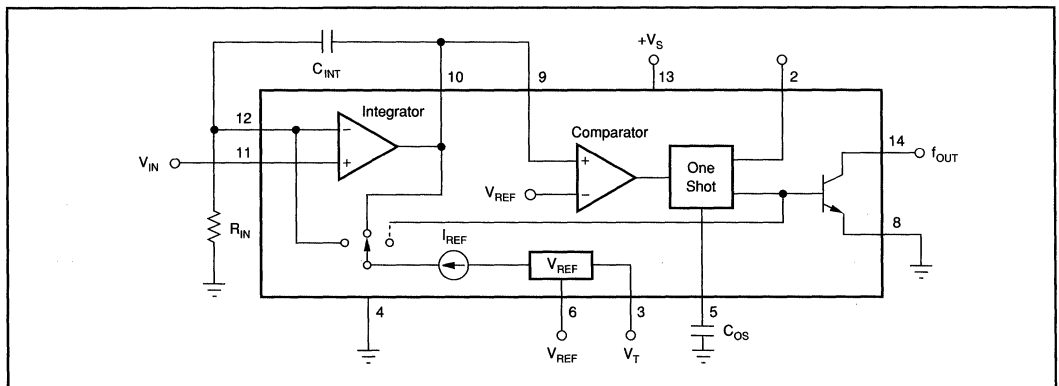
FIGURE 1. VFC121 Architecture.
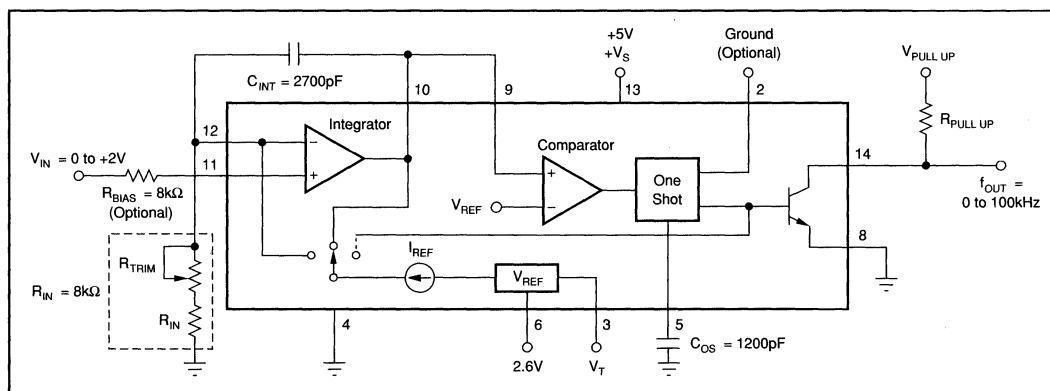
FIGURE 3. 2V Full Scale Input, 100kHz Full Scale Output.

the integrating op amp to see a constant current, reducing errors that might occur if the load were unbalanced.) In this state, the output of the integrator resumes a positive ramp, restarting the cycle.

The output frequency is regulated by the balance of current (or charge) between the current V_{IN}/R_{IN} and the time-averaged reset current. The size of the integrating capacitor, C_{INT}, determines the slew rate of the integrator, and thus how far down the integrator ramps during the one-shot period, but has no effect on the output frequency of the VFC121.

The reference voltage used internally is generated from a bandgap reference, which is actively trimmed to achieve the low drift characteristics of the VFC121. To maximize flexibility of designs using the VFC121, both the bandgap reference voltage and a thermometer voltage are available externally.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC OPERATION

The VFC121 allows users a wide range of input voltages and supply voltages, and easy control of the full scale output frequency. The basic connections are shown in Figure 3, with components that generate a 100kHz output with a 2V full scale input.

For other input and output ranges, the full scale input voltages and full scale output frequencies can be calculated as follows:

$$f_{FS} = \frac{V_{FS}}{2(R_{IN})(C_{OS} + 60)}$$

The full scale input current of 250µA was chosen to provide a 25% duty cycle in the output frequency. The VFC121 is designed to give optimum linearity under these conditions, but other current levels can be used without significantly degrading linearity. By reducing R_{IN}, the integrating current is increased, increasing the positive ramp rate of the integra-

tor output. Since the one-shot period is unchanged, the duty cycle of the output increases.

Stray capacitance at the C_{OS} pin typically adds about 60pF to the capacitance of the external C_{OS}, which accounts for the adjustment in the above equation. This usually becomes negligible as the required output frequency is reduced, and C_{OS} is increased.

R_{BIAS} is included in the circuit in Figure 3 to compensate for the effects of bias currents at the input of the integrating op amp. It is optional in most applications, but when needed, R_{BIAS} should equal R_{IN}.

Table 1 indicates standard external component values for common input voltage ranges and output frequency ranges.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of the external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor, C_{INT}, serves as a "charge bucket," where charge accumulation is induced by the input, V_{IN}, and

FULL SCALE INPUT RANGE (V)		$R_{IN} + R_{TRIM}$ (kΩ)	
2		8	
5		20	
10		40	
FULL SCALE OUTPUT FREQUENCY (kHz)	C_{OS} (pF)	C_{INT} (pF)	
1500	22	150	
1000	68	270	
500	180	470	
250	470	1000	
125	1000	2200	
25	4700	10,000	
NOTE: Higher output frequencies can be achieved by reducing R_{IN}.			

TABLE 1. Standard External Component Values

VFC121

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VOLTAGE-TO-FREQUENCY CONVERTERS

repeatedly reduced during the one-shot period. The size of the bucket (the capacitor value) is not critical, since it primarily determines how far below V_{REF} the output of the integrator ramps during the one-shot period. At the same time, the capacitor used must not leak since capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF, but caution should be used with higher value ceramic capacitors. High-k ceramic capacitors may have voltage non-linearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for higher capacitance values.

During the one-shot period, the output of the integrator is ramping down. To prevent the integrating op amp from being saturated at its minimum output of 0.8V, C_{INT} should be kept at least 1.7 × C_{OS}.

OUTPUT FREQUENCY ADJUSTMENT

The full scale output frequency of the VFC121 can be adjusted using a trim-pot, R_{TRIM} in Figure 3, in series with R_{IN}. For optimum drift vs temperature, a low temperature coefficient fixed resistor of approximately 90% of the calculated R_{IN} requirement should be used in series with a trim-pot approximately 20% of the size of the calculated R_{IN}. The low-drift fixed resistor contributes most of the final R_{IN} resistance, so that the effect of higher drift from the trim-pot is attenuated in the total R_{IN}.

PULL-UP RESISTOR

The VFC121's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply, +V_L. The output transistor is On during the one-shot period, causing the output to be logic Low. The current flowing in this resistor should be limited to 10mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 10mA. The logic power supply can be any positive voltage up to +36V.

ENABLE PIN

If left unconnected, the Enable input will assume a logic Low level, enabling the output stage, Alternatively, the Enable input may be connected directly to ground. This pin can also be driven by standard TTL or CMOS logic.

A logic High at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp positive and saturate at its most positive output swing of approximately V_{REF} + 0.7V.

When the Enable input receives a logic Low (less than 0.8V), a reset current cycle is initiated, (causing f_{OUT} to go Low). The integrator ramps negatively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, the outputs from several VFCs can be connected to a single line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the line. Since disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency, or a multiple, as a nearby VFC. Coupling between the two may cause them to lock to the same frequency or an exact multiple. It then takes a small incremental input voltage change on one of the VFCs to unlock them. Locking cannot occur when unneeded VFCs are disabled.

APPLICATION INFORMATION

OPERATION FROM 10kHz TO 210kHz

The VFC121 is designed to provide an output frequency starting at 0Hz for a 0V input and increasing linearly to the full scale output frequency, f_{FS}, at the full scale input voltage, V_{FS}. For applications where low level inputs, near 0V, are critical, it may be inconvenient to have an output frequency approaching 0Hz. Figure 4 shows a circuit which transforms a 0V to 2V input level into output frequencies from 10kHz to 210kHz, by placing a resistor divider network between the input source and the V_{REF} output of the VFC121. This produces a positive voltage at +V_{IN} when the input to the circuit is grounded. This circuit makes use of the high input impedance at +V_{IN}.

The transfer function of this circuit is:

$$V_{IN} = \frac{f_{OUT} - 10\text{kHz}}{100\text{kHz}} \text{ V}$$

To trim the circuit, first apply 2V to the analog input, and adjust R_1 to give a full scale output frequency of 210kHz. Then apply 0V to the analog input, and adjust R_2 until the output frequency is 10kHz. For absolute precision, it may be necessary to make several iterations trimming R_1 and R_2. In most cases, one iteration will be enough, since the effect of R_2 on

NOTE: Use 1% metal film fixed resistors, Cermet® trim pots, and NPO ceramic capacitors.
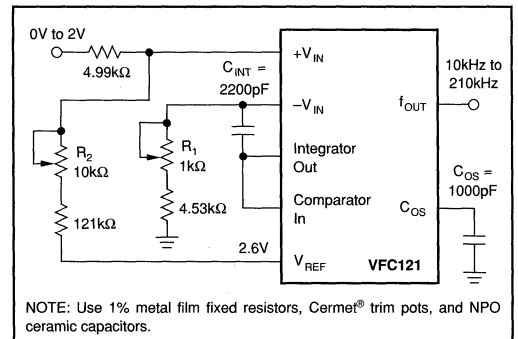
FIGURE 4. Offsetting the Output Frequency.

full scale output frequency is attenuated by the divider network, which sees only a 0.6V total delta at full scale (2.6V at V_{REF} minus 2V full scale input) as compared with a 2.6V delta at a 0V input level.

USING THE VFC121 THERMOMETER VOLTAGE

Because of the high input impedance of the VFC121 (which results from using the non-inverting input to the integrating op amp), it is relatively simple to use a standard multiplexer in front of the VFC121. One of the possible reason to multiplex the input to the VFC121 is to use it to track temperature changes in the operating environment of the electronics in a system, in addition to using the VFC121 in its normal mode to measure an analog signal.

Figure 5 shows a way to do this. In this circuit, the normal analog input signals to be multiplexed through the VFC121 have a full scale voltage of 2V, and generate a full scale output frequency of 100kHz. To measure the electronics system temperature, the user selects the multiplexer channel connected to the thermometer voltage on pin 3. A measured output frequency from the VFC121, with the multiplexer on channel 8, now corresponds to the temperature of the electronics as follows:

$$\text{Temp (}^\circ\text{C)} = \frac{\text{Output Frequency} - 13{,}650}{50}$$
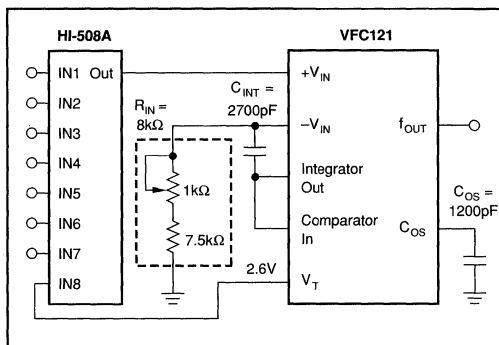
FIGURE 5. Measuring System Temperature.

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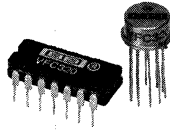
VFC320

Voltage-to-Frequency
and Frequency-to-Voltage
CONVERTER

FEATURES

● **HIGH LINEARITY, 12 to 14 bits**
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
● **V/F OR F/V CONVERSION**
● **6-DECADE DYNAMIC RANGE**
● **20ppm/°C max GAIN DRIFT**
● **OUTPUT TTL/CMOS COMPATIBLE**

APPLICATIONS

● **INEXPENSIVE A/D AND D/A CONVERTER**
● **DIGITAL PANEL METERS**
● **TWO-WIRE DIGITAL TRANSMISSION
  WITH NOISE IMMUNITY**
● **FM MOD/DEMOD OF TRANSDUCER
  SIGNALS**
● **PRECISION LONG TERM INTEGRATOR**
● **HIGH RESOLUTION OPTICAL LINK FOR
  ISOLATION**
● **AC LINE FREQUENCY MONITOR**
● **MOTOR SPEED MONITOR AND CONTROL**

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and fre-
quency-to-voltage converter provides a simple low
cost method of converting analog signals into digital
pulses. The digital output is an open collector and the
digital pulse train repetition rate is proportional to the
amplitude of the analog input voltage. Output pulses
are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved
with relatively few external components. Two exter-
nal resistors and two external capacitors are required
to operate. Full scale frequency and input voltage are
determined by a resistor in series with –In and two
capacitors (one-shot timing and input amplifier inte-
gration). The other resistor is a non-critical open
collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is avail-
able in three performance/temperature grades and two
package configurations. The TO-100 versions are her-
metically sealed, and specified for the –25°C to +85°C
and –55°C to +125°C ranges, and the dual-in-line
units are specified from –25°C to +85°C.

PDS-483H

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SPECIFICATIONS

At T_A = +25°C and ±15VDC power supply, unless otherwise noted.

PARAMETER	CONDITIONS	VFC320BG/BM/SM			VFC320CG/CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range[1]	Fig. 4 with e_2 = 0	>0		Note 2				V
	Fig. 4 with e_1 = 0	<0		−10				V
Current Range[1]	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	μA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage[3]				±0.15			*	mV
Offset Voltage Drift			±5			*		μV/°C
Differential Impedance		300 ‖ 5	650 ‖ 5		*	*		kΩ ‖ pF
Common-Mode								
Impedance		300 ‖ 3	500 ‖ 3		*	*		kΩ ‖ pF
ACCURACY								
Linearity Error[1][4][5]	Fig. 4 with e_2 = 0[6]							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% FSR
Offset Error Input								
Offset Voltage[3]				±15			*	ppm FSR
Offset Drift[7]			±0.5			*		ppm FSR/°C
Gain Error[3]			±5	±10		*	*	% FSR
Gain Drift[7]	f = 10kHz			50			20	ppm FSR/°C
Full Scale Drift	f = 10kHz			50			20	ppm FSR/°C
(Offset Drift and Gain Drift)[7][8][9]								
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% FSR%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			Decades
Settling Time	(V/F) to Specified Linearity							
	For a Full Scale Input Step		Note 10			*		
Overload Recovery	<50% Overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	μA
Voltage, Logic "1"	External Pull-up Resistor							
	Required (See Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		ns
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ f_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 ‖ 10	150 ‖ 10		*	*		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		−V_{CC}		−0.05	*		*	V
Pulse-width Range		0.25			*			μs
OUTPUT FROM OP AMP								
Voltage	I_O = 6mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-Loop			0.1			*	Ω
Capacitive Load	Without Oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6.5	±7.5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		−25		+85	*		*	°C
S Grade		−55		+125				°C
Operating								
B and C Grades		−40		+85	*		*	°C
S Grade		−55		+125				°C
Storage		−65		+150	*		*	°C

* Specification the same as for VFC320BG/BM/SM.

NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by R_{IN} and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For e_1 = 0 typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components' drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.

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Burr-Brown IC Data Book—Data Conversion Products

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VFC320

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VOLTAGE-TO-FREQUENCY CONVERTERS

DICE INFORMATION

VFC320 DIE TOPOGRAPHY
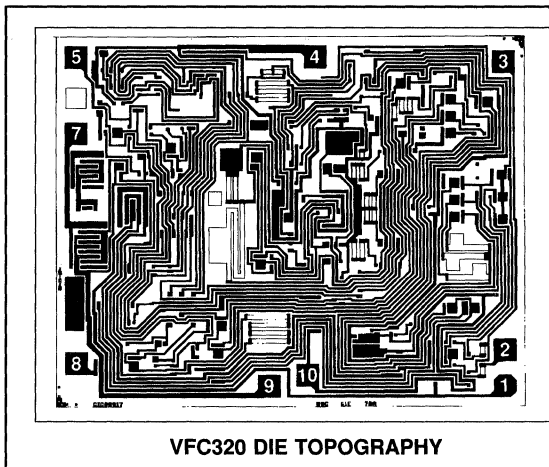
PAD	FUNCTION	PAD	FUNCTION
1	V_{OUT} (Int. Out)	6	NC
2	+In	7	f_{OUT}
3	−In	8	Comp. Input
4	−V_{CC}	9	Common
5	One-Shot Cap.	10	+V_{CC}

NC: No Connection.
Substrate Bias: Electrically connected to −V_S supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	109 x 87 ±5	2.77 x 2.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	

CONNECTION DIAGRAM

NC = no internal connection
External connection permitted.
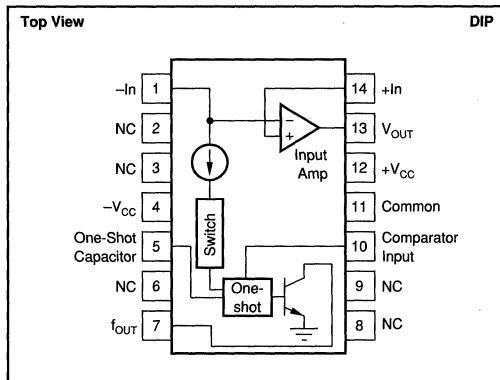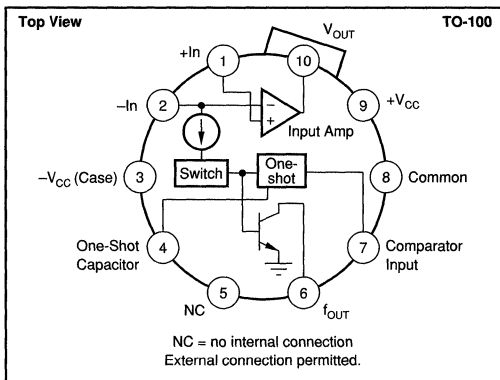
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC320BG	14-Pin Ceramic DIP	−25°C to +85°C
VFC320BM	TO-100	−25°C to +85°C
VFC320SM	TO-100	−55°C to +125°C
VFC320CG	14-Pin Ceramic DIP	−25°C to +85°C
VFC320CM	TO-100	−25°C to +85°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC320BG	14-Pin Ceramic DIP	163
VFC320BM	TO-100	007
VFC320SM	TO-100	007
VFC320CG	14-Pin Ceramic DIP	163
VFC320CM	TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±20V
Output Sink Current at f_{OUT} 50mA
Output Current at V_{OUT} .... +20mA
Input Voltage, −Input .... ±V_{CC}
Input Voltage, +Input .... ±V_{CC}
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero.) Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta_{VIN}$) with operation as close to the chosen full scale frequency as possible

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission.)
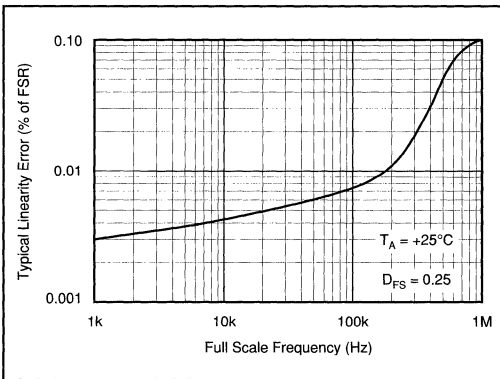
Figure 1. Linearity Error vs Full Scale Frequency.
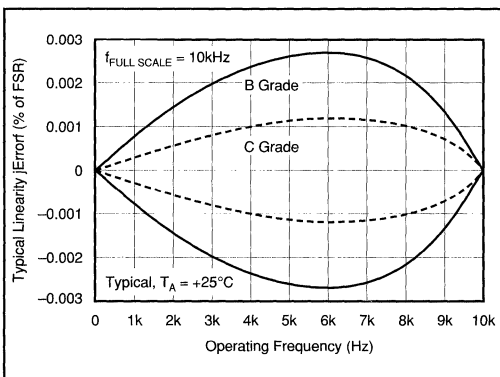
Figure 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.
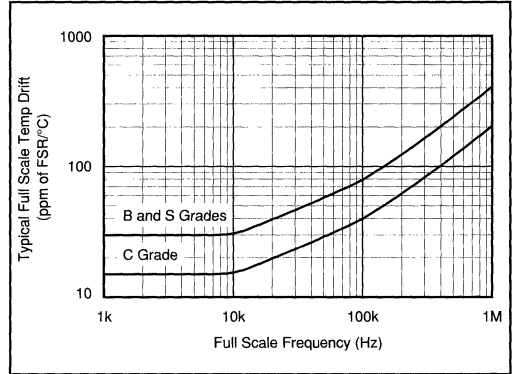
Figure 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50ns plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10µs.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a on-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until $V_{C1} =$ –7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this –7.5V threshold point C_1, comparator B resets the flip-flop, and the ramp voltage

VFC320

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VOLTAGE-TO-FREQUENCY CONVERTERS
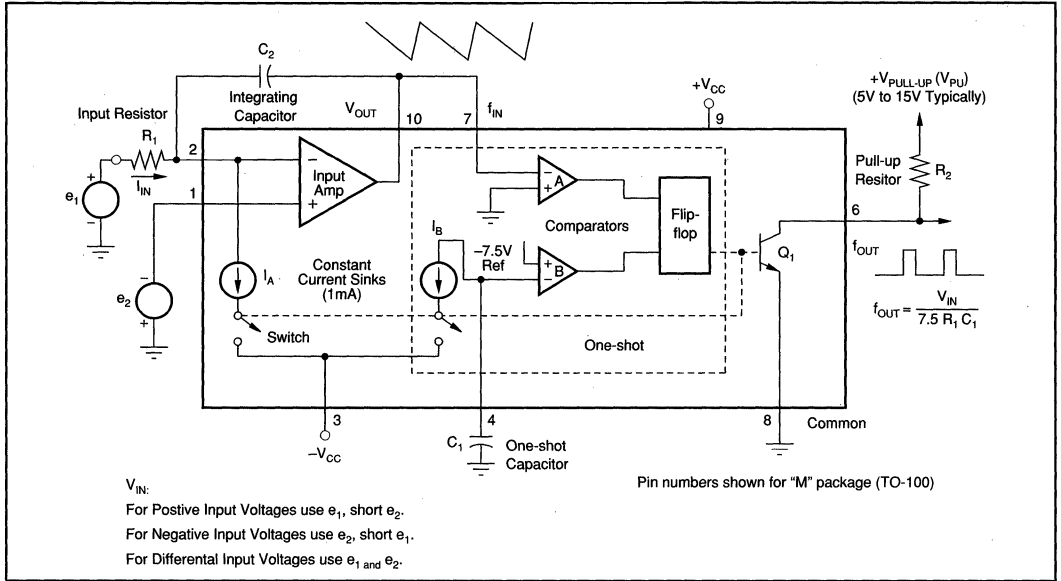
FIGURE 4. Functional Block Diagram of the VFC320.

begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$
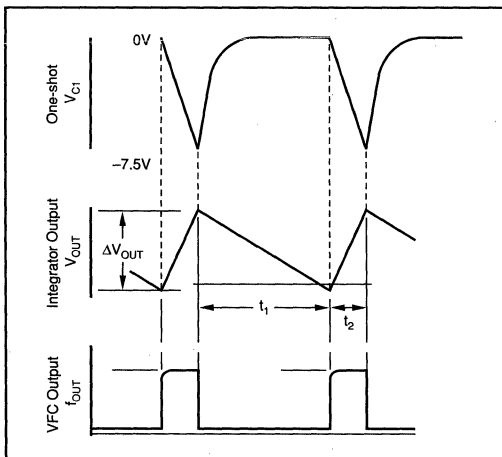
FIGURE 5. Integrator and VFC Output Timing.

In the time $t_1 + t_2$ the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

Thus $\Delta Q = 0 = I_{IN} t_1 + (I_{IN} - I_A) t_2 \quad (2)$

So that $I_{IN} (t_1 + t_2) = I_A t_2 \quad (3)$

But since $t_1 + t_2 = \frac{1}{f_{OUT}}$ and $I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$

$$f_{OUT} = \frac{V_{IN}}{I_A R_2 R_2} \quad (6)$$

In the time t_1, I_B charges the one-shot capacitor C_1 until its voltage reaches $-7.5V$ and trips comparator B.

Thus $t_2 = \frac{C_{IN} 7.5}{I_B} \quad (7)$

Using (7) in (6) yield $f_{OUT} = \frac{V_{IN}}{7.5 R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5 R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN} \, max \, / \, R_1}{1mA} = \frac{I_{IN} \, max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to $I_{IN} \, max = 0.25mA$.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VCF320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.
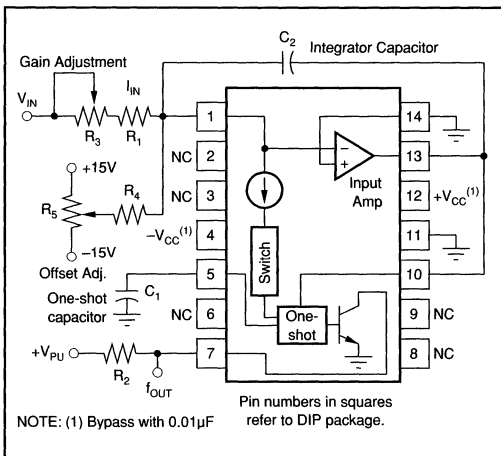
FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.
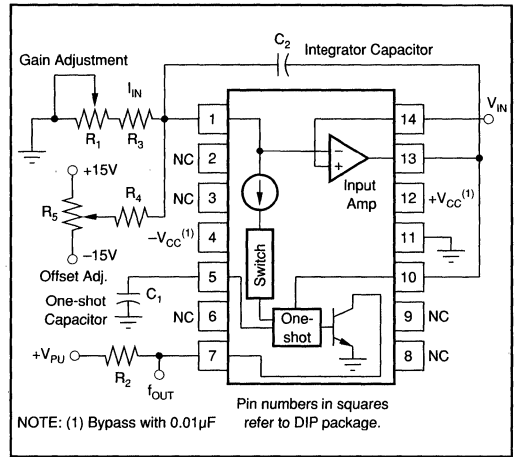
FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general, the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, (5) selecting the integrator capacitor C_2, and (6) selecting the output pull-up resistor, R_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected.

The nominal value is R_1 is

$$R_1 = \frac{V_{IN} max}{0.25mA}$$

$$(10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1 \, NOM} = \frac{V_{IN}}{7.5 \, R_1 \, f_{OUT}}$$

$$(11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1(pF) = \frac{33 \times 10^6}{f_{FS}} - 15$$

$$(12)$$

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VOLTAGE-TO-FREQUENCY CONVERTERS

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at D_{FS} = 25%.
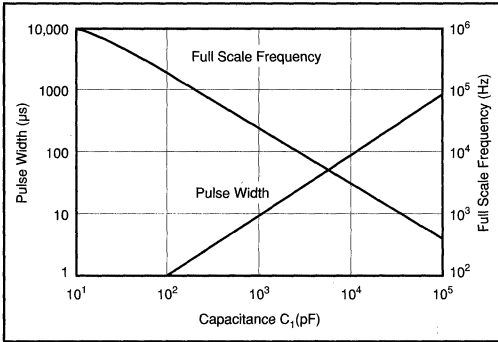
FIGURE 8. Output Pulse Width (D_{FS} = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator determine a range of acceptable values,

$$C_2 \ (\mu F) = \begin{cases} 100/f_{FS}; \text{ if } f_{FS} \leq 100\text{kHz} & (13) \\ 0.001; \text{ if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005; \text{ if } f_{FS} > 500\text{kHz} \end{cases}$$

Output Pull Up Resistor R_2

The open collector output can sink up to 8mA and still be TTL-compatible. Select R_2 according to this equation:

$$R_2 \text{ min } (\Omega) \ V_{PULLUP}/(8\text{mA} - I_{LOAD})$$

A 10% carbon film resistor is suitable for use as R_2.

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for initial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1 to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat stems 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 (D_{FS} = 0.25)

$$C_1 = [(33 \times 10^6)/f_{MAX}] - 15 \qquad [(66 \times 10^6)/f_{MAX}] - 15$$
$$\text{if } D_{FS} = 0.5$$
$$= [(33 \times 10^6)/100\text{kHz}] - 15$$
$$= 315\text{pF}$$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 (D_{RS} = 0.25)

$$R_1 + R_3 = V_{IN} \text{ max}/0.25\text{mA} \qquad V_{IN} \text{ max}/0.5\text{mA}$$
$$\text{if } D_{FS} = 0.5$$
$$= 10\text{V}/0.25\text{mA}$$
$$= 40\text{k}\Omega$$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$$C_2 = 10^2/F_{MAX}$$
$$= 10^2/100\text{kHz}$$
$$= 0.001\mu\text{F}$$

Choose a 0.001μF capacitor with ±5% tolerance.

Selecting R$_2$

R$_2$ = V$_{PULLUP}$/(8mA − I$_{LOAD}$)

=5V/(8mA − 1.6mA), one TTL-load = 1.6mA

=781Ω

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C$_3$ to make t = 0.1t (see Figure 9). For input signals with amplitudes less than 5V, pin 10

should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold.

Errors are nulled using 0.001 X full scale frequency to null offset, and full scale frequency to null the gain error. The procedure is given on this page. Use equations from V/F calculations to find R$_1$, R$_3$, R$_4$, C$_1$ and C$_2$.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits

Figures 10-14 show typical applications of the VFC320.
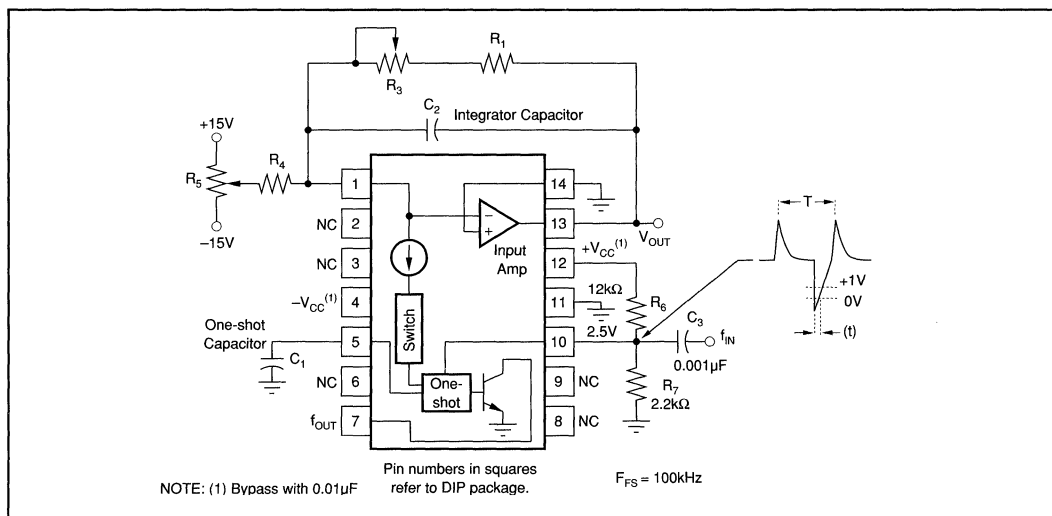
FIGURE 9. Connection Diagram for F/V Conversion.
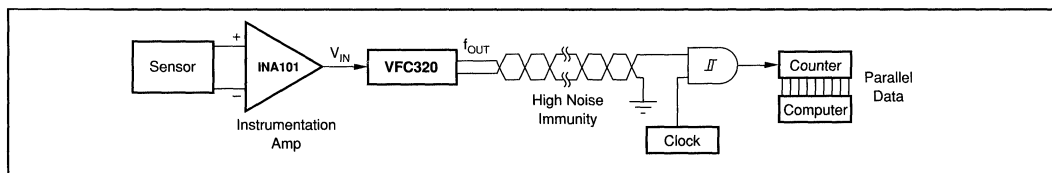
FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.
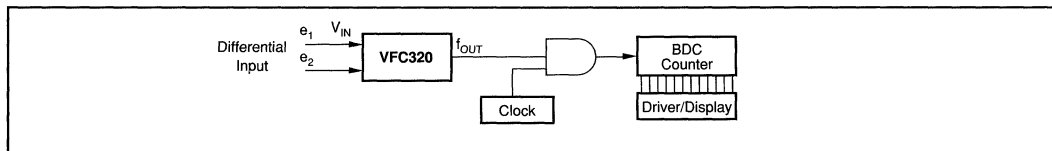
FIGURE 11. Inexpensive Digital Panel Meter.

VFC320

7

VOLTAGE-TO-FREQUENCY CONVERTERS
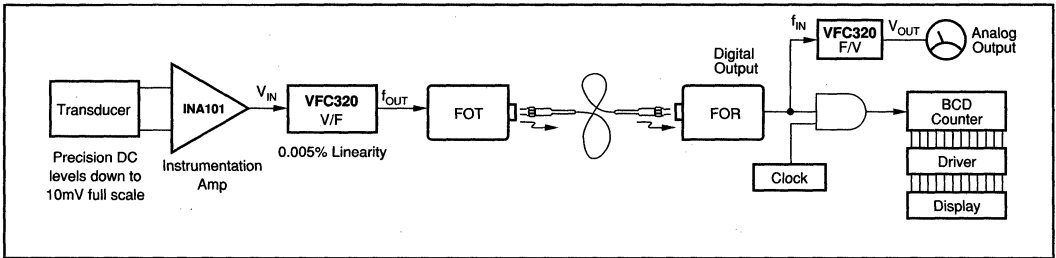
FIGURE 12. Remote Transducer Readout via Fiber Optic Link (Analog and Digital Output).
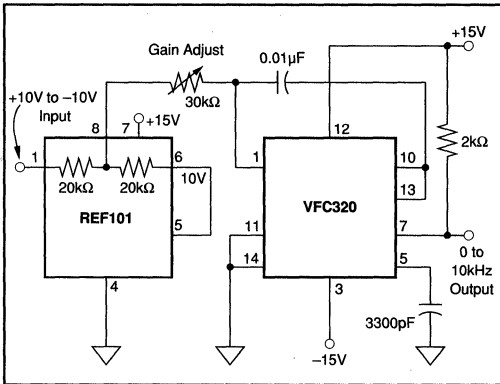
FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.
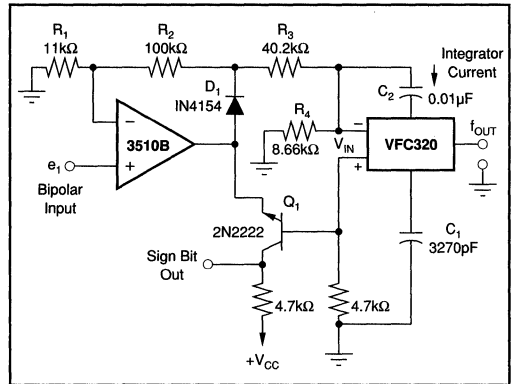
FIGURE 14. Absolute value circuit with the VFC320. Op amp, D_1 and Q_1 (its base-emitter junction funtioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to | e_1 |. The sign bit output provides indication of the input polarity.

8 Digital Audio Products

Burr-Brown pioneered the digital audio industry a decade ago with the introduction of the world's first IC digital-to-analog converter specifically designed for audio applications. Burr-Brown continues to be a leader in this field with a complete line of D/As, A/Ds and Digital filters for all ranges of digital audio—from consumer to professional.

The selection guide, below, will assist in the selection of the proper component for each application—some of the newer products are:

PCM1702—This high-end, 20-bit, D/A is the same architecture and performance as the world famous PCM63 (20 bit, –96dB THD+N). It is constructed using state-of-the-art 1.2μ BiCMOS technology allowing it to be packaged in a small, 20-pin SOIC package. The best choice when highest performance in a small package is required.

PCM1700—This mid-range, 18-bit, D/A is a popular choice for consumer and professional applications where price/performance is of major concern.

PCM1710—This dual D/A offers the maximum performance (–88dB THD+N) in an economy converter for consumer applications. It is a complete converter and contains a digital filter, output low pass filters and op amps.

PCM1712/14/15—These derivations of the popular PCM1710 are tailored for specific applications. The PCM1712 is optimized for economy consumer applications. The PCM1714 is configured for music instruments. The PCM1715 has the output flexability required for communications, multi-media and DSP.

PCM/DF1760—This combination provides 20-bit stereo A/D conversion with performance levels required by high-end consumer and pro audio applications.

PCM/DF1750—For mid-range (18-bit) A/D requirements, there is no better price/performance choice.

DIGITAL AUDIO PRODUCTS

AUDIO DIGITAL-TO-ANALOG CONVERTERS   Boldface = NEW   8

Model	Resolution (Bits)	Max Update Rate	Max THD + N (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package[1]	Max Power Dissipation (mW)	Page No.
PCM53	16	500kHz	–88dB (JP) –92dB (KP)	±10V, ±1mA	Parallel	±15, +5	DDIP	600	A
PCM54	16	500kHz	–82dB (HP) –88dB (JP) –92dB (KP)	±3V, ±1mA	Parallel	±5 to ±12	DDIP	300	8.2.52
PCM55	16	500kHz	–82dB (HP) –88dB (JP)	±3V, ±1mA	Parallel	±5	SO	125	8.2.52
PCM56	16	800kHz	–82dB (P) –88dB (P-J) –92dB (P-K)	±3V, ±1mA	Serial Latched	±5 to ±12	DIP, SO	260	8.2.55
PCM1710	**Dual16/20**	**48KHz**	**–88dB**	**3.2Vpp**	**Serial**	**+5**	**SO**		**8.2.116**
PCM1712	**Dual 16**	**48kHz**	**–87dB (typ)**	**3.1Vpp**	**Serial**	**+5**	**SO**	**225mW (typ)**	**8.2.125**
PCM1714	**Dual 18/20**	**44.1kHz (typ)**	**–96dB (typ)**	**2.8Vpp**	**Serial**	**+5**	**SO**	**125mW (typ)**	**8.2.135**
PCM1715	**Dual 16**	**44.1kHz (typ)**	**–92dB (typ)**	**3.2Vpp**	**Serial**	**+5**	**SO**	**350mW**	**8.2.139**
PCM66	16	200kHz	–82dB (P) –88dB (P-J)	2.6Vp-p, 2-Channel	Serial Latched	+5 Latched	SO	50	8.2.84

AUDIO DIGITAL-TO-ANALOG CONVERTERS (Continued)   Boldface = NEW

Model	Resolution (Bits)	Max Update Rate	Max THD + N (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package[1]	Max Power Dissipation (mW)	Page No.
PCM1700 (Dual DAC)	18	800kHz	−82dB (P) −88dB (P-J) −92dB (P-K)	±3V, ±0.67mA	Serial Latched	±5	DDIP, SO	475	8.2.103
PCM58	18	1MHz	−92dB (P) −94dB (P-J) −96dB (P-K)	±1mA	Serial Latched	+5, −12	DDIP	400	8.2.65
PCM61	18	800kHz	−82dB (P) −88dB (P-J) −92dB (P-K)	±3V, ±1mA	Serial Latched	±5 to ±12	DDIP	260	8.2.70
PCM63	20	1MHz	−88dB (P) −92dB (P-J) −96dB (P-K)	±2mA	Serial Latched	±5	DDIP	300	8.2.74
PCM67/69 (Dual)	18	1MHz	−82dB (P) −88dB (P-J) −92dB (P-K)	1.2mA	Serial Latched	+5	DIP, SO	105	8.2.91
PCM1702	20	1MHz	−88dB (P, U) −92dB (P-J) −96dB (P-K)	±1.2mA	Serial Latched	±5	DIP, SO	250	8.2.108

NOTE: (1) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, SO = Small Outline Surface Mount.

AUDIO ANALOG-TO-DIGITAL CONVERTERS   Boldface = NEW

Description	Model	Resolution (Bits)	Typical DC Linearity Accuracy	Input Range (V)	Conversion Time (µs)	THD+N dB, Max (V_{IN} = ±FS)	Output Format	Pkg[1]	Page No.
Low Cost	PCM78	16	14-Bit	±3	5	−88	Serial	DDIP	8.1.3
Dual	PCM1750	18	14-Bit	±2.75	5	−90	Serial	DDIP, SO	8.1.19
Dual Channel	PCM1760	20	16-Bit	±2.5	20	−90 88	Serial	DDIP, SO	8.1.37

NOTE: (1) DDIP = 0.6" wide DIP, SO = Small Outline Surface Mount.

DIGITAL FILTERS   Boldface = NEW

Description	Model	Input Resolution (Bits)	Typical Resolution (Bits)	Passband Ripple (dB)	Stopband Attenuation (dB)	Power Supply (V)	Pkg[1]	Page No.
Dual Interpolation	DF1700	16	16/18/20	±0.00005dB	>100dB	+5V	DIP/SO	8.3.148
Dual 1/4 or 1/2 Decimating	DF1750	16/18	18	<±0.0005dB	>95dB	+5V	DIP/SO	8.3.158
Dual Decimating	DF1760	20	20	±0.0001dB	>94dB	+5V	DIP/SO	8.1.37

NOTE: (1) DIP = 0.3" wide DIP, SO = Small Outline Surface Mount.

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[BB]
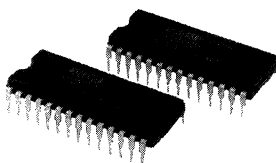
PCM78P

**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

16-Bit Audio
ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **LOW COST/HIGH PERFORMANCE 16-BIT
  AUDIO A/D CONVERTER**
● **FAST 5µs MAX CONVERSION TIME
  (4µs typ)**
● **VERY LOW THD+N (typ –88dB at FS;
  max –82dB)**
● **±3V INPUT RANGE**
● **TWO SERIAL OUTPUT MODES PROVIDE
  VERSATILE INTERFACING**
● **COMPLETE WITH INTERNAL REFERENCE
  AND CLOCK IN 28-PIN PLASTIC DIP**
● **±5V TO ±15V SUPPLY RANGE (600mW
  Power Dissipation)**

APPLICATIONS

● **DSP DATA ACQUISTION**
● **TEST INSTRUMENTATION**
● **SAMPLING KEYBOARD SYNTHESIZERS**
● **DIGITAL AUDIO TAPE**
● **BROADCAST AUDIO PROCESSING**
● **TELECOMMUNICATIONS**

DESCRIPTION

The PCM78P is a low-cost 16-bit A/D converter which
is specifically designed and tested for dynamic appli-
cations. It features very fast, low distortion perform-
ance (4µs/–88dB THD+N typical) and is complete
with internal clock and reference circuitry. The PCM78P
is packaged in a reliable, low-cost 28-pin plastic DIP
and data output is available in user-selectable serial
output formats. The PCM78P is ideal for digital audio
tape (DAT) recorders. Many similar applications such
as digital signal processing and telecom applications
are equally well served by the PCM78P.

The PCM78P uses a SAR technique. Analog and
digital portions are efficiently partitioned into a high-
speed, bipolar section and a low-power CMOS section.
The PCM78P has been optimized for excellent dy-
namic performance and low cost.

PCM78

8.1

DIGITAL AUDIO PRODUCTS—A/D

8.1.3

SPECIFICATIONS

ELECTRICAL

$T_C = +25°C$, $+V_{DD} = +5V$, and $±V_{CC} = ±12V$, and one minute warm-up in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	PCM78P MIN	PCM78P TYP	PCM78P MAX	UNITS
RESOLUTION				16	Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		−3		+3	V
Input Impedance			1.5		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	$I_{IH} = +40µA$	+2		+5.5	V
V_{IL}	$I_{IL} = −100µA$	0		+0.8	V
V_{OH}	$I_{OH} = 2TTL$ Loads	+2.4			V
V_{OL}	$I_{OL} = 2TTL$ Loads			+0.4	V
Data Format			Serial BOB or BTC		
Convert Command			Negative Edge [1]		
Pulse Width		25	50		ns
CONVERSION TIME			4	5	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO-NOISE RATIO (SNR)[2]	$f_S = 200kHz/T_{CONV} = 4µs$[3]				
f = 1kHz (0dB)	BW = 20kHz		90		dB[4]
f = 10kHz (0dB)	BW = 100kHz		80		dB
TOTAL HARMONIC DISTORTION[5]	$f_S = 200kHz/T_{CONV} = 4µs$				
f = 1kHz (0dB)	BW = 20kHz		−91		dB
f = 19kHz (0dB)	BW = 20kHz		−90		dB
f = 10kHz (0dB)	BW = 100kHz		−90		dB
f = 90kHz (0dB)	BW = 100kHz		−89		dB
TOTAL HARMONIC DISTORTION + NOISE[6]	$f_S = 200kHz/T_{CONV} = 4µs$				
f = 1kHz (0dB)	BW = 20kHz		−88	−82	dB
f = 1kHz (−20dB)	BW = 20kHz		−74	−68	dB
f = 1kHz (−60dB)	BW = 20kHz		−34		dB
f = 19kHz (0dB)	BW = 20kHz		−87		dB
f = 10kHz (0dB)	BW = 100kHz		−82		dB
f = 90kHz (0dB)	BW = 100kHz		−81		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±20		mV
Differential Linearity Error			±0.002		% of FSR[7]
Integral Linearity Error			±0.003		% of FSR
Missing Codes			None		14 Bits[8]
DRIFT					
Gain	0°C to +70°C		±25		ppm/°C
Bipolar Zero	0°C to +70°C		±4		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.008		%FSR/%V_{CC}
$−V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.003		%FSR/%V_{DD}
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.75		+15.6	V
$−V_{CC}$		−4.75		−15.6	V
$+V_{DD}$		+4.75		+5.25	V
Current: $+V_{CC}$	$+V_{CC} = +12V$		+15		mA
$−V_{CC}$	$−V_{CC} = −12V$		−21		mA
$+V_{DD}$	$+V_{DD} = +5V$		+7		mA
Power Dissipation	$±V_{CC} = ±12V$		575		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		−50		+100	°C
Operating		−25		+85	°C

NOTES: (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. See detailed text on timing for convert command description when using external clock. (2) Ratio of Noise rms/Signal rms. (3) f = input frequency; f_S = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms. (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR: Full-Scale Range = 6Vp-p. (8) Typically no missing Codes at 14-bit resolution.

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTIUON
1	Analog In	I	Analog Signal Input (1.5kΩ impedance).
2	$-V_{CC}$	I	Analog power supply (–5V to –15V).
3	MSB Adjust	I	Internal adjustment point to allow adjustment of MSB major carry.
4	$+V_{DD}$	I	Power connection for comparator (+5V).
5	No Connection	—	No internal connection.
6	Comparator Common	I	Comparator common connection. Connect to ground.
7	$\overline{MSB}$	O	Parallel output of bit 1 (MSB) inverted.
8	BTC/BOB Select	I	Two's complement (open) or straight binary (grounded) data output format selection.
9	Status	O	Output signal held high until conversion is complete.
10	Clock Out	O	Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ~24ns and same duty cycle).
11	R_1C_1	I	RC connection point used to generate internal clock. Sets clock high time. See text for details.
12	R_2C_2	I	RC connection point used to generate internal clock. Sets clock low time. See text for details.
13	S_{OUT2}	O	Internal shift register containing the previous conversion result. (Alternate latched data output mode).
14	$+V_{DD}$	I	Power connection for +5V logic supply.
15	S_{OUT1}	O	Primary real-time data output synchronized to clock out.
16	External Clock	I	External clock input point (internal clock must be disabled).
17	Int/Ext Clock Select	I	Selects either internal or external clock mode (low = internal; open = external).
18	Short Cycle	I	Terminates conversion at less than 16-bits (open for 16-bit mode). See text for details.
19	Convert Command	I	Starts conversion process (can optionally be generated internally).
20	S_{OUT2} Latch	I	Latches previous conversion result for readout (must be issued with the S_{OUT2} clock to initiate latch and an internal convert command).
21	S_{OUT2} Clock	I	Used to read out internally latched data from previous conversion.
22	Digital Common	I	Digital grounding pin.
23	$+V_{CC}$	I	Analog supply connection (+5V to +15V).
24	V_{POT}	O	Voltage output (~2.5V) for optional adjustment of MSB transition.
25	Reference Decouple	I	Reference decoupling point.
26	Analog Common	I	Analog grounding pin.
27	Reference Out	O	2V reference out. Should not be used except as shown in connection diagram.
28	Speed Up	I	Connection point for a capacitor to speed reference settling. See text for details.

NOTE: Analog and digital commons are connected internally.

INPUT/OUTPUT RELATIONSHIPS

ANALOG INPUT	CONDITION	DIGITAL OUTPUT	
		BTC	BOB
+2.999908V	+ Full Scale	7FFF Hex	FFFF Hex
–3.000000V	–Full Scale	8000 Hex	0000 Hex
0.000000V	Bipolar Zero	0000 Hex	8000 Hex
–0.000092V	Zero-1 LSB	FFFF Hex	7FFF Hex

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM78P	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common .... 0 to +16.5V
$-V_{CC}$ to Analog Common .... 0 to –16.5V
$-V_{DD}$ to Analog Common .... 0 to +7V
Analog Common to Digital Common .... ±0.5V
Logic Inputs to Digital Common .... –0.3V to V_{DD} + 0.5V
Analog Inputs to Analog Common .... ±16.5V
Lead Temperature (soldering, 10s) .... +300°C
Stresses above these ratings may permanently damage the device.

PCM78

8.1

DIGITAL AUDIO PRODUCTS—A/D

TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = ±15V$ unless otherwise noted.

BPZ ERROR vs TEMPERATURE

BIPOLAR GAIN ERROR as % FSR
25°C; N = 33 UNITS

PSRR at +FS INPUT

PSRR at −FS INPUT

V_{REF} vs TEMP

I_{SS} vs SUPPLY VOLTAGE
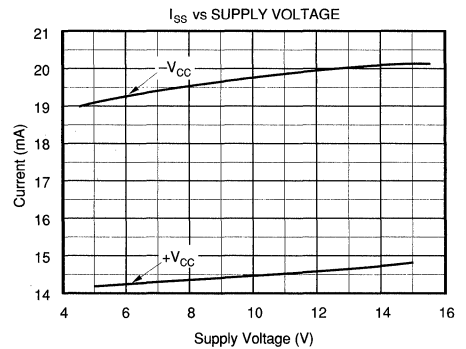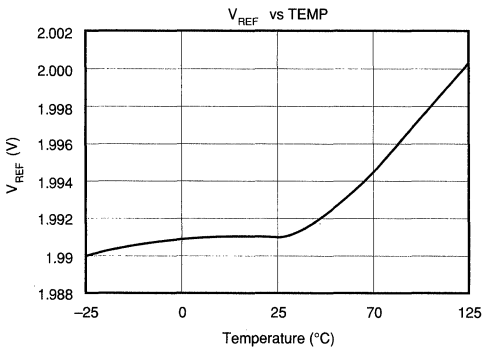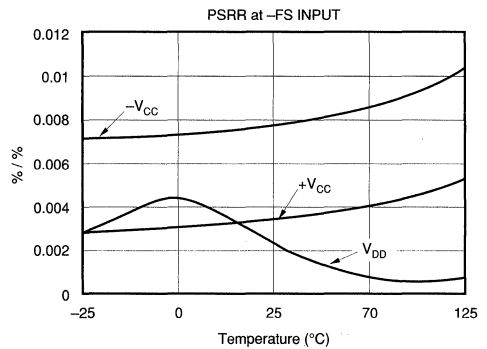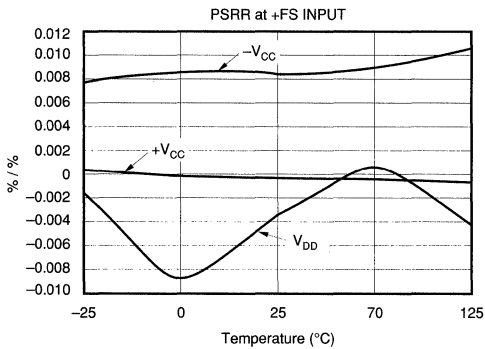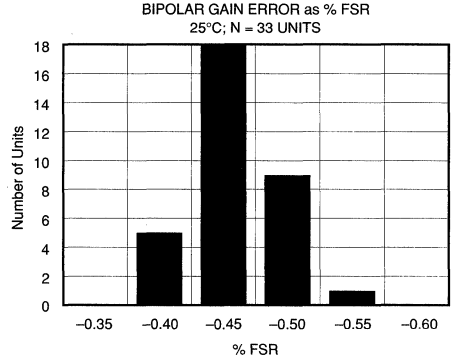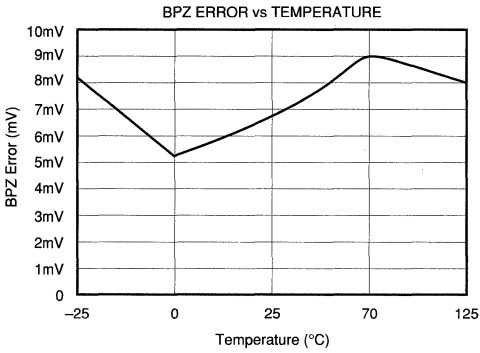
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

INTEGRAL NONLINEARITY
at −25°C

DIFFERENTIAL NONLINEARITY
at −25°C

INTEGRAL NONLINEARITY
at 0°C

DIFFERENTIAL NONLINEARITY
at 0°C
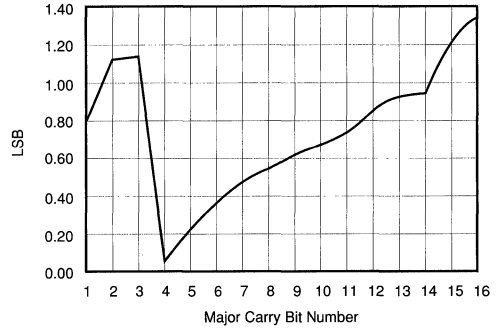
INTEGRAL NONLINEARITY
at 25°C
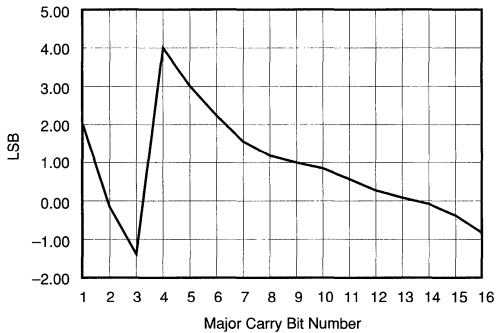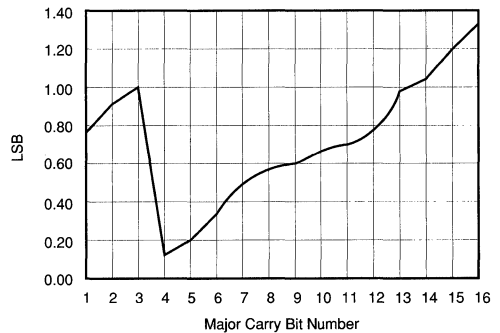
DIFFERENTIAL NONLINEARITY
at 25°C

PCM78

8.1

DIGITAL AUDIO PRODUCTS—A/D

TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted. Histograms done with conversion time = 8µs.

INTEGRAL NONLINEARITY
at 70°C
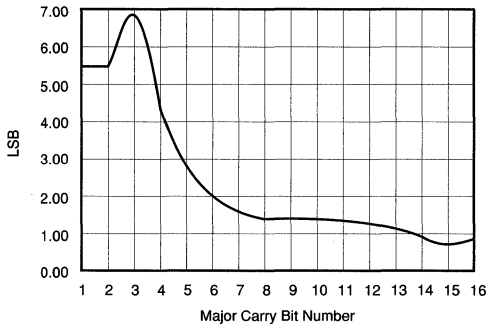
DIFFERENTIAL NONLINEARITY
at 70°C
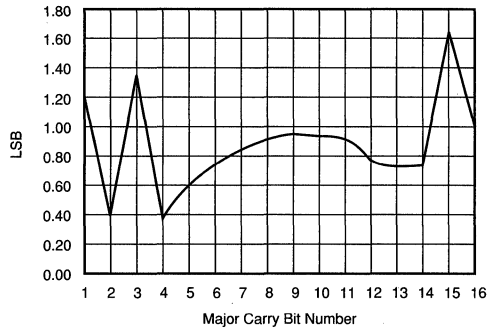
INTEGRAL NONLINEARITY
at 125°C

DIFFERENTIAL NONLINEARITY
at 125°C
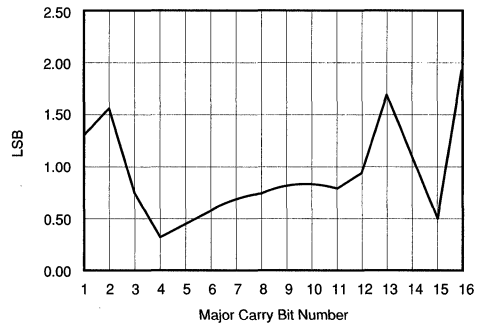
INTEGRAL NONLINEARITY ERROR
(to14-Bit LSB)

DIFFERENTIAL NONLINEARITY ERROR
(to 14-Bit LSB)

BURR - BROWN®

BB

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25°C$, $V_{CC} = ±15V$ unless otherwise noted. Histograms done with Conversion Time = 8µs.

SPECTRAL RESPONSE, $f_{IN} \approx$ 1kHz

Input Frequency 976.6Hz

Fund:	−0.07dB	6th:	−135.02dB
2nd:	−87.80dB	THD:	−87.10dB
3rd:	−97.43dB	SNR:	81.05dB
4th:	−102.35dB	SINAD:	80.09dB
5th:	−107.86dB		

SPECTRAL RESPONSE, $f_{IN} \approx$ 20kHz

Input Frequency 19970.7Hz

Fund:	−0.08dB	6th:	−101.44dB
2nd:	−92.21dB	THD:	−88.12dB
3rd:	−91.59dB	SNR:	79.25dB
4th:	−101.23dB	SINAD:	78.72dB
5th:	−109.32dB		

SPECTRAL RESPONSE, $f_{IN} \approx$ 1kHz

Input Frequency 976.6Hz

Fund:	−20.07dB	6th:	−110.06dB
2nd:	−108.36dB	THD:	−76.75dB
3rd:	−100.44dB	SNR:	61.79dB
4th:	−111.52dB	SINAD:	61.65dB
5th:	−102.06dB		

SPECTRAL RESPONSE, $f_{IN} \approx$ 20kHz

Input Frequency 19970.7Hz

Fund:	−19.94dB	6th:	−107.32dB
2nd:	−105.69dB	THD:	−72.81dB
3rd:	−95.90dB	SNR:	61.60dB
4th:	−106.71dB	SINAD:	61.28dB
5th:	−97.57dB		

SPECTRAL RESPONSE, $f_{IN} \approx$ 1kHz

Input Frequency 976.6Hz

Fund:	−60.06dB	6th:	−106.00dB
2nd:	−109.18dB	THD:	−42.15dB
3rd:	−108.31dB	SNR:	21.73dB
4th:	−134.66dB	SINAD:	21.69dB
5th:	−114.73dB		

SPECTRAL RESPONSE, $f_{IN} \approx$ 20kHz

Input Frequency 19970.7Hz

Fund:	−59.96dB	6th:	−110.11dB
2nd:	−109.09dB	THD:	−41.60dB
3rd:	−124.49dB	SNR:	21.93dB
4th:	−116.40dB	SINAD:	21.88dB
5th:	−112.18dB		

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DIGITAL AUDIO PRODUCTS—A/D

TYPICAL
PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

THD+N vs CONVERSION TIME (0dB)

THD+N (%) vs Convert Time (µs)

THD+N vs CONVERSION TIME (−20dB)

THD+N (%) vs Convert Time (µs)

THD+N vs CONVERSION TIME (−60dB)

THD+N (%) vs Convert Time (µs)

THEORY OF OPERATION

The PCM78P is a successive approximation A/D converter; this type of converter is well suited to high speed and resolution. The accuracy of a successive approximation converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about zero, and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion + Noise (THD + N) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as quantization errors. The THD+N specification is most useful in audio or dynamic signal processing applications. To be useful, THD + N should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for dynamic applications.

DYNAMIC RANGE

Dynamic range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels. The theoretical dynamic range of a converter is approximately 6 x *n*, where *n* is the number of bits of resolution. A 16-bit converter would thus have a theoretical dynamic range of 96dB. The actual useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.
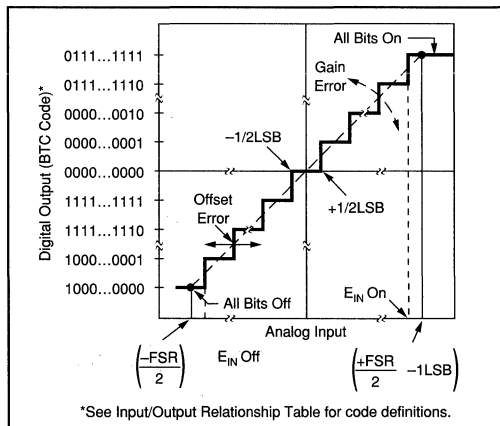
FIGURE 1. Input vs Output for Ideal Bipolar A/D Converter.
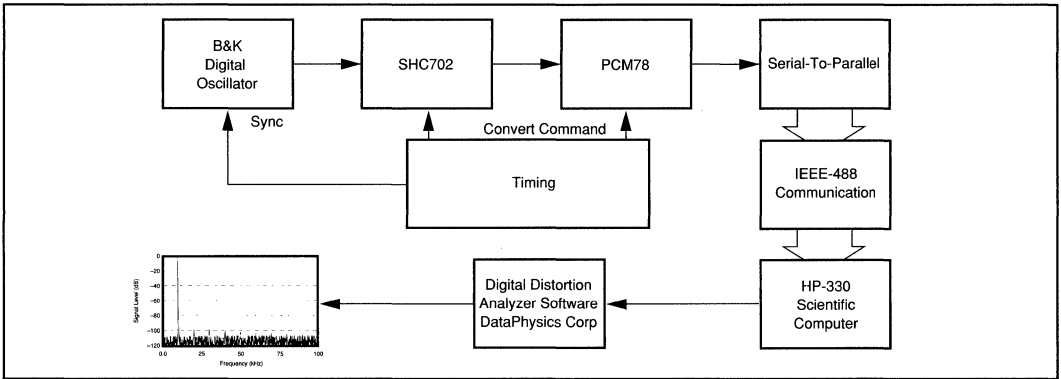
FIGURE 2. Block Diagram of Distortion Test Circuit.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION

Evaluating distortion specifications can be a difficult task, as distortion is often specified in different ways. Total Harmonic Distortion (THD) is defined as the ratio of the square root sum of the squares of the value of rms harmonics to the value of the rms fundamental and is expressed in percent or dB. Note that this measurement only includes energy present in those frequencies which would contain harmonics, and therefore is less than Total Harmonic Distortion plus Noise.

The Total Harmonic Distortion plus Noise (THD + N) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics and rms noise to the value of the rms fundamental and is expressed in percent or dB. This is the most meaningful measurement of a dynamic converter's performance because it includes all energy present in the signal that is not fundamental. A block diagram of the test circuit used to measure the THD and

THD + N of the PCM78 is shown in Figure 2. This digital system is capable of differentiating harmonic energy and noise; conventional distortion analyzers which operate on a tracking notch filter principle cannot distinguish this energy, and therefore only measure THD + N. Unfortunately, in the past, these systems were used for measuring distortion performance of converters, and the distortion was often simply specified as "THD", when in fact it was really THD + N. For this reason, it is often confusing to compare specifications of converters unless one knows exactly what was being measured.

If we assume that the error due to the test circuit of Figure 2 is negligible, then the rms value of the PCM78 error referred to the input can be shown to be

$$THD + N = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i) + E_Q(i) + E_N(i)\right]^2}}{E_{rms}} \times 100\%$$

where N is the number of samples, $E_L(i)$ is the linearity error at each sample, $E_Q(i)$ is the quantization error at each
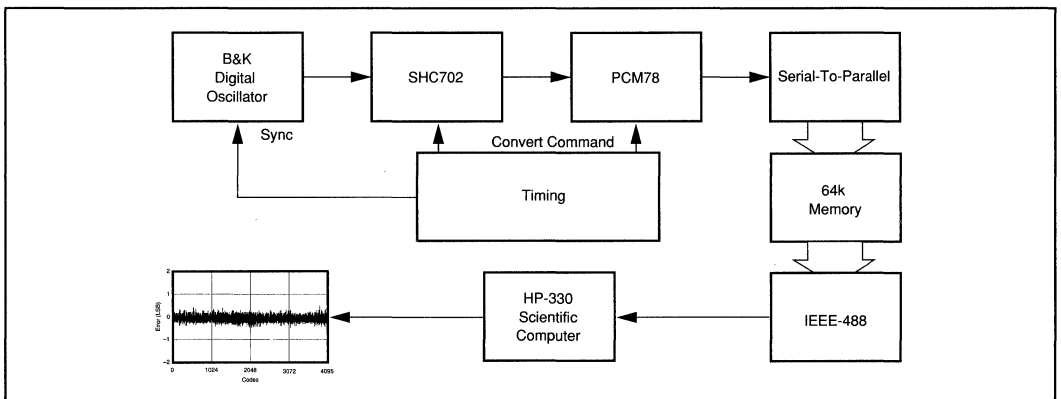
FIGURE 3. Block Diagram of Histogram Test.

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DIGITAL AUDIO PRODUCTS—A/D
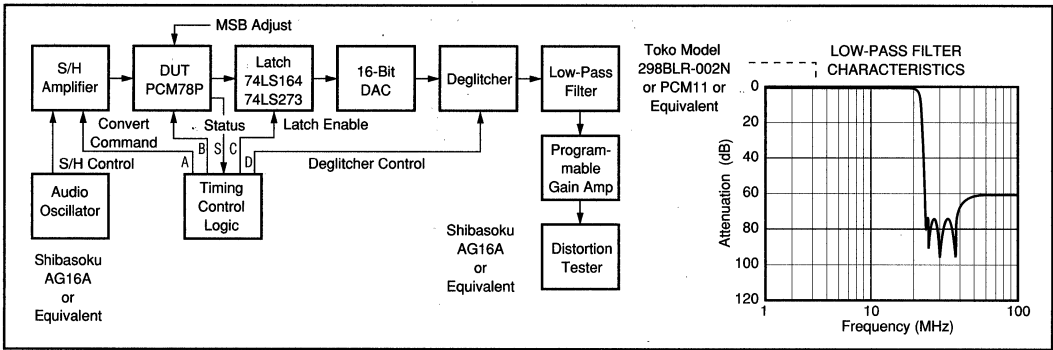
FIGURE 4. Production Distortion + Noise Test System Block Diagram.
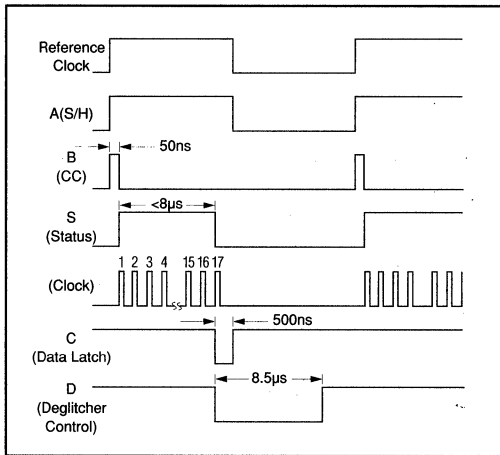
FIGURE 5. Timing Diagram for Figure 4.

sample, and $E_N(i)$ is the residual noise energy present at each sample. Similarly, THD alone can be expressed as

$$THD = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i)\right]^2}}{E_{rms}} \times 100\%$$

These expressions indicate that there is a correlation between THD + N and the square root of the sum of the squares of the linearity errors at each digital word of interest. In order to find this error at each code, a histogram test must be performed on the PCM78, as illustrated in Figure 3. The histogram for every converter is unique, as the linearity errors from converter to converter will vary in their placement along the transfer function. Typical histogram data is shown in the Typical Curves.

However, this expression for THD + N does not mean that the worst case linearity error of the A/D is directly correlated to the THD + N because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM78 the test sampling frequency was chosen to be 200kHz, near the PCM78's fastest rate of conversion. The test frequencies used vary within the audio range, and are stepped in amplitude from 0dB, to –20dB, to –60dB.

In manufacturing the PCM78, the test system shown in Figure 4 is used to test for guaranteed THD + N.

ACCURACY VS CONVERSION TIME AND INPUT SIGNAL LEVEL

The relationship of THD vs input signal level and THD vs conversion time is shown is the typical curves. Slowing the conversion time to more than 8μs results in little added benefit in terms of THD + N.

For applications which are not as concerned with dynamic performance but require DC accuracy and linearity, it is best to use the PCM78 at the longest conversion time possible for the system requirements. Slowing the PCM78 to 8μs-10μs conversion time results in a substantial improvement in linearity. The typical curves show DNL and INL plots for a typical device, at an 8μs conversion time. Due to the segmented architecture of the internal DAC used in the successive approximation conversion technique, significant differential linearity errors occur near bits 3 and 4. Allowing more settling time for the DAC (by slowing the conversion speed) will improve this differential linearity error and give equivalent performance to more costly DC-specified 12-bit to 14-bit A/D converters.

SYSTEM DESIGN CONSIDERATIONS

DIGITAL CIRCUIT CONNECTIONS

The PCM78 comes complete with an internal clock circuit, or it may be clocked by an external clock. Choosing which mode to operate with depends upon the application for which the PCM78 will be used. In an application where the sample rate may not be fixed (transient recording, etc.), using the internal clock set to give a very fast conversion may be the best solution. In systems where the sample rate is fixed, an external clock is probably the better choice since it will allow the digital system design to be synchronous.

In either case, the PCM78 requires 17 clock cycles to complete a conversion. To calculate the clock frequency necessary for a given conversion time, the following equation may be used:

$$f_{CLOCK} = \frac{17}{\text{Conversion Time}}$$

The internal clock operates only during a conversion, and is gated on by the falling edge of the convert command. See Figure 6. The internal clock is available on pin 10, Clock Out. The high and low time of this clock is set by R_1C_1 and R_2C_2 respectively. The duty cycle of the clock should be between 20% to 80%, and may be set to 50% for simplicity.

$$\text{Clock High Time (in ns)} = 1.32R_1C_1$$

$$\text{Clock Low Time (in ns)} = 1.32R_2C_2$$

$$\text{R in k}\Omega; \text{C in pF.}$$

These equations are approximate (±5%); they should be used for determining an initial part value which will then need to be "tweaked" for accurate timing. If highly accurate time bases are required, use of an external clock is recommended.

The external clock is applied at pin 16, and the Int/Ext Clock select (pin 17) should be left open (an internal pull-up resistor assures that the logical state of an open pin is "1"). Using the external clock requires careful placement in time of the convert command. Figure 7 diagrams the recommended timing with an external clock. A simple circuit which assures the proper timing of the convert command is shown in Figure 8.

Due to the design of the Clock/Logic chip in the PCM78, a conversion is begun inside the PCM78 by an asynchronous state machine. This places stringent requirements on the timing of the convert command, as improper timing can cause metastable states within this state machine. Using the circuitry shown in Figure 8, the user is assured of consistent operation, and these invalid states within the state machine are entirely avoided. (Note that this is not a consideration when using an internal clock, as nothing is being clocked when a convert command is presented to the PCM78).

The Clock Out function is a gated form of the external clock, i.e. the 17 clock cycles used in the conversion are present on this pin during conversion. This allows use of a continuous external clock, with Clock Out being the clock that the converter is actually using for conversion. Note that this is simply a delayed (~24ns) version of the external clock, and will have the same frequency and duty cycle.

The S_{OUT2} Latch enables the user to latch data from the previous conversion and read it out at a higher speed than the convert clock. This feature allows the converter to easily interface to digital filtering necessary for oversampling. See Figure 9 for timing information in this mode.

In this mode, the PCM78 generates its own internal convert command when the S_{OUT2} Clock goes high within ±50ns of S_{OUT2} Latch going low; the external convert command may not be used, and pin 19 must be grounded. The timing diagram shows the recommended timing for using this mode. After the S_{OUT2} Latch control signal goes low, data from the SAR is loaded into the S_{OUT2} latch on the next rising edge of the S_{OUT2} Clock. This clock edge should occur prior to the next rising edge of the conversion clock (internal or external), since the SAR will reset itself prior to the latching
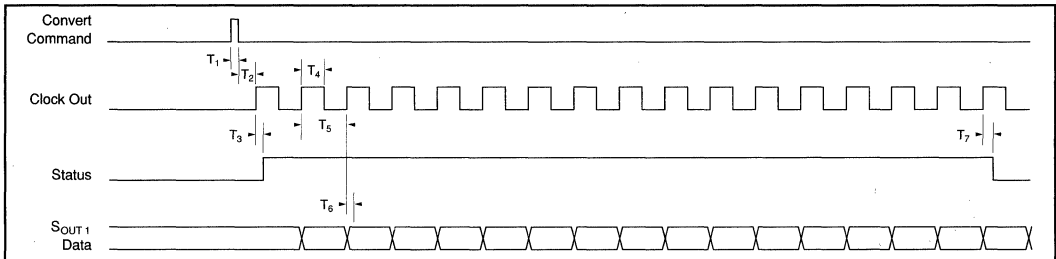
$T_A = +25°C$, $V_{DD} = +5V$, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns)		
		MIN	TYP	MAX
T_1	CONVERT COMMAND pulse width	25	50	(1)
T_2	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	60	70	85
T_3	Delay from rising edge of CLOCK OUT to rising edge of STATUS	8	10	30
T_4	INTERNAL CLOCK pulse width	50	125	450
T_5	INTERNAL CLOCK period	140	290	500
T_6	Delay from rising edge of CLOCK OUT to bit data valid	17	20	50
T_7	Delay from rising edge of 17th clock pulse to falling edge of STATUS	10	15	30

NOTE: (1) When using the internal clock, the clock does not operate until the Convert Command is low. It is therefore possible to keep the convert command high indefinitely, thereby keeping the PCM78 in a halt mode. The conversion cycle begins on the falling edge of convert command, and convert command must remain low during the entire conversion cycle in order to make the PCM78 operate properly.

FIGURE 6. Conversion Timing when using Internal Clock.

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DIGITAL AUDIO PRODUCTS—A/D

$T_A = +25°C$, $V_{DD} = +5V$, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns)		
		MIN	TYP	MAX
T_1	EXTERNAL CLOCK pulse width	50	125	(1)
T_2	EXTERNAL CLOCK period	140	290	(1)
T_3	Delay from falling edge of EXTERNAL CLOCK to rising edge of CONVERT COMMAND	−30	0	420
T_4	CONVERT COMMAND pulse width	10	50	200
T_5	Delay from falling edge of CONVERT COMMAND to rising edge of EXTERNAL CLOCK	20	50	430
T_6	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	40	75	460
T_7	Delay from rising edge of CLOCK OUT to rising edge of STATUS	6	10	30
T_8	Delay from rising edge of CLOCK OUT to bit data valid	15	17	20
T_9	Delay from rising edge of 17th clock pulse to falling edge of STATUS	8	10	30

NOTE: (1) The PCM78 does not contain dynamic digital circuitry, and can be clocked as slowly as the user wishes. In typical applications, the longest clock period may be as long as 1μs.

FIGURE 7. Conversion Timing when using External Clock.

if the convert clock rises before the S_{OUT2} Clock. This condition is avoided as long as the frequency of S_{OUT2} Clock is at least 1.5 times that of the conversion clock.

The internal convert command is generated upon S_{OUT2} Latch going low, and its falling edge occurs upon the first falling edge of S_{OUT2} Clock after S_{OUT2} Latch goes low. S_{OUT2} Latch should remain low for at least 2 cycles of S_{OUT2} Clock to insure proper latching. In many applications, the S_{OUT2} Latch can be the $2f_s$ signal present in many digital audio systems, typically known as WDCK. Figure 10 includes an example of this application.

The data read out on S_{OUT2} is from the conversion previously performed, while the data that is present on S_{OUT1} is the real time readout of the successive approximation as it occurs.

SHORT CYCLE

The PCM78 has the ability to be short cycled to a resolution less than 16 bits. This is accomplished by driving the Short Cycle pin (pin 18) low when the conversion is to be terminated, and holding it low until the next convert command is given. The circuit in Figure 11 will accomplish this function.
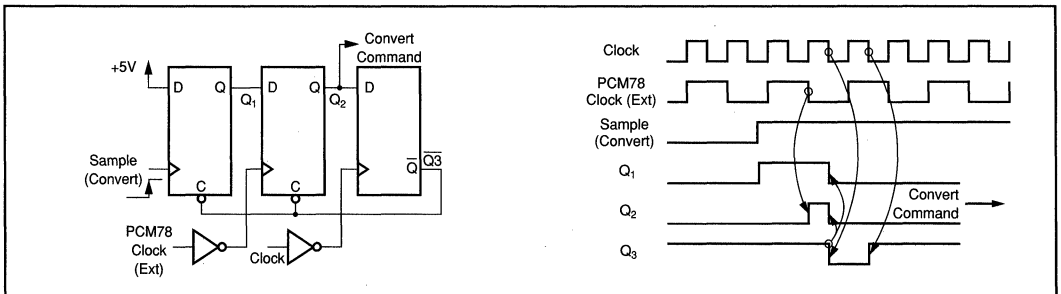
FIGURE 8. Convert Command Timing Circuit for Use with External Clock.

$T_A = +25°C$, $V_{CC} = +5V$, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns)		
		MIN	TYP	MAX
T_1	S_{OUT2} Latch pulse width	50	100	
T_2	S_{OUT2} Clock Cycle		24	
T_3	Delay from rising edge of CLOCK OUT to bit data valid		10	30
T_4	Delay from rising edge of S_{OUT2} Clock to rising edge of Ext Clock	50	125	
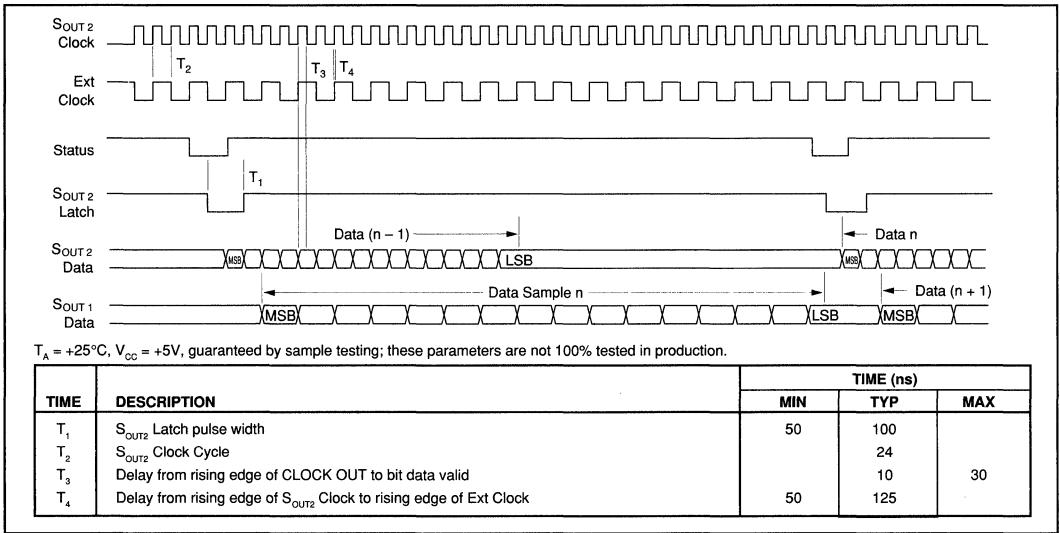
FIGURE 9. Timing when using S_{OUT2} Latch.
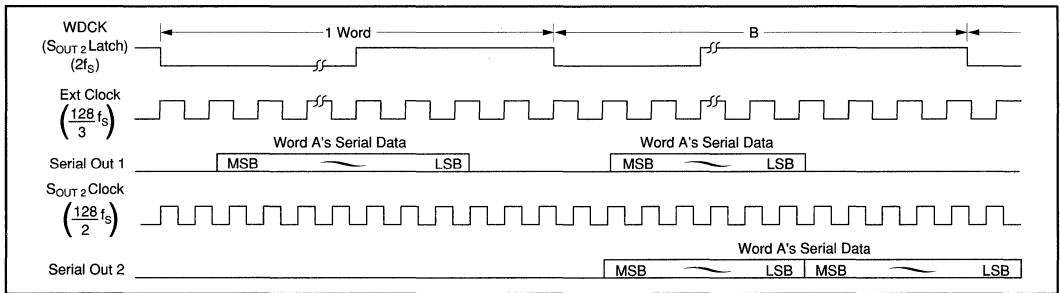
FIGURE 10. Application Example of S_{OUT2} Operation.

NO OF BITS	JUMPER				
	1	2	3	4	5
15	X	X	X	X	O
14	O	O	O	O	X
13	X	O	O	O	X
12	O	X	O	O	X
11	X	X	O	O	X
10	O	O	X	O	X
9	X	O	X	O	X
8	O	X	X	O	X

X: Off   0: On
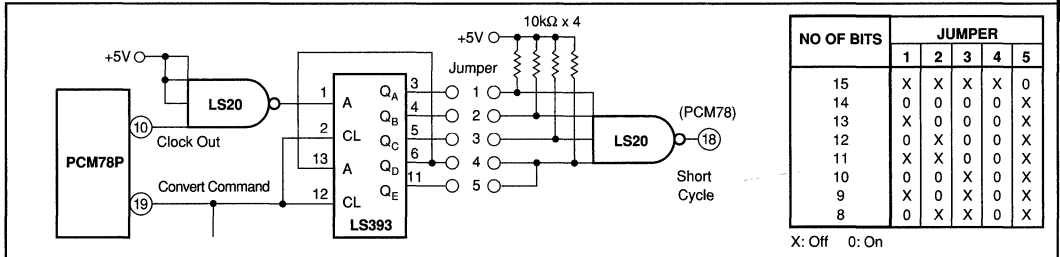
FIGURE 11. Short Cycle Circuit.
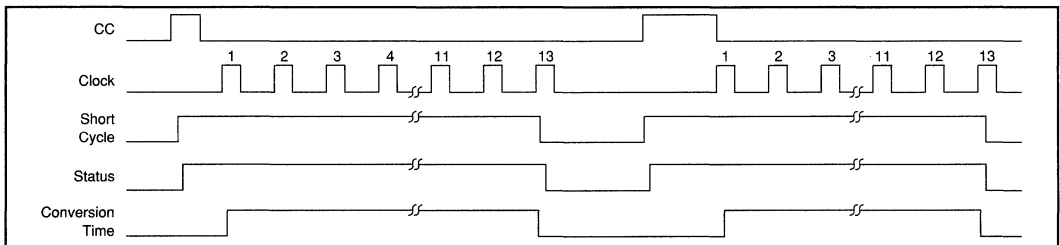
FIGURE 12. Short Cycle Operation Timing.

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DIGITAL AUDIO PRODUCTS—A/D

If Short Cycle is not held low until the next convert command is issued, the Status line will go high in synchronization with Short Cycle. This is because the operation of the Status line becomes invalid after Short Cycle is asserted. An example of the Short Cycle operation is shown in Figure 12.

In those systems where a user may not be using a continuous external clock, it is necessary to assure that a falling edge of external clock occurs after short cycle goes low. This is because conversion actually stops on the first falling edge of external clock after Short Cycle goes low.

ANALOG CIRCUIT CONSIDERATIONS

Layout Precautions

Analog and Digital Common are connected internally in the PCM78, and should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The input pin (pin 1) and the MSB adjust pin (pin 3) are both extremely sensitive to noise; digital lines should be kept away from these pins to avoid coupling digital noise into the sensitive analog circuitry.

Contact factory for a recommended PCB layout for the PCM78.

Power Supply Decoupling

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 13 to obtain noise free operation. These capacitors should be located as close to the ADC as possible. Bypass the 1μF electrolytic capacitors with 0.01μF ceramic or polystyrene capacitors for improved high frequency performance.
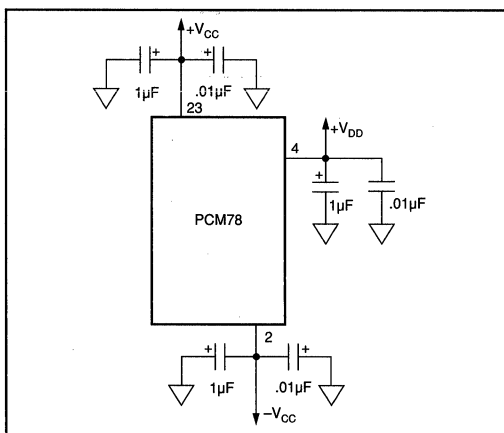
FIGURE 13. Recommended Power Supply Decoupling.

Reference Decoupling and Speed Up

In order to assure the lowest noise operation of the PCM78, the reference may be bypassed by three different capacitors. Pin 25 is a decoupling point for the reference to $-V_{CC}$. The

decoupling capacitor should range from 0.1μF to 4.7μF; larger values can cause reference settling problems which may manifest themselves as missing codes. This capacitor should be as close to the PCM78 as possible, to minimize the potential for coupling noise into the device; with a good board layout it may be best to leave this capacitor out of the circuit altogether, as the extra lead length may only cause more noise in the reference.

Pin 27 is a decoupling point to ground, as well as the output of the 2V reference. This point should not be used to supply reference voltage to external circuitry unless it is buffered. A 2.2μF capacitor is recommended, and the capacitor used here should not exceed 4.7μF.

Pin 28, the Speed Up pin, allows a capacitor to be connected to ground to facilitate reference settling. This does not speed up the conversion time, but it does reduce odd order harmonic distortion. As with the decoupling capacitor on pin 25, this may also contribute to noise; if harmonic content is most important in an application, this capacitor (0.1μF - 10μF) should be connected. In all other cases, it is best to leave the capacitor out of the circuit.

Input Scaling

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. The DAC inside the PCM78 has a ±2mA range, and the nominal ±3V input is scaled by a 1.5kΩ resistor. In order to scale to other ranges, see Table I for recommended scaling resistor values, connected as shown in Figure 14.

INPUT RANGE	R
±10V	8.2kΩ
±5V	3.3kΩ
NOTE: R values shown assume use of 1k trim pot to adjust for scale accuracy.	

TABLE I. PCM78 Input Scaling Resistor Values.
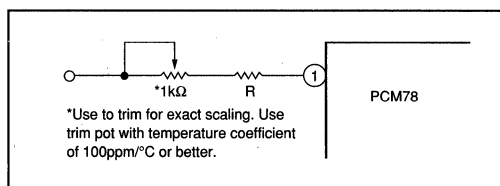
FIGURE 14. PCM78 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM78 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the dynamic input impedance that a successive-approximation converter presents to the the outside world because of the changing currents in this circuit during conversion as the converter steps through its approximations.

If the driving circuit output impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM78 as shown in Figure 15.
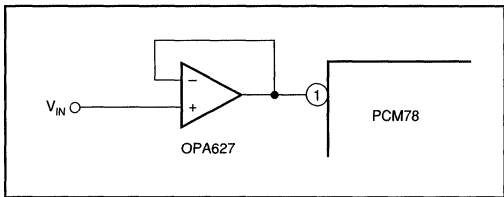
FIGURE 15. Buffer Amplifier for PCM78 Input.

MSB Adjustment

Differential Linearity errors at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. This is important when the signal level is very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small codes changes occurring in the LSB portion of the converter.

The PCM78 is laser trimmed for best performance at the factory without the MSB adjust circuitry installed; if better performance can be obtained it would be by the addition of the MSB adjust circuitry shown in Figure 16.

The best method of adjusting the MSB is by using a real time FFT routine to monitor the levels of odd order harmonics when a sine-wave is being digitized by the PCM78. Adjusting the potentiometer in Figure 16 will allow the user to reduce the magnitude of odd-order harmonics.

An alternate method is to recontruct the data out of the PCM78 through a DAC, and measure THD+N on a conventional distortion analyzer. Adjust the potentiometer for minimum THD+N.
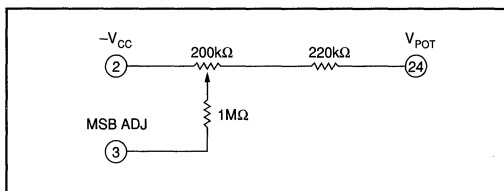
FIGURE 16. MSB Adjust Circuit.

APPLICATIONS INFORMATION

A typical digitization circuit, used on the demonstration board available for the PCM78, is shown in Figure 20. The connections and part values shown in this circuit have been optimized for the best THD+N performance at a 200kHz sample rate.

The PCM78 may be interfaced to many popular digital signal processors, such as the TMS320, DSP56001, and the DSP32. Suggested interface circuits for these processors are shown in Figures 17-19.
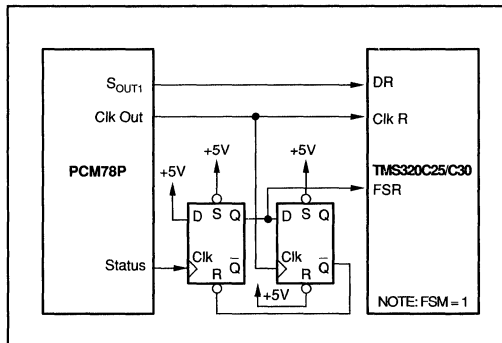
FIGURE 17. PCM78 Interface to TMS320C25/C30 DSP Processors.
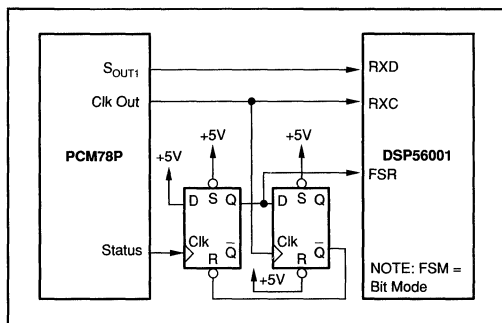
FIGURE 18. PCM78 Interface to Motorola DSP56001 DSP Processor.
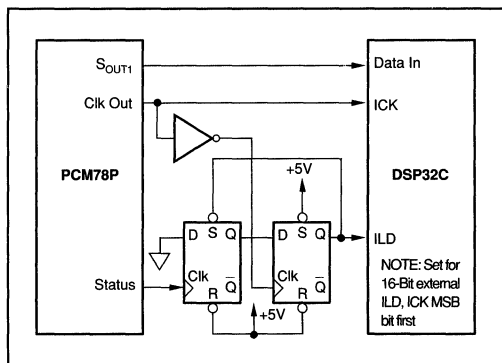
FIGURE 19. PCM78 Interface to AT&T DSP16 & DSP32C Processors.

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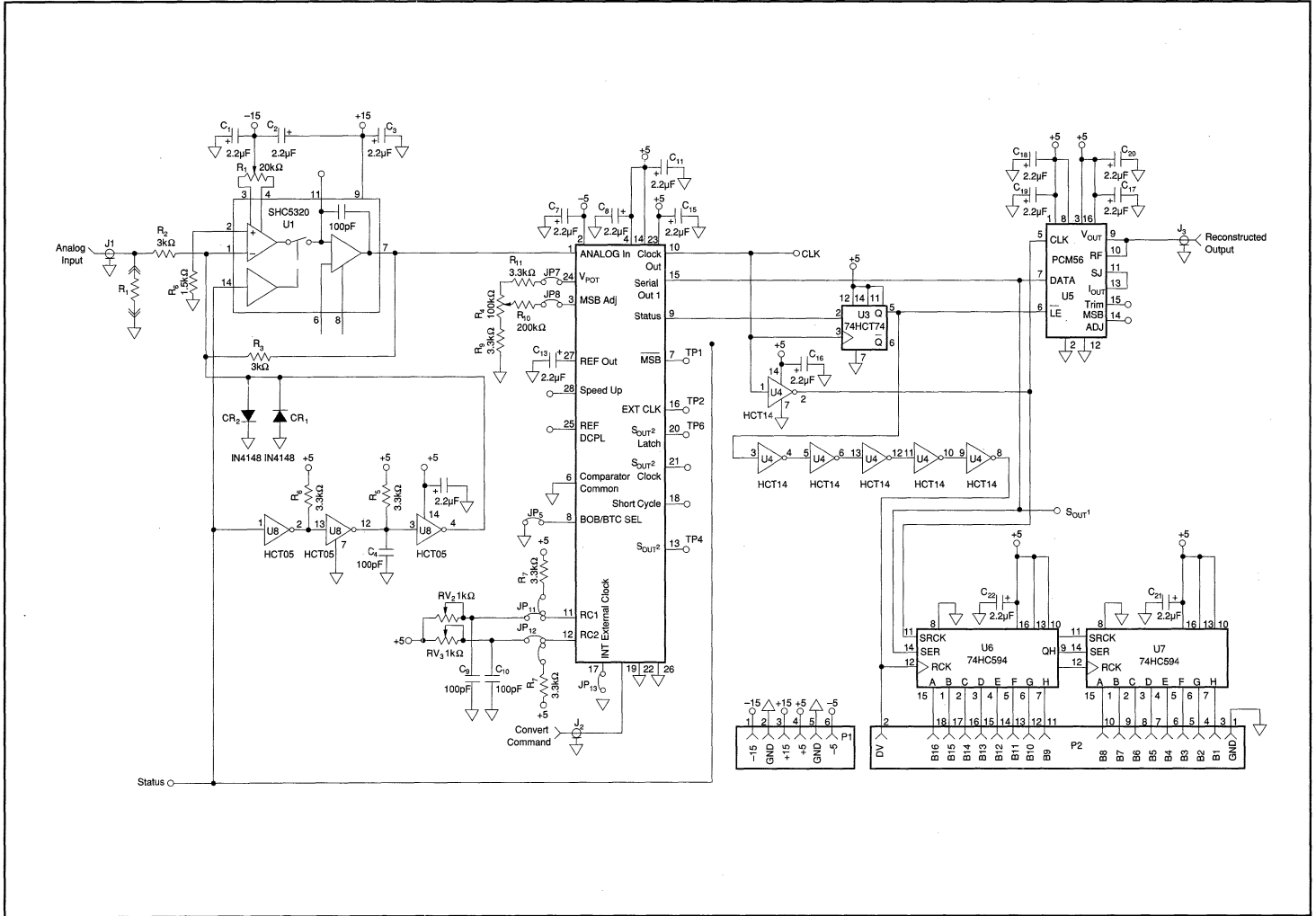
FIGURE 20. Schematic for Demonstration Board (DEM1122).

For Immediate Assistance, Contact Your Local Salesperson

BURR - BROWN®
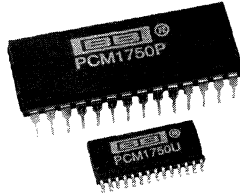
PCM1750P
PCM1750U

DEMO BOARD
AVAILABLE
See Appendix A for
more information.

Dual CMOS 18-Bit Monolithic Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

● **DUAL18-BIT LOW-POWER CMOS AUDIO A/D CONVERTER**

● **FAST 4.5μs MIN CONVERSION TIME INCLUDING S/H**

● **VERY LOW MAX THD+N: –88dB Without External Adjust**

● **COMPLETE WITH INTERNAL REFERENCE AND DUAL S/H FUNCTION**

● **TWO CO-PHASE SAMPLED, ±2.75V AUDIO INPUTS**

● **CAPABLE OF 4X PER CHANNEL OVERSAMPLING RATE**

● **RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX**

● **COMPACT 28-PIN PLASTIC DIP OR SOIC**

DESCRIPTION

The PCM1750 is a low cost, dual 18-bit CMOS analog-to-digital converter optimized for dynamic signal applications. The PCM1750 features true co-phased inputs with an internal sample/hold function for each channel. The PCM1750 also comes complete with an internal reference. Total power dissipation is less than 300mW max using ±5V voltage supplies. Low maximum Total Harmonic Distortion + Noise (–88dB max) is 100% tested. The very fast PCM1750 is capable of 4X x audio bandwidth oversampling rates on both input channels simultaneously, providing greater freedom to designers in selecting input anti-aliasing filters.

PCM1750 outputs serial data in a format that is compatible with many digital filter chips and comes packaged in a space saving 28-pin plastic DIP or SOIC.

PCM1750

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DIGITAL AUDIO PRODUCTS—A/D

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SPECIFICATIONS

ELECTRICAL

At 25°C, and ±V$_A$ = ±5.0V; +V$_D$ = +5.0V, unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

| PARAMETER	CONDITIONS	PCM1750P, U MIN	PCM1750P, U TYP	PCM1750P, U MAX	UNITS
RESOLUTION		18			Bits
DYNAMIC RANGE	THD + N at –60dB Referred to Full Scale	+88	+90		dB
ANALOG INPUT					
Input Range			±2.75		V
Input Capacitance			20		pF
Aperture Delay			10		ns
Aperture Uncertainty (Jitter)			50		ps$_{rms}$
Full Power Input Bandwidth			500		kHz
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS Compatible		
Logic Level: V$_{IH}$	I$_{IH}$ = ±5µA	+3.5		+V$_D$ + 0.3	V
V$_{IL}$	I$_{IL}$ = ±5µA	–0.3		+1.5	V
V$_{OH}$	I$_{SOURCE}$ = 1.0mA	+2.7	+4.7		V
V$_{OL}$	I$_{SINK}$ = 3.2mA		+0.2	+0.4	V
Output Data Format			Serial, MSB First, BTC[1]		
Convert Command			Positive Edge		
Convert Command Pulse Width			81		ns
Conversion Time	Throughput Including Sample/Hold[2]	4.5	5.2	20.8	µs
DYNAMIC CHARACTERISTICS (20Hz to 24kHz; 4X data decimated to 1X)					
Signal-to-Noise Ratio[3]	fs = 192kHz[4]; f$_{IN}$ = 1kHz (0dB)[5]	+88	+90		dB[6]
Total Harmonic Distortion + N[7]	Without External Adjustments				
f$_{IN}$ = 1kHz (0dB)	fs = 192kHz		–90	–88	dB
f$_{IN}$ = 1kHz (–20dB)	fs = 192kHz		–70	–68	dB
f$_{IN}$ = 1kHz (–60dB)	fs = 192kHz		–30	–28	dB
Channel Separation	fs = 192kHz; f$_{IN}$ = 1kHz (0dB) and 0V	+96	+108		dB
ACCURACY					
Gain Error			±2	±5	%
Gain Mismatch	Channel to Channel		±0.5	±2.0	%
BPZ (Bipolar Zero) Error[8]			±2		mV
BPZ Error Mismatch	Channel to Channel		±3		mV
BPZ Differential Linearity Error[9]			±0.002		% of FSR[10]
Linearity Error			±0.003		% of FSR
Warm-up Time			1		ms
DRIFT (With Internal Reference)					
Gain	0°C to 70°C		±50		ppm/°C
Bipolar Zero	0°C to 70°C		±10		ppm of FSR/°C
DRIFT (Exclusive of Internal Reference)					
Gain	0°C to 70°C		±10		ppm/°C
Bipolar Zero	0°C to 70°C		±3		ppm of FSR/°C
REFERENCE					
V$_{REF}$ Output (Pins 19, 24):					
Voltage			+2.75		V
Current			±100		µA
Impedance			0.2		Ω
Accuracy			±25		mV
Drift	0°C to 70°C		±50		ppm/°C
V$_{REF}$ Input (Pins 18, P25):					
Impedance[11]			363 || 120		Ω || pF
POWER SUPPLY REJECTION	% of V$_{IN}$ / % of V$_{SUPPLY}$ [12]		0.03		% / %
POWER SUPPLY REQUIREMENTS					
±V$_A$ Supply Voltage Range		±4.75	±5.00	±5.25	V
+V$_D$ Supply Voltage Range		+4.75	+5.00	+5.25	V
+I$_A$; +I$_D$ Combined Supply Current	+V$_A$; +V$_D$ = +5.0V		+28		mA
–I$_A$ Supply Current	–V$_A$ = –5.0V		–13		mA
Power Dissipation	±V$_A$ = ±5.0V; +V$_D$ = +5.0V		210	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) The PCM1750 is tested and guaranteed at 5.2µs, however it will operate at 4.5µs. The dynamic performance is not guaranteed or tested at this conversion rate. (3) Ratio of Signal$_{RMS}$ / (Distortion$_{RMS}$ + Noise$_{RMS}$). (4) A/D converter sample frequency (4 x 48kHz; 4X oversampling per channel). (5) A/D converter input frequency (signal level). (6) Referred to input signal level. (7) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (8) Externally adjustable to zero error. (9) Differential non-linearity error at bipolar major carry input code. Externally adjustable to zero. (10) Full scale range (5.50V). (11) Refer to equivalent circuit in Figure 1. (12) Worst case operating condition. Refer to typical performance curves.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply Voltage	$-V_A$
2	+5V Analog Supply Voltage	$+V_A$
3	Serial Output (Left Channel)	SOUTL
4	External Clock Input	CLK
5	+5V Analog Supply Voltage	$+V_A$
6	+5V Digital Voltage Supply	$+V_D$
7	+5V Digital Voltage Supply	$+V_D$
8	Digital Common Connection	DCOM
9	Analog Common Connection	ACOM
10	Digital Common Connection	DCOM
11	Convert Command Input	CONVERT
12	Serial Output (Right Channel)	SOUTR
13	+5V Analog Supply Voltage	$+V_A$
14	–5V Analog Supply Voltage	$-V_A$
15	Offset Adjust (Right Channel)	OFF_{ADJR}
16	MSB Adjust (Right Channel)	MSB_{ADJR}
17	Analog Voltage Input (Right Channel; ±2.75V)	V_{INR}
18	Reference Voltage Input (Right Channel)	$VREF_{INR}$
19	Reference Voltage Output (Right Channel)	$VREF_{OUTR}$
20	Analog Common Connection	ACOM
21	Reference Voltage Decouple	$VREF_{CAP}$
22	Reference Common Connection	RCOM
23	Analog Common Connection	ACOM
24	Reference Voltage Output (Left Channel)	$VREF_{OUTL}$
25	Reference Voltage Input (Left Channel)	$VREF_{INL}$
26	Analog Voltage Input (Left Channel; ±2.75V)	V_{INL}
27	MSB Adjust (Left Channel)	MSB_{ADJL}
28	Offset Adjust (Left Channel)	OFF_{ADJL}

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage (V_{IN}) .... $-V_A$ –0.3V to $+V_A$ + 0.3V
$+V_A$; $+V_D$ to ACOM/DCOM .... 0 to +7V
$-V_A$ to ACOM/DCOM .... 0 to –7V
$-V_A$ to $+V_A$; $+V_D$ .... 0 to +14V
ACOM to DCOM .... ±1V
Digital Inputs (pins 4, 11) to DCOM .... –0.3V to $+V_D$ + 0.3V
Power Dissipation 400mW
Lead Temperature, (soldering 10s) .... +300°C
Max Junction Temperature .... 165°C
Thermal Resistance, θ_{JA}: Plastic DIP .... 80°C/W
Thermal Resistance, θ_{JA}: Plastic SOIC .... 100°C/W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1750P	28-Pin Plastic DIP	215
PCM1750U	28-Pin Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE
PCM1750P	28-Pin Plastic DIP
PCM1750U	28-Pin Plastic SOIC

TYPICAL PERFORMANCE CURVES

At 25°C, and $\pm V_A$ = ±5.0V; $+V_D$ = +5V, unless otherwise noted. Where relevant, specifications apply to both left and right input output channels.

THD+N vs FREQUENCY
(With 4X Digital Filter)

THD+N vs FREQUENCY
(Without 4X Digital Filter)

PCM1750

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DIGITAL AUDIO PRODUCTS—A/D

TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, and ±V$_A$ = ±5.0V; +V$_D$ = +5.0V, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

THD vs FREQUENCY
(With 4X Digital Filter)
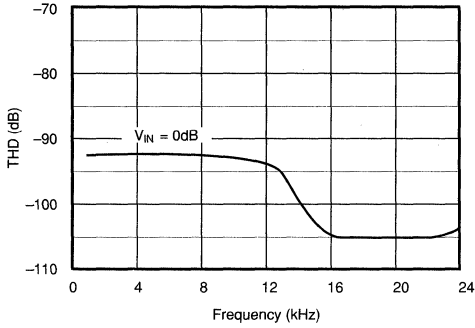
THD vs FREQUENCY
(Without 4X Digital Filter)
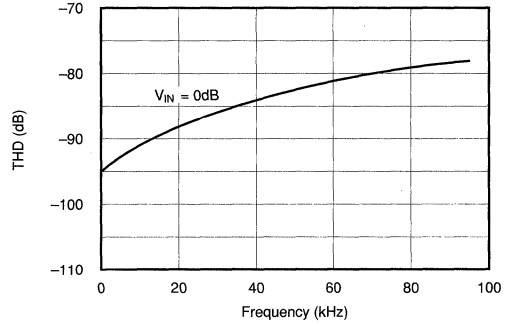
PSR vs FREQUENCY
(−5V SUPPLY)
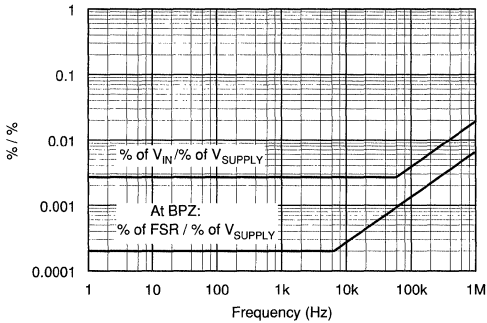
PSR vs FREQUENCY
(+5V SUPPLIES)
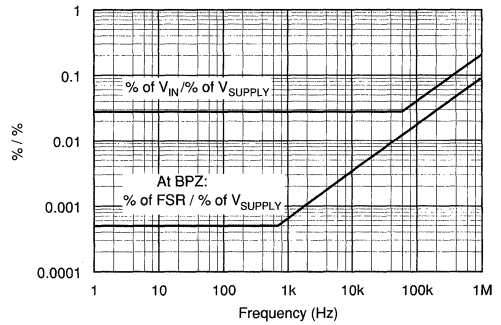
V$_{REF}$ vs TEMPERATURE
(V$_{REF}$ Outputs)
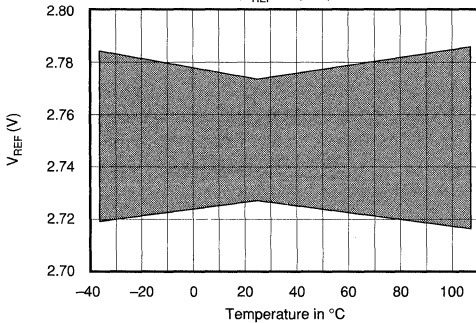
FFT 850Hz (24kHz BW; 2048 POINTS)
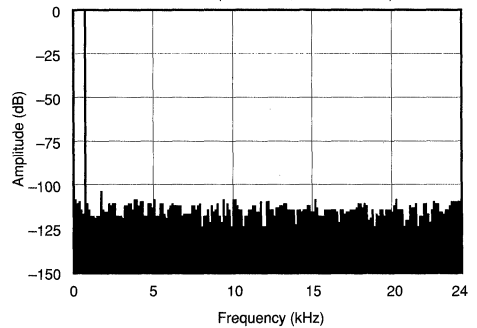
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, and $\pm V_A$; $+V_D = \pm 5V$, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

FFT 20kHz (24kHz BW; 2048 POINTS)

FFT 17kHz and 21kHz (24kHz BW; 16384 POINTS)

FFT 3.7kHz (96kHz BW; 2048 POINTS)

FFT 52kHz (96kHz BW; 2048 POINTS)

FFT 92kHz (96kHz BW; 2048 POINTS)

FFT 88kHz and 92kHz (96kHz BW; 16384 POINTS)

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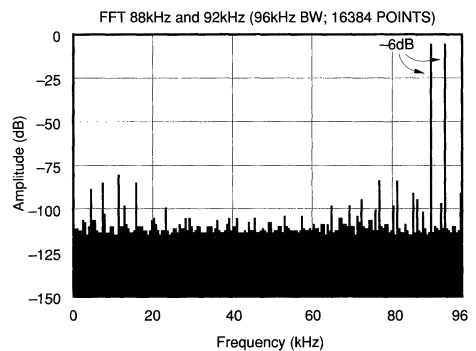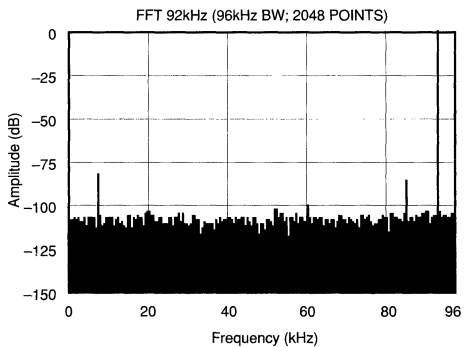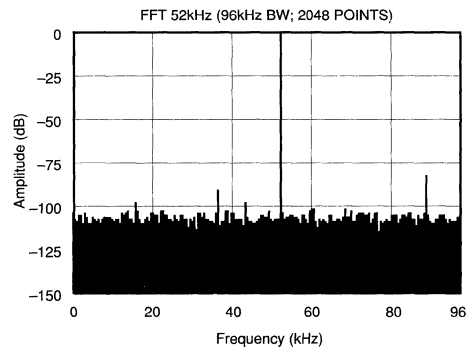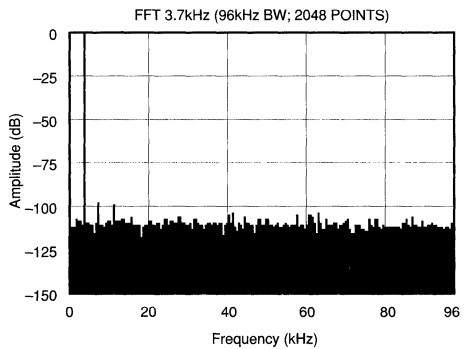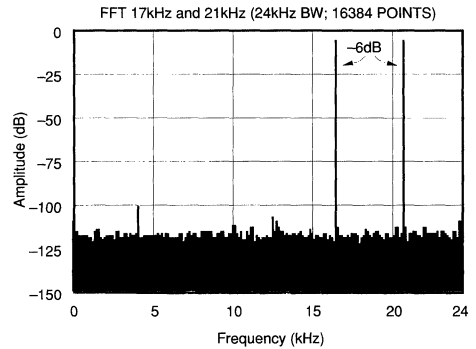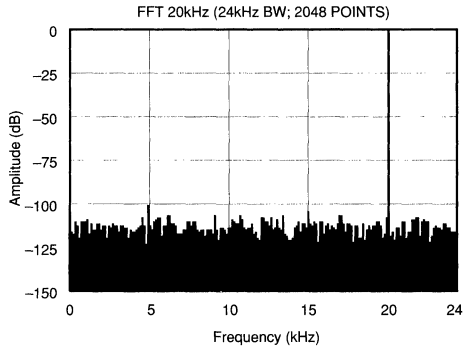
DIGITAL AUDIO PRODUCTS—A/D

THEORY OF OPERATION

OVERVIEW

The PCM1750 is a dual 18-bit successive approximation CMOS analog-to-digital converter with serial data outputs designed especially for digital audio and similar applications. The single-chip converter is fabricated on a 3μ P-well CMOS process which includes poly-poly capacitors, laser-trimmable nichrome resistors, and two layers of interconnect metal. The dual converter employs a switched capacitor architecture which provides separate, simultaneous S/H (sample/hold) functions for each input channel. The separate S/H for each channel results in a desired feature called

co-phase sampling which means that both S/H circuits are switched at the same time into the HOLD mode to capture their respective input signals simultaneously. This eliminates phasing errors produced by alternative architecture ADCs which do not sample the two input channels at the same time.

Switched binary-weighted poly-poly capacitors are used in CDAC (capacitive digital-to-analog converter) configurations to form the successive approximation converter sec-
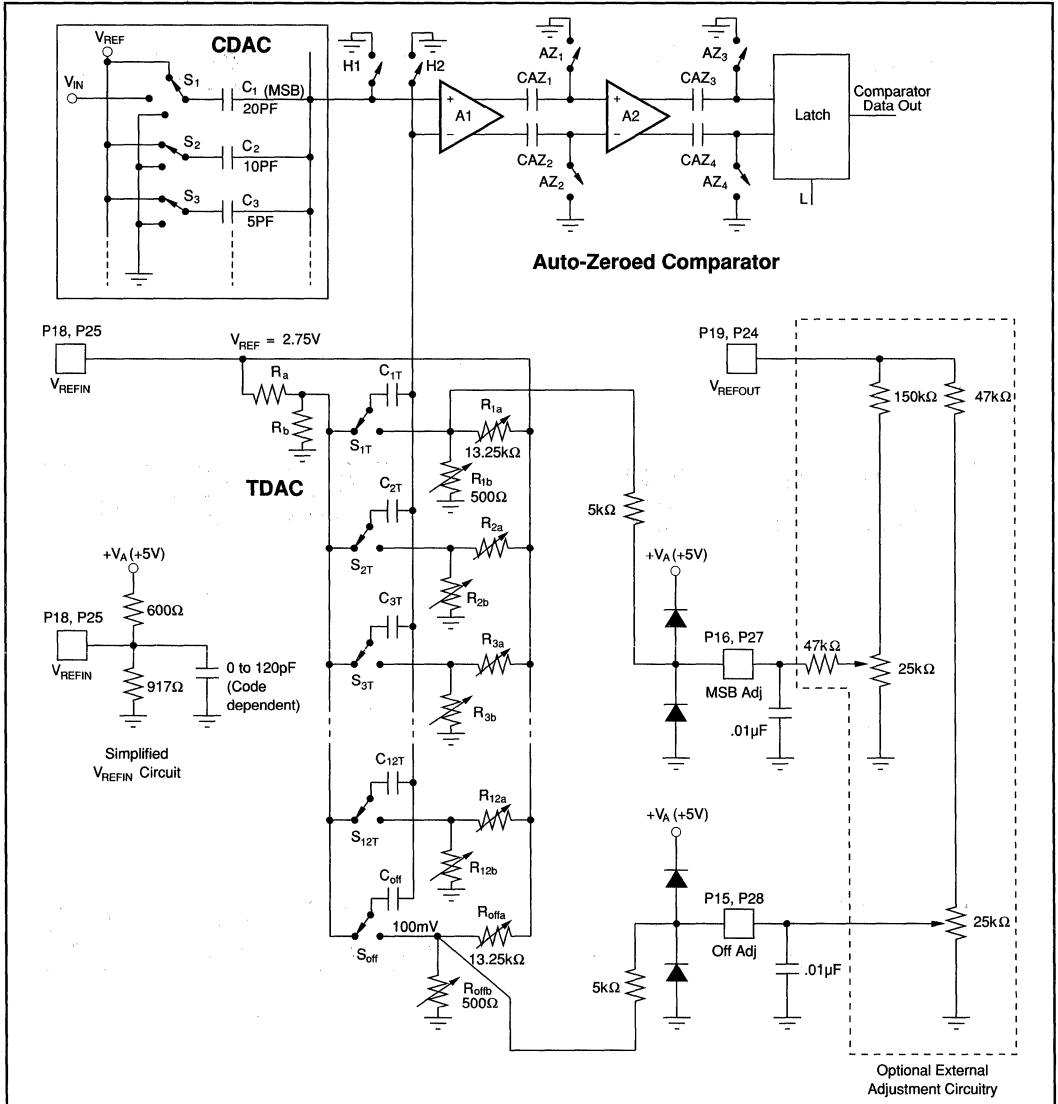
FIGURE 1. PCM1750 Simplified Circuit Diagram.

tions of the PCM1750. Two other switched-capacitor TDACs (trim-DACs, which employ laser-trimmed nichrome resistors) are also used to provide small correction voltages to the latching comparators. These small correction voltages compensate for ratio matching errors of the binary-weighted capacitors in the CDAC. The comparators contain autozeroed preamplifier stages ahead of the latching amplifier stage to produce a one bit, serial data stream that controls the successive approximation algorithm for each channel of the PCM1750.

To simplify user application, the PCM1750 includes an internal band-gap reference with fast settling buffer amplifiers to drive the CDACs. The dual converters operate synchronously (to minimize digital noise conversion errors) using an external system clock (normally at 1X, 2X or 4X the standard 48kHz audio sampling rate). By operating at a 2X or 4X oversampling rate the roll-off requirement for the input anti-aliasing filters is relaxed. For example, 1X systems typically use a 9 to 11 pole LPF (low pass filter) whereas a 4X system can use a 6th (or smaller) order filter when an appropriate digital filter such as the DF1750 is used in conjunction with the sampling system. Oversampling also has the added benefit of improved signal to noise ratio and total harmonic distortion. Two serial outputs, one for each

input channel, provide binary-two's-complement coded output to an optional external digital decimation filter when over sampling operation is desired. The use of the optional companion digital filter, the DF1750, is described later in the installation and application sections of this product data sheet. A separate product data sheet is also available for the Burr-Brown DF1750 giving all the specifications and performance diagrams associated with this digital filter.

SAMPLE (TRACKING) MODE

After each conversion, the dual ADC returns to the SAMPLE mode in order to track the input signals. The switches shown in the simplified circuit diagram of Figure 1 will then be in the following states: S1 connects V_{IN} to C1 ; S2 to S18 connect C2 to C18 to V_{REF}; H1 and H2 connect the top plates of the capacitor arrays to analog common; and the latching comparator is switched into its auto-zero mode by closing AZ1 to AZ4. Notice that C1 serves two purposes: it samples and stores the input signal V_{IN} and it is the MSB of the CDAC. Storing V_{REF} on C2 to C18 creates a bipolar offset, enabling V_{IN} to cover a span from $-V_{REF}$ to $+V_{REF}$.

The 1/f noise as well as the DC input offset voltage of the comparator are removed by an autozeroing cycle which
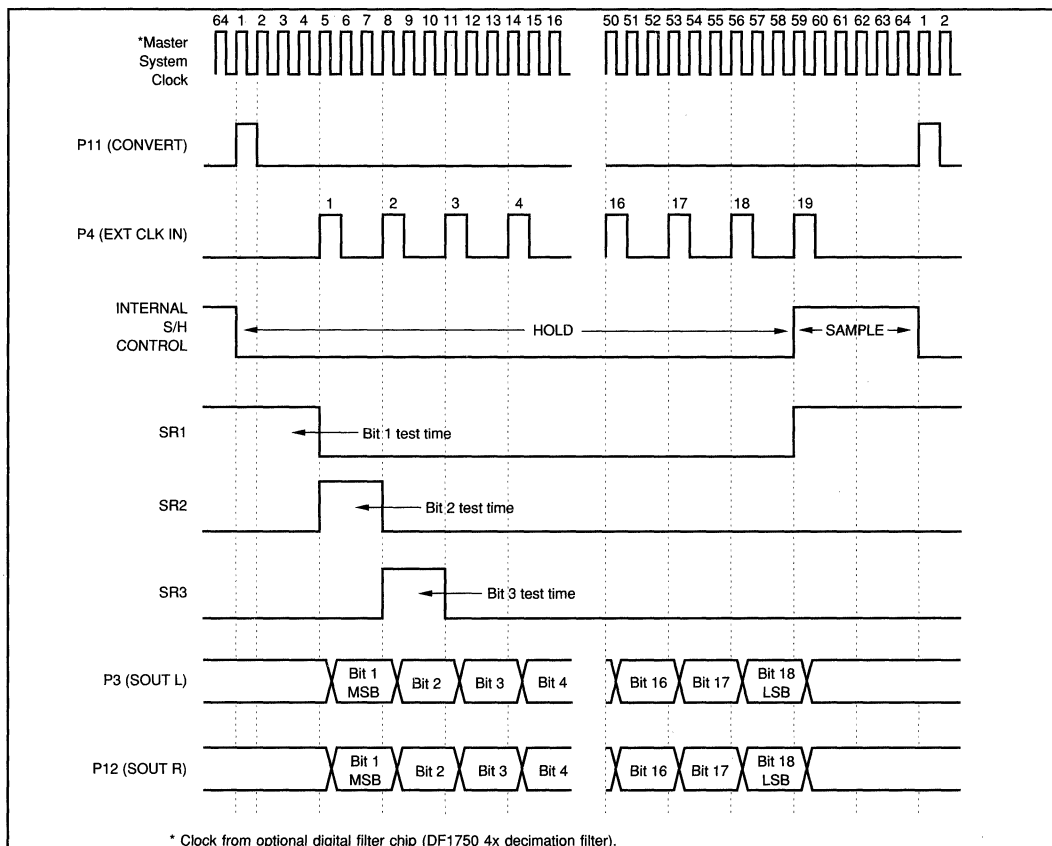
FIGURE 2. PCM1750 Input/Output Timing Diagram.

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DIGITAL AUDIO PRODUCTS—A/D

occurs during the SAMPLE period (see the timing diagram shown in Figure 2). These errors are stored on the AC coupling capacitors (CAZ1 to CAZ4, shown in Figure 1) between the gain stages. During the SAMPLE period the inputs to gain stages A1 and A2 and the latch are grounded by switches H1, H2, and AZ1 to AZ4. Capacitors CAZ1 and CAZ2 track the amplified offset voltage of gain stage A1 and capacitors CAZ3 and CAZ4 do the same for A2. At the beginning of a conversion cycle, the autozeroing switches open and the instantaneous amplified value of both the DC offset voltage and the low-frequency flicker noise is stored on the coupling capacitors to produce zero comparator offset during a conversion cycle.

SUCCESSIVE APPROXIMATION CONVERSION PROCESS

The timing diagram in Figure 2 illustrates the successive approximation routine of the PCM1750. Control signals CONVERT and CLK are derived from a master system clock which comes from a $256f_S$ (256 X the base sampling frequency of 48kHz) clock used by the optional digital filter. There are 64 clocks shown in the timing diagram because the PCM1750 is shown operating at 4 times the standard 48kHz sample rate (192kHz).

Several events occur on the rising edge of the CONVERT command. Switches AZ1 to AZ4, H1 and H2 open and switch S1 reconnects the MSB capacitor, C1, from V_{IN} to

analog common (see Figure 1). This terminates the comparator auto-zero cycle and simultaneously switches (cophase sampling) both converters from tracking their respective input signals into the HOLD mode, thus capturing the instantaneous value of V_{IN} (with a small delay specified as the aperture time).

At the start of a conversion cycle when S1 is switched to analog common, the sampled input signal V_{IN} will appear at the comparator input as $-V_{IN}/2$ due to the 2-to-1 capacitive divider action of Cl = C2 + C3 + ... C18. In a somewhat similar manner, V_{REF} is transferred to the comparator input as $-V_{REF}/2$ to create a bipolar offset.

The 19-bit shift register, shown in Figure 4, controls testing of the bits of the dual ADCs beginning with bit-1 (MSB) and proceeding one bit at a time to bit-18 (LSB), leaving ON those bits that don't cause the cumulative value of the CDAC to exceed the original input value and leaving OFF those bits that do. Since the bits of both channels are tested together, only one shift register is required to control both ranks of 18 data latches.

For example, the testing of bit-2 proceeds in the following manner. The positive pulse from the second shift register element SR2, (see Figure 2 and 4) is applied to the bit-2 data latch and NOR gate. The NOR gate in turn drives S2 and switches bit-2 at the beginning of the bit-2 test interval. Note that the bit interval must be long enough to allow both the comparator input to settle and the comparator to respond. On

PARAMETER		DESCRIPTION	MIN	NOMINAL	MAX	UNITS
T1	(1 x TREF)	Convert Command High	24	33	55	% of T4
T2	(6 x TREF)	S/H Acquisition Time	420	486		ns
T3	(4 x TREF)	Convert to Clock time	281	326	1302	ns
T4	(3 x TREF)	Master Clock Input	211	244	977	ns
T5	(1 x TREF)	Clock High	24	33	55	% of T4
T6	(2 x TREF)	Clock Low	45	67	76	% of T4
T7		Data Hold Time	10			ns
T8		Data Setup Time			100	ns
T9		Data Valid Time	120	154	1212	ns
TCONV	(64 x TREF)	Conversion Throughput Time	4.5	5.2	20.8	µs
TREF	(Sample Rate /64)	Ext Digital Filter Clock	70	81	326	ns

Note: The nominal timing shown in this diagram is all done automatically by the DF1750 digital filter. Only the optional digital filter clock is required when the DF1750 is used.

FIGURE 3. PCM1750 Setup and Hold Timing Diagram.

the next rising edge of CLKIN, at the end of the test interval, the comparator latch is strobed, providing a feedback logic level which tells the second data latch if bit-2 should be kept or rejected. This logic level is stored in the data latch and is passed on to switch S2 via the NOR gate on the falling edge of the pulse from SR2. This decision to keep or reject bit-2 moves the comparator input closer to a null condition, namely, zero potential. This sequential process continues for bit-3 through bit-18 and nulls the comparator inputs to within a value limited by the total system noise and the resolution/speed of the comparator.

Notice from the timing diagram in Figure 2 that the successive approximation algorithm operates synchronously with an external clock to minimize digitally-coupled switching noise from corrupting either the sample-to-hold operation or the critical comparator bit decisions. The two serial output data streams are derived synchronously from the respective latched comparator outputs and are available after a delay of one CLKIN cycle as illustrated in Figure 2. The serial output driver cells are TTL and CMOS compatible.

DIFFERENTIAL LINEARITY CALIBRATION

To understand the calibration of the PCM1750 it is necessary to discuss some of the characteristics of poly-poly capacitors. Poly capacitors are known to have equal or better stability and matching properties when compared to other precision components such as thin film resistors. On a well

controlled process, ratio matching is typically 0.1%—a very respectable number for an untrimmed component. Even more impressive is their ratio tracking versus temperature of approximately 0.1ppm/°C.

Achieving DLE (differential linearity error) of less than 1/2 LSB at the 16-bit level requires ratio matching of the more significant bits to about 0.001%. Since the untrimmed ratio matching of poly capacitors is about two orders of magnitude larger than this requirement, a one-time factory calibration of the upper bits is required as described in the next section. Next, consider the effect of temperature due to the ratio tracking of 0.1ppm/°C. Over a 50°C span, DLE will change less than 1LSB at 18-bits; therefore, recalibration at temperature extremes is not necessary. Because of this excellent stability versus temperature (and versus time, also), the one-time factory calibration to correct initial DLE is more than satisfactory in meeting the accuracy requirements of the PCM1750.

TDAC OPERATION

Operation of the TDAC (trim DAC), which is laser trimmed at the wafer level, is described using bit-1 as an example. Switch S1T (see Figure 1) operates between two voltage levels—a reference level set by voltage divider Ra, Rb and a laser trimmable level set by R1a, R1b. The differences of these two levels is coupled by capacitor C1T to the minus input of the comparator to generate a correction voltage for
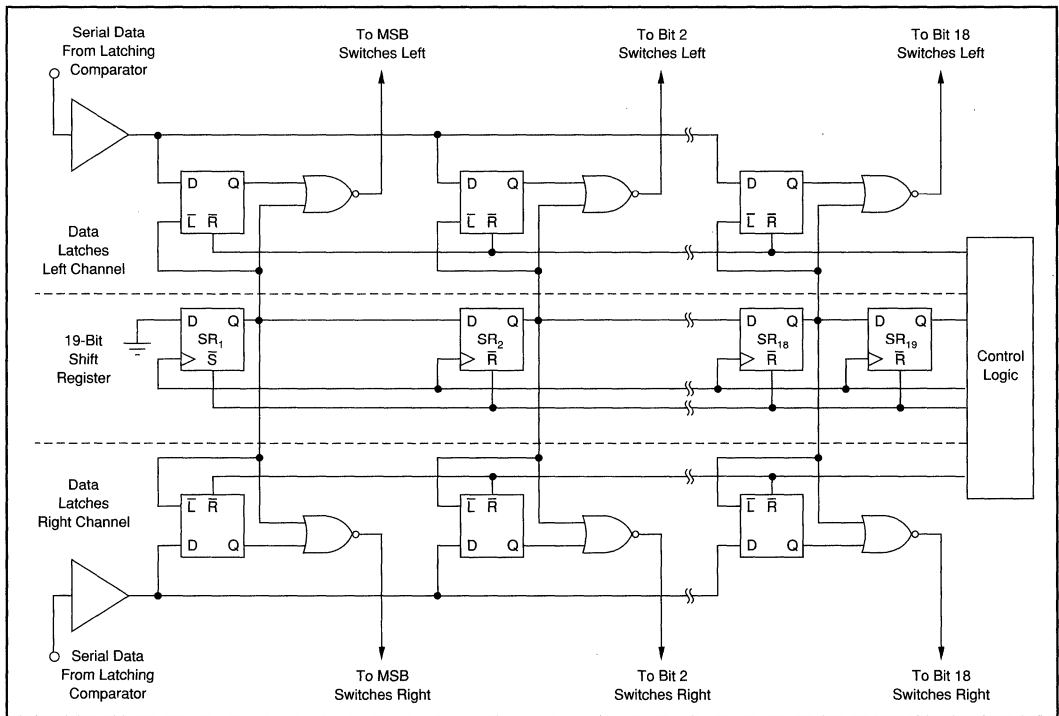
FIGURE 4. PCM1750 Successive Approximation Logic Diagram.

bit-1. The switches of the CDAC and the switches of the TDAC operate concurrently with each other, that is, when a decision is made to keep or reject bit-1, the same decision is made for the correction voltage for bit-1. Even though the ratio stability of the nichrome resistors used in the TDAC may not be as good as the poly capacitors, it is inconsequential because the correction voltage of each bit has a limited range of adjustment.

The DLE at the major carry (a code change from 111...111 to 000...000; in binary two's complement coding) is typically ±1/2 LSB at the 16-bit level, which is sufficient to provide 90dB SNR and –30dB low level distortion (–60dB input). For applications requiring less DLE at the major carry, a pin is provided for each channel to make an external MSB adjustment.

DISCUSSION OF SPECIFICATIONS

RESOLUTION AND DYNAMIC RANGE

The theoretical resolution of the PCM1750 is 18-bits. The maximum possible number of output codes or counts at 18-bits is 262,144 or 108dB (calculated by raising 2 to the 18th power). The relative accuracy of any A/D converter, however, is more a function of it's absolute linearity and signal-to-noise ratio than how many bits of resolution it has. These more pertinent specifications are described later in this section.

Dynamic range, as it is usually defined for digital audio converters, is the measure of THD + N at an effective input signal level of –60dB referred to 0dB. For the PCM1750 this value is typically 90dB and a minimum of 88dB (for audio bandwidth = 20Hz to 24kHz, THD + N at –60db = –30 db typ, –28dB max; f_{IN} = 1kHz and f_S = 192kHz). Resolution is also commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels.

ANALOG INPUT RANGE

The analog input range for the PCM1750 is a bipolar ±2.75V (nominal). Table I gives the precise input/output and voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format. It should be noted that the computed voltage input levels represent center values (the midpoint between code transitions). Output coding is in binary two's complement.

DIGITAL OUTPUT	ANALOG INPUT	VOLTAGE INPUT
262144 LSBs	Full Scale Range	5.50000000V
1 LSB	Minimum Step Size	20.98083496μV
1FFFF$_{HEX}$	+Full Scale	+2.74997902V
00000$_{HEX}$	Bipolar Zero	0.00000000V
3FFFF$_{HEX}$	Bipolar Zero –1LSB	–0.00002098V
20000$_{HEX}$	–Full Scale	–2.75000000V

TABLE I. Analog Input to Digital Output Relationships.

* Gain drift (mostly due to reference drift) rotates the transfer function around the bipolar zero code (00000$_{HEX}$).

NOTE: As the power supply voltages change (mostly due to the +V supply), the transfer function rotates around BPZ. See the power supply rejection specification in the spec table.
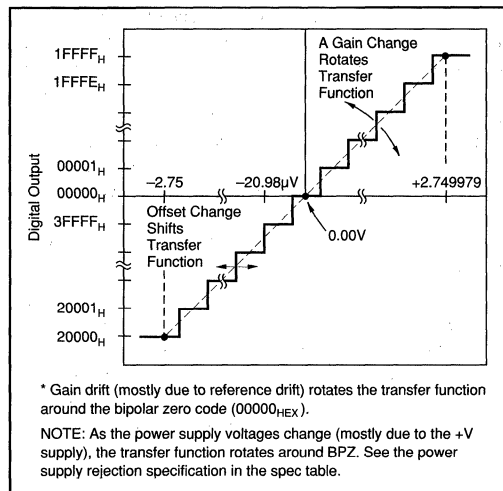
FIGURE 5. Analog Input to Digital Output Diagram.

From Figure 5, the effects of offset and gain errors can be visualized. These errors can change value in response to changes in temperature and/or supply voltage. In addition, gain error (or the full scale range, FSR) changes in direct proportion to the $VREF_{IN}$ voltage value.

SAMPLE AND HOLD PARAMETERS

Aperture Delay and Uncertainty

Aperture delay is the time required to switch from the SAMPLE to HOLD mode. This time is typically 10ns for the PCM1750 and it is constant. Aperture uncertainty (jitter) is the amount of uncertainty associated with the aperture delay. Aperture uncertainty affects the overall accuracy of the converter and is greatest at the maximum input frequency of the converter. The formula for determining the maximum input frequency (f_{MAX}) for a given error contribution due to aperture uncertainty is: $f_{MAX} = (2 \times \pi \times t_{jitter} \times 2^N)^{-1}$ where t_{jitter} is the RMS aperture uncertainty and 2^N is the desired SNR (signal-to-noise ratio) expressed in total number of quantization levels. A 15-bit SNR, therefore, would be expressed as 2^{15} or 32768. Using the typical PCM1750 aperture jitter of 50ps$_{rms}$ and an SNR at the 15-bit level, f_{MAX} = (2 × π × 50ps × 32768)$^{-1}$ or 97.1kHz. This matches very closely with the rated dynamic accuracy of the PCM1750 where THD + N = –88dB max. This means the typical aperture jitter of PCM1750 only becomes a factor when input signals to it exceed 97kHz and/or an SNR greater than 15-bits is desired.

Input Bandwidth

The full power bandwidth of the PCM1750 is that input frequency above which significant distortion is observed (THD+N > 10-bits or –60dB for a full scale input signal). In the data sheet, this number is specified as typically being 500kHz. In wideband operation (when no digital filter is used) the additional full power bandwidth of the PCM1750

can be used to purposely alias a band-limited signal down into the baseband of the converter. This technique is called undersampling and can be used to directly down-convert an intermediate frequency riding on a much higher carrier frequency.

DIGITAL I/O AND TIMING

Input/Output Logic Compatibility

Digital logic on the PCM1750 is CMOS compatible. Digital outputs on the PCM1750 are capable of driving a minimum of two standard TTL input loads.

Digital output coding is in binary two's complement. Table I gives the precise input/output voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format.

Convert Command and External Clock Input

A conversion is initiated on its positive going edge of the convert command. Although the convert command can return low at any time (prior to 50ns before the rising edge of the 19th clock), a typical convert command pulse width of 81ns (as called out in Figure 3) is specified for a 192kHz sample rate (f_s). The reason for a pulse width spec is to reduce problems associated with digital logic feedthrough noise. The return of convert command to a logic low level in the specified time interferes least with the successive approximation process. Also, it should be noted that putting fast logic edges (<5ns) on convert command (P11) and the external clock input (P4) may cause logic feedthrough to the analog stages in the converter and will result in added distortion during the sampling and conversion process. Using the optional DF1750 digital filter provides adequately slow transitions to maintain full specification performance. If necessary, an external RC, on the convert command line may be used to slow fast logic edges.

As with the convert command, the external clock input is positive edge triggered and is not duty-cycle dependent other than to improve digital feedthrough noise immunity. A 50% duty cycle clock can be used instead of 33% if desired. Refer to Figure 3 for recommended timing relationships. Regardless of what clock duty cycle is used, all operations relating to valid data clocking should be synchronized to the rising edge of the clock input.

Although there is a maximum conversion time called out in the specification table, the PCM1750 can have a considerably longer conversion cycle. Droop of the internal capacitors will ulitmately determine what the true maximum conversion time can be. The min/typ/max times shown in Figure 3 are based on minimum sample rate of 48 kHz, a typical of 192kHz, and a maximum of 222kHz. All specifications are tested at 192kHz. The minimum sample rate assumption is based on clock periods that increase as time between convert commands increases. Any sample rate down to near DC can be utilized by observing maximum clock cycle requirements and spacing convert commands to achieve lower sample rates. This means that the time interval T2 shown in Figure 3 does not have a maximum value.

Clock Lockout

Any number of clocks can be given to the PCM1750 beyond the 19 required for normal operation. If a continuous clock is used, all clocks beyond the 19th are gated off by the PCM1750's internal logic until the next positive going edge of the convert command. The converter also goes into the sample (track) mode starting on the positive edge of the 19th clock until the next positive edge of the convert command, regardless of how many additional clocks are offered. The ideal operation of the converter stops the clock input after the 19th during this critical signal acquisition time. This is the timing shown in Figure 3 . The critical timing aspect that must be observed if a clock input other than the recommended is used, is that ample time following the positive edge of convert command proceed the next rising clock edge. If this time is shortened, the most important bit-1 (MSB) decision, which is finalized on the first clock edge after convert command, will be adversely affected. In other words, the clock input cannot have a rising edge during the time interval T3 shown in Figure 3.

SIGNAL-TO-NOISE RATIO

Another specification for A/D converters is signal-to-noise ratio (SNR). For this measurement, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz. An FFT is performed on the digital output and the noise power in the non-harmonic audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

One advantage of using the PCM1750 in this oversampled mode with the optional DF1750 digital decimation filter is that the converter noise is spread over the full 0Hz to 96kHz passband and then suppressed by the digital filter stopband attenuation (from 24kHz to 96kHz). This effectively increases the SNR of the PCM1750 by 6dB when it is used as an audio bandwidth converter. The other advantage is that the need for a higher-order anti-aliasing input filtering is greatly reduced.

THD + N

The key specification for the PCM1750 is total harmonic distortion plus noise (THD + N). In terms of signal measurement, THD + N is the ratio of Distortion$_{RMS}$ + Noise$_{RMS}$ / Signal$_{RMS}$ expressed in dB. For the PCM1750, THD + N is 100% tested at all three specified input levels using the production test setup shown in Figure 6. For this measurement, as with the SNR test, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz (which is 4X the standard digital audio sample rate of 48kHz). An FFT is performed on the digital output and the total power in all audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

For the audio band, the THD + N of the PCM1750 is essentially flat for all frequencies and input signal levels. In the *Typical Performance Curves* THD + N versus Frequency plots are shown at four different input signal levels (with and without a 4X decimation filter): 0dB, –20dB, –40dB, and –60dB.

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DIGITAL AUDIO PRODUCTS—A/D

CHANNEL SEPARATION

To test channel separation a 1kHz signal sampled at 192kHz is placed on one input of the PCM1750 while the other input is held at 0V. An FFT is performed on the idle (0V) channel and the result checked to insure that the 1kHz tone is suppressed by a minimum of 96dB.

GAIN AND OFFSET ERRORS

Initial gain and bipolar offset errors are laser trimmed at the wafer level and 100% final tested to insure compliance with the electrical specifications. Bipolar offset errors can be further reduced to zero by using the optional offset adjustment circuitry shown in the connection diagram (Figure 7). Gain errors can be adjusted by varying V_{REF} to either channel of the converter. This is accomplished by either using an adjustable external reference or by placing buffer amplifiers with adjustable gain between $VREF_{OUT}$ and $VREF_{IN}$ as shown in Figure 8a.

INTEGRAL AND DIFFERENTIAL LINEARITY

DC Linearity Testing

The absolute linearity of the PCM1750 is on the order of 15-bits or more as can be seen from the THD versus Frequency plots in the *Typical Performance Curves*. Not every code in the converter must be 15-bit linear to achieve the specified THD + N performance, but a very high percentage will be that linear. The same observation also applies to differential linearity errors in the PCM1750. Because the PCM1750 is not 100% tested for DC linearity specifications, no minimum or maximum specifications are given for integral or differential linearity errors.

No Missing Codes Operation

A no missing codes specification is not given for the PCM1750 for the same reasons as given above. The PCM1750, however, typically has fewer than 16 codes (less than 0.01%) missing at a 14-bit resolution level. A 100% no missing codes specification cannot be maintained above the 12-bit level, although this has very little impact on overall dynamic performance (THD + N). The few missing codes that do occur at higher resolution levels are at the bit-2 and lower major carry transitions of the converter. There are typically no missing codes (at 14-bits) around the critical bipolar zero operation zone (±1/8 of full scale range around bipolar zero or 0V). The critical bipolar differential linearity error can be reduced from its initial value to zero using the optional MSB adjustment circuitry shown in the connection diagram (Figure 7).

REFERENCE

The gain drift of the PCM1750 is primarily due to the drift associated with the reference. Better drift performance can be achieved using an external reference like the ones explained in the applications section (Figures 8b, 8c). The *Typical Performance Curves* plot of V_{REF} Output versus Temperature shows the full range of operation including initial error and typical gain drift. Pertinent performance data are found in the electrical specification table.

Reference Bypass

Both P18 and P25 ($VREF_{IN}$) should be bypassed with a 10µF to 47µF tantalum capacitor. If there are important system reasons for using the PCM1750 reference externally, the outputs of P19 and P24 must be appropriately buffered, and bypassed (see Figure 8).

POWER SUPPLY REJECTION

Because of the architecture of the PCM1750, power supply rejection varies with input signal size. The spec table value is expressed in the relative terms of percent of V_{IN} per
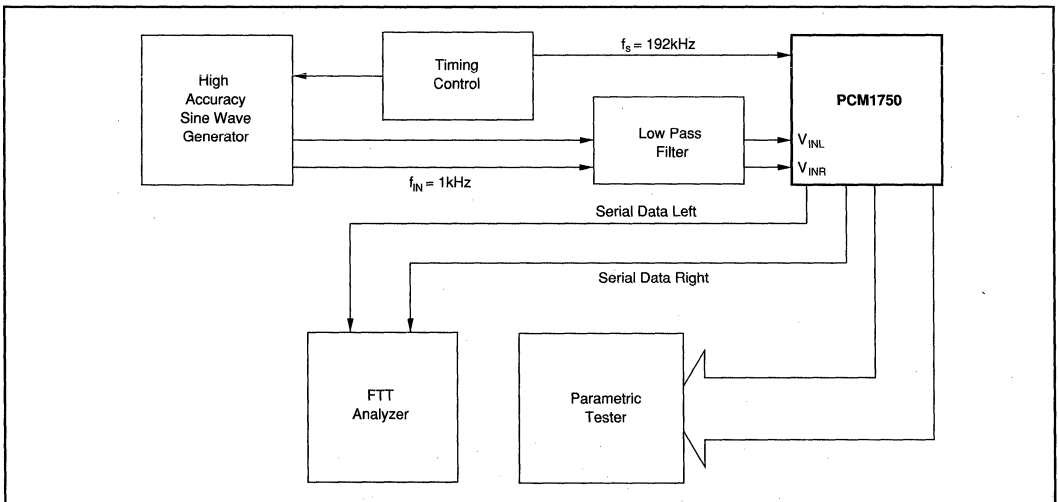
FIGURE 6. PCM1750 Production Test Setup.

percent change of the supply voltage. The PSR versus Frequency plot in the *Typical Performance Curves* show PSR expressed versus an increase in power supply ripple frequency.

PERFORMANCE OVER TEMPERATURE

Specification Temperatures

All critical specifications are tested at 25°C. The drift specification temperature range is from 0°C to +70°C. The PCM1750 will operate over the wider temperature range of –40°C to +85°C.

Gain and Offset Drift

Although the PCM1750 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC drift parameters such as temperature gain and offset drift. The primary cause of drift in the PCM1750 is the bandgap reference. Much lower gain drift can be realized if necessary by using any circuit similar to the external reference circuits shown in Figure 8. Also, refer to the *Typical Performance Curves* of V_{REF} Output versus Temperture.

Dynamic Performance

Dynamic performance is predominated by the absolute linearity of the PCM1750. Because of the excellent ratio tracking versus temperature of poly-poly capacitors, there is virtually no change in dynamic performance of the converter over temperature (primarily THD + N). The dynamic specifications over temperature cannot be guaranteed, however, as they are not 100% tested.

INSTALLATION

ANTI-ALIASING FILTER

To prevent unwanted input signals from being aliased into the passband of the converter, it is necessary to suppress all out of band signals above 1/2 the sampling frequency of the ADC by using a low-pass filter. The requirement for an anti-aliasing filter, however, can be reduced by using oversampling techniques. By raising the sample rate of the converter by a factor of 2 or even 4, the roll off of the anti-aliasing filter can be reduced. In Figure 9, a 6th order, linear-phase, anti-aliasing filter is implemented using low-cost dual audio op amps. This filter will suppress frequencies above 96kHz by 80dB. For many applications a 4th or 2nd order anti-aliasing filter will be adequate when using the PCM1750 in the 4x oversampling mode.
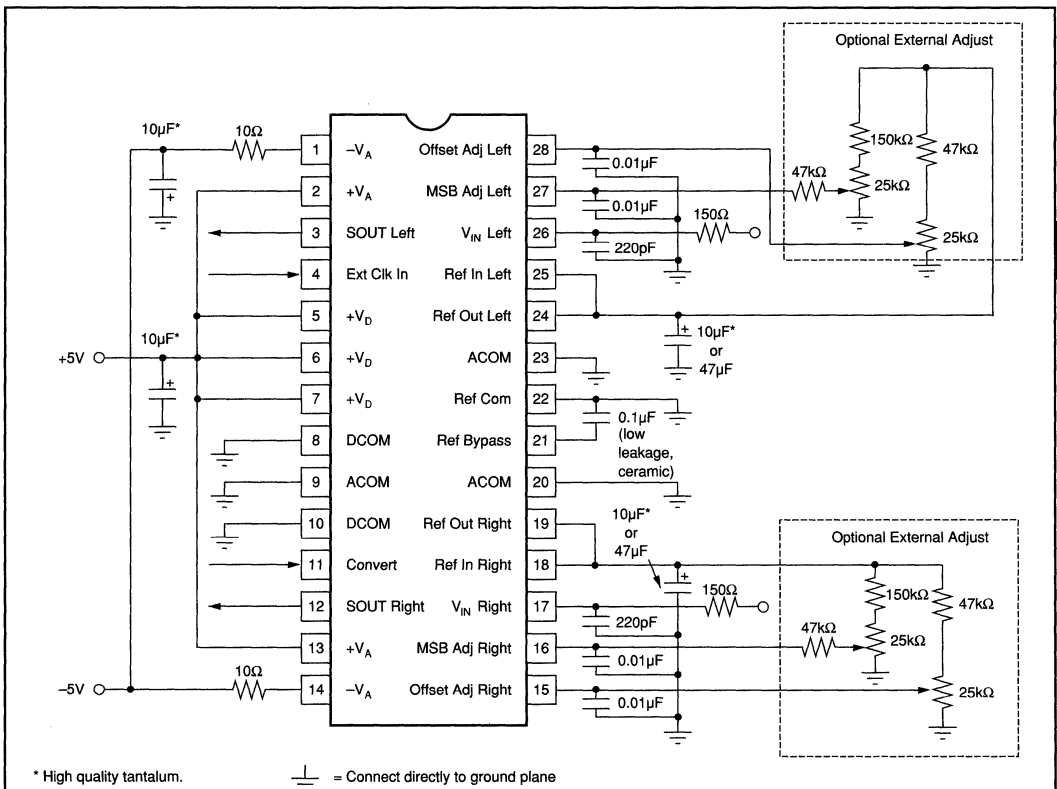
FIGURE 7. PCM1750 Connection Diagram.

INPUT SIGNAL CONDITIONING

RC Input Circuit

Note the 150Ω resistors and 220pF capacitors on each analog input as shown in the connection diagram (Figure 7). This input circuit configuration is required to achieve optimum SNR performance of the PCM1750. Various other component values will yield satisfactory results, but the resistor should never exceed 200Ω.

Buffer Amplifier

To avoid introducing distortion, the PCM1750 input must be driven by a low active impedance source (op amps such as the NE5532, Burr-Brown OPA2604, or equivalent are ideal).

EXTERNAL ADJUSTMENTS

The simplified circuit diagram (see Figure 1) shows one of two complete channels on the PCM1750. The input switched capacitors, trim DAC and comparator are detailed. The trim DAC switches are activated whenever the corresponding bit is chosen during the successive approximation routine. The first 12 bits of the ADC have corresponding trim DAC circuits. The R1a to R12a and R1b to R12b resistors can be laser trimmed at the wafer level if necessary to correct for any nonlinearities. The nominal voltage for the internally generated V_{REF} is 2.75V and it is a relatively low impedance, buffered voltage output. It should be noted that just the act of connecting the optional adjustment circuits will affect the MSB DLEs and bipolar offsets since it is unlikely that the initial potentiometer settings (even if centered) would match the factory trimmed null potentials. If connected, the potentiometers must be properly adjusted.
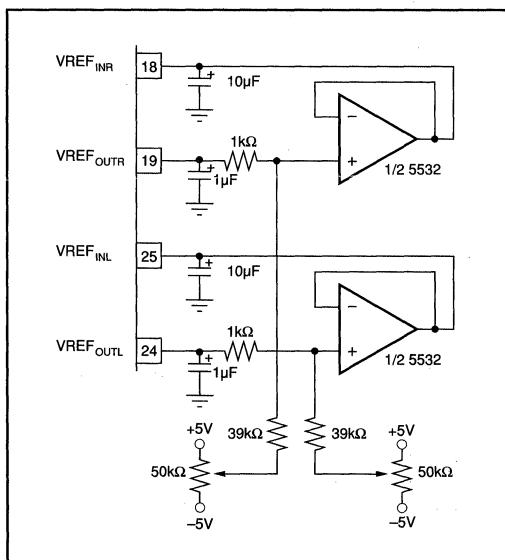
FIGURE 8a. Circuit for External Gain Adjustment Using the Internal Reference.

MSB Adjust

The MSB adjust pin connects to the center of the R1a/R1b resistive divider for bit-1. After laser trimming this point is nominally 100mV. All the MSB and offset adjust pins should be connected to ground using a 0.01µF capacitor, especially if traces to the potentiometers are long. If the adjust pins are not used, they should still be bypassed to ground.

Since there are internal 5kΩ resistors and clamp diodes to both ground and +5V on the MSB and offset adjust pins, there are obvious limits to their range of adjustment. With a nominal internal voltage on these points of +100mV, there will be a greater limitation in making negative adjustments than positive. A negative voltage at either adjustment pin, however, is acceptable up to one diode drop (–0.6V) below ground.

The preferred method of MSB DLE adjustment is to input a small level signal and adjust for minimum THD + N.

Offset Adjust

The offset adjust switch (S_{OFF}) position is controlled by whether the ADC is in the sample or hold mode. Switching from sample to hold effectively allows any charge offsets associated with the sampling process to be eliminated. Grounding the input to the converter as far ahead of the A/D as possible (in front of the anti-aliasing filter for example) and then adjusting the bipolar zero error will remove the offsets associated with the entire sampling system.

LAYOUT CONSIDERATIONS

Power Requirements

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used. Although the PCM1750 positive supplies have separate digital and analog +5V, for most applications the +5V digital supply pins should be connected to the +5V analog supply. If they aren't connected together, a potential latchup condition can occur when the power supplies are not turned on at the same time. If one supply pin is powered and the other is not, the PCM1750 may latch up and draw excessive current. In normal operation, this is not a problem because both $+V_A$ and $+V_D$ should be connected together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "hot" socket exists, care should be taken to power the PCM1750 only after it has been socketed.

All supplies should be bypassed as shown in Figure 7. The bypass capacitors should placed as close to their respective supply pins as possible. Additional .01µF capacitors may be placed in parallel with the larger value capacitors to increase high-frequency rejection, but generally they are not required when high quality tantalums are used. The 0.1µF capacitor between P21 and P22 should be a low leakage type (such as ceramic) and must be put as close to these pins as possible to reduce noise pickup.

The PCM1750 is sensitive to supply voltages outside the absolute maximum ratings shown in the specification tables. Do not exceed –8V on the negative supplies at any time or irreversible damage may occur. Note the 10Ω resistors in series with each –5V supply line (shown in Figure–7) to help protect the part from severe damage if the supplies are over-ranged momentarily.

Grounding Requirements

Because of the high resolution and linearity of the PCM1750, system design problems such as ground path resistance and contact resistance become very important.

The ACOM and DCOM pins are separated internally on the PCM1750. To eliminate unwanted ground loops, all commons (both analog and digital) should be connected to the same low-impedance ground plane. This should be an analog ground plane separate from other high-frequency digital ground planes on the same board. If the analog and digital commons of the PCM1750 are connected to different ground planes, care should be taken to keep them within 0.6V of each other to insure proper operation of the converter.

A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signals should be referenced to the ACOM pins. This will prevent voltage drops in the power supply returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external MSB and offset adjust potentiometers are used, the potentiometers and related resistors should be located as close to the PCM1750 as possible.

Minimizing "Glitches"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. Care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the PCM1750 has an internal sample/hold function, the signal that switches it into the HOLD state (CONVERT going HIGH) is critical, as it would be on any sample/hold amplifier. The CONVERT rising edge should have minimal ringing, especially during the 20ns after it rises.

APPLICATIONS

USING A DIGITAL FILTER

A 4x decimation filter is available for the PCM1750 called the DF1750. It is available in a 28-pin DIP or a 40-pin SOIC package. The use of this filter greatly eases the implementation of the PCM1750 in audio band applications.
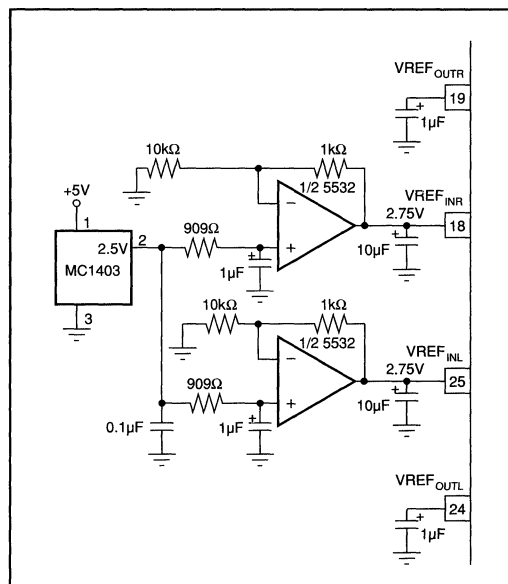
FIGURE 8b. External Reference Circuit Using Standard 2.5V Reference.
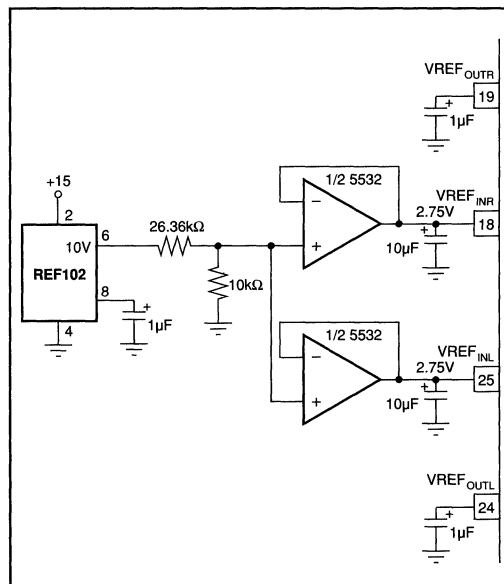
FIGURE 8c. Low Noise, Low Drift External Reference Circuit.

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DIGITAL AUDIO PRODUCTS—A/D

FIGURE 9. Complete Sampling A/D Circuit with Anti-aliasing and Digital Filter, (44.1kHz output data rate).
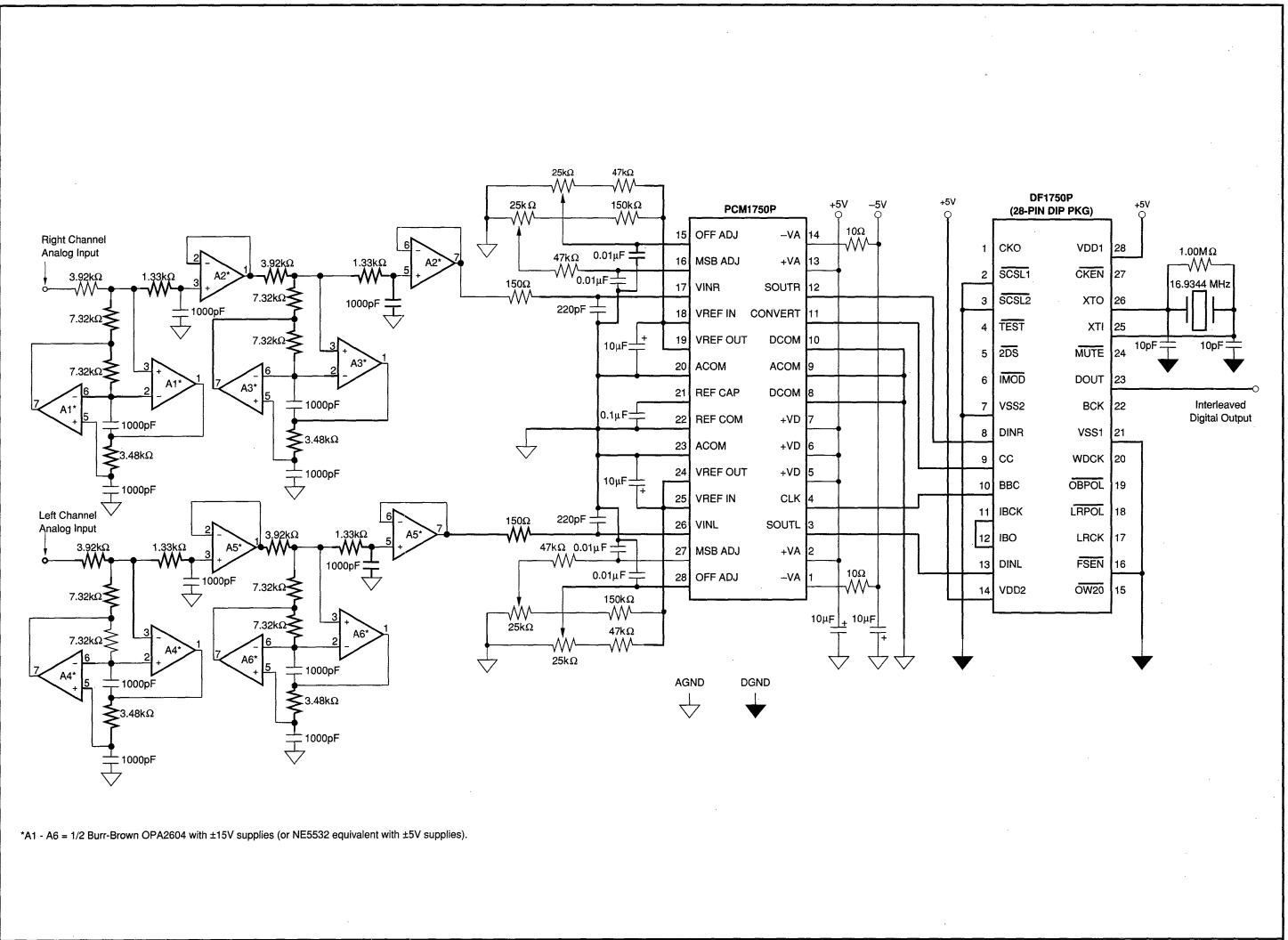
*A1 - A6 = 1/2 Burr-Brown OPA2604 with ±15V supplies (or NE5532 equivalent with ±5V supplies).

USING AN EXTERNAL REFERENCE

Normally $VREF_{OUT}$ is connected directly to $VREF_{IN}$. The typical value for V_{REF} versus Temperature is shown in the *Typical Performance Curves*. If better drift or power supply rejection performance is desired, one of the external reference circuits shown in Figures 8b and 8c can be used. Note that the decoupling capacitors are still connected to $VREF_{IN}$. External gain adjustment is now possible by using the variable output options available on some precision voltage references or by varying the gain on external buffer amplifiers. The range of acceptable external references is from +2.0V to $+V_A$ – 2.0V, with 2.5V types being the most commonly available. Full scale input voltage range will be $\pm VREF_{IN}$ (a +2.5V $VREF_{IN}$ results in a ± 2.5V input range).

If an external reference is used, P19 and P24 must be bypassed with at least 1μF capacitors.

SAMPLING A/D SYSTEM

Figure 9 is a partial schematic of the demonstration fixture for the PCM1750 (orderable by model number DEM1133). It shows the implementation of (1) a 6th order, linear-phase, anti-aliasing filter (22kHz low-pass); (2) the PCM1750P A/D converter; and (3) a 4x digital decimation filter called the DF1750P. Not shown on this schematic, but included on the demo fixture, are latched parallel data outputs with strobe and a serial digital interface format (SPDIF) data transmitter. Also included on the DEM1133 are user breadboard areas for application specific circuit implementation.

CONNECTION TO DSP WITH DIGITAL FILTER

The PCM1750 and DF1750 combination can be connected to the serial ports of most popular DSP processor ICs (such as those made by AT&T, Motorola, TI, and AD) by adding a small amount of external glue logic. Figures 10 and 11 show the timing diagram and schematic for this interface.

To use this interface, the DSP processor IC must be configured for 32 bit word inputs. The glue logic generates a flag bit, as the first bit of the 32 bit word, that signifies either left or right channel data. The flag bit will be low for left channel data and high for right channel data.

The DF1750 can be configured for either 16 or 20 bit data, although only 16 bit data is shown in Figure 10. After the data is transferred into the DSP processor IC, it must be shifted toward the LSB by one bit in order to compensate for a clock delay in the glue logic.
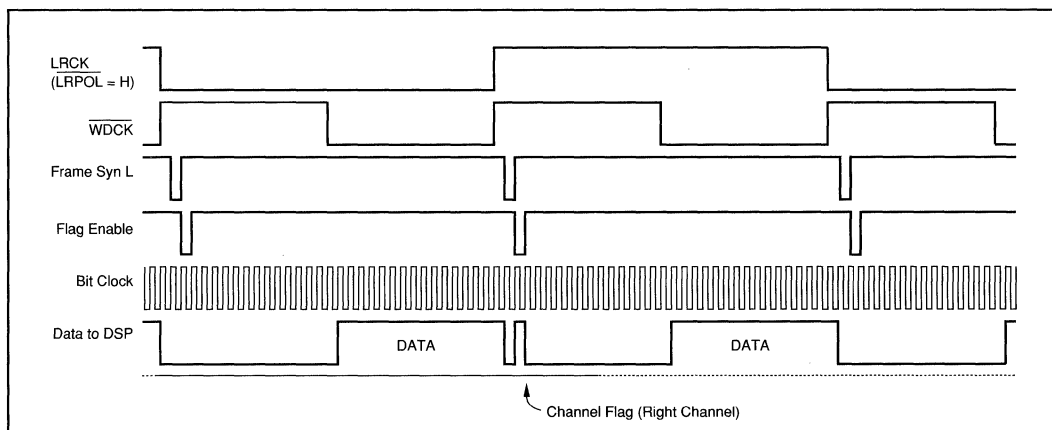
FIGURE 10. PCM1750/DF1750 To DSP IC Timing Diagram.

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DIGITAL AUDIO PRODUCTS—A/D
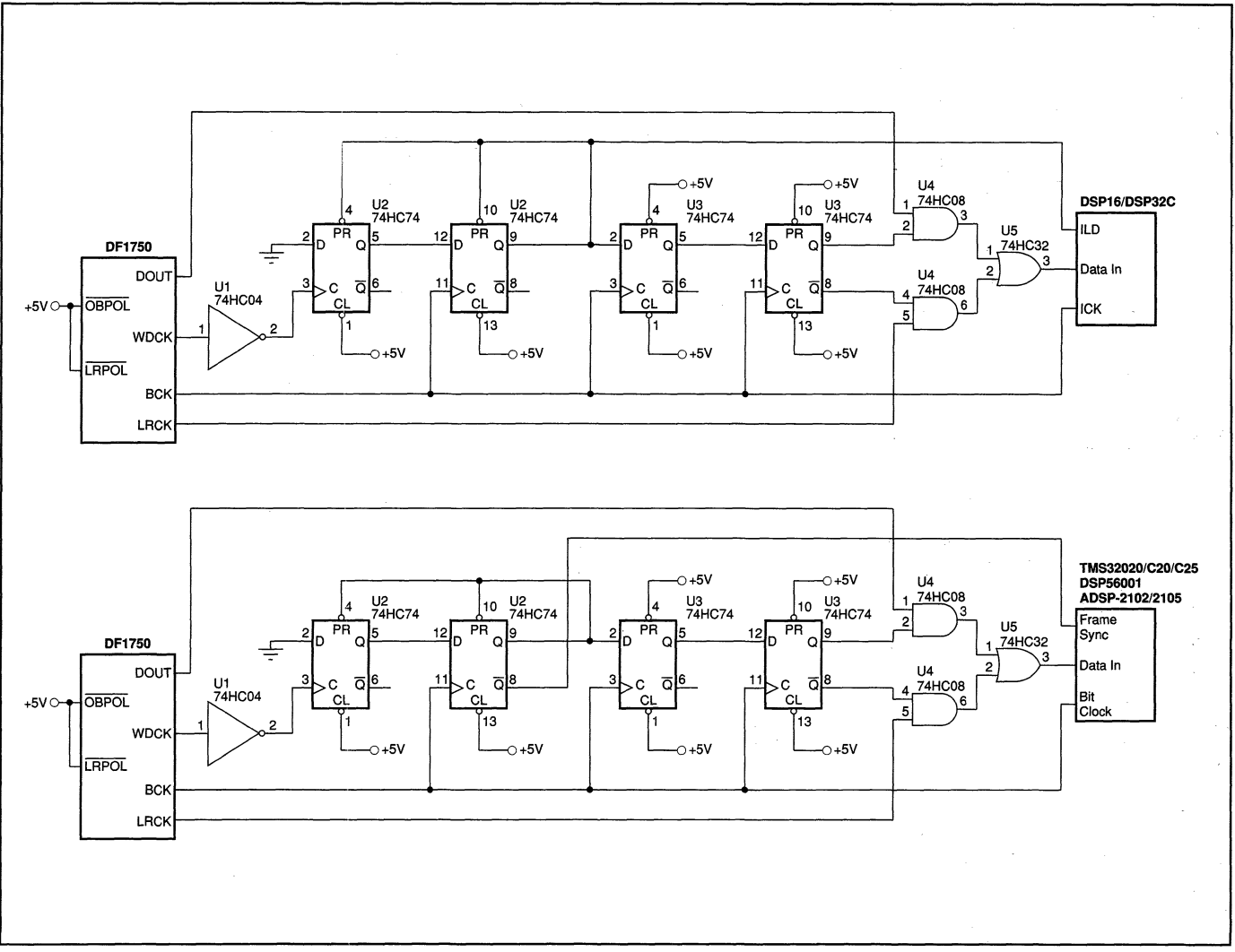
FIGURE 11. PCM1750/DF1750 to DSP IC Schematic.

For Immediate Assistance, Contact Your Local Salesperson

BURR - BROWN®
[BB]
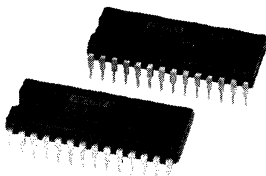
PCM1760P/U
DF1760P/U

**DEMO BOARD
AVAILABLE
See Appendix A for
more information**

Multi-Bit Enhanced Noise Shaping 20-Bit
ANALOG-TO-DIGITAL CONVERSION SYSTEM

FEATURES

● **DUAL 20-BIT MONOLITHIC MODULATOR
(PCM1760) AND MONOLITHIC
DECIMATING DIGITAL FILTER (DF1760)**

● **HIGH PERFORMANCE:
THD + N: –92dB typ, –90dB max
Dynamic Range: 108dB typ
SNR: 108dB min, 110dB typ
Channel Separation: 98dB typ, 94dB min**

● **64X OVERSAMPLING**

● **CO-PHASE CONVERSION**

● **RUNS ON 256fs OR 384fs SYSTEM
CLOCK**

● **VERSATILE INTERFACE CAPABILITY:
16-, 20-Bit Output
MSB First or LSB First Format**

● **OPTIONAL FUNCTIONS:
Offset Error Calibration
Overflow Detection
Power Down Mode (DF1760)**

● **RUNS ON ±5V SUPPLIES (PCM1760) AND
5V SUPPLY (DF1760)**

● **COMPACT 28-PIN PACKAGES:
28-Pin DIP and SOIC**

DESCRIPTION

The PCM1760 and DF1760 combine for a low-cost,
high-performance dual 20-bit, 48kHz sampling ana-
log-to-digital conversion system which is specifically
designed for dynamic applications.

The PCM1760/DF1760 pair form a 4-bit, 4th order,
64X oversampling analog-to-digital converter.

The PCM1760 is a delta-sigma modulator that uses a
4-bit quantizer within the modulation loop to achieve
very high dynamic range.

The DF1760 is a high-performance decimating digital
filter. The DF1760 accepts 4-bit 64fs data from the
PCM1760 and decimates to 20-bit 1fs data.

The FIR filter of the DF1760 has pass-band ripple of
less than ±0.001dB and greater than 100dB of the
reject band attenuation.

PCM1760/DF1760

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DIGITAL AUDIO PRODUCTS—A/D

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$, $\pm V_{dd}$ = +5V, $+V_{DD}$ = +5V, f_S = 48kHz and ext. components = ±2% unless otherwise noted.

PARAMETER	CONDITIONS	PCM1760/DF1760 MIN	PCM1760/DF1760 TYP	PCM1760/DF1760 MAX	UNITS
RESOLUTION		20			Bits
ANALOG INPUT					
Input Range	$R_{IN}1$ = 2.2kΩ		±2.5		Vp-p
Input Impedance	$R_{IN}1$ = 2.2kΩ		$R_{IN}1$		Ω
SAMPLING FREQUENCY					
Cover Range of fs	Integrator Constants: Application[1]	30	48	50	kHz
ACCURACY					
Gain Error			±0.5	±1.0	dB
Gain Mismatch				±0.5	dB
Bipolar Zero Error	V_{IN} = 0 at 20s After Power-On			±0.4	% FSR[2]
Gain Drift	0°C to +70°C		100		ppmfs/°C
Bipolar Zero Drift	0°C to +70°C		20		ppmfs/°C
DYNAMIC CHARACTERISTICS[4]					
THD + N/(0dBFS) P, U	f_{IN} = 1kHz		−92	−90	dB
P-L, U-L			−90	−88	dB
THD + N/(−20dBFS) P, U	f_{IN} = 1kHz		−76	−70	dB
P-L, U-L			−76	−70	dB
THD + N/(−60dBFS) P, U	f_{IN} = 1kHz		−44	−42	dB
P-L, U-L			−44	−42	dB
Dynamic Range P, U	f_{IN} = 1kHz, V_{IN} = −60dBFS, A Filter	104	108		dB
P-L, U-L		104	108		dB
SNR P, U	V_{IN} = 0, A Filter	108	110		dB
P-L, U-L		106	110		dB
Frequency Response	f_{IN} = 20kHz		±0.1		dB
Channel Separation	f_{IN} = 1kHz, A Filter	94	98		dB
DIGITAL FILTER					
Over Sample Rate			64		fs
Ripple in Band	0 - 0.04535fs			±0.0001	dB
Stopband Attenuation −1	0.5465fs - 63.4535fs	−94			dB
Stopband Attenuation −2	0.5465fs - 3.4535fs	−100			dB
LOGIC INPUTS AND OUTPUTS					
Logic Family Input			TTL Level Compatible CMOS		
Frequency (System Clock 1)	256fs		12.288		MHz
Frequency (System Clock 2)	384fs		18.432		MHz
Duty Cycle (System Clock 1)	256fs	40	50	60	%
Duty Cycle (System Clock 2)	384fs	45	50	55	%
Data Clock Input		32	48	64	fs
Logic Family Output			CMOS		
Data Clock Output			64		fs
Data Coding			Two's Complement		
Data Bit Length		16	20		Bits
Data Format			Selectable		
Output Data Delay	fs = 48kHz		1.5		ms
POWER SUPPLY REQUIREMENTS					
Supply Voltage					
$\pm V_{CC}$	PCM1760	±4.75	±5.0	±5.25	V
$\pm V_{dd}$	PCM1760	±4.75	±5.0	±5.25	V
$+V_{DD}$	DF1760	4.75	5.0	5.25	V
Supply Current					
$+I_{CC}$	PCM1760		24	36	mA
$−I_{CC}$	PCM1760		−30	−45	mA
$+I_{dd}$	PCM1760		12	18	mA
$−I_{DD}$	PCM1760		−8	−12	mA
$+I_{DD}$ −1	DF1760, Normal Mode		40	55	mA
$+I_{DD}$ −2	DF1760, Power-Down Mode		4	6.6	mA
Power Consumption	PCM1760		370	500	mW
	DF1760, Normal Mode		200	275	mW
	DF1760, Power-Down Mode		20	33	mW
TEMPERATURE RANGE					
Operating	PCM1760/DF1760	0	+25	+70	°C
Storage	PCM1760/DF1760	−50		+125	°C

NOTES: (1) Integrator Constants are determined by the external components shown in the block diagram. (2) FSR means Full Scale Range, digital output code is from 90000H to 70000H, FSR = 5.0V. (3) Use 20-bit DAC, 20kHz LPF, 400Hz HPF, average response. (4) Average response using a 20-bit reconstruction DAC with 20kHz low-pass filter and 400Hz high-pass filter.

ABSOLUTE MAXIMUM RATINGS—PCM1760

Supply Voltage	±6V
Voltage Mismatch	0.1V
Analog Input	±V_{CC}
Digital Input	+V_{DD} +0.3V
	GND −0.3V
Power Dissipation/P	580mW
Power Dissipation/U	550mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s)	235°C
Operating Temperature	0°C to +70°C
Storage Temperature	−50°C to +125°C

ABSOLUTE MAXIMUM RATINGS—DF1760

Supply Voltage	7.0V
Voltage Mismatch	0.1V
Digital Input	+V_{DD}+0.5V
	V_{SS} −0.5V
Input Current	±20mA
Power Dissipation/P	460mW
Power Dissipation/U	440mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s, reflow)	235°C
Operating Temperature	0°C to +70°c
Storage Temperature	−50°C to +125°C

ORDERING INFORMATION

MODEL	PACKAGE	THD +N (fs)	SNR
PCM1760P	PDIP	−90dB	108dB
PCM1760U	SOIC	−90dB	108dB
PCM1760P-L	PDIP	−88dB	106dB
PCM1760U-L	SOIC	−88dB	106dB
DF1760P	PDIP	NA	NA
DF1760U	SOIC	NA	NA

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1760P	28-Pin PDIP	800
PCM1760U	28-Pin SOIC	804
PCM1760P-L	28-Pin PDIP	800
PCM1760U-L	28-Pin SOIC	804
DF1760P	28-Pin PDIP	801
DF1760U	28-Pin SOIC	805

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN ASSIGNMENTS PCM1760

Top View   **SOIC/DIP**

Out-2R	1		28	NC
In-2R	2		27	BPODC-R
Out-1R	3		26	D_3
In-1R	4		25	D_2
SERVO DC	5		24	D_1
+V_{CC}	6		23	D_0
AGND	7	PCM1760	22	+V_{DD}
−V_{CC}	8		21	DGND
BGDC	9		20	−V_{DD}
NC	10		19	256fs
In-1L	11		18	Strobe
Out-1L	12		17	L/RCK
In-2L	13		16	BPODC-L
Out-2L	14		15	NC
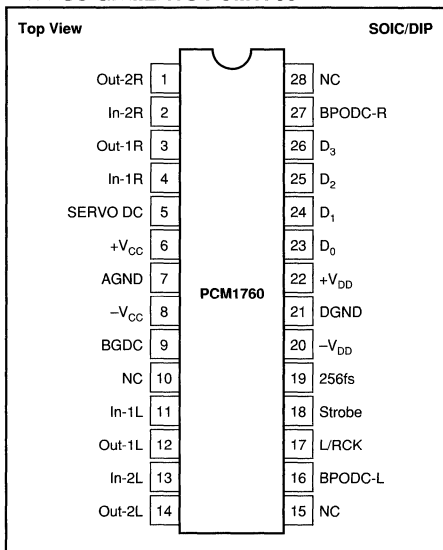
PIN	I/O[1]	NAME	DESCRIPTION
1	O	Out-2R	Right Channel Second Integrator Output
2	I	In-2R	Right Channel Second Integrator Input
3	O	Out-1R	Right Channel First Integrator Output
4	I	In-1R	Right Channel First Integrator Input
5	—	SERVO DC	Servo Amp Decoupling Capacitor
6	—	+V_{CC}	+5V Analog Supply Voltage
7	—	AGND	Analog Common
8	—	−V_{CC}	−5V Analog Supply Voltage
9	—	BGDC	Band Gap Reference Decoupling Capacitor
10	—	NC	No Connection
11	I	In-1L	Left Channel First Integrator Input
12	O	Out-1L	Left Channel First Integrator Output
13	I	In-2L	Left Channel Second Integrator Input
14	O	Out-2L	Left Channel Second Integrator Output
15	—	NC	No Connection
16	—	BPODC-L	Left Channel Bipolar Offset Decoupling Capacitor
17	O	L/RCK	LR Clock Output (64fs)
18	O	Strobe	Data Strobe Output (128fs)
19	I	256fs	256fs Clock Input
20	—	−V_{DD}	−5V Digital Supply Voltage
21	—	DGND	Digital Common
22	—	+V_{DD}	+5V Digital Supply Voltage
23	O	D_0	D_0 Data Output (LSB)
24	O	D_1	D_1 Data Output
25	O	D_2	D_2 Data Output
26	O	D_3	D_3 Data Output (MSB)
27	—	BPODC-R	Right Channel Bipolar Offset Decoupling Capacitor
28	—	NC	No Connection

NOTE: (1) O = Output terminal; I = Input terminal.

PCM1760/DF1760

8.1

DIGITAL AUDIO PRODUCTS—A/D

PIN ASSIGNMENTS DF1760

Top View   **SOIC/DIP**

```
OVL    1          28   V_SS2
OVR    2          27   V_DD2
D_3    3          26   TP2
D_2    4          25   CLKSEL
D_1    5          24   S/M
D_0    6          23   Mode 1
TP1    7   DF1760 22   Mode 2
V_SS1  8          21   /PD
V_DD1  9          20   LRSC
256fs 10          19   FSYNC
Strobe 11         18   SDATA
LRCK  12          17   L/R
CALD  13          16   SCLK
CAL   14          15   SYSCLK
```

PIN	I/O[1]	NAME	DESCRIPTION
1	O	OVL	Left Channel Overflow Output (Active High)
2	O	OVR	Right Channel Overflow Output (Active High)
3	I	D_3	D3 Data Input (MSB)
4	I	D_2	D2 Data Input
5	I	D_1	D1 Data Input
6	I	D_0	D0 Data Input (LSB)
7	–	TP1	Test Pin (No Connection)
8	–	V_{SS1}	Common Channel 1
9	–	V_{DD1}	+5V Channel 1
10	O	256fs	256fs Clock Output
11	I	Strobe	Data Strobe Clock Input (128fs)
12	I	LRCK	LR Clock Input
13	I↑	CALD	Calibration Function Enable (Active Low)
14	O	CAL	Calibration Output (High During Calibration)
15	I	SYSCLK	System Clock Input (256fs or 384fs)
16	I↑/O	SCLK	Data Clock
17	I↑/O	L/R	LR Channel Phase Clock
18	O	SDATA	Serial Data Output (1fs)
19	I↑/O	FSYNC	Frame Clock (2fs)
20	I↑	LRSC	Phase Control of LR Channel Phase Clock
21	I↑	/PD	Power Down Mode Enable Input (Active Low)
22	I↑	Mode2	Output Format Selection Input 2
23	I↑	Mode1	Output Format Selection Input 1
24	I↑	S/M	Slave/Master Mode Selection Input (High Makes Slave Mode)
25	I↑	CLKSEL	System Clock Selection Input (High Makes 256fs)
26	–	TP2	Test Pin (No Connection)
27	–	V_{DD2}	+5V Channel 2
28	–	V_{SS2}	Common Channel 2

NOTE: (1) O = Output terminal; I = Input terminal.

BLOCK DIAGRAM OF DF1760

BURR - BROWN®
BB
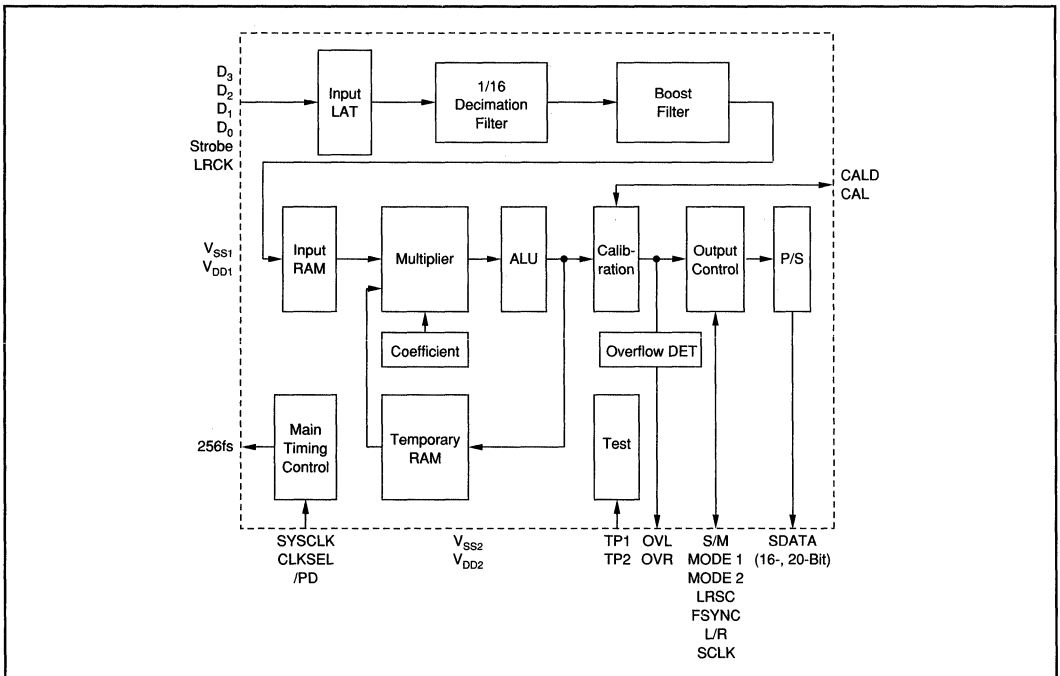
BLOCK DIAGRAM OF PCM1760
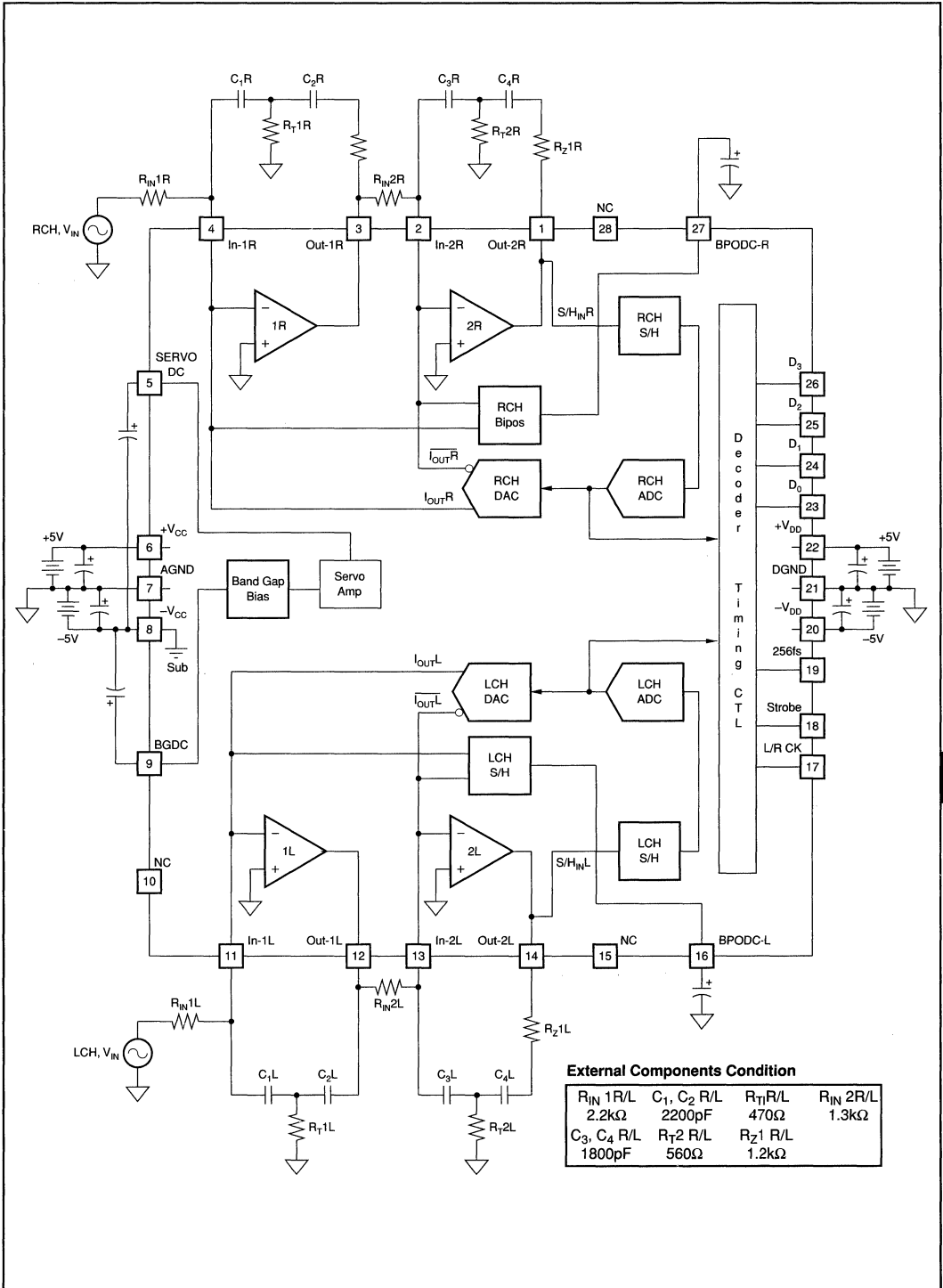
External Components Condition

R_{IN} 1 R/L	C_1, C_2 R/L	R_{TI}R/L	R_{IN} 2R/L
2.2kΩ	2200pF	470Ω	1.3kΩ
C_3, C_4 R/L	R_T2 R/L	R_Z1 R/L	
1800pF	560Ω	1.2kΩ	

PCM1760/DF1760

8.1

DIGITAL AUDIO PRODUCTS—A/D

TYPICAL PERFORMANCE CURVES

OVERALL PASS-BAND
CHARACTERISTICS OF THE DF1760

OVERALL CHARACTERISTICS OF THE DF1760

PASS-BAND CHARACTERISTICS
OF THE FIR PORTION OF THE DF1760

TOTAL PASS-BAND FREQUENCY RESPONSE,
COMBINATION OF PCM1760 AND DF1760

TYPICAL FFT ANALYSIS OF THE 1kHz fs INPUT SIGNAL

fs = 48.000000kHz F_{C1} = 1.171876kHz

DIGITAL AUDIO PRODUCTS—A/D **8.1** **PCM1760/DF1760**
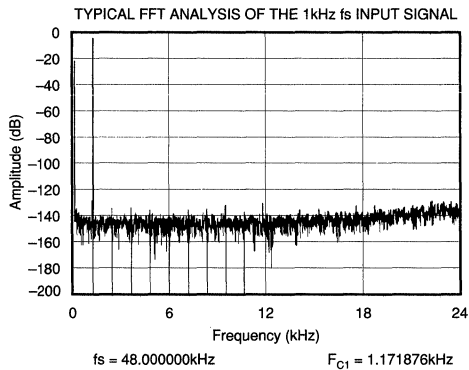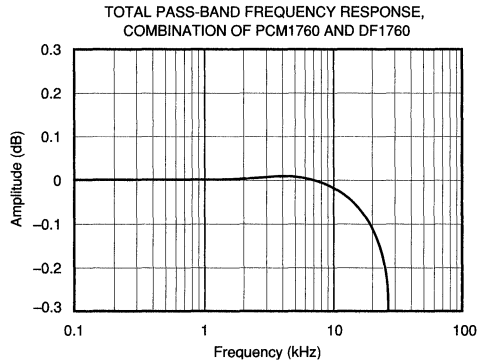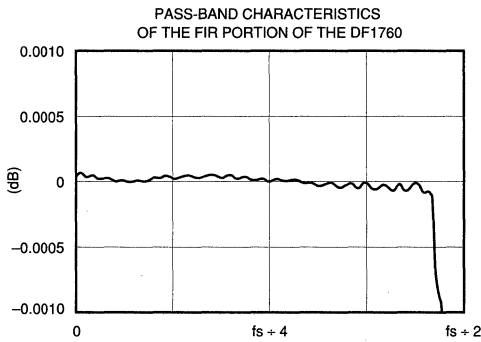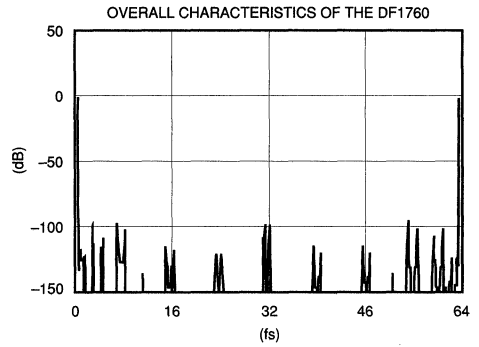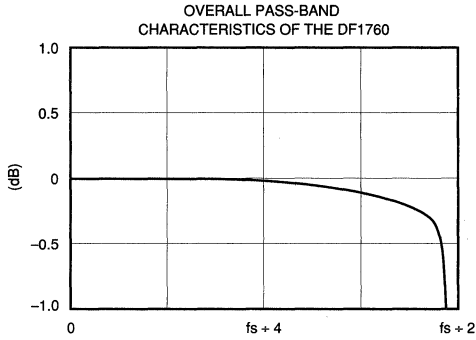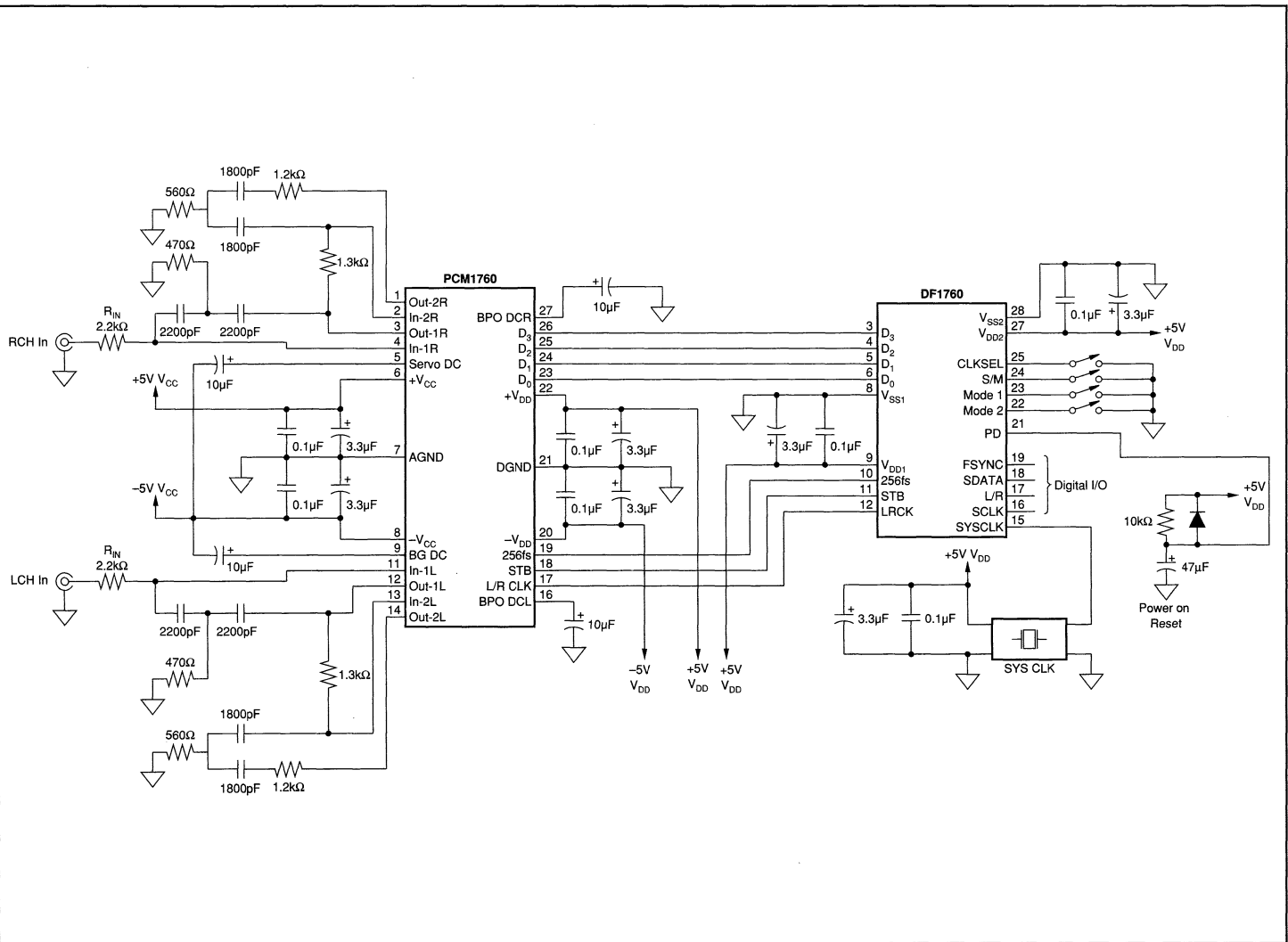
FUNCTIONS OF
THE DIGITAL FILTER

SYSTEM CLOCK

The DF1760 can accept a system clock of either 256fs or 384fs. If a 384fs system clock is used, the DF1760 divides by 2/3 to create the 256fs system clock required for the PCM1760. The system clock is applied to pin 15 (SYSCLK input). The actual clock selection is done by setting pin 25 (CLKSEL input) "high" for 256fs clock and "LOW" for 384fs clock.

The detailed timing requirements for the system clock are shown in Figure 3c.

CLKSEL	SYSCLK
H	256fs
L	384fs

MASTER/SLAVE MODE

The DF1760 can be used in both the master mode and slave mode. In the master mode, the DF1760 outputs L/R (left/right channel phase clock), SCLK (data clock) and FSYNC (frame clock 2fs) signals. In the slave mode, the DF1760 accepts L/R, SCLK and FSYNC signals. The mode selection is done by taking pin 24 (S/M INPUT) "HIGH" for slave mode and "LOW" for master mode.

S/M	MODE
H	Slave
L	Master

OUTPUT DATA FORMAT

The serial output data has four possible formats. The selection of the formats can be done by the Mode 1 and Mode 2 inputs.

MODE 1	MODE 2	FORMATS
H	H	MSB First, 16 Bits, Falling Edge
L	H	MSB First, 20 Bits, Falling Edge
H	L	MSB First, 20 Bits, Rising Edge
L	L	LSB First, 20 Bits, Falling Edge

LR CHANNEL PHASE CLOCK

The status of the LR channel phase clock can be set by the LRSC input.

LRSC	L/R CLOCK AND CHANNEL	
H	H = LCH,	L = RCH
L	L = LCH,	H = RCH

OVERFLOW DETECTION

When a near-to-clipping input condition is detected, OVL output (Pin 1), or OVR output (Pin 2), becomes "HIGH" for a duration of 4096/fs (about 85ms) depending upon on the channel detected.

The OVL and OVR output return to "LOW" after 4096/fs duration automatically.

OFFSET CALIBRATION MODE

The offset error is calibrated by storing the digital data when the input is zero in registers and subtracting it from the future data with actual signal input.

CALD	CALIBRATION
H	Disable
L	Enable

To enable the calibration mode, set the CALD input (Pin 13) "LOW". The calibration mode is disabled by setting the CALD input (Pin 13) "HIGH". The calibration cycle is initiated by setting the /PD input (Pin 21) "LOW" for more than 2 system clock periods and then setting it "HIGH". During the calibration cycle, the CAL output (Pin 14) becomes "HIGH", all the serial data is forced to "LOW", and the L/R (Pin 17), SCLK (Pin 16) and FSYNC (Pin 19) pins become input terminals after the completion of the calibration cycle. The CAL output is "LOW".

POWER DOWN MODE/RESET

The /PD input (Pin 21) has two functions. First, it should be set at "HIGH" after application or restoration of power (V_{SS} and/or V_{DD}) to accomplish the power-on/mode reset function. The detail timing requirements for this function are shown in Figure 3f. Second, the DF1760 is placed in the power down mode by setting the /PD input (Pin 21) "LOW". Set the /PD input (Pin 21) "HIGH" for normal operation mode.

/PD	OPERATION
H	Normal
L	Power Down

The power dissipation of the DF1760 in the power down mode is about 1/10 of the normal operation mode. During the power down mode, the L/R, SCLK, and FSYNC pins become input pins and all the serial data is forced "LOW". The 256fs output is enabled even in the power down mode.

The detailed timing of the power down mode operation and the offset calibration is shown in Figure 3b.

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Delay from Overflow Detection to OVL (OVR) Output	T_{OR}	–	–	0	ns
OVL (OVR) Output Pulse Width	T_{OF}	–	4096	–	1/fs
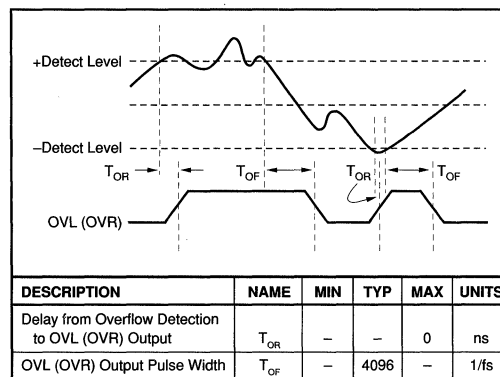
FIGURE 3a. DF1760 Overflow Detection.
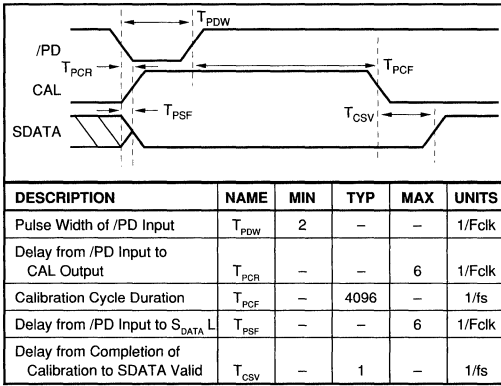
FIGURE 3b. DF1760 Power Down and Offset Calibration.

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Pulse Width of /PD Input	T_{PDW}	2	–	–	1/Fclk
Delay from /PD Input to CAL Output	T_{PCR}	–	–	6	1/Fclk
Calibration Cycle Duration	T_{PCF}	–	4096	–	1/fs
Delay from /PD Input to S_{DATA} L	T_{PSF}	–	–	6	1/Fclk
Delay from Completion of Calibration to SDATA Valid	T_{CSV}	–	1	–	1/fs
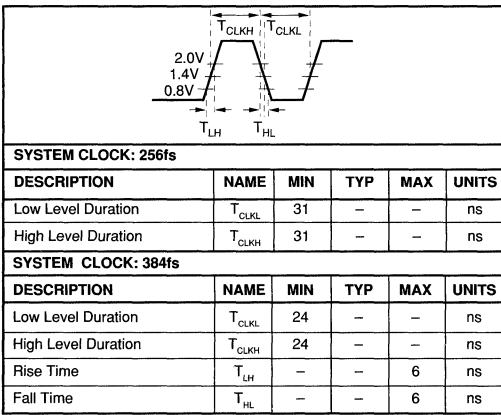
FIGURE 3c. System Clock Timing Requirements of DF1760.

SYSTEM CLOCK: 256fs

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Low Level Duration	T_{CLKL}	31	–	–	ns
High Level Duration	T_{CLKH}	31	–	–	ns

SYSTEM CLOCK: 384fs

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Low Level Duration	T_{CLKL}	24	–	–	ns
High Level Duration	T_{CLKH}	24	–	–	ns
Rise Time	T_{LH}	–	–	6	ns
Fall Time	T_{HL}	–	–	6	ns

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
SCLK Frequency	F_{SLK}	–	64fs	–	
SCLK Frequency Duty Cycle		–	50	–	%
FSYNC Frequency	F_{SYNC}	–	2fs	–	
FSYNC Frequency Duty Cycle		–	50	–	%
Delay from SCLK to L/R Edge	T_{SLR}	–20	–	50	ns
Delay from Falling Edge of SCLK to SDATA Valid	T_{DSS}	–	–	50	ns
Delay from SCLK to FSYNC Edge	T_{SF}	–20	–	50	ns
Delay from Rising Edge of SCLK to SDATA Valid	T_{SDR}	100	–	–	ns
Delay from SDATA Valid to Rising Edge of SCLK	T_{DSV}	100	–	–	ns

FIGURE 3d. Output Timing of Master Mode, DF1760.
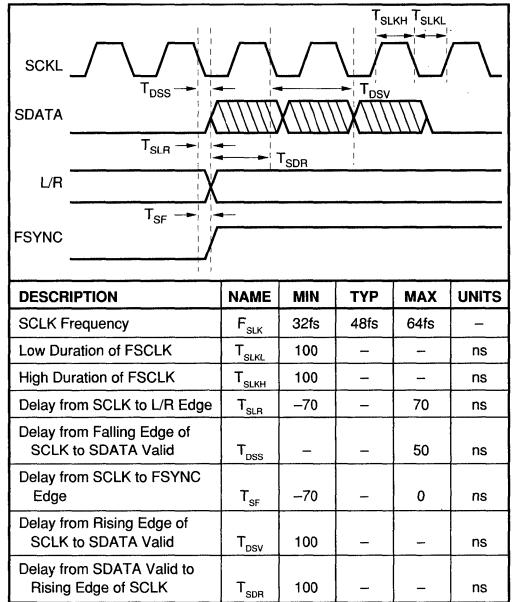
FIGURE 3e. Timing of Slave Mode, DF1760.

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
SCLK Frequency	F_{SLK}	32fs	48fs	64fs	–
Low Duration of FSCLK	T_{SLKL}	100	–	–	ns
High Duration of FSCLK	T_{SLKH}	100	–	–	ns
Delay from SCLK to L/R Edge	T_{SLR}	–70	–	70	ns
Delay from Falling Edge of SCLK to SDATA Valid	T_{DSS}	–	–	50	ns
Delay from SCLK to FSYNC Edge	T_{SF}	–70	–	0	ns
Delay from Rising Edge of SCLK to SDATA Valid	T_{DSV}	100	–	–	ns
Delay from SDATA Valid to Rising Edge of SCLK	T_{SDR}	100	–	–	ns

DESCRIPTION	NAME	MIN	TYP	MAX	UNITS[1]	APPLIES TO MODE
Power on to PD ↑	T_{PDW}	2			1/fs	Master/Slave
PD ↑ to L/R ↑ (LRSC = "H")	T_{SP}	–1		+1	1/Fclk	Slave
PD ↑ to L/R ↓ (LRSC = "L")	T_{SP}	–1		+1	1/Fclk	Slave

NOTE: (1) fs: sampling rate. Fclk: system clock frequency.

FIGURE 3f. Power On and Mode Reset Timing.

PCM1760/DF1760

8.1

DIGITAL AUDIO PRODUCTS—A/D

THEORY OF OPERATION

MULTI-BIT ENHANCED NOISE SHAPING

A block diagram of a typical 1-bit delta-sigma modulator is shown in Figure 4.

In Figure 4, the quantizer consists of a single bit which has two possible states, either "0" or "1". The input signal is sampled at a much higher sample rate than the nyquist sampling frequency. The quantizer output data stream is digitally filtered for higher resolution nyquist data. The theoretical SNR is determined by the number of the order of the integrator and the oversampling rate.
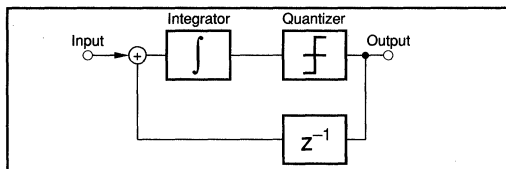
FIGURE 4. Single Stage 1-Bit Delta-Sigma.
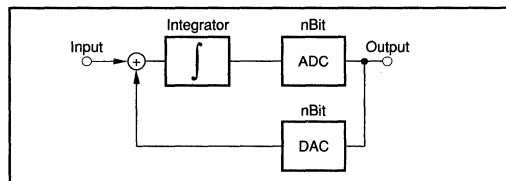
FIGURE 5. Single Stage Multi-bit Delta-Sigma.

There is a practical limit to increasing the numbers of order of the integrator due to an inherent oscillation in the modulator. There is also a limit to increasing the sample rate due to the increase in jitter sensitivity associated with high clock frequencies.

The PCM1760 utilizes a four-bit quantizer instead of the conventional one-bit method. The quantizing noise of a four-bit quantizer is 1/16 of the one-bit version. Using the four-bit quantizer allows for a lesser order number of the integrator and a lower oversampling rate to achieve similar performance to that of a more complex one-bit system.

A block diagram of the PCM1760 modulator is shown in Figure 6. The PCM1760 is a fourth-order integrator that samples at 64x oversampling, and samples left and right channel input signal simultaneously.
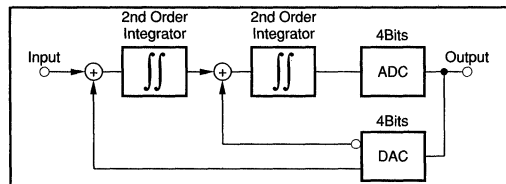
FIGURE 6. Multi-bit Enhanced Noise Shaping.

The DF1760 accepts the four-bit 64fs noise shaped data stream from the PCM1760 and decimates to 1/16 with an initial filter, and then decimates to 1fs 20-bit data using a 4x oversampling filter.

The PCM1760 and DF1760 combination achieves a dynamic range of 108dB and SNR of 110dB even with a single-ended input.

NOTE: (1) Tantalum 3.3µF. (2) Ceramic 0.1µF.
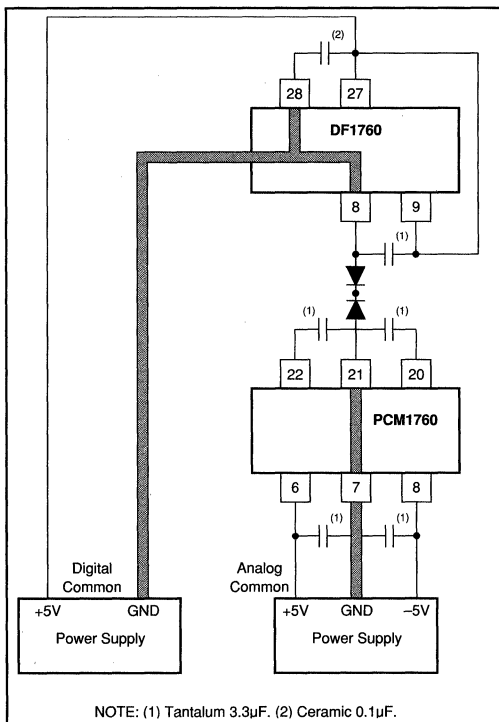
FIGURE 7. Recommended Power Supply Connection and Decoupling.

LAYOUT PRECAUTIONS

Analog common and digital common of the PCM1760 are not connected internally. These should be connected together with the common of the DF1760 as close to the unit as possible, preferably to a large ground plane under the PCM1760.

The use of a separate +5V supply is recommended for the PCM1760 and DF1760, and to connect the common at one point as described above. Low impedance analog and digital commons returns are essential for better performance.

The power supplies should be bypassed with tantalum capacitors as close as possible to the units. See Figure 7 for recommended common connections and power supplies bypassing.

OUTPUT TONE ELIMINATION

When the sampling frequency (fs) is between 40kHz and 50 kHz and the L/R relative offset voltage (ΔVs) is less than or equal to 0.05% of full scale range, the PCM1760 may output a tone similar to an idle tone. This tone is very low and its frequency depends on the input L/R relative offset voltage, ΔVs. This tone never occurs when the sampling frequency (fs) is 32kHz.

To avoid this tone, the offset voltage should be summed using an amplifier, buffer, active low pass filter, etc., to cause the input L/R relative offset voltage (ΔVs) to be greater than 0.05% of full scale range.

It is recommended that:

(A) Sum offset at both L/R channels
   Lch: $V_{IL} = -20mV \pm 10\%$
   Rch: $V_{IR} = +10mV \pm 10\%$

(B) Sum offset at L channel
   Lch: $V_{IL} = -30mV \pm 10\%$
   Rch: $V_{IR} = \pm 1mV$ (by a precircuit)

When FSR = 5V (± 2.5V).

Figure 8 shows an application circuit for summing the offset at both L/R channels.

Alternately, Figure 9 shows an application circuit for use when fs = 48kHz which changes the external integrator circuit of the PCM1760.

MODULATOR COMPONENTS AND SAMPLING FREQUENCY

The PCM1760/DF1760 are capable of 30kHz to 50kHz fs sampling frequency by condition with external components value which are shown in Basic Connection Diagram.

The characteristics of the modulator's integrator can be set by external components. The values in the block diagram on page five are recommended for optimized performance. Low leakage, low voltage coefficient capacitors are recommended for integration capacitors.

The tolerance of external components should be better than ±2%.
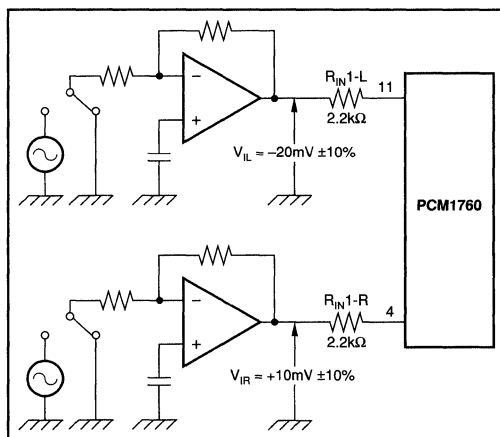
FIGURE 8. Application Example to Eliminate the Tone (offset voltage implementation for both channels).

OFFSET ERROR CALIBRATION

The offset voltage of the PCM1760 and the input stage of the system can be compensated by using the calibration mode of the DF1760. Offset calibration is shown in Figure 10. An optional analog switch is driven by a CAL output of the DF1760. The PD input of the DF1760 is used to initiate the calibration cycle.

ANALOG INPUT AND DIGITAL OUTPUT

Ideal output digital code range for 20-bit resolution is from 8000H (–Full Scale) to 7FFFFH (+Full Scale).

The DF1760, combined with 70000H (±FSR) of the PCM1760, produces a digital output code range at ±FSR input of 90000H (–FSR).

The relationship between analog input and digital output is shown in Table I.

PCM1760/DF1760

8.1

DIGITAL AUDIO PRODUCTS—A/D
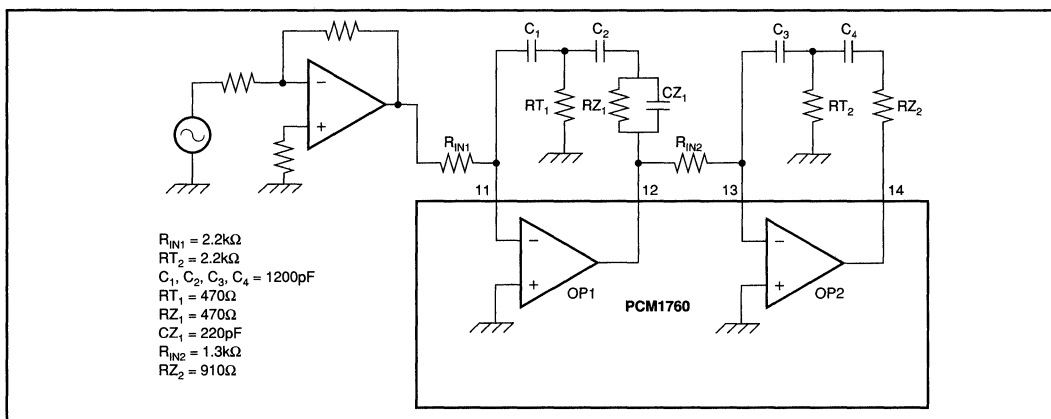
FIGURE 9. Application Example to Eliminate the Tone (alternative modulator's integrator circuit. Only for fs = 48kHz).

$R_{IN1} = 2.2k\Omega$
$RT_2 = 2.2k\Omega$
$C_1, C_2, C_3, C_4 = 1200pF$
$RT_1 = 470\Omega$
$RZ_1 = 470\Omega$
$CZ_1 = 220pF$
$R_{IN2} = 1.3k\Omega$
$RZ_2 = 910\Omega$

ANALOG INPUT	CONDITION	DIGITAL OUTPUT
+2.55V	+Max Input	72000H
+2.50V to +2.55V	Overflow	70000H to 72000H[2]
+2.50V	+FSR	70000H
0V	BPZ (Ideal)	00000H[1]
–2.50V	–FSR	90000H
–2.83V to –2.85V	Overflow	82FFFH to 82000H[2]
–2.85V	–Max Input	82000H

NOTES: (1) Incase of BPZ Error = 0. (2) Overflow detection level is over 70000H or under 82FFFH of digital output code.

TABLE I. Output Codes.

POWER SUPPLY SEQUENCING

The PCM1760 requires $\pm V_{CC}$ and $\pm V_{DD}$ power supplies. To avoid any possibility of latch-up, the $\pm V_{CC}$ and $\pm V_{DD}$ power should all be applied simultaneously or the $+V_{CC}$ and $+V_{DD}$ applied first followed by $-V_{CC}$ and $-V_{DD}$.

POWER-ON RESET AND MODE RESET

The timing requirements for POWER-ON RESET and MODE RESET are shown in Figure 3f. The DF1760 requires POWER-ON RESET when power is applied or restored. MODE RESET is required when any of the following has been changed: system clock, master/slave mode, output data format, L/R clock, calibration after POWER-ON in slave mode.

This reset should be done by holding the /PD input (pin 21) low for more than 2/fs. Suggested reset circuits are given in Figures 11, 12 and 13.

CLOCK INPUT

After power is applied to the DF1760, the system clock should be provided continuously. The DF1760 employs a dynamic logic architecture.
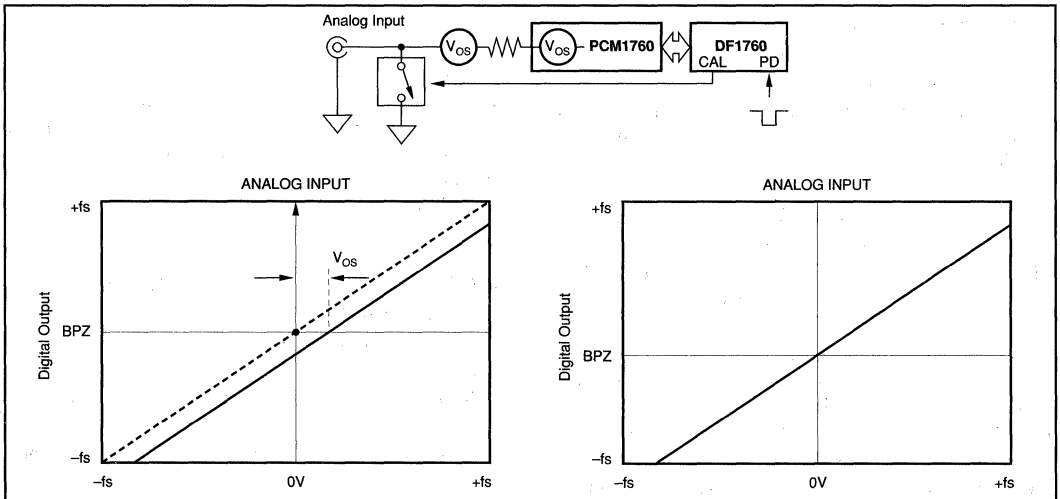
FIGURE 10. Illustration of Offset Calibration.
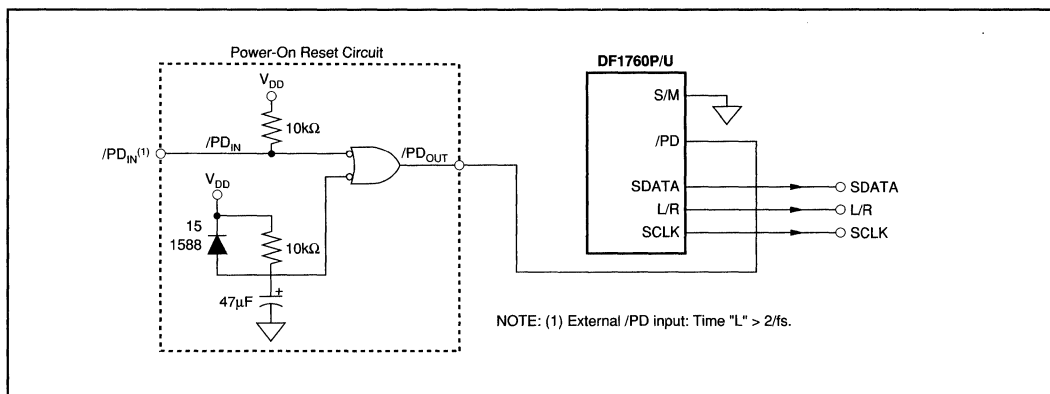
FIGURE 11. Master Mode Reset Circuit.
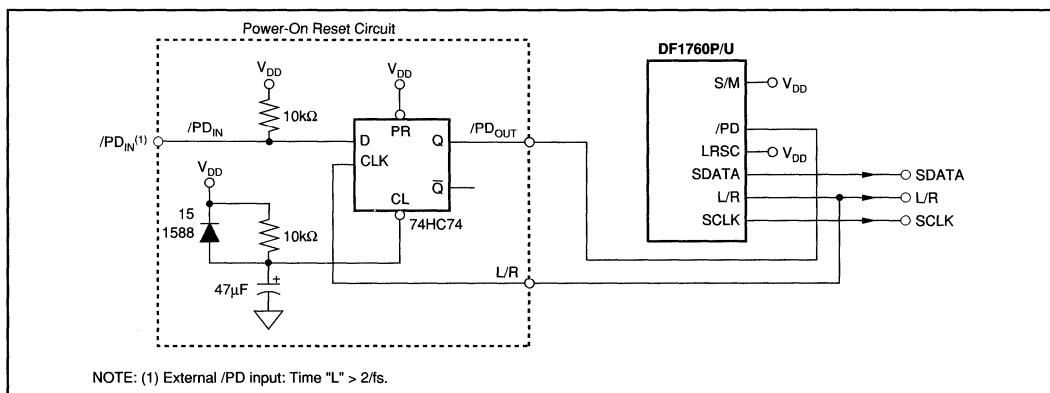
FIGURE 12. Slave Mode Reset Circuit, (LRSC = H).
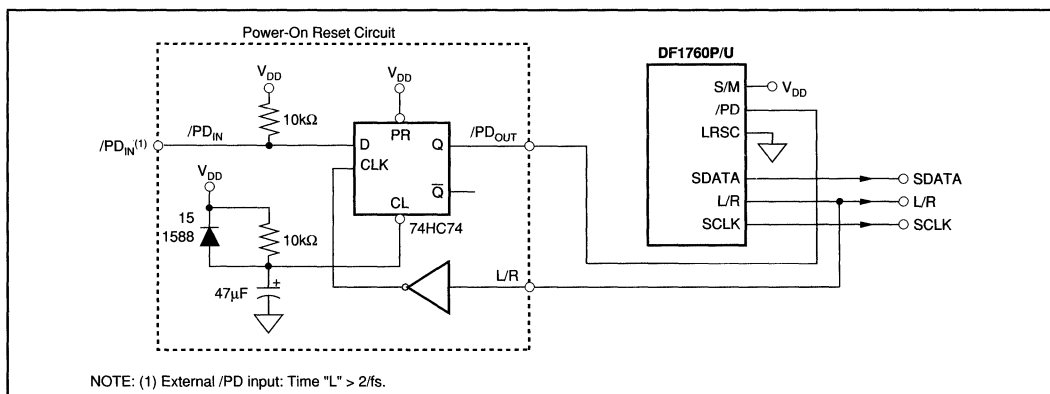
FIGURE 13. Slave Mode Reset Circuit, (LRSC = L).

PCM1760/DF1760

8.1

DIGITAL AUDIO PRODUCTS—A/D

TIMING CHARACTERISTICS
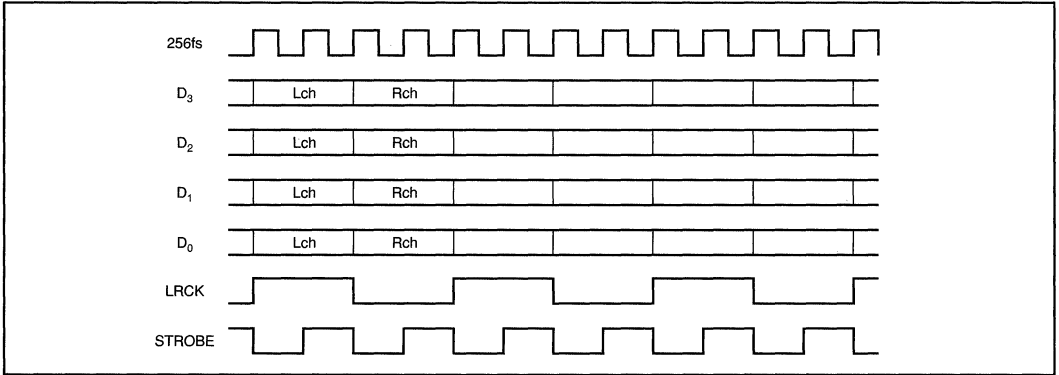
FIGURE 14. Input and Output Format of the DF1760 and PCM1760.
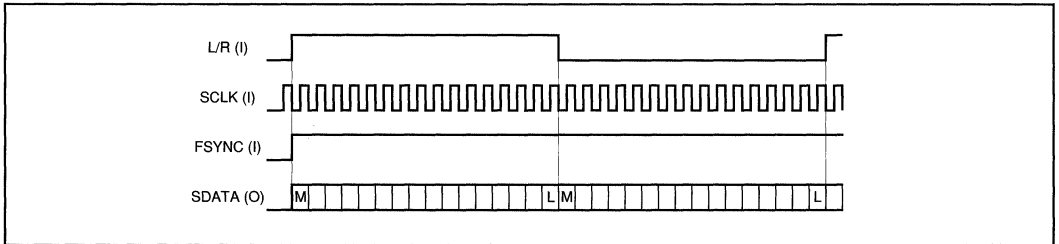
FIGURE 15a. Slave Mode and SCLK = 32fs. (Output format of the DF1760).
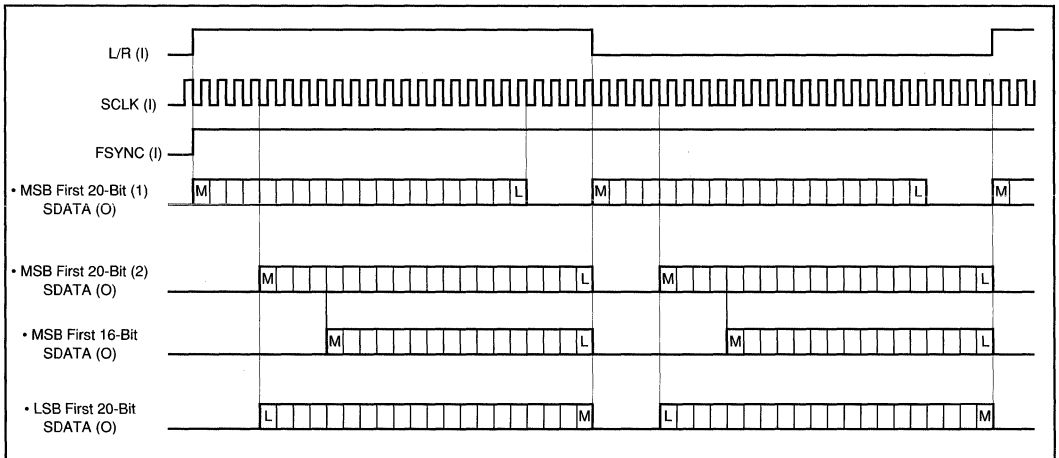
FIGURE 15b. Slave Mode and SCLK = 48fs.
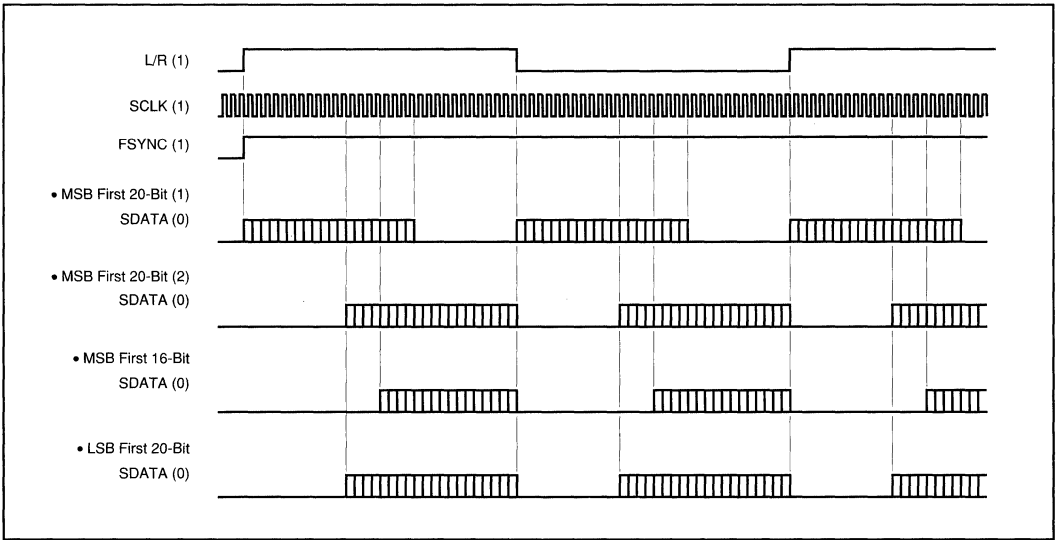
FIGURE 15c. Slave Mode and SCLK = 64fs.
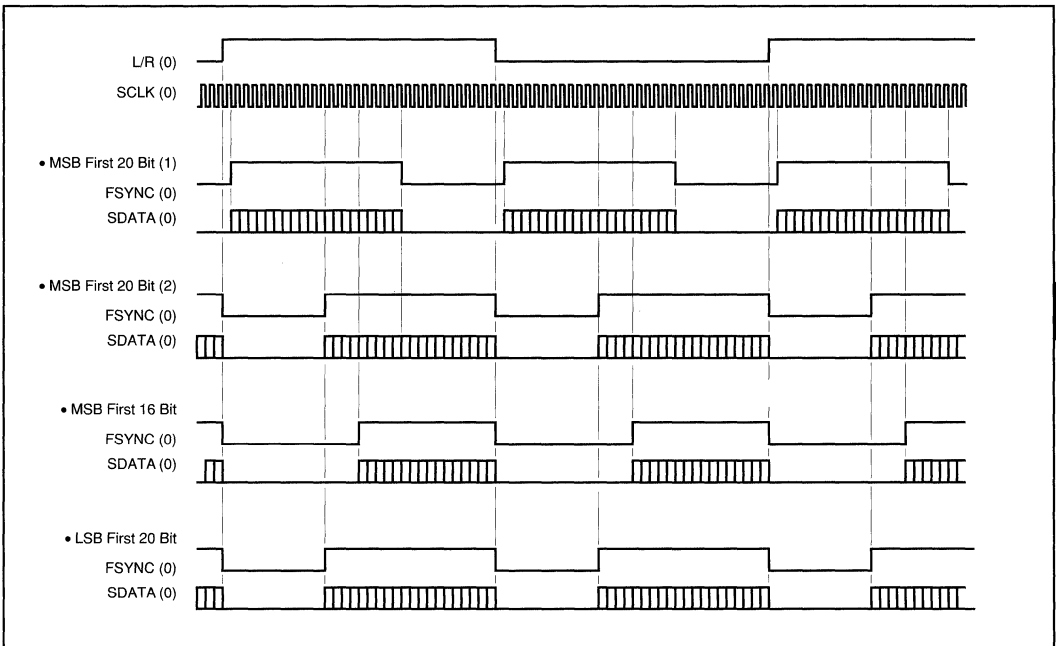
FIGURE 15d. Master Mode.

PCM1760/DF1760

8.1

DIGITAL AUDIO PRODUCTS—A/D

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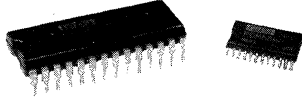
DESIGNED FOR AUDIO

PCM54
PCM55

ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-619.

16-Bit Monolithic
DIGITAL-TO-ANALOG CONVERTERS

FEATURES

● **PARALLEL INPUT FORMAT**
● **16-BIT RESOLUTION**
● **15-BIT MONOTONICITY (typ)**
● **−92dB TOTAL HARMONIC DISTORTION (K Grade)**
● **3μs SETTLING TIME (Voltage Out)**

● **96dB DYNAMIC RANGE**
● **±3V or ±1mA AUDIO OUTPUT**
● **OPERATES ON ±5V (PCM55) to ±12V (PCM54) SUPPLIES**
● **28-PIN DIP (PCM54)**
● **24-LEAD SOIC (PCM55)**

DESCRIPTION

The PCM54 and PCM55 family of converters are parallel input, fully monotonic, 16-bit digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The

converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve THD specifications if desired.

A current output (I_{OUT}) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-pin plastic mini-flatpak.

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SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 12V, unless otherwise noted.

PARAMETER	PCM54HP/PCM55HP MIN	TYP	MAX	PCM54JP/PCM55JP MIN	TYP	MAX	PCM54KP MIN	TYP	MAX	UNITS
DIGITAL INPUTS										
Resolution		16			*			*		Bits
Dynamic Range		96			*			*		dB
Logic Levels (TTL/CMOS Compatible):										
V_{IH}	+2.4		+5.25	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH}, V_{IN} = +2.7V			+40			*			*	μA
I_{IL}, V_{IN} = +0.4V			−0.5			*			*	mA
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error		±2			*			*		%
Bipolar Zero Error		±30			*			*		mV
Differential Linearity Error at Biploar Zero[1]		±0.001			*			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*			*		μV
TOTAL HARMONIC DISTORTION[3]										
(16-Bit Resolution)										
V_O = ±FS at f = 991Hz		−94	−82		−88	*	*		−92	dB
V_O = −20dB at f = 991Hz		−74	−68		*	*	*	−80	−74	dB
V_O = −60dB at f = 991Hz		−34	−28		*	*	*	−40	−34	dB
MONOTONICITY		15			*			*		Bits
SETTLING TIME (to ±0.006% of FSR)										
Voltage Output: 6V Step		3			*			*		μs
1LSB Step		1			*			*		μs
Current Output (1mA Step): 10Ω to 100Ω Load		350			*			*		ns
1kΩ Load[4]		350			*			*		ns
Deglitcher Delay (THD Test)[5]		2.5	4		*	*		*	*	μs
Slew Rate		10			*			*		V/μs
WARM-UP TIME	1			*			*			Min
ANALOG OUTPUT										
Voltage Output: Bipolar Range		±3			*			*		V
Output Current	±2			*			*			mA
Output Impedance		0.1			*			*		Ω
Short-Circuit Duration	Indefinite to Common				*			*		
Current Output:[6]										
Bipolar Range (±30%)		±1			*			*		mA
Bipolar Output Impedance (±30%)		1.2			*			*		kΩ
POWER SUPPLY REQUIREMENTS										
Voltage: +V_{CC} (PCM54)	+4.75	+12	+15.75	*	*	*	*	*	*	V
−V_{CC} (PCM54)	−4.75	−12	−15.75	*	*	*	*	*	*	V
+V_{CC} (PCM55)	+4.75	+5	+7.5	*	*	*	*	*	*	V
−V_{CC} (PCM55)	−4.75	−5	−7.5	*	*	*	*	*	*	V
Supply Drain: +V_{CC}		+13	+20		*	*		*	*	mA
−V_{CC}		−16	−25		*	*		*	*	mA
TEMPERATURE RANGE										
Operating	0		+70	*		*	*		*	°C
Storage	−55		+100	*		*	*		*	°C

* Specifications same as for PMC54HP.

NOTES: (1) Externally adjustable. If external adjustment is not used, connect a 0.01μF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected.

PCM54/55

8.2

DIGITAL AUDIO PRODUCTS—D/A

CONNECTION DIAGRAMS

NOTES: (1) MSB error (BPZ differential linearity error) can be adjusted to zero using this external circuit. (2) Connect to bipolar operation (+V_{CC} ≥ 8.5V for unipolar operation). (3) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21, and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.

NOTES: (1) Connect for bipolar operation. (+V_{CC} ≥ 8.5V for unipolar operation). (2) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19, and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.
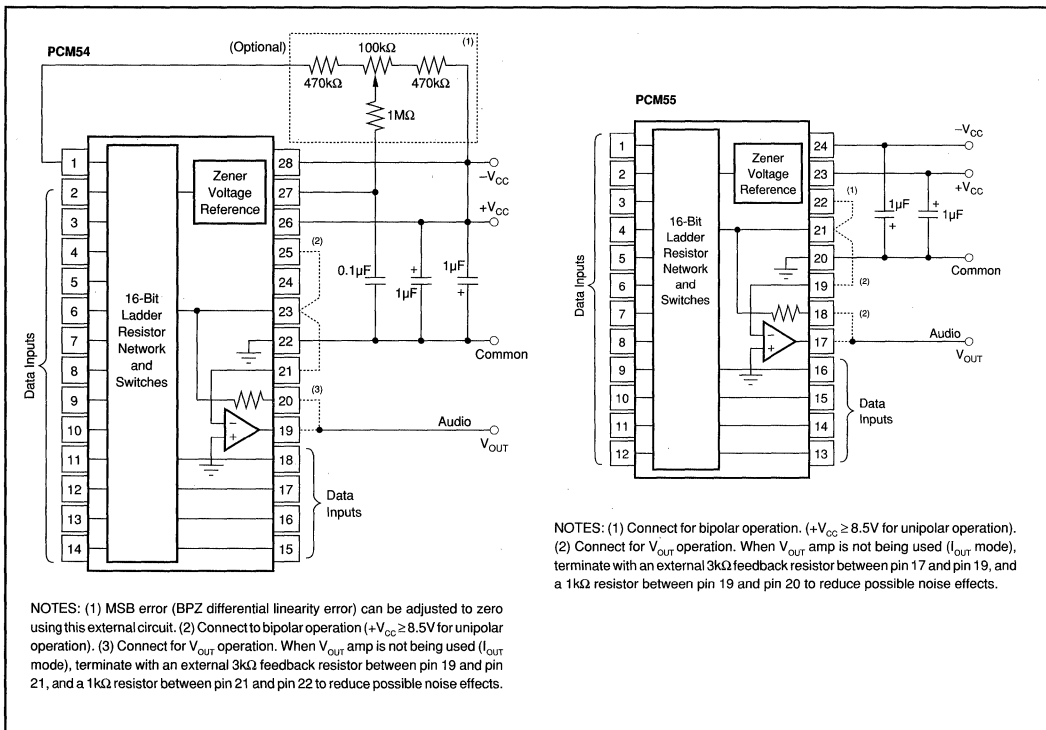
PIN ASSIGNMENTS

PIN	PCM54-DIP	PIN	PCM54-DIP
1	Trim	15	Bit 13
2	Bit 1 (MSB)	16	Bit 14
3	Bit 2	17	Bit 15
4	NC	18	Bit 16 (LSB)
5	Bit 3	19	V_{OUT}
6	Bit 4	20	R_{FB}
7	Bit 5	21	SJ
8	Bit 6	22	Common
9	Bit 7	23	I_{OUT}
10	Bit 8	24	NC
11	Bit 9	25	I_{BPO}
12	Bit 10	26	+V_{CC}
13	Bit 11	27	MSB Adjust
14	Bit 12	28	−V_{CC}

PIN ASSIGNMENTS

PIN	PCM55-SOIC	PIN	PCM55-SOIC
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16
5	Bit 5	17	V_{OUT}
6	Bit 6	18	Feedback Resisitor
7	Bit 7	19	Summing Junction
8	Bit 8	20	Common
9	Bit 9	21	Current Output
10	Bit 10	22	Bipolar Offset
11	Bit 11	23	+V_{CC}
12	Bit 12	24	−V_{CC}

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM54HP	28-Pin DIP	215
PCM54JP	28-Pin DIP	215
PCM54KP	28-Pin DIP	215
PCM55HP	24-Pin SOIC	178
PCM55JP	24-Pin SOIC	178

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage .... ±18VDC
Input Logic Voltage .... −1V to +5.5V
Power Dissipation PCM54 800mW, PCM55 400mW
Storage Temperature .... −55°C to +100°C
Lead Temperature, (soldering, 10s) .... +300°C

ORDERING INFORMATION

MODEL	THD at FS	PACKAGE
PCM54HP	0.008	28-pin DIP
PCM54JP	0.004	28-pin DIP
PCM54KP	0.0025	28-pin DIP
PCM55HP	0.008	24-lead SOIC
PCM55JP	0.004	24-lead SOIC

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PCM56P

PCM56U

DESIGNED FOR AUDIO

Serial Input 16-Bit Monolithic
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **SERIAL INPUT**
● **–92dB MAX THD: FS Input, K Grade, 16 Bits**
● **–74dB MAX THD: –20dB Input, K Grade, 16 Bits**
● **96dB DYNAMIC RANGE**
● **NO EXTERNAL COMPONENTS REQUIRED**
● **16-BIT RESOLUTION**
● **15-BIT MONOTONICITY, TYP**
● **0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR**
● **1.5µs SETTLING TIME, TYP: Voltage Out**
● **±3V OR ±1mA AUDIO OUTPUT**
● **EIAJ STC-007-COMPATIBLE**
● **OPERATES ON ±5V TO ±12V SUPPLIES**
● **PINOUT ALLOWS I_{OUT} OPTION**
● **PLASTIC DIP OR SOIC PACKAGE**

DESCRIPTION

The PCM56 is a state-of-the-art, fully monotonic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

This converter is completely self-contained with a stable, low noise, internal zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V to ±12V. Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero) to further improve total harmonic distortion (THD) specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

The PCM56 is packaged in a high-quality 16-pin molded plastic DIP package or SOIC and has passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.

PCM56P/U

8.2

DIGITAL AUDIO PRODUCTS—D/A

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PDS-700C

8.2.55

SPECIFICATIONS

ELECTRICAL

Typical at +25°C, and nominal power supply voltages ±5V unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
		PCM56U, PCM56P/-J/-K		
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution		16		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	V
V_{IL}	0		+0.8	V
I_{IH}, V_{IN} = +2.7V			+1.0	µA
I_{IL}, V_{IN} = +0.4V			−50	µA
Input Clock Frequency	10.0			MHz
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±2.0		%
Bipolar Zero Error		±30		mV
Differential Linearity Error		±0.001		% of FSR[2]
Noise (rms, 20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		6		µV
TOTAL HARMONIC DISTORTION				
V_O = ±FS at f = 991Hz: PCM56P-K		−94	−92	dB
PCM56P-J		−94	−88	dB
PCM56P, PCM56U		−94	−82	dB
PCM56P-L		−94	−80	dB
V_O = −20dB at f = 991Hz: PCM56P-K		−75	−74	dB
PCM56P-J		−75	-68	dB
PCM56P, PCM56U		−75	-68	dB
PCM56P-L		−75	−60	dB
V_O = −60dB at f = 991Hz: PCM56P-K		−35	−34	dB
PCM56P-J		−35	−28	dB
PCM56P, PCM56U		−35	−28	dB
PCM56P-L		−35	−20	dB
MONOTONICITY		15		Bits
DRIFT (0°C to +70°C)				
Total Drift[3]		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Output: 6V Step		1.5		µs
1LSB		1.0		µs
Slew Rate		12		V/µs
Current Output, 1mA Step: 10Ω to 100Ω Load		350		ns
1kΩ Load[4]		350		ns
WARM-UP TIME	1			Min
OUTPUT				
Voltage Output Configuration: Bipolar Range		±3.0		V
Output Current	±8.0			mA
Output Impedance		0.10		Ω
Short Circuit Duration				
Current Output Configuration:		Indefinite to Common		
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.2		kΩ
POWER SUPPLY REQUIREMENTS[5]				
Voltage: $+V_S$ and $+V_L$	+4.75	+5.00	+13.2	V
$−V_S$ and $−V_L$	−4.75	−5.00	−13.2	V
Supply Drain (No Load): +V ($+V_S$ and $+V_L$ = +5V)		+10.00	+17.0	mA
−V ($−V_S$ and $−V_L$ = −5V)		−25.0	−35.0	mA
+V ($+V_S$ and $+V_L$ = +12V)		+12.0		mA
−V ($−V_S$ and $−V_L$ = −12V)		−27.0		mA
Power Dissipation: V_S and V_L = ±5V		175	260	mW
V_S and V_L = ±12V		468		mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTES: (1) Logic input levels are TTL/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the V_{OUT} mode. (3) This is the combined drift error due to gain, offset, and linearity over temperature. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) All specifications assume $+V_S$ connected to $+V_L$ and $−V_S$ connected to $−V_L$. If supplies are connected separately, $−V_L$ must not be more negative than $−V_S$ supply voltage to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages .... ±16VDC
Input Logic Voltage .... −1V to +V$_S$/+V$_L$
Power Dissipation 850mW
Operating Temperature .... −25°C to +70°C
Storage Temperature .... −60°C to +100°C
Lead Temperature (soldering, 10s) .... +300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM56U	16-Pin SOIC	211
PCM56P	16-Pin Plastic DIP	180
PCM56P-J	16-Pin Plastic DIP	180
PCM56P-K	16-Pin Plastic DIP	180
PCM56P-L	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Analog Negative Supply	−V$_S$
P2	Logic Common	LOG COM
P3	Logic Positive Supply	+V$_L$
P4	No Connection	NC
P5	Clock Input	CLK
P6	Latch Enable Input	LE
P7	Serial Data Input	DATA
P8	Logic Negative Supply	−V$_L$
P9	Voltage Output	V$_{OUT}$
P10	Feedback Resistor	RF
P11	Summing Junction	SJ
P12	Analog Common	ANA COM
P13	Current Output	I$_{OUT}$
P14	MSB Adjustment Terminal	MSB ADJ
P15	MSB Trim-pot Terminal	TRIM
P16	Analog Positive Supply	+V$_S$

CONNECTION DIAGRAM

NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 6.

PCM56P/U

8.2

DIGITAL AUDIO PRODUCTS—D/A
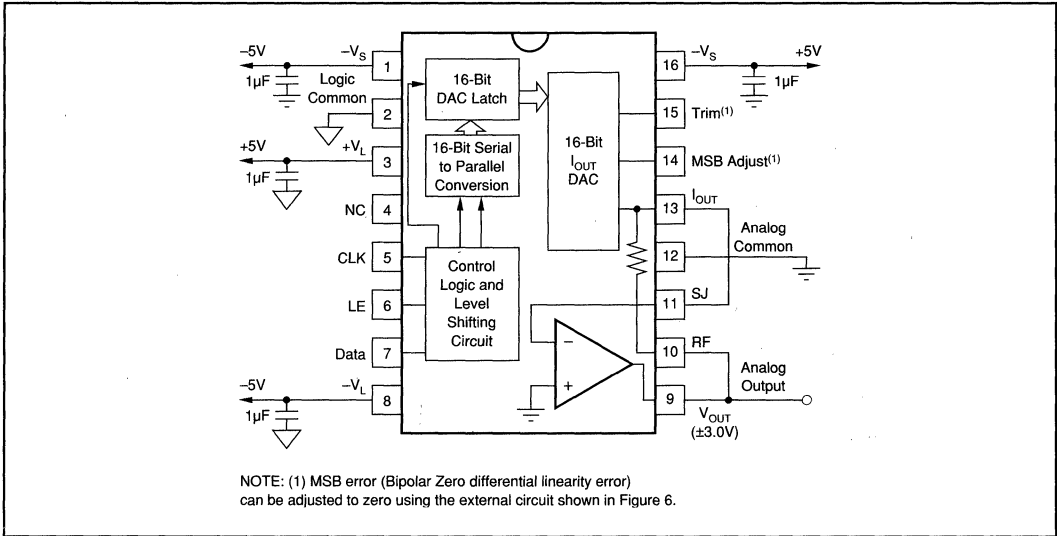
DISCUSSION OF SPECIFICATIONS

The PCM56 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM56 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

DIGITAL INPUT CODES

The PCM56 accepts serial input data (MSB first) in the Binary Two's Complement (BTC) form. Refer to Table I for input/output relationships.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
7FFF Hex	+ Full Scale	+2.999908	−0.999970
8000 Hex	− Full Scale	−3.000000	+1.000000
0000 Hex	Bipolar Zero	0.000000	0.000000
FFFF Hex	Zero −1LSB	−0.000092	+0.030500µA

TABLE I. Digital Input to Analog Output Relationship.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "on" and all other bits "off") is the deviation from 0V out and is factory-trimmed to typically ±30mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM56 is factory trimmed to typically ±0.001% of FSR. The MSB DLE is adjustable to zero using the circuit shown in Figure 6.
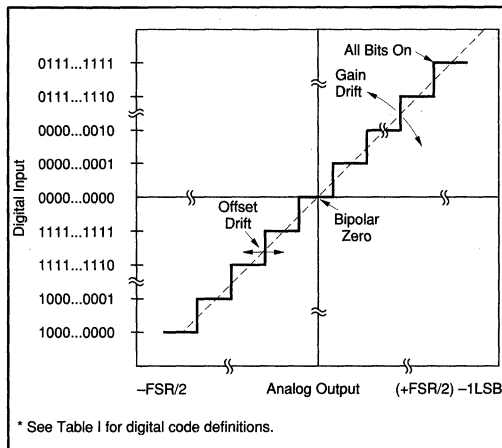
FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM56 power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR: one for a large output voltage change of 6V and one for a 1LSB change. The 1LSB change is measured at the major carry (0000 hex to ffff hex), the point at which the worst-case settling time occurs.
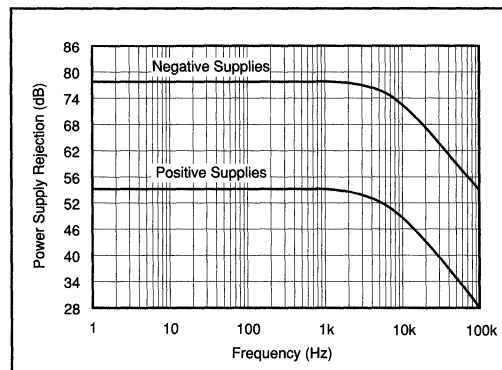
FIGURE 2. Power Supply Sensitivity.
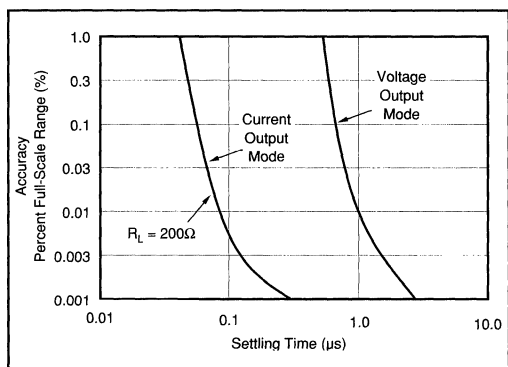
FIGURE 3. Full Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM56 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM56 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 X n, or about 96dB of a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion.

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM56 error referred to the input can be shown to be:

$$\in_{rms} = \sqrt{1/n \sum_{i=1}^{n} \left[E_L(i) + E_Q(i) \right]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM56 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as:

$$THD = \in_{rms} / E_{rms}$$

$$= \frac{\sqrt{1/n \sum_{i=1}^{n} \left[E_L(i) + E_Q(i) \right]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM56 the test period was chosen to be 22.7µs (44.1kHz), which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 991Hz and the amplitude of the input signal is 0dB, –20dB, and –60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.
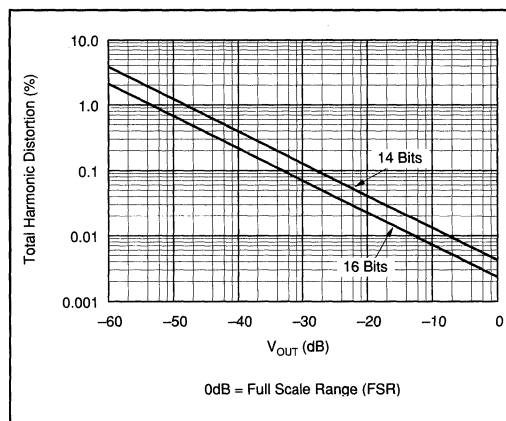
FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

PCM56P/U

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DIGITAL AUDIO PRODUCTS—D/A
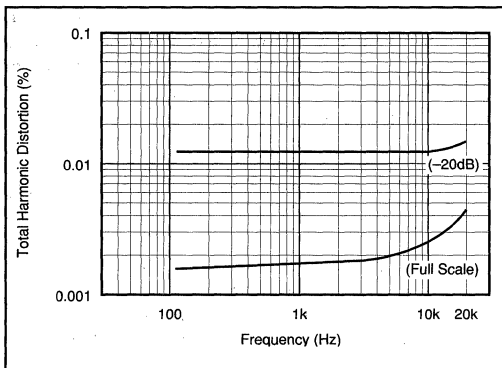
FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM56 can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6, or the PCM56 connection diagram.

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM56, select input code FFFF hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 0000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92μV more than the voltage reading of the previous code (a 1LSB step = 92μV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –80dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.
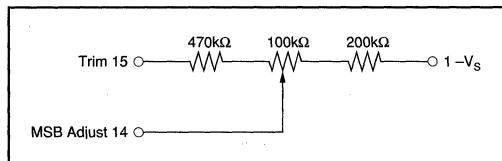
FIGURE 6. MSB Adjustment Circuit.

INPUT TIMING CONSIDERATIONS

Figure 7 and 8 refer to the input timing required to interface the inputs of PCM56 to a serial input data stream. Serial data is accepted in Binary Two's Complement (BTC) with the MSB being loaded first. Data is clocked in on positive going clock (CLK) edges and is latched into the DAC input register on negative going latch enable (LE) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are the ones that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

One requirement for clocking in all 16 bits is the necessity for a "17th" clock pulse. This automatically occurs when the clock is continuous (last bit shifts in on the first bit of the next data word). If the clock is stopped between input of 16-bit data words, the latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. This ensures that the latch is properly set up.

Figure 7 refers to the general input format required for the PCM56. Figure 8 shows the specific relationships between the various signals and their timing constraints.

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used, a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 14. If the circuit is not used, pins 14 and 15 should be left open.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination

NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 7. Input Timing Diagram.
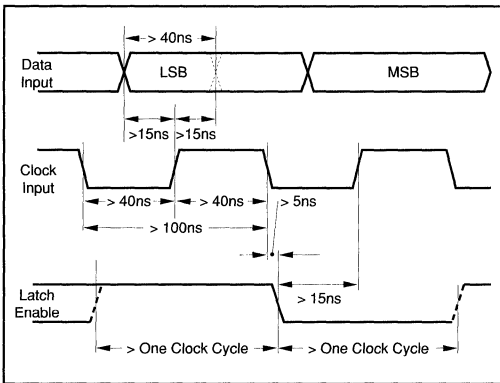
FIGURE 8. Input Timing Relationships.

of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

Figures 9 and 10 show a circuit and timing diagram for a single PCM56 used to obtain both left- and right-channel output in a typical digital audio system. The audio output of the PCM56 is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM56 is a complete D/A converter requiring no external reference or output op amp.

A sample/hold (S/H) amplifier, or "deglitcher" is required at the output of the D/A for both the left and right channel, as shown in Figure 9. The S/H amplifier for the left channel is composed of A_1, SW_1, and associated circuitry. A_1 is used as an integrator to hold the analog voltage in C_1. Since the

source and drain of the FET switch operate at a virtual ground when "C" and "B" are connected in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

Figure 10 shows the deglitcher controls for both left and right channels which are produced by timing control logic. A delay of 1.5μs (tω) is provided to allow the output of the PCM56 to settle within a small error band around its final value before connecting it to the channel output. Due to the fast settling time of the PCM56 it is possible to minimize the delay between the left- and right-channel outputs when using a single D/A converter for both channels. This is important because the right- and left-channel data are recorded in-phase and the use of the slower D/A converter would result in significant phase error at higher frequencies.

The obvious solution to the phase shift problem in a two-channel system would be to use two D/A converters (one per channel) and time the outputs to change simultaneously. Figure 11 shows a block diagram of the final test circuitry used for PCM56. It should be noted that no deglitching circuitry is required on the DAC output to meet specified THD performance. This means that when one PCM56 is used per channel, the need for all the sample/hold and controls circuitry associated with a single DAC (two-channel) design is effectively eliminated. The PCM56 is tested to meet its THD specifications without the need for output deglitching.

A low-pass filter is required after the PCM56 to remove all unwanted frequency components caused by the sampling frequency as well as those resulting from the discrete nature of the D/A output. This filter must have a flat frequency response over the entire audio band (0-20kHz) and a very high attenuation above 20kHz.

Most previous digital audio circuits used a higher order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristic transients contained in music.

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DIGITAL AUDIO PRODUCTS—D/A

SECOND GENERATION SYSTEMS

One method of avoiding the problems associated with a higher order analog filter would be to use digital filter oversampling techniques. Oversampling by a factor of two would move the sampling frequency (88.2kHz) out to a point where only a simple low-order phase-linear analog filter is required after the deglitcher output to remove unwanted intermodulation products. In a digital compact disc application, various VLSI chips perform the functions of error detection/correction, digital filtering, and formatting of the digital information to provide the clock, latch enable, and serial input to the PCM56. These VLSI chips are available from several sources (Sony, Yamaha, Signetics, etc.) and are specifically optimized for digital audio applications.

Oversampled circuitry requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more (for each output channel). A single PCM56 can provide two-channel oversampling at a 4X rate (176.4kHz/channel) and still remain well within the settling time requirements for maintaining specified THD performance. This would reduce the complexities of the analog filter even further from that used in 2X oversampling circuitry.

NOTE: (1) 1 OPA101AM or 1/4 OPA404KP or 1 OPA606KP or OPA2604.
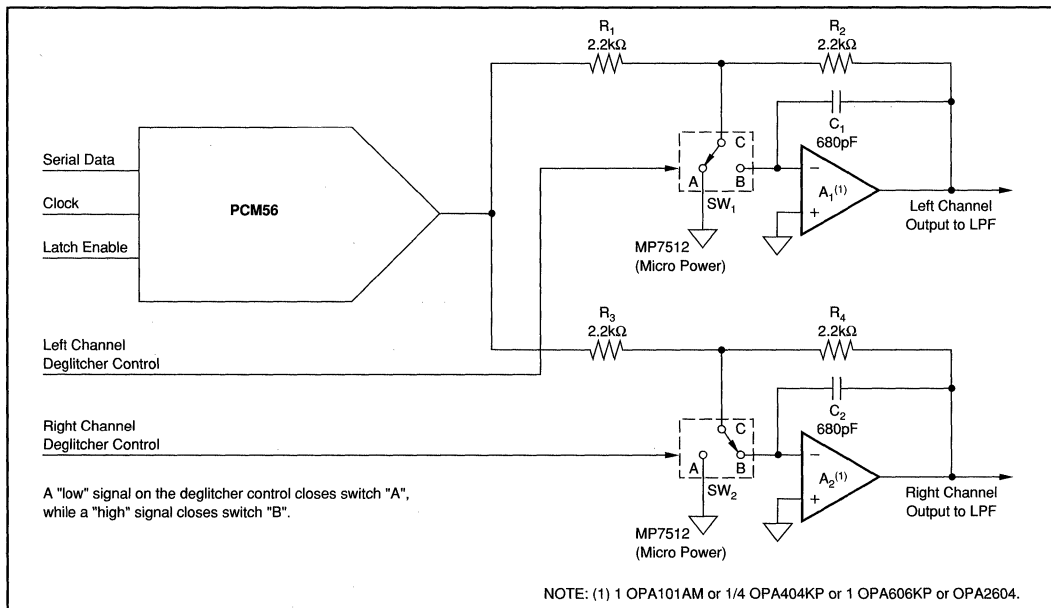
FIGURE 9. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

The deglitcher control signals by timing control logic. The fast settling time of the PCM56 makes it possible to minimize the delay between left and right channels to about 4.5µs, which reduces phase error at the higher audio frequencies.

FIGURE 10. Timing Diagram for the Deglitcher Control Signals.
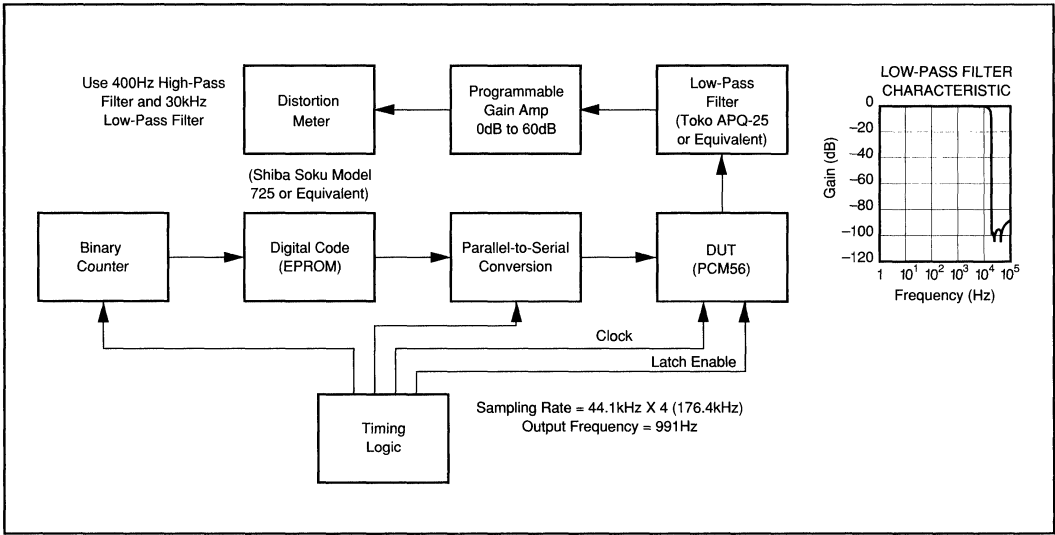
FIGURE 11. Block Diagram of Distortion Test Circuit.

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DIGITAL AUDIO PRODUCTS—D/A

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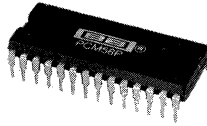
PCM58P

Precision, 18-Bit Monolithic Audio
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **18-BIT MONOLITHIC AUDIO D/A CONVERTER**
- **VERY LOW MAX THD+N: –96dB Without External Adjustment; PCM58P-K**
- **SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P**
- **VERY FAST SETTLING, GLITCH-FREE CURRENT OUTPUT (200ns)**
- **LOW-NOISE SCHMITT TRIGGER LOGIC INPUT CIRCUITRY**
- **COMPLETE WITH REFERENCE**
- **RELIABLE PLASTIC 28-PIN DIP PACKAGE**

DESCRIPTION

The PCM58P is a complete, precision 18-bit digital-to-analog converter with ultra-low distortion over a very wide frequency range. The latched serial input data format of the PCM58P is totally based on the widely successful 16-bit PCM56P format (with the addition of two more data bits). The PCM58P features a very low noise and fast settling current output.

The PCM58P comes in a 28-pin plastic DIP package. A provision is made for external adjustment of the four MSBs to further improve the PCM58P's specifications, if desired. Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.

PDS-868A

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SPECIFICATIONS

ELECTRICAL

All Specifications at 25°C, and ±V$_{CC}$ = +5.0V and −12.0V unless otherwise noted.

PARAMETER	CONDITIONS	PCM58P /P,J/P,K			UNITS
		MIN	TYP	MAX	
RESOLUTION				18	**BITS**
DYNAMIC RANGE			108		**dB**
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V$_{IH}$		+2.0		+V$_{CC}$	V
V$_{IL}$		0.0		0.8	V
I$_{IH}$	V$_{IH}$ = +2.7V			+1.0	μA
I$_{IL}$	V$_{IL}$ = +0.4V			−50	μA
Data Format			Serial BTC[1]		
Input Clock Frequency		16.9	20		MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]	Without MSB Adjustments				
PCM58P:					
f = 991Hz (0dB)[3]	f$_S$ = 176.4kHz[4]		−94	−92	dB
f = 991Hz (−20dB)	f$_S$ = 176.4kHz		−74	−72	dB
f = 991Hz (−60dB)	f$_S$ = 176.4kHz		−40	−34	dB
PCM58P-J:					
f = 991Hz (0dB)	f$_S$ = 176.4kHz		−96	−94	dB
f = 991Hz (−20dB)	f$_S$ = 176.4kHz		−80	−74	dB
f = 991Hz (−60dB)	f$_S$ = 176.4kHz		−40	−34	dB
PCM58P-K:					
f = 991Hz (0dB)	f$_S$ = 176.4kHz		−100	−96	dB
f = 991Hz (−20dB)	f$_S$ = 176.4kHz		−82	−80	dB
f = 991Hz (−60dB)	f$_S$ = 176.4kHz		−42	−40	dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20kHz at BPZ[7]		+126		dB
POWER SUPPLY REJECTION			+72		dB
ANALOG OUTPUT					
Output Range		±0.98	±1.0	±1.02	mA
Output Impedance			1.2		kΩ
Internal Feedback			3		kΩ
Settling Time	1mA Step		200		ns
Glitch Energy		Meets all THD+N Specs Without External Deglitching			
POWER SUPPLY REQUIREMENTS					
+V$_{CC}$ Supply Voltage		+4.75	+5.00	+5.50	V
−V$_{CC}$ Supply Voltage		−10.8	−12.0	−13.2	V
Supply Current +I$_{CC}$	+V$_{CC}$ = +5.0V		+10		mA
−I$_{CC}$	−V$_{CC}$ = −12.0V		−30		mA
Power Dissipation			410		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		−30		+70	°C
Storage		−60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 10kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

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PCM58P

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DIGITAL AUDIO PRODUCTS—D/A

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Decoupling Capacitor	CAP
P2	+Vcc Voltage Supply	$+V_{CC}$
P3	Decoupling Capacitor	CAP
P4	Decoupling Capacitor	CAP
P5	Bipolar Offset Point	BPO
P6	Current DAC I_{OUT}	I_{OUT}
P7	Feedback Resistor	R_{F1}
P8	Analog Common	ACOM
P9	$-V_{CC}$ Voltage Supply	$-V_{CC}$
P10	Feedback Resistor	R_{F2}
P11	Digital Common	DCOM
P12	No Connection	NC
P13	$+V_{CC}$ Voltage Supply	$+V_{CC}$
P14	No Connection	NC
P15	Decoupling Capacitor	CAP
P16	Clock	CLK
P17	DAC Latch Enable	LE
P18	No Connection	NC
P19	Data Input	DATA
P20	$-V_{CC}$ Voltage Supply	$-V_{CC}$
P21	No Connection	NC
P22	No Connection	NC
P23	No Connection	NC
P24	Bit 4 Adjust	B4 ADJ
P25	Bit 3 Adjust	B3 ADJ
P26	Bit 2 Adjust	B2 ADJ
P27	Bit 1 (MSB) Adjust	B1 ADJ
P28	Bit Adjust V_{POT}	V_{POT}

ORDERING INFORMATION

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$ Supply Voltages .... +6V; −16V
Input Logic Voltage .... −1V to $+V_{CC}$
Storage Temperature .... −60°C to +100°C
Lead Temperature (soldering, 10s) .... +300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM58P	28-Pin Plastic DIP	215
PCM58P, J	28-Pin Plastic DIP	215
PCM58P, K	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.
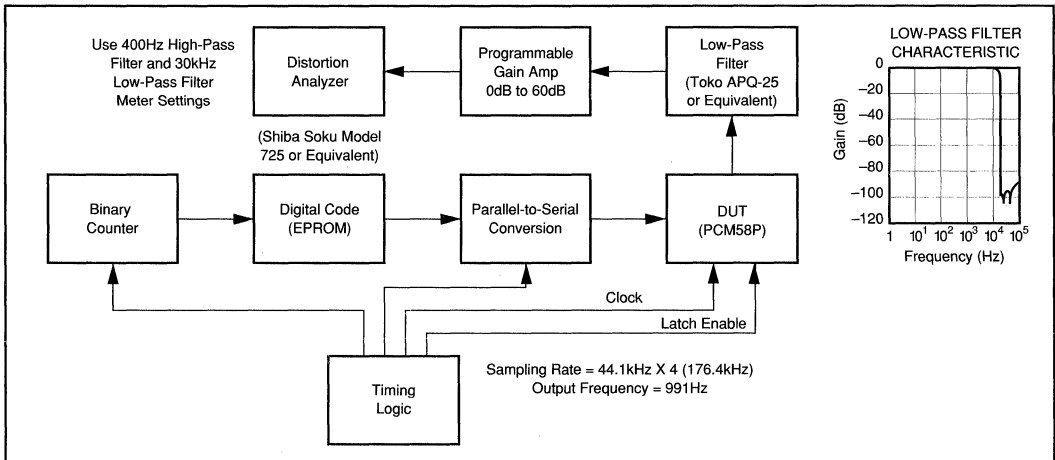
FIGURE 1.   PCM58P Production THD+N Test Setup.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM58P is total harmonic distortion plus noise. Digital data words are read into the PCM58P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz such that a sinewave output of 991Hz is realized. For production testing, the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

In terms of signal measurement, THD+N is the ratio of Distortion$_{RMS}$ + Noise$_{RMS}$ / Signal$_{RMS}$ expressed in dB. For the PCM58P, THD+N is 100% tested at three different output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. This means the PCM58P even meets its –60dB THD+N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM58P, the extremely low THD+N performance is typically indicative of 15-bit to 16-bit integral linearity in the DAC depending on the grade specified. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement. The idle channel SNR for the PCM58P is typically greater than +126dB, making it ideal for low-noise applications.

OFFSET, GAIN, AND TEMPERATURE DRIFT

Although the PCM58P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift and offset drift.

TIMING CONSIDERATIONS

The PCM58P accepts TTL-compatible logic input levels. Noise immunity is enhanced by the use of Schmitt trigger input architectures on all input signal lines. The data format of the PCM58P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table I describes the exact input data to voltage output coding relationship. Any number of bits can precede the 18 bits to be loaded as only the last 18 will be transferred to the parallel DAC register after LE (P17; latch enable) has gone low.

The individual DAC serial input data bit shifts transfer are triggered on positive CLK edges. The serial to parallel data transfer to the DAC occurs on the falling edge of LE (P17). Refer to Figure 2 for graphical relationships of these signals.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9mHz for the PCM58P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16X oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9mHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
3FFFF Hex	+FS	+2.9999943	–0.9999981
20000 Hex	BPZ	0.0000000	0.0000000
1FFFF Hex	BPZ – 1LSB	–0.0000057	+0.0000019
00000 Hex	–FS	–3.0000000	+1.0000000

TABLE I. PCM60P Input/Output Relationships.

P16 (Clock)

P18 (Data)   1 MSB 2 3 4   10 11 12 13 14 15 16 17 18 LSB 1

P17 (Latch Enable)

NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 2. PCM58P Timing Diagram.

PCM58P

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DIGITAL AUDIO PRODUCTS—D/A

"STOPPED-CLOCK" OPERATION

The PCM58P is normally operated with a continuous clock input signal. If the clock is to be stopped in between input data words, the last 18-bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until LE (latch enable) goes low. If the clock input (P16, CLK) is stopped between data words, LE (P17) must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In either case, the setup and hold times for DATA and LE must still be observed as shown in Figure 3.

INSTALLATION

Refer to Figure 4 for proper connection of the PCM58P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P7 and P10) should be connected to ACOM (P8) if not used. The PCM58P requires only a +5V and –12V supply. It is very important that these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors shown in Figure 4 should be used, regardless of how good the supplies are to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM58P as possible.
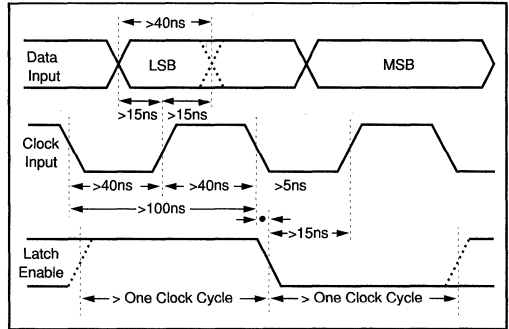
FIGURE 3. PCM58P Setup and Hold Timing Diagram.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, other various decoupling capacitors are required around the supply and reference points with no special tolerances being required. Placement of all capacitors should be as close to the appropriate pins of the PCM58P as possible to reduce noise pickup from surrounding circuitry.
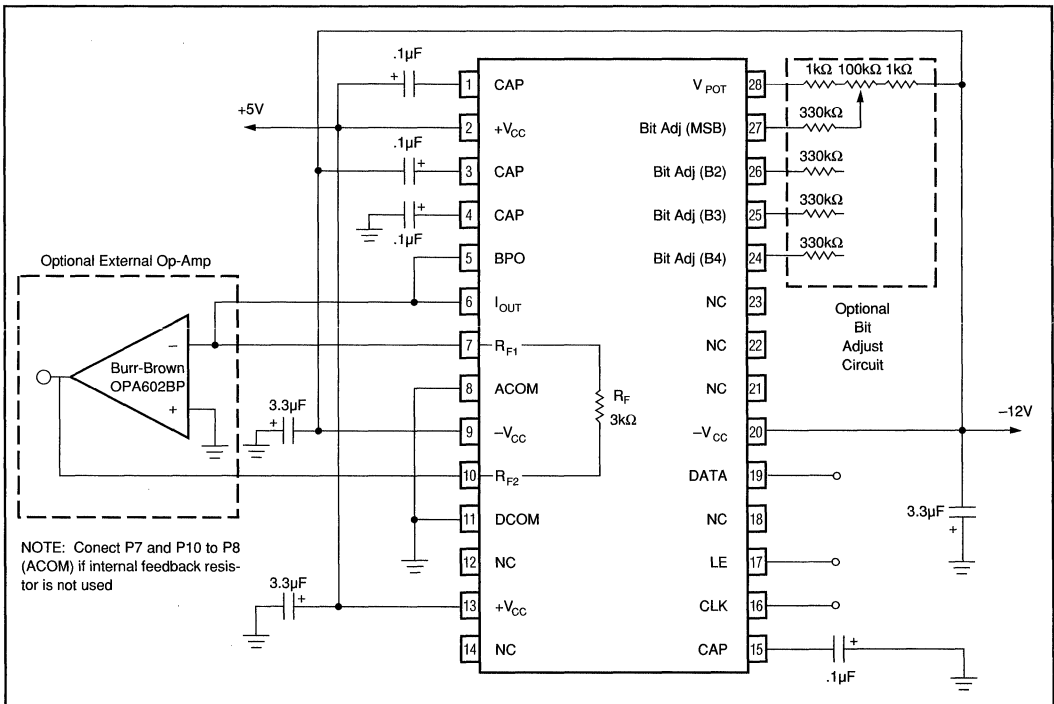
FIGURE 4. PCM58P Connection Diagram.

MSB ADJUSTMENT CIRCUITRY

With the optional bit adjustment circuitry shown in Figure 4, even greater performance can be realized by reducing the first four major bit carry output errors to zero. The most important adjustment for low level outputs would be the step between BPZ (bipolar zero; MSB on, all other bits off) and the code, which is one LSB less than BPZ (MSB off, all other bits on), since every crossing of zero would go through this bipolar major carry point. This MSB bit adjustment would be made by outputing a very low level signal sine wave and calibrating the 100kΩ potentiometer circuit connected to P28 and P27 while monitoring the THD+N of the PCM58P until peak performance is observed.

Bits 2 through 4 can also be adjusted if desired to obtain optimum full-scale output THD+N performance. An additional 100kΩ potentiometer adjustment circuit is required for every additional bit to be adjusted. If bit adjustment is not performed, the respective pins on the PCM58P should be left open.

Once bit adjustment is performed, the reference voltage at VPOT (P28) will track the internal reference, insuring that the THD+N performance of the PCM58P will remain unaffected by external temperature changes.

PCM58P

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DIGITAL AUDIO PRODUCTS—D/A

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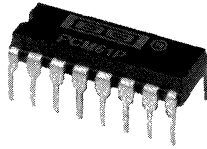
PCM61P

Serial Input 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **18-BIT MONOLITHIC AUDIO D/A CONVERTER**

● **LOW MAX THD + N: –92dB Without External Adjust**

● **100% PIN COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P**

● **GLITCH FREE OUTPUT OF ±3V OR ±1mA**

● **CAPABLE OF 8X OVERSAMPLING RATE IN V_{OUT} MODE**

● **COMPLETE WITH INTERNAL REFERENCE AND OUTPUT OP AMP**

● **RELIABLE PLASTIC 16-PIN DIP PACKAGE**

DESCRIPTION

The PCM61P is an 18-bit totally pin compatible performance replacement for the popular 16-bit PCM56P. With the addition of two extra bits, lower max THD + N (–92dB; PCM61P-K) can be achieved in audio applications already using the PCM56P. The PCM61P is complete with internal reference and output op amp and requires no external parts to function as an 18-bit DAC. The PCM61P is capable of an 8-times oversampling rate (single channel) and meets all of its specifications without an external output deglitcher.

The PCM61P comes in a small, reliable 16-pin plastic DIP package that has passed operating life tests under simultaneous high temperature, high humidity and high pressure testing.

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, and +V$_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM61P/P, J/P, K			UNITS
		MIN	TYP	MAX	
RESOLUTION				18	Bits
DYNAMIC RANGE			108		dB
DIGITAL INPUT					
Logic Family		TTL/CMOS Compatible			
Logic Level: V$_{IH}$		+2		+V$_{CC}$	V
V$_{IL}$		0		+0.8	V
I$_{IH}$	V$_{IH}$ = +2.7V			+1	μA
I$_{IL}$	V$_{IL}$ = +0.4V			−50	μA
Data Format		Serial BTC[1]			
Input Clock Frequency				16.9	MHz
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion + N[2]	Without MSB Adjustments				
PCM61P					
f = 991Hz (0dB)[3]	f$_S$ = 176.4kHz[4]		−88	−82	dB
f = 991Hz (−20dB)	f$_S$ = 176.4kHz		−74	−68	dB
f = 991Hz (−60dB)	f$_S$ = 176.4kHz		−34	−28	dB
PCM61P-J					
f = 991Hz (0dB)	f$_S$ = 176.4kHz		−94	−88	dB
f = 991Hz (−20dB)	f$_S$ = 176.4kHz		−76	−74	dB
f = 991Hz (−60dB)	f$_S$ = 176.4kHz		−36	−34	dB
PCM61P-K					
f = 991Hz (0dB)	f$_S$ = 176.4kHz		−98	−92	dB
f = 991Hz (−20dB)	f$_S$ = 176.4kHz		−80	−74	dB
f = 991Hz (−60dB)	f$_S$ = 176.4kHz		−40	−34	dB
IDLE CHANNEL SNR	20Hz to 20kHz at BPZ[5]		112		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		%
Total Drift[6]	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±4		ppm of FSR/°C
Warm-up Time		1			Minute
MONOTONICITY			16		Bits
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Current		±8			mA
Output Impedance			0.1		Ω
Current: Output Range	±30%		±1		mA
Output Impedance	±30%		1.2		kΩ
SETTLING TIME	To ±0.006% of FSR				
Voltage: 6V Step			1.5		μs
1 LSB			1.0		μs
Slew Rate			12		V/μs
Current: 1mA Step	10Ω to 100Ω Load		250		ns
1mA Step	1kΩ Load		350		ns
Glitch Energy	Meets all THD + N specs without external deglitching				
POWER SUPPLY REQUIREMENTS[7]					
±V$_{CC}$ Supply Voltage		±4.75	±5	±13.2	V
Supply Current: +I$_{CC}$	+V$_{CC}$ = +5V		+10	+17	mA
+I$_{CC}$	+V$_{CC}$ = +12V		+12		mA
−I$_{CC}$	−V$_{CC}$ = −5V		−25	−35	mA
−I$_{CC}$	−V$_{CC}$ = −12V		−27		mA
Power Dissipation	±V$_{CC}$ = ±5V		175	260	mW
	±V$_{CC}$ = ±12V		475		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		−30		+70	°C
Storage		−60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$)/Signal$_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Bipolar zero, using A-weighted filter. (6) This is the combined drift error due to gain, offset, and linearity over temperature. (7) All positive and all negative supply pins must be tied together respectively.

PCM61P

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DIGITAL AUDIO PRODUCTS—D/A

PIN ASSIGNMENTS

PIN	FUNCTION	DESCRIPTION
1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistance
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	-1V to $V_S/+V_L$
Power Dissipation	850mW
Operating Temperature Range	$-25°$C to $+70°$C
Storage Temperature Range	$-60°$C to $+100°$C
Lead Temperature (soldering, 10s)	$+300°$C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM61P-P	16-Pin Plastic DIP	180
PCM61P-J	16-Pin Plastic DIP	180
PCM61P-K	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

CONNECTION DIAGRAM

NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 4.
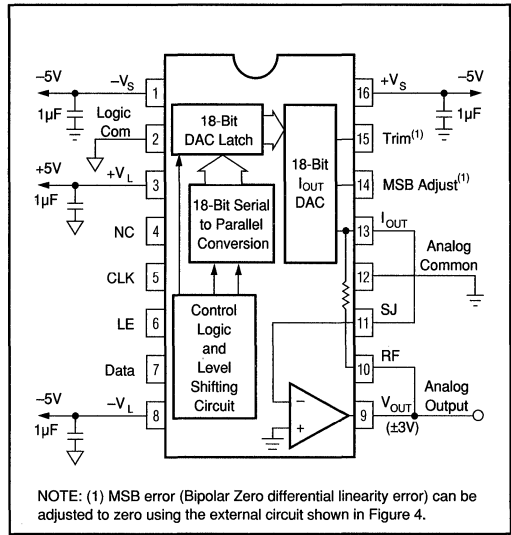
DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+FS	–0.99999237	+2.99997711
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	+0.00000763	–0.00002289
20000 Hex	–FS	+1.00000000	–3.00000000

TABLE I. PCM61P Input/Output Relationships.

NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream.
(2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 1. PCM61P Timing Diagram.

FIGURE 2. PCM61P Setup and Hold Timing Diagram.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9MHz for the PCM61P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16 x oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.
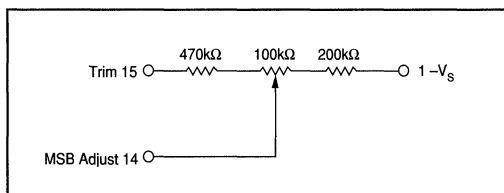
FIGURE 3. MSB Adjust Circuit.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM61P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 3 or the PCM61P connection diagram.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point, which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM61P, select input code 3FFFF hexadecimal (all bits on except the MSB). Measure the output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 00000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the output read 22.9µV more than the voltage reading of the previous code (a 1LSB step = 22.9µV). A much simpler method is to dynamically adjust the DLE at BPZ. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –60dB level sinusoidal output, then adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

PCM61P

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DIGITAL AUDIO PRODUCTS—D/A

BURR - BROWN®
BB

PCM63P

**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

Colinear ™ 20-Bit Monolithic Audio
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ● **COLINEAR 20-BIT AUDIO DAC**
- ● **NEAR-IDEAL LOW LEVEL OPERATION**
- ● **GLITCH-FREE OUTPUT**
- ● **ULTRA LOW –96dB max THD + N
  (Without External Adjustment)**
- ● **116dB SNR min (A-Weight Method)**
- ● **INDUSTRY STD SERIAL INPUT FORMAT**
- ● **FAST (200ns) CURRENT OUTPUT
  (±2mA; ±2% max)**
- ● **CAPABLE OF 16x OVERSAMPLING**
- ● **COMPLETE WITH REFERENCE**

DESCRIPTION

The PCM63P is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB max with a full scale output; PCM63P-K). Incorporated into the PCM63P is a unique *Colinear* dual-DAC per channel architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM63P also features a very low noise (116dB max SNR; A-weighted method) and fast settling current output (200ns typ, 2mA step) which is capable of 16-times oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.

Colinear ™, Burr-Brown Corp.

PDS-1083D

BURR - BROWN®
BB

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C and $\pm V_A$ and $\pm V_D = \pm 5V$, unless otherwise noted.

PARAMETER	CONDITIONS	PCM63P, PCM63P,J, PCM63P,K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale					
PCM63P		96	100		dB
PCM63P-J		100	104		dB
PCM63P-K		104	108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2		$+V_D$	V
V_{IL}		0		0.8	V
I_{IH}	$V_{IH} = +2.7V$			+1	μA
I_{IL}	$V_{IL} = +0.4V$			–50	μA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			30	25	MHz
TOTAL HARMONIC DISTORTION + N[2], Without Adjustments					
PCM63P					
f = 991Hz (0dB)[3]	$f_S = 352.8kHz$[4]		–92	–88	dB
f = 991Hz (–20dB)	$f_S = 352.8kHz$		–80	–74	dB
f = 991Hz (–60dB)	$f_S = 352.8kHz$		–40	–36	dB
PCM63P-J					
f = 991Hz (0dB)	$f_S = 352.8kHz$		–96	–92	dB
f = 991Hz (–20dB)	$f_S = 352.8kHz$		–82	–76	dB
f = 991Hz (–60dB)	$f_S = 352.8kHz$		–44	–40	dB
PCM63P-K					
f = 991Hz (0dB)	$f_S = 352.8kHz$		–100	–96	dB
f = 991Hz (–20dB)	$f_S = 352.8kHz$		–88	–82	dB
f = 991Hz (–60dB)	$f_S = 352.8kHz$		–48	–44	dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±0.3	±1	dB
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20kHz at BPZ[7]	+116	+120		dB
POWER SUPPLY REJECTION			+86		dB
ANALOG OUTPUT					
Output Range		±1.96	±2.00	±2.04	mA
Output Impedance			670		Ω
Internal $R_{FEEDBACK}$			1.5		kΩ
Settling Time	2mA Step		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
$\pm V_A$, $\pm V_D$ Supply Voltage Range		±4.50	±5	±5.50	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D = +5V$		10	15	mA
$-I_A$, $-I_D$ Combined Supply Current	$-V_A$, $-V_D = -5V$		–35	–45	mA
Power Dissipation	$\pm V_A$, $\pm V_D = \pm 5V$		225	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency (signal level). (4) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 1.5kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

PCM63P

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DIGITAL AUDIO PRODUCTS—D/A

DICE INFORMATION

PCM63P DIE TOPOGRAPHY

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	229 x 161 ±5	5.82 x 4.09 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PAD	FUNCTION
1	CAP
2	$+V_A$
3	CAP
4	CAP
5	BPO
6	I_{OUT}
7	ACOM
8	NC
9	RF_1
10	RF_2
11	$-V_D$
12	DCOM
13	$+V_D$
14	NC
15	NC
16	NC
17	NC
18	CLK
19	NC
20	LE
21	DATA
22	NC
23	UB2 Adj
24	LB2 Adj
25	V_{POT}
26	NC
27	NC
28	$-V_A$

NC: No Connection.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Servo Amp Decoupling Capacitor	CAP
P2	+5V Analog Supply Voltage	$+V_A$
P3	Reference Decoupling Capacitor	CAP
P4	Offset Decoupling Capacitor	CAP
P5	Bipolar Offset Current Output (+2mA)	BPO
P6	DAC Current Output (0 to –4mA)	I_{OUT}
P7	Analog Common Connection	ACOM
P8	No Connection	NC
P9	Feedback Resistor Connection (1.5kΩ)	RF_1
P10	Feedback Resistor Connection (1.5kΩ)	RF_2
P11	–5V Digital Supply Voltage	$-V_D$
P12	Digital Common Connection	DCOM
P13	+5V Digital Voltage Supply	$+V_D$
P14	No Connection	NC
P15	No Connection	NC
P16	No Connection	NC
P17	No Connection	NC
P18	DAC Data Clock Input	CLK
P19	No Connection	NC
P20	DAC Data Latch Enable	LE
P21	DAC Data Input	DATA
P22	No Connection	NC
P23	Optional Upper DAC Bit-2 Adjust (–4.29V)*	UB2 Adj
P24	Optional Lower DAC Bit-2 Adjust (–4.29V)*	LB2 Adj
P25	Bit Adjust Reference Voltage Tap (–3.52V)*	V_{POT}
P26	No Connection	NC
P27	No Connection	NC
P28	–5V Analog Supply Voltage	$-V_A$

*Nominal voltages at these nodes assuming $\pm V_A$; $\pm V_D = \pm 5V$.

ABSOLUTE MAXIMUM RATINGS

$+V_A$, $+V_D$ to ACOM/DCOM .... 0V to +8V
$-V_A$, $-V_D$ to ACOM/DCOM .... 0V to –8V
$-V_A$, $-V_D$ to $+V_A$, $+V_D$ .... 0V to +16V
ACOM to DCOM .... ±0.5V
Digital Inputs (pins 18, 20, 21) to DCOM .... –1V to $+V_D$
Power Dissipation 500mW
Lead Temperature, (soldering, 10s) .... +300°C
Max Junction Temperature .... 165°C
Thermal Resistance, θ_{JA} .... 70°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM63P	28-Pin Plastic DIP	215
PCM63P, J	28-Pin Plastic DIP	215
PCM63P, K	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX THD + N, AT 0dB
PCM63P	28-Pin Plastic DIP	0°C to +70°C	–88dB
PCM63P, J	28-Pin Plastic DIP	0°C to +70°C	–92dB
PCM63P, K	28-Pin Plastic DIP	0°C to +70°C	–96dB

TYPICAL PERFORMANCE CURVES

All specifications at 25°C and $\pm V_A$ and $\pm V_D = \pm 5.0V$, unless otherwise noted.

THD + N vs FREQUENCY

-60dB

-40dB

-20dB

0dB

THD +N (dB)

Output Frequency (Hz)

16-BIT LEVEL LINEARITY
(Dithered Fade to Noise)

Deviation from Ideal Level (dB)

Output Signal Level (dB)

16-BIT MONOTONICITY

Output Voltage (mV)

8.83ms/div

-90dB SIGNAL SPECTRUM
(100Hz Bandwidth)

Power Spectrum (dB)

Frequency (Hz)

-90dB SIGNAL
(10Hz to 20kHz Bandwidth)

50µV   200µS

Output Level (µV)

Time (µs)

-110dB SIGNAL
(10Hz to 20kHz Bandwidth)

10µV   200µS

Output Level (µV)

Time (µs)

PCM63P

8.2
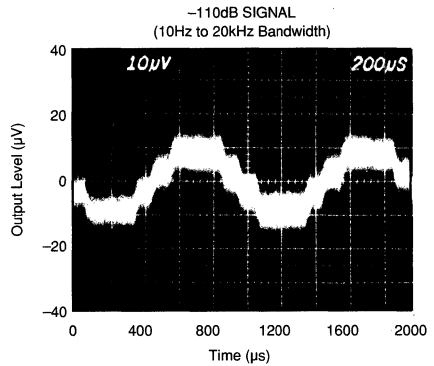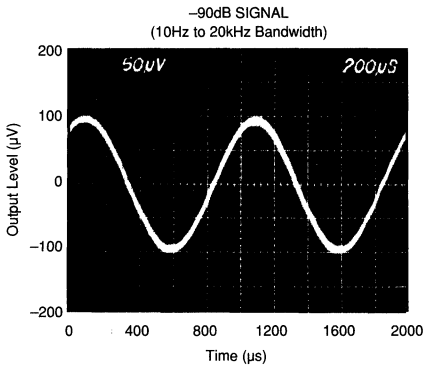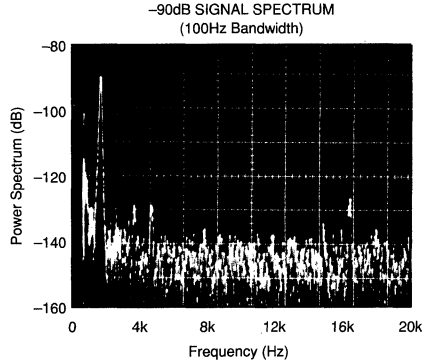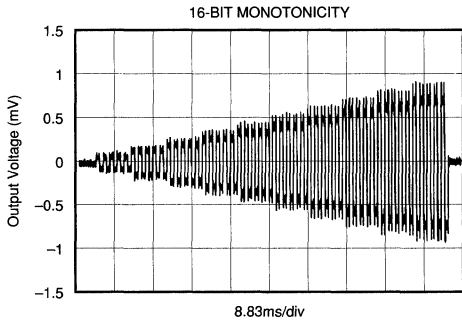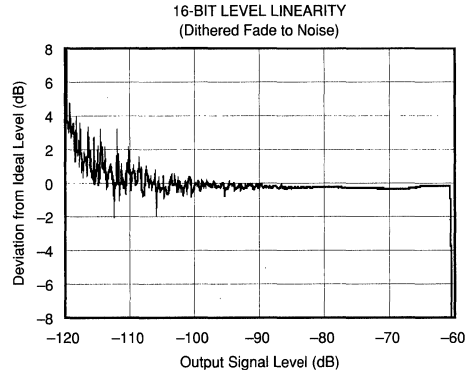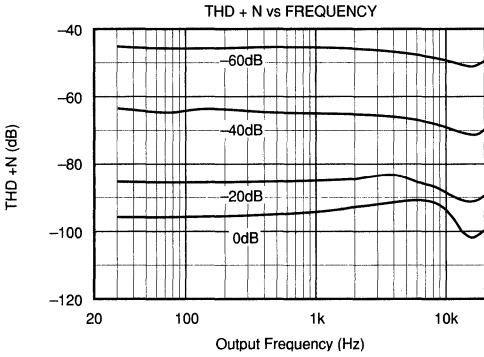
DIGITAL AUDIO PRODUCTS—D/A

THEORY OF OPERATION

DUAL-DAC *COLINEAR* ARCHITECTURE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high oversampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DACs). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM63 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference and a common R-2R ladder to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or dual-DAC *Colinear* approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM63P is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table I shows the conversion made by the internal logic of the PCM63P from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM63P in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specification for the PCM63P is total harmonic distortion plus noise (THD + N). Digital data words are read into the PCM63P at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to an I to V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer. Figure 1 shows a block diagram of the production THD + N test setup.

For the audio bandwidth, THD + N of the PCM63P is essentially flat for all frequencies. The typical performance curve, "THD + N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low-level signal performance of the dual-DAC *Colinear* architecture of the PCM63P.

In terms of signal measurement, THD + N is the ratio of $\text{Distortion}_{RMS} + \text{Noise}_{RMS} / \text{Signal}_{RMS}$ expressed in dB. For the PCM63P, THD + N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD + N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111 + 1LSB*	111...111
+Full Scale – 1LSB	011...110	111...111 + 1LSB*	111...110
Bipolar Zero + 2LSB	000...010	111...111 + 1LSB*	000...010
Bipolar Zero + 1LSB	000...001	111...111 + 1LSB*	000...001
Bipolar Zero	000...000	111...111 + 1LSB*	000...000
Bipolar Zero – 1LSB	111...111	111...111	000...000
Bipolar Zero – 2LSB	111...110	111...110	000...000
–Full Scale + 1LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

*The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to *Colinear* Conversion Chart.
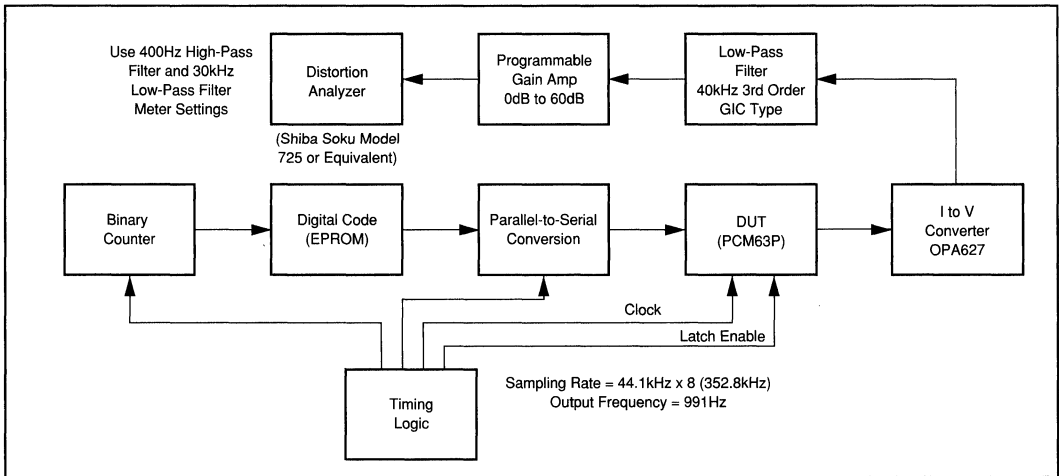
FIGURE 1. Production THD + N Test Setup.

Colinear architecture of the PCM63P, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM63P at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM63P at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal. This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM63P's **Colinear** DAC circuitry.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased from –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-Bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM63P tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATIONS

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM63P is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique dual-DAC **Colinear** architecture of the PCM63P, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-Bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM63P, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bitstream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM63P, the extremely low THD + N performance is typically indicative of 16-bit to 17-bit integral linearity in the DAC, depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

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DIGITAL AUDIO PRODUCTS—D/A

Offset, Gain, And Temperature Drift

Although the PCM63P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM63P accepts TTL compatible logic input levels. Noise immunity is enhanced by the use of differential current mode logic input architectures on all input signal lines. The data format of the PCM63P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after LE (P20, Latch Enable) has gone low.

All DAC serial input data (P21, DATA) bit transfers are triggered on positive clock (P18, CLK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable (P20, LE). The change in the output of the DAC coincides with the falling edge of Latch Enable (P20, LE). Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM63P is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X oversampling) the standard audio word bit length of 24 bits (44.1kHz X 16 X 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The maximum clock rate of 25MHz is guaranteed, but is not 100% final tested. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM63P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable (LE, P20) goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.
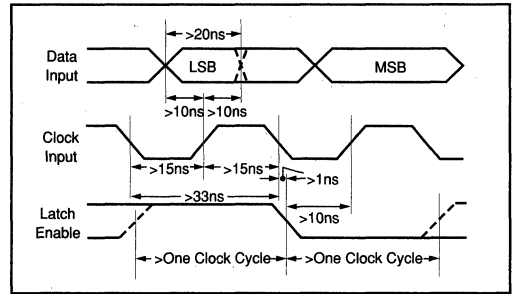
FIGURE 3. Setup and Hold Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT	VOLTAGE OUTPUT (With External Op Amp)
1,048,576LSBs	Full Scale Range	4.00000000mA	6.00000000V
1LSB	NA	3.81469727nA	5.72204590µV
7FFFF$_{HEX}$	+Full Scale	−1.99999619mA	+2.99999428V
00000$_{HEX}$	Bipolar Zero	0.00000000mA	0.00000000V
FFFFF$_{HEX}$	Bipolar Zero − 1LSB	+0.00000381mA	−0.00000572V
80000$_{HEX}$	−Full Scale	+2.00000000mA	−3.00000000V

TABLE II. Digital Input/Output Relationships.

NOTES: (1) If clock is stopped between input of 20-bit data words, Latch Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I$_{OUT}$ changes on negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

INSTALLATION

POWER SUPPLIES

Refer to Figure 4 for proper connection of the PCM63P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P9 and P10) should be left open if not used. The PCM63P only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in Figure 4, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM63P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM63P as possible to reduce noise pickup from surrounding circuitry.

MSB ADJUSTMENT CIRCUITRY

Near optimum performance can be maintained at all signal levels without using the optional MSB adjust circuitry of the PCM63P shown in Figure 5. Adjustability is provided for those cases where slightly better full-scale THD + N is

desired. Use of the MSB adjustments will only affect larger dynamic signals (between 0dB and –6dB). This improvement comes from bettering the gain match between the upper and lower DACs at these signal levels. The change is realized by small adjustments in the bit-2 weights of each DAC. Great care should be taken, however, as improper adjustment will easily result in degraded performance.

In theory, the adjustments would seem very simple to perform, but in practice they are actually quite complex. The first step in the theoretical procedure would involve making each bit-2 weight ideal in relation to its code minus one value (adjusting each potentiometer for zero differential nonlinearity error at the bit-2 major carries). This would be the starting point of each 100kΩ potentiometer for the next adjustment. Then, each potentiometer would be adjusted equally, in opposite directions, to achieve the lowest full-scale THD + N possible (reversing the direction of rotation
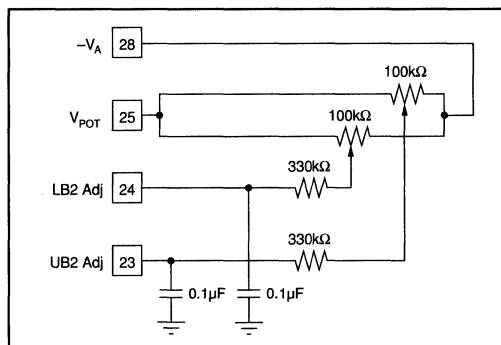
FIGURE 5. Optional Bit-2 Adjustment Circuitry.
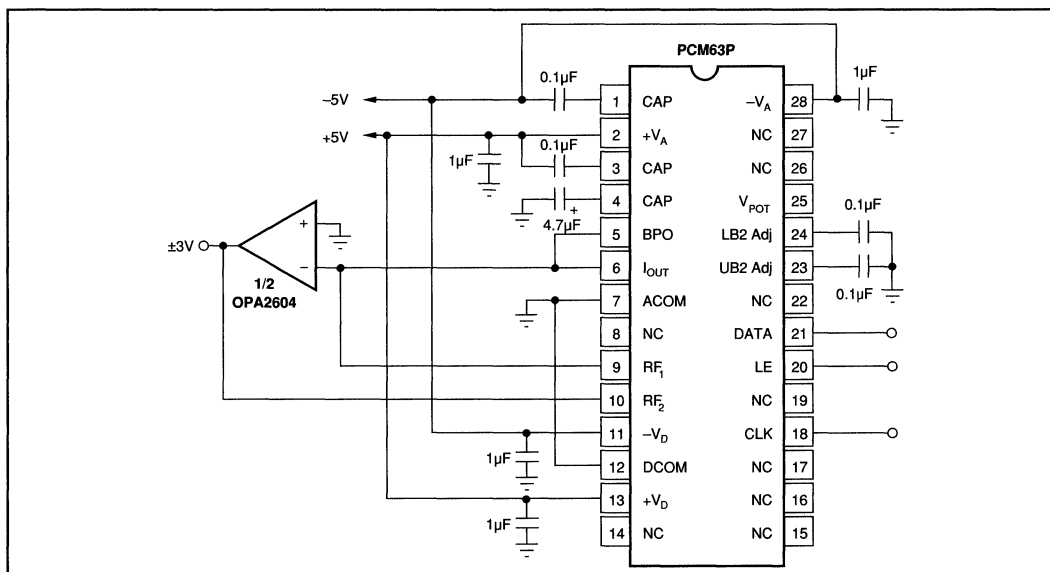
FIGURE 4. Connection Diagram.

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DIGITAL AUDIO PRODUCTS—D/A

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for both if no immediate improvement were noted). This procedure would require the generation of the digital bit-2 major carry code to the input of the PCM63P and a DVM or oscilloscope capable of reading the output voltage for a one LSB step (5.72µV) in addition to a distortion analyzer.

A more practical approach would be to forego the minor correction for the bit-2 major carry adjustment and only adjust for upper and lower DAC gain matching. The problem is that just by connecting the MSB circuitry to the PCM63P, the odds are that the upper and lower bit-2 weights would be greatly changed from their unadjusted states and thereby adversely affect the desired gain adjustment. Just centering the 100kΩ potentiometers would not necessarily provide the correct starting point. To guarantee that each 100kΩ potentiometer would be set to the correct starting or null point (no current into or out of the MSB adjust pins), the voltage drop across each corresponding 330kΩ resistor would have to measure 0V. A voltage drop of ±1.25mV across either 330kΩ resistor would correspond to a ±1LSB change in the null point from its unadjusted state (1LSB in current or 3.81nA x 330kΩ = 1.26mV). Once these starting points for each potentiometer had been set, each potentiometer would then be adjusted equally, in opposite directions, to achieve the lowest full-scale THD + N possible. If no immediate improvement were noted, the direction of rotation for both potentiometers would be reversed. One direction of potentiometer counter-rotations would only make the gain mismatch and resulting THD + N worse, while the opposite would gradually improve and then worsen the THD + N after passing through a no mismatch point. The determina-

tion of the correct starting direction would be arbitrary. This procedure still requires a good DVM in addition to a distortion analyzer.

Each user will have to determine if a small improvement in full-scale THD + N for their application is worth the expense of performing a proper MSB adjustment.

APPLICATIONS

The most common application for the PCM63P is in high-performance and professional digital audio playback, such as in CD and DAT players. The circuit in Figure 6 shows the PCM63P in a typical combination with a digital interface format receiver chip (Yamaha YM3623), an 8X interpolating digital filter (Burr-Brown DF1700P), and two third-order low-pass anti-imaging filters (implemented using Burr-Brown OPA2604APs).

Using an 8X digital filter increases the number of samples to the DAC by a factor of 8, thereby reducing the need for a higher order reconstruction or anti-imaging analog filter on the DAC output. An analog filter can now be constructed using a simple phase-linear GIC (generalized immittance converter) architecture. Excellent sonic performance is achieved using a digital filter in the design, while reducing overall circuit complexity at the same time.

Because of its superior low-level performance, the PCM63P is also ideally suited for other high-performance applications such as direct digital synthesis (DDS).

FIGURE 6. Stereo Audio Application.
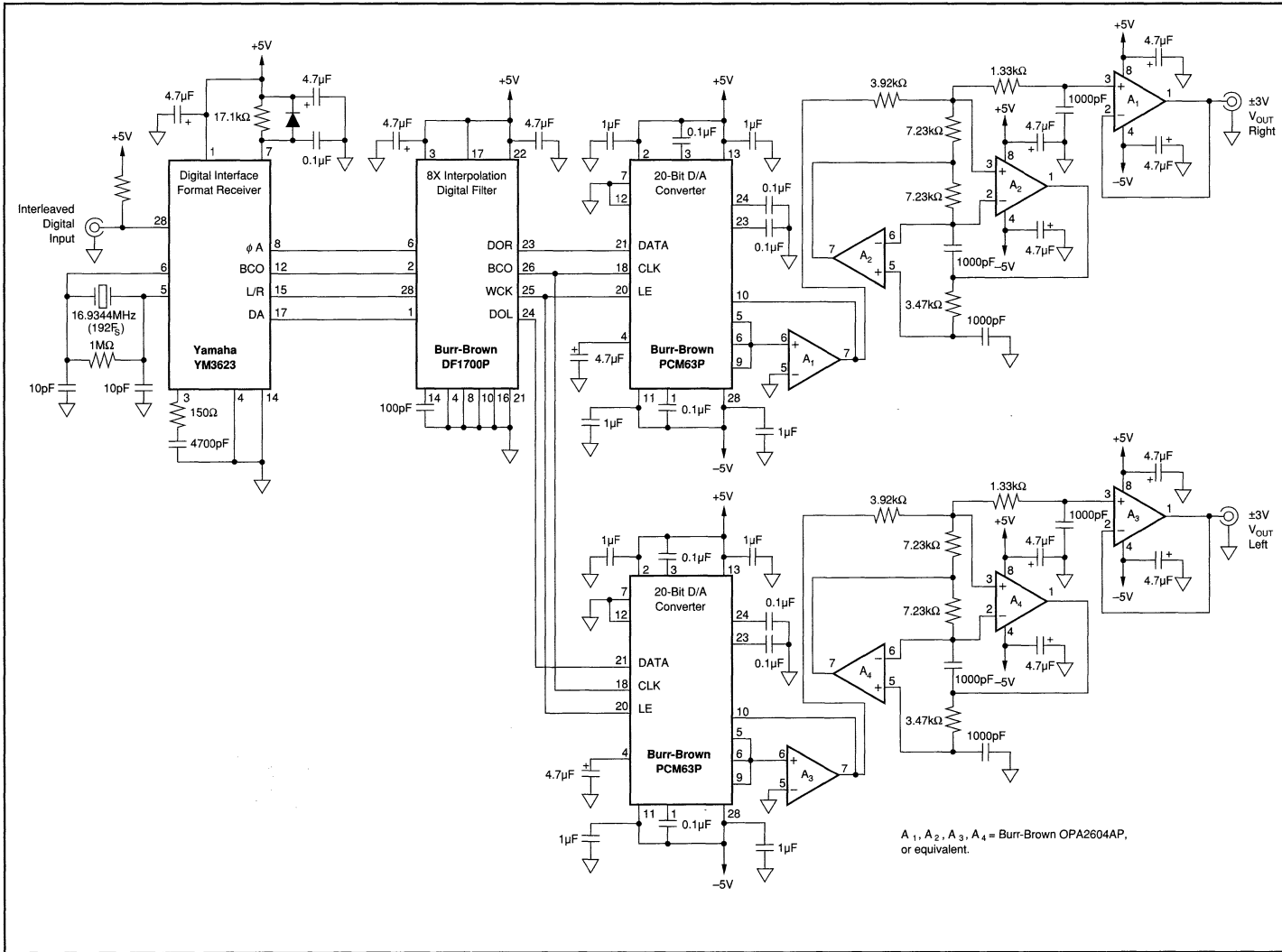
A$_1$, A$_2$, A$_3$, A$_4$ = Burr-Brown OPA2604AP, or equivalent.

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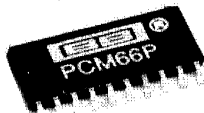
PCM66P

16-Bit CMOS Monolithic Audio
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **LOW COST 16-BIT 2-CHANNEL CMOS MONOLITHIC D/A CONVERTER**

● **SINGLE SUPPLY +5V OPERATION**

● **50mW POWER DISSIPATION**

● **GLITCH-FREE VOLTAGE OUTPUTS**

● **LOW DISTORTION: –86dB max THD + N**

● **COMPLETE WITH REFERENCE**

● **SERIAL INPUT FORMAT**

● **SINGLE OR DUAL DAC MODE OPERATION**

● **PLASTIC 20-PIN SOIC PACKAGE**

DESCRIPTION

The PCM66P is a low cost, dual output 16-bit CMOS digital-to-analog converter. The PCM66P features true glitch-free voltage outputs, internal reference and requires only a single +5V supply. Total power dissipation is less than 50mW max. Low maximum Total Harmonic Distortion + Noise (–86dB max; PCM66P-J) is 100% tested. Either one or two channel output modes are fully user selectable.

The PCM66P comes in a space-saving 20-pin plastic SOIC package. PCM66P accepts a serial data input format and is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, and +V$_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM66P AND PCM66P, J			UNITS
		MIN	TYP	MAX	
RESOLUTION				16	Bits
DYNAMIC RANGE			96		dB
DIGITAL INPUT		TTL Compatible CMOS			
Logic Family					
Logic Level: V$_{IH}$	I$_{IH}$ = +40μA max	+2.4		+5.25	V
V$_{IL}$	I$_{IL}$ = –40μA max	0		0.8	V
Data Format			Serial BTC[1]		
Input Clock Frequency		8.5			MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]					
PCM60P/66P: f = 991Hz (0dB)[3]	f$_S$ = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f$_S$ = 176.4kHz		–68		dB
f = 991Hz (–60dB)	f$_S$ = 176.4kHz		–28		dB
PCM60P-J/66P-J: f = 991Hz (0dB)	f$_S$ = 176.4kHz		–92	–86	dB
f = 991Hz (–20dB)	f$_S$ = 176.4kHz		–68		dB
f = 99lHz (–60db)	f$_S$ = 176.4kHz		–28		dB
CHANNEL SEPARATION		+80	+85		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	V$_{OUT}$ = 2.6		±2	±10	%
Gain Mismatch	Channel to Channel		±1		%
Bipolar Zero Error[5]			±30		mV
Gain Drift	0°C to 70°C		100		ppm/°C
Warm-up Time		1			minute
IDLE CHANNEL SNR[6]	20-20kHz with A-weighted filter		±90		dB
ANALOG OUTPUT					
Output Range			2.6		Vp-p
Output Impedance			2		Ω
Short Circuit Duration	To Be Determined				
Settling Time	Suffieicnt to Meet 176.4kHz THD + N Specs				
Glitch Energy	Meets All THD + N Specs Without External Output Deglitching				
POWER SUPPLY REQUIREMENTS					
+V$_{CC}$ Supply Voltage		+4.75	+5	+5.25	V
Supply Current			+9.5		mA
Power Dissipation	V$_{CC}$ = +5V			50	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency/signal level (on both left and right channels). (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling per channel). (5) Offset error at bipolar zero. (6) Ratio of output at BPZ (Bipolar Zero) to the full scale range using 20kHz low pass filter in addition to an A-weighted filter.

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DIGITAL AUDIO PRODUCTS—D/A

PCM66P PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	Left/Right Clock	LRCLK
2	Word Clock	WDCLK
3	Clock Input	CLK
4	Data Input	DATA
5	No Connection	NC
6	Digital Common	D_{COM}
7	Analog Common	A_{COM}
8	Left Channel V_{OUT}	L CH Out
9	Output Common	V_{COM}
10	Right Channel V_{OUT}	R CH Out
11	Analog Supply	$+V_{CC}$
12	Analog Supply	$+V_{CC}$
13	Reference Decouple	C_{REF}
14	Reference Sense	V_{REF} SENSE
15	Reference Output	V_{REF}
16	Analog Supply	$+V_{CC}$
17	Analog Supply	$+V_{CC}$
18	Digital Supply	$+V_{CC}$
19	Single DAC Mode	SDM SEL
20	Left/Right DAC Select	LRDAC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM66P	20-Pin SOIC	248
PCM66P, J	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

PCM66P   -X

Basic Model Number
   P: Plastic
Performance Grade Code

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage .... ±10V
Input Voltage Range .... −3V to +5.25V
Power Dissipation 50mW
Operating Temperature .... −30°C to +70°C
Storage Temperature .... −60°C to +100°C
Lead Temperature (soldering, 10s) .... +300°C

THEORY OF OPERATION

The PCM66P is a dual output, 16-bit CMOS digital-to-analog audio converter. The PCM66P, complete with internal reference, has two glitch-free voltage outputs and requires only a single +5V power supply. Output modes using either one or two channels per DAC are user selectable. The PCM66P accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.

ONE DAC TWO-CHANNEL OPERATION

Normally, the PCM66P is operated with a continuous clock input in a two-channel output mode. This mode is selected when SDM SEL is held low (single DAC mode select). Refer to the truth table shown by Table I for exact control logic relation-

ships. Data for left and right channel output is loaded alternately into the PCM66P while the control logic switches the left and right output amplifiers between the appropriate integrate and hold modes. Data word latching is controlled by WDCLK (word clock) and channel selection is made by LRCLK (left/right clock). Figure 1 shows the timing for the single DAC two-channel mode of operation. The block diagram in Figure 2 shows how a single DAC output provides switched output to both integrate and hold amplifiers. Output between left and right channels in this mode is not in phase. See Figure 3 for proper connection of the PCM66P in the two-channel DAC mode.

	PIN FUNCTIONS			SERIAL DATA WORD INPUT	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
SDM SEL	LRDAC	LRCLCK	WDCLK			
0	X	0	0	Right	Hold	Hold
0	X	0	1	Right	Integrate	Hold
0	X	1	0	Left	Hold	Hold
0	X	1	1	Left	Hold	Integrate
1	0	0	0	Inhibited	V_{COM}	Hold
1	0	0	1	Inhibited	V_{COM}	Hold
1	0	1	0	Left	V_{COM}	Integrate
1	0	1	1	Left	V_{COM}	Integrate
1	1	0	0	Right	V_{COM}	Hold
1	1	0	1	Right	V_{COM}	Hold
1	1	1	0	Inhibited	V_{COM}	Integrate
1	1	1	1	Inhibited	V_{COM}	Integrate
NOTE: Positive edge of CLK (P3) latches LRCLK (P1), WDCLK (P2), and DATA (P4).						

TABLE I. PCM66P Logic Truth Table.

TWO CHANNEL PER DAC OUTPUT MODE

P3 (CLK)	
P2 (WDCLK)	
P1 (LRCLK)	Load Right Channel Data / Load Left Channel Data
P4 (DATA)	1 2 8 9 10 11 12 13 14 15 16 1 2 8 9 10 11 12 13 14 15 16
P10 (LCH OUT)	Hold / Integrate / Hold
P10 (LCH V_{OUT})	
P12 (RCH OUT)	Hold / Integrate
P12 (RCH V_{OUT})	

NOTES: Single DAC Mode Select = 0; L/R DAC Select = X; WDCLK = 50% duty cycle; Serial Data is read in MSB first with BTC coding (MSB = Bit 1).

SINGLE CHANNEL PER DAC OUTPUT MODE

P3 (CLK) Both DACs	
P2 (WDCLK) Both DACs	
P1 (LRCLK) Both DACs	Load Right DAC Data / Load Left DAC Data
P4 (DATA) Both DACs	1 2 8 9 10 11 12 13 14 15 16 1 2 8 9 10 11 12 13 14 15 16
P12 (RCH OUT) Right DAC	Hold / Integrate
P12 (RCH V_{OUT}) Right DAC	
P12 (RCH OUT) Left DAC	Hold / Integrate
P12 (RCH V_{OUT}) Left DAC	

NOTES: Single DAC Mode Select = 1; L/R DAC Select = 0 (Left DAC) or 1 (Right DAC).

FIGURE 1. PCM66P Timing Diagram.

PCM66P

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DIGITAL AUDIO PRODUCTS—D/A
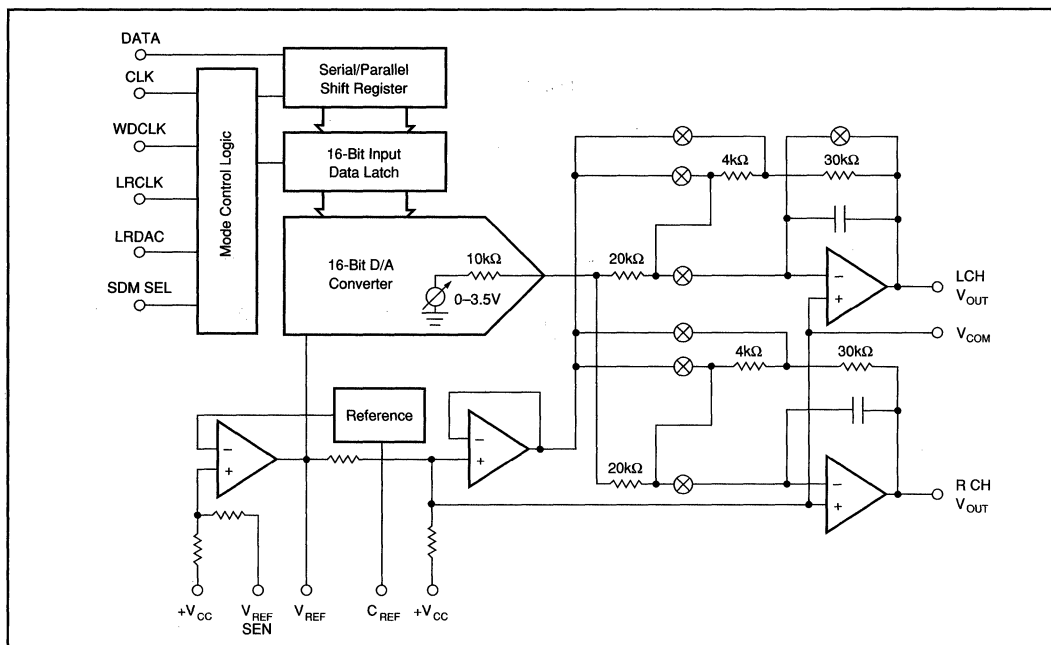
FIGURE 2. PCM66P Block Diagram.
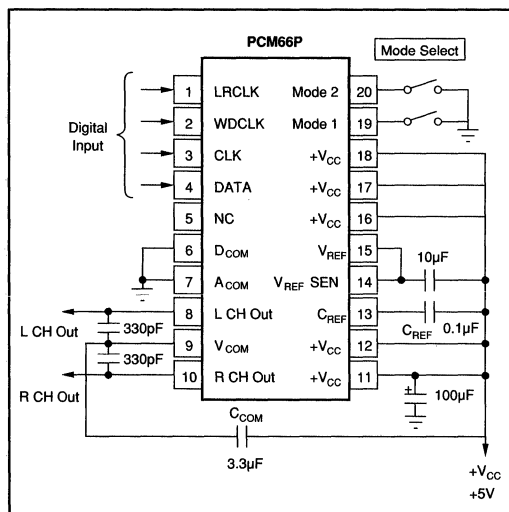
FIGURE 3. PCM66P Connection Diagram.

TWO DAC TWO-CHANNEL OPERATION

In phase, two-channel output can be obtained by using two PCM66Ps and choosing the single DAC mode (setting SDM SEL high). With the use of a high or low input level on LRDAC (P left/right DAC select), each DAC can have its right channel output dedicated to either left or right data

input with no additional input signals being required to latch the appropriate data from an alternating L/R data word input stream. In the single DAC mode, the PCM66P's left channel output is disabled and held at $+V_{COM}$. In this mode both DACs share common inputs for DATA, CLK, WDCLK, and LRCLK. Otherwise circuit connection is the same as the two-channel DAC mode, with the exception of LRDAC whose level selects whether the single DAC will output dedicated left or right channel data.

INTEGRATE AND HOLD OUTPUT AMPLIFIERS

The PCM66P incorporates integrate and hold amplifiers on each output channel. This allows a single, very fast DAC to feed both amplifiers and reduce circuit complexity. It also serves to block the output glitch from the DAC to the individual channel outputs and effectively makes the PCM66P outputs "glitch-free." The PCM66P is a single +5V supply device with a voltage output swing of 2.8Vp-p. The outputs swing asymmetrically around V_{COM} ($+V_{CC} - 2.33V$). See Table II for exact input/output relationships. Since true CMOS amplifiers are used on the PCM66P, the load resistance on the outputs should not be less than 100kΩ and the capacitive loads should not exceed 100pF. For maximum low-distortion performance, output buffer amplifiers should be considered.

DIGITAL INPUT	ANALOG OUTPUT	
Binary Two's Complement (Hex)	DAC Output (V)	Voltage (V) V_{OUT} Mode
7FFF	+FS	+3.5629443
0000	BPZ	+2.1629871
8000	−FS	+0.7630299
2E5B	V_{COM}	+2.6700000

TABLE II. PCM66P Input/Output Relationships.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM66P is total harmonic distortion plus noise. Digital data words are read into the PCM66P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz for each channel, such that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 4 shows a block diagram of the production THD + N test setup.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS}$ + $Noise_{RMS}$/$Signal_{RMS}$ expressed in dB. For the PCM66P, THD + N is 100% tested at three different output levels using the test setup shown in Figure 4. It is significant to note that this circuit does not include any output deglitching circuitry. This means the PCM66P meets even its −60dB THD + N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM66P, the extremely low THD + N performance is typically indicative of 14-bit to 15-bit integral linearity in the DAC depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on either DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement.

OFFSET, GAIN, AND TEMPERATURE DRIFT

The PCM66P is specified for other important parameters such as channel separation and gain mismatch between output channels. And although the PCM66P is primarily meant for use in dynamic applications, typical specs are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift.

TIMING CONSIDERATIONS

The data format of the PCM66P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact input data to voltage output coding relationship. Any number of bits can precede the 16 bits to be loaded, as only the last 16 will be transferred to the parallel DAC register on the first positive edge of CLK (clock input) after WDCLK (word clock) has gone low. All inputs to the PCM66P are TTL level compatible.
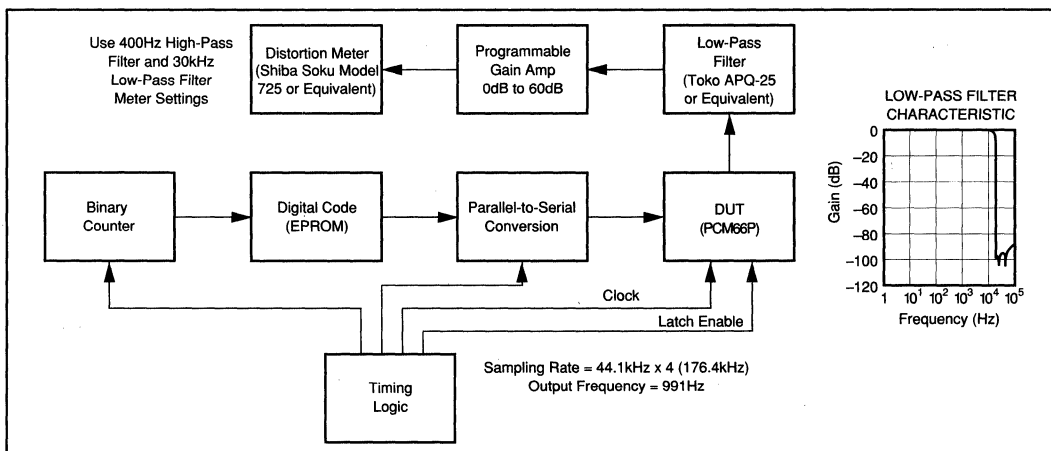
FIGURE 4. THD + N Test Setup Diagram.

WDCLK DUTY CYCLE

WDCLK is the input signal that controls when data is loaded and how long each output is in the integrate mode. It is therefore recommended that a 50% (high) duty cycle be maintained on WDCLK. This will ensure that each output will have enough time to reach its final output value, and that the output level of each channel will be within the gain mismatch specification. Refer to Figure 1 for exact timing relationships of WDCLK to CLK and LRCLK and the outputs of the PCM66P. The WDCLK can be high longer than 50%, as long as setup and hold times shown in Figure 5 are observed and the time high is roughly equivalent for both left and right channels.

SETUP AND HOLD TIME

The individual serial data bit shifts, the serial to parallel data transfer, and left/right control are triggered on positive CLK edges. The setup time required for DATA, WDCLK, and LRCLK to be latched by the next positive going CLK is 15ns minimum. A minimum hold time of 15ns is also required after the positive going CLK edge for each data bit to be shifted into the serial input register. Refer to Figure 5 for the timing relationship of these signals.

MAXIMUM CLOCK RATE

The 100% tested maximum clock rate of 8.47MHz for the PCM66P is derived by multiplying the standard audio sample rate of 44.1kHz times eight (4X oversampling times two channels) times the standard audio word bit length of 24 (44.1kHz $\times$ 4 $\times$ 2 $\times$ 24 = 8.47MHz). Note that this clock rate accommodates a 24-bit word length, even though only 16 bits are actually being used.

"STOPPED-CLOCK" OPERATION

The PCM66P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 16 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until the first clock after the one used to input bit 16 (LSB). This means the data is not shifted into the DHC latch until the start of the next 16-bit data word input, unless at least one additional clock accompanies the 16 used to serially shift in data in the first place. In either case, the setup and hold times for DATA, WDCLK, and LRCLK must still be observed.

INSTALLATION

The PCM66P only requires a single +5V supply. The +5V supply, however, is used in deriving the internal reference. It is therefore very important that this supply be as "clean" as possible to reduce coupling of supply noise to the outputs. If a good analog supply is available at greater than +5V, a zener diode can be used to obtain a stable +5V supply. A
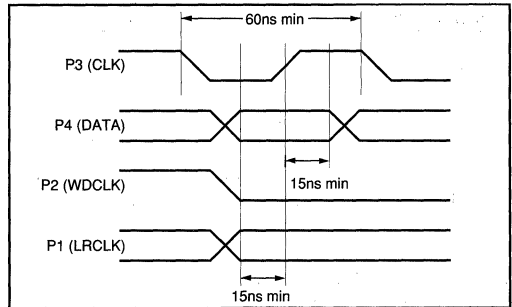
FIGURE 5. PCM66P Setup and Hold Timing Diagram.

100μF decoupling capacitor as shown in Figure 3 should be used regardless of how good the +5V supply is to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM66P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 3, C_{REF} and V_{REF} SENSE should have decoupling capacitors of 0.1μF (C_4) and 10μF (C_5) to +V_{CC} respectively with no special tolerance being required. To maximize channel separation between left and right channels, 5% 300pF capacitors (C_2 and C_3) between V_{COM} and left and right channel outputs are required in addition to a 5% 3μF capacitor (C_1) between V_{COM} and +5V. The ratio of 10k to 1 is the important factor here for proper circuit operation. Placement of all capacitors should be as close to the appropriate pins of the PCM66P as possible to reduce noise pickup from surrounding circuitry.

APPLICATIONS

Probably the most popular use of the PCM66P is in applications requiring single power supply operation. For example, the PCM66P is ideal for automotive compact disk (CD) and digital audio tape (DAT) playback units. To use a more complex bipolar DAC requiring ±5V supplies in the +12V application, for example, would require driving a stable "floating" ground and regulating the +12V to +10V. The single supply CMOS PCM66P would only require a +5V zener diode to regulate its 50mW max supply. The outputs could be AC coupled to the rest of the circuit for perfectly acceptable high dynamic performance. The PCM66P is ideal in any application requiring a minimum of additional circuitry as well as ultra-low-power CMOS performance.

Of course, the PCM66P is the D/A converter of choice in any application requiring very low power dissipation. Portable battery powered test and measurement equipment requiring very low distortion digital to analog converters would be an ideal application for the CMOS PCM66P with its 50mW max power dissipation.

BURR - BROWN®
[BB]
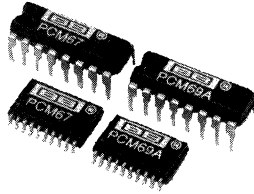
PCM67P/U
PCM69AP/AU

DEMO BOARD
AVAILABLE
See Appendix A for
more information.

Advanced 1 Bit BiCMOS Dual 18-Bit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **18-BIT RESOLUTION DUAL AUDIO DAC**
● **EXCELLENT THD PERFORMANCE:**
   0.0025% (–92dB) at F/S, K Grade
   1.0% (–40dB) at –60dB, K Grade
● **HIGH S/N RATIO: 110dB typ (IHF-A)**
● **DUAL, CO-PHASE**
● **SINGLE SUPPLY +5V OPERATION**
● **LOW POWER: 75mW typical**
● **CAPABLE OF 16X OVERSAMPLING**
● **AVAILABLE IN SPACE SAVING**
   16-PIN DIP OR 20-PIN SOIC
● **OPERATING TEMP RANGE:**
   –25°C to +85°C
● **EXTREMELY LOW GLITCH ENERGY**

DESCRIPTION

The PCM67 and PCM69A dual 18-bit DAC are low cost, dual output 18-bit BiCMOS digital-to-analog converters utilizing a novel architecture to achieve excellent low level performance.

By combining a conventional thin-film R-2R ladder DAC, a digital offset technique with analog correction and an advanced one-bit DAC using first order noise shaping technique, the PCM67 and PCM69A achieve high resolution, minimal glitch, and low zero-crossing distortion.

PCM67 digital offset occurs at bit 9, making it ideal for high-performance CD players. PCM69A digital offset occurs at bit 4, making it an excellent choice for digital musical instruments and audio DSP.

Both PCM67 and PCM69A operate from a single +5V supply. The low power consumption and small size (16-pin PDIP or 20-pin SOIC) make these converters ideal for a variety of digital audio applications.

PCM67/69A

8.2

DIGITAL AUDIO PRODUCTS—D/A

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[BB]

8.2.91

SPECIFICATIONS

ELECTRICAL

All specifications at +25°C and $+V_A$, $+V_D$ = +5V unless otherwise noted

| PARAMETER | CONDITIONS | PCM67/69A | | | UNITS |
		MIN	TYP	MAX	
RESOLUTION			18		Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale			106		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}	$I_{IH} = \pm 5\mu A$	+2		$+V_D$	V
V_{IL}	$I_{IL} = \pm 5\mu A$	0		0.8	V
Data Format			Serial, MSB First, BTC[1]		
Input System Clock Frequency			16.9344		MHz
TOTAL HARMONIC DISTORTION + N[2,3,4]					
PCM67P/69AP, PCM67U/69AU					
f = 991Hz (0dB)	f_S = 352.8kHz		–86	–82	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–68		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–34	dB
PCM67P-J/69AP-J, PCM67U-J/69AU-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–91	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–72		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
PCM67P-K/69AP-K, PCM67U-K/69AU-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–95	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–74		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
CHANNEL SEPARATION	(f = 1kHz)		106		dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±1		dB
Gain Error			±3	±10	%
Gain Mismatch, Channel-to-Channel			±1	±5	%
Gain Drift	0°C to +70°C		95		ppm/°C
Warm-up Time			1		Minute
IDLE CHANNEL SNR[5]	20Hz to 40kHz at BPZ[6]		110		dB
ANALOG OUTPUT					
Output Range (±3%)			1.2		mA
Output Impedance (±30%)			1.8		kΩ
V_{COM}		3.35	3.50	3.65	V
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS, System Clock = 16.9344MHz					
$+V_A$, $+V_D$ Supply Voltage Range	$+V_A = +V_D$	+4.75	+5.00	+5.25	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		15	20	mA
Power Dissipation	$+V_A$, $+V_D$ = +5V		75	105	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$)/Signal$_{RMS}$. (3) D/A converter output frequency/signal level (both left and right channels are "on"). (4) D/A converter sample frequency (8 x 44.1kHz; 8X oversampling per channel). (5) Ratio of Noise$_{RMS}$/Signal$_{RMS}$. Measured using a 40kHz 3rd order GIC (Generalized Immittance Converter) filter and an A-weighted filter. (6) Bipolar Zero.

PIN ASSIGNMENTS

PCM67P PCM69AP	PCM67U PCM69AU	DESCRIPTION	MNEMONIC
1	1	+5V Analog Supply Voltage	$+V_A$
2	2	Left Voltage Common	LV_{COM}
	3	No Connection	NC
3	4	Left Current Output (0 to 1.2mA)	LI_{OUT}
4	5	Servo Decoupling Capacitor	SRVCAP
5	6	Reference Decoupling Capacitor	REFCAP
6	7	Right Current Output (0 to 1.2mA)	RI_{OUT}
	8	No Connection	NC
7	9	Right Voltage Common	RV_{COM}
8	10	Analog Common	ACOM
9	11	Digital Common	DCOM
	12	Mode Control 2	MC2
10	13	Right Data Input	RDATA
11	14	Bit Clock	BTCK
12	15	System Clock	SYSCK
13	16	Word Clock	WDCK
14	17	Left Data Input	LDATA
	18	Mode Control 3	MC3
15	19	Mode Control 1	MC1
16	20	+5V Digital Supply Voltage	$+V_D$

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM67P/69AP	16-Pin Plastic DIP	180
PCM67U/69AU	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_A$, $+V_D$ to ACOM, DCOM .... 0V to +6.5V
ACOM to DCOM .... ±0.5V
Digital Inputs to DCOM .... −0.3V to $+V_D$ + 0.3V
Power Dissipation .... 300mW (U Package), 500mW (P Package)
Lead Temperature, (soldering, 10s) .... +260°C
Max Junction Temperature .... +165°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

8.2

PCM67/69A

DIGITAL AUDIO PRODUCTS—D/A

PIN CONFIGURATION — PCM67P/69AP (16-Pin DIP)
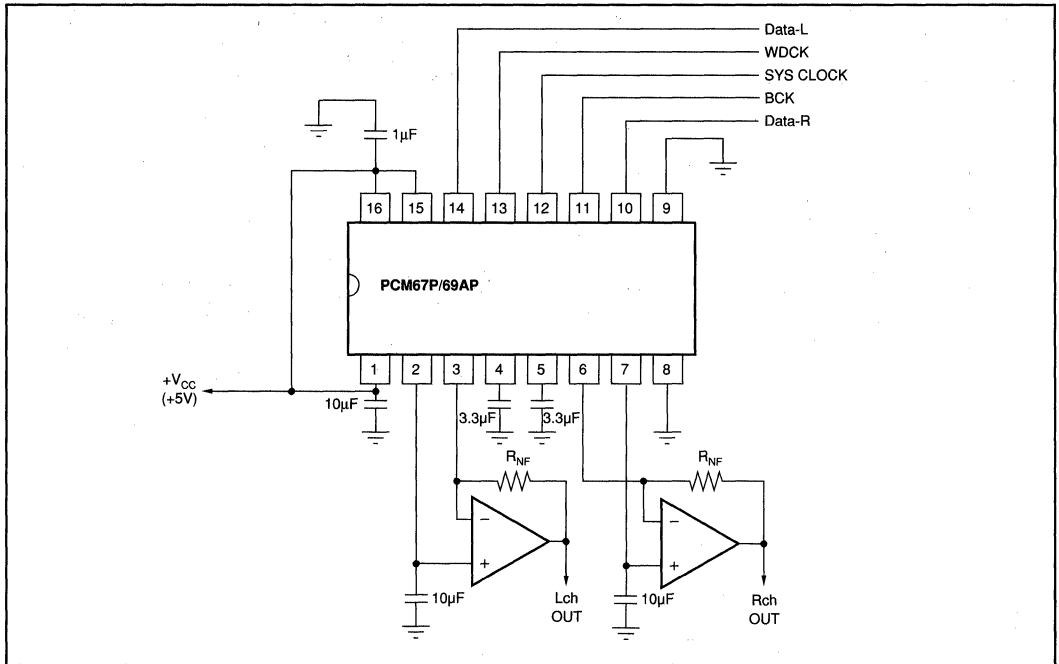
PIN CONFIGURATION — PCM67U/69AU (20-Pin SOIC)
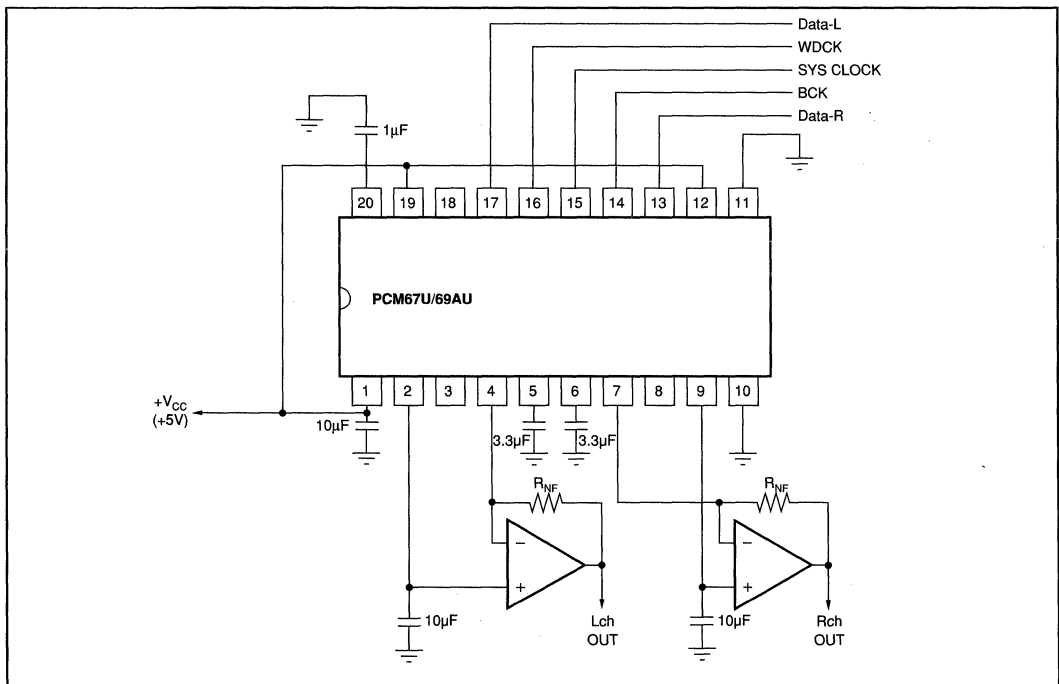
TYPICAL PERFORMANCE CURVES

All specifications at +25°C and V_{CC} = +5.0V unless otherwise noted.

THD vs POWER SUPPLY VOLTAGE

GAIN ERROR / V_{COM} vs POWER SUPPLY

THD vs TEMPERATURE

GAIN ERROR / V_{COM} vs TEMPERATURE

THD vs SYSTEM CLOCK FREQUENCY

CHANNEL SEPARATION vs SIGNAL FREQUENCY

PCM67/69A

8.2
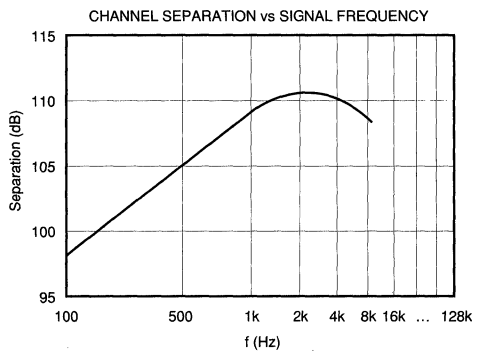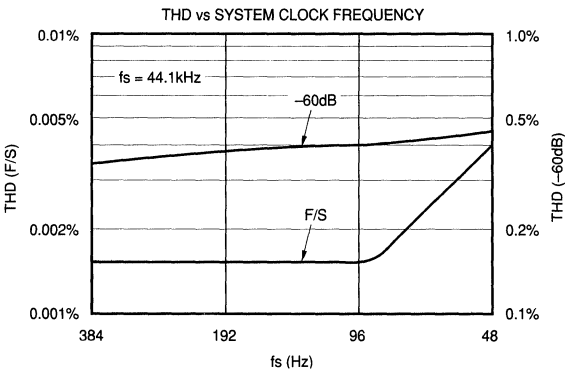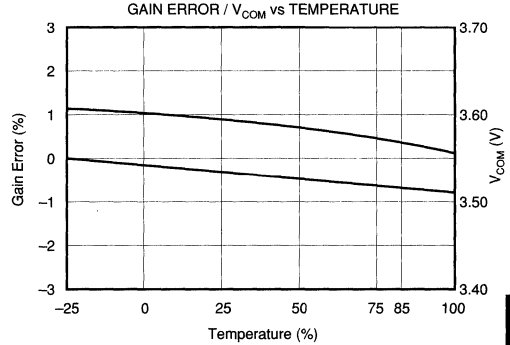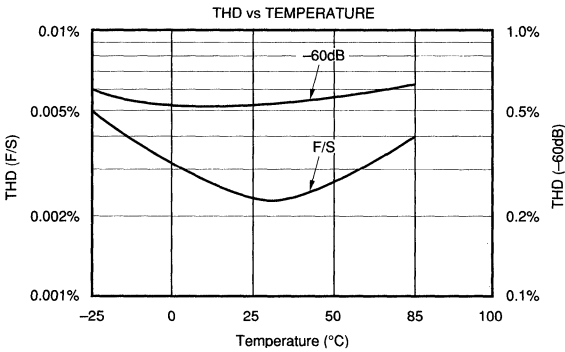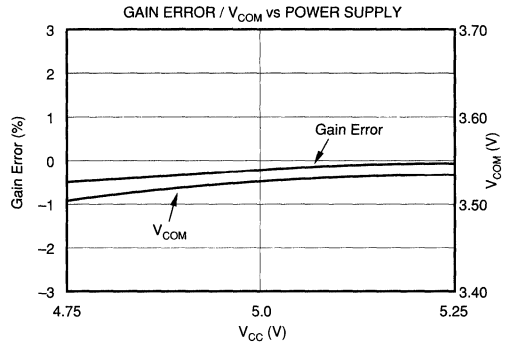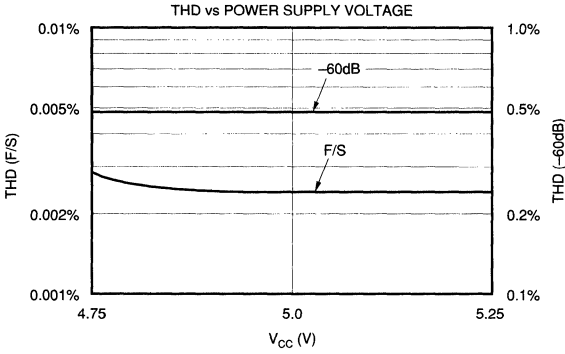
DIGITAL AUDIO PRODUCTS—D/A

DISCUSSION OF SPECIFICATIONS

The PCM67 and PCM69A are specified to provide critical performance criteria for a variety of applications. The accuracy of a D/A converter is described by the transfer function shown in Figure 1.
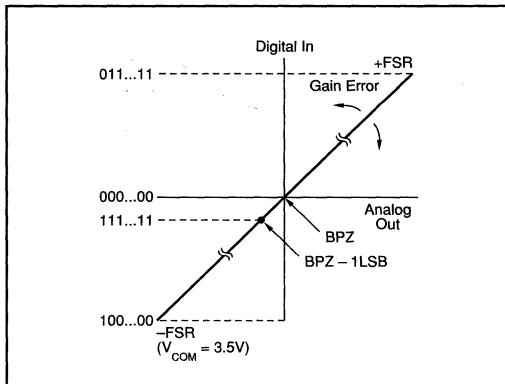
FIGURE 1. Transfer Performance.

DIGITAL INPUT CODE

The PCM67/69A accepts Binary Two's Complement (BTC) digital input code (MSB FIRST).The relationship of digital input to analog output is shown in Table 1.

DIGITAL INPUT	ANALOG OUTPUT (VOLTAGE)	ANALOG OUTPUT (CURRENT)
7FFFFF (HEX)	+FSR	–1.2mA
00003F (HEX)	BPZ	–0.6mA
FFFFFF (HEX)	BPZ – 1LSB	–0.59995mA
80003F (HEX)	–FSR	0mA

TABLE I. Digital Code and Analog Out.

GAIN ERROR AND GAIN MISMATCH, CHANNEL-TO-CHANNEL

Gain error is defined as deviation of the output current span from the ideal span of 1.2mA (FSR) on each channel. Gain error of PCM67/69A is typically ±3% of FSR.

Gain mismatch, channel-to-channel is defined as the difference in gain error between the left channel and right channel.

THE RELATIONSHIP OF V_{COM} AND I/V OUT

The output current range of PCM67 and PCM69A is 0mA to 1.2mA as shown in Table 1.

In the typical application, the non-inverting input of the external I/V op amp is connected to the V_{COM} pin of PCM67 and PCM69A. Accordingly, the output voltage level at FSR after I/V conversion is V_{COM} voltage (+3.5V) as shown in Figure 2.
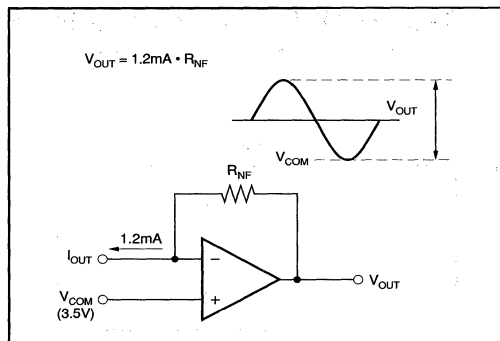
FIGURE 2. I/V Amplifier Circuit.

S/N RATIO

S/N ratio is defined as the ratio of full scale output and no input noise level at BPZ point. The PCM67/69A is specified at 110dB typical with "IHF-A" filter.

LEVEL LINEARITY ERROR

Level linearity error is defined as the deviation of actual analog output level from digital input level. PCM67/69A is specified at 1dB typical at –90dB output level. The 0.5LSB quantization error at –90dB of 16-bit conversion is equal to +1.94dB, –2.5dB.

TOTAL HARMONIC DISTORTION

THD is a key parameter in audio applications, THD is a measure of the magnitude and distribution of the linearity error, differential linearity error, and noise, as well as quantization error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM67/69A error referred to the input can be shown to be

$$\varepsilon_{ms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[E_L(i) + E_Q(i)\right]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM67 or PCM69A at each sampling point. THD can then be expressed as

$$THD = \frac{\varepsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[E_L(i) + E_Q(i)\right]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to THD.

For PCM67 and PCM69A the test period is set at an 8X oversampling rate (352.8kHz = 44.1kHz • 8), which is the typical sample rate for CD player applications.

The test signal frequency is 991Hz and the amplitude of the signal level is F/S (0dB), and –60dB down from F/S.

All THD tests are performed without a deglitcher circuit and without a 20kHz low pass filter.

SYSTEM CLOCK REQUIREMENTS

The PCM67 and PCM69A need a system clock for the one-bit noise shaping DAC operation.

The PCM67 is capable of only a 384Fs corollary system clock frequency such as 192Fs, 96Fs (24 times word rate or integer multiple of 24).

The PCM69A is capable of any system clock up from 48Fs to 384Fs such as 384Fs, 256Fs, 100Fs with condition for timing as described in "Timing of PCM69A" in Figure 5.

The user can choose either model for their application. Table II shows the different SYSCLK options.

MODEL	BASIC SYSCLK	OTHER CAPABLE SYSCLK
PCM67	384Fs	192Fs, 96Fs
PCM69A	Any Clock (with timing condition) Examples: 384Fs, 300Fs, 256Fs, 200Fs, 90Fs	

TABLE II. System Clock Requirements.

LOGIC TIMING

The serial data bit transfers are triggered on positive bit clock (BCK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Word Clock (WDCK). The change in the output of the DAC coincides with the falling edge of WDCK.

Refer to Figure 3 for graphical relationships of these signals. The setup and hold timing relationships for these signals are shown in Figure 4.
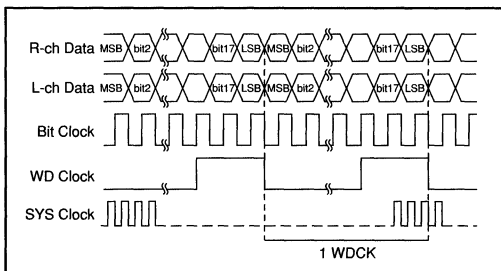
FIGURE 3. Timing Diagram.

The PCM67/69A accepts TTL compatible logic input levels. The data format of the PCM67/69A is BTC with the most significant bit (MSB) being first in the serial input bit stream.

t_{SH}: SYS Clock High Pulse Width : 15ns, min
t_{SL}: SYS Clock Low Pulse Width : 15ns, min
t_{DW}: Data Valid Time : 20ns, min
t_{DSU}: Data Setup Time : 10ns, min
t_{DHO}: Data Hold Time : 5ns, min
t_{CH}: Bit Clock High Pulse Width : 15ns, min
t_{CL}: Bit Clock Low Pulse Width : 15ns, min
t_{CW}: WD Clock Fall Time From Bit Clock Rise : 10ns, min
t_{WC}: Bit Clock Rise Time From WD Clock Fall : 15ns, min
t_{WH}: WD Clock High Pulse Width : 1 SYS Clock Cycle, min
t_{WL}: WD Clock Low Pulse Width : 1 SYS Clock Cycle, min

FIGURE 4. Timing Specification.

TIMING OF PCM69A

PCM69A timing is similar to PCM67 except that PCM69A is capable of operating from any system clock up to 384Fs. For synchronized operation, PCM69A system clock and WDCK timing must be as shown in Figure 5.

t_{n1}: WDCK Fall Delay From Rise of SYSCLK : min 10ns
t_{n2}: SYSCLK Rise Delay From Fall of WDCK : min 20ns
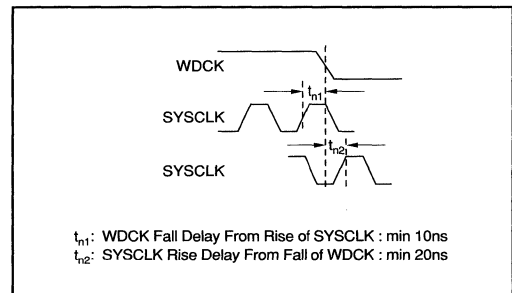
FIGURE 5. Timing of PCM69A for SYSCLK and WDCK.

PCM67/69A

8.2

DIGITAL AUDIO PRODUCTS—D/A

INSTALLATION

POWER SUPPLIES

Refer to "Pin Configuration" diagram for proper connection of the PCM67/69A. The PCM67/69A requires only a +5V supply. Both analog and digital supplies should be tied together at a single point, as no real advantage is gained by using separate supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output.

FILTER CAPACITOR REQUIREMENTS

As shown in the "Pin Configuration" diagram, various sizes of decoupling capacitors can be used with no special tolerances required. All capacitors should be as close to the appropriate pins of the PCM67/69A as possible to reduce noise pickup from surrounding circuitry.

A power supply decoupling capacitor should be used near the analog supply pin to maximize power supply rejection, as shown in Figure 6, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM67/69A as possible.

The value of these capacitors is influenced by actual board layout design and noise from power supplies and other digital input lines.

The best suitable value for the capacitors should be determined by the user's actual application board.

In case of shift to ±3V swing, 0V center

$$R_{NF} = \frac{V_{OUT}}{1.2mA} = \frac{6V}{1.2mA} = 5k\Omega$$

$-FSR\pm(V_S) = -3V$ after offset addition, shift voltage
V_{SHT} is given by
$$V_{SHT} = V_{COM} + 3V = 3.5 + 3 = 6.5V$$

Offset Current I_{OS} is given by
$$I_{OS} = \frac{V_{SHT}}{R_{NF}} = \frac{6.5V}{5k\Omega} = 1.3mA$$

Offset Resistor R_{OS} is given by
$$R_{OS} = \frac{V_{CC} - V_{COM}}{I_{OS}} = \frac{5 - 3.5V}{1.3mA} = 1.15k\Omega$$
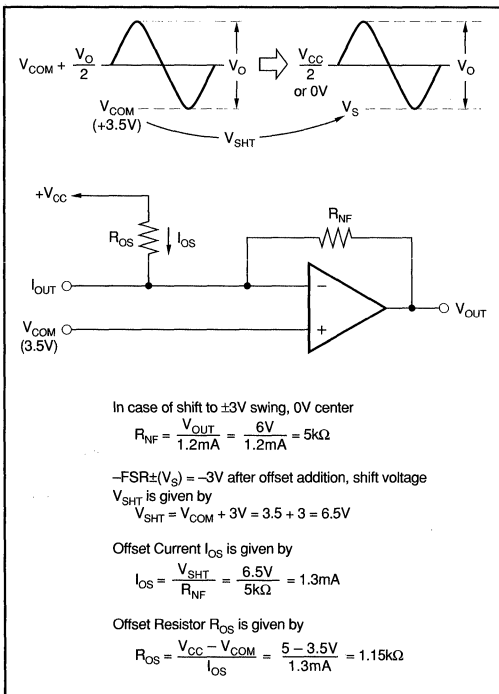
FIGURE 6. Shift of I/V Out Voltage.

SHIFT OF I/V OUT VOLTAGE

If the user requires a bipolar voltage output centered around 0V or one-half of V_{CC}, the output can be shifted by adding an offset current on the inverting point of the I/V op amp as shown in Figure 6.

Note: R_1 and C_1 are noise de-coupling circuits from noise on $+V_{CC}$ power supply line.
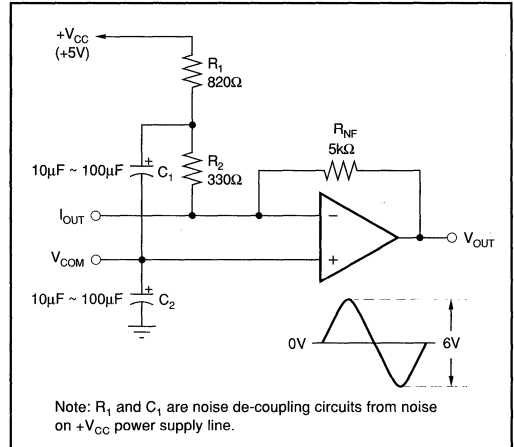
FIGURE 7. Useful Application Circuit for Shift of I/V Out Voltage.

INTERFACE CONTROL FUNCTION

Both the PCM67 and PCM69A (SOIC package type) are capable of 16-bit L/R serial input and 20-bit L/R parallel input as shown in Table 3.

MC1	MC2	MC3	DATA-R	INPUT FORMAT	
0	0	1	0	16-Bit L/R Serial[1]	⎿R⏌⎿L⏌R WDCK
0	0	1	1	16-Bit L/R Serial[1]	⎿L⏌R⎿L⏌R WDCK
0	1	1	0	18-Bit L/R Serial[1]	⎿R⏌⎿L⏌R WDCK
0	1	1	1	18-Bit L/R Serial[1]	⎿L⏌R⎿L⏌R WDCK
1	0	1	X	20-Bit L/R Parallel	
1	0	0	X	20-Bit L/R Parallel	[WDCK Invert]
1	1	1	X	18-Bit L/R Parallel	
1	1	0	X	18-Bit L/R Parallel	[WDCK Invert]

NOTE: (1) Data input to Data-Lch (Pin 17) for L/R serial format.

TABLE III. Interface Control Function of SOIC.

PCM67P and PCM69AP (DIP package) have only 18-bit L/R serial input function as shown in Table 4.

MC1	DATA-R	INPUT FORMAT	
0	0	18-Bit L/R Serial	⎿R⏌⎿L⏌R WDCK
0	1	18-Bit L/R Serial	⎿L⏌R⎿L⏌R WDCK
1	X	18-Bit L/R Parallel	

TABLE IV. Interface Control Function of DIP.

DIGITAL FILTER INTERFACE
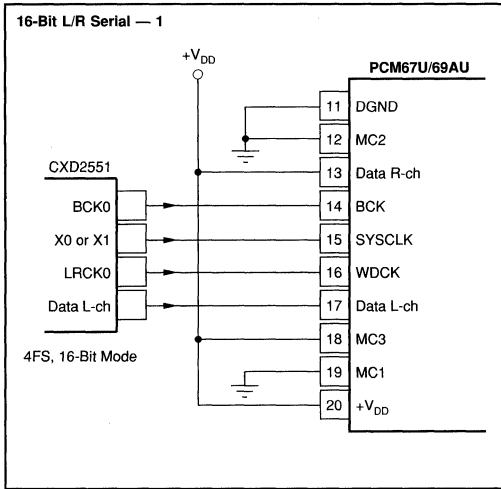
FIGURE 8. Using Sony CXD2551.
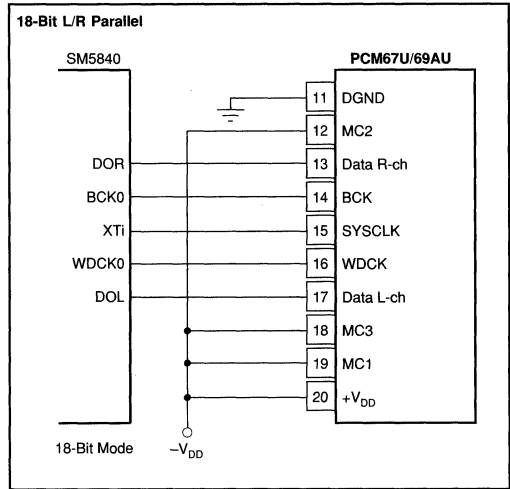
FIGURE 10. Using NPC SM5840.
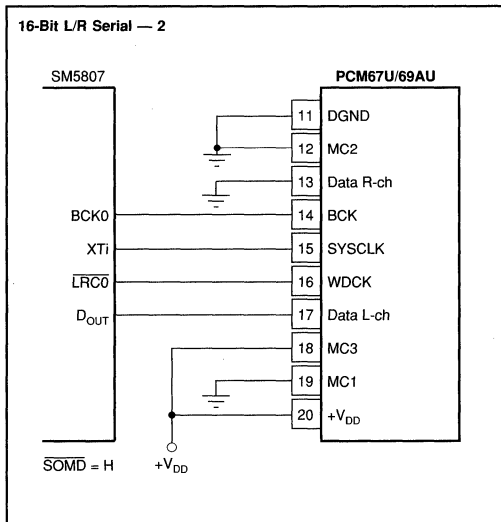
FIGURE 9. Using NPC SM5807.
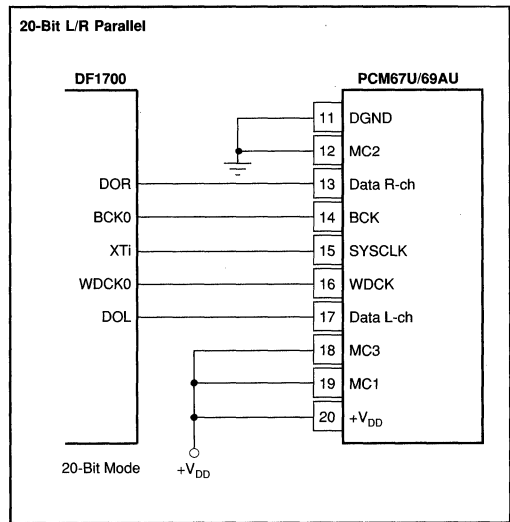
FIGURE 11. Using Burr-Brown DF1700.

PCM67/69A

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DIGITAL AUDIO PRODUCTS—D/A

THEORY OF OPERATION

Digital converters in audio systems have traditionally utilized a laser-trimmed, current-source DAC architecture. Unfortunately, this type of technology suffers from the problems inherent in switching widely varying current levels. Design improvements have helped, but DACs of this type still exhibit low-level nonlinearity due to errors at the major carry.

Recently, DACs employing a different architecture have been introduced. Most of these DACs utilize a one-bit DAC with "noise shaping" techniques and very high oversampling rate to achieve the digital-to-analog conversion. Basically, the trade-off is from very accurate but slow current sources to one rapidly sampled current source whose average output in the audio frequency range is equal to the current desired. Noise shaping insures that the "undesirable" frequencies associated with one-bit DAC output lie outside the audio range.

These "Bitstream", "MASH", or one-bit DACs overcome the low level linearity problems of conventional DACs, since there can be no major carry error. However, this architecture exhibits problems of its own: signal-to-noise performance is usually worse than a similar conventional DAC, "dither noise" may be needed in order to get rid of unwanted tones, a separate high-speed clock may be required, the part may show sensitivity to clock jitter, and a high-order low-pass filter is necessary to filter the DAC output.

The PCM67/69A is a cross between these two architectures. It includes both a conventional laser-trimmed, current-source DAC and an advanced one-bit DAC. The conventional DAC is a 10-bit DAC where each bit weight has been trimmed to 18-bit linearity. The one-bit DAC has a weight equal to bit 10 and employs a first-order noise shaper to generate the "bitstream."

This approach does not eliminate all the problems associated with the two architectures but rather minimizes them as much as possible. The conventional DAC still exhibits some major carry error which would normally reduce low-level linearity. However, to reduce this error even further, the PCM67/69A utilizes an offset technique whereby bit n is subtracted from the digital input code whenever it is positive (see Figure 1 and Table I). When this is done, an offset current equal to the weight of bit n is switched in to compensate. This offset comes from a one-bit DAC which has also been trimmed to 18-bit linearity. While this technique doesn't remove the major carry error completely, the "glitch" is only present in higher amplitude signals where it is much less audible.

As for the one-bit DAC, a number of problems with this architecture are also reduced: the DAC is designed to operate from the system clock, thus eliminating the need for a separate clock; the lower quantizing level of the DAC make it less sensitive to clock jitter; and output filtering requirements are reduced because "out-of-band noise" has smaller amplitude, is "farther-out," and increases much more slowly due to the first-order noise shaper. Still, it is important to keep in mind that the one-bit DAC imposes some design considerations. Figure 2 shows the THD + N of the converter versus "System Clock" frequency. This is the clock used to operate the one-bit DAC and noise shaper. Generally, the higher the oversampling the better. However, near full-scale, the converter is limited by other constraints and higher clock frequencies (past $96f_s$) tend to slightly worsen its performance. At low levels, performance improves almost linearly with increasing clock frequency. The one-bit DAC was designed to operate between $96f_s$ (4X oversampling) and $384f_s$ (16X oversampling). But, it can be operated at $48f_s$ (2X oversampling) with slightly reduced performance.

TOTAL HARMONIC DISTORTION + NOISE

A key specification for audio DACs is usually total harmonic distortion plus noise (THD + N). For the PCM67/69A, THD + N is tested in production as shown in Figure 12. Digital data words are read into the PCM67/69A at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. The output of the DAC goes to an I-to-V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer.
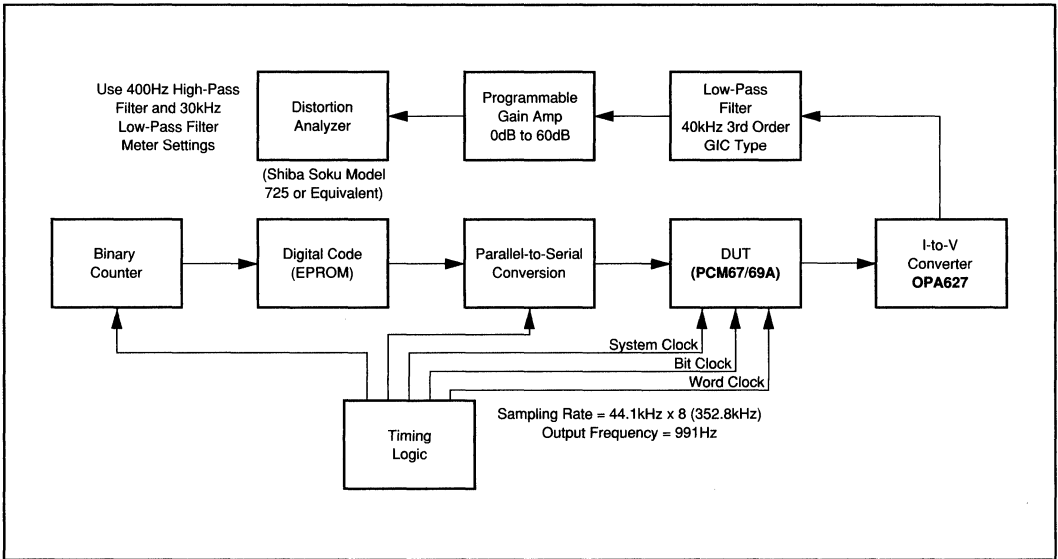
FIGURE 12. PCM67/69A THD + N Production Test.
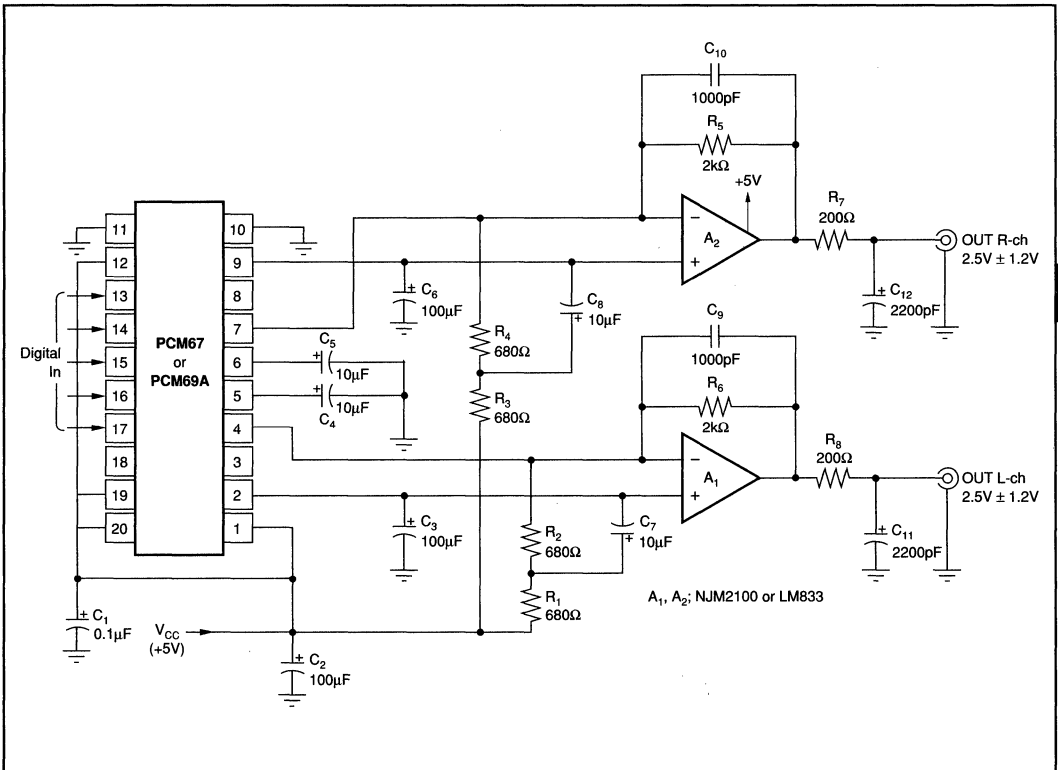
FIGURE 13. Single +5V Power Supply, with LPF, I/V Amp Application Circuit for Portable Digital Audio.

PCM67/69A

8.2

DIGITAL AUDIO PRODUCTS—D/A
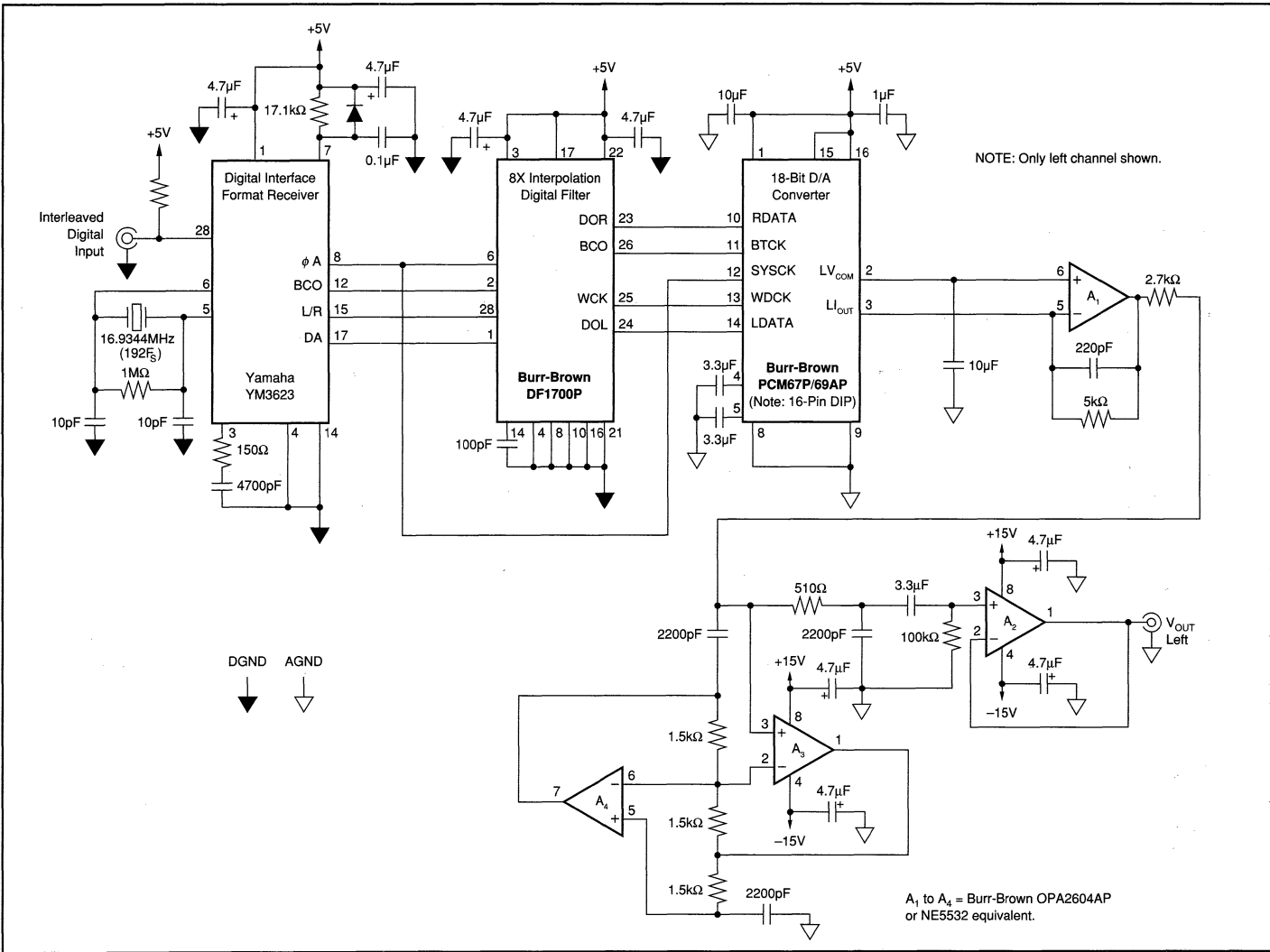
FIGURE 14. HiFi D/A Converter Unit Application with Digital Audio Interface Format.

For Immediate Assistance, Contact Your Local Salesperson

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PCM1700U
PCM1700P

**DEMO BOARD
AVAILABLE
See Appendix A for
more information.**

Dual 18-Bit Monolithic Audio
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **DUAL 18-BIT LOW-POWER MONOLITHIC AUDIO D/A CONVERTER**

● **VERY LOW MAX THD+N: –92dB Without External Adjust**

● **CO-PHASE, GLITCH-FREE ±3V OR ±670μA AUDIO OUTPUTS**

● **CAPABLE OF 16X PER CHANNEL OVERSAMPLING RATE**

● **COMPLETE WITH INTERNAL REFERENCE**

● **SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD PCM56P**

● **RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX**

● **COMPACT 28-PIN PLASTIC DIP OR SOIC**

DESCRIPTION

The PCM1700 is a low cost, high-performance, dual 18-bit digital-to-analog converter. The PCM1700 features true glitch-free, co-phase current and voltage outputs and only requires ±5V supplies. The PCM1700 comes complete with an internal reference and optional MSB adjustability for even greater THD performance. Total power dissipation is less than 400mW max. Low maximum Total Harmonic Distortion + Noise (–92dB max; PCM1700P-K) is 100% tested. The very fast PCM1700 is also capable of 16X oversampling rates on both channels simultaneously, providing freedom in output filter selection.

The PCM1700 comes in space-saving 28-pin plastic DIP and SOIC packages. PCM1700 accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.

PCM1700

8.2

DIGITAL AUDIO PRODUCTS—D/A

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SPECIFICATIONS

ELECTRICAL

At 25°C, and ±V_cc= ±5.00V unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1700U/U-J/U-K, PCM1700P/P-J/P-K			UNITS
		MIN	TYP	MAX	
RESOLUTION		18			Bits
DYNAMIC RANGE			+108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL Compatible		
Logic Level: V_IH		+2		+V_cc	V
V_IL		0		−0.8	V
I_IH	V_IH = +2.7V			+1	μA
I_IL	V_IL = +0.4V			−50	μA
Data Format			Serial BTC[1]		
Input Clock Frequency				16.9	MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[6]					
PCM1700_:					
f = 991kHz (0dB)	f_S = 352.8kHz[4]		−88	−82	dB
f = 991kHz (−20dB)	f_S = 352.8kHz		−74	−68	dB
f_IN = 991kHz (−60dB)	f_S = 352.8kHz		−34	−28	dB
PCM1700_-J:					
f = 991kHz (0dB)	f_S = 352.8kHz		−94	−88	dB
f = 991kHz (−20dB)	f_S = 352.8kHz		−76	−74	dB
f = 991kHz (−60dB)	f_S = 352.8kHz		−36	−34	dB
PCM1700_-K:					
f = 991kHz (0dB)	f_S = 352.8kHz		−98	−92	dB
f = 991kHz (−20dB)	f_S = 352.8kHz		−80	−74	dB
f = 991kHz (−60dB)	f_S = 352.8kHz		−40	−34	dB
CHANNEL SEPARATION		+96	+108		dB
SIGNAL-TO-NOISE RATIO[5]	20Hz to 20kHz at BPZ[6]		+108		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±3	%
Gain Mismatch	Channel to Channel		±1	±3	%
Bipolar Zero Error			10		mV
BPZ Error Mismatch	Channel to Channel		5		mV
BPZ Differential Linearity Error[7]			±1		LSB
Gain Drift			100		ppm/°C
Bipolar Zero Drift			20		ppm of FSR/°C
Warm-up Time		1			minute
POWER SUPPLY REJECTION	±V_cc to V_OUT		+86		dB
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Impedance			0.1		Ω
Current Output			±8		mA
Capacitive Load Drive	R_LOAD = 1.5kΩ		TBD		pF
Short Circuit Duration			Indefinite		
Settling Time			Sufficient to Meet THD + N Specs		
Glitch Energ			Meets All THD + N Specs Without External Output Deglitching		
Current: Output Range	(±2%)		±670		μA
Output Impedance	(±2%)		1.67		kΩ
POWER SUPPLY REQUIREMENTS					
±V_cc Supply Voltage		+4.75	+5.00	+5.25	V
Supply Current: +I_cc	+V_cc = +5.0V		+40		mA
−I_cc	−V_cc = −5.0V		−16		mA
Power Dissipation	±V_cc = ±5.0V		280	475	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		−30		+70	°C
Storage		−60		+100	°C

NOTES: (1) Binary Two's Complement coding. (6) Ratio of (Distortion_RMS + Noise_RMS) / Signal_RMS. (3) D/A converter input frequency/signal level on both left and right channels. (4) D/A converter sample frequency (8 X 44.1kHz; 8X oversampling per channel). (5) Ratio of Noise_RMS / Signal_RMS. Measured using an A-weighted filter. (6) Bipolar zero. (7) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSBs. Adjustable to zero error.

PIN ASSIGNMENTS (Plastic PKG)

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply	$-V_{CC}$
2	Left Channel Servo-Amp Decoupling Point	CAP
3	Left Channel MSB Adjustment	MSB ADJ (L)
4	No Connect	NC
5	Left Channel Bipolar Offset Decoupling Point	CAP
6	Left Channel Current Output	IOUT (L)
7	Left Channel Analog Common	ACOM
8	Left Channel Summing Junction	SJ (L)
9	Left Channel Voltage Output	VOUT (L)
10	No Connect	NC
11	+5V Digital Supply	$+V_{DD}$
12	Left Channel Data Input	DATA
13	Clock Input	CLOCK
14	–5V Logic Supply	$-V_{DD}$
15	Latch Enable Input	LE
16	Right Channel Data Input	DATA (R)
17	Digital Common	DCOM
18	No Connect	NC
19	Right Channel Voltage Output	VOUT (R)
20	Right Channel Summing Junction	SJ (R)
21	Right Channel Analog Common	ACOM
22	Right Channel Current Output	IOUT (R)
23	Right Channel Bipolar Offset Decoupling Point	CAP
24	Right Channel MSB Adjustment	MSB ADJ (R)
25	Right Channel Servo-Amp Decoupling Point	CAP
26	MSB Adjustment Potentiometer Voltage Output	VPOT
27	+5V Analog Supply	$+V_{CC}$
28	Digital Common	DCOM

PIN ASSIGNMENTS (SOIC PKG)

PIN	DESCRIPTION	MNEMONIC
9	–5V Analog Supply	$-V_{CC}$
10	Left Channel Servo-Amp Decoupling Point	CAP
11	Left Channel MSB Adjustment	MSB ADJ (L)
19	No Connect	NC
12	Left Channel Bipolar Offset Decoupling Point	CAP
13	Left Channel Current Output	I_{OUT} (L)
14	Left Channel Analog Common	ACOM
15	Left Channel Summing Junction	SJ (L)
16	Left Channel Voltage Output	V_{OUT} (L)
17	No Connect	NC
18	+5V Digital Supply	$+V_{DD}$
20	Left Channel Data Input	DATA
21	Clock Input	CLOCK
22	–5V Logic Supply	$-V_{DD}$
23	Latch Enable Input	LE
24	Right Channel Data Input	DATA (R)
25	Digital Common	DCOM
26	No Connect	NC
27	Right Channel Voltage Output	V_{OUT} (R)
28	Right Channel Summing Junction	SJ (R)
1	Right Channel Analog Common	ACOM
2	Right Channel Current Output	I_{OUT} (R)
3	Right Channel Bipolar Offset Decoupling Point	CAP
4	Right Channel MSB Adjustment	MSB ADJ (R)
5	Right Channel Servo-Amp Decoupling Point	CAP
6	MSB Adjustment Potentiometer Voltage Output	V_{POT}
7	+5V Analog Supply	$+V_{DD}$
8	Digital Common	DCOM

NOTE: In the SOIC (PCM1700U) package, the die is rotated 90°. Therefore, the pin assignments are different from the DIP. See pin assignments on page 4 for details.

ORDERING INFORMATION

```
                                        PCM1700 ( ) ( )
Basic Model Number ——————————————————
    P: Plastic U: SOIC ————————————————
Performance Grade Code ————————————————
```

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages .... ±7.5VDC
Input Logic Voltage .... –1V to $+V_{CC}$
Power Dissipation 500mW
Operating Temperature .... –25°C to +70°C
Storage Temperature .... –60°C to +100°C
Lead Temperature (soldering, 10s) .... +300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1700U	28-Pin SOIC	217
PCM1700U,J	28-Pin SOIC	217
PCM1700U,K	28-Pin SOIC	217
PCM1700P	28-Pin Plastic DIP	126
PCM1700P,J	28-Pin Plastic DIP	126
PCM1700P,K	28-Pin Plastic DIP	126

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.
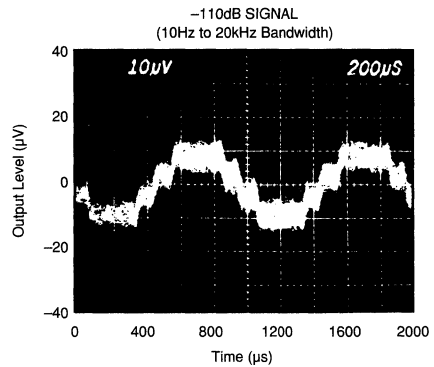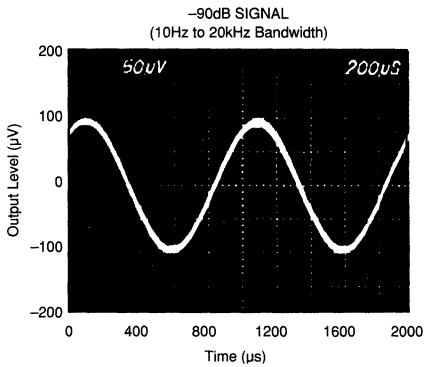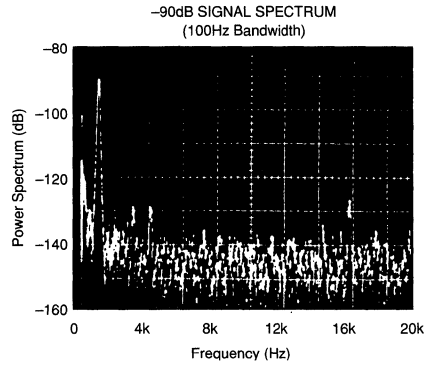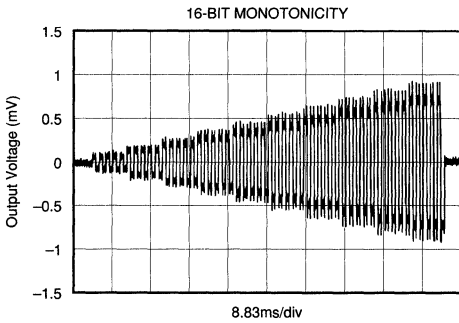
PCM1700

8.2

DIGITAL AUDIO PRODUCTS—D/A
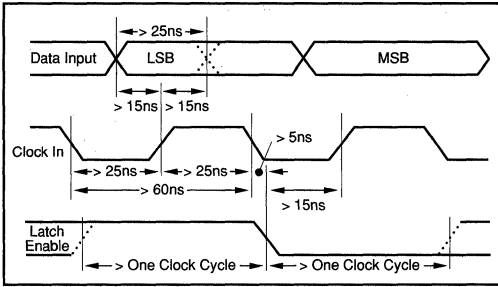
FIGURE 1. PCM1700P Setup and Hold Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+ FS	+2.99997711	–0.66999489
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	–0.00002289	+0.00000511
20000 Hex	– FS	–3.00000000	+0.67000000

TABLE I. PCM1700 Input/Output Relationships.
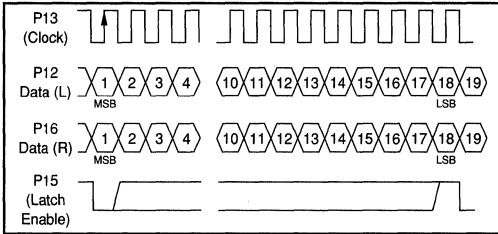
FIGURE 2. Timing Diagram.

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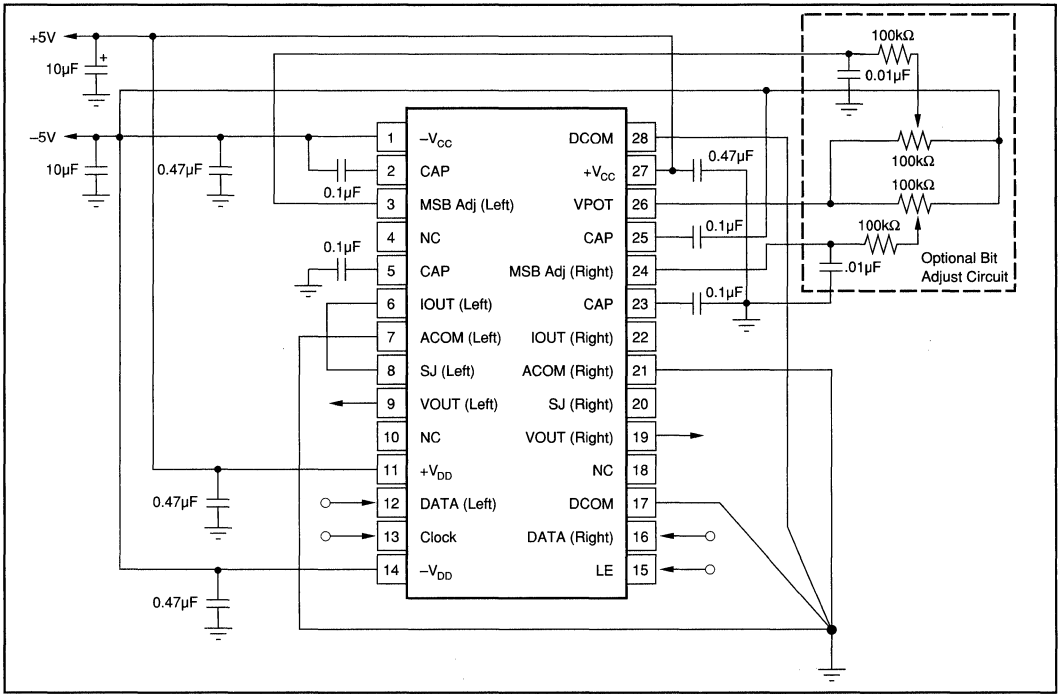
FIGURE 3. Voltage Output Connection Diagram (DIP Package Diagram.)
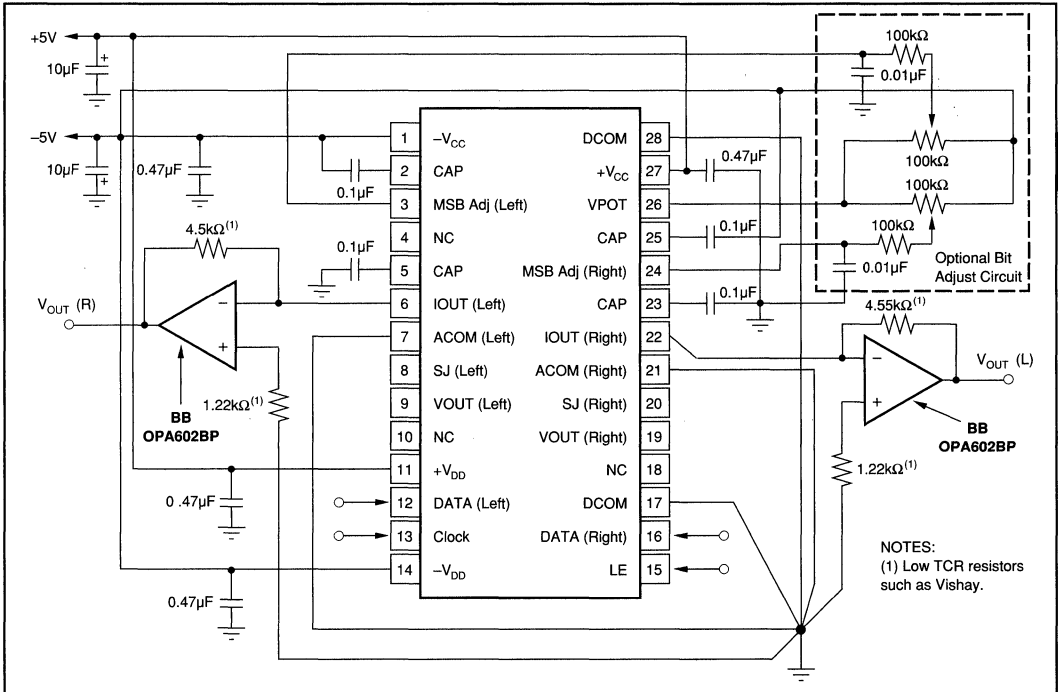
FIGURE 4. Current Output Connection Diagram (DIP Package Diagram.)

PCM1700

8.2

DIGITAL AUDIO PRODUCTS—D/A

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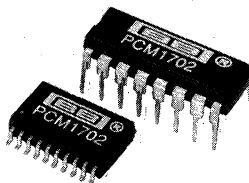
PCM1702P
PCM1702U

DEMO BOARD
AVAILABLE
See Appendix A for
more information.

BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **ULTRA LOW –96dB max THD + N** (No External Adjustment Required)
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **120dB SNR TYP (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT** (±1.2mA)
- **CAPABLE OF 16X OVERSAMPLING**
- **COMPLETE WITH REFERENCE**
- **LOW POWER (150mW typ)**

DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.

PDS-1175A

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SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, $\pm V_{CC}$ and $+V_{DD} = \pm 5V$ unless otherwise noted.

PARAMETER	CONDITIONS	PCM1702P/U, -J, -K MIN	PCM1702P/U, -J, -K TYP	PCM1702P/U, -J, -K MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale, with A-weight			110		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_{DD}$	V
V_{IL}		0		0.8	V
I_{IH}	$V_{IH} = +V_{DD}$			±10	µA
I_{IL}	$V_{IL} = 0V$			±10	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			12.5	20.0	MHz
TOTAL HARMONIC DISTORTION + N[2]					
P/U $\quad V_O = 0dB$	$f_S = 352.8kHz$, f = 1002Hz		–92	–88	dB
$V_O = -20dB$	$f_S = 352.8kHz$, f = 1002Hz		–82	–74	dB
$V_O = -60dB$	$f_S = 352.8kHz$, f = 1002Hz		–46	–40	dB
P/U, -J $\quad V_O = 0dB$	$f_S = 352.8kHz$, f = 1002Hz		–96	–92	dB
$V_O = -20dB$	$f_S = 352.8kHz$, f = 1002Hz		–83	–76	dB
$V_O = -60dB$	$f_S = 352.8kHz$, f = 1002Hz		–48	–42	dB
P/U, -K $\quad V_O = 0dB$	$f_S = 352.8kHz$, f = 1002Hz		–100	–96	dB
$V_O = -20dB$	$f_S = 352.8kHz$, f = 1002Hz		–84	–80	dB
$V_O = -60dB$	$f_S = 352.8kHz$, f = 1002Hz		–50	–44	dB
ACCURACY					
Level Linearity	At –90dB Signal Level		±0.5		dB
Gain Error			±0.5	±3	%
Bipolar Zero Error[5]			±0.25		%
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±5		ppm of FSR/°C
Warm-up Time			1		minute
IDLE CHANNEL SNR[6]	Bipolar Zero, A-weighted Filter	110	120		dB
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	(±0.003% of FSR, 1.2mA Step)		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
Supply Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.00	+5.25	V
$-V_{CC} = -V_{DD}$		–4.75	–5.00	–5.25	V
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5V$		+5.00	+9.0	mA
Combined Supply Current: $-I_{CC}$	$-V_{CC} = -V_{DD} = -5V$		–25.00	–41.0	mA
Power Dissipation	$\pm V_{CC} = \pm V_{DD} = \pm 5V$		150	250	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency (signal level). (4) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA627 and 5kΩ feedback and an A-weighted filter.

PCM1702

DIGITAL AUDIO PRODUCTS—D/A

8.2

ABSOLUTE MAXIMUM RATINGS (DIP Package)

Power Supply Voltage .... ±6.5VDC
Input Logic Voltage .... DGND—0.3V~+V_{DD}+0.3V
Operating Temperature .... −25°C to +85°C
Storage Temperature .... −55°C to +125°C
Power Dissipation 500mW
Lead Temperature (soldering, 10s) .... 260°C

ABSOLUTE MAXIMUM RATINGS (SOP Package)

Power Supply Voltage .... ±6.5VDC
Input Logic Voltage .... DGND—0.3V~+V_{DD}+0.3V
Operating Temperature .... −25°C to +85°C
Storage Temperature .... −55°C to +125°C
Power Dissipation 300mW
Lead Temperature (soldering, 5s) .... 260°C

PIN ASSIGNMENTS (DIP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	9	+V_{CC}
2	CLOCK	10	BPO DC
3	+V_{DD}	11	I_{OUT}
4	DCOM	12	ACOM
5	−V_{DD}	13	ACOM
6	LE	14	SERV DC
7	NC	15	REF DC
8	NC	16	−V_{CC}

PIN ASSIGNMENTS (SOP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	11	+V_{CC}
2	CLOCK	12	BPO DC
3	NC	13	NC
4	+V_{DD}	14	I_{OUT}
5	DCOM	15	ACOM
6	−V_{DD}	16	ACOM
7	LE	17	SERV DC
8	NC	18	NC
9	NC	19	RFE DC
10	NC	20	−V_{CC}

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1702P	16-Pin Plastic DIP	807
PCM1702U	20-Pin Plastic SOP	808

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

CONNECTION DIAGRAM

= SOP

= DIP

TYPICAL PERFORMANCE CURVES

All specifications at 25°C, $\pm V_A$ and $\pm V_D = \pm 5.0V$, unless otherwise noted.

THD + N vs FREQUENCY

(graph: THD +N (dB) vs Output Frequency (Hz), curves labeled −60dB, −40dB, −20dB, 0dB)

16-BIT LEVEL LINEARITY
(Dithered Fade-to-Noise)

(graph: Deviation from Ideal Level (dB) vs Output Signal Level (dB))

16-BIT MONOTONICITY

(graph: Output Voltage (mV) vs 8.83ms/div)

−90dB SIGNAL SPECTRUM
(100Hz Bandwidth)

(graph: Power Spectrum (dB) vs Frequency (Hz))

−90dB SIGNAL
(10Hz to 20kHz Bandwidth)

(graph: Output Level (µV) vs Time (µs), 50uV, 200uS)

−110dB SIGNAL
(10Hz to 20kHz Bandwidth)

(graph: Output Level (µV) vs Time (µs), 10µV, 200µS)

PCM1702

8.2
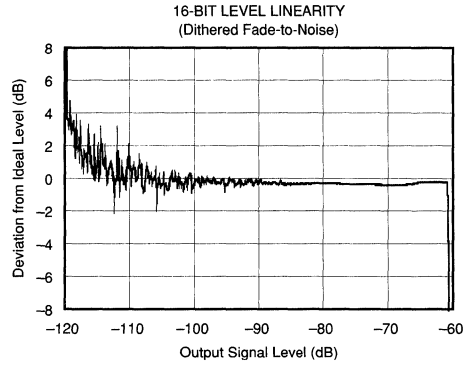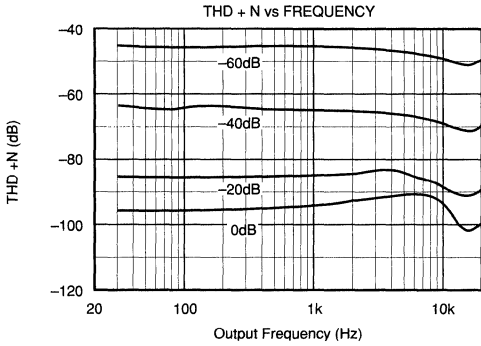
DIGITAL AUDIO PRODUCTS—D/A

THEORY OF OPERATION

ADVANCED SIGN MAGNITUDE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However, even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high over-sampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DAC). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM1702 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference, and a common R-2R ladder for bit current sources by dual balanced current segments to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or advanced sign magnitude approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM1702 is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table 1 shows the conversion made by the internal logic of the PCM1702 from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM1702 in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specifications for the PCM1702 is total harmonic distortion plus noise (THD + N).

Digital data words are read into the PCM1702 at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 1002Hz is realized.

For production testing, the output of the DAC goes to an I to V converter, then through a 40kHz low pass filter, and then to a programmable gain amplifier to provide gain at lower signal output test levels before being fed into an analog-type distortion analyzer. Figure 1 shows a block diagram of the production THD + N test setup.

For the audio bandwidth, THD + N of the PCM1702 is essentially flat for all frequencies. The typical performance curve, "THD + N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low level signal performance of the advanced sign magnitude architecture of the PCM1702.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS}/ Signal_{RMS}$ expressed in dB. For the PCM1702, THD + N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD + N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The advanced sign magnitude architecture of the PCM1702, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111+1LSB[1]	111...111
+Full Scale –1LSB	011...110	111...111+1LSB[1]	111...110
Bipolar Zero +2LSB	000...010	111...111+1LSB[1]	000...010
Bipolar Zero +1LSB	000...001	111...111+1LSB[1]	000...001
Bipolar Zero	000...000	111...111+1LSB[1]	000...000
Bipolar Zero –1LSB	111...111	111...111	000...000
Bipolar Zero –2LSB	111...110	111...110	000...000
–Full Scale +LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000
NOTE: (1) The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.			

TABLE I. Binary Two's Complement to Sign Magnitude Conversion Chart.
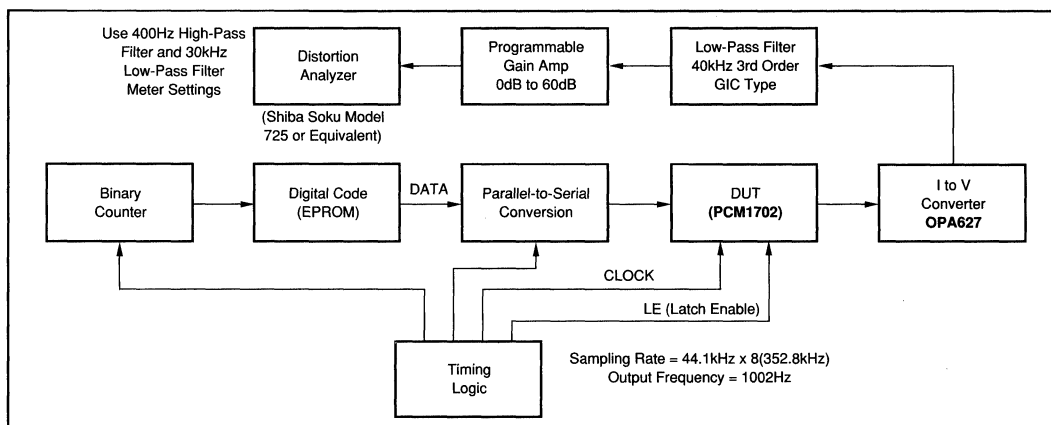
FIGURE 1. Production THD + N Test Setup.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM1702 at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM1702 at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal.

This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM1702 advanced sign magnitude.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased form –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM1702 tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATION

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero, while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM1702 is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique advanced sign magnitude architecture of the PCM1702, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below· zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM1702, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bit-stream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM1702, the extremely low THD + N performance is typically indicative of 17-bit integral linearity in the DAC. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, and Temperature Drift

Although the PCM1702 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM1702 accepts TTL compatible logic input levels. The data format of the PCM1702 is binary two's complement (BTC) with the most significant bit (MSB) being first

PCM1702

8.2

DIGITAL AUDIO PRODUCTS—D/A

in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after Latch Enable (Pin6 <PCM1702P>, Pin7 <PCM1702U>, LE) has gone low.

All DAC serial input data (Pin1, DATA) bit transfers are triggered on positive clock (Pin2, CLOCK), edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable. The change in the output of the DAC occurs at a rising edge of the 4th clock of the CLOCK after the falling edge of Latch Enable. Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM1702 is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X over-sampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM1702 is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT
1,048,576LSBs	Full Scale Range	2.40000000mA
1LSB	NA	2.28882054nA
7FFFF$_{HEX}$	+Full Scale	-1.19999771mA
00000$_{HEX}$	Bipolar Zero -1LSB	0.00000000mA
80000$_{HEX}$	-Full Scale	+1.20000000mA

TABLE II. Digital Input/Output Relationships.

INSTALLATION

POWER SUPPLIES

Refer to CONNECTION DIAGRAM for proper connection of the PCM1702. The PCM1702 only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in CONNECTION DIAGRAM regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM1702 as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in CONNECTION DIAGRAM, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM1702 as possible to reduce noise pickup from surrounding circuitry.
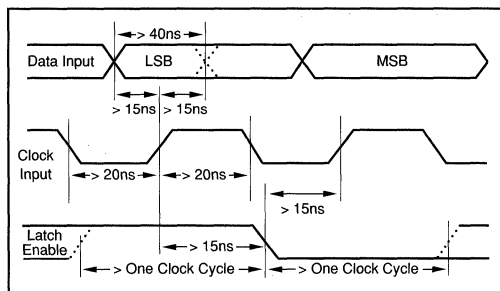
FIGURE 3. Setup and Hold Timing Diagram.
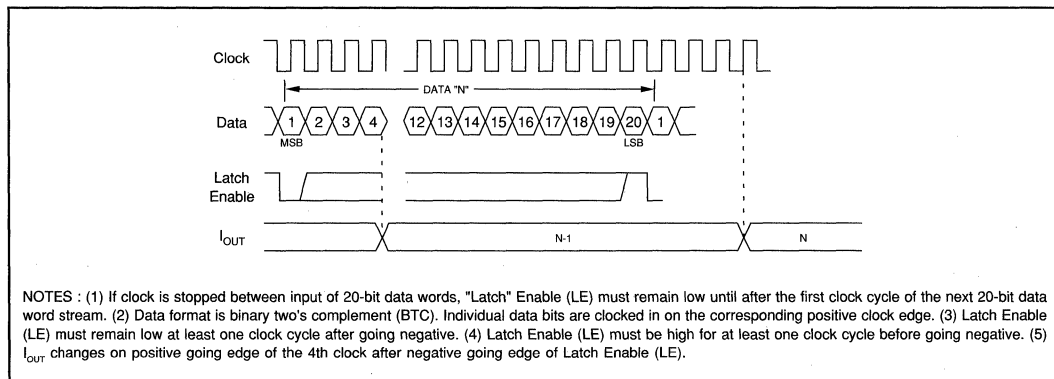
NOTES : (1) If clock is stopped between input of 20-bit data words, "Latch" Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I$_{OUT}$ changes on positive going edge of the 4th clock after negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.
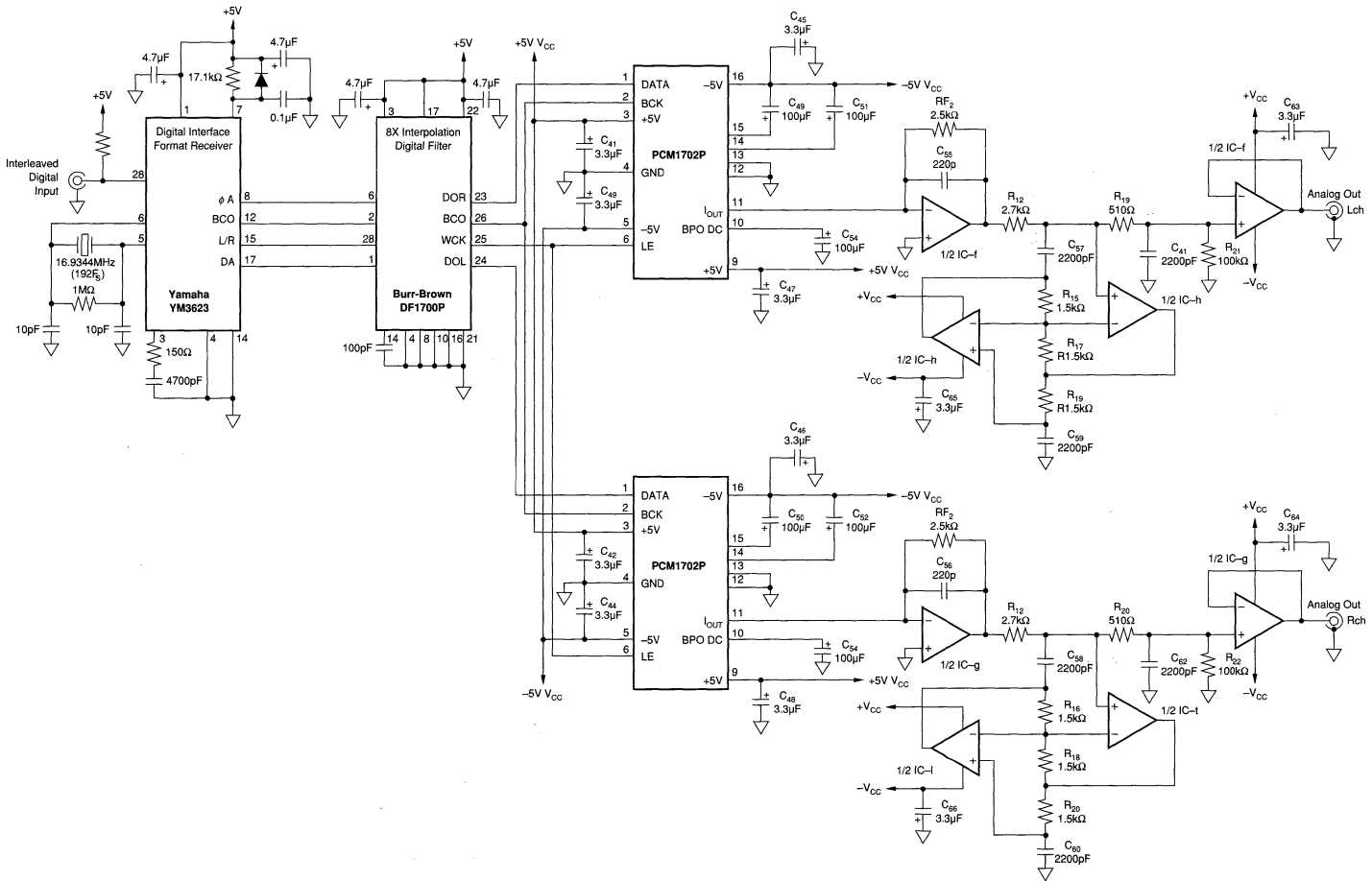
FIGURE 4. Typical Application for Stereo Audio 8X Oversampling system.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

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8.2.115

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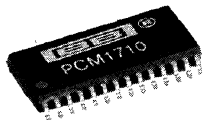
PCM1710U

DEMO BOARD
AVAILABLE
See Appendix A for
more information.

Dual Voltage Output CMOS Delta-Sigma
DIGITAL-TO-ANALOG CONVERTER
With On-Chip Digital Filter

FEATURES

● **DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER**

● **HIGH PERFORMANCE:**
  THD+N: 0.0025% typ
  Dynamic Range: 98dB typ
  S/N RATIO: 110dB typ

● **ANALOG VOLTAGE OUTPUT:**
  V_O = 3.2Vp-p

● **ON-CHIP POST ANALOG LOW PASS FILTER**

● **SYSTEM CLOCK 256fs or 384fs**

● **ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH:**
  Soft Mute and Attenuator
  Digital De-Emphasis
  Double Speed Dubbing Mode

● **SINGLE +5V POWER SUPPLY**

● **SMALL 28-PIN SOIC PACKAGE**

DESCRIPTION

The PCM1710 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1710 is a unique multi-level 4th-order Delta-Sigma architecture that eliminates influence from input clock jitter and RF interferance resulting in truly superior performance.

The PCM1710 will accept 16- and 20-bit input data as well as normal/IIS (1/fs, 32 clock, continuous data) format data.

The on-chip digital filter of the PCM1710 has –62dB stop band attenuation and ±0.008dB ripple in the pass band.

The PCM1710 can be used in a wide variety of consumer audio applications. Its low cost, small size, and signal +5V operation make it ideal for portable, automotive, CD players, BS tuners, music instruments, and other digital audio applications.

Block diagram: Digital In → Input Interface and Attenuator → Oversampling Digital Filter → 4th-Order Multi-Level Delta Sigma → DAC → Low-Pass Filter → Output Op Amp → Lch OUT / Rch OUT. Mode Control feeds the Input Interface; System Clock feeds the Oversampling Digital Filter.
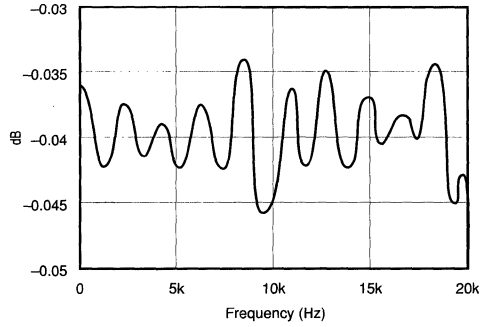
PDS-1217

BURR-BROWN®

SPECIFICATIONS

ELECTRICAL

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, f_{SYS} = 384/256fs, and 16-bit data, unless otherwise noted.

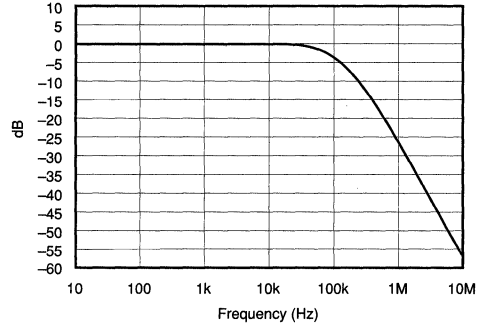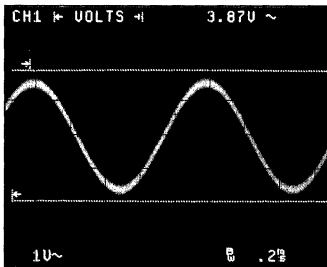| PARAMETER	CONDITIONS	PCM1710U MIN	PCM1710U TYP	PCM1710U MAX	UNITS
RESOLUTION		16		20	Bits
DIGITAL INPUT					
Logic Family					
Input Logic Level (except XTi)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (except XTi)				–200	μA
Input Logic Level (XTi)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTi)				±50	μA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current (CLKO)		±10			mA
Data Format		Normal/IIS (16-Bit only) selectable			
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	384fs	12.288	16.934	18.432	MHz
System Clock Frequency	256fs	8.192	11.2894	12.288	MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	$V_O = 1/2V_{CC}$ at Bipolar Zero		±20.0		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE					
THD+N at F/S (0dB)[1]	f_{IN} = 991kHz		–92	–88	dB
THD+N at –60fdB[1]	f_{IN} = 991kHz		–36	–32	dB
Dynamic Range	EIAJ A-weighted	92	98		dB
S/N Ratio	EIAJ A-weighted	104	110		dB
Channel Separation		90	94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple	Normal Mode		±0.008		dB
Pass Band Ripple	Double Speed Mode		±0.018		dB
Stop Band Attenuation	Normal Mode		–62		dB
Stop Band Attenuation	Double Speed Mode		–58		dB
Pass Band	Normal Mode		0.4535		fs
Pass Band	Double Speed Mode		0.4535		fs
Stop Band	Normal Mode		0.5465		fs
Stop Band	Double Speed Mode		0.5465		fs
De-emphasis Error	(fs 32kHz ~ 48kHz)	–0.53		+0.84	dB
ANALOG OUTPUT					
Voltage Range			3.2		Vp-p
Load Impedance		5			kΩ
Center Voltage			$+1/2V_{CC}$		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current $+I_{CC} +I_{DD}$			45	70	mA
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) 30kHz LPF, 400Hz HPF, Average Mode.

PCM1710

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DIGITAL AUDIO PRODUCTS—D/A

PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	LRCIN	Sample Rate Clock Input (fs)
2	DIN	Data Input
3	BCKIN	Bit Clock Input
4	CLKO	Buffered Output of Oscillator
5	XTI	Oscillator Input (External Clock Input)
6	XTO	Oscillator Output
7	DGND	Digital Ground
8	V_{DD}	Digital Power Supply (+5V)
9	$V_{CC}2R$	Analog (DAC) +V_{CC}, Rch
10	AGND 2R	Analog (DAC) Ground, Rch
11	EXT1R	Output Amp Common, Rch
12	EXT2R	Output Amp Bias, Rch
13	$V_{OUT}R$	Rch Analog Output
14	AGND	Analog Ground

PIN	NAME	FUNCTION
15	V_{CC}	Analog Power Supply (+5V)
16	$V_{OUT}L$	Lch Analog Output
17	EXT2L	Output Amp Bias, Lch
18	EXT1L	Output Amp Common, Lch
19	AGND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) +V_{CC}, Lch
21	V_{DD}	Digital Power Supply, (+5V)
22	DGND	Digital Ground
23	CKSL	System Clock Select (H:384fs, L:256fs)
24	MODE	Operation Mode Select, (H: Serial, L: Parallel)
25	MUTE	Mute Control (H:OFF, L:ON)
26	MD/DM1	Mode Control, Data/De-emphasis selection
27	MC/DM2	Mode Control, BCK/De-emphasis selection
28	ML/DSD	Mode Control, WDCK/Double speed selection

NOTE: All input pins require pull up resistors.
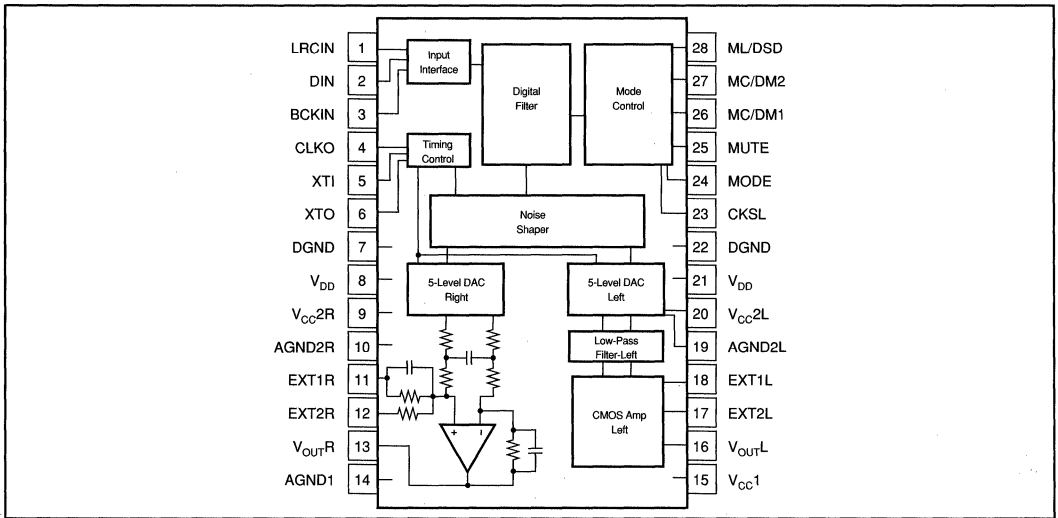
PIN CONFIGURATION

CONNECTION DIAGRAM
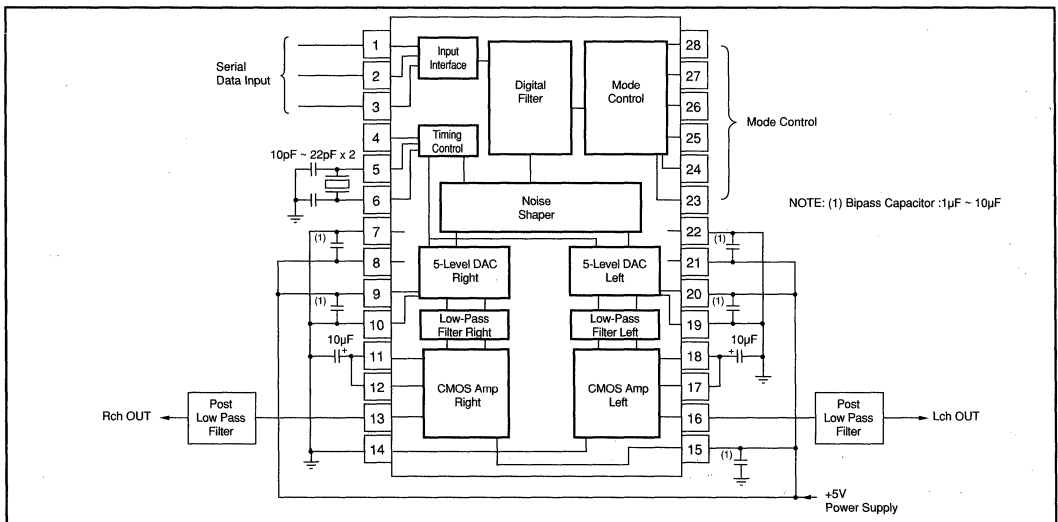
NOTE: (1) Bipass Capacitor :1µF ~ 10µF
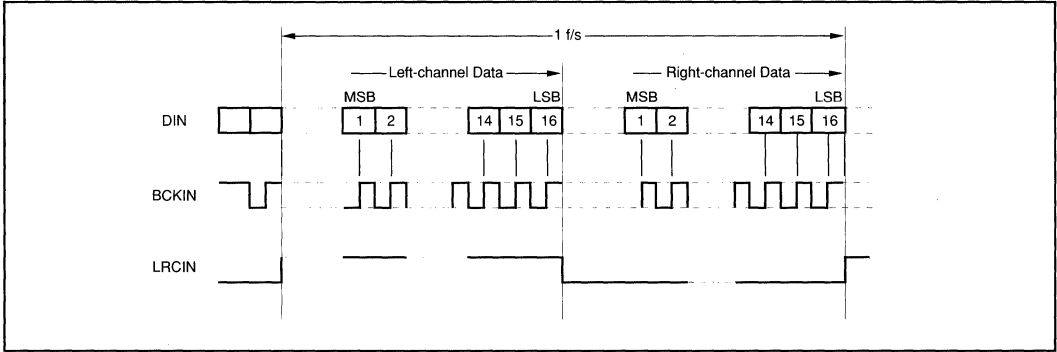
DATA INPUT TIMING

FIGURE 1. Normal Format, 16-Bit (LRCIN H: Lch).
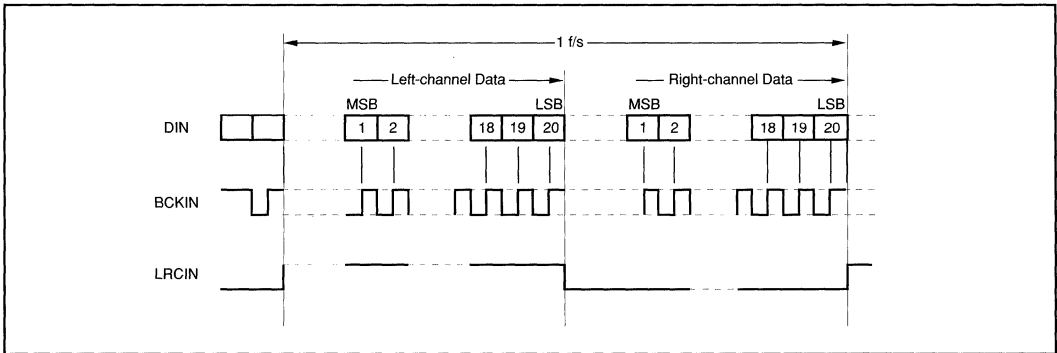
FIGURE 2. Normal Format, 20-Bit (LRCIN H: Lch).
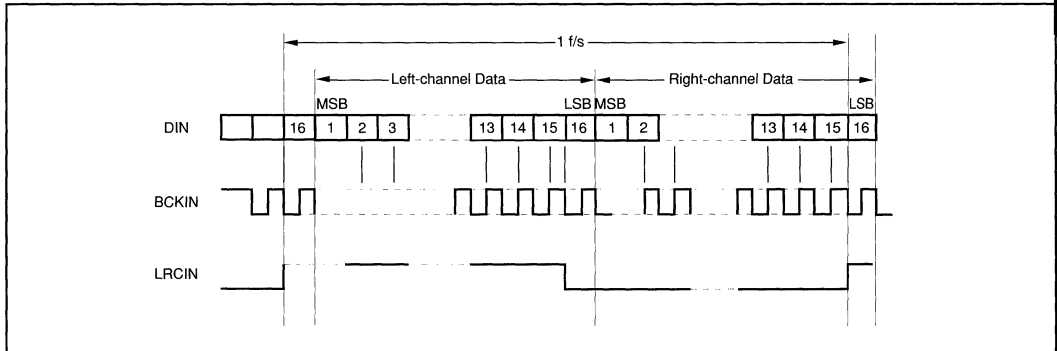
FIGURE 3. IIS Format, (16-bit Only).

PCM1710

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DIGITAL AUDIO PRODUCTS—D/A
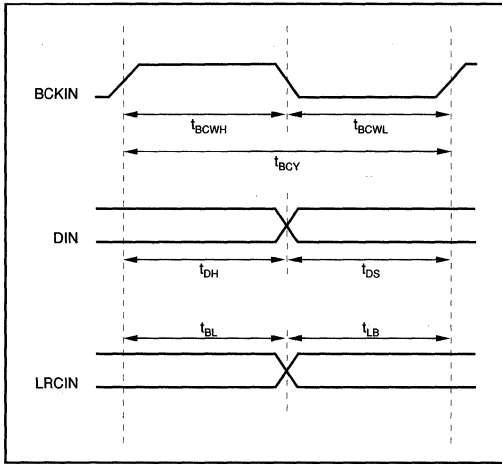
FIGURE 4. Data Input Timing.
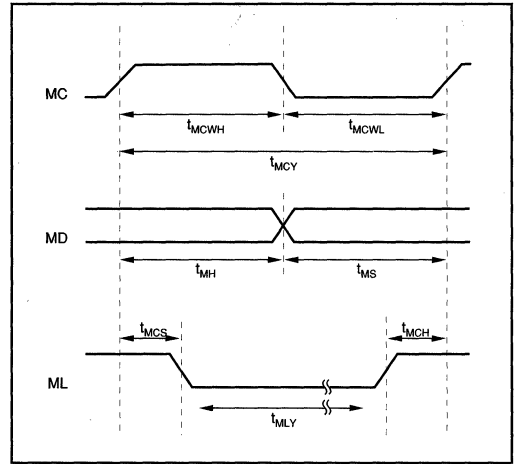
FIGURE 5. Serial Mode Control Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level)	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRC I Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE I. Data Input Timing Specifications.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

TABLE II. Serial Mode Control Timing Specifications.

TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, f_{SYS} = 384/256fs, and 16-bit data, unless otherwise noted.

DIGITAL FILTER

OVERALL FREQUENCY CHARACTERISTIC
NORMAL MODE (De-Emphasis: OFF)

PASSBAND RIPPLE CHARACTERISTIC
NORMAL MODE (De-Emphasis: OFF)

OVERALL FREQUENCY CHARACTERISTIC
DOUBLE SPEED MODE (De-Emphasis: OFF)
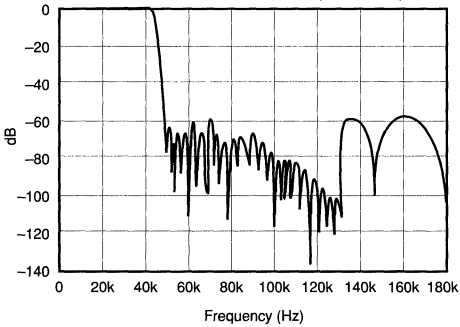
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
DOUBLE SPEED MODE (De-Emphasis: OFF)
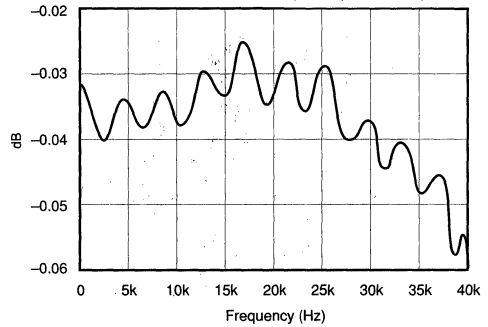
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
DOUBLE SPEED MODE (De-Emphasis: OFF)

DE-EMPHASIS CHARACTERISTIC, NORMAL MODE

PCM1710

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DIGITAL AUDIO PRODUCTS—D/A

TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, $f_{SYS} = 384/256fs$, and 16-bit data, unless otherwise noted.

ANALOG FILTER

SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(20Hz~24kHz, Expanded Scale)

SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(10Hz~10MHz)

OUTPUT WAVE FORM FULL SCALE SIGNAL
(Without External Filter)

MODE CONTROL FUNCTION

The digital functions of PCM1710 are capable of Parallel Mode and Serial Mode. Control functions of both modes are shown below.

MODE CONTROL: SERIAL/PARALLEL SELECTION

MODE = H	Serial Mode
MODE = L	Parallel Mode

TABLE III. Serial and Parallel Mode are Selectable by MODE Pin (Pin 24).

MODE CONTROL: SELECTABLE FUNCTIONS

FUNCTION	SERIAL MODE (MODE = H)	PARALLEL MODE (MODE = L)
Input Data Format Selection	0	X(Normal Mode Fixed)
Input Data Bit Selection	0	X(16-bit Fixed)
Input LRCI Polarity Selection	0	X
De-emphasis Control	0	0
Mute	0	0
Attenuation	0	X
Double Speed Dubbing	0	0
NOTE: 0: Selectable, X: Not Selectable.		

TABLE IV. Selectable Functions in Serial Mode and Parallel Mode.

PARALLEL-MODE: DE-EMPHASIS CONTROL (MODE: L, PIN 24)

DM1 (Pin 26)	DM2 (Pin 27)	De-emphasis
L	L	OFF
H	L	32kHz
L	H	48kHz
H	H	44.1kHz

TABLE V. De-emphasis (Pins 26 and 27).

PARALLEL-MODE: DOUBLE SPEED DUBBING CONTROL (MODE: L, PIN 24)

DSD = H	Normal Mode
DSD = L	Double Speed Dubbing Mode
NOTE: When the Double-Speed Dubbing Mode is selected, the System Clock must be 384fs (CKSL: Pin 23 = H).	

TABLE VI. DSD (Pin 28).

WARNING: When the PARALLEL-MODE is selected, the De-emphasis must be OFF (Pin 26 = L, Pin 27 = L), the Normal Mode must be selected (Pin 28 = H), and the MUTE must be OFF (Pin 5 = H).

SERIAL-MODE CONTROL INPUT FORMAT (MODE: H, PIN 24)

	B0	B1	B2	BITS	MODE FLAG	FUNCTION MODE SELECTION MODE	LH	SELECTED FUNCITON		MODE BY RESET
Mode 1	H	L	L	3	DEEM2			DEEM2		44.1kHz
				4	DEEM1	Sampling Frequency for De-emphasis		DEEM1 0 — 48kHz / 1 32kHz 44.1kHz — 0 1		
				5	IIR	De-emphasis	L	De-emphasis OFF		0
							H	De-emphais ON		
				6	MUTE	Mute	L	Mute OFF		0
							H	Mute ON		
				7	DSD	Double Speed	L	Double-speed OFF		0
							H	Double-speed ON		
Mode 2	H	L	H	3		Not Assigned				
				4	TST	Test Mode	H	Normal "H"		0
				5	IW	Input Resolution	L	16-Bit		0
							H	20-Bit		
				6	LRPL	Polarity for LRCI	L	Lch:high/Rch:low		0
							H	Lch:low/Rch:high		
				7	IIS	Input Format	L	Normal		0
							H	IIS		

TABLE VII. Mode Controls in Serial Mode.

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PCM1710

DIGITAL AUDIO PRODUCTS—D/A

SERIAL MODE CONTROL INPUT FORMAT (MODE: H, Pin 24)

NOTES: (1) Cycle Time for Mode Control — Cycle time for mode control must be set over 128 times of minimum system clock. (2) Attenuator Operation — ATT data D6 and D0 are MSB and LSB, respectively. Attenuation level can be controlled using the following equation:

$$\text{Attenuation Level} = 20 \times \text{LOG}_{10}(1\text{-ATT\_DATA}/127) \text{ (dB)}.$$

Only, in the case of ATT_DATA = 127, attenuation level become minus infinity. (3) Soft Mute Operation — Attenuation level gradually decreases to minus infinity from current level by muting turned-on and increased to previous level by muting turned-off. The signal is completely muted after 127/fs seconds. Mute pin must be set "H" or open for serial interface case.

FIGURE 6. Mode Control Input Format, Serial Mode.

SYSTEM CLOCK
IN NORMAL/DOUBLE SPEED MODE

The system clock frequency must be fixed at 16.9344MHz in both Normal and Double Speed Dubbing Mode. When the sampling frequency entered to LRCIN is named as "fs", the selection of system clock is shown as the below table.

PARAMETER	ML/DSD (Pin 28)	
	H (Normal)	L (Double Speed)
XTI Input Clock Frequency	384fs	192fs
XTI Frequency	16.9344MHz (fs = 44.1kHz)	16.9344MHz (fs = 88.2kHz)
CLKO Output Clock Frequency	384fs	192fs

TABLE VIII.

EXTERNAL SYSTEM CLOCK CONDITION

An external clock (input to XT1), must meet the following conditions.

HIGH LEVEL	$V_{IH} > 0.64V_{DD}$	$T_H > /0\text{ns}$
LOW LEVEL	$V_{IL} < 0.28V_{DD}$	$T_L > /0\text{ns}$

TABLE VIII.
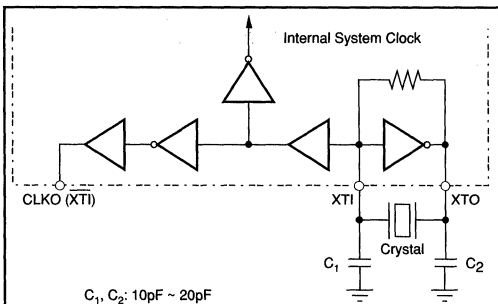
FIGURE 7. External Crystal Oscillator.
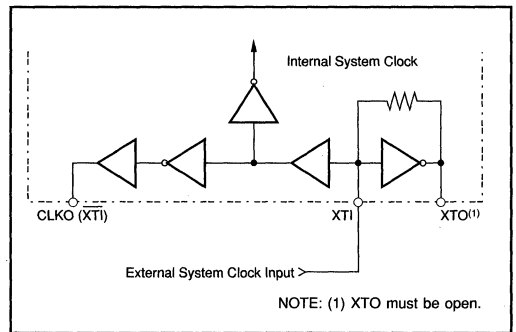
FIGURE 8. External System Clock.

WARNING: If the external clock is removed and accompanied by a noise spike (as might be caused by a mechanical switch), the operation of the PCM1710 may stop. Operation can be recovered by cycling the power supply off and then on again.

INFINITY ZERO DETECT

The PCM1710 monitors the Input Data and Bit Clock. When the Input Data is continuously "zero" for 8192 cycles of the Bit Clock, the Infinity Zero Detect occurs and the DAC outputs are set to BPZ ($1/2V_{CC}$).

When the Input Data is no longer "zero", the Infinity Zero Detect is released.

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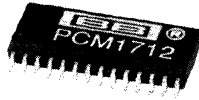
PCM1712U

ADVANCED INFORMATION
SUBJECT TO CHANGE

Dual Voltage Output CMOS Delta-Sigma 16-Bit DIGITAL-TO-ANALOG CONVERTER With On-Chip Digital Filter

FEATURES

- **DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER**
- **HIGH PERFORMANCE:**
  THD+N: 0.0045% (–87dB) typ
  Dynamic Range: 91dB typ
  S/N RATIO: 106dB typ
- **ANALOG VOLTAGE OUTPUT:**
  $V_O = 3.10Vp\text{-}p$
- **ON-CHIP ANALOG LOW PASS FILTER**
- **JITTER TOUGH AND LOW RADIO-FREQUENCY INTERFERENCE ENERGY ARCHITECTURE**
- **SYSTEM CLOCK 384fs**
- **ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH MULTI FUNCTIONS:**
  Double Speed Dubbing Mode
  Soft Mute and Attenuator
  Digital De-Emphasis
- **SINGLE +5V POWER SUPPLY OPERATION**
- **SMALL 28-PIN SOIC PACKAGE**

DESCRIPTION

The PCM1712 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1712 is a unique multi-level 3rd-order Delta-Sigma architecture that eliminates influence from input clock jitter and RF interference resulting in truly superior performance.

The PCM1712 will accept 16-bit input data as well as normal/IIS (32BCK/fs, continuous 16-bit data) format data.

The on-chip digital filter of the PCM1712 has –35dB stop band attenuation and ±0.17dB ripple in the pass band.

The PCM1712 can be used in a wide variety of consumer audio applications. Its low cost, small size, and single +5V operation make it ideal for portable, automotive, CD players, BS tuners, music instruments, games, and other digital audio applications.

PCM1712

8.2

DIGITAL AUDIO PRODUCTS—D/A

Lch/Rch ATT Control

Digital In ○— [Input Interface and Attenuator] → [Oversampling Digital Filter] → [3rd-Order Multi-Level Delta Sigma] → [DAC] → [Low-Pass Filter] → [Output Op Amp] —○ Lch OUT / —○ Rch OUT

Mode Control   System Clock

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SPECIFICATIONS

ELECTRICAL

All specifications at +25°C, +V$_{CC}$ = +V$_{DD}$ = +5V, fs = 44.1kHz, and 16-bit data, SYSCLK = 384fs, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1712U			UNITS
		MIN	TYP	MAX	
RESOLUTION			16		Bits
DIGITAL INPUT/OUTPUT					
Logic Family					
Input Logic Level (except XTI)					
V$_{IH}$		2.0			VDC
V$_{IL}$				0.8	VDC
Input Logic Current (except XTI)					
I$_I$				200	µA
Input Logic Level (XTI)					
V$_{IH}$		3.2			VDC
V$_{IL}$				1.4	VDC
Input Logic Current (XTI)					
I$_I$				±50	µA
Output Logic Level (CLKO):					
V$_{OH}$		4.5			VDC
V$_{OL}$				0.2	VDC
Output Logic Current					
I$_O$		±10			mA
Data Format		Normal/IIS (see Timing) SELECTABLE			
Data Bit		16-Bit/MSB First, Two's Complements			
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	384fs	12.288	16.934	18.432	MHz
DC ACCURACY					
Gain Error			±5.0		% of FSR
Gain Mis-Match Channel-To-Channel			±5.0		% of FSR
Bipolar Zero Error	V$_O$ = 1/2V$_{CC}$ at Bipolar Zero		±20		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE[1]					
THD+N at F/S (0dB)	f$_{IN}$ = 991Hz		–87		dB
THD+N at –60fdB	f$_{IN}$ = 991kHz		–31		dB
Dynamic Range	EIAJ A-weighted		91		dB
S/N Ratio	EIAJ A-weighted		106		dB
Channel Separation	f$_{IN}$ = 991Hz		90		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple[1]	Normal Mode		±0.17		dB
Pass Band Ripple[2]	Double Speed Mode		±0.23		dB
Stop Band Attenuation[1]	Normal Mode		–36		dB
Stop Band Attenuation[2]	Double Speed Mode		–35		dB
Pass Band[1]	Normal Mode		0.4535		fs
Pass Band[2]	Double Speed Mode		0.4535		fs
Stop Band[1]	Normal Mode		0.5465		fs
Stop Band[2]	Double Speed Mode		0.5465		fs
De-emphasis Error	(fs 32kHz ~ 48kHz)	–0.2		+0.55	dB
ANALOG OUTPUT					
Voltage Range	F/S(0dB)OUT		3.10		Vp-p
Load Impedance		5K			Ω
Center Voltage			+1/2V$_{CC}$		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: +V$_{CC}$		+4.5	+5.0	+5.5	VDC
+V$_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current +I$_{CC}$ +I$_{DD}$	+V$_{CC}$ = +V$_{DD}$ = +5.0V		45		mA
Power Dissipation	+V$_{CC}$ = +V$_{DD}$ = +5.0V		225		mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) Meter 400Hz HPF, 30kHz LPF On, Average Mode. (2)??

PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	LRCIN	Sample Rate Clock Input (fs)
2	DIN	Data Input
3	BCKIN	Bit Clock Input
4	CLKO	Buffered Output of Oscillator
5	XTI	Oscillator Input (External Clock Input)
6	XTO	Oscillator Output
7	DGND	Digital Ground
8	V_{DD}	Digital Power Supply (+5V)
9	$V_{CC}2R$	Analog (DAC) $+V_{CC}$, Rch
10	AGND2R	Analog (DAC) Ground, Rch
11	EXT1R	Output Amp Common, Rch
12	EXT2R	Output Amp Bias, Rch
13	$V_{OUT}R$	Rch Analog Output
14	AGND	Analog Ground

PIN	NAME	FUNCTION
15	V_{CC}	Analog Power Supply (+5V)
16	$V_{OUT}L$	Lch Analog Output
17	EXT2L	Output Amp Bias, Lch
18	EXT1L	Output Amp Common, Lch
19	AGND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) $+V_{CC}$, Lch
21	V_{DD}	Digital Power Supply, (+5V)
22	DGND	Digital Ground
23	NC	No Connection
24	MODE	Operation Mode Select, (H: Serial, L: Parallel)
25	MUTE	Mute Control (H:OFF, L:ON)
26	MD/DM1	Mode Control, Data/De-emphasis selection
27	MC/DM2	Mode Control, BCK/De-emphasis selection
28	ML/DSD	Mode Control, WDCK/Double speed selection

NOTE: (1) XTO (Pin 6) must be open when the external clock enter to XTI (Pin 5). (2) All input pins require pull up resistors.

PIN CONFIGURATION

LRCIN 1 — Input Interface
DIN 2
BCKIN 3
CLKO 4 — Timing Control
XTI 5
XTO 6
DGND 7
V_{DD} 8 — 5-Level DAC Right
$V_{CC}2R$ 9
AGND2R 10
EXT1R 11
EXT2R 12
$V_{OUT}R$ 13
AGND1 14

28 ML/DSD
27 MC/DM2
26 MC/DM1
25 MUTE
24 MODE
23 NC
22 DGND
21 V_{DD}
20 $V_{CC}2L$
19 AGND2L
18 EXT1L
17 EXT2L
16 $V_{OUT}L$
15 $V_{CC}1$

Digital Filter — Mode Control — Noise Shaper — 5-Level DAC Left — Low-Pass Filter-Left — CMOS Amp Left

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage .... ±6.5VDC
$+V_{CC}$ to V_{DD} Voltage .... ±0.1V
Input Logic Voltage .... $-0.3V \sim V_{DD}+0.3V$
Power Dissipation 400mW
Operating Temperature Range .... $-25°C$ to $+85°C$
Storage Temperature Range .... $-55°C$ to $+125°C$
Lead Temperature (soldering, 5s) .... $+260°C$

PCM1712

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DIGITAL AUDIO PRODUCTS—D/A

CONNECTION DIAGRAM
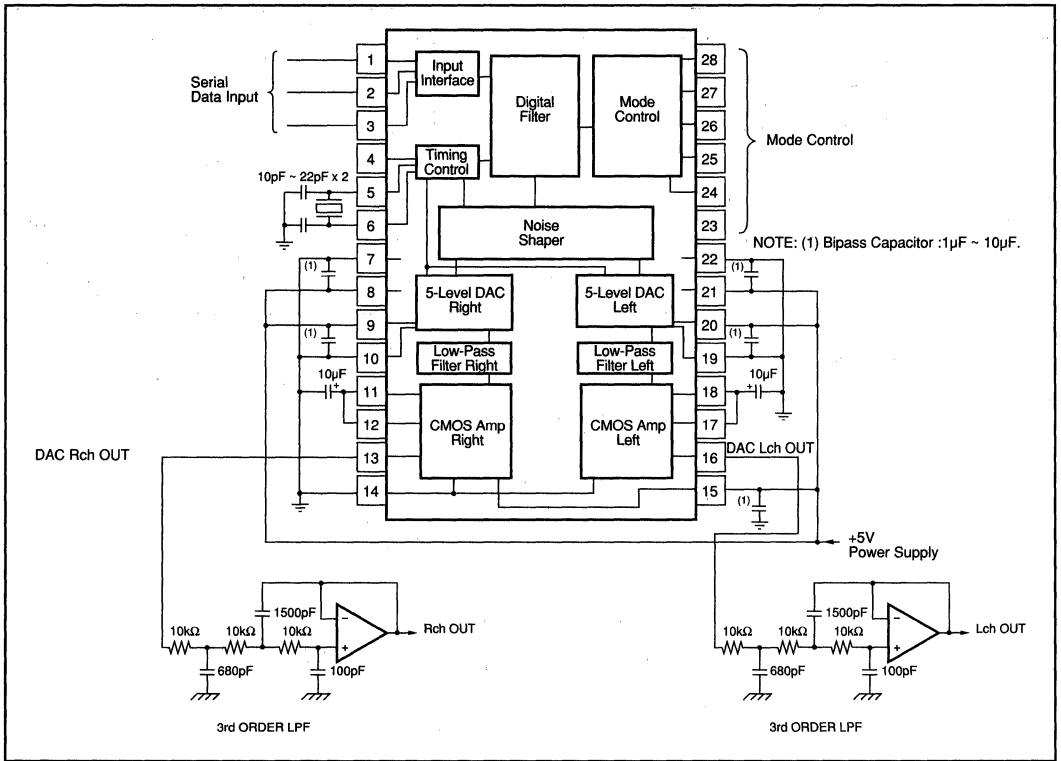
DATA INPUT TIMING

FIGURE 1. Normal Format, 16-Bit (LRCIN H: Lch).

FIGURE 2 . IIS Format, 16-Bit (32 BCKIN/fs, continuous data).

PCM1712

8.2

DIGITAL AUDIO PRODUCTS—D/A
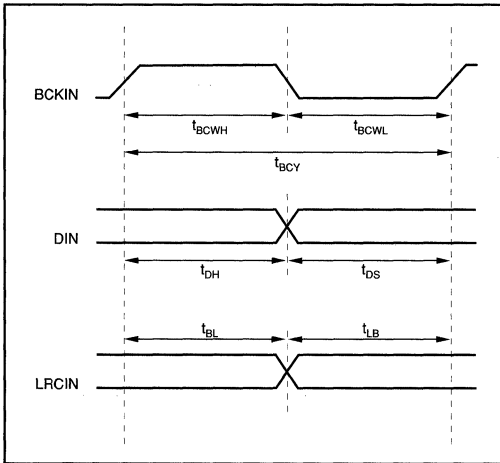
FIGURE 3. Data Input Timing.
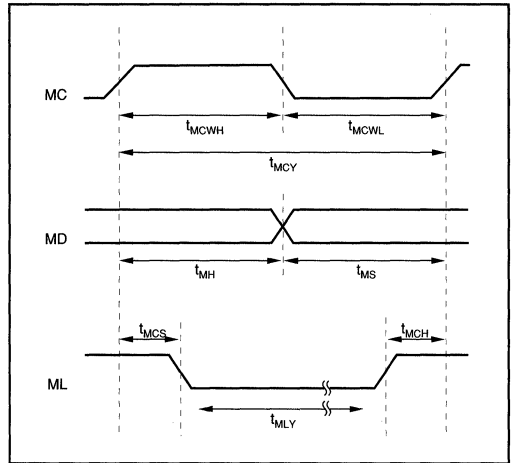
FIGURE 4. Serial Mode Control Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level)	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRC I Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE I. Data Input Timing Specifications.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

TABLE II. Serial Mode Control Timing Specifications.

TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, f_{SYS} = 384/256fs, and 16-bit data, unless otherwise noted.

DIGITAL FILTER

FREQUENCY RESPONSE

FREQUENCY RESPONSE

FREQUENCY RESPONSE

FREQUENCY RESPONSE

FREQUENCY RESPONSE

FREQUENCY RESPONSE

PCM1712

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DIGITAL AUDIO PRODUCTS—D/A

TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, +V_{CC} = +V_{DD} = +5V, fs = 44.1kHz, f_{SYS} = 384/256fs, and 16-bit data, unless otherwise noted.

ANALOG FILTER

SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(20Hz~24kHz, Expanded Scale)

SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(10Hz~10MHz)

MODE CONTROL FUNCTION

The digital functions of PCM1712 are capable of Parallel Mode and Serial Mode. Control functions of both modes are shown below.

MODE CONTROL: SERIAL/PARALLEL SELECTION

MODE = H	Serial Mode
MODE = L	Parallel Mode

TABLE III. Serial and Parallel Mode are Selectable by MODE Pin (Pin 24).

MODE CONTROL: SELECTABLE FUNCTIONS

FUNCTION	SERIAL MODE (MODE = H)	PARALLEL MODE (MODE = L)
Input Data Format Selection	0	X(Normal Mode Fixed)
Input Data Bit Selection	X(16-bit Fixed)	X(16-bit Fixed)
Input LRCI Polarity Selection	0	X
De-emphasis Control	0	0
Mute	0	0
Attenuation	0	X
Double Speed Dubbing	0	0
NOTE: 0: Selectable, X: Not Selectable.		

TABLE IV. Selectable Functions in Serial Mode and Parallel Mode.

PARALLEL-MODE: DE-EMPHASIS CONTROL (MODE: L, PIN 24)

DM1 (Pin 26)	DM2 (Pin 27)	De-emphasis
L	L	OFF
H	L	32kHz
L	H	48kHz
H	H	44.1kHz

TABLE V. De-emphasis (Pins 26 and 27).

PARALLEL-MODE: DOUBLE SPEED DUBBING CONTROL (MODE: L, PIN 28)

DSD = H	Normal Mode
DSD = L	Double Speed Dubbing Mode

TABLE VI. DSD (Pin 28).

SERIAL-MODE CONTROL INPUT FORMAT (MODE: H, PIN 24)

	B0	B1	B2	BITS	MODE FLAG	FUNCTION MODE SELECTION				MODE BY RESET
						MODE	LH	SELECTED FUNCTION		
Mode 1	H	L	L	3	DEEM2	Sampling Frequency for De-emphasis			DEEM2	44.1kHz
				4	DEEM1			DEEM1 0	0 1	
									48kHz	
								1	32kHz 44.1kHz	
				5	IIR	De-emphasis	L	De-emphasis OFF		0
							H	De-emphasis ON		
				6	MUTE	Mute	L	Mute OFF		0
							H	Mute ON		
				7	DSD	Double Speed	L	Double-speed OFF		0
							H	Double-speed ON		
Mode 2	H	L	H	3		Not Assigned				
				4	TST	Test Mode	H	Normal "H"		H
				5		Not Assigned				
				6	LRPL	Polarity for LRCI	L	Lch:high/Rch:low		0
							H	Lch:low/Rch:high		
				7	IIS	Input Format	L	Normal		0
							H	IIS		

TABLE VII. Mode Controls in Serial Mode.

PCM1712

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DIGITAL AUDIO PRODUCTS—D/A

NOTE: (1) Cycle Time for Mode Control: Cycle time for mode control must be set over 192 times of minimum system clock. (2) Attenuator Operation: ATT data D6 and D0 are MSB and LSB, respectively. Attenuation level can be controlled using the following equation; Attenuation Level = $20 \times LOG_{10}$ (1-ATT DATA/ 127) (dB). Only, in the case of ATT DATA = 127, attenuation level becomes minus infinity. (3) Soft Mute Operation: Attenuation level gradually decreased to minus infinity from current level by muting turned-on and increased to previous level by muting turned-off. The signal is completely muted after 127/fs seconds. Mute pin must be set "H" or open for serial interface case. (4) Infinity-Zero Detection: The PCM1712 has infinity-zero detect function. Internal detector is counting number of bit clock with infinity-zero data, if continue 8192 bit clock with infinity-zero data, output of DAC will be set Bipolar Zero (1/2 V_{CC}).

FIGURE 5. Mode Control Input Format, Serial Mode.

OPERATION INSTRUCTION FOR SYSTEM CLOCK

$V_{IH} > 0.64V_{DD}$
$V_{IL} < 0.28V_{DD}$
$T_H > 10ns$
$T_L < 10ns$

In case of system clock inputs to XTI from external, system clock should be input with the following condition.

FIGURE 6. Mode Control Input Format, Serial Mode.

C_1, C_2: 10pF ~ 20pF
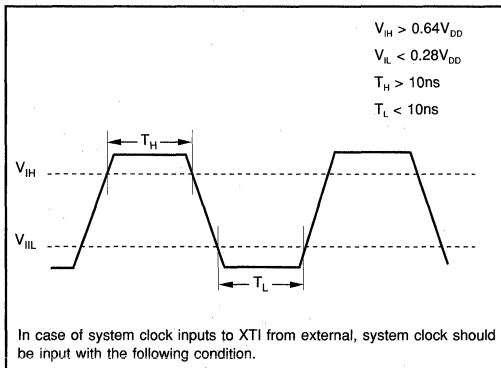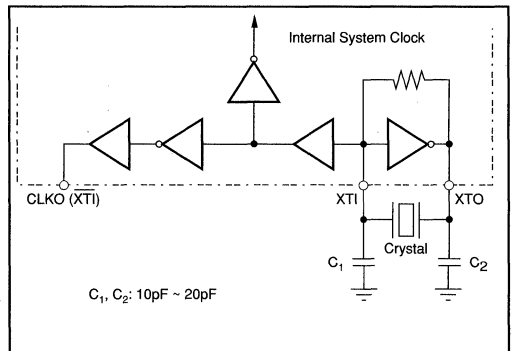
FIGURE 7. External Crystal Oscillator.

SYSTEM CLOCK
IN NORMAL/DOUBLE SPEED MODE

The system clock frequency must be fixed at 16.9344MHz in both Normal and Double Speed Dubbing Mode. When the sampling frequency entered to LRCIN is named as "fs", the selection of system clock is shown as the below table.

PARAMETER	DSD	
	H (Normal)	L (Double Speed)
XTI Input Clock Frequency	384fs	192fs
XTI Frequency	16.9344MHz (fs = 44.1kHz)	16.9344MHz (fs = 88.2kHz)
CLKO Output Clock Frequency	384fs	192fs

TABLE VIII.

NOTE: (1) XTO must be open.

FIGURE 8. External System Clock.

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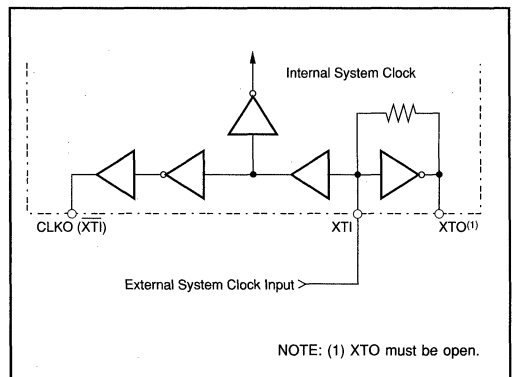
PCM1714U

ADVANCED INFORMATION
SUBJECT TO CHANGE

Dual Voltage Output, CMOS Delta-Sigma
DIGITAL-TO-ANALOG CONVERTER

FEATURES

● **NEW MULTI-LEVEL NOISE-SHAPING ARCHITECTURE**
● **HIGH PERFORMANCE:**
  THD+N: 0.0015% typ
  S/N RATIO: 104dB typ
  DYNAMIC RANGE: 102dB typ
● **DUAL CO-PHASE ANALOG VOLTAGE OUTPUT: 2.8Vp-p**
● **SELECTABLE 18-BIT/20-BIT INTERFACE**
● **VERSATILE SYSTEM CLOCK**
● **TTL LEVEL INPUT INTERFACE**
● **5V SINGLE POWER SUPPLY**
● **LOW POWER DISSIPATION**
● **SMALL 20-PIN SOIC PACKAGE**

DESCRIPTION

The PCM1714U is dual voltage output CMOS Delta-Sigma high performance DAC which is combined with a new Multi-Level Noise-shaping architecture and voltage output amplifier.

This new architecture and internal output amplifier in the PCM1714U provides a clean analog output signal with lower jitter and lower RFI sensitivity than the typical 1-bit DAC.

The PCM1714U accepts 18-bit or 20-bit, MSB first, serial data (Lch/Rch parallel). The PCM1714U does not use forced mute by zero detection which is used by typical 1-bit DAC. The PCM1714U offers very low noise and linear D/A conversion in demanding situations such as fade out signal on electronic piano or music instruments.

PCM1714U

8.2

DIGITAL AUDIO PRODUCTS—D/A

SYSTEMCLOCK
BCK
WDCK → INPUT INTERFACE → INTERPOLATOR → 4TH-ORDER MULTI-LEVEL ΔΣ → DAC → OUTPUT AMP → ○ Lch Out
DINL
DINR → ○ Rch Out

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At +25°C, +V_{CC} = +V_{DD} = +5V, fs = 44.1kHz, 20-bit data, SYSCLK = 256fs, unless otherwise noted.

| PARAMETER | CONDITIONS | PCM1714U | | | UNITS |
		MIN	TYP	MAX	
RESOLUTION		18		20	Bits
DIGITAL INPUT/OUTPUT					
Input Logic Level (except XTI)					
V_{IH}		2.0			VDC
V_{IL}				+0.8	VDC
Input Logic Current (except XTI)					
I_I				−200	µA
Input Logic Level (XTI)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTI)					
I_I				±50	µA
Output Logic Level (CLKO)					
V_{OH}		4.5			VDC
V_{OL}				0.2	VDC
Output Logic Current: I_O		±10			mA
Data Bit			18-Bit/20-Bit Selectable		
Sampling Frequency		1	44.1		kHz
System Clock Frequency		100k	11.2896M	20M	Hz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-match Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Zero Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE					
Effective Bandwidth			SYSCLK/564		Hz
THD+N at F/S (0dB)	f_{IN} = 991Hz		−96		dB
Dynamic Range	EIAJ A-weighted		102		dB
S/N Ratio	EIAJ A-weighted		104		dB
Channel Separation	f_{IN} = 991Hz		94		dB
ANALOG OUTPUT					
Voltage Range	F/S (0dB) OUT		2.8		Vp-p
Load Impedance		5k			Ω
Center Voltage			±1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: +V_{CC}		+4.5	+5.0	+5.5	VDC
−V_{DD}		+4.5	+5.0	+5.5	VDC
Supply Current: +I_{CC} −I_{DD}	+V_{CC} = +V_{DD} = +5.0V		25		mA
Power Dissipation	+V_{CC} = +V_{DD} = +5.0V		125		mW
TEMPERATURE RANGE					
Operation		−25		+85	°C
Storage		−55		+100	°C

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CONNECTION DIAGRAM

PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	DINL	Data Input, Lch
2	DINR	Data Input, Rch
3	BCK	Bit Clock Input
4	WDCK	Word Clock Input
5	V_{DD}	Digital Power Supply (+5V)
6	DGND	Digital Ground
7	XTI	Oscillator Input (External Clock Input)
8	XTO	Oscillator Output
9	CLKO	Buffered Output of Oscillator
10	WD SEL	Word Select Input (18-Bit/20-Bit)
11	$V_{CC}2R$	Analog (DAC) Power Supply (+5V), Rch
12	GND2R	Analog (DAC) Ground, Rch
13	D/C R	DeCoupling, Rch
14	$V_{OUT}R$	Rch Analog Output
15	GND1	Analog Ground
16	$V_{CC}1$	Analog Power Supply (+5V)
17	$V_{OUT}L$	Lch Analog Output
18	D/C L	De Coupling, Lch
19	GND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) Power Supply (+5V), Lch

NOTES: (1) XTO (Pin 8) must be open when the external clock enter to XTI (Pin 7). (2) All input pins are with pull up resistor.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1714U	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PCM1714U

8.2

DIGITAL AUDIO PRODUCTS—D/A
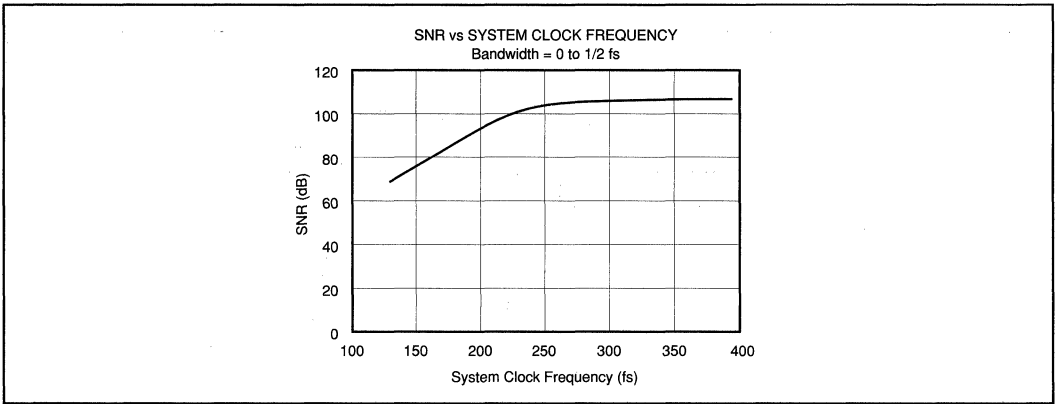
FIGURE 1. System Clock Frequency.

TIMING DIAGRAM
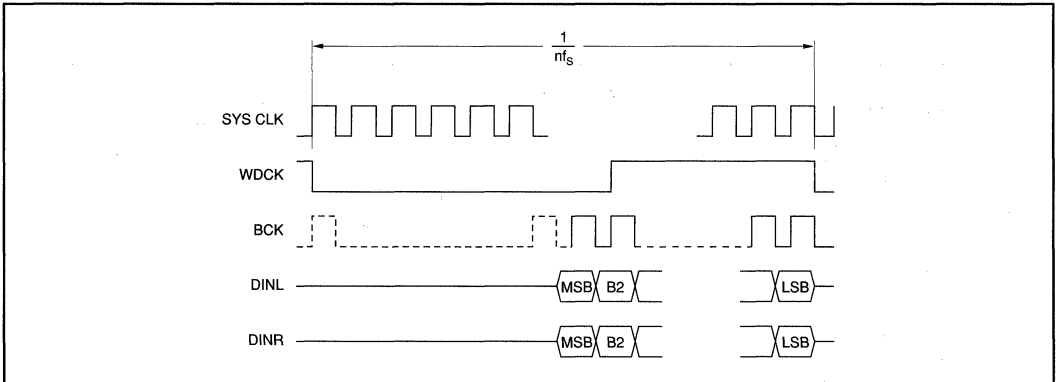
INPUT TIMING CONDITIONS

fs: 32kHz – 48kHz

n: Integer 1 – 8 (capable from 1fs to 8fs input)

SYSCLK: 8 m • nfs (fmax 20MHz)

m: Integer

BCK: More than number of input data bit (fmax 10MHz)

DINL (R): 18-Bit or 20-Bit MSB first, right justified

Example 1: fs = 44.1kHz input
SYSCLK = 8m • fs
if m = 48, then SYSCLK is calculated as SYCSLK = 8 x 48 x fs = 384fs
= 16.934MHz
if m = 32, then SYSCLK is calculated as SYCSLK = 8 x 32 x fs = 256fs
= 11.2896MHz

In above conditions, PCM1714 can be operated with both 384fs or 256fs, or any other system clock which will keep above timing conditions.

Example 2: 8 time over sampling (8fs) input
SYSCLK = 8m • 8fs
if m = 6, then SYSCLK is calculated as SYCSLK = 8 x 6 x 8fs = 384fs
= 16.9344MHz
if m = 8, then SYSCLK is calculated as SYCSLK = 8 x 8 x 8fs = 512fs
= 22.579MHz

In above conditions, PCM1714 can be operated with both 384fs but not 512fs since the system clock frequency at 512fs will exceed the max conditions of PCM1714 system clock (20MHz).

NOTE: SYSCLK > 256fs is recommended to obtain optimized SNR performance. See Figure 1 for the relation of SYSCLK vs SNR.

BURR - BROWN®

PCM1715U

Dual Voltage Output CMOS Delta-Sigma
DIGITAL-TO-ANALOG CONVERTER
With On-Chip Digital Filter

FEATURES

● **DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER**

● **HIGH PERFORMANCE:**
  THD+N: 0.0025% (–92dB) typ
  Dynamic Range: 98dB typ
  S/N RATIO: 110dB typ

● **ANALOG VOLTAGE OUTPUT:**
  V_O = 3.2Vp-p

● **ON-CHIP ANALOG LOW PASS FILTER**

● **JITTER TOUGH AND LOW RADIO FREQUENCY INTERFERENCE ENERGY ARCHITECTURE**

● **SYSTEM CLOCK 256fs or 384fs**

● **ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH:**
  Lch/Rch Individual Attenuator Control
  Digital De-Emphasis (44.1kHz)
  Analog Output Mode Select

● **SINGLE +5V POWER SUPPLY OPERATION**

● **SMALL 28-PIN SOIC PACKAGE**

DESCRIPTION

The PCM1715 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1715 is a unique multi-level 4th-order delta-sigma architecture that eliminates influence from input clock jitter and RF interferance resulting in truly superior performance.

The PCM1715 has individual channel attenuator and analog output mode select function which is suitable for CD-ROM application.

The on-chip digital filter of the PCM1715 has –62dB stop band attenuation and ±0.008dB ripple in the pass band.

The PCM1715 can be used in a wide variety of consumer audio applications. Its low cost, small size, and single +5V operation make it ideal for portable, automotive, CD players, CD-I, CD-ROM, VIDEO-CD, tuners, music instruments, and other digital audio applications.

PCM1715U

8.2

DIGITAL AUDIO PRODUCTS—D/A

BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1715U MIN	PCM1715U TYP	PCM1715U MAX	UNITS
RESOLUTION			16		Bits
DIGITAL INPUT					
Logic Family					
Input Logic Level (except XTi)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (except XTi)				–200	μA
Input Logic Level (XTi)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTi)				±50	μA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current (CLKO)		±10			mA
Data Format		MSB First, Two's Complement			
Sampling Frequency			44.1		kHz
System Clock Frequency	384fs		16.934		MHz
System Clock Frequency	256fs		11.2894		MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20.0		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE					
THD+N at F/S (0dB)[1]	f_{IN} = 991Hz		–92	–88	dB
THD+N at –60dB[1]	f_{IN} = 991Hz		–36	–32	dB
Dynamic Range	EIAJ A-weighted		98		dB
S/N Ratio	EIAJ A-weighted	104	110		dB
Channel Separation	f_{IN} = 991Hz	90	94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple				±0.008	dB
Stop Band Attenuation		–62			dB
Pass Band			0.4535		fs
Stop Band			0.5465		fs
De-emphasis Error	(fs = 44.1kHz)			+0.03	dB
ANALOG OUTPUT					
Voltage Range	fs (0dB) OUT		3.2		Vp-p
Load Impedance		5			kΩ
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current $+I_{CC}+I_{DD}$	$+V_{CC}$ = $+V_{DD}$ = +5.0V		45	70	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5.0V		225	350	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) 30kHz LPF, 400Hz HPF, Average Mode.

PIN CONFIGURATION

PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	LRCIN	Sample Rate Clock Input (fs)
2	DIN	Data Input
3	BCKIN	Bit Clock Input
4	CLKO	Buffered Output of Oscillator
5	XTI	Oscillator Input (External Clock Input)
6	XTO	Oscillator Output
7	DGND	Digital Ground
8	V_{DD}	Digital Power Supply (+5V)
9	$V_{CC}2R$	Analog (DAC) $+V_{CC}$, Rch
10	AGND2R	Analog (DAC) Ground, Rch
11	EXT1R	Output Amp Common, Rch
12	EXT2R	Output Amp Bias, Rch
13	$V_{OUT}R$	Rch Analog Output
14	AGND	Analog Ground

PIN	NAME	FUNCTION
15	$V_{CC}1$	Analog Power Supply (+5V)
16	$V_{OUT}L$	Lch Analog Output
17	EXT2L	Output Amp Bias, Lch
18	EXT1L	Output Amp Common, Lch
19	AGND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) $+V_{CC}$, Lch
21	V_{DD}	Digital Power Supply, (+5V)
22	DGND	Digital Ground
23	CKSL	System Clock Select (H:384fs, L:256fs)
24	NC	No Connection
25	RSTB	Reset
26	MD	Mode Control
27	MC	Mode Control, BCK
28	ML	Mode Control, WDCK

NOTE: All input pins require pull up resistors.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage .... ±6.5VDC
$+V_{CC}$ to V_{DD} Voltage .... ±0.1V
Input Logic Voltage .... $-0.3V \sim V_{DD}$ +0.3V
Power Dissipation 400mW
Operating Temperature .... $-25°C$ to +85°C
Storage Temperature .... $-55°C$ to +125°C
Lead Temperature (soldering, 5s) .... +260°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1715U	28-Pin SOIC	217-4J

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PCM1715U

8.2

DIGITAL AUDIO PRODUCTS—D/A

CONNECTION DIAGRAM

TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

OVERALL FREQUENCY CHARACTERISTIC
(De-Emphasis: OFF)

PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
(De-Emphasis: OFF)

DE-EMPHASIS CHARACTERISTIC

SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(20Hz~24kHz, Expanded Scale)

SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(10Hz~10MHz)
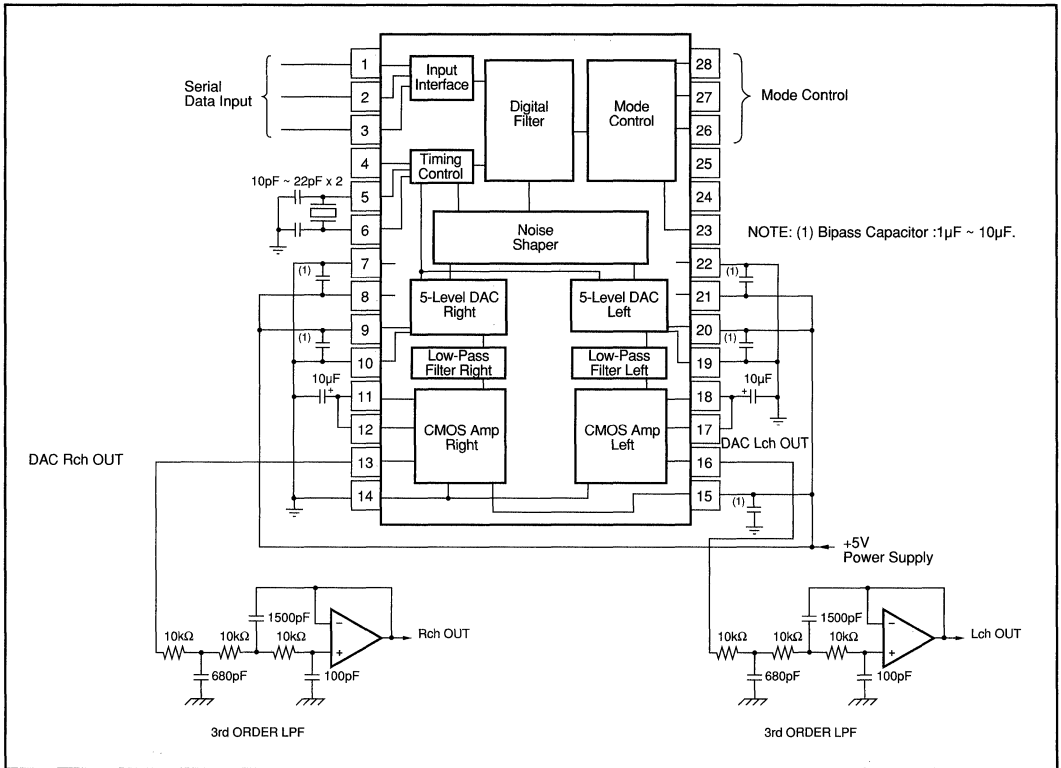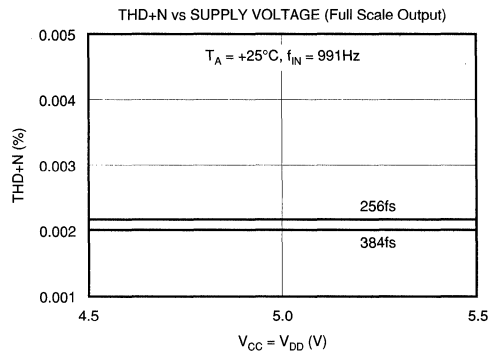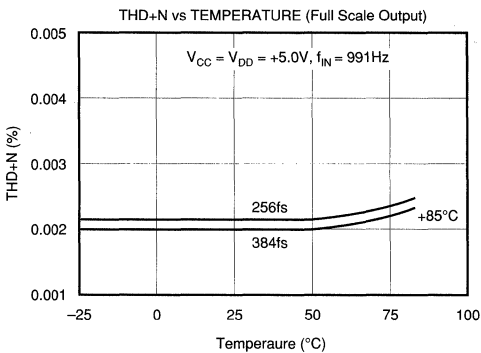
OUTPUT WAVE FORM FULL SCALE SIGNAL
(Without External Filter)

NOTES: (1) Measured at V_{OUT} Pin (Pin 13 or 16). (2) The PCM1715 has internal analog low pass filter to reduce high frequency noise-shaped spectrum. Application of the PCM1715 requires external post analog low pass filter which has 2nd-Order or 3rd-Order attenuation performance to get low noise analog output.

PCM1715U

8.2

DIGITAL AUDIO PRODUCTS—D/A

THEORY OF DELTA-SIGMA OPERATION

The delta-sigma section of the PCM1715 is based on a 5-level amplitude quantizer and a 4th-order filter. This converts the oversampled 16-bit input data to 5-level delta-sigma form. A block diagram of the 5-level modulator is shown in Figure 1.
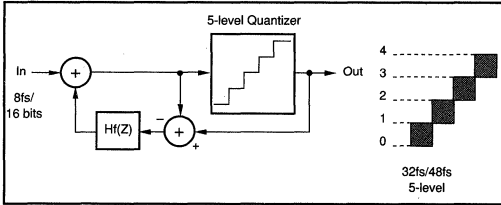
FIGURE 1. Block Diagram of 5-Level Delta-Sigma Quantizer.

This 5-level delta-sigma modulator has the advantage of stability of delta-sigma loop and jitter sensitivity over the typical 1-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8x oversampling digital filter is 48fs at a system clock speed of 384fs, 32fs at a system clock speed of 256fs.

A block diagram of the 4th-order filter section Hf(z) in the delta-sigma modulator is shown in Figure 2.

In general, high order 1-bit delta-sigma modulators have disadvantages due to loop instability. The 5 level delta-sigma modulator of the PCM1715 uses phase compensation techniques to obtain stable operation. In Figure 2, the coefficients, b1 to b4, give the basic form of the filter and –a1 and –a2 are used for phase compensation of the feedback loop.

The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figures 3 and 4. In the audio band, the quantization noise floor level of the PCM1715 is less than –130dB (384fs).

MODE OF OPERATION

Serial inputs to MD, MC, and ML (Pins 26, 27 and 28) control the following functions:

(1) Digital Attenuator [AL0 ~ AL7, AR0 ~ AR7]
Attenuation data is constructed by 8-bit/Lch, 8-bit/Rch (total 16-bit), can be controlled as 255 step attenuation by individual channel. AL0 and AR0 are LSB, and AL7 and AR7 are MSB. Attenuation Level ATT is given by:

$$ATT = 20LOG_{10} (ATT\ DATA/255)\ [dB]$$
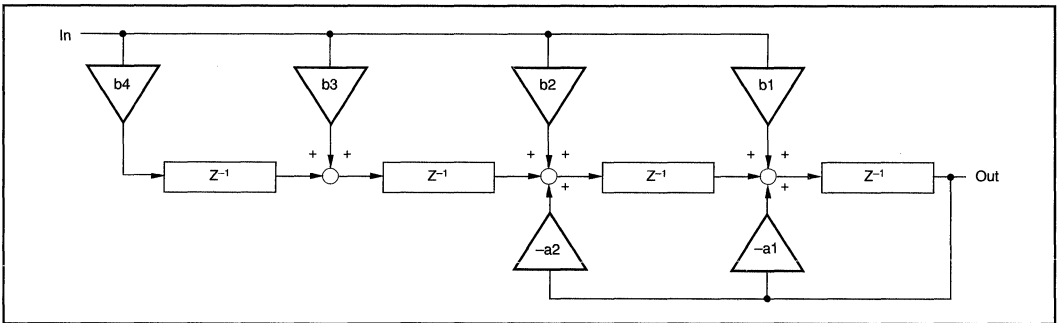
FIGURE 2. Block Diagram of the Hf(z).
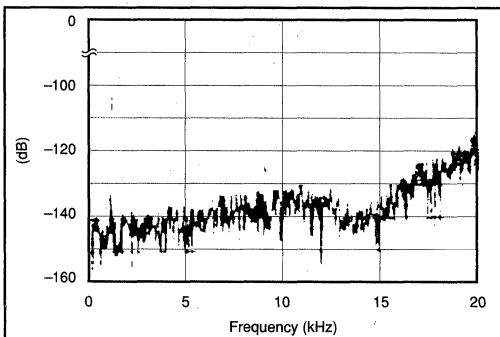
FIGURE 3. Quantization Noise Spectrum (256fs).
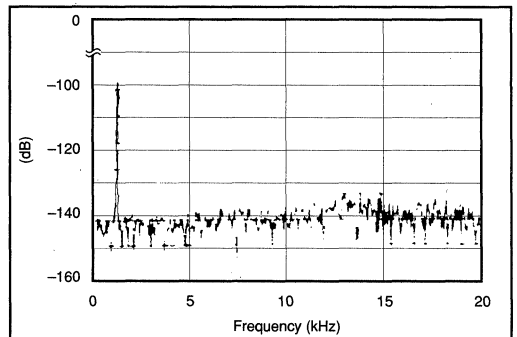
FIGURE 4. Quantization Noise Spectrum (384fs).

At ATT DATA: 0XFF, output is 0dB. At ATT DATA 0X00, output is −∞.

When "Muting" is chosen by output mode control, output goes to −∞ from the present ATT level.

Moving speed from 0dB to −∞ is 1024/f.

Initialized (RESET) ATT level is 0dB.

(2) Versatile Output Mode [PL0 ~ PL3]

By using PL0 ~ PL3 data, up to 16 different output modes (Lch/Rch/L+R/MUTE) can be selected to the output of Lch and Rch, as shown in Table I.

Initialized mode is STEREO mode.

(3) De-emphasis Control (DEM)

De-emphasis function is controlled by DEM flag (H: ON, L: OFF)

De-emphasis is enabled only at 44.1kHzfs. At other fs frequencies, de-emphasis error is not guaranteed. Initialized mode is De-emphasis OFF.

(4) Attenuator Control (ATC)

If common attenuator control of Lch and Rch is needed, use the ATC flag (ATC = "H"). Common attenuation can be controlled by Lch (AL0 ~ AL7) data. Initialized mode is individual.

(5) Infinity-Zero Detection

The PCM1715 has an infinity-zero detect function which monitors the input data and bit clock. When the input

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE I. PCM1715 Output Mode Control.

data is continuously "zero" for 8192 cycles of the bit clock, the infinity zero detect occurs and the DAC outputs are set to bipolar zero ($1/2V_{CC}$).

(6) Reset

Normally, internal initialize (reset) is done automatically at power on ($V_{DD} > 3.5V$). The RSTB-pin (Pin 25) accepts external forced reset by RSTB=L. During RSTB=L, the output of the DAC is invalid, set to $1/2V_{CC}$ after internal initialize (1024XTI clock count after RSTB=H).

MODE CONTROL FORMAT

PCM1715U

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DIGITAL AUDIO PRODUCTS—D/A
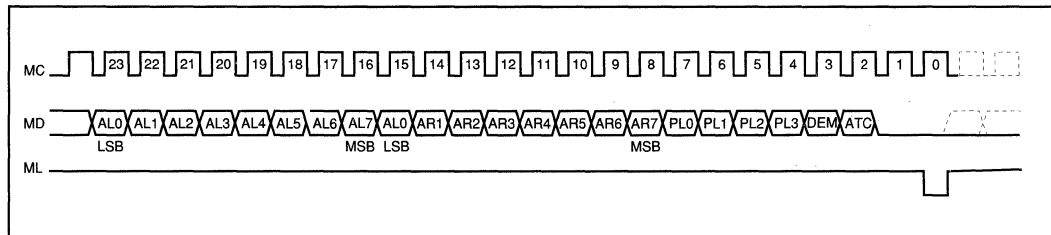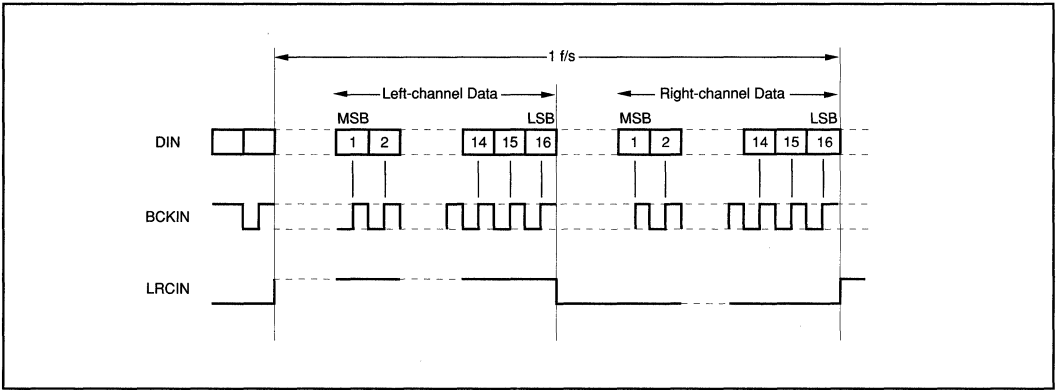
FIGURE 5. Data Input Timing, 16-Bit.
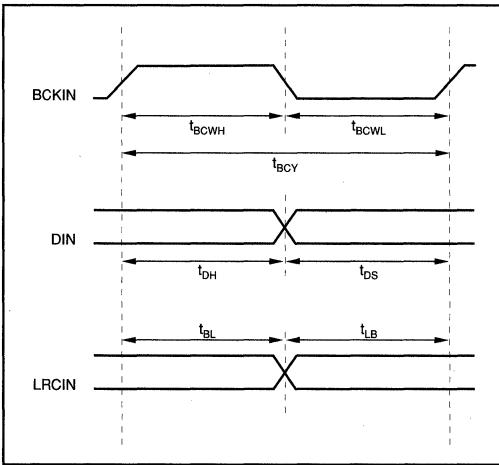
FIGURE 6. Data Input Timing.
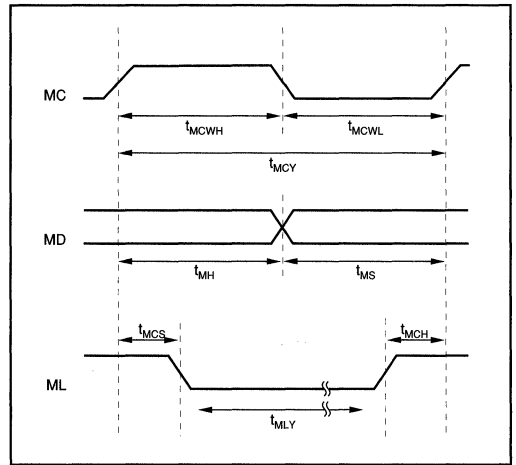
FIGURE 7. Serial Mode Control Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level)	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRCI Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE II. Data Input Timing Specifications.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

TABLE III. Serial Mode Control Timing Specifications.

NOTE: External system clock inputs to XTI should meet the following conditions:
$V_{IH} > 0.64V_{DD}$
$V_{IL} < 0.28V_{DD}$
$T_H > 10ns$
$T_L > 10ns$

FIGURE 8. Operation Instruction For System Clock.

FIGURE 9. Oscillator Circuit Connection Diagram. Optional external crystal oscillator.
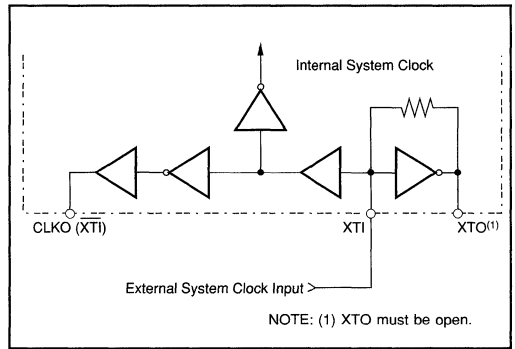
FIGURE 10. Oscillator Circuit Connection Diagram. External system clock.

EVALUATION BOARD

Burr-Brown's DEM-PCM1710 evaluation board for the PCM1710 is capable of evalution of the PCM1715 and PCM1710. Digital input signals for the evaluation board are LRCK, BCK, DATA, and system clock (256fs or 384fs). Power supply requirement is only +5V.

The DEM-PCM1710 has a pattern layout for an optional crystal oscillator. However, the crystal is not installed.

PCM1715U

8.2

DIGITAL AUDIO PRODUCTS—D/A

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BB
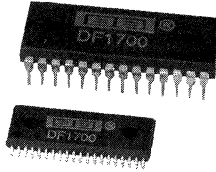
DF1700

Dual Channel, 8x Oversampling
DIGITAL FILTER

FEATURES

● **DUAL CHANNEL DIGITAL INTERPOLATION FILTERS**
● **ACCEPTS 16-BIT INPUT DATA**
● **USER-SELECTABLE FOR 16-, 18-, OR 20-BIT OUTPUT DATA**
● **SERIAL OUTPUT IS COMPATIBLE WITH PCM1700 AND PCM63 DACs**
● **PASSBAND RIPPLE < 0.00005dB**
● **STOPBAND ATTENUATION > 110dB**
● **SINGLE +5V POWER SUPPLY FOR LOW POWER DISSIPATION OF 250mW Max**
● **PLASTIC 28-PIN DIP AND 40-PIN SOIC PACKAGES**

DESCRIPTION

The DF1700 is a high performance, 8x oversampling CMOS digital filter. This filter accepts 16-bit input data and is user-selectable for 16-, 18-, or 20-bit output data. The 8x oversampling feature converts the input data frequency (fs) to an output data frequency of 8 X fs by digital interpolation. By providing 8x oversampled data to an audio DAC, lower order analog filters can be used at the DAC's output, thus reducing filter phase non-linearities. Oversampling with the DF1700 simultaneously improves the fidelity of the analog reconstruction and reduces analog filter complexity at the output of the DAC.

The DF1700 is available in a plastic 28-pin DIP and a 40-pin SOIC package, and is designed for compatibility with the Burr-Brown PCM1700 and PCM63 digital-to-analog converters.

PDS-1093

BURR - BROWN®

BB

PIN CONFIGURATION

Top View   DIP

1	DIN	LRCI	28
2	BCKI	FSCO	27
3	$\overline{CKSL}$	BCKO	26
4	$\overline{CKDV}$	WCKO	25
5	NC	DOL	24
6	XTI	DOR	23
7	XTO	V_{DD}	22
8	V_{SS1}	V_{SS2}	21
9	CKO	DG	20
10	$\overline{SYN}$	NC	19
11	NC	NC	18
12	NC	$\overline{OW18}$	17
13	NC	$\overline{OW20}$	16
14	$\overline{RST}$	$\overline{COB}$	15

Top View   SOIC

1	NC ●	V_{SS1}	40
2	NC	XTO	39
3	NC	XTI	38
4	CKO	$\overline{CKDV}$	37
5	NC	NC	36
6	NC	NC	35
7	$\overline{SYN}$	$\overline{CKSL}$	34
8	NC	BCKI	33
9	NC	DIN	32
10	NC	NC	31
11	$\overline{RST}$	LRCI	30
12	$\overline{COB}$	FSCO	29
13	$\overline{OW20}$	BCKO	28
14	$\overline{OW18}$	WCKO	27
15	NC	NC	26
16	NC	DOL	25
17	NC	NC	24
18	DG	DOR	23
19	NC	NC	22
20	V_{SS2}	V_{DD}	21
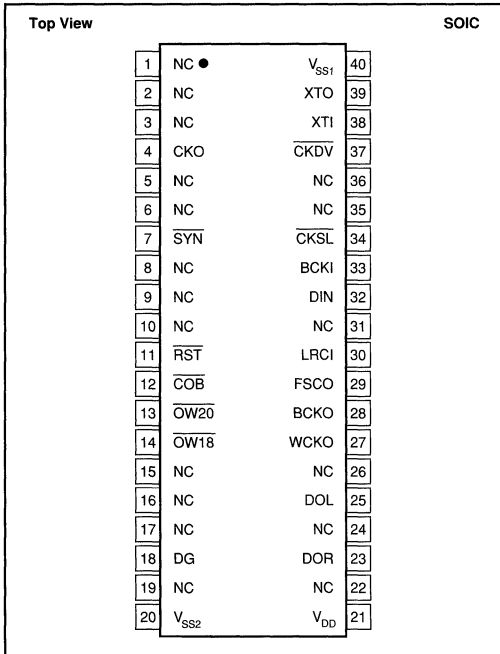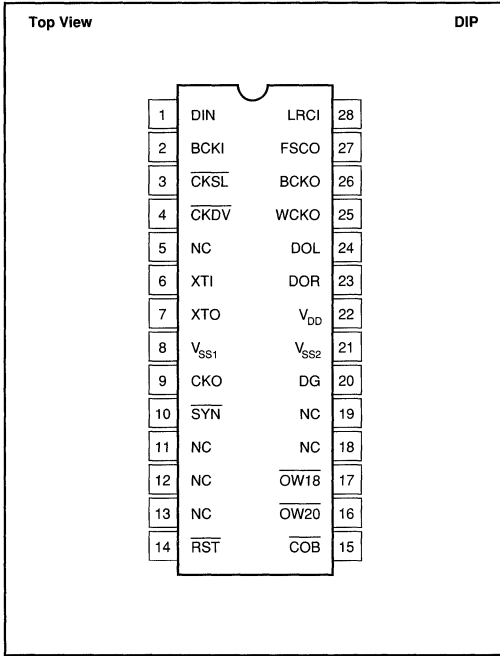
PIN DESCRIPTION

PIN NUMBER		NAME	I/O[1]	DESCRIPTION
SOIC	DIP			
1	–	NC	–	
2	–	NC	–	
3	–	NC	–	
4	9	CKO	O	Clock output (same frequency as XTI input clock).
5	–	NC	–	
6	–	NC	–	
7	10	$\overline{SYN}$	I	H: Free-running mode; L: Forced synchronizing mode.
8	11	NC	–	
9	12	NC	–	
10	13	NC	–	
11	14	$\overline{RST}$	I	H: Normal operation; L: System reset.
12	15	$\overline{COB}$	I	Select output data format— H: Two's complement; L: Complemented offset binary (COB).
13	16	$\overline{OW20}$	I	Select number of output data bits.[2]
14	17	$\overline{OW18}$	I	Select number of output data bits.[2]
15	–	NC	–	
16	18	NC	–	
17	19	NC	–	
18	20	DG	O	Deglitch control clock.
19	–	NC	–	
20	21	V_{SS2}	–	Ground 2.
21	22	V_{DD}	–	Supply voltage (+5V).
22	–	NC	–	
23	23	DOR	O	Rch serial data output (8fs rate).
24	–	NC	–	
25	24	DOL	O	Lch serial data output (8fs rate).
26	–	NC	–	
27	25	WCKO	O	Output timing control (word clock).
28	26	BCKO	O	Output timing control for serial data (bit clock).
29	27	FSCO	O	Internal timing clock (fs rate)
30	28	LRCI	I	Multiplex clock for Lch/Rch input data (fs rate)—H: Lch; L: Rch.
31	–	NC	–	
32	1	DIN	I	Serial data input.
33	2	BCKI	I	Timing clock for serial input data.
34	3	$\overline{CKSL}$	I	Select system clock.[2]
35	–	NC	–	
36	5	NC	–	
37	4	$\overline{CKDV}$	I	Select system clock.[2]
38	6	XTI	I	Input for oscillator or external clock (system clock).
39	7	XTO	O	Output for oscillator; not connected when using external clock.
40	8	V_{SS1}	–	Ground 1.

NOTES: (1) I = Input terminal; O = Output terminal. (2) Refer to the Functional Description section for details.

⚡ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

DF1700

8.3

DIGITAL AUDIO PRODUCTS—DF

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DC SPECIFICATIONS

ELECTRICAL

DIGITAL CHARACTERISTICS: V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to +70°C unless otherwise specified.

PARAMETER	PIN	SYMBOL	CONDITION	DF1700P, U MIN	DF1700P, U TYP	DF1700P, U MAX	UNITS
INPUT							
Logic Family					CMOS		
Logic Voltages	XTI	V_{IL1}				$0.3V_{DD}$	V
	XTI	V_{IH1}		$0.7V_{DD}$			V
	(1)	V_{IL2}				0.5	V
	(1)	V_{IH2}		2.4			V
Input Leakage Current	XTI	I_{LH}	$V_{IN} = V_{DD}$		10	20	µA
	XTI	I_{LL}	$V_{IN} = 0V$		10	20	µA
	(1)	I_{LH}	$V_{IN} = V_{DD}$			1	µA
Input Current	(1)	I_{IL}	$V_{IN} = 0V$		10	20	µA
OUTPUT							
Logic Family					CMOS		
Logic Voltages	(2)	V_{OL}	$I_{OL} = 1.6mA$			0.4	V
	(2)	V_{OH}	$I_{OH} = -0.4mA$	2.5			V
POWER SUPPLY REQUIREMENTS							
Supply Voltages		V_{DD}		4.75	5	5.25	V
Supply Current		I_{DD}	$V_{DD} = 5V, F_{SYS}^{(3)}$			45	mA
Power Dissipation		P_D	Nominal V_{DD}			250	mW
TEMPERATURE RANGE (Ambient, T_A)							
Specification				–20		70	°C
Operating				–20		70	°C

NOTES: (1) Refers to pins LRCI, DIN, BCKI, $\overline{CKSL}$, $\overline{CKDV}$, $\overline{SYN}$, $\overline{RST}$, $\overline{COB}$, $\overline{OW20}$, and $\overline{OW18}$. (2) Refers to pins CKO, DG, DOL, DOR, WCKO, BCKO, and FSCO. (3) F_{SYS} is the frequency of the internal system clock. $F_{SYS} = F_{XTI}$ with $\overline{CKDV}$ = H and $F_{SYS} = F_{XTI}/2$ with $\overline{CKDV}$ = L.

AC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to 70°C unless otherwise specified.

PARAMETER	SYMB	CKSL	CKDV	x fs(1)	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR								
Oscillating Frequency	f_{MAX}	H	H	192	1		13	MHz
	f_{MAX}	H	L	384	2		26	MHz
	f_{MAX}	L	H	256	1		13	MHz
	f_{MAX}	L	L	512	2		26	MHz
EXTERNAL CLOCK								
Clock Pulse Width	t_{CW}	H	H	192	35		500	ns
	t_{CW}	H	L	384	15		250	ns
	t_{CW}	L	H	256	35		500	ns
	t_{CW}	L	L	512	15		250	ns
Clock Period	t_{CY}	H	H	192	76		1000	ns
	t_{CY}	H	L	384	38		500	ns
	t_{CY}	L	H	256	76		1000	ns
	t_{CY}	L	L	512	38		500	ns

Timing Waveform

XTI — Min $0.7V_{DD}$ — $0.5V_{DD}$ — Max $0.3V_{DD}$

$\leftarrow t_{CW} \rightarrow \leftarrow t_{CW} \rightarrow$
$\leftarrow t_{CY} \rightarrow$

NOTES: (1) fs = sampling frequency.

AC SPECIFICATIONS (CONT)

ELECTRICAL

V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = −20°C to 70°C unless otherwise specified.

PARAMETER	SYMBOL	DF1700P, U MIN	TYP	MAX	UNITS
INPUT TIMING (BCKI, DIN, LRCI, XTI)					
BCKI, Pulse Width	t_{BCW}	100			ns
BCKI, Cycle Time	t_{BCY}	200			ns
DIN, Setup Time	t_{DS}	75			ns
DIN, Hold Time	t_{DH}	75			ns
Rising Edge of Last BCKI To Edge of LRCI	t_{BL}	75			ns
Edge of LRCI To Rising Edge of First BCKI	t_{LB}	75			ns
Falling Edge of XTI To Rising Edge of LRCI	t_{XL}	20			ns
Rising Edge of LRCI To Falling Edge of XTI	t_{LX}	0			ns

Timing Waveform

PARAMETER	SYMBOL	CONDITION	DF1700P, U MIN	TYP	MAX	UNITS
OUTPUT TIMING						
BCKO Delay Time	txbH	$\overline{CKDV}$ = L	35		120	ns
from XTI	txbL	$\overline{CKDV}$ = L	35		120	ns
	txbH	$\overline{CKDV}$ = H	35		120	ns
	txbL	$\overline{CKDV}$ = H	35		120	ns
Output Delay	tbdL	C_L = 15pF	−10	0	10	ns
	tbdH	C_L = 15pF	−10	0	10	ns

Timing Waveform

ORDERING INFORMATION

DF1700 (_)

Basic Model Number ——————————————
Package Code ——————————————
P: 28-pin Plastic DIP
U: 40-pin Plastic SOIC

ABSOLUTE MAXIMUM RATINGS

+V_{DD} .... −0.3V to 7.0V
Input Voltage .... −0.3 to V_{DD} +0.3V
Soldering Temperature .... 255°C
Soldering Time 10s
Storage Temperature .... −40°C to +125°C
Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DF1700P	28-Pin Plastic DIP	215
DF1700U	40-Pin SOIC	252

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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DIGITAL AUDIO PRODUCTS—DF

THEORETICAL FILTER CHARACTERISTICS

PARAMETER	CHARACTERISTICS
Passband	0 ~ 0.4535fs
Stopband	0.5465fs ~ 7.4535fs
Passband Ripple	Within ±0.00005dB
Stopband Attenuation	More than 110dB
Group Delay Time	Constant

PASSBAND RIPPLE

STOPBAND ATTENUATION

POLES IN PASSBAND AND STOPBAND
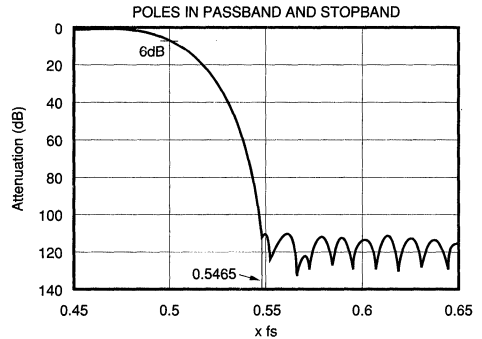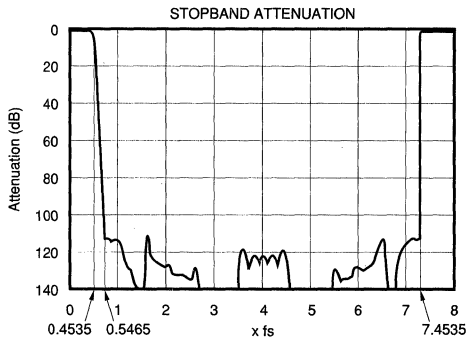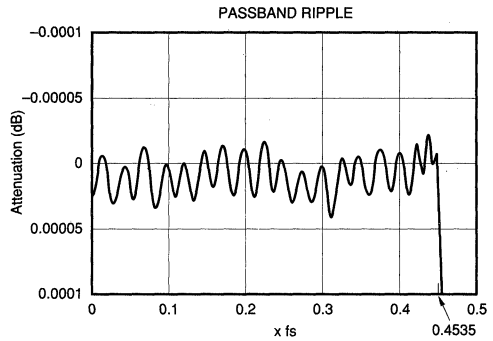
THEORY OF OPERATION

The DF1700 has dual filters. Each filter consists of three cascaded, 2x oversampling finite impulse response (FIR) filters as shown in Figure 1. The output of the first, 153-tap filter is again 2x oversampled by the second, 29-tap filter. This 4x oversampled data is again 2x oversampled by a third, 17-tap filter. This oversampling technique further separates the desired analog signal and the sampling frequency. This is desirable because a low-pass filter is required at the output of a DAC to remove all unwanted frequency components caused by the sampling frequency. With the analog signal frequency further separated from the sampling frequency, a lower order analog filter with much better phase characteristics can be used at the output of the DAC without worrying about fold-over noise.

Input ○ fs → | DF1 153 taps | 2fs → | DF2 29 taps | 4fs → | DF3 17 taps | 8fs → ○ Output

DF1, DF2, and DF3 are 2x oversampling FIR digital filters.
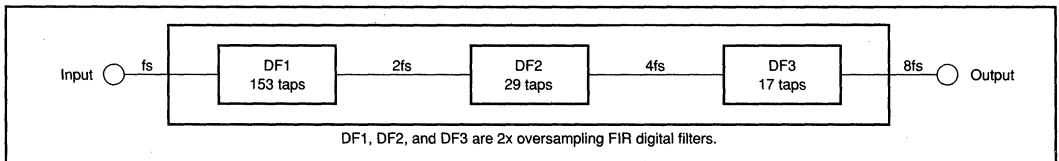
FIGURE 1. Block Diagram of Channel Filter.

FUNCTIONAL DESCRIPTION

SYSTEM CLOCK

The internal system clock of the DF1700 is generated by either a crystal oscillator connected across pins XTI and XTO driving the internal clock generator, or an external clock applied at pin XTI. Four different XTI clock frequencies can be obtained with the control of pins CKDV and CKSL. This will provide the correct clock period of the internal system clock as indicated in Table I. For XTI clock frequencies of 384fs and 512fs, the clock is divided by two for internal use. The system clock signal of the same frequency as pin XTI is available at pin CKO.

DATA

Serial Data Input

The 16-bit input data format is two's complement and MSB first. The serial data input timing is the rising edge of BCKI (Figure 2). Consequently the input serial data must be changed at the falling edge of BCKI. The input data is latched to the internal register at the edge of LRCI.

Serial Data Output

The serial data output mode is selected by pins $\overline{OW18}$ and $\overline{OW20}$ as shown in Table II.

The output data format is MSB first and either two's complement or complementary offset binary (COB). The format of output data is selected by the $\overline{COB}$ pin:

$\overline{COB}$ = H   Two's complement
$\overline{COB}$ = L   Complemented Offset Binary (COB)

The output data from the DF1700 can be fed directly to the data inputs of either the PCM1700 or PCM63 with the BCKO clock output serving as the input clock to these DACs. The data bits will be clocked into the DAC on the rising edges of BCKO (Figure 3).

CONDITION		XTI	CLOCK PERIOD OF
$\overline{CKDV}$	$\overline{CKSL}$	CLOCK (F_{XI})	INTERNAL SYSTEM CLOCK
H	H	192fs	$1/F_{XI}$
H	L	256fs	$1/F_{XI}$
L	H	384fs	$2/F_{XI}$
L	L	512fs	$2/F_{XI}$

NOTE: fs = sampling frequency.

TABLE I. System Clock Frequency Selection.

$\overline{OW18}$	$\overline{OW20}$	NO. OF OUTPUT DATA BITS
H	H	16
L	H	18
H	L	20

TABLE II. Programming the Number of Output Data Bits.

CLOCK SYNCHRONIZATION

The internal clock for the arithmetic circuitry and output interface is derived by the system clock from the XTI pin, and is independent of the input circuitry timing from the BCKI and LRCI input clocks. There are two synchronization modes: the Free-Running Mode and the Forced Synchronization Mode.
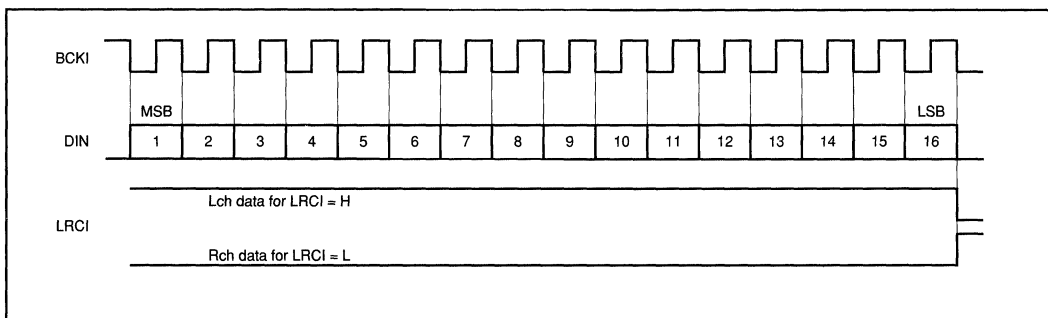
FIGURE 2. Input Timing Waveforms for Clocking Data into the DF1700.
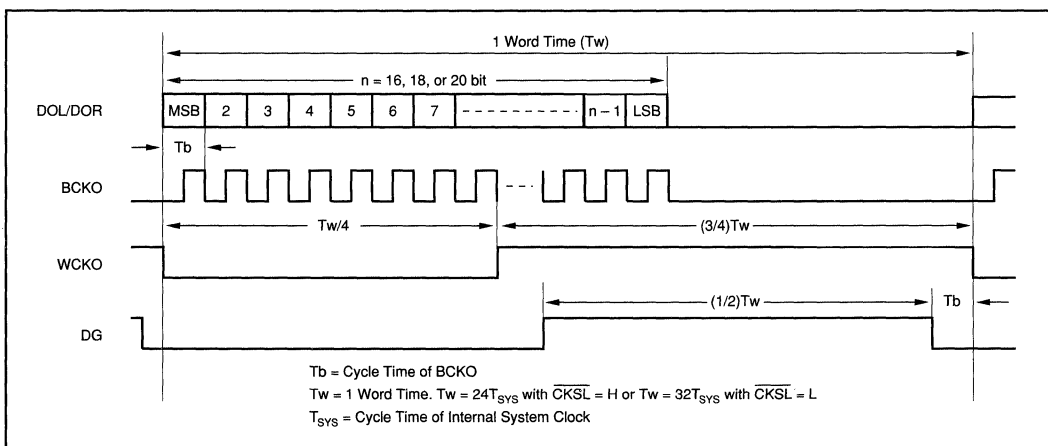
FIGURE 3. Output Data Timing Waveforms.

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DIGITAL AUDIO PRODUCTS—DF

Free-Running Mode ($\overline{SYN}$ = H)

No adjustment of the internal clock takes place for phase differences between the internal clock and the LRCI clock of up to ±3/8 of the input data sample period (1/fs). Hence, internal timing is not affected even if jitter is present on the LRCI clock input, and no jitter or timing glitches appear on the data output. If the clock phase differences exceed the ±3/8fs limit, or if the RESET function is executed, the internal clock is synchronized to the rising edge of LRCI.

Forced Synchronization Mode ($\overline{SYN}$ = L)

In this mode the internal clock is resynchronized at each rising edge of LRCI. Note that device misoperation may occur if jitter in the LRCI input shortens the LRCI period below the required system clock period. Furthermore, if the LRCI period is too long, internal arithmetic operations will function correctly, but output timing is adversely affected.

The internal timing clock derived from the system clock is available at the FSCO pin.

SYSTEM RESET

The RESET function is useful for synchronizing the internal arithmetic circuitry and output section clock with the LRCI external input clock when operating in the free-running mode
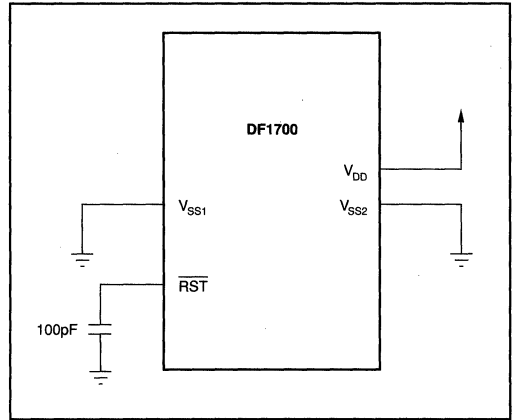
FIGURE 4. System Reset Circuit.

($\overline{SYN}$ = H). It is not necessary to reset in the forced synchronization mode. Reset is also not required if the output timing needs not be synchronized with LRCI. Figure 4 shows the connection to reset the DF1700 on power-up.

TIMING DIAGRAMS
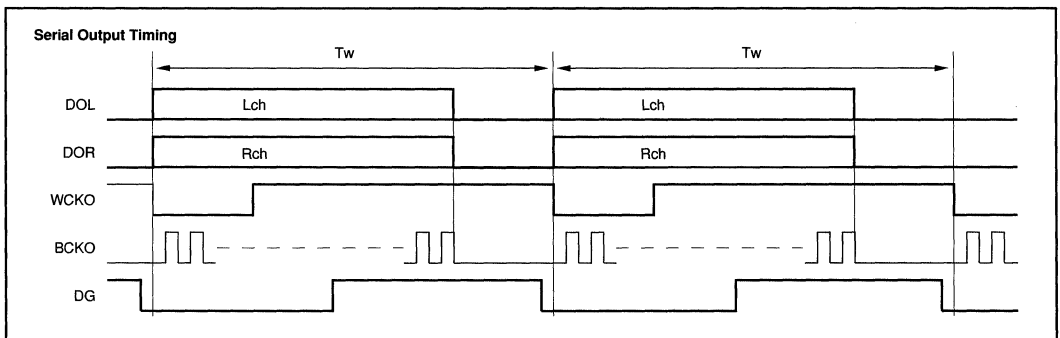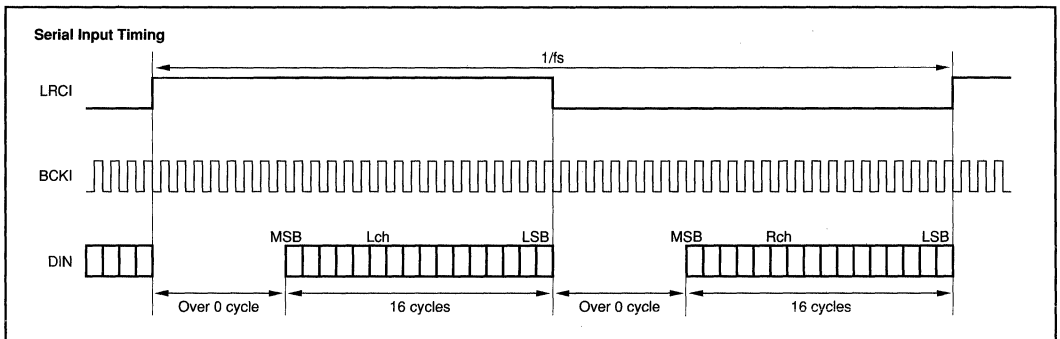
APPLICATIONS

The most common application for the DF1700 is in high performance digital audio playback such as compact disc players. Digital information from a compact disc is often formatted using a digital interface format receiver chip (DIFRC). The DF1700 can be interfaced directly to the output of many popular DIFRCs as shown in Figure 5.

The fs data stream which has been formatted by the DIFRC is 8x oversampled by the DF1700 and separated into left and right channel data for input to the PCM1700 DAC (Figure 6). The analog stereo outputs from the PCM1700 each pass

through a three pole Generalized Immittance Converter (GIC) low-pass filter which has extremely low distortion and negligible phase shift. An evaluation board, the DEM1143, is available from Burr-Brown for the PCM1700/DF1700. This board has the features mentioned above as well as an AES/EBU interface and breadboard area for user experimentation. Figure 7 shows a similar circuit diagram with the DF1700 providing 8x oversampled data to a pair of PCM63 DACs.
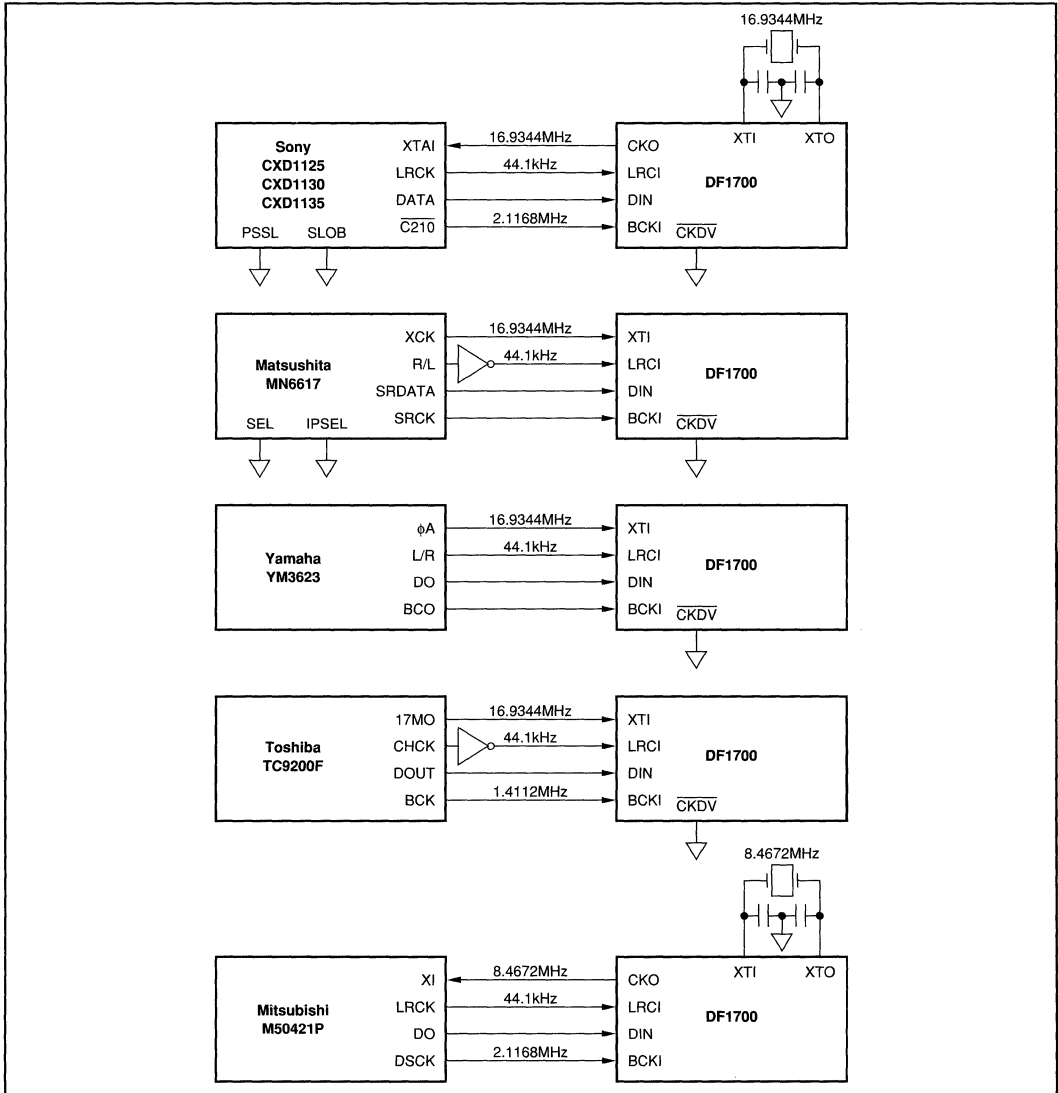
FIGURE 5. Interfacing the DF1700 to Various Digital Interface Format Receiver Chips (DIFRCs).
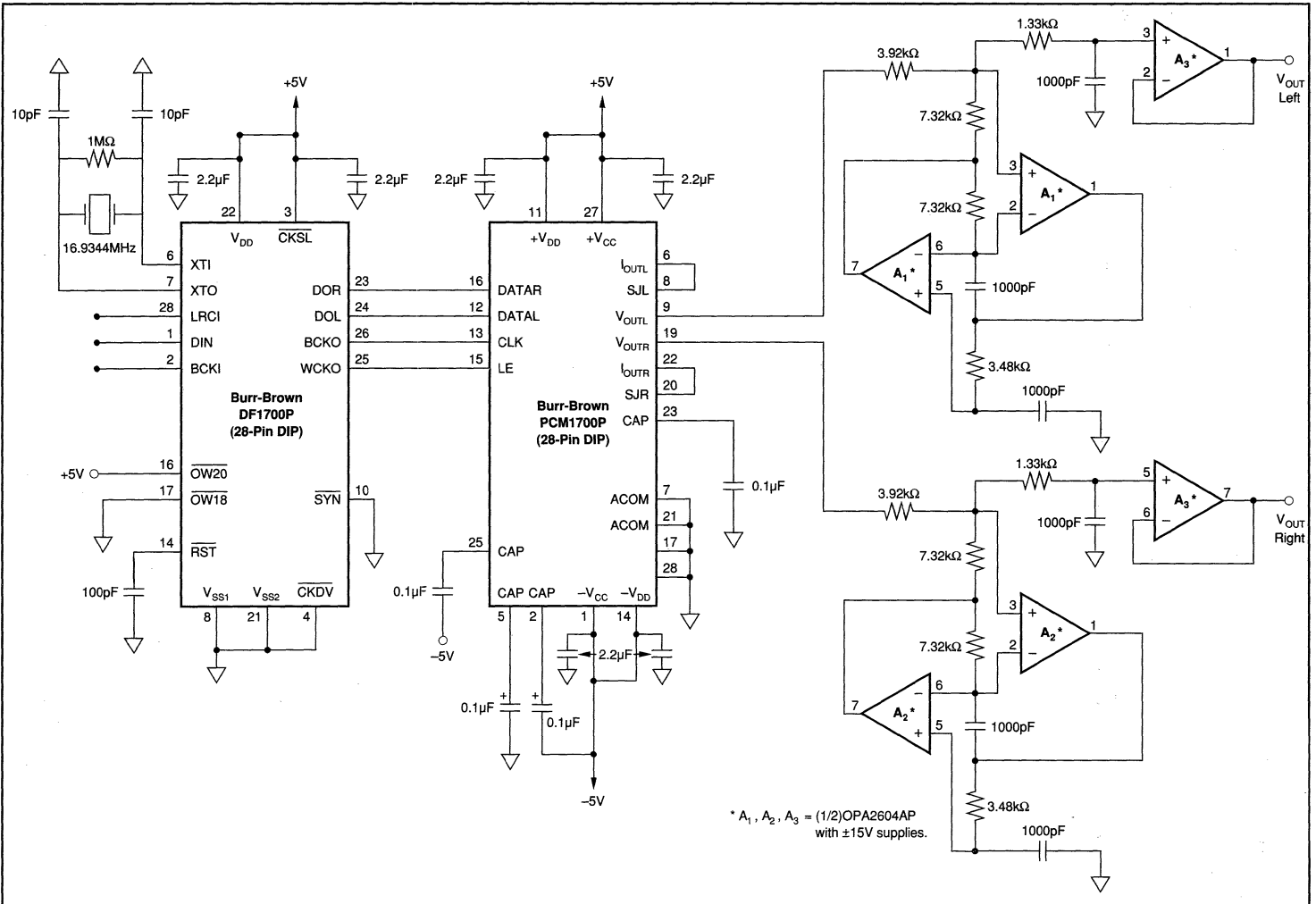
DF1700

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DIGITAL AUDIO PRODUCTS—DF

For Immediate Assistance, Contact Your Local Salesperson

FIGURE 6. Circuit Diagram for the DF1700 Providing Oversampled Data to the PCM1700P Dual-Channel DAC.
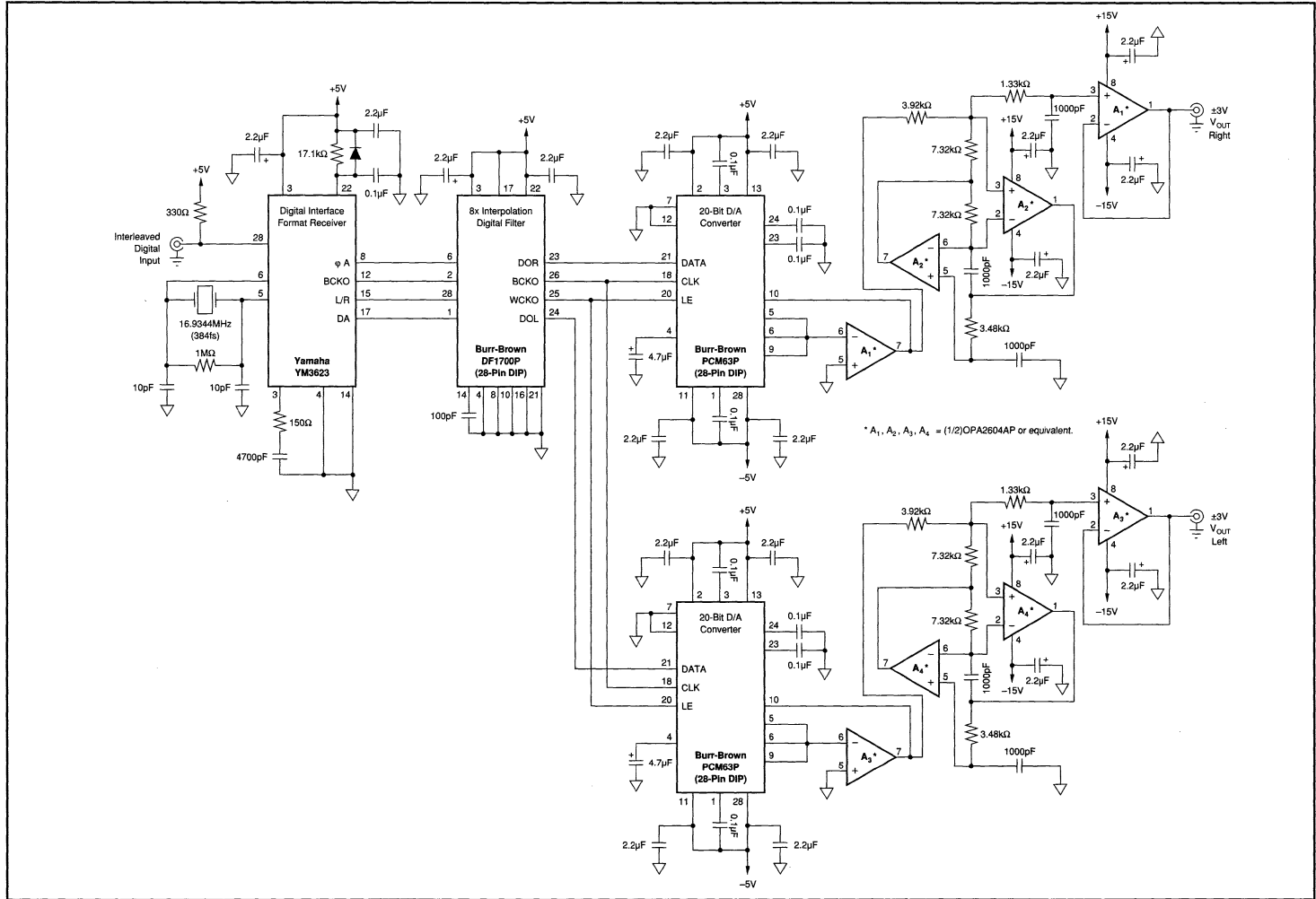
FIGURE 7. Circuit Diagram for the DF1700 Providing Oversampled Data to a Pair of PCM63P DACs.

DIGITAL AUDIO PRODUCTS—DF **8.3** **DF1700**

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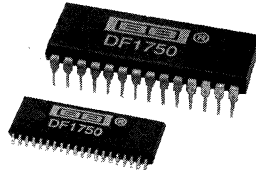
DF1750

Dual Channel
DIGITAL DECIMATION FILTER

FEATURES

● **USER SELECTABLE FOR 1/4 OR 1/2 DECIMATING RATIOS**

● **USER SELECTABLE FOR 16- OR 18-BIT INPUT DATA**

● **SERIAL DATA INPUT IS COMPATIBLE WITH THE BURR-BROWN PCM1750 ADC**

● **FILTERS OUT-OF-BAND NOISE WITH STOPBAND ATTENUATION > 95dB**

● **PASSBAND RIPPLE < 0.0005dB**

● **SINGLE +5V SUPPLY OPERATION WITH LOW POWER DISSIPATION OF ONLY 250mW**

DESCRIPTION

The DF1750 is a high performance 1/4 or 1/2 decimating digital filter that is designed for digital audio applications. This device decimates and filters 2x or 4x (2fs or 4fs) oversampled data from the output of an ADC to a data frequency of fs. The technique of oversampling and decimating allows the input to an oversampling ADC to be processed by a much lower order, linear phase, analog low-pass filter. This simultaneously improves system performance while reducing circuit complexity and cost.

The DF1750 provides output data word rates (fs) up to 50.5kHz and it is compatible with the Burr-Brown PCM1750, dual 18-bit analog-to-digital converter.

Block diagram with the following labeled blocks and signals:

Top inputs: SCSL1, SCSL2, 2DS, IBCK, DINL, DINR

Left side inputs: XTI, XTO, CKEN, CKO, CC, BBC, IBO, TEST

Blocks: System Clock, Input Interface Circuit, Timing Control, FIR Filter Circuit, Output Interface Circuit

Right side: IMOD, OW20, FSEN

Bottom outputs: LRCK, WDCK, BCK, DOUT, MUTE, LRPOL, OBPOL

PDS-1092

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PIN CONFIGURATION

Top View — SOIC — Top View — DIP

PIN DESCRIPTION

PIN NO. DIP	SOIC	NAME	I/O*	DESCRIPTION	PIN NO. DIP	SOIC	NAME	I/O*	DESCRIPTION
1	1	CKO	o	Clock output (the same as XTI frequency), CKO = L when $\overline{\text{CKEN}}$ = H	15	21	$\overline{\text{OW20}}$	ip	Output data bit select (16bit: $\overline{\text{OW20}}$ = H, 20 bit: $\overline{\text{OW20}}$ = L)
–	2	(NC)			–	22	(NC)		
2	3	$\overline{\text{SCSL1}}$	ip	XTI Frequency select	16	23	$\overline{\text{FSEN}}$	ip	I/O pin select ($\overline{\text{FSEN}}$ = H: BCK, WDCK, LRCK pin=Input) ($\overline{\text{FSEN}}$ = L: BCK, WDCK, LRCK pin=Output)
3	4	$\overline{\text{SCSL2}}$	ip	(Refer to XTI pin description)	17	24	LRCK	ip	fs clock
4	5	$\overline{\text{TEST}}$	ip	Test, (Test = L; test mode)	18	25	$\overline{\text{LRPOL}}$	ip	LRCK polarity select ($\overline{\text{LRPOL}}$ = H: Lch/Rch=Low/High) ($\overline{\text{LRPOL}}$ = L: Lch/Rch=High/Low)
–	6	(NC)			–	26	(NC)		
5	7	$\overline{\text{2DS}}$	ip	1/4 or 1/2 decimating select $\overline{\text{2DS}}$ = H: 1/4 decimating,					
			ip	$\overline{\text{2DS}}$ = L: 1/2 decimating	19	27	$\overline{\text{OBPOL}}$	ip	BCK polarity select
6	8	$\overline{\text{IMOD}}$	ip	A/D converter interface mode select	20	28	WDCK	ip/o	2fs clock
–	9	(NC)			21	29	Vss1	–	GND 1
7	10	Vss2	–	GND 2	–	30	(NC)		
8	11	DINR	ip	Rch input data	–	31	(NC)		
–	12	(NC)			22	32	BCK	ip/o	Output data bit clock
9	13	CC	o	A/D converter control signal	23	33	DOUT	o	Data output (Lch or Rch serial data output).
10	14	BBC	o	A/D converter control signal	–	34	(NC)		
–	15	(NC)			24	35	$\overline{\text{MUTE}}$	ip	Data output mute, ($\overline{\text{MUTE}}$ = L: DOUT = L)
					25	36	XTI	i	Oscillator Input (512fs: $\overline{\text{SCSL1}}$ = H, $\overline{\text{SCSL2}}$ = H) (256fs: $\overline{\text{SCSL1}}$ = H, $\overline{\text{SCSL2}}$ = L) (768fs: $\overline{\text{SCSL1}}$ = L, $\overline{\text{SCSL2}}$ = H) (384fs: $\overline{\text{SCSL1}}$ = L, $\overline{\text{SCSL2}}$ = L)
11	16	IBCK	ip	Input data bit clock input					
12	17	IBO	o	Input data bit clock output	26	37	XTO	o	Oscillator Output
13	18	DINL	ip	Lch input data	–	38	(NC)		
14	19	VDD2	–	+5V	27	39	$\overline{\text{CKEN}}$	ip	CKO output select, ($\overline{\text{CKEN}}$ = H, CKO = L)
–	20	(NC)			28	40	VDD1	–	+5V

*i = Input pin   ip = input with pull-up resistor   o = Output pin   ip/o = Input with pull-up resistor when $\overline{\text{FSEN}}$ = H, output with $\overline{\text{FSEN}}$ = L.

DIGITAL AUDIO PRODUCTS—DF   DF1750   8.3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}) .... −0.3V to +7.0V
Input Voltage (V_{IN}) .... −0.3V to V_{DD} + 0.3V
Soldering Temperature .... +255°C
Soldering Time 10s
Storage Temperature .... −40°C to +125°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DF1750P	28-Pin Plastic DIP	215
DF1750U	40-Pin Plastic SOIC	252

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

⊗ ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

DC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = −20°C to +80°C unless otherwise specified.

PARAMETER	PIN	SYMBOL	CONDITION	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
INPUTS							
Logic Family					CMOS		
Logic Voltages	XTI	V_{IL1}	For Clock Input			$0.3V_{DD}$	V
	XTI	V_{IH1}	For Clock Input	$0.7V_{DD}$			V
	XTI	V_{CLK}	For AC Coupling	1.8			V_{P-P}
	(1),(2)	V_{IL2}	$\overline{FSEN}$ = H			0.5	V
	(1),(2)	V_{IH2}	$\overline{FSEN}$ = H	2.4			V
Logic Currents	XTI	I_{IL1}	V_{IN} = 0V		5	10	μA
	XTI	I_{IH1}	V_{IN} = V_{DD}		5	10	μA
	(1),(2)	I_{IL2}	V_{IN} = 0V, $\overline{FSEN}$ = H		10	20	μA
Input Leakage Current	(1),(2)	I_{LH1}	V_{IN} = V_{DD}, $\overline{FSEN}$ = H			1.0	μA
OUTPUTS							
Logic Family					CMOS		
Logic Voltages	(2),(3)	V_{OL}	I_{OL} = 1.6mA, $\overline{FSEN}$ = L			0.4	V
	(2),(3)	V_{OH}	I_{OH} = −0.4mA, $\overline{FSEN}$ = L	2.5			V
POWER SUPPLY REQUIREMENTS							
Supply Voltage		V_{DD1}, V_{DD2}			+5		V
Supply Current		I_{DD}	V_{DD} = 5V(4), $\overline{FSEN}$ = H			30	mA
Power Dissipation		P_D	Nominal V_{DD}			250	mW
TEMPERATURE RANGE (AMBIENT, T_A)							
Specification				−20		+80	°C
Operating				−20		+80	°C

NOTES: (1) Refers to pins $\overline{SCSL1}$, $\overline{SCSL2}$, $\overline{TEST}$, $\overline{2DS}$, $\overline{IMOD}$, DINR, IBCK, DINL, $\overline{OW20}$, $\overline{MUTE}$, OBPOL, LRPOL, $\overline{FSEN}$, CKEN. (2) Refers to pins BCK, WDCK, LRCK. (3) Refers to pins CKO, CC, BBC, IBO, DOUT. (4) Test Condition: $\overline{SCSL1}$ = H, $\overline{SCSL2}$ = H, $\overline{TEST}$ = H, $\overline{2DS}$ = H, $\overline{IMOD}$ = H, $\overline{OW20}$ = H, $\overline{MUTE}$ = H, $\overline{OBPOL}$ = H, $\overline{LRPOL}$ = H, $\overline{FSEN}$ = L, $\overline{CKEN}$ = L. T_{CY} = 38ns (XTI Clock Period), C_L = 0pF (Capacitive Load), DINL, DINR (Applicable Input Data).

AC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = −20°C to +80°C unless otherwise specified.

XTI Clock

PARAMETER	SYMBOL	CONDITION SCSL1	CONDITION SCSL2	SYS FREQ	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
Crystal Oscillator Frequency	F_{OSC}	H	H	512fs[1]	8		26	MHz
		H	L	256fs	4		13	MHz
		L	H	768fs	12		26	MHz
		L	L	384fs	6		20	MHz
External Clock Pulse Width	t_{CW}	H	H	512fs	15		70	ns
		H	L	256fs	38		140	ns
		L	H	768fs	15		50	ns
		L	L	384fs	25		100	ns
External Clock Pulse Period	t_{CY}	H	H	512fs	38		125	ns
		H	L	256fs	77		250	ns
		L	H	768fs	38		84	ns
		L	L	384fs	50		167	ns
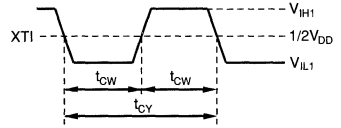
AC Coupling is required with an external clock.

NOTE: (1) fs = Sampling frequency.

ADC CONTROL SIGNAL TIMING (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = H

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{2DS}$ = H					
CC Pulse Width (H)	T1	65	1/256fs		ns
S/H Acquisition Time	T2	670	9/256fs		ns
CC-BBC Time	T3	285	4/256fs		ns
BBC Pulse Period	T4	228	3/256fs		ns
BBC Pulse Width (H)	T5	65	1/256fs		ns
BBC Pulse Width (L)	T6	140	2/256fs		ns
BBC-IBO Time	T7	140	2/256fs		ns
IBO Pulse Period	T8	228	3/256fs		ns
IBO Pulse Width (H)	T9	140	2/256fs		ns
IBO Pulse Width (L)	T10	65	1/256fs		ns
$\overline{2DS}$ = L					
CC Pulse Width (H)	T1	130	1/256fs		ns
S/H Acquisition Time	T2	1350	9/256fs		ns
CC-BBC Time	T3	570	4/256fs		ns
BBC Pulse Period	T4	456	3/256fs		ns
BBC Pulse Width (H)	T5	130	1/256fs		ns
BBC Pulse Width (L)	T6	280	2/256fs		ns
BBC-IBO Time	T7	280	2/256fs		ns
IBO Pulse Period	T8	456	3/256fs		ns
IBO Pulse Width (H)	T9	280	2/256fs		ns
IBO Pulse Width (L)	T10	130	1/256fs		ns
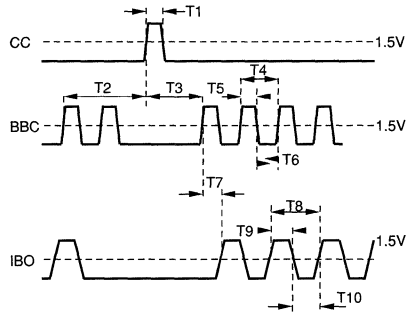
DF1750

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DIGITAL AUDIO PRODUCTS—DF

SERIAL INPUT TIMING (IBCK, DINL, DINR) WITH $\overline{IMOD}$=H

PARAMETER	SYMBOL	DF1750P/U			UNIT
		MIN	TYP	MAX	
$\overline{2DS}$ = H					
IBCK Pulse Width	t_{IBW}	50	1/256fs		ns
IBCK Pulse Period	t_{IBY}	3/12.928MHz[1]	3/256fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
$\overline{2DS}$ = L					
IBCK Pulse Width	t_{IBW}	50	1/128fs		ns
IBCK Pulse Period	t_{IBY}	3/12.928MHz[1]	3/128fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns

Normally, IBO output is connected to IBCK (Refer to the applications diagram).

NOTE: (1) 12.928MHz = 256 x 50.5kHz (max sampling frequency).

ADC CONTROL SIGNAL TIMING (CC, BBC, AND IBO) WITH $\overline{IMOD}$ = L

PARAMETER	SYMBOL	DF1750P/U			UNIT
		MIN	TYP	MAX	
$\overline{2DS}$ = H					
CC Pulse Width (H)	t_{CCW}		1/8fs		ns
BBC Pulse Width	t_{BBW}	130	1/128fs		ns
BBC Pulse Period	t_{BBY}		1/64fs		ns
IBO Pulse Width	t_{BOW}	130	1/128fs		ns
IBO Pulse Period	t_{BOY}		1/64fs		ns
CC-BBC Time	t_{CCBB}	-5	0	20	ns
CC-IBO Time	t_{CCBO}	130	1/128fs		ns
BBC-IBO Time	t_{BBBO}	130	1/128fs		ns
$\overline{2DS}$ = L					
CC Pulse Width (H)	t_{CCW}		1/4fs		ns
BBC Pulse Width	t_{BBW}	280	1/64fs		ns
BBC Pulse Period	t_{BBY}		1/32fs		ns
IBO Pulse Width	t_{BOW}	280	1/64fs		ns
IBO Pulse Period	t_{BOY}		1/32fs		ns
CC-BBC Time	t_{CCBB}	-5	0	20	ns
CC-IBO Time	t_{CCBO}	280	1/64fs		ns
BBC-IBOTime	t_{BBBO}	280	1/64fs		ns

SERIAL INPUT TIMING (IBCK, DINL, DINR) WITH $\overline{\text{IMOD}}$ = L

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
$\overline{\text{2DS}}$ = H					
IBCK Pulse Width	t_{IBW}	100	1/128fs		ns
IBCK Pulse Period	t_{IBY}	1/3.232MHz[1]	1/64fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
$\overline{\text{2DS}}$ = L					
IBCK Pulse Width	t_{IBW}	100	1/64fs		ns
IBCK Pulse Period	t_{IBY}	1/3.232MHz[1]	1/32fs		ns
Data Word Latch Set-up Time	t_{SL}	50			ns
Data Word Latch Hold Time	t_{HL}	50			ns
DINL, DINR Set-up Time	t_{SD}	25			ns
DINL, DINR Hold Time	t_{HD}	25			ns
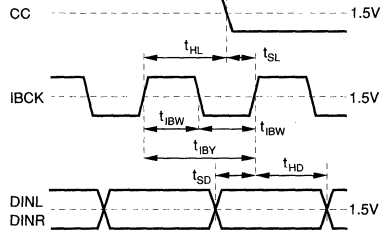
Normally, IBO output is connected to IBCK.
(Refer to the application diagram).

NOTE: (1) 3.232MHz = 64 x 50.5kHz (max sampling frequency).

SERIAL OUTPUT TIMING WITH $\overline{\text{FSEN}}$ = H

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT	REMARKS
BCK Pulse Width	t_{BCW}	100	1/128fs		ns	
BCK Pulse Period	t_{BCY}	1/3.232MHz[1]	1/64fs		ns	
LRCK Pulse Width	t_{LCW}		1/2fs		µs	Duty = 50%
LRCK Pulse Period	t_{LCY}	1/50.5kHz	1/fs		µs	
LRCK Set-up Time	t_{BL}	50			ns	
LRCK Hold Time	t_{LB}	50			ns	
Output Data Hold Time	t_{H}	0			ns	C_L = 0pF
Output Data Delay Time	t_{D}			100	ns	C_L = 15pF
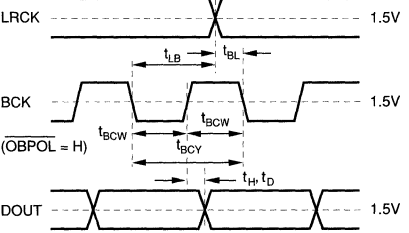
NOTE: (1) 3.232MHz = 64 x 50.5kHz (max sampling frequency).

SERIAL OUTPUT TIMING WITH $\overline{\text{FSEN}}$ = L

PARAMETER	SYMBOL	DF1750P/U MIN	DF1750P/U TYP	DF1750P/U MAX	UNIT
BCK Pulse Width	t_{OBCW}	140	1/128fs		ns
BCK Pulse Period	t_{OBCY}		1/64fs		ns
WDCK Pulse Width	t_{WDCW}		1/4fs		µs
WDCK Pulse Period	t_{WDCY}		1/2fs		µs
LRCK Pulse Width	t_{LRCW}		1/2fs		µs
LRCK Pulse Period	t_{LRCY}		1/fs		µs
Output Data Delay Time	t_{DHL}	−10		30	ns
	t_{DLH}	−10		30	ns

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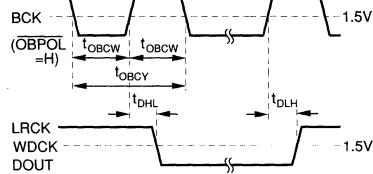
DIGITAL AUDIO PRODUCTS—DF

THEORY

According to the Nyquist Theorem, digital audio recordings sampled at a rate of 44.1kHz (CD) or 48kHz (DAT) should accurately reproduce the full 20kHz audio bandwidth. Unfortunately, if frequencies higher than1/2 the sample rate are seen at the input of an analog-to-digital converter, aliasing back into the baseband will occur. At these sample frequencies, the way to assure that aliasing does not occur is to use complicated high order filters at the input of the ADC . These filters can be expensive and they can also have undesirable phase characteristics. These problems can be avoided by using an oversampling ADC (such as the PCM1750) with a decimating filter, where a high order filter can be replaced with a low order filter which has very little phase distortion (Figure 1).

With the oversampling-decimating technique, the input signal (Figure 2a) is band limited by a low order analog low-pass filter as shown in Figure 2b. This signal is 4-times oversampled, with its spectra and foldover noise shown in Figure 2c. The DF1750 first rejects the high frequency components of the 4fs ADC output (Figure 2d). A 1/2 decimating filter then processes this data into a 2fs data stream. This output spectra is shown in Figure 2e. The high frequency components of the 2fs data are then removed, producing the output spectra shown in Figure 2f. A second 1/2 decimating filter processes the 2fs data to a final fs data stream and the original signal is restored without distortion (Figure 2g). Note, when operating in the 1/2 decimating mode the DF1750 processes data through the first LPF and a single 1/2 decimating filter only.
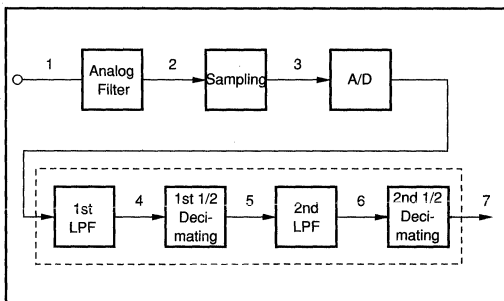
FIGURE 1. A Block Diagram of an Oversampling ADC Followed by Digital Decimation.
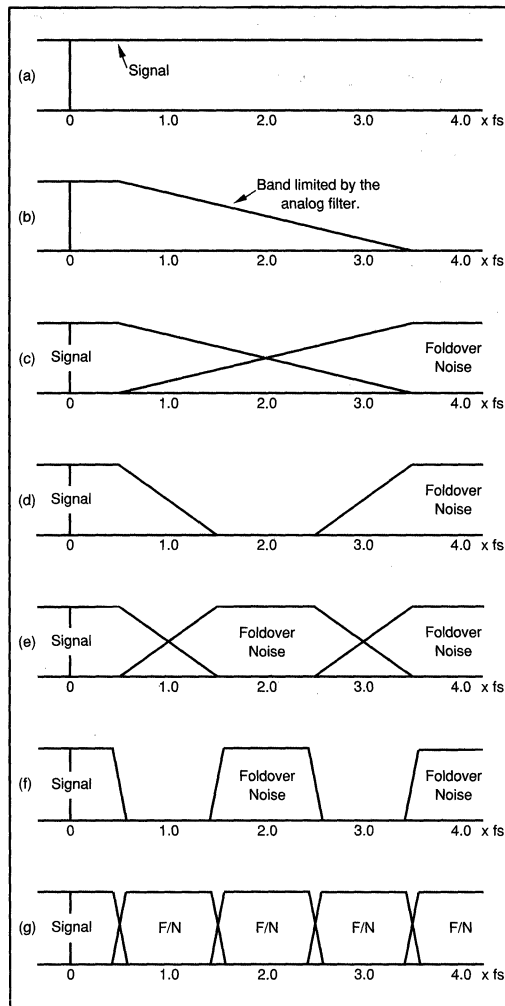
FIGURE 2. The Associated Spectra of the Oversampling-Decimating Technique.

THEORETICAL FILTER CHARACTERISTICS

1/4 DECIMATING, INPUT DATA FREQUENCY = 4fs

PARAMETER	CHARACTERISTICS
Passband	DC to 0.4583fs
Stopband	0.5417fs and Above
Passband Ripple	±0.0005 dB
Stopband Attenuation	95dB min, 0.5417fs to 1.4583fs
	88dB min, 1.4583fs to 2.5417fs
	95dB min, 2.5417fs to 3.4583fs
Group Delay Time	Constant, Linear Phase

1/2 DECIMATING, INPUT DATA FREQUENCY = 2fs

PARAMETER	CHARACTERISTICS
Passband	DC to 0.4583fs
Stopband	0.5417fs and above
Passband Ripple	±0.0002dB
Stopband Attenuation	95dB min, 0.5417fs to 1.4583fs
Group Delay Time	Constant, Linear Phase

DF1750 1/4 Decimating Filter Tranfer Characteristics.
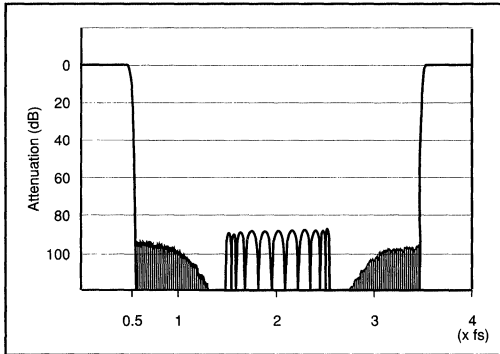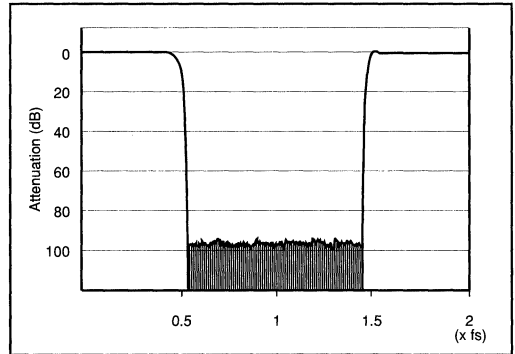
DF1750 1/2 Decimating Filter Transfer Characteristics.
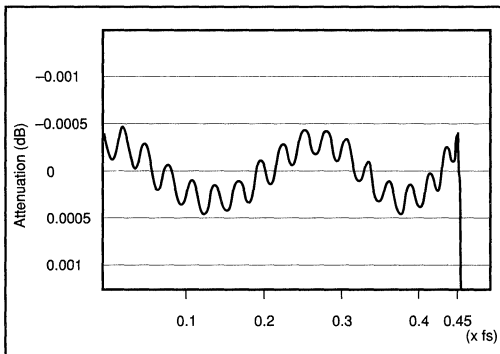
DF1750 1/4 Decimating Passband Frequency Response.
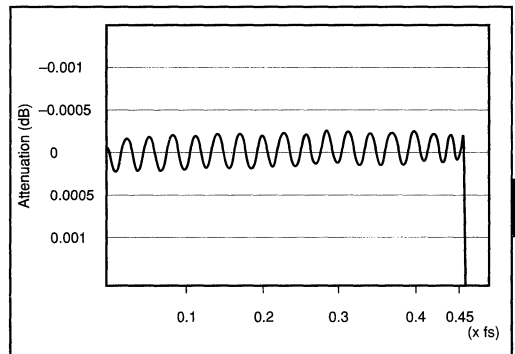
DF1750 1/2 Decimating Passband Frequency Response.
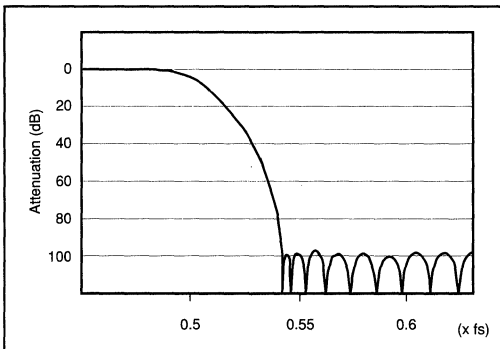
DF1750 1/4 Decimating Transitionband Frequency Response.
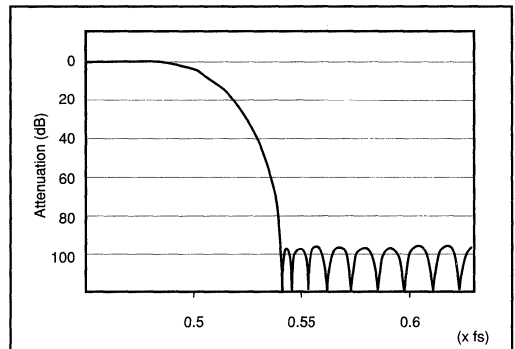
DF1750 1/2 Decimating Transitionband Frequency Response.

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DIGITAL AUDIO PRODUCTS—DF

BURR - BROWN®
BB

Burr-Brown IC Data Book—Data Conversion Products

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FUNCTIONAL DESCRIPTION

1/4 AND 1/2 DECIMATING FUNCTIONS

1/4 or 1/2 decimating filtering converts 4fs or 2fs oversampled data back to a sampling rate of fs data by a digital filtering algorithm. $\overline{2DS}$ is used to select 1/4 or 1/2 decimating.

$\overline{2DS}$ = H; 1/4 decimating (0.5417fs ~ 3.4583fs)
$\overline{2DS}$ = L; 1/2 decimating (0.5417fs ~ 1.4583fs)

The filter arithmetic block consists of two 1/2 decimating finite impulse response (FIR) filters as shown in Figure 3.
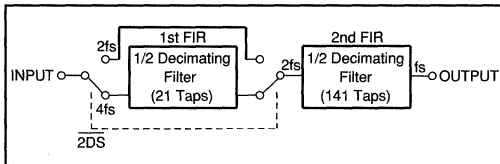
FIGURE 3. Filter Arithmetic Structure

SYSTEM CLOCK

The system clock frequency can be 256fs, 364fs, 512fs, or 768fs selectable with $\overline{SCSL1}$ and $\overline{SCSL2}$ as indicated in Table I. An external clock (applied to Pin XTI) or crystal oscillator (Pins XTI and XTO) can be employed. AC coupling is required for an external clock.

The XTI input clock is available as an output at pin CKO, when $\overline{CKEN}$ = L. CKO stays low when $\overline{CKEN}$ = H.

$\overline{SCSL1}$		H		L	
$\overline{SCSL2}$		H	L	H	L
XTI Clock Frequency	F_{XI}	512fs	256fs	768fs	384fs
Clock Input		External Clock or Crystal Oscillator			
Internal System Clock Frequency	F_{SYS}	256fs			

TABLE I. System Clock and Internal Clock Frequency Selection.

SERIAL DATA INPUT

The DF1750 is programmed for accepting the correct number of input data bits per word by the $\overline{IMOD}$ pin. A 16-bit input word is selected with $\overline{IMOD}$ = L and an 18-bit input word is selected with $\overline{IMOD}$ = H. Set $\overline{IMOD}$ = H for use with the PCM1750. The serial input data format is two's complement and MSB first. Both the left and right channel data are loaded into the DF1750 simutaneously.

Each bit of the data is loaded to each channel's SIPO (Serial/parallel conversion register) by the rising edge of the Input Bit Clock, IBCK (Figure 4). After the serial input data is loaded, the data is latched into a parallel register by the rising edge of CC for $\overline{IMOD}$ = H and the falling edge of CC for $\overline{IMOD}$ = L (Figure 5).
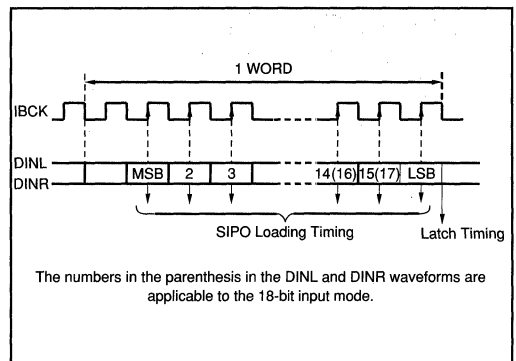
FIGURE 4. SIPO Input Data Loading Timing.
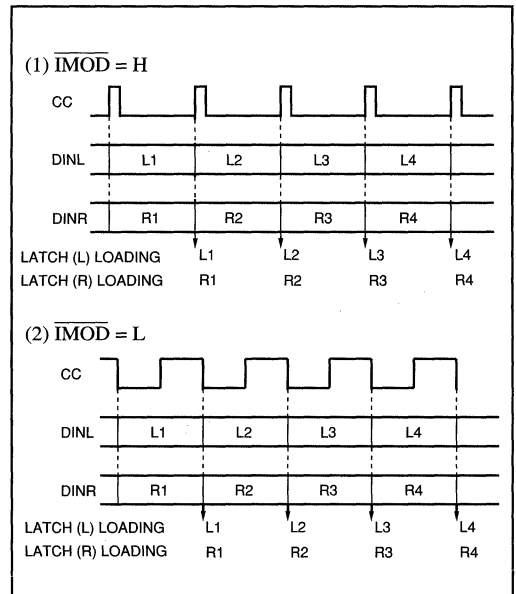
FIGURE 5. Input Data Latch/Loading Timing.

ADC CONTROL SIGNALS (CC, BBC, AND IBO) WITH $\overline{\text{IMOD}}$ = H
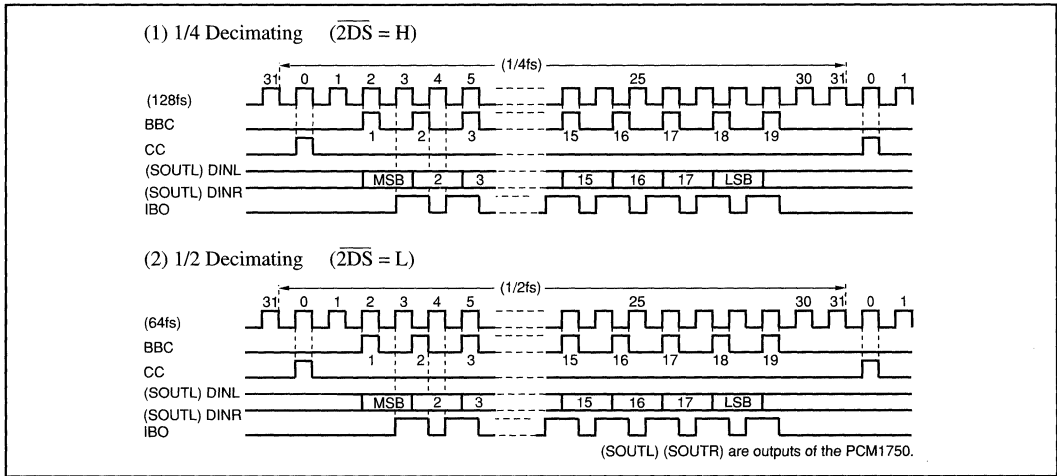
FIGURE 6. ADC Control Signals With $\overline{\text{IMOD}}$ = H. (Applicable for use with the Burr-Brown PCM1750 ADC).

ADC CONTROL SIGNALS
(CC, BBC AND IBO) WITH $\overline{\text{IMOD}}$ = L
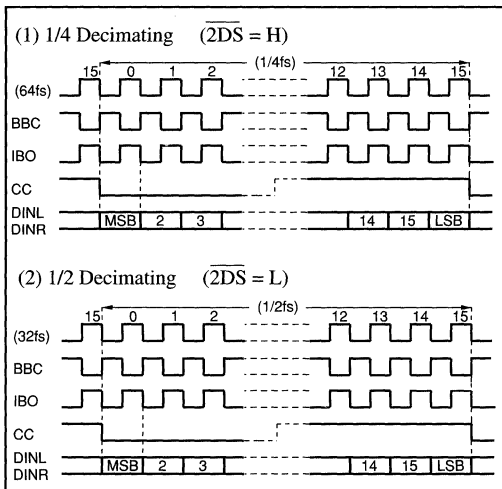
FIGURE 7. ADC Control Signals with $\overline{\text{IMOD}}$ = L.

OUTPUT INTERFACE
(BCK, WDCK, LRCK, $\overline{\text{OBPOL}}$, $\overline{\text{LRPOL}}$, $\overline{\text{FSEN}}$)

The output of the DF1750 can be interfaced to many different devices by programming the output interface pins. These pins provide the following functions:

a. Output control clocks, BCK, WDCK, LRCK I/O selection ($\overline{\text{FSEN}}$).

$\overline{\text{FSEN}}$ = H; BCK WDCK, LRCK = Input
$\overline{\text{FSEN}}$ = L; BCK WDCK, LRCK = Output

b. Sampling rate clock (LRCK)
When $\overline{\text{FSEN}}$ = H, apply a 50% duty cycle sampling frequency (fs) to pin LRCK.
When $\overline{\text{FSEN}}$ = L, a fs clock generated from the system clock is available at pin LRCK.

c. Word Clock (WDCK)
When $\overline{\text{FSEN}}$ = L, WDCK provides a 2fs clock that is derived from the system clock.

d. Output bit clock
When $\overline{\text{FSEN}}$ = H, apply a 64fs clock to pin BCK.
When $\overline{\text{FSEN}}$ = L, a 64fs clock generated from the system clock is available at pin BCK.

e. LRCK polarity selection ($\overline{\text{LRPDL}}$)
$\overline{\text{LRPOL}}$ = H; Lch/Rch = Low/High
$\overline{\text{LRPOL}}$ = L; Lch/Rch = High/Low
(Regardless of LRCK's I/O mode).

f. BCK polarity selection ($\overline{\text{OBPOL}}$)
$\overline{\text{OBPOL}}$ = H; DOUT changes state at rising edge of BCK.
$\overline{\text{OBPOL}}$ = L; DOUT changes state at falling edge of BCK.
(Regardless of BCK's I/O mode).

g. Timing relation between XTI and BCK, WDCK, LRCK clocks.
When $\overline{\text{FSEN}}$ = H, clocks to BCK and LRCK must be synchronized to XTI. However, there is no limit on their phase differences (between XTI and BCK, LRCK clocks).

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DIGITAL AUDIO PRODUCTS—DF

SERIAL DATA OUTPUT

The number of bits per output data word is selected with the $\overline{OW20}$ pin. With $\overline{OW20}$ = H a 16-bit output is selected and with $\overline{OW20}$ = L a 20-bit output is selected.

The serial output data format is two's complement and MSB first. The left and right channel outputs are alternated, with the left channel preceeding the right channel. Each data word is allocated in each pulse of LRCK and the LSB is located at the end of the LRCK pulse as shown in Figure 8.

The output of the DF1750 can be muted by the use of the $\overline{MUTE}$ pin. When $\overline{MUTE}$ = L, the output stays low (muted). Under normal operation $\overline{MUTE}$ = H.
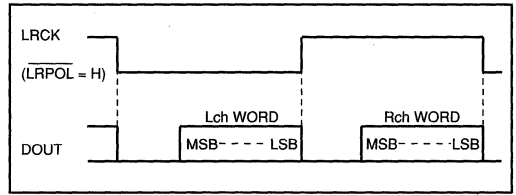
FIGURE 8. Output Timing.

TIMING DIAGRAMS

INPUT

1/2 decimating $(\overline{2DS} = L)$ $\overline{IMOD} = H$

NOTE: Bit 1 is the most significant bit.

1/2 decimating $(\overline{2DS} = L)$ $\overline{IMOD} = L$

NOTE: Bit 1 is the most significant bit.
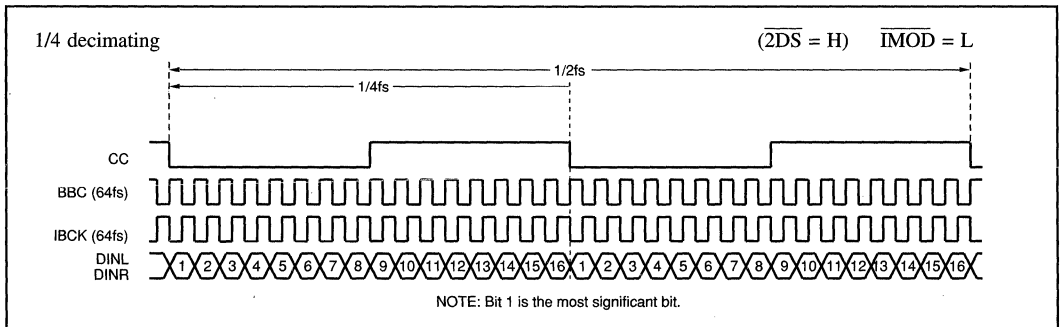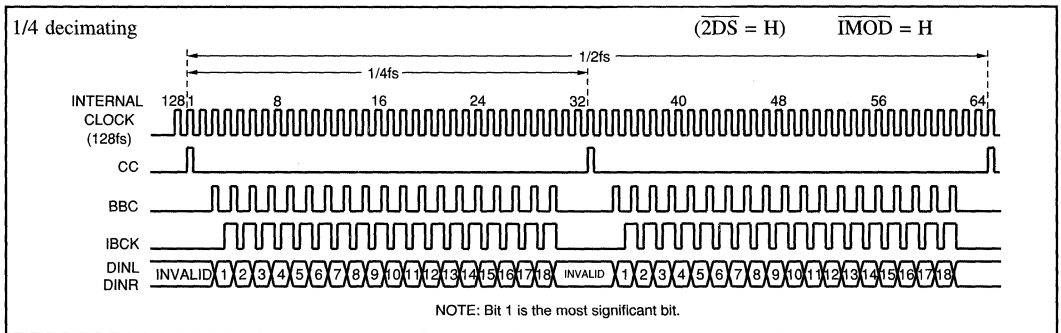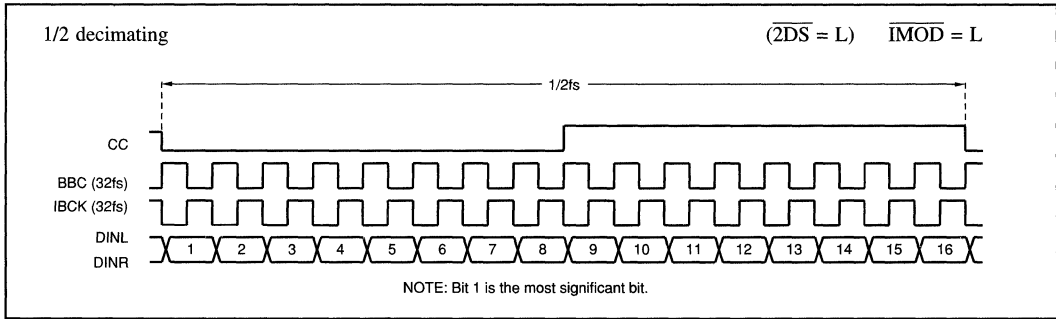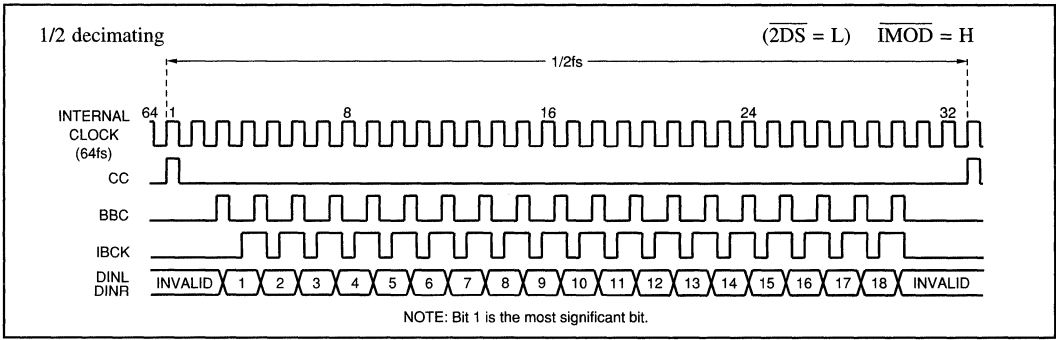
OUTPUT
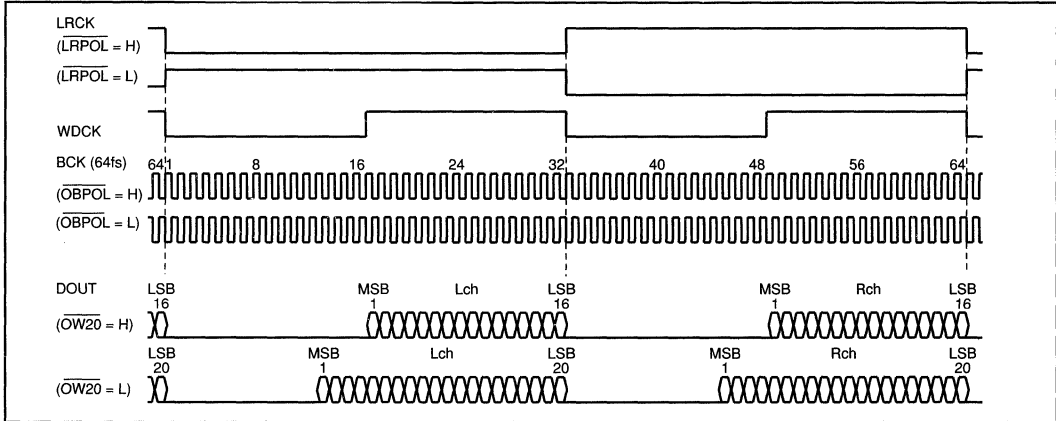
APPLICATIONS

A typical circuit configuration for digital audio recording is shown in Figure 9. Each of the stereo input channels passes through a six pole Generalized Immitance Converter (GIC) low pass analog filter. This filter features extremely low distortion and negligible phase shift. The band limited signals are 4X oversampled by the dual-channel PCM1750 A/D converter. Clock and convert signals are provided to the PCM1750 by the DF1750. The 4fs oversampled data of the PCM1750 is filtered by the DF1750 to provide a data stream of fs. A PCM1750/DF1750 evaluation board, DEM1133, is available from Burr-Brown. This board incorporates the features mentioned above as well as an AES/EBU interface, test points for monitoring both the serial and parallel data outputs, and a breadboard area for user experimentation.

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DIGITAL AUDIO PRODUCTS—DF
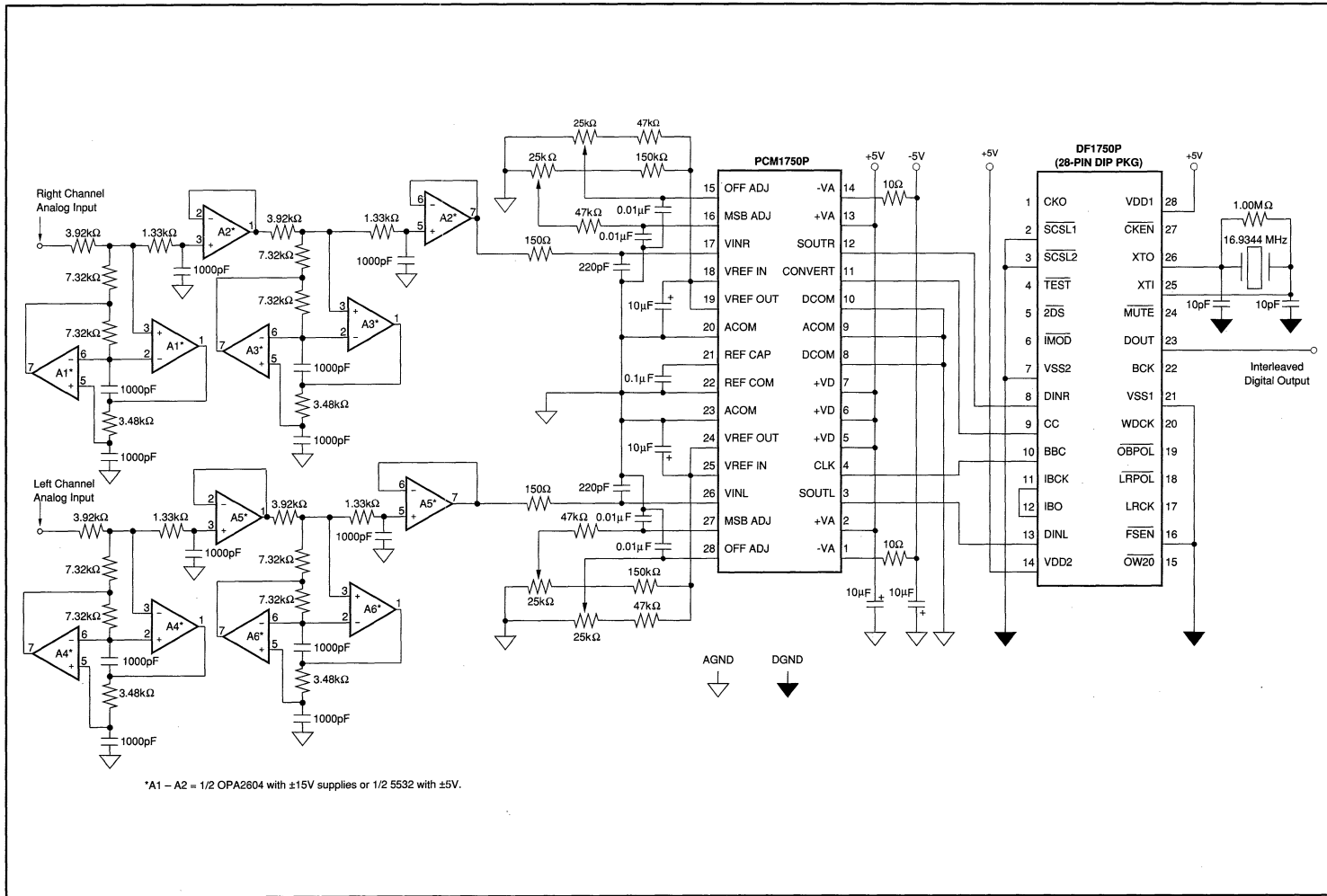
FIGURE 9. Circuit diagram for a typical digital audio application using the DF1750 for decimating oversampled data from the output of the PCM1750 dual channel ADC. The OPA2604s are configured in a generalized immittence converter (GIC) filter arrangement to avoid aliasing in the PCM1750.

Appendix A

Demonstration Boards

Burr-Brown offers a wide variety of demonstration boards for both its Linear and Data Conversion Products. New boards for new products are continually being added to the selection— contact the factory your local salesperson for availability.

NOTE: All evaluation fixtures whose model number ends with a 'C' include the product or products mentioned. All other do not include the product, except where specifically noted.

MODEL	PRODUCT	DESCRIPTION
DEM-ACF2101BP-C	ACF2101BP	Evaluation Fixture with Programmable Timing Generator
DEM-ADC614-E	ADC603/614	Evaluation Fixture—Digital/Analog Output (Formerly DEM 1123)
DEM-ADC701-E	ADC701/SHC702	Evaluation Fixture—Digital/Analog Output (Formerly DEM 1113)
DEM-ADS7804/05C	ADS7804/05	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7806/07C	ADS7806/07	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7808/09C	ADS7808/09	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7810/19C	ADS7810/19	Evaluation Fixture—Analog Input and Digital Output
DEM-BUF600-1GC	BUF600AP	Evaluation Fixture—900MHz Buffer Amplifier
DEM-BUF601-1GC	BUF601AP	Evaluation Fixture—650MHz Buffer Amplifier
DEM-DAC600-E	DAC600	Evaluation Fixture—SMA Digital Inputs and Analog SMA Output (an external reference can be provided via a BNC input). The fixture provides a socket for the DAC600, which must be ordered separately.
DEM-DAC650J-E	DAC650JL	Evaluation Fixture—Digital Input and Analog Output (all SMA connectors). The part is included and soldered to the board.
DEM-DAC650K-E	DAC650KL	Evaluation Fixture—Digital Input and Analog Output (all SMA connectors). The part is included and soldered to the board.
DEM-DDC101P-C	DDC101P	Evaluation Fixture, includes the DDC101 board, interface board to connect to parallel PC-port and software. Supports all DDC101 options plus FFT.
DEM-DSP102/202C	DSP102/202	Evaluation Fixture—DSP Interface with Programmable Timing Generator
DEM-ISC300-SC	ISC300	Evaluation Fixture—Universal Precision Isolated Measurement Channel.
DEM-ISO212-8-GC	ISO212	Evaluation Fixture—8 Input Channels, Tri-port isolation
DEM-IXR100-SC	IXR100	Evaluation Fixture—Isolated, self-powered 4-20mA two-wire transmitter

DEMONSTRATION BOARDS

A

MODEL	PRODUCT	DESCRIPTION
DEM-MPC100-1GC	MPC100AU	Evaluation Fixture—4 to 1 High Speed Multiplexer and Output Buffer BUF601AU
DEM-MPC102-1GC	MPC102AU	Evaluation Fixture—Dual 2 to 1 High Speed Multiplexer and optional output buffer, BUF601AU
DEM-OPA620G/P-C	OPA620/621	Evaluation Fixture Kit for DIP packages—Generic Op Amp Configurations (Formerly DEM 1135)
DEM-OPA622-1GC	OPA622AP	Evaluation Fixture—For voltage and current feedback configuration
DEM-OPA623-1GC	OPA623AP	Evaluation Fixture—High Speed current feedback Op Amp
DEM-OPA628AP-C	OPA628AP	Evaluation Fixture-User selectable configuration for the DIP package
DEM-OPA628AU-C	OPA628AU	Evaluation Fixture-User selectable configuration for the SOIC package
DEM-OPA64XP-Y	OPA64XP	Evaluation Fixture—Three boards are offered for the DIP package of the OPA64X series of operational amplifiers. DEM-OPA64XP-F: follower configuration; DEM-OPA64XP-N: noninverting configuration; DEM-OPA64XP-I: inverting configuration. (Note: each board will operate with any OPA64XP series op-amp. No component is included—it must be ordered separately.)
DEM-OPA64XU-Y	OPA64XU	Evaluation Fixture—Three boards are offered for the SOIC package of the OPA64X series of operational amplifiers. DEM-OPA64XU-F: follower configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-I: inverting configuration. (Note: each board will operate with any OPA64XU series op-amp. No component is included—it must be ordered separately.)
DEM-OPA660-XXX	OPA660	Evaluation Fixture—Five boards are offered for five different configurations. DEM-OPA660-1GC: Diamond transistor and buffer; DEM-OPA660-2GC: Current-feedback operational amplifier; DEM-OPA660-3GC: Direct-feedback amplifier; DEM-OPA660-4G: Layouts for all applications using SOIC (unassembled); DEM-OPA660-5G: Layouts for all applications using DIP packages (unassembled)
DEM-OPA2662-1GC	OPA2662	Evaluation Fixture-High speed voltage controlled current source
DEM-PCM1700P-C	PCM1700	Evaluation Fixture—Serial/SPDIF Inputs (Formerly DEM-1143). Includes product.
DEM-PCM1702	PCM1702	Evaluation Fixture—Serial digital input, 8X digital interpolator (NPC5842), and analog output. A PCM1702P is included. The board will interface directly to the DEM-1760. The fixture does not accept SPDIF input.
DEM-PCM1710	PCM1710U	Evaluation Fixture—Serial Digital Audio In. Left and Right channel analog out.

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MODEL	PRODUCT	DESCRIPTION
DEM-DAI1710	PCM1710U	Evaluation Fixture—Includes Digital Audio Interface (DAI) receiver chip and dual 2nd-order lowpass output filters
DEM-PCM1715	PCM1715U	Evaluation Fixture—Serial digital audio in. Left and right channel analog out
DEM-PCM1750P-C	PCM1750	Evaluation Fixture—Serial/Parallel Output, SPDF Out (Formerly DEM 1133). Includes product.
DEM-PCM1760	PCM1760/DF1760	Evaluation Fixture—Analog input and serial digital output. A PCM1760P and DF1760P are included. The board will interface directly to the DEM-1702. The fixture does not provide SPDIF output.
DEM-PCM63P-C	PCM63P	Evaluation Fixture—Includes Dual PCM63s, SPDIF Input
DEM-PCM67P-C	PCM67P	Evaluation Fixture—Includes Dual PCM67s (single/dual supply operation), SPDIF Input
DEMPCM78P-C	PCM78P	Evaluation Fixture—Analog Input, Parallel Data Output. Includes SHC5320 sample hold and PCM56 as a reconstruction ADC (formerly DEM-1122).
DEM-SHC605AU	SCH605AU	Evaluation Fixture—Analog input, digital control input, and sample/hold output (all SMA connectors). A SHC605AU is included and is soldered to the board.
DEM-SDM862/863-1-SC		SDM862/863 Evaluation Fixture—LCC package, also covers SDM872/873
DEM-SDM862/863-2-SC		SDM862/863 Evaluation Fixture—PGA package, also covers SDM872/873
DEM-VCA610AP-C	VCA610AP	Evaluation Fixture—Voltage Controlled Amplifier

DEMONSTRATION BOARDS

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DEM-ADS605HB
EVALUATION FIXTURE
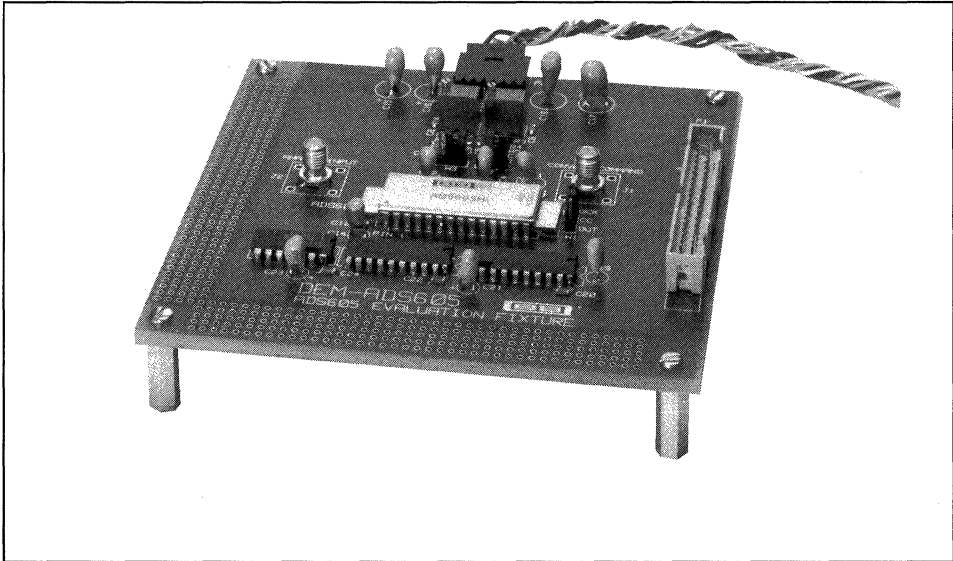
FEATURES

● **UNIVERSAL INPUT AND OUTPUT CONNECTORS**
● **DUT INCLUDED WITH DEMO BOARD**
● **OPTIMUM PC BOARD LAYOUT AND BYPASSING**
● **GAIN AND OFFSET ADJUST INCLUDED**
● **5" x 5" (12.7 cm x 12.7cm) DIMENSIONS**

APPLICATIONS

● **EVALUATE ADS605H OR ADS605HB PERFORMANCE**
● **EVALUATE HIGH FREQUENCY THREE-LAYER PC BOARD LAYOUT**
● **INCOMING INSPECTION TEST FIXTURE**

DESCRIPTION

The DEM-ADS605 evaluation fixtures are fully assembled printed circuit boards including the ADS605. By supplying the power, analog input and convert command signals, the ADS605 can be quickly evaluated. A choice of either the ADS605H or ADS605HB is included with this board.

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POWER SUPPLIES

This demonstration board requires the application of a
−5.2V supply, a +5V supply and a ground.

OFFSET AND GAIN

The gain and offset potentiometers (shown in Figure 1) have
a ±2% and ±2% adjustment range respectively and are
hooked up to the ADC. If these adjustments are not desired,
ground pins 21 and 22 with jumpers W2 and W3.

APPLYING A CONVERT COMMAND

The convert command pulse should be generated from a low
jitter source. A convert command with jitter will degrade
your realized SNR.

The convert command pulse width "high" time should be
between 37ns and 47ns long. A pulse width of 50ns (a 50%
duty cycle) will NOT be acceptable. A convert command
pulse width outside of this range will degrade the DNL and
SNR performance substantially due to digital noise coupling
into the internal analog circuitry at sensitive times in the
internal conversion cycle.

LATCHING THE OUTPUT DATA

The data from the TTL outputs of the ADS605 is factory
preset to be latched into buffered TTL latches on the falling
edge of the Data Valid signal. Alternatively, jumper "W1"
can be set to latch on the falling edge of the convert
command.

ADS605 ORDERING INFORMATION

DEM-ADS605 ( ) H HB

Basic Model Number
Performance Grade Code

Package Code
With Standard ADS605H
With Standard High Grade ADS605HB
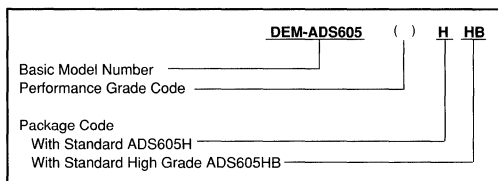
PARTS LIST

REFERENCE DESIGN	DESCRIPTION	QUANTITY
C1, C4, C5, C6, C7 C8, C9, C10, C11, C13, C20, C22, C24	CHIP CAP C1206A104K 5RAC (0.1µF)	13
C2, C3, C12, C14, C19, C21, C23	Kemet T356F226K106AS (2.2µF) Tantalum	7
C15, C16, C17, C18	Kemet T356J107K010AS (100µF) Tantalum	4
R1, R2, R5, R8	RN55C5ROF 1% Film Resistor (51Ω)	4
R4, R7	1206 Surface Mount (10KΩ)	2
R3, R6	3299W001202 (2k pot)	2
Advanced Interconnections	KSS100-85TG (Pin)	14
U1, U2	74F574 Buffered Latch	2
U3	74F14 Inverter Gates	1
P1	102203-3 (40-pin plug) Amp	1
P2	102203-3 (6-pin plug)	1
J1, J2	142-0701-201 EF Johnson DIGI-Key SMA connector	2
DUT	ADS605	1
W1, W2, W3	Jumper TS-120-G-A Samtec	3
Shunt Samtect	Snt-100-BK-G-H	3

DEM-ADS605

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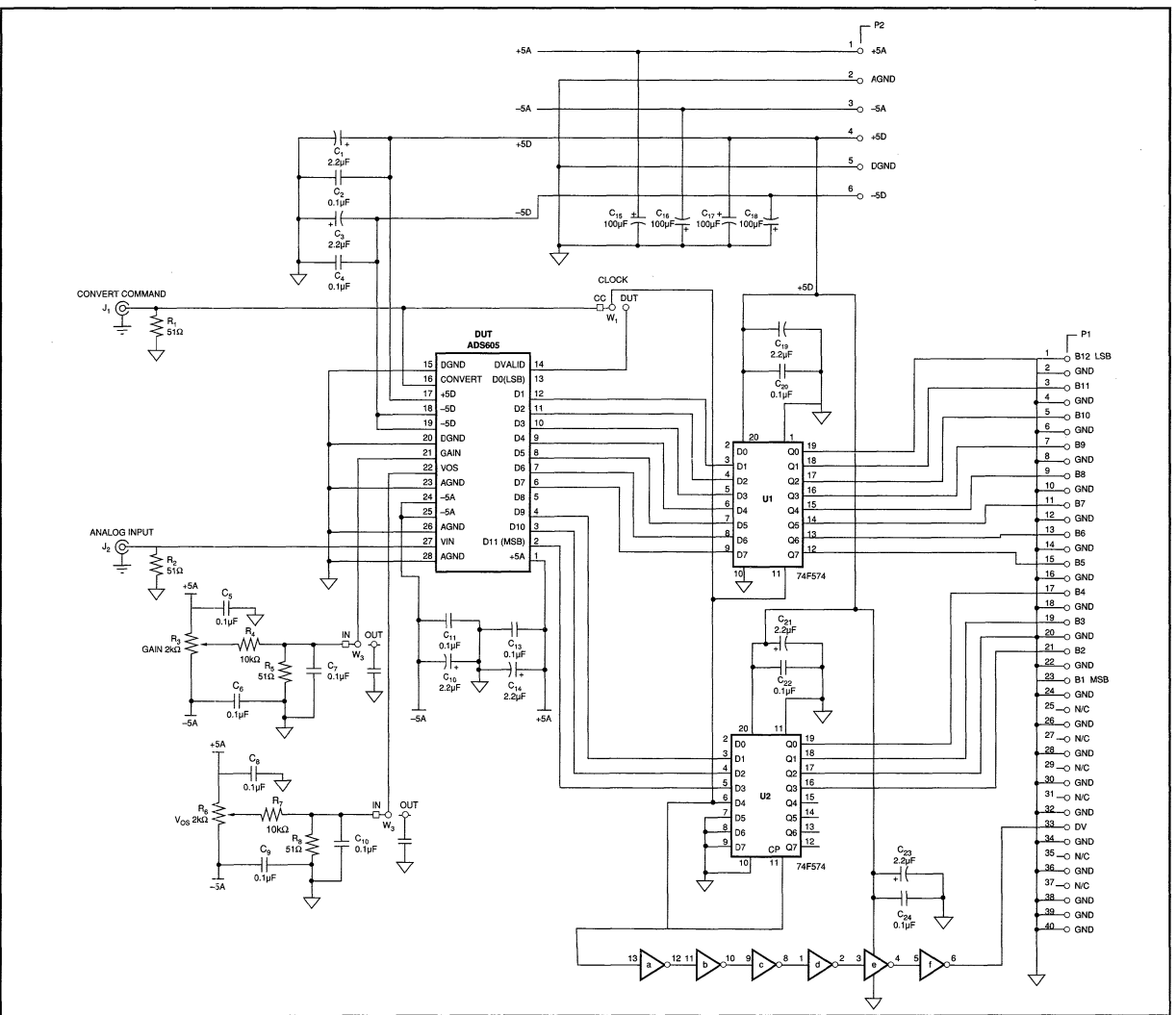
FIGURE 1. Circuit Diagram of ADS605HB.

For Immediate Assistance, Contact Your Local Salesperson
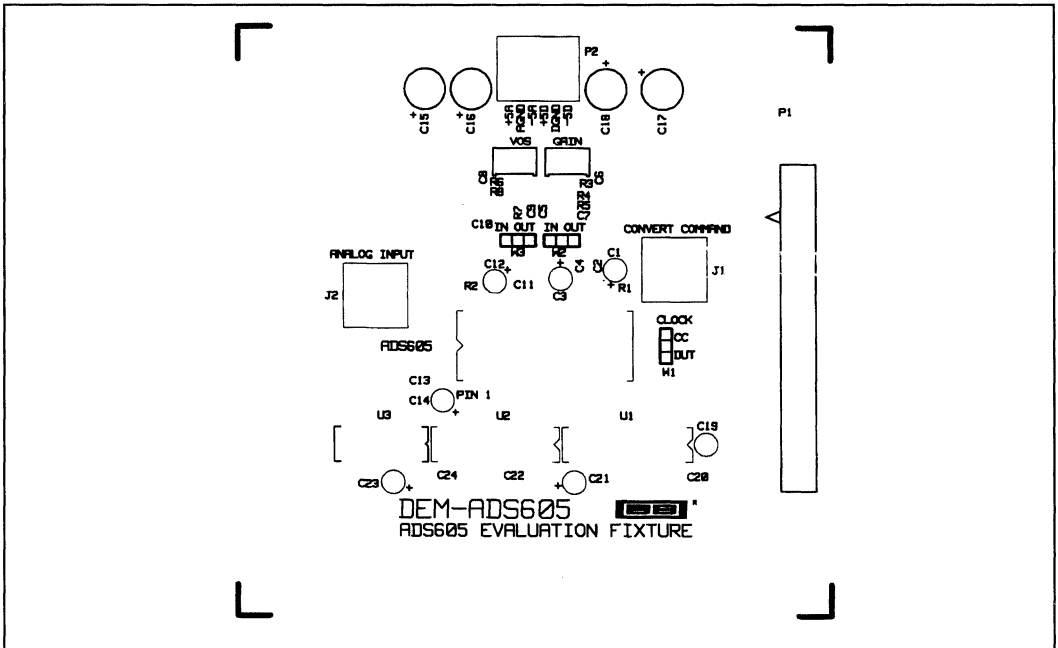
FIGURE 2. ADS605 Silkscreen.
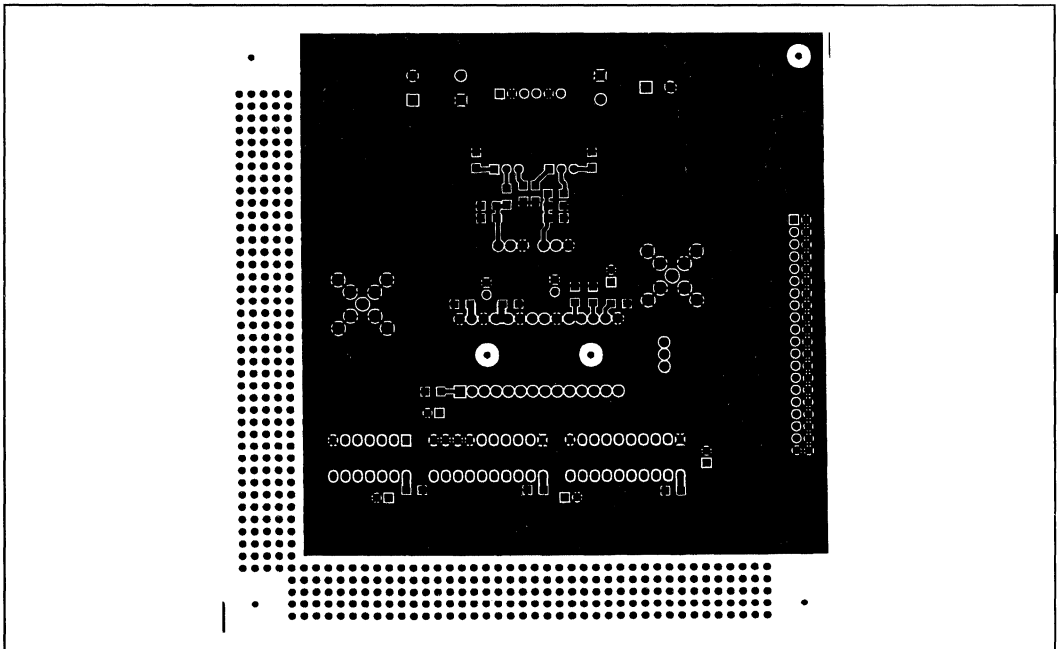
FIGURE 3. ADS605 Top Layer Analog Ground Plane, Top View.
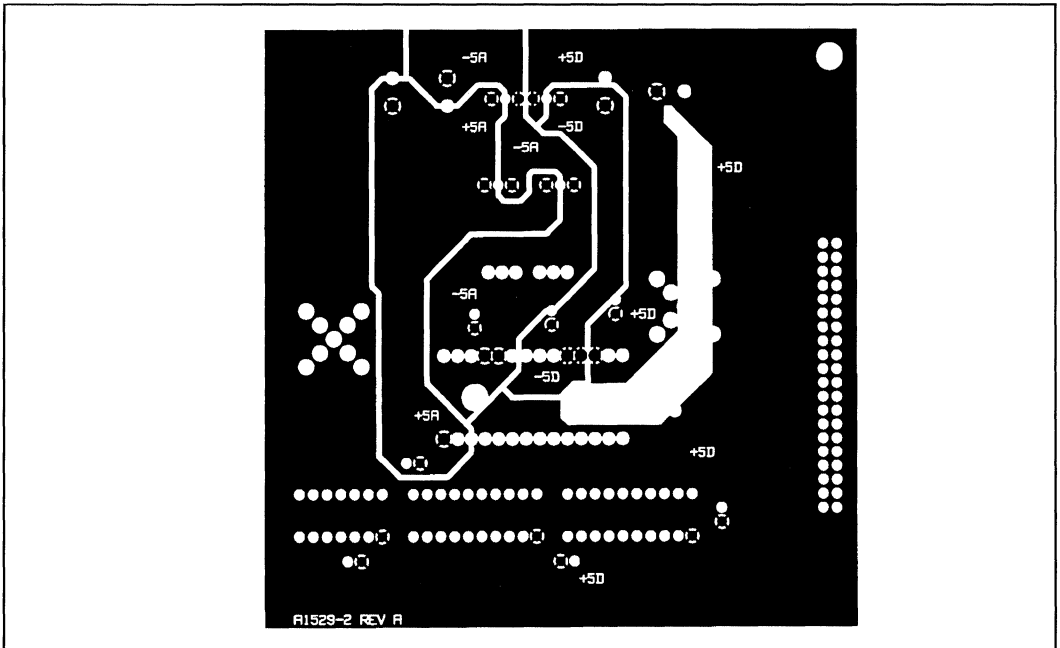
FIGURE 4. ADS605 Middle Layer Power Plane, Top View.
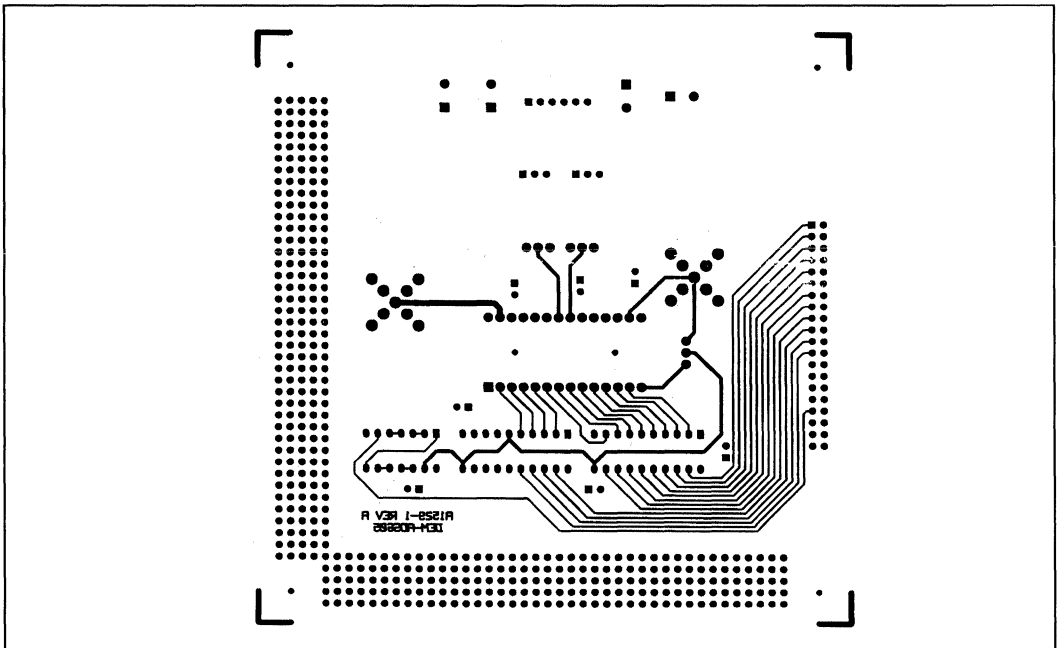
FIGURE 5. ADS605 Bottom Layer, Interconnect, Top View.

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DEM-ADS7804/05C

EVALUATION FIXTURE

DEM-ADS7804/05

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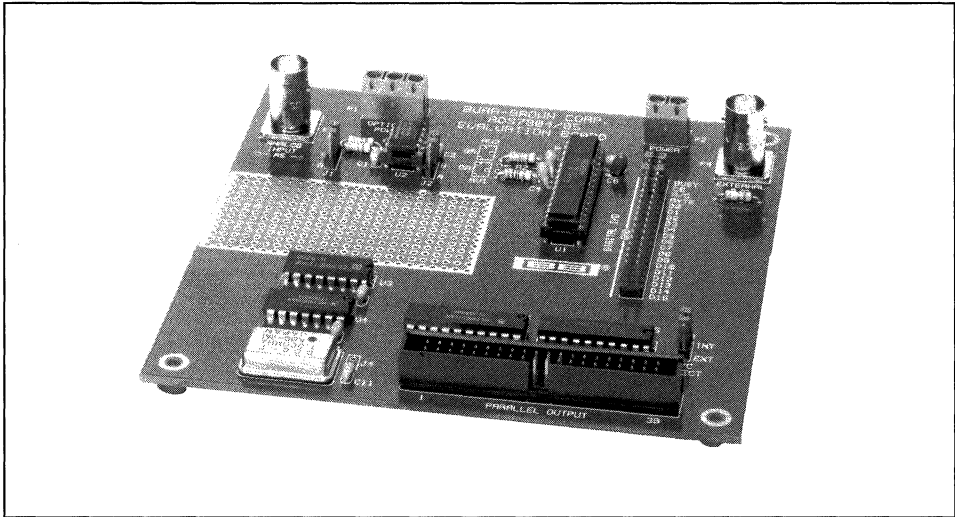
FEATURES

- ● **100kHz 12-BIT ADS7804P AND 16-BIT ADS7805P INCLUDED**
- ● **16-BIT BUFFERED PARALLEL OUTPUT**
- ● **CONNECTOR FOR ALL DIGITAL I/O PINS**
- ● **CRYSTAL OSCILLATOR BASED 100kHz CONVERT COMMAND GENERATOR**
- ● **EXTERNAL CONVERT COMAND CONNECTOR**
- ● **PROTOTYPE AREA**

APPLICATIONS

- ● **EVALUATE ADS7804P AND ADS7805P PERFORMANCE**
- ● **BREADBOARD COMPLETE ANALOG SYSTEM**
- ● **EVALUATE SIMPLE TWO-LAYER PCB LAYOUT**
- ● **INCOMING INSPECTION TEST FIXTURE**

DESCRIPTION

The DEM-ADS7804/05C Evaluation Fixture is a fully assembled printed circuit board used to evaluate ADS7804P and ADS7805P. This device incorporates an analog input amplifier (with provisions to bypass this amplifier), a parallel digital output buffer, a crystal oscillator based 100kHz convert command generator, an external convert command connector and a 2.3" x 1.2" breadboard area. The DEM-ADS7804/05C achieves full converter performance on a two-layer board.

This fixture requires only a single +5V power supply. An optional bipolar power supply connector is provided for the input amplifier and breadboarding.

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TABLE OF CONTENTS

HOW TO USE THIS MANUAL

A table and diagrams are included in the "Factory Settings" section showing how the board is configured from the factory. A listing of other components, which are shipped with the board, is also included.

The Step-by-Step Basic Operations section describes all of the options. At the end of each step, a figure illustrates factory settings. Items installed are highlighted in those figures.

For further details on the OPA671, ADS7804P, ADS7805P, or any other device on the DEM-ADS7804/05C, refer to the specific product data sheet.

FIGURE 1. PCB Legend.

FACTORY SETTINGS

With a +5V supply connected to P2, the DEM-ADS7804/05C starts converting at 100kHz with an input range of ±10V. Data can be read in bytes or full parallel from P5.

Buffered full parallel can be read from P6. The following is a listing of "factory settings".

MAKE SELECTION FOR EACH STEP (1)	FACTORY SETTINGS	OPTIONS (requires alteration of the demo board, all needed components included).
1. Device	ADS7805P installed.	ADS7804P included for installation.
2. Input Amplifier	OPA671 bypassed.	Switching jumpers on J1 and J2 to "B" selects input amplifier. Apply ±15V to P1.
3. Offset Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometers included for installation. See Step-by-Step Basic Operations, step 3.
Gain Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometers included for installation. See Step-by-Step Basic Operations, step 3.
4. Convert Command	On-board 100kHz convert command generator connected to R/C.	Apply external convert command generator (≤100kHz) to P4 and switch J3 to "EXT".
5. Output Format	12/16-bit buffered full-parallel output (P6)	Full parallel or 8-bit byte reading output (P5).
6. Power Supplies	2-pin power block (P2) ready for +5V.	3-pin power block (P1) ready for ±15V (for use with breadboard and optional input amplifier).
NOTE: (1) Each of these steps is explained in detail in the Step-by-Step Basic Operations section.		

TABLE I. Quick Reference to Factory Settings and Other Options.

DEM-ADS7804/05

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FACTORY SETTINGS (CONT)

Hardware	Installed	Comments
P1	Yes	3-Pin Power Block
P2	Yes	2-Pin Power Block
P3	Yes	PCB Mount BNC Connector
P4	Yes	PCB Mount BNC Connector
P5	Yes	20 X 2 Header
P6	Yes	20 X 2 Shrouded Header
U1	Yes	28-Pin Socket for ADS7804P or ADS7805P
U2	Yes	8-Pin Socket for OPA671
J1-J3	Yes	3 x 1 Headers
J4	No	Refer to Step-by-Step Basic Operations, Step 4B.

FIGURE 2. Hardware Installed.

Jumpers for:	Setting	Comments
J1, J2	"A"	U2 (Input Amplifier Socket) bypassed
J3	"INT"	Crystal On-Board Convert Command Generator Selected (Outputs 100kHz to R/C)
P5	Pin 37 to 38	CS Tied LOW
P5	Pin 33 to 34	BYTE Tied LOW

FIGURE 3. Jumpers Installed.

FACTORY SETTINGS (CONT)

ICs	Installed	Comments
ADS7804P	No	Included in Package
ADS7805P	Yes	Plugged into 28-Pin Socket (U1)
OPA671	Yes	Plugged into 8-Pin Socket (U2)
U3	Yes	4-Bit Decade Counter
U4	Yes	Hex Schmit Inverters
U5, U6	Yes	8-Bit Latch
U7	Yes	1.000MHz Crystal Oscillator

FIGURE 4. ICs Installed.

Resistors	Installed	Comments
R2	No	576kΩ 1/4W 1%[1]
R3	No	33.2kΩ 1/4W 1%[1]
R5	No	49.9kΩ 1/4W 1%[1]
R1	Yes	33.2kΩ 1/4W 1%
R4	Yes	200Ω 1/4W 1%
R6-R8	Yes	4.99kΩ 1/4W 1%
R9	Yes	49.9Ω 1/4W 1%

Pots	Installed	Comments
RV1, RV2	No	50kΩ 1/4W 1%[1]

Capacitors	Installed	Comments
C1, C2, C5, C7-C11	Yes	0.1µF (50V)
C3, C4	Yes	2.2µF (25V)
C6	Yes	10µF (10V)

NOTE: (1) Included in Package.

FIGURE 5. Resistors and Capacitors Installed.

DEM-ADS7804/05

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STEP-BY-STEP BASIC OPERATIONS

STEP 1 — ADS7804P OR ADS7805P

A) To test the ADS7804P, install an ADS7804P in U1.

B) To test the ADS7805P, install an ADS7805P in U1.

Factory Setting: C3, C4, C5, C6 and 28-pin socket (U1) soldered to the board. ADS7805P plugged into U1.
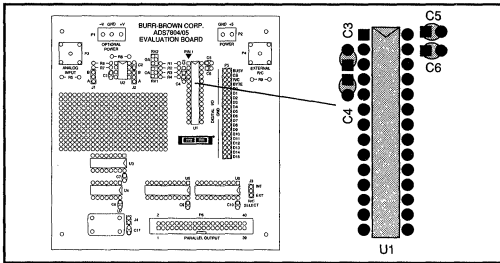
FIGURE 6. Factory Settings For Step 1.

Step 2 — On-Board Input Amplifier

To use the on-board input amplifier, jumpers J1 and J2 must be set to the "B" position, and P1 (Optional Power) must be supplied with ±15V. The factory setting of the amplifier yields an inverting gain of 2. Combinations of resistors R6, R7, and R8 will affect the gain of the amplifier as follows:

$$\text{GAIN} = -(R8)/(R6 \| R7)$$

NOTE: The on-board input amplifier may improve the quality of the signal reaching the ADS7804P or ADS7805P. This depends on the output characteristics of the signal generator.

Factory Setting: J1 and J2 set to "A", bypassing the amplifier, R6, R7, R8, C1, C2 and 8-pin socket (U2) soldered to the board. OPA671 plugged into U2.
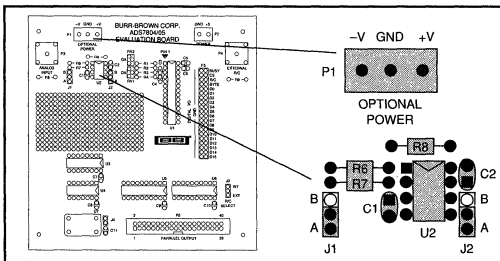
FIGURE 7. Factory Settings for Step 2.

Step 3 — Offset/Gain Adjust

Offset Adjust

A) To adjust offset, install RV1 (50kΩ) and R3 (33.2kΩ), ground the input, then adjust RV1. See Figure 8 for location of RV1 and R3.

Gain Adjust

B) To adjust gain, install RV2 (50kΩ) and R2 (576kΩ), then adjust RV2. Do this for +10V and –10V. See Figure 8.

NOTE: The offset directly affects the gain. Always trim offset first. For maximum precision, more than one iteration of these adjustments may be required.

Factory Setting: ±10V input range without offset/gain trim, R1 and R4 soldered to the board.
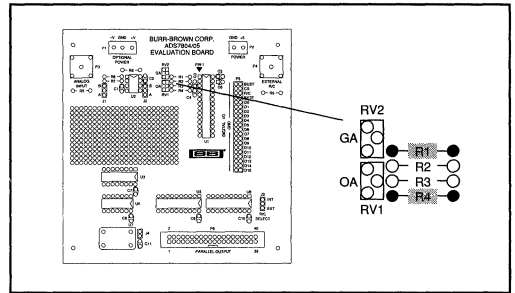
FIGURE 8. Factory Settings for Step 3.

Step 4 — Convert Command Generator

A) J3 set to "INT" selects the on-board convert command generator operating at 100kHz (divided down from 1MHz by U3).

B) J3 set to "EXT" selects an external convert command generator. Apply a negative-going pulse, 100ns in duration, to P4 (External Convert Command). This connector is terminated on the board with a 50Ω resistor (R9). Adjust the voltage of the generator for a 0V to 5V swing and the pulse rate to the desired frequency (≤100kHz). NOTE: When using an external convert command, the trace powering the on-board convert command generator can be cut to eliminate any noise contributions due to the oscillator. To reconnect, install a jumper at J4.

Factory Setting: J3 set to "INT", conversions synchronized to on-board convert command generator at 100kHz. P4, R9, U3, U7, C7 and C11 soldered to the board.
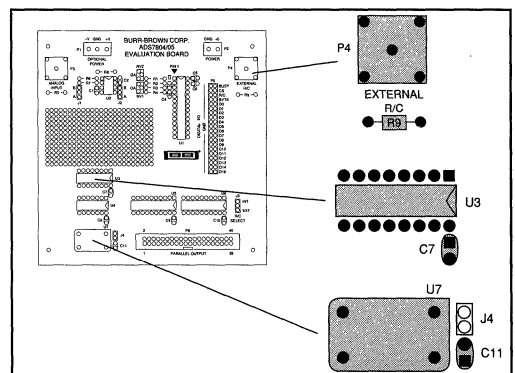
FIGURE 9. Factory Settings for Step 4.
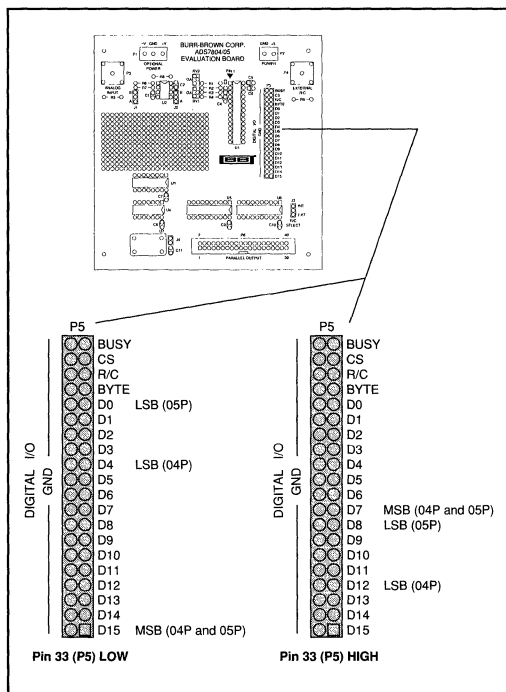
FIGURE 10. Location of MSBs and LSBs on P5.
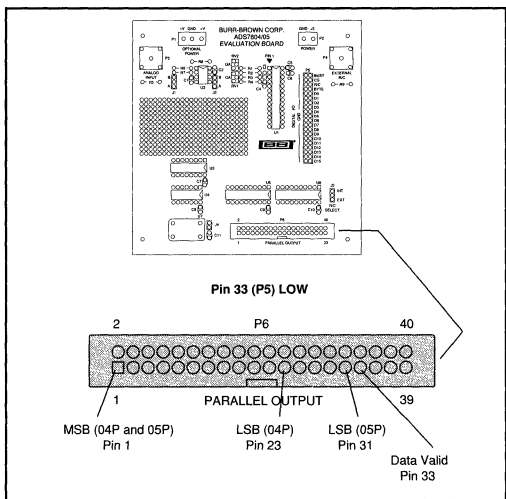
FIGURE 11. Location of MSBs and LSBs on P6.

Step 5 — Parallel or Byte-Reading Output

A) P5 outputs byte-reading and full parallel data — See Figure 10.

B) P6 outputs buffered full parallel data—See Figure 11.

A rising edge pulse will be output on pin 33 (Data Valid) of P6 signifying the end of a conversion and that data is valid. Data will be from the most recently completed conversion. Be sure to tie pin 33 of P5 to pin 34 of P5 with a jumper. This puts the MSB on pin 1 of P6.

Factory Setting: Pin 33 jumpered to pin 34 (P5), P5, P6, U4, U5, U6, C8, C9 and C10 soldered to the board (See Figures 10, 11, and 12).
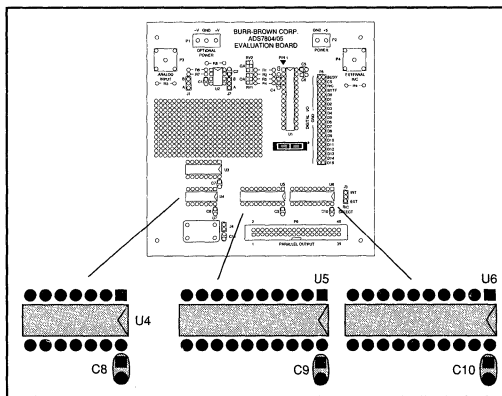
FIGURE 12. Factory Settings for Step 5.

Step 6 — Power Supplies

A) A 5V power supply connected to P2 (Power) is all that is required to operate the DEM-ADS7804/05C.

B) If the optional amplifier is used, P1 must be supplied with power (OPA671 requires at least ±15V for this application).

Factory Setting: P1 and P2 ready to be connected to the appropriate power supplies.

FIGURE 13. Factory Settings for Step 6.

DEM-ADS7804/05

A

FIGURE 14. DEM-ADS7804/05C Circuit Diagram.

A.16

PIN	ADS7804P FUNCTION	ADS7805P FUNCTION	PIN	ADS7804/05P FUNCTIONS
1	D11(MSB)	D15(MSB)	2	GND
3	D10	D14	4	GND
5	D9	D13	6	GND
7	D8	D12	8	GND
9	D7	D11	10	GND
11	D6	D10	12	GND
13	D5	D9	14	GND
15	D4	D8	16	GND
17	D3	D7	18	GND
19	D2	D6	20	GND
21	D1	D5	22	GND
23	D0 (LSB)	D4	24	GND
25	Data Zero	D3	26	GND
27	Data Zero	D2	28	GND
29	Data Zero	D1	30	GND
31	Data Zero	D0 (LSB)	32	GND
33	BYTE	BYTE	34	GND
35	R/C̄	R/C̄	36	GND
37	C̄S̄	C̄S̄	38	GND
39	B̄U̅S̄Ȳ	B̄U̅S̄Ȳ	40	GND

TABLE II. Pinout of the Digital I/O Connector (P5). Pin 33 tied to pin 34 on P5 (BYTE is LOW).

PIN	ADS7804P FUNCTION	ADS7805P FUNCTION	PIN	ADS7804/05P FUNCTIONS
1	D11(MSB)	D15(MSB)	2	GND
3	D10	D14	4	GND
5	D9	D13	6	GND
7	D8	D12	8	GND
9	D7	D11	10	GND
11	D6	D10	12	GND
13	D5	D9	14	GND
15	D4	D8	16	GND
17	D3	D7	18	GND
19	D2	D6	20	GND
21	D1	D5	22	GND
23	D0 (LSB)	D4	24	GND
25	Data Zero	D3	26	GND
27	Data Zero	D2	28	GND
29	Data Zero	D1	30	GND
31	Data Zero	D0 (LSB)	32	GND
33	BYTE	BYTE	34	GND
35	R/C̄	R/C̄	36	GND
37	C̄S̄	C̄S̄	38	GND
39	B̄U̅S̄Ȳ	B̄U̅S̄Ȳ	40	GND

TABLE III. Pinout of Buffered Output (P6). Pin 33 tied to pin 34 on P5 (BYTE is LOW).
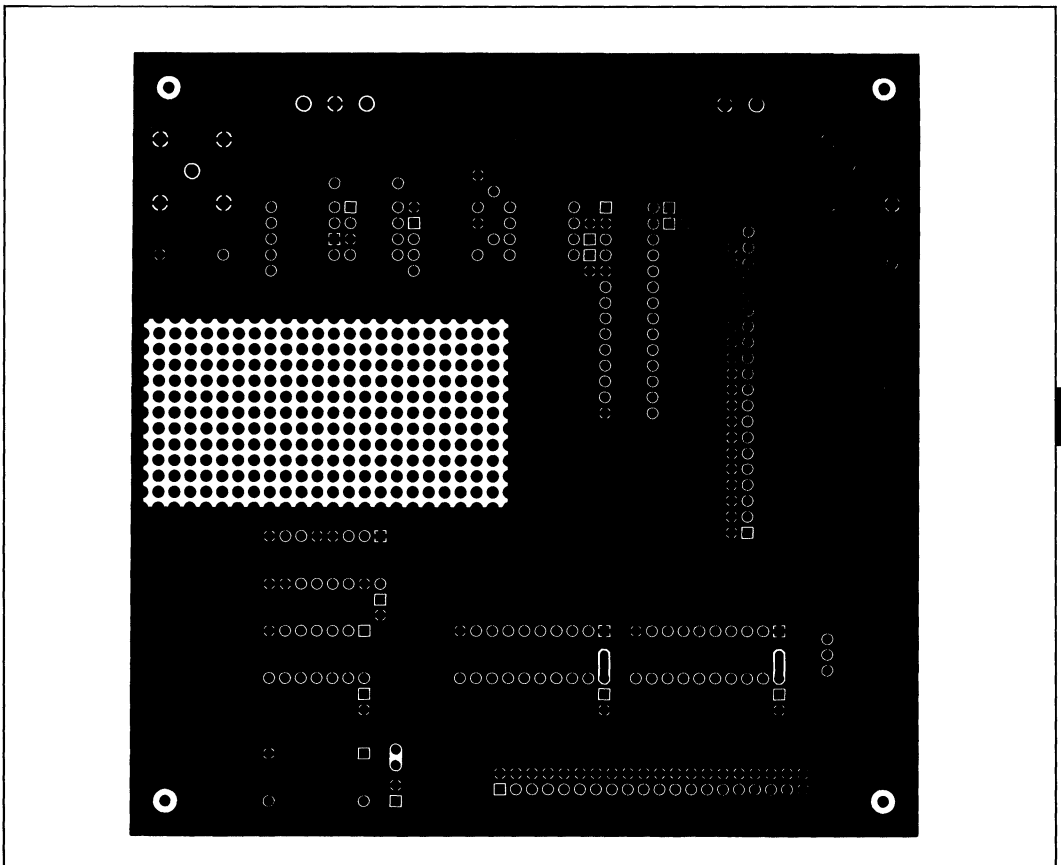
FIGURE 15. PCB Component Side (Ground Plane).

DEM-ADS7804/05

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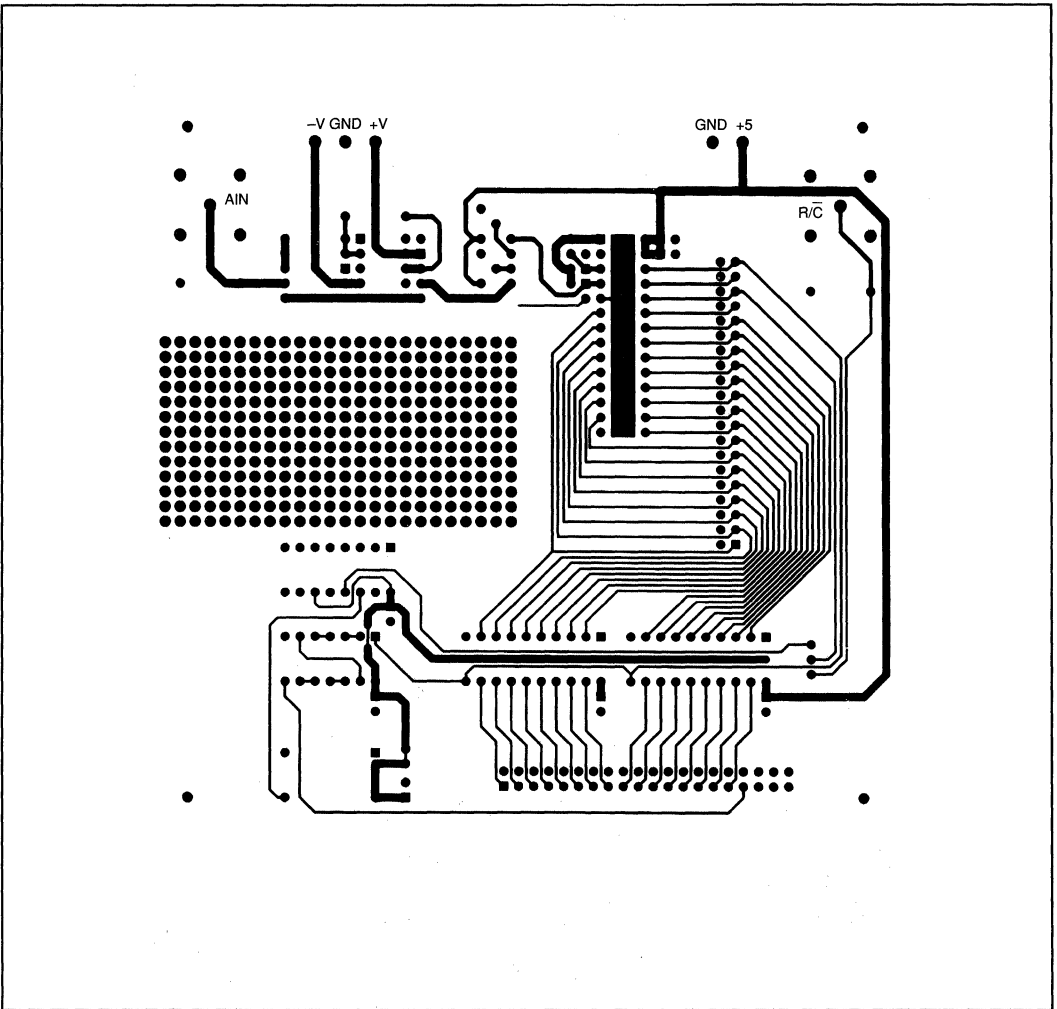
FIGURE 16. PCB Solder Side

INSTALLED COMPONENT LIST

REFERENCE	QUANTITY	PART NUMBER	DESCRIPTION	MANUFACTURER[1]
C1, C2, C5, C7-C11	8	SR205C104KAA	0.1µF 50V X 7R Ceramic Capacitor	Kemet
C3, C4	3	TAP225K025SCS	2.2µF 25V Tantalum Capacitor	AVX
C6	1	TAP106K010SCS	10µF 16V Tantalum Capacitor	AVX
J1-J3	3	NSH-3SB-S1-T	3 X 1 Header	Robinson Nugent
P1	1	ED500/3DS	3-pin Power Block	On-Shore Technology
P2	1	ED500/2DS	2-pin Power Block	On-Shore Technology
P3, P4	2	KC-79-274-M06	PCB Mount BNC Connector	Kings
P5	1	NSH-40DB-S1-T	20 X 2 Header	Robinson Nugent
P6	1	IDH-40LP-S3-TG	20 X 2 Shrouded Header	Robinson Nugent
R1	1	5043EM33K20F	33.2kΩ 1/4W 1% MF Resistor	Philips
R4	1	5043EM200R0F	200Ω 1/4W 1% MF Resistor	Philips
R6-R8	3	5043EM499K0F	4.99kΩ 1/4W 1% MF Resistor	Philips
R9	1	5043EM49R90F	49.9Ω 1/4W 1% MF Resistor	Philips
U1	1	ADS7805P	16-Bit Sampling A/D Converter	Burr-Brown
U2	1	OPA671	Op Amp	Burr-Brown
U3	1	74HC190	4-Bit Decade Counter	T.I.
U4	1	74HC14	Hex Schmitt Inverters	T.I.
U5, U6	2	74HC574	8-Bit Latch	T.I.
U7	1	DOC-2-1.000MHz	1.000MHz Crystal Oscillator	Daiwa
	4	MSB-2366-G-C-STP	0.1 Centerline Shunt	McKenzie
U1	1	DIP-328011B	28-Pin Socket (0.3")	McKenzie
U2	1	DIP-308011B	8-Pin Socket	McKenzie

PACKING LIST

REFERENCE	QUANTITY	ITEM	DESCRIPTION	MANUFACTURER[1]
Demo Board	1	DEM-ADS7804/05C	Fully assembled printed circuit board with ADS7805P installed.	Burr-Brown
U1	1	ADS7804P	12-bit 10µs Sampling CMOS A/D Converter	Burr-Brown
RV1,RV2	2	RJ26FW503	50kΩ 1/4" trimmer resistors	Bourns
R2	1	5043EM576kOF	576kΩ 1/4W 1% MF resistor	Phillips
R3	1	5043EM33KOF	33.2kΩ 1/4W 1% MF resistor	Phillips
ADS7806P	1	PDS-1156A	ADS7804 Product Data Sheet	Burr-Brown
ADS7807P	1	PDS-1157A	ADS7805 Product Data Sheet	Burr-Brown
Demo Board Info.	1	LI-448	DEM-ADS7804/05C Manual	Burr-Brown

NOTE: (1) For reference only. Equivalent components may be used.

DEM-ADS7804/05

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DEM-ADS7806/07C
EVALUATION FIXTURE
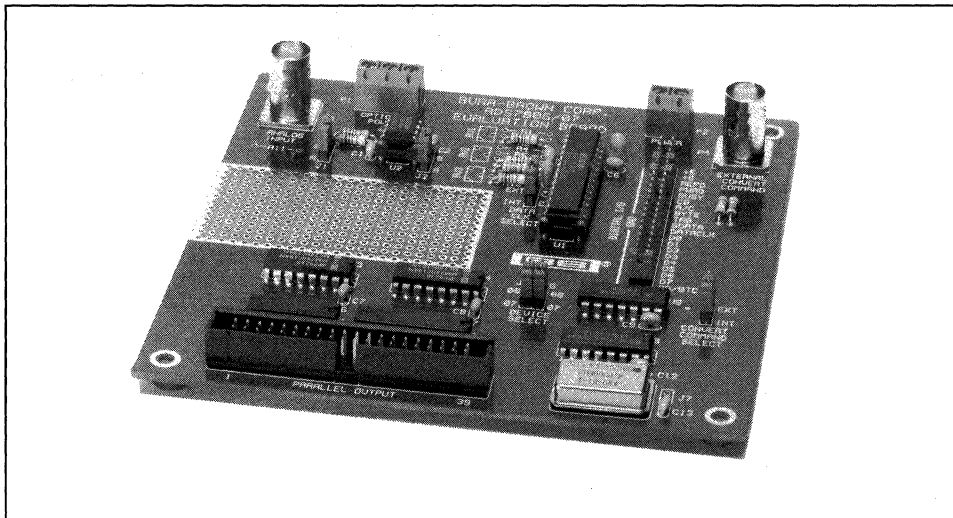
FEATURES

● **40kHz 12-BIT ADS7806P AND 16-BIT ADS7807P INCLUDED**

● **16-BIT BUFFERED PARALLEL OUTPUT**

● **CONNECTOR FOR ALL DIGITAL I/O PINS**

● **CRYSTAL OSCILLATOR BASED 40kHZ CONVERT COMMAND GENERATOR**

● **EXTERNAL CONVERT COMMAND CONNECTOR**

● **PROTOTYPE AREA**

APPLICATIONS

● **EVALUATE ADS7806P AND ADS7807P PERFORMANCE**

● **BREADBOARD COMPLETE ANALOG SYSTEM**

● **EVALUATE SIMPLE TWO LAYER PCB LAYOUT**

● **INCOMING INSPECTION TEST FIXTURE**

DESCRIPTION

The DEM-ADS7806/07C Evaluation Fixture is a fully assembled printed circuit board intended to evaluate the ADS7806P and ADS7807P. This device incorporates an analog input amplifier (with provisions to bypass this amplifier), a parallel digital output buffer, a crystal oscillator based 40kHz convert command generator, an external convert command connector, and a 2.3" x 1.2" breadboard area. The DEM-ADS7806/07C achieves full converter performance on a two layer board.

This fixture requires only a single +5V power supply. An optional bipolar power supply connector is provided for the input buffer and breadboarding.

LI-447A

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HOW TO USE THIS MANUAL

A table and diagrams are included in the "Factory Settings" section showing how the board is configured from the factory. A listing of other components, which are shipped with the board, is also included.

The Step-by-Step Basic Operations section describes all of the options. At the end of each step, a figure illustrates factory settings. Items installed are highlighted in these figures.

For further details on the OPA604, ADS7806P, ADS7807P or any other device on the DEM-ADS7806/07C, refer to the product data sheet for that device.

DEM-ADS7806/07

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FIGURE 1. PCB Legend.

FACTORY SETTINGS

With a +5V supply connected to P2, the DEM-ADS7806/07C starts converting at 40kHz and is set for an input range of ±10V. Byte-reading parallel or serial output can be read on P5, and buffered full-parallel output on P6. The following is a listing of "factory settings".

MAKE SELECTION FOR EACH STEP[1]	FACTORY SETTINGS	OTHER OPTIONS (requires alteration of the demo board, all needed components included.)
1. Device	ADS7807P installed.	ADS7806P included for installation. Switch jumper J4 and J5 to "06".
2. Input Amplifier	OPA604 bypassed.	Switching jumpers on J1 and J2 to "B" selects input amplifier. Apply ±15V to P1.
3. Input Range	±10V	0V-5V and 0V-4V.
Offset Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometer included for installation. See Step-by-Step Basic Operations, Step 3.
Gain Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometer included for installation, See Step-by-Step Basic Operations, Step 3.
4. Convert Command	On-board 40kHz convert command generator connected to R/C.	Apply external convert command generator, (≤40kHz) to P4 and switch J6 to "EXT".
5. Binary Format	Binary Two's Complement	Removing the jumper from pin 1 to pin 2 of P5 selects Straight Binary format.
6. Output Format	12/16-bit Buffered Full Parallel Output (P6)	12/16-bit Serial Output (P5) 8-bit Byte-Reading Output (P5)
7. Power Supplies	2-pin Power Block (P2) ready for +5V.	3-pin Power Block (P1) ready for ±15V (for use with breadboard and optional input amplifier).
NOTE: (1) Each of these steps is explained in the Step-by-Step Basic Operations Section.		

TABLE I. Quick Reference to Factory Settings and Other Options.

FACTORY SETTINGS (CONT)

Hardware	Installed	Comments
P1	Yes	3-pin Power Block
P2	Yes	2-pin Power Block
P3	Yes	PCB Mount BNC Connector
P4	Yes	PCB Mount BNC Connector
P5	Yes	20 X 2 Header
P6	Yes	20 X 2 Shrouded Header
U1	Yes	28-pin Socket for ADS7806P or ADS7807P
U2	Yes	8-pin Socket for OPA604
J1-6	Yes	3x1 Headers
J7	No	Refer to Step-by-Step Basic Operations, Step 4B

FIGURE 2. Hardware Installed.

Jumpers for:	Setting	Comments
J1, J2	"A"	U2 (Input Amplifier Socket) bypassed
J3	"INT"	Internal Data Clock Selected
J4, J5	"07"	Set for ADS7807P Operation
J6	"INT"	Crystal On-Board Convert Command Generator Selected (Outputs 40kHz to R/C̄)
P5	Pin 33 to 34	PWRD Tied LOW
P5	Pin 29 to 30	C̄S̄ Tied LOW
P5	Pin 25 to 26	BYTE Tied LOW
P5	Pin 1 to 2	SB/B̄T̄C̄ Tied LOW

FIGURE 3. Jumpers Installed.

DEM-ADS7806/07

A

FACTORY SETTINGS (CONT)

ICs	Installed	Comments
ADS7806P	No	Included in Package
ADS7807P	Yes	Plugged into 28-pin Socket (U1)
OPA604	Yes	Plugged into 8-pin Socket (U2)
U3, U4	Yes	4-bit Shift Register
U5	Yes	Hex Schmit Inverter
U6	Yes	8-bit Shift Register
U7	Yes	8-bit Latch
U8	Yes	Dual Decade Counter
U9	Yes	4.000MHz Crystal Oscillator

FIGURE 4. ICs Installed.

Resistors	Installed	Comments
R1	No	200Ω 1/4W 1%[1]
R5	No	100Ω 1/4W 1%[1]
R2, R4, R6	No	33.2kΩ 1/4W 1%[1]
R9	No	1MΩ 1/4W 1%[1]
R11	No	49.9Ω 1/4W 1%[1]
R3	Yes	200Ω 1/4W 1%
R7	Yes	100Ω 1/4W 1%
R8	Yes	66.5kΩ 1/4W 1%
R10, R12-15,R17	Yes	10kΩ 1/4W 1%
R16	Yes	49.9Ω 1/4W 1%

Potentiometers	Installed	Comments
RV1 - RV3	No	50kΩ 1/4"[1]

Capacitors	Installed	Comments
C1, C2, C6 - 13	Yes	0.1µF (50V)
C3, C4	Yes	2.2µF (25V)
C5	Yes	10µF (10V)

NOTE: (1) Included in Package.

FIGURE 5. Resistors and Capacitors Installed.

STEP-BY-STEP
BASIC OPERATIONS

Step 1 — ADS7806P or ADS7807P

A) To test the ADS7806P, set jumpers J4 and J5 to the "06" position and install an ADS7806P into U1.

B) To test the ADS7807P, set jumpers J4 and J5 to the "07" position and install an ADS7807P into U1.

Factory Setting: J4 and J5 set to "07", C3, C4, C5, C6 and 28-pin socket (U1) soldered to the board. ADS7807P plugged into socket (U1).
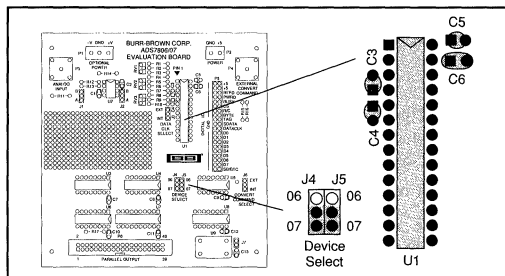
FIGURE 6. Factory Settings for Step 1.

Step 2 — On-Board Input Amplifier

To use the on-board input amplifier, jumpers J1 and J2 must be set to the "B" position, and P1 (Optional Power) must be supplied with ±15V. The factory setting of the amplifier yields an inverting gain of two. Combinations of resistors R12, R13, and R14 will affect the gain of the amplifier as follows:

$$\text{Gain} = - (R14)/(R12 \| R13)$$

NOTE: The on-board input amplifier may improve the quality of the signal reaching the ADS7806P or ADS7807P. This depends on the output characteristics of the signal generator.

Factory Setting: J1 and J2 set to "A", bypassing the amplifier, R12, R13, R14, C1, C2 and 8-pin socket (U2) soldered to the board. OPA604 plugged into socket (U2).
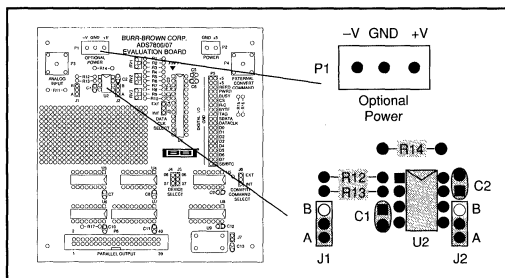
FIGURE 7. Factory Settings for Step 2.

Step 3 — Input Range, Offset/Gain Adjust

Input Range

A) Using Table II, choose the input voltage range for your application. Note that using the optional input amplifier will directly affect the input voltage seen at the converter input (factory setting for the gain of the amplifier is –2V/V).
Install the proper resistors.

Offset Adjust

B) To adjust offset, install the proper potentiometer and resistors, ground the input, then adjust the pot accordingly (see Table II and Figure 8).

Gain Adjust

C) To adjust gain, install the proper potentiometer and resistors, then adjust the pot accordingly. Do this for +FS and –FS (see Table II and Figure 8).

NOTE: Offset directly affects the gain. Always trim offset first. For maximum precision, more than one iteration of those adjustments may be required.

Ref Des. Value	FOR ±10V INPUT RANGE		FOR 0V TO 5V INPUT RANGE		FOR 0V TO 4V INPUT RANGE	
	With Trim	Without Trim	With Trim	Without Trim	With Trim	Without Trim
R1 (200Ω)			Install	Install		
R2 (33.2kΩ)			Install(1)		Install(1)	
R3 (200Ω)	Install	Install			Install	Install
R4 (33.2kΩ)				Install		Install
R5 (100Ω)			Install	Install	Install	Install
R6 (33.2kΩ)	Install(1)					
R7(100Ω)	Install	Install				
R8 (66.5kΩ)		Install				
R9 (1MΩ)	Install(2)		Install(2)		Install(2)	
RV1 (50kΩ)			Install(1)		Install(1)	
RV2(50kΩ)	Install(1)					
RV3 (50kΩ)	Install(2)		Install(2)		Install(2)	

NOTES: (1) Components associated with offset trim. (2) Components associated with gain trim.

TABLE II. Input Ranges With and Without Trim.

Factory Setting: ±10V input range without offset/gain trim, R3, R7 and R8 soldered into board.

Note: R10 soldered to the board but not involved with input range. R10 functions as a pull-up resistor for SB/BTC pin.
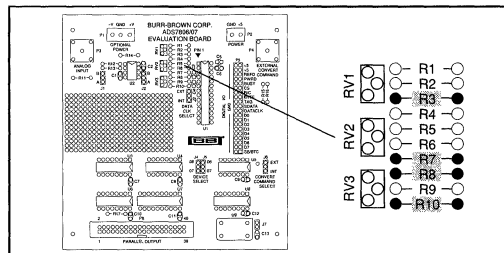

FIGURE 8. Factory Setting for Step 3.

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Step 4 — On-Board or External Convert Command Generator?

A) J6 set to "INT" selects the on-board convert command generator operating at 40kHz (divided down from 4MHz by U8).

B) J6 set to "EXT" selects an external convert command generator. Apply a negative-going pulse, 100ns in duration, to P4 (External Convert Command). This connector is terminated on the board with a 50Ω resistor (R16). Adjust the voltage of the generator for a 0V to 5V swing and the pulse rate to the desired frequency (≤ 40kHz).

NOTE: When using an external convert command, the trace powering the on-board convert command generator can be cut to eliminate any noise contributions due to the oscillator. To reconnect the power, install a jumper at J7.

Factory Setting: J6 set to "INT", conversions synchronized to on-board convert command generator at 40kHz. P4, R15, R16, C12, C13, U8 and U9 soldered to the board.

NOTE: R15 installed but not involved with the internal/external convert command.
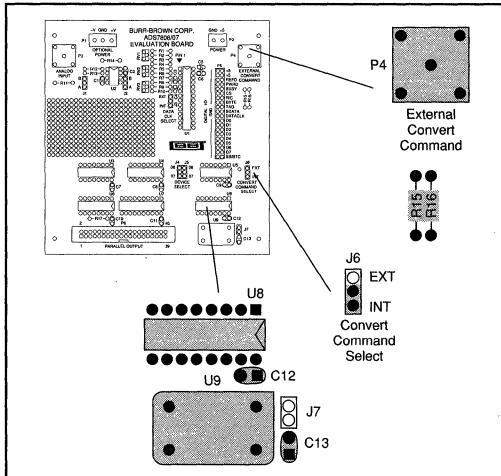
FIGURE 9. Factory Settings for Step 4.

Step 5 — SB or BTC Format?

A) To get data in Binary Two's Complement format, place a jumper from pin 1 to pin 2 on P5.

B) To get data in Straight Binary format, remove the jumper from pin 1 to pin 2 on P5.

Factory Setting: Pin 1 jumpered to pin 2 on P5, output format is Binary Two's Complement.

NOTE: Pins 25, 29 and 33 also have jumpers but are not involved in the output format.
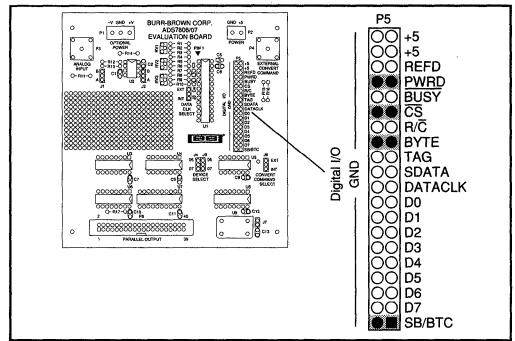
FIGURE 10. Factory Settings for Step 5.

Step 6 — Parallel or Serial Output?

Serial Output

A) To use the internal data clock, set J3 to "INT". Data from the last conversion will be clocked out on pin 21 of P5 at the start of a conversion synchronized to:

- 12 clock pulses output on pin 19 of P5 (ADS7806P)
- 16 clock pulses output on pin 19 of P5 (ADS7807P)

Data is valid on both the rising and falling edges of the internal data clock. Using the internal clock is preferred to optimize system performance.

B) To use an external data clock, set J3 to "EXT" and apply an external clock to pin 19 of P5. Data will be output on pin 21 of P5 synchronized to:

- 12 clock pulses input on pin 19 of P5 (ADS7806P)
- 16 clock pulses input on pin 19 of P5 (ADS7807P)

The frequency of the external clock must not exceed 10MHz. A duty cycle of 40% to 60% is suggested. BUSY (pin 31 of P5) can be used to latch the data. The data will always be from the most recently completed conversion.

Parallel Output

C) P5 outputs byte-reading parallel data on pins 3, 5 ...15, 17. Refer to the PDS of the ADS7806P and ADS7807P for specific details on the MSB and LSB locations. If pin 25 of P5 is:

- LOW, the 8 MSBs will be present on the output
- HIGH, the 8 LSBs will be present on the output

Data will be from the most recently completed conversion.

D) P6 outputs 16-bit buffered parallel data converted from serial to parallel via U3, U4, U6, and U7. Data can be acquired on pins:

- 1 (MSB), 3 ... 21, 23 (LSB) with pins 25, 27, 29 and 31 outputting LOWs for the ADS7806P
- 1 (MSB), 3 ... 29, 31 (LSB) for the ADS7807P

A rising edge pulse will be output on pin 33 (DATA VALID) of P6 signifying the end of a conversion and that data is valid. Data will be from the most recently completed conversion. Be sure pin 25 of P5 is tied to pin 26 of P5 with a jumper. This puts the MSB on pin 1 of P6.

Factory Setting: J3 set to "INT". Pin 25 jumpered to pin 26 on P5. P5, P6, U3, U4, U6, and U7 soldered to the board.

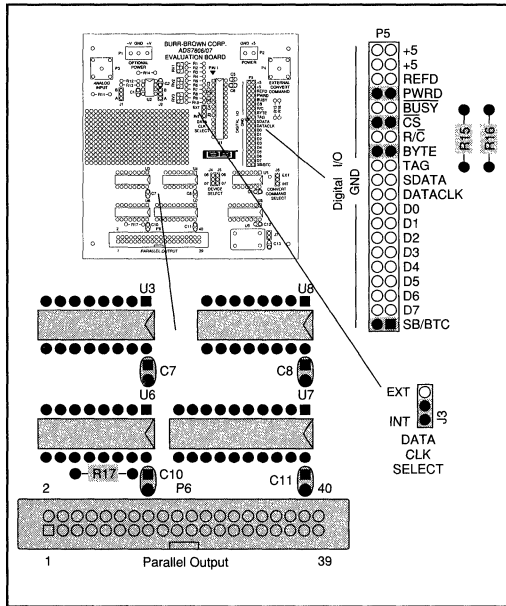NOTE: Pins 1, 29, and 33 of P5 have jumpers but are not involved with the output format.

FIGURE 11. Factory Settings for Step 6.

Step 7 — Power Supplies?

A) A 5V power supply connected to P2 (POWER), is all that is required to operate the DEM-ADS7806/07C.

B) If the optional amplifier is used, P1 must be supplied with power (OPA604 requires at least ±15V for this application).

Factory Setting: P1 and P2 connectors soldered to the board and ready for connection to the appropriate power supplies.
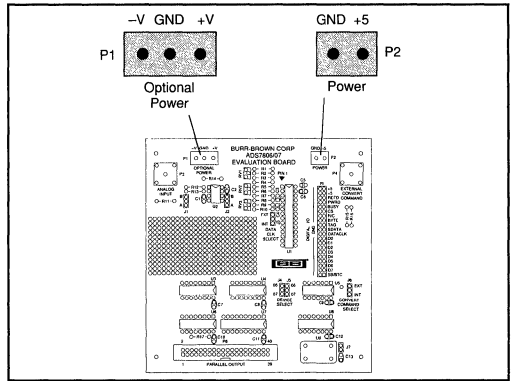
FIGURE 12. Factory Settings for Step 7.

OTHER OPTIONS

The following pins on P5 serve optional functions of the ADS7806P or ADS7807P:

REFD	pin 35
PWRD	pin 33
$\overline{CS}$	pin 29
TAG	pin 23

Refer to ADS7806P and ADS7807P product data sheets for the description of these options.

Factory Setting: REFD connected to pull-down resistor R15. PWRD tied LOW with jumper from pin 33 to pin 34. $\overline{CS}$ tied LOW with jumper from pin 29 to pin 30. TAG, no jumper.

NOTE: R15 is the pull-down resistor for REFD. R16 is not involved with these functions.

FIGURE 13. Factory Settings for Other Options.

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For Immediate Assistance, Contact Your Local Salesperson

FIGURE 14. ADS7806/07 Circuit Diagram.

PIN	ADS7806/07P FUNCTION	PIN	ADS7806/07P FUNCTION
1	SB/$\overline{BTC}$	2	GND
3	D7	4	GND
5	D6	6	GND
7	D5	8	GND
9	D4	10	GND
11	D3	12	GND
13	D2	14	GND
15	D1	16	GND
17	D0	18	GND
19	DATACLK	20	GND
21	SDATA	22	GND
23	TAG	24	GND
25	BYTE	26	GND
27	R/$\overline{C}$	28	GND
29	$\overline{CS}$	30	GND
31	$\overline{BUSY}$	32	GND
33	PWRD	34	GND
35	REFD	36	GND
37	+5V	38	GND
39	+5V	40	GND

TABLE III. Pinout of the Digital I/O Connectors (P5) Pin 25 Tied to pin 26 of P5 (BYTE is LOW).

PIN	ADS7806P FUNCTION	ADS7807P FUNCTION	PIN	ADS7806/07P FUNCTIONS
1	Bit 1 (MSB)	Bit 1 (MSB)	2	GND
3	Bit 2	Bit 2	4	GND
5	Bit 3	Bit 3	6	GND
7	Bit 4	Bit 4	8	GND
9	Bit 5	Bit 5	10	GND
11	Bit 6	Bit 6	12	GND
13	Bit 7	Bit 7	14	GND
15	Bit 8	Bit 8	16	GND
17	Bit 9	Bit 9	18	GND
19	Bit 10	Bit 10	20	GND
21	Bit 11	Bit 11	22	GND
23	Bit 12(LSB)	Bit 12	24	GND
25	Tag 1[1]	Bit 13	26	GND
27	Tag 2[1]	Bit 14	28	GND
29	Tag 3[1]	Bit 15	30	GND
31	Tag 4[1]	Bit 16 (LSB)	32	GND
33	DATA VALID	DATA VALID	34	GND
35	NC	NC	36	GND
37	NC	NC	38	GND
39	GND	GND	40	GND

NOTE: (1) Tag data will appear when clocking out more than 12 bits of data for the ADS7806P using an external data clock. Refer to the product data sheet.

TABLE IV. Pinout of the Buffered Parallel Output. Pin 25 Tied to pin 26 of P5 (BYTE is LOW).

FIGURE 15. PCB Component Side.

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FIGURE 16. PCB Solder Side.

INSTALLED COMPONENT LIST

REFERENCE	QUANTITY	PART NUMBER	DESCRIPTION	MANUFACTURER[1]
C1, C2, C6-13	10	SR205C104KAA	0.1µF 50VX7R Ceramic Capacitor	AVX
C3, C4	2	TAP225K025SCS	2.2µF 25V Tantalum Capacitor	AVX
C5	1	TAP106K010SCS	10µF 10V Tantalum Capacitor	AVX
J1-J6	6	NSH-3SB-S1-T	3 X 1 Header	Robinson Nugent
P1	1	ED500/3DS	3-pin Power Block	On-Shore Technology
P2	1	ED500/2DS	2-pin Power Block	On-Shore Technology
P3, P4	2	KC-79-274-M06	PCB Mount BNC Connector	Kings
P5	1	NSH-40DB-S1-T	20 X 2 Header	Robinson Nugent
P6	1	IDH-40LP-S3-TG	20 X 2 Shrouded Header	Robinson Nugent
R3	2	5063JD200R0F	200Ω 1/4W 1% MF Resistor	Philips
R10, R12-15, R17	6	5063JD10K00F	10kΩ 1/4W 1% MF Resistor	Philips
R16	1	5063JD49R90F	49.9Ω 1/4W 1% MF Resistor	Philips
R7	1	5063JD100R0F	100Ω 1/4W 1% MF Resistor	Philips
R8	1	5063JD66K50F	66.5kΩ 1/4W 1% MF Resistor	Philips
U1	1	ADS7807P	16-Bit Sampling A/D	Burr-Brown
U2	1	OPA604	Op Amp DIP	Burr-Brown
U3, U4	2	74HC194	4-Bit Shift Register	T.I.
U5	1	74HC14	Hex Schmit Inverters	T.I.
U6	1	74HC594	8-Bit Shift Register	T.I.
U7	1	74HC574	8-Bit Latch DIP	T.I.
U8	1	74HC390	Dual Decade Counter	T.I.
U9	1	F1100E 4.000MHz	4.000MHz Crystal Oscillator	Fox
	7	MSB-2366-G-C-STP	0.1 Center Line Shunt	McKenzie
U1	1	DIP-328011B	28-Pin Socket (0.3")	McKenzie
U2	1	DIP-308011B	8-Pin Socket	Mckenzie

NOTE: (1) For reference only. Equivalent components may be used.

PACKING LIST

REFERENCE	QUANTITY	ITEM	DESCRIPTION	MANUFACTURER[1]
Demo Board	1	DEM-ADS7806/07C	Fully assembled printed circuit board with ADS7807P installed	Burr-Brown
U1	1	ADS7806P	12-bit 25µs Sampling CMOS A/D Converter	Burr-Brown
RV1-RV3	2	RJ26FW503	50kΩ 1.4" trimmer resistors (for gain and offset adjust)	Bourns
R1	1	5063JD200ROF	200Ω 1/4W 1% MF resistor	Phillips
R2 R4, R6	3	506JD33k2OF	33.2kΩ 1/4W 1% MF resistor	Phillips
R5	1	5063JD100ROF	100Ω 1/4W 1% MF resistor	Phillips
R9	1	5063JD1M000F	1MΩ 1/4W 1% MF resistor	Phillips
R11	1	506JD49R9OF	49.9Ω 1/4W 1% MF resistor	Phillips
ADS7807P	1	PDS-1158B	ADS7806P Product Data Sheet	Burr-Brown
ADS7806P	1	PDS-1159B	ADS7807P Product Data Sheet	Burr-Brown
Demo Board Info	1	LI-447	DEM-ADS7806/07C Manual	Burr-Brown

NOTE: (1) For reference only. Equivalent components may be used.
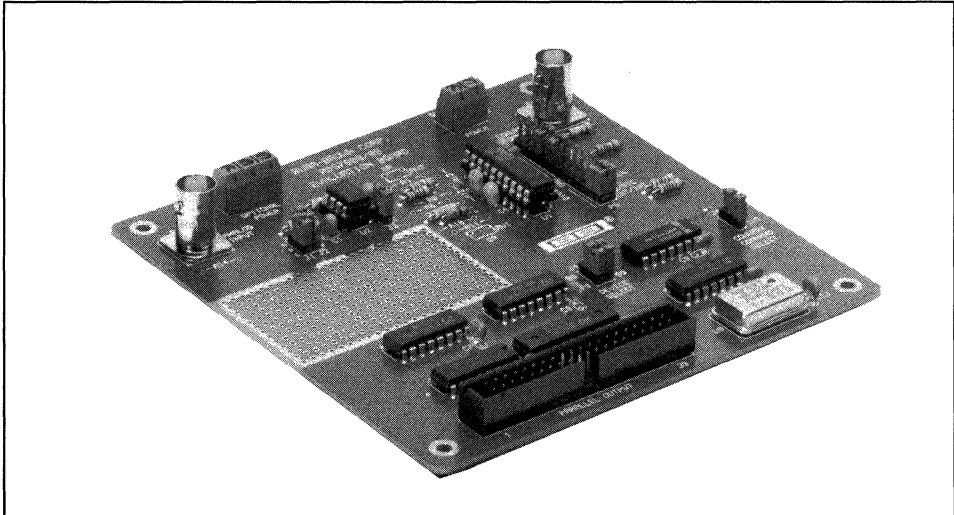
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DEM-ADS7808/09C
EVALUATION FIXTURE

FEATURES

- **100kHz 12-BIT ADS7808P AND 16-BIT ADS7809P INCLUDED**
- **16-BIT BUFFERED PARALLEL OUTPUT**
- **CONNECTOR FOR ALL DIGITAL I/O PINS**
- **CRYSTAL OSCILLATOR BASED 100kHz CONVERT COMMAND GENERATOR**
- **EXTERNAL CONVERT COMMAND CONNECTOR**
- **PROTOTYPE AREA**

APPLICATIONS

- **EVALUATE ADS7808P AND ADS7809P PERFORMANCE**
- **BREADBOARD COMPLETE ANALOG SYSTEM**
- **EVALUATE SIMPLE TWO LAYER PCB LAYOUT**
- **INCOMING INSPECTION TEST FIXTURE**

DESCRIPTION

The DEM-ADS7808/09C Evaluation Fixture is a fully assembled printed circuit board intended to evaluate the ADS7808P and ADS7809P. This device incorporates an analog input amplifier (with provisions to bypass this amplifier), a parallel digital output buffer, a crystal oscillator based 100kHz convert command generator, an external convert command connector, and a 2.3" x 1.2" breadboard area. The DEM-ADS7808/09C achieves full converter performance on a two layer board.

This fixture requires only a single +5V power supply. An optional bipolar power supply connector is provided for the input amplifier and breadboarding.

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HOW TO USE THIS MANUAL

A table and diagrams are included in the "Factory Settings" section showing how the board is configured from the factory. A listing of other components, which are shipped with the board, is also included.

The Step-by-Step Basic Operations section describes all of the options. At the end of each step, a figure illustrates factory settings. Items installed are highlighted in these figures.

For further details on the OPA671, ADS7808P, ADS7809P or any other device on the DEM-ADS7808/09C, refer to the product data sheet for that device.

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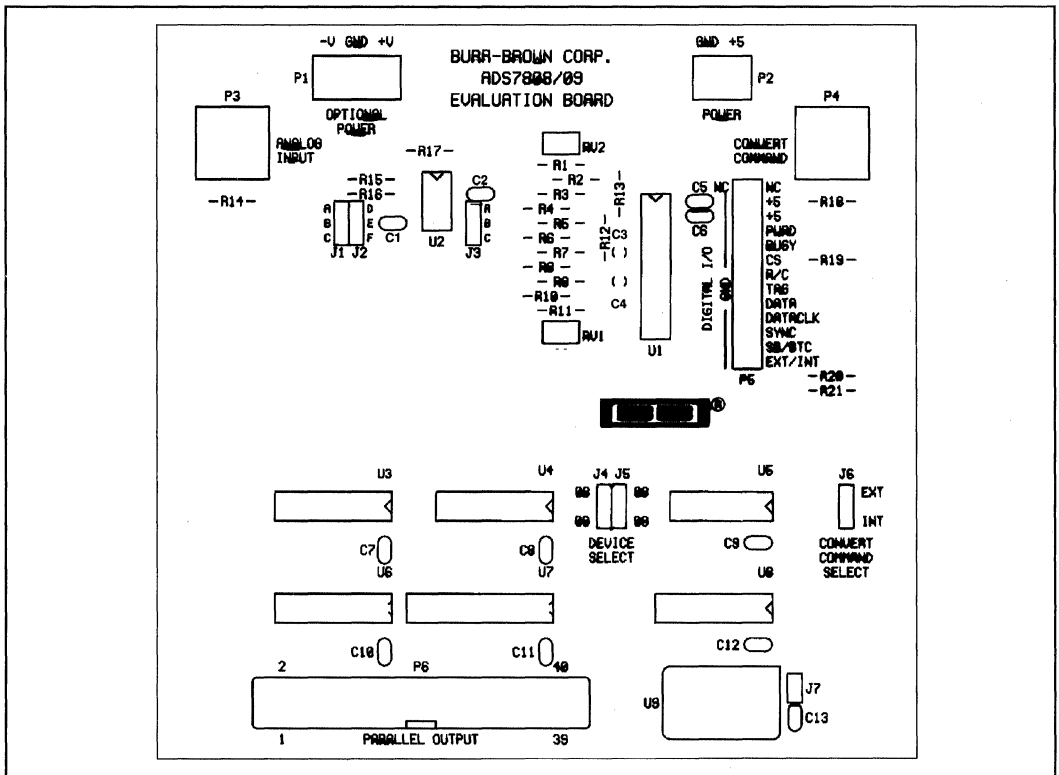
FIGURE 1. PCB Legend.

FACTORY SETTINGS

With a +5V supply connected to P2, the DEM-ADS7808/09C starts converting at 100kHz and is set for an input range of ±10V. Serial output can be read on P5, and buffered full-parallel output on P6. The following is a listing of "factory settings".

MAKE SELECTION FOR EACH STEP[1]	FACTORY SETTINGS	OTHER OPTIONS (requires alteration of the demo board, all needed components included.)
1. Device	ADS7809P installed.	ADS7808P included for installation. Switch jumper J4 and J5 to "08".
2. Input Amplifier	OPA671 bypassed.	Refer to step 2 for op amp configurations. Apply ±15V to P1.
3. Input Range	±10V	±5V, ±3.33V, 0-10V, 0-5V, 0-4V.
Offset Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometer included for installation. See Step-by-Step Basic Operations, Step 3.
Gain Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometer included for installation, See Step-by-Step Basic Operations, Step 3.
4. Convert Command	On-board 100kHz convert command generator connected to R/$\overline{C}$.	Apply external convert command generator, (≤100kHz) to P4 and switch J6 to "EXT".
5. Binary Format	Binary Two's Complement	Removing the SB/BTC jumper from P5 selects Straight Binary format.
6. Output Format	12/16-bit Buffered Full Parallel Output (P6)	12/16-bit Serial Output (P5)
7. Power Supplies	2-pin Power Block (P2) ready for +5V.	3-pin Power Block (P1) ready for ±15V (for use with breadboard and optional input amplifier).

NOTE: (1) Each of these steps is explained in the Step-by-Step Basic Operations Section.

TABLE I. Quick Reference to Factory Settings and Other Options.
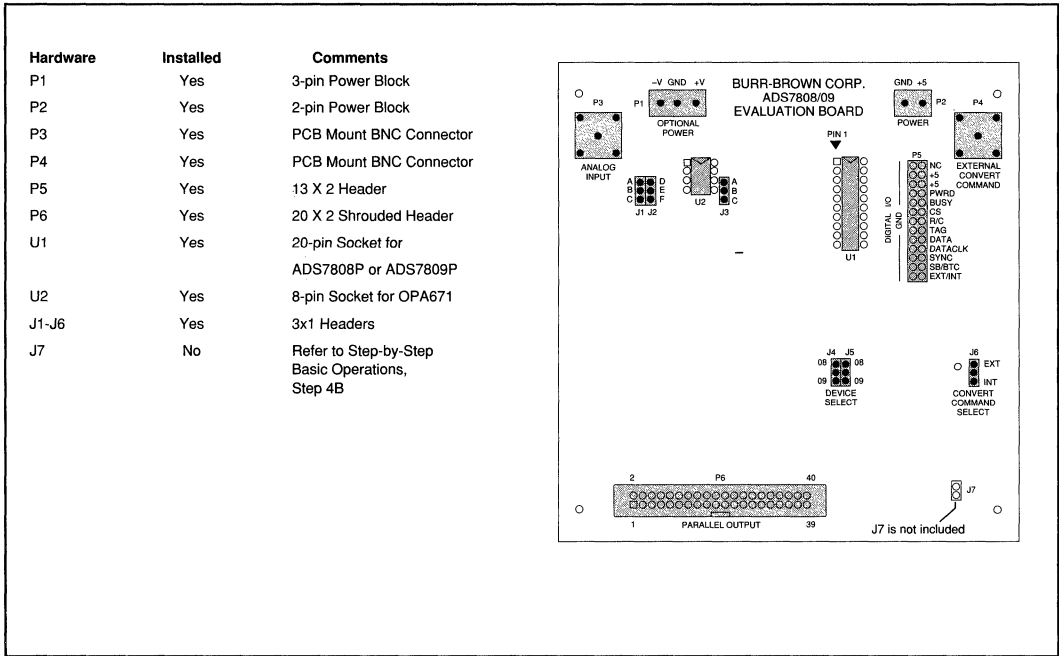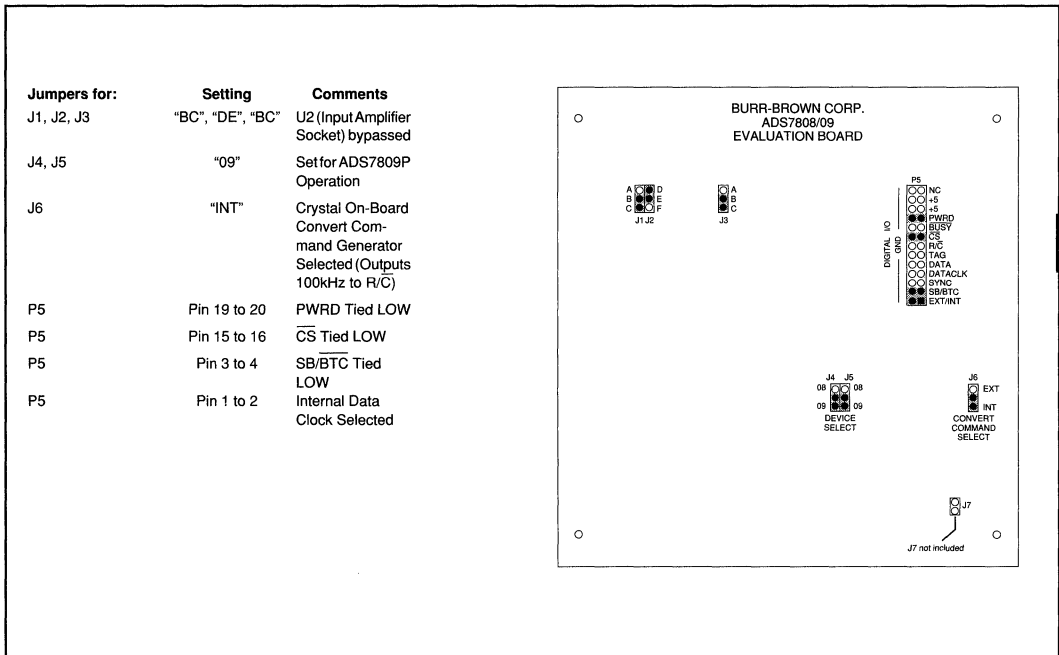
FACTORY SETTINGS (CONT)

Hardware	Installed	Comments
P1	Yes	3-pin Power Block
P2	Yes	2-pin Power Block
P3	Yes	PCB Mount BNC Connector
P4	Yes	PCB Mount BNC Connector
P5	Yes	13 X 2 Header
P6	Yes	20 X 2 Shrouded Header
U1	Yes	20-pin Socket for ADS7808P or ADS7809P
U2	Yes	8-pin Socket for OPA671
J1-J6	Yes	3x1 Headers
J7	No	Refer to Step-by-Step Basic Operations, Step 4B

FIGURE 2. Hardware Installed.

Jumpers for:	Setting	Comments
J1, J2, J3	"BC", "DE", "BC"	U2 (Input Amplifier Socket) bypassed
J4, J5	"09"	Set for ADS7809P Operation
J6	"INT"	Crystal On-Board Convert Command Generator Selected (Outputs 100kHz to R/C̄)
P5	Pin 19 to 20	PWRD Tied LOW
P5	Pin 15 to 16	C̄S̄ Tied LOW
P5	Pin 3 to 4	SB/BTC Tied LOW
P5	Pin 1 to 2	Internal Data Clock Selected

FIGURE 3. Jumpers Installed.

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FACTORY SETTINGS (CONT)

ICs	Installed	Comments
ADS7808P	No	Included in Package
ADS7809P	Yes	Plugged into 20-pin Socket (U1)
OPA671	Yes	Plugged into 8-pin Socket (U2)
U3, U4	Yes	4-bit Shift Register
U5	Yes	Hex Schmit Inverter
U6	Yes	8-bit Shift Register
U7	Yes	8-bit Latch
U8	Yes	Dual Decade Counter
U9	Yes	1.000MHz Crystal Oscillator

FIGURE 4. ICs Installed.

Resistors	Installed	Comments
R1	No	200Ω 1/4W 1% [1]
R2, R6, R12	No	33.2kΩ 1/4W 1% [1]
R7, R10	No	0Ω Jumper 1/4W [1]
R11	No	576kΩ 1/4W 1% [1]
R5, R13	No	100Ω 1/4W 1% [1]
R3	Yes	200Ω 1/4W 1% [1]
R4	Yes	100Ω 1/4W 1%
R8	Yes	33.2kΩ 1/4W 1%
R9	Yes	0Ω Jumper 1/4W
R14	No	Termination Resistor
R15-R17	Yes	4.99kΩ 1/4W 1%
R18	Yes	49.9Ω 1/4W 1%
R19-R21	Yes	10kΩ 1/4W 1%

Potentiometers	Installed	Comments
RV1, RV2	No	50kΩ 1/4" 10-turn [1]

Capacitors	Installed	Comments
C3, C4,	Yes	2.2µF (25V) Tantalum
C1, C2, C6 - C13	Yes	0.1µF (50V) Ceramic
C5	Yes	10µF (10V) Tantalum

NOTE: (1) Included in Package.

FIGURE 5. Resistors and Capacitors Installed.

STEP-BY-STEP
BASIC OPERATIONS

Step 1 — ADS7808P or ADS7809P

A) To test the ADS7808P, set jumpers J4 and J5 to the "08" position and install an ADS7808P into U1.

B) To test the ADS7809P, set jumpers J4 and J5 to the "09" position and install an ADS7809P into U1.

Factory Setting: J4 and J5 set to "09", C3, C4, C5, C6 and 20-pin socket (U1) soldered to the board. ADS7809P plugged into socket (U1).
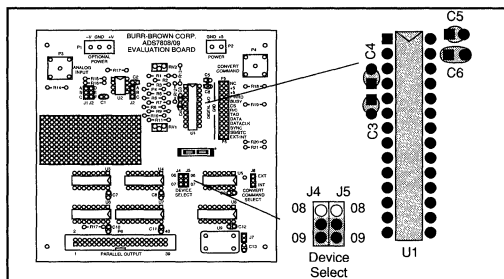
FIGURE 6. Factory Settings for Step 1.

Step 2 — On-Board Input Amplifier

To use the on-board input amplifier, supply P1 (Optional Power) with ±15V and move jumpers J1-J3 as follows:

Inverting Gain

Set jumpers J1 and J3 to AB and jumper J2 to DE (fig 6A) or EF (Fig 6B).
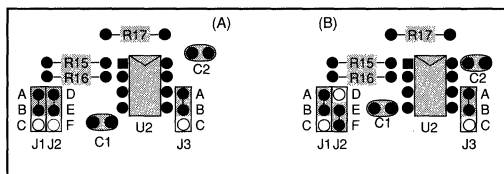
FIGURES 6a. and 6b.

The factory setting of the amplifier and resistors yields an inverting gain of two. Combinations of resistors R15, R16, and R17 will affect the gain as follows:

$$\text{Gain} = -(R17) / (R15 \parallel R16)$$

Non-Inverting Gain

Set jumper J3 to AB and combine J1 and J2 to connect B to E and A to D.
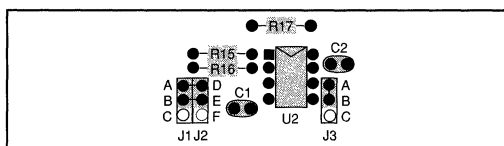
FIGURES 6c.

The factory setting of the amplifier and resistors yields a gain of three. Combinations of R15, R16, and R17 will affect the gain as follows:

$$\text{Gain} = \frac{[R17 + (R15 \parallel R16)]}{(R15 \parallel R16)}$$

NOTE: The on-board input amplifier may improve the quality of the signal reaching the ADS7808P or ADS7809P. This depends on the output characteristics of the signal generator.

Factory Setting: J1 and J3 set to BC and J2 set to DE, bypassing the amplifier. R15, R16, R17, C1, C2 and 8-pin socket (U2) soldered to the board. OPA671 plugged into socket (U2).
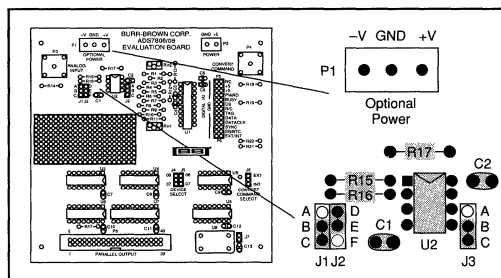

FIGURE 7. Factory Settings for Step 2.

Step 3 — Input Range, Offset/Gain Adjust

Input Range

A) Using Table II for bipolar ranges and Table III for unipolar ranges, choose the input voltage range for your application. Note that using the optional input amplifier will directly affect the input voltage seen at the converter input. (Refer to Step 2 for the gain of the amplifier in both the inverting and non-inverting configurations). Install the proper resistors.

Offset Adjust

B) To adjust offset, install the proper potentiometer and resistors, ground the input, then adjust the pot accordingly (see Table II and Figure 8).

Gain Adjust

C) To adjust gain, install the proper potentiometer and resistors, then adjust the pot accordingly. Do this for +FS and −FS (see Table II and Figure 8).

NOTE: Offset directly affects the gain. Always trim offset first. For maximum precision, more than one iteration of those adjustments may be required.

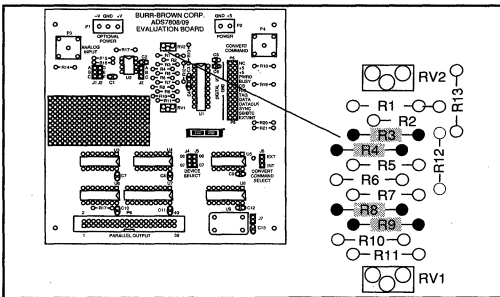**Factory Setting**: ±10V input range without offset/gain trim, R3, R4, R8 and R9 soldered into board.

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FIGURE 8. Factory Setting for Step 3.

Ref. Des. Value	FOR ±10V INPUT RANGE		FOR ±5V INPUT RANGE		FOR ±3.33V INPUT RANGE	
	With Trim	Without Trim	With Trim	Without Trim	With Trim	Without Trim
R1 (200Ω)			Install	Install		
R2 (33.2kΩ)			Install(2)			
R3 (200Ω)	Install	Install			Install	Install
R4 (100Ω)	Install	Install				
R5 (100Ω)			Install	Install	Install	Install
R6 (33.2kΩ)	Install(2)				Install(2)	
R7 (0Ω)						
R8 (33.2kΩ)		Install				Install
R9 (0Ω)	Install	Install	Install	Install	Install	Install
R10 (0Ω)						
R11 (576kΩ)	Install(1)		Install(1)		Install(1)	
R12(33.2kΩ)				Install		
R13 (100Ω)						
RV1 (50kΩ)	Install(1)		Install(1)		Install(1)	
RV2(50kΩ)	Install(2)		Install(2)		Install(2)	
NOTES: (1) Components associated with gain trim. (2) Components associated with offset trim.						

TABLE II. Bipolar Input Ranges With and Without Trim.

Step 4 — On-Board or External Convert Command Generator?

A) J6 set to "INT" selects the on-board convert command generator operating at 100kHz (divided down from 1MHz by U8).

B) J6 set to "EXT" selects an external convert command generator. Apply a negative-going pulse, 100ns in duration, to P4 (External Convert Command). This connector is terminated on the board with a 50Ω resistor (R18). Adjust the voltage of the generator for a 0V to 5V swing and the pulse rate to the desired frequency ($\leq$ 100kHz).

NOTE: When using an external convert command, the trace powering the on-board convert command generator can be cut to eliminate any noise contributions due to the oscillator. To reconnect the power, install a jumper at J7.

Factory Setting: J6 set to "INT", conversions synchronized to on-board convert command generator at 100kHz. P4, R18, C12, C13, U8 and U9 soldered to the board.

Ref. Des. Value	FOR 0 TO 10V INPUT RANGE		FOR 0V TO 5V INPUT RANGE		FOR 0V TO 4V INPUT RANGE	
	With Trim	Without Trim	With Trim	Without Trim	With Trim	Without Trim
R1 (200Ω)	Install	Install	Install	Install		
R2 (33.2kΩ)	Install(2)		Install(2)			
R3 (200Ω)					Install	Install
R4 (100Ω)			Install	Install	Install	Install
R5 (100Ω)	Install	Install				
R6 (33.2kΩ)					Install(2)	
R7 (0Ω)			Install	Install	Install	Install
R8 (33.2kΩ)						Install
R9 (0Ω)						
R10 (0Ω)	Install	Install				
R11 (576kΩ)	Install(1)		Install(1)		Install(1)	
R12(33.2kΩ)		Install		Install		
R13 (100Ω)						
RV1 (50kΩ)	Install(1)		Install(1)		Install(1)	
RV2(50kΩ)	Install(2)		Install(2)		Install(2)	
NOTES: (1) Components associated with gain trim. (2) Components associated with offset trim.						

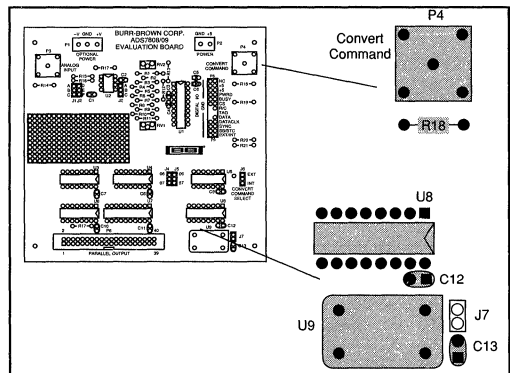TABLE III. Unipolar Input Ranges With and Without Trim.

FIGURE 9. Factory Setting for Step 4.

Step 5 — SB or BTC Format?

A) To get data in Binary Two's Complement format, place a jumper from pin 3 to pin 4 on P5.

B) To get data in Straight Binary format, remove the jumper from pin 3 to pin 4 on P5.

Factory Setting: Pin 3 jumpered to pin 4 on P5, output format is Binary Two's Complement.

NOTE: Pins 1, 15 and 19 also have jumpers but are not involved in the binary output format.
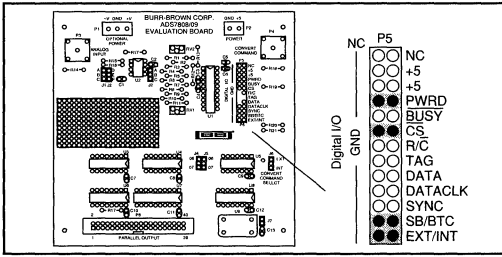
FIGURE 10. Factory Setting for Step 5.

Step 6 — Parallel or Serial Output?

Serial Output

A) To use the internal data clock, place a jumper from pin 1 to pin 2 on P5. Set J6 to "INT". Data from the last conversion will be clocked out on pin 9 of P5 at the start of a conversion synchronized to:

  • 12 clock pulses output on pin 7 of P5 (ADS7808P)
  • 16 clock pulses output on pin 7 of P5 (ADS7809P)

Data is valid on both the rising and falling edges of the internal data clock. Using the internal clock is preferred to optimize system performance.

B) To use an external data clock, remove the jumper from pin 1 to pin 2 on P5 and apply an external clock to pin 7 of P5. A positive SYNC pulse will follow a read command (rising edge on R/C with CS LOW or a falling edge on CS with R/C HIGH). The MSB will be valid on the first rising or falling edge of the external data clock after SYNC goes LOW. Data will be output on pin 9 of P5 synchronized to:

  • 12 clock pulses input on pin 7 of P5 (ADS7808P)
  • 16 clock pulses input on pin 7 of P5 (ADS7809P)

The frequency of the external clock must not exceed 10MHz. A duty cycle of 40% to 60% is suggested. BUSY (pin 17 of P5) can be used to latch the data. The data will always be from the most recently completed conversion.

Parallel Output

C) P6 outputs 16-bit buffered parallel data converted from serial to parallel via U3, U4, U6, and U7. Data can be acquired on pins:

  • 1 (MSB), 3 ... 21, 23 (LSB) with pins 25, 27, 29 and 31 outputting LOWs for the ADS7808P
  • 1 (MSB), 3 ... 29, 31 (LSB) for the ADS7809P

A rising edge pulse will be output on pin 33 (DATA VALID) of P6 signifying the end of a conversion and that data is valid. Data will be from the most recently completed conversion. Be sure pin 1 is tied to pin 2 of P5 with a jumper. This selects the internal data clock. Serial data will be converted to parallel.

Factory Setting: Pin 1 jumpered to pin 2 on P5. P5, P6, U3, U4, U6, and U7 soldered to the board.

NOTE: Pins 3, 15, and 19 of P5 have jumpers but are not involved with the output format. R21 is a pull-up resistor for the EXT/INT pin on the converter.
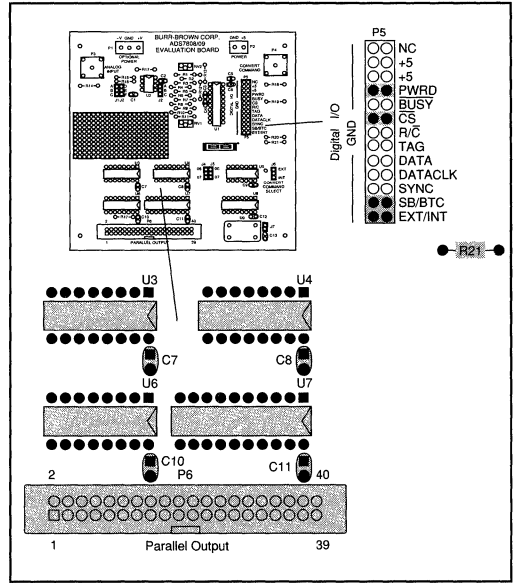

FIGURE 11. Factory Settings for Step 6.

Step 7 — Power Supplies?

A) A 5V power supply connected to P2 (POWER), is all that is required to operate the DEM-ADS7808/09C.

B) If the optional amplifier is used, P1 must be supplied with power (OPA671 requires at least ±15V for this application when using ±10V input range).

Factory Setting: P1 and P2 connectors soldered to the board and ready for connection to the appropriate power supplies.
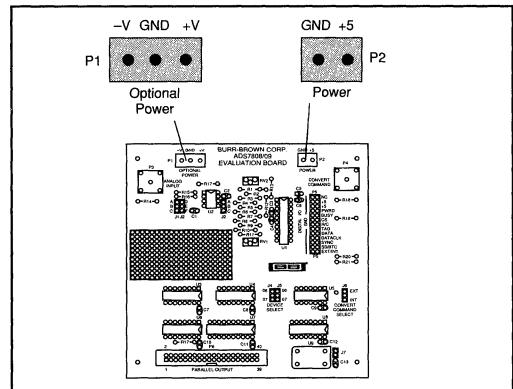

FIGURE 12. Factory Settings for Step 7.

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OTHER OPTIONS

The following pins on P5 serve optional functions of the ADS7808P or ADS7809P:

PWRD	pin 19
CS	pin 15
TAG	pin 11

Refer to ADS7808P and ADS7809P product data sheets for the description of these options.

Factory Setting: PWRD tied LOW with jumper from pin 19 to pin 20. CS tied LOW with jumper from pin 15 to pin 16. TAG, no jumper.
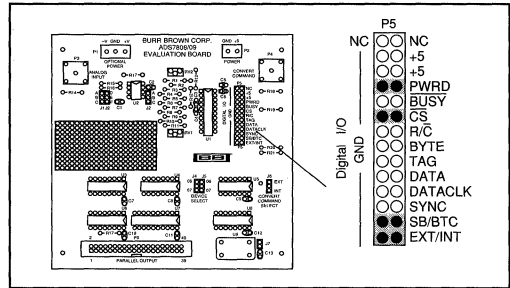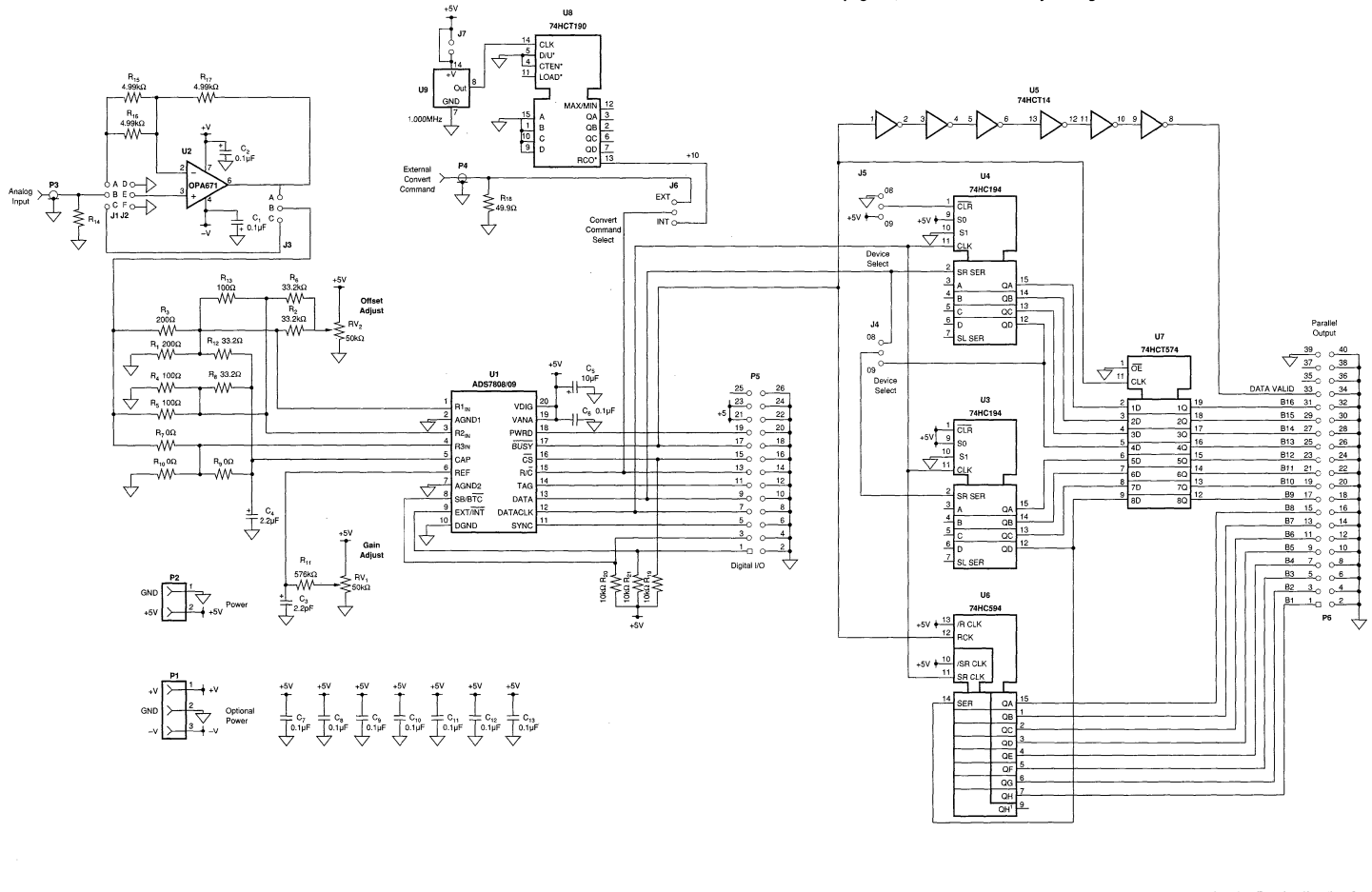

FIGURE 13. Factory Settings for Other Options.

NOTE: This circuit diagram includes the offset and gain circuitry for all input ranges.
Refer to pages 3, 4 and 5 for the factory settings.

FIGURE 14. DEM-ADS7808/09C Circuit Diagram.

DEM-ADS7808/09

PIN	ADS7808/09P FUNCTION	PIN	ADS7808/09P FUNCTION
1	EXT/$\overline{\text{INT}}$	2	GND
3	SB/$\overline{\text{BTC}}$	4	GND
5	SYNC	6	GND
7	DATACLK	8	GND
9	DATA	10	GND
11	TAG	12	GND
13	R/$\overline{\text{C}}$	14	GND
15	$\overline{\text{CS}}$	16	GND
17	$\overline{\text{BUSY}}$	18	GND
19	PWRD	20	GND
21	+5	22	GND
23	+5	24	GND
25	NC	26	NC

TABLE III. Pinout of the Digital I/O Connector (P5).

PIN	ADS7808/09P FUNCTION	PIN	ADS7808/09PFUNCTION
1	Bit 1 (MSB)	2	GND
3	Bit 2	4	GND
5	Bit 3	6	GND
7	Bit 4	8	GND
9	Bit 5	10	GND
11	Bit 6	12	GND
13	Bit 7	14	GND
15	Bit 8	16	GND
17	Bit 9	18	GND
19	Bit 10	20	GND
21	Bit 11	22	GND
23	Bit 12	24	GND
25	Bit 13	26	GND
27	Bit 14	28	GND
29	Bit 15	30	GND
31	Bit 16 (LSB)	32	GND
33	DATA VALID	34	GND
35	NC	36	GND
37	NC	38	GND
39	GND	40	GND

NOTE: (1) Tag data will appear when clocking out more than 12 bits of data for the ADS7808P, or 16 bits of data for the ADS7809P, using an external data clock. Refer to the product data sheet.

TABLE IV. Pinout of the Buffered Parallel Output Connector (P6).
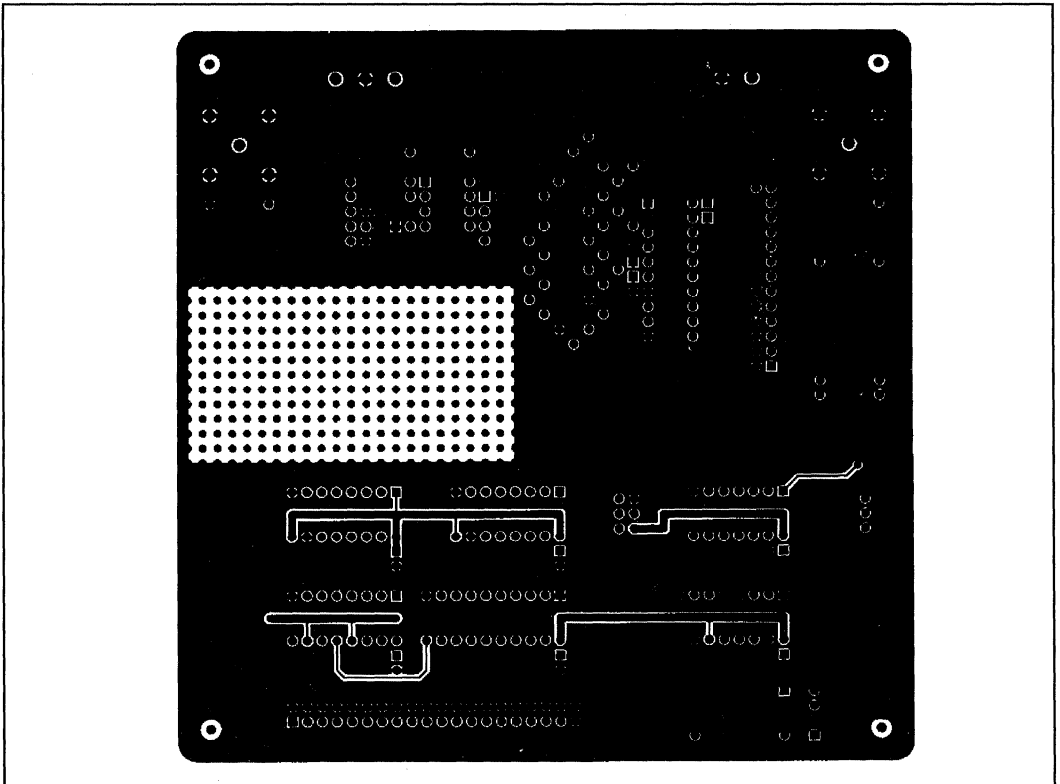

FIGURE 15. PCB Component Side
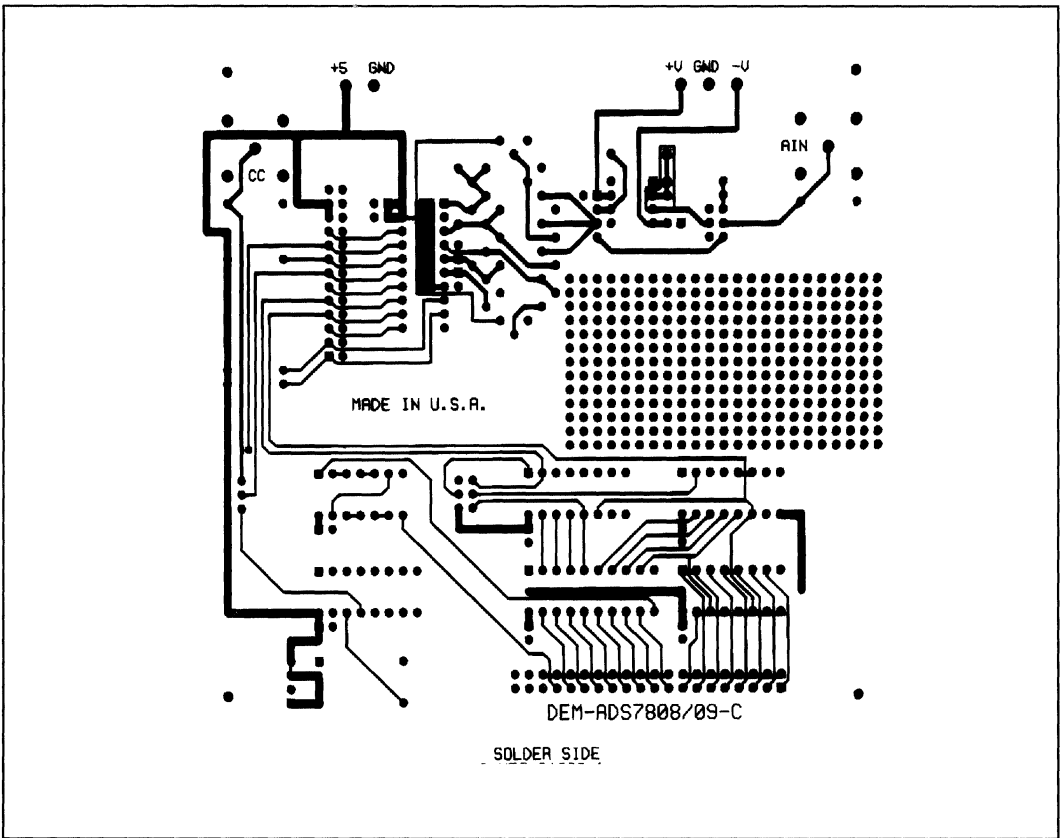
FIGURE 16. PCB Solder Side.

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INSTALLED COMPONENT LIST

REFERENCE	QUANTITY	PART NUMBER	DESCRIPTION	MANUFACTURER[1]
C3, C4	2	TAP225K025SCS	2.2µF 25V Tantalum Capacitor	AVX
C1, C2, C6-C13	10	SR205C104KAA	0.1µF 50V X7R Ceramic Capacitor	Kemet
C5	1	TAP106KO10SCS	10µF 10V Tantalum Capacitor	AVX
J1-J6	6	NSH-3SB-S1-T	3x1 0.1" Header	Robinson Nugent
P1	1	ED500/3DS	3-Terminal Power Block	On-Shore Tech.
P2	1	ED500/2DS	2-Terminal Power Block	On-Shore Tech.
P3,P4	2	KC-79-274-M06	PC Mount BNC Connector	Kings
P5	1	NSH-26-DB-S1-T	13 x 2 0.1" Header	Robinson Nugent
P6	1	IDH-40LP-S3-TG	20 x 2 0.1" Shrouded Header	Robinson Nugent
R8	1	SFR55	33.2kΩ 1/4W 1% MF Resistor	Philips
R3	1	SFR55	200Ω 1/4W 1% MF Resistor	Philips
R15-R17	3	SFR55	4.99kΩ 1/4W 1% MF Resistor	Philips
R18	1	SFR55	49.9Ω 1/4W 1% MF Resistor	Philips
R19-R21	3	SFR55	10kΩ 1/4W 1% MF Resistor	Philips
R9	1	FRJ-55	0Ω Jumper (1/4W size)	Dale
R4	1	SFR55	100Ω 1/4W 1% MF Resistor	Philips
U1	1	ADS7809P	16-Bit 100kHz Sampling ADC	Burr-Brown
U2	1	OPA671AP	Op Amp	Burr-Brown
U3, U4	2	74HC194	4-Bit Shift Register DIP	T.I.
U5	1	74HCT14	Hex Schmitt Inverter DIP	T.I.
U6	1	74HC594	8-Bit Shift Register DIP	T.I.
U7	1	74HCT574	8-Bit Latch DIP	T.I.
U8	1	74HCT190	Decade Counter DIP	T.I.
U9	1	DOC-2-1.000MHz	1.000MHz Crystal Oscillator (4-Pin)	Dawia
U2	1	DIP308-11B	8-Pin DIP Socket	McKenzie
U1	1	DIP320-11B	20-Pin DIP Socket	McKenzie
	4	SJ-5003	Bumpon Hemisphere 0.44 x 0.20 Black	3M
	10	ME151-8001	0.1" Shunt Block	Mouser

NOTE: (1) For reference only. Equivalent components may be used.

PACKING LIST

REFERENCE	QUANTITY	ITEM	DESCRIPTION	MANUFACTURER[1]
Demo Board	1	DEM-ADS7808/09C	Fully assembled printed circuit board with ADS7809P installed	Burr-Brown
ADS7808P	1	PDS-1155A	ADS7808 Product Data Sheet	Burr-Brown
ADS7809P	1	PDS-1154A	ADS7809 Product Data Sheet	Burr-Brown
Demo Board Info	1	LI-457	DEM-ADS7808/09C Manual	Burr-Brown
R2, R6, R12	3	SFR55	33.2kΩ 1/4W 1% MF Resistor	Philips
R1	1	SFR55	200Ω 1/4W 1% MF Resistor	Philips
R7, R10	2	FRJ-55	0Ω Jumper (1/4W size)	Dale
R11	1	SFR55	576kΩ 1/4W 1% MF Resistor	Philips
R5, R13	2	SFR55	100Ω 1/4W 1% MF Resistor	Philips
RV1, RV2	2	RJ26FW503	50kΩ 1/4" Ten-Turn Pot	Bourns
U1	1	ADS7808P	12-Bit 100kHz Sampling ADS	Burr-Brown

NOTE: (1) For reference only. Equivalent components may be used.

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DEM-ADS7810/19C

EVALUATION FIXTURE
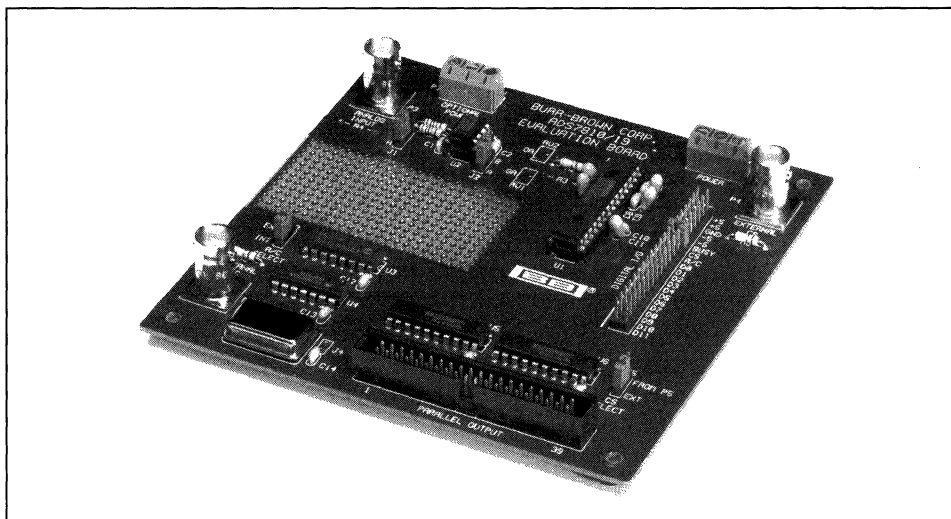
FEATURES

● **800kHz 12-BIT ADS7810P AND ADS7819P INCLUDED**

● **12-BIT BUFFERED PARALLEL OUTPUT**

● **CONNECTOR FOR ALL DIGITAL I/O PINS**

● **CRYSTAL OSCILLATOR BASED 800kHz CONVERT COMMAND GENERATOR**

● **EXTERNAL R/C̄ AND C̄S̄ CONNECTORS**

● **PROTOTYPE AREA**

APPLICATIONS

● **EVALUATE ADS7810P AND ADS7819P PERFORMANCE**

● **BREADBOARD COMPLETE ANALOG SYSTEM**

● **EVALUATE SIMPLE TWO-LAYER PCB LAYOUT**

● **INCOMING INSPECTION TEST FIXTURE**

DESCRIPTION

The DEM-ADS7810/19C Evaluation Fixture is a fully assembled printed circuit board used to evaluate ADS7810P and ADS7819P. This device incorporates an analog input amplifier (with provisions to bypass this amplifier), a parallel digital output buffer, a crystal oscillator-based 800kHz convert command generator, external R/C̄ and C̄S̄ connectors, and a 2.3" x 1.2" breadboard area. The DEM-ADS7810/19C achieves full converter performance on a two-layer board.

This fixture requires only ±5V power supplies. An optional bipolar power supply connector is provided for the input amplifier and breadboarding.

DEM-ADS7810/19

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TABLE OF CONTENTS

HOW TO USE THIS MANUAL

A table and diagrams are included in the "Factory Settings" section showing how the board is configured from the factory. A listing of other components, which are shipped with the board, is also included.

The Step-by-Step Basic Operations section describes all of the options. At the end of each step, a figure illustrates factory settings. Items installed are highlighted in those figures.

For further details on the OPA671, ADS7810P, ADS7819P, or any other device on the DEM-ADS7810/19C, refer to the specific product data sheet.
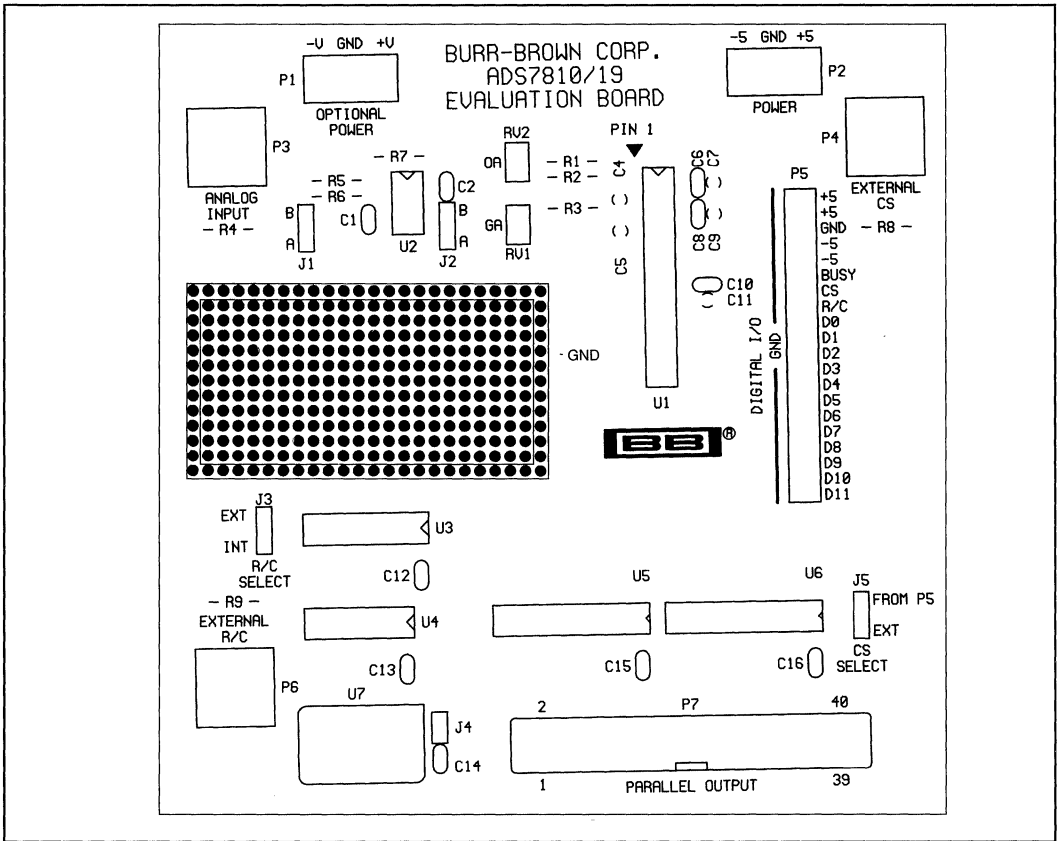
FIGURE 1. PCB Legend.

FACTORY SETTINGS

With ±5V supplies connected to P2, the DEM-ADS7810/19C starts converting at 800kHz with an input range of ±10V(ADS7810P) or ±2.5V (ADS7819P). Data can be read in full parallel from P5. Buffered full parallel can be read from P6. The following is a listing of "factory settings".

MAKE SELECTION FOR EACH STEP (1)	FACTORY SETTINGS	OPTIONS (requires alteration of the demo board, all needed components included).
1. Device	ADS7810P installed.	ADS7819P included for installation.
2. Input Amplifier	OPA671 bypassed.	Switching jumpers on J1 and J2 to "B" selects input amplifier. Apply ±15V to P1.
3. Offset Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometers included for installation. See Step-by-Step Basic Operations, step 3.
Gain Adjust	Trim circuit not installed.	Trim circuit resistors and potentiometers included for installation. See Step-by-Step Basic Operations, step 3.
4. Convert Command	On-board 800kHz convert command generator connected to R/C. CS tied LOW on P5 with a jumper.	A combination of R/C and CS can be used to control the conversions via P4 and P6. Refer to the product datasheets for timing diagrams and limits.
5. Output Format	12-bit buffered full parallel output.	Full parallel output (P5).
6. Power Supplies	3-pin power block (P2) ready for ±5V.	3-pin power block (P1) ready for ±15V (for use with breadboard and optional input amplifier).
NOTE: (1) Each of these steps is explained in detail in the Step-by-Step Basic Operations section.		

TABLE I. Quick Reference to Factory Settings and Other Options.

DEM-ADS7810/19

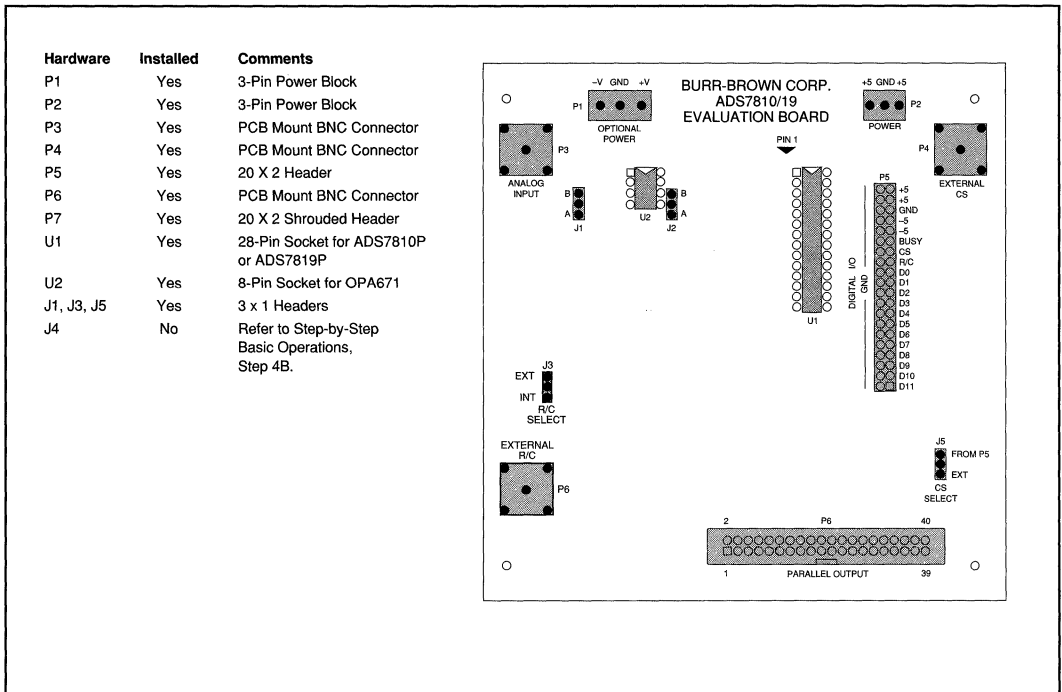# FACTORY SETTINGS (CONT)

Hardware	Installed	Comments
P1	Yes	3-Pin Power Block
P2	Yes	3-Pin Power Block
P3	Yes	PCB Mount BNC Connector
P4	Yes	PCB Mount BNC Connector
P5	Yes	20 X 2 Header
P6	Yes	PCB Mount BNC Connector
P7	Yes	20 X 2 Shrouded Header
U1	Yes	28-Pin Socket for ADS7810P or ADS7819P
U2	Yes	8-Pin Socket for OPA671
J1, J3, J5	Yes	3 x 1 Headers
J4	No	Refer to Step-by-Step Basic Operations, Step 4B.

FIGURE 2. Hardware Installed.

Jumpers for:	Setting	Comments
J1, J2	"A"	U2 (Input Amplifier Socket) bypassed
J3	"INT"	Crystal On-Board Convert Command Generator Selected (Outputs 800kHz to R/$\overline{C}$)
J5	"From P5"	$\overline{CS}$ Controlled by Pin 27 of P5
P5	Pin 27 to 28	$\overline{CS}$ Tied LOW

FIGURE 3. Jumpers Installed.

FACTORY SETTINGS (CONT)

ICs	Installed	Comments
ADS7819P	No	Included in Package
ADS7810P	Yes	Plugged into 28-Pin Socket (U1)
OPA671	Yes	Plugged into 8-Pin Socket (U2)
U3	Yes	4-Bit Decade Counter
U4	Yes	Hex Schmitt Inverters
U5, U6	Yes	8-Bit Latch
U7	Yes	8.000MHz Crystal Oscillator

FIGURE 4. ICs Installed.

Resistors	Installed	Comments
R1	No	4.99kΩ 1/4W 1%[1]
R3	No	221kΩ 1/4W 1%[1]
R4	No	49.9 Ω 1/4W 1%[1]
R2, R8, R9	Yes	49.9 Ω 1/4W 1%
R5, R6, R7	Yes	1kΩ 1/4W 1%

Pots	Installed	Comments
RV1, RV2	No	5kΩ 1/4" 1%[1]

Capacitors	Installed	Comments
C1, C2, C6,C8, C10, C12-C16	Yes	0.1µF (50V ceramic)
C4, C5, C7, C9, C11	Yes	10µF (10V Tantalum)

NOTE: (1) Included in Package.

FIGURE 5. Resistors and Capacitors Installed.

DEM-ADS7810/19

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STEP-BY-STEP
BASIC OPERATIONS

STEP 1 — ADS7810P OR ADS7819P

A) To test the ADS7810P, install an ADS7810P in U1.

B) To test the ADS7819P, install an ADS7819P in U1.

NOTE: The ADS7810P has an input range of ±10V. The ADS7819P has an input range or ±2.5V. No alteration of the board is necessary when switching from one to the other.

Factory Setting: C4-C11 and 28-pin socket soldered to the board. ADS7810P plugged into U1.
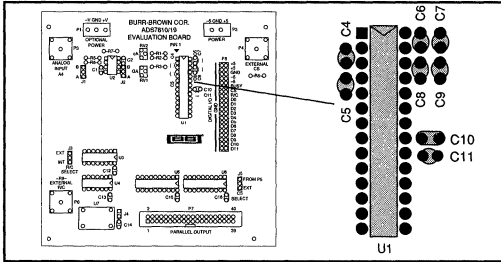

FIGURE 6. Factory Settings For Step 1.

Step 2 — On-Board Input Amplifier

To use the on-board input amplifier, jumpers J1 and J2 must be set to the "B" position, and P1 (Optional Power) must be supplied with ±15V. The factory setting of the amplifier yields an inverting gain of 2. Combinations of resistors R5, R6, and R7 will affect the gain of the amplifier as follows:

$$\text{GAIN} = -(R7)/(R5 \parallel R6)$$

NOTE: The on-board input amplifier may improve the quality of the signal reaching the ADS7810P or ADS7819P. This depends on the output characteristics of the signal generator.

Factory Setting: J1 and J2 set to "A", bypassing the amplifier, R5, R6, R7, C1, C2 and 8-pin socket (U2) soldered to the board. OPA671 plugged into U2.
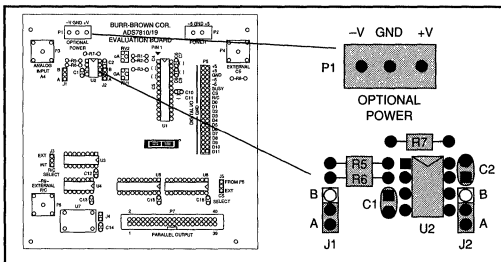

FIGURE 7. Factory Settings for Step 2.

Step 3 — Offset/Gain Adjust

Offset Adjust

A) To adjust offset, install RV2 (5kΩ) and R1 (4.99kΩ), ground the input, then adjust RV2. See Figure 8 for location of RV2 and R1.

Gain Adjust

B) To adjust gain, install RV1 (5kΩ) and R3 (221kΩ), then adjust RV1. Do this for +full scale and –full scale. See Figure 8.

NOTE: The offset directly affects the gain. Always trim offset first. For maximum precision, more than one iteration of these adjustments may be required.

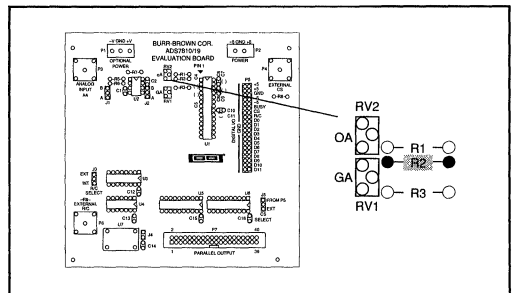**Factory Setting:** ±10V input range without offset/gain trim, R2 soldered to the board.

FIGURE 8. Factory Settings for Step 3.

Step 4 — Convert Command Generator

A) J3 set to "INT" selects the on-board convert command generator operating at 800kHz (divided down from 8MHz by U3).

B) J3 set to "EXT" selects an external convert command generator. Apply a negative-going pulse, 100ns in duration, to P6 (External Convert Command). This connector is terminated on the board with a 50Ω resistor (R8). Adjust the voltage of the generator for a 0V to 5V swing and the pulse rate to the desired frequency (≤800kHz). NOTE: When using an external convert command, the trace powering the on-board convert command generator can be cut to eliminate any noise contributions due to the oscillator. To reconnect, install a jumper at J4.

C) J3 and J5 set to "EXT" allows the user to control the "read" and "convert" commands via P4 ($\overline{CS}$) and P6 (R/$\overline{C}$). Refer to the product data sheets for timing diagrams and limits.

Factory Setting: J5 set to "From P5", J3 set to "INT", conversions synchronized to on-board convert command generator at 800kHz. P4, P6, R8, R9, U3, U7, C12 and C14 soldered to the board.
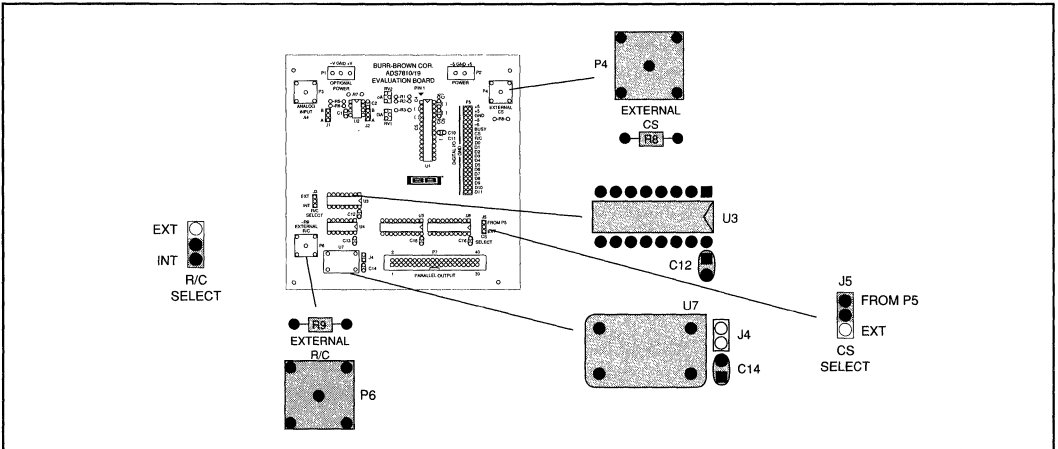
FIGURE 9. Factory Settings for Step 4.

Step 5 — Parallel Output

A) P5 outputs full parallel data — See Figure 10.

B) P6 outputs buffered full parallel data—See Figure 10.

A rising edge pulse will be output on pin 33 (Data Valid) of P6 signifying the end of a conversion and that data is valid. Data will be from the most recently completed conversion.

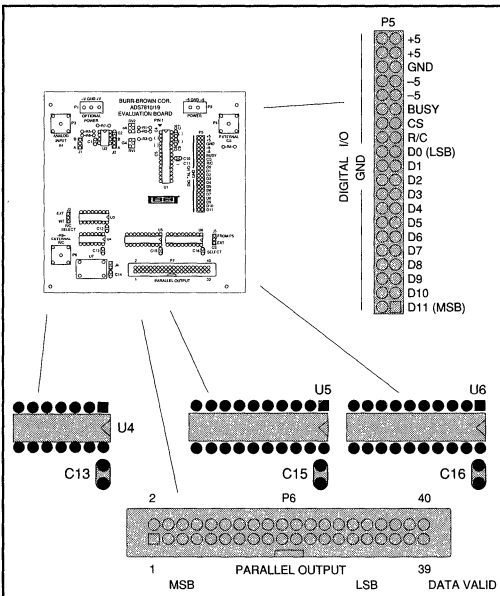**Factory Setting**: P5, P6, U4, U5, U6, C13, C15 and C16 soldered to the board. Buffered full parallel output on P6.

Step 6 — Power Supplies

A) ±5V power supplies connected to P2 (Power) is all that is required to operate the DEM-ADS7810/19C.

B) If the optional amplifier is used, P1 must be supplied with power (OPA671 requires at least ±15V for this application).

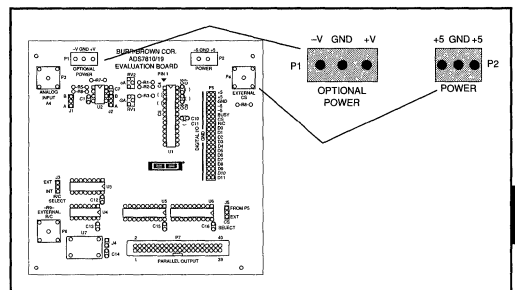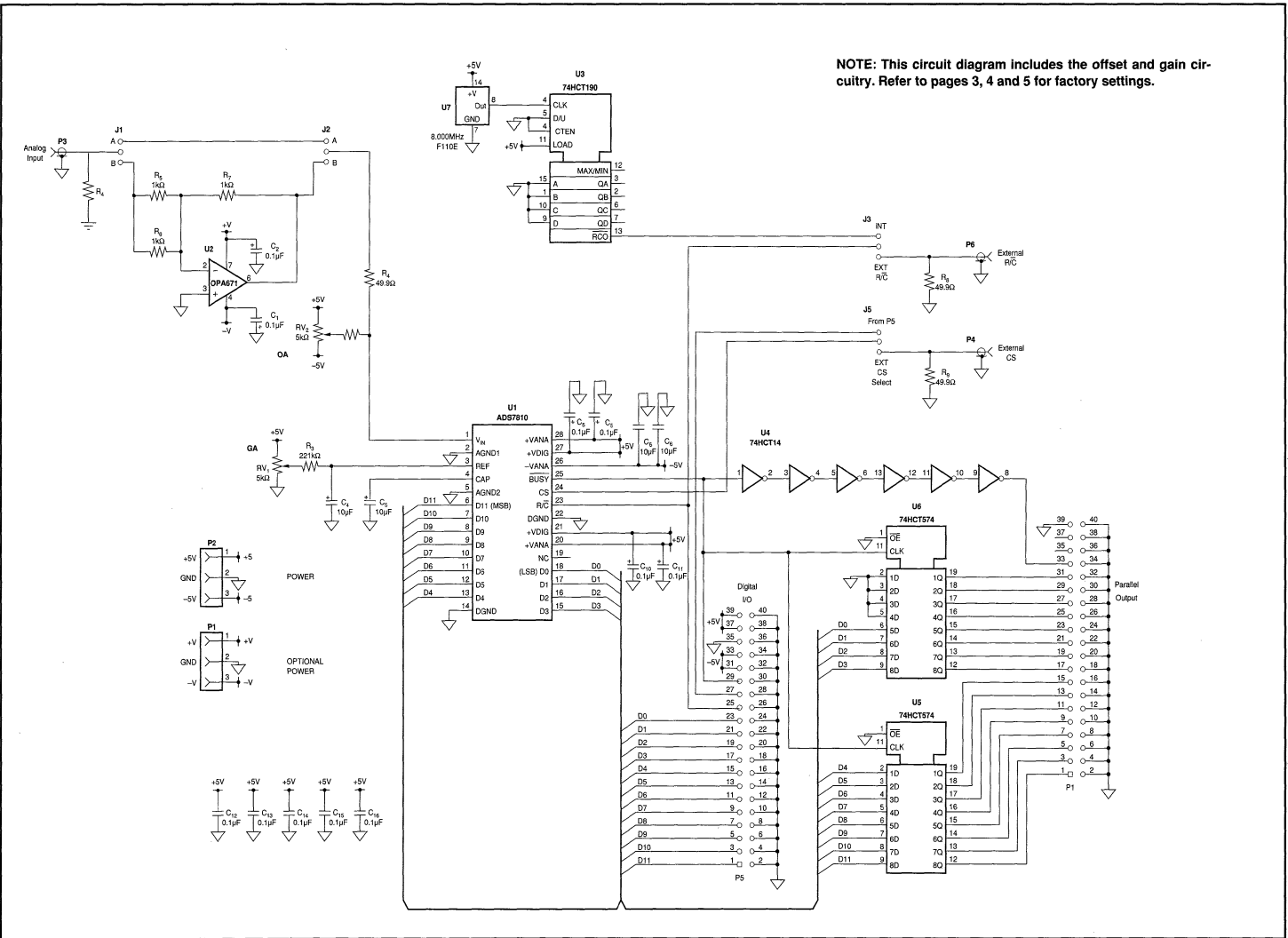**Factory Setting**: P1 and P2 ready to be connected to the appropriate power supplies.

FIGURE 11. Factory Settings for Step 6.

FIGURE 10. Factory Settings for Step 5.

DEM-ADS7810/19

FIGURE 12. DEM-ADS7810/19C Circuit Diagram.

Burr-Brown IC Data Book—Data Conversion Products

NOTE: This circuit diagram includes the offset and gain circuitry. Refer to pages 3, 4 and 5 for factory settings.

PIN	ADS7810/19P FUNCTION	ADS7810/19P FUNCTION	PIN
1	D11(MSB)	GND	2
3	D10	GND	4
5	D9	GND	6
7	D8	GND	8
9	D7	GND	10
11	D6	GND	12
13	D5	GND	14
15	D4	GND	16
17	D3	GND	18
19	D2	GND	20
21	D1	GND	22
23	D0 (LSB)	GND	24
25	R/$\overline{C}$	GND	26
27	$\overline{CS}$	GND	28
29	BUSY	GND	30
31	–5V	GND	32
33	–5V	GND	34
35	GND	GND	36
37	+5V	GND	38
39	+5V	GND	40

TABLE II. Pinout of the Digital I/O Connector (P5).

PIN	ADS7810/19P FUNCTION	ADS7810/19P FUNCTION	PIN
1	B1(MSB)	GND	2
3	B2	GND	4
5	B3	GND	6
7	B4	GND	8
9	B5	GND	10
11	B6	GND	12
13	B7	GND	14
15	B8	GND	16
17	B9	GND	18
19	B10	GND	20
21	B11	GND	22
23	B12	GND	24
25	DATA LOW	GND	26
27	DATA LOW	GND	28
29	DATA LOW	GND	30
31	DATA LOW	GND	32
33	DATA VALID	GND	34
35		GND	36
37		GND	38
39	GND	GND	40

TABLE III. Pinout of Buffered Output (P6).
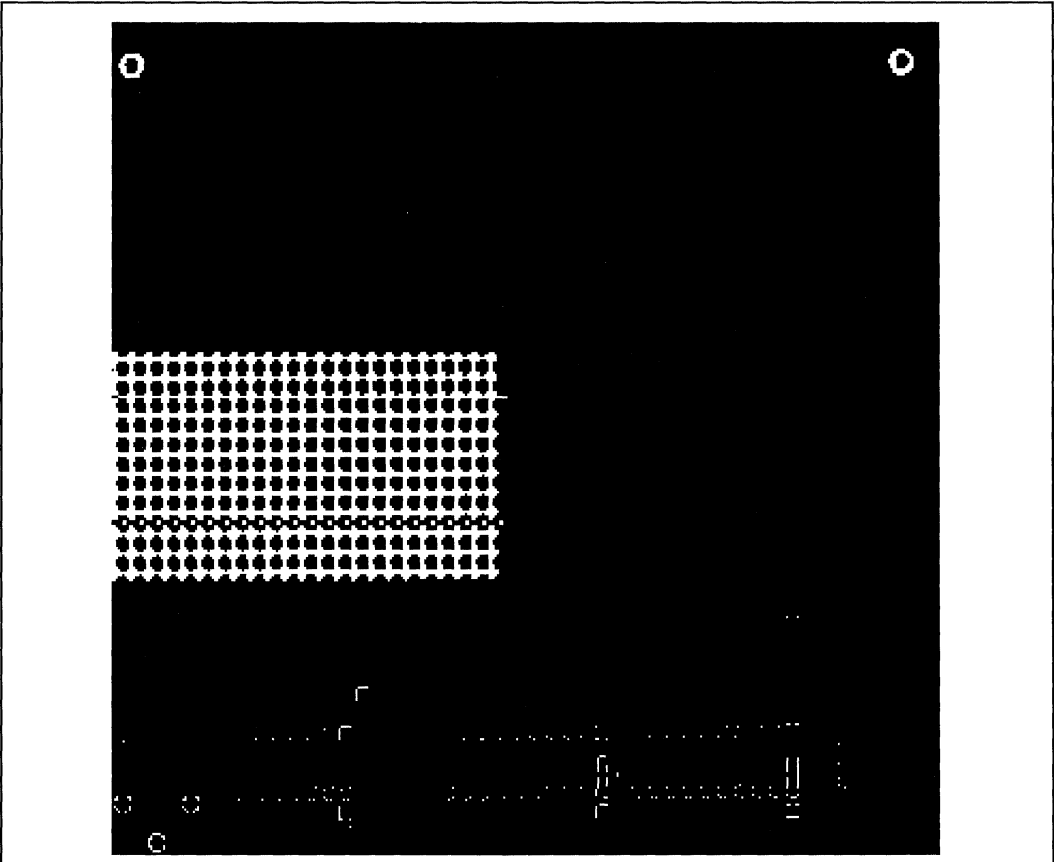
FIGURE 13. PCB Component Side (Ground Plane).

DEM-ADS7810/19

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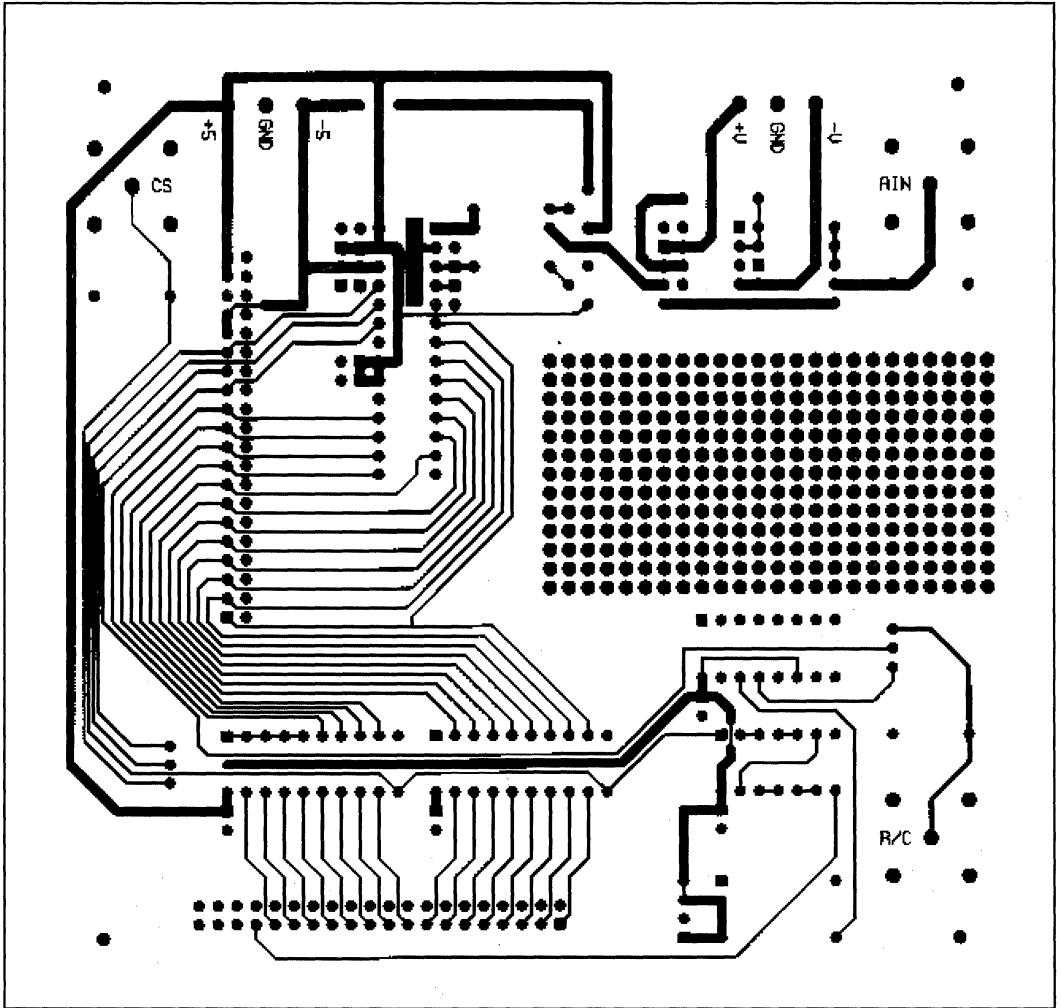FIGURE 14. PCB Solder Side

INSTALLED COMPONENT LIST

REFERENCE	QUANTITY	PART NUMBER	DESCRIPTION	MANUFACTURER[1]
C1, C2, C6, C8-C10 C12-C16	10	SR205C104KAA	0.1µF Ceramic Capacitor	AVX
C3-5, 7, 9,11	6	TAP106K010SCS	10µF 10V Tantalum Capacitor	AVX
J1-J3, J5	4	NSH-3SB-S1-T	3 X 1 Header	Robinson Nugent
P7	1	IDH-40LP-S3-TG	20 x 2 Shrouded Header	Robinson Nugent
P1, P2	2	ED500/3DS	3-pin Power Block	On-Shore Technology
P3, P4, P6	3	KC-79-274-M06	PCB Mount BNC Connector	Kings
P5	1	NSH-40DB-S1-T	20 X 2 Header	Robinson Nugent
R2, R8, R9	3	5043ED49R90F	49.9Ω 1/4W 1% MF Resistor	Philips
R5, R6, R7	3	5193ED1K000F	1kΩ 1/4W 1% MF Resistor	Philips
U1	1	ADS7810P	12-Bit Sampling A/D Converter	Burr-Brown
U2	1	OPA671	Op Amp	Burr-Brown
U3	1	74HC190	4-Bit Decade Counter DIP	T.I.
U4	1	74HC14	Hex Schmitt Inverters DIP	T.I.
U5, U6	2	74HC574	8-Bit Latch DIP	T.I.
U7	1	F1100E	8.000MHz Crystal Oscillator	Fox
	5	MSB-2366-G-C-STP	0.1 Centerline Shunt	McKenzie
U1	1	DIP-328011B	28-Pin Socket (0.3")	McKenzie
U2	1	DIP-308011B	8-Pin Socket	McKenzie

PACKING LIST

REFERENCE	QUANTITY	ITEM	DESCRIPTION	MANUFACTURER[1]
Demo Board	1	DEM-ADS7810/19C	Fully assembled printed circuit board with ADS7810P installed.	Burr-Brown
U1	1	ADS7819P	12-bit Sampling A/D Converter	Burr-Brown
RV1,RV2	2	RJ26FW502	5kΩ 1/4" trimmer resistors	Bourns
R1	1	5043ED4k990F	4.99kΩ 1/4W 1% MF resistor	Phillips
R3	1	5043ED4221KF	221kΩ 1/4W 1% MF resistor	Phillips
ADS7810P	1	PDS-1138A	ADS7810 Product Data Sheet	Burr-Brown
ADS7819P	1	PDS-1193A	ADS7819 Product Data Sheet	Burr-Brown
Demo Board Info.	1	LI-454	DEM-ADS7810/19C Manual	Burr-Brown

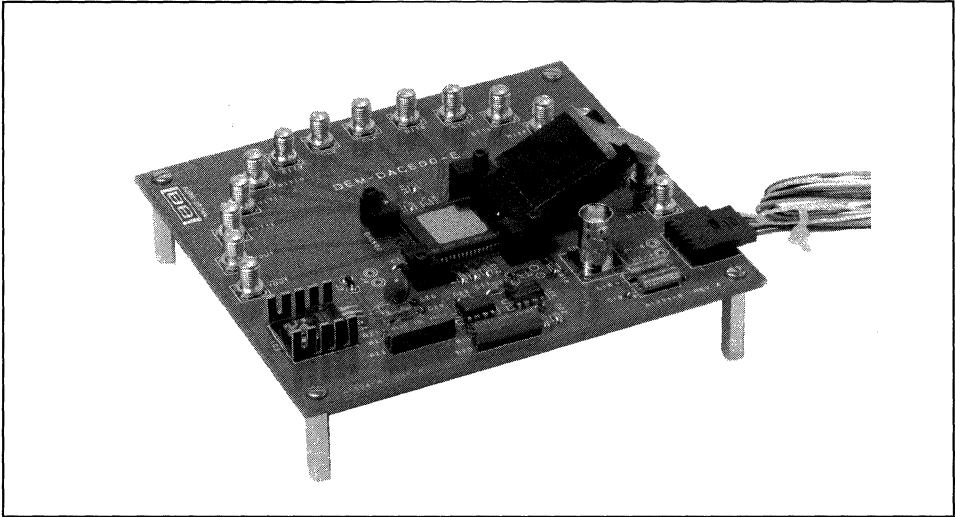NOTE: (1) For reference only. Equivalent components may be used.

DEM-ADS7810/19

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DEM-DAC600-E
EVALUATION FIXTURE

FEATURES

● **PROVIDES FOR FAST AND EASY PERFORMANCE TESTING**

● **GIVES OPTIMIZED PC BOARD LAYOUT**

● **SMA CONNECTORS FOR ALL DIGITAL INPUTS**

● **BNC CONNECTOR FOR VARIABLE REFERENCE INPUTS**

● **50Ω PULL-DOWN RESISTORS ON BOARD**

DESCRIPTION

The DEM-DAC600-E is an evaluation board for the DAC600—a 12-bit, 256MHz digital-to-analog converter with ECL compatible inputs. By supplying the power, bit inputs and clock, both the DC and AC performance of the DAC can be quickly evalutated. Refer to Figure 1 for the schematic of the board. Since there are different grades of the DAC600, a DAC600 is not included with this board.

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POWER SUPPLIES

This demonstration board requires the application of a −5.2V supply for the DAC, a +5V supply for the on board reference (optional), and a ground.

INPUTS

This evaluation board has high frequency SMA connectors for the digital inputs. There are 50Ω pull-down resistors to −2V on the digital inputs provided for on the demo board. The −2V circuit is derived from the −5.2V power supply per Figure 3. The −2V reference can be trimmed by adjusting R_{22}. This potential can be measured at J_3.

DAC REFERENCE OPTIONS

The DAC600 uses an external +1V reference which is supplied on the evaluation board using the circuit in Figure 4. This reference circuit can be adjusted to different values by adjusting resistor R_{20}. The reference value can be measured at jumper J_1. Since the DAC can be used in a multiplying mode, a provision has been made so that an external AC signal can be supplied as a reference. This input is terminated with 50Ω to ground. These options are selected through either jumpers J_1 or J_2. Care must be taken not to exceed the maximum input reference range.

DUT PLACEMENT

A DUT clamp is provided on the board for evaluation of multiple DACs. To work the clamp, simply place the connective elastomer sheet down first, place the unit on top of the elastomer with Pin 1 aligned with the white dot on the PC board and fasten the clamp. Because the elastomer does not have unlimited elasticity, it is recommended that the DUT be taken off of the elastomer when not in use.

OUTPUT

The DAC600 has complementary outputs V_{OUT} and $V_{OUT NOT}$. Both of these outputs have 50Ω output impedances. These outputs should be terminated correctly. Since $V_{OUT NOT}$ is the output that is trimmed to the highest accuracy, this output is recommended for single ended operation. The unused output should be terminated to match the impedance of the used output. SMA connectors are provided for these analog outputs.

SIGNAL LINE TERMINATION

It was found that terminating the signal lines at the DAC600 can cause ground currents which produce spurs in the 108-118MHz range. As a result all bit and clock line resistors R13-R16 as well as capacitors C13-C17, C27, and C28, have been removed from the demo board. This allows the use of series termination as a method of connecting the signals to the demo board.

When using series termination to obtain 50Ω, a 47Ω resistor is placed at the output of the driving gate. The drive cable or 50Ω line is connected in series with the resistor. See Figure 1.

DEM-DAC600-E PARTS LIST

REFERENCE DESIGNATION	DESCRIPTION	QUANTITY
P_1	Amp 102203-3 6 Pin-Plug	1
All capacitors except C_{18}, C_{19}, C_{25}, C_{26}	Chip Capacitor CFC106D104 (0.1µF)	21
C_{24}	Chip Capacitor CFC100C103 (0.01µF)	1
C_{18}, C_{19}	CF252-106 10µF Electrolytic Capacitors (leaded device)	2
C_{25}	CF252-105 1µF Electrolytic Capacitors (leaded device)	1
C_{26}	47µF Tantalum	1
C_{27}, C_{28}	10µF Tantalum	2
All resistors except R_{19}, R_{20}, R_{21}, R_{22}, R_{23}	Chip Resistors 50Ω	18
R_{19}	1kΩ 1% Film Resistor (leaded device)	1
R_{20}	10kΩ Trim Pot	1
R_{21}	499Ω 1% Film Resistor (leaded device)	1
R_{23}	200Ω 1% Film Resistor (leaded device)	1
R_{22}	200Ω Trim Pot	1
IC_1	Burr-Brown REF200 (8-pin DIP)	1
IC_2	Burr-Brown OPA602 (8-pin DIP)	1
	Optional DUT Holder	1
IC_3	LM337T (3 term adj neg volt reg 1.5 amp)	1
SMA	DIGI-Key J500-NC 0.2" PC mount SMA (see attached)	16
BNC	PC Mount BNC Kings KC-79-274-M06	1
Misc.	DUT Clamp	1
Misc.	1" X 1" SHIN-ETSU Elastomer Conductive Interconnect Sheet	1

NOTE: R_1, R_2 do not exist, as they were removed from the drawings.

Consult an ECL handbook for proper methods of series termination, as the 47Ω mentioned is an approximation.

If it is desired to terminate at the DAC, the components listed in the DEM-DAC600-E data sheet can be added. If this is done, C27 should be placed in parallel with C13 and C28 in parallel with C15. With J3 installed, −2V is supplied to the pull down resistors.
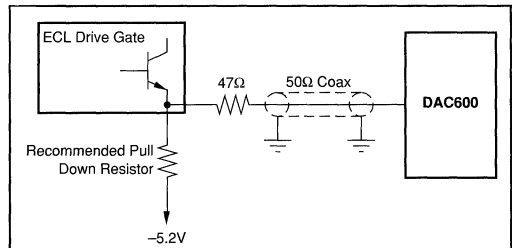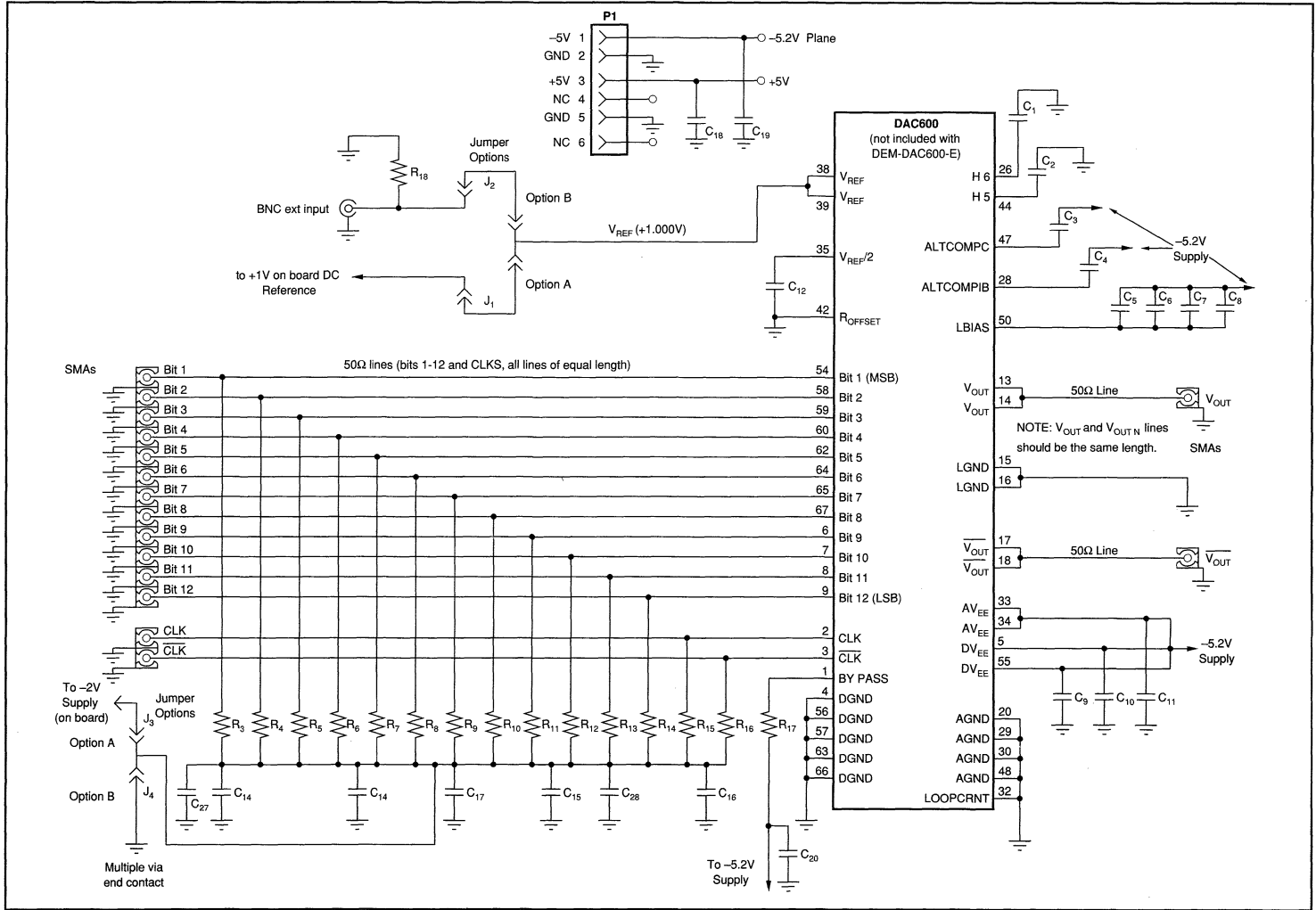

FIGURE 1. ECL Drive Gate Termination.

DEM-DAC600

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For Immediate Assistance, Contact Your Local Salesperson

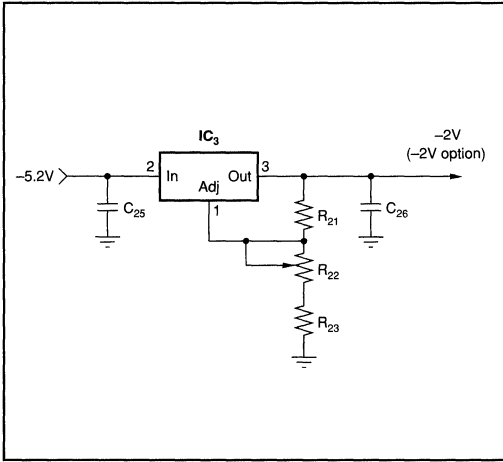FIGURE 2. DEM-DAC600-E Schematic.

FIGURE 3. –2.0V Pull-Down Supply for Digital Inputs (on-board).
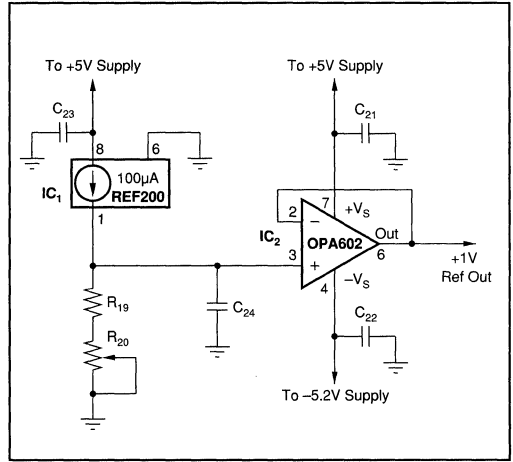
FIGURE 4. DEM-DAC600-E On-Board +1.0V Reference Circuit.

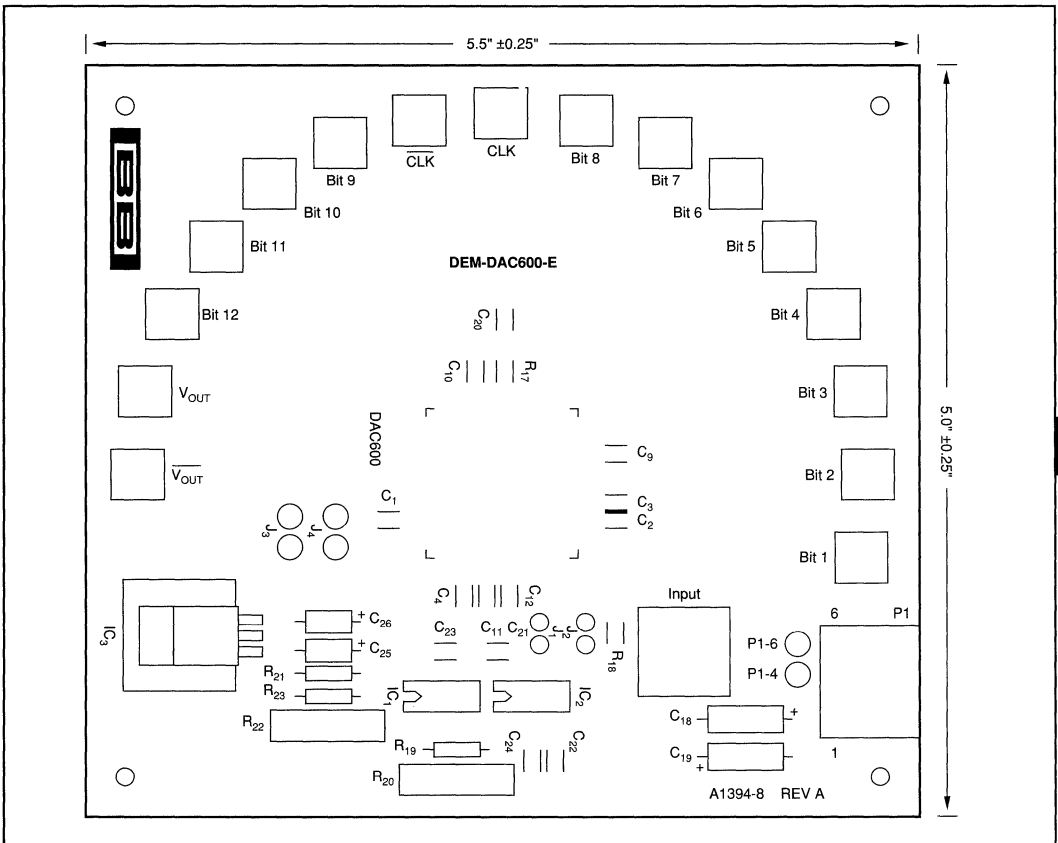FIGURE 5. DEM-600-E Component Placement.

DEM-DAC600

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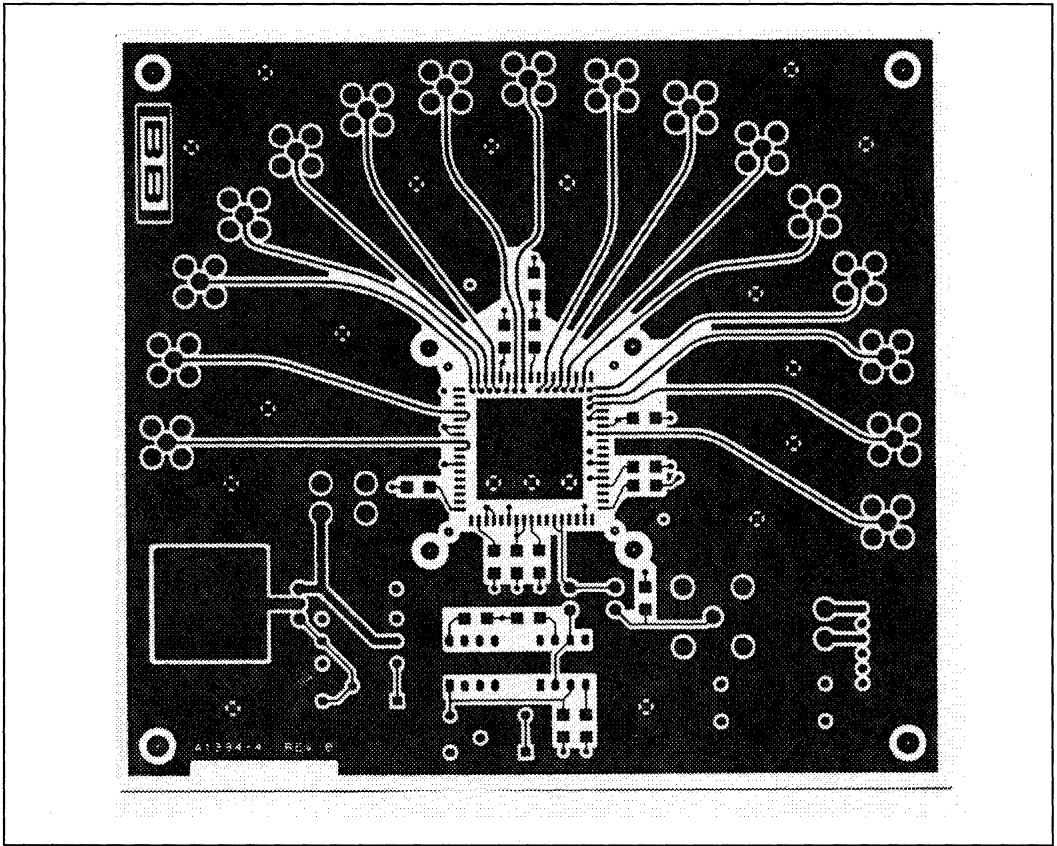
FIGURE 6. Signal Layer (Top Layer).
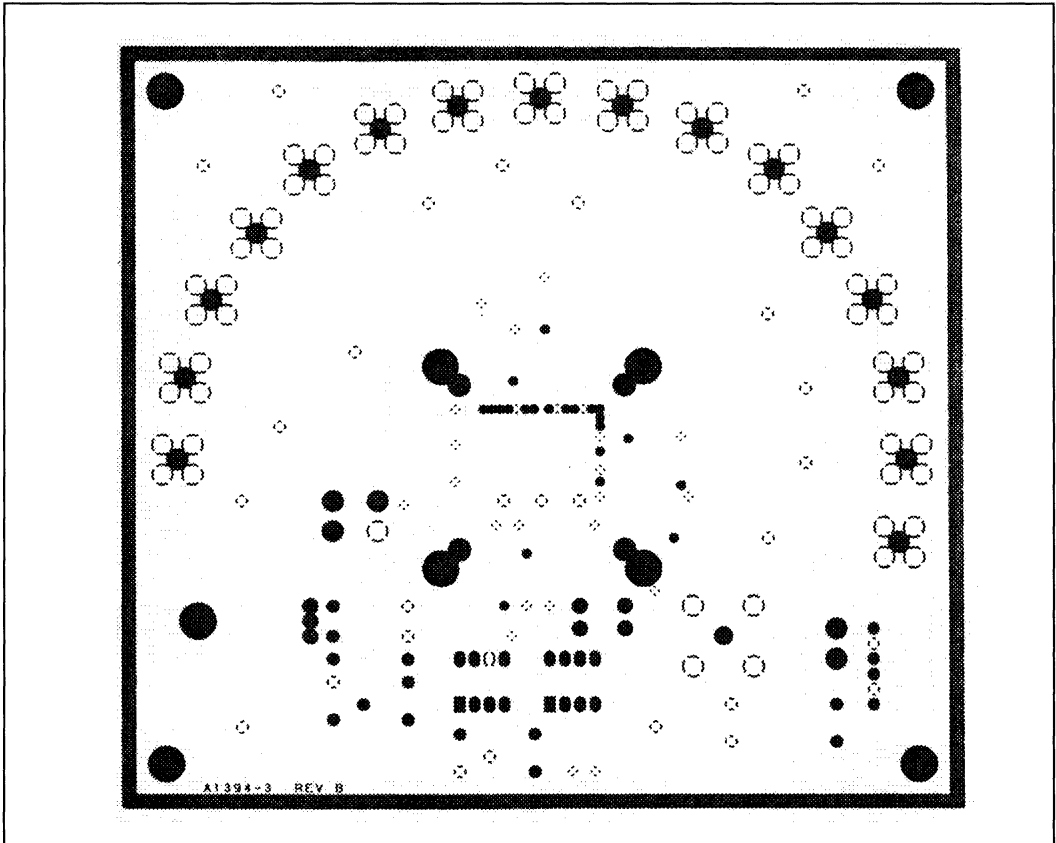
FIGURE 7. Analog Ground Plane (Layer 2).

DEM-DAC600

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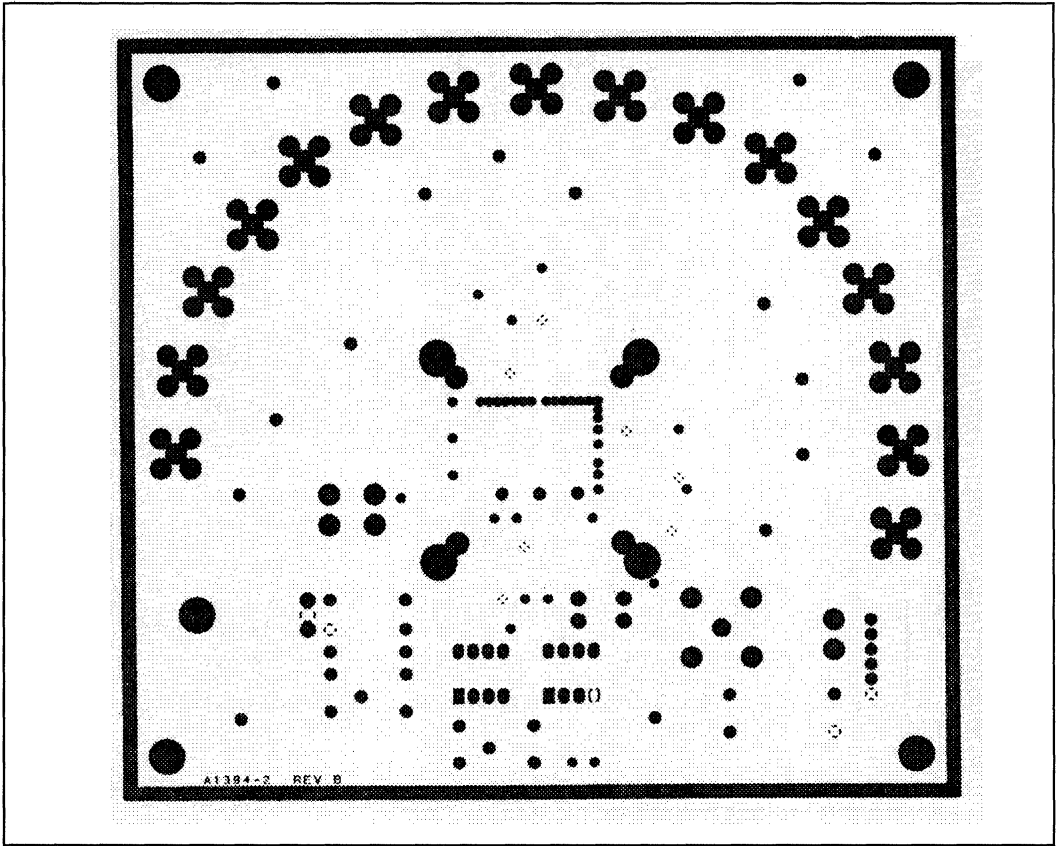
FIGURE 8. –5.2V Power Plane (Layer 3).
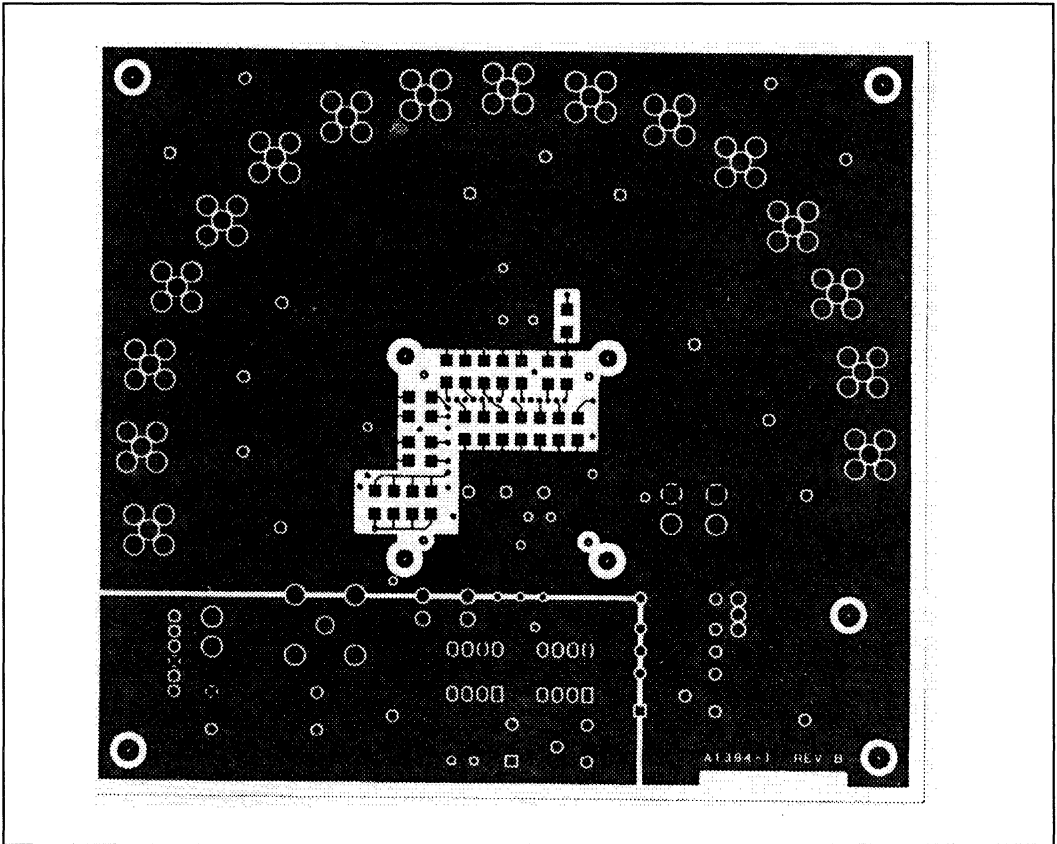
FIGURE 9. –2V Supply Plane (Large Area) and +5V Supply Plane (Layer 4).

DEM-DAC600

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DEM-DAI1710
EVALUTION FIXTURE FOR
PCM1710 WITH DAI INTERFACE
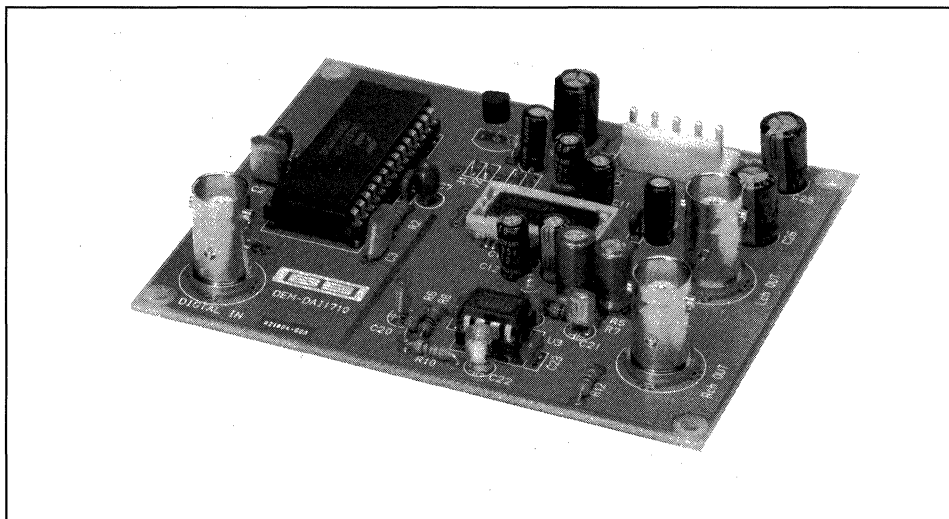
FEATURES

- **NEWLY DESIGNED MULTI-LEVEL $\Delta\Sigma$ ARCHITECTURE DAC: PCM1710U**
- **STANDARD DIGITAL AUDIO INTERFACE COAX/BNC CONNECTOR INPUT**
- **SAMPLING RATE: 32kHz/44.1kHz/48kHz**
- **SUPERIOR DYNAMIC PERFORMANCE**
- **2nd-ORDER ACTIVE LPF (fc = 24kHz)**
- **STEREO VOLTAGE OUTPUT: 2Vrms**
- **POWER SUPPLY: +5V, ±5V to ±15V**
- **BOARD SIZE: 3.94" x 3.15" (100mm x 80mm)**

DESCRIPTION

The DEM-DAI1710 is a fully assembled, PCM1710 included, printed circuit board for evaluation of the PCM1710U, dual $\Delta\Sigma$ 20-bit audio Digital-to-Analog converter. The DEM-DAI1710 includes a Digital Audio Interface (DAI) receiver chip for ease of use and to provide the 256fs system clock to the PCM1710. Also included are dual 2nd-order lowpass output filters, employing Burr-Brown's OPA2604 dual FET Op Amp, which outputs stereo 2Vrms signals at the output BNC connectors.

All of the many features of the PCM1710 can be evaluated by using the DEM-DAI1710 jumper selections. The DEM-DAI1710 requires +5V and ±5V to ±15V power supplies.

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OPERATIONAL CONDITIONS OF THE PCM1710

The DEM-DAI1710 accepts standard digital audio interface format from the on-board DAI receiver IC.

By Interface to DAI receiver IC (CS8412), operational conditions of the PCM1710 are selected to as follows:

• Parallel Mode/Normal Speed

• 16-bit Normal Interface

• 256fs System Clock Operation

Figure 1 shows selected conditions by Jumpers J1 thru J4. By changing jumper select, the PCM1710 can be operated in its other modes.
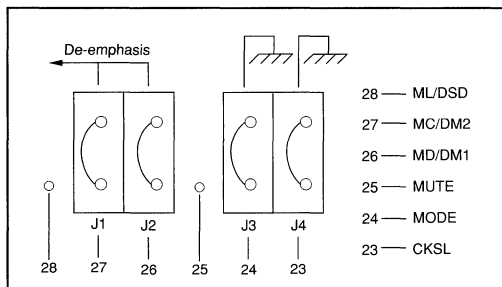
FIGURE 1. Jumper Function.

ELECTRICAL PERFORMANCE

DIGITAL SECTION
Digital Interface: Standard Digital Audio Interface
Digital Input: Coax/BNC Connector, 75Ω
Sample Rate: 32kHz/44.1kHz/48kHz
System Clock: 256fs

ANALOG SECTION
THD + N at F/S: –92dB typ (with 20kHz LPF)
–70dB typ (with 30kHz LPF)
S/N Ratio: 108dB typ (ELAJ, A-weighted)
Dynamic Range: 98dB typ (ELAJ, A-weighted)
Analog Output: 2Vrms
De-emphasis Error: ±0.1dB (fs: 44.1kHz)

POWER SUPPLY REQUIREMENTS
+V_{CC}: +4.75V to +5.25V
+I_{CC}: +60mA typ, +120mA max
±V_S: ±5V to ±15V
±I_S: ±15mA max

TEST CONDITIONS

The DEM-DAI1710 has 2nd-order active LPF (fc = 24kHz) on board. However, by sampling theory, the noise spectrum out of the audio band still remains.

Figure 3 shows test block diagram of the DEM-DAI1710, using a 20kHz LPF to reduce noise spectrum out of the audio band.

Typical THD + N performance with 20kHz LPF is –92dB, without 20kHz LPF (with 30kHz LPF on THD meter) is –70dB.

BLOCK DIAGRAM

FIGURE 2. Block Diagram of the DEM-DAI1710.
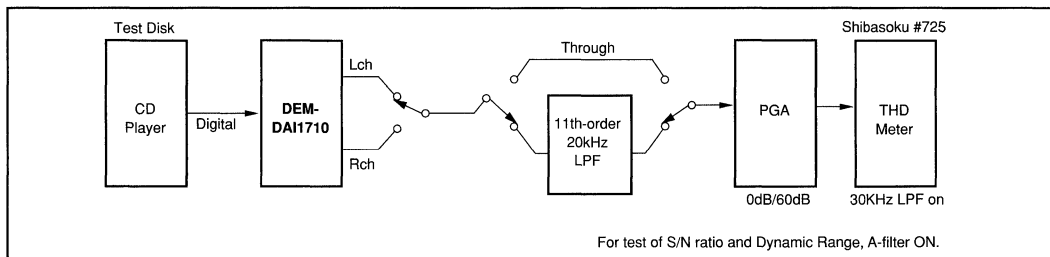
FIGURE 3. Test Block Diagram.

DEM-DAI1710

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SCHEMATIC CIRCUIT DIAGRAM

CN — GND +V$_{CC}$ –V$_S$ GND +V$_S$

C$_{27}$ 100µF   C$_{26}$ 100µF   C$_{25}$ 100µF
R$_{15}$ 10kΩ   R$_{14}$ 10kΩ   R$_{13}$ 10kΩ
+5V V$_{CC}$ –V$_S$ +V$_S$

+5V V$_{CC}$

U1
CS8412CP
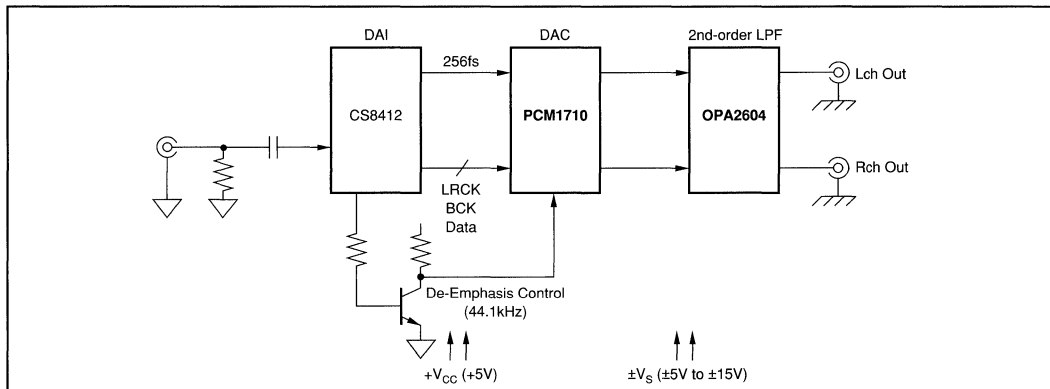C$_C$/FO   SDATA
M1
+V$_D$
DGND
RXP   AGND
RXN   FRT
FSYNC   MCK
SCK
CS12/FCK   M3

C$_4$ 10µF   C$_5$ 0.1µF
C$_6$ 0.1µF   C$_7$ 10µF
+V$_A$
C$_1$ 0.047µF
C$_2$ 0.047µF
Digital In
R$_1$ 75Ω
R$_2$ 1KΩ
C$_3$ 0.047µF

U2
PCM1710U
LRCIN   ML/DSD
DIN   MC/DM2
BCKIN   MD/DM1
CLCKO   MUTE
XTI   MODE
XTO   CKSL
DGND   DGND
V$_{DD}$ V$_{DD}$
V$_{CC2R}$ V$_{CC2L}$
AGND2R   AGND2L
EXT1R   EXT1L
EXT2R   EXT2L
V$_{OUTR}$ V$_{OUTL}$
AGND1   V$_{CC1}$

J1 J2 J3 J4

+5V V$_{CC}$
R$_3$ 10kΩ
R$_4$ 10kΩ
C$_{16}$ 10µF
Q1
C1815 or equivalent

C$_{12}$ +10µF   C$_{13}$ 0.1µF
C$_{14}$ 0.1µF   C$_{15}$ 10µF
C$_{10}$ 10µF
C$_{11}$ 10µF
C$_8$ 10µF   C$_9$ 0.1µF

+V$_S$
C$_{23}$ 0.1µF

C$_{18}$ 4.7µF
R$_8$ 10kΩ
C$_{22}$ 330pF
R$_6$ 5.6kΩ   R$_{10}$ 3.9kΩ
R$_{12}$ 100Ω
C$_{20}$ 2700pF
1/2 U3
OPA2604
Rch Out

C$_{17}$ 4.7µF
R$_7$ 10kΩ
C$_{21}$ 330pF
R$_5$ 5.6kΩ   R$_9$ 3.9kΩ
R$_{11}$ 100Ω
C$_{19}$ 2700pF
1/2 U3
OPA2604
C$_{24}$ 0.1µF
Lch Out

–V$_S$

TYPICAL PERFORMANCE

FIGURE 4a. –60dB Output spectrum (f = 1kHz. BW = 100kHz).
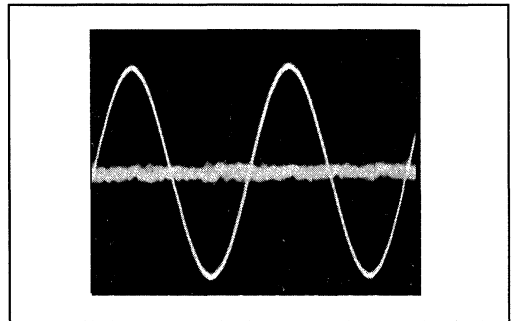
FIGURE 4b. –60dB Output (f = 1kHz). Signal waveform and distortion waveform. THD + N = 1.2%.

PC BOARD LAYOUT
Parts Location
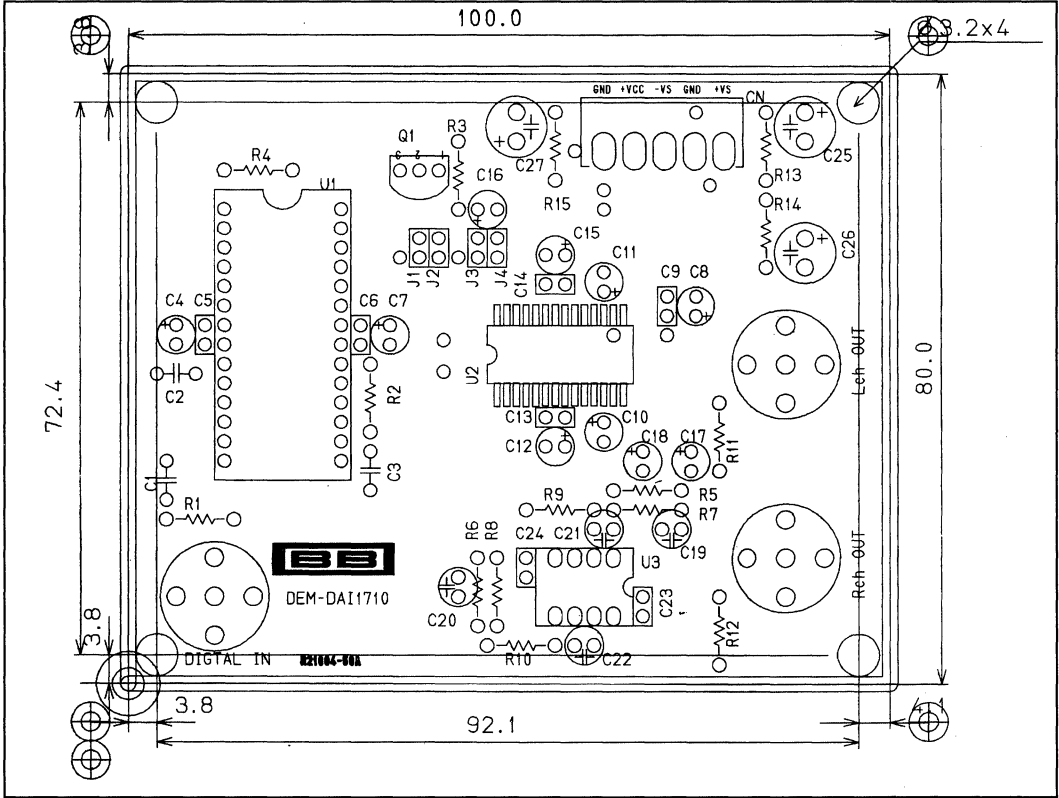
Top View
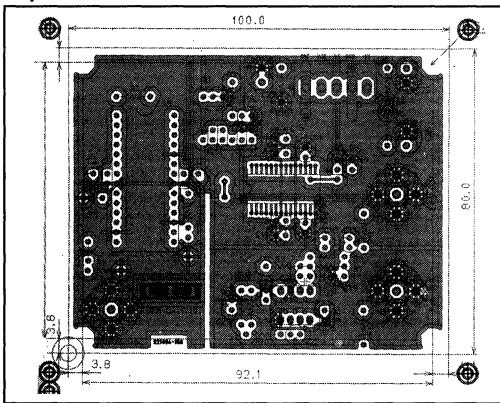
Bottom View
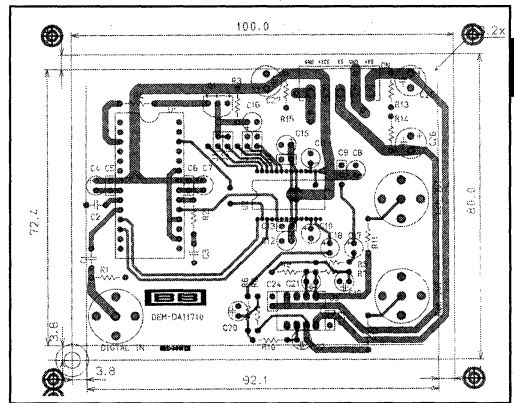
DEM-DAI1710

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DEM-OPA64x
EVALUATION FIXTURES
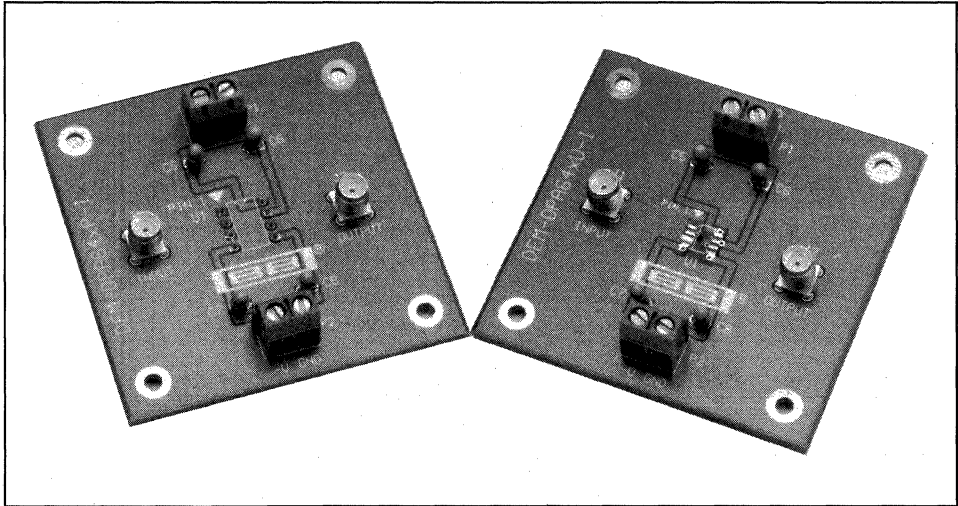
FEATURES

● **SOIC AND DIP VERSIONS**

● **SURFACE MOUNT COMPONENTS FOR OPTIMUM PERFORMANCE**

● **SMA INPUT AND OUTPUT JACKS FOR MAXIMUM FREQUENCY RESPONSE**

● **2.5" X 2.5" DIMENSIONS**

● **DIP WITH PIN SOCKETS**
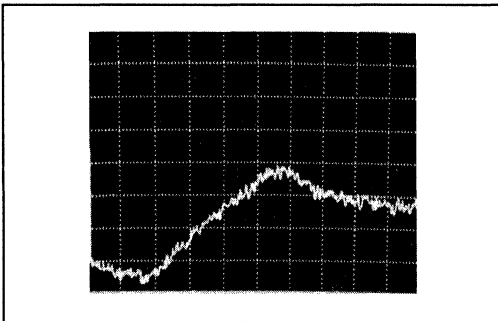
● **UNIVERSAL POWER SUPPLY CONNECTIONS**

● **INPUT AND OUTPUT TERMINATION INCLUDED**

APPLICATIONS

● **EVALUATE OPA64xU (SOIC) AND OPA64xP (DIP) PERFORMANCE**

● **EVALUATE HIGH-FREQUENCY, TWO LAYER PCB LAYOUT**

● **INCOMING INSPECTION TEST FIXTURE**

DESCRIPTION

The DEM-OPA64x evaluation fixtures are fully as-
sembled printed circuit boards, except for the gain
setting resistors, which are included. There are six
different layouts—three for SOICs and three for DIPs.
The three layouts are optimized for different circuits,
which include a voltage follower, an inverting and a
non-inverting configuration.

These demonstration boards are used to evaluate the
Burr-Brown OPA64x series of operational amplifiers.
Operational amplifiers are not included with the DEM-
OPA64x. These demonstration boards incorporate
surface-mount resistors and surface-mount ceramic
bypass capacitors. The feedback resistor is placed
directly between the input and output pins. This is
necessary to achieve greater than 500MHz bandwidth
performance. The size of the circuit traces and feed-
throughs are minimized to reduce parasitic capaci-
tance, and separate bypass capacitors are placed
directly at each of the four power pins to maintain low
harmonic distortion.

The fixture requires a bipolar ±5V power supply.
Separate power supply paths are required for each

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power pin to achieve low even-order harmonic distortion. This approach minimizes non-linear output stage currents coupling into the input gain stages. The orientation of the power traces and the ceramic bypass capacitors have been empirically determined to give the best harmonic distortion. The connection from the top side of the board to the bottom was made as short as possible. Wide power supply traces are recommended to reduce series impedance at high frequencies.

Solid ground planes are used on both sides of the board and are connected solidly together. The ground plane is removed around the feedback resistor and signal paths to reduce parasitic capacitance and ground plane noise coupling.

ORDERING INFORMATION

PART NUMBER	PACKAGE	CIRCUIT CONFIGURATION
DEM-OPA640xU-F	SOIC	Voltage Follower
DEM-OPA64xU-I	SOIC	Inverting
DEM-OPA64xU-N	SOIC	Non-Inverting
DEM-OPA64xP-F	DIP	Voltage Follower
DEM-OPA64xP-I	DIP	Inverting
DEM-OPA64xP-N	DIP	Non-Inverting

COMPONENT LIST

REF. DES.	QUANTITY	PART NUMBER	DESCRIPTION	MANUFACTURER
C_{1-4}	4	C1206C104M5UAC	0.1µF 50V X7R Ceramic Capacitor	Kemet
C_{5-8}	4	TAP225K025SCS	2.2µF 25V Tantalum Capacitor	AVX
$P_{1,2}$	2	ED500/2DS	2-Pin Power Block	On-Shore Technology
$J_{1,2}$	2	9650-1111-0000	PCB Mount SMA Connector	AEP
	5	CRCW1206000ZT	0Ω 1206 Chip Resistor	Dale
	5	CRCW12061000FT	100Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW12062000FT	200Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW120624R9FT	24.9Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW120644R2FT	44.2Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW120649R9FT	49.9Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW120656R2FT	56.2Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW120666R5FT	66.5Ω 1206 Chip Resistor, 1% MF	Dale
	5	CRCW12064020FT	402Ω 1206 Chip Resistor, 1% MF	Dale
	1	PPCDIP-308-710C	8-Pin Socket	McKenzie
	1		Printed Circuit Board	

DEM-OPA64x

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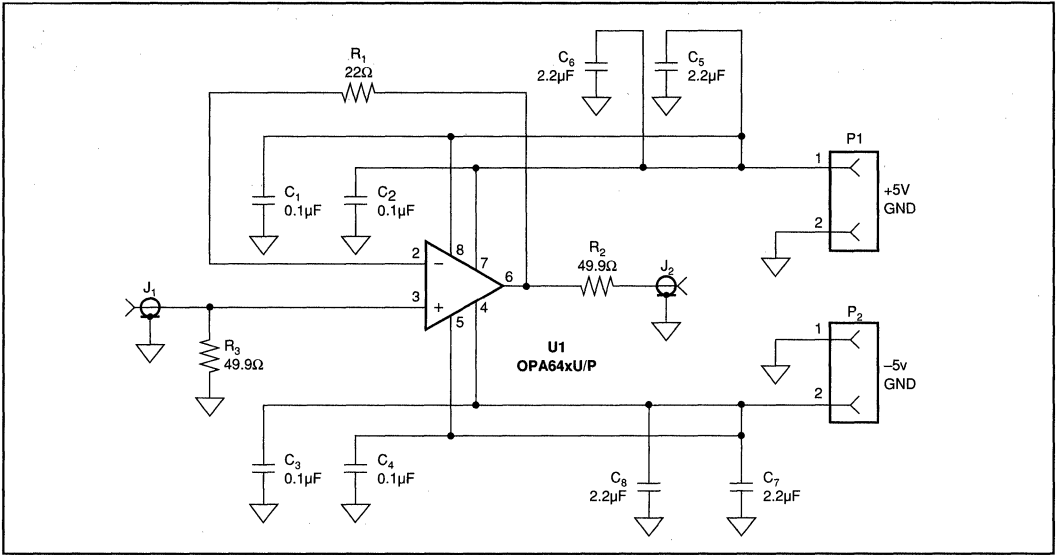
FIGURE 1. DEM-OPA64xU/P-F Voltage Follower.
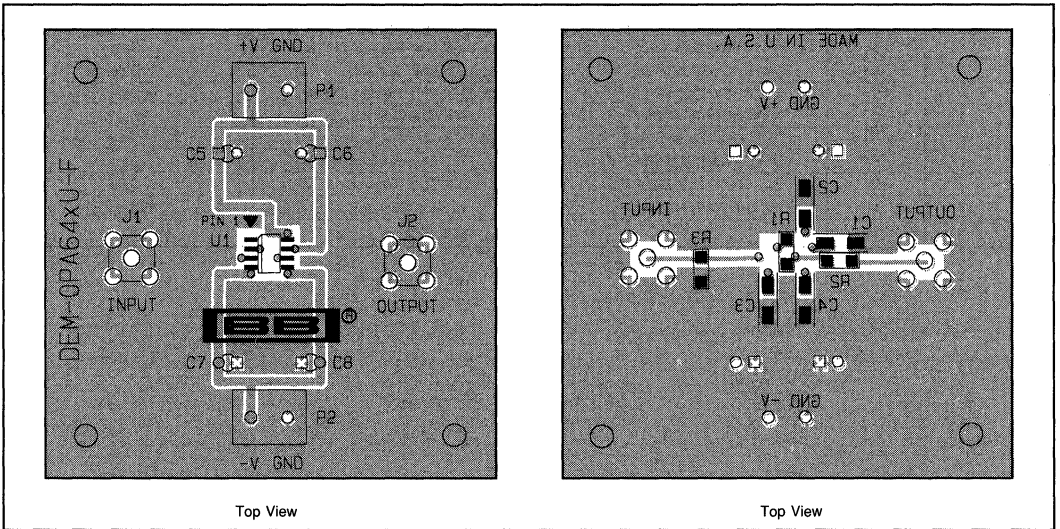
FIGURE 2. DEM-OPA64xU-F. The layout shown is 1.2x actual for clarity.
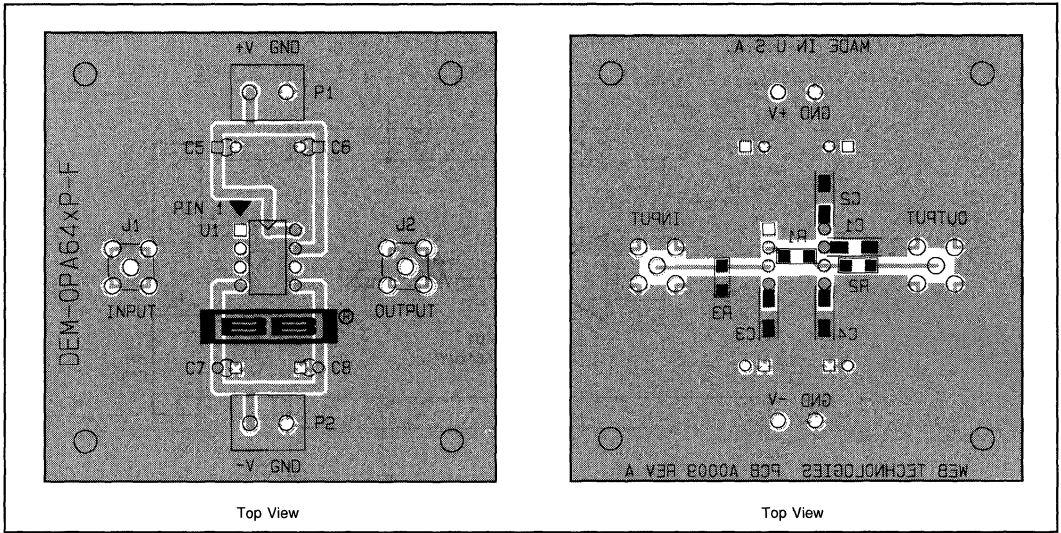
FIGURE 3. DEM-OPA64xP-F. The layout shown is 1.2x actual for clarity.

DEM-OPA64x

A
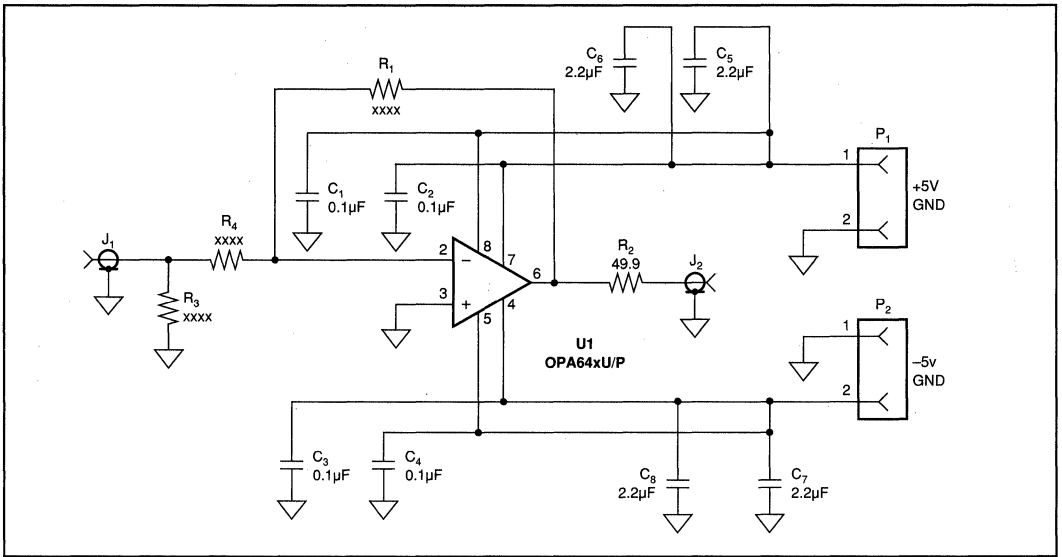
FIGURE 4. DEM-OPA64xU/P-I Inverting.
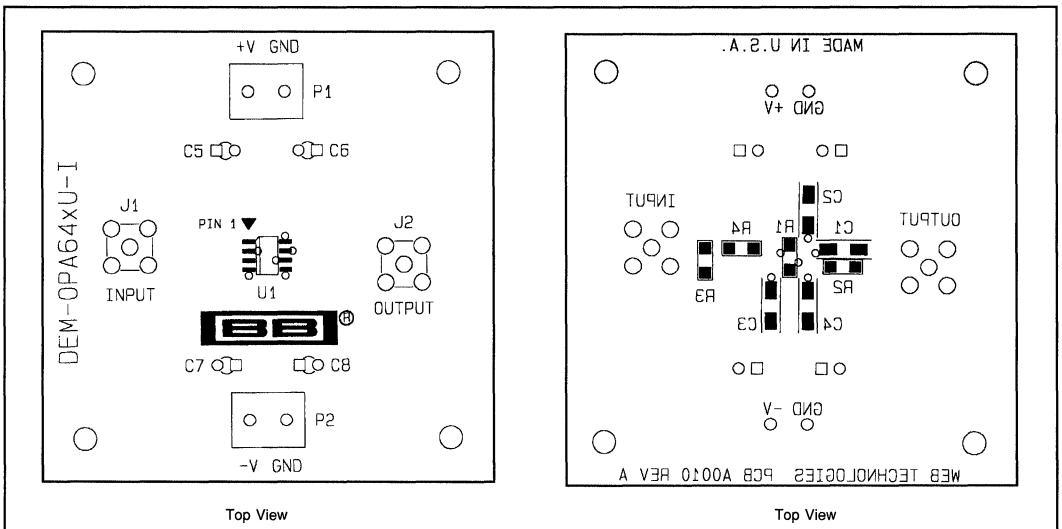
FIGURE 5. DEM-OPA64xU-I. The layout shown is 1.2x actual for clarity.
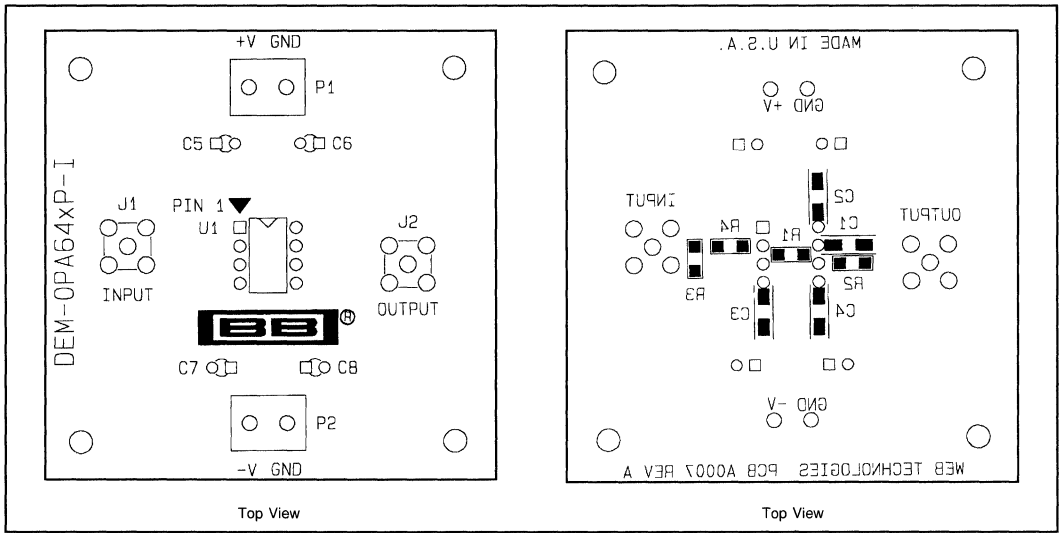
FIGURE 6. DEM-OPA64xP-I. The layout shown is 1.2x actual for clarity.

DEM-OPA64x

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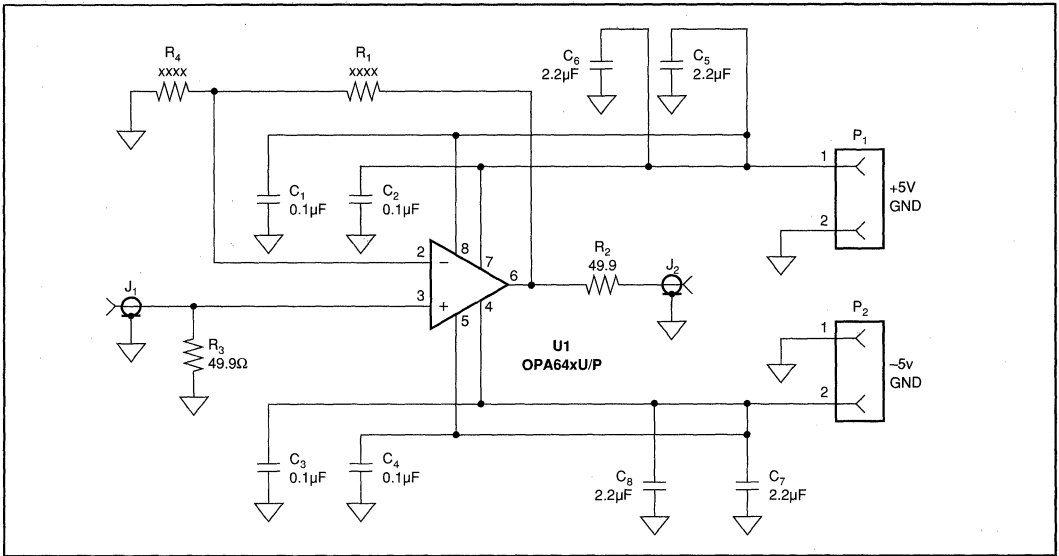
FIGURE 7. DEM-OPA64xU/P-N Non-Inverting.

Top View   Top View
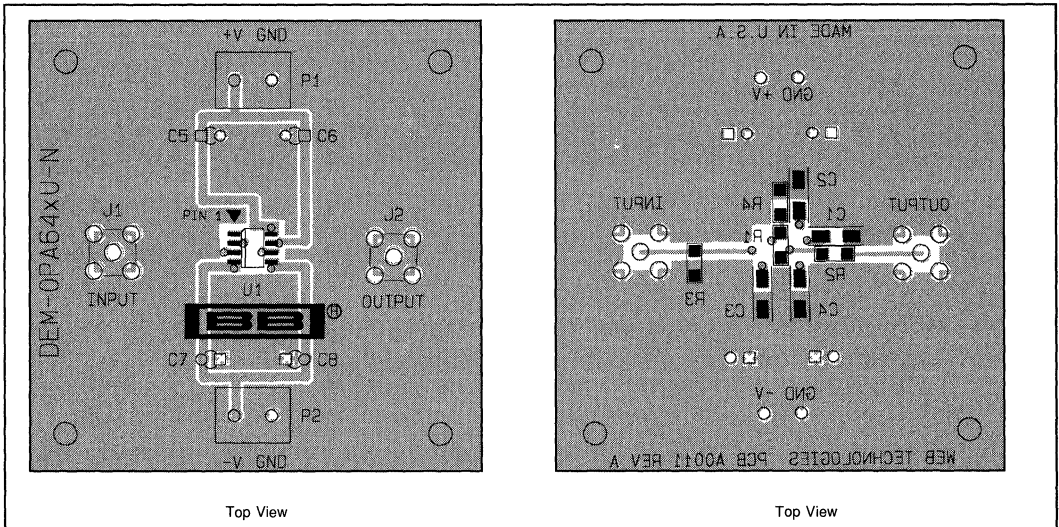
FIGURE 8. DEM-OPA64xU-N. The layout shown is 1.2x actual for clarity.

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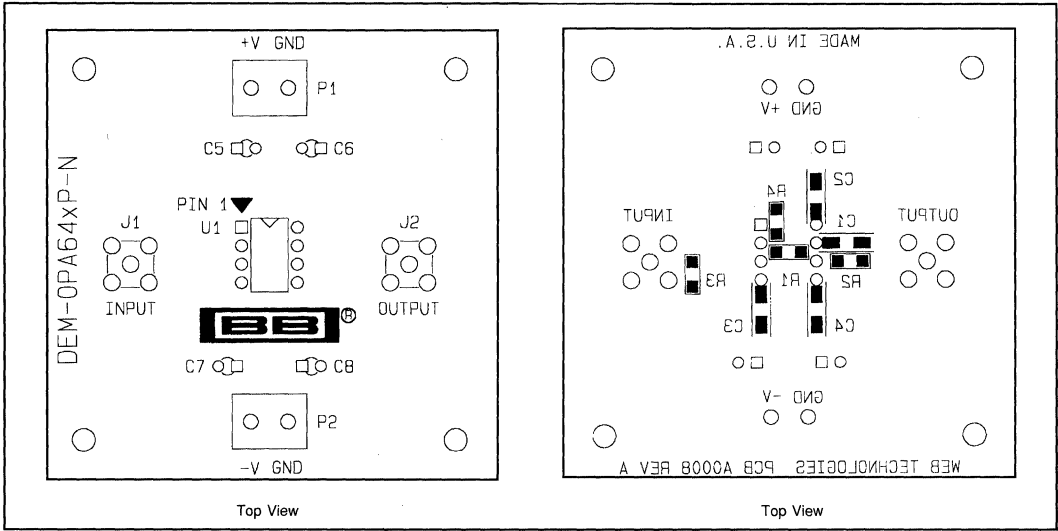
FIGURE 9. DEM-OPA64xP-N. The layout shown is 1.2x actual for clarity.

DEM-OPA64x

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**DEM-PCM1702
EVALUATION FIXTURE**
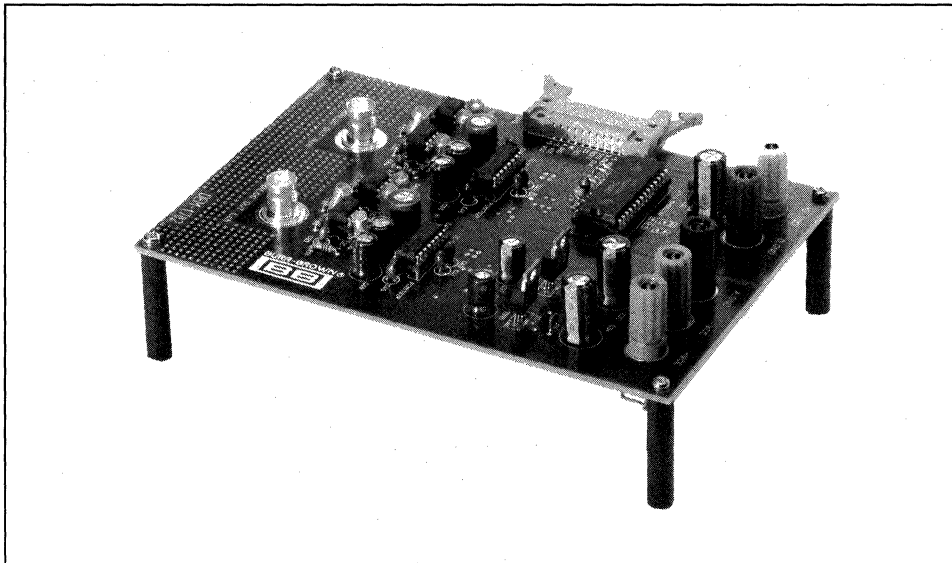
FEATURES

● **COMPLETE 20-BIT STEREO
  D/A CONVERSION SYSTEM**
● **NEW SIGN-MAGNITUDE DAC: PCM1702P**
● **8x DIGITAL FILTER: SM5842AP**
● **HIGH PERFORMANCE
  THD+N at (F/S): 0.0015%
  Dynamic Range: 108dB (EIAJ)
  S/N Ratio: 120dB (EIAJ)
  Non Zero Cross Distortion**
● **SERIAL DIGITAL INTERFACE**
● **ANALOG OUTPUT: ±3V**
● **POWER SUPPLY: ±9V to ±12V, +5V**
● **DIRECT INTERFACE TO DEM-PCM1760**
● **BOARD SIZE: 182mm X 128mm**

DESCRIPTION

The DEM-PCM1702 is an evaluation fixture for Burr-Brown's sign-magnitude, 20-bit digital-to-analog converter, the PCM-1702. It is primarily intended for quick evaluation of the PCM1702P's spectral purity and sound fidelity.

Two PCM1702s are provided to allow full stereo evaluation. The input to the DEM-PCM1702 can be the output serial data from DEM-PCM1760 (Burr-Brown's evaluation fixture for its 20-bit A/D and digital filter, the PCM1760 and DF1760), or other digital signal source through the interface connector.

The number of digital input data bits and optional functions are selectable by switches on board.

The analog output signal is filtered by a GIC type low pass filter (dual OP AMP) and the filtered output appears on the output connectors (BNCs).

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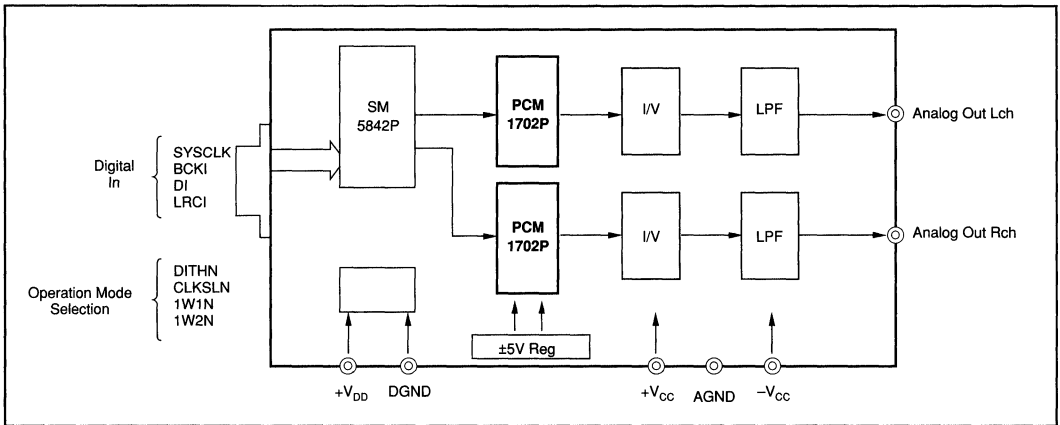
FIGURE 1. Block Diagram of the DEM-PCM1702.
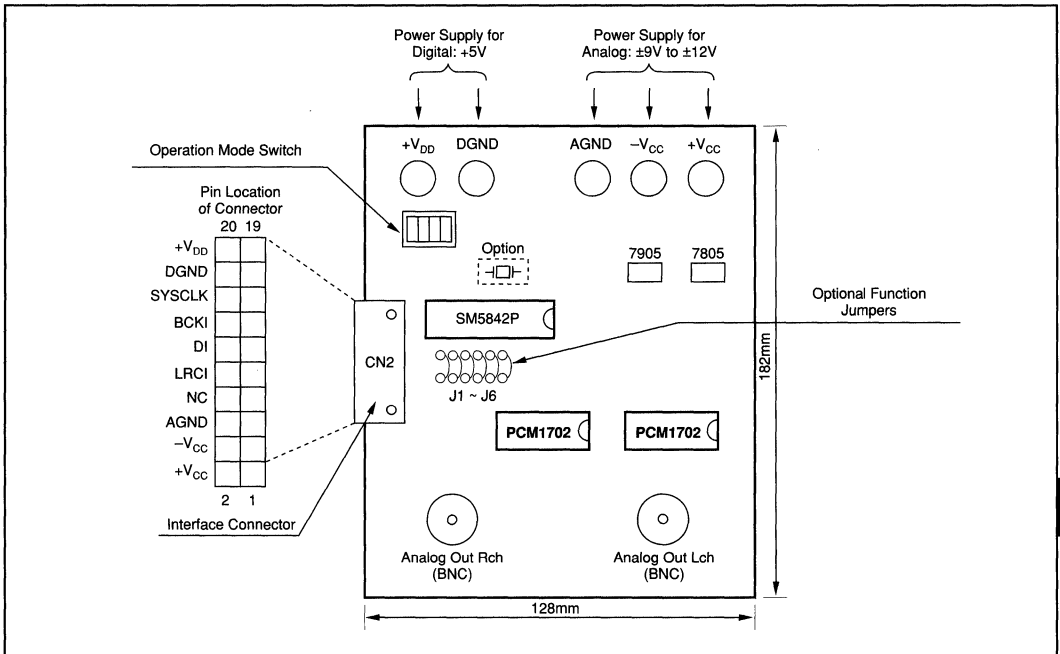
FIGURE 2. Component Location and Function.

DEM-PCM1702

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OPERATION MODE SELECT SWITCH

The Operation Mode Select switch provides for the selection of dither, system clock and input format as described in the tables below.

NAME	FUNCTION	L	H
DITHN	Dither Select	Dither On	Dither Off
CLKSL	System Clock Select	256fs	384fs
1W1N (2N)	Input Format Select	Table of Below	

INPUT FORMAT	1W1N	1W2N
MSB First, Right-justified, 16-Bit	H	H
MSB First, Right-justified, 18-Bit	L	H
MSB First, Right-justified, 20-Bit	H	L
MSB First, Right-justified, 24-Bit	L	L

For detailed timing infomation, see the data sheet for the NPC SM5842AP.

From the factory, these switches are set to provide for no dither, system clock equal 256fs and data format set for MSB first, right justified, 20-bit, as shown below.
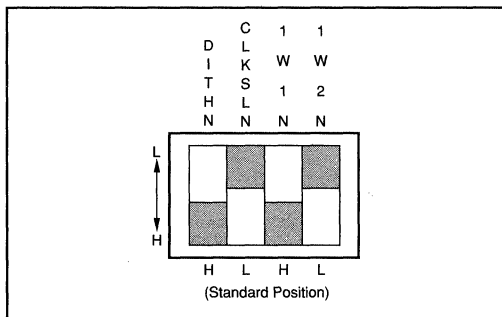
FIGURE 3. Opeeration Mode Select Switch.

OPTIONAL FUNCTION JUMPERS

The optional functions of right and left channel de-emphasis, the de-emphasis system clock, and right and left channel mute are controlled by jumpers J1 through J6 as shown in the following table.

JUMPER #	FUNCTION	JUMPER	NO JUMPER
J1	De-emphasis, Rch	OFF	ON
J2	De-emphasis, Lch	OFF	ON
J3	De-emphasis, fs-32kHz		X
J4	De-emphasis, fs-32kHz		X
J3	De-emphasis, fs-41.4kHz	X	
J4	De-emphasis, fs-41.4kHz	X	
J3	De-emphasis, fs-48kHz	X	
J4	De-emphasis, fs-48kHz		X
J5	Mute, Rch	No Mute	Mute
J6	Mute, Lch	No Mute	Mute

From the factory, Jumpers J1, J2, J5 and J6 are installed, as shown below, setting the system clock at 32kHz, no de-emphasis and no mute.
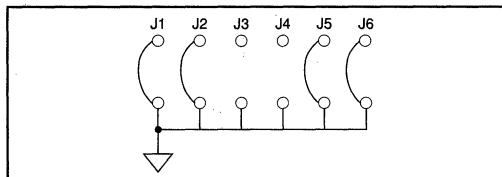
FIGURE 4. Optional Function Jumpers.

SYSTEM CLOCK OPERATION

A system clock (SYSCLK) is required for operation of the DEM-PCM1702. If the DEM-PCM1702 is being used with the DEM-PCM1760, the 256fs or 384fs system clock is provided by the DEM-PCM1760 through pin 16 of the Interface Connector, as described below. (NOTE: Care must be taken to insure both boards are set to the same master clock.)

If the DEM-PCM1702 is being used where it must generate the 256fs or 384fs master clock, the appropriate crystal can be connected to the SM5842.

COMBINATION WITH DEM-PCM1760

The DEM-PCM1702 can be directly combined with the DEM-PCM1760 (20-bit stereo A/D conversion system).

In this case, the connector pins of the DEM-PCM1702 and the DEM-PCM1760 are connected directly together.

The power supply for the DEM-PCM1760 is provided by the DEM-PCM1702 and the serial digital data (within system clock) is provided to the DEM-PCM1702 from the DEM-PCM1760.
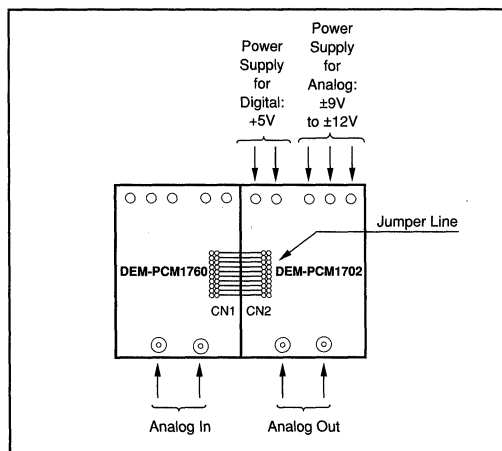
FIGURE 5. Combination with DEM-PCM1760.
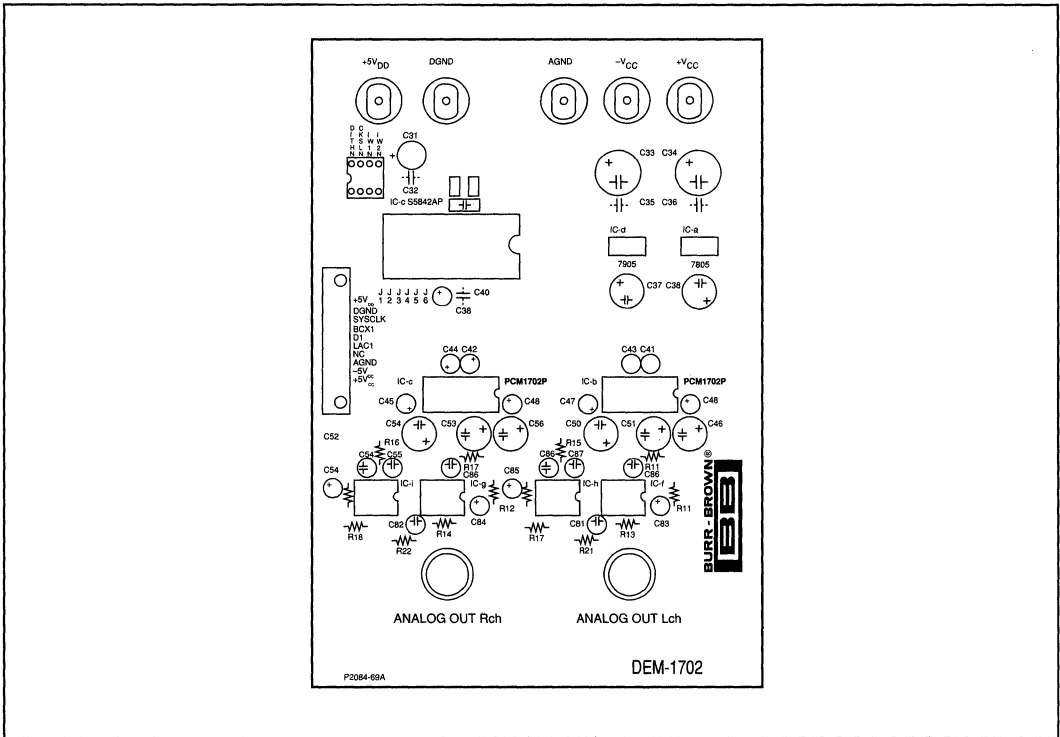
FIGURE 6. DEM-PCM1702 Board Layout and Component Location.

DEM-PCM1702

A
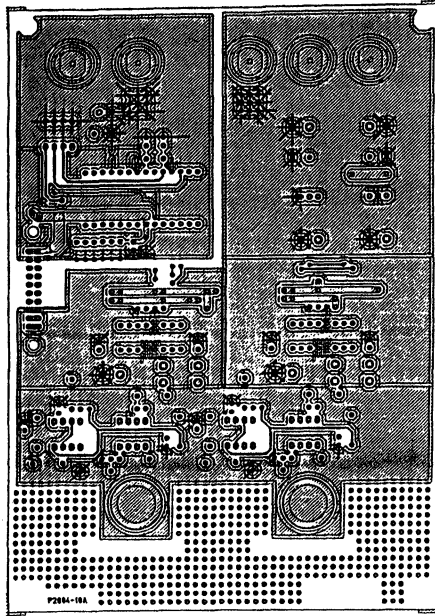
TOP

BOTTOM

FIGURE 7. DEM-PCM1702 Layer 1 and Layer 2.

Burr-Brown IC Data Book—Data Conversion Products

FIGURE 8. DEM-PCM1702 Circuit Diagram.

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DEM-PCM1702

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DEM-PCM1710
EVALUATION FIXTURE
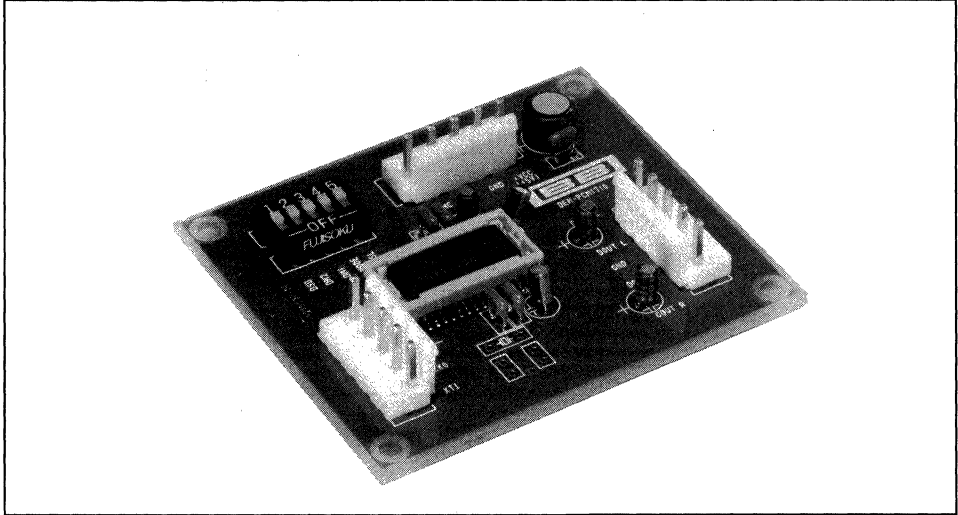
FEATURES

● **DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER**

● **HIGH PERFORMANCE: THD+N: 0.0025%**
  Dynamic Range: 98dB typ
  S/N Ratio: 110dB typ

● **ANALOG VOLTAGE OUTPUT: V_o = 3.2Vp-p**

● **ON-CHIP POST ANALOG LOW PASS FILTER**

● **SYSTEM CLOCK 256fs or 384fs**

● **ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH:**
  Soft Mute and Attenuator
  Digital De-Emphasis
  Double Speed Dubbing Mode

● **SINGLE +5V POWER SUPPLY**

DESCRIPTION

The DEM-PCM1710 is an evaluation fixture for the PCM1710 (16/20-bit stereo digital-to-analog converter with on-chip digital filter) primarily intended for quick evaluation of the PCM1710's performance.

The DEM-PCM1710 is capable of either serial or parallel output, can accept either an external system clock (256fs or 384fs) or a user-installed crystal oscillator. Other digital input signals are: LRCK, BCK, and DATA.

All of the functions of the PCM1710 (De-Emphasis, Mute, Double Speed) can be easily controlled by on-board switches.

Power supply requirement is +5V only.

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BLOCK DIAGRAM

COMPONENT LOCATION AND FUNCTION

NOTE: See Burr-Brown data sheet for PCM1710U (PDS-1217) for complete operation description and instructions for the PCM1710U.
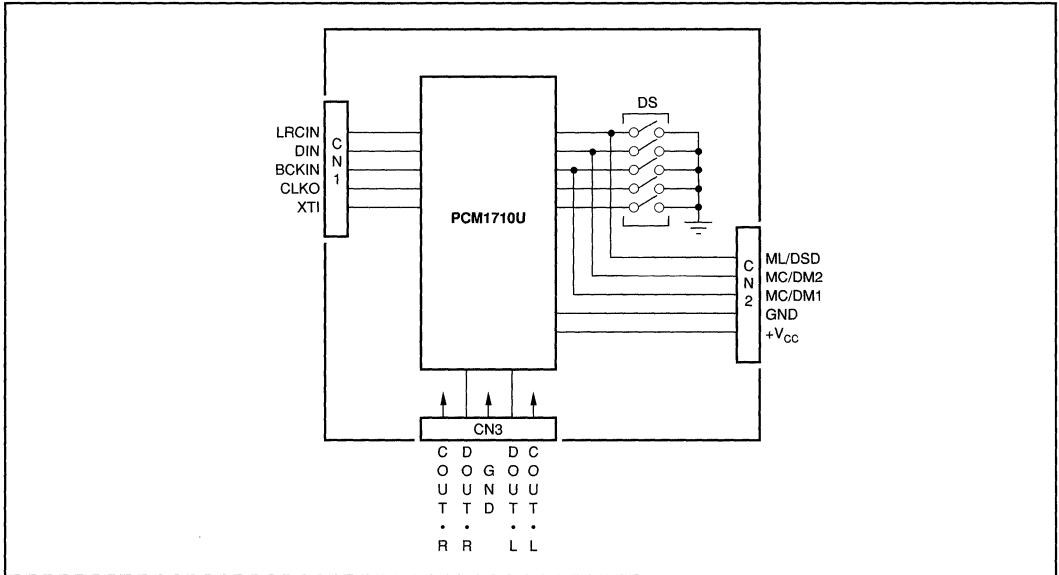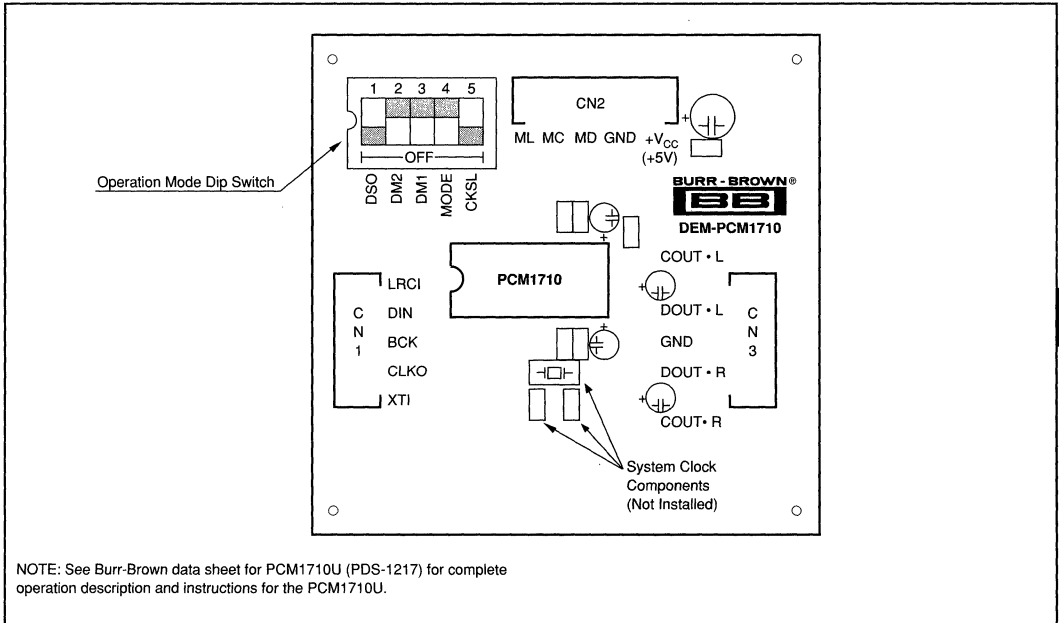
DEM-PCM1710

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CIRCUIT DIAGRAM
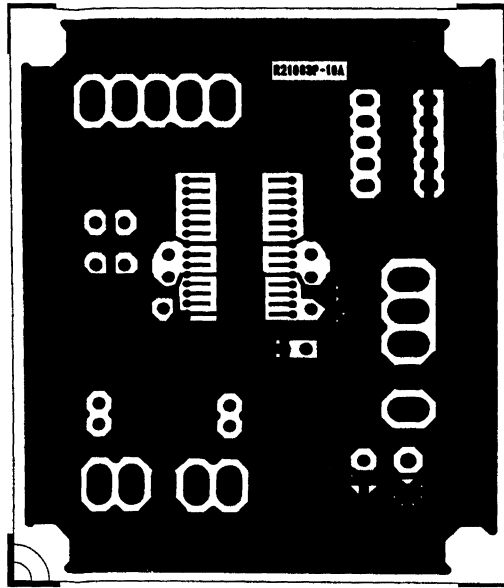
NOTE: (1) Bypass Capacitor.

PATTERN LAYOUT

TOP

BOTTOM

DEM-PCM1710

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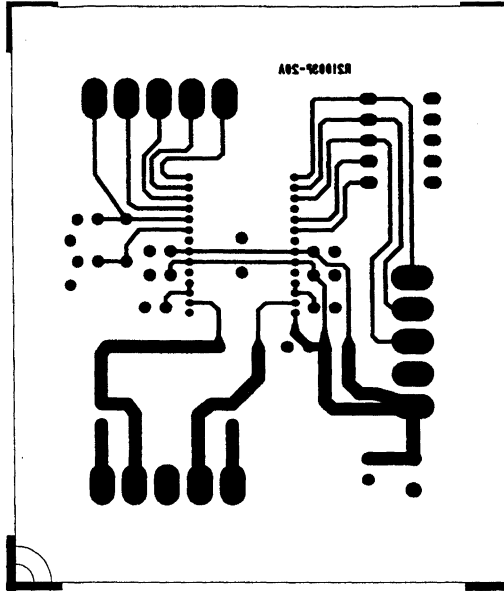
DEM-PCM1760
EVALUATION FIXTURE

FEATURES

● **COMPLETE 20-BIT STEREO A/D CONVERSION SYSTEM**

● **20-BIT A/D CONVERTER: PCM1760**

● **HIGH PERFORMANCE DIGITAL FILTER: DF1760**

● **SERIAL DIGITAL INTERFACE**

● **HIGH PERFORMANCE**
   THD+N (F/S): 0.0015%
   Dynamic Range: 108dB (EIAJ)
   S/N Ratio: 108dB (EIAJ)

● **ANALOG INPUT: ±2.5V**

● **POWER SUPPLY: ±5V, +5V**

● **DIRECT INTERFACE TO DEM-PCM1702**

● **BOARD SIZE: 182mm x 128mm**

DESCRIPTION

The DEM-PCM1760 is an evaluation fixture for the PCM1760/DF1760 (20-bit stereo analog-to-digital conversion system) primarily intended for quick evaluation of the PCM1760/DF1760's spectral purity and sound fidelity.

The PCM1760 is provided for evaluation with ±5V analog power supply and the DF1760 is provided for evaluation with +5V digital power supply.

The input to the DEM-PCM1760 is ±2.5V full scale analog signal and output from the DEM-PCM1760 is a serial digital interface signal consisting of SYSCLK, SCLK, SDATA, and L/R.

The output digital data format is selectable and the operation mode is also selectable by function switches on the board.

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BLOCK DIAGRAM

COMPONENT LOCATION AND FUNCTION

DEM-PCM1760

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NAME	FUNCTION	H	L
CLKSEL	Master Clock Select	265fs	384fs
S/M	Slave/Master Select	Slave	Master
M1, M2	Output Format	Table of Below	

OUTPUT FORMAT	M1	M2
MSB First, 16-Bit, Falling Edge	H	H
MSB First, 20-Bit, Falling Edge	L	H
MSB First, 20-Bit, Rising Edge	H	L
MSB First, 20-Bit, Falling Edge	L	L

NOTE: The detailed timing information of output format is referred to the data sheet of PCM1760/DF1760.
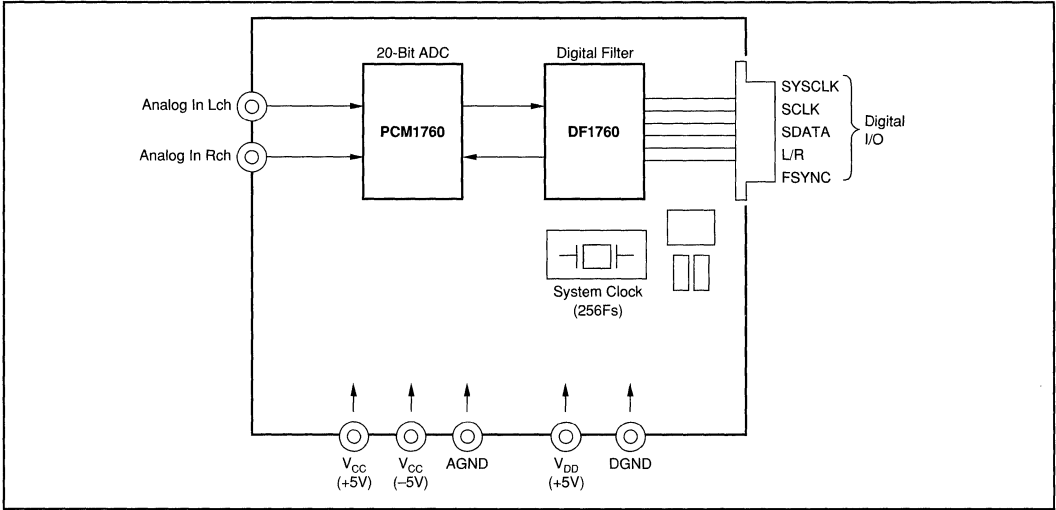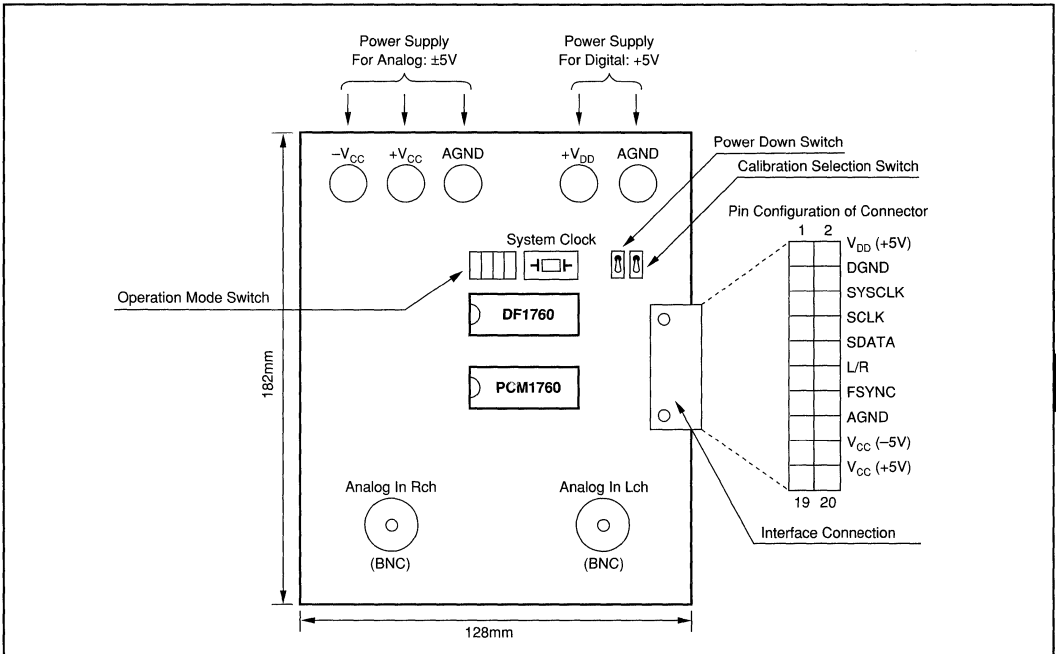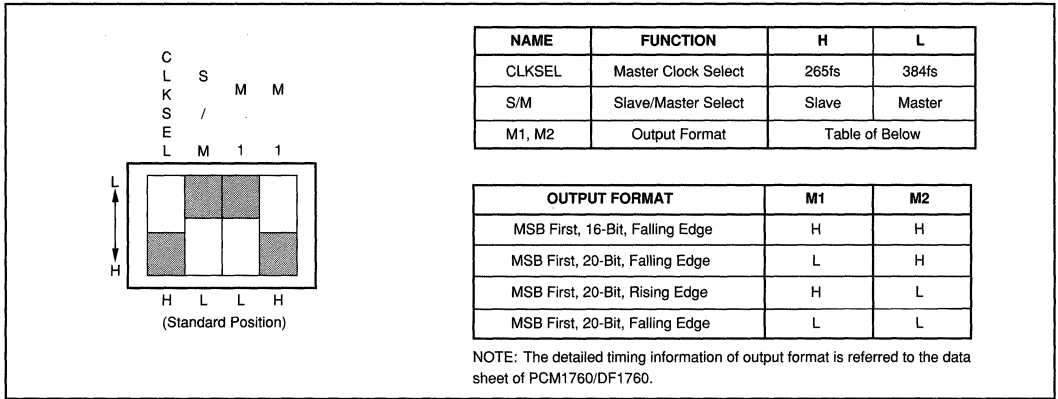
FIGURE 1. Operation Mode Select Switch.

CALIBRATION SELECT SWITCH (CALD)

H: Calibration off

L: Calibration on

POWER DOWN SWITCH (PD)
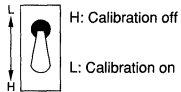
H: Normal Mode
L: Power Down Mode and Trigger of Calibration
CALD = L, (Start at Rising Edge of PD)
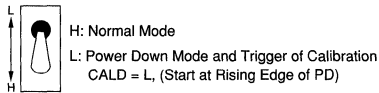
COMBINATION WITH DEM-PCM1702

The DEM-PCM1760 can be directly combined with the DEM-PCM1702 (20-bit stereo D/A conversion system) through the interface connector on the board.

In this case, the power supply should be connected to the DEM-PCM1702 and jumper line should be connected between the connector pin of the DEM-PCM1760 and the connector pin of the DEM-PCM1702.

The power supply for the DEM-PCM1760 is supplied from the DEM-PCM1702 through the jumper line and the DEM-PCM1760 outputs serial data for the DEM-PCM1702.
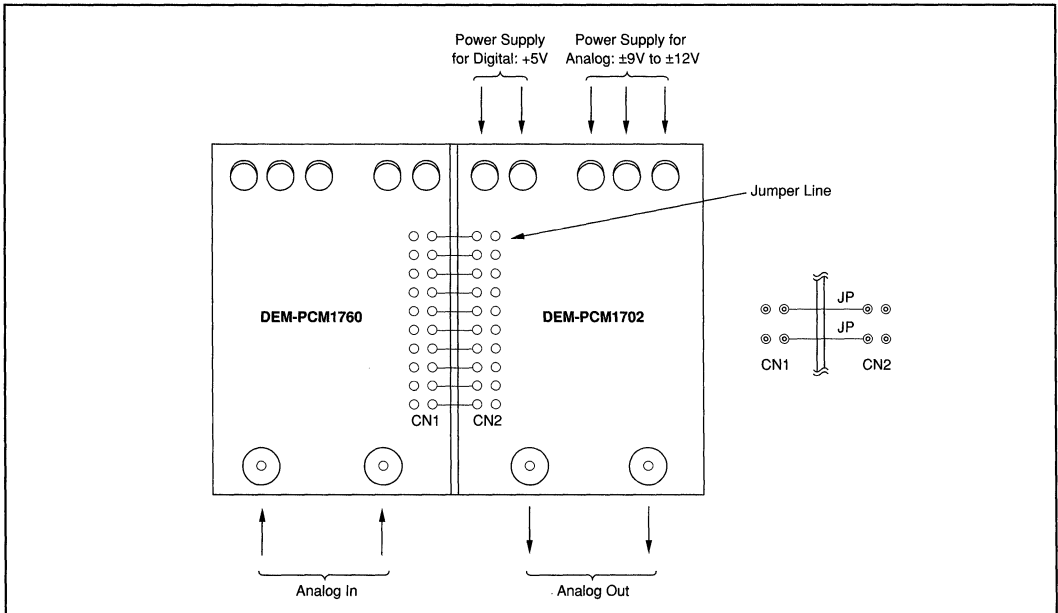
FIGURE 2.
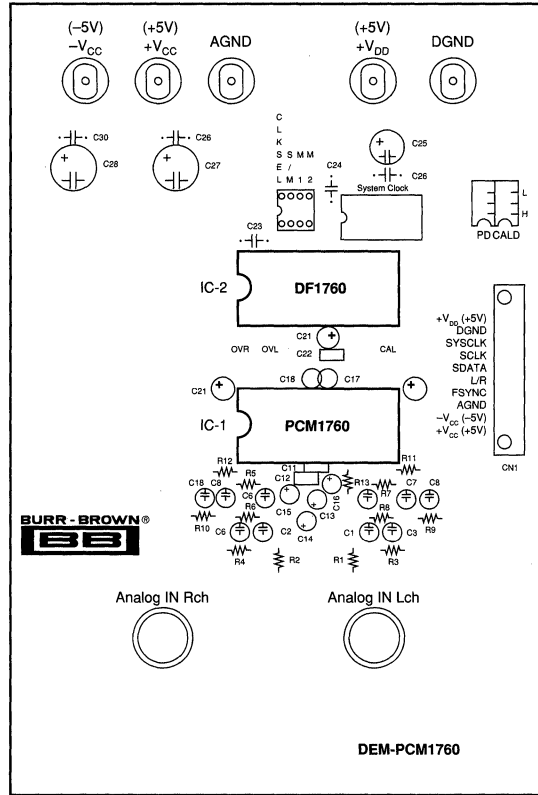
FIGURE 3. DEM-PCM1760 Board Layout—Component Layout.

DEM-PCM1760

A
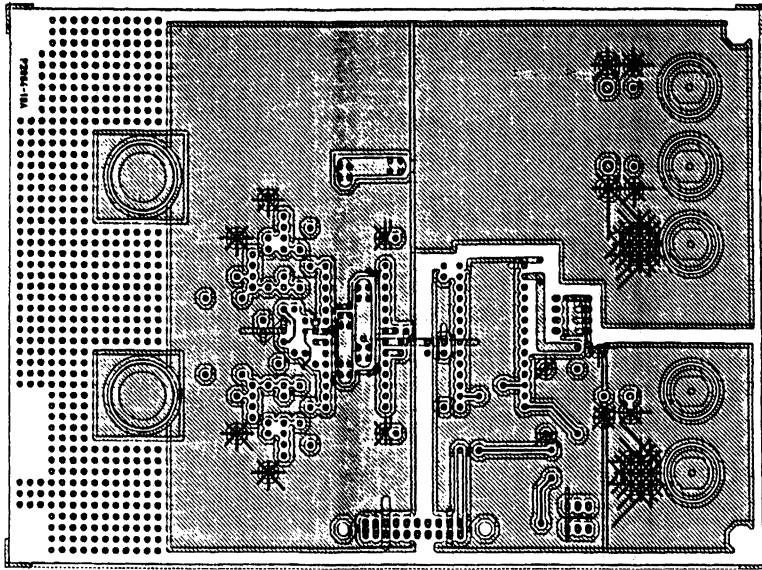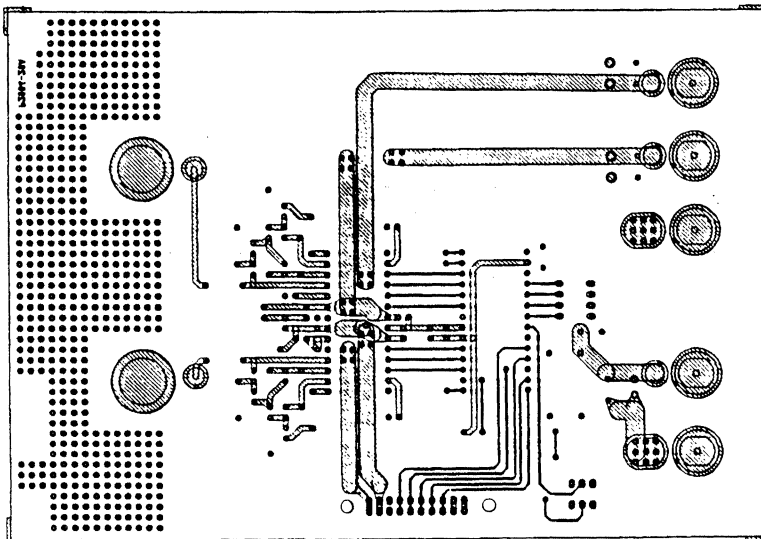
LAYER 1 (TOP)

LAYER 2 (BOTTOM)

FIGURE 4.
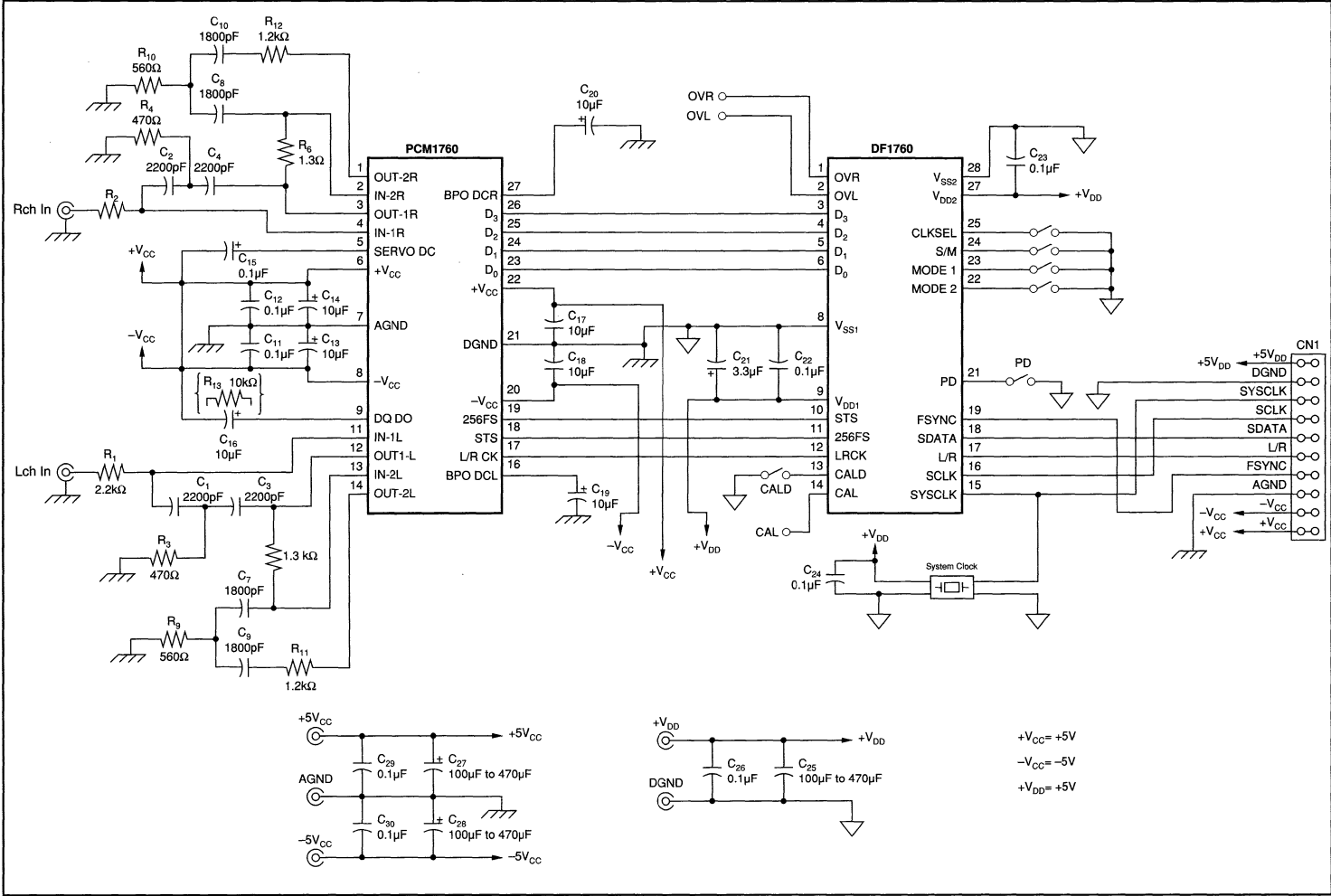
FIGURE 5. Circuit Diagram.

DEM-PCM1760

Appendix B

Cross Reference Guide

Definitions of pin compatibility: P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function and performance, but not pin for pin. C/P = Closest Part. Similar function and performance, but with significant differences.

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
1480	Teledyne-Philbrick	3583JM	P/P
175	Calex	INA101AM	F/E
175L	Calex	INA101AM	F/E
176J	Calex	INA101AM	F/E
176K	Calex	INA101AM	F/E
176L	Calex	INA101AM	F/E
178	Calex	INA101AM	F/E
286J	Analog Devices	3656	F/E
290A	Analog Devices	ISO122P	C/P
433	Analog Devices	4302	F/E
436	Analog Devices	MPY100AG	F/E
6M4314	Gennum	MPC100AP	C/P
6M8108	Gennum	MPC100AP	C/P
6X414A	Gennum	MPC100AP	F/E
6X4201	Gennum	MPC100AP	C/P
6X4304	Gennum	MPC100AP	C/P
6X434	Gennum	MPC100AP	F/E
757	Analog Devices	LOG100JP	F/E
7580	Beckman	DAC80-CBI-V	P/P
877-80	Beckman	DAC80-CBI-V	P/P
877-85	Beckman	DAC85H-CBI-V	P/P
AD OP-27	Analog Devices	OPA27	P/P
AD OP-37	Analog Devices	OPA37	P/P
AD101A	Analog Devices	3507J	C/P
AD101	Intersil (Harris)	3507J	C/P
AD1139	Analog Devices	DAC729JH	F/E
AD1145	Analog Devices	DAC709KH	F/E
AD1147	Analog Devices	DAC729JH	C/P
AD1148	Analog Devices	DAC729JH	C/P
AD1154	Analog Devices	SHC702JM	F/E
AD1201	Intech	ADC601JG	F/E
AD1341	Analog Devices	SDM862	F/E
AD1376	Analog Devices	ADC76JG	P/P
AD1376	Analog Devices	PCM75	P/P
AD1380	Analog Devices	ADC700JH	C/P
AD1674	Analog Devices	ADS774JP	F/E
AD1678	Analog Devices	ADS7800AH	F/E
AD171	Analog Devices	3582J	C/P
AD1856	Analog Devices	PCM56P	P/P
AD1860	Analog Devices	PCM61P	P/P
AD1862	Analog Devices	PCM63P	F/E
AD1864	Analog Devices	PCM1700P	F/E
AD1865	Analog Devices	PCM1700P	F/E
AD1876	Analog Devices	PCM78P	F/E
AD202	Analog Devices	ISO212JP	C/P
AD203	Analog Devices	ISO103	C/P
AD203N	Analog Devices	ISO103	F/E

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
AD204	Analog Devices	ISO212JP	C/P
AD208	Analog Devices	ISO212JP	C/P
AD210	Analog Devices	3656	F/E
AD210	Analog Devices	ISO103	C/P
AD2700	Analog Devices	REF10JM	C/P
AD2701	Analog Devices	REF101JM	C/P
AD2702	Analog Devices	REF101JM	C/P
AD2710	Analog Devices	REF10JM	C/P
AD2712	Analog Devices	REF101JM	F/E
AD289	Analog Devices	ISO102	C/P
AD293	Analog Devices	ISO102	C/P
AD294	Analog Devices	ISO102	C/P
AD295	Analog Devices	3656MG	F/E
AD346	Analog Devices	SHC5320	F/E
AD346	Analog Devices	SHC804BM	F/E
AD3554	Analog Devices	3554AM	C/P
AD363	Analog Devices	SDM872JH	C/P
AD364	Analog Devices	SDM873JH	C/P
AD376	Analog Devices	ADC76JG	P/P
AD380	Analog Devices	OPA605AM	C/P
AD380	Analog Devices	OPA654	F/E
AD381	Analog Devices	OPA606KM	P/P
AD382	Analog Devices	OPA605AM	C/P
AD3860	Analog Devices	DAC811AH	P/P
AD386	Analog Devices	SHC702	F/E
AD386	Analog Devices	SHC76	F/E
AD389	Analog Devices	SHC76KM	P/P
AD390	Analog Devices	DAC4813	F/E
AD503	Analog Devices	OPA121KM	P/P
AD503	Intersil (Harris)	OPA101	P/E
AD504	Analog Devices	OPA27GJ	F/E
AD506	Analog Devices	OPA121KM	P/P
AD507	Analog Devices	3507J	P/P
AD509	Analog Devices	3507J	P/P
AD510	Analog Devices	OPA27GJ	P/P
AD515	Analog Devices	AD515JH	P/P
AD517	Analog Devices	OPA27GJ	F/E
AD518	Analog Devices	3507J	F/E
AD521	Analog Devices	INA101AG	F/E
AD522	Analog Devices	INA101AM	F/E
AD5240	Analog Devices	ADC84KG-12	P/P
AD5240	Analog Devices	ADC85	P/P
AD524	Analog Devices	INA110AG	F/E
AD526	Analog Devices	PGA102	F/E
AD526	Analog Devices	PGA203KP	C/P
AD532	Analog Devices	MPY100AM	P/P
AD533	Analog Devices	MPY100AM	F/E

CROSS REFERENCE GUIDE

B

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
AD534	Analog Devices	MPY534JD	P/P	AD650	Analog Devices	VFC110AP	C/P
AD535	Analog Devices	MPY534JD	F/E	AD651	Analog Devices	VFC100AG	P/P
AD536	Analog Devices	4341	F/E	AD652	Analog Devices	VFC101N	P/P
AD537	Analog Devices	VFC32BM	C/P	AD654	Analog Devices	VFC121AP	C/P
AD538	Analog Devices	4302	F/E	AD662	Analog Devices	DAC667JP	C/P
AD539	Analog Devices	MPY634AM	C/P	AD667	Analog Devices	DAC667JP	P/P
AD542	Analog Devices	OPA121KM	F/E	AD671	Analog Devices	ADC601JG	F/E
AD544	Analog Devices	OPA606KM	F/E	AD671	Analog Devices	ADS602	F/E
AD545A	Analog Devices	OPA111	P/P	AD671	Analog Devices	ADS7800	F/E
AD545	Analog Devices	OPA111AM	P/P	AD674A	Analog Devices	ADC674AJH	P/P
AD546	Analog Devices	OPA121KM	P/P	AD676	Analog Devices	ADS7805	C/P
AD547	Analog Devices	OPA111AM	F/E	AD677	Analog Devices	ADS7809	C/P
AD548	Analog Devices	OPA111AM	F/E	AD678	Analog Devices	ADS7800AH	F/E
AD549	Analog Devices	OPA128JM	F/E	AD679	Analog Devices	ADC700KH	F/E
AD5539	Analog Devices	OPA621KP	F/E	AD683	Analog Devices	SHC804BM	F/E
AD562	Analog Devices	DAC80-CBI-V	C/P	AD693	Analog Devices	XTR101AG	F/E
AD562	Analog Devices	DAC85	C/P	AD694	Analog Devices	XTR110KP	F/E
AD563	Analog Devices	DAC80-CBI-V	C/P	AD704	Analog Devices	OPA404KP	C/P
AD563	Analog Devices	DAC85	C/P	AD705	Analog Devices	OPA177GP	C/P
AD565A	Analog Devices	DAC80-CBI-I	C/P	AD706	Analog Devices	OPA2111KP	C/P
AD565A	Analog Devices	DAC85	C/P	AD707	Analog Devices	OPA177EZ	P/P
AD565	Analog Devices	DAC65	C/P	AD708	Analog Devices	OPA1013AM	C/P
AD565	Analog Devices	DAC80-CBI-I	C/P	AD711	Analog Devices	OPA602AM	P/P
AD565	Maxim	DAC80-CBI-I	C/P	AD711	Analog Devices	OPA604AP	P/P
AD566A	Analog Devices	DAC80-CBI-I	C/P	AD712	Analog Devices	OPA2107AM	C/P
AD566A	Analog Devices	DAC85	C/P	AD712	Analog Devices	OPA2604AP	C/P
AD566	Analog Devices	DAC80-CBI-I	C/P	AD713	Analog Devices	OPA404KP	P/P
AD567	Analog Devices	DAC811AH	F/E	AD7245	Analog Devices	DAC667JP	C/P
AD568	Analog Devices	DAC812BM	F/E	AD7247	Analog Devices	DAC2815	C/P
AD569	Analog Devices	DAC709KH	C/P	AD7248	Analog Devices	DAC667JP	C/P
AD572	Analog Devices	ADC84KG-12	F/E	AD734	Analog Devices	MPY600AP	C/P
AD573	Analog Devices	ADC574AJH	C/P	AD736	Analog Devices	4341	C/P
AD573	Analog Devices	ADS574	C/P	AD737	Analog Devices	4341	C/P
AD574	Analog Devices	ADC574AJH	P/P	AD741	Analog Devices	OPA177GP	P/P
AD578	Analog Devices	ADC80AG-12	F/E	AD743	Analog Devices	OPA627AP	F/E
AD579	Analog Devices	ADC601JG	C/P	AD744	Analog Devices	OPA602	F/E
AD581	Analog Devices	REF102AM	C/P	AD744	Analog Devices	OPA606	F/E
AD582	Analog Devices	SHC298AM	C/P	AD744	Analog Devices	OPA627AP	C/P
AD583	Analog Devices	SHC5320KH	F/E	AD745	Analog Devices	OPA637	P/E
AD584	Analog Devices	REF101JM	C/P	AD746	Analog Devices	OPA2107AP	P/P
AD585	Analog Devices	SHC5320KH	F/E	AD871	Analog Devices	ADS605	C/P
AD587	Analog Devices	REF102BM	P/P	AD872	Analog Devices	ADS605	C/P
AD588	Analog Devices	REF101JM	C/P	AD7501	Analog Devices	MPC508	F/E
AD600	Analog Devices	VCA610	C/P	AD7501	Analog Devices	MPC508	F/E
AD6012	Analog Devices	DAC80-CBI-V	C/P	AD7502	Analog Devices	MPC509	F/E
AD602	Analog Devices	VCA610	C/P	AD7502	Analog Devices	MPC509	F/E
AD606	Analog Devices	INA101AM	F/E	AD7503	Analog Devices	MPC508	C/P
AD611	Analog Devices	OPA121KM	F/E	AD7503	Analog Devices	MPC508	F/E
AD612	Analog Devices	PGA200AG	F/E	AD7503	Analog Devices	MPC508	C/P
AD614	Analog Devices	PGA200AG	F/E	AD7506	Analog Devices	MPC16	P/P
AD620	Analog Devices	INA114	P/E	AD7506	Analog Devices	MPC506	P/P
AD621	Analog Devices	INA131	C/P	AD7506	Analog Devices	MPC506	P/P
AD624	Analog Devices	INA110AG	P/P	AD7507	Analog Devices	MPC507	P/P
AD625	Analog Devices	INA103KP	F/E	AD7507	Analog Devices	MPC507	P/P
AD632	Analog Devices	MPY534	P/E	AD7507	Analog Devices	MPC8	P/P
AD633	Analog Devices	MPY634AM	C/P	AD7521	Analog Devices	DAC7541AJP	P/P
AD642	Analog Devices	OPA2111AM	C/P	AD7521	Intersil (Harris)	DAC7541AJP	P/P
AD644	Analog Devices	OPA2111AM	C/P	AD7521	Maxim	DAC7541AJP	P/P
AD645	Analog Devices	OPA111BM	P/P	AD7521	National Semiconductor	DAC7541AJP	P/P
AD645	Analog Devices	OPA627	F/E	AD7524	Analog Devices	DAC7801	C/P
AD647	Analog Devices	OPA2111AM	F/E	AD7528	Analog Devices	DAC7528	P/P
AD648	Analog Devices	OPA2107AM	F/E	AD7531	Analog Devices	DAC7541AJP	P/P

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
AD7531	Intersil (Harris)	DAC7541AJP	P/P
AD7531	Maxim	DAC7541AJP	P/P
AD7531	National Semiconductor	DAC7541AJP	P/P
AD7537	Analog Devices	DAC7801KP	F/E
AD7538	Analog Devices	DAC702	C/P
AD7541A	Analog Devices	DAC7541AJP	P/P
AD7541A	Maxim	DAC7541AJP	P/P
AD7541	Analog Devices	DAC7541AJP	P/P
AD7541	Intersil (Harris)	DAC7541AJP	P/P
AD7541	Maxim	DAC7541AJP	P/P
AD7542	Analog Devices	DAC811AH	C/P
AD7543	Analog Devices	DAC7800KP	C/P
AD7545A	Analog Devices	DAC7545AH	P/P
AD7545	Analog Devices	DAC7545AH	P/P
AD7545	Maxim	DAC7545AH	P/P
AD7546	Analog Devices	DAC707KH	F/E
AD7547	Analog Devices	DAC7802KP	F/E
AD7548	Analog Devices	DAC811AH	C/P
AD7549	Analog Devices	DAC7802KP	F/E
AD7572	Analog Devices	ADC774JH	F/E
AD7572	Analog Devices	ADS774	F/E
AD7578	Analog Devices	ADC7802BP	C/P
AD7579	Analog Devices	ADS574JP	C/P
AD7580	Analog Devices	ADS574JP	C/P
AD7582	Analog Devices	ADC7802BP	F/E
AD759	Analog Devices	LOG100	C/P
AD766	Analog Devices	PCM56P	F/E
AD7672	Analog Devices	ADS7800JP	F/E
AD767	Analog Devices	DAC667JP	F/E
AD767	Analog Devices	DAC811	F/E
AD795	Analog Devices	OPA124	P/P
AD7772	Analog Devices	ADC804BH	C/P
AD7845	Analog Devices	DAC667JP	C/P
AD7848	Analog Devices	DAC667JP	C/P
AD7870	Analog Devices	ADS774JP	F/E
AD7878	Analog Devices	ADS774JP	F/E
AD811	Analog Devices	BUF634	C/P
AD829	Analog Devices	OPA620KP	F/E
AD829	Analog Devices	OPA621	F/E
AD834	Analog Devices	MPY600AP	C/P
AD840	Analog Devices	OPA621KP	C/P
AD841	Analog Devices	OPA620KP	F/E
AD842	Analog Devices	OPA621KP	F/E
AD843	Analog Devices	OPA671AP	F/E
AD844	Analog Devices	3554AM	C/P
AD844	Analog Devices	OPA603	C/P
AD845	Analog Devices	OPA637AP	F/E
AD846	Analog Devices	OPA603AP	F/E
AD847	Analog Devices	OPA671	C/P
AD848	Analog Devices	OPA620	C/P
AD849	Analog Devices	OPA621	C/P
AD9003	Analog Devices	ADS602JG	F/E
AD9005	Analog Devices	ADC603JH	F/E
AD9300	Analog Devices	MPC100AP	C/P
AD9610	Analog Devices	OPA600	C/P
AD9617	Analog Devices	OPA603AP	F/E
AD9617	Analog Devices	OPA644	P/P
AD9618	Analog Devices	OPA603AP	F/E
AD9620	Analog Devices	OPA633KP	C/P
AD9630	Analog Devices	BUF601	P/E
AD9712	Analog Devices	DAC65JP	F/E
AD9713	Analog Devices	DAC65	F/E

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
ADA160Q	Zeltex	DAC729JH	F/E
ADADC80	Analog Devices	ADC80AG-12	P/P
ADADC84	Analog Devices	ADC84KG-12	P/P
ADADC85	Analog Devices	ADC85H-12	P/P
ADC-EH12B3	Datel	ADC80AG-12	C/P
ADC-HX12B	Datel	ADC84KG-12	P/P
ADC00401	DDC	ADC80AG-12	F/E
ADC00403	DDC	ADC80AG-12	F/E
ADC1080	National Semiconductor	ADC80AG-12	P/P
ADC1103	Analog Devices	ADC80AG-12	F/E
ADC1130	Analog Devices	ADC71JG	C/P
ADC1131	Analog Devices	ADC71JG	C/P
ADC1140	Analog Devices	ADC71JG	C/P
ADC1280	National Semiconductor	ADC80AG-12	P/P
ADC386	National Semiconductor	SHC702JM	F/E
ADC4450	DDC	ADC80AG-12	F/E
ADC511	Datel	ADC601JG	F/E
ADC810	Datel	ADC80AG-12	F/E
ADC811	Datel	ADC80AG-12	F/E
ADC817	Datel	ADC80AG-12	F/E
ADC827	Datel	ADC80AG-12	F/E
ADC910	PMI (Analog Devices)	ADS7800	C/P
ADC912	PMI (Analog Devices)	ADS774	C/P
ADC922	PMI (Analog Devices)	ADS7800	C/P
ADCHX12	Datel	ADC84	P/P
ADDAC71	Analog Devices	DAC71-COB-V	P/P
ADDAC72	Analog Devices	DAC72BH-COB-V	P/P
ADDAC80	Analog Devices	DAC80-CBI-V	P/P
ADDAC85	Analog Devices	DAC85H-CBI-V	P/P
ADDAC87	Analog Devices	DAC87H-CBI-V	P/P
ADG506A	Analog Devices	MPC506	C/P
ADG506A	Analog Devices	MPC506	C/P
ADG507A	Analog Devices	MPC507	C/P
ADG507A	Analog Devices	MPC507	C/P
ADG508A	Analog Devices	MPC508	C/P
ADG508A	Analog Devices	MPC508	C/P
ADG509A	Analog Devices	MPC509	C/P
ADG509A	Analog Devices	MPC509	C/P
ADH-051	DDC	ADC80AG-12	C/P
ADH8516	DDC	ADC80AG-12	F/E
ADH8585	DDC	ADC85H-12	P/P
ADH8586	DDC	ADC85H-12	F/E
ADLH0032	Analog Devices	OPA605AM	C/P
ADLH0033	Analog Devices	OPA633KP	F/E
ADOP-07	Analog Devices	OPA177GZ	F/E
ADOP-27	Analog Devices	OPA27GJ	P/P
ADOP-37	Analog Devices	OPA37GJ	P/P
ADREF01	Analog Devices	REF102AP	P/P
ADS130	Datel	ADC603JH	F/E
ADVFC32	Analog Devices	VFC32BM	P/P
AM6012	Maxim	DAC80-CBI-V	C/P
AMP-01	PMI (Analog Devices)	INA101AM	F/E
AMP-01	PMI (Analog Devices)	INA104	F/E
AMP-02	PMI (Analog Devices)	INA103KP	C/P
AMP-02	PMI (Analog Devices)	INA111	P/P
AMP-02	PMI (Analog Devices)	INA114	P/P
AMP-02	PMI (Analog Devices)	INA114	P/E
AMP-03	PMI (Analog Devices)	INA105KP	P/E
AMP-05	PMI (Analog Devices)	INA110AG	F/E
BB3553	Maxim	3553AM	P/P
BB3554	Maxim	3554AM	P/P
BT104	Brooktree	DAC65JP	C/P

CROSS REFERENCE GUIDE

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
BT105	Brooktree	DAC65JP	C/P	DAC377	Sipex	DAC729JH	C/P
BUF-03	PMI (Analog Devices)	BUF634	C/P	DAC391	Hybrid	DAC812BM	C/P
BUF-03	PMI (Analog Devices)	OPA633		DAC612	Datel	DAC811AH	C/P
CAV1210	Analog Devices	ADC603JH	C/P	DAC7528	Analog Devices	DAC7528	P/P
CLC400	Comlinear	OPA620KG	C/P	DAC8043	Analog Devices	DAC8043	P/P
CLC401	Comlinear	OPA620KG	C/P	DAC8221	PMI (Analog Devices)	DAC7802KP	F/E
CLC404	Comlinear	OPA623	C/P	DAC8222	PMI (Analog Devices)	DAC7802KP	F/E
CLC409	Comlinear	OPA623	P/E	DAC87	DDC	DAC87H-CBI-V	P/P
CLC411	Comlinear	OPA623	C/P	DAC9332-16	Hybrid	DAC709KH	F/E
CLC500	Comlinear	OPA620KG	F/E	DAC9349	Hybrid	DAC80-CBI-V	C/P
CLC501	Comlinear	OPA620KG	F/E	DAC9377	Hybrid	DAC707KH	F/E
CLC520	Comlinear	VCA610	C/P	DACHK	Micro Networks	DAC811AH	F/E
CLC912	Comlinear	DAC65JP	F/E	DACHP16	Datel	DAC701	P/P
CLC925	Comlinear	ADC603	C/P	DACHP16	Datel	DAC703	P/P
CLC925	Comlinear	ADC603JH	F/E	DACHZ12	Datel	DAC85	P/P
CLC926	Comlinear	ADC603JH	F/E	DAS1128	Analog Devices	SDM873JH	F/E
CS5102A	Crystal	ADS7807	C/P	DG506A	Maxim	MPC506	P/E
CS5101A	Crystal	ADS7809	C/P	DG506	Silconix	MPC506	P/P
CS5326	Crystal Semiconductor	PCM1750P	C/P	DG506	Siliconix	MPC16	P/P
CS5327	Crystal Semiconductor	PCM1750P	C/P	DG506	Siliconix	MPC506	P/P
CS5328	Crystal Semiconductor	PCM1750P	C/P	DG507A	Maxim	MPC507	P/E
CS5329	Crystal Semiconductor	PCM1750P	C/P	DG507	Silconix	MPC507	P/P
CS5336	Crystal Semiconductor	PCM1750P	C/P	DG507	Siliconix	MPC507	P/P
CS5337	Crystal Semiconductor	PCM1750P	C/P	DG507	Siliconix	MPC8	P/P
CS5338	Crystal Semiconductor	PCM1750P	C/P	DG508A	Maxim	MPC508	P/E
CS533P	Crystal Semiconductor	PCM1750P	C/P	DG508	Silconix	MPC508	P/P
D6534	Siliconix	MPC100AP	C/P	DG508	Siliconix	MPC508	P/P
D6538	Siliconix	MPC100AP	C/P	DG508	Siliconix	MPC8	P/P
D6884	Siliconix	MPC100AP	C/P	DG509A	Maxim	MPC509	P/E
D6894	Siliconix	MPC100AP	C/P	DG509	Silconix	MPC509	P/P
DAC-01	PMI (Analog Devices)	NONE		DG509	Silconix	MPC509	P/P
DAC-02	PMI (Analog Devices)	NONE		DG509	Siliconix	MPC4	P/P
DAC-03	PMI (Analog Devices)	NONE		EL2001	Élantec	BUF634	C/P
DAC-08	PMI (Analog Devices)	NONE		EL2002	Elantec	BUF634	C/P
DAC-10	PMI (Analog Devices)	NONE		EL2003	Elantek	OPA633KP	P/P
DAC-20	PMI (Analog Devices)	NONE		EL2007	Elantek	OPA541AM	C/P
DAC-71	Datel	DAC71-COB-V	P/P	EL2008	Elantec	BUF634	C/P
DAC-72	Datel	DAC72BH-COB-V	P/P	EL2009	Elantec	BUF634	C/P
DAC-86	PMI (Analog Devices)	NONE		EL2020	Elantek	OPA603AP	C/P
DAC-HF12B	Datel	DAC812BM	C/P	EL2030	Elantek	OPA603AP	C/P
DAC-HF12	Datel	DAC65JP	F/E	EL2072	Elantec	BUF601	P/P
DAC-HK12B	Datel	DAC811AH	F/E	GX434	Gennum	MPC100	C/P
DAC-HP16	Datel	DAC71-COB-V	P/P	HA-2400	Harris	OPA676JG	F/E
DAC-HY12	Datel	DAC80-CBI-V	P/P	HA-2420	Harris	SHC5320KH	C/P
DAC-HZ12B	Datel	DAC85H-CBI-V	P/P	HA-2425	Harris	SHC5320KH	C/P
DAC-S	DDC	DAC85H-CBI-V	P/P	HA-2500	Harris	3507J	F/E
DAC-SL	DDC	DAC811AH	F/E	HA-2505	Harris	OPA602	P/E
DAC02701	DDC	DAC811AH	F/E	HA-2510	Harris	3507J	F/E
DAC1136	Analog Devices	DAC729JH	P/P	HA-2520	Harris	3507J	P/P
DAC1138	Analog Devices	DAC729KH	F/E	HA-2525	Harris	3507	P/P
DAC1208	National Semiconductor	DAC811AH	F/E	HA-2539	Harris	OPA605AM	C/P
DAC1218	National Semiconductor	DAC7541AJP	F/E	HA-2540	Harris	OPA605AM	C/P
DAC1219	National Semiconductor	DAC7541AJP	F/E	HA-2541	Harris	OPA605AM	C/P
DAC1230	National Semiconductor	DAC811AH	F/E	HA-2542	Harris	OPA605AM	C/P
DAC1280	National Semiconductor	DAC80-CBI-V	P/P	HA-2546	Harris	MPY600AP	C/P
DAC1285	National Semiconductor	DAC85H-CBI-V	P/P	HA-2547	Harris	MPY600AP	C/P
DAC1286	National Semiconductor	DAC80-CBI-V	P/P	HA-2600	Harris	3507J	C/P
DAC1287	National Semiconductor	DAC87H-CBI-V	P/P	HA-2605	Harris	3507	P/E
DAC331	Hybrid	DAC7541AJP	F/E	HA-2620	Harris	3507J	P/P
DAC336-12	Hybrid	DAC811AH	F/E	HA-2625	Harris	3507	P/E
DAC347	Hybrid	DAC7541AJP	F/E	HA-2630	Harris	3553AM	C/P
DAC377	Hybrid	DAC729JH	C/P	HA-2640	Harris	OPA445M	P/E

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number			Burr-Brown Part Number	Pin Compatibility
HA-2645	Harris	OPA445AP	P/E	HI-547-5	Harris		MPC8D	P/P
HA-2645	Harris	OPA445BM	C/P	HI-548-5	Harris		MPC8S	P/P
HA-2650	Harris	OPA2111AM	C/P	HI-549-5	Harris		MPC4D	P/P
HA-4156	Harris	OPA404AG	C/P	HI-5660	Harris		DAC80-CBI-V	C/P
HA-4741	Harris	OPA404AG	C/P	HI-5680	Harris		DAC80-CBI-V	P/P
HA-5002	Harris	OPA633KP	C/P	HI-5685	Harris		DAC85H-CBI-V	P/P
HA-5004	Harris	OPA603AP	C/P	HI-5687	Harris		DAC87H-CBI-V	P/P
HA-5033	Harris	OPA633KP	P/P	HI-5690	Harris		DAC80-CBI-V	C/P
HA-5062	Harris	OPA2111AM	C/P	HI-5695	Harris		DAC85H-CBI-V	C/P
HA-5064	Harris	OPA404AG	F/E	HI-574A	Harris		ADC574AJH	P/P
HA-5082	Harris	OPA2111AM	F/E	HI-5811	Harris		DAC811AH	P/P
HA-5084	Harris	OPA404AG	F/E	HI-674A	Harris		ADC674A	P/P
HA-5100	Harris	OPA606KM	C/P	HI-774A	Harris		ADC774JP	P/P
HA-5102	Harris	OPA2111AM	C/P	HI-774	Harris		ADC774JP	P/P
HA-5104	Harris	OPA404AG	F/E	HI-DAC16	Harris		DAC71-COB-V	F/E
HA-5110	Harris	3551J	F/E	HI518	Harris		MPC801	P/P
HA-5112	Harris	OPA2111AM	C/P	HI574	Harris		ADC574	P/P
HA-5114	Harris	OPA404AG	F/E	HI674	Harris		ADC674	P/P
HA-5130	Harris	OPA27GJ	F/E	HOS-050	Analog Devices		3554AM	C/P
HA-5135	Harris	OPA27GJ	F/E	HOS-060	Analog Devices		3554AM	C/P
HA-5142	Harris	OPA2111AM	C/P	HOS-100	Analog Devices		OPA633KP	P/P
HA-5144	Harris	OPA404AG	C/P	HOS-200	Analog Devices		OPA633KP	F/E
HA-5147	Harris	OPA37GJ	F/E	HS3120	Hybrid		DAC811AH	F/E
HA-5160	Harris	OPA602AM	F/E	HS3160	Hybrid		DAC703KH	C/P
HA-5170	Harris	OPA111AM	F/E	HS346	Hybrid		SHC5320KH	C/P
HA-5180	Harris	OPA111AM	P/P	HS3860	Hybrid		DAC811AH	F/E
HA-5190	Harris	OPA605AM	C/P	HS7541	Hybrid		DAC7541AJP	P/P
HA-5320	Harris	SHC5320KH	P/P	HS7545	Hybrid		DAC7545AH	P/P
HA-5330	Harris	SHC803BM	C/P	HS9338	Hybrid		DAC811AH	F/E
HA-OP07	Harris	OPA177GZ	P/P	HS9377	Hybrid		DAC707KH	F/E
HA-OP27	Harris	OPA27GJ	P/P	HS9378	Hybrid		DAC707KH	F/E
HA-OP37	Harris	OPA37GJ	P/P	HS9393	Hybrid		DAC65JP	F/E
HA6033	Harris	BUF634	C/P	HS9394	Hybrid		DAC65JP	F/E
HAS-050	Analog Devices	3554AM	C/P	HS9410	Hybrid		SDM872JH	C/P
HAS-1202A	Analog Devices	ADC80AG-12	C/P	HS9576	Hybrid		ADC76JG	P/P
HAS-1202	Analog Devices	ADC80AG-12	F/E	HSDAC80	Hybrid		DAC80-CBI-V	P/P
HDAS-16	Datel	SDM857JG	F/E	HSDAC87	Hybrid		DAC87H-CBI-V	P/P
HDAS-8	Datel	SDM857JG	F/E	HT0025	Analog Devices		SHC600BH	F/E
HDS1240	Analog Devices	DAC65JP	F/E	HTC0300	Analog Devices		SHC804BM	P/P
HFA1100	Harris	BUF600	C/P	HTS0010	Analog Devices		SHC600BH	F/E
HFA1100	Harris	OPA623	C/P	HY6110	Hytek		PGA200AG	C/P
HFA1112	Harris	BUF601	C/P	ICH8515	Intersil	(Harris)	OPA541AM	C/P
HFA1120	Harris	OPA623	C/P	ICL7134	Intersil	(Harris)	DAC709KH	C/P
HFA5033	Harris	BUF600	C/P	ICL7145	Intersil	(Harris)	DAC707KH	C/P
HI-0508	Maxim	MPC508	P/P	ICL7146	Intersil	(Harris)	DAC811AH	C/P
HI-0508	Maxim	MPC508	P/P	ICL7605	Intersil	(Harris)	INA101AM	F/E
HI-0509	Maxim	MPC509	P/P	ICL7606	Intersil	(Harris)	INA101AM	F/E
HI-0509	Maxim	MPC509	P/P	ICL8013	Intersil	(Harris)	MPY100	F/E
HI-506	Harris Semiconductor	MPC16	P/P	IH5108	Harris		MPC8	P/P
HI-506	Harris	MPC506	P/P	IH5108	Harris		MPC801	P/P
HI-507	Harris	MPC507	P/P	IH5108	Intersil	(Harris)	MPC508	P/P
HI-507	Harris	MPC8	P/P	IH5110-15	Intersil	(Harris)	SHC298AM	C/P
HI-508	Harris	MPC508	P/P	IH5208	Harris		MPC4	P/P
HI-508	Harris	MPC8	P/P	IH5208	Harris		MPC801	P/P
HI-508	Maxim	MPC508	P/P	IH5208	Intersil	(Harris)	MPC507	P/P
HI-509	Harris	MPC509	P/P	IH6108	Harris		MPC8	P/P
HI-5127	Harris	OPA27	P/E	IH6108	Harris		MPC801	P/P
HI-5137	Harris	OPA37	P/E	IH6108	Intersil	(Harris)	MPC508	P/P
HI-516	Harris	MPC800	P/P	IH6116	Harris		MPC800	P/P
HI-516	Harris	MPC800KG	P/P	IH6116	Intersil	(Harris)	MPC506	P/P
HI-518	Harris	MPC801KG	P/P	IH6216	Harris		MPC8	P/P
HI-546-5	Harris	MPC16S	P/P	IH6216	Intersil	(Harris)	MPC507	P/P

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
LF11508	National Semiconductor	MPC508	P/P	LH740A	National Semiconductor	OPA121KM	P/P
LF11509	National Semiconductor	MPC509	P/P	LM101A	LTC	OPA27GJ	C/P
LF13741	National Semiconductor	OPA121KM	P/P	LM101A	National Semiconductor	OPA27GJ	C/P
LF155A	LTC	OPA606KM	F/E	LM107	LTC	OPA177GP	C/P
LF155A	National Semiconductor	OPA606KM	F/E	LM107	National Semiconductor	OPA177GP	C/P
LF156A	LTC	OPA606KM	F/E	LM112	LTC	OPA27EJ	C/P
LF156A	National Semiconductor	OPA606KM	F/E	LM112	National Semiconductor	OPA27EJ	C/P
LF157A	National Semiconductor	OPA606KM	F/E	LM118	Harris	3507J	C/P
LF198	National Semiconductor	SHC298AM	P/P	LM118	LTC	3507	C/P
LF198	Texas Instruments	SHC298	P/P	LM118	National Semiconductor	3507J	C/P
LF298	National Semiconductor	SHC298	P/P	LM11C	Motorola	OPA602	P/E
LF351	Motorola	OPA604	P/E	LM12	National Semiconductor	OPA541AM	C/P
LF351	Motorola	OPA604	P/E	LM131	National Semiconductor	VFC32BM	C/P
LF351	National Semiconductor	OPA156AM	P/P	LM143	National Semiconductor	OPA445BM	C/P
LF353	Harris	OPA2111AM	P/P	LM144	National Semiconductor	OPA445BM	C/P
LF353	Motorola	OPA2111	P/P	LM1558	National Semiconductor	OPA2111AM	C/P
LF353	National Semiconductor	OPA2111AM	P/P	LM158A	National Semiconductor	OPA2111AM	C/P
LF355	LTC	OPA121	P/E	LM163	National Semiconductor	INA101AM	F/E
LF356	LTC	OPA121	P/E	LM185	LTC	REF1004	F/E
LF356	Motorola	OPA602	P/E	LM208	Intersil (Harris)	ISO212JP	C/P
LF357	Motorola	OPA637	C/P	LM2904	National Semiconductor	OPA2111AM	C/P
LF398A	National Semiconductor	SHC298AM	P/P	LM307	Motorola	OPA77	P/P
LF398	National Semiconductor	SHC298AM	P/P	LM318	LTC	3507	C/P
LF398	Texas Instruments	SHC298	P/P	LM324	National Semiconductor	OPA1013	C/P
LF400C		OPA606KM	F/E	LM331	National Semiconductor	VFC32BM	C/P
LF411	National Semiconductor	OPA602AM	P/P	LM334	National Semiconductor	REF200AM	C/P
LF412A	National Semiconductor	OPA2111AM	F/E	LM343	National Semiconductor	OPA445BM	C/P
LF412	National Semiconductor	OPA2111	P/P	LM358	Motorola	OPA1013	C/P
LF441	Motorola	OPA606	P/E	LM358	National Semiconductor	OPA2111AM	C/P
LF442A	National Semiconductor	OPA2111AM	F/E	LM363	National Semiconductor	INA101HP	F/E
LF444A	National Semiconductor	OPA404AG	P/P	LM607	National Semiconductor	OPA27GJ	C/P
LH0002	National Semiconductor	3553AM	C/P	LM6125	National Semiconductor	BUF634	C/P
LH0003	National Semiconductor	3507J	C/P	LM627	National Semiconductor	OPA627	P/P
LH0004	National Semiconductor	3580J	C/P	LM6361	National Semiconductor	3507	F/E
LH0005	National Semiconductor	OPA605AM	C/P	LM637	National Semiconductor	OPA637	P/P
LH0021	National Semiconductor	3571	C/P	LM675	National Semiconductor	OPA511AM	C/P
LH0022	National Semiconductor	OPA121KM	P/P	LM709A	National Semiconductor	3507J	C/P
LH0023	National Semiconductor	SHC298AM	C/P	LM725A	National Semiconductor	OPA27EJ	C/P
LH0024	National Semiconductor	3551J	F/E	LM747A	National Semiconductor	OPA2111AM	C/P
LH0032	National Semiconductor	OPA605AM	C/P	LM748	National Semiconductor	OPA27EJ	C/P
LH0033	National Semiconductor	OPA633KP	F/E	LM833	Motorola	OPA2107	C/P
LH0036	National Semiconductor	INA114	C/P	LM837	National Semiconductor	OPA404AG	C/P
LH0038	National Semiconductor	INA114	C/P	LMC660	National Semiconductor	OPA404AG	C/P
LH0042	National Semiconductor	OPA121KM	P/P	LT1001CN8	LTC	OPA177GP	P/P
LH0043	National Semiconductor	SHC298AM	C/P	LT1001	LTC	OPA27GJ	F/E
LH0044	National Semiconductor	OPA27GJ	F/E	LT1002	LTC	OPA2111AM	C/P
LH0052	National Semiconductor	OPA111AM	P/P	LT1004	LTC	REF1004	P/P
LH0053	National Semiconductor	SHC5320KH	C/P	LT1007	LTC	OPA27GJ	P/P
LH0053	National Semiconductor	SHC85	C/P	LT1010	Linear Technology	BUF634	C/P
LH0063	National Semiconductor	3553AM	F/E	LT1010	LTC	OPA633KP	C/P
LH0070	LTC	REF10	C/P	LT1013	LTC	OPA1013ACH	P/P
LH0084		PGA200AG	F/E	LT1013	Texas Instruments	OPA1013	P/P
LH0086	National Semiconductor	PGA102AG	F/E	LT1014	LTC	OPA404AG	C/P
LH0091	National Semiconductor	4341	C/P	LT1019	LTC	REF10JM	C/P
LH0094	National Semiconductor	4302	F/E	LT1021	LTC	REF102AM	P/P
LH0101	Maxim	OPA541AM	C/P	LT1022	LTC	OPA606KM	P/P
LH0101	National Semiconductor	OPA541AM	C/P	LT1023	LTC	OPA606KM	C/P
LH2011	National Semiconductor	OPA2111AM	C/P	LT1024	LTC	OPA2111AM	C/P
LH2101A	National Semiconductor	OPA2111AM	C/P	LT1025	LTC	OPA603	C/P
LH2108A	LTC	OPA2111AM	C/P	LT1027	LTC	REF02	C/P
LH2108A	National Semiconductor	OPA2111AM	C/P	LT1028	LTC	OPA27GJ	C/P
LH4001	National Semiconductor	OPA633KP	C/P	LT1031	LTC	REF10	C/P

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
LT1037	LTC	OPA37GJ	P/P
LT1055	LTC	OPA606KM	P/P
LT1056	LTC	OPA606KM	P/P
LT1057	LTC	OPA2111AM	C/P
LT1058	LTC	OPA404AG	F/E
LT1117	LTC	REG1117	P/P
LT118A	LTC	3507J	F/E
LT1223	LTC	OPA623	C/P
LT581	LTC	REF10	C/P
LTC1272	LTC	ADS7800	C/P
LTC1278	LTC	ADS7810	C/P
MAX195	Maxim	ADS7809	C/P
MAX310	Maxim	MPC100AP	C/P
MAX311	Maxim	MPC100AP	C/P
MAX358	Maxim	MPC508	P/P
MAX359	Maxim	MPC509	P/P
MAX450	Maxim	MPC100AP	C/P
MAX453	Maxim	MPC100AP	C/P
MAX454	Maxim	MPC100AP	F/E
MAX456	Maxim	MPC100AP	C/P
MAX543	Maxim	DAC8043	P/P
MAX7528	Maxim	DAC7528	P/P
MAX7537	Maxim	DAC7801KP	F/E
MAX7547	Maxim	DAC7802KP	F/E
MC1456	Motorola	OPA2604	C/P
MC1458	Motorola	OPA2604	C/P
MC1595	Motorola	MPY600AP	C/P
MC1596	Motorola	MPY600AP	C/P
MC1741	Motorola	OPA177	P/P
MC1747	Motorola	OPA1013	C/P
MC34001	Motorola	OPA602	P/P
MC34002	Motorola	OPA2604	C/P
MC34080	Motorola	OPA602	C/P
MC34080	Motorola	OPA606	C/P
MC34081	Motorola	OPA602	P/P
MC34082	Motorola	OPA2604	C/P
MC34083	Motorola	OPA2107	P/P
MC34181	Motorola	OPA111	F/E
MC34182	Motorola	OPA2111	C/P
MC3458	Motorola	OPA1013	C/P
MC4558	Motorola	OPA2604	C/P
MDAS-16	Datel	SDM872JG	C/P
MDAS-8D	Datel	SDM873JH	F/E
MN0300A	Micro Networks	SHC804BM	F/E
MN2020	Micro Networks	PGA102AG	C/P
MN3210	Micro Networks	DAC71-COB-V	P/P
MN3300	Micro Networks	DAC71-COB-V	P/P
MN3310	Micro Networks	DAC703KH	P/P
MN3660	Micro Networks	DAC811AH	C/P
MN375	Micro Networks	SHC804BM	F/E
MN376	Micro Networks	SHC804BM	F/E
MN379	Micro Networks	SHC600BH	F/E
MN3850	Micro Networks	DAC85H-CBI-V	P/P
MN3860	Micro Networks	DAC811AH	F/E
MN5200	Micro Networks	ADC84KG-12	F/E
MN5210-14	Micro Networks	ADC84KG-12	F/E
MN5245	Micro Networks	ADC80AG-12	F/E
MN5246	Micro Networks	ADC601JG	F/E
MN5248	Micro Networks	ADC601	P/P
MN5280	Micro Networks	ADC71JG	C/P
MN5282	Micro Networks	ADC71JG	C/P
MN5290	Micro Networks	ADC76JG	C/P

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MN5291	Micro Networks	ADC76JG	C/P
MN5610	Micro Networks	ADC84KG-12	F/E
MN574A	Micro Networks	ADC574AJH	P/P
MN7100	Micro Networks	SDM872JH	F/E
MN7130	Micro Networks	SDM862JH	F/E
MN7150	Micro Networks	SDM873JH	F/E
MNADC80	Micro Networks	ADC80AG-12	P/P
MNADC84	Micro Networks	ADC84KG-12	P/P
MNADC85	Micro Networks	ADC85H-12	P/P
MNADC87	Micro Networks	ADC87H-12	P/P
MNDAC80	Micro Networks	DAC80-CBI-V	P/P
MNDAC85	Micro Networks	DAC85H-CBI-V	P/P
MNDAC87	Micro Networks	DAC87H-CBI-V	P/P
MNDAC88	Micro Networks	DAC811AH	F/E
MP574	Micro Power Systems	ADC574AJH	P/P
MP6812	Analogic	SDM863JH	F/E
MP7506	Micro Power Systems	MPC16	P/P
MP7506	Micro Power Systems	MPC506	P/P
MP7507	Micro Power Devices	MPC8	P/P
MP7507	Micro Power Systems	MPC507	P/P
MP7508	Micro Power Devices	MPC8	P/P
MP7508	Micro Power Systems	MPC508	P/P
MP7509	Micro Power Devices	MPC4	P/P
MP7509	Micro Power Systems	MPC509	P/P
MP7531	Micro Power Systems	DAC7541AJP	P/P
MP7541A	Micro Power Systems	DAC7541AJP	P/P
MP7542	Micro Power Systems	DAC7545AH	C/P
MP7545	Micro Power Systems	DAC7541AJP	P/P
MP7616	Micro Power Systems	DAC703KH	C/P
MP7621	Micro Power Systems	DAC7541AJP	P/P
MP7622	Micro Power Systems	DAC7545AH	C/P
MP7623	Micro Power Systems	DAC7541AJP	P/P
MP8014	Analogic	ADC76JG	F/E
MP8016	Analogic	ADC76JG	F/E
MP8116	Analogic	DAC729JH	F/E
MP9331-16	Micro Power Systems	DAC709KH	F/E
MP9377-16	Micro Power Systems	DAC707KH	F/E
MPI814	Analogic	DAC70BH-COB-I	F/E
MPI914	Analogic	DAC70BH-COB-I	F/E
MUX08	Analog Devices	MPC8	C/P
MUX08	PMI (Analog Devices)	MPC508	P/P
MUX16	Analog Devices	MPC16	P/P
MUX16	PMI (Analog Devices)	MPC506	P/P
MUX24	PMI (Analog Devices)	MPC4	P/P
MUX24	PMI (Analog Devices)	MPC509	P/P
MUX28	Analog Devices	MPC8	C/P
MUX28	PMI (Analog Devices)	MPC507	P/P
MX-1606	Datel	MPC506	P/P
MX-808	Datel	MPC508	P/P
MX-818	Datel	MPC801KG	P/P
MX1606	Datel	MPC16	P/P
MX1616	Datel	MPC800	P/P
MX1616	Datel	MPC800KG	P/P
MX808	Datel	MPC508	P/P
MX808	Datel	MPC8S	P/P
MX818	Datel	MPC801	P/P
MXD-409	Datel	MPC509	P/P
MXD-807	Datel	MPC507	P/P
MXD409	Datel	MPC4	P/P
MXD409	Datel	MPC509	P/P
MXD807	Datel	MPC507	P/P
MXD807	Datel	MPC8	P/P

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
NE5532	Signetics	OPA2604	P/P
NE5534	Signetics	OPA604	P/P
OMA2541	Omnirel	OPA2541	P/P
OMA501	Omnirel	OPA501	P/P
OMA502	Omnirel	OPA502	P/P
OMA511	Omnirel	OPA511	P/P
OMA512	Omnirel	OPA512	P/P
OMA541	Omnirel	OPA541M	P/P
MP7610AN	MicroPower Systems	DAC7610P	P/P
MP7610AS	MicroPower Systems	DAC7610U	P/P
MP7610BN	MicroPower Systems	DAC7610PB	P/P
MP7610BS	MicroPower Systems	DAC7610UB	P/P
MP7611AE	MicroPower Systems	DAC7611U	P/P
MP7611BE	MicroPower Systems	DAC7611UB	P/P
MP7612AN	MicroPower Systems	DAC7612P	P/P
MP7612AS	MicroPower Systems	DAC7612U	P/P
MP7612BN	MicroPower Systems	DAC7612PB	P/P
MP7612BS	MicroPower Systems	DAC7612UB	P/P
MP7613AE	MicroPower Systems	DAC7613U	P/P
MP7613BE	MicroPower Systems	DAC7613UB	P/P
OP-01	PMI (Analog Devices)	OPA606KM	C/P
OP-04	PMI (Analog Devices)	OPA2111AM	C/P
OP-05	LTC	OPA27GJ	F/E
OP-05	PMI (Analog Devices)	OPA27GJ	F/E
OP-05	Raytheon/LTC	OPA27GJ	F/E
OP-05	Raytheon	OPA27GJ	F/E
OP-06	PMI (Analog Devices)	OPA37GJ	C/P
OP-07	LTC	OPA177GZ	P/P
OP-07	PMI (Analog Devices)	OPA177GZ	P/P
OP-07	Raytheon/LTC	OPA177GZ	P/P
OP-07	Raytheon	OPA177GZ	P/P
OP-08	PMI (Analog Devices)	OPA111AM	C/P
OP-10	PMI (Analog Devices)	OPA2111AM	C/P
OP-111	PMI (Analog Devices)	OPA111AM	P/P
OP-14	PMI (Analog Devices)	OPA2111AM	C/P
OP-15	LTC	OPA606KM	P/P
OP-15	PMI (Analog Devices)	OPA606KM	P/P
OP-16	LTC	OPA606KM	P/P
OP-16	PMI (Analog Devices)	OPA606KM	P/P
OP-177	PMI (Analog Devices)	OPA177GP	P/P
OP-17	LTC	OPA606KM	F/E
OP-17	PMI (Analog Devices)	OPA606KM	F/E
OP-200	PMI (Analog Devices)	OPA1013	C/P
OP-207	PMI (Analog Devices)	OPA2111AM	C/P
OP-215	PMI (Analog Devices)	OPA2111AM	C/P
OP-220	PMI (Analog Devices)	OPA1013	C/P
OP-220	PMI (Analog Devices)	OPA2111AM	C/P
OP-221	PMI (Analog Devices)	OPA2111AM	C/P
OP-227	LTC	OPA2111AM	C/P
OP-227	PMI (Analog Devices)	OPA2111AM	C/P
OP-237	LTC	OPA2111AM	C/P
OP-260	PMI (Analog Devices)	OPA603AP	C/P
OP-275	PMI (Analog Devices)	OPA2604	F/E
OP-27	PMI (Analog Devices)	OPA27GJ	P/P
OP-27	Raytheon	OPA27GJ	P/P
OP-285	PMI (Analog Devices)	OPA2107	F/E
OP-297	PMI (Analog Devices)	OPA1013	C/P
OP-37	PMI (Analog Devices)	OPA37GJ	P/P
OP-37	Raytheon	OPA37GJ	P/P
OP-400	PMI (Analog Devices)	OPA404AG	C/P
OP-41	PMI (Analog Devices)	OPA103	F/E
OP-41	PMI (Analog Devices)	OPA111AM	F/E

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
OP-420	PMI (Analog Devices)	OPA404AG	C/P
OP-421	PMI (Analog Devices)	OPA404AG	C/P
OP-42	PMI (Analog Devices)	OPA101	C/P
OP-42	PMI (Analog Devices)	OPA602AM	F/E
OP-43	PMI (Analog Devices)	OPA111AM	F/E
OP-44	PMI (Analog Devices)	OPA602AM	C/P
OP-470	PMI (Analog Devices)	OPA404AG	C/P
OP-47	Raytheon	OPA37GJ	F/E
OP-50	PMI (Analog Devices)	OPA27GJ	C/P
OP-77	PMI (Analog Devices)	OPA77EZ	P/P
OP-80	PMI (Analog Devices)	OPA128JM	F/E
OP-80	PMI (Analog Devices)	OPA128JM	F/E
OP07	LTC	OPA177	P/E
OP471	PMI (Analog Devices)	OPA404	F/E
PA01	Apex	OPA511AM	P/P
PA02	Apex	OPA541AM	C/P
PA07	Apex	OPA512BM	C/P
PA08	Apex	3583JM	C/P
PA10	Apex	OPA512BM	F/E
PA11	Apex	OPA511AM	P/P
PA12A	Apex	OPA512SM	P/P
PA12	Apex	OPA502	P/P
PA12	Apex	OPA512BM	P/P
PA25	Apex	OPA2541	C/P
PA51	Apex	OPA501AM	P/P
PA61	Apex	OPA512BM	C/P
PA73	Apex	3573AM	P/P
PA80	Apex	3580J	P/P
PA81	Apex	3581J	P/P
PA82	Apex	3582J	P/P
PA83	Apex	3583JM	P/P
PA84	Apex	3584JM	P/P
PM155A	PMI (Analog Devices)	OPA156AM	P/P
PM156A	PMI (Analog Devices)	OPA156AM	P/P
PM157A	PMI (Analog Devices)	OPA606KM	F/E
PM2108A	PMI (Analog Devices)	OPA2111AM	C/P
PM725	PMI (Analog Devices)	OPA27GJ	F/E
PM747	PMI (Analog Devices)	OPA2111AM	C/P
PM7541	PMI (Analog Devices)	DAC7541AJP	P/P
PM7545	PMI (Analog Devices)	DAC7545AH	P/P
PM8012	PMI (Analog Devices)	DAC7545AH	F/E
RC1458	Raytheon	OPA2111AM	C/P
RC2041	Raytheon	OPA2111AM	C/P
RC2043	Raytheon	OPA2111AM	C/P
RC4136	Raytheon	OPA404AG	C/P
RC4153	Raytheon	VFC320BM	C/P
RC4156	Raytheon	OPA404AG	C/P
RC4558	Raytheon	OPA2111AM	Pin
RC4559	Raytheon	OPA2111AM	Compatibility
RC4560	Raytheon	OPA2111AM	C/P
RC4562	Raytheon	OPA2111AM	C/P
RC4739	Raytheon	OPA2111AM	C/P
RC5532	Raytheon	OPA2111AM	C/P
RC5534	Raytheon	OPA37GJ	F/E
RC714	Raytheon	OPA27GJ	P/P
RC747	Raytheon	OPA2111AM	C/P
REF-01	LTC	REF102AM	F/E
REF01	Maxim	REF102AM	P/P
REF01	PMI (Analog Devices)	REF102AM	P/P
REF02AH	LTC	REF02RM	P/P
REF02AJ	Analog Devices	REF02RM	P/P
REF02AJ	Maxim	REF02RM	P/P

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
REF02CCSA	Maxim	REF02AU	P/P
REF02CH	LTC	REF02AM	P/P
REF02CJ8	LTC	REF02AG	P/P
REF02CJ	Analog Devices	REF02AM	P/P
REF02CJ	Analog Devices	REF02AM	P/P
REF02CJ	Maxim	REF02AM	P/P
REF02CN8	LTC	REF02AP	P/P
REF02CP	Analog Devices	REF02BP	P/P
REF02CP	Maxim	REF02BP	P/P
REF02CS	Analog Devices	REF02BU	P/P
REF02CZ	Analog Devices	REF02AG	P/P
REF02CZ	Maxim	REF02AG	P/P
REF02DCSA	Maxim	REF02AU	P/P
REF02DH	LTC	REF02AM	P/P
REF02DJ8	LTC	REF02AG	P/P
REF02DJ	Analog Devices	REF02AM	P/P
REF02DJ	Maxim	REF02AM	P/P
REF02DN8	LTC	REF02AP	P/P
REF02DP	Analog Devices	REF02AP	P/P
REF02DP	Maxim	REF02AP	P/P
REF02DZ	Analog Devices	REF02AG	P/P
REF02DZ	Maxim	REF02AG	P/P
REF02EH	LTC	REF02CM	P/P
REF02EH	LTC	REF02CM	P/P
REF02EJ8	LTC	REF02BG	P/P
REF02EJ	Analog Devices	REF02CM	P/P
REF02EJ	Maxim	REF02CM	P/P
REF02EN8	LTC	REF02BP	P/P
REF02EZ	Analog Devices	REF02BG	P/P
REF02EZ	Maxim	REF02BG	P/P
REF02HCSA	Maxim	REF02BU	P/P
REF02HH	LTC	REF02BM	P/P
REF02HJ8	LTC	REF02BG	P/P
REF02HJ	Analog Devices	REF02BM	P/P
REF02HJ	Analog Devices	REF02BM	P/P
REF02HJ	Maxim	REF02BM	P/P
REF02H	LTC	REF02SM	P/P
REF02HN8	LTC	REF02BP	P/P
REF02HP	Analog Devices	REF02BP	P/P
REF02HP	Maxim	REF02BP	P/P
REF02HZ	Analog Devices	REF02BG	P/P
REF02HZ	Maxim	REF02BG	P/P
REF02J	Analog Devices	REF02SM	P/P
REF02J	Maxim	REF02SM	P/P
REF02		REF02	P/P
REF05		REF05	P/P
REF10	Micro Power Systems	REF10KM	P/P
REF10	PMI (Analog Devices)	REF10KM	P/P
SHA1A	Analog Devices	SHC85	F/E
SHA21	Analog Devices	SHC803BM	F/E
SHA2A-5A	Analog Devices	SHC804BM	F/E
SHC85	Analog Devices	SHC85	P/P
SHM-20	Datel	SHC5320KH	P/P
SHM-4860	Datel	SHC804BM	P/P
SHM-6	Datel	SHC5320KH	C/P
SHM-9	Datel	SHC5320KH	C/P
SHM-HU	Datel	SHC804BM	C/P
SHM-IC-1	Datel	SHC298AM	C/P
SHM-LM-2	Datel	SHC298AM	P/P
SHM360	Datel	SHC600	F/E
SHM361	Datel	SHC601BH	F/E
SM5813	NPC	DF1700	P/P

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
SMP-10	PMI (Analog Devices)	SHC298AM	F/E
SMP-11	PMI (Analog Devices)	SHC298AM	F/E
SMP-81	PMI (Analog Devices)	SHC5320KH	C/P
SP9345	Sipex	DAC4813	F/E
SP7920	SPT	ADS605	C/P
SSM-2015	PMI (Analog Devices)	INA103AG	F/E
SSM-2016	PMI (Analog Devices)	INA103AG	F/E
SSM-2017	PMI (Analog Devices)	INA103AG	F/E
SSM-2141	Analog Devices	INA105	P/P
TDC1012	PMI (Analog Devices)	DAC65JP	F/E
TEA2114	Thomson	MPC100AP	C/P
TEA6415	Thomson	MPC100AP	C/P
THA-0523	DDC	SHC804BM	P/P
THC1201	TRW	ADC603JH	F/E
TL071	Texas Instruments	OPA604	P/E
TL072	Texas Instruments	OPA2604	P/E
TL072	Texas Instruments	OPA2604	P/E
TL081	Motorola	OPA604	P/P
TL082	Texas Instruments	OPA2604	P/P
TL084	Texas Instruments	OPA404KP	P/P
TL087	Texas Instruments	OPA604	F/E
TL088	Texas Instruments	OPA604	F/E
TLO71	Motorola	OPA604	P/P
TLO72	Motorola	OPA2107	C/P
TP4002	Teledyne-Philbrick	DAC71-COB-V	F/E
TP4855	Teledyne-Philbrick	SHC803BM	F/E
TP4860	Teledyne-Philbrick	SHC804BM	P/P
TPADC85	Teledyne-Philbrick	ADC85H-12	P/P
TPADC87	Teledyne-Philbrick	ADC87H-12	P/P
VA033	VTC	OPA633KP	P/P
VLN-3755	Sprague	OPA2541AM	C/P
ZAD354	Zeltex	DAC71-C0B-V	F/E
ZAD7100	Zeltex	ADC80AG-12	F/E
ZAD7400	Zeltex	ADC76JG	F/E
ZAD8000	Zeltex	DAC70BH-COB-I	F/E
ZD354	Zeltex	DAC71-C0B-V	F/E
ZD364	Zeltex	DAC71-C0B-V	F/E
ZD384	Zeltex	DAC71-C0B-V	F/E
ZD394	Zeltex	DAC71-C0B-V	F/E
ZDA160	Zeltex	DAC729JH	F/E
VC5601DWP	Unitrode	REG5601	P/P

CROSS REFERENCE GUIDE

B

Appendix C

Tape and Reel Specifications

For users of automatic pick and place equipment, surface mount devices are available in embossed carrier tape and reel.

Burr-Brown uses the highest quality materials available in its Tape and Reel packaging. The documented packaging process meets EIA481-A requirements.

The following illustrates tape sizes, mechanical orientation (polarization), quantity per 13" reel and reel dimensions.

Use Table I to determine tape and reel sizes and quantities.

PACKAGE NUMBER[1]	TAPE WIDTH W (mm)	PART PITCH P (mm)	DEVICES PER 13" Reel
178	24	16	1000
182	12	8	2500
211	16	12	1000
217	24	12	1000
219	24	16	1000
221	24	12	1000
235	16	8	2500
239	24	12	1000
248	24	12	1000
311	12	8	2500

NOTE: (1) Package number for any Burr-Brown product can be found in each product data sheet in the table titled, "Package Information".

TABLE I.
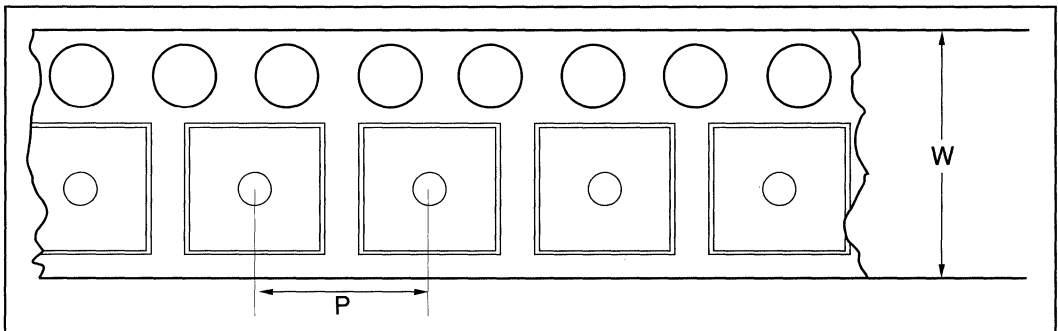
FIGURE 1.

User Direction of Feed

FIGURE 2.

TAPE AND REEL SPECIFICATIONS
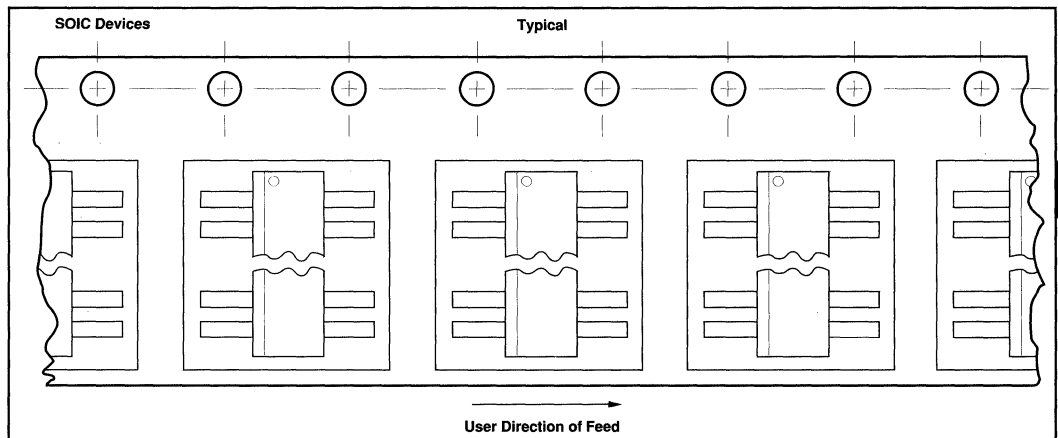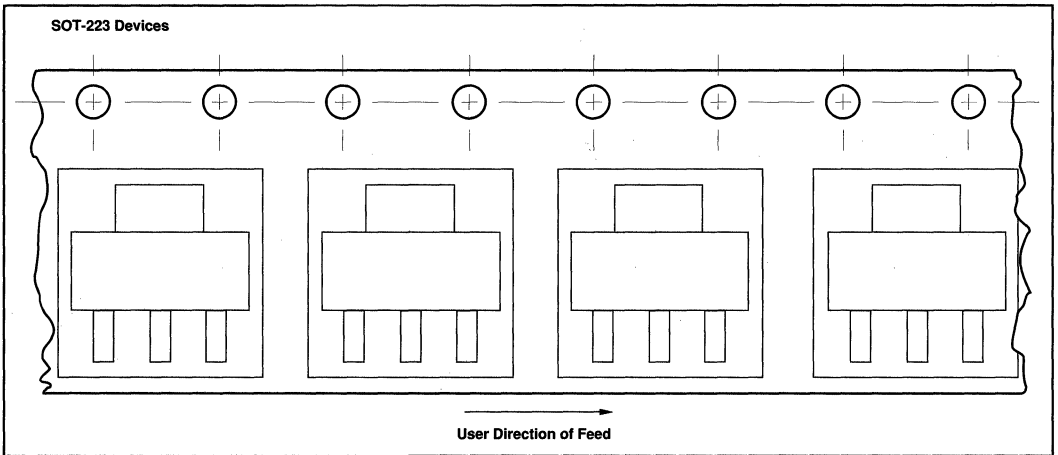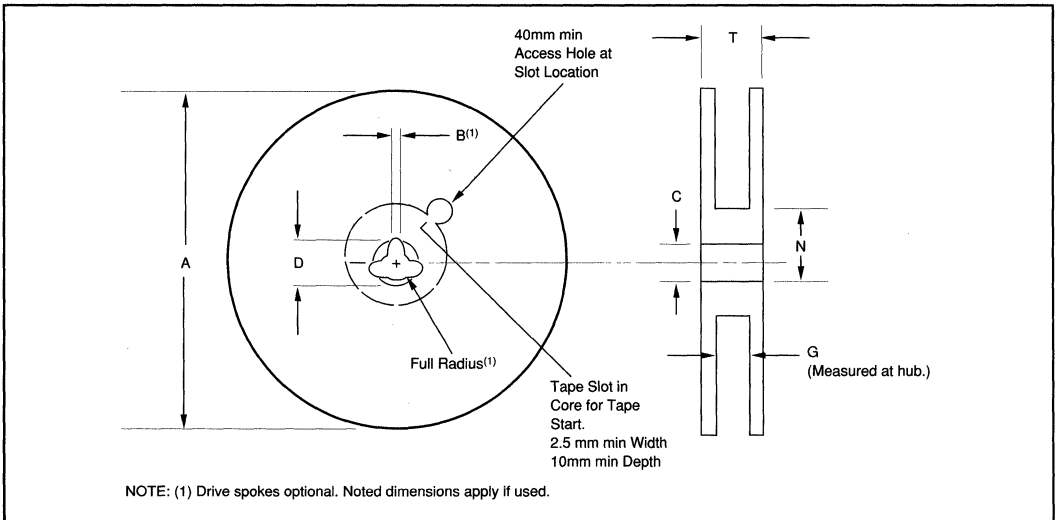
FIGURE 3.

FIGURE 4.

TAPE SIZE	A MAX	B MAX	C	D MIN	N MIN	G	T MAX
12mm	330mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	12.4 + 1.0 (–0.0mm)	18.4mm
16mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	16.4 + 1.0 (–0.08mm)	22.4mm
24mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	24.4 + 1.0 (–0.00mm)	30.4mm

TABLE II.

Appendix D

Package Drawings (Mechanicals)

Package Number 001 — Metal TO-99
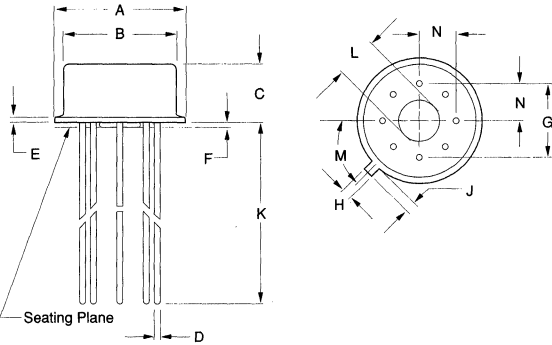
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 006 — 8-Pin Plastic Single-Wide DIP
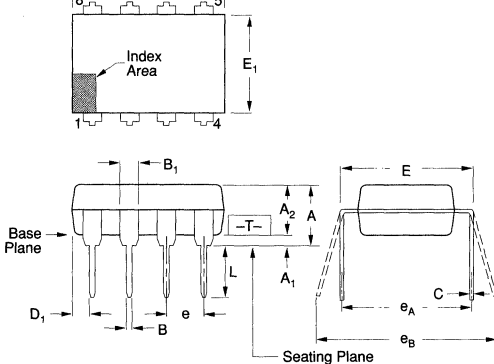
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (3)	—	.210	—	5.33
A₁ (3)	.015	—	0.38	—
A₂	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B₁	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D (4)	.348	.430	8.84	10.92
D₁	.005	—	0.13	—
E (5)	.300	.325	7.62	8.26
E₁ (4)	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
eₐ (5)	.300 BASIC		7.63 BASIC	
e_B (6)	—	.430	—	10.92
L (3)	.115	.160	2.92	4.06
N (7)	8		8	

(1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(3) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and eₐ measured with the leads constrained to be perpendicular to plane T.
(6) eB is measured at the lead tips with the leads unconstrained.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 4, 5, and 8) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.


Package Number 007 — TO-100
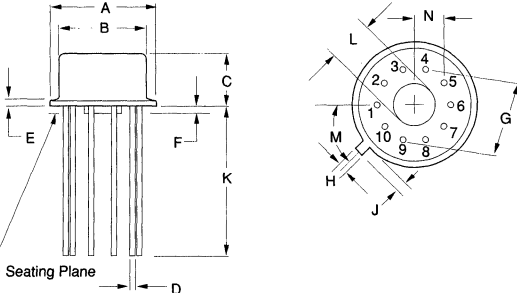
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

MECHANICALS

D

Package Number 010 — 14-Pin Plastic Single Wide DIP
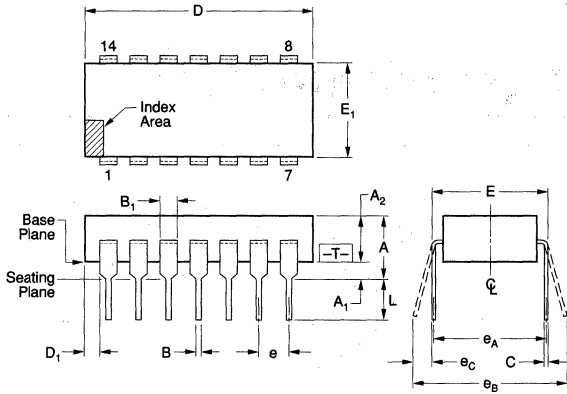
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A[3]	—	.210	—	5.33
A$_1$[3]	.015	—	0.38	—
A$_2$	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B$_1$	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D[4]	.725	.795	18.42	20.19
D$_1$	.005	—	0.13	—
E[5]	.300	.325	7.62	8.26
E$_1$[4]	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e$_A$[5]	.300 BASIC		7.63 BASIC	
e$_B$[6]	—	.430	—	10.92
L[3]	.115	.160	2.92	4.06
N[7]	14		14	

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.

(3) Dimensions A, A$_1$, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E$_1$ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and e$_A$ measured with the leads constrained to be perpendicular to plane T.
(6) e$_B$ and e$_C$ are measured at the lead tips with the leads unconstrained. e$_C$ must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

Package Number 107— 14-Pin
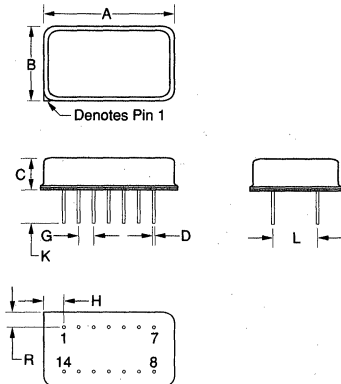
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Package Number 113 — 24-Pin
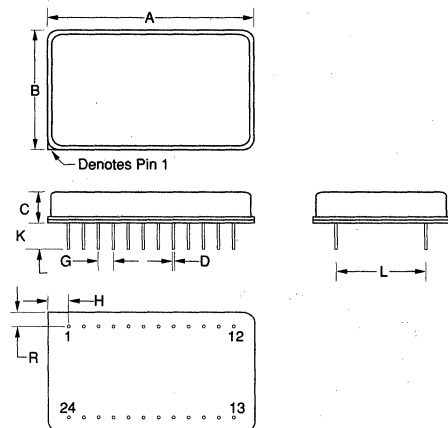
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

Package Number 116 — 32-Pin DIP

Denotes Pin 1
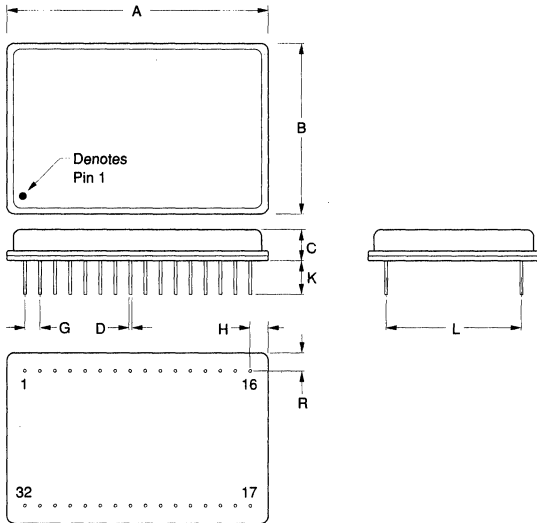
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
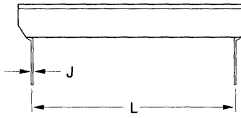
Package Number 125 — 24-Pin Ceramic DIP

Seating Plane
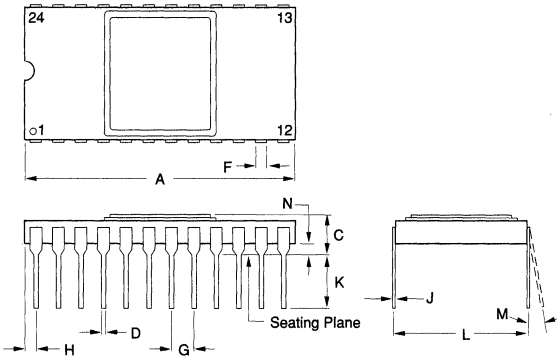
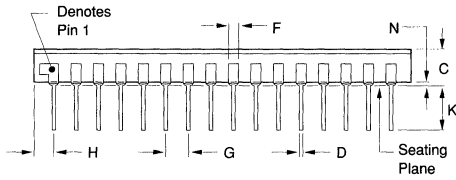|	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 129 — 16-Pin Ceramic DIP

Denotes Pin 1

Seating Plane
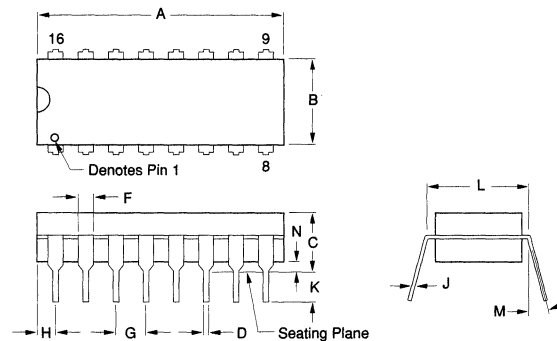
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.753	.885	19.30	22.48
B	.280	.295	7.11	7.50
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on the package.

MECHANICALS

D

Package Number 137 — 14-Pin Hermetic DIP
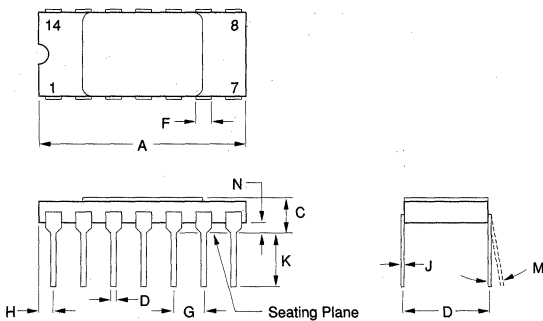
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 144-1 — 28-Pin Hermetic DIP
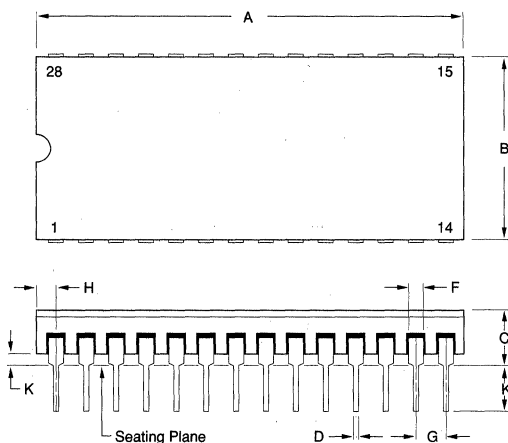
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.465	35.20	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.210	4.06	5.33
D	.015	.019	0.38	0.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.035	.095	0.89	2.41
J	.008	.012	0.20	0.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.020	.060	0.51	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 149 — 28-Pin Hermetic Ceramic DIP
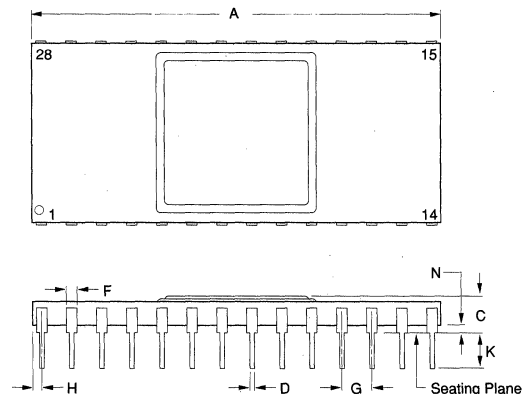
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 153 — 32-Pin Ceramic Bottom-Braze
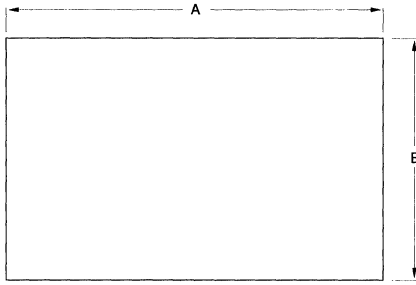
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Package Number 163 — 14-Pin Side-Braze Ceramic
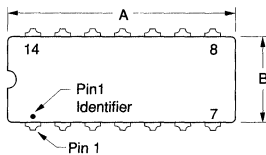
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.753	.767	19.13	19.48
B	.280	.295	7.12	7.50
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.085	—	2.16
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTES: (1) Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
(2) Pin numbers shown for reference only. May not be marked on the package.
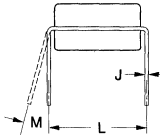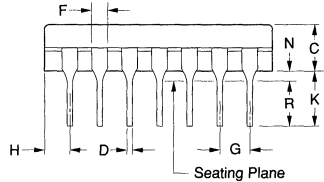
Package Number 165 — 24-Lead Ceramic Side Braze DIP, .600 Row Spacing
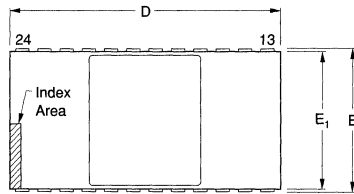
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.085	.190	2.16	4.83
A1	.020	.070	0.51	1.78
B	.015	.023	0.38	0.58
B1	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	1.180	1.220	29.97	30.99
E	.595	.625	15.11	15.88
E1(6)	.575	.610	14.61	15.49
e1(2)	.100 TYPICAL		2.54 TYPICAL	
eA(2)	.600 TYPICAL		15.24 TYPICAL	
L	.125	.175	3.18	4.45
N(4)	24		24	
Q1	.010	—	2.54	—
S	.030	.065	0.76	1.65
α(3)	0°	15°	0°	15°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5-1973.
(2) Leads within .13mm (.005in) radius of true position (TP) with maximum material condition.
(3) α applies to spread leads prior to installation.
(4) N is the number of terminal positions.
(5) Outlines on which the seating plane is coincident with the base plane (A1 = 0), terminals lead standoffs are not required, and B1 may equal B along any part of the lead above the seating/base plane.
(6) E1 does not include particles of packing materials.
(7) Controlling dimension: Inch.

MECHANICALS

D
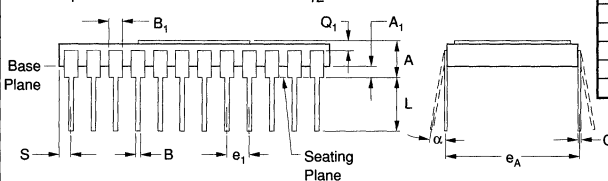
Package Number 167 — 24-Pin Plastic Double-Wide DIP
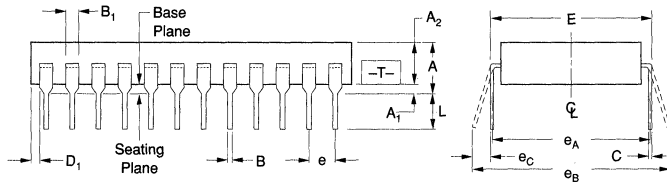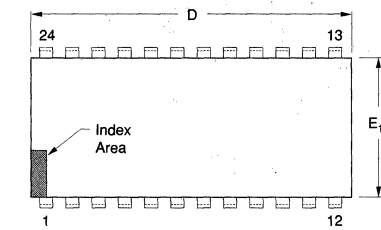
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (3)	—	.250	—	6.35
A₁ (3)	.015	—	0.38	—
A₂	.125	.195	3.18	4.95
B	.014	.022	0.36	0.56
B₁	.030	.070	1.14	1.78
C	.008	.015	0.20	0.38
D (4)	1.150	1.290	29.21	32.77
D₁	.005	—	0.13	—
E (5)	.600	.625	15.24	15.88
E₁ (4)	.485	.580	12.32	14.73
e	.100 BASIC		2.54 BASIC	
eA (5)	.600 BASIC		15.24 BASIC	
eB (6)	—	.700	—	17.78
L (3)	.115	.200	2.92	5.08
N (7)	24		24	

NOTES:
(1) Controlling dimension: INCH. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(3) Dimensions A, A₁ and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and eA measured with the leads constrained to be perpendicular to plane T.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 12, 13, and 24) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

Package Number 172-2 — 32-Pin Side-Braze Ceramic with Metal Lid
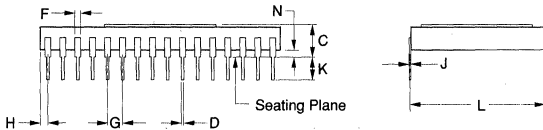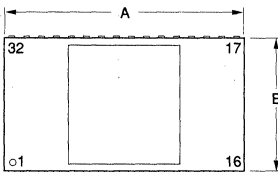
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYPICAL		1.02 TYPICAL	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

## Package Number 172-5 — 32-Pin Side-Braze Ceramic with Metal Lid
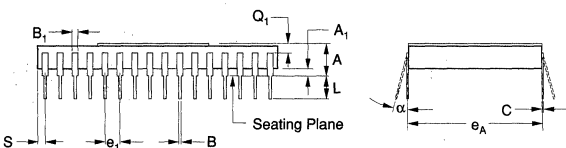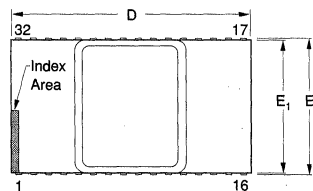
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.145	.195	3.68	4.95
A₁	.040	.060	1.02	1.52
B	.015	.023	0.38	0.58
B₁	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	1.580	1.620	40.13	41.15
E	.900	.920	22.86	23.37
E₁	.885	.905	22.48	22.99
e₁ (6)	.100 TYPICAL		2.54 TYPICAL	
eA (2)	.900 TYPICAL		22.86 TYPICAL	
L (2)	.125	.175	3.18	4.45
N (4)	32		32	
Q₁	.010	—	2.54	—
S	.030	.065	0.76	1.65
α (3)	0°	15°	0°	15°

NOTE: (1) Dimensioning and tolerancing per ANSI Y14.5-1973.
(2) Leads within 0.13mm (.005") radius of true position (TP) with maximum material condition.
(3) α applies to spread leads prior to installation.
(4) N is the number of terminal positions.
(5) Outlines on which the seating plane is coincident with the base plane (A₁ = 0), terminals lead standoffs are not required, and B₁ may equal B along any part of the lead above the seating plane.
(6) E₁ does not include particles of package materials.
(7) Controlling dimension: Inch.

Package Number 178 — 24-Pin SOIC
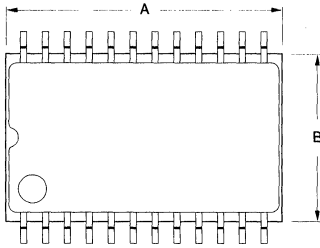
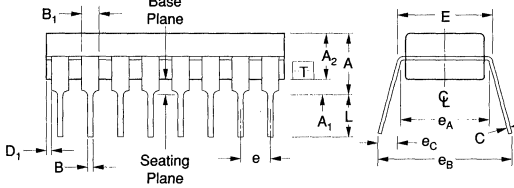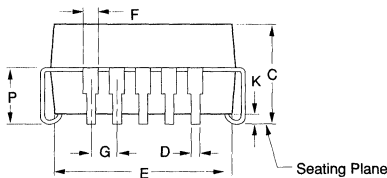| DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.614	.630	15.60	16.00
B	.346	.362	8.80	9.20
C	—	.098	—	2.50
D	.012	.020	0.30	0.50
G	.046	.054	1.17	1.37

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
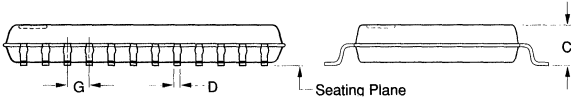
Package Number 180 — 16-Pin Plastic, Single-Wide DIP
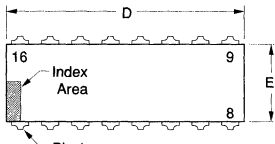
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A [1]	—	.210	—	5.33
A₁ [1]	.015	—	0.38	—
A₂	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B₁	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D [2]	.745	.840	18.92	21.34
D₁	.005	—	0.13	—
E [3]	.300	.325	7.62	8.26
E₁ [2]	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
eA [3]	.300 BASIC		7.62 BASIC	
eB [4]	—	.430	—	10.92

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L [1]	.115	.160	2.92	4.06
N [5]	16		16	

(1) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(2) D and E₁ dimensions for plastic packages do not include mold flash or protursions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(3) E and eₐ are measured with the leads constrained to be perpendicular to plane T.
(4) eᵦ and e_c are measured at the lead tips with the leads unconstrained. e_c must be zero or greater.
(5) N is the maximum number of terminal positions.
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Package Number 181 — 20-Pin LCC
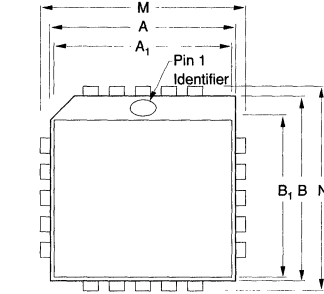
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.350	.356	8.89	9.04
A₁	.338	.344	8.59	8.74
B	.350	.356	8.89	9.04
B₁	.290	.330	7.37	8.38
C	.165	.180	4.19	4.57
D	.013	.021	0.33	0.53
E	.290	.330	7.37	8.38
F	.026	.032	0.66	0.81
G	.050 BASIC		1.27 BASIC	
K	.020	—	0.51	—
M	.385	.395	9.78	10.03
N	.385	.395	9.78	10.03
P	.090	.120	2.29	3.05

MECHANICALS

D

Package Number 182 — 8-Pin SO-8 Surface Mount
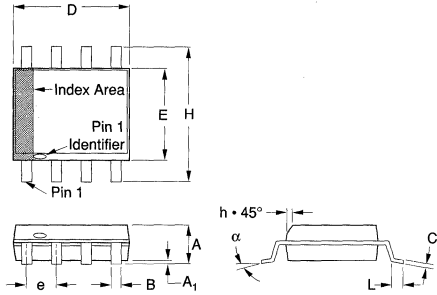
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.054	.068	1.37	1.73
A₁	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.

Package Number 211 — 16-Lead SOIC
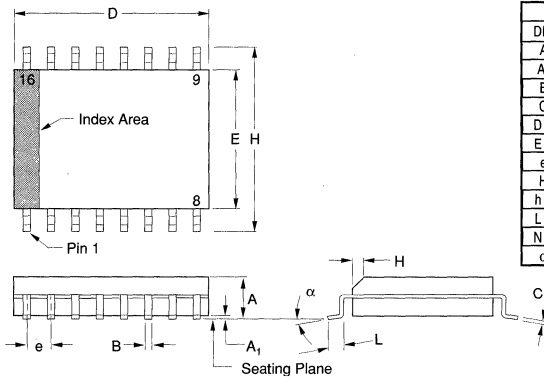
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.093	.104	2.36	2.64
A₁	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D (1)	.398	.413	10.11	10.49
E (1)	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h (2)	.010	.029	0.25	0.74
L (3)	.016	.050	0.41	1.27
N (4)	16		16	
α	0°	8°	0°	8°

(1) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.086in.).
(2) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
(3) L is the length of terminal for soldering to a substrate.
(4) N is the number of terminal positions.

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Package Number 212 — 32-Pin Side-Braze Ceramic with Metal Lid
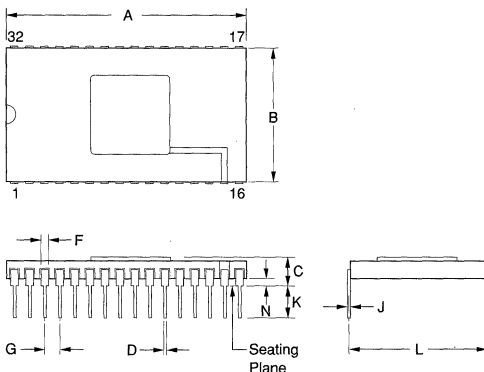
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.584	1.616	40.23	41.05
B	.885	.905	22.48	22.99
C	.124	.166	3.15	4.22
D	.016	.020	0.41	0.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.900 BASIC		22.86 BASIC	
N	.040	.060	1.02	1.52

Package Number 214 — 40-Pin Hermetic DIP
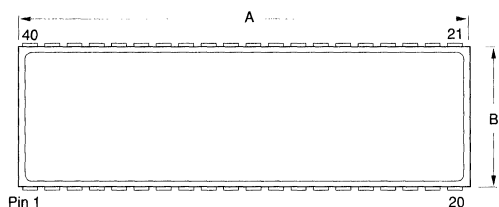
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.980	2.040	50.29	51.82
B	.610	.630	15.49	16.00
C	.150	.200	3.81	5.08
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.009	.012	0.23	0.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
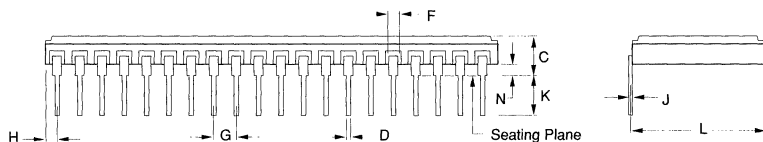
Package Number 215 — 28-Pin Plastic, Double-Wide DIP
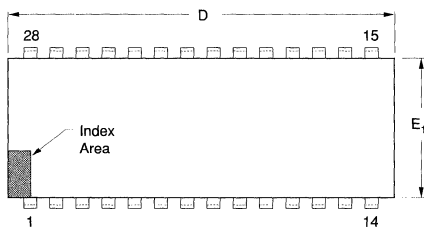
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A [3]	—	.250	—	6.35
A₁ [3]	.015	—	0.38	—
A₂	.125	.195	3.18	4.95
B	.014	.022	0.36	0.56
B₁	.030	.070	0.76	1.78
C	.008	.015	0.20	0.38
D [4]	1.380	1.565	35.05	39.75
D₁	.005	—	0.13	—
E [5]	.600	.625	15.24	15.88
E₁ [4]	.485	.580	12.32	14.73
e	.100 BASIC		2.54 BASIC	
eₐ [5]	.600 BASIC		15.24 BASIC	
e_B [6]	—	.700	—	17.78
L [3]	.115	.200	2.92	5.08
N [7]	28		28	

NOTES:
(1) Controlling dimension: INCH. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(3) Dimensions A, A₁ and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and eₐ measured with the leads constrained to be perpendicular to plane T.
(6) e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 14, 15, and 28) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.
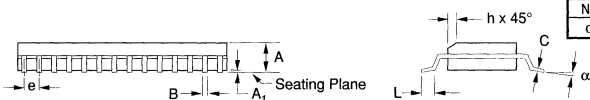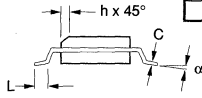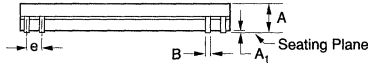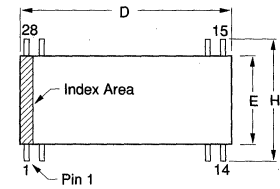
Package Number 217 — 28-Lead SOIC

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.093	.104	2.36	2.64
A₁	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D [2]	.697	.712	17.70	18.08
E [2]	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h [3]	.010	.029	0.25	0.74
L [4]	.016	.050	0.41	1.27
N [5]	28		28	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(2) "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in).
(3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
(4) "L" is the length of terminal for soldering to a substrate.
(5) "N" is the number of terminal positions.
(6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

MECHANICALS

D

Package Number 217-1 — 28-Lead SOIC, ISO Package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A1	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D(2)	.697	.712	17.70	18.08
E(2)	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h(3)	.010	.029	0.25	0.74
L(4)	.016	.050	0.41	1.27
N(5)	8		8	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M–1982.
(2) "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in).
(3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
(4) "L" is the length of terminal for soldering to a substrate.
(5) "N" is the number of terminal positions.
(6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

**Package Number 218 — 18-Pin Plastic Single-Wide DIP**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A (3)	—	.210	—	5.33
A1 (3)	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D (4)	.845	.925	21.46	23.50
D1	.005	—	0.13	—
E (5)	.300	.325	7.62	8.26
E1 (4)	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
eA (5)	.300 BASIC		7.63 BASIC	
eB (6)	—	.430	—	10.92
L (3)	.115	.160	2.92	4.06
N (7)	18		18	

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M–1982.
(3) Dimensions A, A1, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E1 dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and eA measured with the leads constrained to be perpendicular to plane T.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 9, 10, and 18) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines

Package Number 219 — 18-Lead SOIC
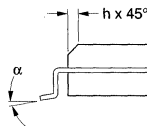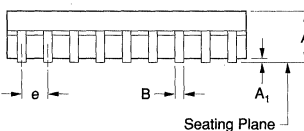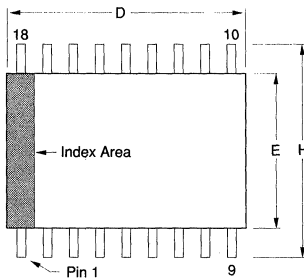
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A1	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D(2)	.447	.462	11.35	11.73
E(2)	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h(3)	.010	.029	0.25	0.74
L(4)	.016	.050	0.41	1.27
N(5)	18		18	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M–1982.
(2) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086in).
(3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
(4) L is the length of terminal for soldering to a substrate.
(5) N is the number of terminal positions.
(6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

Package Number 221— 20-Lead SOIC
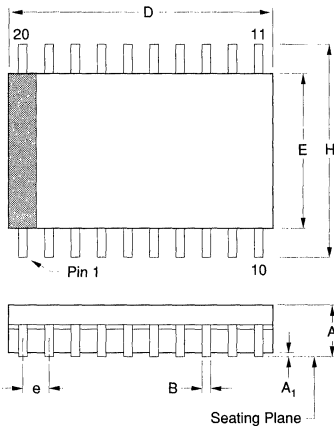
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A$_1$	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D$^{(2)}$	.497	.511	12.62	12.98
E$^{(2)}$	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h$^{(3)}$	.010	.029	0.25	0.74
L$^{(4)}$	.016	.050	0.41	1.27
N$^{(5)}$	20		20	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(2) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086in).
(3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
(4) L is the length of terminal for soldering to a substrate.
(5) N is the number of terminal positions.
(6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

**Package Number 222 — 20-Pin Plastic Single-Wide DIP**
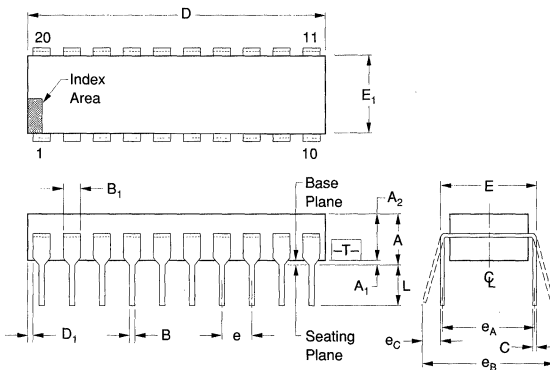
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A $^{(3)}$	—	.210	—	5.33
A$_1$ $^{(3)}$	.015	—	0.38	—
A$_2$	.115	.195	2.92	4.95
B	.014	.022	0.36	0.59
B$_1$	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D $^{(4)}$	.925	1.060	23.50	26.92
D$_1$	.005	—	0.13	—
E $^{(5)}$	.300	.325	7.62	8.26
E$_1$ $^{(4)}$	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e$_A$ $^{(5)}$	.300 BASIC		7.63 BASIC	
e$_B$ $^{(6)}$	—	.430	—	10.92
L $^{(3)}$	.115	.160	2.92	4.06
N $^{(7)}$	20		20	

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M–1982.
(3) Dimensions A, A$_1$, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E$_1$ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or prorusions shall not exceed .010 inch (0.25mm).
(5) E and e$_A$ measured with the leads constrained to be perpendicular to plane T.
(6) e$_B$ and e$_C$ are measured at the lead tips with the leads unconstrained. e$_C$ must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 10, 11, and 20) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines

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Package Number 228 — 28-Pin Side-Braze Ceramic
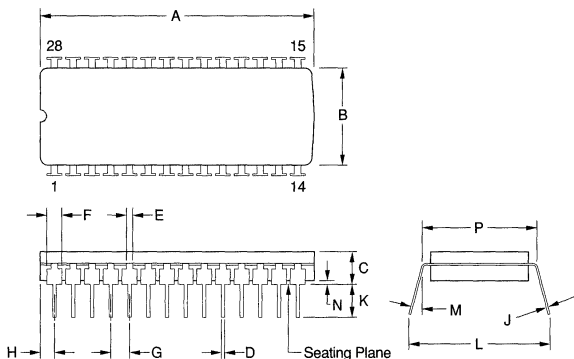
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.440	1.460	36.57	37.08
B	.514	.526	13.06	13.36
C	.155	.193	3.94	4.90
D	.018 TYPICAL		0.46 TYPICAL	
E	.035 TYPICAL		0.89 TYPICAL	
F	.080 TYPICAL		2.03 TYPICAL	
G	.100 BASIC		2.54 BASIC	
H	.070	.080	1.78	2.03
J	.0098	.0102	0.249	0.259
K	.175 BASIC		4.45 BASIC	
L	.645	.675	16.38	17.15
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56
P	.608	.614	15.44	15.60

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICALS

D

Package Number 230 — 40-Pin Ceramic DIP
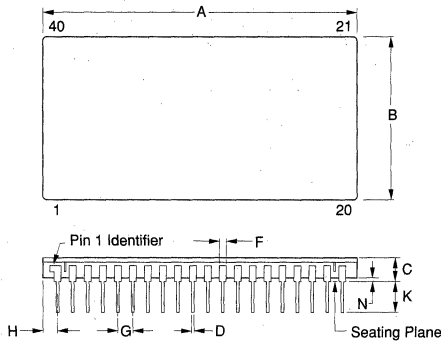
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.075	2.115	52.71	53.72
B	1.080	1.100	27.43	27.94
C	.145	.175	3.68	4.45
D	.018 TYPICAL		0.46 TYPICAL	
F	.040 TYPICAL		1.02 TYPICAL	
G	.100 TYPICAL		2.54 TYPICAL	
H	.093	.103	2.36	2.62
J	.020 BASIC		0.51 BASIC	
K	.205 BASIC		5.21 BASIC	
L	.900 BASIC		22.86 BASIC	
N	.015	.035	0.38	0.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 234 — 46-Lead
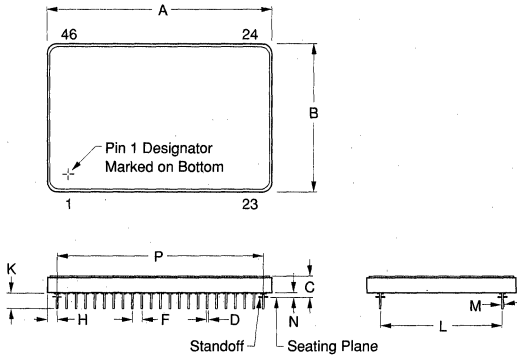
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.205	.251	5.21	6.38
D	.015	.021	0.38	0.53
F	.095	.105	2.41	2.67
H	.085	.105	2.16	2.67
K	.155	.185	3.94	4.70
L	1.290	1.310	32.77	33.27
M	—	10°	—	10°
N	.045	.055	1.14	1.40
P	2.190	2.210	55.63	56.13

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Package Number 235 — 14-Lead SOIC
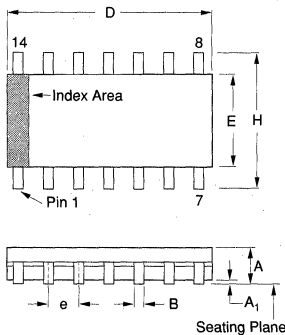
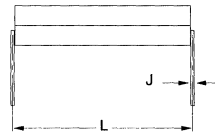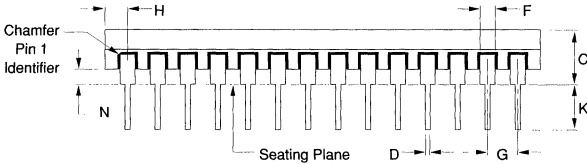| DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.054	.068	1.37	1.73
A₁	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D(2)	.337	.344	8.56	8.74
E(2)	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h(3)	.010	.019	0.25	0.48
L(4)	.016	.050	0.41	1.27
N(5)	14		14	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the shaded area.
4. L is the length of the terminal for soldering to a substrate.
5. N is the number of terminal positions.
6. Lead to lead coplanarity shall be less than 0.004 inches from the seating plane.

Package Number 237 — 28-Pin Ceramic DIP
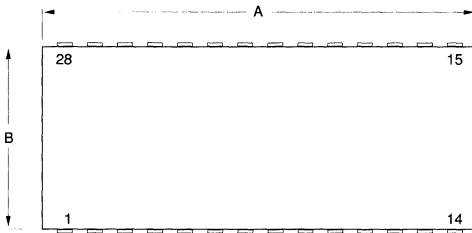
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
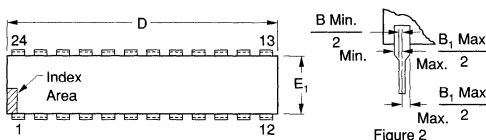
Package Number 239 — 24-Lead SOIC
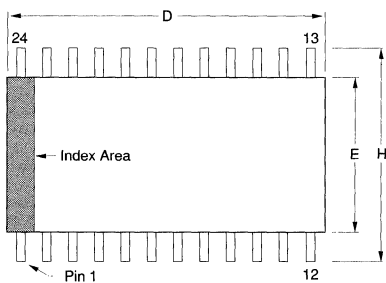
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.093	.104	2.36	2.64
A_1	.0040	.0118	0.10	0.30
B	.014	.019	0.36	0.48
C	.009	.012	0.23	0.30
$D^{(2)}$	.5985	.6140	15.20	15.60
$E^{(2)}$	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.395	.418	10.03	10.62
$h^{(3)}$	.010	.029	0.25	0.74
$L^{(4)}$	.016	.050	0.41	1.27
$N^{(5)}$	24		24	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982. (2) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086in). (3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area. (4) L is the length of terminal for soldering to a substrate. (5) N is the number of terminal positions. (6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.
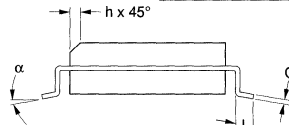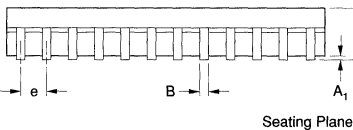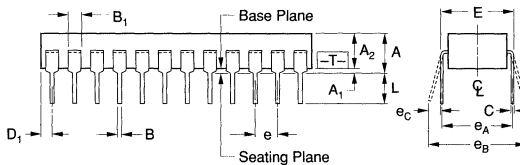
Package Number 243 — 24-Pin Plastic Single Wide DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
$A^{(3)}$	—	.210	—	5.33
$A_1^{(3)}$	.015	—	0.38	—
A_2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B_1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
$D^{(4)}$	1.125	1.275	28.58	32.39
D_1	.005	—	0.13	—
$E^{(5)}$	.300	.325	7.62	8.26
$E_1^{(4)}$	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
$eA^{(5)}$	.300 BASIC		7.63 BASIC	
$eB^{(6)}$	—	.430	—	10.92
$L^{(3)}$	.115	.160	2.92	4.06
$N^{(7)}$	24		24	

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

(2) Dimensioning and tolerancing per ANSI Y14.5M–1982. (3) Dimensions A, A_1, and L are measured with the package seated in JEDEC seating plane gauge GS-3. (4) D and E_1 dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm). (5) E and e_A measured with the leads constrained to be perpendicular to plane T. (6) e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater. (7) N is the maximum number of terminal positions. (8) Corner leads (1, 12, 13, and 24) may be configured as shown in Figure 2. (9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.
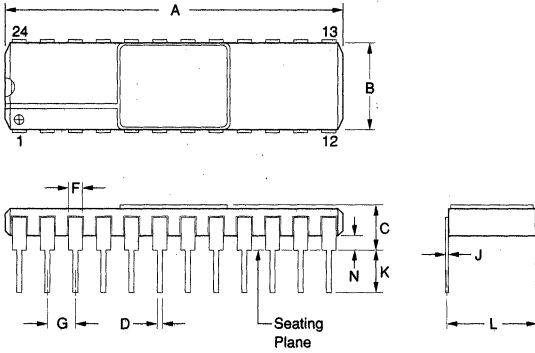
MECHANICALS

D

Package Number 245 — 24-Pin Side-Braze Ceramic with Metal Lid

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.188	1.212	30.18	30.78
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 TYPICAL		1.27 TYPICAL	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

Package Number 246 — 28-Pin Plastic Single Wide DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A [3]	—	.210	—	5.33
A1 [3]	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D [4]	1.320	1.380	33.53	35.05
D1	.005	—	0.13	—
E [5]	.300	.325	7.62	8.26
E1 [4]	.270	.295	6.86	7.49
e	.100 BASIC		2.54 BASIC	
eA [5]	.300 BASIC		7.62 BASIC	
eB [6]	—	.430	—	10.92
L [3]	.115	.160	2.92	4.06
N [7]	28		28	

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(3) Dimensions A, A1, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E1 dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and eA measured with the leads constrained to be perpendicular to plane T.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

Package Number 247 — 0.3" 28-Pin Hermetic DIP
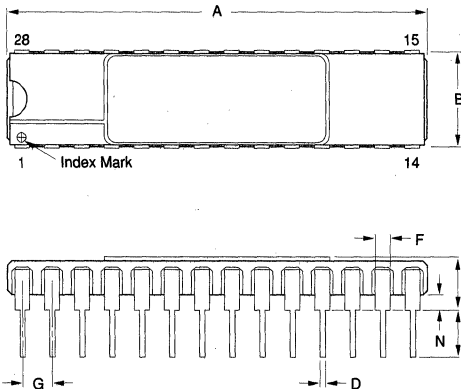
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 248 — 20-Pin Plastic SOIC
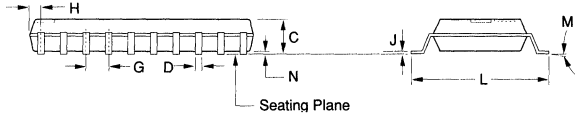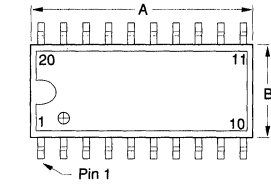
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.494	.498	12.55	12.65
B	.206	.210	5.23	5.33
C	.071	.077	1.80	1.96
D	.013	.017	0.33	0.43
G	.050 BASIC		1.27 BASIC	
H	.021	.025	0.53	0.64
J	.0076	.0082	0.19	0.21
L	.303	.311	7.70	7.90
M	3°	5°	3°	5°
N	.002	.006	0.05	0.15

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 251 — 28-Pin LCC
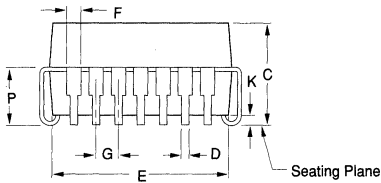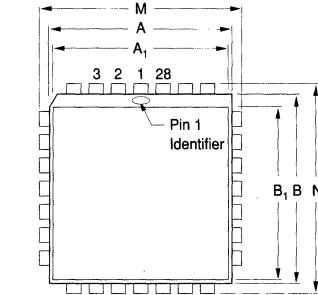
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.450	0.460	11.43	11.68
A₁	0.450	0.460	11.43	11.68
B	0.450	0.460	11.43	11.68
B₁	0.450	0.460	11.43	11.68
C	0.165	0.180	4.19	4.57
D	0.013	0.023	0.33	0.58
E	0.390	0.430	9.91	10.92
F	0.026	0.032	0.66	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.015	0.025	0.38	0.64
M	0.485	0.495	12.32	12.57
N	0.485	0.495	12.32	12.57
P	0.100	0.110	2.54	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 252 — 40-Pin Plastic SOIC
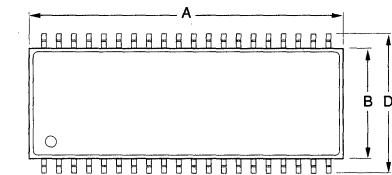
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.036	1.059	26.30	26.90
B	.362	.378	9.20	9.60
C	.099	.107	2.50	2.70
D	.453	.476	11.50	12.10
E	.042	.058	1.07	1.47
F	.012	.020	0.30	0.50
G	.043	.051	1.10	1.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

MECHANICALS

D

Package Number 256 — 68-Lead with Gull Wings

0.020 x 45°
Pin 1 Indicator

0.040 x 45°
3 Places

Seating Plane
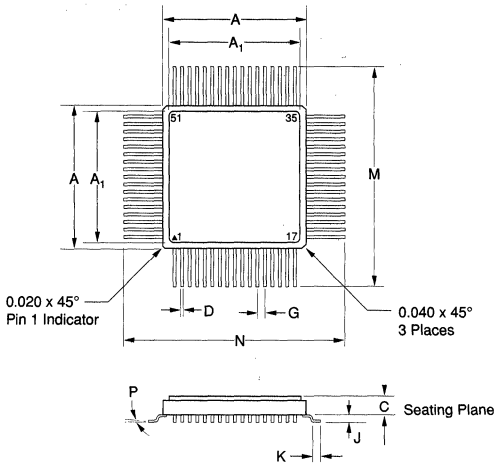
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.940	.960	23.88	24.38
A₁	.865	.875	21.97	22.23
C	.200 REF		4.81 REF	
D	.013	.025	0.33	0.64
G	.050 BASIC		1.27 BASIC	
J	.045	.055	1.14	1.40
K	.045 REF		1.14 REF	
M	1.200	1.220	30.48	30.99
N	1.200	1.220	30.48	30.99
P	0°	6°	0°	6°

NOTE: Formed leads shall be planar with respect to one another within 0.004 max at seating plane.

Package Number 265 — 16-Pin PDIP

Index Area

Pin 1

h • 45°

Seating Plane
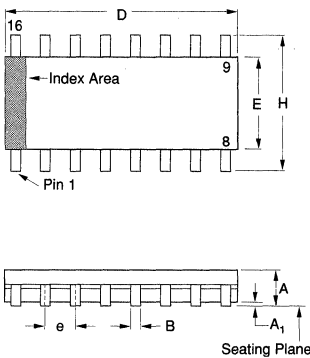
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A₁	.0040	.0098	0.10	0.25
B	.0138	.0192	0.35	0.49
C	.0075	.0098	0.19	0.25
D⁽²⁾	.3859	.3937	9.80	10.00
E⁽²⁾	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
H	.2284	.2440	5.80	6.20
h⁽³⁾	.0099	.0196	0.25	0.50
L⁽⁴⁾	.016	.050	0.41	1.27
N⁽⁵⁾	16		16	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14, 5M–1982.
2. "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the shaded area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.
6. Lead to lead coplanarity shall be less than 0.004 inches from the seating plane.

Package Number 266 — 18-Pin Side-Braze Ceramic

Index Area and
Terminal No. 1 ID Area

Base Plane

Seating Plane
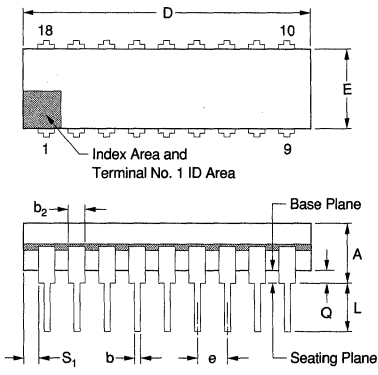
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	.200	—	5.08
b	.014	.026	0.36	0.66
b₂	.045	.065	1.14	1.65
C	.008	.018	0.20	0.46
D	—	.960	—	24.38
E	.220	.310	5.59	7.87
e	.100 BASIC		2.54 BASIC	
eₐ	.300 BASIC		7.62 BASIC	
eₐ/2	.150 BASIC		3.81 BASIC	
L	.125	.200	3.18	5.08
N	18		18	
Q	.015	.070	0.38	1.78
S₁	.005	—	0.13	—
α	90°	105°	90°	105°

NOTE: Dimensions are MIL-STD-1835 Compliant (Ref GDIP-P188, D-6).

Package Number 312-1 — 68-Pin Plastic Quad
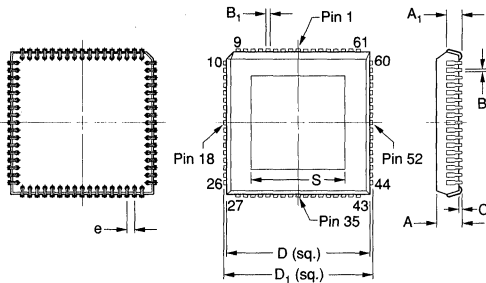
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.167	.177	4.24	4.50
A$_1$	.100	.110	2.54	2.79
B	.016	.020	0.41	0.51
B$_1$	.026	.032	0.66	0.81
C	.020	.025	0.51	0.64
D	.985	.995	25.02	25.27
D$_1$(2)	.950	.958	24.13	24.33
e	.050 BASIC		1.27 BASIC	
N	68		68	
S	.618	.628	15.70	15.95

NOTES: (1) All dimensions and tolerances conform to ANSI Y14.5M-1982.

(2) Dimension D$_1$ does not include mold protrusion. Allowable mold protrusion is .254mm/.010 inch.

(3) Controlling Dimension: Inch.

Package Number 317 — 28-Pin Plastic Dual-In-Line
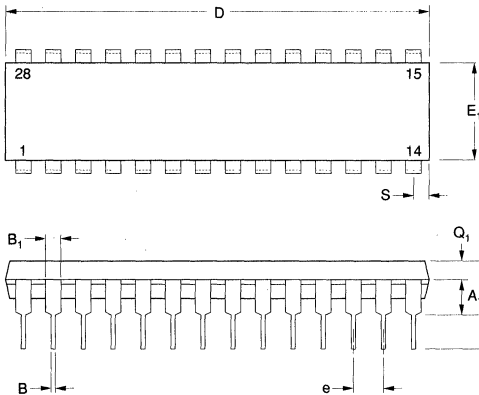
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A(3)	.130	.230	3.30	5.84
A$_1$(3)	.015	—	0.381	—
B	.014	.023	0.356	0.584
B$_1$(8)	.038	.065	0.965	1.65
C	.008	.015	0.203	0.381
D(4)	1.340	1.485	34.04	37.72
E(5)	.400	.425	10.16	10.80
E$_1$(4)	.265	.385	9.27	9.78
e	.100 BASIC		2.54 BASIC	
L(3)	.115	.160	2.92	4.06
α	0°	15°	0°	15°
Q$_1$	.055	.070	1.40	1.78
S	.020	.100	0.508	2.54

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(3) Dimensions A, A$_1$, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E$_1$ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E is measured at the lead tips with the leads constrained to be perpendicular to plane T.
(6) Corner leads (1, 14, 15, and 28) may be configured as shown in Figure 2.
(7) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
(8) The minimum limit for dimensions B$_1$ may be .023" (0.58mm) for all four corner leads only.

Package Number 318 — 28-Lead Small Outline
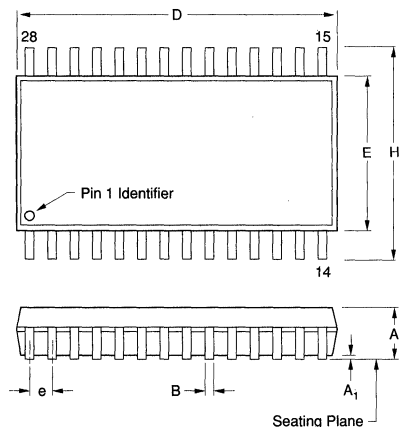
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.090	.100	2.286	2.54
A$_1$	.004	.010	0.102	0.279
B	.014	.020	0.356	0.508
C	.006	.0125	0.152	0.318
D(2)	.706	.718	17.93	18.24
E(2)	.340	.350	8.64	8.89
e	.050 BASIC		1.27 BASIC	
H	.463	.477	11.76	12.12
L(4)	.020	.042	0.406	0.889
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(2) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086in).
(3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
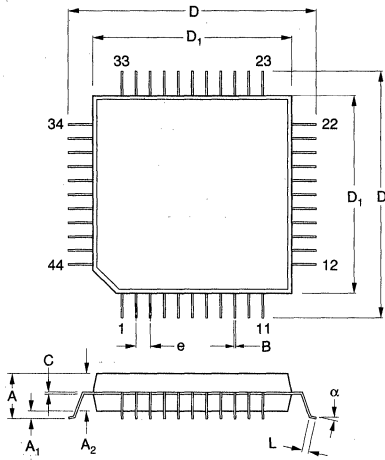(4) L is the length of terminal for soldering to a substrate.
(5) N is the number of terminal positions.
(6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

MECHANICALS

D

Package Number 319 — 44-Lead Plastic Quad Flat Pack

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	.124	—	3.15
A1	.010	—	0.25	—
A2	.102	.110	2.60	2.80
B	.012	.016	0.30	0.40
C	.005	.009	0.13	0.23
D	.667	.687	16.95	17.45
D1	.547	.555	13.90	14.10
e	.039 BASIC		1.00 BASIC	
L	.026	.040	0.65	1.03
α	0°	7°	0°	7°

Package Number 800 — 28-Pin Plastic, DIP
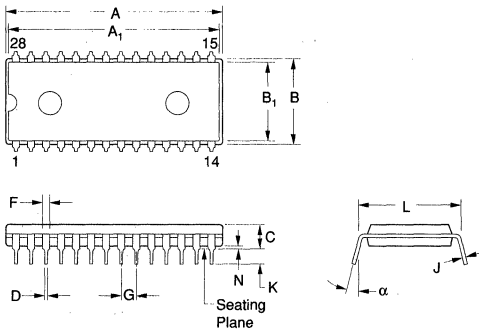
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	1.441	—	36.60
A1	1.402 TYPICAL		35.6 TYPICAL	
B	—	.236	—	14.6
B1	.528 TYPICAL		13.4 TYPICAL	
C	—	.224	—	5.70
D	.016	.017	0.42	0.44
F	.047 BASIC		1.20 TYPICAL	
G	.090	.110	2.29	2.79
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.600 BASIC		15.24 BASIC	
α	0°	15°	0°	15°
N	.020	—	0.51	—

Package Number 801 — 28-Pin Plastic DIP
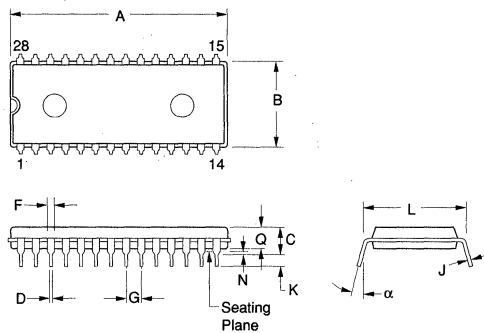
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.417	1.449	36.00	36.80
B	.516	.539	13.10	13.70
C	—	.224	—	5.70
D	.015	.023	0.38	0.58
G	.100 TYPICAL		2.54 TYPICAL	
J	.006	.014	0.15	0.35
K	.098	—	2.50	—
L	.600 TYPICAL		15.24 TYPICAL	
N	.020	—	0.50	—
Q	—	.224	—	5.70
α	0°	15°	0°	15°

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BB

Package Number 802 — 16-Pin Plastic DIP
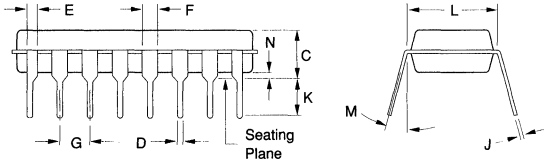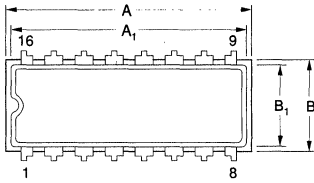
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	.800	—	20.32
A₁	.740	.772	18.80	19.60
B	—	.291	—	7.40
B₁	.234	.262	5.95	6.65
C	—	.199	—	5.06
D	.015	.023	0.38	0.58
E	.035 TYP		0.89 TYP	
F	.059 TYP		1.50 TYP	
G	.100 TYP		2.54 TYP	
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 TYP		7.62 TYP	
M	0°	15°	0°	15°
N	.020	—	0.51	—

Package Number 803 — 16-Pin SOIC
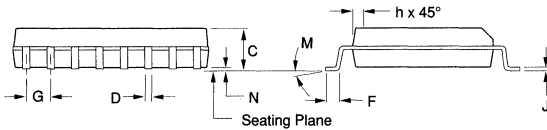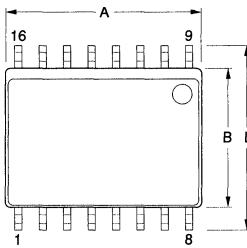
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.402	.408	10.21	10.36
B	.292	.298	7.42	7.60
C	.094	.104	2.39	2.64
D	.014	.020	0.35	0.51
G	.050 BASIC		1.27 BASIC	
h	.010	.016	0.25	0.41
J	.009	.013	0.23	0.32
L	.398	.416	10.11	10.57
M	0°	8°	0°	8°
N	.004	.012	0.10	0.30

(1) Lead frame: DLIN 194.
(2) Lead finish: Solder plated.
(3) Back ejector pin marked "Korea".
(4) Both package length and width do not include flash.
(5) Formed lead shall be planar with respect to one another within 0.004 inches.
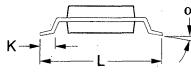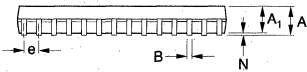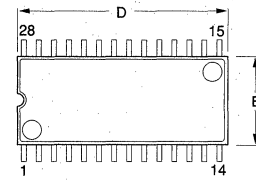
Package Number 804 — 28-Pin Plastic SOIC
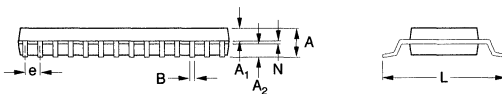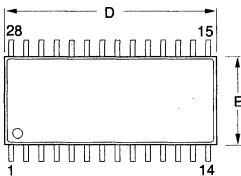
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.31	2.39
A₁	.050 BASIC		1.045 BASIC	
A₂	.050 BASIC		1.045 BASIC	
B	.0095	.012	0.35	0.48
D	.697	.712	17.81	18.06
E	.292	.299	7.42	7.62
e	.050 BASIC		1.27 BASIC	
N	.016	.050	0.23	0.32
L	.398	.414	10.11	10.51

MECHANICALS

D

Package Number 805 — 28-Pin Plastic SOIC

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.118	—	3.00
A₁	.096	.108	2.45	2.75
B	.012	.020	0.30	0.50
D	.709	.732	18.00	18.60
E	.323	.339	8.20	8.60
e	.050 TYPICAL		1.27 TYPICAL	
K	.039 BASIC		1.00 BASIC	
L	.449	.480	11.40	12.20
N	.000	.008	0.00	0.20
α	0°	10°	0°	10°

Package Number 806 — 28-Pin Plastic SOIC
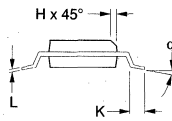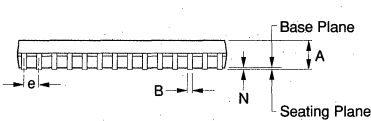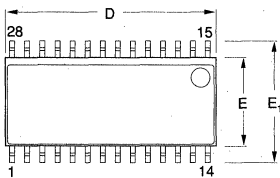
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.094	.104	2.39	2.64
B	.0138	.020	0.35	0.51
D	.702	.709	17.83	17.98
E	.292	.298	7.42	7.57
E₁	.398	.416	10.11	10.57
e	.050 BASIC		1.27 BASIC	
H	.010	.016	0.25	0.41
K	.016	.035	0.41	0.89
L	.0091	.0125	0.231	0.318
N	.004	.0118	0.10	0.30
α	0°	8°	0°	8°

NOTES: (1) Lead frame. (2) Lead finish, solder plated. (3) Back ejector pin marked "KOREA." (4) Both package length and width do not include flash. (5) Formed lead shall be planar with respect to one another within 0.004 inches. (6) Controlling dimension: Inches.

Package Number 807 — 16-Pin Plastic DIP
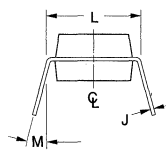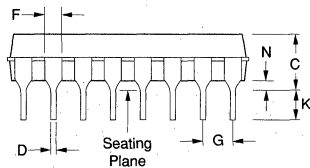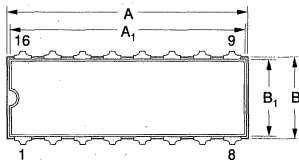
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	.800	—	20.32
A₁	.724	.787	18.4	20.0
B	—	.291	—	7.40
B₁	.234	.262	5.95	6.65
C	—	.200	—	5.06
D	.016	.020	0.41	0.51
F	.059 BASIC		1.50 BASIC	
G	.090	.110	2.29	2.79
J	.007	.015	0.19	0.38
K	.100		2.54	
L	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.020	—	0.51	—

Package Number 808 — 20-Pin Plastic SOP
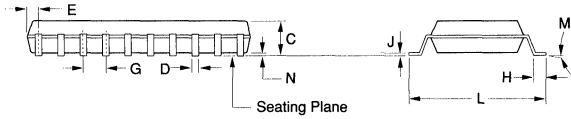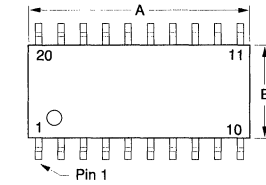
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	.512	—	13.00
B	.213 BASIC		5.40 BASIC	
C	—	.087	—	2.20
D	.012	.019	0.30	0.50
E	—	.031	—	0.80
G	.044	.056	1.12	1.42
H	.019	.035	0.50	0.90
J	.004	.012	0.10	0.30
L	.295	.319	7.50	8.10
M	0°	10°	0°	10°
N	0	.0078	0	0.20

Package Number 809 — 28-Pin Plastic SOIC
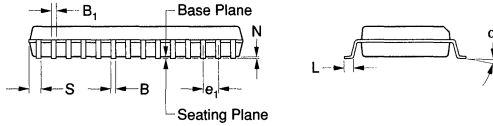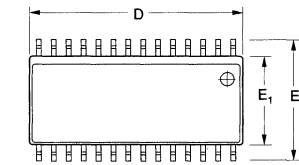
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
B	.014	.017	0.36	0.42
D	—	.714	—	18.13
E	.398	.414	10.11	10.51
E₁	.292	.300	7.42	7.62
e₁	.050 TYPICAL		1.27 TYPICAL	
L	.023 TYPICAL		0.58 TYPICAL	
N	.002	.008	0.05	0.20
S	.028 TYPICAL		0.71 TYPICAL	
α	5° TYPICAL		5° TYPICAL	

Package Number 904 — 28-Pin Ceramic DIP
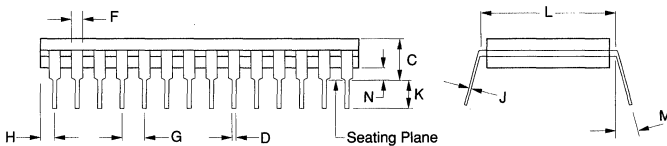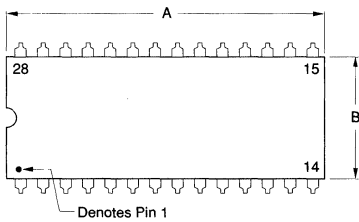
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.360	1.470	34.54	37.34
B	.500	.590	12.70	14.99
C	.169	.200	4.29	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.015	0.18	0.38
K	.100	.150	2.54	3.81
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.020	.090	0.51	2.29

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.

MECHANICALS

D

Package Number 905 — 28-Pin Plastic, Dual-Wide DIP

Denotes Pin 1
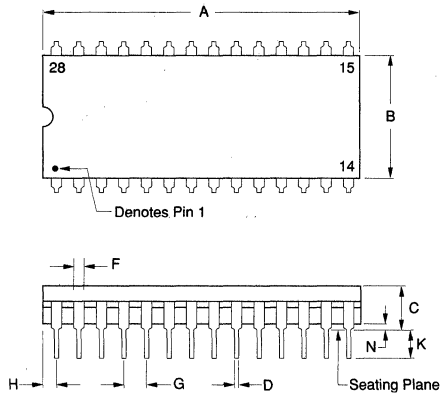
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.350	1.470	34.29	37.34
B	.520	.575	13.21	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.065	1.09	1.65
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.150	2.54	3.81
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.015	.040	0.38	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.


Package Number 906

Pin 1 Identification
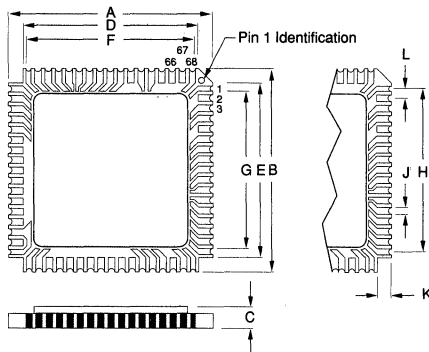
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.945	.965	24.003	24.511
B	.945	.965	24.003	24.511
C	.076	.094	1.934	2.388
D	.841	.859	21.361	21.819
E	.841	.859	21.361	21.819
F	.755	.785	19.177	19.939
G	.755	.785	19.177	19.939
H	.800 BASIC		20.320 BASIC	
J	.027	.033	.686	.838
K	.045 BASIC		1.143 BASIC	
L	.050 BASIC		1.270 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

TERMINATION: Gold plated nickel on refractory metallization.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 4.37 grms (0.124 oz)

Package Number 907

TOP VIEW   **Bottom VIEW**

Pin 1 Identifier
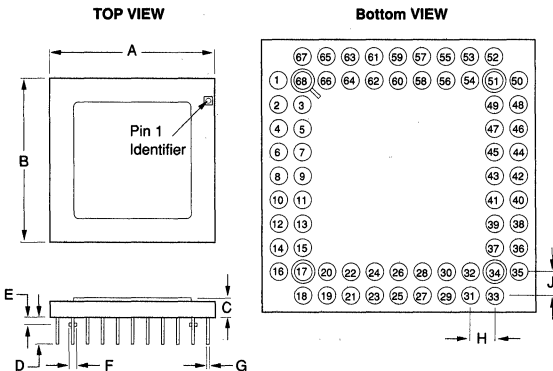
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.095	.120	2.413	3.048
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100 BASIC		2.540 BASIC	
J	.100 BASIC		2.540 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
TERMINATION: Gold plated KOVAR.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 9 grms (0.32 oz)

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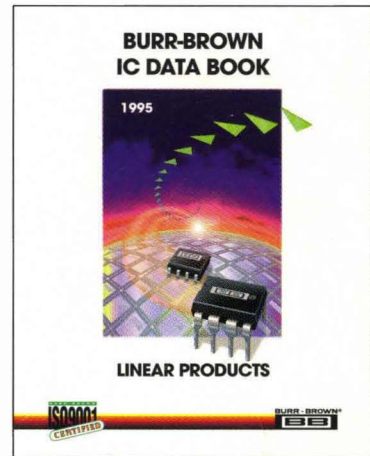Wauwatosa, WI
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