ISO9001 CERTIFIED

Mixed Signal Products

Burr-Brown IC Data Book

BURR - BROWN®

1996/1997

1996/1997

Mixed Signal Products

BURR - BROWN®

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For information on any of these products or to receive the *Burr-Brown Linear Products IC Data Book*, call our automated literature request line at 1-520-741-3884, or contact your local sales representative.

How to Use This Book

If you know the **MODEL NUMBER,**	Use the Model Index on the **INSIDE FRONT COVER.**
If you know the **PRODUCT TYPE,**	Use the **TABBED TABLE OF CONTENTS,** or use the **SELECTION GUIDE TABLES** at the front of each tabbed section.
If you want **NEW MODELS,**	Use the Model Index on the **INSIDE FRONT COVER** or the **SELECTION GUIDE TABLES** at the front of each tabbed section. All new models contained in this edition are shown in **boldface.** Also, contact your local Burr-Brown representative for information on new models released since publication of this data book.
If you want a **PRICE,**	Contact your local Burr-Brown office or sales representative. See the sales office listing at the back of the book.
If you want **TAPE & REEL,**	See **TAPE & REEL INFORMATION,** Appendix B, or contact your local Burr-Brown representative.

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1 Burr-Brown Corporation

About Burr-Brown

Corporate Profile

Burr-Brown Corporation designs, manufactures, and markets a broad line of high-performance, standard analog and mixed signal integrated circuits used in the processing of electronic signals. Our products are used in a wide range of markets and applications, including industrial and process control, test and measurement, medical and scientific instrumentation, medical imaging, digital audio and video, telecommunications, personal computers, and multimedia.

Our product strategy is to design proprietary circuits that yield maximum functional value in our customers' applications. Many of the products, although produced in standard configurations, are strategically designed, specified, and tested to position them for targeted applications such as audio signal processing or sensor-specific signal conditioning.

Burr-Brown's products include: operational amplifiers, instrumentation amplifiers, programmable gain amplifiers, isolation amplifiers, DC/DC converters, voltage references and regulators, voltage-to-frequency converters, optoelectronic amplifiers, analog-to-digital converters, digital-to-analog converters, and "application specific" standard products. Our products are manufactured using a variety of wafer fabrication processes that include bipolar, complementary bipolar, BiCMOS and CMOS with lithography requirements down to the 0.6 micron level.

We sell our products worldwide through our direct sales force, independent sales representatives, and third-party distributors. Burr-Brown has six direct sales offices in the United States and international sales subsidiaries in France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom. Through direct sales and distributors, our products reach over 25,000 OEM customers worldwide. Sales are divided evenly throughout the world, with approximately one-third from the United States market, one-third from Europe, and the remainder from Japan and the South East Asian region.

Burr-Brown employs over 1,900 people worldwide with manufacturing and technical facilities in Tucson, Arizona; Atsugi, Japan; and Livingston, Scotland. Located in Tucson, Arizona, corporate headquarters also includes an integrated circuit wafer fab, assembly and test operations. Burr-Brown was incorporated in Arizona in 1956; stock is traded on NASDAQ under the symbol, BBRC.

Burr-Brown Receives ISO9001 Certification in U.S. and Europe

In September 1993, Burr-Brown Corporation received ISO9001 certification in the United States and Europe, simultaneously. In the United States, registration is recognized through the TUV Product Service Quality Registrar by the Registration Accreditation Board (RAB). Certification is accepted through the Electronics Industries Quality Registrar by the Dutch Registration Board (RCV) in Europe.

ISO9001 is the international standard for assessing the quality systems of companies that design, manufacture, and test products. Adopted by 91 member countries, it's the international quality standard for manufacturing, trade, and communications industries. Certification indicates that a formal quality system exists for all processes and that these processes are audited on a timely basis.

Applications Library

Applications Bulletins and Design Software

APPLICATIONS LIBRARY

The following applications information is available from Burr-Brown at no charge.

Call 1-800-548-6132 to order.

APPLICATIONS BULLETINS

Increasing INA117 Differential Input Range AB-001
Make a Precision Current Source or Current Sink AB-002
Voltage-Reference Filters AB-003
Make a Precision –10V Reference AB-004
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Sales and Service

ABOUT THIS BOOK

To keep with the easy-to-use format we established last year, the *Burr-Brown Integrated Circuits Data Books* for 1996/97 will be similar to the 1995 books. Both the Linear Products and Mixed Signal Products books are available free from your local salesperson or representative—see **Sales Office Listings** at back of book—or by calling our literature request line at **1-800-548-6132** (US or Canada). Order both, or just the one that fits your needs.

How to Use This Book

Burr-Brown product numbers are listed in the Selection Trees and Tables at the beginning of each tabbed section. With these tools you can quickly compare specs among different products and choose the best part for your design. Products appearing in **boldface** type are new products introduced by Burr-Brown since publication of the 1995 data books.

Data sheets are arranged alphanumerically by product type, so if you know the name of the part you can find it quickly. Or, use the Product Index on the **inside front cover**, or page numbers as listed in the Selection Guide trees and tables.

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Burr-Brown is committed to providing the best customer service in the industry—whether it be a need for additional technical literature, technical assistance, to place an order, or to return products. For immediate assistance with any problem or inquiry, contact your local Burr-Brown salesperson or representative. See **Sales Office Listings** at back of book.

Direct factory assistance is available by calling the following number: **1-800-548-6132** (US or Canada; 7:00am to 5:00pm MST).

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In addition to individual data sheets, Burr-Brown also provides its customers with applications bulletins, promotional samples, comprehensive brochures featuring many product types, and applications assistance by calling **1-800-548-6132** (US or Canada).

Internet

Burr-Brown information is now available on the Internet via the World Wide Web. Customers with Internet access can visit our home page at **http://www.burr-brown.com/** to obtain on-line data sheets and corporate information any time of the day, any day of the year.

FAX*Line*

Burr-Brown's **FAX*Line*** is available for customers to request product literature. Call **1-800-548-6133** (USA/Canada Only) to receive a Document Catalog, complete with **FAX*Line*** literature order numbers. Up to three pieces of literature may be requested per call.

Prices and Quotations

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement. Please call your local sales representative or distributor (see list at the back of this book).

Placing Orders

You can place orders via telephone, FAX, or mail with any authorized Burr-Brown field sales office, sales representative, or authorized distributors. See **Sales Office Listings** at back of book for the office nearest you.

Sales and Service

Returns and Warranty Service

When returning products for any reason, contact Burr-Brown prior to shipping for authorization and shipping instructions. For complete instructions, contact your local salesperson or representative. Customers outside the USA should call the nearest sales office for details and information—see **International Sales Office Listing** at back of book.

To return product, please call for your Return Material Authorization (RMA) number. Ship units prepaid and supply the original purchase order number and date, along with an explanation for the return. Upon receipt of the returned devices, Burr-Brown will verify and inform you of the warranty status, cost to repair or replace, credits, and status of replacements where applicable.

2 A/D Converters, Data Acquisition Components

Burr-Brown's Analog-to-Digital (A/D) converter product line offers a broad selection of resolutions, 12-, 14-, and 16-bit for industrial applications, and 16-, 18-, and 20-bit designed especially for audio applications.

A new line of *SpeedPLUS*™ 10- and 12-bit resolution, 10-40MHz sampling rate A/D converters was recently introduced. The **ADS800** family of converters is fabricated on 0.6µm CMOS process, utilizing a leading-edge pipeline architecture. ADS800 converters are complete with a quantizer, wideband track/hold, internal reference, and three-state outputs.

ADS7819 is a 12-bit monolithic, 800kHz sampling A/D complete with an internal sample/hold, clock and internal 2.5V reference. It uses state-of-the-art CMOS structures, contains a parallel microprocessor interface, and has three-state output drivers.

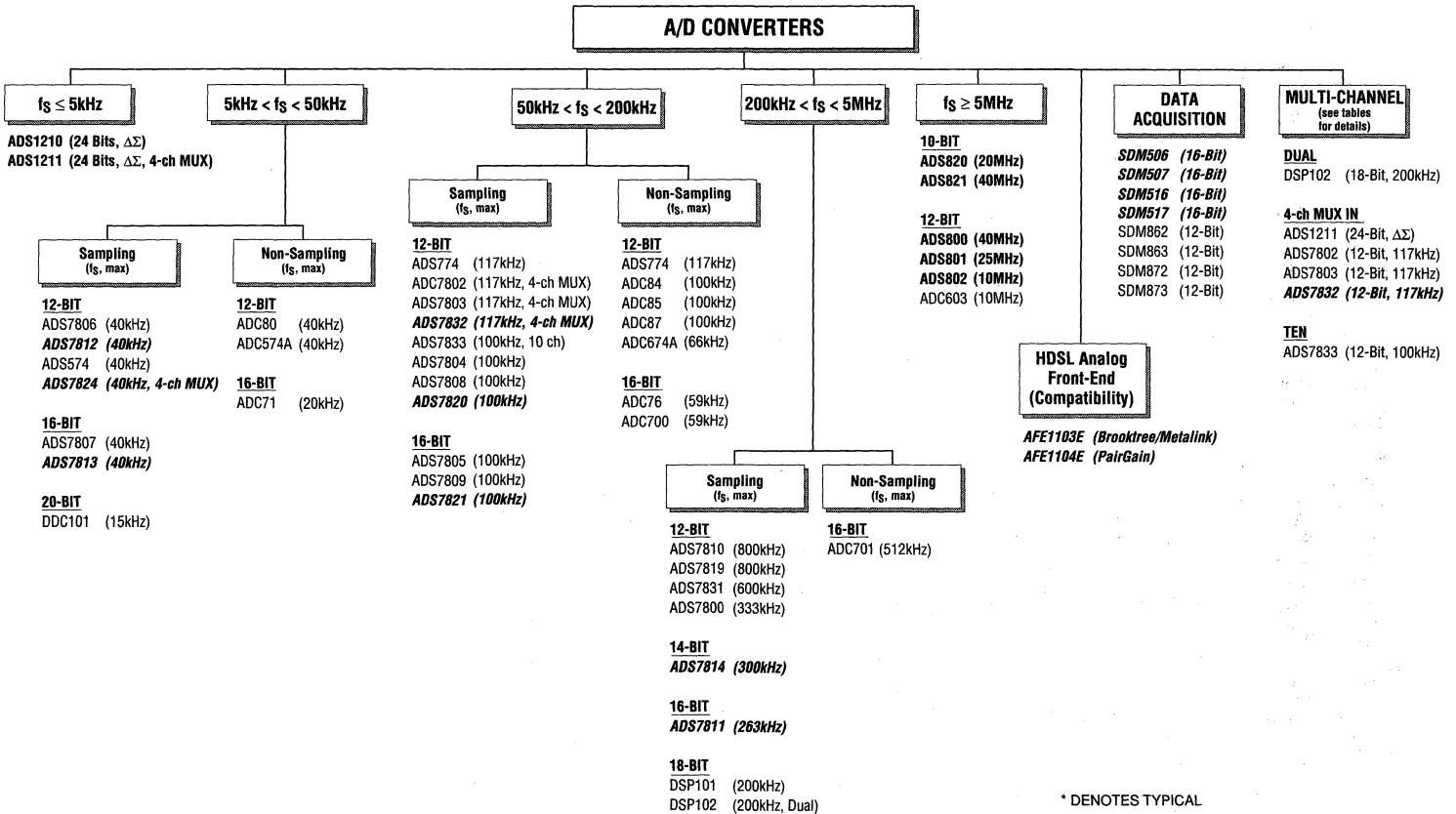
ADS7831 is a 12-bit monolithic, 600kHz sampling A/D complete with an internal sample/hold, clock and internal 2.5V reference. Its high spectral performance make it especially suitable for applications such as HDSL, modems, and wireless communication systems.

ADS7833 is a complete 10 channel data acquisition system—its three A/Ds operate simultaneously at a 150kHz per converter sample rate with up to five channels of simultaneous sample and hold channels—it also contains digitally programmable input ranges and an 8-bit voltage output.

ADS7820 is a new, complete 0-5V analog input 12-bit 100kHz sampling A/D converter. Part of a new generation of Burr-Brown sampling A/D converters, it offers faster sampling rates, multiple channels, lower power, and more analog input ranges.

ADS1210 and ADS1211 are precision, wide dynamic range, delta-sigma A/D converters with 24-bit resolution operating from a single +5V supply. Dynamic range is increased by the inclusion of a low-noise programmable gain amplifier with gain range of 1 to 16 in binary steps. Both converters include a flexible synchronous serial interface which is SPI compatible, and offers a two-wire control mode for low cost isolation.

The **DDC101** is a 20-bit, 15kHz integrating A/D converter with digital error correction and direct photosensor interface.



* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Product	Resolution (Bits)	Linearity Error max (%FSR)	Input Range (see table, pg 2.5) (V)	Sampling Rate (kHz)	NMC	THD (dB, max)	Temp Range[1]	Pkg[2]	Serial or Parallel	Description
ADC71	16	±0.003	D, E, F, N, R, S	20	14	—	Ind, Com	TDIP	S, P	Industry Std Pinouts
ADC76	16	±0.003	D, E, N, R, S	60	14	—	Ind, Com	TDIP	S, P	Industry Std Pinouts
ADC80AG	12	±0.012	D, E, N, R, S	40	12	—	Ind	TDIP	S, P	Industry Std Pinout and Interface Medium Speed Monolithic
ADC80MAH	12	±0.012	D, E, N, R, S	40	12	—	Ind	TDIP	S, P	Industry Std Pinout and Interface Medium Speed Monolithic
ADC84KG	12	±0.012	D, E, N, R, S	100	12	—	Ind	TDIP	S, P	Medium Speed
ADC85H	12	±0.012	D, E, N, R, S	100	12	—	Com	TDIP	S, P	Medium Speed
ADC87H	12	±0.012	D, E, N, R, S	100	12	—	Mil	TDIP	S, P	Mil Temperature Range
ADC574A	12	±0.012	E, F, R, S	40	12	—	Mil, Ind, Com	DDIP	P	Industry Std Pinout and Interface Medium Speed Monolithic
ADC603	12	±0.018	L	10MHz	NS	–68*	Com, Ind, Mil	QDIP	P	High Speed Medium Resolution
ADC674A	12	±0.012	E, F, R, S	66	12	—	Mil, Ind, Com	DDIP	P	Industry Std Pinout and Interface Medium Speed Monolithic
ADC700	16	±0.003	D, E, F, N, R, S	59	14	—	Mil, Ind, Com	TDIP	S, P	Data-Bus Interface
ADC701	16	±0.003	D, E, G, R, S	512kHz	NS	–94w/SHC702*	Com	TDIP	P	High Accuracy, High Resolution
ADC774	12	±0.012	E, F, R, S	117	12	—	Mil, Ind, Com	DDIP	P	Industry Std Pinout and Interface Medium Speed Monolithic
ADC803	12	±0.012	G, R, S	1MHz	NS	NA	Ind, Mil	HMD	P	High Speed Medium Resolution
ADC7802	12	±0.012	D	117	12	—	Ext	DDIP, PLCC	P	High-Accuracy, 4-Channel MUX, Auto-Calibration, Sampling
ADS574	12	±0.012	E, F, R, S	40kHz	12	—	Com, Mil	DIP, DDIP, SO	P	Sampling 574 Type
ADS774	12	±0.012	E, F, R, S	117	12	—	Com, Mil	DIP, DDIP, SO	P	Sampling 774 Type
ADS800	**12**	**±0.024**	**Z**	**40MHz**	**12**		**Com**	**SOIC**	**P**	**Sampling, Internal Reference**
ADS801	**12**	**±0.024**	**Z**	**25MHz**	**12**		**Com**	**SOIC**	**P**	**Sampling, Internal Reference**
ADS802	**12**	**±0.024**	**Z**	**10MHz**	**12**		**Com**	**SOIC**	**P**	**Sampling, Internal Reference**
ADS820	**10**	**±0.097**	**Z**	**20MHz**	**10**		**Com**	**SOIC**	**P**	**Sampling, Internal Reference, Low Power**
ADS821	**10**	**±0.097**	**Z**	**40MHz**	**10**		**Com**	**SOIC**	**P**	**Sampling, Internal Reference**
ADS1210	**24**	**±0.003**	**D, S**	**Programmable**	**24**	**—**	**XInd**	**SOIC, PDIP**	**S**	**Low Power, Single-Channel, ΔΣ, Differential In**
ADS1211	**24**	**±0.003**	**D, S**	**Programmable**	**24**	**—**	**XInd**	**SOIC, PDIP**	**S**	**Low Power, 4-Channel MUX, ΔΣ, Differential In**
ADS7800	12	±0.012	R, S	333kHz	12	—	Com, Ind	DIP, SOIC	P	Sampling, Interface
ADS7803	12	±0.018	D	117	12	—	Ext	DDIP, PLCC	P	High-Accuracy, 4-Channel MUX, Auto-Calibration, Sampling
ADS7804	12	±0.012	S	100	12	—	Ext	PDIP, SOIC	P	Full Parallel, Pin Compatible to ADS7805
ADS7805	16	±0.0023	S	100	16	–96	Ext	PDIP, SOIC	P	Full Parallel, Pin Compatible to ADS7804
ADS7806	12	±0.012	C, D, S	40	12	–80	Ext	PDIP, SOIC	S, P	8-Bit Bytes or Serial, Pin Compatible to ADS7807
ADS7807	16	±0.0023	C, D, S	40	16	–96	Ext	PDIP, SOIC	S, P	8-Bit Bytes or Serial, Pin Compatible to ADS7806
ADS7808	12	±0.012	C, D, E, P, R, S	100	12	–80	Ext	PDIP, SOIC	S	Pin Compatible to ADS7809
ADS7809	16	±0.0023	C, D, E, P, R, S	100	16	–96	Ext	PDIP, SOIC	S	Pin Compatible to ADS7808
ADS7810	12	0.018	S	800	12	–77	Ext	PDIP, SOIC	P	
ADS7811	16	±0.0015	N	263	16	–96	XInd	PDIP, SOIC	P	Sampling, w/Internal Reference

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

GENERAL (CONT)

Product	Resolution (Bits)	Linearity Error max (%FSR)	Input Range (see table, pg 2.5) (V)	Sampling Rate (kHz)	NMC	THD (dB, max)	Temp Range[1]	Pkg[2]	Serial or Parallel	Description
ADS7812	***12***	***±0.012***	***S, AA, R, E, M, P, BB***	***40***	***12***	***–80***	***XInd***	***PDIP, SO***	***S***	***Sampling pin compatible with ADS7813***
ADS7813	***16***	***±0.0023***	***S, AA, R, E, M, P, BB***	***40***	***16***	***–96***	***XInd***	***PDIP, SO***	***S***	***Sampling pin compatible with ADS7812***
ADS7814	***14***	***±0.018***	***N***	***300***	***14***	***–90***	***XInd***	***PDIP, SO***	***P***	***Sampling, with output latches***
ADS7819	12	0.018	N	800	12	–77	Ext	PDIP, SOIC	P	
ADS7820	12	±0.01	D	100	12	–80	XInd	PDIP, SOIC	P	Sampling, pin compatible with ADS7821
ADS7821	16	±0.006	D	100	16	–90	Ind	PDIP, SOIC	P	Sampling, pin compatible with ADS7820
ADS7824	12	±0.01	S	40	12	–80	XInd	PDIP, SOIC	S, P	Sampling, 4-ch mux input
ADS7825	16	±0.002	S	40	16	–90	XInd	PDIP, SOIC	S, P	Sampling, 4-ch mux input
ADS7831	12	0.024	N	600	12	–77	Ext	PDIP, SOIC	P	Low Cost
ADS7832	***12***	***±0.049***	***B***	***117***	***12***	***–75****	***XInd***	***PDIP, PLCC***	***P***	***Sampling, 8-bit bytes out***
ADS7833	12	0.05	I, L, M, N	100	12	—	Ext	PLCC	S	3-channel, simultaneous sampling
DDC101	20	±2.5ppm[3]	Current	15	18	—	Ind	DDIP, SOIC	S	High Accuracy
DSP101	18	0.003	O	200	—	–90	Com	DDIP	S	DSP Compatible, Single Channel
DSP102	18	0.003	O	200	—	–90	Com	DDIP	S	DSP Compatible, Dual Channel

NOTES: (1) Com = 0°C to +70°C, Ext = –40°C to +85°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) DIP = 0.3" wide DIP, DDIP = 0.6" wide DIP, TDIP = 0.9" wide DIP, PLCC = Plastic Leaded Chip Carrier, SO = Small Outline Surface Mount. (3) Linearity errors ±0.025% reading ±2.5ppm FSR.

HDSL ANALOG FRONT END

Product	Design Speed	Minimum Speed	Power	Compatibility	Description
AFE1103E	***E1/T1***	***PCM-4***	***300mW***	***Brooktree/Metalink***	***Burr-Brown's HDSL Analog Front End greatly reduces the size and cost of an HDSL system by providing all of the active analog circuitry needed to connect the Brooktree Bt8952 HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section performs initial filters and digitizes the symbol data received on the telephone line and passes it to the HDSL DSP chip. The HDSL Analog Interface is a monolithic device fabricated on 0.6µ CMOS. It operates on a single +5V supply (using only 300mW). It is housed in a 48-pin SSOP package. This unit is second sourced by Brooktree's Bt8921.***
AFE1104E	***E1/T1***	***PCM-4***	***300mW***	***PairGain***	***Burr-Brown's HDSL Analog Front End greatly reduces the size and cost of an HDSL system by providing all of the active analog circuitry needed to connect PairGain Technologies SPAROW HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section performs initial echo cancellation and filters and digitizes the symbol data received on the telephone line and passes it to the HDSL DSP chip. The HDSL Analog Interface is a monolithic device fabricated on 0.6µ CMOS. It operates on a single +5V supply (using only 300mW). It is housed in a 48-pin SSOP package.***

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

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Product	Channels	Resolution (Bits)	Linearity Error (%FSR)	Input Range (see table, pg 2.5) (V)	Throughput Rate (kHz)	Temp Range[2]	Pkg[3]	Description
SDM506[5]	***16-Channel, single ended***	***16***	***±0.012***	***S, R, P, E***	***100***	***XInd***	***PLCC***	***Serial Out***
SDM507[5]	***8-Channel, differential***	***16***	***±0.012***	***D, C***	***100***	***XInd***	***PLCC***	***Serial Out***
SDM516[5]	***16-Channel, single ended***	***16***	***±0.012***	***S***	***100***	***XInd***	***PLCC***	***Parallel Out***
SDM517[5]	***8-Channel, differential***	***16***	***±0.012***	***S***	***100***	***XInd***	***PLCC***	***Parallel Out***
SDM862[1]	16-Channel, single ended	12	±0.012	R, S, E	33	Com, Ind, Mil	LCC, PGA	Parallel Out
SDM863[1]	8-Channel, differential	12	±0.012	R, S, E	33	Com, Ind, Mil	LCC, PGA	Parallel Out
SDM872[1]	16-Channel, single ended	12	±0.012	R, S, E	50	Com, Ind, Mil	LCC, PGA	Parallel Out
SDM873[1]	8-Channel, differential	12	±0.012	R, S, E	50	Com, Ind, Mil	LCC, PGA	Parallel Out

NOTES: (1) Internal instrumentation amplifier can be pin programmed for G = 1, 10, 100. (2) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, XInd = –40°C to 85°C, Mil = –55°C to +125°C. (3) LCC = Hermetic 0.95" (typ) square Leadless Chip Carrier, PGA = Hermetic 1.1" (typ) square Pin Grid Array. (4) Internal programmable gain amplifier can be programmable for G = 1, 10, 100, 1000.

KEY FOR A/D CONVERTER INPUT RANGE SPECIFICATION TABLE

SPECIFICATION CODE	RANGE (V)	SPECIFICATION CODE	RANGE (V)
A	0 to 1.25	L	±1.25
B	0 to 2.5	M	±2.0
C	0 to 4	N	±2.5
D	0 to 5	O	±2.75
E	0 to 10	P	±3.33
F	0 to 20	Q	±4.0
G	0 to –10	R	±5.0
H	±0.312	S	±10.0
I	±0.5	Z	1.25 to 3.25
J	±0.625	AA	0.3125 to 2.8125
K	±1.0	BB	0.5 to 4.5

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

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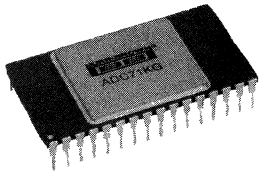
BURR-BROWN®



ADC71

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11060

16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

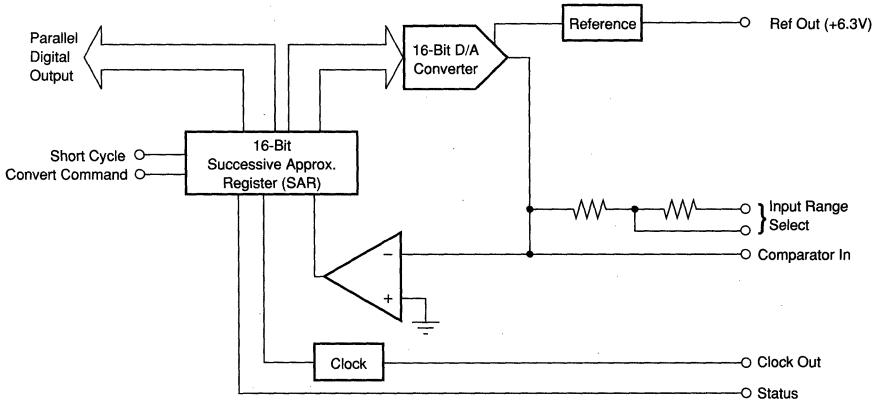
- **16-BIT RESOLUTION**
- **±0.003% MAXIMUM NONLINEARITY**
- **COMPACT DESIGN: 32-pin Hermetic Ceramic Package**
- **CONVERSION SPEED: 50µs max**

DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses laser-trimmed ICs and is packaged in a convenient 32-pin hermetic ceramic dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

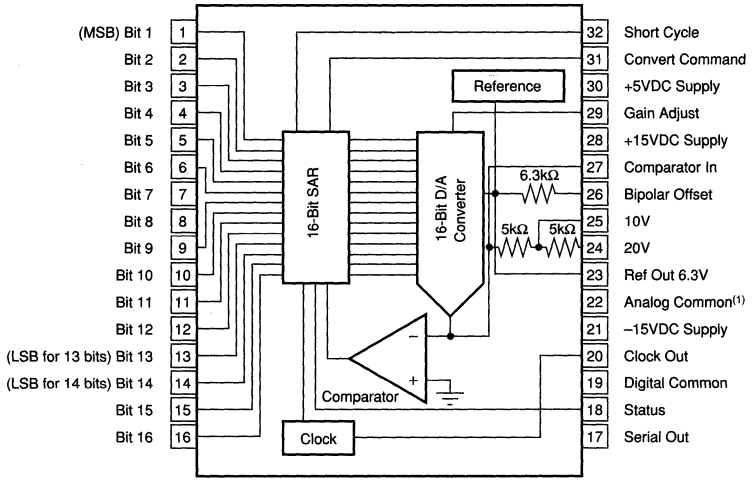
At +25°C and rated power supplies, unless otherwise noted.

PARAMETER	ADC71J, K MIN	ADC71J, K TYP	ADC71J, K MAX	ADC71A, B MIN	ADC71A, B TYP	ADC71A, B MAX	UNITS
RESOLUTION			16			16	Bits
INPUTS							
ANALOG							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Input Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL[1]							
Convert Command Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)							
Logic Loading			1				TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%
Offset[2]: Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR[3]
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error: K, B			±0.003			±0.003	% of FSR
J, A			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_S
+5VDC		0.001			0.001		% of FSR/%V_S
CONVERSION TIME[4]							
14 Bits			50			50	µs
WARM-UP TIME	5			*			min
DRIFT							
Gain		±10	±15		*	*	ppm/°C
Offset: Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13 Bits)	0		+70	–25		+85	°C
K, B (14 Bits)	0		+70	–25		+85	°C
OUTPUT							
DIGITAL DATA							
(All Codes Complementary)							
Parallel Output Codes[5]: Unipolar		CSB					
Bipolar		COB, CTC[6]					
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB					
Output Drive			2			*	TTL Loads
Status		Logic "1" During Conversion					
Status Output Drive			2			2	TTL Loads
Clock Output Drive			2			2	TTL Loads
Frequency[7]		280			*		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with							
No Degradation of Specs			±200			±200	µA
Temp Coefficient			±10			*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		655			655		mW
Rated Voltage, Analog	±11.4	±15	±16	*	*	*	VDC
Rated Voltage, Digital	+4.75	+5	+4.75	*	*	*	VDC
Supply Drain +15VDC		+10	+15		*	*	mA
Supply Drain –15VDC		–28	–35		*	*	mA
Supply Drain +5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	–25		+85	°C
Operating (Derated Specs)	–25		+85	–55		+125	°C
Storage	–55		+125	–55		+125	°C

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max Logic "1" = 2.4V min. (2) Adjustable to zero. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section. (5) See Table I. CSB = Complementary Straight Binary. COB = Complementary Offset Binary. CTC = Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (Pin 1).

PIN CONFIGURATION

Top View **DIP**



NOTE: (1) Metal lid of package is connected to pin 22 (Analog Common).

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0 to +16.5V
$-V_{CC}$ to Common	0V to –16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

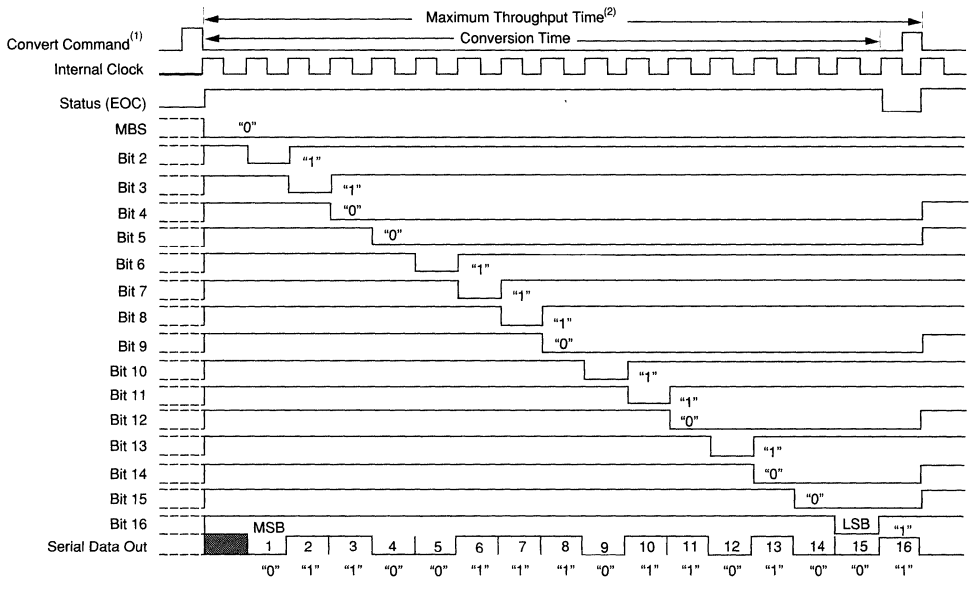
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC71JG	32-Pin Hermetic DIP	172-5
ADC71KG	32-Pin Hermetic DIP	172-5
ADC71AG	32-Pin Hermetic DIP	172-5
ADC71BG	32-Pin Hermetic DIP	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	NONLINEARITY
ADC71JG	0°C to +70°C	±0.006% FSR
ADC71KG	0°C to +70°C	±0.003% FSR
ADC71AG	–25°C to +85°C	±0.006% FSR
ADC71BG	–25°C to +85°C	±0.003% FSR



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 57µs for 16 bits.

FIGURE 1. ADC71 Timing Diagram.

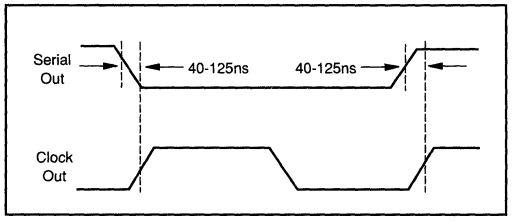


FIGURE 2. Timing Relationship of Serial Data to Clock.

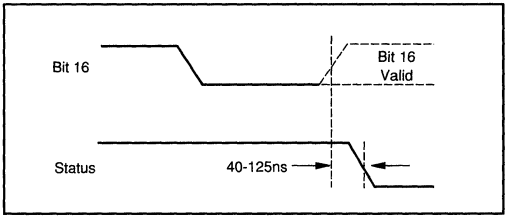


FIGURE 3. Timing Relationship of Valid Data to Status.

Binary (BIN) Output	**INPUT VOLTAGE RANGE AND LSB VALUES**						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB							
000 ... 000(4)	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

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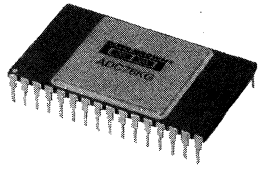


ADC76

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 11063

16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **16-BIT RESOLUTION**
- **LINEARITY ERROR: ±0.003% max (KG, BG)**
- **NO MISSING CODES GUARANTEED FROM –25°C TO +85°C**
- **17µs CONVERSION TIME (16-Bit)**
- **SERIAL AND PARALLEL OUTPUTS**

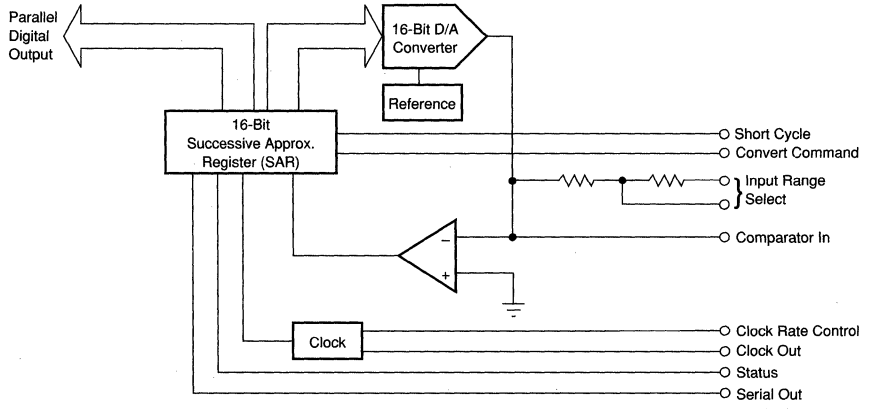
DESCRIPTION

The ADC76 is a high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art laser-trimmed IC thin-film resistors and is packaged in a hermetic 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and –25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



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SPECIFICATIONS

ELECTRICAL

At +25°C, and rated power supplies, unless otherwise noted.

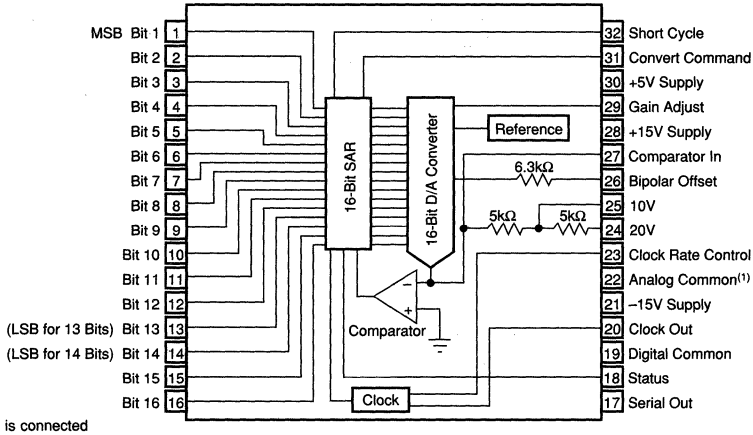
PARAMETER	ADC76J, K MIN	ADC76J, K TYP	ADC76J, K MAX	ADC76A, B MIN	ADC76A, B TYP	ADC76A, B MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10			*		V
		0 to +20			*		
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS(1)							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		*	*	%
Offset Error: Unipolar(2)		±0.05	±0.1		*	*	% of FSR(3)
Bipolar(2)		±0.1	±0.2		*	*	% of FSR
Linearity Error: K, B			±0.003			*	% of FSR
J, A			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.001	±0.003		*	*	% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME(4)							
14 Bits			15			*	µs
15 Bits			16			*	µs
16 Bits			17			*	µs
WARM-UP TIME	5			*			Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-bit)	0		+70	–25		+85	°C
K, B (14-bit)	0		+70	–25		+85	°C
OUTPUT DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes(5): Unipolar		CSB			*		
Bipolar		COB, CTC(6)			*		
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive			2			*	TTL Loads
Internal Clock: Clock Output Drive			2			*	TTL Loads
Frequency(7)	933		1400	*		*	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.655			*		W
Rated Voltage: Analog	±11.4	±15	±16	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+10	+15		*	*	mA
–15VDC		–28	–35		*	*	mA
+5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	–25		+85	°C
Storage	–55		+125	*		*	°C

*Specification same as ADC76J, K.

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1' = 2.4V, min. (2) Adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB = Complementary Straight Binary, COB = Complementary Offset Binary, CTC = Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz.

PIN CONFIGURATION

Top View **DIP**



NOTE: (1) Metal lid is connected to pin 22 (Analog Common).

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0V to +16.5V
$-V_{CC}$ to Common	0V to –16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	300°C

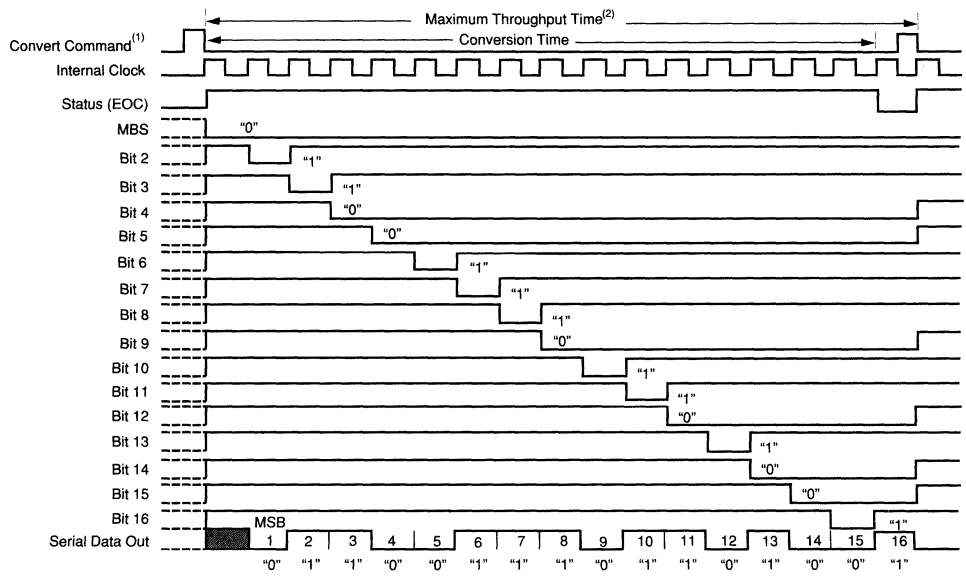
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC76JG	32-Pin Hermetic DIP	172-5
ADC76KG	32-Pin Hermetic DIP	172-5
ADC76AG	32-Pin Hermetic DIP	172-5
ADC76BG	32-Pin Hermetic DIP	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
ADC76AG	±0.006	–25°C to +85°C
ADC76BG	±0.003	–25°C to +85°C
ADC76JG	±0.006	0°C to +70°C
ADC76KG	±0.003	0°C to +70°C



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 17µs for 16 bits.

FIGURE 1. ADC76 Timing Diagram.

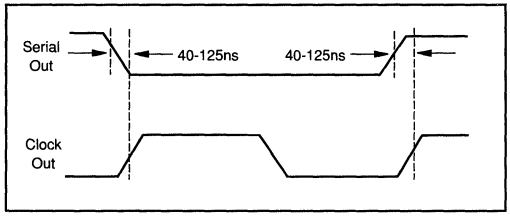


FIGURE 2. Timing Relationship of Serial Data to Clock.

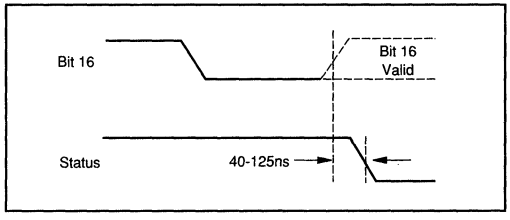


FIGURE 3. Timing Relationship of Valid Data to Status.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB							
000 ... 000(4)	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

BURR-BROWN®

ADC80

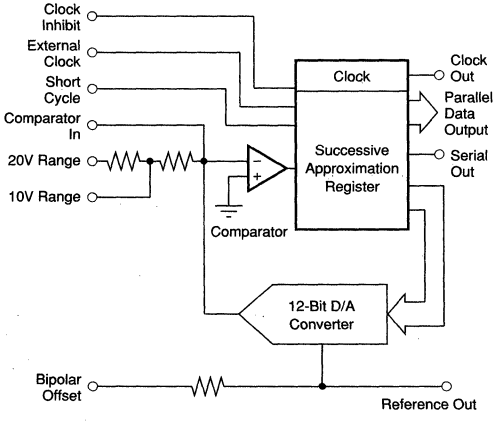
ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10676

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **INDUSTRY-STANDARD 12-BIT ADC**
- **±0.012% LINEARITY**
- **25µs max CONVERSION TIME**
- **±12V OR ±15V OPERATION**
- **NO MISSING CODES: –25°C to +85°C**
- **HERMETIC 32-PIN PACKAGE**
- **PARALLEL AND SERIAL OUTPUTS**
- **595mW max DISSIPATION**



DESCRIPTION

The ADC80 is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25µs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80AG MIN	ADC80AG TYP	ADC80AG MAX	UNITS
RESOLUTION				
ADC80AG-12, ADC80-AGZ-12[1]			12	Bits
ADC80AG-10			10	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
0 to +10V, +5V	4.9	5	5.1	kΩ
±10V	9.8	10	10.2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2		5.5	V
V_{IL} (Logic "0")	–0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			–150	µA
I_{IL} (V_{IN} = +0.4V)			500	µA
Convert Command Pulse Width[2]	100		2000	ns
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.1	±0.3	% of FSR[4]
Offset Error[3]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error: ADC80AG-12, ADC80AGZ-12			±0.012	% of FSR
ADC80AG-10			±0.048	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11.4V ≤ $\pm V_{CC}$ ≤ 16.5V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[5]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	–25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[6]				
ADC80AG-12, ADC80-AGZ-12	15	22	25	µs
ADC80AG-10	13	20	22	µs
OUTPUT				
DIGITAL (Bits 1-12 , Clock Out, Status, Serial Out)				
Output Codes[7]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[8]		CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{SOURCE} ≤ 80µA)	+2.4			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	V
Source Current Available for External Loads[9]	200			µA
Temperature Coefficient		±10	±30	ppm/°C

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80AG MIN	ADC80AG TYP	ADC80AG MAX	UNITS
POWER SUPPLY REQUIREMENTS (For all models)				
Voltage: $\pm V_{CC}$	±11.4	±15	±16.5	V
V_{DD}	+4.5	+5	+5.5	V
Current: $+I_{CC}$		5	8.5	mA
$-I_{CC}$		21	26	mA
I_{DD}		11	15	mA
Power Dissipation ($\pm V_{CC}$ = 15V)		450	595	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	–25		+85	°C
Operating (derated specs)	–55		+125	°C
Storage	–65		+150	°C

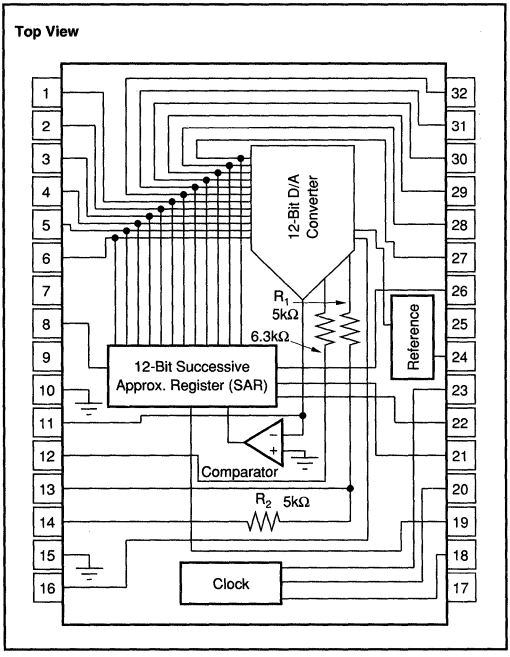
NOTES: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12. (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 2µs (max) to assure the specified conversion time. (3) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drifts. (6) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time: see "Short Cycle Feature" section. (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table 1 for additional information. (8) NRZ means Non-Return-to-Zero coding. (9) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10 (LSB-10 Bits)
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB-12 Bits)
7	NC(1)	26	Serial Out
8	Bit 1 ($\overline{MSB}$)	25	$-V_{CC}$
9	+5V Digital Supply	24	Reference Out (+6.3V)
10	Digital Common(2)	23	Clock Out
11	Comparator In	22	Status
12	Bipolar Offset	21	Short Cycle
13	R_1 10V Range	20	Clock Inhibit
14	R_2 20V Range	19	External Clock
15	Analog Common	18	Convert Command
16	Gain Adjust	17	$+V_{CC}$

NOTE: (1) +5V applied to pin 7 has no effect on circuit. (2) Metal lid of package is connected to pin 10.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to –16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common	–0.3V to $+V_{DD}$ +0.5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, (soldering, 10s)	+300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

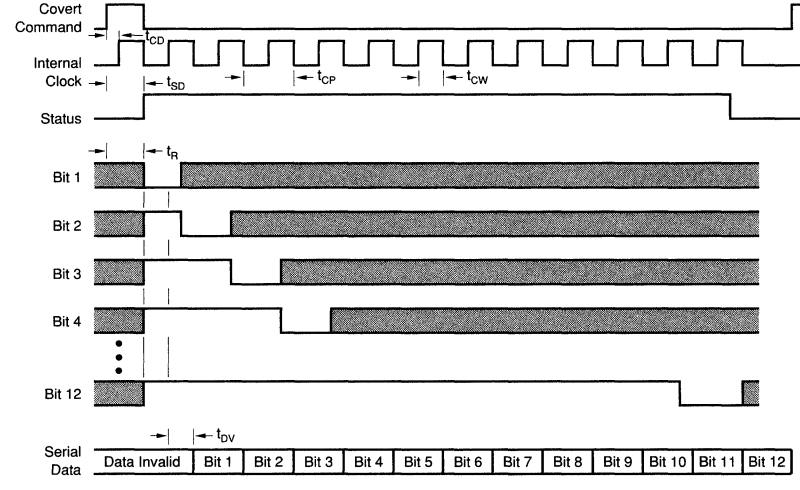
MODEL	RESOLUTION (Bits)
ADC80AG-10	10
ADC80G-12	12
ADC80GZ-12[1]	12

NOTE: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADC80AG-10	32-Pin Hermetic	172
ADC80G-12	32-Pin Hermetic	172
ADC80AZ-12[1]	32-Pin Hermetic	172

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



SYMBOL	PARAMETER	TYP	UNITS
t_{CD}	Clock delay from convert command	30	ns
t_{CP}	Nominal clock period	1.65	µs
t_{CW}	Nominal clock pulse width	0.65	µs
t_{SD}	Status delay from convert command	130	ns
t_R	All bits reset delay from convert command	65	ns
t_{DV}	Data valid time from clock pulse high	–5	ns

FIGURE 1. ADC80 Timing Diagram (nominal values at +25°C with internal clock).

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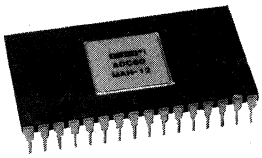


ADC80MAH-12

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10694

Monolithic 12-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **INDUSTRY-STANDARD 12-BIT ADC**
- **MONOLITHIC CONSTRUCTION**
- **LOW COST**
- **±0.012% LINEARITY**
- **25µs max CONVERSION TIME**
- **±12V OR ±15V OPERATION**
- **NO MISSING CODES: –25°C to +85°C**
- **HERMETIC 32-PIN PACKAGE**
- **PARALLEL OR SERIAL OUTPUTS**
- **705mW max DISSIPATION**

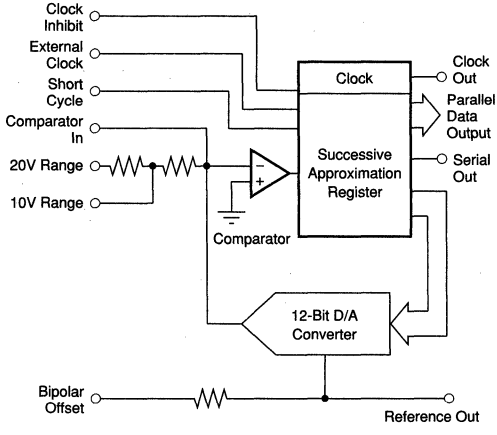
DESCRIPTION

The ADC80MAH-12 is a 12-bit single-chip successive-approximation analog-to-digital converter for low cost converter applications. It is complete with a comparator, a 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, a successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25µs makes the ADC80MAH-12 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, this A/D converter may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation. The convert command circuits have been redesigned to allow simplified free-running operation with internal or external clock.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80MAH-12 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80MAH-12 MIN	TYP	MAX	UNITS
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
0 to +10V, ±5V	4.9	5	5.1	kΩ
±10V	9.8	10	10.2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2		5.5	V
V_{IL} (Logic "0")	–0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			20	µA
I_{IL} (V_{IN} = +0.4V)	–20			µA
Convert Command Pulse Width[1]	100ns		20	µs
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.01	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11.4V ≤ $\pm V_{CC}$ ≤ 16.5V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ $\pm V_{DD}$ ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	–25		±85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]		22	25	µs
OUTPUT				
DIGITAL (Bits 1-12 , Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{SOURCE} ≤ 80µA)	+2.4			V
Internal Clock Frequency		520		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.20	+6.3	+6.40	V
Source Current Available for External Loads[8]	200			µA
Temperature Coefficient		±10	±30	ppm/°C

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V, unless otherwise specified.

PARAMETER	ADC80MAH-12 MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS				
Rated Supply Voltages		+5, ±12 or ±15		V
Supply Ranges: $\pm V_{CC}$	±11.4		+16.5	V
V_{DD}	+4.5		+5.5	V
Supply Drain: $+I_{CC}$ ($+V_{CC}$ = 15V)		8.5	11	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)		21	24	mA
I_{DD} (V_{CC} = 5V)		30	36	mA
Power Dissipation ($\pm V_{CC}$ = 15V, V_{DD} = 5V)		593	705	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	–25		+85	°C
Operating (derated specs)	–55		+125	°C
Storage	–65		+150	°C

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 20µs (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means Non-Return-to-Zero coding. (8) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

ABSOLUTE MAXIMUM RATINGS PCM1760

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to –16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common	–0.3V to $+V_{CC}$
Analog Inputs (Analog In, Bipolar Offset) to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, (soldering, 10s)	+300°C
Maximum Junction Temperature	+160°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	RESOLUTION (Bits)
ADC80MAH-12	12
BURN-IN SCREENING OPTION	
MODEL	**BURN-IN TEMPERATURE (160h)(1)**
ADC80MAH-12-BI	12

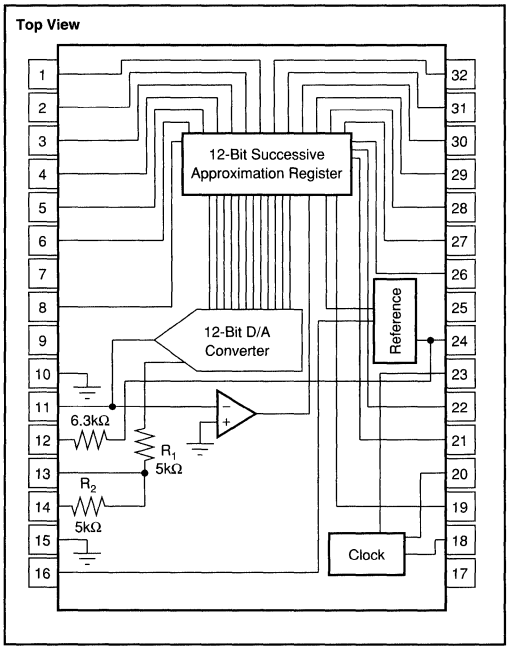
NOTE: (1) Or equivalent.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC80MAH-12	32-Pin Hermetic	212

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

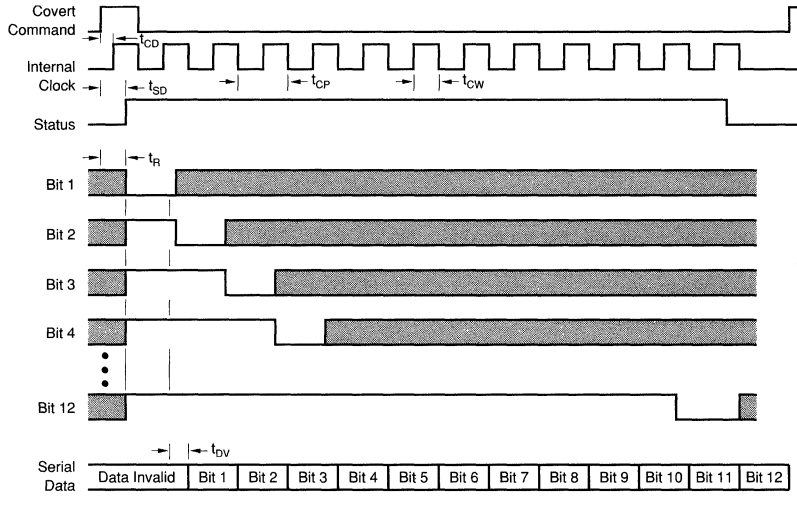
CONNECTION DIAGRAM



PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10 (LSB-10 Bits)
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB-12 Bits)
7	NC(1)	26	Serial Out
8	Bit 1 ($\overline{\text{MSB}}$)	25	$-V_{CC}$
9	+5V Digital Supply	24	Reference Out (+6.3V)
10	Digital Common	23	Clock Out
11	Comparator In	22	Status
12	Bipolar Offset	21	Short Cycle
13	R_1 10V Range	20	Clock Inhibit
14	R_2 20V Range	19	External Clock
15	Analog Common	18	Convert Command
16	Gain Adjust	17	$+V_{CC}$

NOTE: (1) +5V applied to pin 7 has no effect on circuit.



SYMBOL	PARAMETER	TYP	UNITS
t_{CD}	Clock delay from convert command	153	ns
t_{CP}	Nominal clock period	1.81	µs
t_{CW}	Nominal clock pulse width	0.87	µs
t_{SD}	Status delay from convert command	186	ns
t_R	All bits reset delay from convert command	141	ns
t_{DV}	Data valid time from clock pulse high	–15	ns

FIGURE 1. Timing Diagram (nominal values at +25°C with internal clock).

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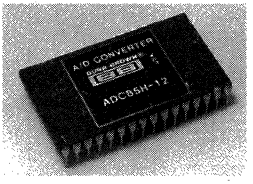

ADC84
ADC85H
ADC87H

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- INDUSTRY STANDARD 12-BIT A/D CONVERTERS
- COMPLETE WITH CLOCK AND INPUT BUFFER
- HIGH SPEED CONVERSION: 10µs (max)
- REDUCED CHIP COUNT—HIGH RELIABILITY
- LOWER POWER DISSIPATION: 450MW (typ)
- ±0.012% max LINEARITY ERROR
- THREE TEMPERATURE RANGES:
  0°C to +70°C—ADC84
  –25°C to +85°C—ADC85H
  –55°C to +125°C—ADC87H
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- PARALLEL AND SERIAL OUTPUTS
- ±12V OR ±15V POWER SUPPLY OPERATION
- HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP

DESCRIPTION

ADC84, ADC85H, and ADC87H analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

They are complete with internal reference and input buffer amplifier. Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast 10µs conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ±12VDC or ±15VDC and +5VDC.

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SPECIFICATIONS

ELECTRICAL

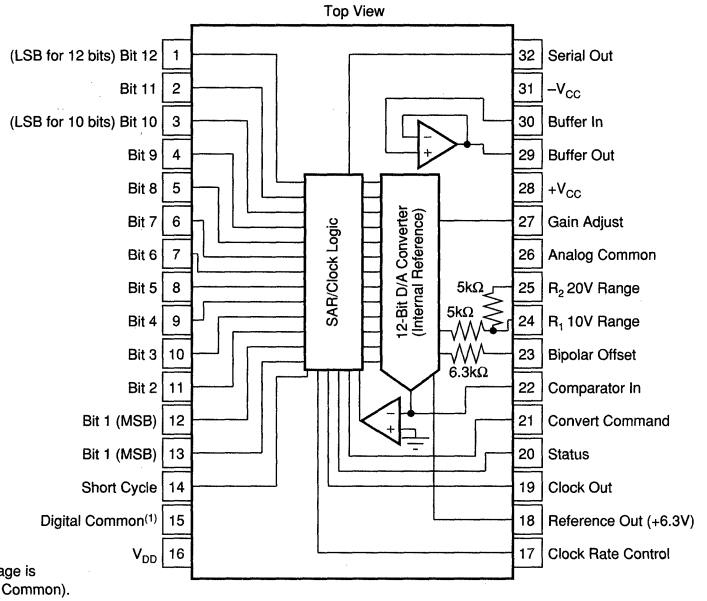
Specified at +25°C and rated supplies, unless otherwise noted.

PARAMETER	ADC84KG-12[1] MIN	ADC84KG-12[1] TYP	ADC84KG-12[1] MAX	ADC85H-12 MIN	ADC85H-12 TYP	ADC85H-12 MAX	ADC87H-12 MIN	ADC87H-12 TYP	ADC87H-12 MAX	UNITS
RESOLUTION			12			*			*	Bits
ANALOG INPUTS										
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*			*		V
Unipolar		0 to +5, 0 to +10			*			*		V
Impedance (Direct Input): 0 to +5V, ±2.5V	2.45	2.5	2.55	*	*	*	*	*	*	kΩ
0 to +10V, ±5V	4.9	5	5.1	*	*	*	*	*	*	kΩ
±10V	9.8	10	10.2	*	*	*	*	*	*	kΩ
Buffer Amplifier: Impedance	100			*			*			MΩ
Bias Current		50			*			*		nA
Settling Time to 0.01% for 20V Step[2]		2			*			*		µs
DIGITAL INPUTS[3]										
Convert Command		Positive pulse 50ns (min), trailing edge initiates conversion								
Logic Loading		1			*			*		TTL Load
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error [4]		±0.1	±0.25		*	*		*	*	%
Offset Error[4]: Unipolar		±0.05	±0.2		*	*		*	*	% of FSR[5]
Bipolar		±0.1	±0.25		*	*		*	*	% of FSR
Linearity Error[6]			±0.012			*			*	% of FSR
Inherent Quantization Error		±0.5			*			*		LSB
Differential Linearity Error		±0.5			*			*		LSB
No Missing Codes Temperature Range	0		+70	–25		+85	–55		+125	°C
POWER SUPPLY SENSITIVITY										
Gain and Offset: ±15V		±0.004			*			*		% of FSR/%V_S
+5V		±0.001			*			*		% of FSR/%V_S
DRIFT										
Gain			±30			±15			±15	ppm/°C
Offset: Unipolar		±3			±3				±5	ppm of FSR/°C
Bipolar			±15			±7			±10	ppm of FSR/°C
Linearity			±3			±2			±2	ppm of FSR/°C
Monotonicity		Guaranteed			*			*		
CONVERSION TIME			10			*			*	µs
DIGITAL OUTPUT[3]										
(All Modes Complementary)										
Parallel Output Codes: Unipolar		CSB			*			*		
Bipolar		COB, CTC			*			*		
Output Drive		2			*			*		TTL Loads
Serial Data Codes (NRZ)		CSB, COB			*			*		
Output Drive		2			*			*		TTL Loads
Status		Logic "1" During Conversion			*			*		
Output Drive		2			*			*		TTL Loads
Internal Clock: Output Drive		2			*			*		TTL Loads
Frequency[7]		1.35			*			*		MHz
INTERNAL REFERENCE VOLTAGE										
Reference Output	+6.2	+6.3	+6.4	*	*	*	*	*	*	V
Max. External Current with No Degradation			200			*			*	µA
Tempco of Drift			±20		±5	±10		±5	±10	ppm/°C
POWER SUPPLY REQUIREMENTS										
Rated Supply Voltages		+5, ±12 or ±15			*			*		V
Supply Ranges: V_{DD}	+4.75		+5.25	*		*	*		*	V
$\pm V_{CC}$	±11.4		±16.5	*		*	*		*	V
Supply Drain: $+I_{CC}$			20			*			*	mA
$-I_{CC}$			25			*			*	mA
I_{DD}			10			*			*	mA
Total Power Dissipation		450	725		*	*		*	*	mW
TEMPERATURE RANGE										
Specification	0		+70	–25		+85	–55		+125	°C
Operating (with Derated Specs)	–25		+85	–55		+125				°C
Storage	–65		+150	*		*	*		*	°C

•Specification is the same as ADC84KG-12.

NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6µs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V (min). For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.

CONNECTION DIAGRAM — ADC84, 85H, 87H



NOTE: (1) Metal lid of package is connected to pin 15 (Digital Common).

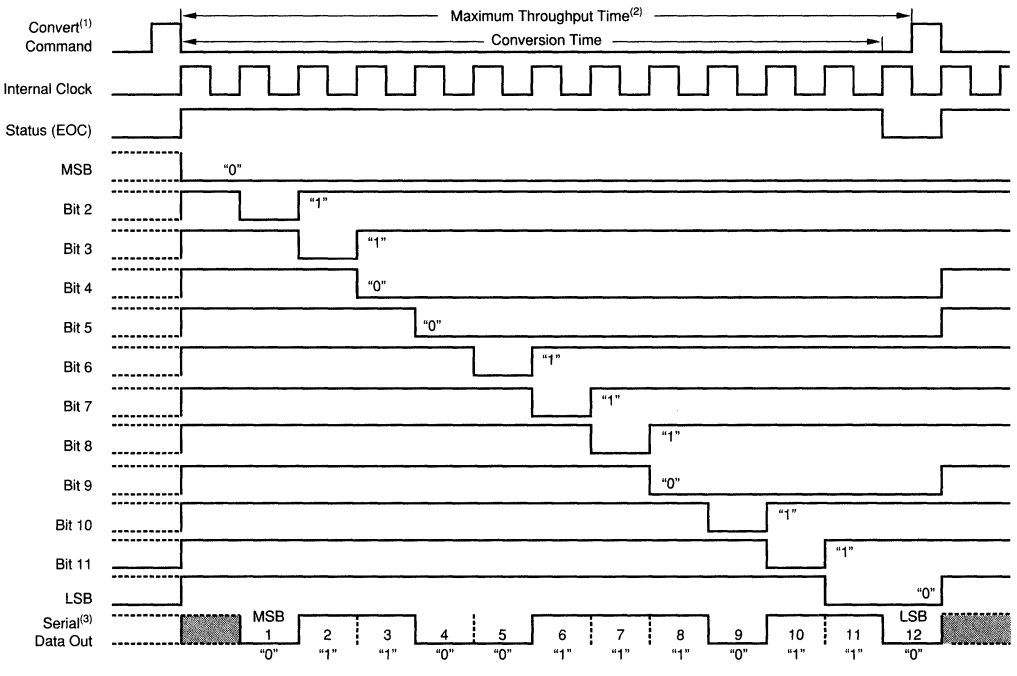
ORDERING INFORMATION

MODEL	RESOLUTION (Bits)	TEMPERATURE RANGE
ADC84KG-10	10	0°C to +70°C
ADC84KG-12	12	0°C to +70°C
ADC85H-12	12	–25°C to +85°C
ADC87H-12	12	–55°C to +125°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC84KG-10	Case Ceramic DIP	172-5
ADC84KG-12	Case Ceramic DIP	172-5
ADC85H-12	32-Pin Side-brazed	172-5
ADC87H-12	32-Pin Side-brazed	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 10.5µs for 12 bits and 6.4µs for 10 bits. (3) Use trailing edge of clock to strobe serial output.

FIGURE 1. Timing Diagram.

BURR - BROWN®

ADC574A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, or 16-BIT MICROPROCESSOR BUS INTERFACE**
- **IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS**
  Conversion Time: 25μs max
  Bus Access Time: 150ns max
  A_0 Input: Bus Contention During Read Operation Eliminated
- **DUAL IN-LINE PLASTIC, PLCC AND HERMETIC CERAMIC**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  0°C to +75°C: ADC574AJ and K Grades
  –55°C to +125°C: ADC574ASH, TH

DESCRIPTION

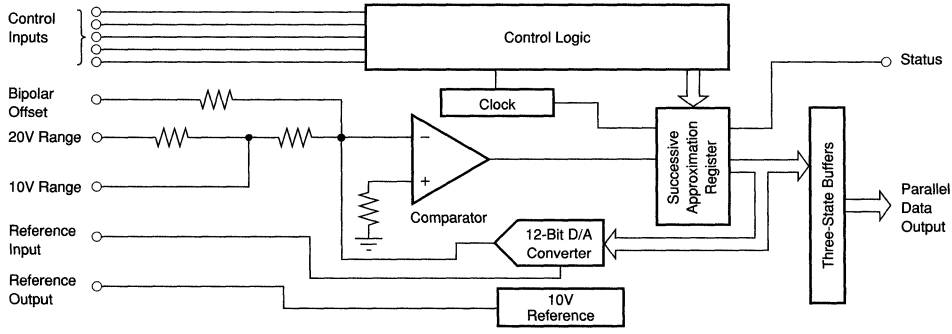
The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 25μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, and a hermetic side-brazed ceramic DIP.



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BURR - BROWN®

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, and V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC574AJP, JH, SH MIN	ADC574AJP, JH, SH TYP	ADC574AJP, JH, SH MAX	ADC574AKP, KH, TH MIN	ADC574AKP, KH, TH TYP	ADC574AKP, KH, TH MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	*	*	*	kΩ
±10V, 0V to +20V	9.4	10	10.6	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	*		*	V
Logic 0	–0.5		+0.8	*		*	V
Current	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			*	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(Adjustable to Zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < + 12.6V			±2			±1	LSB
–16.5V < V_{EE} < –13.5V or –12.6V < V_{EE} < – 11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			*	LSB
CONVERSION TIME [4]							
8-Bit Cycle	10	13	17	*	*	*	µs
12-Bit Cycle	15	20	25	*	*	*	µs
OUTPUTS							
DIGITAL (DB_{11}–DB_0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High -Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF

SPECIFICATIONS (CONT)

ELECTRICAL

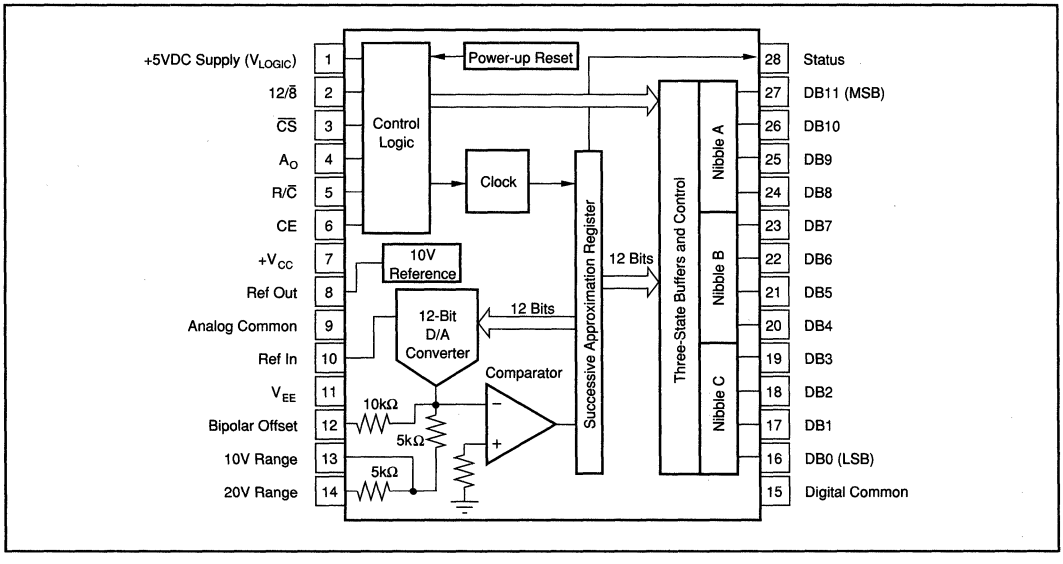
At T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, and V_{LOGIC} = +5V unless otherwise specified.

PARAMETERS	ADC574AJP, JH, SH			ADC574AKP, KH, TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	*	*	*	V
Source Current Available for External Loads[5]	2.0			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

* Same specifications as ADC574AJP, AJH, ASH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at ±25°C (see Optional External Full Scale and Offset Adjustments section). (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendors' 574 and 574A type specifications tables. (3) Using internal reference. (4) See Controlling the ADC574A section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common	0V to +16.5V
V_{EE} to Digital Common	0V to –16.5V
V_{LOGIC} Digital Common	0V to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	–0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering,10s)	+300°C
Thermal Resistance, θ_{JA} : Ceramic	50°C/W
Plastic	100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC574s. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "–BI" models: +85°C
Ceramic "–BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "–BI" to the base model number (e.g., ADC574AKP-BI).

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})
ADC574AJP	Plastic DIP	0°C to +75°C	±1LSB
ADC574AKP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC574AJH	Ceramic DIP	0°C to +75°C	±1LSB
ADC574AKH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC574ASH	Ceramic DIP	–55°C to +125°C	±1LSB
ADC574ATH	Ceramic DIP	–55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMP (160 Hours)
ADC574AJP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC574AKP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC574AJH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC574AKH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC574ASH-BI	Ceramic DIP	–55°C to +125°C	+125°C
ADC574ATH-BI	Ceramic DIP	–55°C to +125°C	+125°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC574AJP	Plastic DIP	215
ADC574AKP	Plastic DIP	215
ADC574AJH	Ceramic DIP	149
ADC574AKH	Ceramic DIP	149
ADC574ASH	Ceramic DIP	149
ADC574ATH	Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

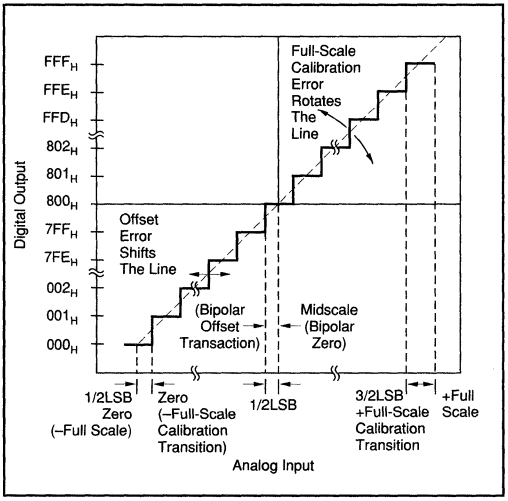


FIGURE 1. ADC574A Transfer Characteristics Terminology.

Thus, for a converter connected for biopolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination to appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

ADC574AKP, KN, KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2 LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	**Defined as:**	**±10V**	**±5V**	**0 to +10V**	**0 to +20V**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n =12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+Full-Scale Calibration	+10V – 3/2LSB	+5 – 3/2LSB	+10V – 3/2LSB	+10V – 3/2LSB
$7FF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	±10V – 1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10µF tantalum-type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC574A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω, 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω, 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset and gain adjustments are still performed as described below. However, you must recalculate full-scale adjustment voltages proportionately. A fixed metal-film resistor can be used because the input impedance of the ADC574A is trimmed to less than ±6% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC574A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE — UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal-film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV

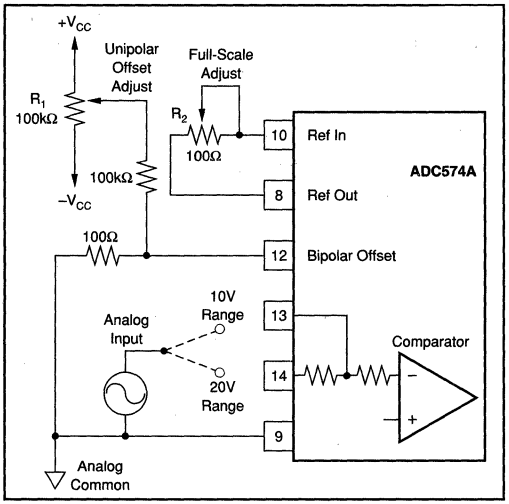


FIGURE 2. Unipolar Configuration.

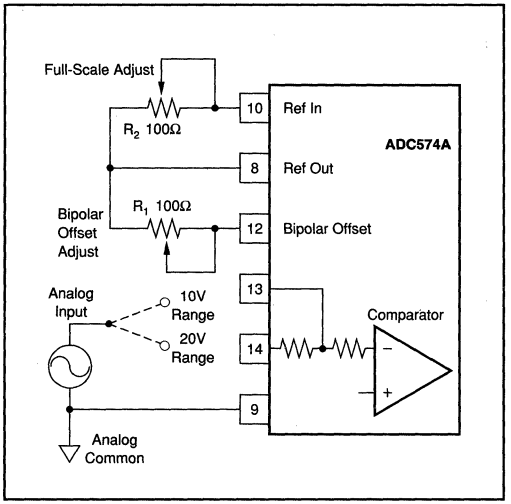


FIGURE 3. Bipolar Configuration.

for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal-film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC574A

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$(Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADC574A Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

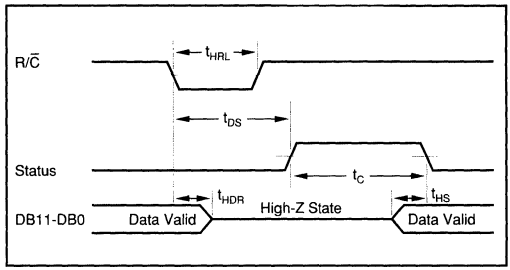


FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

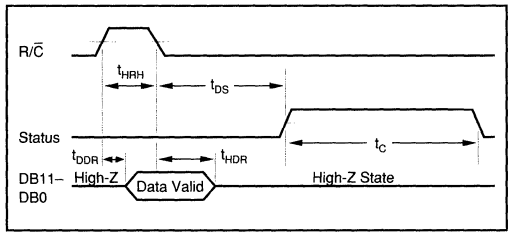


FIGURE 5. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12-bit cycle	15	20	25	µs
	8-bit cycle	10	13	17	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	300	400	1000	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

TABLE V. Timing Specifications.

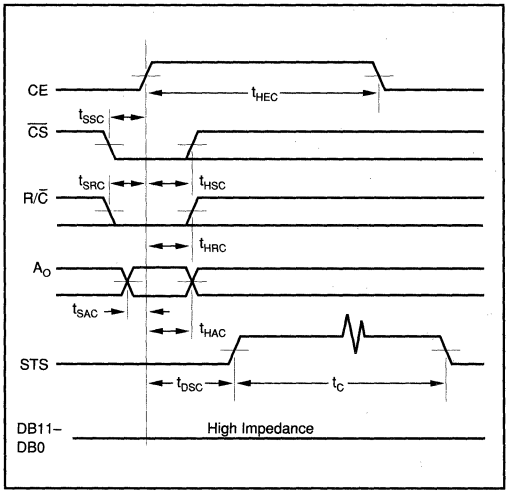


FIGURE 6. Conversion Cycle Timing.

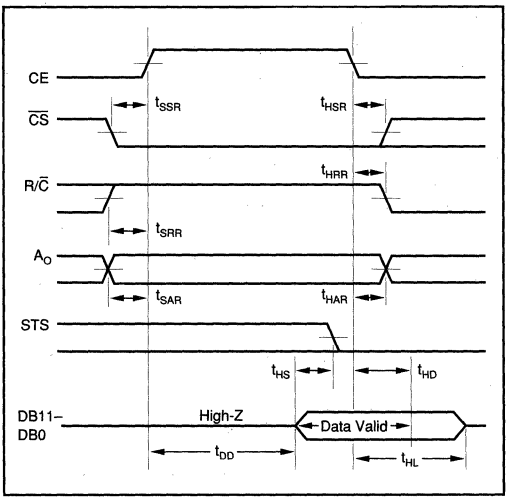


FIGURE 7. Read Cycle Timing.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15µs (t_{DD} max + t_{HS} min) before STATUS goes low. Refer to Figure 7 for these timing relationships.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

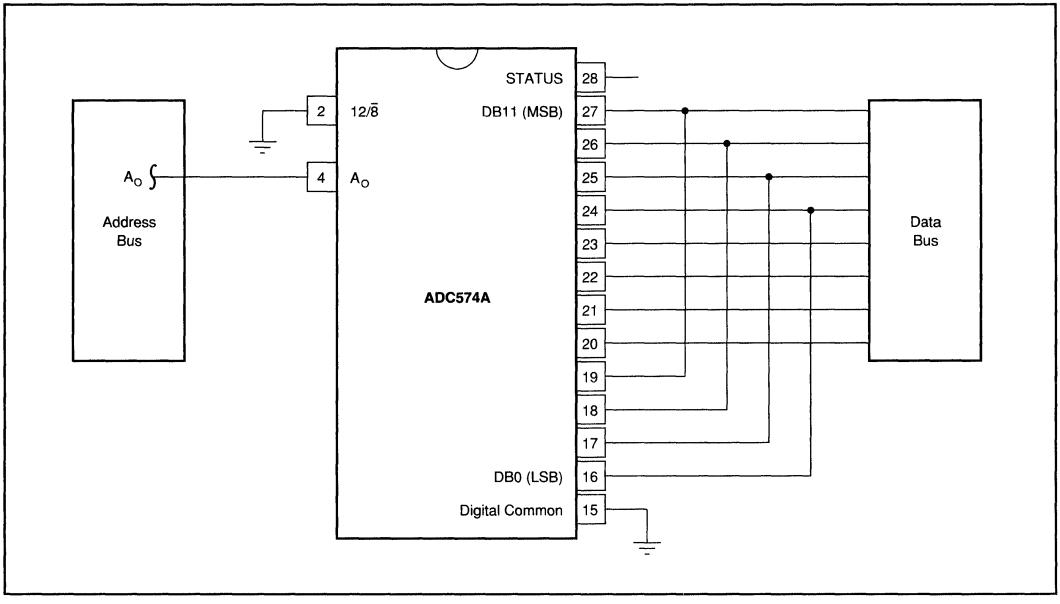


FIGURE 9. Connection to an 8-Bit Bus.

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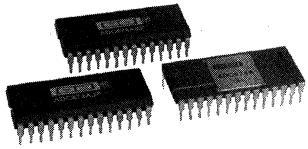


ADC674A

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10551

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**
- **IMPROVED PERFORMANCE SECOND SOURCE FOR ADC574A/674A-TYPE A/D CONVERTERS**
  Conversion Time: 15µs max
  Bus Access Time:150ns max
  A_0 Input: Bus Contention During Read Operation Eliminated
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  0°C to +75°C ADC674AJH, KH, JP, KP Grades
  –55°C to +125°C (ADC674ASH, TH Grades)

DESCRIPTION

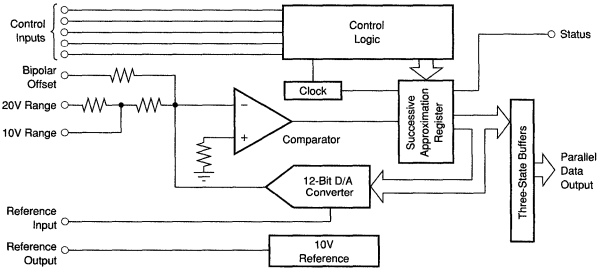
The ADC674A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC674A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±12V or +15V, V_{EE} = –12V or –15VDC, and V_{LOGIC} = +5V, unless otherwise noted.

PARAMETER	ADC674AJP, JH, SH MIN	ADC674AJP, JH, SH TYP	ADC674AJP, JH, SH MAX	ADC674AKP, KH, TH MIN	ADC674AKP, KH, TH TYP	ADC674AKP, KH, TH MAX	UNITS
RESOULUTION			12			*	Bits
ANALOG INPUTS							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	*	*	*	kΩ
±10V, 0V to +20V	9.4	10	10.6	*	*	*	k Ω
DIGITAL INPUTS (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		±5.5	*		*	V
Logic 0	–0.5		±0.8	*		*	V
Current	–5	0.2	±5	*	*	*	µA
Capacitiance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C			±1			±1/2	LSB
Linearity Error			±2			*	LSB
Unipolar Offset Error (adjustable to zero)			±10			±4	LSB
Bipolar Offset Error (adjustable to zero)							
Full-Scale Calibration Error[1] (adjustable to zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (differential linearity)	11	±1/2		12			Bits
Inherent Quantization Error					*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustmen[1]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (differential linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
+16.5V < V_{EE} < +13.5V or –12.6V < V_{EE} < –11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			*	LSB
CONVERSION TIME[4]							
8-Bit Cycle	6	8	10	*	*	*	µs
12-Bit Cycle	9	12	15	*	*	*	µs
DIGITAL OUTPUT (DB_{11}—DB_0, Status)							
(Over Temperature Range)							
Outputs Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only , High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	±10	±10.1	*	*	*	V
Source Current Available for External Loads[5]	2			*			mA

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, V_{CC} = ±12V or +15V, V_{EE} = –12V or –15VDC, and V_{LOGIC} = +5V, unless otherwise noted.

PARAMETER	ADC674AJP, AJH, ASH MIN	ADC674AJP, AJH, ASH TYP	ADC674AJP, AJH, ASH MAX	ADC674AKP, AKH, ATH MIN	ADC674AKP, AKH, ATH TYP	ADC674AKP, AKH, ATH MAX	UNITS
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC} +11.4		+16.5	*		*	V	
V_{EE}	–11.4		–16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specification: K, J Grades	0		+75	*		*	°C
S, T Grades	–55		+125	*		*	°C
Storage	–65		+150	*		*	°C

* Specifications same as ADC674AJP, AJH, ASH.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see Optional External Full Scale and Offset Adjustments section). (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20 V; for a 0 to +10V range, FS means 10V. The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendor's 674A type specification tables. (3) Using internal reference. (4) See Controlling the ADC674A section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to –16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... –0.5V to V_{LOGIC} +0.5V
Analog Inputs REF IN, BIP. OFF., $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering, 10s) ..... +300°C
Thermal Resistance, θ_{JA}: Ceramic ..... 50°C/W
Plastic ..... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC674As. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g., ADC674AKP-BI).

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR max (T_{MIN} to T_{MAX})
ADC674AJP	Plastic DIP	0°C to +75°C	±1LSB
ADC674AKP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC674AJH	Ceramic DIP	0°C to +75°C	±1LSB
ADC674AKH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC674ASH	Ceramic DIP	–55°C to +125°C	±1LSB
ADC674ATH	Ceramic DIP	–55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMPERATURE (160 Hours)(1)
ADC674AJP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC674AKP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC674AJH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC674AKH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC674ASH-BI	Ceramic DIP	–55°C to +125°C	+125°C
ADC674ATH-BI	Ceramic DIP	–55°C to +125°C	+125°C

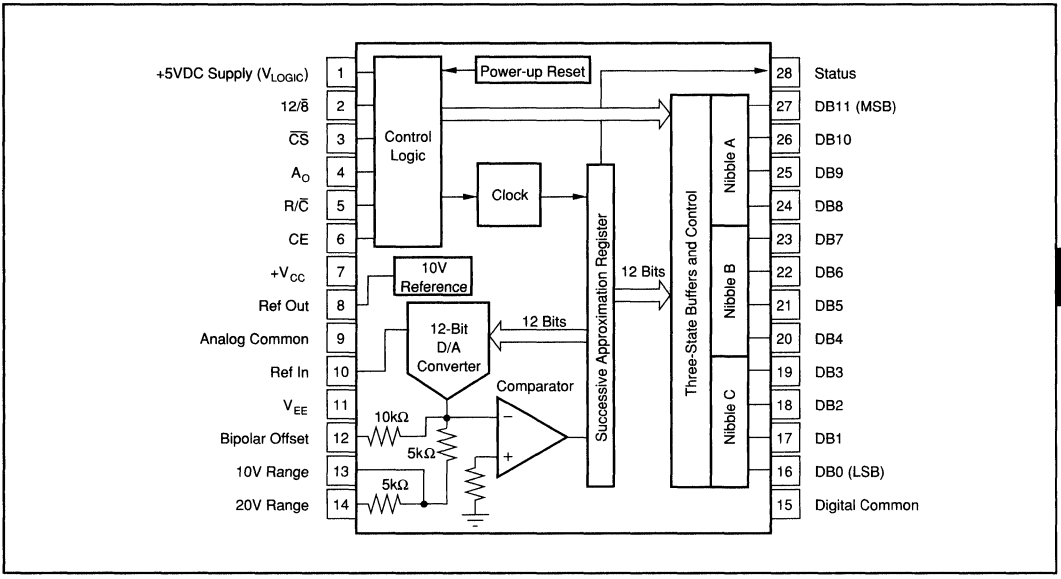
NOTE: (1) Or equivalent combination of time and temperature.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC674AJP	Plastic DIP	215
ADC674AKP	Plastic DIP	215
ADC674AJH	Ceramic DIP	149
ADC674AKH	Ceramic DIP	149
ADC674ASH	Ceramic DIP	149
ADC674ATH	Ceramic DIP	149
ADC674AJP-BI	Plastic DIP	215
ADC674AKP-BI	Plastic DIP	215
ADC674AJH-BI	Ceramic DIP	149
ADC674AKH-BI	Ceramic DIP	149
ADC674ASH-BI	Ceramic DIP	149
ADC674ATH-BI	Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION



CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/C input. Full control consists of selecting an 8- or 112-bit conversion cycle, initiating the conversion, and the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/8, CS, A_0, R/C, and CE) are all TTL-/CMOS-compatible. The functions of the control inputs are described in Table I. The control function truth table is listed in Table II.

CE	CS	R/C	12/8	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. Control Input Truth Table.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
CS (Pin 3)	Chip Select (active low)	Must be low ("0") ot either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/C (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses ±8MSBs (high byte) and A_0 = "1" accesses 4LSBs and trailing "0s" (low byte).
12/8 (Pin 2)	Data Mode Select ("1" = 12-bits)	When reading output data. 12/8 = "1" enables all 12 output bits simultaneously. 12/8 = "0" will enable the MSBs or LSBs as determined by the A_0 line. ("0" = 8-bits)

TABLE I. ADC674A Control Line Functions.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 1 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 2 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode, the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table III.

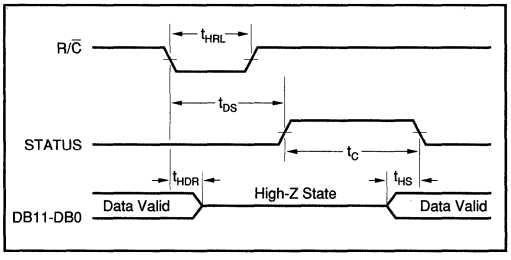


FIGURE 1. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversions.

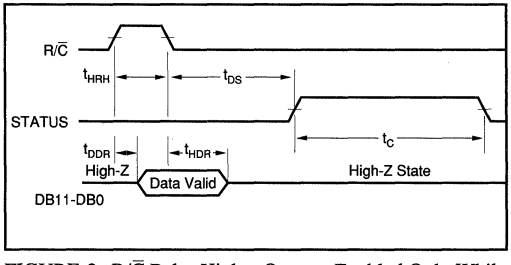


FIGURE 2. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE III. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion the 3LSBs (DB0 - DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table II. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 3. The specifications for timing are contained in Table IV.

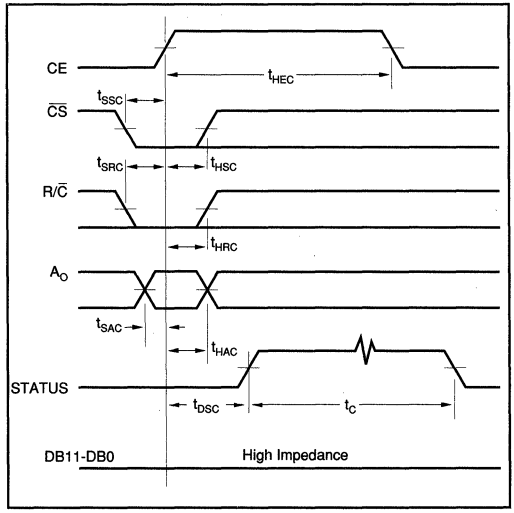


FIGURE 3. Conversion Cycle Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 To CE Setup	0			ns
t_{HAC}	A_0 Valid During CE high	50	20		ns
t_C	Conversion Time, 12 Bit Cycle	9	12	15	µs
	8 Bit Cycle	6	8	10	µs
Read Mode					
t_{DD}	Access Time From CE		75	150	ns
t_{HD}	Data Valid After CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0		ns
t_{HRR}	R/$\overline{C}$ high After CE Low		0		ns
t_{HAR}	A_0 Valid After CE Low		50		ns
t_{HS}	STS delay After Data Valid	100	300	600	ns

NOTE: Specifications are at + 25°C and measured at 50% level of transitions.

TABLE IV. Timing Specifications

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 4 and Table IV for timing relationships and specifications.

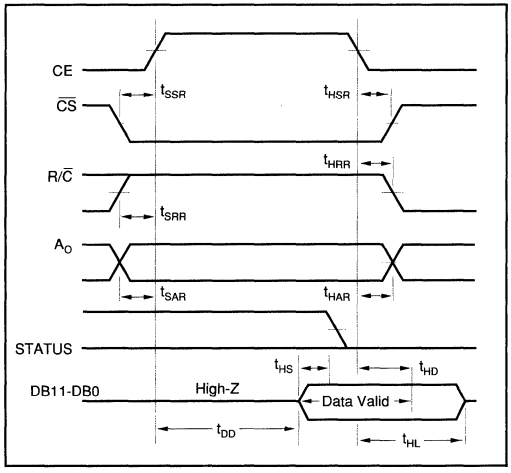


FIGURE 4. Read Cycle Timing.

BURR-BROWN®

ADC700

16-Bit Resolution with Microprocessor Interface A/D CONVERTER

FEATURES

- **COMPLETE WITH REFERENCE, CLOCK, 8-BIT PORT MICROPROCESSOR INTERFACE**
- **CONVERSION TIME: 17µs max**
- **LINEARITY ERROR: ±0.003% FSR max**
- **NO MISSING CODES TO 14 BITS OVER TEMPERATURE**
- **SPECIFIED AT ±12V AND ±15V SUPPLIES**
- **OUTPUT BUFFER LATCH FOR IMPROVED INTERFACE TIMING FLEXIBILITY**
- **PARALLEL AND SERIAL DATA OUTPUT**
- **SMALL PACKAGE: 28-Pin DIP**

DESCRIPTION

The ADC700 is a complete 16-bit resolution successive approximation analog-to-digital converter.

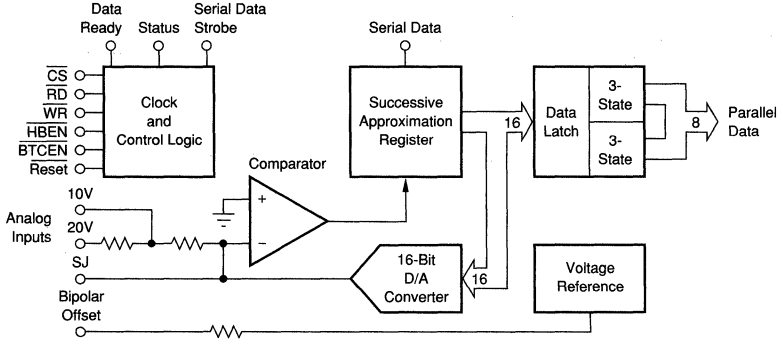
The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Gain and Zero errors may be externally trimmed to zero. Analog input ranges of 0V to +5V, 0V to +10V, 0V to +20V, ±2.5V, ±5V, and ±10V are available.

The conversion time is 17µs max for a 16-bit conversion over the three specification temperature ranges.

After a conversion, output data is stored in a latch separate from the successive approximation logic. This permits reading data during the next conversion, a feature that provides flexible interface timing, especially for interrupt-driven interfaces.

Data is available in two 8-bit bytes from TTL-compatible three-state output drivers. Output data is coded in Straight Binary for unipolar input signals and Bipolar Offset Binary or Twos complement for bipolar input signals. BOB or BTC is selected by a logic function available on one of the pins.

The ADC700 is available in commercial, industrial and military temperature ranges. It is packaged in a hermetic 28-pin side-braze ceramic DIP.



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SPECIFICATIONS

ELECTRICAL

At T_A = 25°C and at rated supplies: V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V, unless otherwise noted.

CHARACTERISTICS	ADC700JH,AH,RH MIN	ADC700JH,AH,RH TYP	ADC700JH,AH,RH MAX	ADC700KH,BH,SH MIN	ADC700KH,BH,SH TYP	ADC700KH,BH,SH MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0V to +5V, ±2.5V		2.5 ±1%			*		kΩ
0V to +10V, ±5V		5 ±1%			*		kΩ
0V to +20V, ±10V		10 ±1%			*		kΩ
DIGITAL SIGNALS (Over Specification Temperature Range)							
Inputs							
Logic Levels[1]							
V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±20			*	µA
Outputs							
Logic Levels							
V_{OL} (I_{OL} = −1.6mA)			+0.4			*	V
V_{OH} (I_{OH} = +20µA)	+2.4			*			V
$I_{LEAKAGE}$							
Data Outputs Only, High Z		10			*		nA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.006			±0.003	% of FSR[2]
Differential Linearity Error			±0.012			±0.006	% of FSR
Gain Error[3]		±0.1	±0.2		*	*	%
Zero Error[3]							
Bipolar Zero		±0.1	±0.2		*	*	% of FSR
Unipolar Zero		±0.05	±0.1		*	*	% of FSR
Noise at Transitions (3σp-p)		±0.001	±0.003		*	*	% of FSR
Power Supply Sensitivity							
$+V_{CC}$		±0.0015			*		%FSR/%V_{CC}
$-V_{CC}$		±0.0015			*		%FSR/%V_{CC}
V_{DD}		±0.0005			*		%FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)							
Gain Drift		±8	±15		*	*	ppm/°C
Zero Drift							
Bipolar Zero		±5	±10		*	*	ppm of FSR/°C
Unipolar Zero		±2	±4		*	*	ppm of FSR/°C
Linearity Drift		±1	±3		*	±2	ppm of FSR/°C
No Missing Codes Temperature Range							
JH (13-bit), KH (14-bit)	0		+70	*		*	°C
AH (13-bit), BH (14 bit)	−25		+85	*		*	°C
RH (13-bit), SH (14-bit)	−55		+125	*		*	°C
CONVERSION TIME 16 bits		15	17		*	*	µs
WARM-UP TIME	5			*			min
OUTPUT DATA CODES[4]							
Unipolar Parallel		USB			*		
Bipolar Parallel[5]		BTC, BOB			*		
Serial Output (NRZ)		USB, BOB			*		
POWER SUPPLY REQUIREMENTS							
Voltage Range							
$+V_{CC}$	+11.4	+15	+16	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16	*	*	*	VDC
V_{DD}	+4.75	+5	+5.25	*	*	*	VDC
Current[5]							
$+V_{CC}$		+10	+15		*	*	mA
$-V_{CC}$		−28	−35		*	*	mA
V_{DD}		+17	+20		*	*	mA
Power Dissipation		645	765		*	*	mW
TEMPERATURE RANGE							
Specification							
J, K Grades	0		+70	*		*	°C
A, B Grades	−25		+85	*		*	°C
R, S Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

TIMING SPECIFICATIONS[6]

At V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V, unless otherwise noted.

PARAMETER	LIMIT AT T_A = 25°C	LIMIT AT T_A = 0, +70°C −25°C, +85°C	LIMIT AT T_A = −55°C, +125°C	UNITS	DESCRIPTION
CONVERSION AND SERIAL DATA OUTPUT TIMING					
t_1	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Setup time
t_2	110	130	145	ns, max	$\overline{WR}$ to Status delay
t_3	40	40	40	ns, min	$\overline{WR}$ pulse width
t_4	0	0	0	ns, min	$\overline{CS}$ to $\overline{WR}$ Hold time
t_5	15	17	17	µs, max	Conversion time
t_6	550	600	650	ns, max	Data Ready to Status time
t_7	1100	1150	1250	ns, max	$\overline{WR}$ to first Serial Data Strobe
t_8	250	210	200	ns, min	First Serial Data to first Serial Data Strobe
t_9	310	360	400	ns, max	Last Serial Data Strobe to Status
t_{10}	0	0	0	ns, min	Status to $\overline{WR}$ Setup time
PARALLEL DATA OUTPUT TIMING					
t_{11}	0	0	0	ns, min	$\overline{HBEN}$ to $\overline{RD}$ Setup time
t_{12}	0	0	0	ns, min	$\overline{CS}$ to $\overline{RD}$ Setup time
t_{13}[7]	50	58	66	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 20pF (High Byte bus access time)
	70	81	95	ns, max	High Byte Data Valid after $\overline{RD}$ C_L = 100pF (High Byte bus access time)
t_{14}	40	40	40	ns, min	$\overline{RD}$ pulse width
t_{15}	40	45	50	ns, max	Data Ready delay from $\overline{RD}$ ($\overline{HBEN}$ asserted)
t_{16}[8]	50	60	65	ns, max	Data Hold time after $\overline{RD}$ (bus relinquish time)
t_{17}	0	0	0	ns, min	$\overline{RD}$ to $\overline{CS}$ Hold time
t_{18}	0	0	0	ns, min	$\overline{RD}$ to $\overline{HBEN}$ Hold time
RESET TIMING					
t_{19}	60	70	80	ns, max	Data Ready low delay from $\overline{Reset}$
t_{20}	70	81	95	ns, max	Status low delay from $\overline{Reset}$

*Same specs as ADC700JH, AH, RH.

NOTES: (1) TTL, LSTTL, and 5V CMOS compatible. (2) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (3) Externally adjustable to zero. (4) See Table I. USB – Unipolar Straight Binary; BTC – Binary Two's Complement; BOB – Bipolar Offset Binary; NRZ – Non Return to Zero. (5) Max supply current is specified at rated supply voltages. (6) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. (7) t_{13} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V. (8) t_{16} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

ABSOLUTE MAXIMUM RATINGS

$+V_{DD}$ to Digital Common	0V to +7V
$+V_{CC}$ to Analog Common	0V to +18V
$-V_{CC}$ to Analog Common	0V to −18V
Digital Common to Analog Common	−1V to +1V
Digital Inputs to Digital Common	−0.5V to V_{DD} + 0.5V
Analog Inputs	+16.5V
Power Dissipation	1000mW
Storage Temperature	−60°C to +150°C
Lead Temperature, (soldering, 10s)	+300°C

NOTES: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

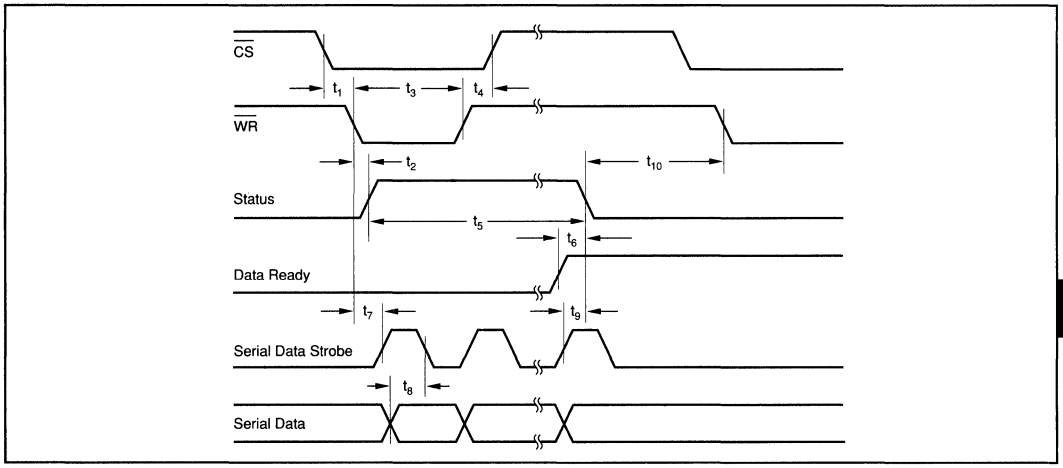
PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADC700JH	28-Pin Ceramic DIP	237
ADC700KH	28-Pin Ceramic DIP	237
ADC700AH	28-Pin Ceramic DIP	237
ADC700BH	28-Pin Ceramic DIP	237
ADC700RH	28-Pin Ceramic DIP	237
ADC700SH	28-Pin Ceramic DIP	237

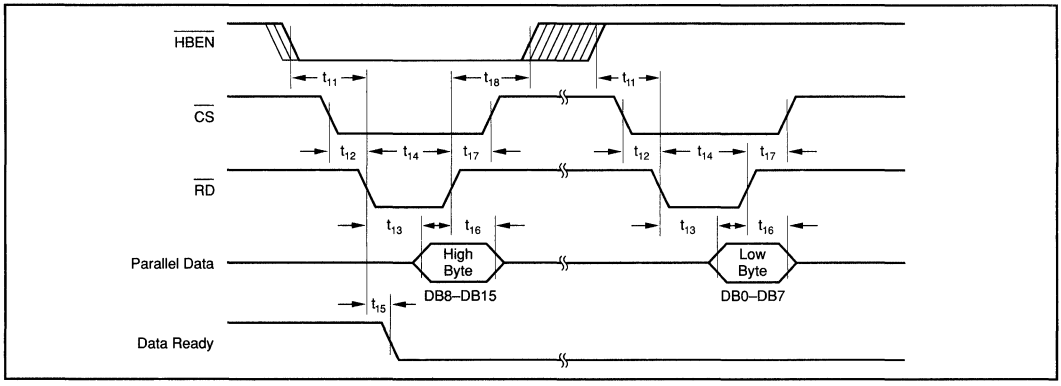
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

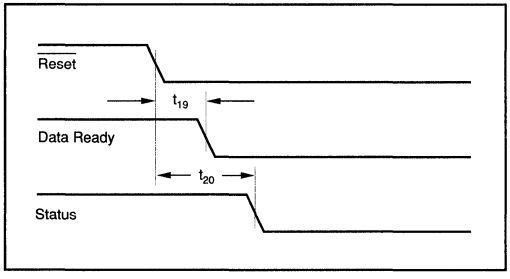
MODEL	TEMPERATURE RANGE	LINEARITY ERROR (%FSR)
ADC700JH	0°C to 70°C	±0.006
ADC700KH	0°C to 70°C	±0.003
ADC700AH	−25°C to +85°C	±0.006
ADC700BH	−25°C to +85°C	±0.003
ADC700RH	−55°C to +125°C	±0.006
ADC700SH	−55°C to +125°C	±0.003



Start of Conversion and Serial Data Output Timing.

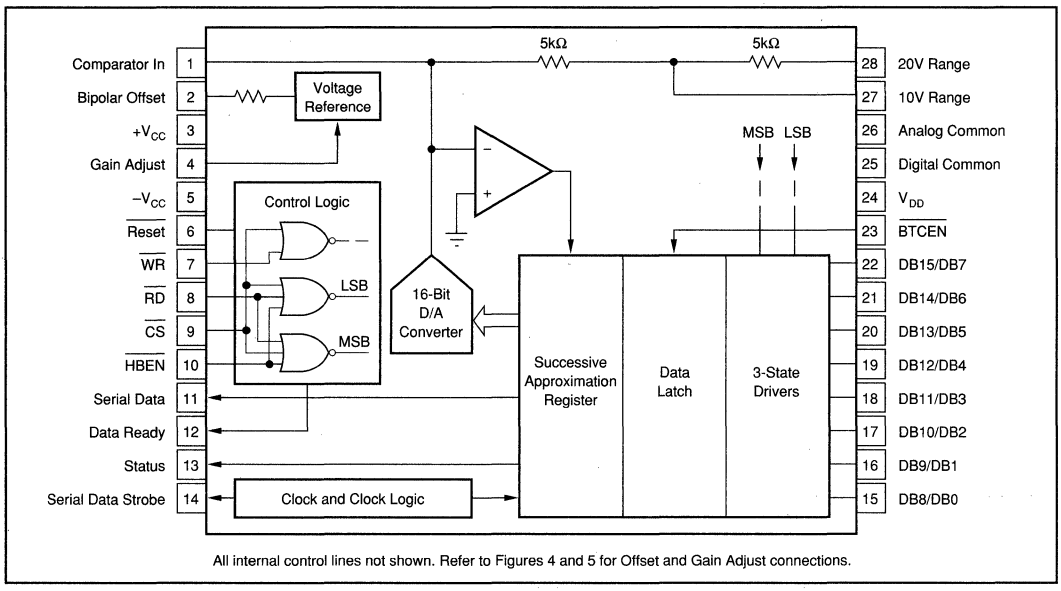


ADC700 Parallel Output Timing.



ADC700 Reset Function Timing Diagram.

PIN CONFIGURATION



All internal control lines not shown. Refer to Figures 4 and 5 for Offset and Gain Adjust connections.

DESCRIPTION AND OPERATING FEATURES

The ADC700 is a 16-bit resolution successive approximation A/D converter. Parallel digital data as well as serial data is available. Several features have been included in the ADC700 making it easier to interface with microprocessors and/or serial data systems. Several analog input ranges are available.

Some of the key operating features are described here. More detail is given in later sections of the data sheet. Refer to the block diagram above.

RESET

The ADC700 has a $\overline{\text{Reset}}$ input that must be asserted upon power-up or after a power interruption. This initializes the SAR, the output buffer register and Data Ready flag. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700.

PARALLEL DATA

The parallel data output is available through an 8-bit port with 3-state output drivers. High byte and low byte are selected by $\overline{\text{HBEN}}$ (pin 10).

A buffer/latch is included between the successive approximation register (SAR) and the 3-state drivers. This feature permits more flexible interface timing than is possible from most successive approximation converters.

The "old" word can be read during the next conversion. A Data Ready flag (pin 12) is asserted when a "new" word is in the buffer register. The Data Ready flag goes low ("0") when the most significant byte (high byte) is read. If the "old" word is not read, or if only the least significant byte (low byte) is read, Data Ready is not reset. The next conversion output will overwrite the data latch when the conversion is complete. The Data Ready flag remains high. Refer to timing diagrams in the Specifications section.

SERIAL DATA

Sixteen-bit serial data output is available (pin 11) along with a serial output strobe (pin 14). This serial data strobe is not the internal SAR clock but is a special strobe for serial data consisting of 16 negative-going edges (during conversion) occurring about 200ns after each serial data bit is valid. This feature eases the interface to shift registers or through opto-couplers for applications requiring galvanic isolation.

STATUS

The familiar Status (or Busy) flag, present in successive approximation A/D converters, is available (pin 13) and indicates that a conversion is in progress. Status is valid 110ns after assertion of the convert command ($\overline{\text{WR}}$ low). Status cannot be used as a sample-hold control because there is not enough time for the sample-hold to settle to the required error band before the ADC700 makes its first conversion decision.

CHIP SELECT

$\overline{\text{CS}}$ (pin 9) selects the ADC700. No other functions can be implemented unless $\overline{\text{CS}}$ is asserted. $\overline{\text{WR}}$ (pin 7) is the start-of-conversion strobe. $\overline{\text{RD}}$ strobes each output data byte, selected by $\overline{\text{HBEN}}$ (pin 10), to the 3-state drivers.

TWO'S COMPLEMENT DATA CODE

$\overline{\text{BTCEN}}$ (pin 23) is a logic function that implements the Binary Two's Complement output code for bipolar (+ and –) analog input signal operation. This feature is compatible with twos complement arithmetic in microprocessor math algorithms.

INTERNAL CLOCK

The ADC700 has a self-contained clock to sequence the A/D logic. The clock is not available externally. An external 16-pulse strobe (pin 14) is brought out to clock serial data only. Use of ADC700 with external clock is not possible.

INTERNAL VOLTAGE REFERENCE

The ADC700 has an internal low-noise buried-zener voltage reference. The reference circuit has been drift compensated over the MIL temperature range using a laser trim algorithm. The reference voltage is not available externally.

DISCUSSION OF SPECIFICATIONS

BASIC DEFINITIONS

Refer to Figure 3 for an illustration of A/D converter terminology and to Table II in the Calibration section.

Full Scale Range, FSR

The nominal range of the A/D converter. For ADC700, the FSR is 20V for the 0V to +20V and the –10V to +10V input ranges or 10V for the 0V to +10V and –5V to +5V input ranges.

Least Significant Bit, LSB

The smallest analog input change resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is $FSR(2^{-N})$.

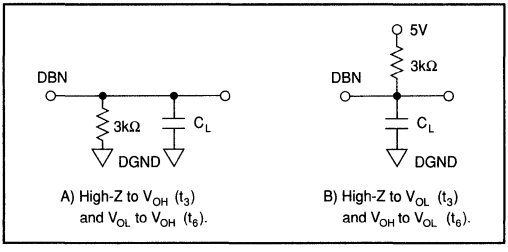


FIGURE 1. Load Circuits for Access Time.

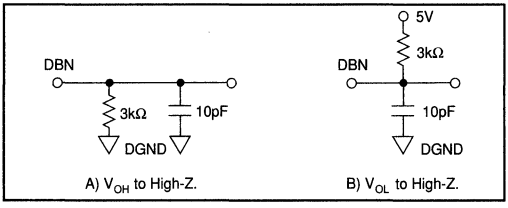


FIGURE 2. Load Circuits for Output Float Delay.

Most Significant Bit, MSB

That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution

An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

ACCURACY

Linearity Error, Integral Linearity Error (ILE)

Linearity Error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near positive full scale (at $+V_{FS}$ –1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at Zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$). Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADC700KH ILE is ±0.003% of FSR which is 1/2 LSB at 14-bits.

Differential Linearity Error (DLE), No Missing Codes

Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than –1LSB anywhere along the range, the A/D will have at least one missing code. ADC700KH is specified to have a DLE of ±0.006% of FSR, which is ±1LSB at 14 bits. ADC700KH is specified to have *no missing codes* at the 14-bit level over specified temperature ranges.

Gain Error

The deviation from the ideal magnitude of the input span between the first code midpoint (at $-V_{FS}$ + 1/2LSB, for bipolar operation; at Zero for unipolar operation) to the last code midpoint (V_{FS} –1LSB). As with the linearity error

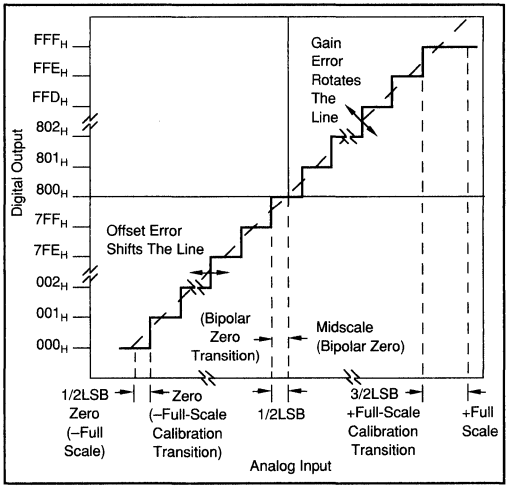


FIGURE 3. Transfer Characteristic Terminology.

measurements, code transition values are the locations actually measured for this spec. The ideal gain is V_{FSR} –2LSB. Gain Error is expressed in % (of reading). See Figure 3.

Gain Error of the ADC700 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error—The deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error—The deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at – V_{FS} +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADC700 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a percentage of FSR.

Bipolar Zero Error—The deviation of the actual mid-scale-code midpoint value from zero. Transition values are the actual measured parameter and it is 1/2 LSB below zero volts. The error is comprised of Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error of bit 1. Bipolar Zero Error is expressed as a percentage of FSR.

Power Supply Sensitivity

Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. PSR is specified in units of %FSR/% change in each supply voltage.

The major effect of power supply voltage deviations from the rated values will be a small change in the Gain (scale factor). Power Supply Sensitivity is also a function of ripple frequency. Figure 4 illustrates typical Power Supply Sensitivity performance of ADC700 versus ripple frequency.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADC700, system design problems such as ground path resistance and contact resistance become very important. For a 16-bit resolution converter with a +10V Full-Scale Range, 1LSB is 153µV. Circuit situations that cause only second- or third-order errors in 8-, 10-, or 12-bit A/D converters can induce first-order errors in 16-bit resolution devices.

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the analog and digital common lines.

Power Supply Returns (Analog Common and Digital Common)

Connect Analog Common and Digital Common together right at the converter with the ground plane. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. Connect a 1 to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing

Every power-supply line leading into an A/D converter must be bypassed to its common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground—connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 10µF to 100µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals

Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Shield Other Sensitive Points

The most critical of these is the comparator input (pin 1). If this pin is not used for offset adjustment, then it should be surrounded with ground plane or low-impedance power

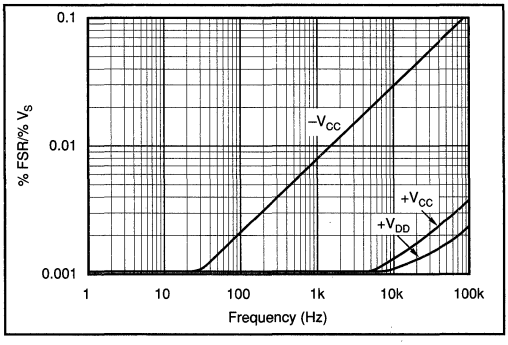


FIGURE 4. Power Supply Rejection Ripple vs Frequency.

supply plane. If it is used for offset adjustment, the series resistor and potentiometer should be located as close to the converter as possible.

The Gain Adjust (pin 4) is an input that has a relatively high input impedance and is susceptible to noise pickup. The Gain Adjust pin should be bypassed with a 0.01µF to 0.1µF capacitor whether or not the gain adjust feature is used.

If the 20V Analog input range is used (pin 28), the 10V Range input (pin 27) may need to be shielded with ground plane to reduce noise pickup.

ANALOG SIGNAL SOURCE IMPEDANCE

The input impedance of the ADC700, typical of most successive approximation A/D converters, is relatively low (2.5kΩ to 10kΩ). The input current of a successive approximation A/D converter changes rapidly during the conversion algorithm as each bit current is compared to the analog input current. Since the output impedance of a closed-loop amplifier or a sample-hold amplifier increases with frequency and, in addition, the amplifier must settle to the required accuracy in time for the next comparison/decision after such a disturbance, care must be taken to select the proper driving amplifier.

Unfortunately, high-accuracy operational amplifiers tend to have low bandwidth, while wide-band amplifiers tend to have lower accuracy. One solution is to use a wide-band but perhaps less precise amplifier. Another solution is to add a wide-band buffer amplifier such as the Burr-Brown OPA633 inside the feedback loop of a slower (but precision) amplifier, Figure 5. This reduces the output impedance at high frequencies yet preserves the accuracy at low frequencies. When a sample/hold is needed, a high-linearity, high-speed sample/hold such as the Burr-Brown SHC76 should be used to drive the ADC700.

ANALOG INPUT RANGES

The analog input circuits of the ADC700 can be connected to accept unipolar or bipolar input signals. These ranges and connections are tabulated in Table I. Circuit connections are shown in Figures 6 and 7. Gain and offset adjustments are described in the calibration section.

To operate the ADC700 with a range that gives other convenient values for the LSB, the input resistor may be increased or decreased slightly without seriously affecting the Gain Drift of the converter. Since the input resistors of the ADC700 are within ±2% from unit to unit, this can be consistently done with a fixed series or parallel resistor. The ADC700 can then be calibrated using the Gain and Offset adjustments described in the calibration section. For example, using the ±10V input range, one can decrease the range slightly by paralleling the 10kΩ input resistor (pin 28 to pin 1) with a 610kΩ metal film resistor to achieve a 300µV LSB instead of the nominal standard 305.17578µV binary LSB.

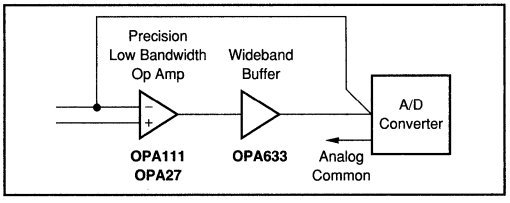


FIGURE 5. Wideband Buffer Reduces Output Impedance at High Frequencies.

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Gain and Offset Error may be trimmed to zero using external Gain and Offset trim potentiometers connected to the ADC700 as shown in Figures 6 and Figure 7. A calibration procedure in described in the Operating Instructions section.

Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature. These potentiometers may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 1 (Comparator In) and pin 4 (Gain Adjust) may be left open if no external adjustment is planned; however, pin 4 should always be bypassed with 0.01µF or larger to Analog Common.

OPERATING INSTRUCTIONS

CALIBRATION

Offset and Gain may be trimmed by external Offset and Gain potentiometers. Offset is adjusted first and then Gain. Calibration values are listed in Table II for all ADC700 input ranges. Offset and Gain calibration can be accomplished to a precision of about ±1/2LSB using a static adjustment procedure described below. By summing a small sine or triangular wave voltage with the accurate calibration voltage applied to the analog input, the output can be swept through each of the calibration codes to more accurately determine the transition points listed in Table II. NOTE: The transition points are not the same as the code midpoints used in the static calibration example.

OFFSET ADJUSTMENT, 14-BIT RESOLUTION EXAMPLE

Static Adjustment Procedure (At Code Midpoints)

0V to +10V Range—Set the analog input to $+1LSB_{14}$ = 0.00061V. Adjust the Offset potentiometer for a digital output of 0004_H. Set the analog input to +Full Scale – $2LSB_{14}$ = +9.9987V. Adjust the Gain potentiometer for a digital output of $FFFC_H$. For a half-scale calibration check, set the analog input to +5.0000V and read a digital output code of 8000_H.

INPUT SIGNAL RANGE	OUTPUT CODE		CONNECT PIN 2 TO PIN	CONNECT PIN 28 TO PIN	CONNECT SIGNAL TO PIN
	$\overline{BTCEN}$ = 1	$\overline{BTCEN}$ = 0			
±10V	BOB	BTC	1	Input Signal	28
±5V	BOB	BTC	1	Open	27
±2.5V	BOB	BTC	1	Pin 1	27
0V to +5V	USB	—	26	Pin 1	27
0V to +10V	USB	—	26	Open	27
0V to +20V	USB	—	26	Input Signal	28

TABLE I. ADC700 Input Range Connections.

ANALOG INPUT RANGE	VOLTAGE (V)					
	±10	±5	±2.5	0 TO +20	0 TO +10	0 TO +5
$+V_{FS}$	+10	+5	+2.5	+20	+10	+5
$-V_{FS}$	−10	−5	−2.5	0	0	0
FSR	20	10	5	20	10	5
TRANSITION CODES (Hexadecimal)	**TRANSITION VALUES (V)**					
For 16-bit Resolution (Reading all 16 bits)						
$FFFE_H$ to $FFFF_H$	+9.999542	+4.999771	+2.499886	+19.999542	+9.99971	+4.999886
$7FFF_H$ to 8000_H	−152.5µV	−38µV	−19µV	+9.999847	+4.999924	+2.499962
0000_H to 0001_H	−9.999847	−4.999924	−2.499962	+152µV	+76µV	+38µV
LSB (FSR/2^{16})	305µV	153µV	38µV	305µV	153µV	76µV
For 15-bit Resolution (Reading all 16 bits, Ignoring DB_0)						
$FFFD_H$ to $7FFE_H$	+9.999084	+4.999542	+2.499771	+19.999084	+9.999542	+4.999771
$7FFE_H$ to 8000_H	−305µV	−153µV	−76µV	+9.999625	+4.999847	+2.499924
0000_H to 0002_H	−9.999695	−4.999847	−2.499924	+305µV	+152µV	+76µV
LSB (FSR/2^{15})	610µV	305µV	153µV	610µV	305µV	153µV
For 14-bit Resolution (Reading all 16 bits, Ignoring DB_0 and DB_1)						
$FFFC_H$ to $FFFD_H$	+9.99817	+4.99908	+2.49954	+19.99817	+9.99908	+4.99954
$7FFD_H$ to 8000_H	−610µV	−305µV	−153µV	+9.99939	+4.999695	+2.499847
0000_H to 0004_H	−9.999390	−4.999694	−2.499847	+610µV	+305µV	+153µV
LSB (FSR/2^{14})	1221µV	610µV	305µV	1221µV	610µV	305µV

TABLE II. Transition Values for Calibration.

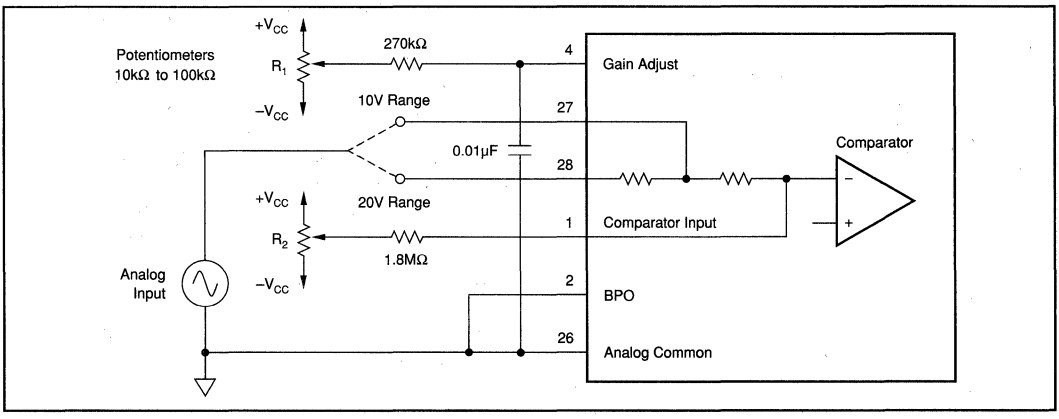


FIGURE 6. Unipolar Input Configuration with Gain and Offset Adjust Connections.

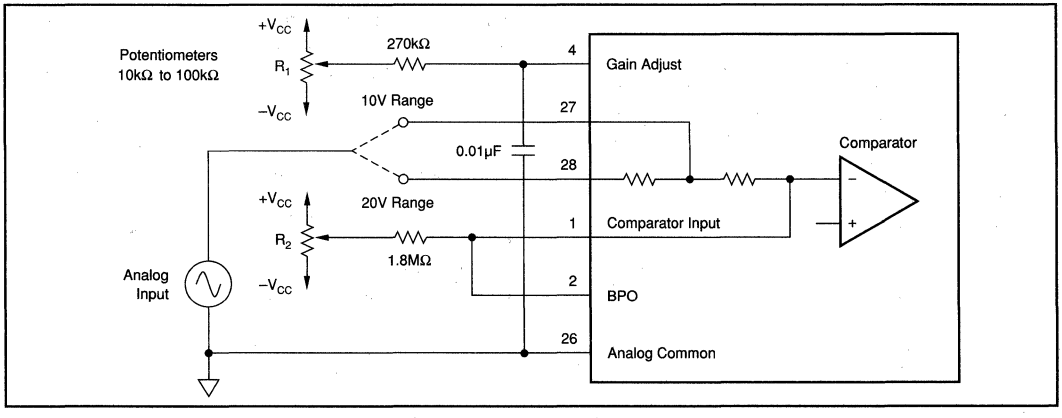


FIGURE 7. Bipolar Input Configuration with Gain and Offset Adjust Connections.

–10V to +10V Range—Set the analog input to –FS + $1LSB_{14}$ = –9.99878V. Adjust the Offset potentiometer for a digital output of 0004_H (8004_H if $\overline{BTCEN}$ is asserted). Set the analog input to +9.9976V. Adjust the Gain potentiometer for a digital output of $FFFC_H$ ($7FFC_H$ if $\overline{BTCEN}$ is assrted). For a half-scale calibration check, set the analog input to 0.0000V and read a digital output code of 8000_H (0000_H if $\overline{BTCEN}$ is asserted).

CONTROLLING AND INTERFACING THE ADC700

RESET

The ADC700 requires a Reset command upon power-up or after a power interruption to guarantee the condition of internal registers. If Status powers-up High, no conversion can be started. Reset initializes the SAR, the output buffer register, and the Data Ready flag and terminates a conversion in progress. Since microprocessor systems already use a power-on reset circuit, the same system reset signal can be used to initialize the ADC700. A power-up circuit is shown in Figure 8. Refer to Reset function timing diagram following the Timing Specifications Table.

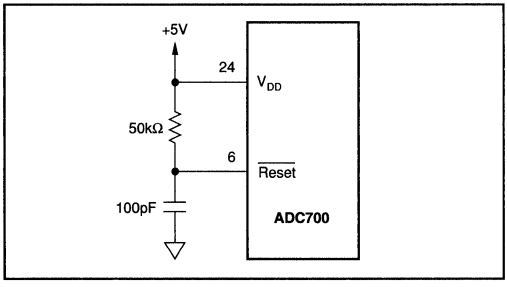


FIGURE 8. Power-Up Reset Circuit.

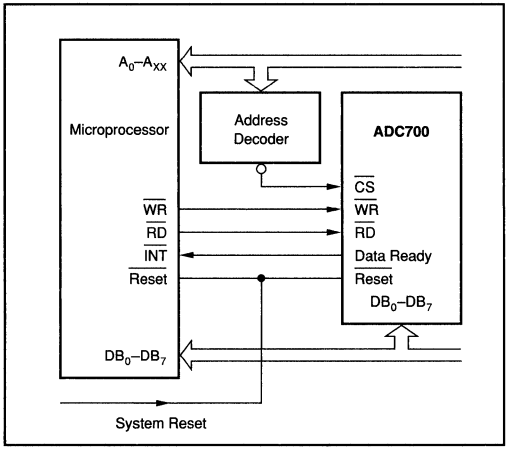


FIGURE 9. Parallel Data Bus Interface.

START OF CONVERSION

A conversion is started by asserting $\overline{CS}$ and $\overline{WR}$ Low. Status goes high about $t = t_1 + t_2 = 110ns$ later. The first successive approximation decision occurs about 900ns after $\overline{WR}$ is asserted. Status goes Low after the conversion is complete. Refer to Start of Conversion and Serial Data Output Timing following the Timing Specifications Table.

DATA READY FLAG

The data latch feature permits data to be read during the following conversion. The Data Ready flag indicates that the data from the most recent conversion is latched in the output data latch and that it hasn't been read. Data Ready remains High until the most significant data byte is read. If a subsequent conversion is initiated and completed, the new word will be stored in the output data latch regardless of the state of the Data Ready flag. The preceding word will be overwritten and lost.

READING PARALLEL DATA

Parallel data is latched in the output data latch at the end of a conversion. Data can be read any time, even during the subsequent conversion. The output data latch is not cleared by reading the data. Only the Data Ready flag is cleared by reading the MSB.

The output three-state drivers are enabled by asserting the $\overline{CS}$ and $\overline{RD}$ inputs Low. When $\overline{HBEN}$ is Low, the most significant eight bits are enabled and the Data Ready flag is cleared. When $\overline{HBEN}$ is High, the least significant eight bits are enabled. Refer to Parallel Data Output Timing information following the Timing Specifications Table.

To reduce noise interference to the absolute minimum, data should be read after the current conversion is complete. However, data can be read during the following conversion, with minimal interference, to maximize the sampling rate of the converter.

A typical parallel interface is illustrated in Figure 9.

READING SERIAL DATA

Serial data output of the ADC700 is facilitated by a Serial Data Strobe that provides 16 negative-going edges for strobing an external serial to parallel shift register located perhaps on the other side of an opto-coupler. Refer to the Serial Data Timing information following the Timing Specifications Table. An example of an isolation connection using the serial port feature is illustrated in Figure 10.

CONTINUOUS CONVERSION OPERATION

When $\overline{CS}$ is permanently connected to Digital Common and Status is connected to $\overline{WR}$, Figure 11, the ADC700 will continuously convert. The repetition time will not be precise and will vary slightly with the temperature for the ADC700 because the time will be determined by the internal clock frequency and control-circuit gate delays. If a precise repetition rate is needed, the continuous conversion connection should not be used.

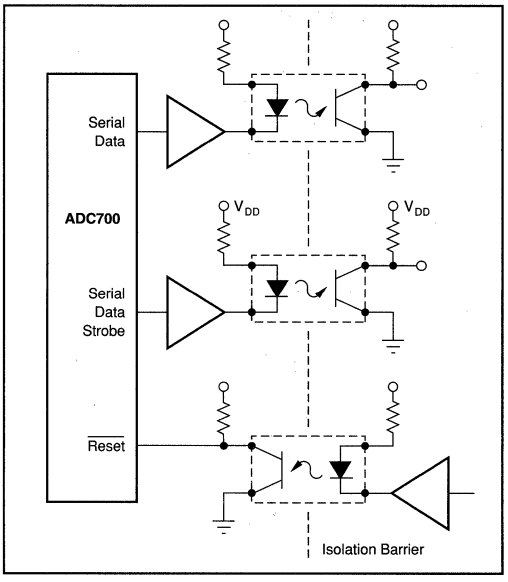


FIGURE 10. Serial Data Output Providing Convenient Isolation.

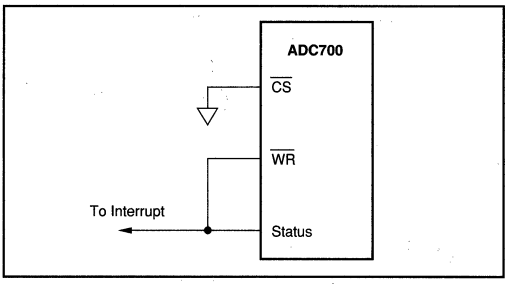


FIGURE 11. Continuous Conversion Circuit Connection.

PIN DESIGNATION	DEFINITION	FUNCTION
$\overline{CS}$ (Pin 9)	Chip Select	Must be Low to either initiate a conversion or read output data.
$\overline{WR}$ (Pin 7)	Write (Convert)	Conversion begins after the High-to-Low transition.
$\overline{RD}$ (Pin 8)	Read	Turns ON the three-state output drivers upon being asserted low.
$\overline{HBEN}$ (Pin 10)	High Byte Enable "1" = Low Byte "0" = High Byte	Selects the MSB or the LSB for readout. Data Ready is cleared when $\overline{HBEN}$ is Low and $\overline{RD}$ is asserted.
$\overline{Reset}$ (Pin 6)	Reset	Resets internal logic. Must be asserted after power-up or a power interruption clears Status and Data Ready to Low.
$\overline{BTCEN}$ (Pin 23)	BTC Enable	Sets the output code to Binary Twos Complement (BTC) when Low. Output code is Bipolar Offset Binary (BOB) when High.

TABLE III. Control Line Functions.

CONTROL LINE					
$\overline{RESET}$	$\overline{WR}$	$\overline{RD}$	$\overline{HBEN}$	$\overline{CS}$	OPERATION
0	X	X	X	X	Reset converter logic. Status and Data Ready set Low.
1	X	X	X	1	No operation.
1	0	X	X	0	Initiate conversion.
1	1	0	0	0	Places High Byte on output port. Clears Data Ready flag.
1	1	0	1	0	Placed Low Byte on output port. Does not clear Data Ready flag.
1	0	0	0	0	Initiates conversion and places High Byte or output port. Clears Data Ready.
1	0	0	1	0	Initiates conversion and places Low Byte on output port. Does not clear Data Ready flag.
NOTE: If a conversion command is asserted while a conversion is in progress, the command is ignored. If the conversion command remains asserted when a conversion is finished, a new conversion will begin.					

TABLE IV. Control Input Truth Table.

Because the last data-word is stored in the data latch, it is possible to read it during the next A/D conversion. Assertion of $\overline{CS}$ and $\overline{HBEN}$ for reading parallel data should be timed from Status going low. The two-byte read operation must be complete before the conversion in process is complete or the Data Read is invalid.

Serial Data is available during continuous conversion with word synchronization available from STATUS.

USING A SAMPLE/HOLD WITH ADC700

Figure 12 illustrates using ADC700 with the Burr-Brown SHC76. The sample-to-hold settling time (to 14 bits, ±0.003%FSR) of the SHC76 is 1µs typ, 3µs max. The time from the Status going High to the first conversion decision is about 900ns. Therefore a time delay between the Sample-to-Hold command to the $\overline{WR}$ command to the ADC700 is required.

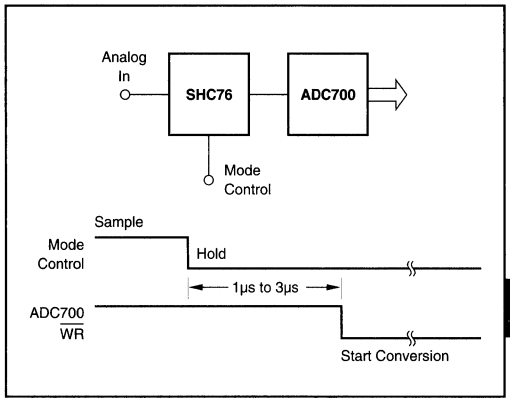
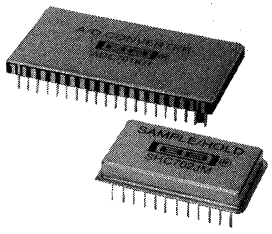


FIGURE 12. Using Sample/Hold with ADC700 Requires Time Delay Between Sample and Start-of-Conversion.

BURR - BROWN®



ADC701
SHC702

16-Bit 512kHz SAMPLING A/D CONVERTER SYSTEM

FEATURES

- CONVERSION RATE: to 512kHz Over Temp
- NO MISSING CODES AT 16 BITS
- SPURIOUS-FREE DYNAMIC RANGE: 107dB
- LOW NONLINEARITY: ±0.0015%
- SELECTABLE INPUT RANGES: ±5V, ±10V, 0 to +10V, 0 to +5V, –10V to 0
- LOW POWER DISSIPATION: 2.8W Typical Including Sample/Hold
- METAL AND CERAMIC DIP PACKAGES

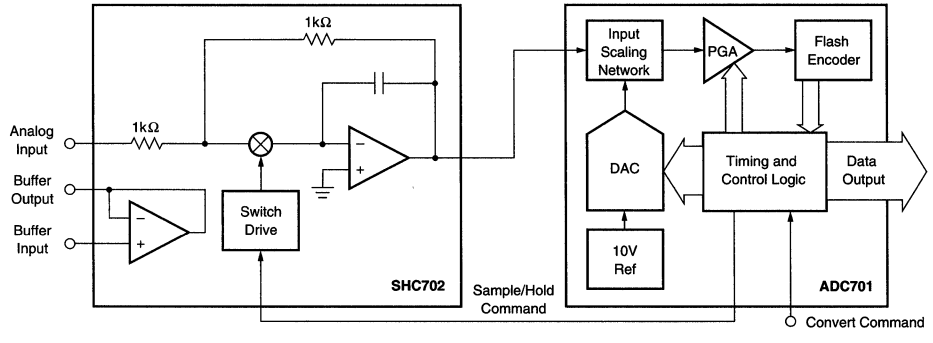
APPLICATIONS

- MEDICAL IMAGING
- SONAR
- PROFESSIONAL AUDIO RECORDING
- AUTOMATIC TEST EQUIPMENT
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- ULTRASOUND SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- REPLACES DISCRETE MODULAR ADCs

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

At T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five-minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH MIN	ADC701JH TYP	ADC701JH MAX	ADC701KH MIN	ADC701KH TYP	ADC701KH MAX	UNITS
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar			0 to +5, 0 to +10, −10 to 0				V
	Bipolar			±5, ±10				V
Resistance	0 to +5V Range	2.45	2.5	2.55	*	*	*	kΩ
	0 to +10V, −10 to 0, ±5V Ranges	4.9	5	5.1	*	*	*	kΩ
	±10V Range	9.8	10	10.2	*	*	*	kΩ
Capacitance	All Ranges		5			*		pF
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Convert Command	Start Conversion			Rising Edge				
Pulse Width	t = Conversion Period	50		t − 50	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[1]	0 to +10V Range		±0.03	±0.1		*	*	%
	±10V Range		±0.03	±0.1		*	*	%
Power Supply Sensitivity of Gain	All Ranges, All Supplies		±0.005	±0.1		*	*	%/V
Input Offset Error[1]	0 to +10V Range		±1	±3		*	*	mV
	±10V Range		±5	±10		*	*	mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		±0.006	±0.1		*	*	%FSR/V
Integral Linearity Error[2]			±0.002	±0.003		±0.0012	*	%FSR[3]
Differential Linearity Error[2]			±0.0006	±0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{SOURCE} \leq 50\Omega$		0.6			*		LSB rms
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		512	*		*	kHz
Conversion Time[4]	Unadjusted		1.45	1.5		*	*	µs
OUTPUTS								
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Data Coding	Unipolar Ranges			Straight Binary				
	Bipolar Ranges			Offset Binary				
Logic "0" Levels (V_{OL})	$I_{OL} \leq 3.2$mA		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \leq 80\mu$A	4	4.9		*	*		V
Data Valid Setup Time Before Strobe	Both Edges	28	37		*	*		ns
INTERNAL REFERENCE								
Voltage	$R_{LOAD} \geq 5k\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*		mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		−4.25	−5	−6	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30		*	*	mA
$-I_{CC}$			33	45		*	*	mA
$+I_{DD1}$			45	55		*	*	mA
$-I_{DD1}$			37	50		*	*	mA
$+I_{DD2}$			133	150		*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A Min to T_A Max	+15		+55	0		+70	°C
Gain Error	All Ranges		±10	±15		*	*	ppm/°C
Input Offset Error	All Unipolar Ranges		±1	±5		*	*	ppm FSR/°C
	All Bipolar Ranges		±1	±5		*	*	ppm FSR/°C
Integral Linearity Error[2]			±0.2			*	±0.5	ppm/°C
Differential Linearity Error[2]			±0.05			*	±0.3	ppm/°C
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			±3			*		ppm/°C
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/°C
Sample Rate	Unadjusted	DC		512	*		*	kHz

* Same specifications as ADC701JH.

SPECIFICATIONS

ELECTRICAL (SHC702 ONLY)

At T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, and five-minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	SHC702JM MIN	SHC702JM TYP	SHC702JM MAX	UNITS
INPUTS (Without Input Buffer)					
ANALOG					
Voltage Range		±10.25	±11		V
Resistance		0.98	1	1.02	kΩ
Capacitance			3		pF
DIGITAL					
Logic Family			LSTTL		
Input Loading			2		LSTTL Loads
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain	R_{SOURCE} = 0Ω		–1		V/V
Gain Error	R_{SOURCE} = 0Ω		±0.02	±0.1	%
Linearity Error	Sample Mode		±0.0003		%FSR
Offset Error	Sample Mode		±0.5	±3	mV
Charge Offset (Pedestal) Error	Sample/Hold Mode, $R_{SOURCE} \leq 50\Omega$		±0.5	±5	mV
Droop Rate	Hold Mode		±0.2	±2	µV/µs
Dynamic Nonlinearity	Sample/Hold Mode		±0.0005		%FSR
Power Supply Sensitivity	Offset Plus Charge Offset, All Supplies		±0.003		%FSR/V
DYNAMIC CHARACTERISTICS					
Acquisition Time	10V Step to ±150µV		600		ns
	5V Step to ±150µV		500		ns
Sample-to-Hold Settling Time[5]	to ±150µV		120		ns
Aperture Delay Time			20		ns
Aperture Uncertainty (Jitter)			10	25	ps rms
Slew Rate			150		V/µs
Small Signal Bandwidth	V_{IN} = ±1V		3.1		MHz
Full-Power Bandwidth	V_{IN} = ±10V		2		MHz
Feedthrough Rejection	Hold Mode, 10Vp-p Square Wave Input		0.001		%
OUTPUT					
Voltage Range	$R_{LOAD} \geq 1k\Omega$	±10.25	±11		V
Output Current		±40			mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
Output Impedance	DC		0.01	0.1	Ω
INPUT BUFFER CHARACTERISTICS					
INPUT					
Impedance			10^{13} || 3		Ω||pF
Bias Current	V_{IN} = ±10V		±2	±15	pA
Offset Voltage	$R_{SOURCE} \leq 10k\Omega$		±0.3	±1.5	mV
Voltage Range		±10.25	±11		V
DYNAMIC CHARACTERISTICS					
Slew Rate		20	35		V/µs
Full-Power Bandwidth	V_{IN} = ±10V		570		kHz
Settling Time	10V Step to ±150µV		1.7		µs
OUTPUT					
Output Current		±15	±20		mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$	Operating	+13.5	+15	+16.5	V
$-V_{CC}$		–13.5	–15	–16.5	V
$+V_{DD1}$		+4.75	+5	+5.25	V
Current: $+I_{CC}$	Operating		33	40	mA
$-I_{CC}$			18	25	mA
$+I_{DD1}$			5	10	mA
Power Dissipation	Nominal Voltages		790	950	mW
PERFORMANCE OVER TEMPERATURE					
Specification Temperature Range	T_A Min to T_A Max	0		+70	°C
Sample/Hold Gain Error	R_{SOURCE} = 0Ω		±1	±5	ppm/°C
Sample/Hold Offset Error	$R_{SOURCE} \leq 50\Omega$		±10	±30	µV/°C
Sample/Hold Charge Offset Error	$R_{SOURCE} \leq 50\Omega$		±10	±80	µV/°C
Droop Rate				±50	µV/µs
Buffer Offset Error	$R_{SOURCE} \leq 10k\Omega$		±3	±15	µV/°C

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and ±10V ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected. (4) ADC conversion time is defined as the time that the Sample/Hold must remain in the Hold mode; i.e., the duration of the Sample/Hold command. This time must be added to the Sample/Hold acqusition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

SPECIFICATIONS

ELECTRICAL (COMBINED ADC701/SHC702)

At T_A= +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five-minute warmup in a convection environment, ±5V input range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Rate	Unadjusted	DC		512	kHz
Dynamic Nonlinearity			±0.002		%FSR
Total Harmonic Distortion (THD)	f_{IN} = 20kHz (–0.3dB)		–103		dB
	f_{IN} = 199kHz (–0.2dB)		–82		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 20kHz (–0.3dB)		107		dB
	f_{IN} = 199kHz (–12dB)		94		dB
Two-Tone Intermodulation Distortion (IMD)	f_1 = 195kHz (–6.5dB), f_2 = 200kHz (–6.5dB)		–81		dBC
	f_1 = 195kHz (–12.5dB), fF_2 = 200kHz (–12.5dB)		–86		dBC
Signal-to-Noise Ratio (SNR)	f_{IN} = 5kHz (–0.5dB)		93		dB
Total Power Dissipation	Operating		2.8	3.25	W

ADC701 PIN ASSIGNMENTS

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Bit 1/9 (Bit 1 = MSB)	40	$-V_{DD1}$ (–5V) Analog
2	Bit 2/10	39	Common (Analog)
3	Bit 3/11	38	$+V_{DD1}$ (+5V) Analog
4	Bit 4/12	37	Reference (Gain) Adjust
5	Bit 5/13	36	+10V Reference Output(2)
6	Bit 6/14	35	Common (Reference)
7	Bit 7/15	34	DNC
8	Bit 8/16	33	Common (Analog)
9	Clip Detect Output	32	+10V Reference Input(2)
10	$+V_{DD2}$ (+5V) Digital	31	Input D (1)
11	Common (Digital)	30	Input C (1)
12	Data Strobe	29	Common (Signal)
13	High/Low Byte Select	28	Input B (1)
14	Convert Command	27	Input A (1)
15	Sample/Hold Control(3)	26	$-V_{CC}$ (–15V) Analog
16	Common (Digital)	25	Common (Power)
17	Common (Digital)	24	$+V_{CC}$ (+15V) Analog
18	Clock Adjust	23	DNC(4)
19	Common (Digital)	22	Offset Adjust
20	$+V_{DD2}$ (+5V) Digital	21	Offset Adjust

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC701JH	Metal and Ceramic	230
ADC701KH	Metal and Ceramic	230

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ADC701 ORDERING INFORMATION

ADC701 ( ) H

Basic Model Number

Performance Grade Code
- K: 0°C to +70°C Ambient Temperature
- J: +15°C to +55°C Ambient Temperature

Package Code
- H: Metal and Ceramic

ADC701 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$\pm V_{DD1}$, $+V_{DD2}$	±7V, +7V
Analog Input	$\pm V_{CC}$
Logic Input	–0.5V to ($+V_{DD2}$ + 0.3V)
Logic Output	±25mA
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	3W

Stresses above these ratings may permanently damage the device.

ADC701 OUTPUT CODING

INPUT LEVEL (Exact Center of Code)	NOMINAL INPUT VOLTAGE TO ADC701 (Multiply by –1 for SHC702 Input Voltage) 0–10V RANGE (1LSB ≈153µV)	±10V RANGE (1LSB ≈05µV	±5V RANGE (1LSB ≈153µV)	OUTPUT CODE (1 = Logic High) MSB LSB	CLIP DETECT
Underrange	< –76µV	< –10.000153V	< –5.000076V	0000 0000 0000 0000	1
–FS	0V	–10V	–5V	0000 0000 0000 0000	0
–FS + 1LSB	+153µV	–9.999695V	–4.999847V	0000 0000 0000 0001	0
–3/4FS	+1.25V	–7.5V	–3.75V	0010 0000 0000 0000	0
–1/2FS	+2.5V	–5V	–2.5V	0100 0000 0000 0000	0
–1/4FS	+3.75V	–2.5V	–1.25V	0110 0000 0000 0000	0
–1LSB	+4.999847V	–305µV	–153µV	0111 1111 1111 1111	0
Mid-Scale	+5V	0V	0V	1000 0000 0000 0000	0
+1LSB	+5.000153V	+305µV	+153µV	1000 0000 0000 0001	0
+1/4FS	+6.25V	+2.5V	+1.25V	1010 0000 0000 0000	0
+1/2FS	+7.5V	+5V	+2.5V	1100 0000 0000 0000	0
+3/4FS	+8.75V	+7.5V	+3.75V	1110 0000 0000 0000	0
+FS –2LSB	+9.999695V	+9.99939V	+4.999695V	1111 1111 1111 1110	0
+FS – 1LSB	+9.999847V	+9.999695V	+4.999847V	1111 1111 1111 1111	0
Overrange	> +9.999924V	> +9.999847V	> +4.999924V	1111 1111 1111 1111	1

SHC702 PIN ASSIGNMENTS

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Sample/Hold Output	24	$+V_{CC}$ (+15V) Analog
2	NC[3]	23	Common (Power)
3	NC	22	$-V_{CC}$ (–15V) Analog
4	NC	21	Common (Analog)
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	Buffer Amp Input[2]
9	$+V_{DD1}$ (+5V) Analog	16	NC
10	Common (Digital)	15	Common (Signal)
11	$\overline{\text{Hold}}$ Input[1]	14	Buffer Amp Output
12	Hold Input[1]	13	Analog Input

NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC702JM	24-Pin	113

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

SHC702 ORDERING INFORMATION

SHC702 J M

Basic Model Number

Performance Grade Code

J: 0°C to +70°C Ambient Temperature

Package Code

M: Metal

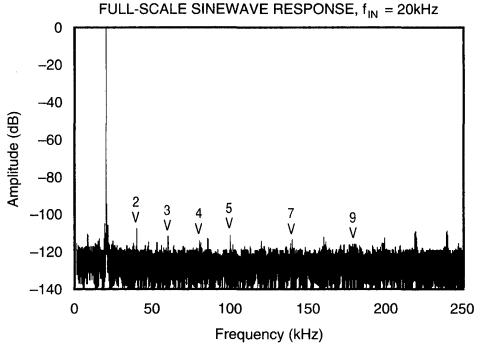
SHC702 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD1}$	+7V
Analog and Buffer Inputs	$\pm V_{CC}$
Outputs	Indefinite Short to Common
Logic Inputs	–0.5V to ($+V_{DD1}$ + 0.3V)
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	1.5W

Stresses above these ratings may permanently damage the device.

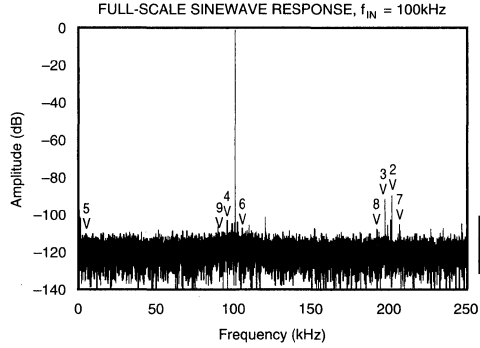
TYPICAL DYNAMIC PERFORMANCE (ADC701/SHC702)[1]

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 20kHz



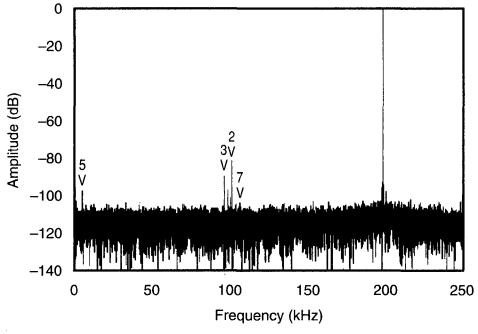
Input Frequency	19.9890136719 kHz		
Fundamental	–0.3 dB	4th Harmonic	–115.6 dB
2nd Harmonic	–107.5 dB	5th Harmonic	–111.2 dB
3rd Harmonic	–111.5 dB	6th Harmonic	–124.5 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 100kHz



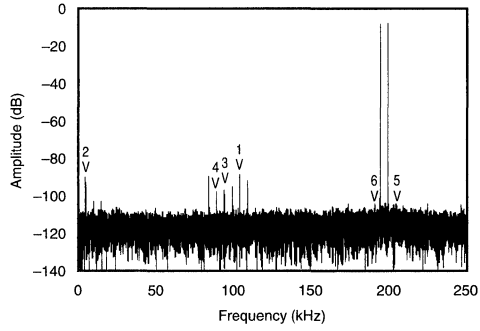
Input Frequency	100.982666016 kHz		
Fundamental	–0.5 dB	4th Harmonic	–102.5 dB
2nd Harmonic	–89.1 dB	5th Harmonic	–110.2 dB
3rd Harmonic	–90.5 dB	6th Harmonic	–106.8 dB

FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 200kHz



Input Frequency	199.005126953 kHz		
Fundamental	–0.7dB	4th Harmonic	–111.5dB
2nd Harmonic	–81.4dB	5th Harmonic	–97.0dB
3rd Harmonic	–89.4dB	6th Harmonic	–112.5dB

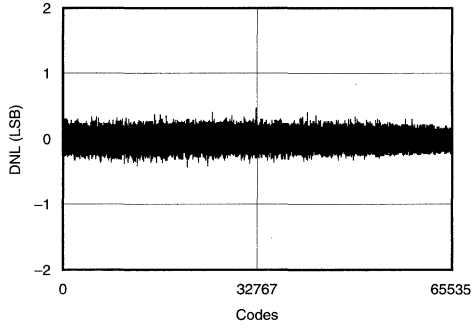
TWO-TONE INTERMODULATION RESPONSE, f_{IN} = 195kHz and 200kHz



Frequency 1	194.976806641 kHz		
Frequency 2	199.981689453 kHz		
f_1	–6.8dB	3 > f_1+2f_2	–96.0dB
f_2	–6.3dB	4 > $2f_1+f_2$	–96.8dB
1 > f_1+f_2	–87.7dB	5 > f_1-2f_2	–104.9dB
2 > f_1-f_2	–88.8dB	6 > $2f_1-f_2$	–109.0dB

NOTE: (1) For figures above, sampling rate = 500.0000000000kHz. 16,384 point FFT, non-windowed. Noise floor limited by synthesized generators.

DIFFERENTIAL NONLINEARITY OF ALL CODES, 19.6 MILLION SAMPLES



THEORY OF OPERATION

The ADC701 uses a three-step subranging architecture, meaning that the analog-to-digital conversion is performed in three passes which constitute coarse, medium and fine approximations of the input signal. Refer to Figures 1 and 2 for simplified block diagrams of the system.

Before the input signal is presented to the ADC, it must be sampled with high linearity and low aperture error by the sample/hold amplifier.

In the SHC702, the sampling switch is placed at the summing junction (virtual ground) of a high speed FET amplifier (Figure 1). This arrangement maintains constant charge injection independent of the signal amplitude, which is critically important for good linearity performance. The sampling switch itself is a high speed DMOS FET whose gate is driven from a fast-slewing control signal, thus minimizing the time aperture between the fully closed (sample mode) and the fully open (hold mode) states of the switch. The signal voltage is held across the feedback capacitor, forcing the op-amp to maintain a constant output voltage for the duration of the A/D conversion. Feedthrough from the input, already low due to the MOSFET's low capacitance, is further reduced by clamping the summing point to ground with another FET.

The ADC701 input voltage is converted to a current through the input scaling resistors (Figure 2), and this current is applied to the summing junction (virtual ground) of error amplifier A_1. The current output of the DAC (0 to 2mA) is also applied to the summing point. If bipolar operation is selected, the 10V reference output is applied to input D, creating a 1mA offset current which sums with the input current.

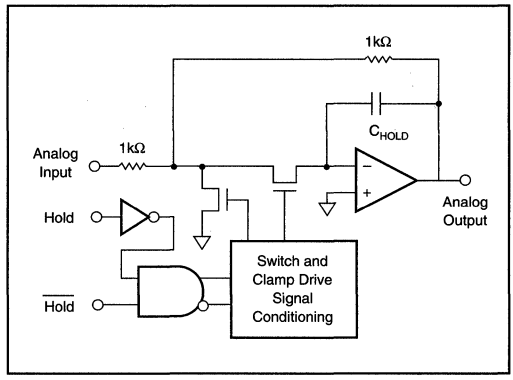


FIGURE 1. Simplified Block Diagram of the SHC702.

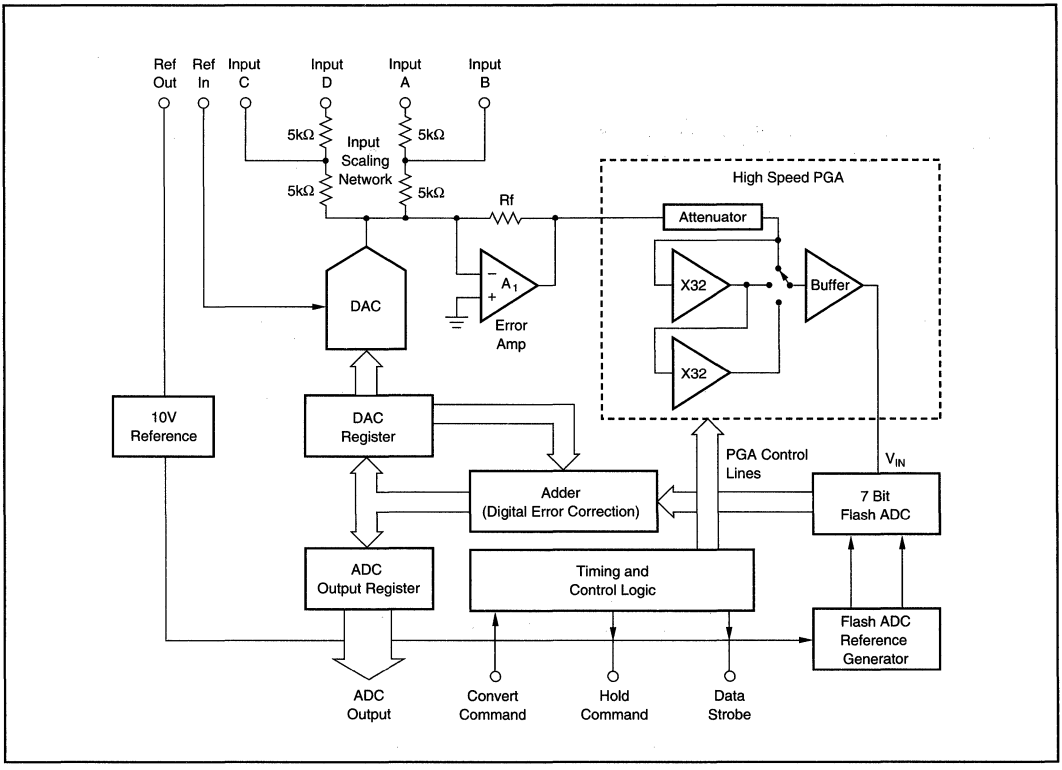


FIGURE 2. Simplified Block Diagram of the ADC701.

At the beginning of each conversion, the DAC is reset to mid-scale so that its output current is exactly 1mA. This 1mA is subtracted from the input signal current. The difference current flows through Rf and appears as an error voltage at the output of A_1.

During the first pass, the programmable gain amplifier (PGA) is set to unity gain, which matches the error voltage range to the input range of the flash ADC. The error signal is digitized to 7-bit resolution by the flash ADC, creating a coarse approximation of the digital output value, which is then applied to the DAC.

Since the DAC output is now approximately equal to the input signal current, the remaining difference current flowing through Rf is small—ideally less than 1/128 of full scale, which is due to the built-in quantizing uncertainty of the 7-bit flash ADC. However, other sources of error (e.g., integral and differential nonlinearity of the flash ADC, gain and offset of the PGA, settling and noise errors throughout the signal path) cause the possible error range to be significantly greater. In fact, the ADC701 is designed to handle remainder signals up to 1/32 of full scale, which is four times the "ideal" value.

Therefore, the PGA is set during the second pass to a gain of 32, allowing the small remainder signal to match the full range of the flash ADC. This is again digitized to 7-bit resolution and added to the previous result to create the "medium" approximation of the input signal. Because the full-scale range of the flash represents 1/32 of the input signal's full range, the 7-bit flash output is shifted right by 5 bits before being added to the original 7-bit "coarse" result, creating a 12-bit word. There is an overlap of two bits because the two least significant bits of the first-pass result correspond to the two most significant bits of the second-pass result. This overlap in the adder is called "digital error correction"—the mechanism that allows nonideal remainders from the first pass to be corrected in the second pass.

The 12-bit approximation is applied once again to the DAC, causing the remaining difference current to become yet smaller. For the third pass, the PGA's gain is increased by another factor of 32, and the remainder is again digitized by the flash ADC.

At this point in the conversion, all of the necessary data has been latched and it is no longer necessary to hold the analog signals from the sample/hold or the DAC. From a systems perspective, the conversion is now complete because the sample/hold is released to begin acquiring the next input sample and the DAC is reset to mid-scale for the next conversion. Meanwhile, the final result from the flash is added to the previous 12-bit result. Again there is a two-bit overlap to allow for error correction. The adder output is monitored to prevent a digital "rollover" condition, so that the ADC clips properly at the signal extremes. The upper sixteen bits of the final adder result are stored in the ADC's output register, ready to be presented in byte-sequential form at the eight output data lines. The overrange or "clip" condition can also be detected externally by monitoring pin 9. Refer to the section on ADC701 Digital I/O for further detail.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC701/SHC702 combination is designed to be easy to use in a wide variety of applications, without sacrificing flexibility of the analog and digital interface.

SHC702 INTERFACE

The connection diagram (Figure 3) shows the basic hookup. At the SHC702 input, the user may opt to connect the built-in FET buffer amplifier. The buffer is most useful in multi-channel applications where the signal bandwidth is less than 100kHz. In those applications, it serves to isolate the multiplexer output from the 1kΩ input impedance of the sample/hold. For higher frequency applications and for any system that does not require the very high impedance, the best results (lowest noise and distortion) will be achieved by driving the SHC702's analog input directly. If the buffer is not used, its input should be grounded to avoid random noise pickup and saturation of the buffer op amp.

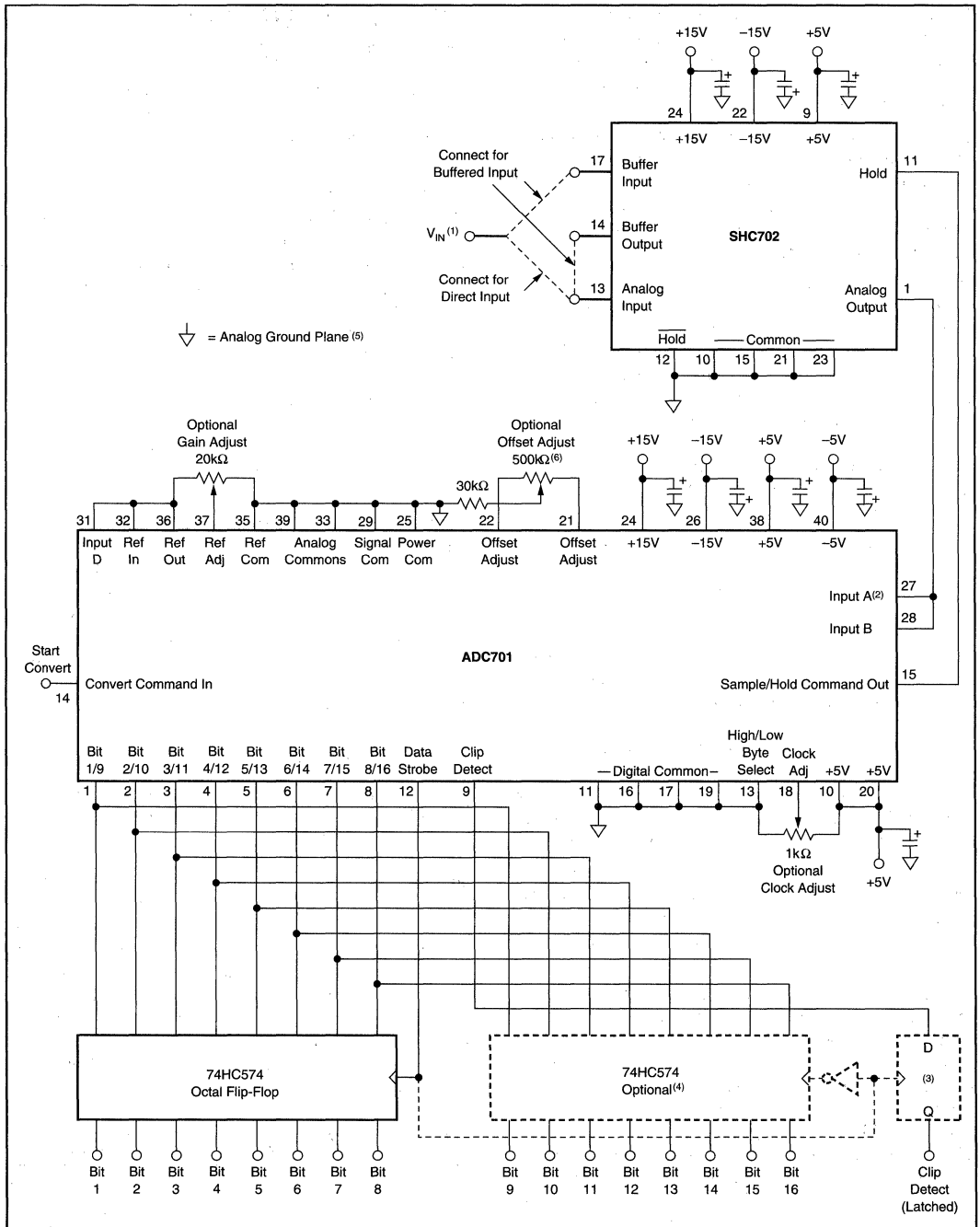
Only two connections are required between the SHC702 and the ADC701: SHC702 analog output to ADC701 input(s) and the digital Hold Command from the ADC701 to the SHC702. As always, it is best to avoid routing these analog and digital lines along parallel traces. Although the placement of the SHC702 relative to the ADC is not extremely critical, one good approach is to mount the SHC along one end of the ADC package as shown in Figure 4. This minimizes the length of the interconnections and keeps the digital lines well away from sensitive analog signals.

ADC701 INPUT CONNECTIONS

The ADC input network has four separate terminals, allowing many different input ranges. These should be connected as indicated in Table I. Most users will take advantage of the ADC701's built-in reference circuit, which has very low noise and excellent temperature stability. To use the internal reference, it is only necessary to connect pin 36 (Reference Output) to pin 32 (Reference Input). To use an external 10V reference (to cause the ADC gain to track a system reference, for example), pin 36 is left unconnected and the external reference is applied to pin 32. If required, the ADC701 will typically accommodate a five to ten percent variation in the 10V reference. External references should have very low noise to avoid degrading the excellent signal-to-noise ratio (SNR) of the ADC701.

INPUT RANGE	CONNECT V_{IN} TO	CONNECT Ref In TO
0 to +10V	Input A and Input D	—
±10V	Input A	Input D
±5V	Input A and Input B	Input D
−10V to 0	Input A and Input B	Input C and Input D
0 to +5V	Input B and Input C	—

TABLE I. ADC701 Input Connection Table.



NOTES: (1) For lowest distortion at high input frequencies the non-buffered option should be used. If the buffer is not used, its input should be grounded. (2) Shown connected for ±5V input range. Refer to Input Connection Table for other options. (3) If the Clip Detect feature is used, then the signal may be latched with a simple D type flip-flop as shown. See the section on ADC701 Digital I/O for additional applications information. (4) The second octal flip-flop is recommended but optional — it provides added digital signal isolation and buffering, and also permits three-state logic output compatibility. (5) All commons should be connected to the analog ground plane. Refer to the section on "Power and Ground Connections." (6) The Offset Adjust circuit shown provides an adjustment range of approximately ±0.25% FSR.

FIGURE 3. ADC701/SHC702 Connection Diagram.

OFFSET, GAIN AND CONVERSION SPEED ADJUSTMENTS (OPTIONAL)

Adjustment of the reference voltage is the most straightforward way to adjust the ADC gain. For the internal reference, this is accomplished by connecting a 20kΩ potentiometer as shown in Figure 3. This will provide a gain trim range of about ±3%. It is also possible to use external series or parallel resistance in the input network, but that is more cumbersome and usually will degrade the gain stability over temperature due to tempco (temperature coefficient) mismatches among the resistors.

ADC offset may be adjusted by connecting a 500kΩ potentiometer to pins 21 and 22, with the wiper connected through a series 30kΩ resistor to ground as shown in Figure 3. This will provide an offset trim range of approximately ±0.25% FSR. For a larger trim range of offset or gain, it is recommended that trims be accomplished elsewhere in the system.

The Clock Adjust input (pin 18) is intended primarily for small adjustments of the conversion time. However, this will rarely be necessary because the ADC701 is guaranteed to convert up to 512kHz over the specified temperature range without external clock adjustment.

POWER AND GROUND CONNECTIONS

Experience with testing and applying the ADC701 shows that it will perform well in most board layouts, provided that appropriate care is taken with grounding and bypassing.

Power supplies may be shared between the ADC701, SHC702 and other analog circuitry without difficulty. It is recommended that each power pin be locally bypassed to the ground plane with a high quality tantalum capacitor of at least 1µF. If at all possible, power should be derived from well-regulated linear supplies—switching power supplies will require much more effort for proper decoupling and are not recommended for this or any high performance wideband analog system.

The +5V Digital supply pins, though not as sensitive to noise as the +5V Analog pin, should nonetheless be kept as quiet as possible. If the system digital supply is noisy, then it is best to use the system +5V analog supply for all of the +5V connections on the ADC701 and SHC702 rather than trying to separate them. If only one +5V supply is available and it is shared with other system logic, then extra bypassing and/or supply filtering may be required.

The –5V supply will operate with any voltage between –4.75 and –6V. If –5V is not available from the system supplies, then an industry-standard 7905 regulator may be used to derive –5V from the –15V supply.

All ground pins on both the ADC701 and the SHC702 should be connected directly to a common ground plane. This is true for both analog and digital grounds. However, it is also helpful to recognize where the digital ground currents flow in the system, and to provide PC board return paths for potentially troublesome digital currents in addition to the ground plane connections. For example, the ADC701 output data lines will sink current (statically and/or dynamically) when in the low state. This current comes from the power supply that runs the interface logic, and so must return to that supply's ground. If the ground termination is placed such that this digital current will flow away from the ADC701, then the existing ground plane will suffice to carry the current. On the other hand, if the ground termination must be placed such that the digital current flows across the ADC or SHC layout, then it would be advisable to break the analog ground plane under the package (to stop the flow of current across the package) and to provide a separate trace (several centimeters wide) on another PC board layer to carry the digital return current from pins 11 and 19 to the termination point. If the ADC701 must interface into a fairly noisy digital environment, then another approach is to keep the first layer of latches and/or buffers connected to the ADC701 power and ground planes, so that the ADC itself is connected to "quiet" circuits with short return paths. This transfers the interface problem to the outputs of the latches, where it can be managed with less impact on the analog components.

PHYSICAL INSTALLATION

The packages may be soldered directly into a PC board or mounted in low-profile machined pin sockets with good results. Use of tall (long lead length) sockets, adapters or headers is not recommended unless a local ground plane and bypass capacitors can be mounted directly under the packages.

In a room-temperature environment or inside an enclosure with moderate airflow, the ADC701 and SHC702 normally do not require heat-sinking. However, to keep the devices running as cool as possible, it is helpful to install a thin heat-transfer plate under the packages to conduct heat into the ground plane. The plate may be made from metal (copper, aluminum or steel) or from a special heat-conductive material such as Sil-Pad[1]. The Sil-Pad material has the advantage of being electrically insulating and somewhat pliable, so that it will tend to distribute pressure evenly and conform to the package—an advantage in systems where the board may be flexed or subjected to vibration.

PC BOARD LAYOUT

An optimized layout has been designed for the DEM-ADC701-E demonstration fixture. For information concerning the demo board and the layout, contact your local sales representative.

ADC701 Digital I/O

Refer to the timing diagram, Figure 4. The conversion process is initiated by a rising edge on the Convert Command input. This will immediately bring the sample/hold command output to a logic high state (Hold mode).

After the ADC701 conversion is completed (approximately 1.5µs after the convert command edge), the Sample/Hold Command falls to a low state, enabling the sample/hold to begin acquisition of the next input sample. However, the ADC701 internal clock continues to run so that the output data may be processed.

There are two methods of reading data from the ADC:

1. Strobed Output—This will usually be the easiest and fastest method. The data are presented sequentially as high and low bytes of the total 16-bit word. The sequence High-Low or Low-High is controlled by the state of the High/Low Byte Select input. The first byte is valid on the rising edge of the Data Strobe output; the second byte is valid on the falling edge.
2. Polled output—With this method, data strobes will occur as described above, but they are ignored by the user. Instead, the user waits until the Data Strobe output falls, and then manually selects high and low output data by means of the High/Low Byte Select input. This polling procedure may be carried out during the subsequent ADC conversion cycle, but two precautions must be observed: First, the user should avoid switching the High/Low Byte Select immediately before or after the next convert command. This will prevent digital switching noise from coupling into the system at the instant of analog sampling. Second, the polling sequence must be completed before the ADC begins to strobe out data from the subsequent conversion.

OPTIONS FOR STROBED OUTPUT

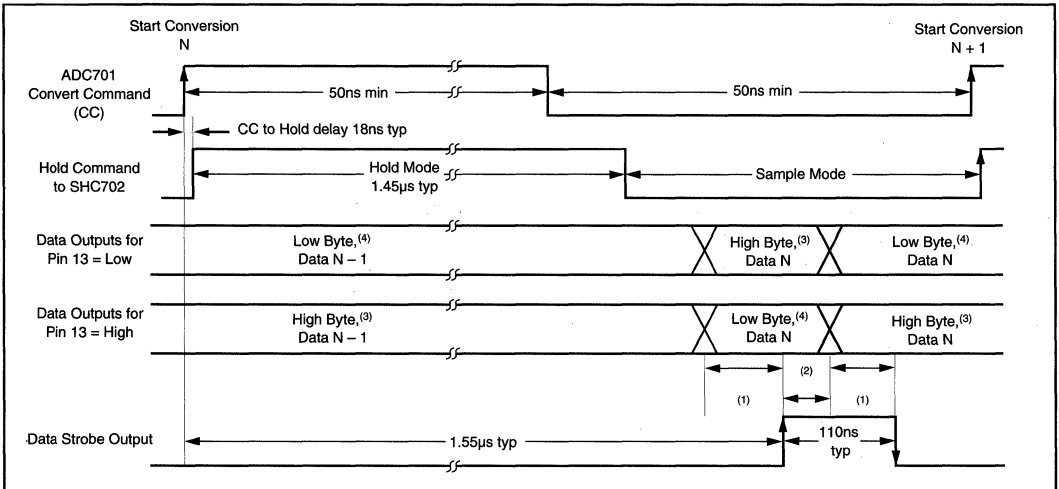
There are several ways in practice to implement the logic interface. Figure 3 shows the simplest configurations. In order to convert the ADC701's byte-sequential data into 16-bit parallel form, the minimum requirement is for one single octal flip-flop, such as a 74HC574 or equivalent. This will latch the first byte on the rising edge of the ADC701 Data Strobe. Then the second byte becomes valid, and all 16 bits may be strobed to the outside system on the falling edge of the Data Strobe.

For better noise isolation of the ADC701 from the digital system, or if full three-state capability is required for the 16 output lines, a second octal flip-flop can be added as shown in the dashed lines of Figure 3. This will also require an inverter to convert the falling Data Strobe edge into a rising clock edge for the second flip-flop IC.

If it is desirable to have all 16 output lines change simultaneously (for example when driving a D/A converter), then a third octal flip-flop (not shown in Figure 3) may be added to re-latch the output of the first byte. By driving that device's clock also from the inverted Data Strobe, fully synchronous switching of the 16 output bits will be achieved.

USING THE CLIP DETECT OUTPUT

The ADC701 provides a built-in Clip Detect signal on pin 9 which indicates an ADC overrange or underrange condition. The Clip Detect signal is only valid when the High Byte becomes valid as shown in Figure 4. Therefore, the simplest way to latch the Clip Detect signal is to provide an extra flip-flop which is clocked on the same strobe edge as the High Byte flip-flop. Such a setup is illustrated in Figure 3. The Clip Detect signal remains at logic 0 under normal conditions, and indicates a clip condition by rising to a logic 1.



NOTES: (1) Setup Time 28ns min, 37ns typ. (2) Hold Time 30ns min, 73ns typ. (3) High Byte refers to ADC bits 1 - 8, the most significant 8 bits. Also, the Clip Detect signal on pin 9 is valid simultaneously with High Byte. (4) Low Byte refers to ADC bits 9 - 16, the least significant bits.

FIGURE 4. ADC701 Interface Timing Diagram.

The latched version of Clip Detect may be used to generate an interrupt to the user's system computer, which would then launch a service routine to generate the appropriate alarms or corrective action. Another possible application would be to stretch the pulse using a monostable so that it would be easily visible when driving an LED warning lamp.

In some systems, it may be desirable to provide separate latched outputs for Underrange and Overrange. These conditions may be separately detected by using simple logic to implement the boolean equations:

$$\text{Underrange} = \text{Clip Detect AND } \overline{\text{Anybit}}$$

$$\text{Overrange} = \text{Clip Detect AND Anybit}$$

where "Anybit" is any one of the data output bits.

The Underrange and Overrange signals would then be latched into two separate flip-flops. A simple solution using a single '74 dual flip-flop and a single '00 quad NAND provides enough logic to implement the logic equations, with a spare NAND gate left over to use for creating the inverted Data Strobe signal.

USING THE ADC701 AT MAXIMUM CONVERSION RATES

The ADC701 is guaranteed to accept Convert commands at a rate of DC to 512kHz over the specified operating temperature range. At a conversion rate of 500kHz, the total throughput time of 2µs allows for the 1.5µs ADC conversion time plus 500ns for the digital output timing and sample/hold acquisition time.

If the user tries to exceed the maximum conversion rate by a large amount, the Convert Command of conversion N+1 will occur before the Data Strobe has fallen from conversion N. In such a situation, the ADC701 will simply ignore every other Convert command so the actual conversion rate will become half of the Convert command rate. Otherwise, the conversion will proceed normally. Note that the ADC timing slows down at high temperatures, so the frequency at which this occurs will vary with temperature—although it is still guaranteed to be greater than 512kHz over the specified temperature range.

Another consideration for operation at very high rates is that the sample/hold acquisition time becomes shorter as the conversion rate is increased. Users will note that the available acquisition time becomes less than 550ns at rates above 500kHz, which is less than the typical SHC702 acquisition time for a 10V step to 150µV accuracy. However, the signal degradation is gradual as the acquisition time is shortened—even at 512kHz, there is enough time to acquire a 5V step to better than 500µV. Also, most signal processing environments do not contain full-power signals at the Nyquist frequency, but rather show a rolloff of signal power at high frequencies. If the ability to acquire extremely large input changes at extremely high conversion rates is of paramount importance, the user may elect to use a Burr-Brown model SHC803 sample/hold instead—it is pin compatible with the SHC702 and provides much faster acquisition time at the expense of some extra noise and higher distortion at low input frequencies.

TESTING THE ADC701/SHC702

The ADC701 and SHC702 together form a very high performance converter system and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digital output is the best method of examining total system performance. Attempts to evaluate the system by analog reconstruction through a D/A converter will usually prove unsatisfactory; assuming that the static and dynamic distortions of the D/A can be brought below the required level (–110dB), the performance will still be beyond the range of presently available spectrum analyzers.

Even when the analysis is done using FFT techniques, several key issues must be addressed. First, the parameters of the FFT need to be adequate to perform the analysis and extract meaningful data. Second, the proper selection of test frequencies is critical for good results. Third, the limitations of commercial signal generators must be considered. These three points are addressed in later sections. Finally, the test board layout must follow the recommendations discussed on pages 8 through 10.

DYNAMIC PERFORMANCE DEFINITIONS

1. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to 3rd-order)}}{\text{Sinewave Signal Power}}$$

4. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}}$$

IMD is referred to the larger of the test signals f_1 or f_2—**not** to the total signal power, which would result in a number approximately 6dB "better." The zero frequency bin (DC) is not included in these calculations—it represents total offset of the ADC, SHC and test equipment and is of little importance in dynamic signal processing applications.

FFT Parameters

Accurate FFT analysis of 16-bit systems requires adequate computing hardware and software. The FFT length (number of points) should be relatively large—at least 4K and preferably 16K or larger. There are several reasons for this:

1. The converter itself has 64K codes. Ideally, the test would guarantee that all codes are tested at least once. Practically speaking, however, that would require immensely long FFTs (>>64K points) or averaging of a large number of smaller FFTs. By using an FFT length of 4K or greater and proper selection of the test frequencies, a very good statistical picture of the ADC performance will be obtained which shows the effect of any defects in the transfer function.
2. The noise floor of the output spectrum is not low enough if less than 4K points are taken. Shorter FFTs have fewer bins to cover the output spectrum, so a larger fraction of the total system noise appears in each bin. Although the SNR of the ADC701/SCH702 system is in the range of –93dB, the noise level of the available generators may increase the total measured noise power to –80dB. Every doubling of the FFT length will spread the noise power among twice as many bins, resulting in a 3dB reduction of the spectral noise floor. In order to resolve spurious components that are at the level of –110dB, an average noise floor of less than –113dB would be barely adequate. This requires at least 2048 bins in the output half-spectrum, corresponding to a 4K-point FFT. Even at this level, it will be difficult or impossible to separate higher order harmonics in the ADC701 response from the average noise level, indicating that longer FFTs are desirable.
3. Following the guidelines for test frequency selection which are outlined in the next section, it becomes clear that longer FFTs allow a much wider choice of test frequencies without concern for sophisticated data windowing or code coverage problems.

Besides the consideration of FFT length, it is important to realize that the FFT calculations must be performed with high-precision arithmetic. The use of 32-bit fixed or floating point calculations will generally be inadequate because the noise floor due to calculation errors alone will interfere with the ADC performance data. Unfortunately, this consideration precludes the use of most DSP accelerator boards and similar hardware. In order to preserve the full dynamic range of the ADC output, it is best to use standard 64- or 80-bit arithmetic. To avoid excessively long calculation times, the FFT algorithm should be written in an efficiently compiled language and make use of techniques such as trigonometric look-up tables in software and dedicated floating-point coprocessors in hardware. There are several commercial software packages available from Burr-Brown and others that meet these requirements.

SELECTION OF TEST FREQUENCIES

The FFT (and any similar DSP operation) treats the total time-domain record length as one cycle of an infinitely long periodic signal. Therefore, if the end of the sampled record does not match up smoothly with the beginning, the output spectrum will contain serious errors known as leakage or truncation error[2]. This well-known problem is usually handled by applying a windowing function to the time-domain samples, suppressing the worst effects of the mismatch. However, the most often used windows such as Hanning, Hamming, raised cosine, etc., are completely inadequate for 16-bit ADC testing. More sophisticated functions such as the four-sample Blackman-Harris window[3] will provide much better results, although there still will be obvious spreading of the spectral lines.

The most successful approach is to eliminate the need for windowing by properly selecting the test signal frequency (or frequencies) in relation to the ADC sampling frequency[4]. If the time sample contains exactly an integer number of cycles, then there is no mismatch or truncation error. Another point to consider is that the sampling frequency should not be an exact integer multiple of the signal frequency, which would tend to reduce the number of different ADC codes that are tested and also tend to artificially concentrate quantization error in the harmonics of the test signal.

Both of these criteria are met by choosing an FFT length which is a power of two (the most standard and fastest to compute) and choosing a test frequency which causes an exact **odd** integer number of cycles to appear in the time record. In software, this selection can be accomplished very easily:

1. Determine the desired sampling frequency f_S.
2. Determine the desired input signal frequency f_{APPROX}.
3. Determine the FFT length N, which should be a power of 2 (e.g., 4096 or 16384).
4. Divide f_{APPROX} by f_S, multiply the quotient by N, and round the result to the nearest odd integer. This is M, the number of cycles in the time record.
5. Multiply M by f_S and divide by N to obtain the exact input signal frequency f_{ACTUAL}.

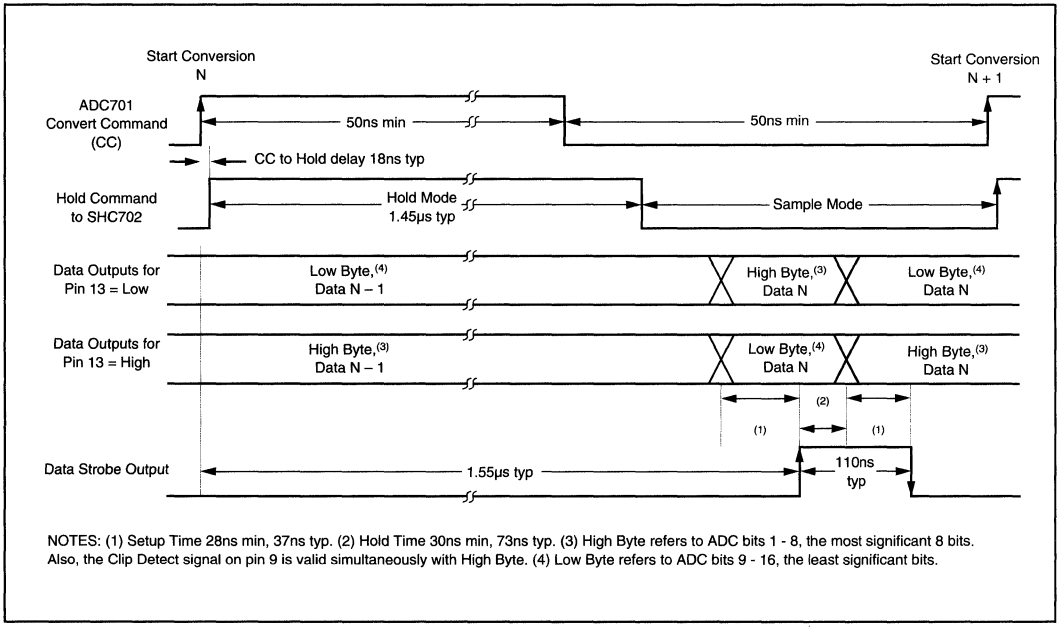
SIGNAL GENERATOR CONSIDERATIONS

To suppress leakage effects, the calculated ratio of f_S to f_{ACTUAL} must be precisely maintained during the test. This requirement is met easily by the use of synthesized signal generators whose reference oscillators can be locked together. Other possible approaches include external phase locking of non-synthesized generators and direct digital synthesis techniques. If it is not possible to use phase-locked signals, then a Blackman-Harris window may be used as mentioned previously.

Another key issue is the purity of both the signal and sampling frequency generators. The sampling clock's phase noise (jitter) will act as another source of SNR degradation. This is not serious as long as the jitter is random and the noise sidebands contain no sharp peaks. The HP3325 synthesizer is suitable for this purpose. The input signal generator will require more attention because its distortion will usually be greater than that of the ADC701/SHC702. Presently, the lowest distortion synthesized generator is the Brüel & Kjær Model 1051 (or 1049). This is suitable for testing the system in the audio range. The upper frequency limit of the B&K synthesizer is 200kHz. Above 20kHz, the distortion becomes a limiting factor, and low-pass filters must be inserted into the signal path to reduce the harmonic and spurious content.

As noted previously, the combined noise contributions of the signal generator and sampling clock generator far exceed the SNR of the ADC701/SHC702 itself. The SNR has been measured separately by applying a highly filtered sinewave to the input, resulting in typical SNR performance of –93dB. However, the filters employed to achieve this low-noise test stimulus are found to cause reactive loading of the signal source which results in increased distortion. Therefore it is best to separate the tests for SNR from those for THD and IMD, unless a suitably pure **and** low-noise signal can be generated.

Figures 5 and 6 show block diagrams of FFT test setups for the ADC701 and SHC702, summarizing the placement of the major components discussed above. The Typical Dynamic Performance section shows typical results obtained from testing the ADC701/SHC702 at a 500kHz conversion rate, using 16K samples for the FFT analysis.



NOTES: (1) Setup Time 28ns min, 37ns typ. (2) Hold Time 30ns min, 73ns typ. (3) High Byte refers to ADC bits 1 - 8, the most significant 8 bits. Also, the Clip Detect signal on pin 9 is valid simultaneously with High Byte. (4) Low Byte refers to ADC bits 9 - 16, the least significant bits.

FIGURE 5. FFT Test Configuration for Single-Tone Testing.

HISTOGRAM TESTING

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral nonlinearity of the SHC and ADC. The influence of differential linearity errors is harder to distinguish in a spectral plot—it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity (DL) performance is by using the popular histogram test method [5]. Application of the histogram test to the ADC701/SHC702 is relatively straightforward, though once again extra precision is required for a 16-bit system compared to 8- or 12-bit systems. Basically, this means that a very large number of samples are required to build an accurate statistical picture of each code width. If a histogram is taken using only one million points, then the average number of samples per code is less than fifteen. This is inadequate for good statistical confidence, and the resulting DL plot will look considerably worse than the actual performance of the converter. In practice 10 to 20 million samples will demonstrate good results for a 16-bit system and expose any serious flaws in the DL performance. If the memory incrementing hardware can keep pace with the ADC701, then 20 million samples can be accumulated in well under one minute. The last figure on page six shows the results of a 19.6 million point histogram taken at an input frequency of 1kHz.

NOTES:

1. Available from Bergquist, 5300 Edina Industrial Blvd., Minneapolis, MN 55435 (612) 835-2322.
2. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.
3. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
4. Halbert, Joel M. and Belcher, R. Allan, "Selection of Test Signals for DSP-Based Testing of Digital Audio Systems", Journal of the Audio Engineering Society, Vol. 34, No. 7/8, July/August, 1986, pp 546-555.
5. "Dynamic Tests for A/D Converter Performance", Application Bulletin AB-133, Burr-Brown Corporation, Tucson, AZ, 1985.

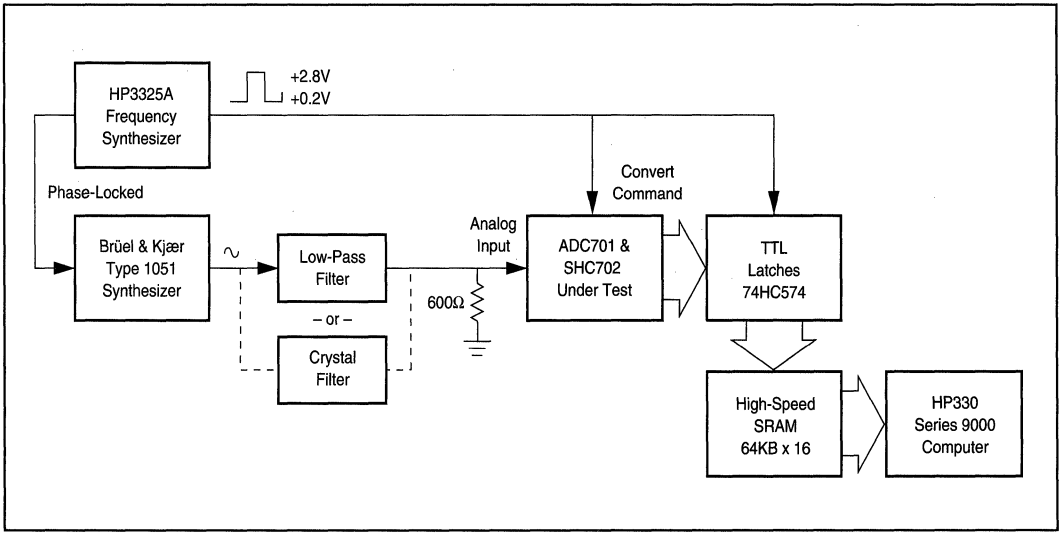
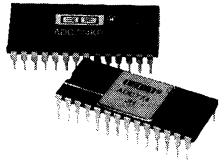


FIGURE 6. FFT Test Configuration for Two-Tone (Intermodulation) Testing.

BURR-BROWN®



ADC774

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10835

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, or 16-BIT MICROPROCESSOR BUS INTERFACE**
- **ALTERNATE SOURCE FOR HI774 A/D CONVERTER: 8.5µs Conversion Time, 150ns Bus Access Time**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  0°C to +75°C: ADC774J, K
  –55°C to +125°C: ADC774SH, TH

DESCRIPTION

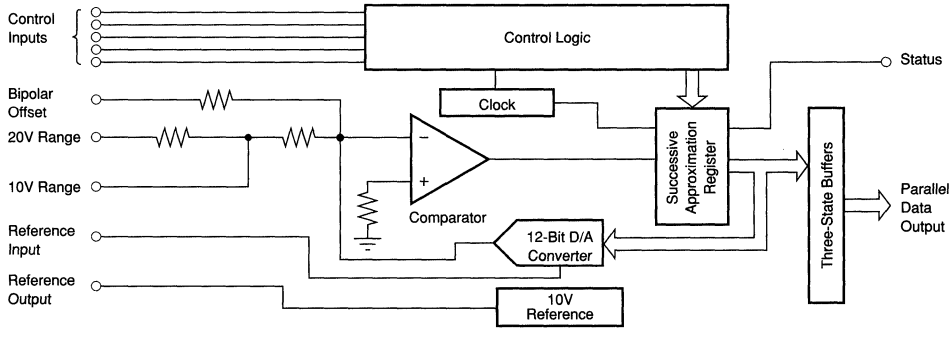
The ADC774 is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 8.5µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC774, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or a hermetic side-brazed ceramic DIP.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH MIN	ADC774J, ADC774SH TYP	ADC774J, ADC774SH MAX	ADC774K, ADC774TH MIN	ADC774K, ADC774TH TYP	ADC774K, ADC774TH MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	3.75	5	6.25	*	*	*	kΩ
±10V, 0V to +20V	7.5	10	12.5	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	*		*	V
Logic 0	–0.5		+0.8	*		*	V
Current	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			*	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(Adjustable to Zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1] : J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} <+16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
–16.5V < V_{EE} <–13.5V or –12.6V < V_{EE} < –11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} <+5.5V			±1/2			*	LSB
CONVERSION TIME [4,5]							
8-Bit Cycle		5	5.3		*	*	µs
12-Bit Cycle		7.5	8.5		*	*	µs
OUTPUTS							
DIGITAL (DB11 – DB0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

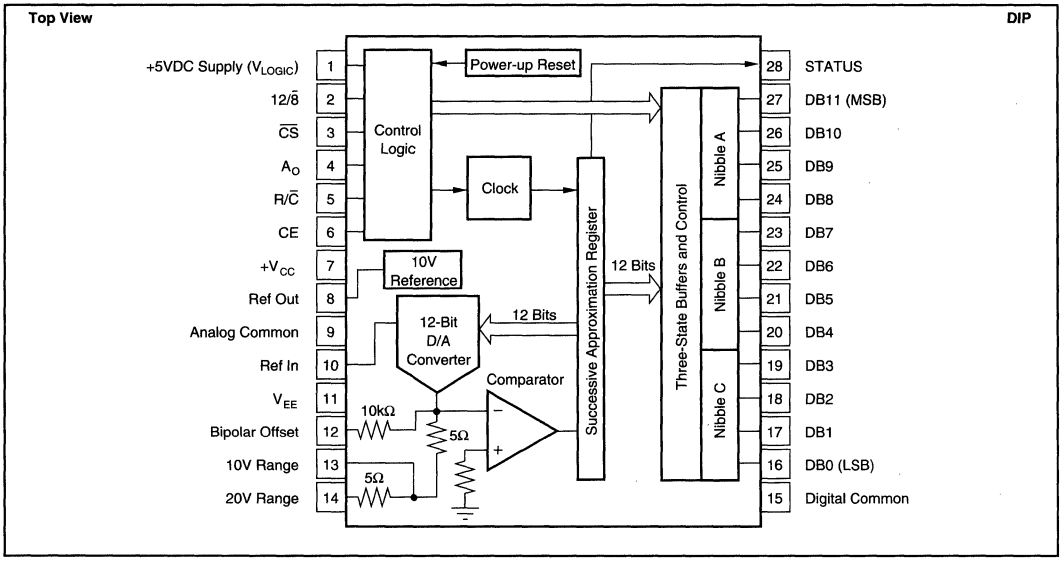
PARAMETER	ADC774J, ADC774SH			ADC774K, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INTERNAL REFERENCE VOLRAGE							
Voltage	+9.9	+10	+10.1	*	*	*	V
Source Current Available for External Loads (6)	2.0			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN} , T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as ADC774JH, JP, SH.

NOTES: (1) With fixed 50Ω resistor from Ref Out to Ref In. This parameter is also adjustable to zero at +25C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range FS means 20V; for a 0V to +10V range, FS means 10V. The term Full Scale for these specification instead of Full-Scale Range is used to be consistent with other vendors' specifications tables. (3) Using internal reference. (4) See "Controlling the ADC774" section for detailed information concerning digital timing. (5) The Harris HI-774 uses a subranging/error correction technique that allows one to begin conversion before a preceding sample-hold or multiplexer has settled to ±1/2LSB. For 12-bit accurate conversions, the input transient to the ADC774 must settle to less than ±1/2LSB before conversion is started. The ADC774 is compatible with HI-774 in all other respects. (6) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION

Top View **DIP**



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common	0V to +16.5V
V_{EE} to Digital Common	0V to −16.5V
V_{LOGIC} Digital Common	0V to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	−0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering,10s)	+300°C
Thermal Resistance, θ_{JA} : Ceramic	50°C/W
Plastic	100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADC774JP	28-Pin Plastic DIP	215
ADC774KP	28-Pin Plastic DIP	215
ADC774JH	28-Pin Ceramic DIP	149
ADC774KH	28-Pin Ceramic DIP	149
ADC774SH	28-Pin Ceramic DIP	149
ADC774TH	28-Pin Ceramic DIP	149
ADC774JP-BI	28-Pin Plastic DIP	215
ADC774KP-BI	28-Pin Plastic DIP	215
ADC774JH-BI	28-Pin Ceramic DIP	149
ADC774KH-BI	28-Pin Ceramic DIP	149
ADC774SH-BI	28-Pin Ceramic DIP	149
ADC774TH-BI	28-Pin Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})
ADC774JP	Plastic DIP	0°C TO +75°C	±1LSB
ADC774KP	Plastic DIP	0°C to +75°C	±1/2LSB
ADC774JH	Ceramic DIP	0°C to +75°C	±1LSB
ADC774KH	Ceramic DIP	0°C to +75°C	±1/2LSB
ADC774SH	Ceramic DIP	−55°C to +125°C	±1LSB
ADC774TH	Ceramic DIP	−55°C to +125°C	±3/4LSB

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMP (160 HOURS)[1]
ADC774JP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC774KP-BI	Plastic DIP	0°C to +75°C	+85°C
ADC774JH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC774KH-BI	Ceramic DIP	0°C to +75°C	+125°C
ADC774SH-BI	Ceramic DIP	−55°C to +125°C	+125°C
ADC774TH-BI	Ceramic DIP	−55°C to +125°C	+125°C

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC774s. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g. ADC774KP-BI). See Ordering Information for pricing.

CONTROLLING THE ADC774

This is an abridged data sheet. For Discussion of Specifications, Installation, Calibration refer to ADC574A data sheet or order PDS-835.

The Burr-Brown ADC774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL-/CMOS-compatible. The functions of the control inputs are described in Table I. The control function truth table is listed in Table II.

Read footnote 5 to the Electrical Specifications table if using ADC774 to replace the HI-774.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

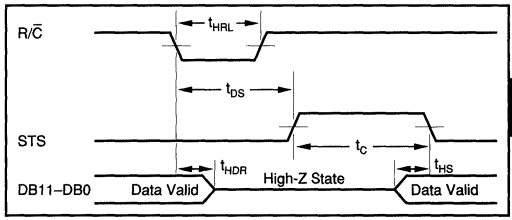


FIGURE 1. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

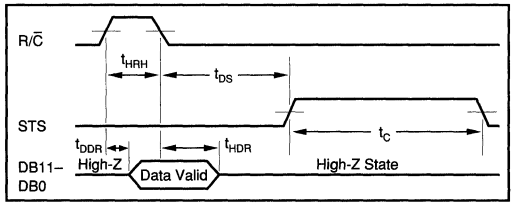


FIGURE 2. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE I. ADC774 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. Control Input Truth Table.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid		150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE III. Stand-Alone Mode Timing.

Figure 1 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 2 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table III.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3 LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

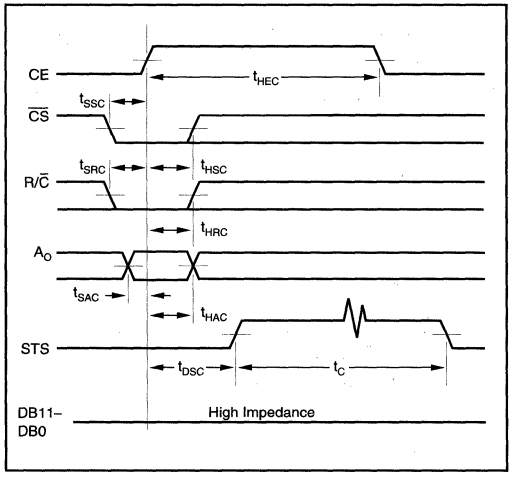


FIGURE 3. Conversion Cycle Timing.

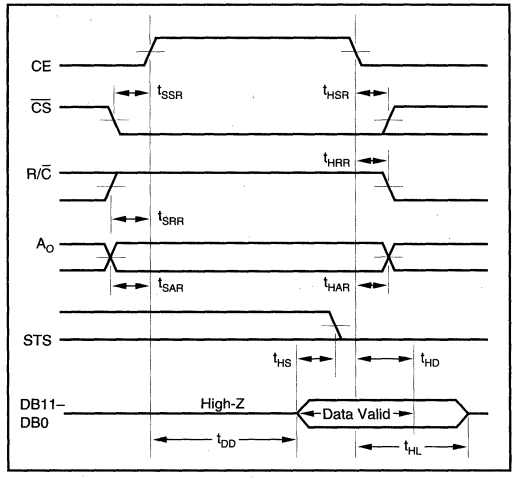


FIGURE 4. Read Cycle Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time				
	12-bit cycle at 25°C		7.5	8.5	µs
	0 to +75°C			9.0	µs
	–55°C to +125°C			9.5	µs
	8-bit cycle at 25°C		5	5.3	µs
	0 to +75°C			5.6	µs
	–55° to +125°C			6	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid		150	375	ns

TABLE IV. Timing Specifications.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occurring on any of three logic inputs ($\overline{CE}$, CS, and R/$\overline{C}$) as shown in Table II. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 3. The specifications for timing are contained in Table IV.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 4 and Table IV for timing relation

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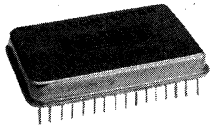


ADC803

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10493

High Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **12-BIT RESOLUTION**
- **LINEARITY ERROR: ±0.12%, max (C Grade)**
- **NO MISSING CODES: –55°C to +125°C (S Grade)**
- **HIGH SINAD RATIO: 72dB**
- **LOW HARMONIC DISTORTION: –73dB**
- **CONVERSION TIME: 500ns, 8 Bits**
  670ns, 10 Bits
  1.5µs, 12 Bits

DESCRIPTION

The ADC803 is a high speed hybrid successive approximation analog-to-digital converter utilizing laser-trimmed thin film components.

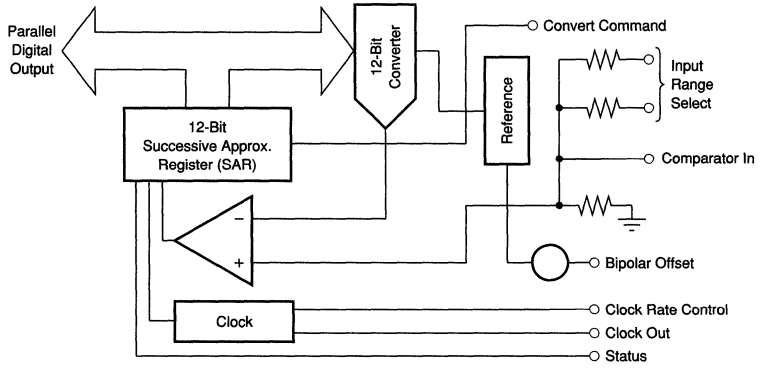
It is complete with internal reference, clock, and comparator, and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5µs.

With user-adjusted conversion time set at 1µs, ±1LSB accuracy can be achieved. The gain and offset errors may be externally trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to –10V, ±5V, and ±10V.

Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At +25°C, rated power supplies, 1.5µs conversion time, and after 6-minute warm-up, unless otherwise noted.

PARAMETER	ADC803CM MIN	ADC803CM TYP	ADC803CM MAX	ADC803BM MIN	ADC803BM TYP	ADC803BM MAX	ADC803SM MIN	ADC803SM TYP	ADC803SM MAX	UNITS
RESOLUTION			12			12			12	Bits
INPUTS										
ANALOG										
Voltage Ranges: Bipolar		±5, ±10			*			*		V
Unipolar		0 to –10			*			*		V
Impedance: –10V to 0V, ±5V		1.4			*			*		kΩ
±10V		2.4			*			*		kΩ
DIGITAL										
Convert Command		Negative pulse 50ns wide (min) trailing edge (0 to 1) initiates conversion.								
Logic Loading			4			*			*	TTL Loads
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error [1]		±0.04	±0.1		±0.08	±0.2		±0.04	±0.1	%
Offset Error[1]: Unipolar		±0.05	±0.2		±0.07	±0.3		*	*	% of FSR[2]
Bipolar		±0.02	±0.1		*	±0.2		*	*	% of FSR
Linearity Error:										
1.5µs Conversion Time		±0.009	±0.012			±0.020		±0.012	±0.015	% of FSR
1.0µs Conversion Time		±0.015	±0.020		±0.020					% of FSR
Differential Linearity Error:										
1.5µs Conversion Time		±0.012	±0.015			±0.020		*	*	% of FSR
1.0µs Conversion Time			±0.024		±0.024			*		% of FSR
Inherent Quantization Error		1/2			*			*		LSB
POWER SUPPLY SENSITIVITY										
Gain and Offset: +15VDC		±0.0036			*			*		% of FSR/%V_{CC}
–15VDC		±0.0005			*			*		% of FSR/%V_{CC}
+5VDC		±0.001			*			*		% of FSR/%V_{DD}
Conversion Time: +15VDC		±0.7			*			*		%/%V_{CC}
–15VDC		None			*			*		%/%V_{CC}
+5VDC		±0.8			*			*		%/%V_{DD}
CONVERSION TIME										
Factory Set	1.3		1.5	*		*	*		*	µs
Range of Adjustments	0.8		2.2	*		*	*		*	µs
DRIFT										
Gain		±10	±30		±15	*		*	*	ppm of FSR/°C
Offset: Unipolar		±2	±7		±3	*		*	*	ppm of FSR/°C
Bipolar		±3	±10		±5	*		*	*	ppm of FSR/°C
Linearity Error										
–25°C to +85°C:										
1.5µs Conversion Time		±0.012	±0.018			±0.024			*	% of FSR
1.0µs Conversion Time		±0.015			±0.020				*	% of FSR
–55°C to +125°C:										
1.7µs Conversion Time, max[4]								±0.015	±0.024	% of FSR
Differential Linearity Error										
–25°C to +85°C:										
1.5µs Conversion Time		±0.012	±0.018			±0.024				% of FSR
1.0µs Conversion Time		±0.015			±0.024					% of FSR
–55°C to +125°C:										
1.7µs Conversion Time, max[4]		±0.1						±0.015	±0.024	% of FSR
Conversion Time					*			*		% of FSR
No Missing Code Temp. Range:										
1.5µs Conversion Time	–25		+85	*		*				°C
1.7µs Conversion Time, max[4]							–55		+125	°C
OUTPUT										
DIGITAL DATA										
Parallel										
Output Codes: Unipolar		Complementary Straight Binary			*			*		
Bipolar		Bipolar Offset Binary			*			*		
Output Drive	6			*			*			TTL Loads
Status		Logic "1" During Conversion			*			*		
Status Output Drive	6			*			*			TTL Loads
Internal Clock										
Clock Output Drive	3			*			*			TTL Loads
Frequency (without external clock adj.)		8			*			*		MHz

SPECIFICATIONS (CONT)

At +25°C, rated power supplies, 1.5µs conversion time, and after 6-minute warm-up, unless otherwise noted.

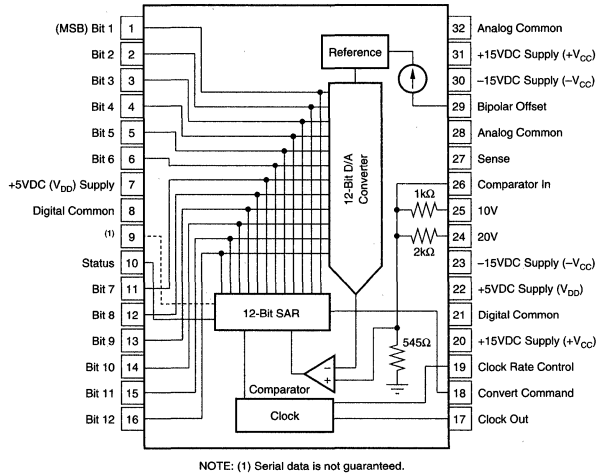
PARAMETER	ADC803CM			ADC803BM			ADC803SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS										
Power Consumption										
Rated Voltage: Analog ($\pm V_{CC}$)	±14.25	±15	±15.75	*	*	*	*	*	*	VDC
Digital (V_{DD})	+4.75	+5	+5.25	*	*	*	*	*	*	VDC
Supply Drain: +15V		+27	+32		*	*		*	*	mA
−15V		−38	−55		*	*		*	*	mA
+5V		+180	+210		*	*		*	*	mA
TEMPERATURE RANGE (Ambient)										
Specification	−25		+85	*		*	−55		+125	°C
Storage	−55		+125	*		*	*		*	°C

* Same specification as for ADC803CM.

NOTES: (1) Adjustable to zero. See Optional Gain and Offset Adjustment section. (2) FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR. (3) See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle. (4) Conversion time is factory-set at approximately 1.4µs at +25°C. As temperature increases, the conversion time increases. At +125°C the conversion time will be no more than 1.7µs. No Missing Codes is guaranteed over −55°C to +125°C provided the conversion time is allowed to increase with temperature.

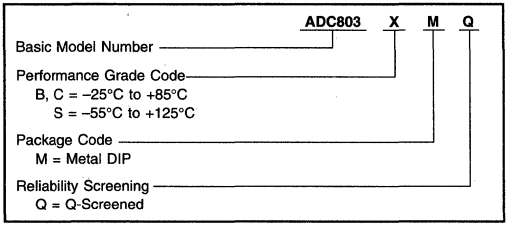
ADC803 dynamic performance characteristics are described in a report titled "Analogue-to-Digital Converter Performance Tests Using the Fast Fourier Transform" by R. A. Belcher, University College of Swansea, Wales, UK. (available from Burr-Brown on letterhead request).

CONNECTION DIAGRAM



NOTE: (1) Serial data is not guaranteed.

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage To Analog Common	±18V
Digital Supply Voltage To Digital Common	+7V
Digital Controls Inputs	+5.5V
Analog Inputs	±15V
Operating Temperature: Ambient	+125°C
Case	+135°C
Storage Temperature	+125°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC803	32-Pin Metal	116

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR - BROWN®

ADC7802

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

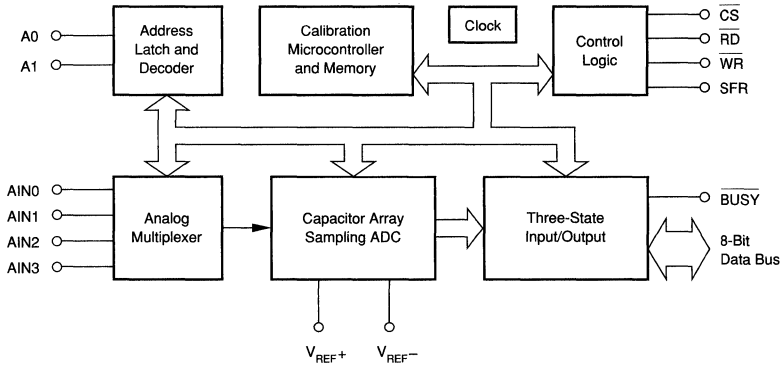
FEATURES

- TOTAL UNADJUSTED ERROR ≤ 1/2LSB OVER FULL TEMPERATURE RANGE
- FOUR-CHANNEL INPUT MULTIPLEXER
- LOW POWER: 10mW plus Power Down Mode
- SINGLE SUPPLY: +5V
- FAST CONVERSION TIME: 8.5µs Including Acquisition
- AUTOCAL: No Offset or Gain Adjust Required
- UNIPOLAR INPUTS: 0V to 5V
- MICROPROCESSOR-COMPATIBLE INTERFACE
- INTERNAL SAMPLE/HOLD

DESCRIPTION

The ADC7802 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. An autocalibration cycle, occurring automatically at power on, guarantees a total unadjusted error within ±1/2LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part very easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADC7802 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



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SPECIFICATIONS

ELECTRICAL

At $V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_A \geq V_D \geq V_{REF}+$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external with 50% duty cycle, $T_A = -40°C$ to $+85°C$, after calibration cycle at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADC7802BP, ADC7802BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = 25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \leq V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance: [1] $V_{REF}+$		4.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	µA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz, 50% Duty Cycle			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz, 50% Duty Cycle			17	µs
	CLK = 500kHz, 50% Duty Cycle			34	µs
With Internal Clock Using	$T_A = +25°C$			10	µs
Recommended Clock Components	$T_A = -40°C$ to $+85°C$		10		µs
Analog Signal Bandwidth [2]			500		Hz
Slew Rate [2]		8			mV/µs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
ACCURACY					
Total Adjusted Error,[3] All Channels				±1/2	LSB
Differential Nonlinearity				±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels			±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	µA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	µA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	µA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA
DIGITAL OUTPUTS					
V_{OL}	$I_{SINK} = 1.6mA$			0.4	V
V_{OH}	$I_{SOURCE} = 200µA$	4			V
Leakage Current	High-Z State, $V_{OUT} = 0V$ to V_D			±1	µA
Output Capacitance	High-Z State	4		15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III, Page 9		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 4.5V, the total error will typically not exceed ±1LSB. (2) Faster signals can be accurately converted by using an external sample/hold in front of the ADC7802. (3) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground	6.5V
V_D to Digital Ground	6.5V
Pin V_A to Pin V_D	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	–0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground	–0.3V to V_D + 0.3V
Maximum Junction Temperature	150°C
Internal Power Dissipation	875mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	75°C/W
PLCC	75°C/W

ORDERING INFORMATION

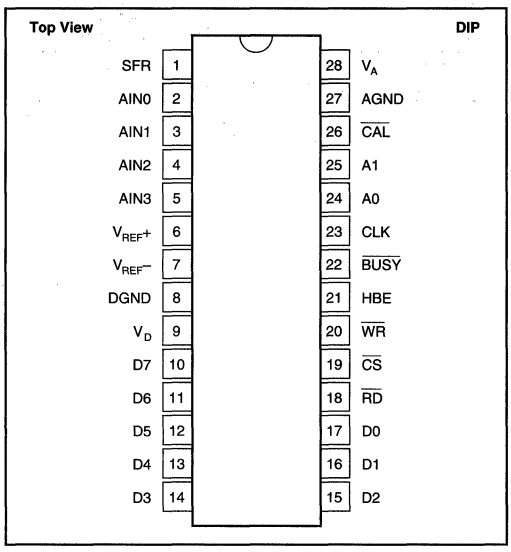
MODEL	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE, °C	PACKAGE
ADC7802BN	±1/2	–40 to +85	PLCC
ADC7802BP	±1/2	–40 to +85	Plastic DIP

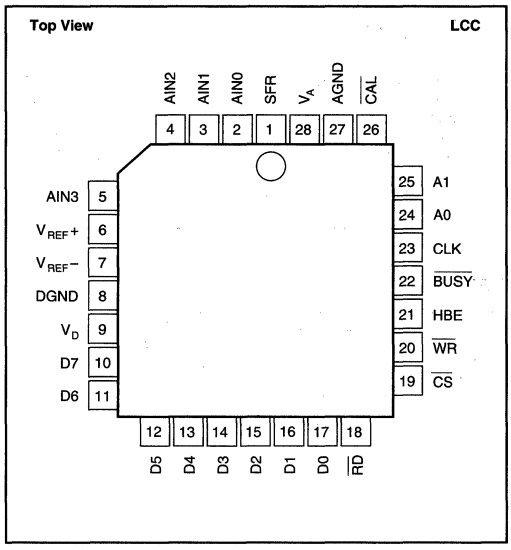
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC7802BN	28-Pin PLCC	251
ADC7802BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATIONS





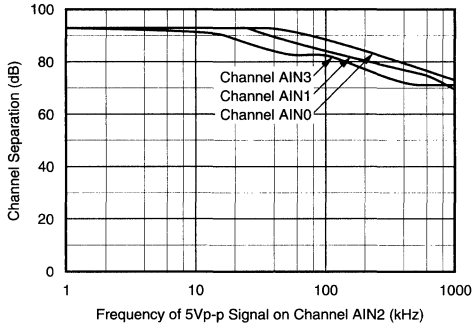
PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	V_{REF}+	Positive voltage reference input. Normally +5V. Must be ≤ V_A.
7	V_{REF}−	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be ≤ V_A and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$.)
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal/external clock operation. For external clock operation, connect pin 23 to a 74 HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 / A0 / Selected Channel LOW / LOW / AIN0 LOW / HIGH / AIN1 HIGH / LOW / AIN2 HIGH / HIGH / AIN3
26	$\overline{CAL}$	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be ≥ V_D and V_{REF}+.

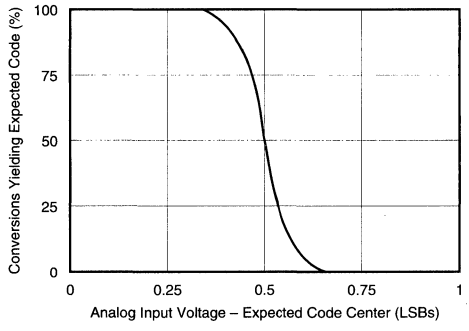
TYPICAL PERFORMANCE CURVES

At $V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, unless otherwise specified.

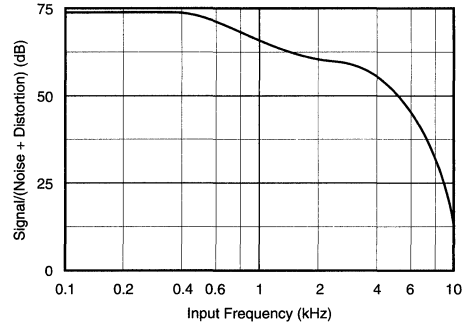
CHANNEL SEPARATION vs FREQUENCY



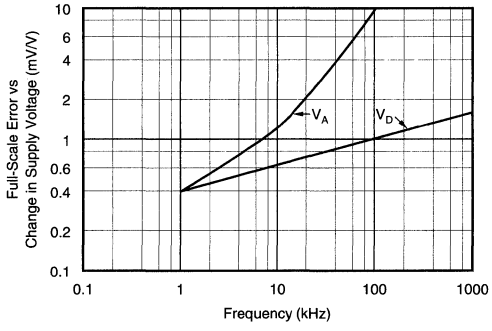
CODE TRANSITION NOISE



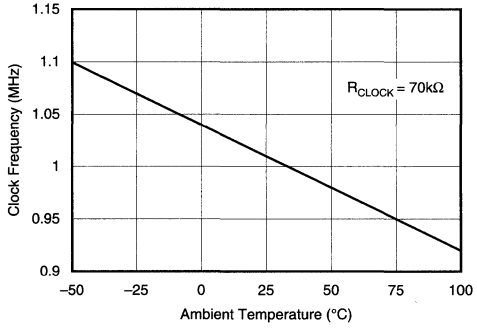
SIGNAL/(NOISE + DISTORTION)
vs INPUT FREQUENCY



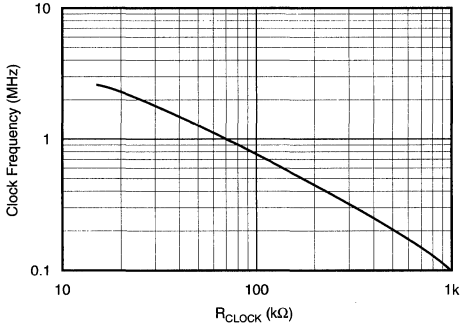
POWER SUPPLY REJECTION vs FREQUENCY



INTERNAL CLOCK FREQUENCY
vs TEMPERATURE



INTERNAL CLOCK FREQUENCY
vs R_{CLOCK}



THEORY OF OPERATION

ADC7802 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator. This allows offset errors to be corrected during the acquisition phase of each conversion cycle.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by a microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. This is faster than a complex digital error correction system, which could slow down the throughput rate. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADC7802 to most micro-controllers, microprocessors or digital storage systems.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADC7802 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles, during which the comparator offset is also auto-zeroed to below 1/4LSB of error. The successive approximation conversion takes place during clock cycles 6 through 17.

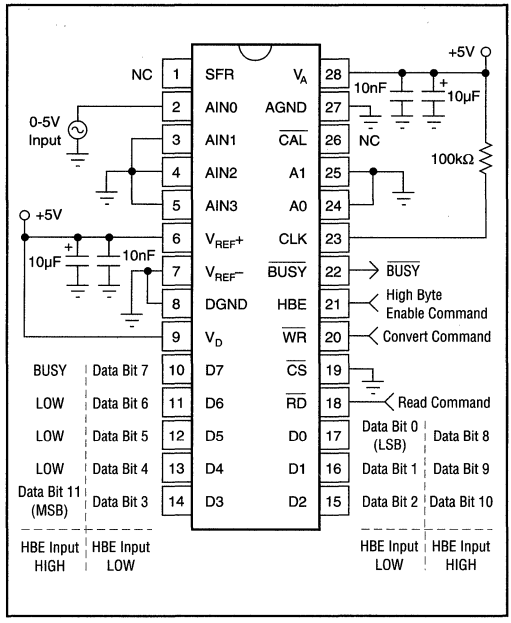


FIGURE 1. Basic Operation.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages and reference voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

READING DATA

Data from the ADC7802 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADC7802 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

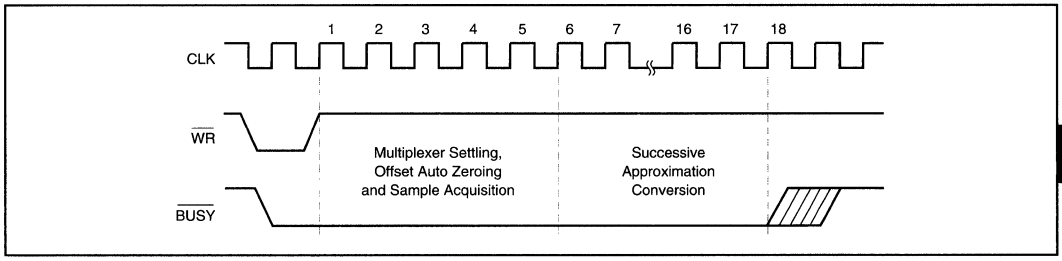


FIGURE 2. Converter Timing.

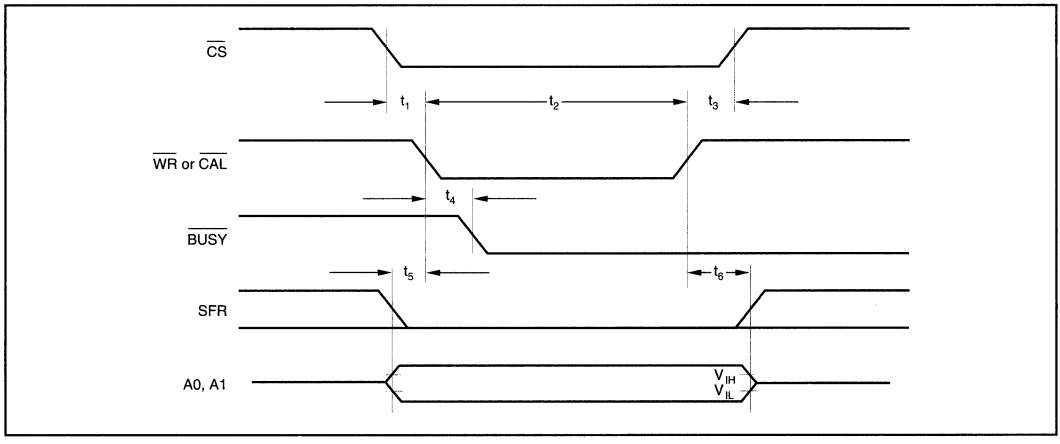


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

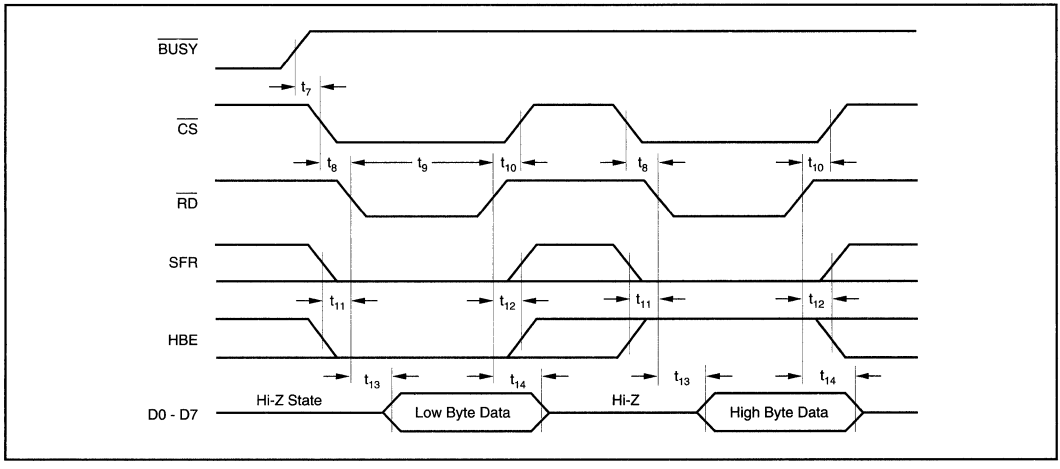


FIGURE 4. Read Cycle Timing.

TRANSPARENT MODE

This is the default mode for ADC7802. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 and LOWs to D1 to D7 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 8 show the digital timing of ADC7802 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADC7802, or to write additional instructions to the converter. Access to the Special Function Register is made by driving SFR HIGH.

SYMBOL	PARAMETER [1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time [2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time [2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time [2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time [2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time) [3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time) [3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR [3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL} = 20ns$ (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal $\overline{WR}$ pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 7 and 8 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 1MHz external, T_A = –40°C to +85°C).

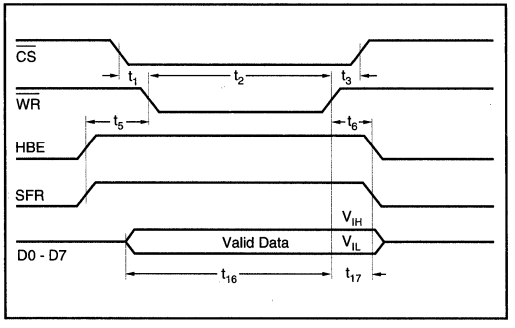


FIGURE 5. Writing to the SFR.

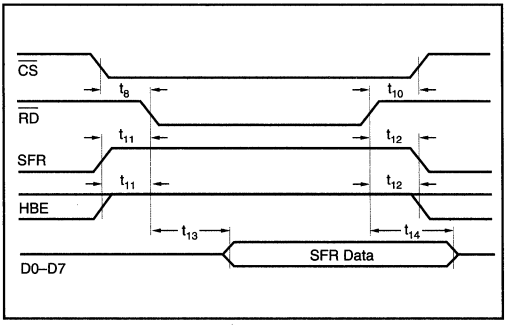


FIGURE 6. Reading the SFR.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH as shown in Figure 4.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADC7802 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, Latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2		Reserved for factory use.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occured during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

Writing a HIGH to D3 in the FSR puts the ADC7802 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) The timing is shown in Figure 3. Note that writing to the SFR also initiates a new conversion.

CONTROL LINES

Table IV shows the functions of the various control lines on the ADC7802. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

	$\overline{CS}/\overline{WR}$	SFR/HBE	D0	D1	D3	D5	D7	D2/D4/D6
Enables Transparent Mode for Data Latches.	LOW	HIGH	LOW	X	LOW	X	LOW	LOW
Enables Latched Output Mode for Data Latches.	LOW	HIGH	HIGH	X	LOW	X	LOW	LOW
Initiates Calibration Cycle.	LOW	HIGH	X	HIGH	LOW	X	LOW	LOW
Resets Power Fail flag.	LOW	HIGH	X	X	LOW	LOW	LOW	LOW
Activates Power Down Mode	LOW	HIGH	X	X	HIGH	X	LOW	LOW

NOTES: (1) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down. (2) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D2, D3, D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle.
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

INSTALLATION

INPUT BANDWIDTH

From the typical performance curves, it is clear that ADC7802 can accurately digitize signals up to 500Hz, but distortion will increase beyond this point. Input signals slewing faster than 8mV/µs can degrade accuracy. This is a result of the high-precision auto-zeroing circuit used during the acquisition phase. For applications requiring higher signal bandwidth, any good external sample/hold, like the SHC5320, can be used.

INPUT IMPEDANCE

ADC7802 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

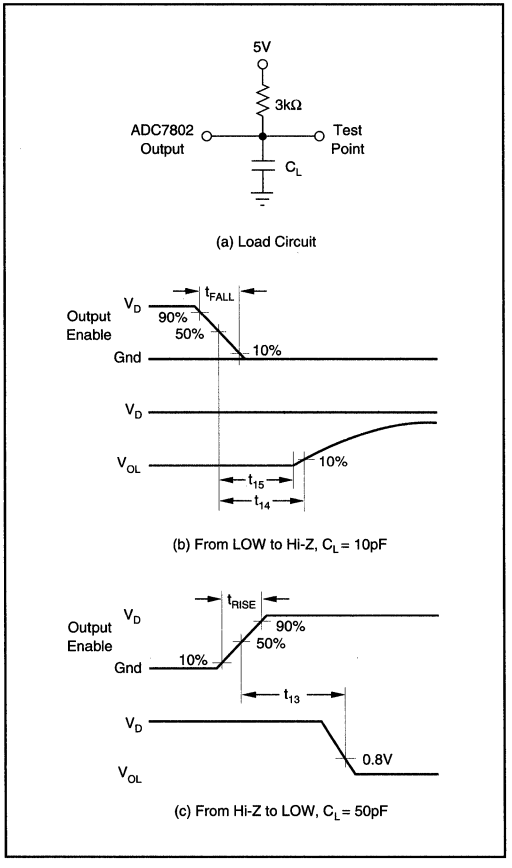


FIGURE 7. Measuring Active LOW to/from Hi-Z State.

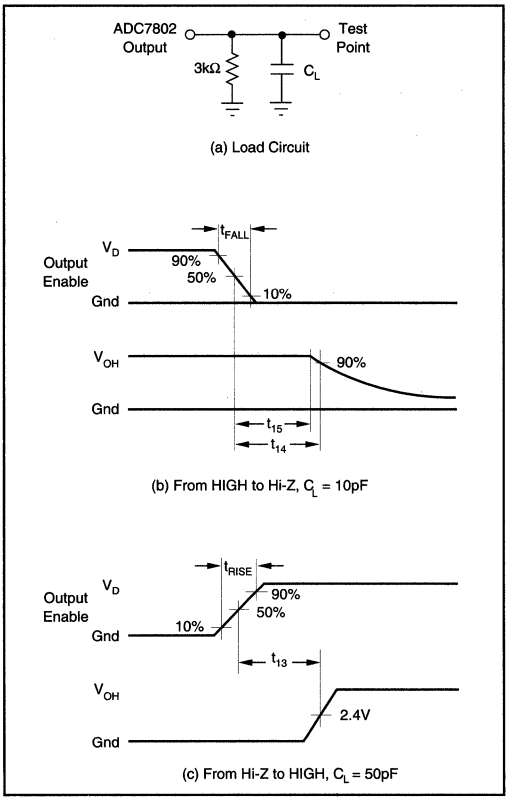


FIGURE 8. Measuring Active HIGH to/from Hi-Z State.

In many applications, a simple passive low-pass filter as shown in Figure 9a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 9a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 9b should be used.

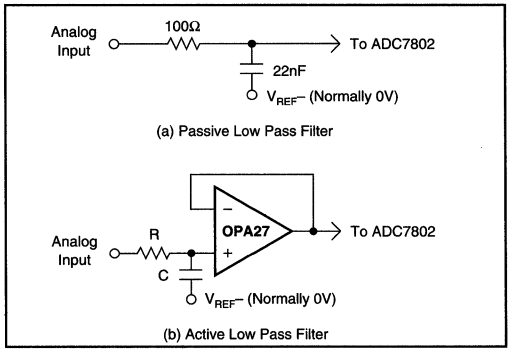


FIGURE 9. Input Signal Conditioning.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADC7802, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADC7802 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 2.5V and $V_{REF}-$ as high as 1V. As long as there is at least a 2.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB. (1/2LSB for a 5V span is 610µV, which is 1LSB for a 2.5V span.)

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADC7802 should be bypassed with 10µF tantalum capacitors as close to the part as possible. Although ADC7802 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 10 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADC7802 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADC7802, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The $V_{REF}-$ pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADC7802 clock from an external source is shown in Figure 11a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The minimum pulse width of the external clock must be 200ns. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.2MHz.

INTERNAL CLOCK OPERATION

Figure 11b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

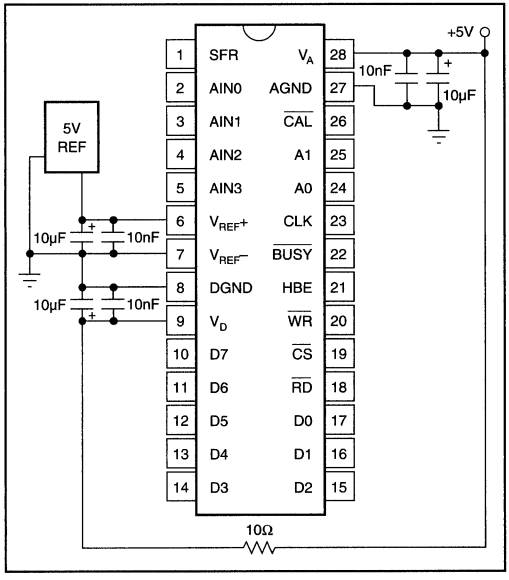


FIGURE 10. Power Supply and Reference Decoupling.

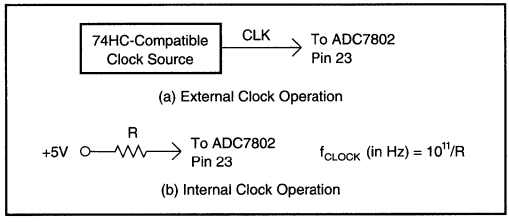


FIGURE 11. Internal Clock Operation.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in many applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 12 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802, using a precision, low-cost complete difference amplifier, INA105.

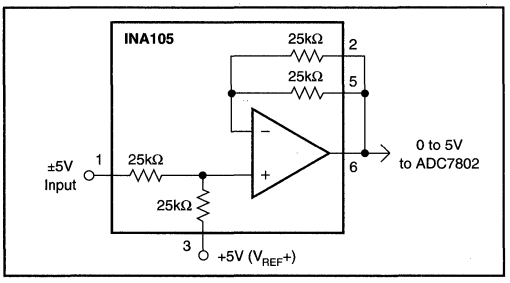


FIGURE 12. ±5V Input Range.

Figure 13 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802. The precision of this circuit will depend on the matching and tracking of the three resistors used.

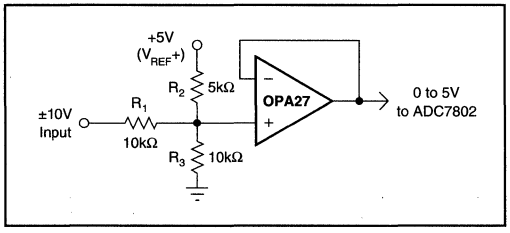


FIGURE 13. ±10V Input Range.

To trim this circuit for full 12-bit precision, R_2 and R_3 need to be adjustable over appropriate ranges. To trim, first have the ADC7802 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R_3 until the ADC7802 output toggles between the codes FFE hex and FFF hex. This makes R_3 extremely close to R_1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R_2 until the ADC7802 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADC7802, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 14 shows a typical interface to Motorola microprocessors, while Figure 15 shows how the result can be placed in register D0.

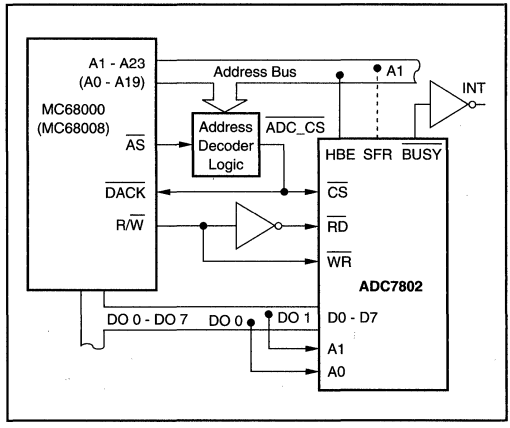


FIGURE 14. Interface to Motorola Microprocessors.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the DO register, as shown in Figure 15. The address decoder must pull down $\overline{\text{ADC\_CS}}$ at ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 16 shows a typical interface to Intel.

A conversion is initiated by a write instruction to address $\overline{\text{ADC\_CS}}$. Data pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the $\overline{\text{ADC\_CS}}$ address fetches the Low byte, and a read instruction from the $\overline{\text{ADC\_CS}}$ address +2 fetches the High byte.

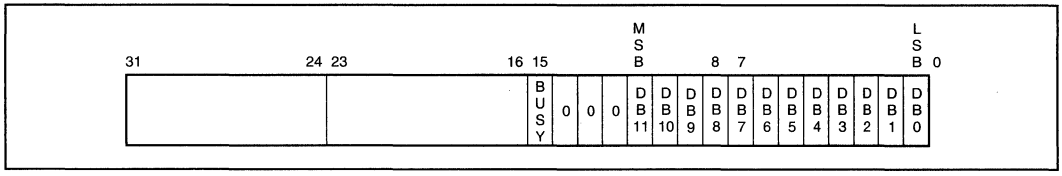


FIGURE 15. Conversion Results in Motorola Register D0.

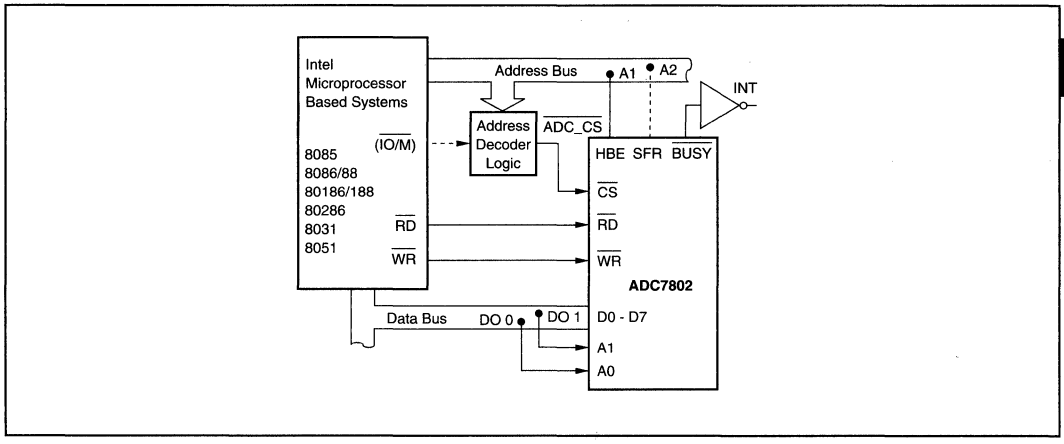
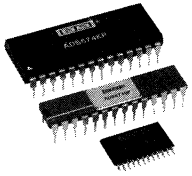


FIGURE 16. Interface to Intel Microprocessors.

BURR - BROWN®



ADS574

Microprocessor-Compatible Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- **COMPATIBLE WITH ADC574**
- **COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE**
- **FAST ACQUISITION AND CONVERSION: 25µs max**
- **ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS**
- **GUARANTEED AC AND DC PERFORMANCE**
- **SINGLE +5V SUPPLY OPERATION**
- **LOW POWER: 100mW max**
- **PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC**

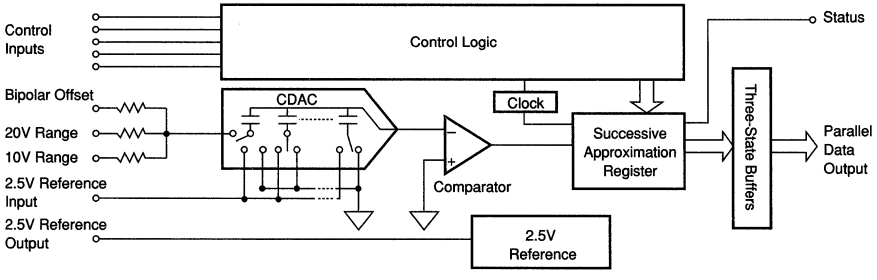
DESCRIPTION

The ADS574 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574 models in most applications, with internal sampling, much lower power consumption, and capability to operate from a single +5V supply.

The ADS574 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time for 12-bit conversions is 25µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS574 requires +5V, with –12V or –15V optional, depending on usage. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic DIPs and 28-pin SOICs.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, sampling frequency of 40kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS574JE/JP/JU MIN	ADS574JE/JP/JU TYP	ADS574JE/JP/JU MAX	ADS574KE/KP/KU MIN	ADS574KE/KP/KU TYP	ADS574KE/KP/KU MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	15	21		*	*		kΩ
±10V, 0V to +20V	60	84		*	*		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1] (adjustable to zero)			±0.25			*	% of FS [2]
No Missing Codes Resolution (Diff. Linearity)	12			12			Bits
T_{MIN} to T_{MAX} [3]							
Linearity Error			±1			±1/2	LSB
Full-Scale Calibration Error			±0.47			±0.37	% of FS
Unipolar Offset			±4			±3	LSB
Bipolar Offset			±12			±5	LSB
No Missing Codes Resolution	12			12			Bits
AC ACCURACY [4]							
Spurious Free Dynamic Range	73	78		76	*		dB
Total Harmonic Distortion		−77	−72		*	−75	dB
Signal-to-Noise Ratio	69	72		71	*		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	*		dB
Intermodulation Distortion (F_{IN1} = 10kHz, F_{IN2} = 11.5kHz)		−75			*		
TEMPERATURE COEFFICIENTS [5]							
Unipolar Offset		±1			*		ppm/°C
Bipolar Offset		±2			*		ppm/°C
Full-Scale Calibration		±12			*		ppm/°C
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration[6]							
+4.75V < V_{DD} < +5.25V			±1/2			*	LSB
CONVERSION TIME (Including Acquisition Time)							
t_{AQ} + t_C at 25°C:							
8-Bit Cycle		16	18		*	*	µs
12-Bit Cycle		22	25		*	*	µs
12-Bit Cycle, T_{MIN} to T_{MAX}		22	25		*	*	µs
SAMPLING DYNAMICS							
Sampling Rate	40			*			kHz
Aperture Delay, t_{AP}							
With V_{EE} = +5V		20			*		ns
With V_{EE} = 0V to −15V		4.0			*		µs
Aperture Uncertainty (Jitter)							
With V_{EE} = +5V		300			*		ps, rms
With V_{EE} = 0V to −15V		30			*		ns, rms
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF

SPECIFICATIONS (CONT)

ELECTRICAL

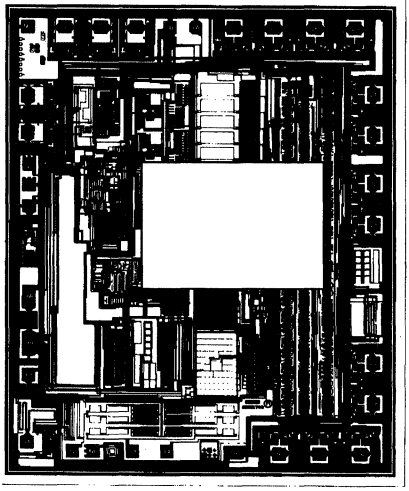
At $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 40kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS574JE/JP/JU MIN	ADS574JE/JP/JU TYP	ADS574JE/JP/JU MAX	ADS574KE/KP/KU MIN	ADS574KE/KP/KU TYP	ADS574KE/KP/KU MAX	UNITS
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} (7)	–16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} (7) (V_{EE} = –15V)		–1			*		mA
I_{DD}		+13	+20		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX}) (V_{EE} = 0V to +5V)		65	100		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating:	–40		+85	*		*	°C
Storage	–65		+150	*		*	°C

*Same specification as ADS574JE/JP/JU.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at T_{MIN} and T_{MAX}. (4) Based on using V_{EE} = +5V, which starts a conversion immediately upon a convert command. Using V_{EE} = 0V to –15V makes the ADS574/ADS774 emulate standard ADC574 operation. In this mode, the internal sample/hold acquires the input signal after receiving the convert command, and does not assume that the input level has been stable before the convert command arrives. (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

DICE INFORMATION



ADS574 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	V_{DD}	15	Digital Common
2	12/$\overline{8}$	16	DB0 (LSB)
3	$\overline{CS}$	17	DB1
4	A_0	18	DB2
5	R/$\overline{C}$	19	DB3
6	CE	20	DB4
7	NC	21	DB5
8	2.5V Ref Out	22	DB6
9A, 9B	Analog Common	23	DB7
10	2.5 Ref In	24	DB8
11	V_{EE} (Mode Control)	25	DB9
12	Bipolar Offset	26	DB10
13	10V Range	27	DB11 (MSB)
14	20V Range	28	Status

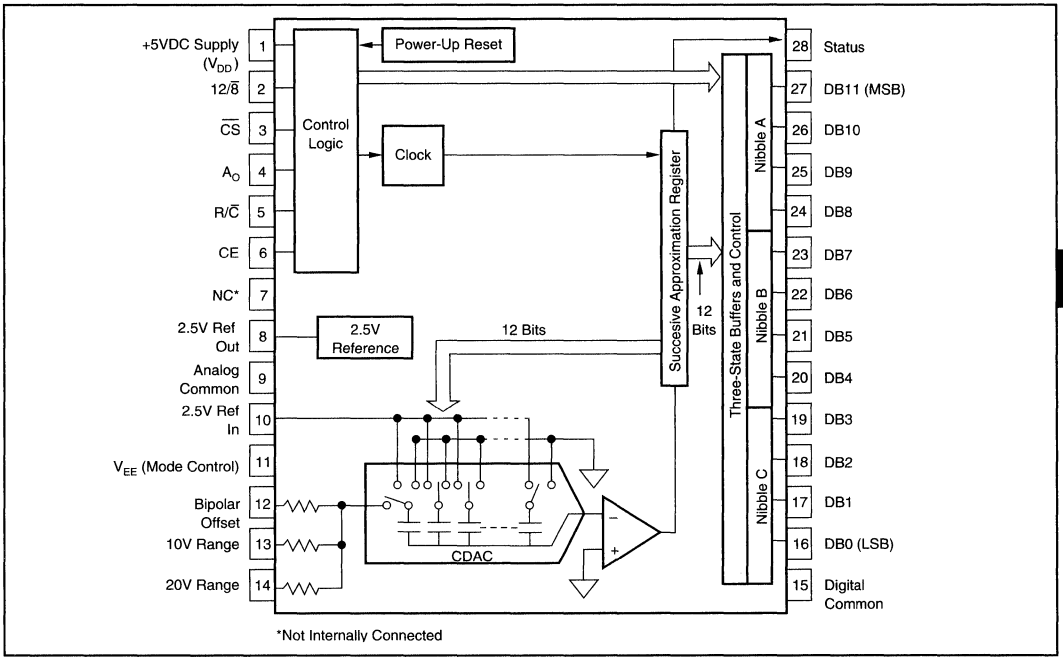
Substrate Bias: $+V_{DD}$

NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	172 x 142 ±5	4.37 x 3.61 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common	$+V_{DD}$ to −16.5V
V_{DD} to Digital Common	0V to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, CS, A_0, 12/8, R/C) to Digital Common	−0.5V to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{DD}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering,10s)	+300°C
Thermal Resistance, θ_{JA} : Ceramic DIPs	50°C/W
Plastic DIPs	100°C/W
SOIC	100°C/W

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS574JE	0.3" Plastic DIP	246
ADS574KE	0.3" Plastic DIP	246
ADS574JP	0.6" Plastic DIP	215
ADS574KP	0.6" Plastic DIP	215
ADS574JU	SOIC	217
ADS574KU	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

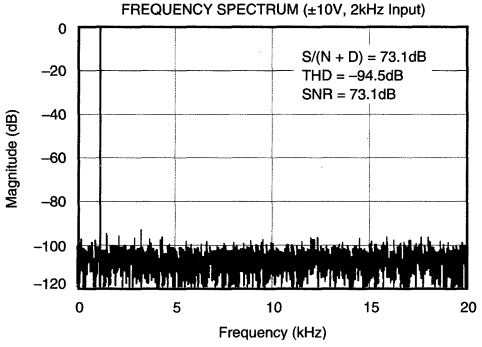
MODEL	PACKAGE	SINAD[1]	TEMPERATURE RANGE	LINEARITY ERROR
ADS574JE	0.3" Plastic DIP	68	0°C to +70°C	±1LSB
ADS574KE	0.3" Plastic DIP	70	0°C to +70°C	±1/2LSB
ADS574JP	0.6" Plastic DIP	68	0°C to +70°C	±1LSB
ADS574KP	0.6" Plastic DIP	70	0°C to +70°C	±1/2LSB
ADS574JU	SOIC	68	0°C to +70°C	±1LSB
ADS574KU	SOIC	70	0°C to +70°C	±1/2LSB

NOTE: (1) SINAD is Signal-to-(Noise and Distortion) expressed in dB.

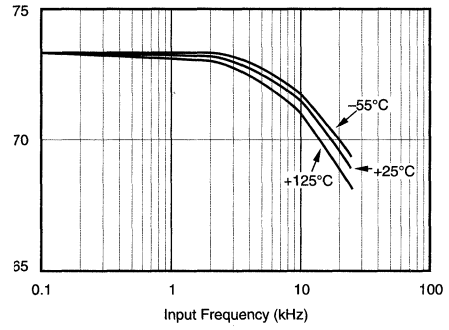
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 40kHz; unless otherwise specified. All plots use 4096 point FFTs.

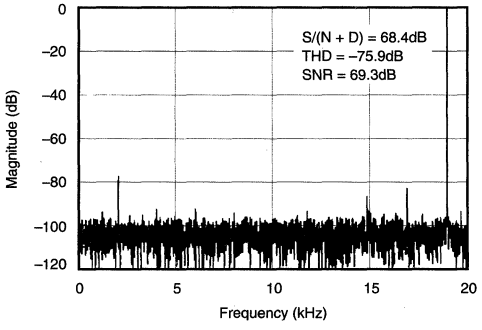
FREQUENCY SPECTRUM (±10V, 2kHz Input)



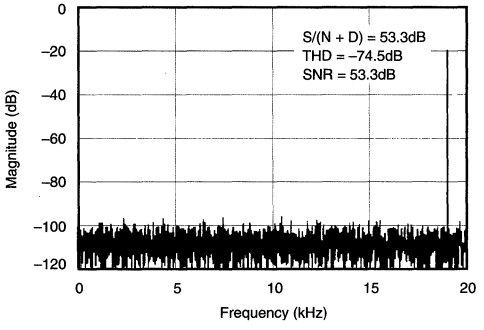
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



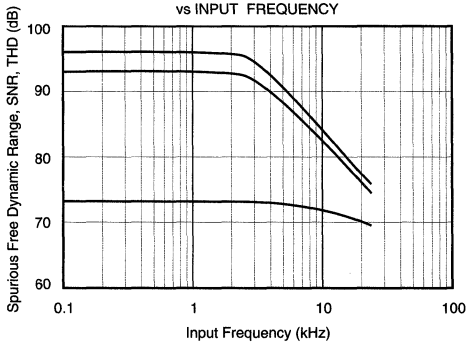
FREQUENCY SPECTRUM (±10V, 19kHz Input)



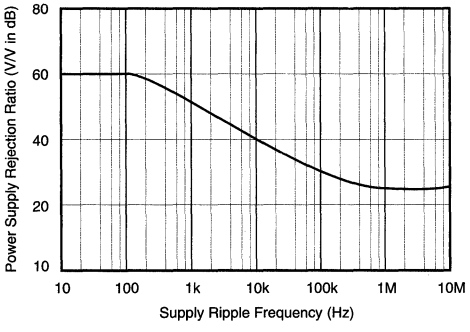
FREQUENCY SPECTRUM (±1V, 19kHz Input)



SPURIOUS FREE DYNAMIC RANGE, SNR AND THD
vs INPUT FREQUENCY



POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY



THEORY OF OPERATION

In the ADS574, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

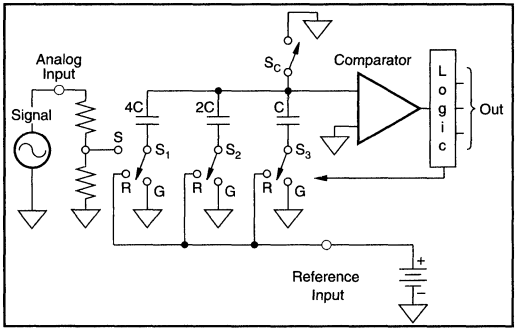


FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_c is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_c is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G". Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum circuit required to operate the ADS574 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS574 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS574.

The ADS574 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS574 is designed to complete a conversion and accurately acquire a new signal in 25µs max over the full operating temperature range, so that conversions can take place at a full 40kHz.

CONTROLLING THE ADS574

The Burr-Brown ADS574 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to +5V. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

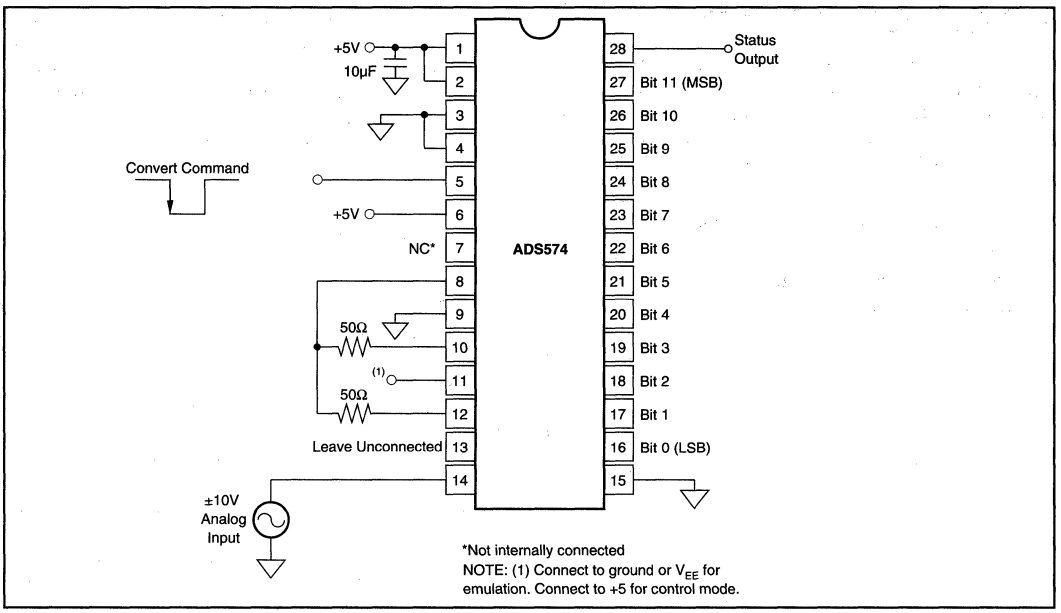


FIGURE 2. Basic ±10V Operation.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	+5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8 n = 12	$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	 + Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (– Full-Scale Calibration)	 +10V – 3/2LSB 0 – 1/2LSB –10V + 1/2LSB	 +5V – 3/2LSB 0 – 1/2LSB –5V + 1/2LSB	 +10V – 3/2LSB +5V – 1/2LSB 0 to +1/2LSB	 +10V – 3/2LSB ±10V – 1/2LSB 0 to +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be LOW ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS574 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS574 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

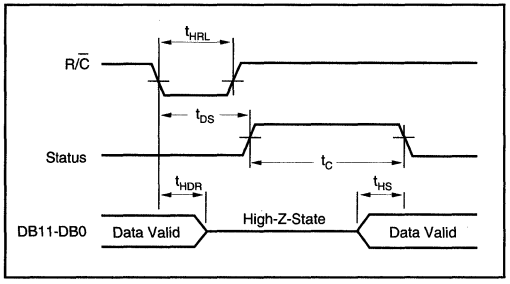


FIGURE 3. R/C Pulse Low—Outputs Enabled After Conversion.

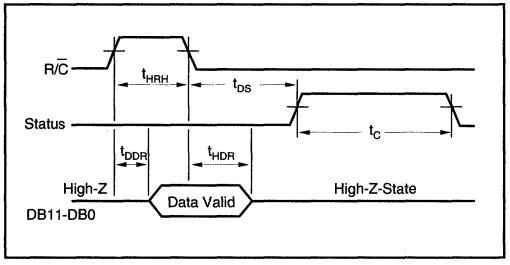


FIGURE 4. R/C Pulse High — Outputs Enabled Only While R/C Is High.

S/H CONTROL MODE AND ADC574 EMULATION MODE

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode it is assumed that during the required 4µs acquisition time the signal is not slewing faster than the slew rate of the ADS574. No assumption is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command.

This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized by the internal sample/hold circuit, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, no assumption is made about the input signal prior to the convert command. A delay time is introduced between the convert command and the start of conversion to allow the ADS574 enough time to acquire the input signal before converting. The delay increases the effective aperture time from 0.02µs to 4µs, but allows the ADS574 to replace the ADC574 in any circuit. Any slewing of the analog input prior to the convert command in existing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	25			ns
t_{DS}	STS Delay from R/C			200	ns
t_{HDR}	Data Valid After R/C Low	25			ns
t_{HRH}	High R/C Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	CS to CE setup	50	20		ns
t_{HSC}	CS low during CE high	50	20		ns
t_{SRC}	R/C to CE setup	50	0		ns
t_{HRC}	R/C low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	CS to CE setup	50	0		ns
t_{SRR}	R/C to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	CS valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STC delay after data valid	300	400	1000	

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).

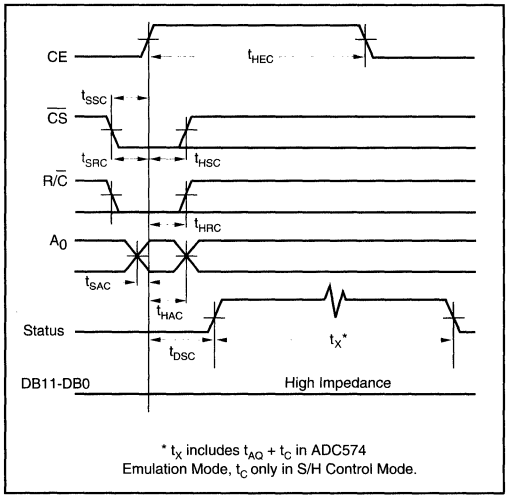


FIGURE 5. Conversion Cycle Timing.

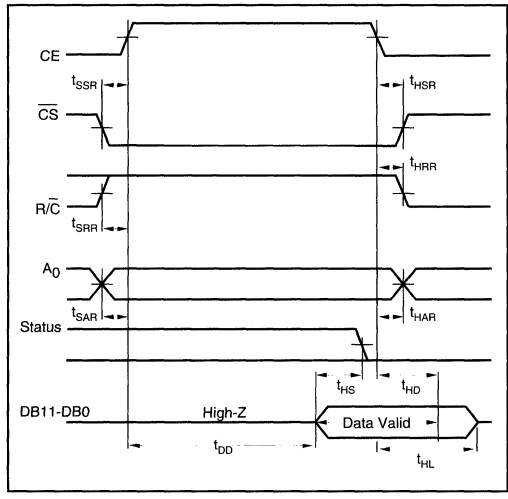


FIGURE 6. Read Cycle Timing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

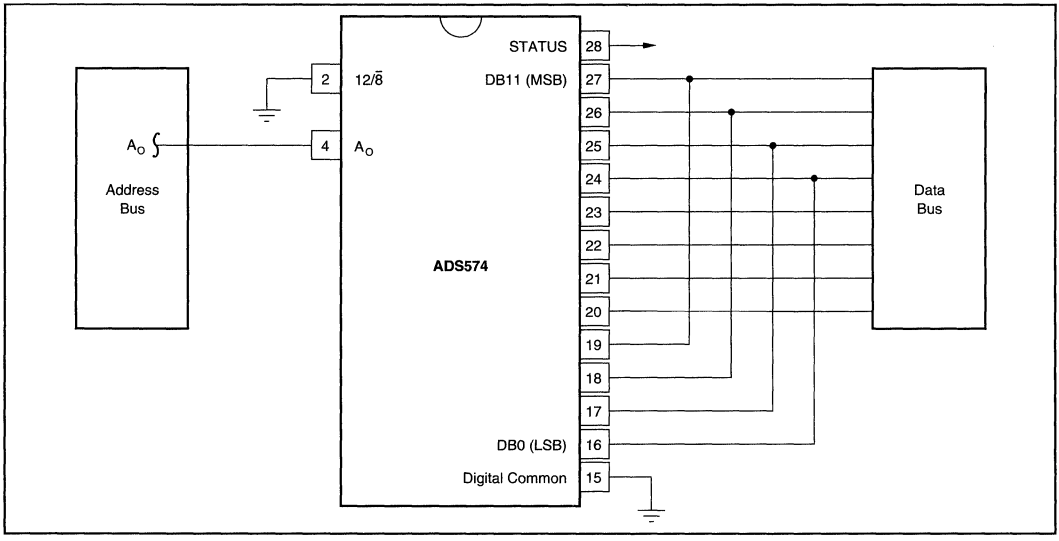


FIGURE 8. Connection to an 8-Bit Bus.

systems (due to multiplexers, sample/holds, etc. in front of the converter) does not affect the accuracy of the ADS574 conversion in the Emulation Mode.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

Basically, the Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS574 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The Emulation Mode allows the ADS574 to be dropped into almost all existing ADC574 sockets without changes to any other existing system hardware or software. The input to the ADS574 in the Emulation Mode does not need to be stable before a convert command is received, so that multiplexers, programmable gain amplifiers, etc., can be slewing quickly any time before a convert command is given as long as the analog input to the ADS574 is stable after the convert command is received, as it needs to be in existing ADC574 systems for accurate operation. In fact, even in the Emulation Mode, system throughput can be speeded up, since the input to the ADS574 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC574s.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS574, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

SYMBOL	PARAMETER	S/H CONTROL MODE (Pin 11 Connected to +5V) MIN	TYP	MAX	ADC574 EMULATION MODE (Pin 11 Connected to 0V to –15V) MIN	TYP	MAX	UNITS
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		22	25		22	25	µs
	8-bit Conversions		16	18		16	18	µs
t_C	Conversion Time:							
	12-bit Conversions		18			18		µs
	8-bit Conversions		12			12		µs
t_{AQ}	Acquisition Time		4			4		µs
t_{AP}	Aperture Delay		20			4000		ns
t_J	Aperture Uncertainty		0.3			30		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.

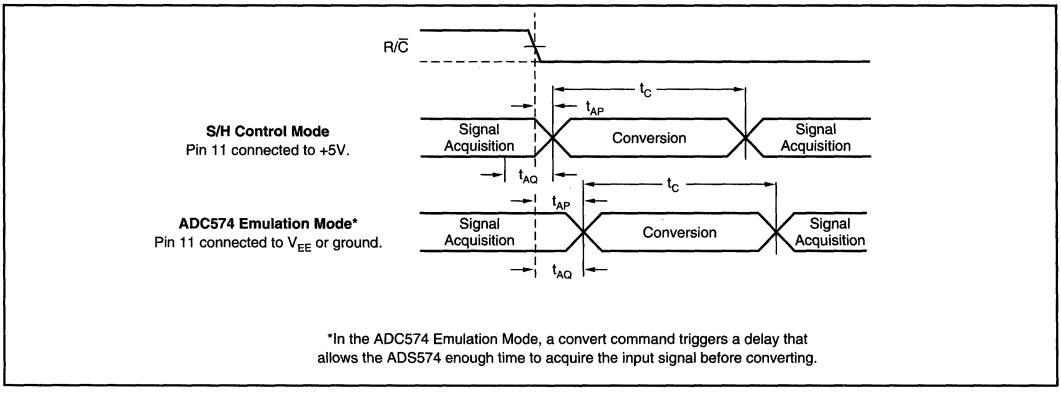


FIGURE 9. Signal Acquisition and Conversion Timing.

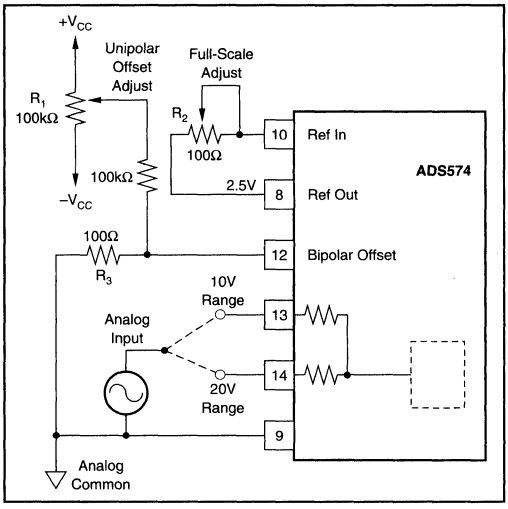


FIGURE 10. Unipolar Configuration.

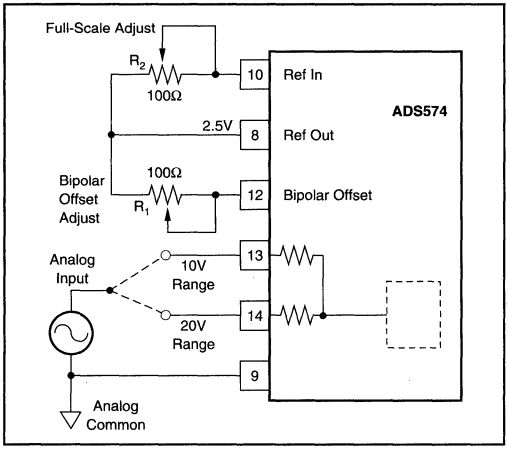


FIGURE 11. Bipolar Configuration.

If the 10V analog input range is used (either bipolar or unipolar), the 20V range input (pin 14) should be shielded with ground plane to reduce noise pickup.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS574.

POWER SUPPLY DECOUPLING

On the ADS574, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC574 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC574 socket, the –15V on pin 11 selects the ADC574 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS574 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS574 is typically 84kΩ in the 20V ranges and 21kΩ in the 10V ranges. This is significantly higher than that of traditional ADC574 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS574. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high imped-

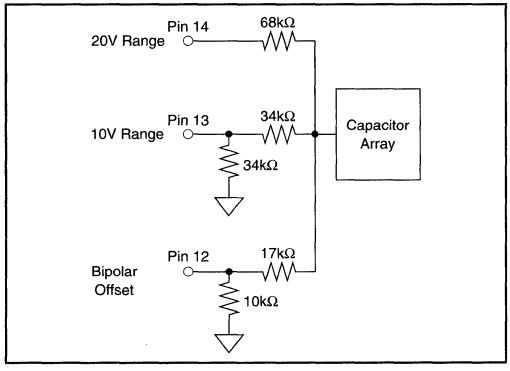


FIGURE 12. ADS574 Input Structure.

ance node as compared with traditional ADC574 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS574 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected to analog common pin 9. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (68kΩ + 68kΩ || 17kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide offset adjust response the same as that of traditional ADC574 architectures without needing to change the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS574 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is where +12V or +15V is supplied on traditional ADC574s. Pin 11, the –12V or –15V supply input on traditional ADC574s, is used only as a logic input on the ADS574. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS574, and this resistor will add 10mW to 15mW to the power consumption of the ADS574 when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS574 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS574 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 10 with a 50Ω, 1% metal film resistor, omitting the other adjustment components. Connect pin 12 to pin 9.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, replace the potentiometers in Figure 11 by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

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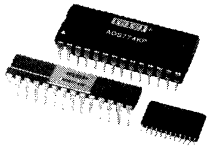


ADS774

Microprocessor-Compatible Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- COMPATIBLE WITH ADC574, ADC674 AND ADC774 SOCKETS
- COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE
- FAST ACQUISITION AND CONVERSION: 8.5µs max OVER TEMPERATURE
- ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS
- GUARANTEED AC AND DC PERFORMANCE
- SINGLE +5V SUPPLY OPERATION
- LOW POWER: 120mW max
- PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC

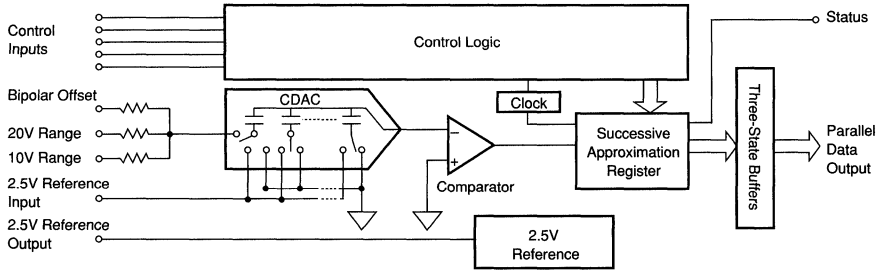
DESCRIPTION

The ADS774 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574, ADC674, and ADC774 models in most applications, with internal sampling, much lower power consumption, and the ability to operate from a single +5V supply.

The ADS774 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time is 8.5µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS774 requires +5V, with –15V optional. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic DIP and 28-pin SOICs.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, f_{IN} = 10kHz; unless otherwise specified.

	ADS774JE/JP/JU			ADS774KE/KP/KU			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar			0 to +10, 0 to +20				V
Bipolar			±5, ±10				V
Impedance: 0 to +10V, ±5V	8.5	12		*	*		kΩ
±10V, 0V to +20V	35	50		*	*		kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Voltages: Logic 1	+2.0		+5.5	*		*	V
Logic 0	–0.5		+0.8	*		*	V
Current	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error [1] (adjustable to zero)			±0.25			*	% of FS [2]
No Missing Codes Resolution	12			12			Bits
T_{MIN} to T_{MAX} [3]							
Linearity Error			±1			±1/2	LSB
Full-Scale Calibration Error			±0.47			±0.37	% of FS
Unipolar Offset			±4			±3	LSB
Bipolar Offset			±12			±5	LSB
No Missing Codes Resolution	12			12			Bits
AC ACCURACY [4]							
Spurious Free Dynamic Range	73	78		76	*		dB
Total Harmonic Distortion		–77	–72		*	–75	dB
Signal-to-Noise Ratio	69	72		71	*		dB
Signal-to-(Noise + Distortion) Ratio	68	71		70	*		dB
Intermodulation Distortion (F_{IN1} = 20kHz, F_{IN2} = 23kHz)		–75			*		
TEMPERATURE COEFFICIENTS [5]							
Unipolar Offset		±1			*		ppm/°C
Bipolar Offset		±2			*		ppm/°C
Full-Scale Calibration		±12			*		ppm/°C
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration[6]							
+4.75V < V_{DD} < +5.25V							
Max Change			±1/2			*	LSB
CONVERSION TIME (Including Acquisition Time)							
$t_{AQ} + t_C$ at 25°C:							
8-Bit Cycle		5.5	5.9		*	*	µs
12-Bit Cycle		7.5	8		*	*	µs
12-Bit Cycle, T_{MIN} to T_{MAX}:		8	8.5		*	*	µs
SAMPLING DYNAMICS							
Sampling Rate at 25°C	125			*			kHz
T_{MIN} to T_{MAX}	117			*			kHz
Aperture Delay, t_{AP}							
With V_{EE} = +5V		20			*		ns
With V_{EE} = 0V to –15V		1.6			*		µs
Aperture Uncertainty (Jitter)							
With V_{EE} = +5V		300			*		ps, rms
With V_{EE} = 0V to –15V		10			*		ns, rms
Settling time to 0.01% for Full-Scale Input Change		1.4			*		µs

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, f_{IN} = 10kHz; unless otherwise specified.

PARAMETER	ADS774JE/JP/JU MIN	ADS774JE/JP/JU TYP	ADS774JE/JP/JU MAX	ADS774KE/KP/KU MIN	ADS774KE/KP/KU TYP	ADS774KE/KP/KU MAX	UNITS
OUTPUTS							
DIGITAL (DB_{11} - DB_0, STATUS)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+2.4	+2.5	+2.6	*	*	*	V
Source Current Available for External Loads	0.5			*			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{EE} (7)	–16.5		V_{DD}	*		*	V
V_{DD}	+4.5		+5.5	*		*	V
Current: I_{EE} (7) (V_{EE} = –15V)		–1			*		mA
I_{DD}		+15	+24		*	*	mA
Power Dissipation (T_{MIN} to T_{MAX})							
(V_{EE} = 0V to +5V)		75	120		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating:	–40		+85	*		*	°C
Storage Temperature Range	–65		+150	*		*	°C

*Same specification as ADS774JE/JP/JU.

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. (3) Maximum error at T_{MIN} and T_{MAX}. (4) Based on using V_{EE} = +5V, which is the Control Mode. See the section "S/H Control Mode and ADC774 Emulation Mode." (5) Using internal reference. (6) This is worst case change in accuracy from accuracy with a +5V supply. (7) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5µA typ; when V_{EE} = +5V, I_{EE} = +167µA typ.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common	$+V_{DD}$ to −16.5V
V_{DD} to Digital Common	0V to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	−0.5V to V_{DD} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{DD}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering,10s)	+300°C
Thermal Resistance, θ_{JA} : Ceramic DIPs	50°C/W
Plastic DIPs	100°C/W
SOIC	100°C/W

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS774JE	28-pin 0.3" Plastic DIP	246
ADS774KE	28-pin 0.3" Plastic DIP	246
ADS774JP	28-pin 0.6" Plastic DIP	215
ADS774KP	28-pin 0.6" Plastic DIP	215
ADS774JU	28-pin SOIC	217
ADS774KU	28-pin SOIC	217

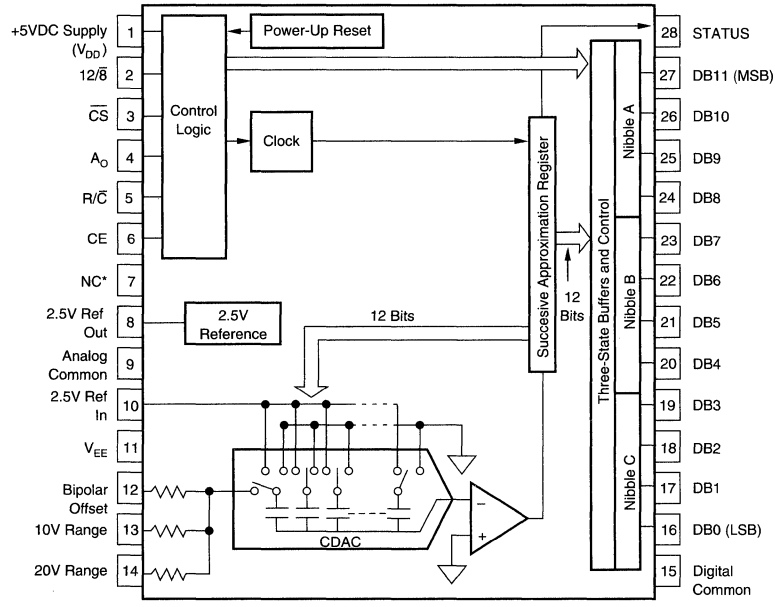
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	SINAD[1]	TEMPERATURE RANGE	LINEARITY ERROR
ADS774JE	0.3" Plastic DIP	68dB	0°C to +70°C	±1LSB
ADS774KE	0.3" Plastic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JP	0.6" Plastic DIP	68dB	0°C to +70°C	±1LSB
ADS774KP	0.6" Plastic DIP	70dB	0°C to +70°C	±1/2LSB
ADS774JU	SOIC	68dB	0°C to +70°C	±1LSB
ADS774KU	SOIC	70dB	0°C to +70°C	±1/2LSB

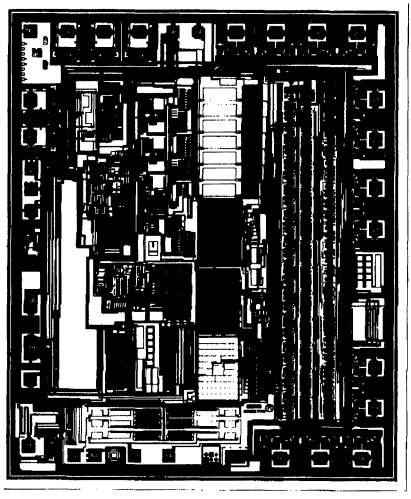
NOTE: (1) SINAD is Signal-to-(Noise and Distortion) expressed in dB.

CONNECTION DIAGRAM



*Not Internally Connected

DICE INFORMATION



ADS774 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	V_{DD}	15	Digital Common
2	12/8	16	DB0 (LSB)
3	CS	17	DB1
4	A_0	18	DB2
5	R/C	19	DB3
6	CE	20	DB4
7	NC	21	DB5
8	2.5V Ref Out	22	DB6
9A, 9B	Analog Common	23	DB7
10	2.5 Ref In	24	DB8
11	V_{EE} (Mode Control)	25	DB9
12	Bipolar Offset	26	DB10
13	10V Range	27	DB11 (MSB)
14	20V Range	28	Status

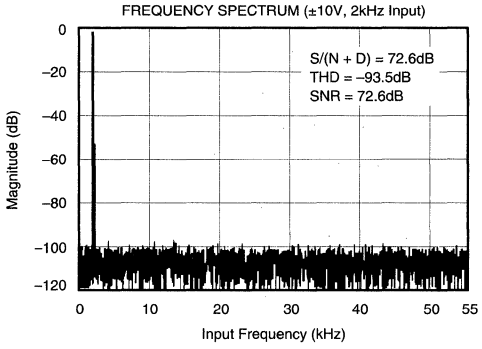
Substrate Bias: $+V_{DD}$
NC: No Connection.

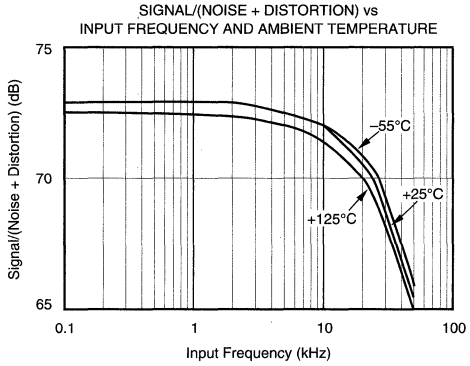
MECHANICAL INFORMATION

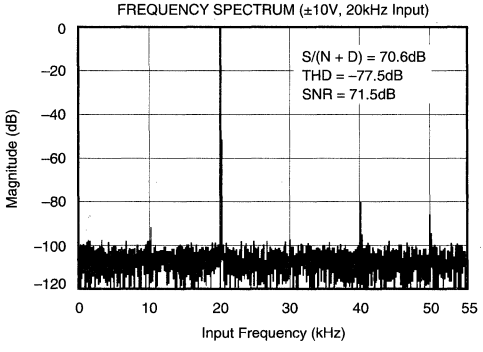
	MILS (0.001")	MILLIMETERS
Die Size	172 x 142 ±5	4.37 x 3.61 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization	Aluminum	

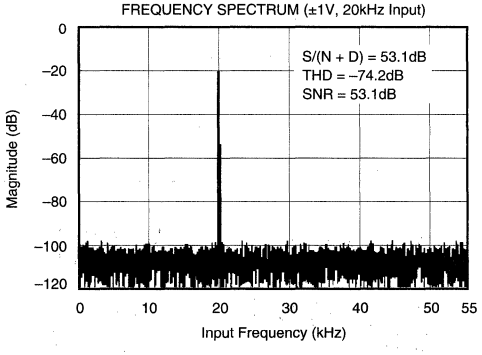
TYPICAL PERFORMANCE CURVES

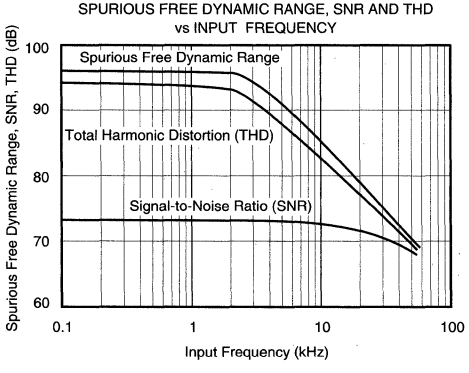
At T_A = +25°C, V_{DD} = V_{EE} = +5V; Bipolar ±10V Input Range; sampling frequency of 110kHz; unless otherwise specified. All plots use 4096 point FFTs.

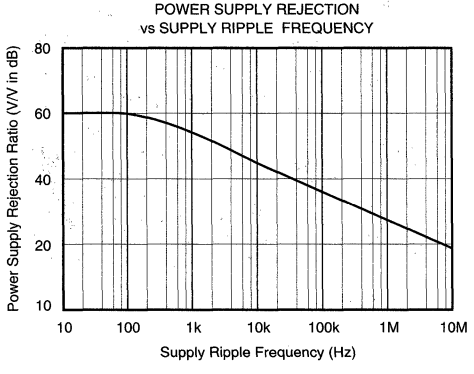












THEORY OF OPERATION

In the ADS774, the advantages of advanced CMOS technology—high logic density, stable capacitors, precision analog switches—and Burr-Brown's state of the art laser trimming techniques are combined to produce a fast, low power analog-to-digital converter with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution A/D converter with only 3 bits is shown in Figure 1.

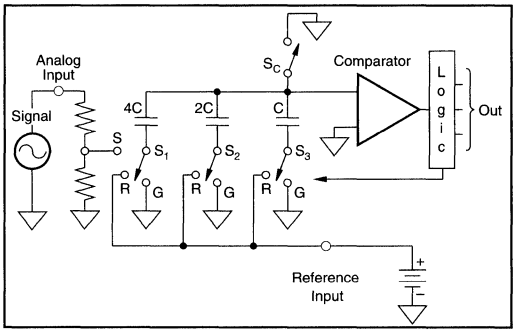


FIGURE 1. 3-Bit Charge Redistribution A/D.

INPUT SCALING

Precision laser-trimmed scaling resistors at the input divide standard input ranges (0V to +10V, 0V to +20V, ±5V or ±10V) into levels compatible with the CMOS characteristics of the internal capacitor array.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position "G". Switch S_C is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_C is opened to float the comparator input. The charge trapped in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2, and S_3 to positions "R" (to connect to the reference) or "G" (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G". Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made the voltage level at the comparator will be within 1/2LSB of GND, and a digital word which represents the analog input can be determined from the positions of S_1, S_2 and S_3.

OPERATION

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the ADS774 in a basic ±10V range in the Control Mode (discussed in detail in a later section.) The falling edge of a Convert Command (a pulse taking pin 5 LOW for a minimum of 25ns) both switches the ADS774 input to the hold state and initiates the conversion. Pin 28 (STATUS) will output a HIGH during the conversion, and falls only after the conversion is completed and the data has been latched on the data output pins (pins 16 to 27.) Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins in a High-Z state and inhibits the input lines. This means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS774.

The ADS774 will begin acquiring a new sample as soon as the conversion is completed, even before the STATUS output falls, and will track the input signal until the next conversion is started. The ADS774 is designed to complete a conversion and accurately acquire a new signal in 8.5µs max over the full operating temperature range, so that conversions can take place at a full 117kHz.

CONTROLLING THE ADS774

The Burr-Brown ADS774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or the 8 MSB bits followed by the 4 LSB bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is shown in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to +5V. The output data are

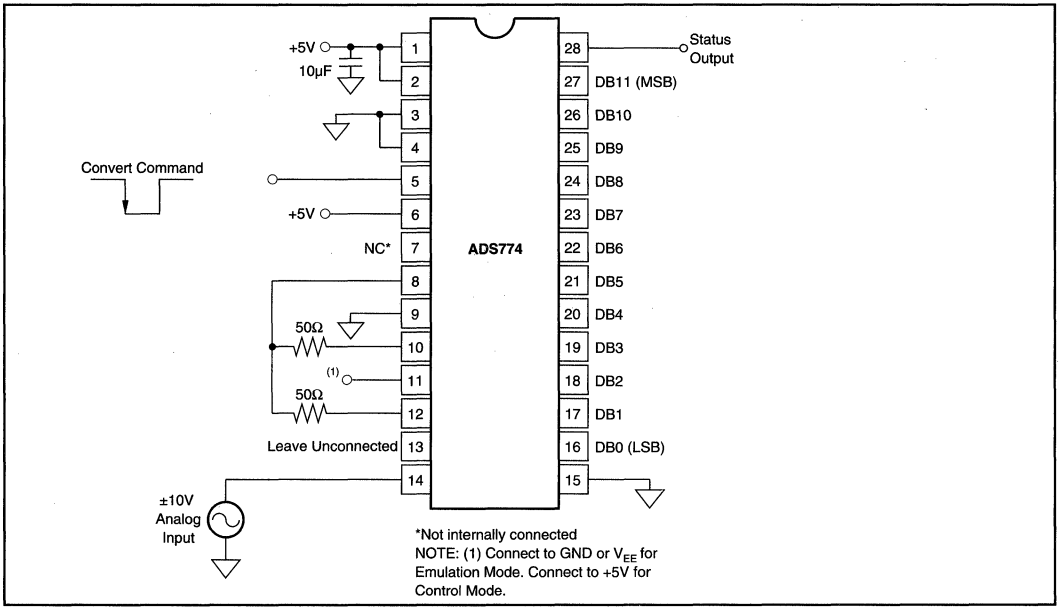


FIGURE 2. Basic ±10V Operation.

presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and STATUS is LOW. Thus, there are two possible modes of operation; data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case the R/$\overline{C}$ pulse must remain LOW for a minimum of 25ns.

Figure 3 illustrates timing with an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion.

Figure 4 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode the output data from the previous conversion is enabled during the time R/$\overline{C}$ is HIGH. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a HIGH R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched HIGH, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is LOW. If all 12 bits are read following an 8-bit conversion, the 4LSBs (DB0-DB3) will be LOW (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition occurring on any of three logic inputs ($\overline{CE}$, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of the critical input. Timing relationships for start of conversion timing are illustrated in Figure 5. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	±5V	0V to +10V	0V to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V – 3/2LSB	+5V – 3/2LSB	+10V – 3/2LSB	+20V – 3/2LSB
$7FFF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0V – 1/2LSB	0V – 1/2LSB	+5V – 1/2LSB	+10V – 1/2LSB
000_H to 001_H	Zero Calibration (– Full-Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0V +1/2LSB	0V +1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be HIGH ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be LOW ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be LOW ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be HIGH ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

TABLE III. Control Input Truth Table.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ HIGH, STATUS LOW, CE HIGH, and $\overline{CS}$ LOW. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 6 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the HIGH or LOW condition, although it is fully TTL and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is HIGH, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is LOW, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is LOW, the byte addressed contains the 8MSBs. When A_0 is HIGH, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. Connection of the ADS774 to an 8-bit bus for transfer of the data is illustrated in Figure 8. The design of the ADS774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together in Figure 8 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

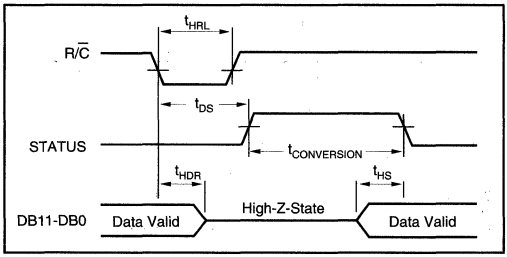


FIGURE 3. R/C Pulse Low—Outputs Enabled After Conversion.

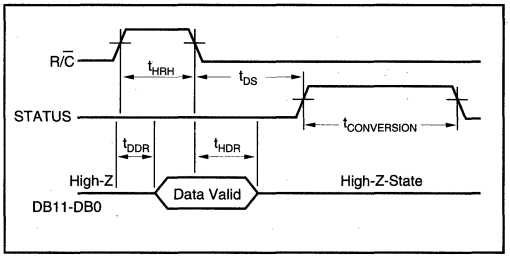


FIGURE 4. R/C Pulse High — Outputs Enabled Only While R/C Is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	25			ns
t_{DS}	STS Delay from R/C			200	ns
t_{HDR}	Data Valid After R/C Low	25			ns
t_{HRH}	High R/C Pulse Width	100			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing. ($T_A = T_{MIN}$ to T_{MAX}).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	CS to CE setup	50	20		ns
t_{HSC}	CS low during CE high	50	20		ns
t_{SRC}	R/C to CE setup	50	0		ns
t_{HRC}	R/C low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	CS to CE setup	50	0		ns
t_{SRR}	R/C to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	CS valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STATUS delay after data valid	75	150	375	ns

TABLE V. Timing Specifications, Fully Controlled Operation. ($T_A = T_{MIN}$ to T_{MAX}).

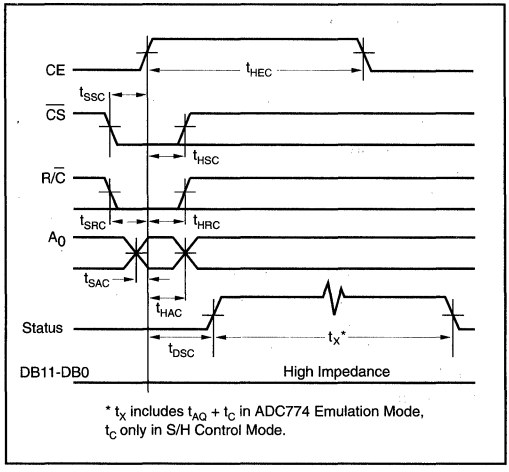


FIGURE 5. Conversion Cycle Timing.

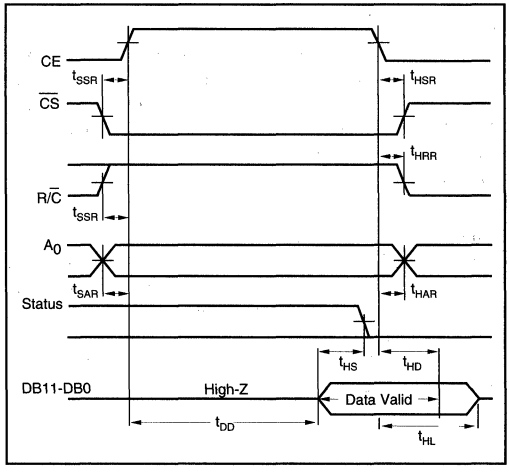


FIGURE 6. Read Cycle Timing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

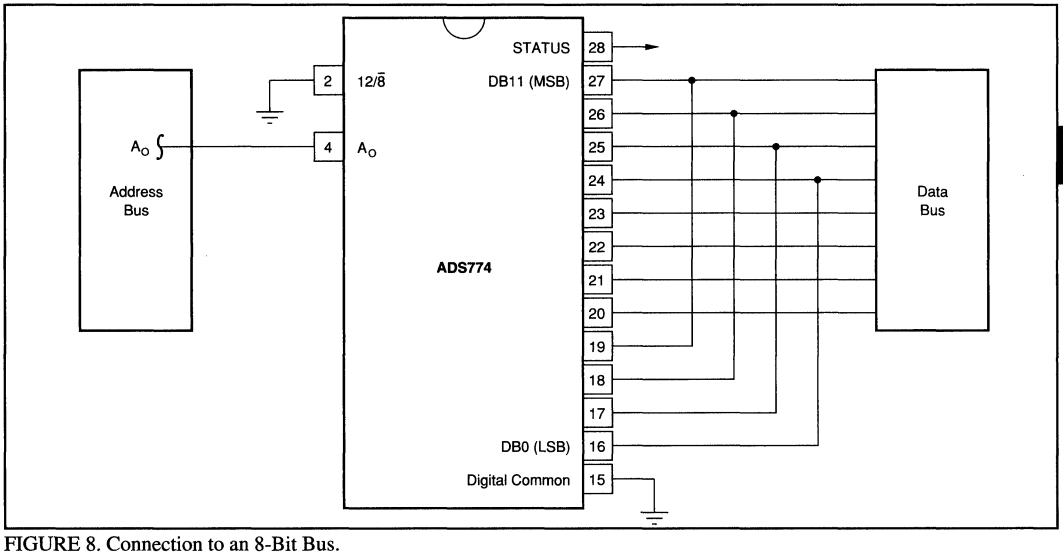


FIGURE 8. Connection to an 8-Bit Bus.

S/H CONTROL MODE AND ADC774 EMULATION MODE

The Emulation Mode allows the ADS774 to be dropped into most existing ADC774 sockets without changes to other system hardware or software. In existing sockets, the analog input is held stable during the conversion period so that accurate conversions can proceed, but the input can change rapidly at any time before the conversion starts. The Emulation Mode uses the stability of the analog input during the conversion period to both acquire and convert in a maximum of 8µs (8.5µs over temperature.) In fact, system throughput can be increased, since the input to the ADS774 can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC774s.

The Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and A/D, the ADS774 in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. The differences are shown in Figure 9 and Table VI. In the Control Mode, it is assumed that during the required 1.4µs acquisition time the signal is not changing faster than the ADS774 can track. No assumption is made about the input level after the convert command arrives, since the input signal is sampled and conversion begins immediately after the convert command. This means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized in the Control Mode, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, a delay time is introduced between the convert command and the start of conversion to allow the ADS774 enough time to acquire the input signal before converting. This increases the effective aperture delay time from 0.02µs to 1.6µs, but allows the ADS774 to replace the ADC774 in most circuits without additional changes. In designs where the input to the ADS774 is changing rapidly in the 200ns prior to a convert command, system performance may be enhanced by delaying the convert command by 200ns.

When using the ADS774 in the Emulation Mode to replace existing converters in current designs, a sample/hold amplifier often precedes the converter. In these cases, no additional delay in the convert command will be needed. The existing sample/hold will not be slewing excessively when going from the sample mode to the hold mode prior to a conversion.

In both modes, as soon as the conversion is completed the internal sample/hold circuit immediately begins slewing to track the input signal.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

The speed of the ADS774 requires special caution regarding whichever input pin is unused. For 10V input ranges, pin 14 (20V Range) must be unconnected, and for 20V input ranges, pin 13 (10V Range) must be unconnected. In both cases, the unconnected input should be shielded with ground plane to reduce noise pickup.

In particular, the unused input pin should not be connected to any capacitive load, including high impedance switches. Even a few pF on the unused pin can degrade acquisition time.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be as close as possible to the ADS774.

POWER SUPPLY DECOUPLING

On the ADS774, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC774 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC774 socket, the –15V on pin 11 selects the ADC774 Emulation Mode. Since pin 11 is used as a logic input, it is immune to typical supply variations.

		S/H CONTROL MODE (Pin 11 Connected to +5V)			ADC774 EMULATION MODE (Pin 11 Connected to 0V to –15V)			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
$t_{AQ} + t_C$	Throughput Time:							
	12-bit Conversions		8	8.5		8	8.5	µs
	8-bit Conversions		6	6.3		6	6.3	µs
t_C	Conversion Time:							
	12-bit Conversions		6.4			6.4		µs
	8-bit Conversions		4.4			4.4		µs
t_{AQ}	Acquisition Time		1.4			1.4		µs
t_{AP}	Aperture Delay		20			1600		ns
t_J	Aperture Uncertainty		0.3			10		ns

TABLE VI. Conversion Timing, T_{MIN} to T_{MAX}.

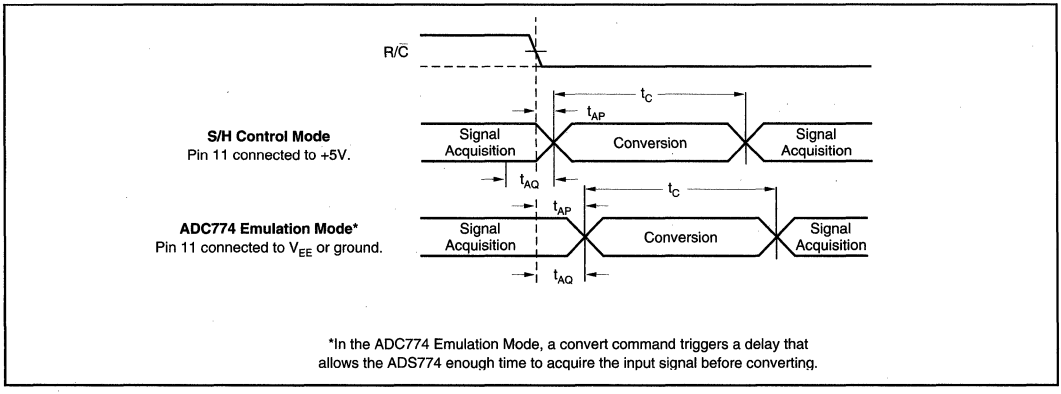


FIGURE 9. Signal Acquisition and Conversion Timing.

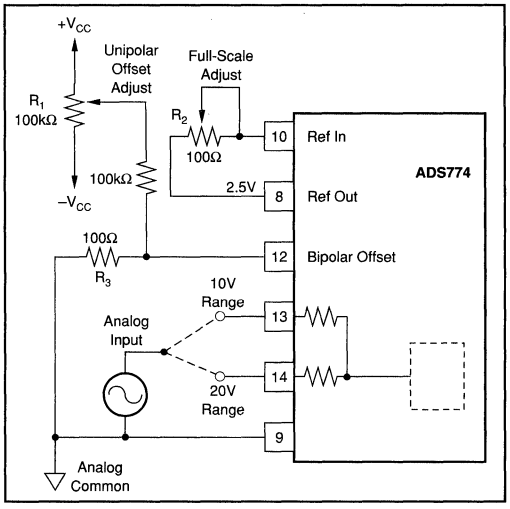


FIGURE 10. Unipolar Configuration.

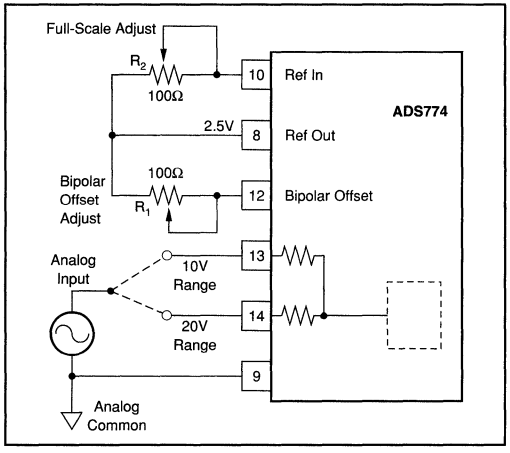


FIGURE 11. Bipolar Configuration.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 2. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figures 10 and 11 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described below.

The input impedance of the ADS774 is typically 50kΩ in the 20V ranges and 12kΩ in the 10V ranges. This is significantly higher than that of traditional ADC774 architectures, reducing the load on the input source in most applications.

INPUT STRUCTURE

Figure 12 shows the resistor divider input structure of the ADS774. Since the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high impedance node as compared with traditional ADC774 architectures, where the resistor divider network looks into a comparator input node at virtual ground.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and the analog input to the ADS774 must be converted to this range. Unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected to pin 9, analog common. From Figure 12, it is clear that the input to the capacitor array will be the analog input voltage on pin 14 divided by the resistor network (42kΩ + 42kΩ || 10.5kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

The main effect of the 10kΩ internal resistor on pin 12 is to provide the same offset adjust response as that of traditional ADC774 architectures without changing the external trimpot values.

SINGLE SUPPLY OPERATION

The ADS774 is designed to operate from a single +5V supply, and handle all of the unipolar and bipolar input ranges, in either the Control Mode or the Emulation Mode as described above. Pin 7 is not connected internally. This is

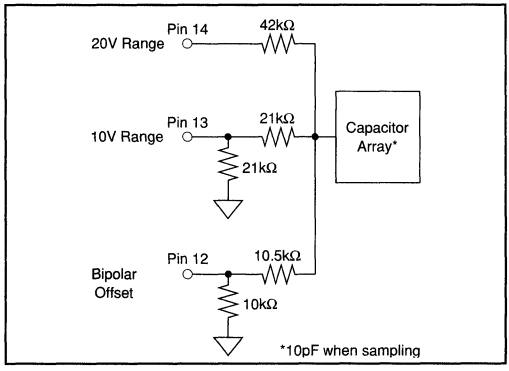


FIGURE 12. ADS774 Input Structure.

where +12V or +15V is supplied on traditional ADC774s. Pin 11, the –12V or –15V supply input on traditional ADC774s, is used only as a logic input on the ADS774. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS774, and this resistor will add 10mW to 15mW to the power consumption of the ADS774 when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS774 to function with a single +5V supply.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS774 as shown in Figures 10 and 11 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 10 with a 50Ω 1% metal film resistor and connect pin 12 to pin 9, omitting the other adjustment components.

If adjustment is required, connect the converter as shown in Figure 10. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (HIGH). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, replace the potentiometers in Figure 11 by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 11. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

BURR-BROWN®

ADS800

SpeedPlus™ 12-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW POWER: 390mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY
- 3-STATE OUTPUTS

APPLICATIONS

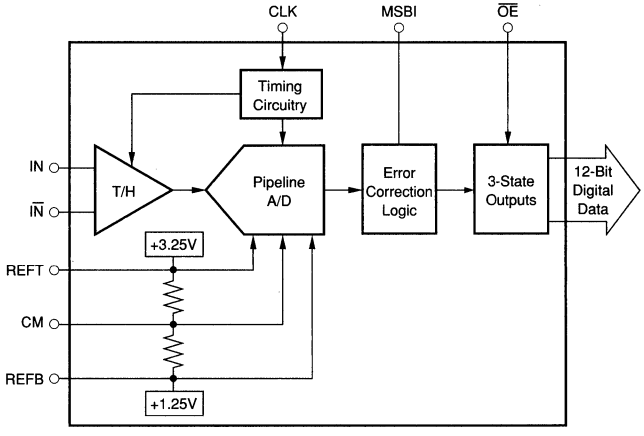
- IF AND BASEBAND DIGITIZATION
- DIGITAL COMMUNICATIONS
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING

DESCRIPTION

The ADS800 is a low power, monolithic 12-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference and three-state outputs. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS800 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications, test instrumentation and video applications.

This high performance A/D converter is specified over temperature for AC and DC performance at a 40MHz sampling rate. The ADS800 is available in a 28-pin SOIC package.



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SPECIFICATIONS

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS800U MIN	ADS800U TYP	ADS800U MAX	UNITS
Resolution					12	Bits
Specified Temperature Range	$T_{AMBIENT}$		0		+70	°C
Operating Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full Scale Input Range	Both Inputs, 180° Out of Phase		+1.25		+3.25	V
Common-Mode Voltage				+2.25		V
Analog Input Bandwidth (–3dB)						
Small Signal	–20dBFS(1) Input	+25°C		400		MHz
Full Power	0dBFS Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY(2)						
Gain Error		+25°C		±0.4	±1.5	%
		Full		±0.6	±2.5	%
Gain Tempco				±95		ppm/°C
Power Supply Rejection of Gain	Delta $+V_S$ = ±5%	+25°C		0.01	0.15	%FSR/%
Input Offset Error		+25°C		±2.4	±3.4	%
		Full		±2.6	±3.5	%FSR/%
Power Supply Rejection of Offset	Delta $+V_S$ = ±5%	+25°C		0.02	0.15	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		40M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error						
f = 500kHz	t_H = 13ns(3)	+25°C		±0.6	±1.0	LSB
		Full		±0.8		LSB
f = 12MHz		+25°C		±0.4	±1.0	LSB
		Full		±0.5		LSB
Integral Linearity Error at f = 500kHz		Full		±1.9		LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	65	72		dBFS
		Full	60	66		dBFS
f = 12MHz (–1dBFS input)		+25°C	58	61		dBFS
		Full	55	61		dBFS
Two-Tone Intermodulation Distortion (IMD)(4)						
f = 4.4MHz and 4.5MHz (–7dBFS each tone)		+25°C		–63		dBc
		Full		–62		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	61	64		dB
		Full	57	63		dB
f = 12MHz (–1dBFS input)		+25°C	61	62		dB
		Full	56	62		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	59	63		dB
		Full	54	64		dB
f = 12MHz (–1dBFS input)		+25°C	56	58		dB
		Full	51	57		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error	NTSC or PAL	+25°C		0.1		degrees
Aperture Delay Time		+25°C		2		ns
Aperture Jitter		+25°C		7		ps rms
Overvoltage Recovery Time(5)	1.5x Full Scale Input	+25°C		2		ns

NOTE: (1) dBFS refers to dB below Full Scale. (2) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) Refer to Timing Diagram footnotes for the f_{IN} = 500kHz differential linearity performance condition. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (5) No "rollover" of bits.

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS800U MIN	ADS800U TYP	ADS800U MAX	UNITS
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC		
Logic Levels	Logic "LO", C_L = 15pF max	Full	0		0.4	V
	Logic "HI", C_L = 15pF max	Full	+2.5		$+V_S$	V
3-State Enable Time				20	40	ns
3-State Disable Time		Full		2	10	ns
POWER SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		78	93	mA
	Operating	Full		78	97	mA
Power Consumption	Operating	+25°C		390	465	mW
	Operating	Full		390	485	mW
Thermal Resistance, θ_{JA}						
28-Pin SOIC				75		°C/W

ORDERING INFORMATION

ADS800 (U)

Basic Model Number

Package Code

U: 28-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS800U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V Max
External Bottom Reference Voltage (REFB)	+1.1V Min

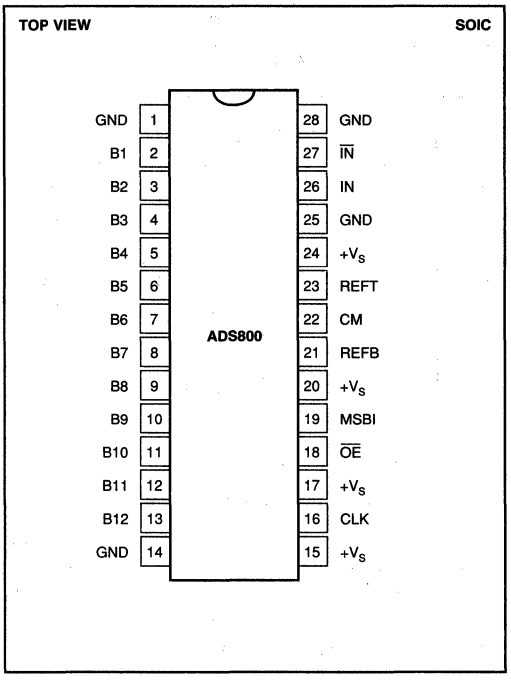
NOTE: (1) Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

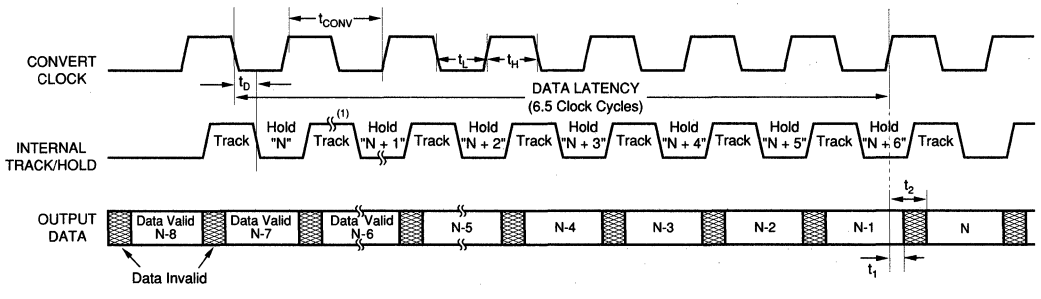
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10
12	B11	Bit 11
13	B12	Bit 12, Least Significant Bit
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM

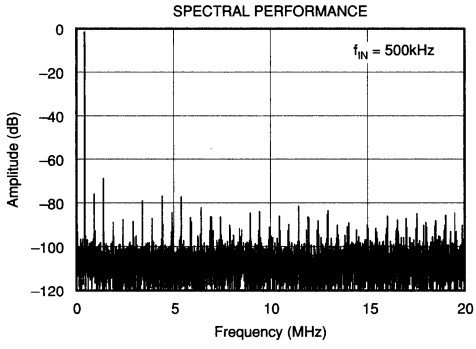


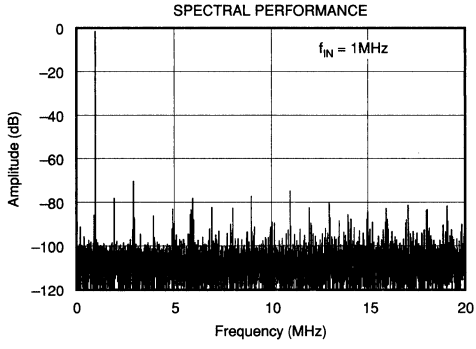
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse Low	12	12.5		ns
t_H	Clock Pulse High	12(2)	12.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

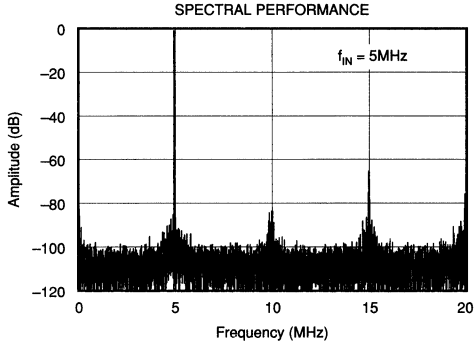
NOTE: (1) " § " indicates the portion of the waveform that will stretch out at slower sample rates. (2) t_H must be 13ns minimum if no missing codes is desired only for the conditions of t_{CONV} ≤28ns and f_{IN} <2MHz. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

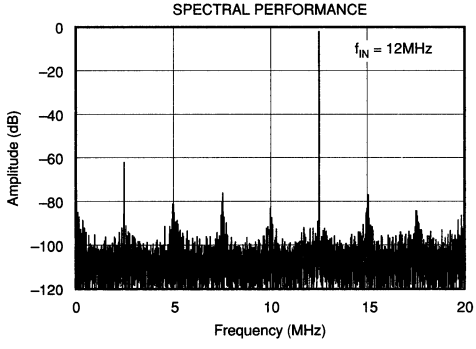
TYPICAL PERFORMANCE CURVES

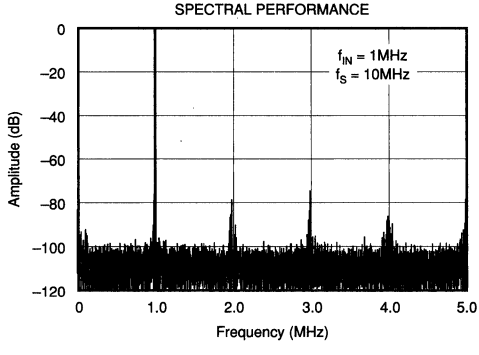
At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

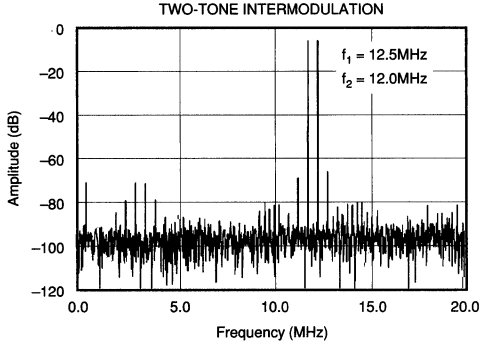








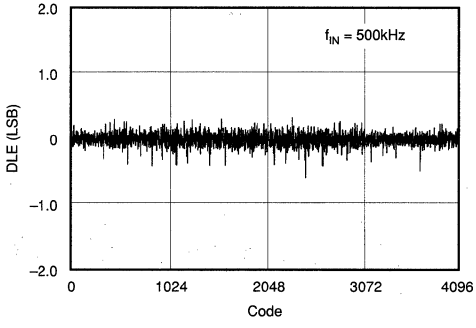




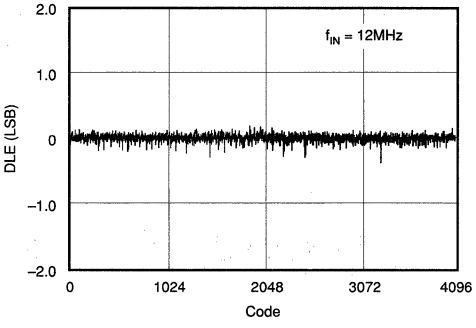
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

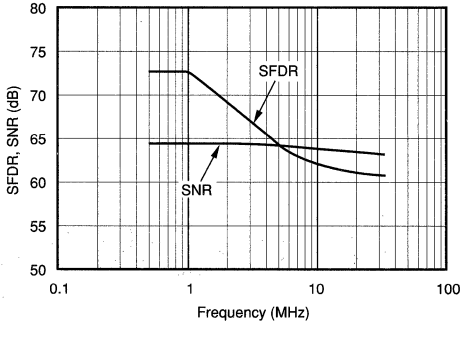
DIFFERENTIAL LINEARITY ERROR



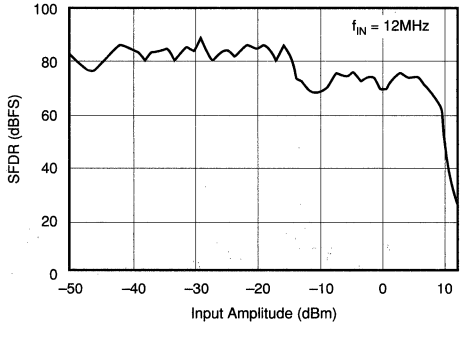
DIFFERENTIAL LINEARITY ERROR



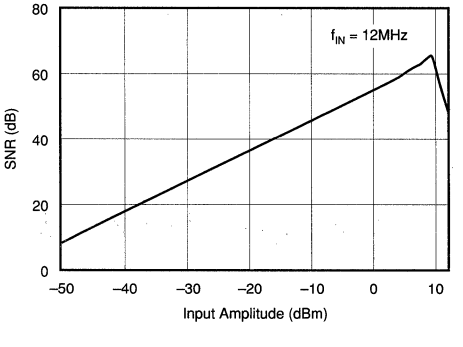
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



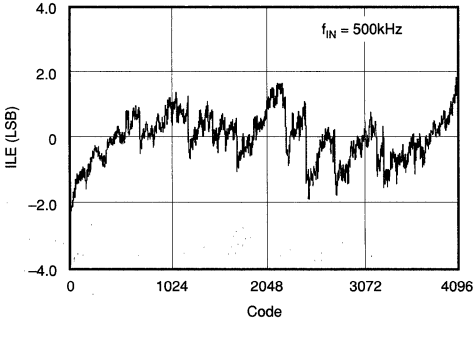
SWEPT POWER SFDR



SWEPT POWER SNR



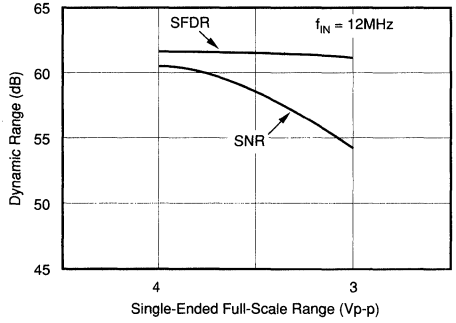
INTEGRAL LINEARITY ERROR



TYPICAL PERFORMANCE CURVES (CONT)

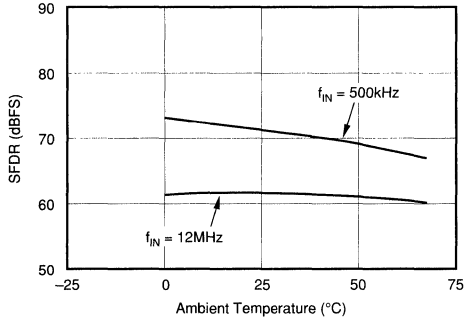
At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

DYNAMIC PERFORMANCE
vs SINGLE-ENDED FULL-SCALE INPUT RANGE

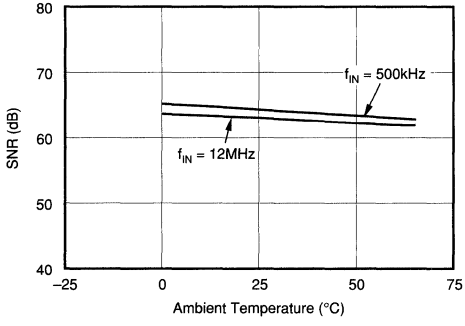


NOTE: $REFT_{EXT}$ varied, REFB is fixed at the internal value of +1.25V.

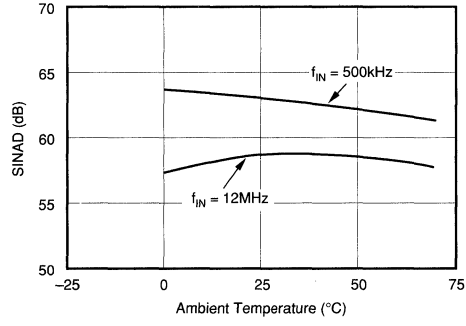
SPURIOUS FREE DYNAMIC RANGE (SFDR)
vs TEMPERATURE



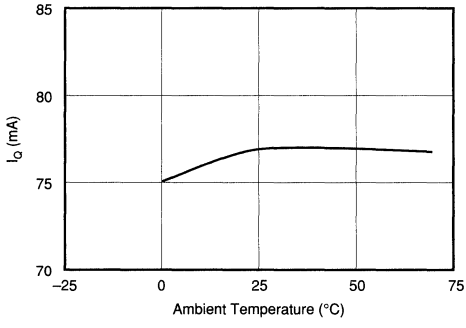
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



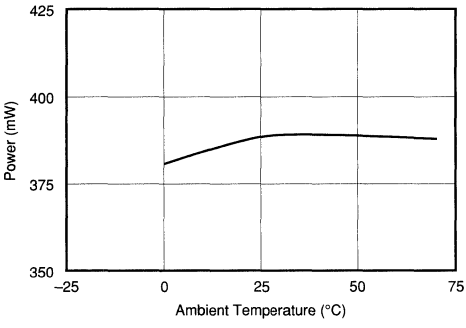
SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



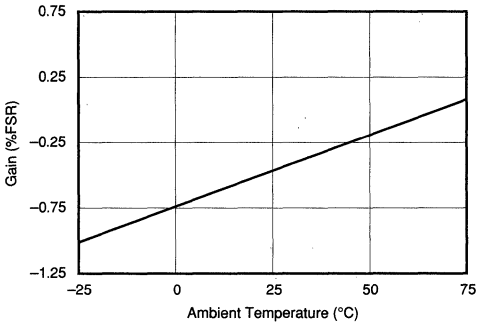
POWER DISSIPATION vs TEMPERATURE



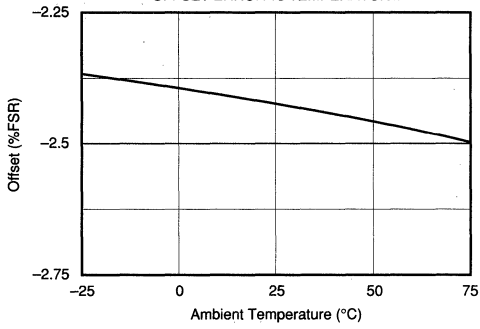
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

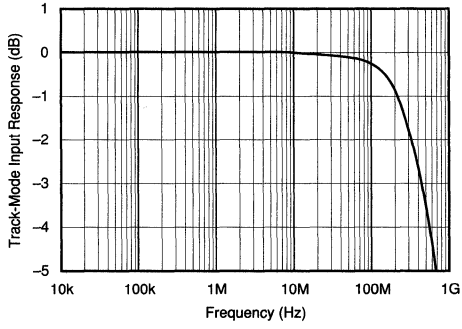
GAIN ERROR vs TEMPERATURE



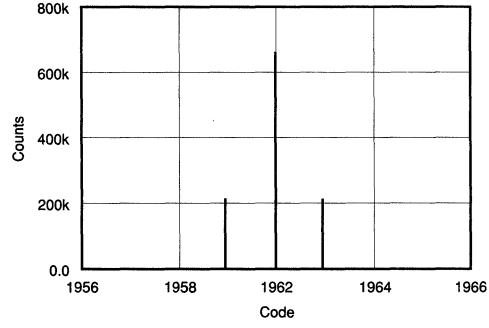
OFFSET ERROR vs TEMPERATURE



TRACK-MODE SMALL-SIGNAL INPUT BANDWIDTH



OUTPUT NOISE HISTOGRAM (INPUT GROUNDED)



THEORY OF OPERATION

The ADS800 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 12-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 11 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

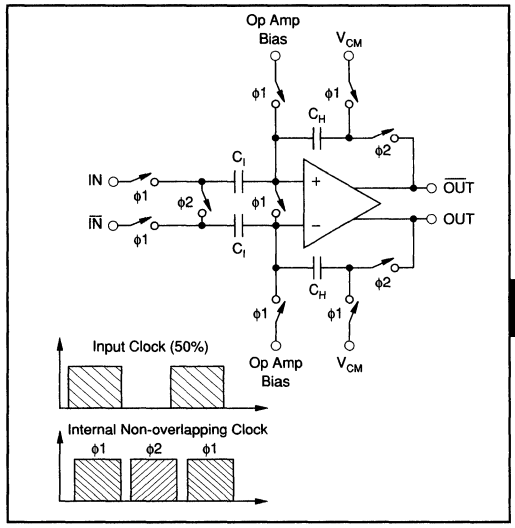


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

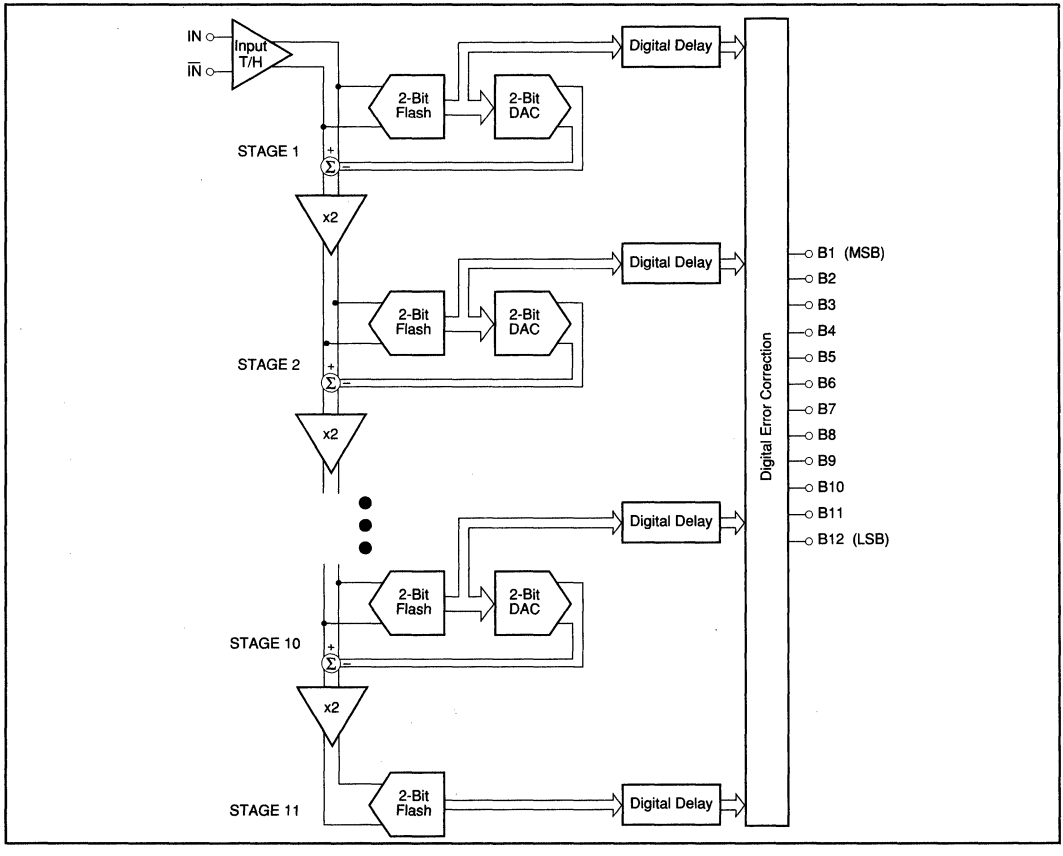


FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS800 excellent differential linearity and guarantees no missing codes at the 12-bit level.

Since there are two pipeline stages per external clock cycle, there is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS800 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS800 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended input, and ADS800 drive circuits, refer to the applications section.

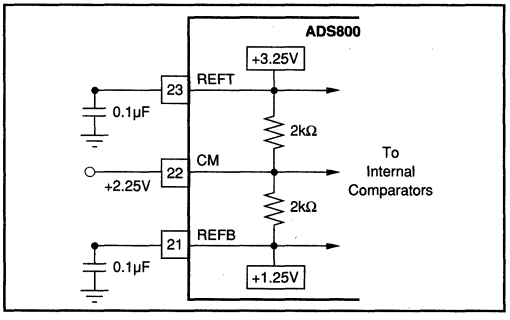


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. Both the rising and falling edges of the externally applied clock control the various interstage conversions in the pipeline. Therefore, the clock signal's jitter, rise/fall times and duty cycle can affect conversion performance.

- Low clock **jitter** is critical to SNR performance in frequency-domain signal environments.
- Clock **rise and fall times** should be as short as possible (<2ns for best performance).
- For most applications, the clock duty should be set to 50%. However, for applications requiring no missing codes, a slight skew in the duty cycle will improve DNL performance for conversion rates >35MHz and input frequencies <2MHz (see Timing Diagram). A possible method for skewing the 50% duty cycle source is shown in Figure 4.

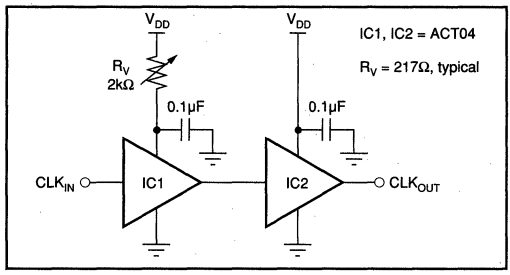


FIGURE 4. Clock Skew Circuit.

DIGITAL OUTPUT DATA

The 12-bit output data is provided at CMOS logic levels. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a logic "HI" voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS800 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

	OUTPUT CODE	
DIFFERENTIAL INPUT[1]	SOB PIN 19 FLOATING or LO	BTC PIN 19 HI
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	111111111111	011111111111
+FS –1LSB	111111111111	011111111111
+FS –2LSB	111111111110	011111111110
+3/4 Full Scale	111000000000	011000000000
+1/2 Full Scale	110000000000	010000000000
+1/4 Full Scale	101000000000	001000000000
+1LSB	100000000001	000000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	100000000000	000000000000
–1LSB	011111111111	111111111111
–1/4 Full Scale	011000000000	111000000000
–1/2 Full Scale	010000000000	110000000000
–3/4 Full Scale	001000000000	101000000000
–FS +1LSB	000000000001	100000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	000000000000	100000000000
Note: In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.		

TABLE I. Coding Table for the ADS800.

APPLICATIONS

DRIVING THE ADS800

The ADS800 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential

output is created on the secondary if the center tap is tied to the common-mode voltage of +2.25V per Figure 5. This transformer-coupled input arrangement provides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{IN}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

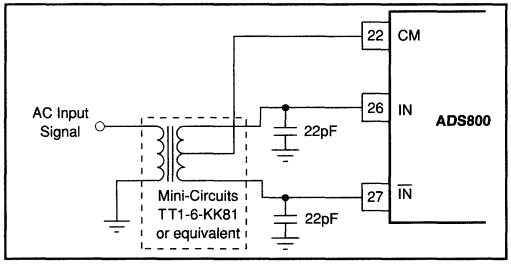


FIGURE 5. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

If the signal needs to be DC coupled to the input of the ADS800, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 6 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to guarantee a low distortion +3.25V output swing. Other amplifiers can be used in place of the OPA642s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier.

The ADS800 can also be configured with a single-ended input full scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage as shown in Figure 7. This configuration will result in increased even-order harmonics, especially at higher input frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

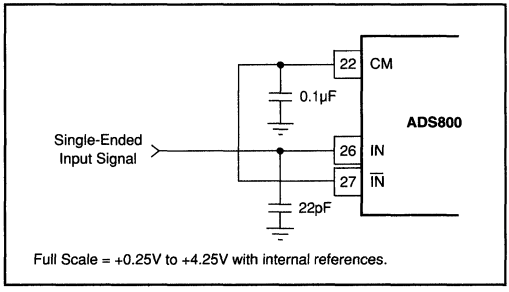


FIGURE 7. Single-Ended Input Connection.

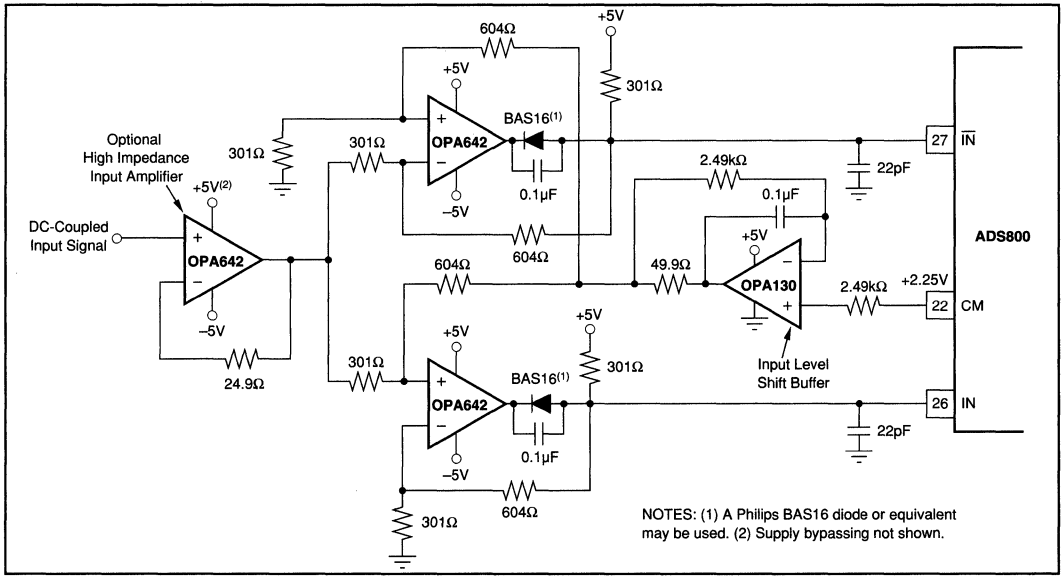


FIGURE 6. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

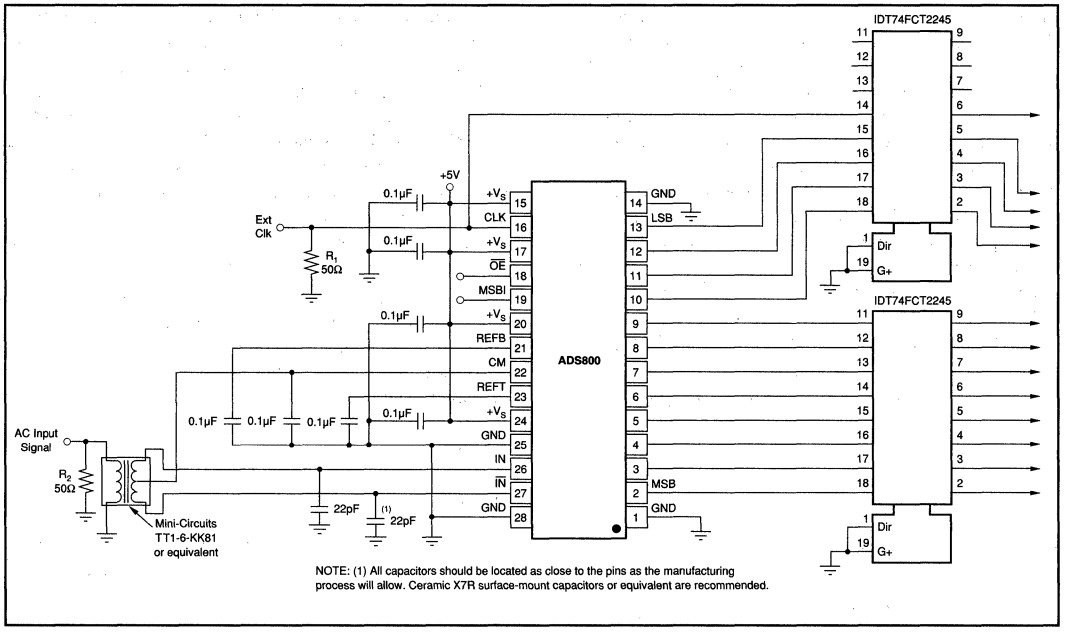


FIGURE 8. ADS800 Interface Schematic with AC-Coupling and External Buffers.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may overridden by external references that have at least 25mA of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full scale input range of the ADS800. Changing the full scale range to a lower value has the benefit of easing the swing requirements of external input drive amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V and the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V and the difference between the external references are greater than or equal to 1.5V.

For the differential configuration, the full scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \bullet (REFT_{EXT} - REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the typical performance curves for expected performance vs full scale input range.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS800 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS800 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS800. Using a signal amplitude slightly lower than full scale will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

BURR-BROWN®

ADS801

SpeedPlus™ 12-Bit, 25MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- NO MISSING CODES
- LOW POWER: 270mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY
- 3-STATE OUTPUTS
- PACKAGE: 28-Pin SOIC

APPLICATIONS

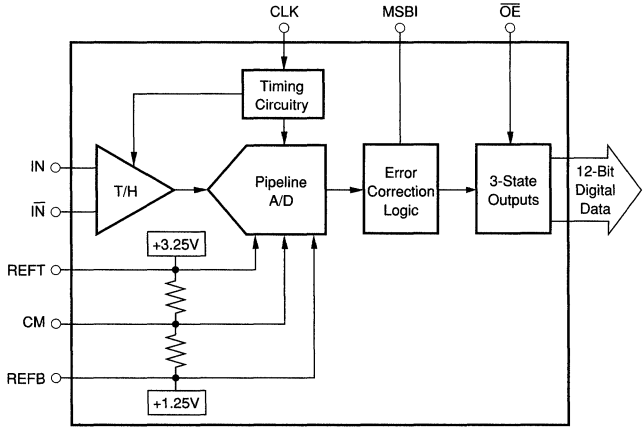
- IF AND BASEBAND DIGITIZATION
- DIGITAL COMMUNICATIONS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING
- GAMMA CAMERAS

DESCRIPTION

The ADS801 is a low power, monolithic 12-bit, 25MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference, and three-state outputs. It operates from a single +5V power supply and can be configured to accept either single-ended or differential input signals.

The ADS801 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications, instrumentation and video applications.

This high performance A/D converter is specified over temperature for AC and DC performance at a 25MHz sampling rate. The ADS801 is available in a 28-pin SOIC package.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS801U MIN	ADS801U TYP	ADS801U MAX	UNITS
Resolution				12 Guaranteed		Bits
Specified Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full Scale Input Range	Both Inputs, 180° Out of Phase		+1.25		+3.25	V
Common-Mode Voltage				+2.25		V
Analog Input Bandwidth (–3dB)						
Small Signal	–20dBFS[1] Input	+25°C		400		MHz
Full Power	0dBFS Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY[2]						
Gain Error		+25°C		±0.6	±1.5	%
		Full		±1.0	±2.5	%
Gain Tempco				±85		ppm/°C
Power Supply Rejection of Gain	Delta +V_S = ±5%	+25°C		0.03	0.15	%FSR/%
Input Offset Error		+25°C		±2.0	±2.5	%
		Full		±2.1	±3.0	%FSR/%
Power Supply Rejection of Offset	Delta +V_S = ±5%	+25°C		0.05	0.15	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		25M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error						
f = 500kHz		+25°C		±0.3	±1.0	LSB
		0°C to +85°C		±0.4	±1.0	LSB
f = 10MHz		+25°C		±0.3	±1.0	LSB
		0°C to +85°C		±0.4	±1.0	LSB
No Missing Codes		0°C to +85°C		Guaranteed		LSB
Integral Linearity Error at f = 500kHz		Full		±1.7		LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	63	77		dBFS
		Full	62	73		dBFS
f = 10MHz (–1dBFS input)		+25°C	57	61		dBFS
		Full	55	61		dBFS
Two-Tone Intermodulation Distortion (IMD)[3]						
f = 4.4MHz and 4.5MHz (–7dBFS each tone)		+25°C		–64		dBc
		Full		–63		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	64	66		dB
		Full	61	64		dB
f = 10MHz (–1dBFS input)		+25°C	62	65		dB
		Full	58	64		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	63	66		dB
		Full	60	63		dB
f = 10MHz (–1dBFS input)		+25°C	56	59		dB
		Full	54	58		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error	NTSC or PAL	+25°C		0.1		degrees
Aperture Delay Time		+25°C		2		ns
Aperture Jitter		+25°C		7		ps rms
Overvoltage Recovery Time[4]	1.5x Full Scale Input	+25°C		2		ns

NOTE: (1) dBFS refers to dB below Full Scale. (2) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (4) No "rollover" of bits.

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS801U MIN	ADS801U TYP	ADS801U MAX	UNITS
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC		
Logic Levels	Logic "LO", C_L = 15pF max	Full	0		0.4	V
	Logic "HI", C_L = 15pF max	Full	+2.5		$+V_S$	V
3-State Enable Time				20	40	ns
3-State Disable Time		Full		2	10	ns
POWER SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		54	65	mA
	Operating	Full		54	68	mA
Power Consumption	Operating	+25°C		270	325	mW
	Operating	Full		270	340	mW
Thermal Resistance, θ_{JA}						
28-Pin SOIC				75		°C/W

ORDERING INFORMATION

ADS801 (U)

Basic Model Number

Package Code

U: 28-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS801U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V Max
External Bottom Reference Voltage (REFB)	+1.1V Min

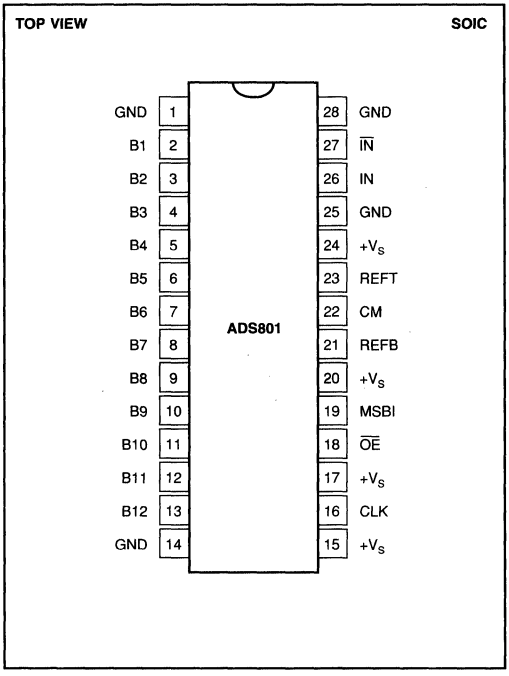
NOTE: Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

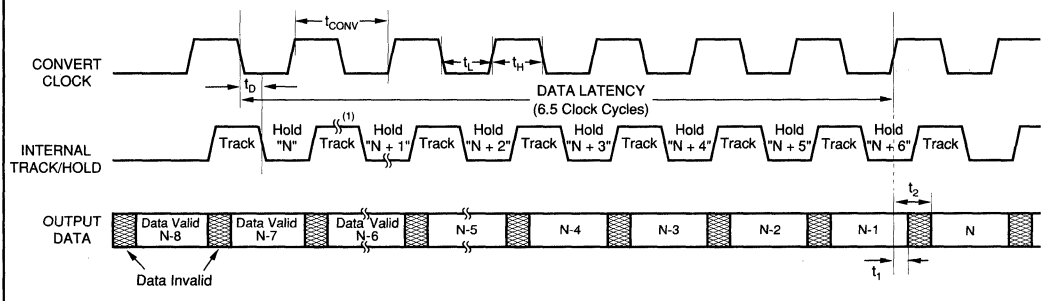
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10
12	B11	Bit 11
13	B12	Bit 12, Least Significant Bit
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM



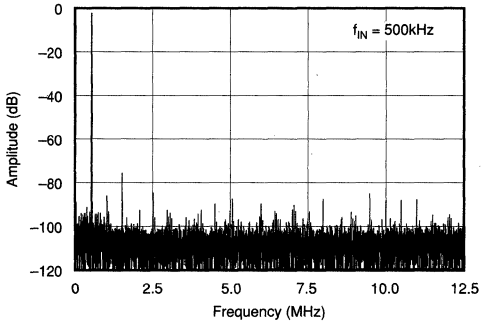
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	40		100µs	ns
t_L	Clock Pulse Low	19	20		ns
t_H	Clock Pulse High	19	20		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

NOTE: (1) " ≬ " indicates the portion of the waveform that will stretch out at slower sample rates.

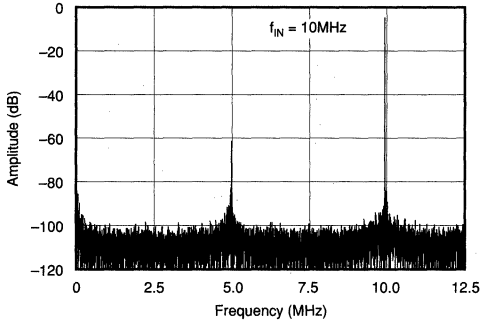
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

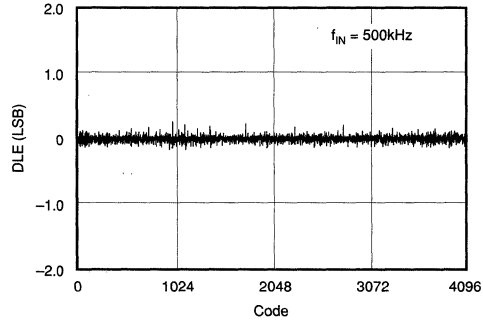
SPECTRAL PERFORMANCE



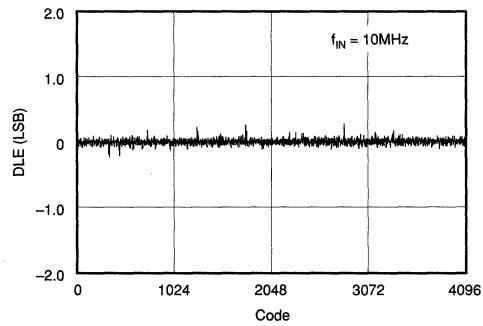
SPECTRAL PERFORMANCE



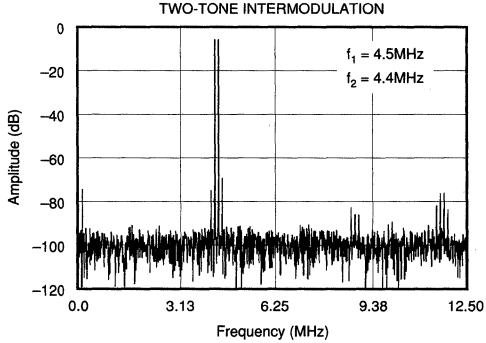
DIFFERENTIAL LINEARITY ERROR



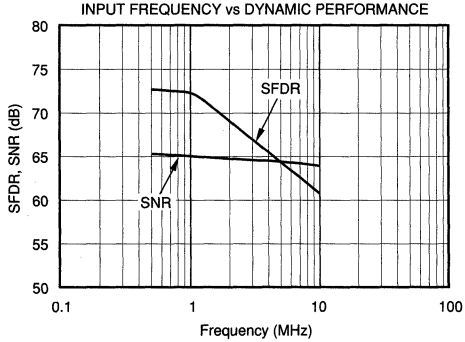
DIFFERENTIAL LINEARITY ERROR



TWO-TONE INTERMODULATION



INPUT FREQUENCY vs DYNAMIC PERFORMANCE



TYPICAL PERFORMANCE CURVES (CONT)

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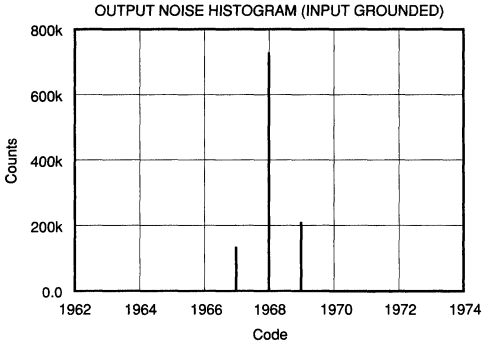
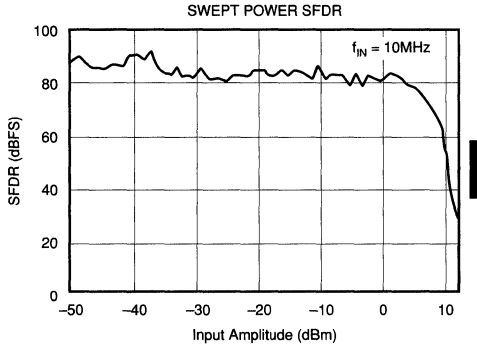
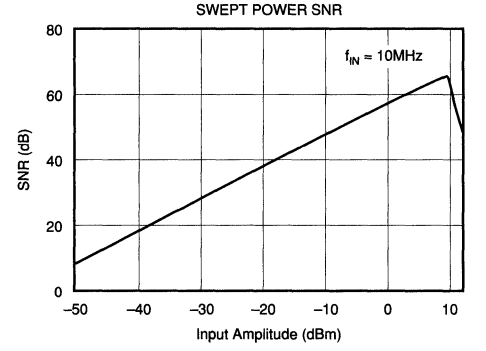
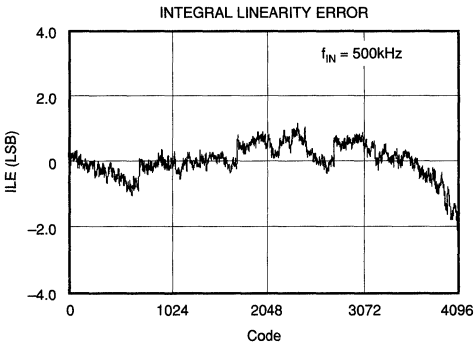
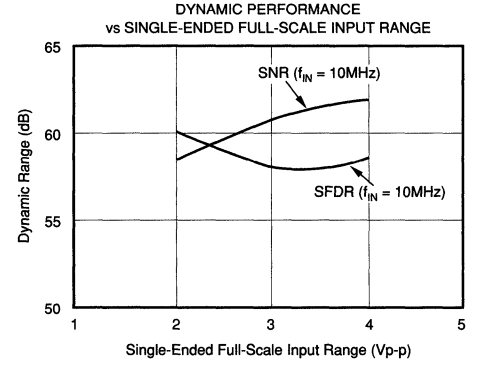
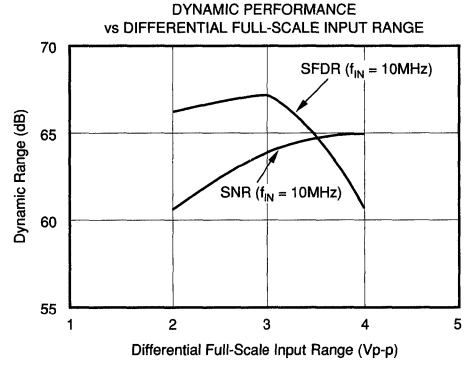








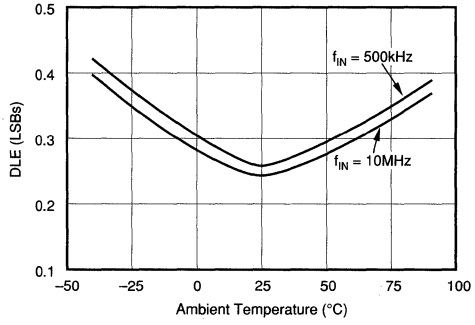




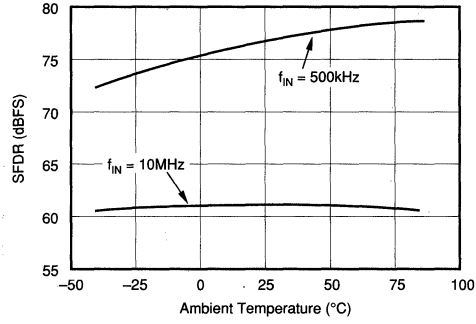
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

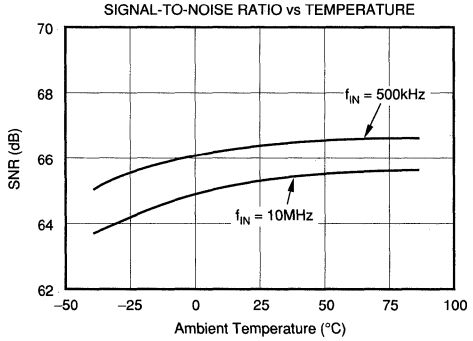
DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



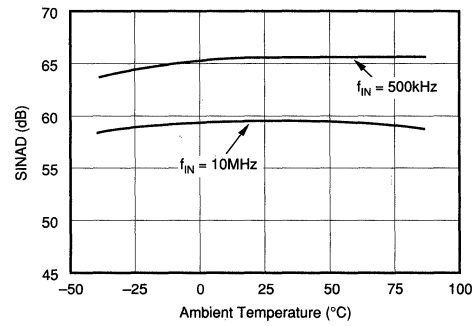
SPURIOUS FREE DYNAMIC RANGE (SFDR) vs TEMPERATURE



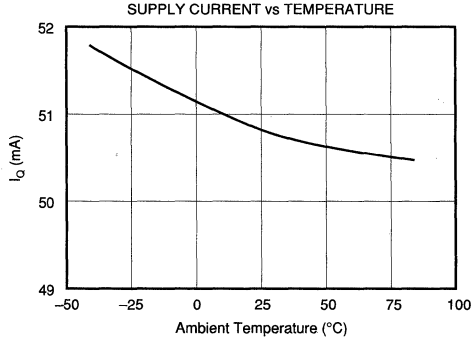
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



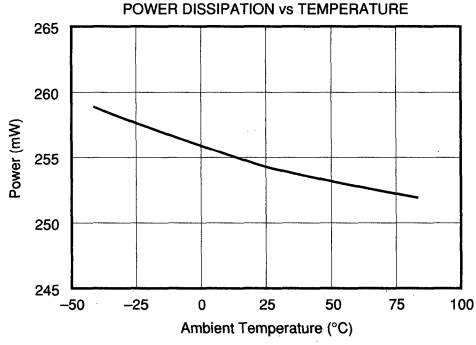
SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE

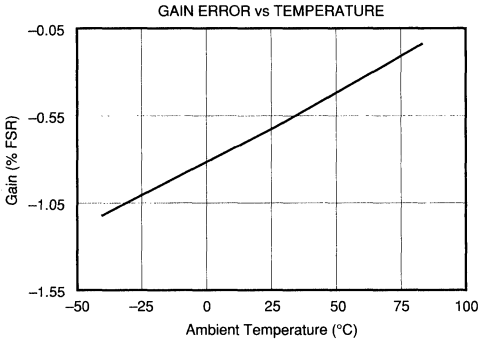


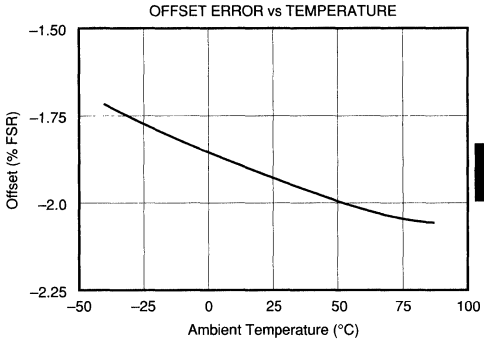
POWER DISSIPATION vs TEMPERATURE

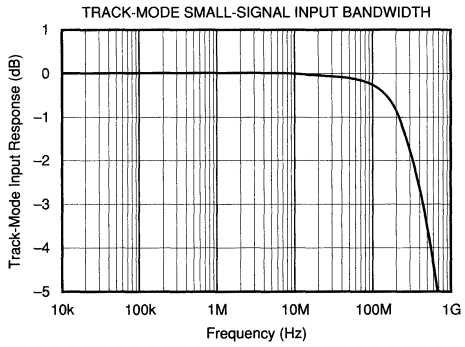


TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 25MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.







THEORY OF OPERATION

The ADS801 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 12-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which is a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 11 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

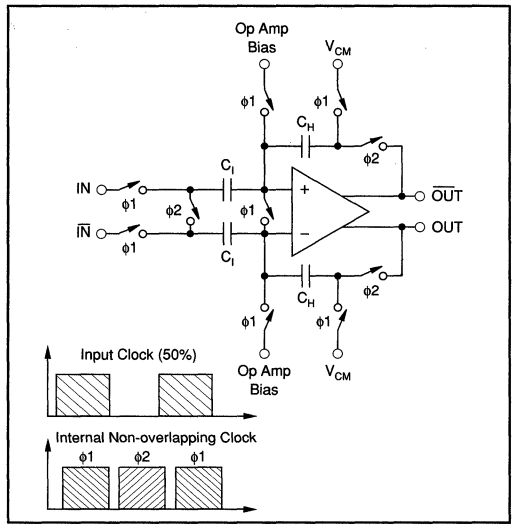


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

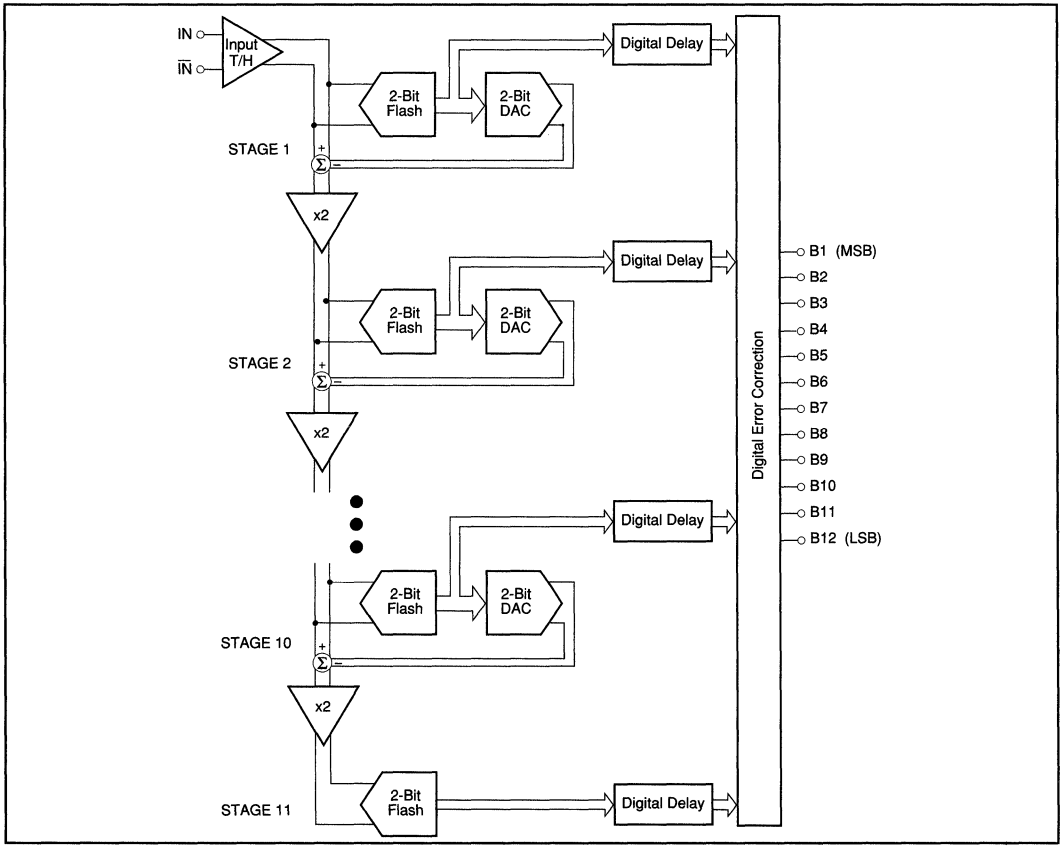


FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS801 excellent differential linearity and guarantees no missing codes at the 12-bit level.

Since there are two pipeline stages per external clock cycle, there is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS801 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS801 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended input, and ADS801 drive circuits, refer to the applications section.

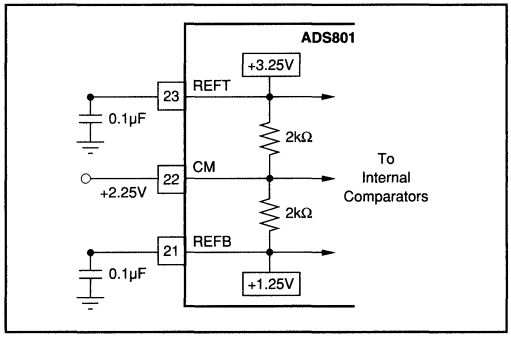


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. The rising and falling edges of the externally applied convert command clock control the various interstage conversions in the pipeline. Therefore, the duty cycle of the clock should be held at 50% with low jitter and fast rise/fall times of 2ns or less. This is particularly important when digitizing a high frequency input and operating at the maximum sample rate. Deviation from a 50% duty cycle will effectively shorten some of the interstage settling times, thus degrading the SNR and DNL performance.

DIGITAL OUTPUT DATA

The 12-bit output data is provided at CMOS logic levels. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a logic "HI" voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS801 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

DIFFERENTIAL INPUT[1]	OUTPUT CODE: SOB PIN 19 FLOATING or LO	OUTPUT CODE: BTC PIN 19 HI
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	111111111111	011111111111
+FS –1LSB	111111111111	011111111111
+FS –2LSB	111111111110	011111111110
+3/4 Full Scale	111000000000	011000000000
+1/2 Full Scale	110000000000	010000000000
+1/4 Full Scale	101000000000	001000000000
+1LSB	100000000001	000000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	100000000000	000000000000
–1LSB	011111111111	111111111111
–1/4 Full Scale	011000000000	111000000000
–1/2 Full Scale	010000000000	110000000000
–3/4 Full Scale	001000000000	101000000000
–FS +1LSB	000000000001	100000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	000000000000	100000000000

Note: In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.

TABLE I. Coding Table for the ADS801.

APPLICATIONS

DRIVING THE ADS801

The ADS801 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode voltage of +2.25V per Figure 4. This transformer-coupled input arrangement pro-

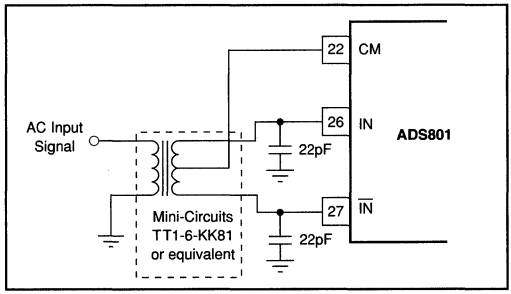


FIGURE 4. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

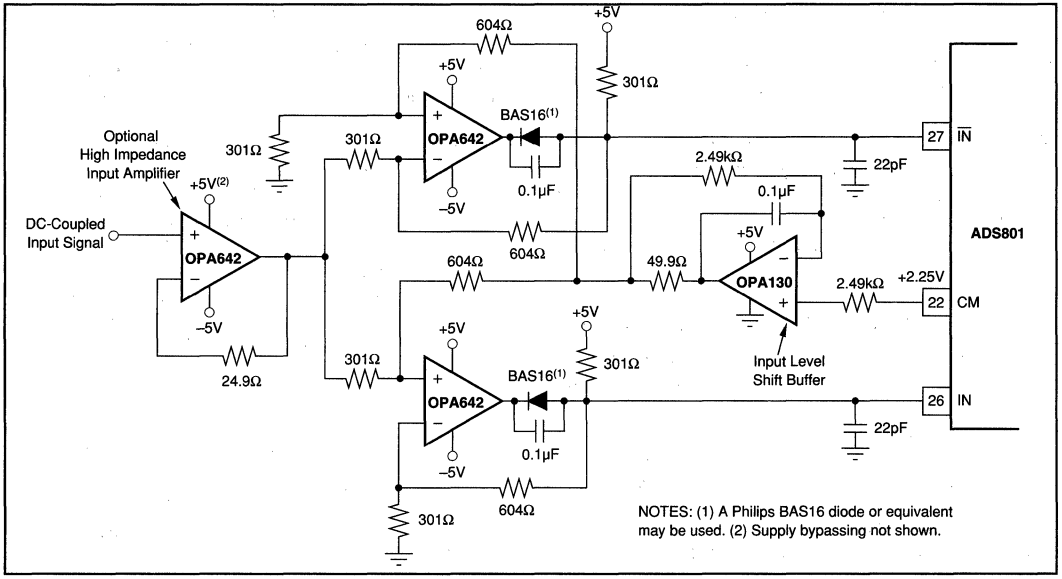


FIGURE 5. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

vides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{\text{IN}}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

If the signal needs to be DC coupled to the input of the ADS801, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 5 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to guarantee a low distortion +3.25V output swing. Other amplifiers can be used in place of the OPA642s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier.

The ADS801 can also be configured with a single-ended input full scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage as shown in Figure 6. This configuration will result in increased even-order harmonics, especially at higher input

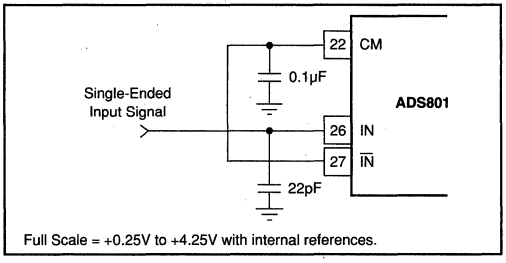


FIGURE 6. Single-Ended Input Connection.

frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may overridden by external references that have at least 25mA of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full scale input range of the ADS801. Changing the full scale range to a lower value has the benefit of easing the swing requirements of external input amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V and the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V and the difference between the external references are greater than or equal to 1.5V.

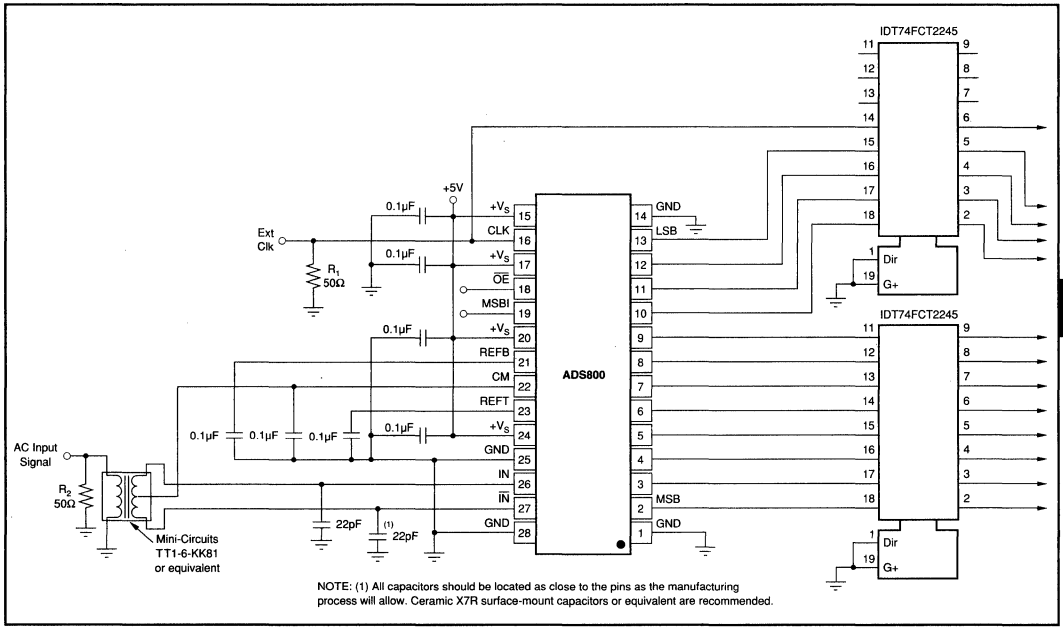


FIGURE 7. ADS801 Interface Schematic with AC-Coupling and External Buffers.

For the differential configuration, the full scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \cdot (REFT_{EXT} - REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the typical performance curves for expected performance vs full scale input range.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS801 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS801 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS801. Using a signal amplitude slightly lower than full scale will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

BURR-BROWN®

ADS802

SpeedPLUS™ 12-Bit, 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- NO MISSING CODES
- LOW POWER: 250mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY
- 3-STATE OUTPUTS

APPLICATIONS

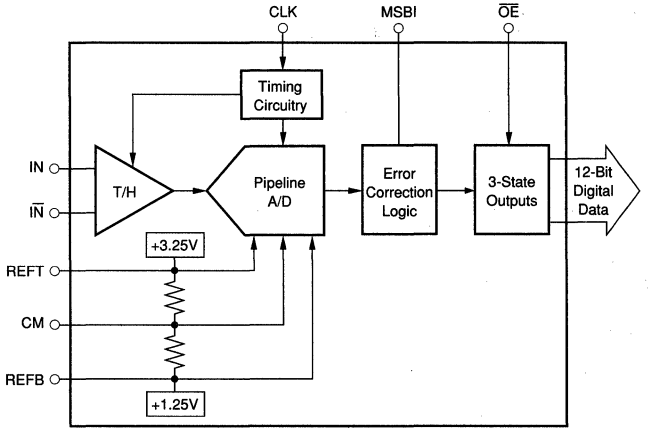
- IF AND BASEBAND DIGITIZATION
- DATA ACQUISITION CARDS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING
- GAMMA CAMERAS

DESCRIPTION

The ADS802 is a low power, monolithic 12-bit, 10MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference and three-state outputs. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS802 employs digital error correction in order to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR, and high oversampling capability give it the extra margin needed for telecommunications, test instrumentation and video applications.

This high performance A/D converter is specified for AC and DC performance at a 10MHz sampling rate. The ADS802 is available in a 28-pin SOIC package.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = +5V, and Sampling Rate = 10MHz, with a 50% duty cycle clock having 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS802U MIN	ADS802U TYP	ADS802U MAX	UNITS
Resolution				12 Guaranteed		Bits
Specified Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full Scale Input Range	Both Inputs		+1.25		+3.25	V
Common-Mode Voltage				+2.25		V
Analog Input Bandwidth (–3dB)						
Small Signal	–20dBFS(1) Input	+25°C		400		MHz
Full Power	0dBFS Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY(2)						
Gain Error		+25°C		±0.6	±1.5	%
		Full		±1.0	±2.5	%
Gain Tempco				±85		ppm/°C
Power Supply Rejection of Gain	Delta $+V_S$ = ±5%	+25°C		0.03	0.1	%FSR/%
Input Offset Error		+25°C		±2.0	±2.5	%
		Full		±2.1	±3.0	%FSR/%
Power Supply Rejection of Offset	Delta $+V_S$ = ±5%	+25°C		0.05	0.1	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		10M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error						
f = 500kHz		+25°C		±0.3	±1.0	LSB
		0°C to +85°C		±0.4	±1.0	LSB
f = 5MHz		+25°C		±0.4	±1.0	LSB
		0°C to +85°C		±0.4	±1.0	LSB
No Missing Codes		0°C to +85°C		Guaranteed		LSB
Integral Linearity Error at f = 500kHz	Best Fit	0°C to +85°C		±1.7	±2.75	LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	67	77		dBFS
		Full	66	75		dBFS
f = 5MHz (–1dBFS input)		+25°C	63	67		dBFS
		Full	62	66		dBFS
Two-Tone Intermodulation Distortion (IMD)(3)						
f = 4.4MHz and 4.5MHz (–7dBFS each tone)		+25°C		–65		dBc
		Full		–64		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	65	67		dB
		Full	64	67		dB
f = 5MHz (–1dBFS input)		+25°C	64	66		dB
		Full	62	66		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	63	66		dB
		Full	61	65		dB
f = 5MHz (–1dBFS input)		+25°C	61	63		dB
		Full	60	62		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error	NTSC or PAL	+25°C		0.1		degrees
Aperture Delay Time		+25°C		2		ns
Aperture Jitter		+25°C		7		ps rms
Overvoltage Recovery Time(4)	1.5x Full Scale Input	+25°C		2		ns

NOTE: (1) dBFS refers to dB below Full Scale. (2). Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 7dB lower. (4) No "rollover" of bits.

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, and Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS802U MIN	ADS802U TYP	ADS802U MAX	UNITS
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC		
Logic Levels	Logic "LO"	Full	0		0.4	V
	Logic "HI"	Full	2.0		$+V_S$	V
3-State Enable Time		Full		20	40	ns
3-State Disable Time		Full		2	10	ns
POWER SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		51	62	mA
	Operating	Full		52	62	mA
Power Consumption	Operating	+25°C		250	310	mW
	Operating	Full		260	310	mW
Thermal Resistance, θ_{JA}						
28-Pin SOIC				75		°C/W

ORDERING INFORMATION

ADS802 (U)

Basic Model Number

Package Code

U: 28-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS802U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V Max
External Bottom Reference Voltage (REFB)	+1.1V Min

NOTE: Stresses above these ratings may permanently damage the device.

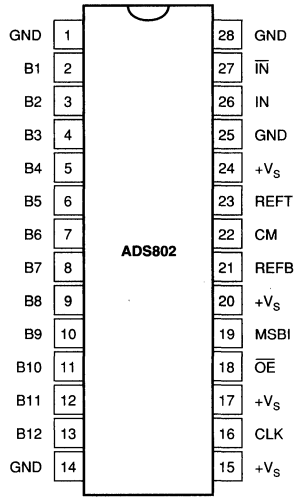
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN CONFIGURATION

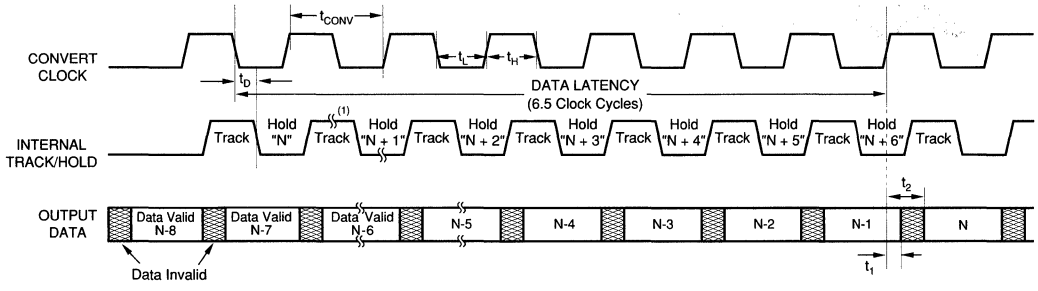
TOP VIEW — SOIC



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10
12	B11	Bit 11
13	B12	Bit 12, Least Significant Bit
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM



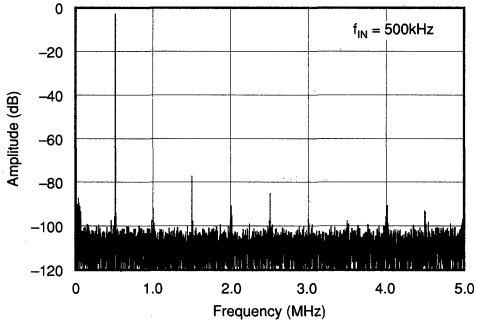
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	100		100µs	ns
t_L	Clock Pulse Low	48	50		ns
t_H	Clock Pulse High	48	50		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

NOTE: (1) "≬" indicates the portion of the waveform that will stretch out at slower sample rates.

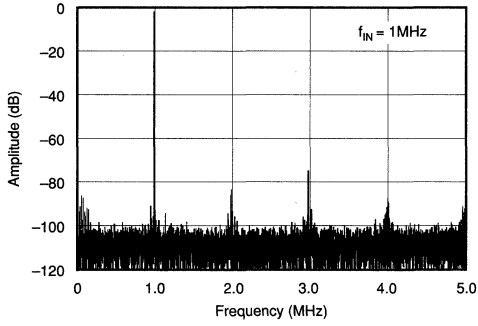
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, Sampling Rate = 10MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

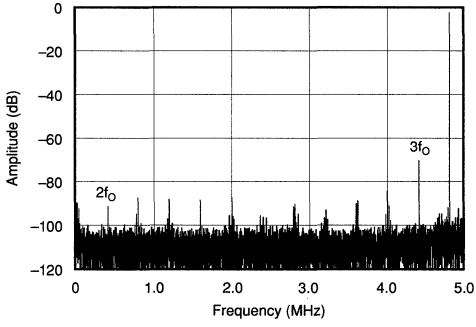
SPECTRAL PERFORMANCE



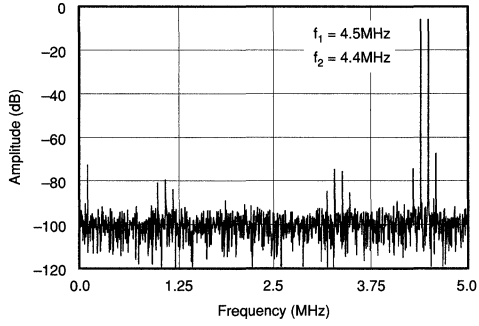
SPECTRAL PERFORMANCE



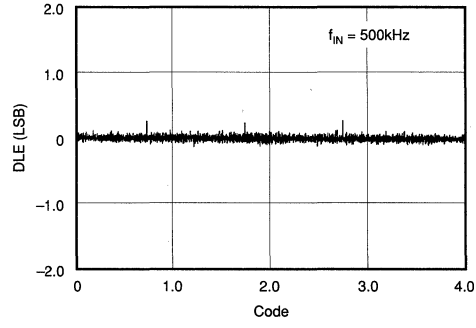
SPECTRAL PERFORMANCE



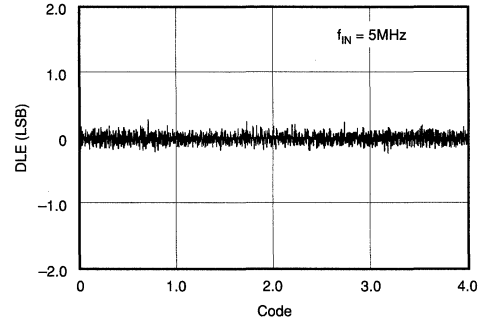
TWO-TONE INTERMODULATION



DIFFERENTIAL LINEARITY ERROR



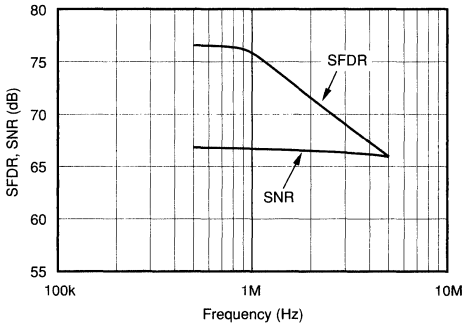
DIFFERENTIAL LINEARITY ERROR



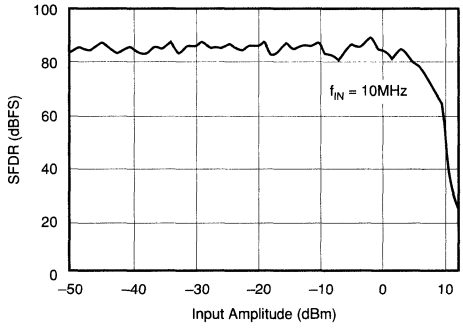
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 10MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

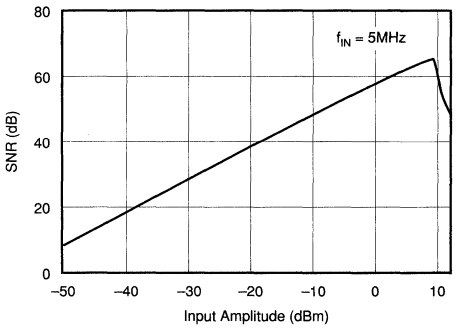
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



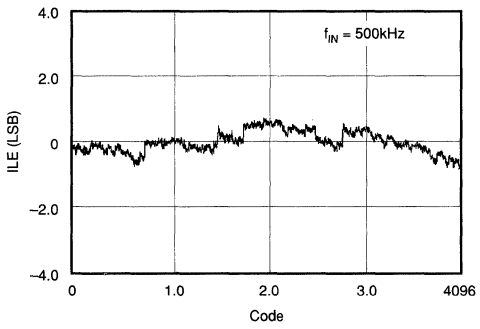
SWEPT POWER SFDR



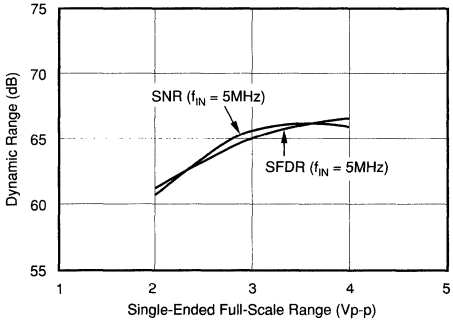
SWEPT POWER SNR



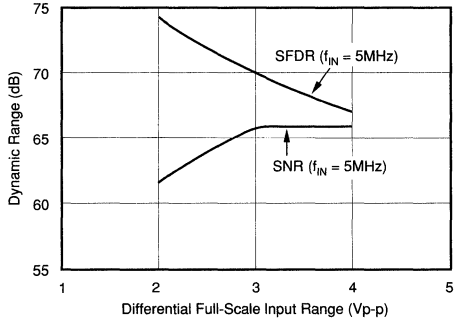
INTEGRAL LINEARITY ERROR



DYNAMIC PERFORMANCE
vs SINGLE-ENDED FULL-SCALE INPUT RANGE



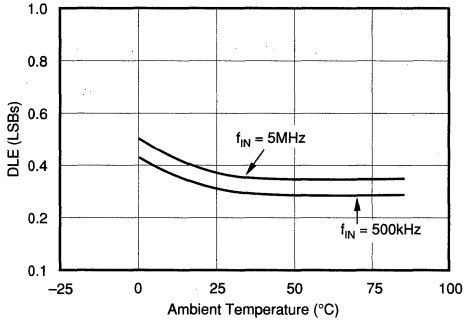
DYNAMIC PERFORMANCE
vs DIFFERENTIAL FULL-SCALE INPUT RANGE



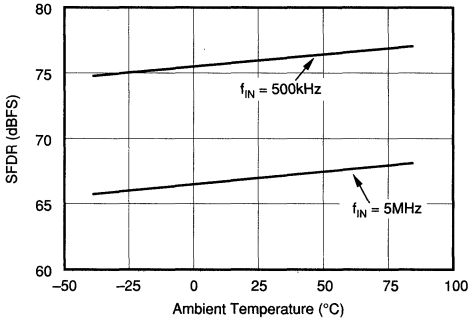
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 10MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

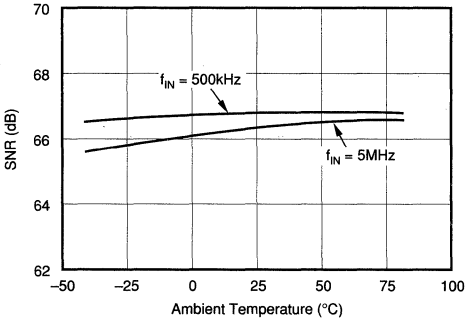
DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



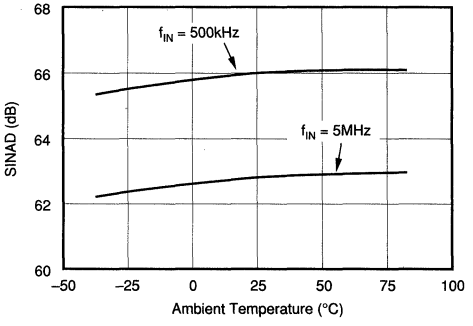
SPURIOUS FREE DYNAMIC RANGE (SFDR) vs TEMPERATURE



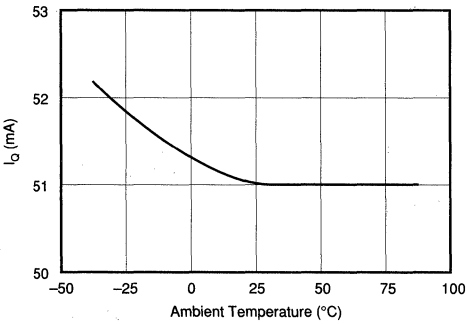
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



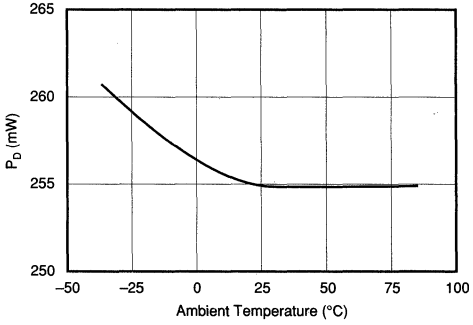
SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE

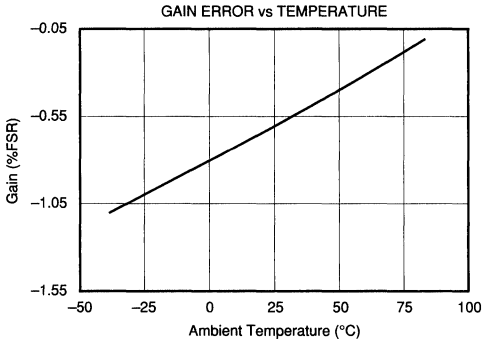


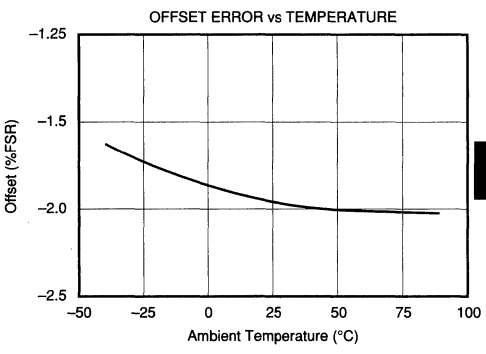
POWER DISSIPATION vs TEMPERATURE

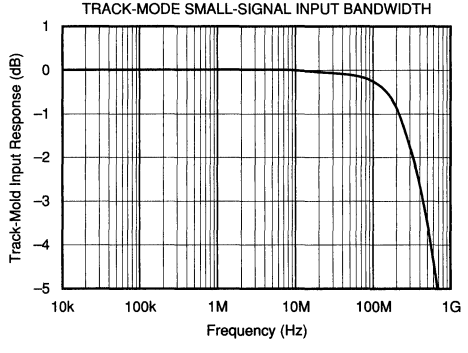


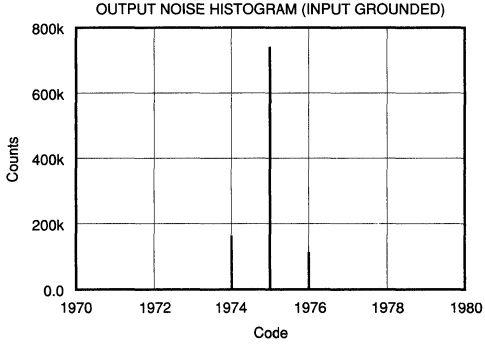
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 10MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.









THEORY OF OPERATION

The ADS802 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 12-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 11 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

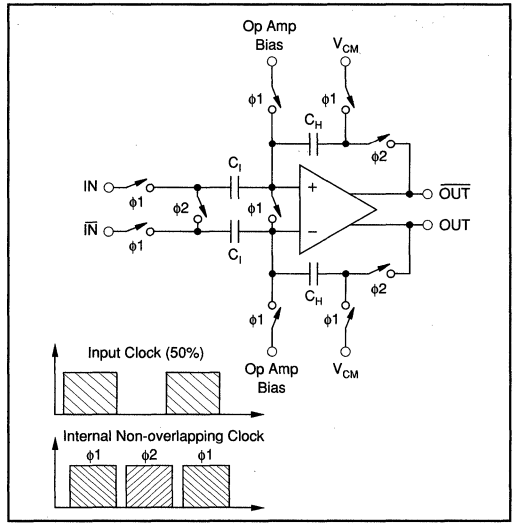


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

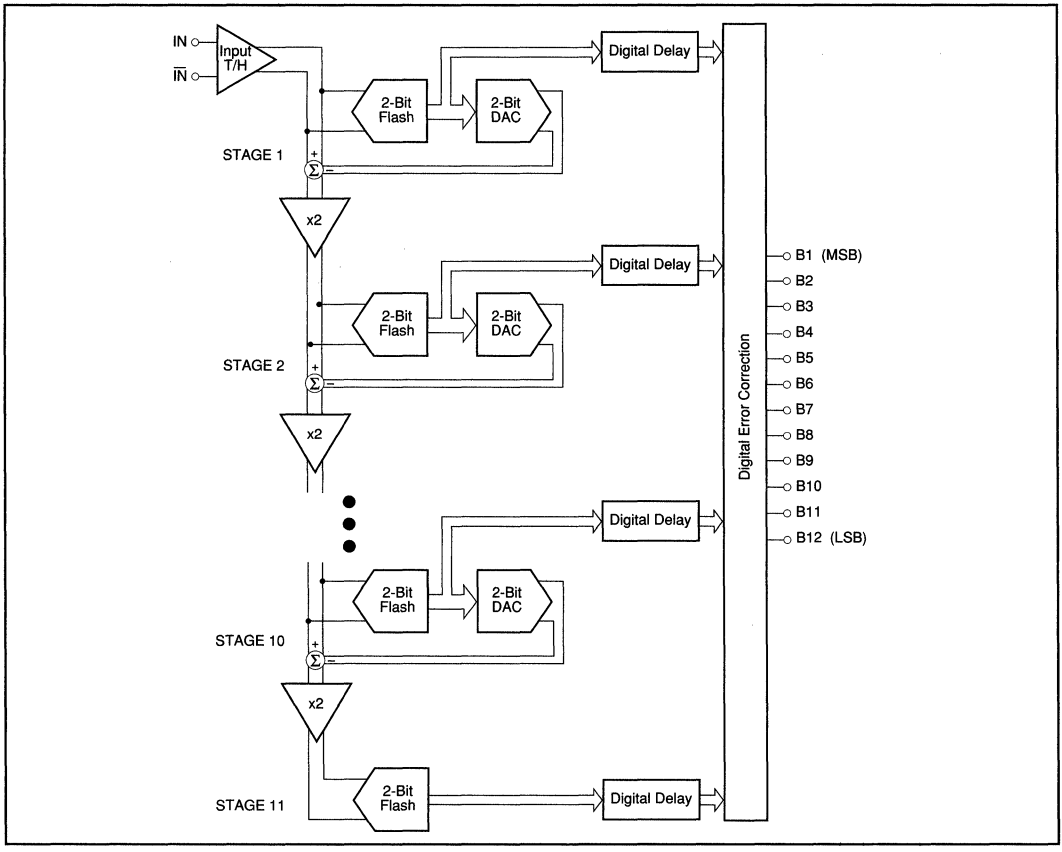


FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS802 excellent differential linearity and guarantees no missing codes at the 12-bit level.

Since there are two pipeline stages per external clock cycle, there is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS802 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS802 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended input, and ADS802 drive circuits, refer to the applications section.

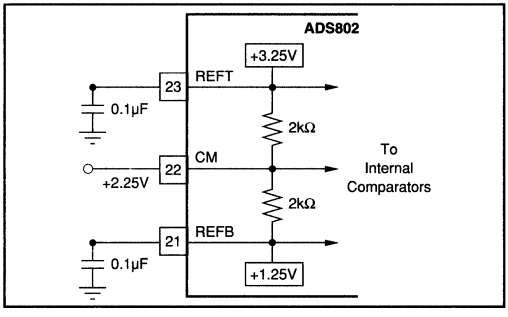


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. The rising and falling edges of the externally applied convert command clock control the various interstage conversions in the pipeline. Therefore, the duty cycle of the clock should be held at 50% with low jitter and fast rise/fall times of 2ns or less. This is particularly important when digitizing a high frequency input and operating at the maximum sample rate. Deviation from a 50% duty cycle will effectively shorten some of the interstage settling times, thus degrading the SNR and DNL performance.

DIGITAL OUTPUT DATA

The 12-bit output data is provided at CMOS logic levels. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a logic "HI" voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS802 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

	OUTPUT CODE	
DIFFERENTIAL INPUT[1]	SOB PIN 19 FLOATING or LOW	BTC PIN 19 HIGH
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	111111111111	011111111111
+FS –1LSB	111111111111	011111111111
+FS –2LSB	111111111110	011111111110
+3/4 Full Scale	111000000000	011000000000
+1/2 Full Scale	110000000000	010000000000
+1/4 Full Scale	101000000000	001000000000
+1LSB	100000000001	000000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	100000000000	000000000000
–1LSB	011111111111	111111111111
–1/4 Full Scale	011000000000	111000000000
–1/2 Full Scale	010000000000	110000000000
–3/4 Full Scale	001000000000	101000000000
–FS +1LSB	000000000001	100000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	000000000000	100000000000

Note: In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.

TABLE I. Coding Table for the ADS802.

APPLICATIONS

DRIVING THE ADS802

The ADS802 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode voltage of +2.25V Figure 4. This transformer-coupled input arrangeme

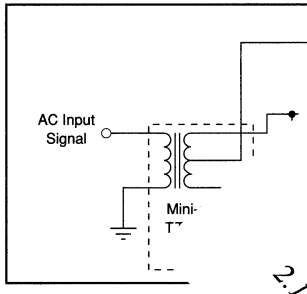


FIGURE 4. AC-Couple
Circuit Using

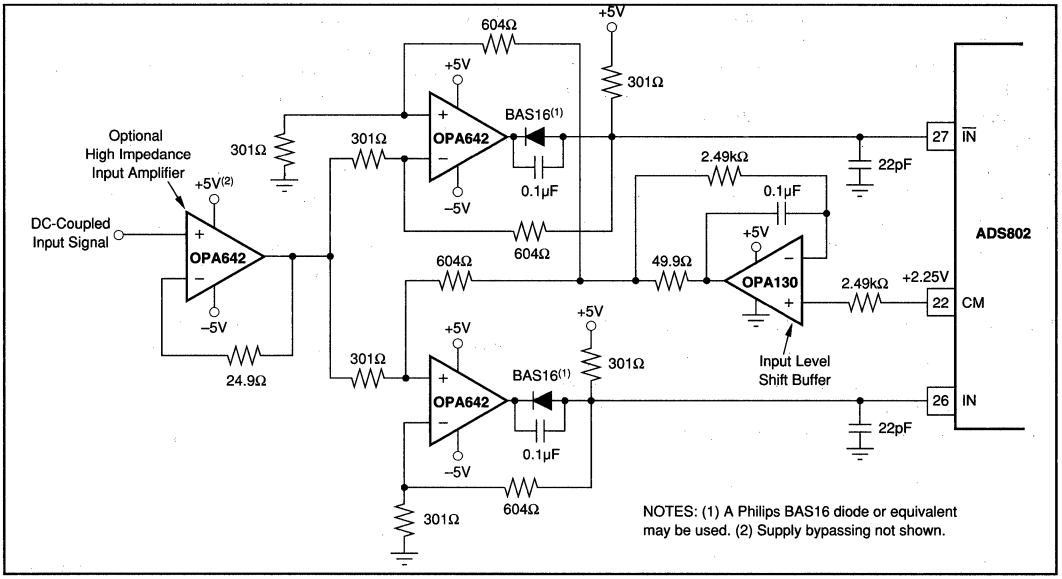


FIGURE 5. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

vides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{IN}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

If the signal needs to be DC coupled to the input of the ADS802, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 5 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to guarantee a low distortion +3.25V output swing. Other amplifiers can be used in place of the OPA642s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a single supply operational amplifier.

ADS802 can also be configured with a single-ended input. The full scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage as in Figure 6. This configuration will result in even-order harmonics, especially at higher input frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

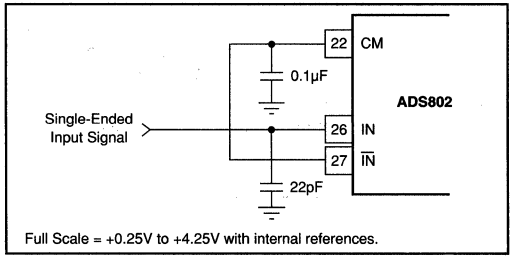


FIGURE 6. Single-Ended Input Connection.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may overridden by external references that have at least 25mA of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full scale input range of the ADS802. Changing the full scale range to a lower value has the benefit of easing the swing requirements of external input drive amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V and the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V and the difference between the external references are greater than or equal to 1.5V.

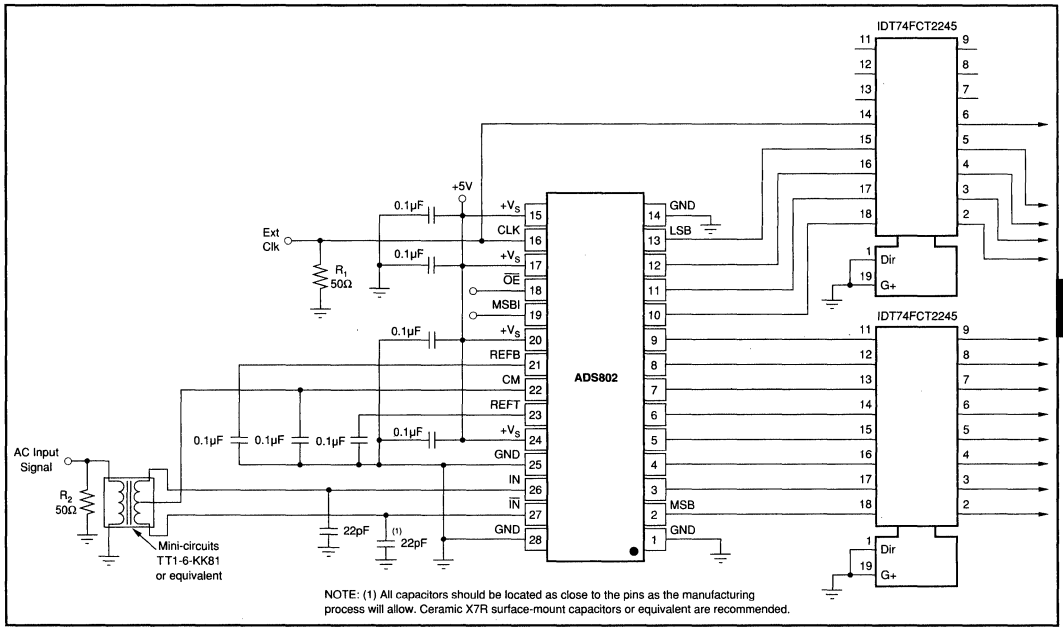


FIGURE 7. ADS802 Interface Schematic with AC-Coupling and External Buffers.

For the differential configuration, the full scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \cdot (REFT_{EXT} - REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the typical performance curves for expected performance vs full scale input range.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS802 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS802 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS802. Using a signal amplitude slightly lower than full scale will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

BURR-BROWN®

ADS820

SpeedPlus™ 10-Bit, 20MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- NO MISSING CODES
- INTERNAL REFERENCE
- LOW DIFFERENTIAL LINEARITY ERROR: 0.2LSB
- LOW POWER: 195mW
- HIGH SNR: 60dB
- WIDEBAND TRACK/HOLD: 65MHz
- 3-STATE OUTPUTS
- PACKAGE: 28-Pin SOIC

APPLICATIONS

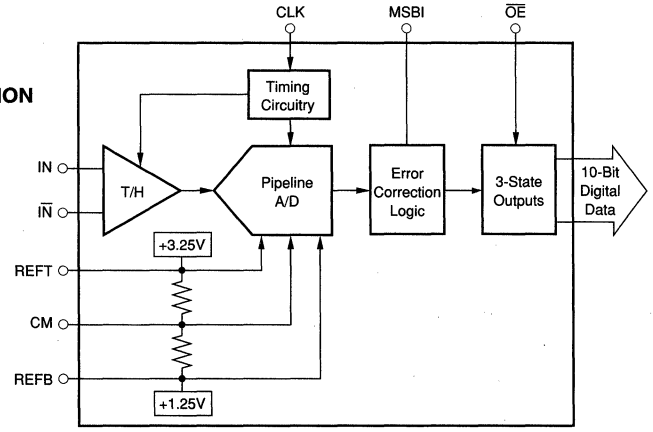
- SET-TOP BOXES
- CABLE MODEMS
- VIDEO DIGITIZING
- CCD IMAGING
  - Camcorders
  - Copiers
  - Scanners
  - Security Cameras
- IF AND BASEBAND DIGITIZATION

DESCRIPTION

The ADS820 is a low power, monolithic 10-bit, 20MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 10-bit quantizer with internal track/hold, reference, and a power down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS820 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high performance converter is specified for AC and DC performance at a 20MHz sampling rate. The ADS820 is available in a 28-pin SOIC package.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS820U MIN	ADS820U TYP	ADS820U MAX	UNITS
Resolution				10 Guaranteed		Bits
Specified Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full Scale Input Range			+1.25		+3.25	V
Common-Mode Voltage				2.25		V
Analog Input Bandwidth (–3dB)						
Small Signal	–20dB Input	+25°C		120		MHz
Full Power	0dB Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY[2]						
Gain Error		+25°C		±0.6	±1.5	%
		Full		±1.0	±2.5	%
Gain Tempco				±85		ppm/°C
Power Supply Rejection of Gain	Delta $+V_S$ = ±5%	+25°C		0.01	0.1	%FSR/%
Input Offset Error		+25°C		±2.0	±2.5	%
		Full		±2.1	±3.0	%FSR/%
Power Supply Rejection of Offset	Delta $+V_S$ = ±5%	+25°C		0.02	0.1	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		20M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error						
f = 500kHz		+25°C		±0.15	±1.0	LSB
		Full		±0.15	±1.0	LSB
f = 10MHz		+25°C		±0.2	±1.0	LSB
		Full		±0.2	±1.0	LSB
No Missing Codes		Full		Guaranteed		
Integral Linearity Error at f = 500kHz		Full		±0.5	±2.0	LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	67	77		dBFS
		Full	64	74		dBFS
f = 10MHz (–1dBFS input)		+25°C	59	63		dBFS
		Full	57	62		dBFS
Two-Tone Intermodulation Distortion (IMD)[3]						
f = 4.4MHz and 4.5MHz (referred to –1dBFS envelope)		+25°C		–61		dBc
		Full		–60		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	58	60.5		dB
		Full	56	60		dB
f = 10MHz (–1dBFS input)		+25°C	58	60		dB
		Full	56	60		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	58	60		dB
		Full	55	60		dB
f = 10MHz (–1dBFS input)		+25°C	56	58		dB
		Full	54	57		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error	NTSC or PAL	+25°C		0.1		degrees
Effective Bits[4]	f_{IN} = 3.58MHz			9.5		Bits
Aperture Delay Time		+25°C		2		ns
Aperture Jitter		+25°C		7		ps rms
Overvoltage Recovery Time[5]	1.5x Full Scale Input	+25°C		2		ns

NOTE: (1) dBFS refers to dB below Full Scale. (2) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (4) Based on (SINAD – 1.76)/6.02. (5) No "rollover" of bits.

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS820U MIN	ADS820U TYP	ADS820U MAX	UNITS
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC		
Logic Levels	Logic "LO", C_L = 15pF	Full	0		0.4	V
	Logic "HI", C_L = 15pF	Full	2.5		$+V_S$	V
3-State Enable Time				20	40	ns
3-State Disable Time		Full		2	10	ns
POWER SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		39	47	mA
	Operating	Full		40	55	mA
Power Consumption	Operating	+25°C		195	235	mW
	Operating	Full		200	275	MW
Thermal Resistance, θ_{JA}						
28-Pin SOIC				75		°C/W

ORDERING INFORMATION

ADS820 (U)

Basic Model Number

Package Code

U: 28-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS820U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V Max
External Bottom Reference Voltage (REFB)	+1.1V Min

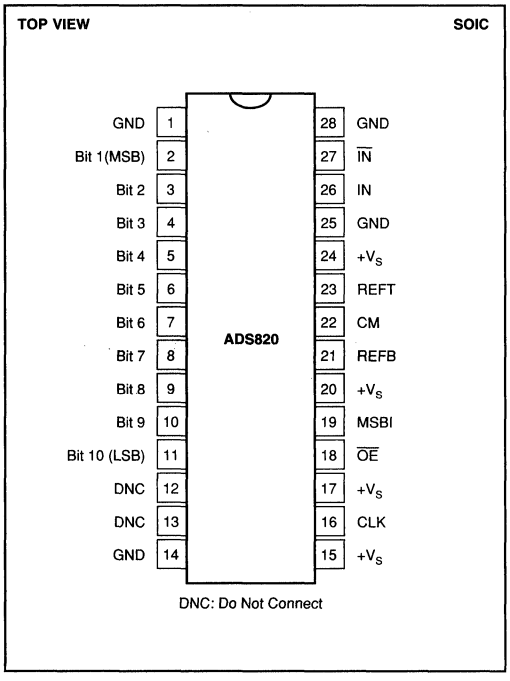
NOTE: Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

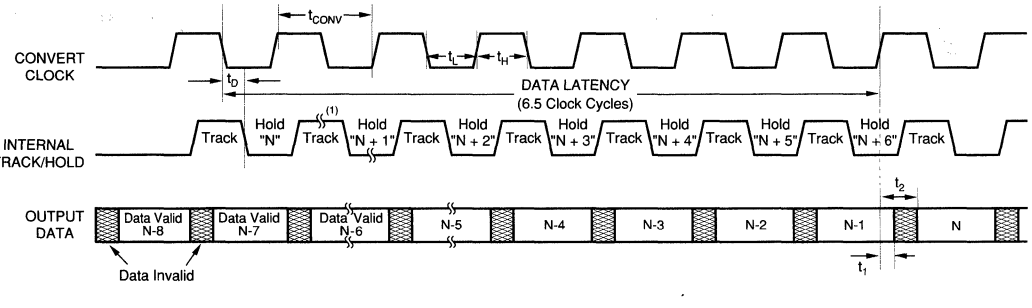
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10, Least Significant Bit
12	DNC	Do not connect.
13	DNC	Do not connect.
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistor.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistor.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM



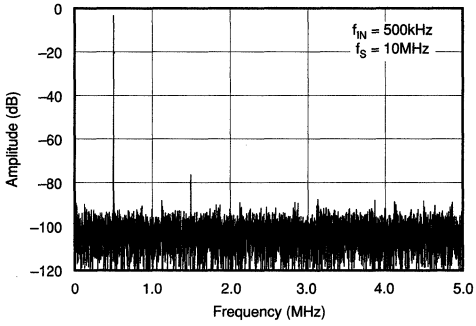
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	50		100µs	ns
t_L	Clock Pulse Low	24	25		ns
t_H	Clock Pulse High	24	25		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

NOTE: (1) " ⟆ " indicates the portion of the waveform that will stretch out at slower sample rates.

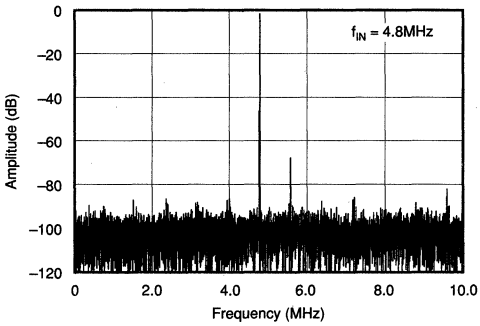
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

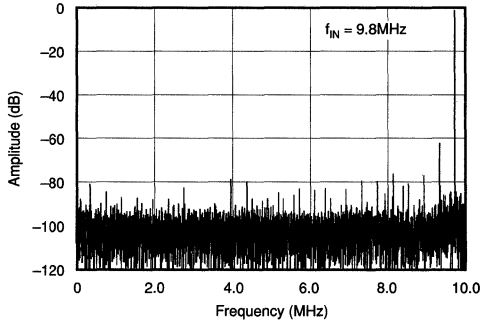
SPECTRAL PERFORMANCE



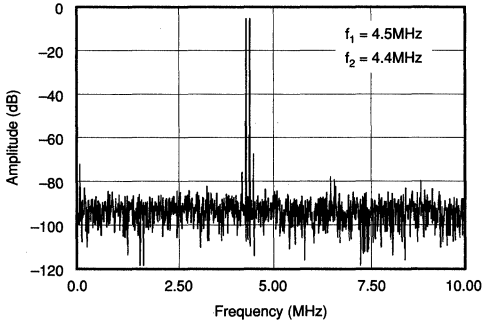
SPECTRAL PERFORMANCE



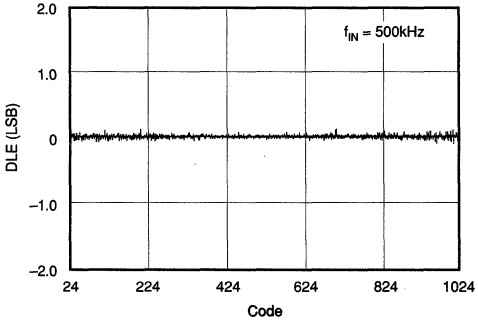
SPECTRAL PERFORMANCE



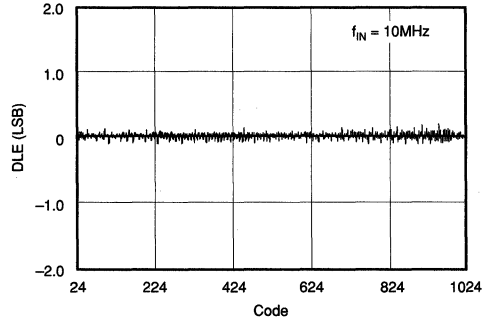
TWO-TONE INTERMODULATION



DIFFERENTIAL LINEARITY ERROR

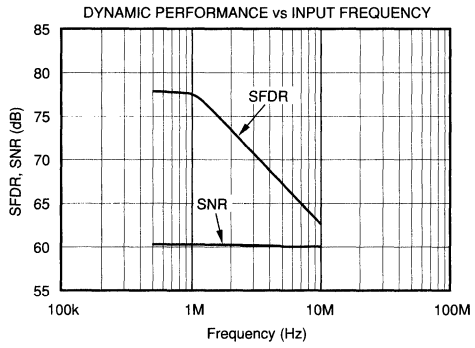


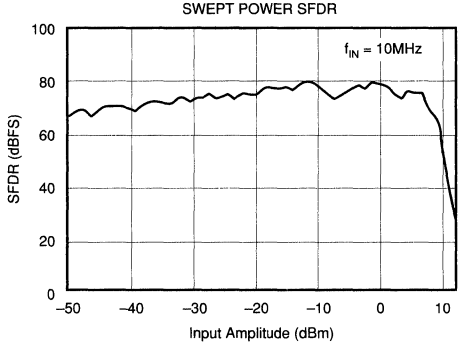
DIFFERENTIAL LINEARITY ERROR

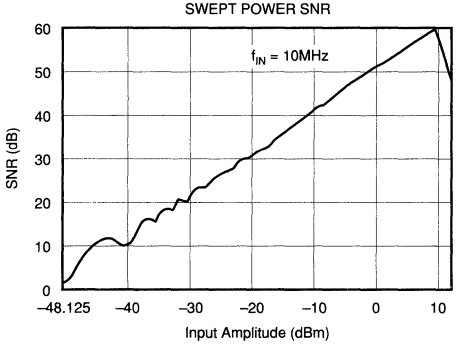


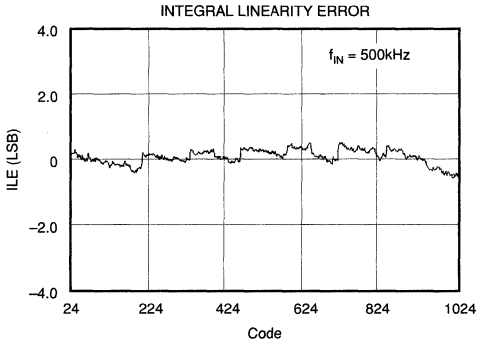
TYPICAL PERFORMANCE CURVES (CONT)

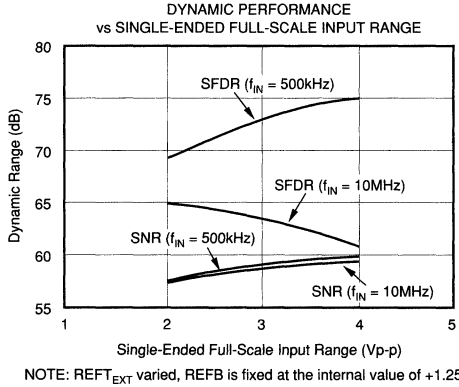
At T_A = +25°C, V_S = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.



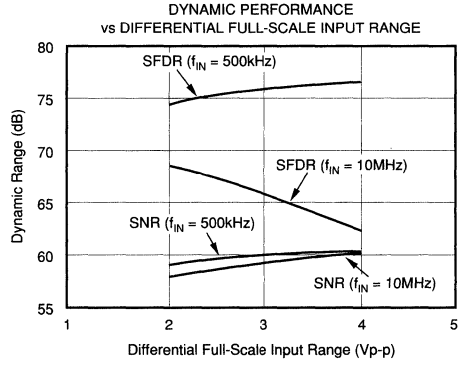








NOTE: $REFT_{EXT}$ varied, REFB is fixed at the internal value of +1.25V.

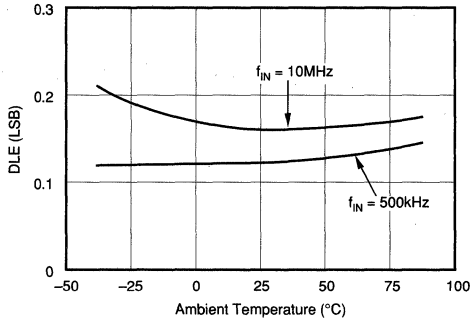


NOTE: $REFT_{EXT}$ varied, REFB is fixed at internal value of +1.25V.

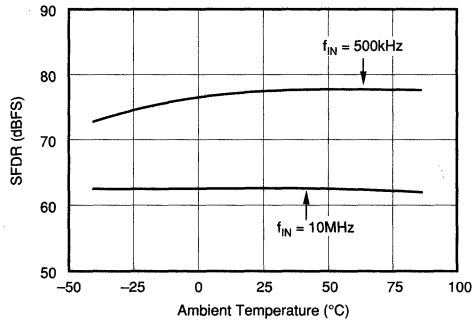
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

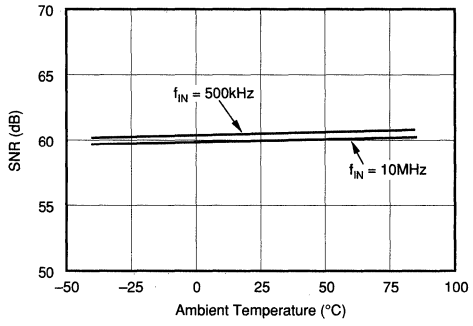
DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



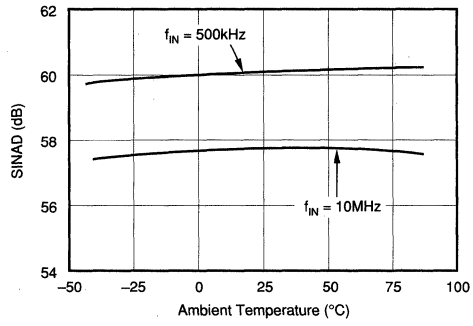
SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



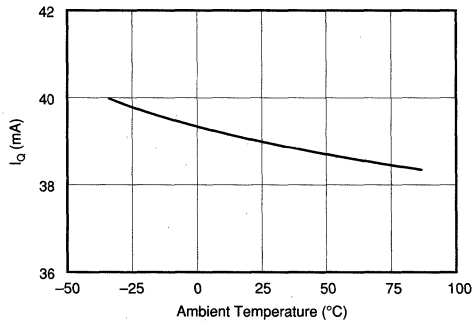
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



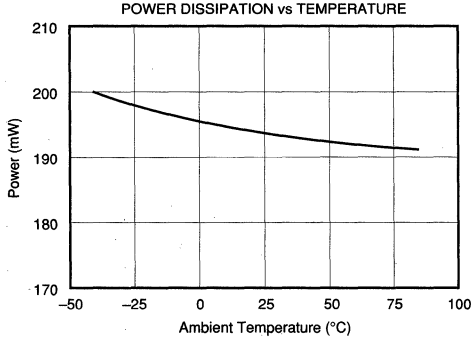
SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



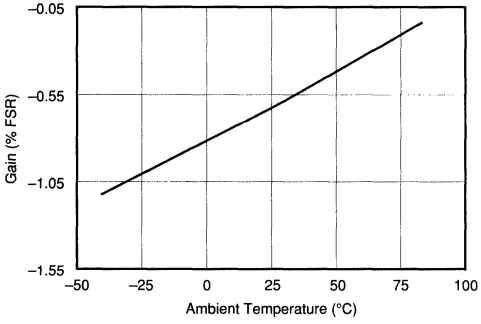
POWER DISSIPATION vs TEMPERATURE



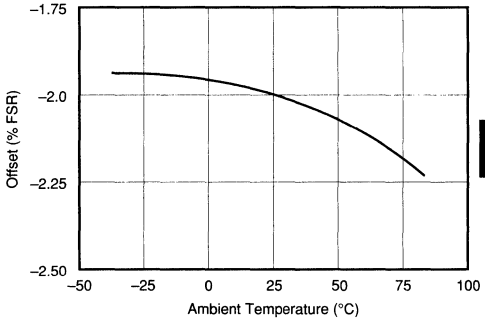
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 20MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

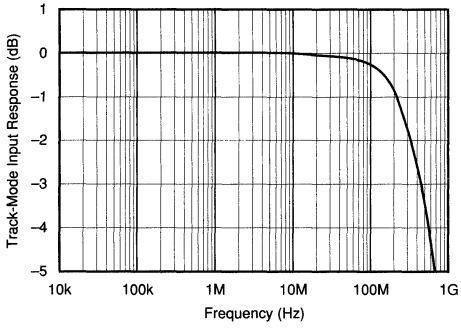
GAIN ERROR vs TEMPERATURE



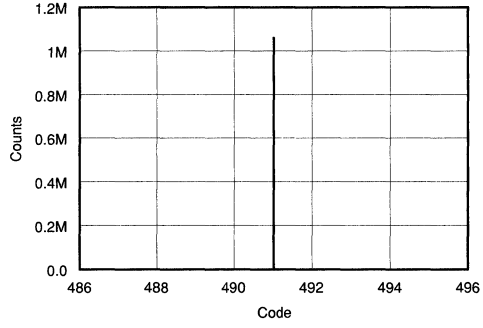
OFFSET ERROR vs TEMPERATURE



TRACK-MODE SMALL-SIGNAL INPUT BANDWIDTH



OUTPUT NOISE HISTOGRAM



THEORY OF OPERATION

The ADS820 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 10-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 9 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

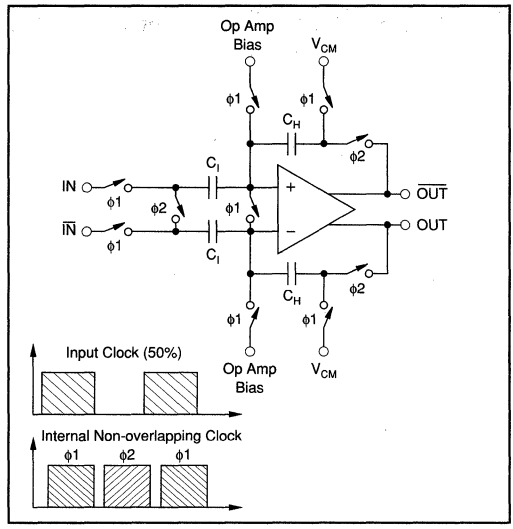


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

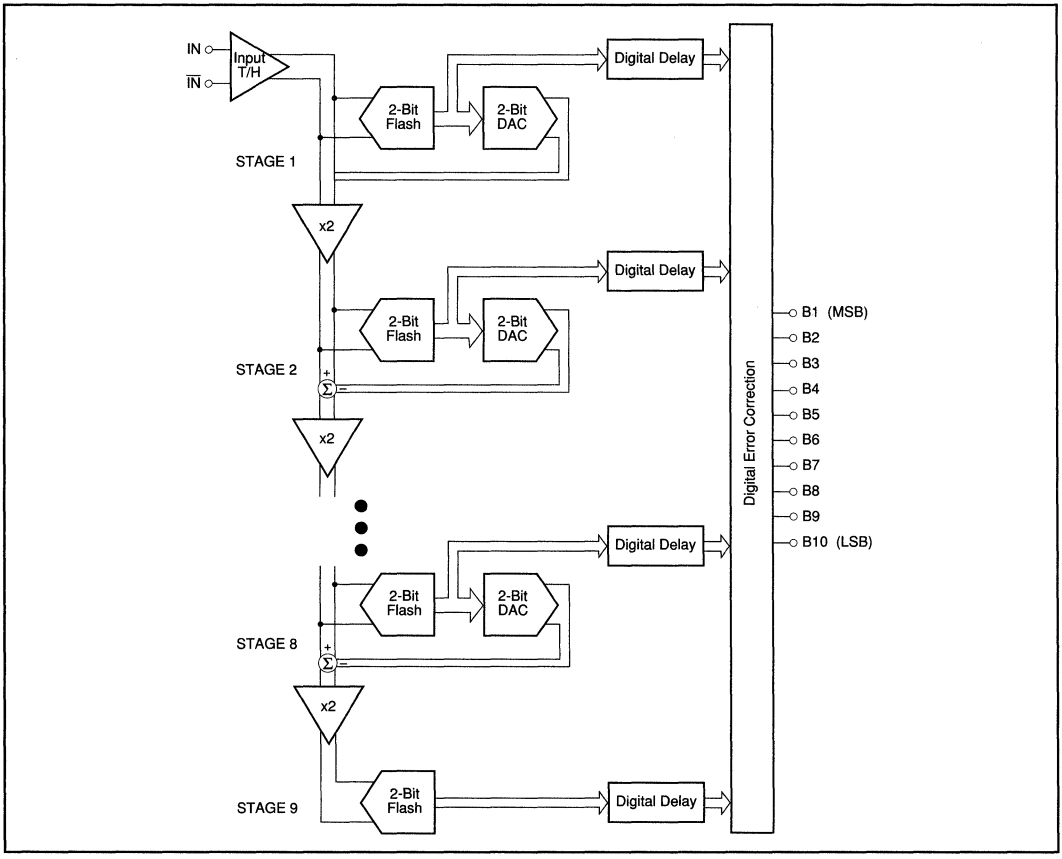


FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS820 excellent differential linearity and guarantees no missing codes at the 10-bit level.

There is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS820 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS820 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale reference (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended inputs, and ADS820 drive circuits, refer to the applications section.

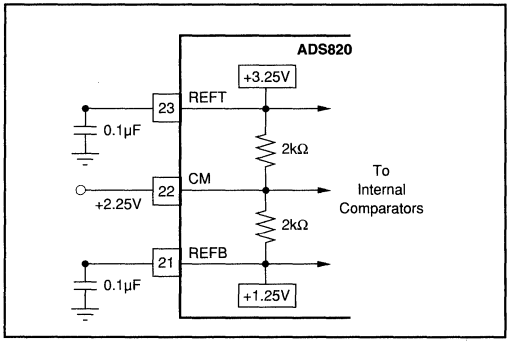


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. The rising and falling edge of the externally applied convert command clock control the various interstage conversions in the pipeline. Therefore, the duty cycle of the clock should be held at 50% with low jitter and fast rise/fall times of 2ns or less. This is especially important when digitizing a high frequency input and operating at the maximum sample rate. Deviation from a 50% duty cycle will effectively shorten some of the interstage settling times, thus degrading the SNR and DNL performance.

DIGITAL OUTPUT DATA

The 10-bit output data is provided at CMOS logic levels. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a high voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS820 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

	OUTPUT CODE	
DIFFERENTIAL INPUT[1]	SOB PIN 19 FLOATING or LO	BTC PIN 19 HI
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	1111111111	0111111111
+FS –1LSB	1111111111	0111111111
+FS –2LSB	1111111110	0111111110
+3/4 Full Scale	1110000000	0110000000
+1/2 Full Scale	1100000000	0100000000
+1/4 Full Scale	1010000000	0010000000
+1LSB	1000000001	0000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	1000000000	0000000000
–1LSB	0111111111	1111111111
–1/4 Full Scale	0110000000	1110000000
–1/2 Full Scale	0100000000	1100000000
–3/4 Full Scale	0010000000	1010000000
–FS +1LSB	0000000001	1000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	0000000000	1000000000

Note: In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.

TABLE I. Coding Table for the ADS820.

APPLICATIONS

DRIVING THE ADS820

The ADS820 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode voltage (CM) of +2.25V per Figure 4. This transformer-coupled input arrangement pro-

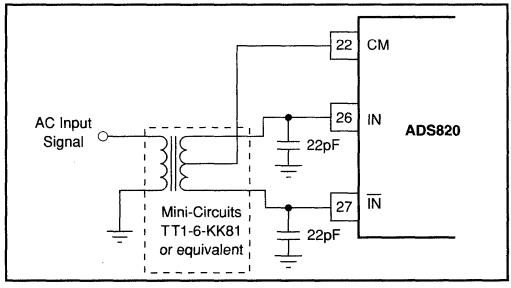


FIGURE 4. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

vides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{IN}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

If the signal needs to be DC coupled to the input of the ADS820, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 5 will provide the necessary input shifting required for signals centered around ground. It also

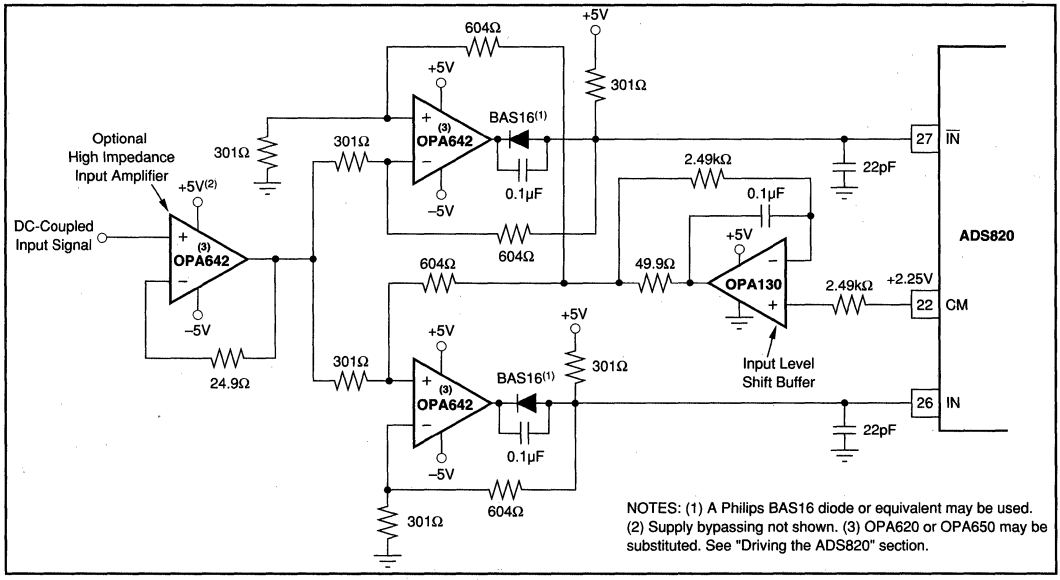


FIGURE 5. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

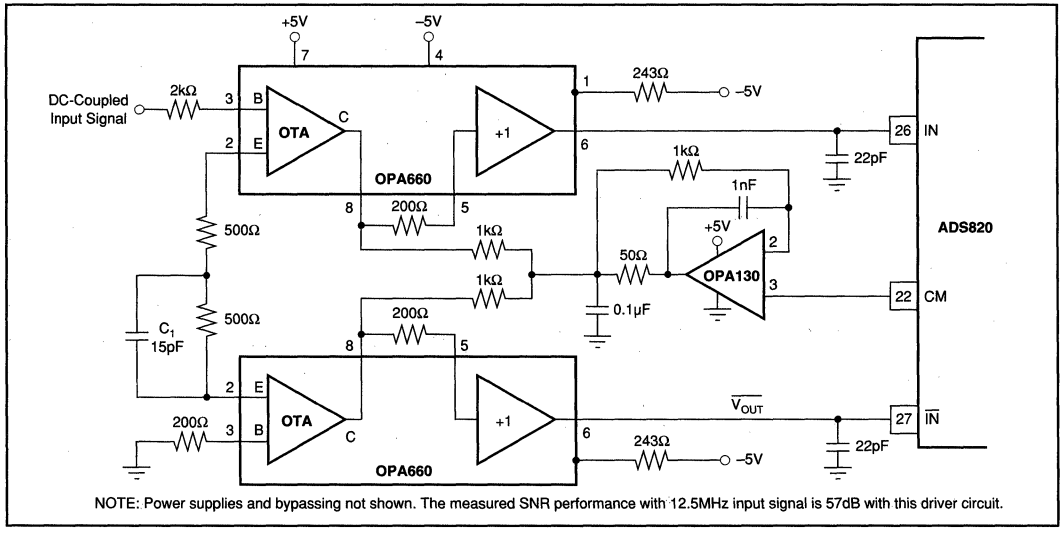


FIGURE 6. A Wideband DC-Coupled, Single-Ended to Differential Input Driver Circuit.

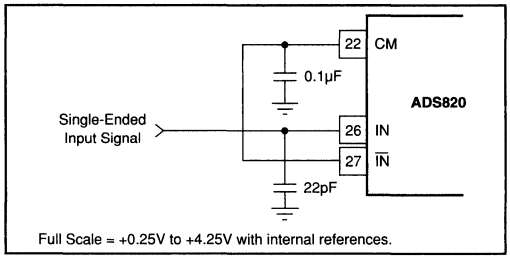


FIGURE 7. Single-Ended Input Connection.

employs a diode for output level shifting to guarantee a low distortion +3.25V output swing. Another DC-coupled circuit is shown in Figure 6. Other amplifiers can be used in place of the OPA642s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier. The OPA620 and OPA621, or the lower power OPA650 and OPA651 can be used in place of the OPA642s in Figure 5. In that configuration, the OPA650 and OPA651 will typically swing to within 100mV of positive full scale. If the OPA621 or OPA651 is used, the input buffer must be configured in a gain of 2.

The ADS820 can also be configured with a single-ended input full scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage as shown in Figure 7. This configuration will result in increased even-order harmonics, especially at higher input frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may overridden by external references that have at least 25mA of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full scale input range of the ADS820. Changing the full scale range to a lower value has the benefit of easing the swing requirements of external input amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V and the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V and the difference between the external references are greater than or equal to 800mV.

For the differential configuration, the full scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \cdot (REFT_{EXT} - REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the typical performance curves for expected performance vs full scale input range.

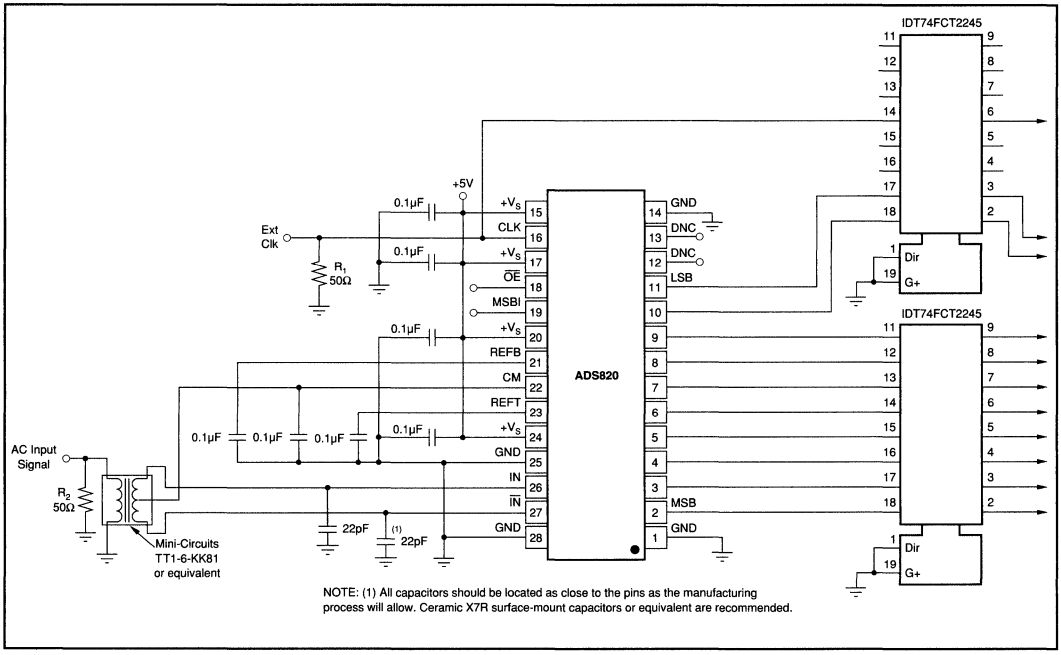


FIGURE 8. ADS820 Interface Schematic with AC-Coupling and External Buffers.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS820 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS820 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS820. Using a signal amplitude slightly lower than full scale will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

BURR-BROWN®

ADS821

SpeedPlus™ 10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- NO MISSING CODES
- INTERNAL REFERENCE
- LOW POWER: 380mW
- HIGH SNR: 58dB
- INTERNAL TRACK/HOLD
- 3-STATE OUTPUTS
- PACKAGE: 28-Pin SOIC

APPLICATIONS

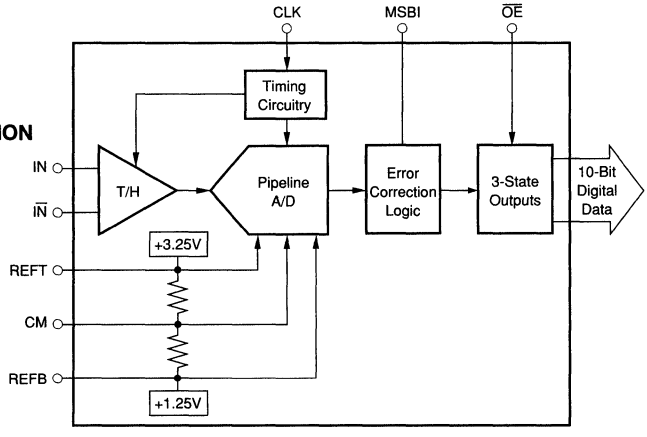
- VIDEO DIGITIZING
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- SET-TOP BOXES
- CABLE MODEMS
- CCD IMAGING
  - Color Copiers
  - Scanners
  - Camcorders
  - Security Cameras
  - Fax Machines
- IF AND BASEBAND DIGITIZATION
- TEST INSTRUMENTATION

DESCRIPTION

The ADS821 is a low power, monolithic 10-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 10-bit quantizer with internal track/hold, reference, and a power down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS821 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high performance converter is specified for AC and DC performance at a 40MHz sampling rate. The ADS821 is available in a 28-pin SOIC package.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS821U MIN	ADS821U TYP	ADS821U MAX	UNITS
Resolution					10	Bits
Specified Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full Scale Input Range			+1.25		+3.25	V
Common-Mode Voltage				2.25		V
Analog Input Bandwidth (–3dB)						
Small Signal	–20dBFS(1) Input	+25°C		120		MHz
Full Power	0dB Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY(2)						
Gain Error		+25°C		±0.6	±1.5	%
		Full		±1.1	±2.5	%
Gain Tempco				±85		ppm/°C
Power Supply Rejection of Gain	Delta +V_S = ±5%	+25°C		0.01	0.15	%FSR/%
Input Offset Error		+25°C		±2.0	±2.5	%
		Full		±2.1	±3.0	%FSR/%
Power Supply Rejection of Offset	Delta +V_S = ±5%	+25°C		0.02	0.15	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		40M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error	t_H = 13ns(3)					
f = 500kHz		+25°C		±0.5	±1.0	LSB
		0°C to +70°C		±0.6	±1.0	LSB
f = 12MHz		+25°C		±0.5	±1.0	LSB
		0°C to +70°C		±0.6	±1.0	LSB
No Missing Codes		0°C to +70°C		Guaranteed		
Integral Linearity Error at f = 500kHz		0°C to +70°C		±0.5	±2.0	LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	60	70		dBFS
		Full	54	67		dBFS
f = 12MHz (–1dBFS input)		+25°C	58	63		dBFS
		Full	54	62		dBFS
Two-Tone Intermodulation Distortion (IMD)(4)						
f = 4.4MHz and 4.5MHz (referred to –1dBFS envelope)		+25°C		–61		dBc
		Full		–60		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	57	59		dB
		Full	55	59		dB
f = 12MHz (–1dBFS input)		+25°C	56	58		dB
		Full	54	58		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	56	58.5		dB
		Full	55	58		dB
f = 12MHz (–1dBFS input)		+25°C	53	57		dB
		Full	51	56		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error	NTSC or PAL	+25°C		0.1		degrees
Effective Bits(4)	f_{IN} = 3.58MHz	+25°C		9.3		Bits
Aperture Delay Time		+25°C		2		ns
Aperture Jitter		+25°C		7		ps rms
Overvoltage Recovery Time(6)	1.5x Full Scale Input	+25°C		2		ns

NOTE: (1) dBFS refers to dB below Full Scale. (2) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (3) Refer to Timing Diagram footnotes for the f_{IN} = 500kHz differential linearity error performance condition. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 7dB lower. (5) Based on (SINAD – 1.76)/6.02. (6) No "rollover" of bits.

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS821U MIN	ADS821U TYP	ADS821U MAX	UNITS
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC		
Logic Levels	Logic "LO", C_L = 15pF	Full	0		0.4	V
	Logic "HI", C_L = 15pF	Full	2.5		$+V_S$	V
3-State Enable Time				20	40	ns
3-State Disable Time		Full		2	10	ns
POWER SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		76	88	mA
	Operating	Full		78	90	mA
Power Consumption	Operating	+25°C		380	440	mW
	Operating	Full		390	450	mW
Thermal Resistance, θ_{JA}						
28-Pin SOIC				75		°C/W

ORDERING INFORMATION

ADS821 (U)

Basic Model Number

Package Code

U: 28-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS821U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V max
External Bottom Reference Voltage (REFB)	+1.1V min

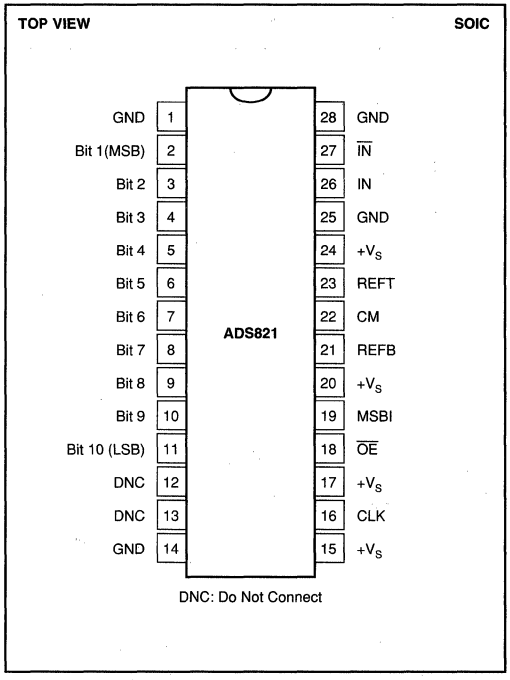
NOTE: Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

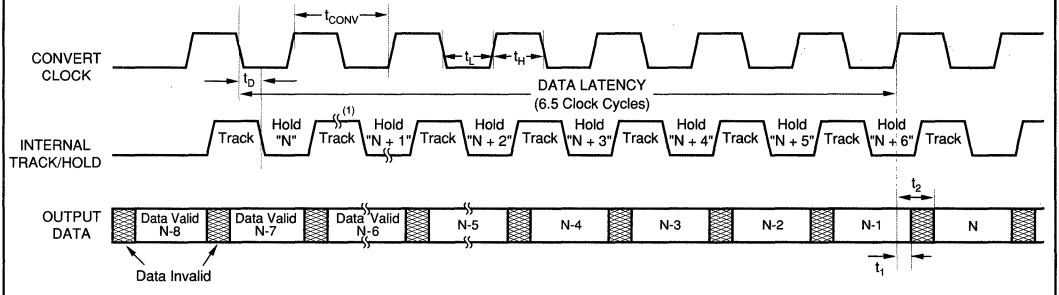
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10, Least Significant Bit
12	DNC	Do not connect.
13	DNC	Do not connect.
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistor.
19	MSBI	Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistor.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM

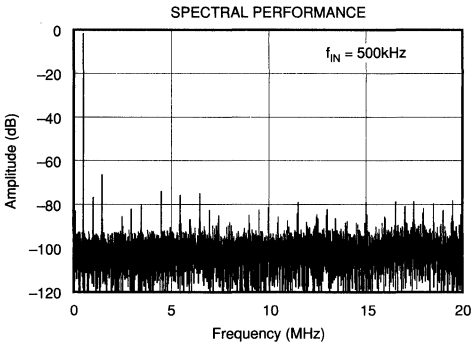


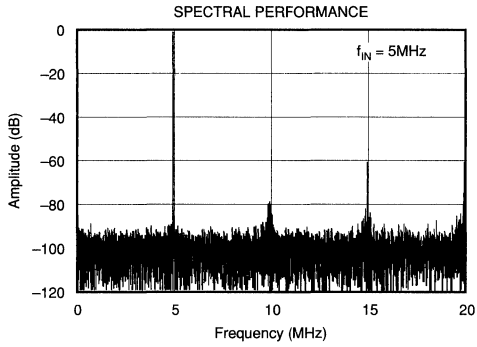
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse Low	12	12.5		ns
t_H	Clock Pulse High	12(2)	12.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

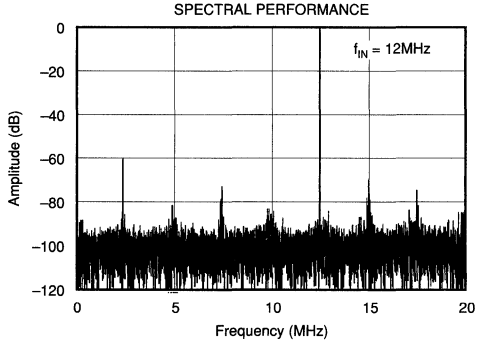
NOTE: (1) "§" indicates the portion of the waveform that will stretch out at slower sample rates. (2) t_H must be 13ns minimum if no missing codes is desired only for the conditions of t_{CONV} ≤28ns and f_{IN} <2MHz. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

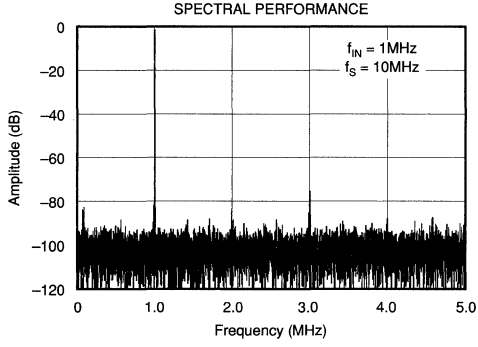
TYPICAL PERFORMANCE CURVES

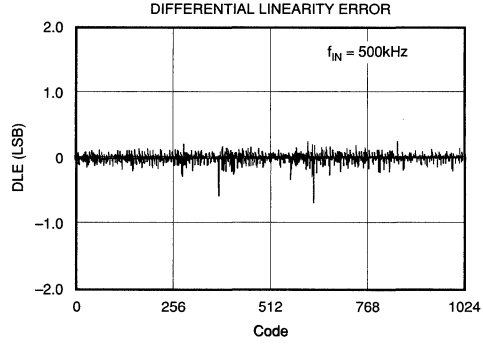
At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

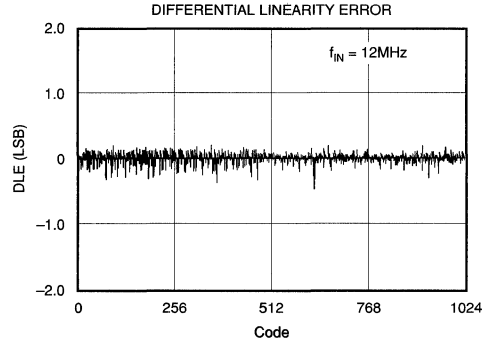








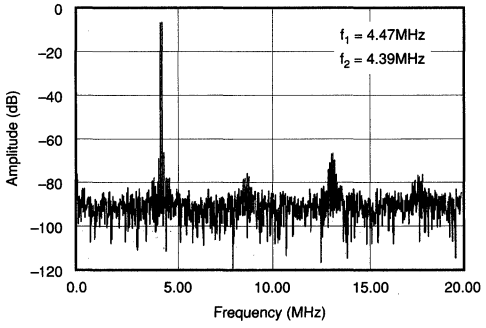




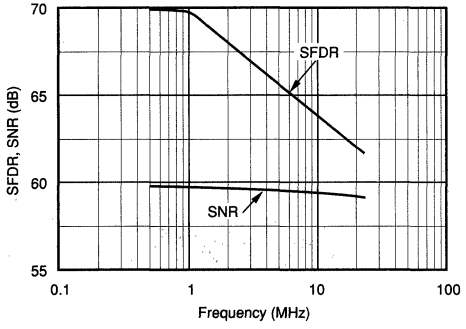
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

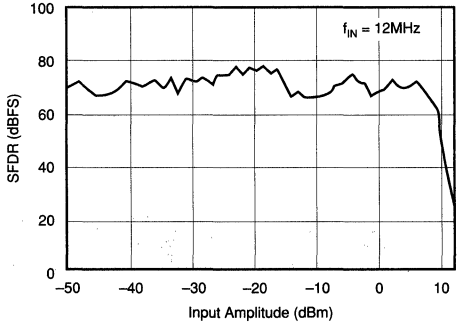
TWO-TONE INTERMODULATION



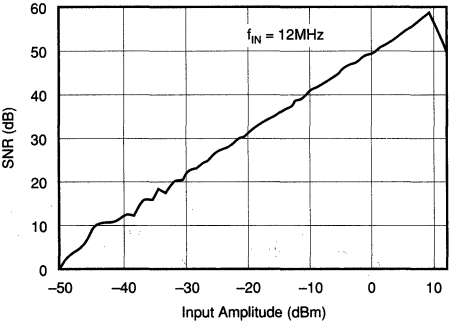
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



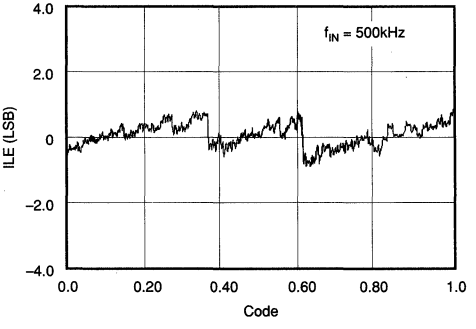
SWEPT POWER SFDR



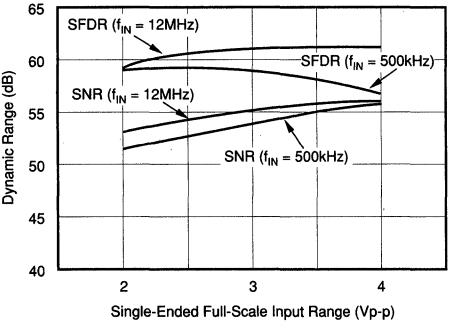
SWEPT POWER SNR



INTEGRAL LINEARITY ERROR



DYNAMIC PERFORMANCE
vs SINGLE-ENDED FULL-SCALE INPUT RANGE

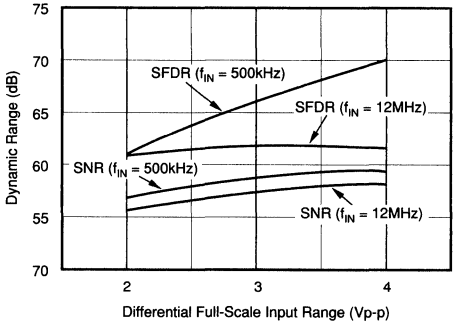


NOTE: $REFT_{EXT}$ varied, REFB is fixed at the internal value of +1.25V.

TYPICAL PERFORMANCE CURVES (CONT)

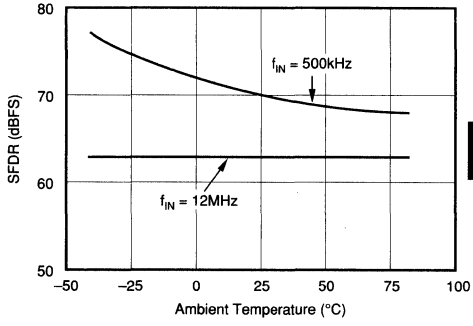
At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

DYNAMIC PERFORMANCE
vs DIFFERENTIAL FULL-SCALE INPUT RANGE

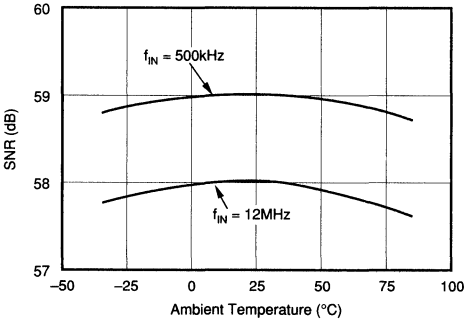


NOTE: $REFT_{EXT}$ varied, REFB is fixed at internal value of +1.25V.

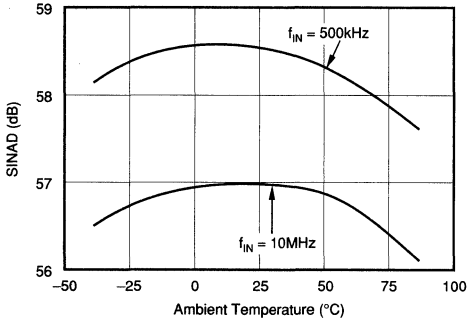
SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE



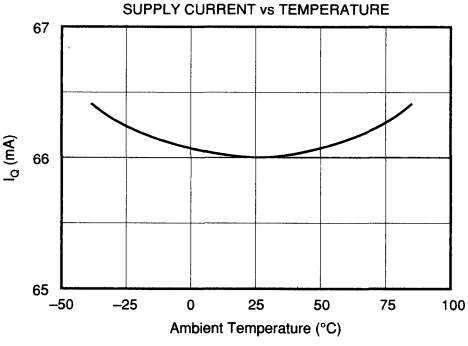
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



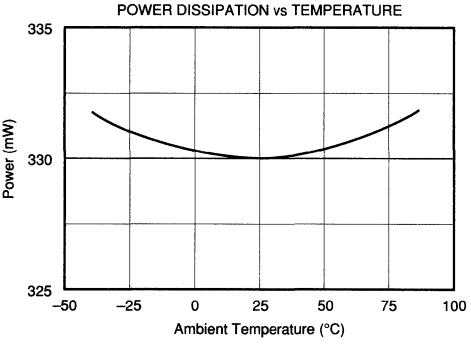
SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



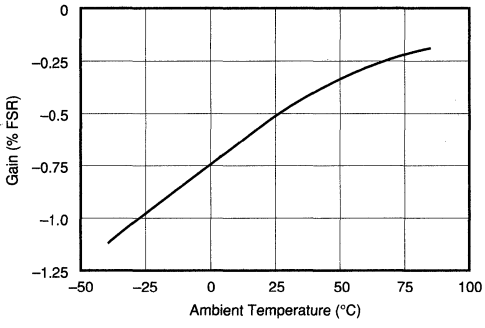
POWER DISSIPATION vs TEMPERATURE



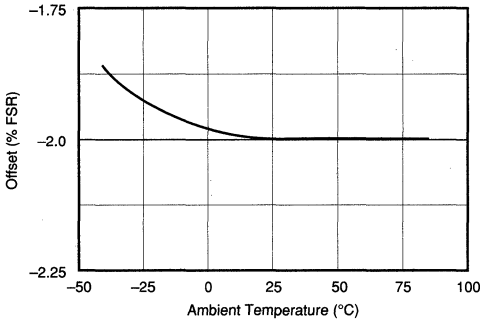
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

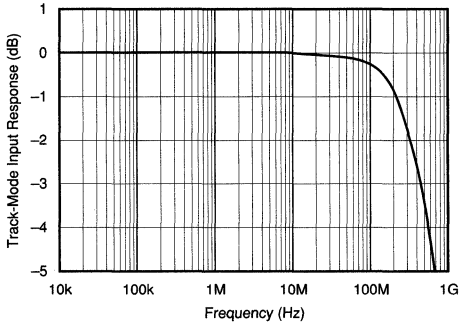
GAIN ERROR vs TEMPERATURE



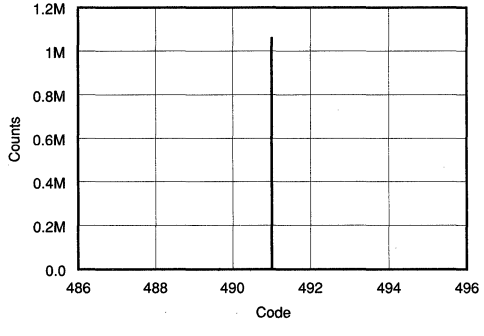
OFFSET ERROR vs TEMPERATURE



TRACK-MODE SMALL-SIGNAL INPUT BANDWIDTH



OUTPUT NOISE HISTOGRAM



THEORY OF OPERATION

The ADS821 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 10-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi 1$ and $\phi 2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 9 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

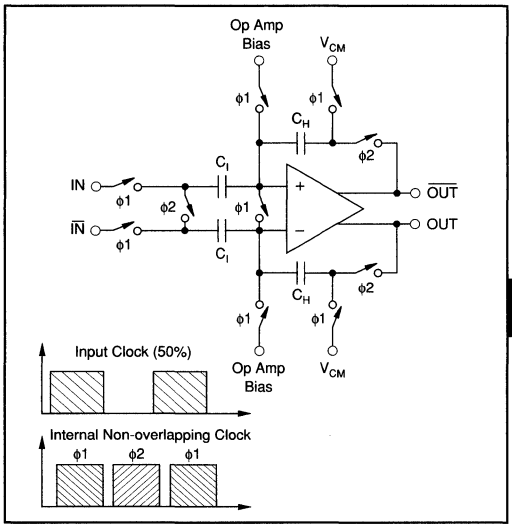


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

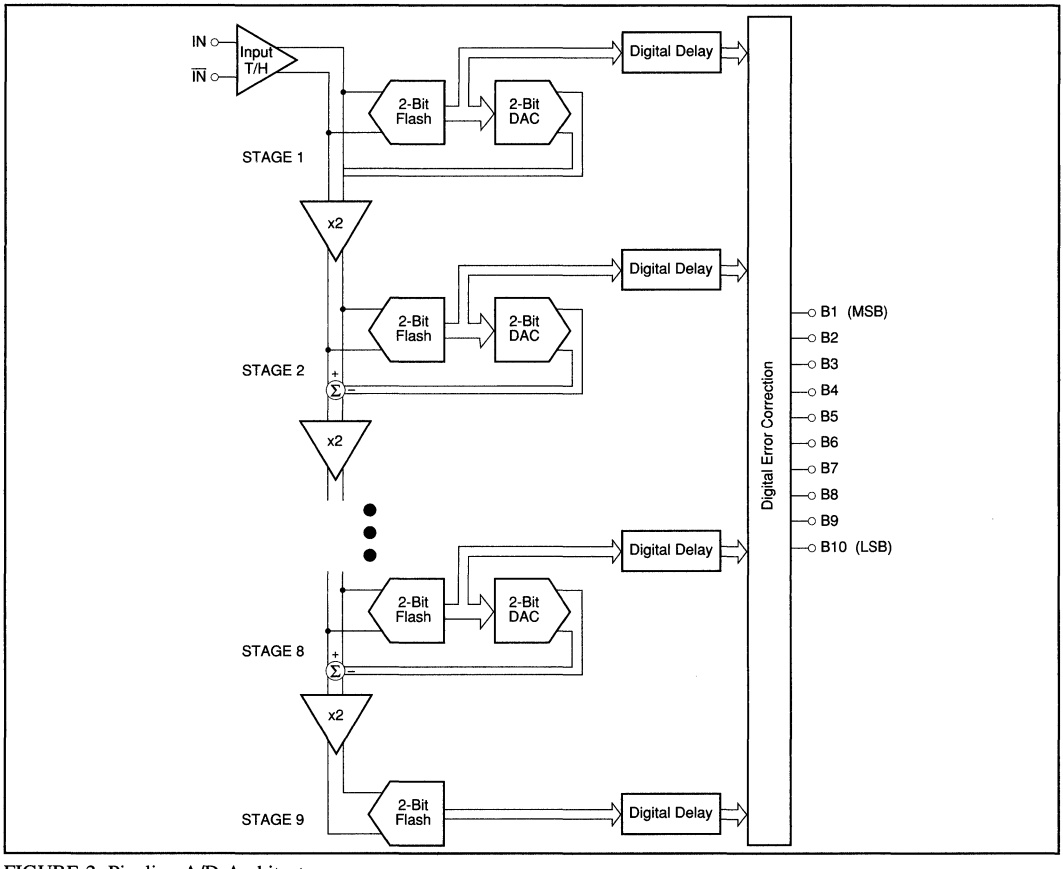


FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS821 excellent differential linearity and guarantees no missing codes at the 10-bit level.

The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS821 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS821 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale reference (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended inputs, and ADS821 drive circuits, refer to the applications section.

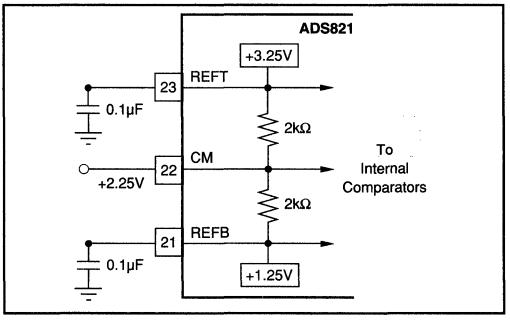


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. Both the rising and falling edges of the externally applied clock control the various interstage conversions in the pipeline. Therefore, the clock signal's jitter, rise/fall times and duty cycle can affect conversion performance.

- Low clock **jitter** is critical to SNR performance in frequency-domain signal environments.
- Clock **rise and fall times** should be as short as possible (<2ns for best performance).
- For most applications, the clock duty should be set to 50%. However, for applications requiring no missing codes, a slight skew in the duty cycle will improve DNL performance for conversion rates >35MHz and input frequencies <2MHz (see Timing Diagram). A possible method for skewing the 50% duty cycle source is shown in Figure 4.

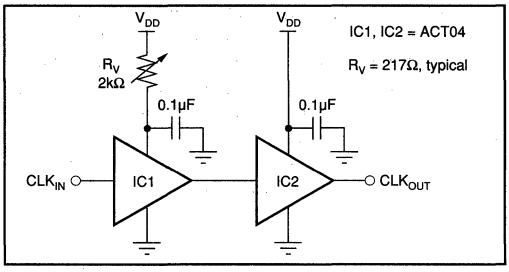


FIGURE 4. Clock Skew Circuit.

DIGITAL OUTPUT DATA

The 10-bit output data is provided at CMOS logic levels. There is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a high voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS821 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

	OUTPUT CODE	
DIFFERENTIAL INPUT[1]	SOB PIN 19 FLOATING or LO	BTC PIN 19 HI
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	1111111111	0111111111
+FS –1LSB	1111111111	0111111111
+FS –2LSB	1111111110	0111111110
+3/4 Full Scale	1110000000	0110000000
+1/2 Full Scale	1100000000	0100000000
+1/4 Full Scale	1010000000	0010000000
+1LSB	1000000001	0000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	1000000000	0000000000
–1LSB	0111111111	1111111111
–1/4 Full Scale	0110000000	1110000000
–1/2 Full Scale	0100000000	1100000000
–3/4 Full Scale	0010000000	1010000000
–FS +1LSB	0000000001	1000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	0000000000	1000000000
Note: In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.		

TABLE I. Coding Table for the ADS821.

APPLICATIONS

DRIVING THE ADS821

The ADS821 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A

differential output is created on the secondary if the center tap is tied to the common-mode voltage (CM) of +2.25V per Figure 5. This transformer-coupled input arrangement provides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered refer-

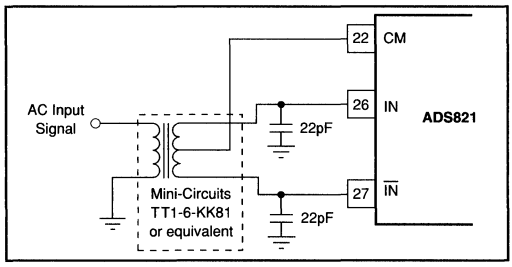


FIGURE 5. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

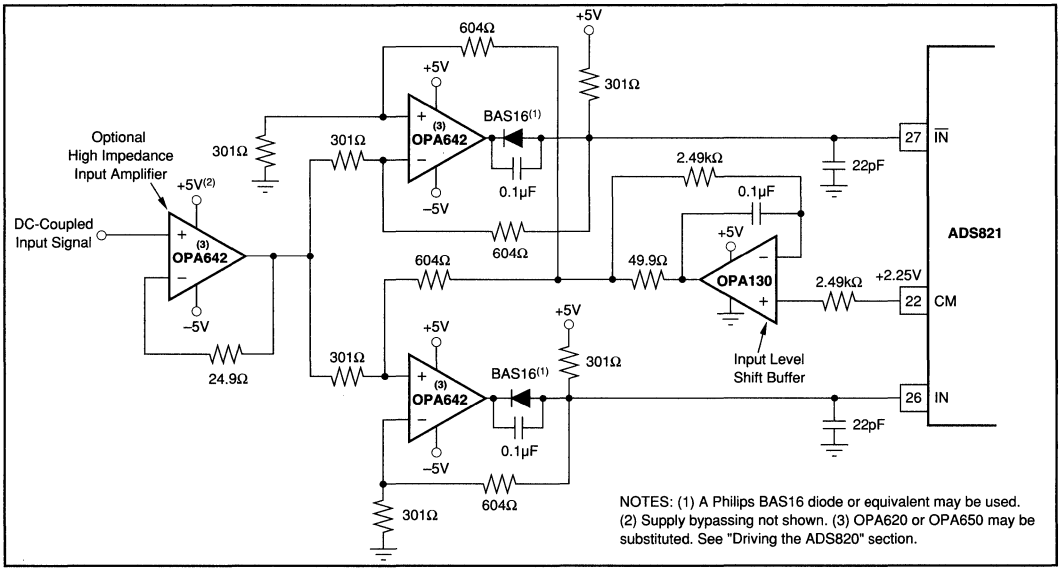


FIGURE 6. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

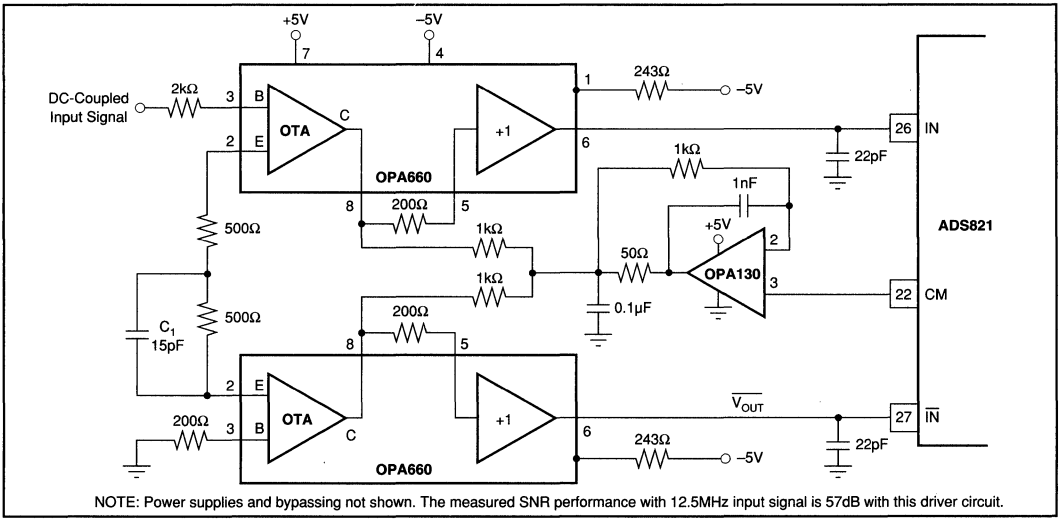


FIGURE 7. A Wideband DC-Coupled, Single-Ended to Differential Input Driver Circuit.

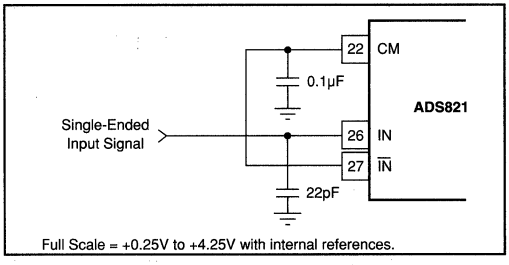


FIGURE 8. Single-Ended Input Connection.

ence for driving external circuitry. The analog IN and $\overline{IN}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

If the signal needs to be DC coupled to the input of the ADS821, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 6 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to guarantee a low distortion +3.25V output swing. Another DC-coupled circuit is shown in Figure 7. Other amplifiers can be used in place of the OPA642s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier. The OPA620 and OPA621, or the lower power OPA650 or OPA651 can be used in place of the OPA642s in Figure 6. In that configuration, the OPA650 and OPA651 will typically swing to within 100mV of positive full scale. If the OPA621 or OPA651 is used, the input buffer must be configured in a gain of 2.

The ADS821 can also be configured with a single-ended input full scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage as shown in Figure 8. This configuration will result in increased even-order harmonics, especially at higher input frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may overridden by external references that have at least 25mA of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full scale input range of the ADS821. Changing the full scale

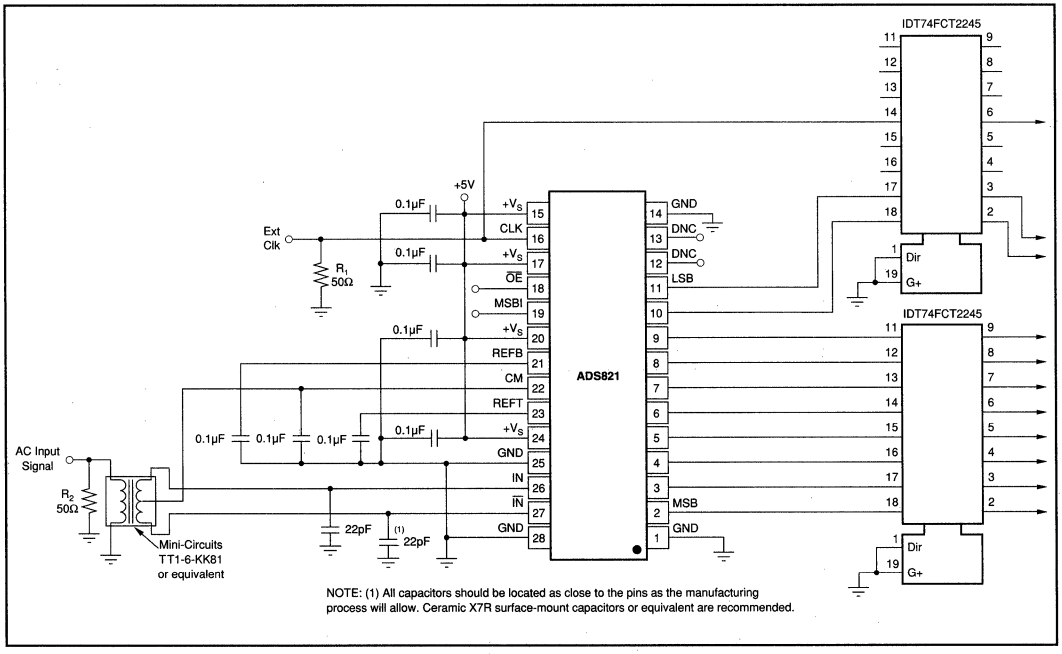


FIGURE 9. ADS821 Interface Schematic with AC-Coupling and External Buffers.

range to a lower value has the benefit of easing the swing requirements of external input amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V and the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V and the difference between the external references are greater than or equal to 800mV.

For the differential configuration, the full scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \bullet (REFT_{EXT} - REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the typical performance curves for expected performance vs full scale input range.

PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS821 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS821 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS821. Using a signal amplitude slightly lower than full scale will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

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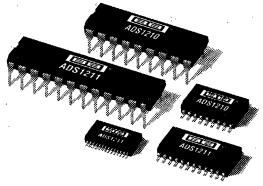


ADS1210
ADS1211

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- DELTA-SIGMA A/D CONVERTER
- 24 BITS NO MISSING CODES
- 23 BITS EFFECTIVE RESOLUTION AT 10Hz AND 20 BITS AT 1000Hz
- DIFFERENTIAL INPUTS
- PROGRAMMABLE GAIN AMPLIFIER
- FLEXIBLE SPI COMPATIBLE SSI INTERFACE WITH 2-WIRE MODE
- PROGRAMMABLE CUT-OFF FREQUENCY UP TO 16KHz
- INTERNAL/EXTERNAL REFERENCE
- ON CHIP SELF-CALIBRATION
- ADS1211 INCLUDES 4 CHANNEL MUX

APPLICATIONS

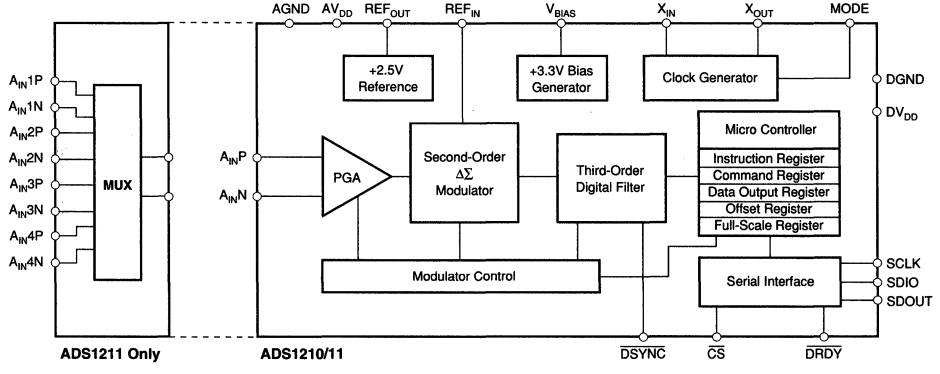
- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

DESCRIPTION

The ADS1210 and ADS1211 are precision, wide dynamic range, delta-sigma analog-to-digital converters with 24-bit resolution operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level voltage signals. The delta-sigma architecture is used for wide dynamic range and to guarantee 24 bits of no missing code performance. An effective resolution of 23 bits is achieved through the use of a very low-noise input amplifier at conversion rates up to 10Hz. Effective resolutions of 19 bits can be maintained up to a sample rate of 1kHz through the use of the unique Turbo modulator mode of operation. The dynamic range of the converters is further increased by providing a low-noise programmable gain amplifier with a gain range of 1 to 16 in binary steps.

The ADS1210 and ADS1211 are designed for high resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. Both converters include a flexible synchronous serial interface which is SPI compatible and also offers a two-wire control mode for low cost isolation.

The ADS1210 is a single channel converter and is offered in both 18-pin DIP and SOIC packages. The ADS1211 includes a 4 channel input multiplexer and is available in 24-pin DIP, 24-pin SOIC, and 28-pin SSOP packages.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

All specifications typical at +25°C, AV_{DD} = DV_{DD} = +5V, f_{SC} = 10MHz, and external V_{REF} = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1210U, P/ADS1211U, P, E MIN	TYP	MAX	UNITS
ANALOG INPUT					
Input Voltage Range - Unipolar[1]		0		+5	V
Bipolar[1, 2]		–10		+10	V
Input Impedance	G = Gain of PGA		4/G		MΩ
Programmable Gain Amplifier	User Selectable Gain Ranges	1		16	
Input Capacitance			20		pF
Input Leakage Current			100		pA
SYSTEMS PERFORMANCE					
Resolution			24		Bits
No Missing Codes	f_S = 60Hz Normal Mode	24			Bits
	f_S = 100Hz Turbo Mode X4	21			Bits
	f_S = 250Hz Turbo Mode X8	20			Bits
	f_S = 500Hz Turbo Mode X16	20			Bits
	f_S = 1000Hz Turbo Mode X16	20			Bits
Integral Linearity	f_S = 60Hz			±0.003	%FSR
	f_S = 1000Hz Turbo Mode X16			±0.003	%FSR
Unipolar Offset Error[3]			See Note 4		
Unipolar Offset Drift[5]			1		µV/°C
Gain Error[3]			See Note 4		
Gain Error Drift[5]			1		µV/°C
Common-Mode Rejection	At dc	100			dB
	f_S = 50Hz	160			dB
	f_S = 60Hz	160			dB
Normal-Mode Rejection	f_S = 50Hz	100			dB
	f_S = 60Hz	100			dB
Output Noise	See Typical Performance Curves				
Power Supply Rejection			60		dB
VOLTAGE REFERENCE					
Internal Reference			2.5		V
REF_{OUT}, Internal Reference Drift			60		ppm/°C
Internal Reference Noise			50		µVp-p
REF_{IN}, External Reference		1		$+V_{DD}$	V
V_{BIAS}, Output	Derived from REF_{IN}		3.3		V
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +5µA	2.0		$+V_{DD}$	V
V_{IL}	I_{IL} = +5µA	0		0.8	V
V_{OH}	I_{OH} = 2 TTL Loads	2.4		$+V_{DD}$	V
V_{OL}	I_{OL} = 2 TTL Loads	0		0.4	V
System Clock Rate: f_{SC}		0.5		10	MHz
Output Data Rate: f_S	User Programmable, f_{SC} = 10MHz	2.4		16,000	Hz
Data Format	Command Register Programmable		Two's Complement or Offset Binary		
POWER SUPPLY REQUIREMENTS					
Power Supply Voltage		4.75		5.25	V
Quiescent Current	V_{DD} = +5V, Normal Mode, f_{SC} = 10MHz		6	8	mA
	V_{DD} = +5V, Normal Mode, f_{SC} = 2MHz			3.5	mA
	V_{DD} = +5V, Sleep Mode				mA
Power Dissipation	V_{DD} = +5V, Normal Mode		30	40	mW
	V_{DD} = +5V, Turbo Mode X16		65	80	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) In order to achieve the converter's plus or minus full-scale input voltage, the input must be fully differential ($A_{IN}N$ = REF_{IN} – ($A_{IN}P$ –REF_{IN})). If the input is single-ended ($A_{IN}N$ = REF_{IN}), only plus or minus one-half full-scale will be achieved. (2) This range is set with external resistors and V_{BIAS}. Other ranges are possible. (3) Applies after calibration. (4) These errors will be of the order of the effective resolution of the converter. Refer to the Typical Performance Curves which apply to the desired mode of operation. (5) Recalibration can be used to remove these errors.

ABSOLUTE MAXIMUM RATINGS

Analog Input:
- Input Current ..... 100mA, Momentary
  10mA, Continuous
- Input Voltage ..... AV_{DD} +0.5V to GND –0.5V

Power Supply Voltage:
- AV_{DD} ..... +7V

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

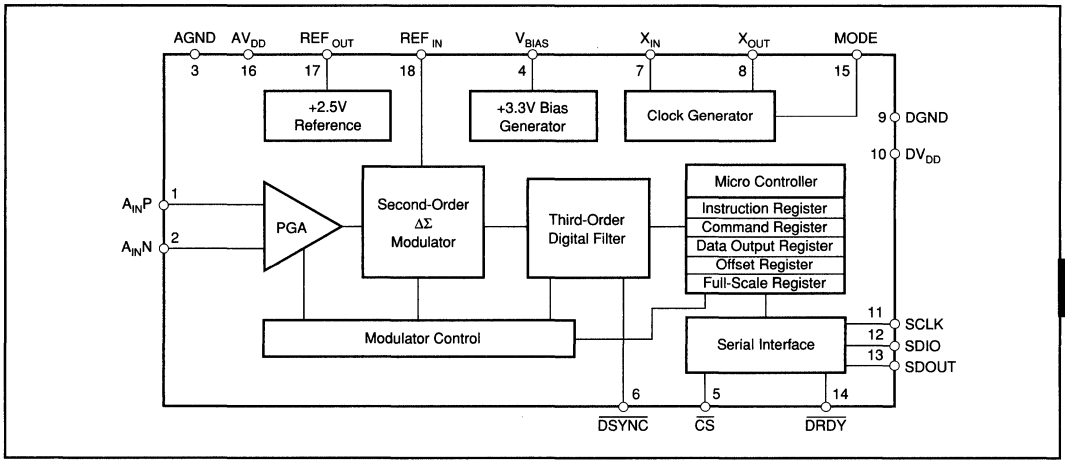
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS1210P	18-Pin Plastic DIP	218
ADS1210U	18-Lead SOIC	219
ADS1211P	24-Pin Plastic DIP	243
ADS1211U	24-Lead SOIC	239
ADS1211E	28-Lead SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

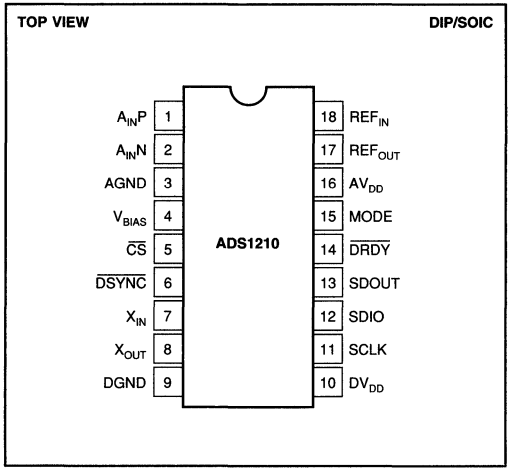
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ADS1210P	18-Pin Plastic DIP	–40°C to +85°C
ADS1210U	18-Lead SOIC	–40°C to +85°C
ADS1211P	24-Pin Plastic DIP	–40°C to +85°C
ADS1211U	24-Lead SOIC	–40°C to +85°C
ADS1211E	28-Lead SSOP	–40°C to +85°C

ADS1210 SIMPLIFIED BLOCK DIAGRAM



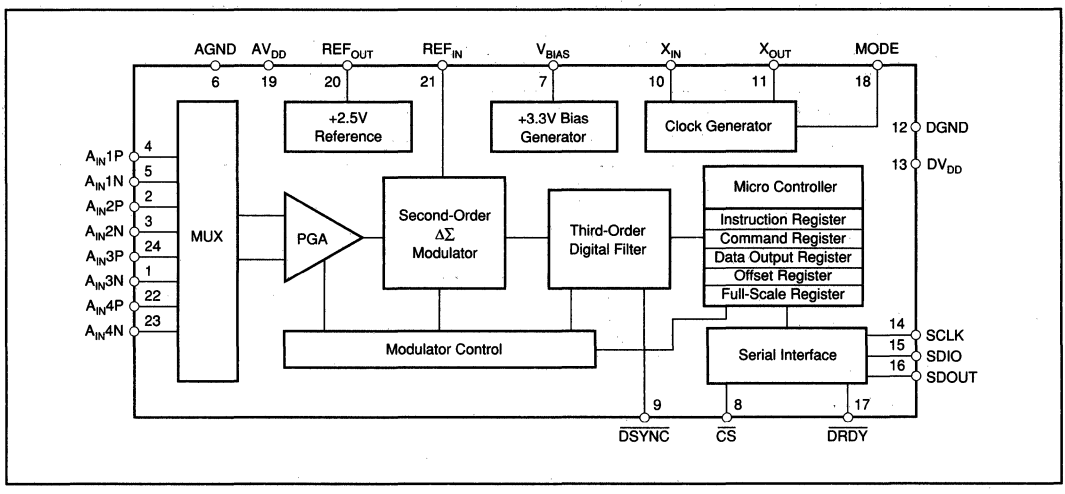
ADS1210 PIN CONFIGURATION



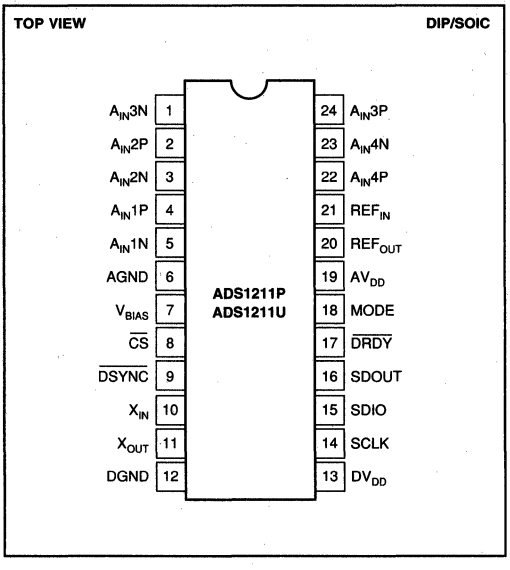
ADS1210 PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	$A_{IN}P$	Noninverting Input.
2	$A_{IN}N$	Inverting Input.
3	AGND	Analog Ground.
4	V_{BIAS}	Bias Voltage Output, +3.3V nominal.
5	$\overline{CS}$	Chip Select Input.
6	$\overline{DSYNC}$	Control Input to Synchronize Serial Output Data.
7	X_{IN}	System Clock Input.
8	X_{OUT}	System Clock Output (for Crystal or Resonator).
9	DGND	Digital Ground.
10	DV_{DD}	Digital Supply, +5V nominal. Must be ≤AV_{DD}.
11	SCLK	Clock Input/Output for serial data transfer.
12	SDIO	Serial Data Input (can also function as Serial Data Output).
13	SDOUT	Serial Data Output.
14	$\overline{DRDY}$	Data Ready.
15	MODE	SCLK Control Input (Master = 1, Slave = 0).
16	AV_{DD}	Analog Supply, +5V nominal.
17	REF_{OUT}	Reference Output, +2.5V nominal.
18	REF_{IN}	Reference Input.

ADS1211 SIMPLIFIED BLOCK DIAGRAM



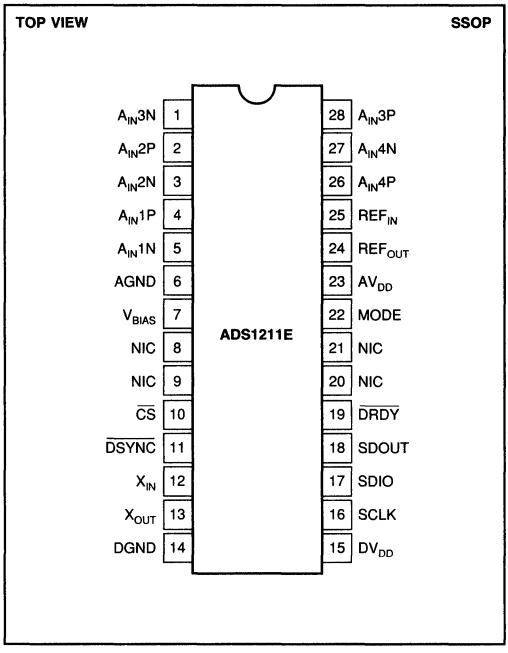
ADS1211P AND ADS1211U PIN CONFIGURATION



ADS1211P AND ADS1211U PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	$A_{IN}3N$	Inverting Input Channel 3.
2	$A_{IN}2P$	Noninverting Input Channel 2.
3	$A_{IN}2N$	Inverting Input Channel 2.
4	$A_{IN}1P$	Noninverting Input Channel 1.
5	$A_{IN}1N$	Inverting Input Channel 1.
6	AGND	Analog Ground.
7	V_{BIAS}	Bias Voltage Output, +3.3V nominal.
8	$\overline{CS}$	Chip Select Input.
9	$\overline{DSYNC}$	Control Input to Synchronize Serial Output Data.
10	X_{IN}	System Clock Input.
11	X_{OUT}	System Clock Output (for Crystal or Resonator).
12	DGND	Digital Ground.
13	DV_{DD}	Digital Supply, +5V nominal. Must be ≤AV_{DD}.
14	SCLK	Clock Input/Output for serial data transfer.
15	SDIO	Serial Data Input (can also function as Serial Data Output).
16	SDOUT	Serial Data Output.
17	$\overline{DRDY}$	Data Ready.
18	MODE	SCLK Control Input (Master = 1, Slave = 0).
19	AV_{DD}	Analog Supply, +5V nominal.
20	REF_{OUT}	Reference Output: +2.5V nominal.
21	REF_{IN}	Reference Input.
22	$A_{IN}4P$	Noninverting Input Channel 4.
23	$A_{IN}4N$	Inverting Input Channel 4.
24	$A_{IN}3P$	Noninverting Input Channel 3.

ADS1211E CONFIGURATION



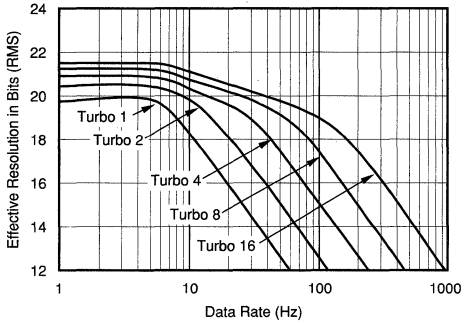
ADS1211E PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	$A_{IN}3N$	Inverting Input Channel 3.
2	$A_{IN}2P$	Noninverting Input Channel 2.
3	$A_{IN}2N$	Inverting Input Channel 2.
4	$A_{IN}1P$	Noninverting Input Channel 1.
5	$A_{IN}1N$	Inverting Input Channel 1.
6	AGND	Analog Ground.
7	V_{BIAS}	Bias Voltage Output, +3.3V nominal.
8	NIC	Not Internally Connected.
9	NIC	Not Internally Connected.
10	$\overline{CS}$	Chip Select Input.
11	$\overline{DSYNC}$	Control Input to Synchronize Serial Output Data.
12	X_{IN}	System Clock Input.
13	X_{OUT}	System Clock Output (for Crystal or Resonator).
14	DGND	Digital Ground.
15	DV_{DD}	Digital Supply, +5V nominal. Must be $\leq AV_{DD}$.
16	SCLK	Clock Input/Output for serial data transfer.
17	SDIO	Serial Data Input (can also function as Serial Data Output).
18	SDOUT	Serial Data Output.
19	$\overline{DRDY}$	Data Ready.
20	NIC	Not Internally Connected.
21	NIC	Not Internally Connected.
22	MODE	SCLK Control Input (Master = 1, Slave = 0).
23	AV_{DD}	Analog Supply, +5V nominal.
24	REF_{OUT}	Reference Output: +2.5V nominal.
25	REF_{IN}	Reference Input.
26	$A_{IN}4P$	Noninverting Input Channel 4.
27	$A_{IN}4N$	Inverting Input Channel 4.
28	$A_{IN}3P$	Noninverting Input Channel 3.

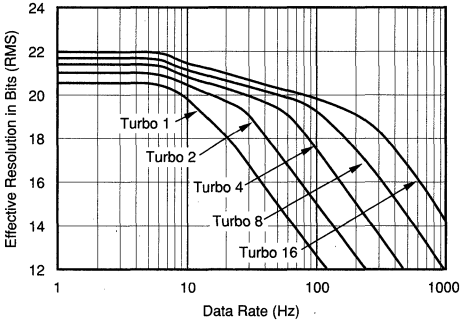
TYPICAL PERFORMANCE CURVES

At T = +25°C, AV_{DD} = DV_{DD} = +5V, f_{SC} = 10MHz, and V_{REF} = +2.5V, unless otherwise specified.

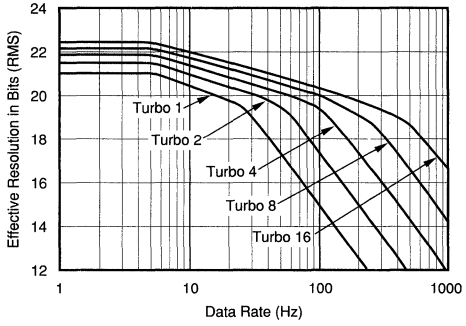
EFFECTIVE RESOLUTION vs DATA RATE
(1.25MHz Clock)



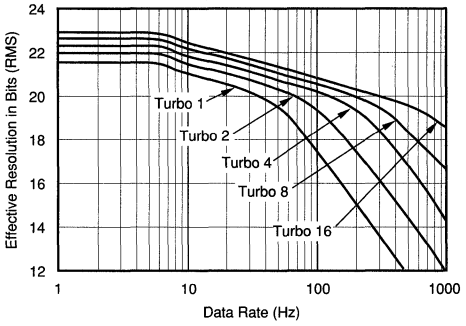
EFFECTIVE RESOLUTION vs DATA RATE
(2.5MHz Clock)



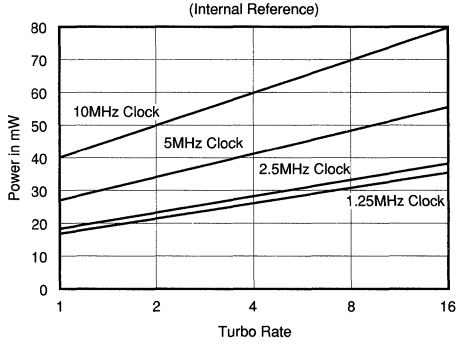
EFFECTIVE RESOLUTION vs DATA RATE
(5MHz Clock)



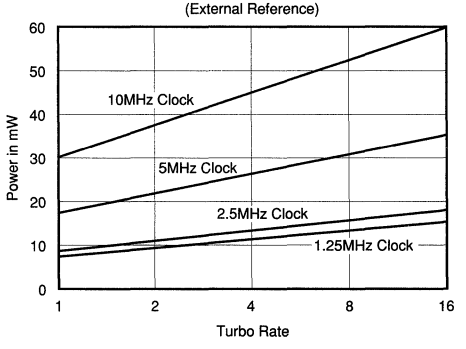
EFFECTIVE RESOLUTION vs DATA RATE
(10MHz Clock)



POWER vs TURBO RATE
(Internal Reference)



POWER vs TURBO RATE
(External Reference)



THEORY OF OPERATION

The ADS1210 and ADS1211 are 24-bit A/D converters consisting of a programmable gain amplifier (PGA); a second-order delta-sigma modulator; a programmable digital filter; a micro controller including the Instruction, Command, and Calibration registers; a serial interface; a clock generator, and the modulator control for the turbo mode of operation. The ADS1211 includes a 4-channel input multiplexer.

The 24-bit A/D converter of the ADS1210/11 is a precision, wide range, second-order delta-sigma architecture, capable of achieving very high resolution digital results. At lower resolutions, it achieves a 16kHz sample rate. In order to provide low system noise, common-mode rejection at 160dB and excellent power supply rejection, the design topology is based on a fully differential switched capacitor architecture. A unique feature of the ADS1210/11, called Turbo Mode, has the ability to externally control the sampling frequency of the input modulator. Normally, the modulator operates at 20kHz with a 10MHz system clock. The modulator sampling frequency can be programmed, through the control register, to oversample at 40kHz, 80kHz, 160kHz and 320kHz to improve the performance of the converter.

The programmable gain amplifier (PGA) has a gain range of 1 to 16, increasing the dynamic range and simplifying the interface to the more common transducers. The PGA gain is implemented by increasing the number of samples of the input capacitor from 20kHz for a gain of 1 to 320kHz for a gain of 16. Since the Turbo Mode and PGA functions are implemented by varying the oversampling frequency of the modulator, the combination of PGA gain and Turbo Mode rate is limited to 16. For example, at a Turbo Mode rate of 8 (160kHz at 10MHz) the PGA gain is limited to 2.

TURBO MODE RATE	PGA GAIN RANGES
1 (Normal Mode)	1, 2, 4, 8, 16
2	1, 2, 4, 8
4	1, 2, 4
8	1, 2
16	1

TABLE I. Turbo Mode Rate vs PGA Gain.

	FULL SCALE INPUT				
INPUT RANGE	G = 1	G = 2	G = 4	G = 8	G = 16
0/5V	5V	2.5V	1.25V	625mV	312.5mV
±10V	±10V	±5V	±2.5V	±1.25V	±625mV

TABLE II. Full-Scale Input vs Input Range and PGA Gain.

The ADS1210/11 modulator sampling rate is the system clock divided by 512 and is operational with system clocks from 0.5MHz to 10MHz. The combination of programmable modulator frequency, Turbo Mode, a PGA and a variable system clock allows a number of performance solutions in resolution, signal bandwidth, input range, and power consumption. Table III shows the effective resolution, data rate and PGA gain in the normal, Turbo Mode rate of 1 configuration with a system clock of 10MHz. Effective resolution is used as the figure of merit in the tables to simplify comparisons between data rate, gain and clock rate and is defined as the ratio of output rms noise to the to input full scale.

DATA RATE	–3dB FREQUENCY	EFFECTIVE RESOLUTION				
		G = 1	G = 2	G = 4	G = 8	G = 16
10	2.62Hz	22	22	22	22	21
25	6.55Hz	21	21	21	21	21
30	7.86Hz	21	21	21	21	21
50	13.1Hz	20	20	20	20	20
60	15.72Hz	20	20	20	20	20
100	26.2Hz	18	18	18	18	18
250	65.5Hz	15	15	15	15	15
500	131Hz	12	12	12	12	12
1000	262Hz	10	10	10	10	10

TABLE III. Effective Resolution vs Data Rate and PGA Gain, Turbo Mode Rate 1.

DIGITAL FILTER

The filter response is programmable for output data rates from 2.4Hz to 16kHz with a 10MHz clock and 0.24Hz to 1.6kHz with a 1MHz clock. The digital filter can also be used to provide notch frequencies for specific response nulls. In this way, power line frequencies such as 50Hz and 60Hz can be rejected.

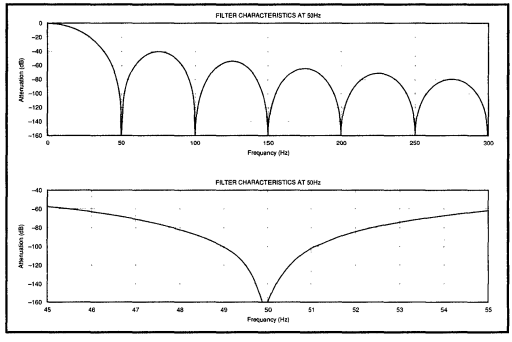


FIGURE 1. 50Hz Digital Filter Characteristics.

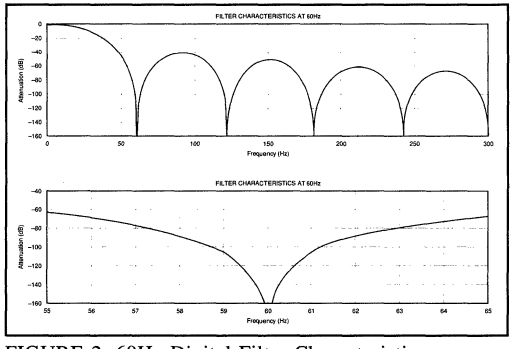


FIGURE 2. 60Hz Digital Filter Characteristics.

CALIBRATION

Four different kinds of calibration schemes are available to calibrate offset and gain errors. Self-calibration automatically shorts the inputs for offset calibration and connects the inputs to the reference for full-scale calibration. System calibration provides correction for system errors. The ADS1210/11 can be independently calibrated for user applied offset and full-scale inputs.

SERIAL INTERFACE

The ADS1210/11 is controlled through its serial interface and an 8-bit instruction code. This may be followed by a 32-bit command code which controls the device's internal configuration.

The serial interface is a synchronous serial interface which can operate via 2, 3, 4, or 5 "wires". The serial clock can be derived by the ADS1210/11 from its system clock (MODE = 1, master mode), or provided by an external source (MODE = 0, slave mode).

TURBO MODE

The ADS1210/11 has a programmable modulator sampling frequency function called Turbo Mode, by which the modulator sampling frequency can be increased by 2, 4, 8, or 16. With the increase of modulator sampling frequency, the system performance increases with some increase in power dissipation. In this manner, the ADS1210/11 can offer 20 bits of effective resolution at 1kHz conversion rate with 16 times increase of sampling frequency. The effective resolution at each of the Turbo Mode rates and data rates are shown in Table IV and the noise figures in Table V.

DATA RATE	TURBO MODE RATE 2	TURBO MODE RATE 4	TURBO MODE RATE 8	TURBO MODE RATE 16
5Hz	23	23	23	23
10Hz	22	23	23	23
20Hz	21	22	22	23
40Hz	21	22	22	23
50Hz	21	21	21	22
60Hz	21	21	21	21
100Hz	20	21	21	21
250Hz	17	19	20	21
500Hz	15	17	19	20
1000Hz	12	15	17	20
2000Hz			14	16

TABLE IV. Data Rate vs Effective Resolution and Turbo Mode Rate.

The Turbo Mode also provides the flexibility to use a low frequency system clock to save power, or to use a system clock derived from a common clock source and still maintain a high resolution. For example, if the system clock were reduced from 10MHz to 5MHz, the turbo 2x mode preserves the performance.

DATA RATE	TURBO MODE RATE 2	TURBO MODE RATE 4	TURBO MODE RATE 8	TURBO MODE RATE 16
5Hz	.69	.69	.69	.69
10Hz	.97	.79	.69	.69
20Hz	1.54	1.24	.79	.79
40Hz	1.69	1.36	1.17	.96
50Hz	2.27	1.76	1.51	1.37
60Hz	2.60	1.93	1.66	1.50
100Hz	4.85	2.53	2.14	1.94
250Hz	37.2	6.09	3.48	3.07
500Hz	208.66	26.70	6.67	4.38
1000Hz	1180	147.72	26.98	7.70
2000Hz				TBD

TABLE V. Data Rate vs Noise (μVrms) and Turbo Mode Rate.

DATA RATE	SYSTEM CLOCK	TURBO MODE RATE	EFFECTIVE RESOLUTION
10Hz	10MHz	1	22
10Hz	5MHz	2	22
10Hz	2.5MHz	4	22
10Hz	1.25MHz	8	22
10Hz	1.25MHz	16	23
60Hz	10MHz	1	20
60Hz	5MHz	2	20
60Hz	2.5MHz	4	20
60Hz	1.25MHz	8	20
60Hz	1.25MHz	16	21
100Hz	10MHz	1	18
100Hz	5MHz	2	18
100Hz	2.5MHz	4	18
100Hz	1.25MHz	8	18
100Hz	1.25MHz	16	19

TABLE VI. System Clock vs Turbo Mode Rate and Resolution.

SYSTEM CONFIGURATION

The Micro Controller (MC) consists of an ALU and a register bank. The MC has three states: power on reset, test, and convert. In the power on reset state, the MC resets all the registers to their default state, sets up the modulator to a stable state, and performs self-calibration at 10Hz cut-off frequency. In the test mode, the MC separates the modulator output and the decimator input so that the modulator output can be externally tested and an external test stream can be applied to the decimator. The convert mode is the normal mode of operation for the ADS1210/11.

INSR	Instruction Register	8 Bits
DOR	Data Output Register	24 Bits
CMR	Command Register	32 Bits
OCR	Offset Calibration Register	24 Bits
FCR	Full Scale Calibration Register	24 Bits

TABLE VII. ADS1210/11 Registers.

The ADS1210/11 has 5 registers, shown in Table VII that control the operation of the ADS1210/11 and contain the output data or calibration data. The instruction register (INSR) utilizes an 8-bit instruction code which determines what type of communication will occur next. The command register (CMR) has a 32-bit command code to set up the ADS1210/11 calibration mode, PGA gain, Turbo Mode, data format, digital filter decimation ratio (output data rate), and channel selection.

INSTRUCTION REGISTER

The instruction register is an 8-bit register which controls the serial interface to either read data or to write control codes to the other registers. The control code written to the instruction register determines the status of the next read or write operation and to which register this operation will be directed.

R/$\overline{W}$	MB1	MB0	0	A3	A2	A1	A0

TABLE VIII. Instruction Register.

Read/Write Bit—Write operations require that a 0 be written to the instruction register so that write operation actually takes place. Read instructions require a 1 to be written to this bit.

R/$\overline{W}$	
0	Write
1	Read

Multiple Bytes Access Bits—The Multiple Bytes Access bits control the word length when reading or writing to the ADS1210/11.

MB1	MB0	
0	0	1 Byte
0	1	2 Bytes
1	0	3 Bytes
1	1	4 Bytes

Internal Register Address—These 4 bits select the registers which will be read or written to during the next cycle of operation.

A3	A2	A1	A0	
0	0	0	0	Data Output Register Byte 2
0	0	0	1	Data Output Register Byte 1
0	0	1	0	Data Output Register Byte 0
0	1	0	0	Command Register Byte 3
0	1	0	1	Command Register Byte 2
0	1	1	0	Command Register Byte 1
0	1	1	1	Command Register Byte 0
1	0	0	0	Offset Cal Register Byte 2
1	0	0	1	Offset Cal Register Byte 1
1	0	1	0	Offset Cal Register Byte 0
1	1	0	0	Full Scale Cal Register Byte 2
1	1	0	1	Full Scale Register Byte 1
1	1	1	0	Full Scale Cal Register Byte 0

COMMAND REGISTER

The command register word is comprised of 32 bits of information in 4 bytes of 8 bits each. The command register controls all of the functionality of the ADS1210/11. The new configuration takes effect on the negative transition of the last bit in the last byte of data being written to the command register.

MSB			Byte3				
V_{BIAS}	V_{REF}	DF	U/$\overline{B}$	BD	MSB	SDL	$\overline{DRDY}$
			Byte2				
MD2	MD1	MD0	G2	G1	G0	CH1	CH0
			Byte1				
SF2	SF1	SF0	DR12	DR11	DR10	DR9	DR8
			Byte0				LSB
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

TABLE IX. Command Register.

Biasing Voltage Bit—The Biasing Voltage bit turns on a +3.3V bias voltage for use with a voltage divider when applying a ±10V input signal.

V_{BIAS}	+3.3V	
0	Off	Default
1	On	

Internal Reference Bit—The internal reference bit turns the internal reference on and off allowing an external reference to be used.

REF	+2.5V	
0	Off	
1	On	Default

Data Format Bit—The Data Format bit programs the output data to either be in a two's compliment or in an offset binary format.

DF		
0	Two's Compliment	Default
1	Offset Binary	

Unipolar/Bipolar Input Bit—The Bipolar/Unipolar bit sets the conversion mode.

U/$\overline{B}$		
0	Bipolar	Default
1	Unipolar	

Byte Order Bit for Data Output Register—The Byte Order bit determines the order in which the output data bytes will be read, either as MSB byte or as LSB byte first.

BD		
0	Byte Access From MSB Byte to LSB Byte	Default
1	Byte Access From LSB Byte to MSB Byte	

Data Order Bit for Data Output Register—The Data Order bit determines the order in which the output data will be read, either as MSB first or as LSB first.

MSB		
0	MSB First	Default
1	LSB First	

Serial Data Line Bit—The Serial Data Line bit is used to program the SDIO line as a serial input and output when the bit is set to 0. Setting the bit to 1 programs the SDIO line to be a serial input and to use SDOUT for serial output data.

SDL		
0	SDIO Line Used for I/O	Default
1	SDIO Line Used for Input, SDOUT Line Used for Output	

Data Ready (Read Only)—The Data Ready bit is a read only bit indicating the end of conversion.

$\overline{DRDY}$	
0	Data Ready
1	Data Not Ready

Operation Mode Bits—The Operating Mode bits control the calibration functions of the ADS1210/11. In operation the normal mode is used to perform conversions. The Self Calibration mode is a one-step calibration sequence that calibrates both the offset and full scale.

The System Offset Calibration is performed at the selected gain on the offset voltage on the input to the PGA during the calibration sequence. If the Instruction Register is set to Write mode, then data may also be written to the Offset Calibration Register. The System Full-Scale Calibration is performed at the selected gain on the voltage on the input to the PGA during the calibration sequence. If the Instruction register is set to Write mode, then data may also be written to the full-scale calibration register.

The Pseudo System Calibration provides offset correction for the selected channel and calibration to the internal reference. The Background Calibration provides continuous self-calibration of the full scale and offset. Background calibration occurs as part of the conversion process, extending the conversion time and slowing the data output rate by a factor of six.

MD2	MD1	MD0	
0	0	0	Normal Mode
0	0	1	Self Cal
0	1	0	System Offset Cal
0	1	1	System Full-Scale Cal
1	0	0	Pseudo System Cal
1	0	1	Background Cal
1	1	0	Sleep
1	1	1	Reserved for Future Use

PGA Gain Bits—The PGA Gain bits set the gain of the Programmable Gain Amplifier.

G2	G1	G0	GAIN	
0	0	0	1	Default
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	

Channel Selection Bits—The Channel Selection bits determine the differential analog input to be converted. For the ADS1210, the input channel must always be channel 1.

CH1	CH0		
0	0	Channel 1	Default
0	1	Channel 2	
1	0	Channel 3	
1	1	Channel 4	

Sampling Frequency Bits—The Sampling Frequency bits select the modulator sampling frequency as a function of the system clock. The modulator sampling rate can be determined by the following equation:

$$\frac{f_{SC} \bullet \text{Turbo Mode}}{512}$$

where f_{SC} is the system clock frequency (X_{IN} clock). For example, in th normal mode of operation (Turbo Mode equals one), the modulator sampling rate is 20kHz.

SF2	SF1	SF0	TURBO MODE RATE	PGA RANGE	
0	0	0	1	1-16	Default
0	0	1	2	1-8	
0	1	0	4	1-4	
0	1	1	8	1-2	
1	0	0	16	1	

Decimation Ratio—The ADS1210/11 decimator uses a $Sinc^3$ digital filter for easy programmability. The 13 bits used to program the filter determine the cut-off frequency, the position of the first notch and the data rate. The data rate for the ADS1210/11 is determined by the following equation:

$$\frac{f_{SC} \bullet \text{Turbo Mode}}{512 \bullet \text{Decimation Ratio}}$$

where f_{SC} is the system clock frequency (X_{IN} clock). Table X gives decimation ratios for various data rates with the ADS1210/11 operating in the normal mode of operation (Turbo Mode equals one).

DR12	DR11	DR10	DR9	DR8	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	DECIMATION RATIO	DATA(1) RATE (Hz)	
0	0	0	0	0	0	0	0	1	0	1	0	0	20	1000	Default
0	0	1	1	1	1	1	0	1	0	0	0	0	1953	10	
0	0	0	1	1	0	0	1	0	0	0	0	0	977	20	
0	0	0	0	1	1	0	0	1	0	0	0	0	391	50	
0	0	0	0	1	0	1	1	0	0	0	0	1	326	60	
0	0	0	0	0	1	1	0	0	1	0	0	0	195	100	
0	0	0	0	0	0	1	0	1	0	0	0	0	78	250	
0	0	0	0	0	0	0	1	0	1	0	0	0	39	500	

NOTE: (1) System Clock = 10MHz.

Table X. Decimation Ratio.

Default Values—Table XI shows the default condition for the Command Register.

MSB			Byte3				
0	1	0	0	0	0	0	x
			Byte2				
0	0	0	0	0	0	0	0
			Byte1				
0	0	0	0	0	0	0	0
			Byte0				LSB
0	0	0	1	0	1	0	0

TABLE XI. Command Register Default Condition.

Offset Calibration Register—The ADS1210/11 has a 24-bit read/write calibration register that is used for the offset coefficients. After calibration, the results of the operation are stored in this register and are available to the user. This data can be used in subsequent processing, or if multiple offset calibrations are performed, the data can be averaged and written back to the register to provide a high accuracy zero point.

MSB			Byte2				
OR23	OR22	OR21	OR20	OR19	OR18	OR17	OR16
			Byte1				
OR15	OR14	OR13	OR12	OR11	OR10	OR9	OR8
			Byte0				LSB
OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0

TABLE XII. Offset Register.

Full-Scale Calibration Register—The ADS1210/11 has a 24-bit read/write calibration register that is used for the full-scale coefficients. After calibration, the results of the operation are stored in this register and are available to the user. This data can be used in subsequent processing, or if multiple full-scale calibrations are performed, the data can be averaged and written back to the register to provide a high accuracy full-scale point.

MSB			Byte2				
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
			Byte1				
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8
			Byte0				LSB
FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0

TABLE XIII. Full-Scale Register.

SERIAL INTERFACING

The converter's SSI (synchronous serial interface) allows a variety of serial interface configurations. Figure 3 shows an interface to a 8xCSI microprocessor and Figure 4 shows a two-wire interface with a Motorola 68HC11. Figures 5 and 6 show two different types of isolated interfaces. Figure 7 shows a typical timing diagram for SPI (serial peripheral interface) communications.

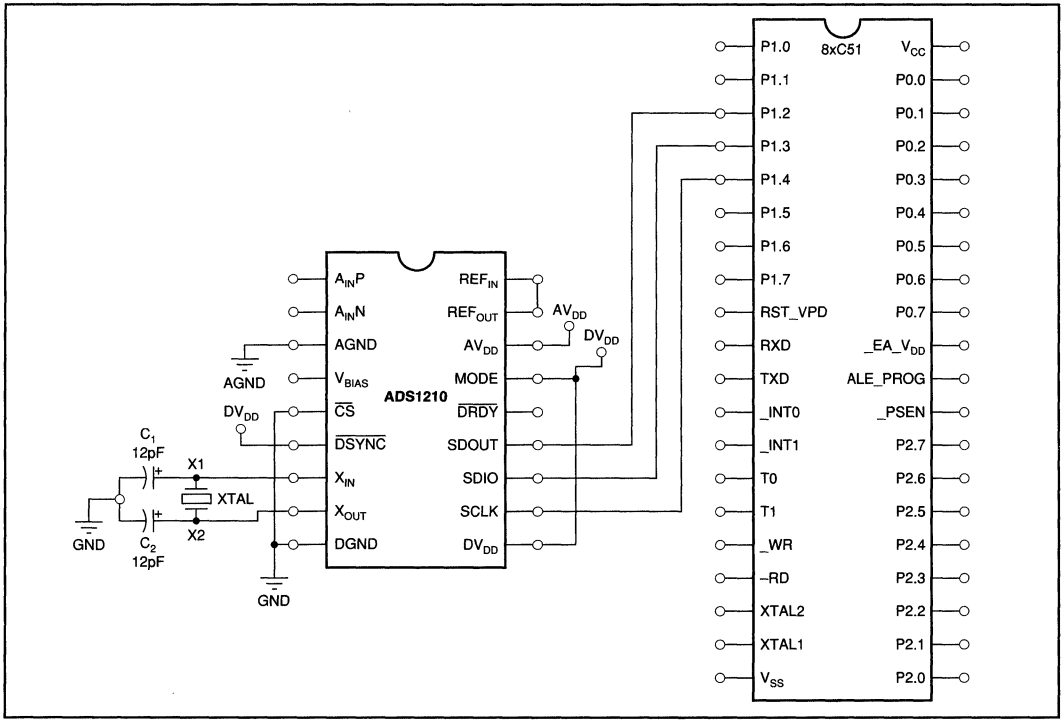


FIGURE 3. Three-Wire Interface With 8xC51 Processors.

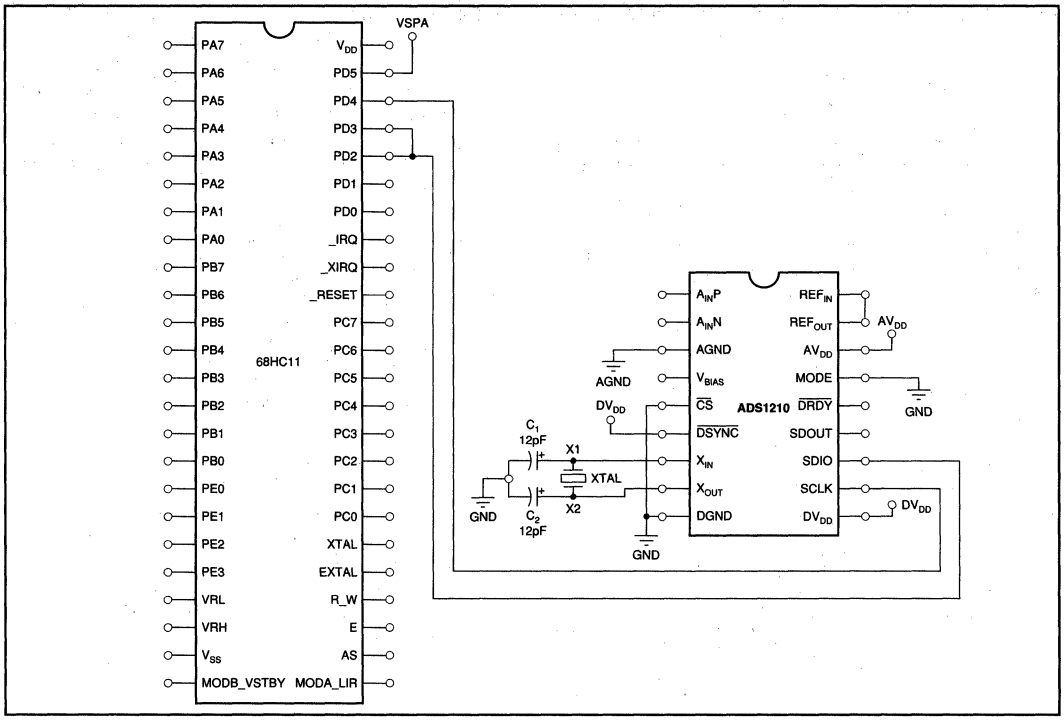


FIGURE 4. Two-Wire Interface With 68HC11 Processors.

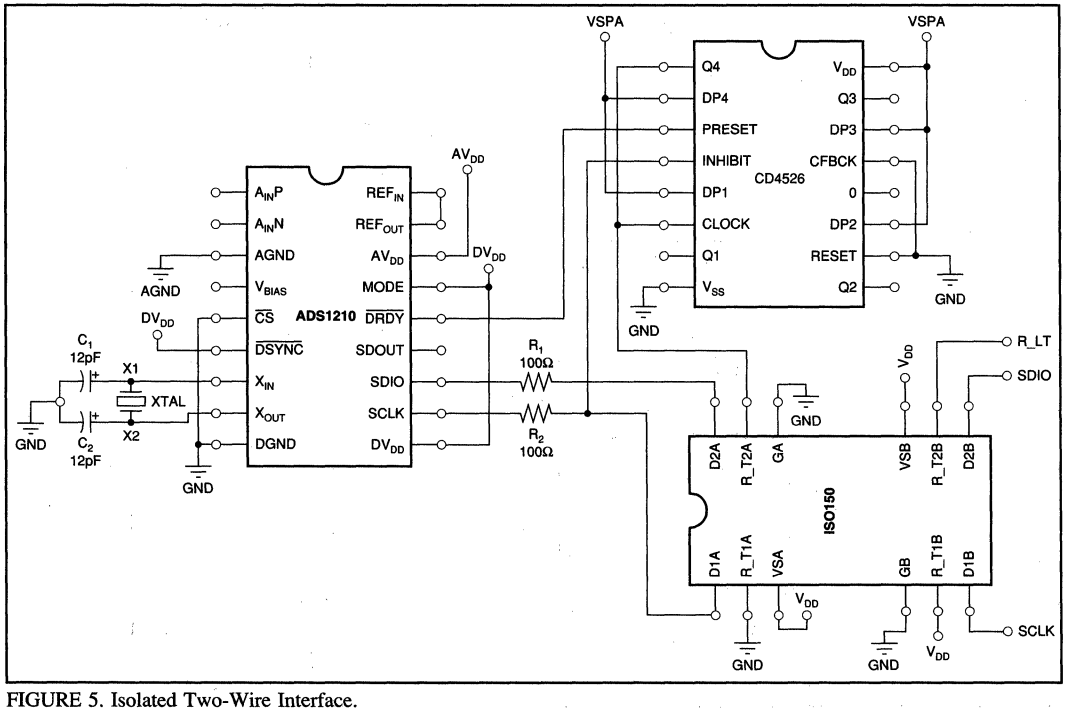


FIGURE 5. Isolated Two-Wire Interface.

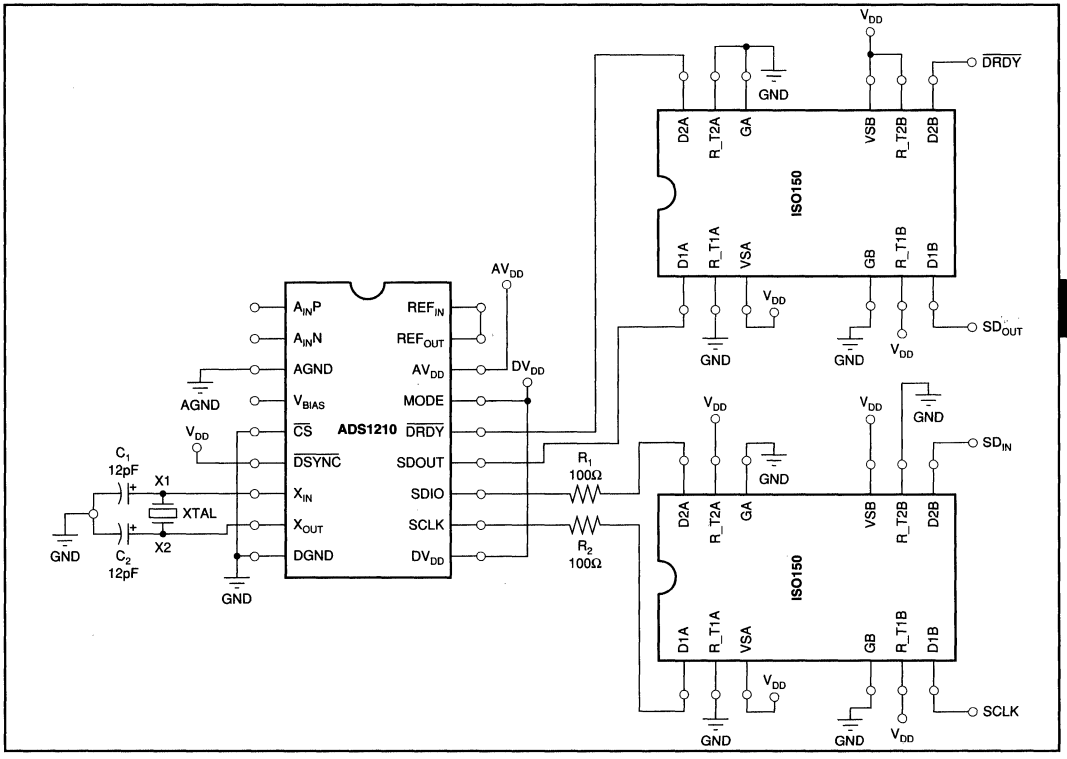


FIGURE 6. Isolated Four-Wire Interface.

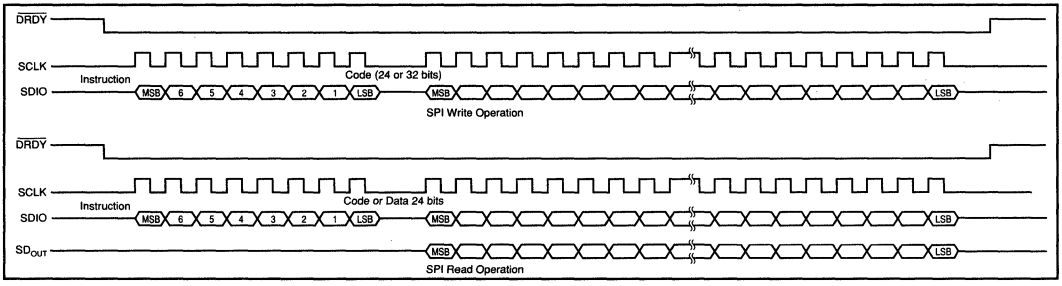


FIGURE 7. SPI Timing.

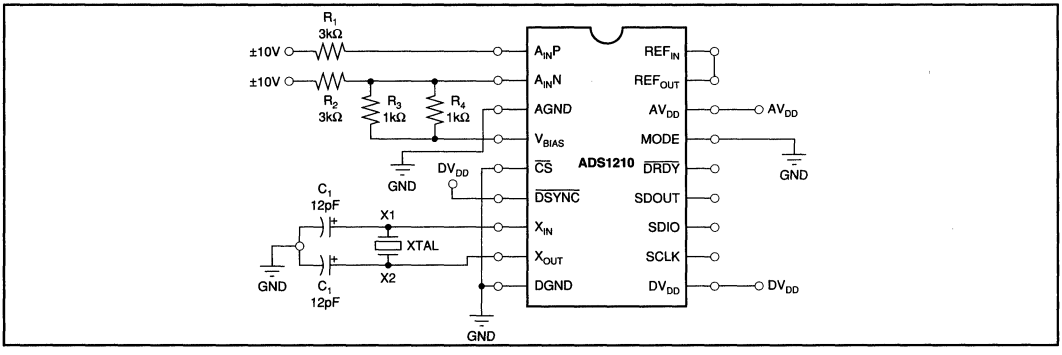


FIGURE 8. Differential ±10V Input Configuration. (For lower power dissipation: $R_1 = R_2 = 9k\Omega$, $R_3 = R_4 = 3k\Omega$.)

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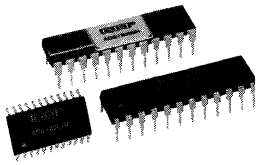


ADS7800

12-Bit 3µs Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 333k SAMPLES PER SECOND
- STANDARD ±10V AND ±5V INPUT RANGES
- DC PERFORMANCE OVER TEMP:
  No Missing Codes
  1/2LSB Integral Linearity Error
  3/4LSB Differential Linearity Error
- AC PERFORMANCE OVER TEMP:
  72dB Signal-to-Noise Ratio
  80dB Spurious-free Dynamic Range
  –80dB Total Harmonic Distortion
- INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND 3-STATE OUTPUTS
- POWER DISSIPATION: 215mW max
- PACKAGE: 24-Pin Single-wide DIP
  24-Lead SOIC

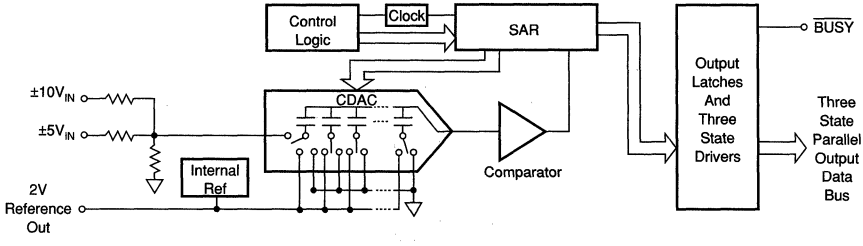
DESCRIPTION

The ADS7800 is a complete 12-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a –12V or –15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and –40°C to +85°C temperature ranges.



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SPECIFICATIONS

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH MIN	ADS7800JP/JU/AH TYP	ADS7800JP/JU/AH MAX	ADS7800KP/KU/BH MIN	ADS7800KP/KU/BH TYP	ADS7800KP/KU/BH MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V/±5V			*		V
Impedance	±10V Range	4.4	6.3	8.1	*	*	*	kΩ
	±5V Range	2.9	4.2	5.4	*	*	*	kΩ
THROUGHPUT SPEED								
Conversion Time	Conversion Alone		2.5	2.7		*	*	µs
Complete Cycle	Acquisition + Conversion		2.6	3.0		*	*	µs
Throughput Rate		333	380		*	*		kHz
DC ACCURACY								
Full Scale Error[1]				±0.50			±0.35	%
Full Scale Error Drift			6			*		ppm/°C
Integral Linearity Error				±1			±1/2	LSB[2]
Differential Linearity Error				±1			±3/4	LSB
No Missing Codes			Guaranteed			Guaranteed		
Bipolar Zero[1]				±4			±2	LSB
Bipolar Zero Drift			1			*		ppm/°C
Power Supply Sensitivity								
	$-16.5V < -V_S < -13.5V$			±1/2			*	LSB
	$-12.6V < -V_S < -11.4V$			±1/2			*	LSB
	$+4.75V < V_S < +5.25V$			±1			±1/2	LSB
Transition Noise[3]			0.1			*		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 47kHz	74	77		77	80		dB[4]
Total Harmonic Distortion	f_{IN} = 47kHz		–77	–74		–80	–77	dB
Two-tone Intermodulation Distortion	f_{IN1} = 24.4kHz (–6dB) f_{IN2} = 28.5kHz (–6dB)		–77	–74		–80	–77	dB
Signal-to-(Noise + Distortion) Ratio	f_{IN} = 47kHz	67	70		69	72		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 47kHz	68	71		70	73		dB
SAMPLING DYNAMICS								
Aperture Delay			13			*		ns
Aperture Jitter			150			*		ps, rms
Transient Response[5]			130			*		ns
Overvoltage Recovery[6]			150			*		ns
INTERNAL REFERENCE VOLTAGE								
Voltage		1.9	2.0	2.1	*	*	*	V
Source Current Available for External Loads			10			*		µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		+5.3	*		*	V
I_{IL}		–5			*			µA
I_{IH}		+5			*			µA
DIGITAL OUTPUTS								
Data Format				Parallel, 12-bit or 8-bit/4-bit				
Data Coding				Binary Offset Binary				
V_{OL}	I_{SINK} = 1.6mA	0.0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5.0	*		*	V
$I_{LEAKAGE}$ (High-Z State)			±0.1	±5		*	*	µA
POWER SUPPLIES								
Rated Voltage								
$-V_S$		–11.4	–15	–16.5	*	*	*	V
V_S (V_{SA} and V_{SD})		+4.75	+5.0	+5.25	*	*	*	V
Current								
$-I_S$			3.5	6		*	*	mA
I_S			18	25		*	*	mA
Power Consumption			135	215		*	*	mW

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH			ADS7800KP/KU/BH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	JP/JU/KP/KU	0		+70	*		*	°C
	AH/BH	–40		+85	*		*	°C
Operating	JP/KP/JU/KU	–40		+85	*		*	°C
Storage		–65		+150	*		*	°C

* Same as specification for ADS7800JP/JU/AH.

NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the ±5V range, 1LSB = 4.88mV for the ±10V range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C. (4) All specifications in dB are referred to a full-scale input, either ±10V or ±5V. (5) For full scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after 2 x F_S input overvoltage.

PIN ASSIGNMENTS

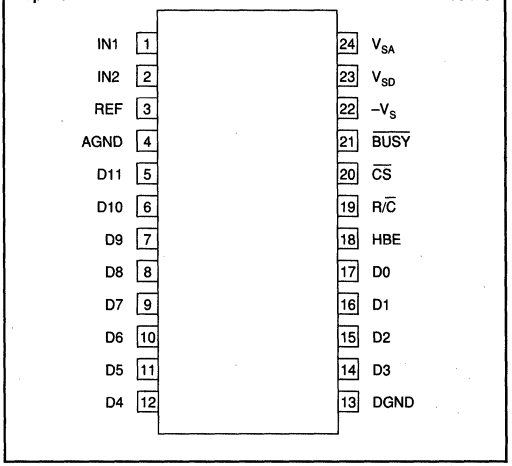
PIN #	NAME	DESCRIPTION
1	IN1	±10V Analog Input. Connected to GND for ±5V range.
2	IN2	±5V Analog Input. Connected to GND for ±10V range.
3	REF	+2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads.
4	AGND	Analog Ground. Connect to pin 13.
5	D11	Data Bit 11. Most Significant Bit (MSB).
6	D10	Data Bit 10.
7	D9	Data Bit 9.
8	D8	Data Bit 8.
9	D7	Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.
10	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
11	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
12	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
13	DGND	Digital Ground. Connect to pin 4.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH.
18	HBE	High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion.
19	R/$\overline{C}$	Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and $\overline{BUSY}$ is HIGH.
20	$\overline{CS}$	Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.
21	$\overline{BUSY}$	Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode.
22	$-V_S$	Negative Power Supply. –12V or –15V. Bypass to GND.
23	V_{SD}	Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND.
24	V_{SA}	Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND.

ABSOLUTE MAXIMUM RATINGS

$-V_S$ to ANALOG COMMON	–16.5V
V_S to DIGITAL COMMON	+7V
Pin 23 (V_{SD}) to Pin 24 (V_{SA})	±0.3V
ANALOG COMMON to DIGITAL COMMON	±1V
Control Inputs to DIGITAL COMMON	–0.3 to V_S + 0.3V
Analog Input Voltage	±20V
Maximum Junction Temperature	160°C
Internal Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}:	
Plastic DIP	100°C/W
SOIC	100°C/W
Ceramic	50°C/W

PIN CONFIGURATION

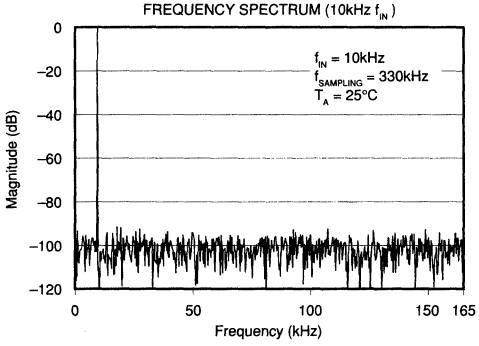
Top View **DIP/SOIC**



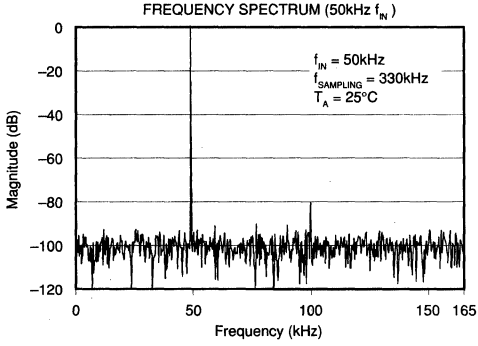
TYPICAL PERFORMANCE CURVES

At $+V_S$ = +5V, $-V_S$ = −15V, and T_A = +25°C, unless otherwise noted. All plots use 1024 point FFTs.

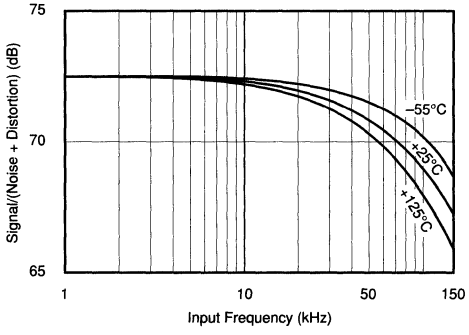
FREQUENCY SPECTRUM (10kHz f_{IN})



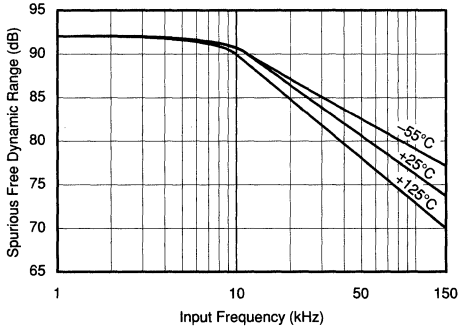
FREQUENCY SPECTRUM (50kHz f_{IN})



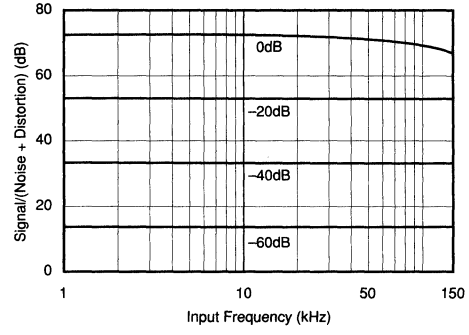
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



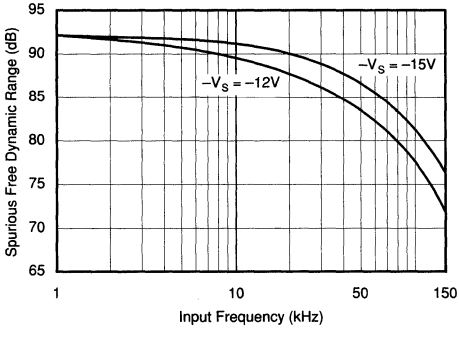
SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



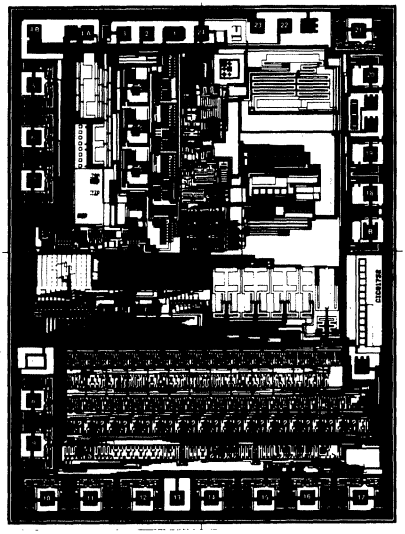
SIGNAL/(NOISE + DISTORTION) vs
FREQUENCY AND AMPLITUDE



SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND NEGATIVE SUPPLY VOLTAGE



DICE INFORMATION



ADS7800 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	±10V Analog Input	15	D_2
2	±5V Analog Input	16	D_1
3	+2V Reference Output	17	D_0
4a	Analog Ground Sense[1]		
4b	Analog Ground [1]		
5	D_{11}(MSB)	18	HBE
6	D_{10}	19	R/E
7	D_9		
8	D_8		
9	D_7	20	$\overline{CS}$
10	D_6	21	$\overline{BUSY}$
11	D_5		
12	D_4	22	$-V_S$
13	Digital Ground	23	$+V_{SD}$
14	D_3	24	V_{SA}

NOTE: Bond pads 4 and 5 to same pin.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	136 x 181 ±5	3.45 x 4.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10

ORDERING INFORMATION

MODEL	INTEGRAL LINEARITY ERROR (LSB)	SIGNAL-TO-(NOISE+DISTORTION) RATIO (dB min)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7800JP	±1	67	0 to +70	Plastic DIP
ADS7800KP	±1/2	69	0 to +70	Plastic DIP
ADS7800JU	±1	67	0 to +70	Plastic SOIC
ADS7800KU	±1/2	69	0 to +70	Plastic SOIC
ADS7800AH	±1	67	–40 to +85	Ceramic DIP
ADS7800BH	±1/2	69	–40 to +85	Ceramic DIP

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS7800JP	24-Pin Plastic DIP	243
ADS7800JP	24-Pin Plastic DIP	243
ADS7800JU	24-Pin Plastic SOIC	239
ADS7800KU	24-Pin Plastic SOIC	239
ADS7800AH	24-Pin Ceramic DIP	245
ADS7800BH	24-Pin Ceramic DIP	245

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

THEORY OF OPERATION

The ADS7800 combines the advantages of advanced CMOS technology (logic density, stable capacitors, and good analog switches) with Burr-Brown's proven skills in laser-trimmed thin-film resistors to provide a complete sampling A/D converter.

A basic charge-redistribution successive approximation architecture converts analog input voltages into digital words. Figure 1 shows the operation of a simplified three bit charge redistribution A/D. Precision laser-trimmed scaling resistors at the input divide standard input ranges (±10V or ±5V for the ADS7800) into levels compatible with the CMOS characteristics of the internal capacitor array.

While in the sampling mode, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal, and the remaining array switches (S_2 and S_3) are set to position "R" to provide an accurate bipolar offset from the reference source REF. At the same time, switch S_C is also in the closed position to auto-zero any offset errors in the CMOS comparator.

When a convert command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command, switches S_2 and S_3 are opened to trap an offset charge, and switch S_C is opened to float the comparator input. The charge trapped on the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2 and S_3 to positions "R" (to connect to REF) or "G" (to connect to GND) successively, changing the voltage generated at the comparator input node.

The first approximation connects the MSB capacitor via switch S_1 to REF, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G", and moves on to make the next approximation by connecting S_2 to REF and S_3 to GND. When the three successive approximation steps are made for this simple converter, the voltage level at the comparator will be within 1/2LSB of GND, and the data output word will be based on reading the positions of S_1, S_2 and S_3.

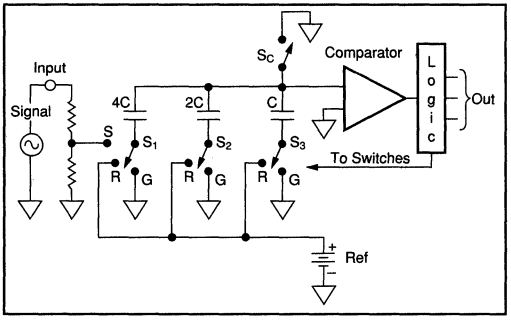


FIGURE 1. 3-Bit Charge Redistribution A/D.

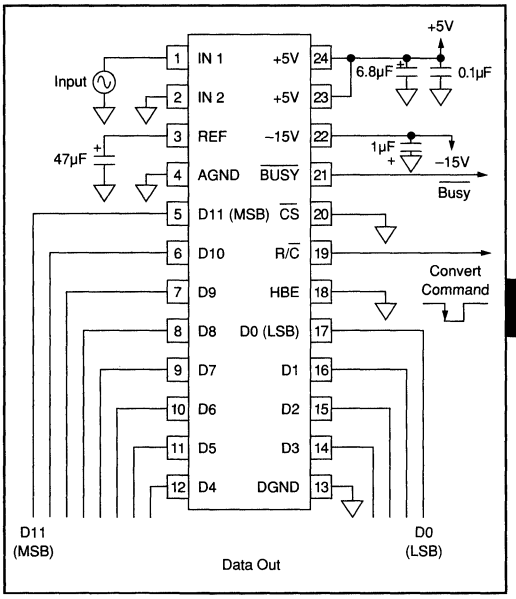


FIGURE 2. Basic ±10V Operation.

OPERATION

BASIC OPERATION

Figure 2 shows the simple hookup circuit required to operate the ADS7800 in a ±10V range in the Convert Mode. A convert command arriving on pin 19, R/$\overline{C}$, (a pulse taking pin 19 LOW for a minimum of 40ns) puts the ADS7800 in the hold mode, and a conversion is started. Pin 21, $\overline{BUSY}$, will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output latches. Thus, the rising edge of the signal on pin 21 can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits input lines. This means that pulses on pin 19 are ignored, so that new conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the ADS7800.

In the Read Mode, the input to pin 19 is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ on pin 19 will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the ADS7800 in a hold mode, and initiates a new conversion.

The ADS7800 will begin acquiring a new sample as soon as the conversion is completed, even before the $\overline{BUSY}$ output rises on pin 21, and will track the input signal until the next conversion is started, whether in the Convert Mode or the Read Mode.

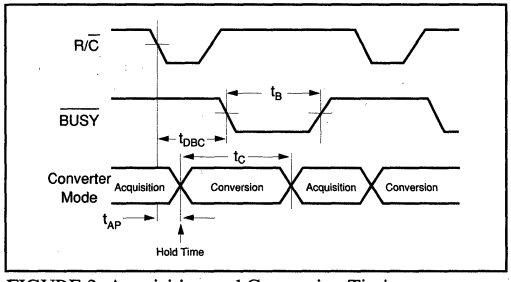


FIGURE 3. Acquisition and Conversion Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

TABLE I. Acquisition and Conversion Timing.

For use with an 8-bit bus, the data can be read out in two bytes under the control of pin 18, HBE. With a LOW input on pin 18, at the end of a conversion, the 8 LSBs of data are loaded into the latches on pins 9 through 12 and 14 through 17. Taking pin 18 HIGH then loads the 4 MSBs on pins 14 through 17, with pins 9 through 12 being forced LOW.

ANALOG INPUT RANGES

The ADS7800 offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration. (See Figures 4 and 5, or 10 and 11.)

CONTROLLING THE ADS7800

The ADS7800 can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the ADS7800 may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in Table II.

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	OPERATION
1	X	X	1	None - Outputs in Hi-Z State.
0	1↓0	0	1	Holds Signal and Initiates Conversion.
0	1	0	1	Output Three-State Buffers Enabled once Conversion has Finished.
0	1	1	1	Enable Hi-Byte in 8-bit Bus Mode.
0	1↓0	1	1	Inhibit Start of Conversion.
0	0	1	1	None - Outputs in Hi-Z State.
X	X	X	0	Conversion in Progress. Outputs Hi-Z State. New Conversion Inhibited until Present Conversion has Finished.

TABLE II. Control Line Functions.

For stand-alone operation, control of the ADS7800 is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition on R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and $\overline{BUSY}$ is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain LOW a minimum of 40ns.

Figure 6 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access of the data after completion of the conversion.

Figure 7 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

CONVERSION START

A conversion is initiated on the ADS7800 only by a negative transition occurring on R/$\overline{C}$, as shown in Table I. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$. Timing relationships for start of conversion are illustrated in Figure 8.

The $\overline{BUSY}$ output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

INTERNAL CLOCK

The ADS7800 has an internal clock that is factory trimmed to achieve a typical conversion time of 2.47µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3µs.

READING DATA

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{C}$ is HIGH, $\overline{BUSY}$ is HIGH and $\overline{CS}$ is LOW. Upon satisfaction of these conditions, the data lines are enabled according to the state of HBE. See Figure 9 and Table III for timing relationships and specifications.

CALIBRATION

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS7800 as shown in Figures 10 and 11.

If adjustment of offset and full scale is not required, connections as shown in Figures 4 and 5 should be used.

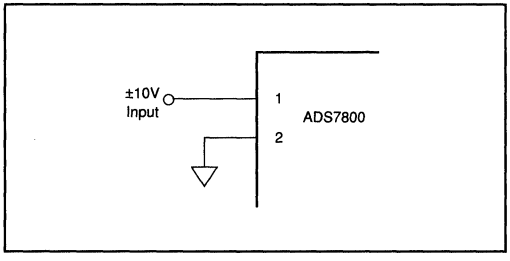


FIGURE 4. ±10V Range Without Trims.

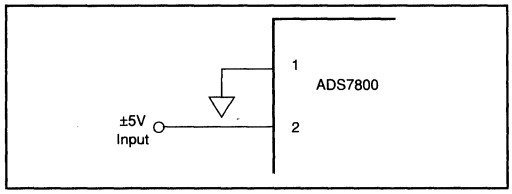


FIGURE 5. ±5V Range Without Trims.

CALIBRATION PROCEDURE

First, trim offset, by applying at the input (pin 1 or 2) the mid-point transition voltage (–2.44mV for the ±10V range, –1.22mV for the ±5V range.) With the ADS7800 converting continually, adjust potentiometer R_1 until the MSB (D11 on pin 5) is toggling alternately HIGH and LOW.

Next adjust full scale, by applying at the input a DC input signal that is 3/2LSB below the nominal full scale voltage (+9.9927V for the ±10V range, +4.9963V for the ±5V range.) With the ADS7800 converting continually, adjust R_2 until the LSB (D0 on pin 17) is toggling HIGH and LOW with all of the other bits HIGH.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADS7800, system design problems such as ground path resistance and contact resistance become very important.

ANALOG SIGNAL SOURCE IMPEDANCE

The input resistance of the ADS7800 is 6.3kΩ or 4.2kΩ (for the ±10V and ±5V ranges respectively.) To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal.

Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the ADS7800, to maximize accuracy on the chip. They should be connected together as close as possible to the unit.

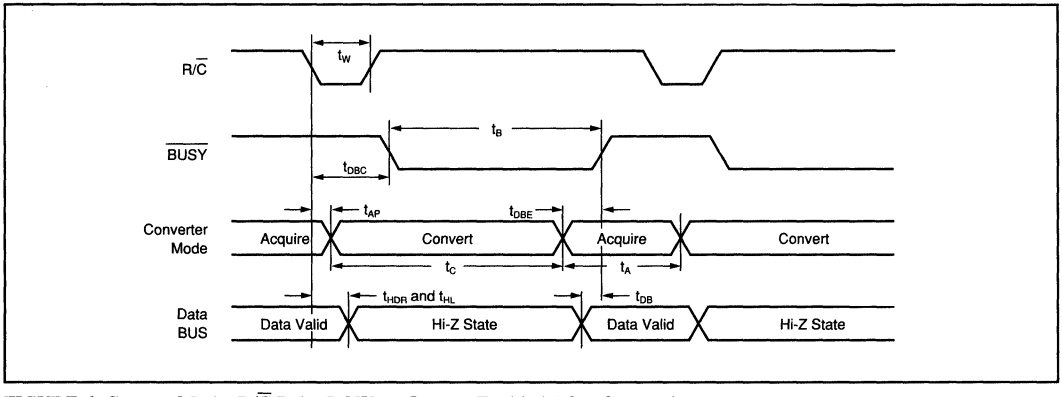


FIGURE 6. Convert Mode: R/$\overline{C}$ Pulse LOW — Outputs Enabled After Conversion.

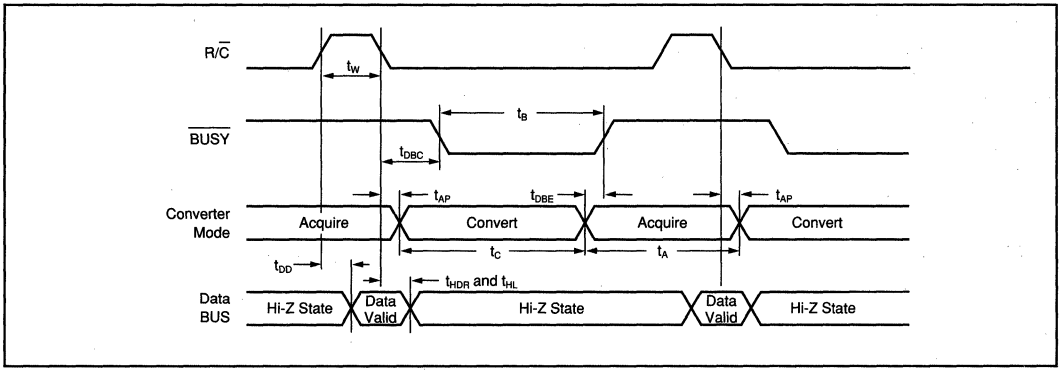


FIGURE 7. Read Mode: R/$\overline{C}$ Pulse HIGH— Outputs Enabled Only When R/$\overline{C}$ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	R/$\overline{C}$ Pulse Width	40	10		ns
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ LOW		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		ns
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
t_A+t_C	Throughput Time		2.6	3.0	µs
t_{HDR}	Valid Data Held After R/$\overline{C}$ LOW	20	50		ns
t_S	$\overline{CS}$ or HBE LOW before R/$\overline{C}$ Falls	25	5		ns
t_H	$\overline{CS}$ or HBE LOW after R/$\overline{C}$ Falls	25	0		ns
t_{DD}	Data Valid from $\overline{CS}$ LOW, R/$\overline{C}$ HIGH, and HBE in Desired State (Load = 100pF)		65	150	ns
t_{HDR}	Valid Data Held After R/$\overline{C}$ Low	20	50		ns
t_{HL}	Delay to Hi-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown)		50	150	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

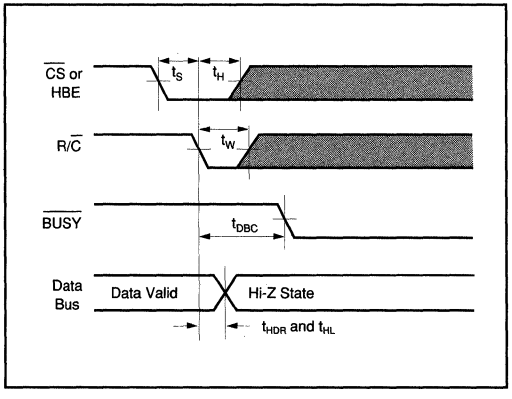


FIGURE 8. Conversion Start Timing.

Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain maximum system accuracy, both should be well isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the ADS7800.

The V_S pins (23 and 24) should be connected together and bypassed with a parallel combination of a 6.8µF tantalum capacitor and a 0.1µF ceramic capacitor located close to the converter to obtain noise-free operation. (See Figure 2.) The $-V_S$ pin 22 should be bypassed with a 1µF tantalum capacitor, again as close as possible to the ADS7800.

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the

converter if at all possible. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the ADS7800, which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the ADS7800 as possible.

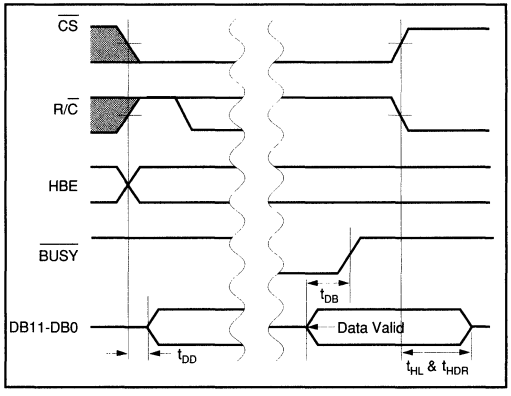


FIGURE 9. Read Cycle Timing.

REFERENCE BYPASS

Pin 3 (REF) should be bypassed with a 22µF to 47µF tantalum capacitor. A rated working voltage of 2V or more is acceptable here. This pin is used to enhance the system accuracy of the internal reference circuit, and is not recommended for driving external signals. If there are important system reasons for using the ADS7800 reference externally, the output of pin 3 must be appropriately buffered.

"HOT SOCKET" PRECAUTION

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the ADS7800 may "Latch Up" and draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to power the ADS7800 only after it has been socketed.

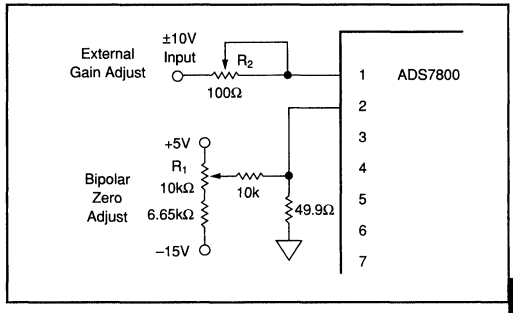


FIGURE 10. ±10V Range With External Trims.

MINIMIZING "GLITCHES"

Coupling of external transients into an A/D converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using the ADS7800. These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the ADS7800 has an internal sample/hold function, the signal that puts it into the hold state (R/$\overline{C}$ going LOW) is critical, as it would be on any sample/hold amplifier. The R/$\overline{C}$ falling edge should be sharp and have minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitching the ADS7800 while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/$\overline{C}$, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).

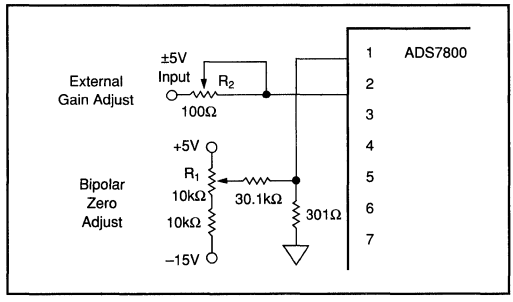


FIGURE 11. ±5V Range With External Trims.

Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the ADS7800. If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{BUSY}$ output can be used to enable the buffer.

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{C}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the ADS7800.

Finally, in multiplexed systems, the timing on when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{C}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the ADS7800 input. Whenever possible, it is safer to wait until the conversion is completed before switching the multiplexer. The extremely fast acquisition time and conversion time of the ADS7800 make this practical in many applications.

INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range Defined As:		±10V	±5V
Analog Input Connected to Pin		1	2
Pin Connected to GND		2	1
One Least Significant Bit (LSB)	FSR/2^{12}	20V/2^{12}	10V/2^{12}
		4.88mV	2.44mV
OUTPUT TRANSITION VALUES			
FFE_H to FFF_H	+Full Scale	+10V–3/2LSB	+5V–3/2LSB
		+9.9927V	+4.9963V
$7FF_H$ to 800_H	Mid Scale	0V–1/2LSB	0V–1/2LSB
	(Bipolar Zero)	–2.44mV	–1.22mV
000_H to 001_H	–Full Scale	–10V+1/2LSB	–5V+1/2LSB
		–9.9976V	–4.9988V

TABLE IV. Input Voltages, Transition Values, and LSB Values.

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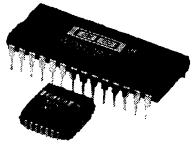


ADS7803

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

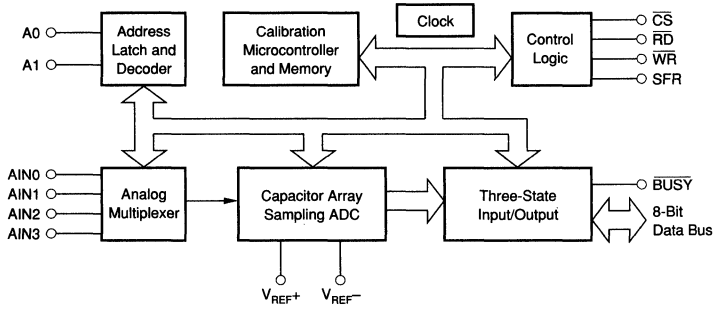
FEATURES

- LOW POWER: 10mW plus Power Down
- SIGNAL-TO-(NOISE + DISTORTION) RATIO OVER TEMPERATURE:
  69dB min with f_{IN} = 1kHz
  66dB min with f_{IN} = 50kHz
- FAST CONVERSION TIME: 8.5µs Including Acquisition (117kHz Sampling Rate)
- DC PERFORMANCE OVER TEMPERATURE:
  ±3/4 LSB max Total Error
  ±1/4 LSB max Channel Mismatch
- FOUR-CHANNEL INPUT MULTIPLEXER
- SINGLE SUPPLY: +5V
- PIN COMPATIBLE WITH ADC7802

DESCRIPTION

The ADS7803 is a monolithic CMOS 12-bit analog-to-digital converter with internal sample/hold and four-channel multiplexer. It is designed and tested for full dynamic performance with input signals to 50kHz. An autocalibration cycle guarantees a total unadjusted error within ±3/4LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADS7803 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 2MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7803BP/ADS7803BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+ = 5V$, $V_{REF}- = 0V$	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	$T_A = +25°C$			10	nA
	$T_A = -40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \le V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance[1]: $V_{REF}+$		4.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+ = 5V$, $V_{REF}- = 0V$		10	100	µA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz			17	µs
	CLK = 500kHz			34	µs
With Internal Clock Using Recommended	$T_A = +25°C$			10	µs
Clock Components	$T_A = -40°C$ to $+85°C$		10		µs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
DC ACCURACY					
Total Error, All Channels[2]			±1/2	±3/4	LSB
Differential Nonlinearity			±1/4	±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels		±1/8	±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels		±1/8	±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D = 4.75V$ to $5.25V$		±1/8		LSB
AC ACCURACY					
Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 1kHz$	69	71		dB
	$f_{IN} = 50kHz$	66	69		dB
Total Harmonic Distortion	$f_{IN} = 50kHz$		–75		dB
Signal-to-Noise Ratio	$f_{IN} = 50kHz$		70		dB
Spurious Free Dynamic Range	$f_{IN} = 1kHz$		90		dB
	$f_{IN} = 50kHz$		82		dB
SAMPLING DYNAMICS					
Full Power Bandwidth	–3dB		4		MHz
Aperture Delay	SFR D2 LOW		2500		ns
Offset Error	SRF D2 HIGH		5		ns
	SFR D2 LOW		±1/8	±1/4	LSB
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±1/2	±1	LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±4		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	$T_A = +25°C$, $V_{IN} = 0$ to V_D			1	µA
	$T_A = -40°C$ to $+85°C$, $V_{IN} = 0$ to V_D			10	µA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	µA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA

NOTES: (1) For $(V_{REF}+) - (V_{REF}-)$ as low as 4.5V, the total error will typically not exceed ±1LSB. (2) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

SPECIFICATIONS (CONT)

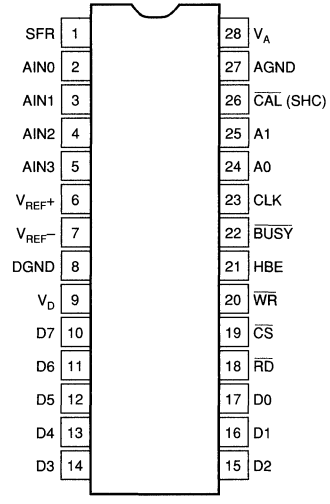
ELECTRICAL

$V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_{REF}-$ = AGND = DGND = 0V; CLK = 2MHz external, T_A = –40°C to +85°C, after calibration at any temperature, unless otherwise specified.

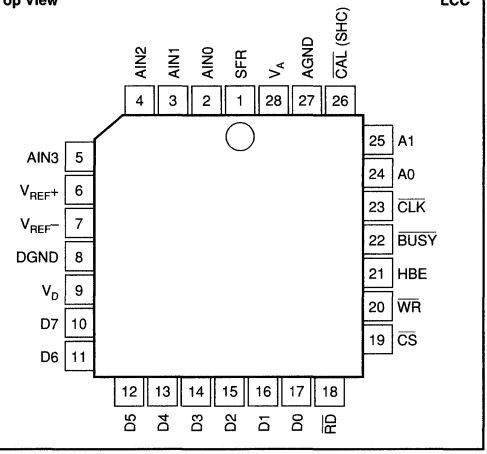
PARAMETER	CONDITIONS	ADS7803BP/ADS7803BN MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS					
V_{OL}	I_{SINK} = 1.6mA			0.4	V
V_{OH}	I_{SOURCE} = 200µA	4			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_D			±1	µA
Output Capacitance	High-Z State		4	15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

PIN CONFIGURATIONS

Top View DIP



Top View LCC



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC7803BN	28-Pin LCC	251
ADS7803BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

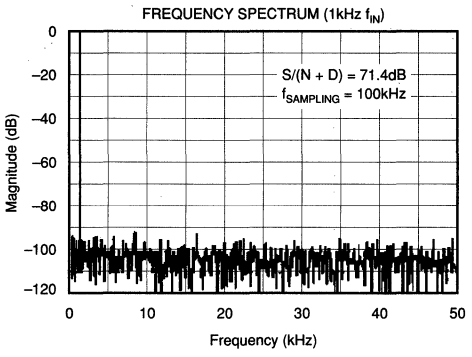
V_A to Analog Ground	6.5V
V_D to Digital Ground	6.5V
Pin V_A to Pin V_D	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	–0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground	–0.3V to V_D + 0.3V
Maximum Junction Temperature	150°C
Internal Power Dissipation	875mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	75°C/W
PLCC	75°C/W

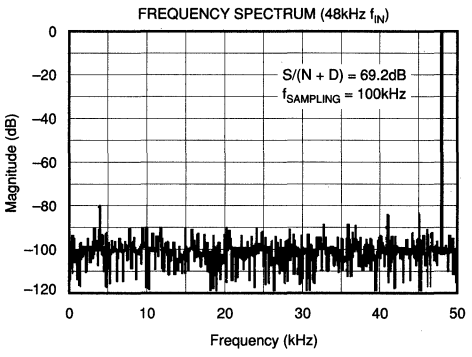
ORDERING INFORMATION

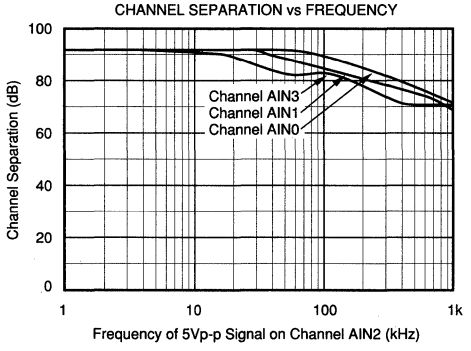
MODEL	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO, dB	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE
ADS7803BN	69	±3/4	–40°C to +85°C
ADS7803BP	69	±3/4	–40°C to +85°C

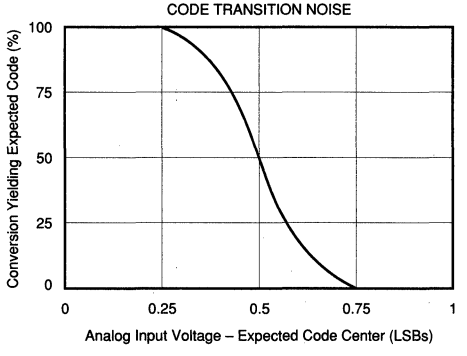
TYPICAL PERFORMANCE CURVES

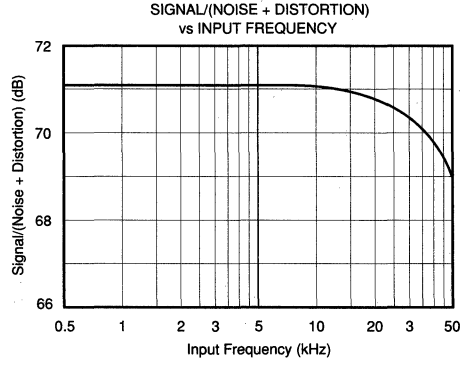
At $V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, dynamic performance based on 2048 point FFTs, unless otherwise noted.

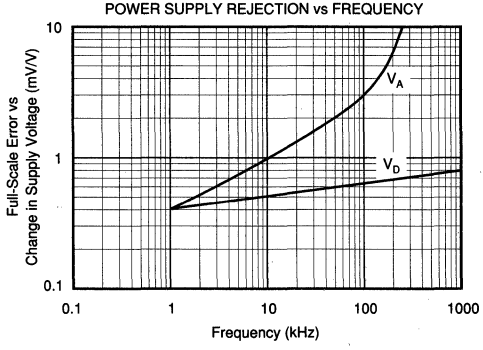






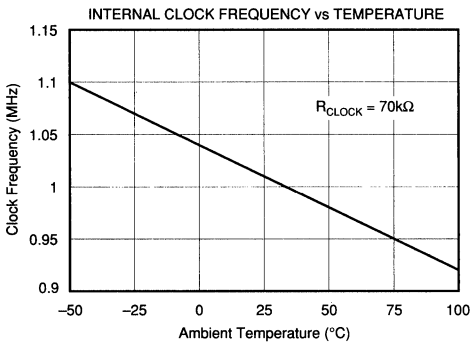


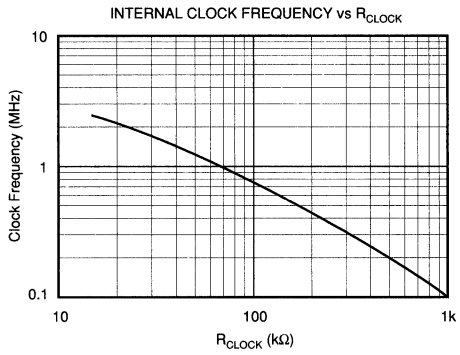




TYPICAL PERFORMANCE CURVES (CONT)

At $V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, dynamic performance based on 2048 point FFTs , unless otherwise noted.





THEORY OF OPERATION

ADS7803 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by an on-chip microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADS7803 to most micro-controllers, microprocessors or digital storage systems.

The on-chip sampling provides excellent dynamic performance for input signals to 50kHz, and has a full-power –3dB bandwidth of 4MHz. Full control over sample-to-hold timing is available for applications where this is critical.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW, with a 50µW power down option.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADS7803 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

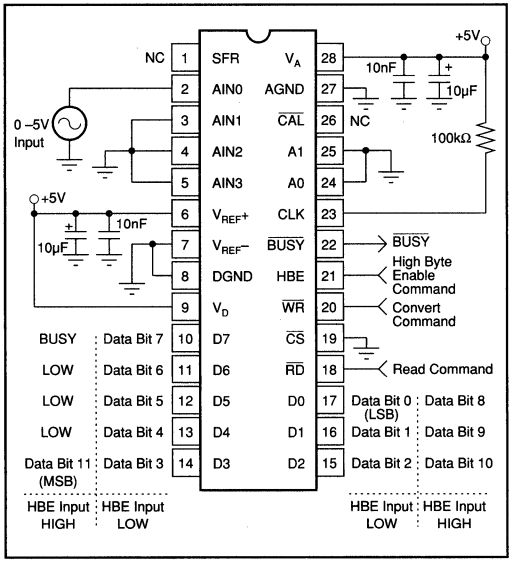


FIGURE 1. Basic Operation.

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles. The successive approximation conversion takes place during clock cycles 6 through 17.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

A conversion can also be initiated by a rising edge on pin 26, if a HIGH has been written to D2 of the Special Function Register, as discussed below.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. Thus, at the end of a calibration cycle, there is valid conversion data in the output registers. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	$V_{REF}+$	Positive voltage reference input. Normally +5V. Must be $\leq V_A$.
7	$V_{REF}-$	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be $\leq V_A$ and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$).
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal or external clock operation. For external clock operation, connect pin 23 to a 74HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 / A0 / Selected Channel LOW / LOW / AIN0 LOW / HIGH / AIN1 HIGH / LOW / AIN2 HIGH / HIGH / AIN3
26	$\overline{CAL}$ (SHC)	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. If D2 of the SFR is programmed HIGH, pin 26 will be used as an input to control the sample-to-hold timing. A rising edge on pin 26 will switch from sample-mode to hold-mode and initiate a conversion. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be $\geq V_D$ and $V_{REF}+$.

READING DATA

Data from the ADS7803 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are

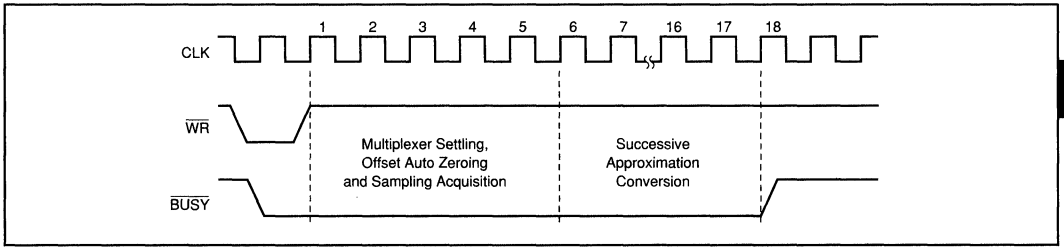


FIGURE 2. Converter Timing.

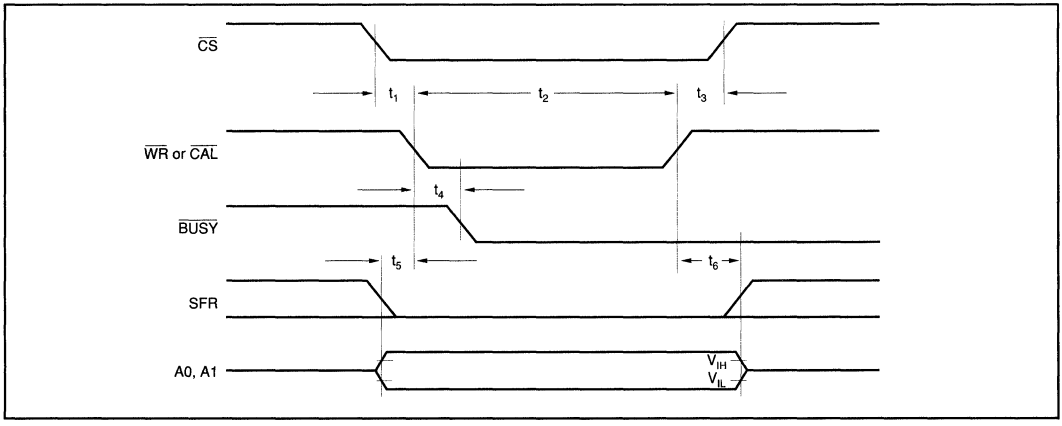


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

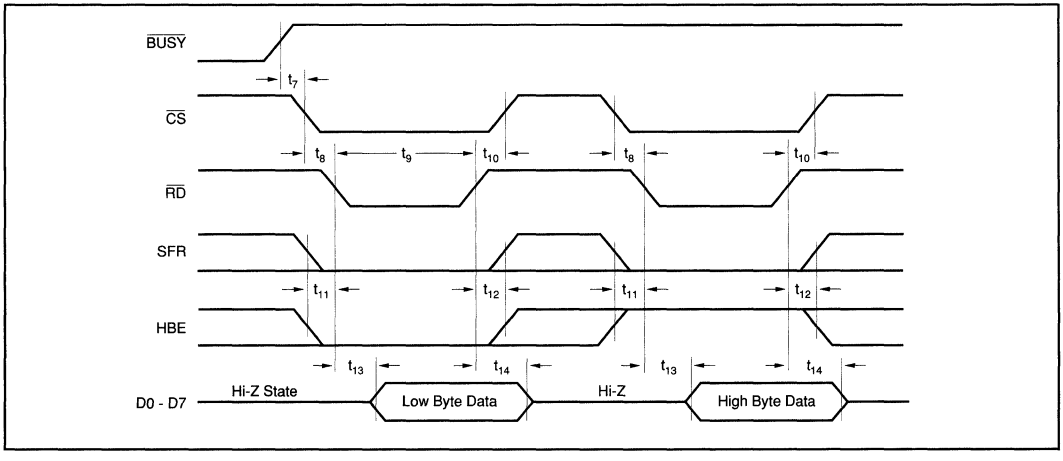


FIGURE 4. Read Cycle Timing.

LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADS7803 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

TRANSPARENT MODE

This is the default mode for ADS7803. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 9 show the digital timing of ADS7803 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADS7803, or to write additional instructions to the converter.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADS7803 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) Note that writing to the SFR also initiates a new conversion.

SYMBOL	PARAMETER[1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time[2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time[2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time[2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time[2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time)[3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time)[3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR[3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns
t_{18}	Acquisition Time. Pin 26 LOW with D2 in SFR HIGH	2.5			µs
t_{19}	Sample-to-Hold Aperture Delay. (D2 in SFR HIGH)		5		ns
t_{20}	Delay from rising edge on pin 26 to start of conversion. (D2 in SFR HIGH)			1.5	CLK cycles

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 8 and 9 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 2MHz external, T_A = –40°C to +85°C).

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, latched Output Mode enabled.
D1	$\overline{CAL}$ Flag	If HIGH, calibration cycle in progress.
D2	Pin 26 Status	If LOW, pin 26 used as input to initiate calibration cycle. If HIGH, pin 26 used as input to control sample-to-hold timing.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	$\overline{CAL}$ ERROR Flag	If HIGH, an overflow occurred during calibration.
D7	$\overline{BUSY}$ Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

POWER DOWN MODE

Writing a HIGH to D3 in the SFR puts the ADS7803 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. The internal clock and analog circuitry are turned off, although the output registers and SFR can still be accessed normally. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. Note that if the power supply falls below 3V and then recovers, a calibration is automatically initiated, and the SFR will be reset. D3 will be LOW, and the ADS7803 will not be in the Power Down Mode.

During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7803 will revert to power down. Also, writing to D1 and D3 in the SFR will initiate a calibration, do a single conversion and revert to the Power Down Mode, in 185 clock cycles. Accurate conversion results will be available in the output registers.

The activation delay from power down to normal operation is included in the sampling time. No extra time is required, either when coming out of the Power Down Mode or when making a single conversion in the Power Down Mode.

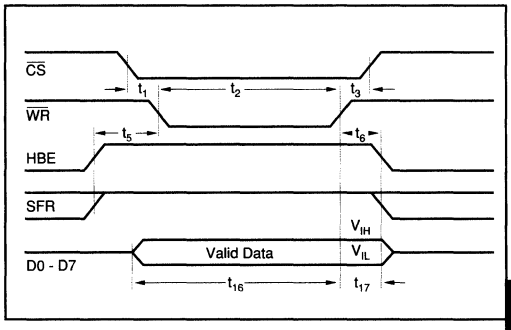


FIGURE 5. Writing to the SFR.

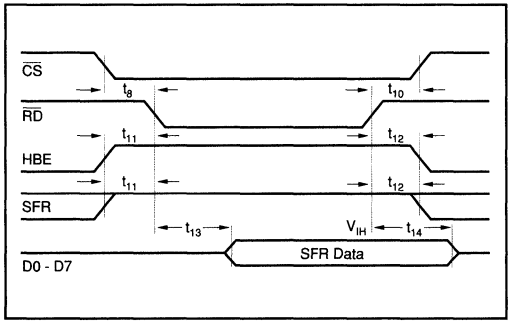


FIGURE 6. Reading the FSR.

SAMPLE/HOLD CONTROL MODE

With D2 in the SFR HIGH, a rising edge input on pin 26 will switch the ADS7803 from sample-mode to hold-mode with a 5ns aperture delay. This also initiates a conversion, which will start within 1.5 CLK cycles.

This mode allows full control over the sample-to-hold timing, which is especially useful where external events trigger sampling timing.

In the Sample/Hold Control Mode, pin 26 must be held LOW a minimum of 2.5µs between conversions to allow accurate acquisition of input signals. Also, offset error will increase in this mode, since auto-zeroing of the comparator is not synchronized to the sampling. Minimum offset is achieved by synchronizing the sampling signal to CLK, whether internal or external. Ideally, the sampling signal

OPERATION	$\overline{CS}/\overline{WR}$	SFR/HBE	D0	D1	D2	D3	D5	D4/D6/D7
Enables Transparent Mode for Data Latches	LOW	HIGH	LOW	X	X	X	X	LOW
Enables Latched Output Mode for Data Latches	LOW	HIGH	HIGH(1)	X	X	X	X	LOW
Initiates Calibration Cycle	LOW	HIGH	X	HIGH	X	X	X	LOW
Activates Sample/Hold Control Mode	LOW	HIGH	X	X	HIGH(1)	X	X	LOW
Activates Power Down Mode(2)	LOW	HIGH	X	X	X	HIGH(1)	X	LOW
Resets Power Fail Flag	LOW	HIGH	X	X	X	X	LOW	LOW

NOTES: (1) Writing a LOW here reactivates the standard mode of operation. (2) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7803 will revert to power down. (3) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

rising edge should be delayed 20ns from the falling edge of CLK. This will keep offset error to about 1LSB.

In the Sample/Hold Control Mode, a LOW pulse on $\overline{WR}$ (with $\overline{CS}$ LOW) will not initiate a conversion, but the rising edge will latch the multiplexer channel according to the inputs on A0 and A1. When changing channels, this must be done at least 2.5µs before pin 26 goes HIGH (to start a conversion.)

CONTROL LINES

Table IV shows the functions of the various control lines on the ADS7803. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

INSTALLATION

INPUT IMPEDANCE

ADS7803 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

In many applications, a simple passive low-pass filter as shown in Figure 10a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 10a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 10b should be used.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADS7803, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADS7803

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle. (See SFR section for alternate use as Sample/Hold Control Mode input.)
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

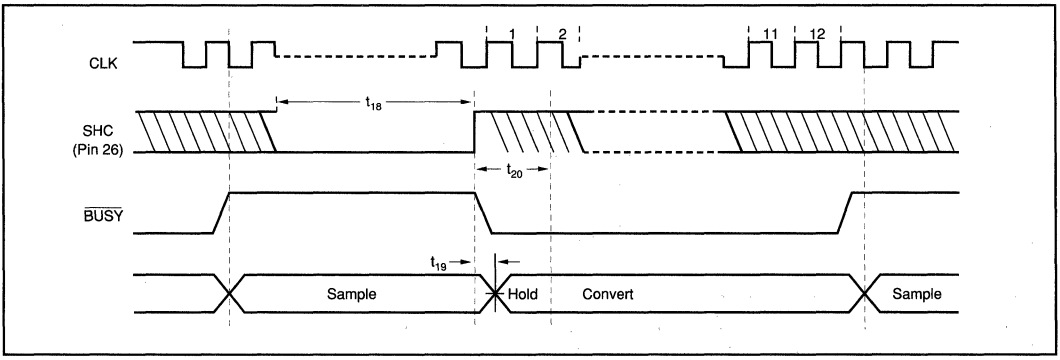


FIGURE 7. Timing for Initiating Conversion in Sample/Hold Control Mode (D2 in SFR HIGH).

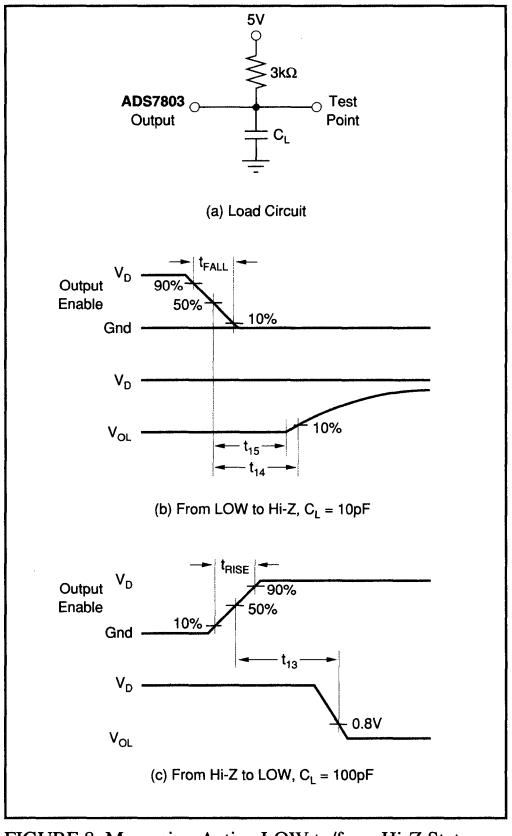


FIGURE 8. Measuring Active LOW to/from Hi-Z State.

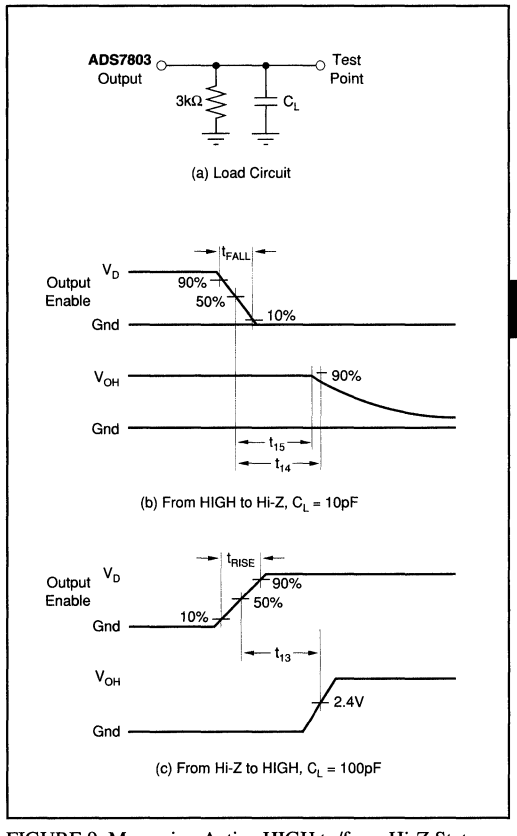


FIGURE 9. Measuring Active HIGH to/from Hi-Z State.

to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}- = 0V$, the converter can function with $V_{REF}+$ as low as 4.5V and $V_{REF}-$ as high as 1V.

As long as there is at least a 4.5V difference between $V_{REF}+$ and $V_{REF}-$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADS7803 should be bypassed with 10µF tantalum capacitors as close to the part as possible. Although ADS7803 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur.

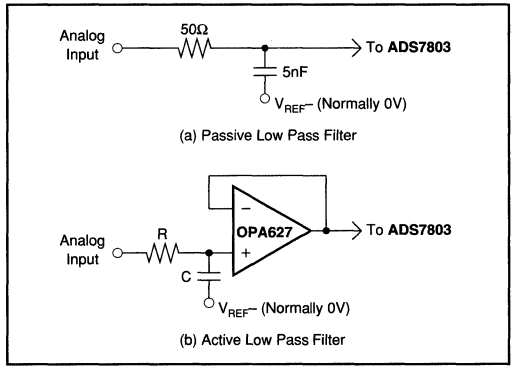


FIGURE 10. Input Signal Conditioning.

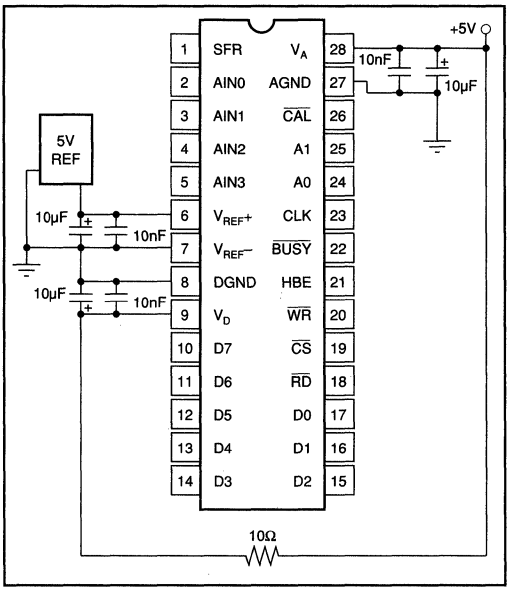


FIGURE 11. Power Supply and Reference Decoupling.

Figure 11 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADS7803 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADS7803, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The V_{REF}– pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADS7803 clock from an external source is shown in Figure 12a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The duty cycle of the external clock can vary as long as the LOW time and HIGH time are each at least 200ns wide. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.4MHz.

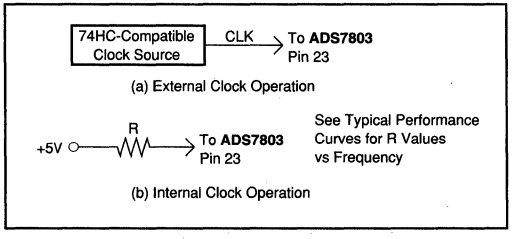


FIGURE 12. Internal Clock Operation.

INTERNAL CLOCK OPERATION

Figure 12b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 13 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADS7803, using a precision, low-cost complete difference amplifier, INA105.

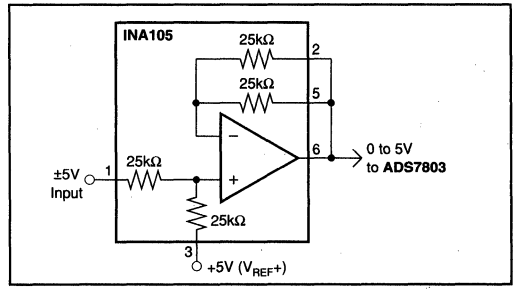


FIGURE 13. ±5V Input Range.

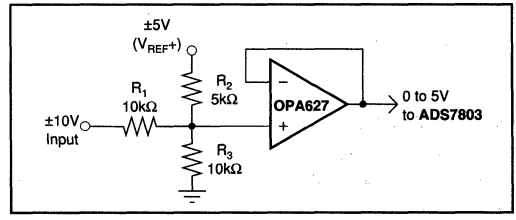


FIGURE 14. ±10V Input Range.

Figure 14 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADS7803. The precision of this circuit will depend on the matching and tracking of the three resistors used.

To trim this circuit for full 12-bit precision, R_2 and R_3 need to be adjustable over appropriate ranges. To trim, first have the ADS7803 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R_3 until the ADS7803 output toggles between the codes FFE hex and FFF hex. This makes R_3 extremely close to R_1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R_2 until the ADS7803 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADS7803, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 15 show a typical interface to Motorola microprocessors, while Figure 16 shows how the result can be placed in register D0.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

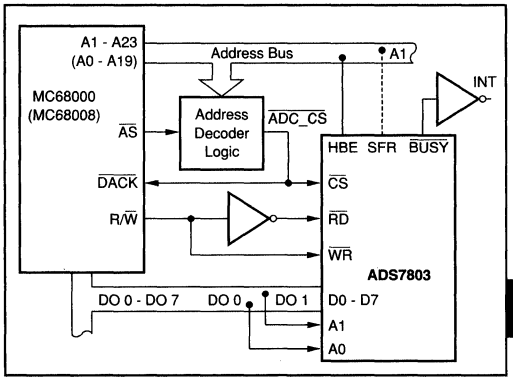


FIGURE 15. Interface to Motorola Microprocessors.

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the D0 register, as shown in Figure 15. The address decoder must pull down ADC_CS AT ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 17 shows a typical interface to Intel.

A conversion is initiated by write instruction to address ADC_CS. Data pins DO0 and DO1 select the analog input channel. The BUSY signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the ADC_CS address fetches the Low byte, and a read instruction from the ADC_CS address +2 fetches the High byte.

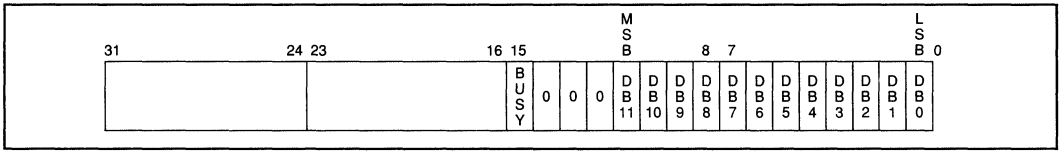


FIGURE 16. Conversion Results in Motorola Register D0.

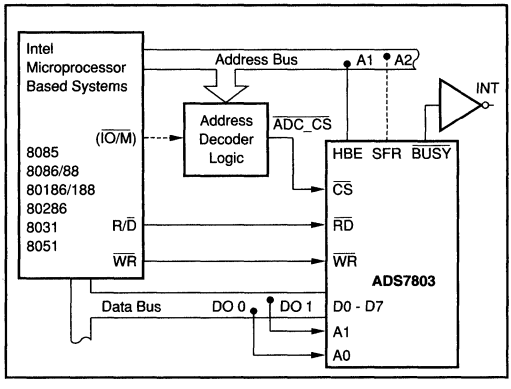
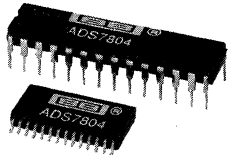


FIGURE 17. Interface to Intel Microprocessors.

BURR-BROWN®



ADS7804

DEMO BOARD AVAILABLE
See Appendix A

12-Bit 10µs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

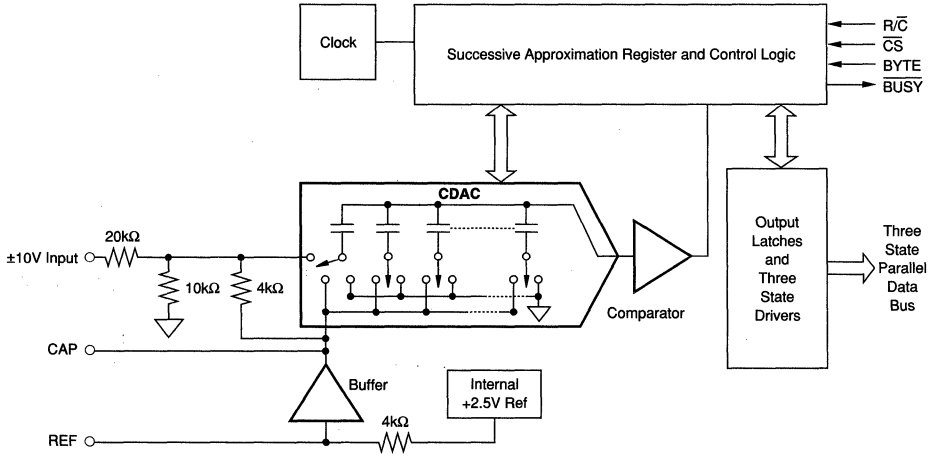
- **100kHz min SAMPLING RATE**
- **STANDARD ±10V INPUT RANGE**
- **72dB min SINAD WITH 45kHz INPUT**
- **±0.45 LSB max INL**
- **DNL: 12 Bits "No Missing Codes"**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 16-BIT ADS7805**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **FULL PARALLEL DATA OUTPUT**
- **100mW max POWER DISSIPATION**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7804 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7804 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7804 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



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SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, and V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7804P, U			ADS7804PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V			*		V
Impedance			23			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			5.7	8		*	*	µs
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±0.9			±0.45	LSB[1]
Differential Linearity Error				±0.9			±0.45	LSB
No Missing Codes			Guaranteed			*		Bits
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±10			±10	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 45kHz	80			*			dB[5]
Total Harmonic Distortion	f_{IN} = 45kHz			–80			*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 45kHz	70			72			dB
Signal-to-Noise	f_{IN} = 45kHz	70			72			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8					ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 12 bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, and V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7804P, U			ADS7804PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
$+I_{DIG}$			0.3			*		mA
$+I_{ANA}$			16			*		mA
Power Dissipation	f_S = 100kHz			100			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7804, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} ..... ±25V
CAP ..... $+V_{ANA}$ +0.3V to AGND2 –0.3V
REF ..... Indefinite Short to AGND2
Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7804P	Plastic DIP	246
ADS7804PB	Plastic DIP	246
ADS7804U	SOIC	217
ADS7804UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

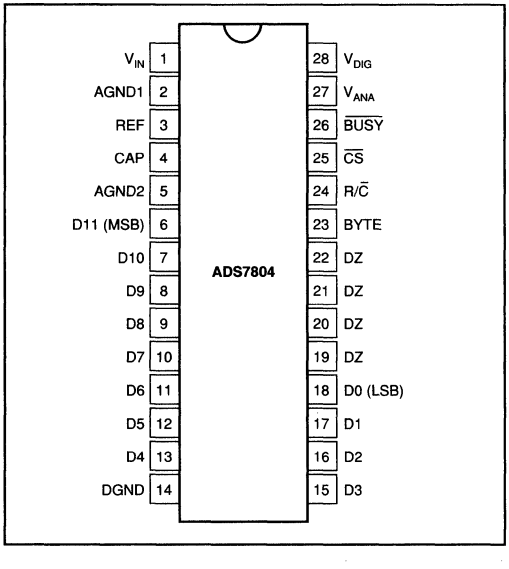
ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7804P	±0.9	70	–40°C to +85°C	Plastic DIP
ADS7804PB	±0.45	72	–40°C to +85°C	Plastic DIP
ADS7804U	±0.9	70	–40°C to +85°C	SOIC
ADS7804UB	±0.45	72	–40°C to +85°C	SOIC

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	LOW when $\overline{CS}$ LOW, R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7804 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns (6µs max) will initiate a conversion. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7804 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7804 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7804 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 3 through 5 for timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in process.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in process.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in process.

NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".

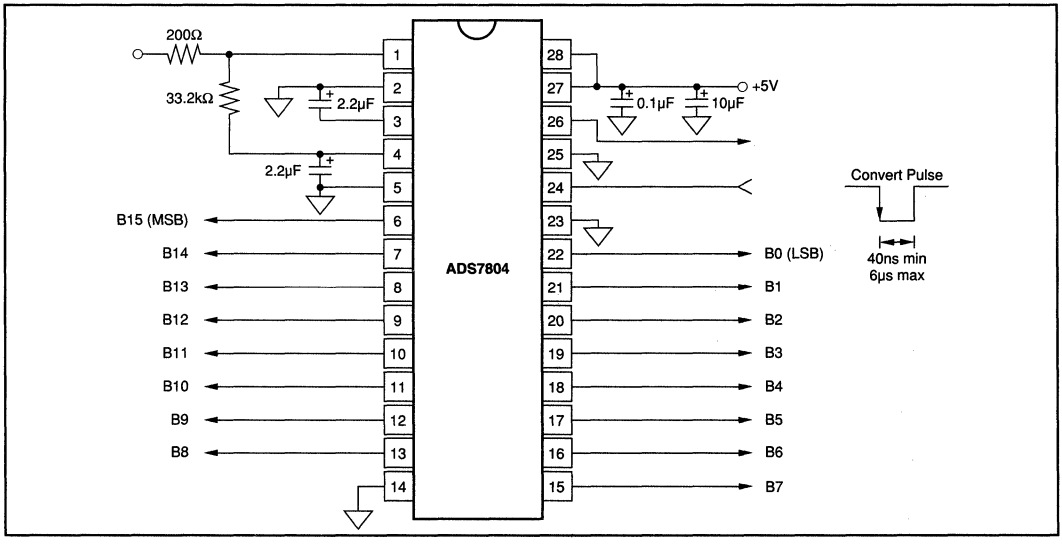


FIGURE 1. Basic Operation.

READING DATA

The ADS7804 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	4.88mV		
+Full Scale (10V – 1LSB)	9.99512V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–4.88mV	1111 1111 1111	FFF
–Full Scale	–10V	1000 0000 0000	800

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D11-D0 (pin 6-13 and 15-18 when BYTE is LOW). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 16µs after the start of conversion 'n'. Do not attempt to read data from 16µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		6000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		7.4		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

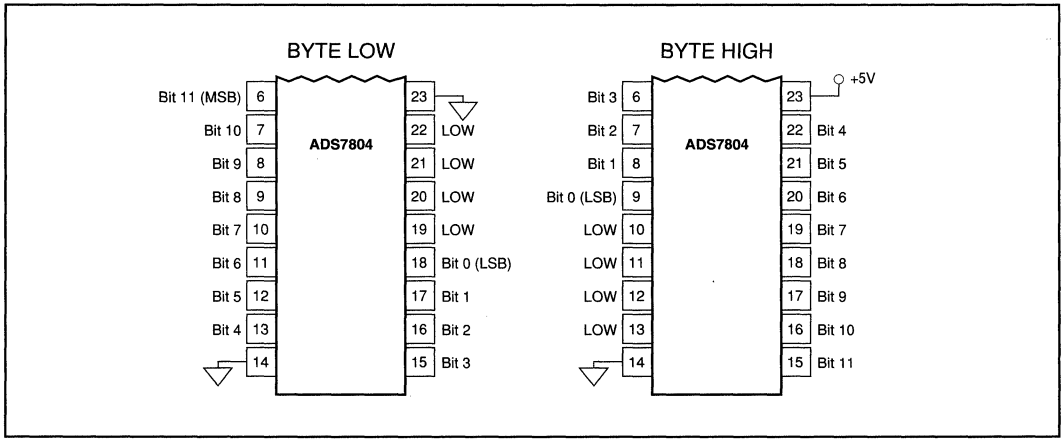


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

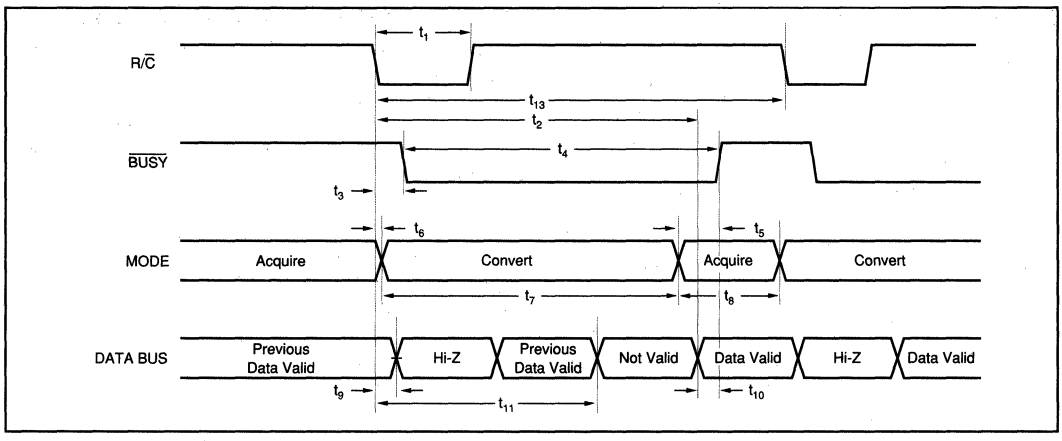


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

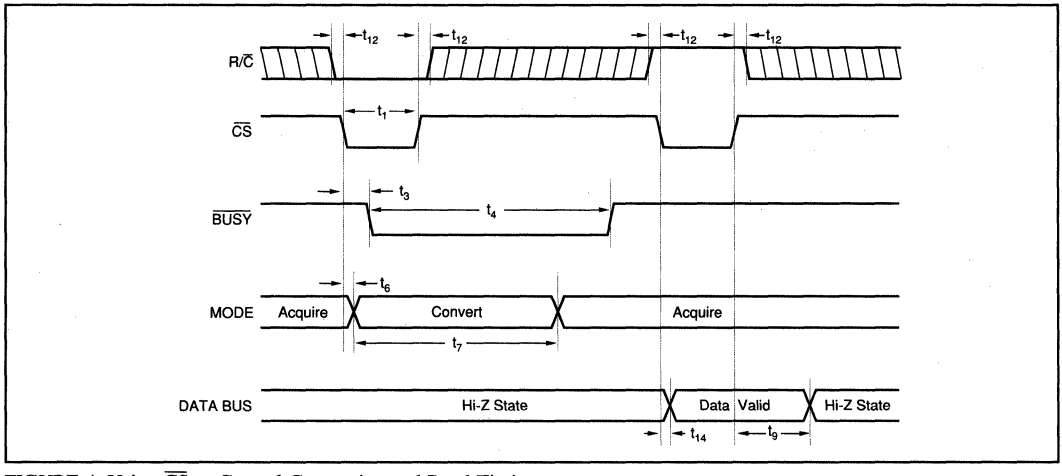


FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

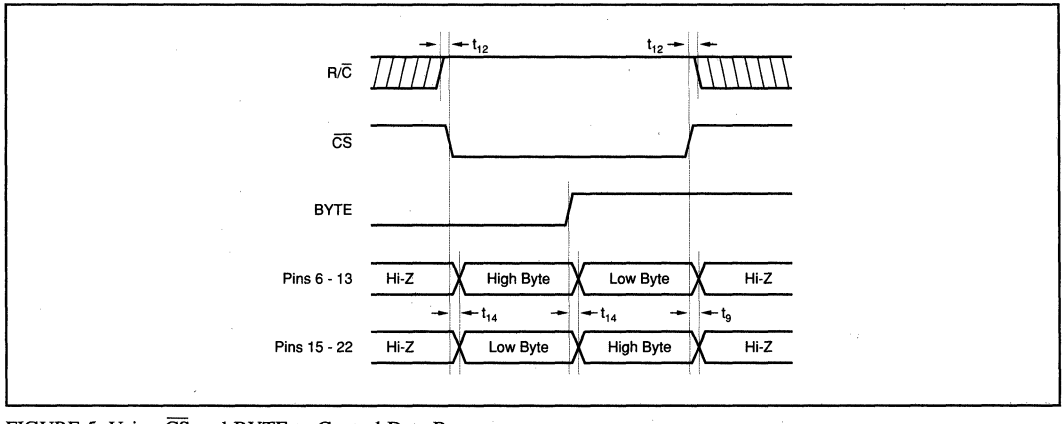


FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

INPUT RANGES

The ADS7804 offers a standard ±10V input range. Figure 6 shows the necessary circuit connections for the ADS7804 with and without hardware trim. Offset and full scale error[1] specifications are tested and guaranteed with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The nominal input impedance of 23kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

The ADS7804 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7804, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is ±15mV for the offset and ±60mV for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7804 in software, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Table V for range of offset and gain errors with and without external resistors.

NO CALIBRATION

See Figure 6b for circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7804 will be bound by the shaded region seen in Figure 7 with a typical offset of –30mV and a typical gain error of –1.5%. Refer to Table V for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPZ	–10 < BPZ < 10 –2 < BPZ < 2	–45 < BPZ < 5 –8 < BPZ < 1	mV LSBs
Gain Error	–0.5 < error < 0.5 –0.25 < error < 0.25[1]	–0.6 < error < –0.55 –0.45 < error < –0.3[1]	% of FSR
NOTE: (1) High Grade.			

TABLE VII. Bipolar Offset and Gain Errors With and Without External Resistors.

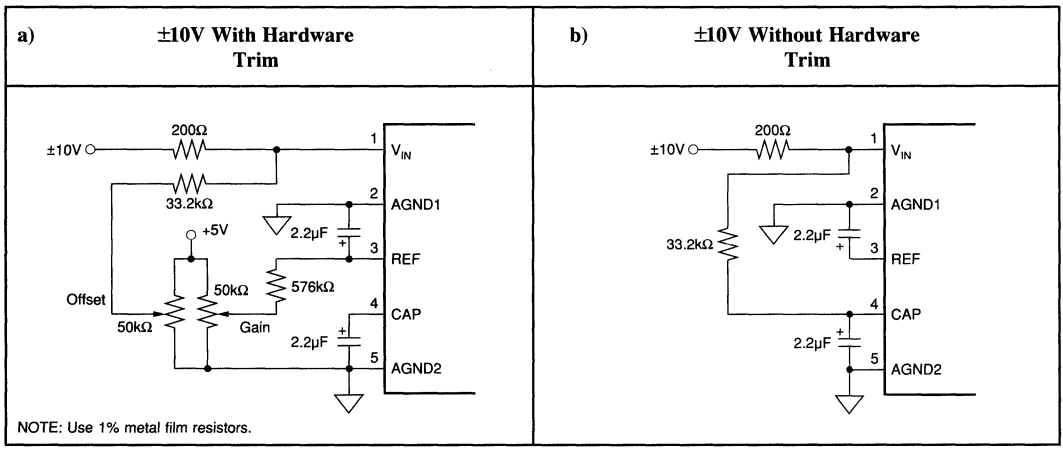


FIGURE 6. Circuit Diagram With and Without External Resistors.

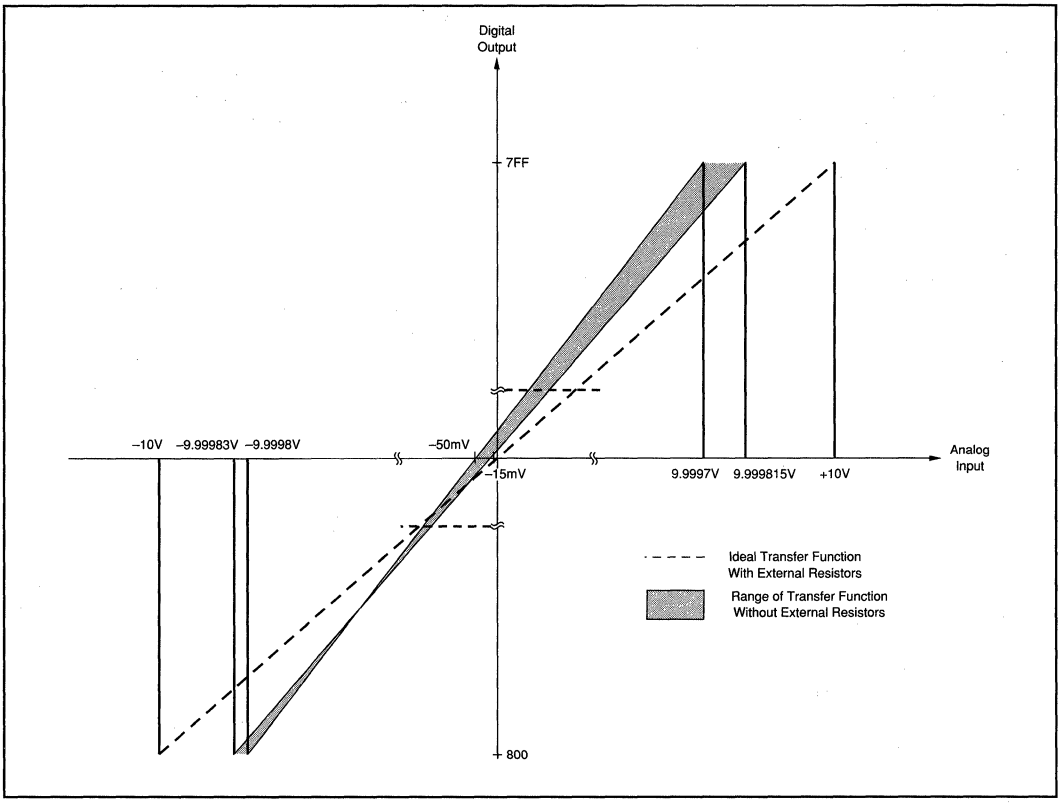


FIGURE 7. Full Scale Transfer Function.

REFERENCE

The ADS7804 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7804. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7804 uses 90% of its power for the analog circuitry. The ADS7804 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7804. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7804, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7804.

The resistive front end of the ADS7804 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7804 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7804 has an internal LSB size of 610μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7805 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of 38μV.

APPLICATIONS

Call factory for updated data sheet which includes standard DSP, microprocessor, and microcontroller interfaces.

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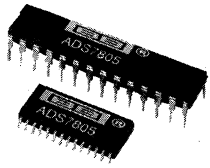


ADS7805

DEMO BOARD AVAILABLE
See Appendix A

16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

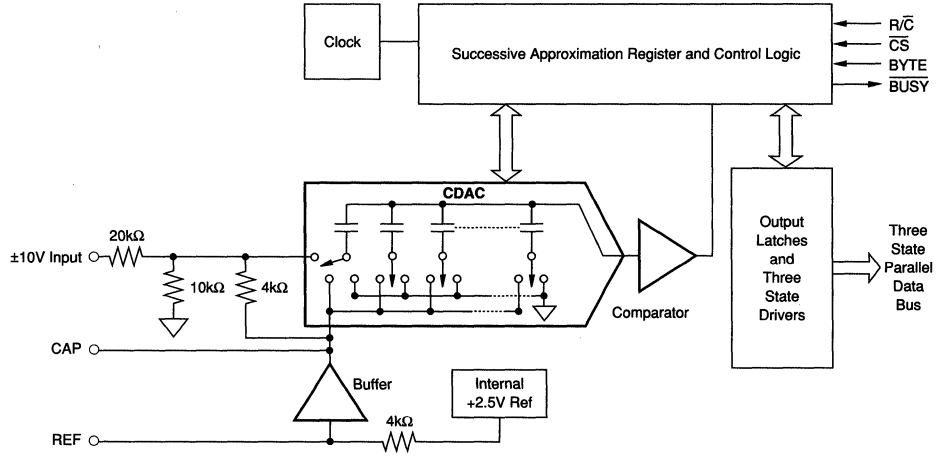
- **100kHz min SAMPLING RATE**
- **STANDARD ±10V INPUT RANGE**
- **86dB min SINAD WITH 20kHz INPUT**
- **±3.0 LSB max INL**
- **DNL: 16-bits "No Missing Codes"**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 12-BIT ADS7804**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **FULL PARALLEL DATA OUTPUT**
- **100mW max POWER DISSIPATION**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7805 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7805 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7805 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V			*		V
Impedance			23			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±4			±3	LSB[1]
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90			94			dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz			–90			–94	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20kHz	83			86			dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 20kHz	83			86			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS			Parallel 16-bits					
Data Format			Binary Two's Complement					
Data Coding								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation	f_S = 100kHz			100			*	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	•		•	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7805, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	±25V
CAP	$+V_{ANA}$ +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7805P	Plastic DIP	246
ADS7805PB	Plastic DIP	246
ADS7805U	SOIC	217
ADS7805UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

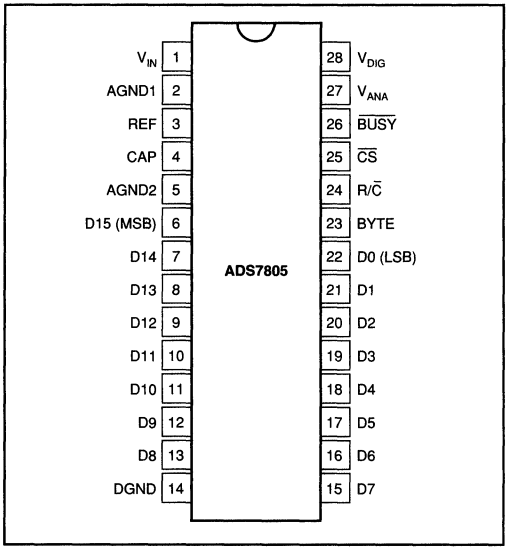
ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7805P	±4	83	–25°C to +85°C	Plastic DIP
ADS7805PB	±3	86	–25°C to +85°C	Plastic DIP
ADS7805U	±4	83	–25°C to +85°C	SOIC
ADS7805UB	±3	86	–25°C to +85°C	SOIC

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7805 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns (7µs max) will initiate a conversion. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7805 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 3 through 5 for timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 3 and 4 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".

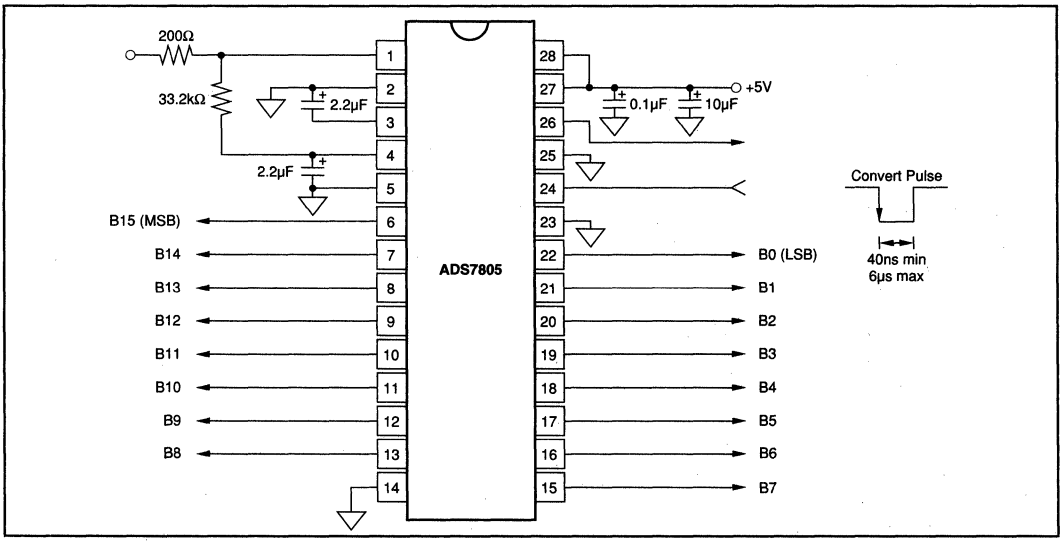


FIGURE 1. Basic Operation.

READING DATA

The ADS7805 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	305µV		
+Full Scale (10V – 1LSB)	9.999695V	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
One LSB below Midscale	–305µV	1111 1111 1111 1111	FFFF
–Full Scale	–10V	1000 0000 0000 0000	8000

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D15-D0 (pin 6-13 and 15-22). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 7µs after the start of conversion 'n'. Do not attempt to read data from 7µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		7000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		7.4		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

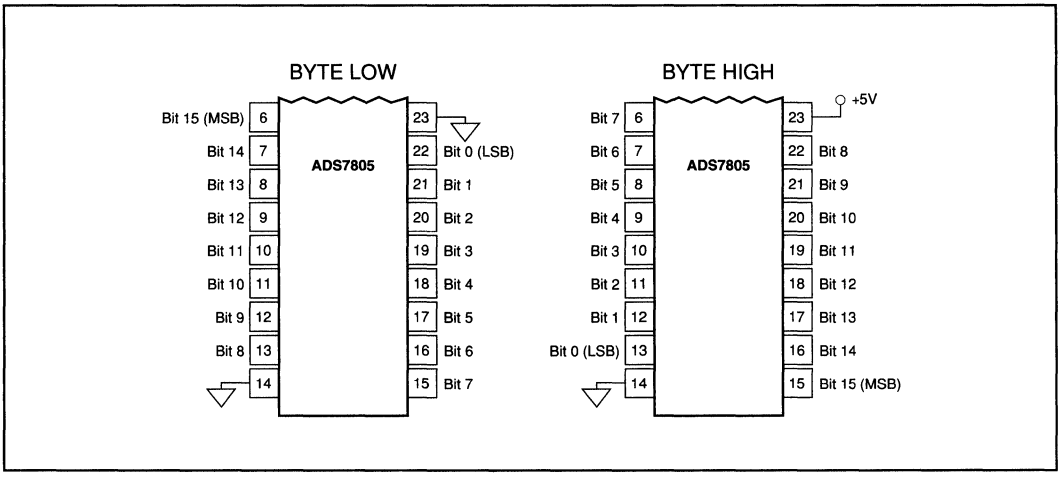


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

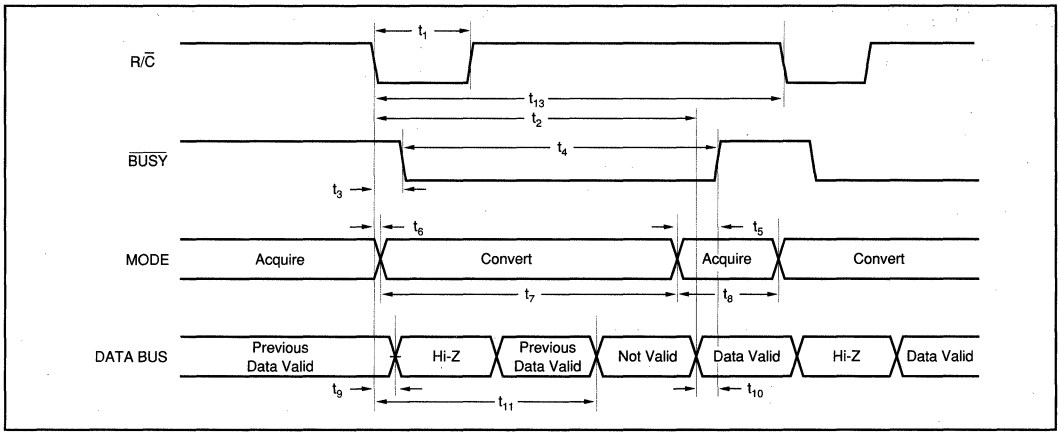


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

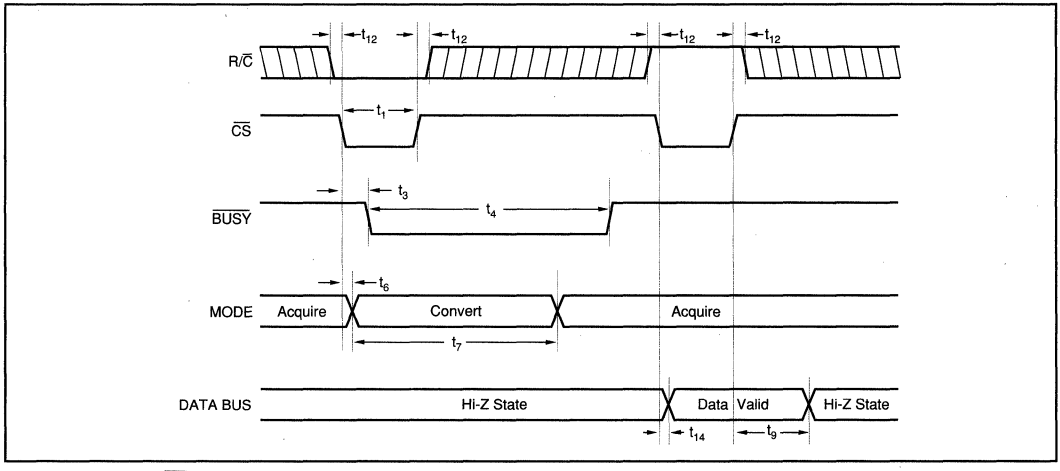


FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

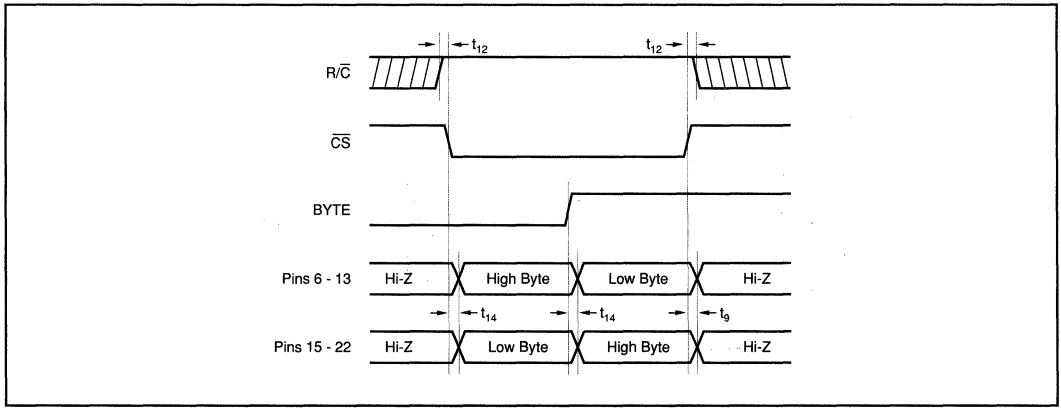


FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

INPUT RANGES

The ADS7805 offers a standard ±10V input range. Figure 6 shows the necessary circuit connections for the ADS7805 with and without hardware trim. Offset and full scale error[1] specifications are tested and guaranteed with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The nominal input impedance of 23kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection guaranteed to at lease ±25V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

The ADS7805 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7805, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is ±15mV for the offset and ±60mV for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7805 in software, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Table V for range of offset and gain errors with and without external resistors.

NO CALIBRATION

See Figure 6b for circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7805 will be bound by the shaded region seen in Figure 7 with a typical offset of –30mV and a typical gain error of –1.5%. Refer to Table V for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPO	–10 < BPO < 10 –30 < BPO < 30	–50 < BPO < –15 –150 < BPO < –45	mV LSBs
Gain Error	–0.5 < error < 0.5	–2 < error < –1	% of FSR

TABLE V. Offset and Gain Errors With and Without External Resistors.

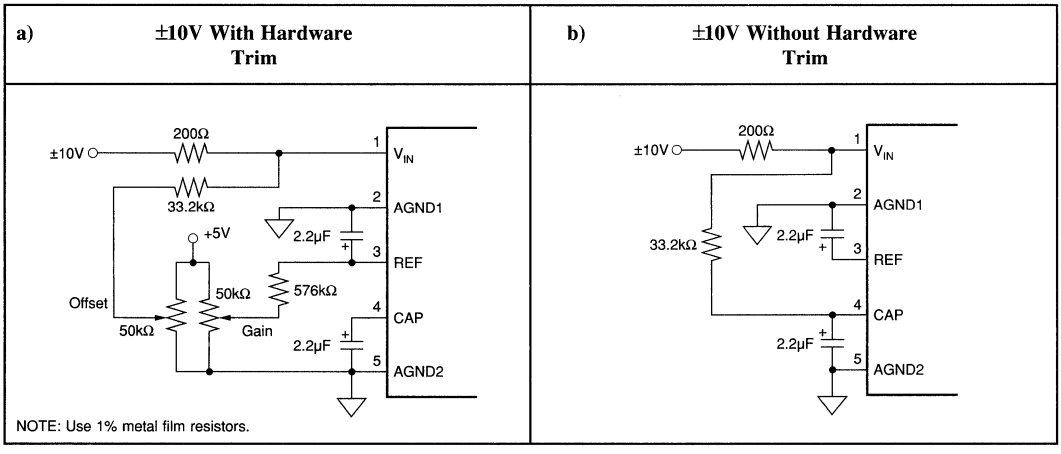


FIGURE 6. Circuit Diagram With and Without External Resistors.

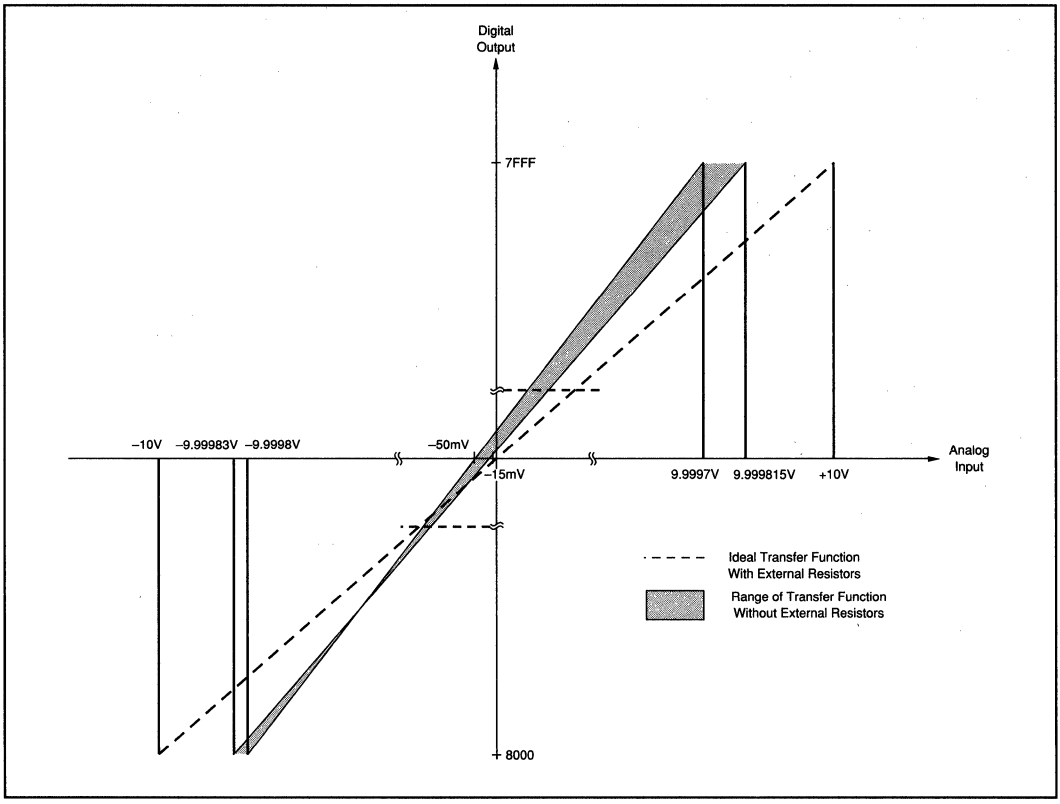


FIGURE 7. Full Scale Transfer Function.

REFERENCE

The ADS7805 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7805. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7805 uses 90% of its power for the analog circuitry. The ADS7805 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7805. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7805, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7805.

The resistive front end of the ADS7805 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7805 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7805 has an internal LSB size of 38μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

APPLICATIONS

Call factory for updated data sheet which includes standard DSP, microprocessor, and microcontroller interfaces.

BURR-BROWN®

ADS7806

DEMO BOARD AVAILABLE
See Appendix A

Low-Power 12-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

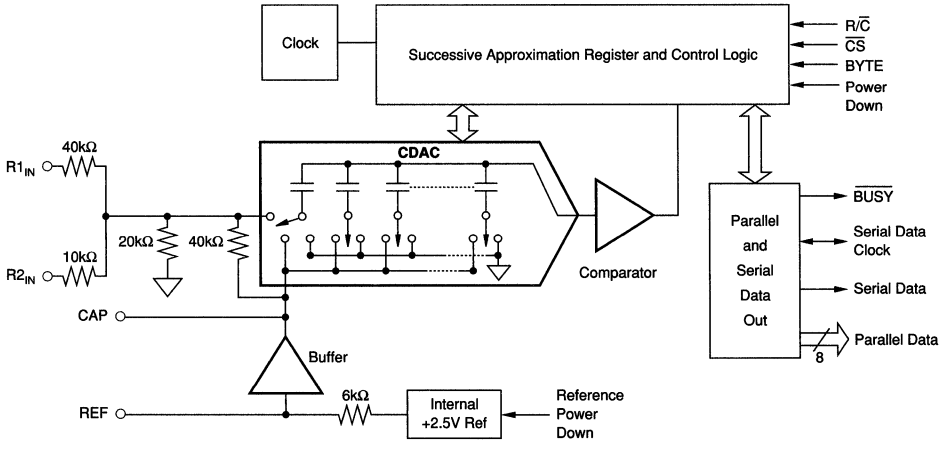
- **35mW max POWER DISSIPATION**
- **50µW POWER DOWN MODE**
- **25µs max ACQUISITION AND CONVERSION**
- **±1/2LSB max INL AND DNL**
- **72dB min SINAD WITH 1kHz INPUT**
- **±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES**
- **SINGLE +5V SUPPLY OPERATION**
- **PARALLEL AND SERIAL DATA OUTPUT**
- **PIN-COMPATIBLE WITH 16-BIT ADS7807**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7806 is a low-power 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7806 can acquire and convert to full 12-bit accuracy in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7806 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7806P, U MIN	ADS7806P, U TYP	ADS7806P, U MAX	ADS7806PB, UB MIN	ADS7806PB, UB TYP	ADS7806PB, UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table II)				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error			±0.15	±0.9		*	±0.45	LSB[1]
Differential Linearity Error			±0.15	±0.9		*	±0.45	LSB
No Missing Codes			Guaranteed			*		Bits
Transition Noise[2]			0.1			*		LSB
Gain Error			±0.2			±0.1		%
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error[3]	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error[3]	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down[5]	2.2µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V	80	90		*	*		dB[6]
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–90	–80		*	*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V	70	73		72	*		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V	70	73		72	*		dB
Usable Bandwidth[7]			130			*		kHz
Full Power Bandwidth (-3dB)			600			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			20			*		ps
Transient Response	FS Step			5			*	µs
Overvoltage Recovery[8]			750			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS								
Data Format		Parallel 12-bits in 2-bytes; Serial						
Data Coding		Binary Two's Complement or Straight Binary						
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7806P, U			ADS7806PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	R_L = 3.3kΩ, C_L = 50pF			83			*	ns
Bus Relinquish Time	R_L = 3.3kΩ, C_L = 10pF			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6			*		mA
I_{ANA}			5.0			*		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, f_S = 40kHz		28	35		*	*	mW
	REFD HIGH		23			*		mW
	PWRD and REFD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7806 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, and AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7806P	±0.9	70	–40°C to +85°C	Plastic DIP
ADS7806PB	±0.45	72	–40°C to +85°C	Plastic DIP
ADS7806U	±0.9	70	–40°C to +85°C	SOIC
ADS7806UB	±0.45	72	–40°C to +85°C	SOIC

PACKAGE INFORMATION

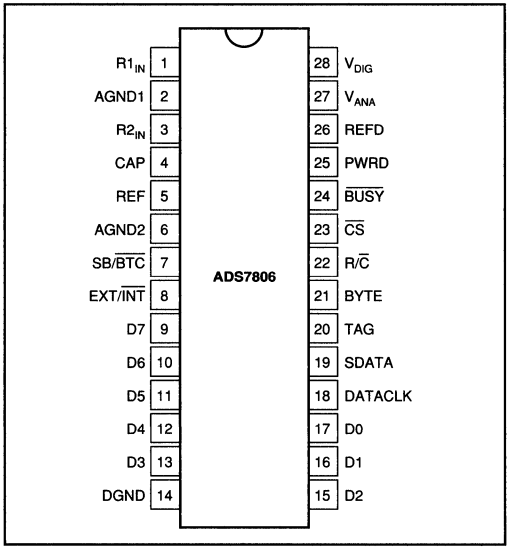
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS7806P	Plastic DIP	246
ADS7806PB	Plastic DIP	246
ADS7806U	SOIC	217
ADS7806UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$R1_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Sense Ground.
3	$R2_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground.
7	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{INT}$	I	External/Internal data clock select.
9	D7	O	Data Bit 3 if BYTE is HIGH. Data bit 11 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
11	D5	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
12	D4	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
13	D3	O	LOW if BYTE is HIGH. Data bit 7 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D2	O	LOW if BYTE is HIGH. Data bit 6 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
16	D1	O	LOW if BYTE is HIGH. Data bit 5 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
17	D0	O	LOW if BYTE is HIGH. Data bit 4 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK.
20	TAG	I	Serial Input When Using an External Data Clock.
21	BYTE	I	Selects 8 most significant bits (LOW) or 4 least significant bits (HIGH) on parallel output pins.
22	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
23	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V_{ANA}		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



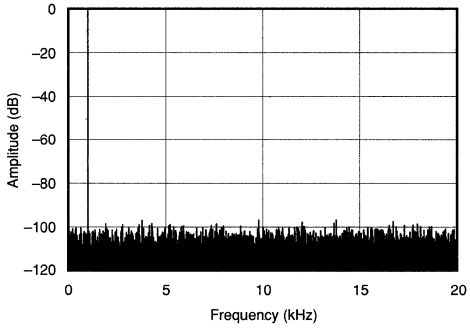
ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

TABLE II. Input Range Connections. See also Figure 7.

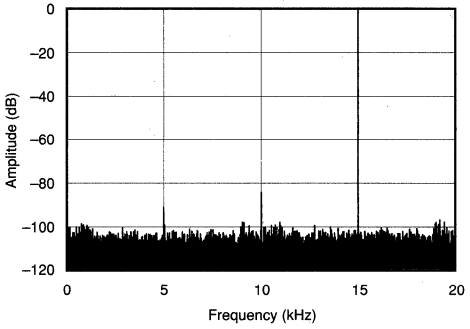
TYPICAL PERFORMANCE CURVES

T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

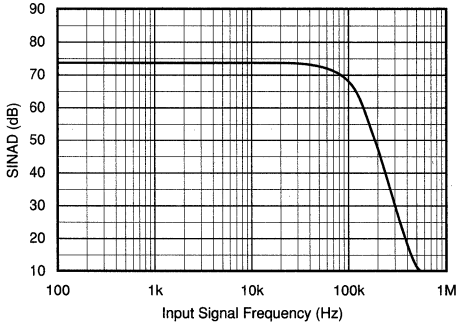
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



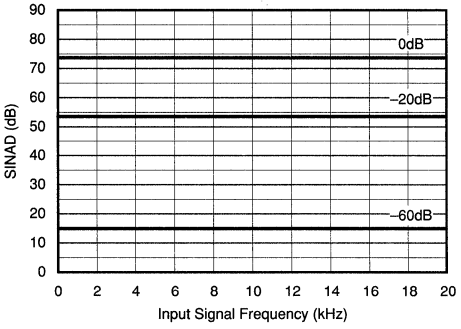
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



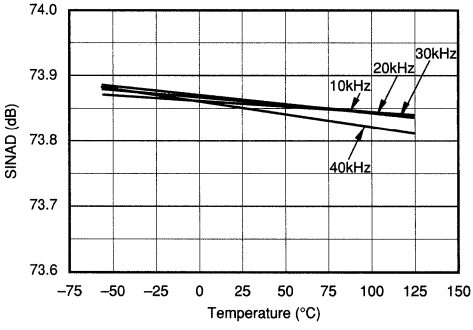
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



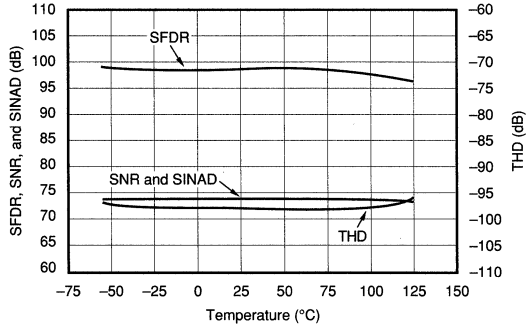
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

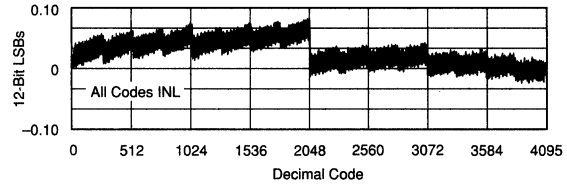


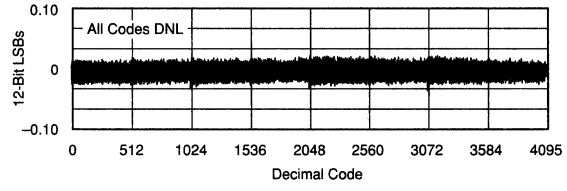
A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

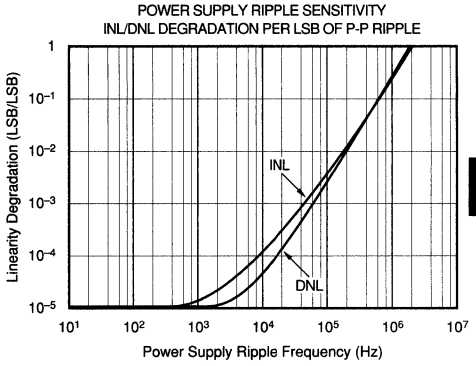


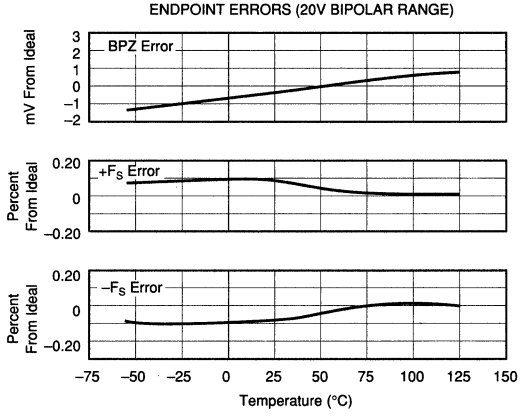
TYPICAL PERFORMANCE CURVES (CONT)

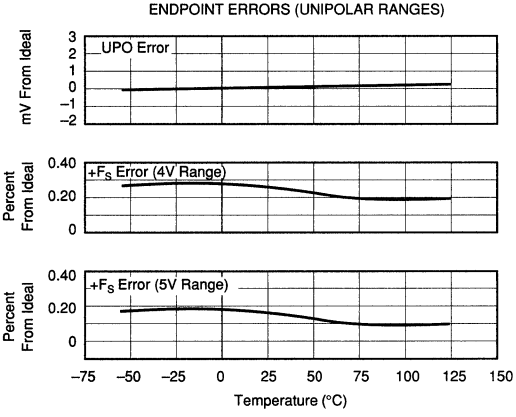
T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

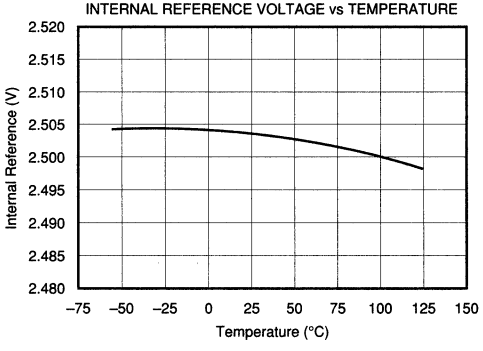


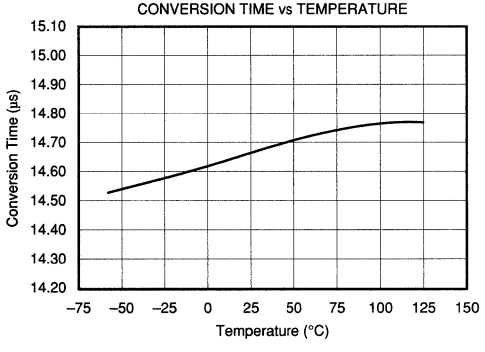












BASIC OPERATION

PARALLEL OUTPUT

Figure 1a) shows a basic circuit to operate the ADS7806 with a ±10V input range and parallel output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the 8 most significant bits will be valid when $\overline{BUSY}$ rises; if BYTE is HIGH, the 4 least significant bits will be valid when $\overline{BUSY}$ rises. Data will be output in Binary Two's Complement format. $\overline{BUSY}$ going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

SERIAL OUTPUT

Figure 1b) shows a basic circuit to operate the ADS7806 with a ±10V input range and serial output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 19) synchronized to 12 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7806 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

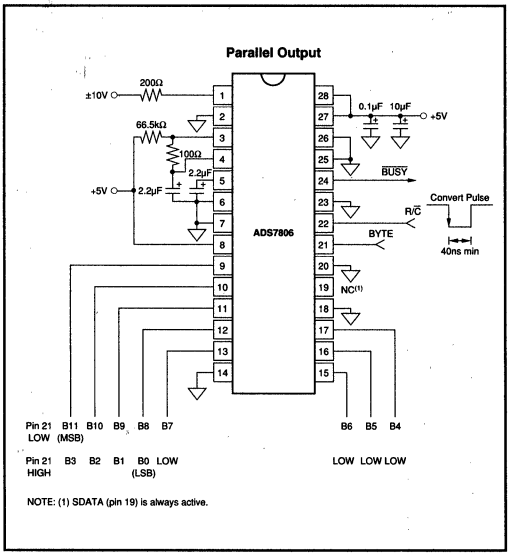


FIGURE 1a. Basic ±10V Operation, both Parallel and Serial Output.

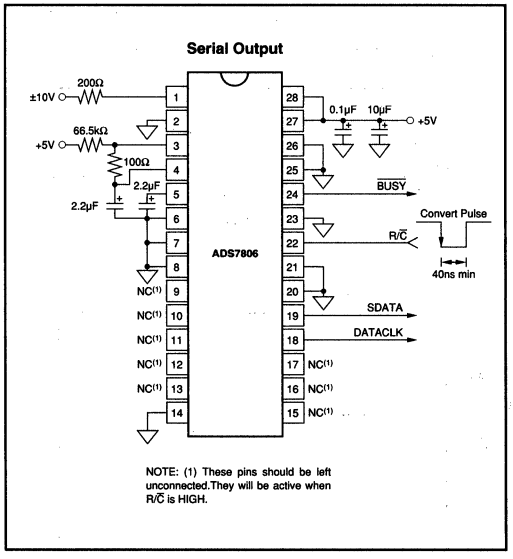


FIGURE 1b. Basic ±10V Operation with Serial Output.

The ADS7806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables III and IV for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 6 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.
NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".			

Table III. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion 'n', serial data from conversion 'n-1' will be output on SDATA (pin 19) following the start of conversion 'n'. See **Internal Data Clock** in the **Reading Data** section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

READING DATA

The ADS7806 outputs serial or parallel data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{BTC}$ (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table V for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
0	↓	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion "n" completed. Valid data from conversion "n" clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	↑	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	0	↑	X	X	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion "n" in progress.
NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion "n-1".					

Table IV. Control Functions When Using Serial Output.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-Scale Range Least Significant Bit (LSB)	±10 4.88mV	0V to 5V 1.22mV	0V to 4V 976µV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.99512V	4.99878V	3.999024V	0111 1111 1111 1111	7FF	1111 1111 1111 1111	FFF
Midscale	0V	2.5V	2V	0000 0000 0000 0000	000	1000 0000 0000 0000	800
One LSB Below Midscale	–4.88mV	2.49878V	1.999024V	1111 1111 1111 1111	FFF	0111 1111 1111 1111	7FF
–Full Scale	–10V	0V	0V	1000 0000 0000 0000	800	0000 0000 0000 0000	000

Table V. Output Codes and Ideal Input Voltages.

port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port, but data cannot be read through the serial port prior to reading the same data on the parallel port.

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{C}$ (pin 22) is HIGH and $\overline{CS}$ (pin 23) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17) . When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 4 least significant bits will be valid with the LSB on D4. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output will contain indeterminate data.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pins 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table VI and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to read data beyond 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table VI and Figures 2 and 3 for timing constraints.

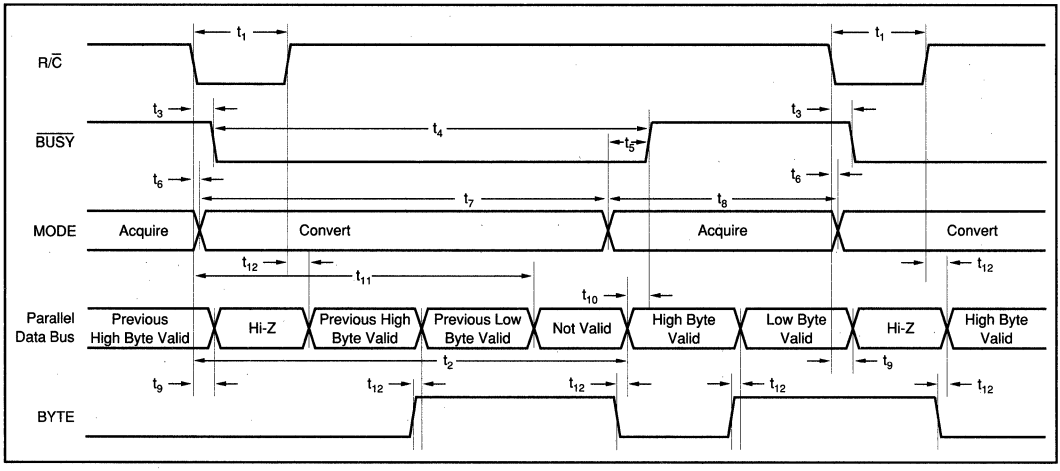


FIGURE 2. Conversion Timing with Parallel Output ($\overline{CS}$ and DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

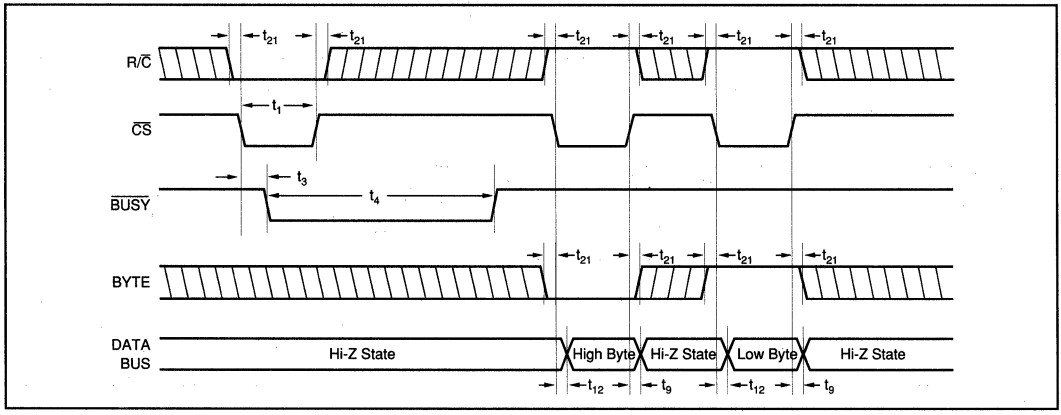


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing with Parallel Outputs.

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_2	Data Valid Delay after R/$\overline{C}$ LOW		14.7	20	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			85	ns
t_4	$\overline{BUSY}$ LOW		14.7	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		14.7	20	µs
t_8	Acquisition Time			5	µs
t_9	Bus Relinquish Time	10		83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	20	60		ns
t_{11}	Previous Data Valid after Start of Conversion	12	14.7		µs
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{16}	Data Valid after DATACLK LOW Delay	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK LOW	40			ns
t_{19}	External DATACLK HIGH	50			ns
t_{20}	$\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time	25			ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{22}	Valid Data after DATACLK HIGH	25			ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE VI. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During A Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7806 will output 12 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 19), synchronized to 12 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7806, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 19) after conversion 'n' is completed or during conversion 'n + 1'.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ LOW and use R/$\overline{C}$ to initiate conversions. While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12µs after the start of conversion 'n' until $\overline{BUSY}$ rises, the internal logic will shift the results of conversion 'n' into the output register. If $\overline{CS}$ is LOW, R/$\overline{C}$ is HIGH, and the external clock is HIGH at this point, data will be lost. So, with $\overline{CS}$ LOW, either R/$\overline{C}$ and/or DATACLK must be LOW during this period to avoid losing valid data.

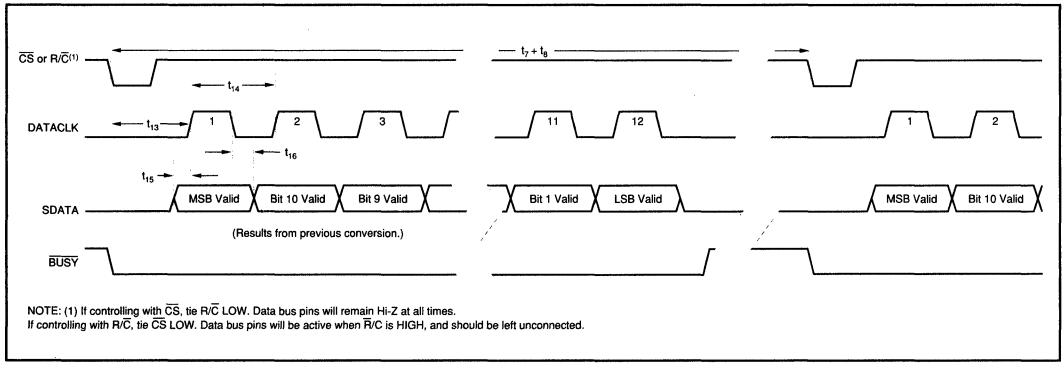


FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

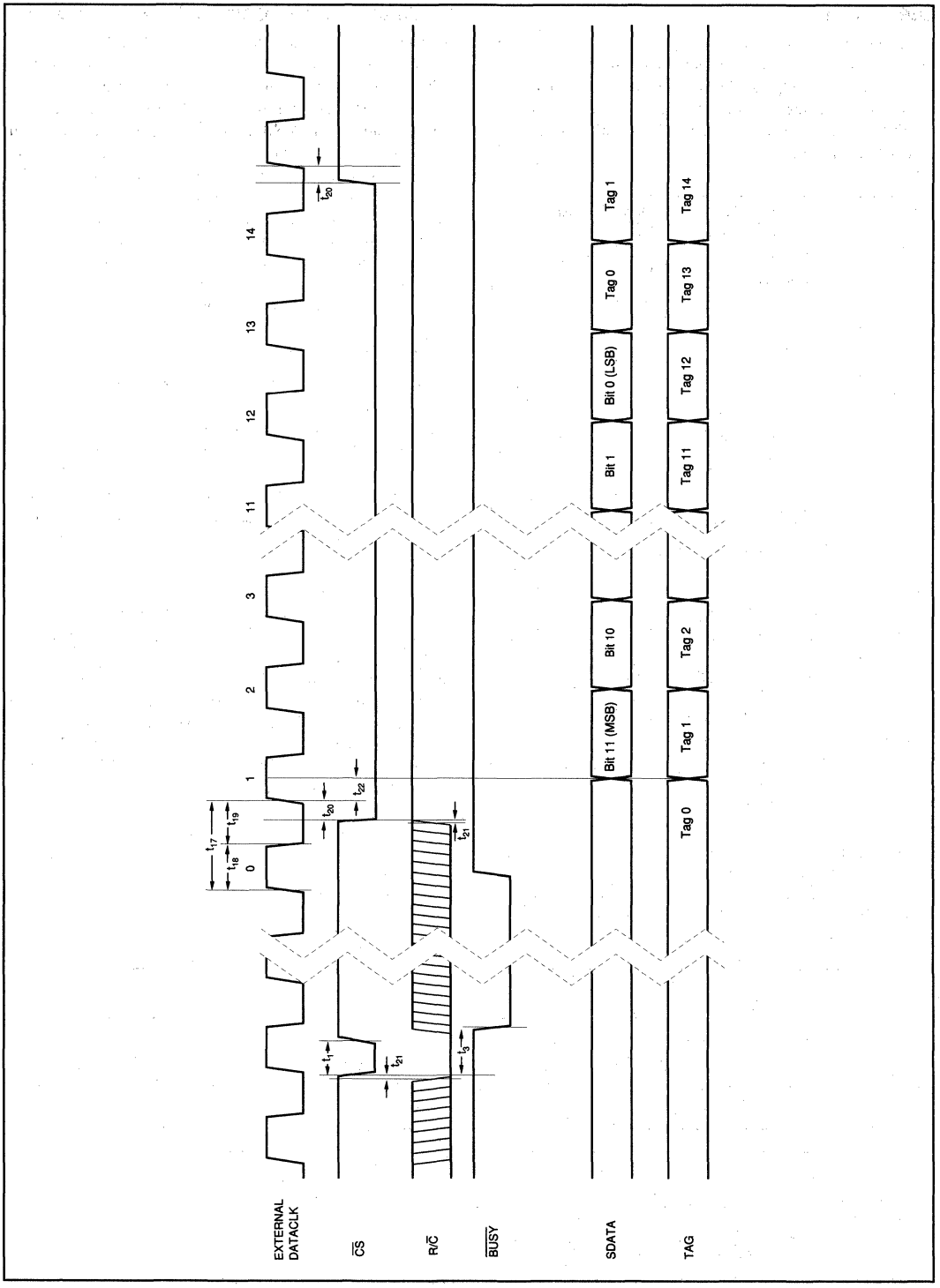


FIGURE 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied HIGH) Read after Conversion.

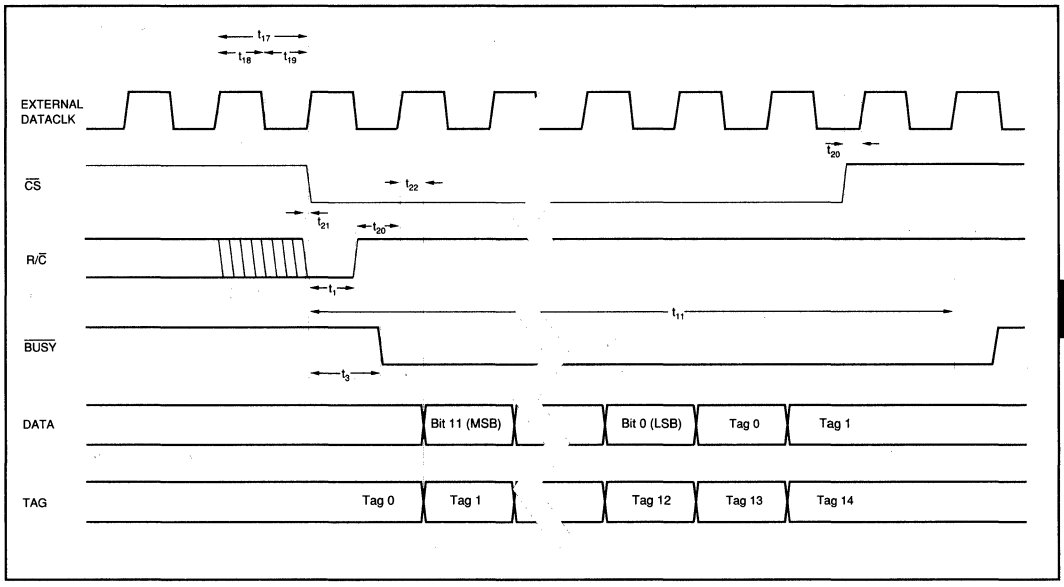


FIGURE 6. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH) Read During a Conversion.

EXTERNAL DATA CLOCK (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 12th falling edge and 13th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 13th falling edge and the 14th rising edge of DATACLK; the second input bit will be valid on the 14th falling edge and the 15th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table VI and Figure 5.

EXTERNAL DATA CLOCK (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to clock out data from 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

TAG FEATURE

TAG (Pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 12 bits of valid data have been output.

INPUT RANGES

The ADS7806 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 7a and 7b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 7b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

used for each input range (see Figure 8). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. There will be no wrapping or folding over for analog inputs outside the nominal range.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VII. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 7a).

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7806 in hardware, install the resistors shown in Figure 7a. Table VII lists the hardware trim ranges relative to the input for each input range.

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 7b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VIII for the range of offset and gain errors with and without the external resistors.

NO CALIBRATION

See Figure 7b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be consid-

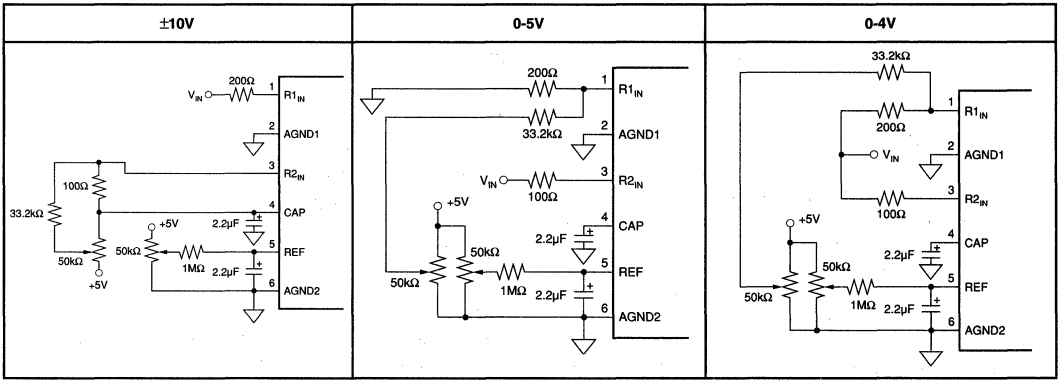


FIGURE 7a. Circuit Diagrams (With Hardware Trim).

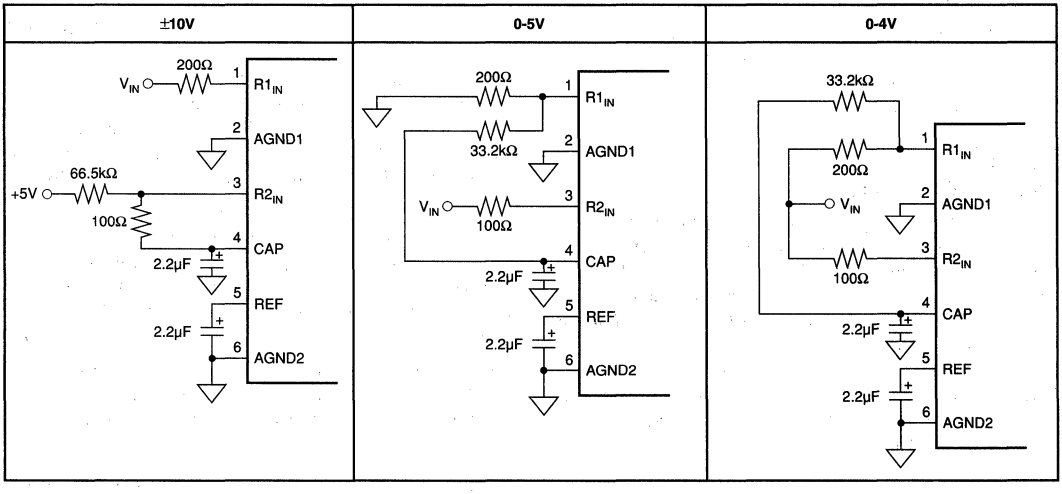


FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

ered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external resistors shown in Figure 7b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VIII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 8 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 9. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full specifications. The actual input impedance of the internal resistor network looking into pin 1 or pin 3 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ADS7806 can operate with its internal 2.5V reference or an external reference. By applying an external reference to

INPUT RANGE	OFFSET ERROR			GAIN ERROR		
	W/ RESISTORS	W/OUT RESISTORS		W/ RESISTORS	W/OUT RESISTORS	
(V)	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	–10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	+15	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–0.3 ≤ G ≤ 0.5 –0.1 ≤ G(1) ≤ 0.2	+0.05 +0.05
0 to 5	–3 ≤ UPO ≤ 3	–12 ≤ UPO ≤ –3	–7.5	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
0 to 4	–3 ≤ UPO ≤ 3	–10.5 ≤ UPO ≤ –1.5	–6	–0.4 ≤ G ≤ 0.4 –0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2

Note: (1) High Grade.

TABLE VIII. Range of Offset and Gain Errors with and without External Resistors

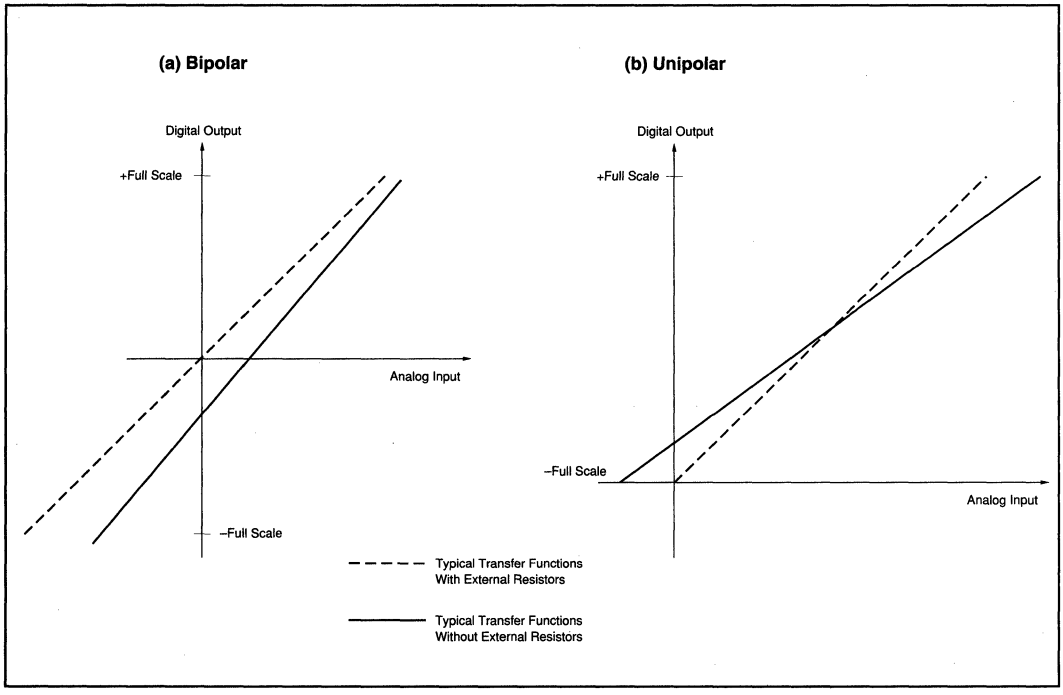


FIGURE 8. Typical Transfer Functions With and Without External Resistors.

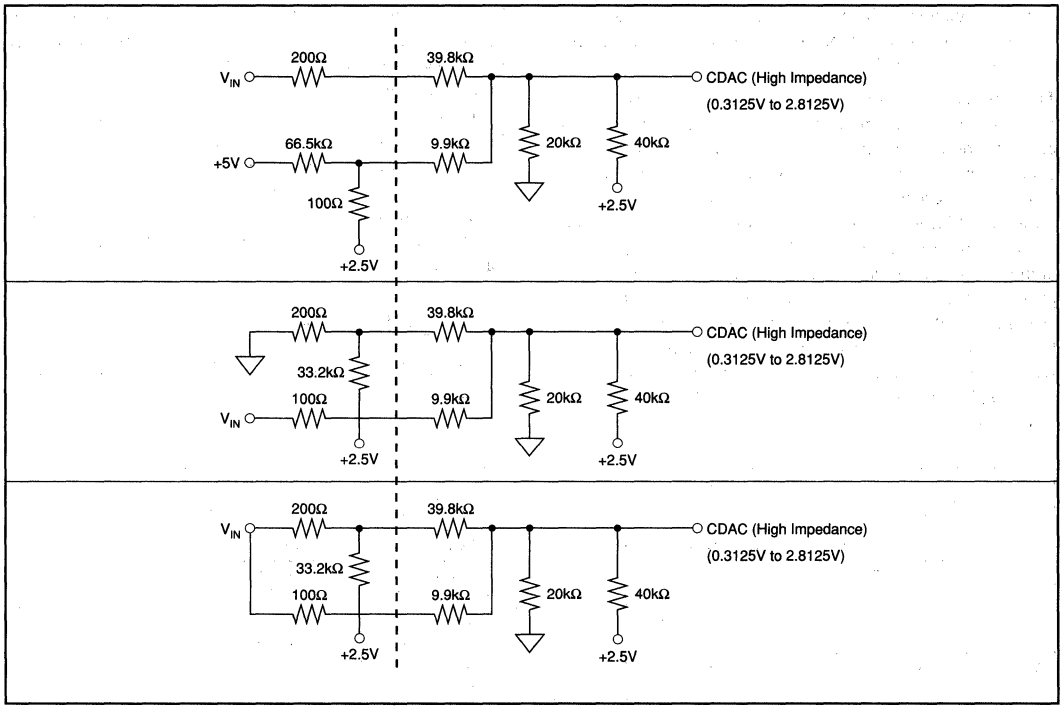


FIGURE 9. Circuit Diagrams Showing External and Internal Resistors.

pin 5, the internal reference can be bypassed; REFD (pin 26) tied HIGH will power-down the internal reference reducing the overall power consumption of the ADS7806 by approximately 5mW.

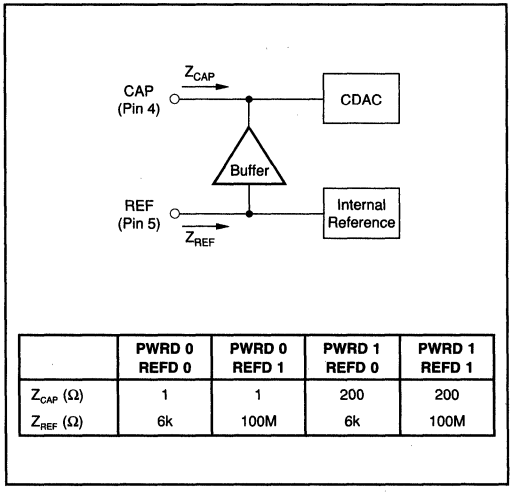
The internal reference has approximately an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

The ADS7806 also has an internal buffer for the reference voltage. See Figure 10 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 10. Characteristic Impedances of Internal Buffer.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the

output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

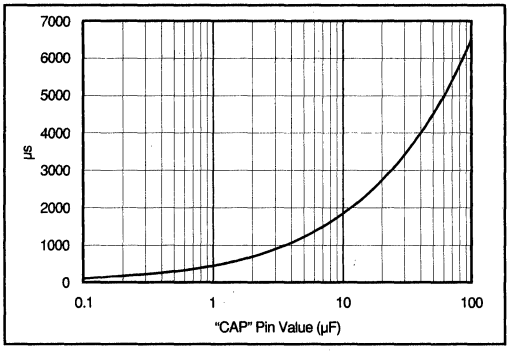


FIGURE 11. Power-Down to Power-Up Time vs Capacitor Value on CAP.

REFERENCE AND POWER DOWN

The ADS7806 has analog power down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26) respectively. PWRD and REFD HIGH will power down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms, using a 2.2µF capacitor connected to CAP. See Figure 11 for power-down to power-up recovery time relative to the capacitor value on CAP. With +5V applied to V_{DIG}, the digital circuitry of the ADS7806 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD HIGH will power down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

REFD

REFD HIGH will power down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7806 uses 90% of its power for the analog circuitry. The ADS7806 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7806. D_{GND} is the digital supply ground. A_{GND2} is the analog supply ground. A_{GND1} is the ground to which all analog signals internal to the A/D are referenced. A_{GND1} is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7806 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7806.

The resistive front end of the ADS7806 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7806 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7806 has an internal LSB size of 610μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance. The effects of this phenomenon will be more obvious when using the pin-compatible ADS7807 or any of the other 16-bit converters in the ADS Family. This is due to the smaller internal LSB size of 38μV.

APPLICATIONS INFORMATION

QSPI INTERFACING

Figure 12 shows a simple interface between the ADS7806 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7806 is the only serial peripheral.

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from LOW to HIGH occurs on Slave Select (SS) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the and the A/D may be "out-of-sync."

Figure 13 shows another interface between the ADS7806 and a QSPI equipped microcontroller. The interface allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7806 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated and prevent a conversion from taking place.

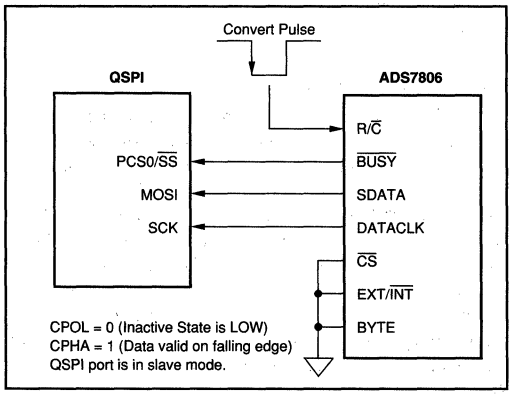


FIGURE 12. QSPI Interface to the ADS7806.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an eight bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go LOW starting a conversion. The second, a twelve bit transfer, causes only PCS1 ($\overline{CS}$) to go LOW. This is when the valid data will be transferred.

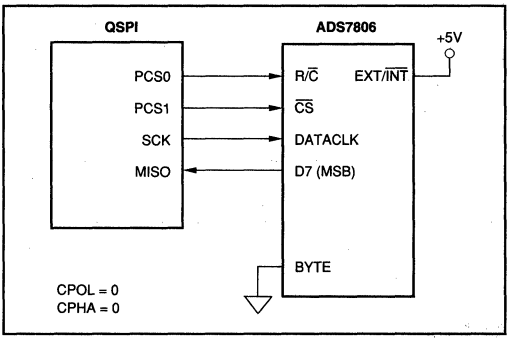


FIGURE 13. QSPI Interface to the ADS7806. Processor Initiates Conversions.

For both transfers, the DT register (delay after transfer) is used to cause a 19μs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7806. This timing is thus locked to the crystal based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to two (4.19MHz SCK), DT set to ten, the first serial transfer set to eight bits, the second set to twelve bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first eight bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the eight bit transfer should be set to 20H and for the twelve bit transfer to 61H.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 12. The microcontroller will need to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 13 might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse itself.

DSP56000 INTERFACING

The DSP56000 serial interface has an SPI compatibility mode with some enhancements. Figure 14 shows an interface between the ADS7806 and the DSP56000 which is very similar to the QSPI interface seen in Figure 12. As mentioned in the QSPI section, the DSP56000 must be programmed to enable the interface when a LOW to HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 15. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to two). The prescale modulus should be set to five.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet shows that the pulse width is (0.7)RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the **Starting A Conversion** section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is 35.6kHz. If a slower oscillator can be tolerated on the DSP56000, a conversion rate of 40kHz can be achieved by using a 19.2MHz clock and a prescale modulus of four.

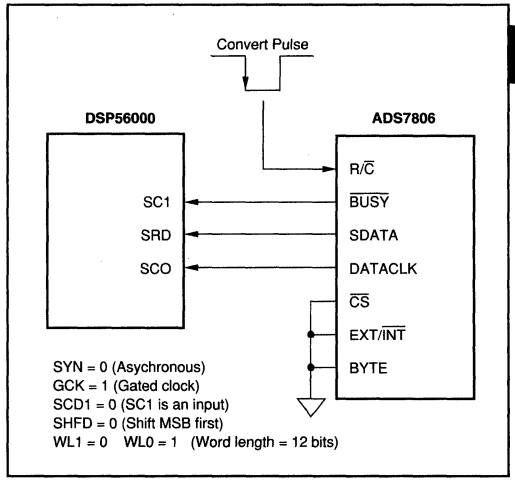


FIGURE 14. DSP56000 Interface to the ADS7806.

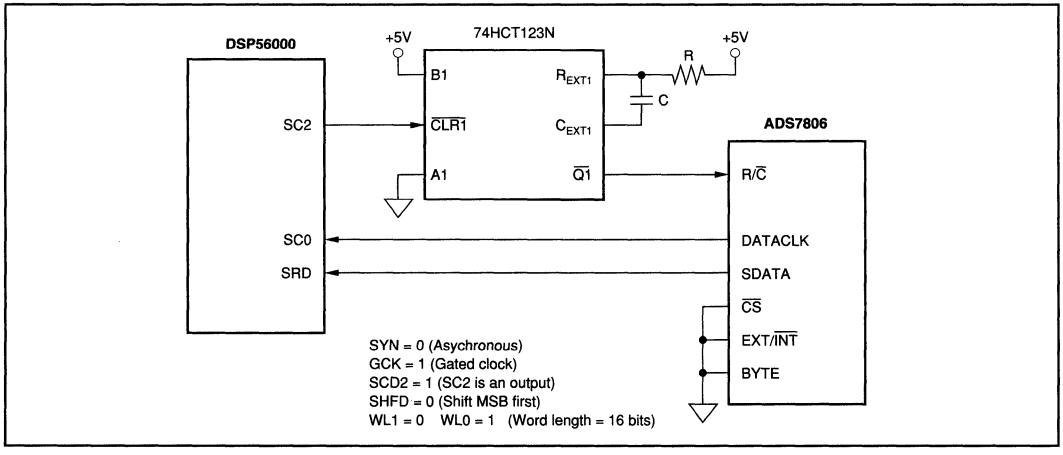


FIGURE 15. DSP56000 Interface to the ADS7806. Processor Initiates Conversions.

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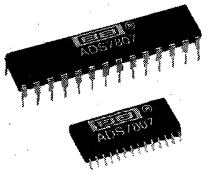


ADS7807

Low-Power 16-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

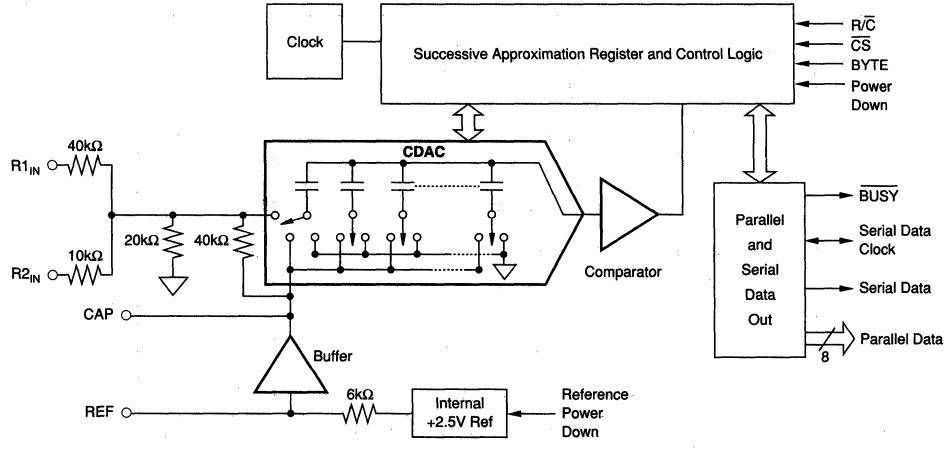
- **35mW max POWER DISSIPATION**
- **50µW POWER DOWN MODE**
- **25µs max ACQUISITION AND CONVERSION**
- **±1.5LSB max INL**
- **DNL: 16 bits "No Missing Codes"**
- **86dB min SINAD WITH 1kHz INPUT**
- **±10V, 0V TO +5V, AND 0V TO +4V INPUT RANGES**
- **SINGLE +5V SUPPLY OPERATION**
- **PARALLEL AND SERIAL DATA OUTPUT**
- **PIN-COMPATIBLE WITH 12-BIT ADS7806**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7807 is a low-power, 16-bit, sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7807 can acquire and convert 16-bits to within ±1.5LSB in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

The 28-pin ADS7807 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U			ADS7807PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0 to +5, 0 to +4				V
Impedance				(See Table II)				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, –2			+1.5, –1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			0.8			*		LSB
Gain Error			±0.2			±0.1		%
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5			*		ppm/°C
Bipolar Zero Error[3]	±10V Range			±10			*	mV
Bipolar Zero Error Drift	±10V Range		±0.5			*		ppm/°C
Unipolar Zero Error[3]	0V to 5V, 0V to 4V Ranges			±3			*	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down[5]	2.2µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V	90	100		96	*		dB[6]
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–100	–90		*	–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V	83	88		86	*		dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V	83	88		86	*		dB
Usable Bandwidth[7]			130			*		kHz
Full Power Bandwidth (–3dB)			600			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			20			*		ps
Transient Response	FS Step			5			*	µs
Overvoltage Recovery[8]			750			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS		Parallel 16 bits in 2-bytes; Serial						
Data Format		Binary Two's Complement or Straight Binary						
Data Coding								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7807P, U			ADS7807PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	R_L = 3.3kΩ, C_L = 50pF			83			*	ns
Bus Relinquish Time	R_L = 3.3kΩ, C_L = 10pF			83			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.6			*		mA
I_{ANA}			5.0			*		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, f_S = 40kHz		28	35		*	*	mW
	REFD HIGH		23			*		mW
	PWRD and REFD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 305µV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) This is the time delay after the ADS7807 is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert Command after this delay will yield accurate results. (6) All specifications in dB are referred to a full-scale input. (7) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (8) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, and AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	GUARANTEED NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7807P	±3	15	83	–40°C to +85°C	Plastic DIP
ADS7807PB	±1.5	16	86	–40°C to +85°C	Plastic DIP
ADS7807U	±3	15	83	–40°C to +85°C	SOIC
ADS7807UB	±1.5	16	86	–40°C to +85°C	SOIC

PACKAGE INFORMATION

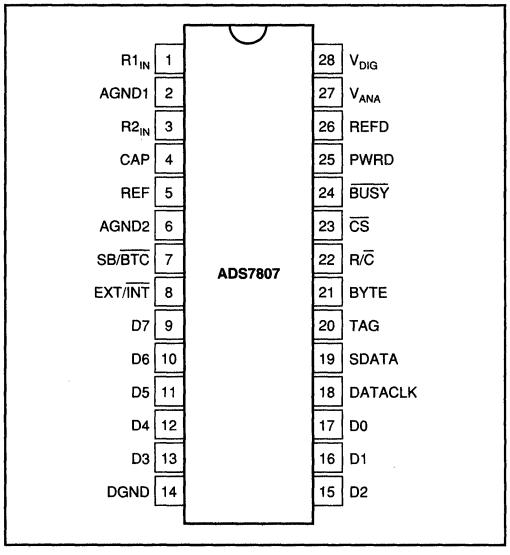
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS7807P	Plastic DIP	246
ADS7807PB	Plastic DIP	246
ADS7807U	SOIC	217
ADS7807UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$R1_{IN}$		Analog Input. See Figure 7.
2	AGND1		Analog Sense Ground.
3	$R2_{IN}$		Analog Input. See Figure 7.
4	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
5	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
6	AGND2		Analog Ground.
7	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
8	EXT/$\overline{INT}$	I	External/Internal data clock select.
9	D7	O	Data Bit 7 if BYTE is HIGH. Data bit 15 (MSB) if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW. Leave unconnected when using serial output.
10	D6	O	Data Bit 6 if BYTE is HIGH. Data bit 14 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
11	D5	O	Data Bit 5 if BYTE is HIGH. Data bit 13 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
12	D4	O	Data Bit 4 if BYTE is HIGH. Data bit 12 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
13	D3	O	Data Bit 3 if BYTE is HIGH. Data bit 11 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D2	O	Data Bit 2 if BYTE is HIGH. Data bit 10 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
16	D1	O	Data Bit 1 if BYTE is HIGH. Data bit 9 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
17	D0	O	Data Bit 0 (LSB) if BYTE is HIGH. Data bit 8 if BYTE is LOW. Hi-Z when $\overline{CS}$ is HIGH and/or R/$\overline{C}$ is LOW.
18	DATACLK	I/O	Data Clock Output when EXT/$\overline{INT}$ is LOW. Data clock input when EXT/$\overline{INT}$ is HIGH.
19	SDATA	O	Serial Output Synchronized to DATACLK.
20	TAG	I	Serial Input When Using an External Data Clock.
21	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH) on parallel output pins.
22	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
23	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ is LOW, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is LOW, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	PWRD HIGH shuts down all analog circuitry except the reference. Digital circuitry remains active.
26	REFD	I	REFD HIGH shuts down the internal reference. External reference will be required for conversions.
27	V_{ANA}		Analog Supply. Nominally +5V. Decouple with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



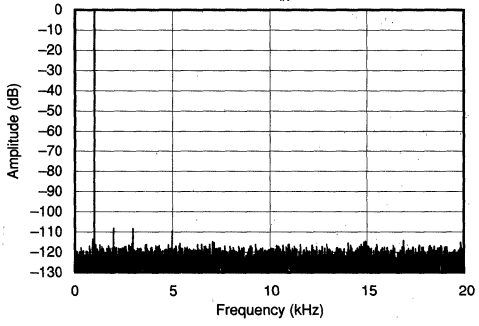
ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

TABLE II. Input Range Connections. See also Figure 7.

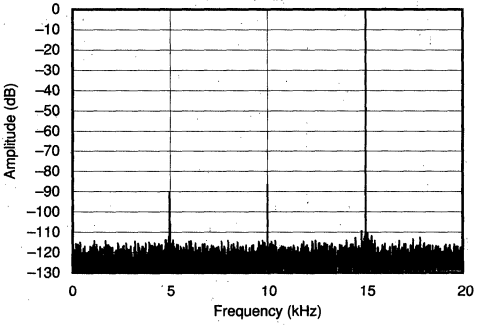
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

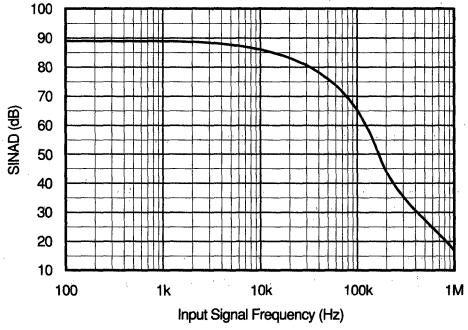
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



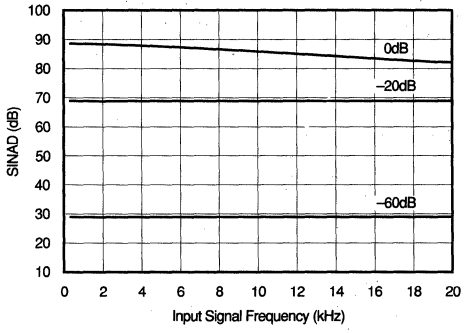
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



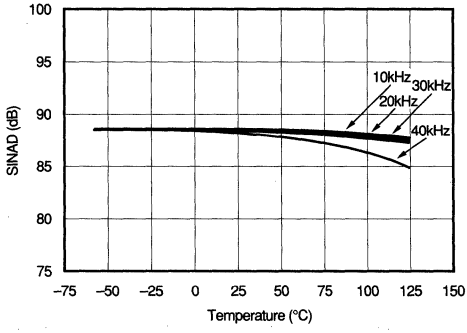
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



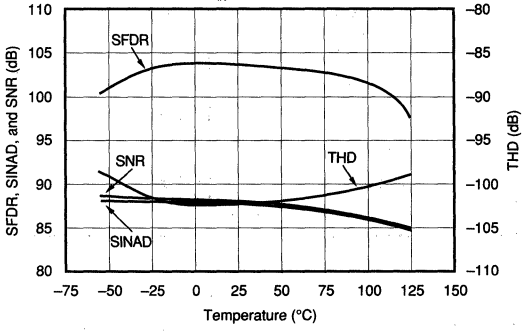
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

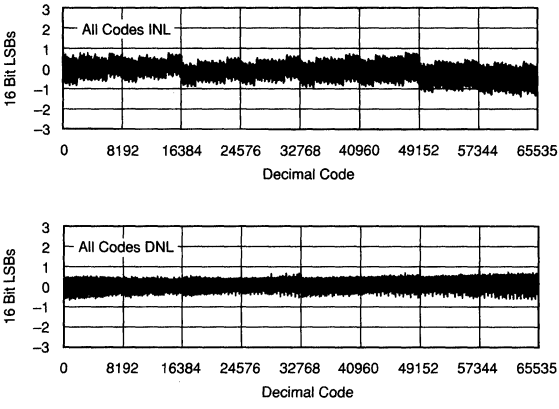


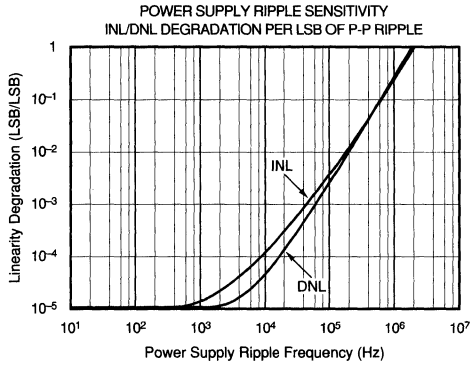
A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

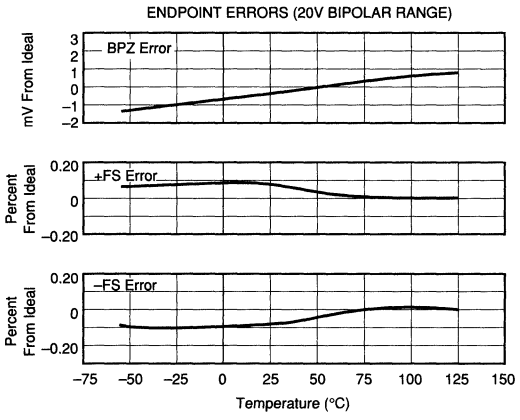


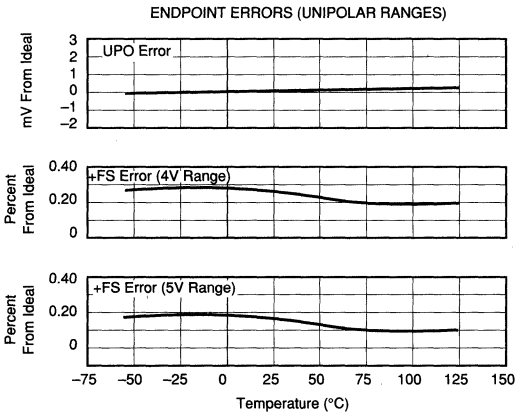
TYPICAL PERFORMANCE CURVES (CONT)

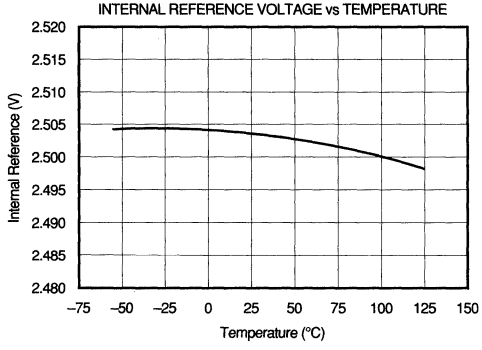
At T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 7b, unless otherwise specified.

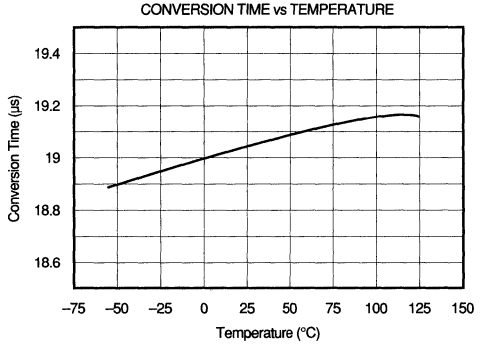












BASIC OPERATION

PARALLEL OUTPUT

Figure 1a) shows a basic circuit to operate the ADS7807 with a ±10V input range and parallel output. Taking R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns (12µs max) will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the 8 most significant bits will be valid when $\overline{BUSY}$ rises; if BYTE is HIGH, the 8 least significant bits will be valid when $\overline{BUSY}$ rises. Data will be output in Binary Two's Complement format. $\overline{BUSY}$ going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

SERIAL OUTPUT

Figure 1b) shows a basic circuit to operate the ADS7807 with a ±10V input range and serial output. Taking R/$\overline{C}$ (pin 22) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 19) synchronized to 16 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns puts the sample/hold of the ADS7807 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

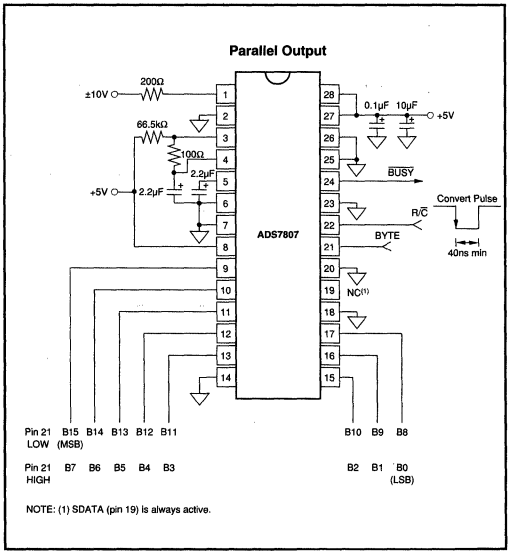


FIGURE 1a. Basic ±10V Operation, both Parallel and Serial Output.

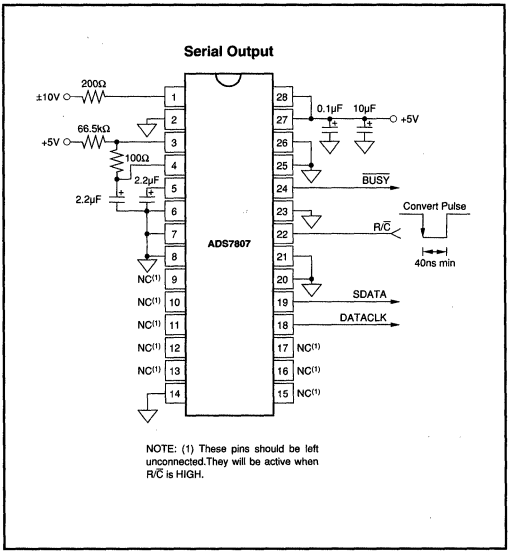


FIGURE 1b. Basic ±10V Operation with Serial Output.

The ADS7807 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. Refer to Tables III and IV for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 6 for timing diagrams.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.
NOTE: (1) See Figures 2 and 3 for constraints on data valid from conversion "n-1".			

Table III. Control Functions When Using Parallel Output (DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is LOW when initiating conversion 'n', serial data from conversion 'n-1' will be output on SDATA (pin 19) following the start of conversion 'n'. See **Internal Data Clock** in the **Reading Data** section.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output and the serial output (only when using an external data clock) will be affected whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

READING DATA

The ADS7807 outputs serial or parallel data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{BTC}$ (pin 7) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table V for ideal output codes.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
0	↓	1	1	Input	Initiates conversion "n". Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion "n" completed. Valid data from conversion "n" clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	↑	0	1	Input	Valid data from conversion "n-1" output on SDATA synchronized to external data clock. Conversion "n" in progress.
0	0	↑	X	X	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion "n" in progress.
NOTE: (1) See Figures 4, 5, and 6 for constraints on data valid from conversion "n-1".					

Table IV. Control Functions When Using Serial Output.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-Scale Range Least Significant Bit (LSB)	±10 305µV	0V to 5V 76µV	0V to 4V 61µV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.999695V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

Table V. Output Codes and Ideal Input Voltages.

port will shift the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port, but data cannot be read through the serial port prior to reading the same data on the parallel port.

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) HIGH and DATACLK (pin 18) LOW. SDATA (pin 19) should be left unconnected. The parallel output will be active when R/$\overline{C}$ (pin 22) is HIGH and $\overline{CS}$ (pin 23) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17) . When BYTE (pin 21) is LOW, the 8 most significant bits will be valid with the MSB on D7. When BYTE is HIGH, the 8 least significant bits will be valid with the LSB on D0. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output will contain indeterminate data.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. Valid data from conversion 'n' will be available on D7-D0 (pins 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table VI and Figures 2 and 3 for timing constraints.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to read data beyond 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) goes HIGH; this may result in reading invalid data. Refer to Table VI and Figures 2 and 3 for timing constraints.

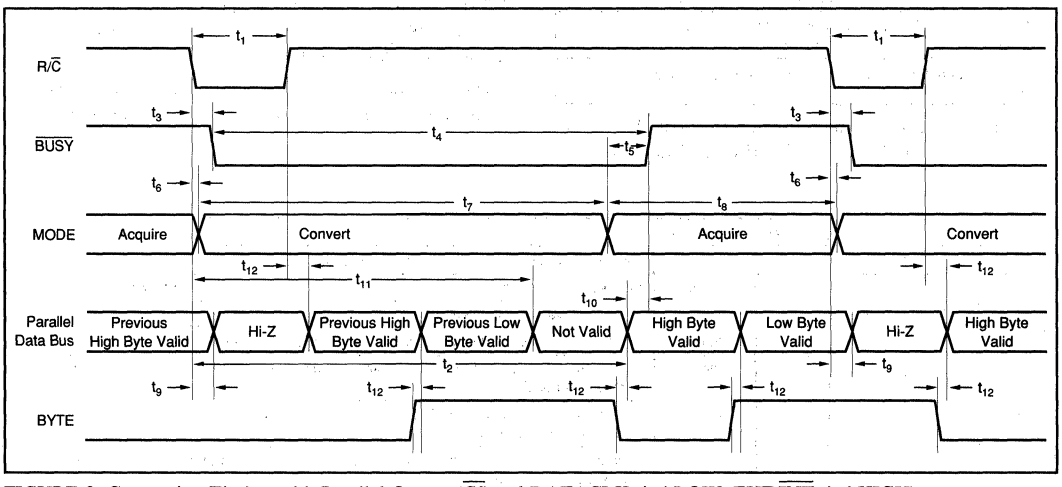


FIGURE 2. Conversion Timing with Parallel Output ($\overline{CS}$ and DATACLK tied LOW, EXT/$\overline{INT}$ tied HIGH).

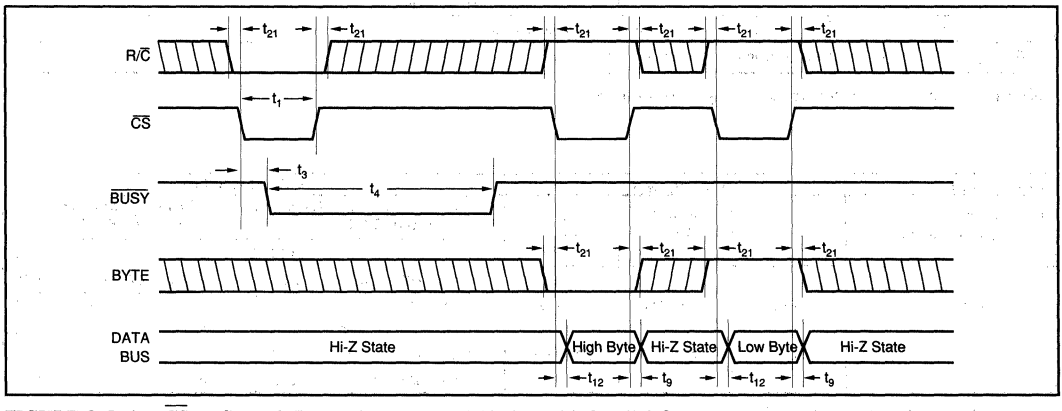


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing with Parallel Outputs.

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins will come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is LOW and R/$\overline{C}$ (pin 22) is HIGH. The serial output can not be tri-stated and is always active. Refer to the **Applications Information** section for specific serial interfaces.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_2	Data Valid Delay after R/$\overline{C}$ LOW		19	20	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			85	ns
t_4	$\overline{BUSY}$ LOW		19	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		19	20	µs
t_8	Acquisition Time			5	µs
t_9	Bus Relinquish Time	10		83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	20	60		ns
t_{11}	Previous Data Valid after Start of Conversion	12	19		µs
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{16}	Data Valid after DATACLK LOW Delay	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK LOW	40			ns
t_{19}	External DATACLK HIGH	50			ns
t_{20}	$\overline{CS}$ and R/$\overline{C}$ to External DATACLK Setup Time	25			ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{22}	Valid Data after DATACLK HIGH	25			ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE VI. Conversion and Data Timing. T_A = –40°C to +85°C.

INTERNAL DATA CLOCK (During a Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) LOW. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ADS7807 will output 16 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 19), synchronized to 16 clock pulses output on DATACLK (pin 18). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 16th clock pulse, DATACLK will remain LOW until the next conversion is initiated, while SDATA will go to whatever logic level was input on TAG (pin 20) during the first clock pulse. Refer to Table VI and Figure 4.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) HIGH. The external data clock is not a conversion clock; it can only be used as a data clock. To enable the output mode of the ADS7807, $\overline{CS}$ (pin 23) must be LOW and R/$\overline{C}$ (pin 22) must be HIGH. DATACLK must be HIGH for 20% to 70% of the total data clock period; the clock rate can be between DC and 10MHz. Serial data from conversion 'n' can be output on SDATA (pin 19) after conversion 'n' is completed or during conversion 'n + 1'.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ LOW and use R/$\overline{C}$ to initiate conversions.

While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12µs after the start of conversion 'n' until $\overline{BUSY}$ rises, the internal logic will shift the results of conversion 'n' into the output register. If $\overline{CS}$ is LOW, R/$\overline{C}$ HIGH, and the external clock is HIGH at this point, data will be lost. So, with $\overline{CS}$ LOW, either R/$\overline{C}$ and/or DATACLK must be LOW during this period to avoid losing valid data.

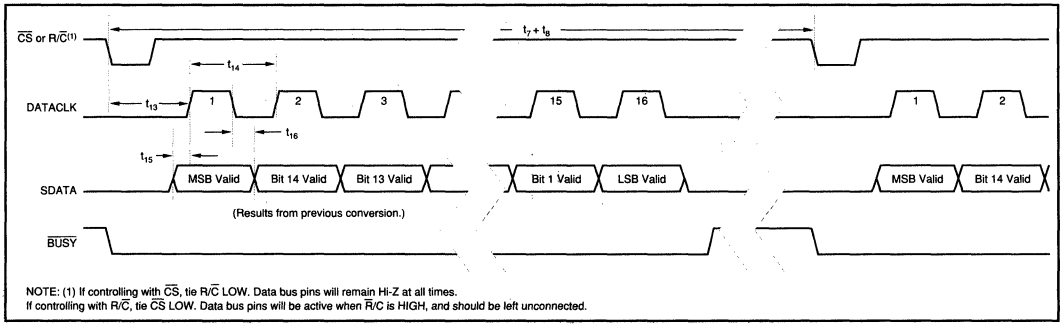


FIGURE 4. Serial Data Timing Using Internal Data Clock (TAG tied LOW).

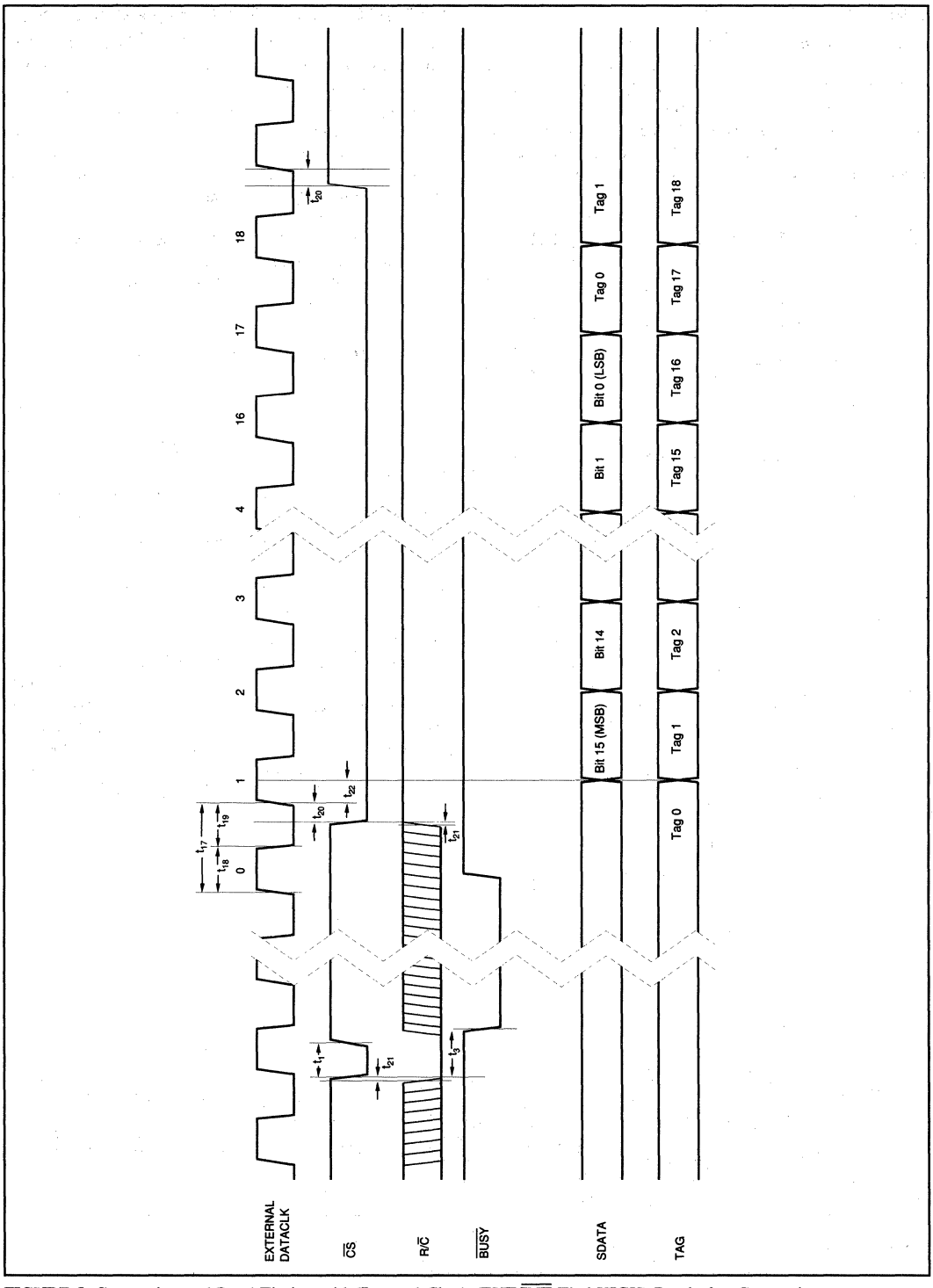


FIGURE 5. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied HIGH) Read after Conversion.

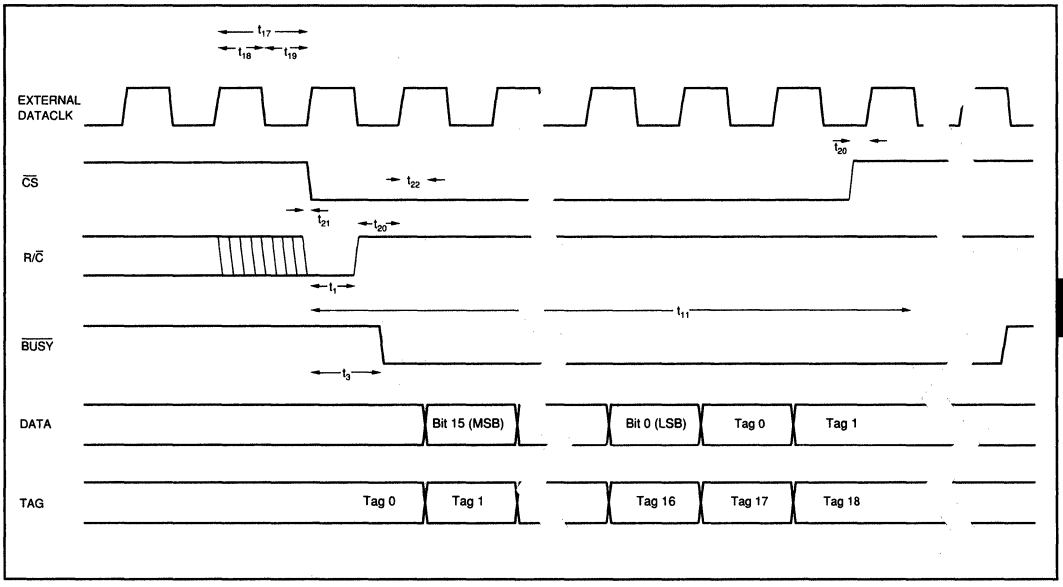


FIGURE 6. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH) Read During a Conversion.

EXTERNAL DATA CLOCK (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) will go HIGH. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, valid data from conversion 'n' will be output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB will be valid on the first falling edge and the second rising edge of the external data clock. The LSB will be valid on the 16th falling edge and 17th rising edge of the data clock. TAG (pin 20) will input a bit of data for every external clock pulse. The first bit input on TAG will be valid on SDATA on the 17th falling edge and the 18th rising edge of DATACLK; the second input bit will be valid on the 18th falling edge and the 19th rising edge, etc. With a continuous data clock, TAG data will be output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table VI and Figure 5.

EXTERNAL DATA CLOCK (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 12µs after the start of conversion 'n'. Do not attempt to clock out data from 12µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 24) rises; this will result in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table VI and Figure 6.

TAG FEATURE

TAG (Pin 20) inputs serial data synchronized to the external or internal data clock.

When using an external data clock, the serial bit stream input on TAG will follow the LSB output on SDATA until the internal output register is updated with new conversion results. See Table VI and Figures 5 and 6.

The logic level input on TAG for the first rising edge of the internal data clock will be valid on SDATA after all 16 bits of valid data have been output.

INPUT RANGES

The ADS7807 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 7a and 7b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 7b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

used for each input range (see Figure 8). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. Wrapping or folding over for analog inputs outside the nominal range will not occur.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VII. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 7a).

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7807 in hardware, install the resistors shown in Figure 7a. Table VII lists the hardware trim ranges relative to the input for each input range.

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 7b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VIII for the range of offset and gain errors with and without the external resistors.

NO CALIBRATION

See Figure 7b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

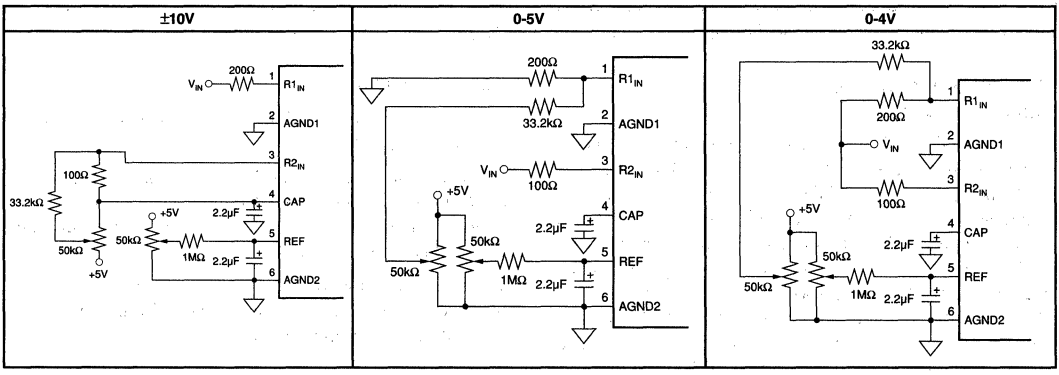


FIGURE 7a. Circuit Diagrams (With Hardware Trim).

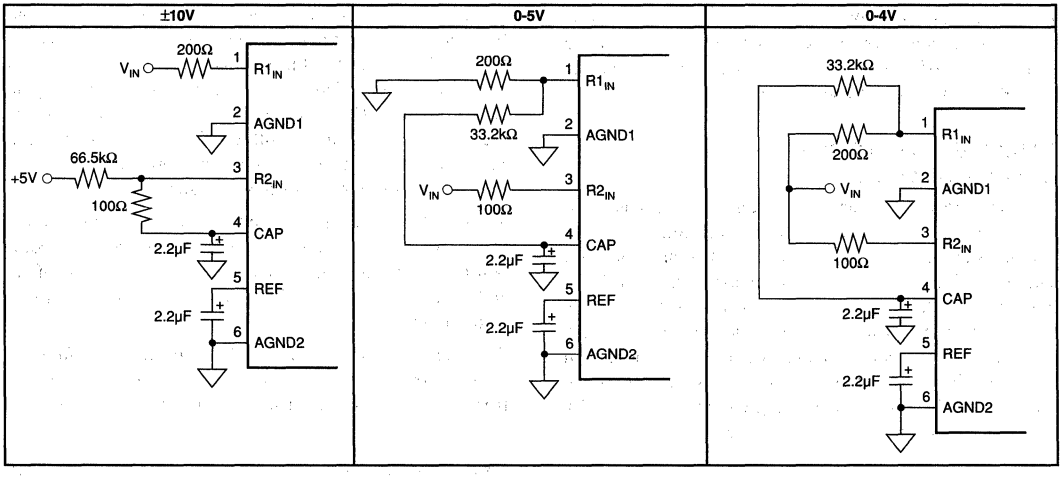


FIGURE 7b. Circuit Diagrams (Without Hardware Trim).

The external resistors shown in Figure 7b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VIII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 8 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 9. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full scale specifications. The actual input impedance of the internal resistor network looking into pin 1 or pin 3 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ADS7807 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed; REFD (pin 26) tied HIGH will power-down the internal reference reducing

INPUT RANGE	OFFSET ERROR			GAIN ERROR		
	W/ RESISTORS	W/OUT RESISTORS		W/ RESISTORS	W/OUT RESISTORS	
(V)	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	–10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	15	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–0.3 ≤ G ≤ 0.5 –0.1 ≤ G(1) ≤ 0.2	+0.05 +0.05
0 to 5	–3 ≤ UPO ≤ 3	–12 ≤ UPO ≤ –3	–7.5	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
0 to 4	–3 ≤ UPO ≤ 3	–10.5 ≤ UPO ≤ –1.5	–6	–0.4 ≤ G ≤ 0.4 –0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
Note: (1) High Grade.						

TABLE VIII. Range of Offset and Gain Errors with and without External Resistors.

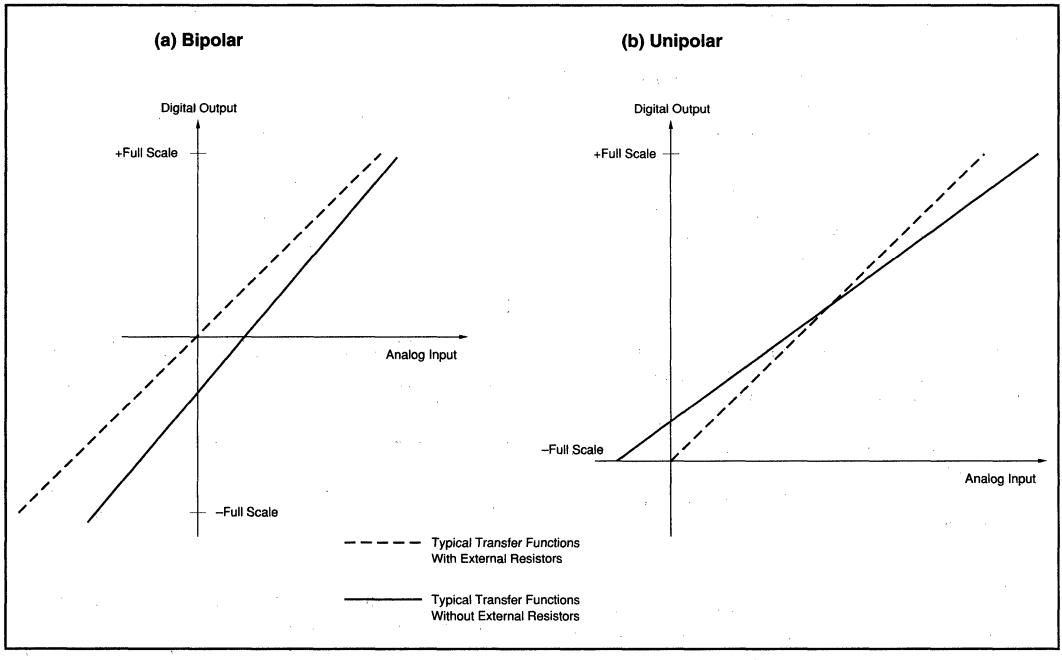


FIGURE 8. Typical Transfer Functions With and Without External Resistors.

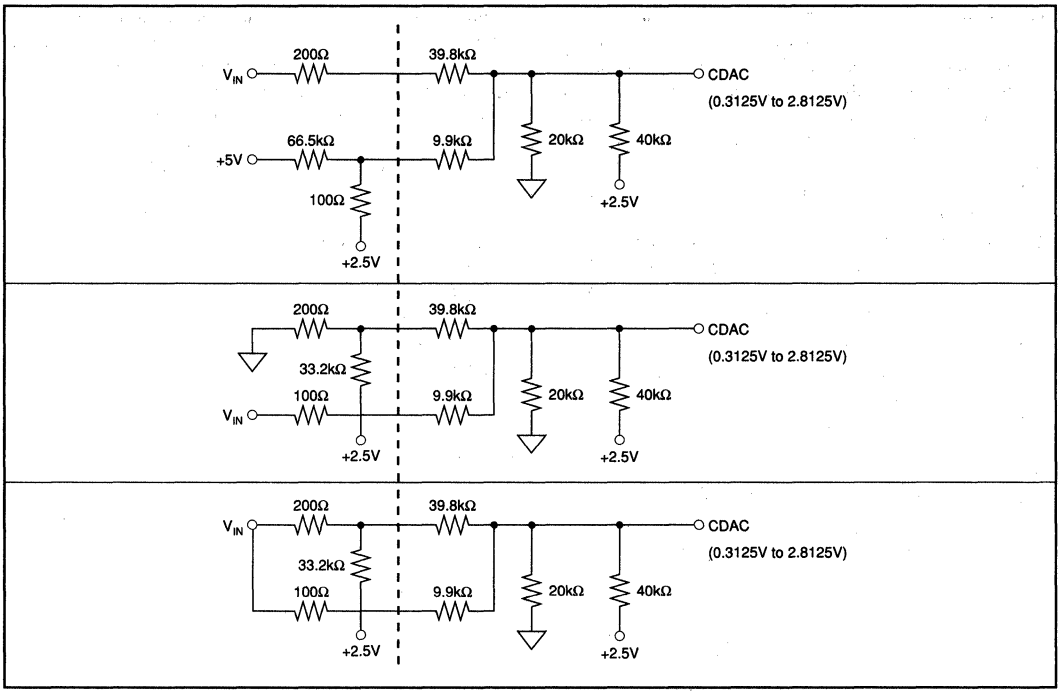


FIGURE 9. Circuit Diagrams Showing External and Internal Resistors.

the overall power consumption of the ADS7807 by approximately 5mW.

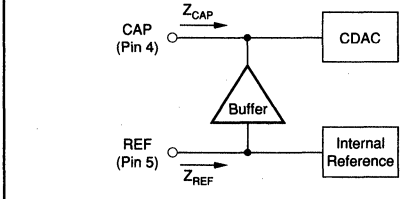
The internal reference has approximately an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

The ADS7807 also has an internal buffer for the reference voltage. See Figure 10 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 10.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 10. Characteristic Impedances of Internal Buffer.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion

cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figures 10 and 11.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

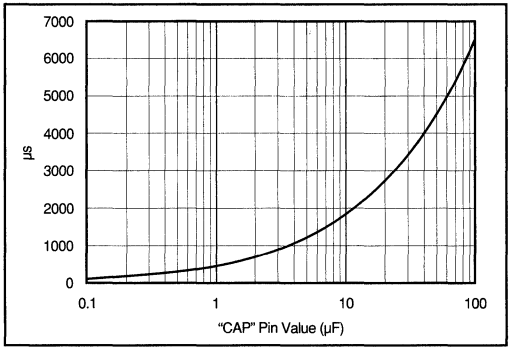


FIGURE 11. Power-Down to Power-Up Time vs Capacitor Value on CAP.

REFERENCE AND POWER DOWN

The ADS7807 has analog power down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26) respectively. PWRD and REFD HIGH will power down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50µW. Power recovery is typically 1ms, using a 2.2µF capacitor connected to CAP. See Figure 11 for power-down to power-up recovery time relative to the capacitor value on CAP. With +5V applied to V_{DIG}, the digital circuitry of the ADS7807 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD HIGH will power down all of the analog circuitry except for the reference. Data from the previous conversion will be maintained in the internal registers and can still be read. With PWRD HIGH, a convert command yields meaningless data.

REFD

REFD HIGH will power down the internal 2.5V reference. All other analog circuitry, including the reference buffer, will be active. REFD should be HIGH when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 10 for the characteristic impedance of the reference buffer's input for both REFD HIGH and LOW. The internal reference consumes approximately 5mW.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7807 uses 90% of its power for the analog circuitry. The ADS7807 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7807. D_{GND} is the digital supply ground. A_{GND2} is the analog supply ground. A_{GND1} is the ground to which all analog signals internal to the A/D are referenced. A_{GND1} is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS7807 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7807.

The resistive front end of the ADS7807 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS7807 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7807 has an internal LSB size of 38μV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

APPLICATIONS INFORMATION

TRANSITION NOISE

Apply a DC input to the ADS7807 and initiate 1000 conversions. The digital output of the converter will vary in output codes due to the internal noise of the ADS7807. This is true for all 16-bit SAR converters. The transition noise specification found in the electrical specifications section is a statistical figure which represents the one sigma limit or rms value of these output codes.

Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal output code for the input voltage value. The ±1σ, ±2σ, and ±3σ distributions will represent 68.3%, 95.5%, and 99.7% of all codes. Multiplying TN by 6 will yield the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the 5 code distribution when executing 1000 conversions. The ADS7807 has a TN of 0.8 LSBs which yields 5 output codes for a ±3σ distribution. See Figures 12 and 13 for 1000 and 10,000 conversion histogram results.

AVERAGING

The noise of the converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$ where n is the number of averages. For example, averaging four conversion results will reduce the TN by 1/2 to 0.4 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to lowpass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by two, the signal-to-noise ratio will improve 3dB.

QSPI INTERFACING

Figure 14 shows a simple interface between the ADS7807 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7807 is the only serial peripheral.

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from LOW to HIGH occurs on Slave Select (SS) from BUSY (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the A/D may be "out-of-sync".

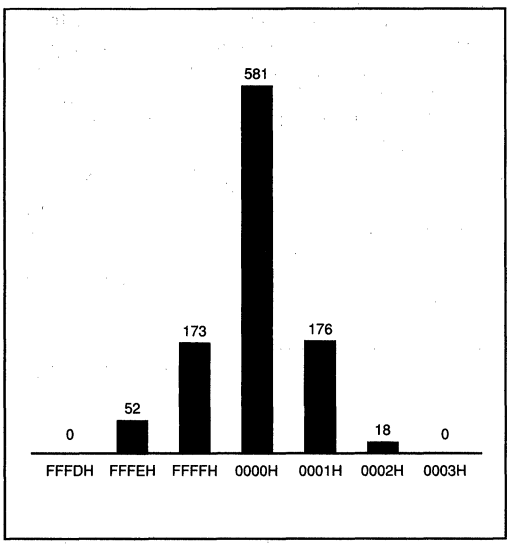


FIGURE 12. Histogram of 1000 Conversions with Input Grounded.

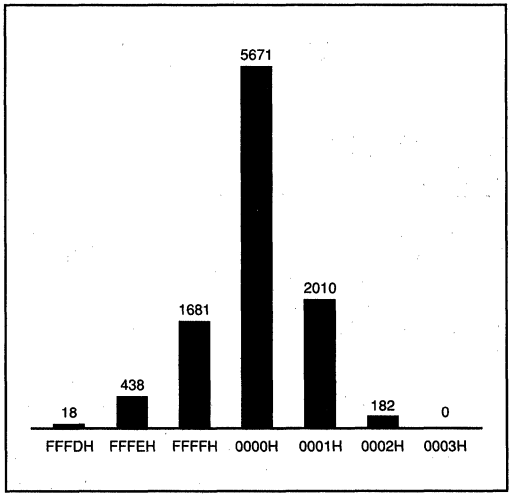


FIGURE 13. Histogram of 10,000 Conversions with Input Grounded.

Figure 15 shows another interface between the ADS7807 and a QSPI equipped microcontroller which allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS7807 instead of the serial output (SDATA). Using D7 instead of the serial port offers tri-state capability which allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left HIGH; that will keep D7 tri-stated.

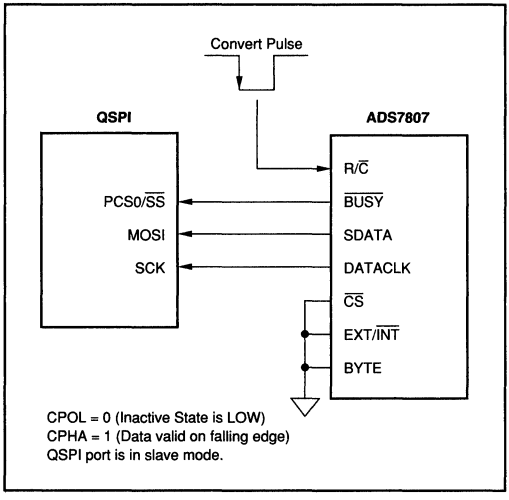


FIGURE 14. QSPI Interface to the ADS7807.

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an eight bit transfer, causes PCS0 (R/$\overline{C}$) and PCS1 ($\overline{CS}$) to go LOW starting a conversion. The second, a sixteen bit transfer, causes only PCS1 ($\overline{CS}$) to go LOW. This is when the valid data will be transferred.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine which generates the appropriate timing for the ADS7807. This timing is thus locked to the crystal based timing of the microcontroller and not interrupt driven. So, this interface is appropriate for both AC and DC measurements.

For the fastest conversion rate, the baud rate should be set to two (4.19MHz SCK), DT set to ten, the first serial transfer set to eight bits, the second set to 16 bits, and DSCK disabled (in the command control byte). This will allow for a 23kHz maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently

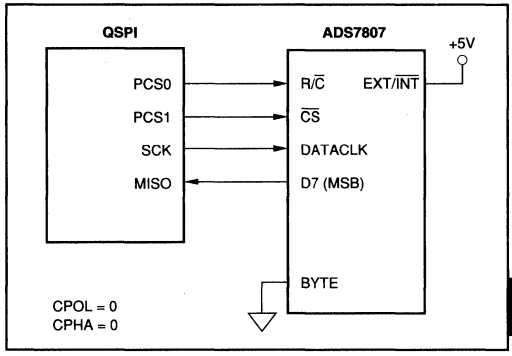


FIGURE 15. QSPI Interface to the ADS7807. Processor Initiates Conversions.

initiating a second conversion during the first eight bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally LOW and data captured on the rising edge). The command control byte for the eight bit transfer should be set to 20H and for the sixteen bit transfer to 61H.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 14. The microcontroller will need to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 15 might be possible. For most microcontrollers with SPI interface, the automatic generation of the start-of-conversion pulse will be impossible and will have to be done with software. This will limit the interface to 'DC' applications due to the insufficient jitter performance of the convert pulse itself.

DSP56000 INTERFACING

The DSP56000 serial interface has SPI compatibility mode with some enhancements. Figure 16 shows an interface between the ADS7807 and the DSP56000 which is very similar to the QSPI interface seen in Figure 14. As mentioned in the QSPI section, the DSP56000 must be programmed to enable the interface when a LOW to HIGH transition on SC1 is observed ($\overline{BUSY}$ going HIGH at the end of conversion).

The DSP56000 can also provide the convert pulse by including a monostable multi-vibrator as seen in Figure 17. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to two). The prescale modulus should be set to three.

The monostable multi-vibrator in this circuit will provide varying pulse widths for the convert pulse. The pulse width will be determined by the external R and C values used with the multi-vibrator. The 74HCT123N data sheet shows that the pulse width is (0.7) RC. Choosing a pulse width as close to the minimum value specified in this data sheet will offer the best performance. See the **Starting A Conversion** section of this data sheet for details on the conversion pulse width.

The maximum conversion rate for a 20.48MHz DSP56000 is exactly 40kHz. Note that this will not be the case for the ADS7806. See the ADS7806 data sheet for more information.

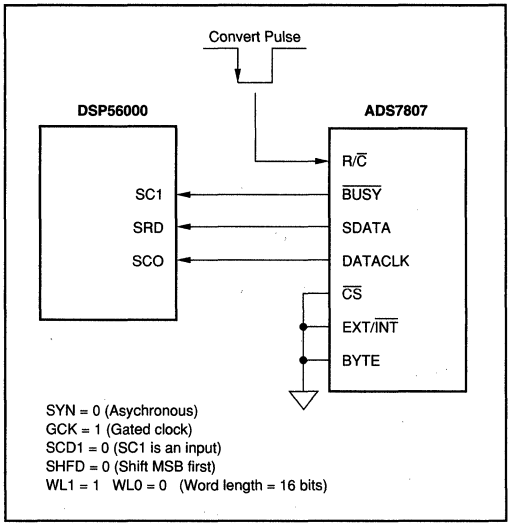


FIGURE 16. DSP56000 Interface to the ADS7807.

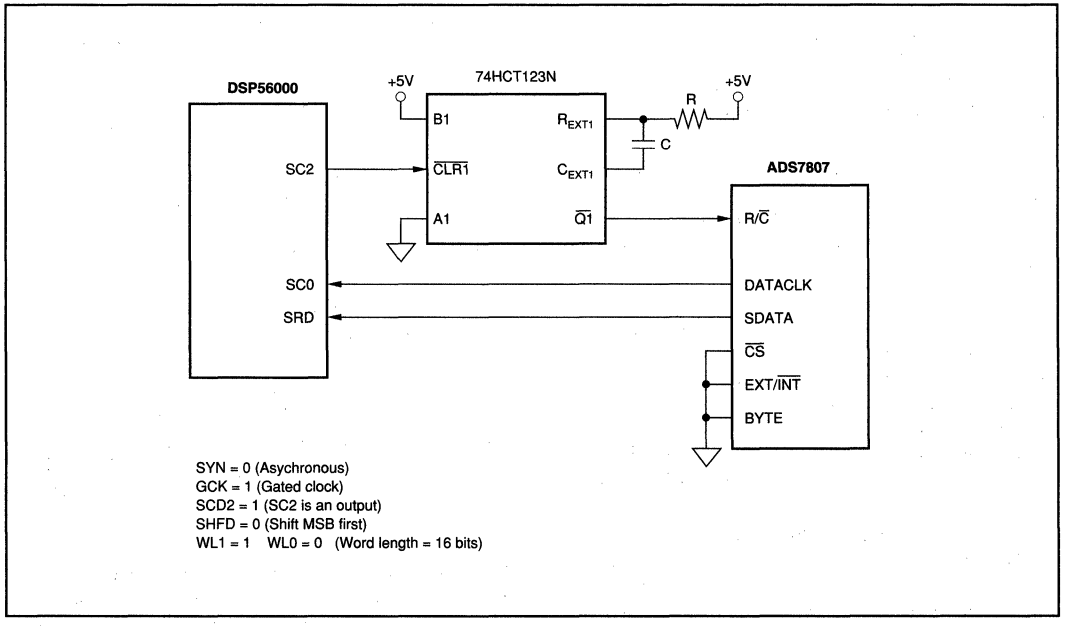


FIGURE 17. DSP56000 Interface to the ADS7807. Processor Initiates Conversions.

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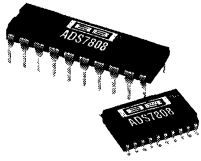


ADS7808

DEMO BOARD AVAILABLE
See Appendix A

12-Bit 10µs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

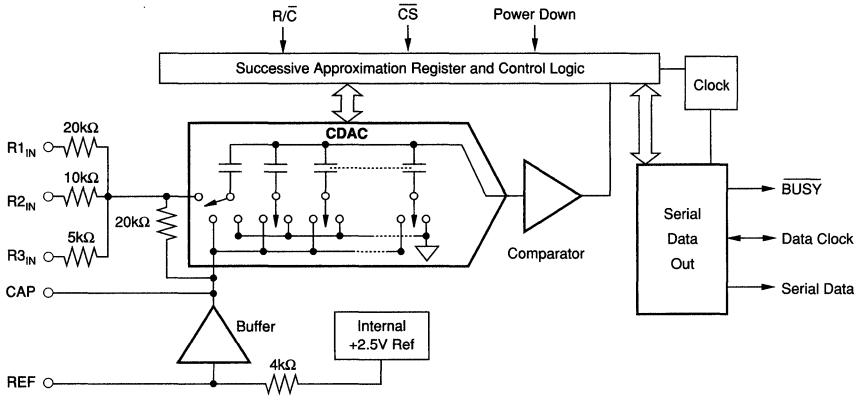
- 100kHz SAMPLING RATE
- 72dB SINAD WITH 45kHz INPUT
- ±1/2 LSB INL AND DNL
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7809
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

DESCRIPTION

The ADS7808 is a complete 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 12-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7808 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7808 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7808 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



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SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808P/U MIN	ADS7808P/U TYP	ADS7808P/U MAX	ADS7808PB/UB MIN	ADS7808PB/UB TYP	ADS7808PB/UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V, 0V to 5V, etc. (See Table I)					
Impedance			See Table I					
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			5.7	8		*	*	µs
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±0.9			±0.45	LSB[1]
Differential Linearity Error				±0.9			±0.45	LSB
No Missing Codes			Guaranteed			*		
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10			*	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2			±2		ppm/°C
Unipolar Zero Error[3]	Unipolar Ranges			±3			*	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			*		ppm/°C
Recovery to Rated Accuracy after Power Down	1µF Capacitor to CAP		1			*		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 45kHz	80	90		*	*		dB[5]
Total Harmonic Distortion	f_{IN} = 45kHz		–90	–80		*	*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 45kHz	70	73		72	*		dB
Signal-to-Noise	f_{IN} = 45kHz	70	73		72	*		dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808P/U MIN	ADS7808P/U TYP	ADS7808P/U MAX	ADS7808PB/UB MIN	ADS7808PB/UB TYP	ADS7808PB/UB MAX	UNITS
DIGITAL OUTPUTS								
Data Format			Serial 12 bits					
Data Coding			Binary Two's Complement or Straight Binary					
Pipeline Delay			Conversion results only available after completed conversion.					
Data Clock			Selectable for internal or external data clock					
Internal	EXT/$\overline{INT}$ LOW		2.3			*		MHz
(Output Only When Transmitting Data)								
External	EXT/$\overline{INT}$ HIGH	0.1		10	*		*	MHz
(Can Run Continually)								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation: PWRD LOW	V_{DIG} = V_{ANA} = 5V, f_S = 100kHz			100			*	mW
PWRD HIGH			50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°CW

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to (Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
CAP	V_{ANA}+0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7808P	20-Pin Plastic DIP	222
ADS7808PB	20-Pin Plastic DIP	222
ADS7808U	20-Pin SOIC	221
ADS7808UB	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

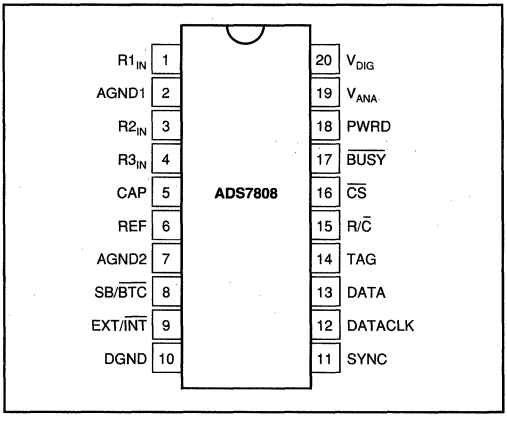
ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO(dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7808P	±0.9	70	–40°C to +85°C	20-Pin Plastic DIP
ADS7808PB	±0.45	72	–40°C to +85°C	20-Pin Plastic DIP
ADS7808U	±0.9	70	–40°C to +85°C	20-Pin SOIC
ADS7808UB	±0.45	72	–40°C to +85°C	20-Pin SOIC

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	$R1_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	$R2_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
4	$R3_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2µF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 12 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 12 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 12-bits of data, the ADS7808 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3.) If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 12 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3.
15	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{CS}$	Chip Select. Internally OR'ed with R/$\overline{C}$.
17	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V_{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
20	V_{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V_{ANA}.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.33	V_{IN}	V_{IN}	CAP	10.7kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		4500	ns
t_2	$\overline{BUSY}$ Delay			65	ns
t_3	$\overline{BUSY}$ LOW			8	µs
t_4	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		5.7	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	R/$\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK Period	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20		$t_{12} + 5$	ns
t_{16}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15		35	ns
t_{18}	Data Valid Delay	25		55	ns
t_{19}	$\overline{CS}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{CS}$ LOW	4.5			µs

TABLE II. Conversion and Data Timing T_A = –40°C to +85°C.

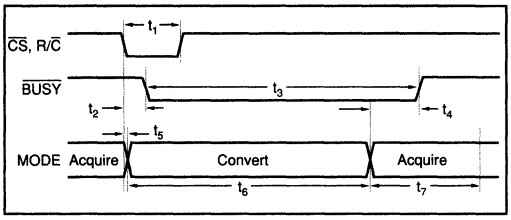


FIGURE 1. Basic Conversion Timing.

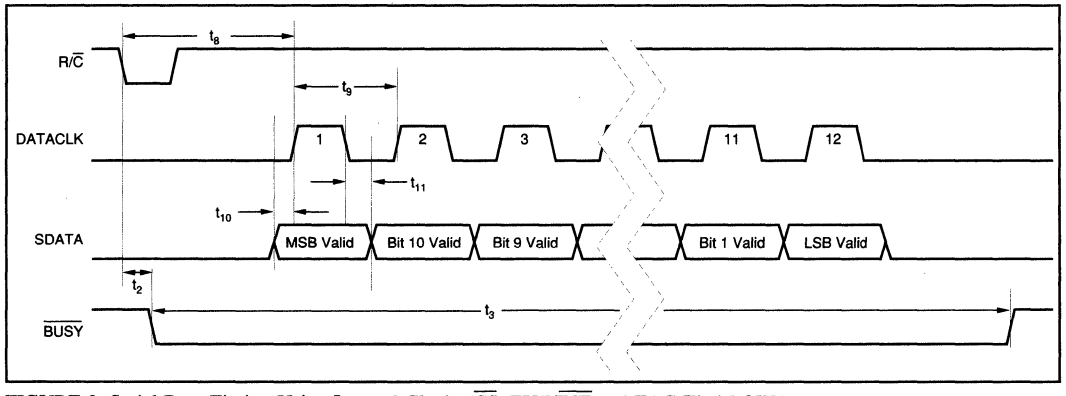


FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{CS}$, EXT/$\overline{INT}$ and TAG Tied LOW.)

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK.(1) Conversion "n" in process.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK .(1) Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

Table III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
							HEX BINARY CODE	CODE	HEX BINARY CODE	CODE
Full-Scale Range	±10	±5	±3.33V	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS – 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	–2.44mV	–1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table IV. Output Codes and Ideal Input Voltages.

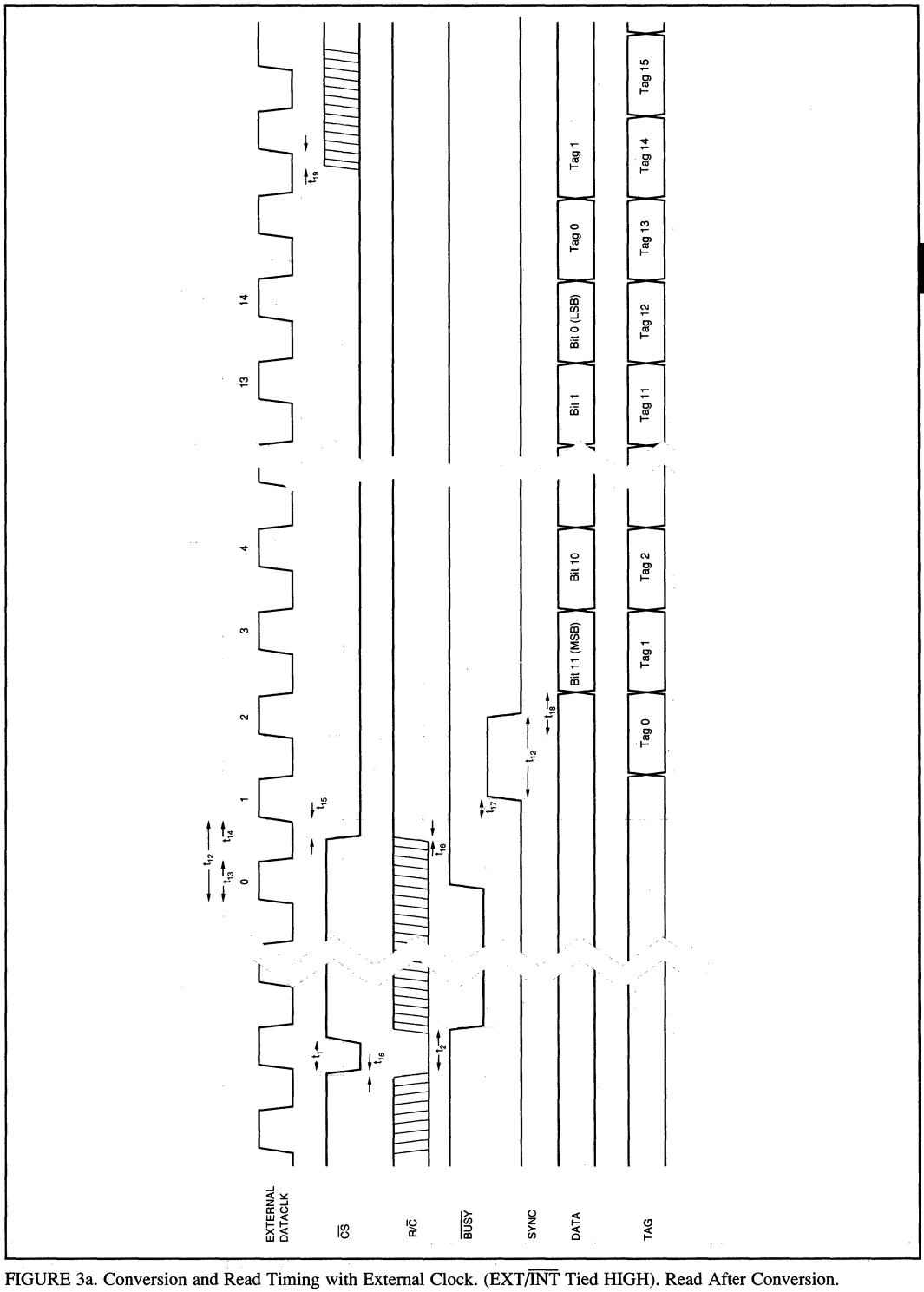


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied HIGH). Read After Conversion.

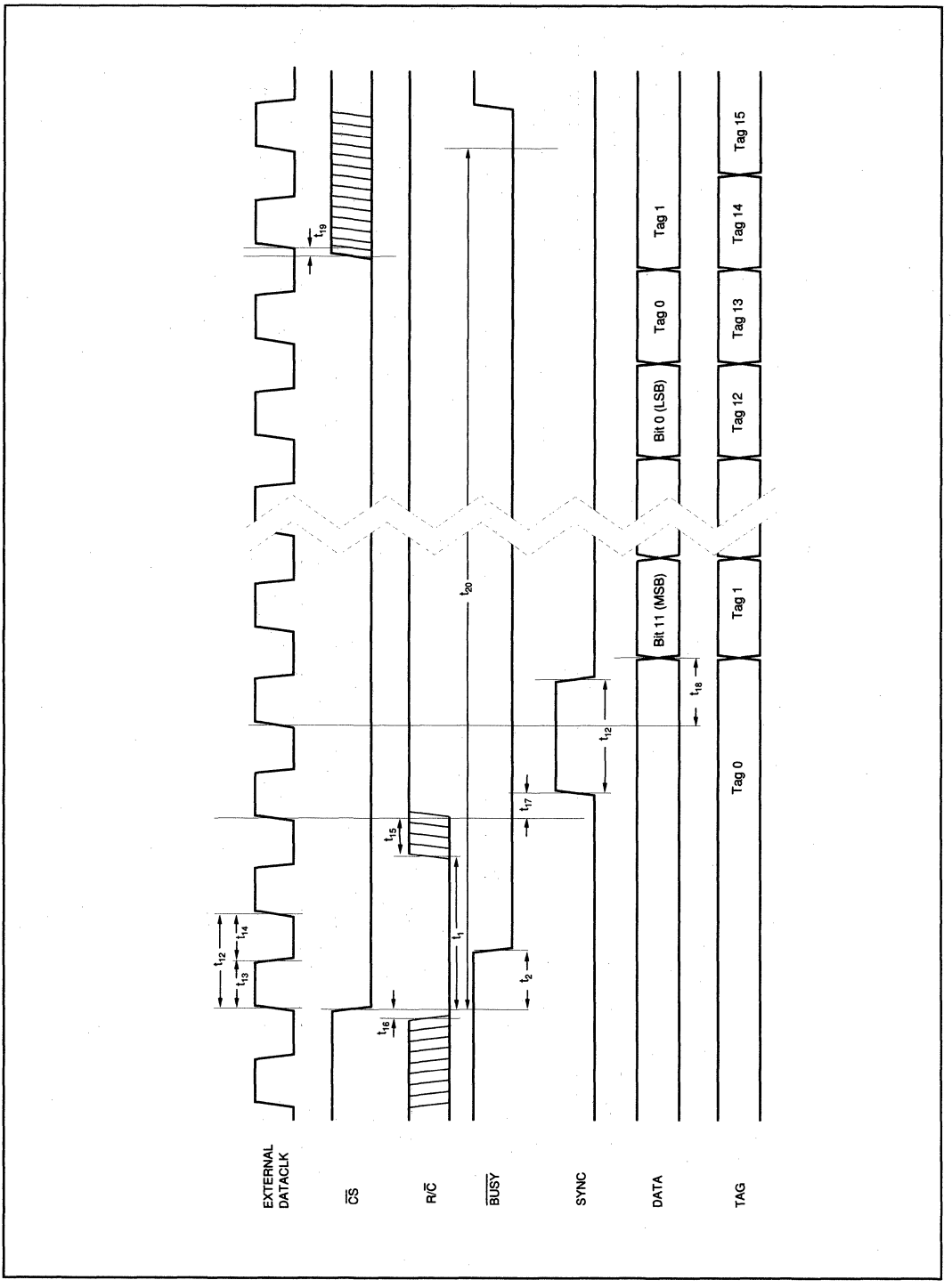


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied HIGH.) Read During Conversion (Previous Conversion Results).

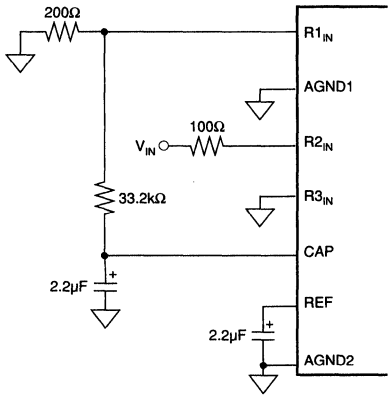
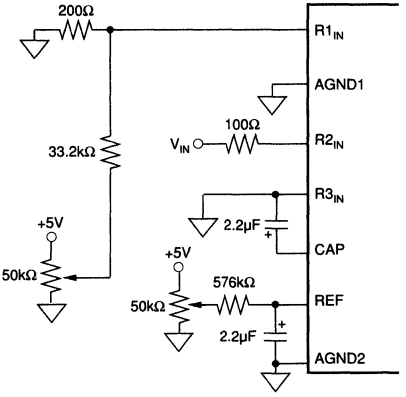
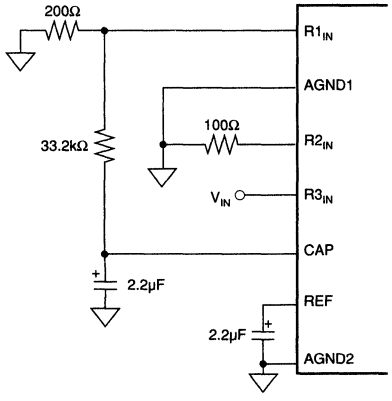
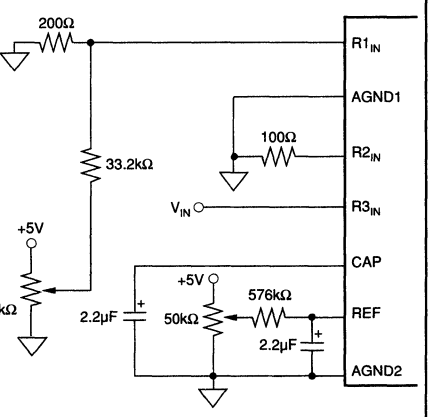
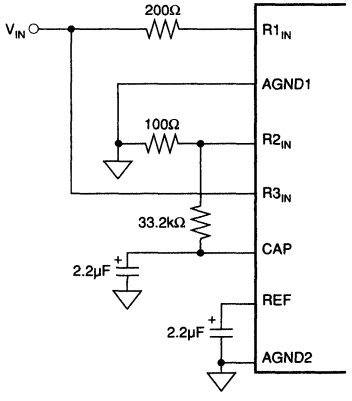
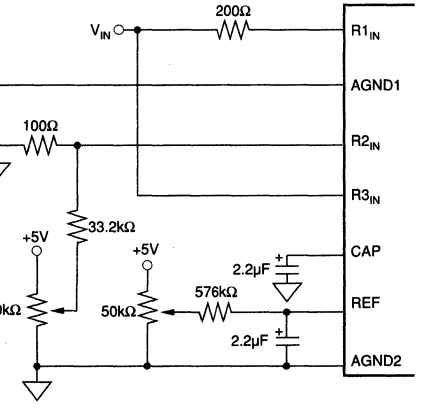
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

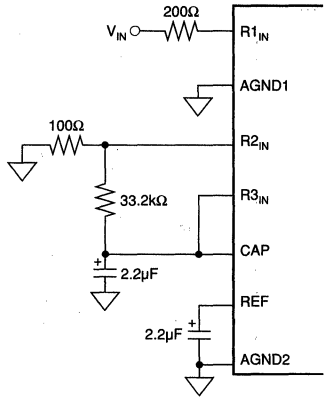
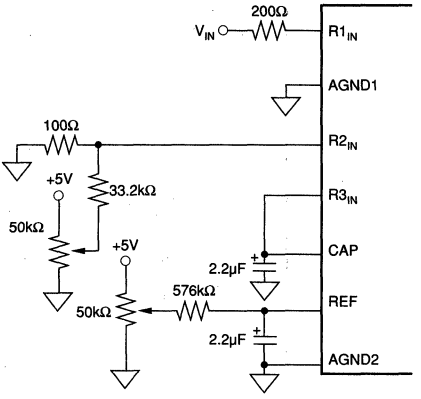
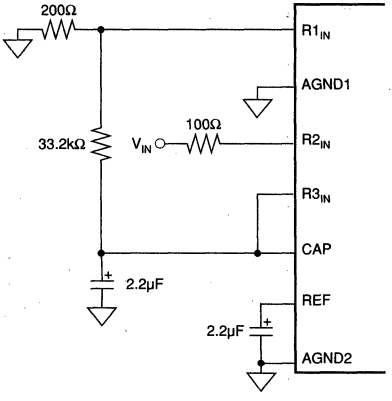
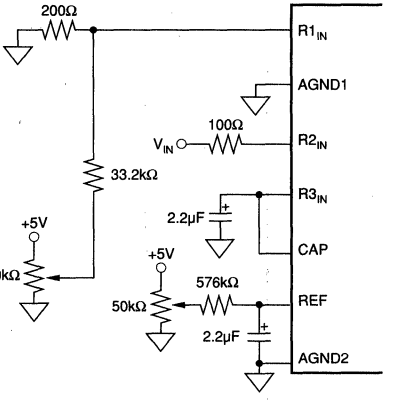
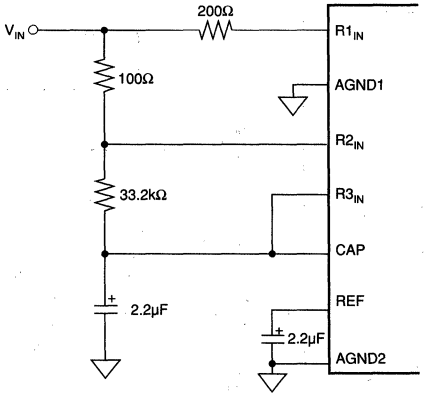
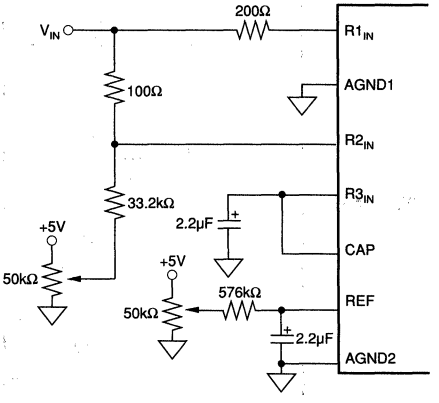
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

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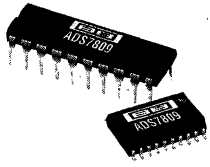


ADS7809

DEMO BOARD AVAILABLE
See Appendix A

16-Bit 10µs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

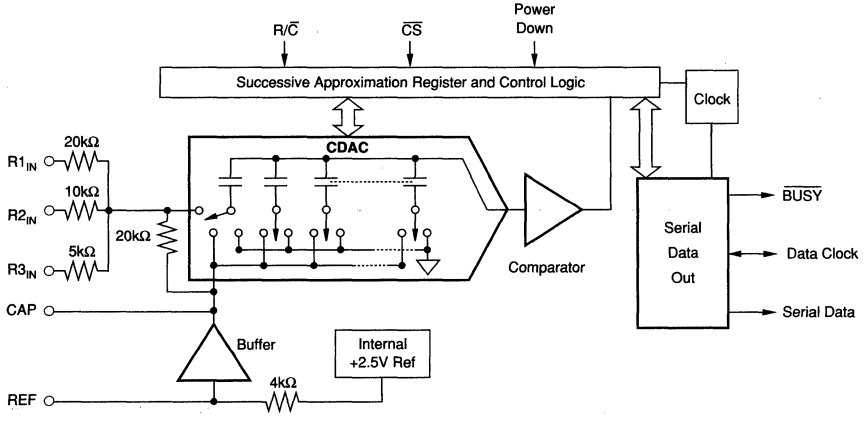
- 100kHz SAMPLING RATE
- 83dB SINAD WITH 20kHz INPUT
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7808
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

DESCRIPTION

The ADS7809 is a complete 16-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7809 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809P, U			UNITS
		MIN	TYP	MAX	
RESOLUTION				16	Bits
ANALOG INPUT					
Voltage Ranges			±10, 0V to 5V, etc. (See Table I)		
Impedance			See Table I		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Cycle	Acquire and Convert			10	µs
Throughput Rate		100			kHz
DC ACCURACY					
Integral Linearity Error				±3	LSB[1]
No Missing Codes		15			Bits
Transition Noise[2]			1.3		LSB
Full Scale Error[3,4]				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2		ppm/°C
Unipolar Zero Error[3]	0V tp 10V Ranges			±5	mV
Unipolar Zero Error[3]	0V to 4V, 0V to 5V Ranges			±3	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2		ppm/°C
Recovery to Rated Accuracy after Power Down	1µF Capacitor to CAP		1		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90	100		dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz		–100	–90	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20kHz	83	88		dB
	–60dB Input		30		dB
Signal-to-Noise	f_{IN} = 20kHz	83	88		dB
Full-Power Bandwidth[6]			250		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Transient Response	FS Step			2	µs
Overvoltage Recovery[7]			150		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer)			1		µA
External Reference Voltage Range For Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.0		V_D +0.3V	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809P, U MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS					
Data Format			Serial 16 bits		
Data Co			Binary Two's Complement or Straight Binary		
Pipeline Delay			Conversion results only available after completed conversion.		
Data Clock			Selectable for internal or external data clock		
Internal	EXT/$\overline{INT}$ LOW		2.3		MHz
(Output Only When Transmitting Data)					
External	EXT/$\overline{INT}$ HIGH	0.1		10	MHz
(Can Run Continually)					
V_{OL}	I_{SINK} = 1.6mA			+0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5	µA
Output Capacitance	High-Z State			15	pF
POWER SUPPLIES					
Specified Performance					
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
I_{DIG}			0.3		mA
I_{ANA}			16		mA
Power Dissipation: PWRD LOW	V_{ANA} = V_{DIG} = 5V, f_S = 100kHz			100	mW
PWRD HIGH			50		µW
TEMPERATURE RANGE					
Specified Performance		–25		+85	°C
Derated Performance		–55		+125	°C
Storage		–65		+150	°C
Thermal Resistance (θ_{JA})					
Plastic DIP			75		°C/W
SOIC			75		°C/W

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
CAP	V_{ANA}+0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, *Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7809P	20-Pin Plastic DIP	222
ADS7809U	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

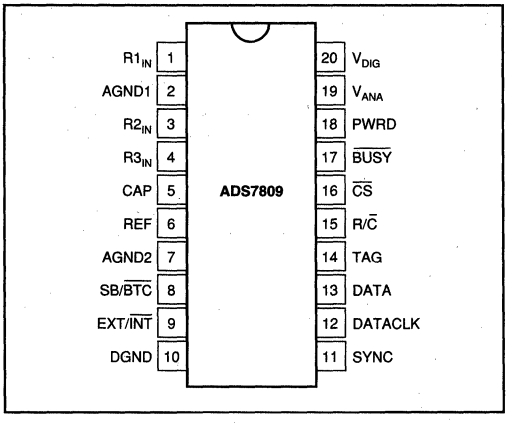
ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	GUARANTEED NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ADS7809P	±4	15	83	–25°C to +85°C	20-Pin Plastic DIP
ADS7809U	±4	15	83	–25°C to +85°C	20-Pin SOIC

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	$R1_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	$R2_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
4	$R3_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2µF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16 bits of data, the ADS7809 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3.) If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3.
15	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{CS}$	Chip Select. Internally OR'ed with R/$\overline{C}$.
17	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V_{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
20	V_{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V_{ANA}.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.33V	V_{IN}	V_{IN}	CAP	10.7kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		6000	ns
t_2	$\overline{BUSY}$ Delay			65	ns
t_3	$\overline{BUSY}$ LOW			8	µs
t_4	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		7.6	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	R/$\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20		t_{12} +5	ns
t_{16}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15		35	ns
t_{18}	Data Valid Delay	25		55	ns
t_{19}	$\overline{CS}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{CS}$ LOW	6			µs

TABLE II. Conversion and Data Timing. T_A = –25°C to +85°C.

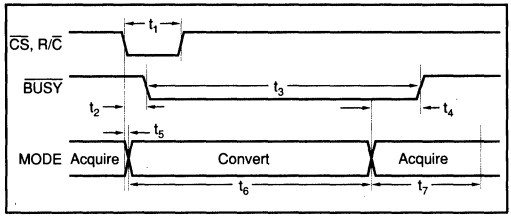


FIGURE 1. Basic Conversion Timing.

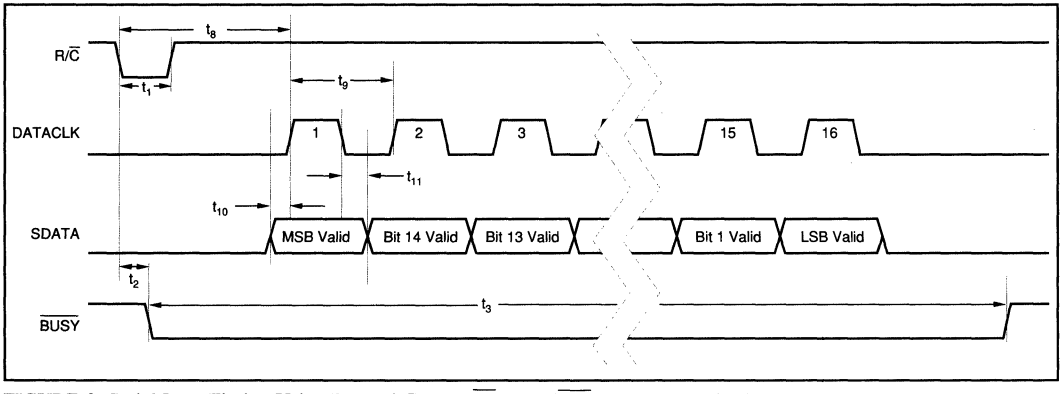


FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{CS}$, EXT/$\overline{INT}$ and TAG Tied LOW.)

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 16 clock pulses ouput on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n–1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK.(1) Conversion "n" in process.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n–1" clocked out synchronized to external DATACLK .(1) Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

TABLE III. Control Truth Table.

							DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
DESCRIPTION	ANALOG INPUT						BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305µV	153µV	102µV	153µV	76µV	61µV				
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

TABLE IV. Output Codes and Ideal Input Voltages.

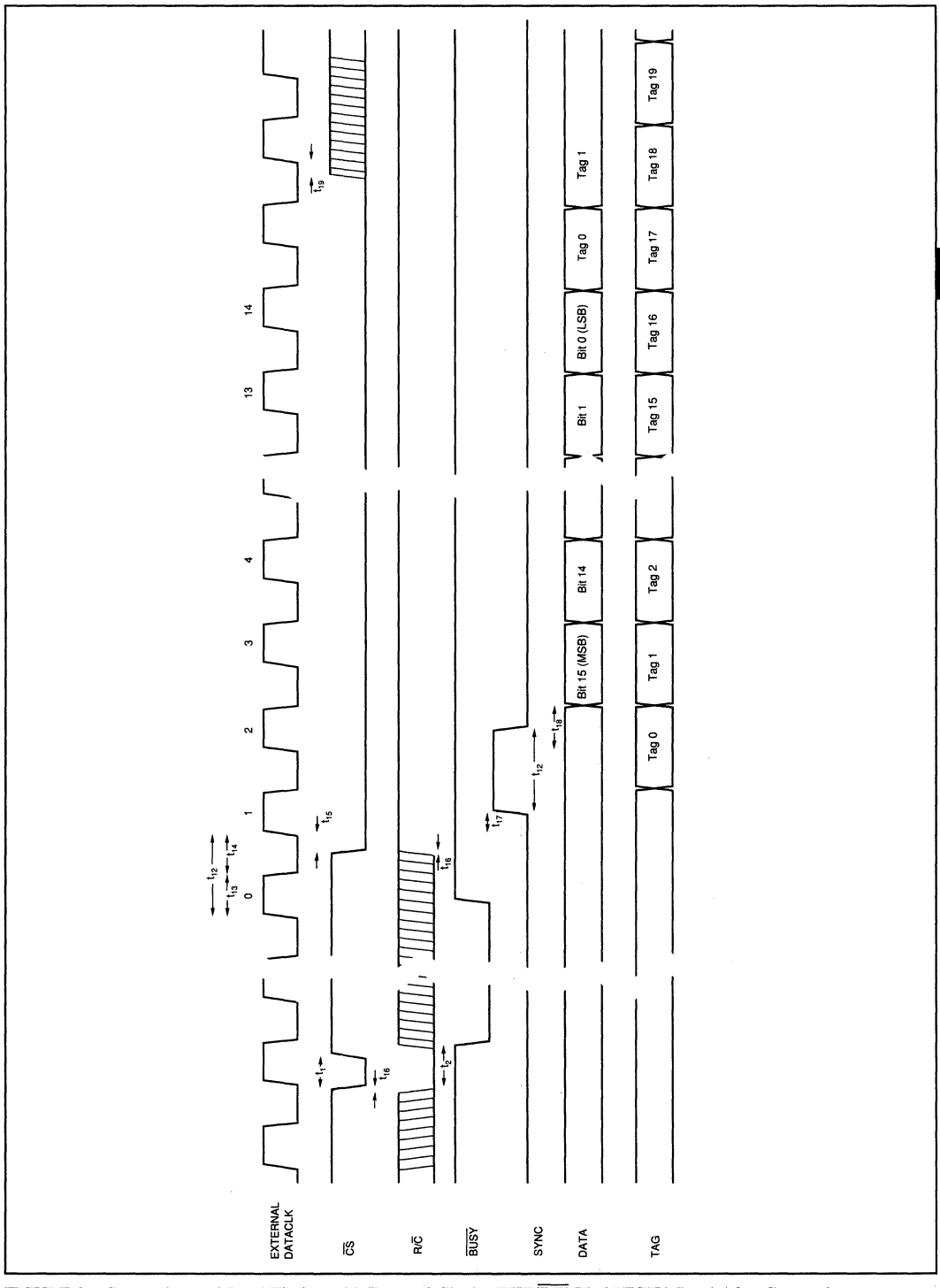


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied HIGH.) Read After Conversion.

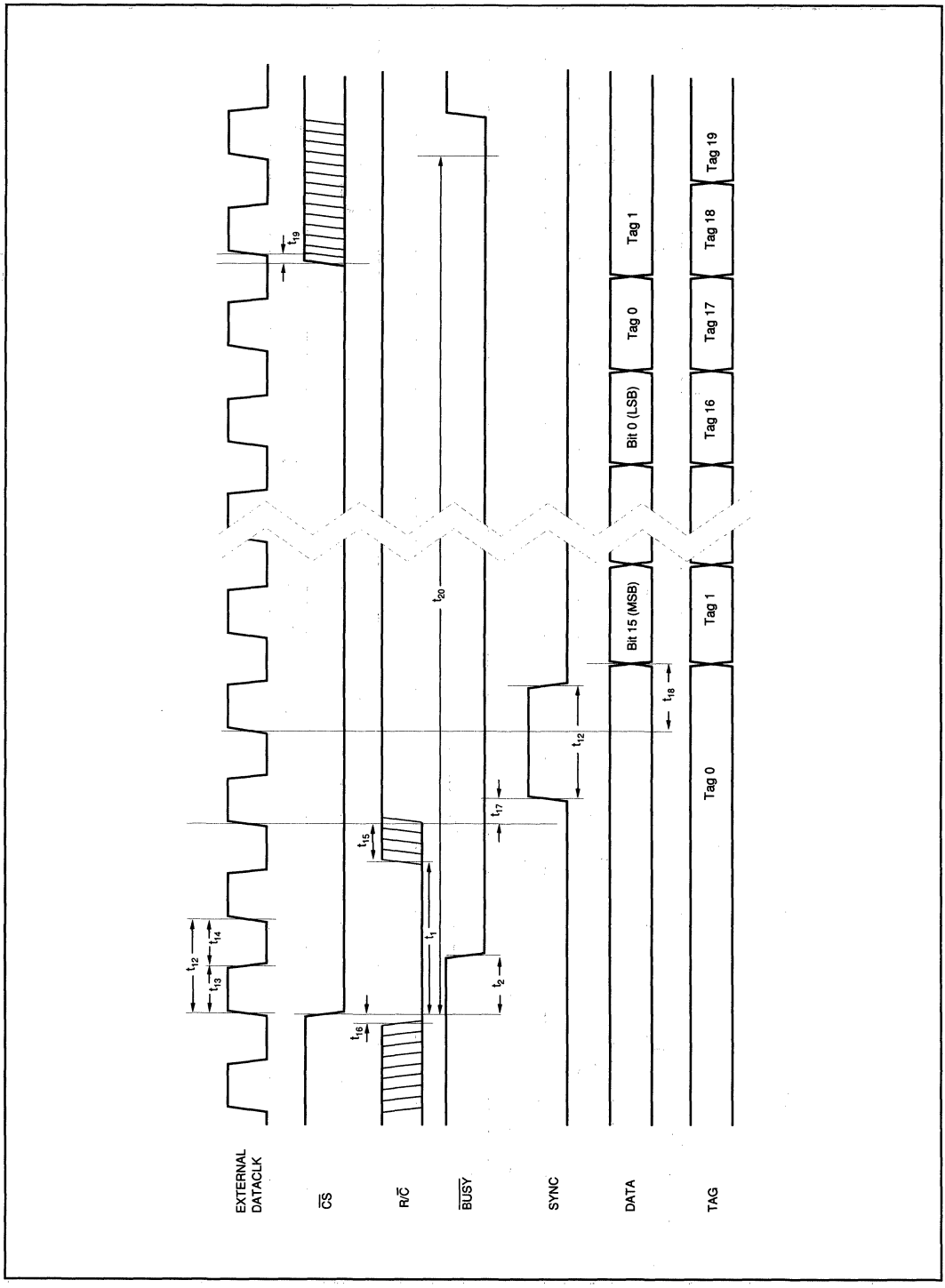


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied HIGH.) Read During Conversion (Previous Conversion Results).

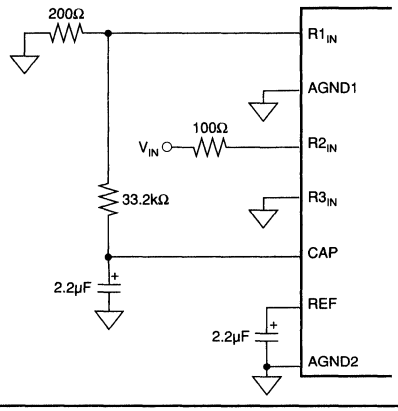
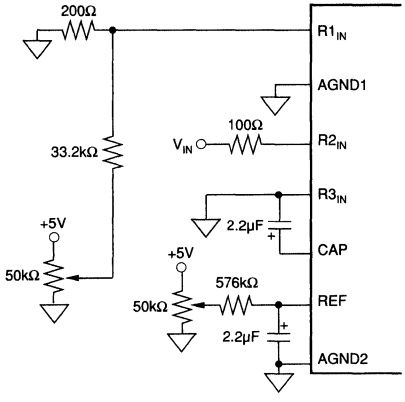
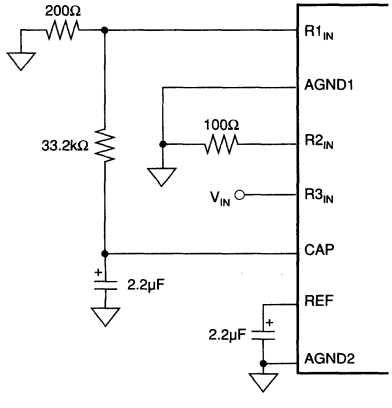
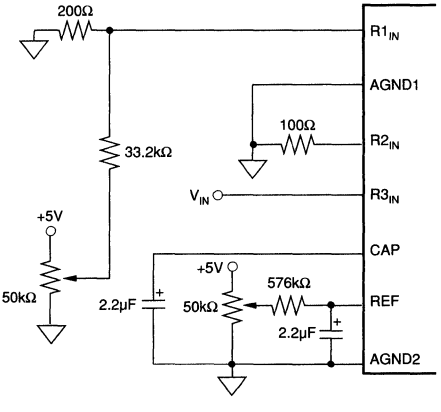
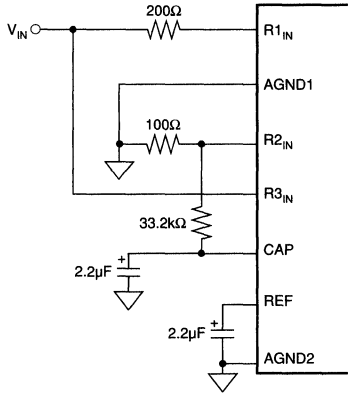
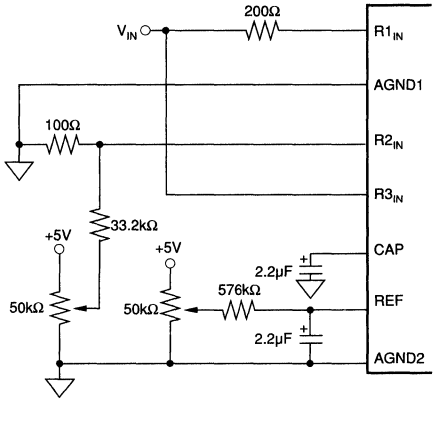
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

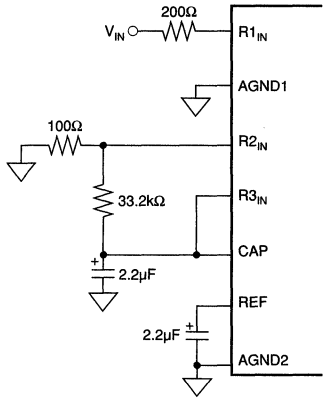
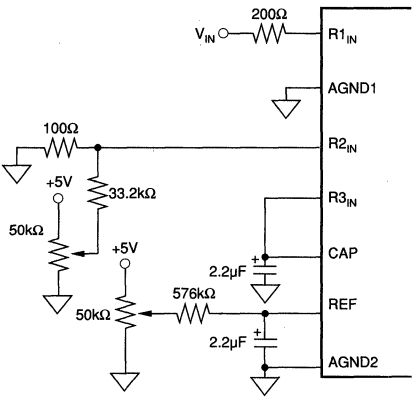
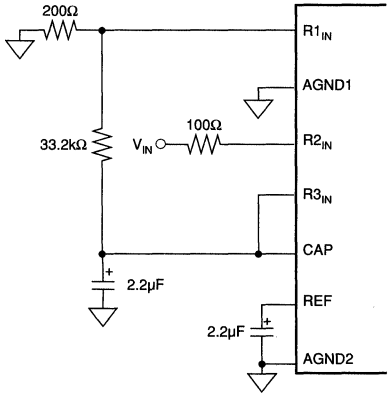
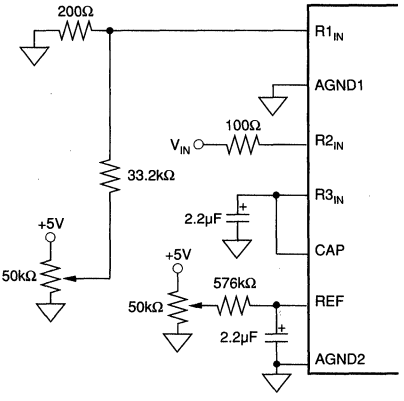
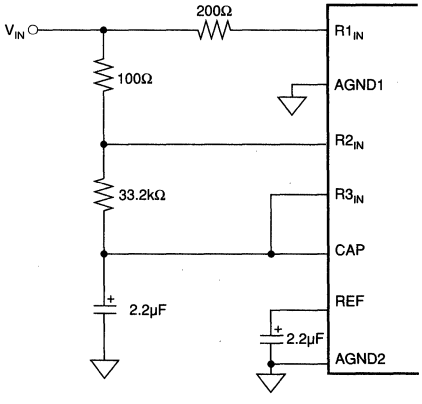
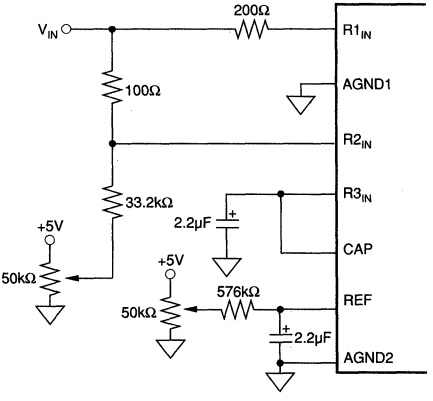
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

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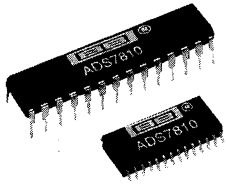


ADS7810

DEMO BOARD AVAILABLE
See Appendix A

12-Bit 800kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

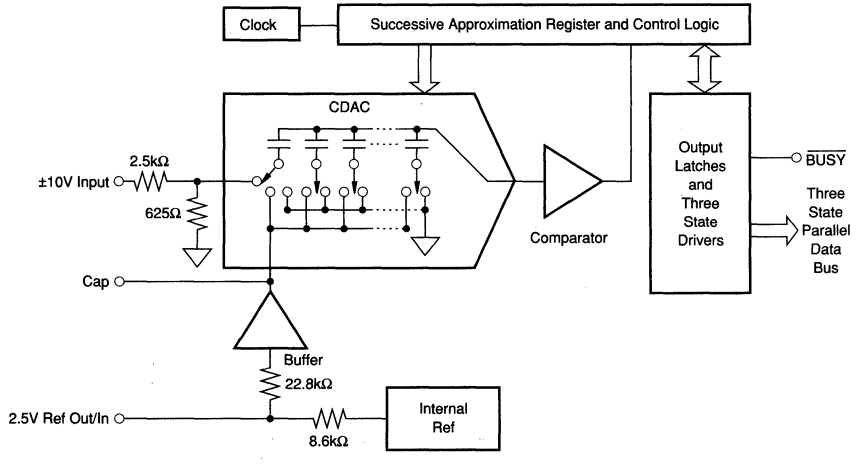
- 1.25µs THROUGHPUT TIME
- STANDARD ±10V INPUT RANGE
- 69dB min SINAD WITH 250kHz INPUT
- ±3/4 LSB max INL AND ±1 LSB max DNL
- INTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/LATCHES
- 250mW max POWER DISSIPATION
- 28-PIN 0.3" PDIP AND SOIC

DESCRIPTION

The ADS7810 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7810 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide the industry-standard ±10V input range, while an innovative design allows operation from ±5V supplies, with power dissipation under 250mW.

The 28-pin ADS7810 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C, to +85°C, f_S = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7810P, U			ADS7810PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±10			*		V
Impedance			3.1			*		kΩ
Capacitance			5			*		pF
THROUGHPUT SPEED								
Conversion Time			985			*		ns
Complete Cycle	Acquire & Convert			1240			*	ns
Throughput Rate		800			*			kHz
DC ACCURACY								
Integral Linearity Error				±1			±0.75	LSB[1]
Differential Linearity Error				±1			±1	LSB
No Missing Codes			Guaranteed			*		
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3, 4]				±0.5			±0.25	%
Full Scale Error Drift			±5			±3		ppm/°C
Full Scale Error[3, 4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±8			±4	LSB
Bipolar Zero Error Drift			±1			±0.5		ppm/°C
Power Supply Sensitivity								
$(+V_{DIG} = +V_{ANA} = V_D)$	+4.75V < V_D < +5.25V			±5			*	LSB
	–5.25V < $-V_{ANA}$ < –4.75V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 250kHz	74			77			dB[5]
Total Harmonic Distortion	f_{IN} = 250kHz			–74			–77	dB
Signal-to-(Noise+Distortion)	f_{IN} = 250kHz	67			69			dB
Signal-to-Noise	f_{IN} = 250kHz	68			70			dB
Full-Power Bandwidth[6]			1.5			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			20			*		ns
Aperture Jitter			Sufficient to Meet AC Specs			*		
Transient Response	FS Step		100			*		ns
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			100			*		nA
Internal Reference Drift			8					ppm/°C
External Reference Voltage Range For Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		V_D + 0.3	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 12-bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+2.8			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C, to +85°C, f_S = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7810P, U			ADS7810PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
$+V_{DIG} = +V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$-V_{ANA}$		–5.25	–5	–4.75	*	*	*	V
$+I_{DIG}$			+16			*		mA
$+I_{ANA}$			+16			*		mA
$-I_{ANA}$			–13			*		mA
Derated Performance								
$+V_{DIG} = +V_{ANA}$		+4.5	+5	+5.5	*	*	*	V
$-V_{ANA}$		–5.5	–5	–4.5	*	*	*	V
Power Dissipation	f_S = 800kHz			250			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125				°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7810, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	±25V
CAP	$+V_{ANA}$ +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2
	Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
$+V_{ANA}$	+7V
$+V_{DIG}$ to $+V_{ANA}$	+0.3V
$+V_{DIG}$	7V
$-V_{ANA}$	–7V
Digital Inputs	–0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

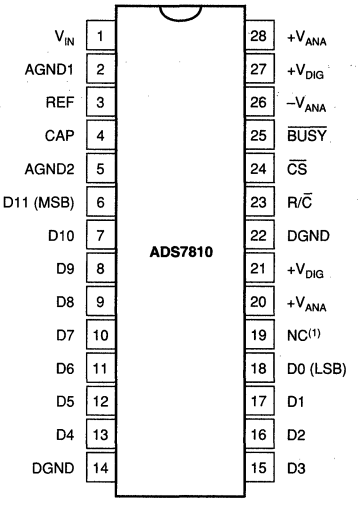
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7810P	28-Pin Plastic DIP	246
ADS7810PB	28-Pin Plastic DIP	246
ADS7810U	28-Pin SOIC	217
ADS7810UB	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7810P	±1	67	–40°C to +85°C	Plastic DIP
ADS7810PB	±0.75	69	–40°C to +85°C	Plastic DIP
ADS7810U	±1	67	–40°C to +85°C	SOIC
ADS7810UB	±0.75	69	–40°C to +85°C	SOIC

PIN CONFIGURATION



NOTE: (1) Not Internally Connected.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	Data Valid Delay After R/$\overline{C}$ LOW		1030	1150	ns
t_3	$\overline{BUSY}$ Delay From R/$\overline{C}$ LOW		85	125	ns
t_4	$\overline{BUSY}$ LOW		1000	1115	ns
t_5	$\overline{BUSY}$ Delay After End of Conversion		80		ns
t_6	Aperture Delay		20		ns
t_7	Conversion Time		985	1090	ns
t_8	Acquisition Time		100	150	ns
t_7 & t_8	Throughput Time		1085	1240	ns
t_9	Bus Relinquish Time	20	50	83	ns
t_{10}	$\overline{BUSY}$ Delay After Data Valid	20	55	90	ns
t_{11}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	5			ns
t_{12}	Time Between Conversions	1250			ns
t_{13}	Bus Access Time	10	35	83	ns

TABLE I. Timing Specifications (T_{MIN} to T_{MAX}).

PIN ASSIGNMENTS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±10V.
2	AGND1		Analog Ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum to ground.
5	AGND2		Analog Ground.
6	D11 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
7	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
8	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
9	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
10	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
11	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
12	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
13	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
14	DGND		Digital Ground.
15	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
16	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
17	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
18	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
19			Not internally connected.
20	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28, and decouple to ground with 0.1µF ceramic and 10µF tantulum capacitors.
21	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28.
22	DGND		Digital ground.
23	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits.
24	$\overline{CS}$	I	Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits.
25	$\overline{BUSY}$	O	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to read the data.
26	$-V_{ANA}$		Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantulum capacitors.
27	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28.
28	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27.

BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7810 with a full parallel data output. Taking R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus enabled when conversion is completed.
0	↑	0	Conversion in progress. Databus enabled when conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register, but outputs are still tri-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table II. Control Line Functions for 'read' and 'convert'.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7810 in the hold state and starts a conversion. BUSY (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 3 for timing diagrams.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	4.88mV		
+Full Scale (10V – 1LSB)	9.995V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–4.88mV	1111 1111 1111	FFF
–Full Scale	–10V	1000 0000 0000	800

TABLE III. Ideal Input Voltages and Output Codes.

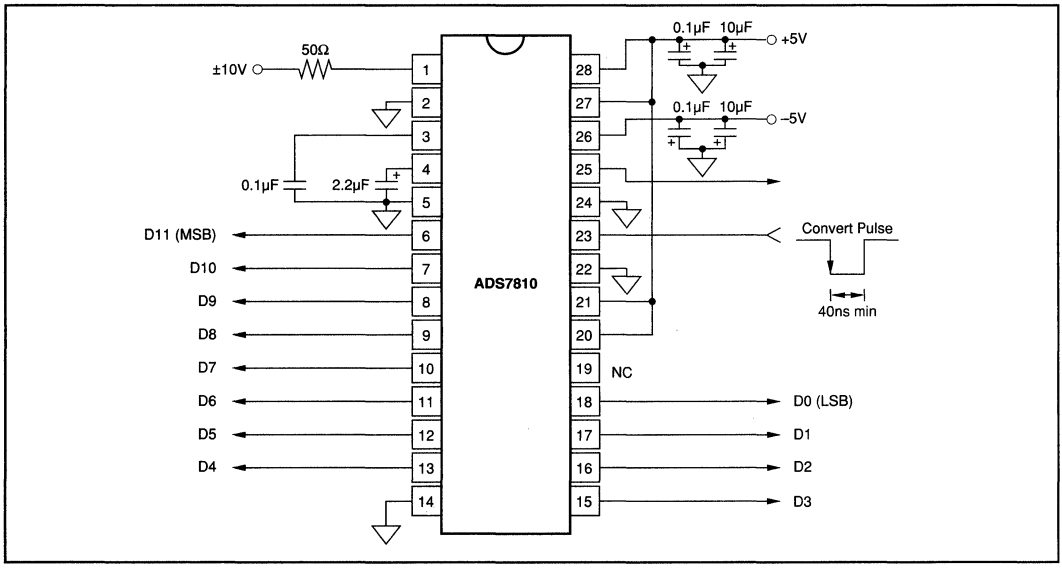


FIGURE 1. Basic Operation

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 5ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the Reading Data section and refer to Table II for control line functions for 'read' and 'convert' modes.

READING DATA

The ADS7810 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on pins 6-13 and pins 15-18. Refer to Table III for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table I and Figures 2 and 3.

Note! For the best possible performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

INPUT RANGES

The ADS7810 offers a standard ±10V input range. Figure 4 shows the necessary circuit connections for the ADS7810 with and without external trim. Offset and full scale error(1) specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4. This external resistor makes it possible to trim the offset ±50mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain are negligible or they will be trimmed in software. See the Calibration section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and external 50Ω resistor. The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor used for the external offset adjustment circuitry does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

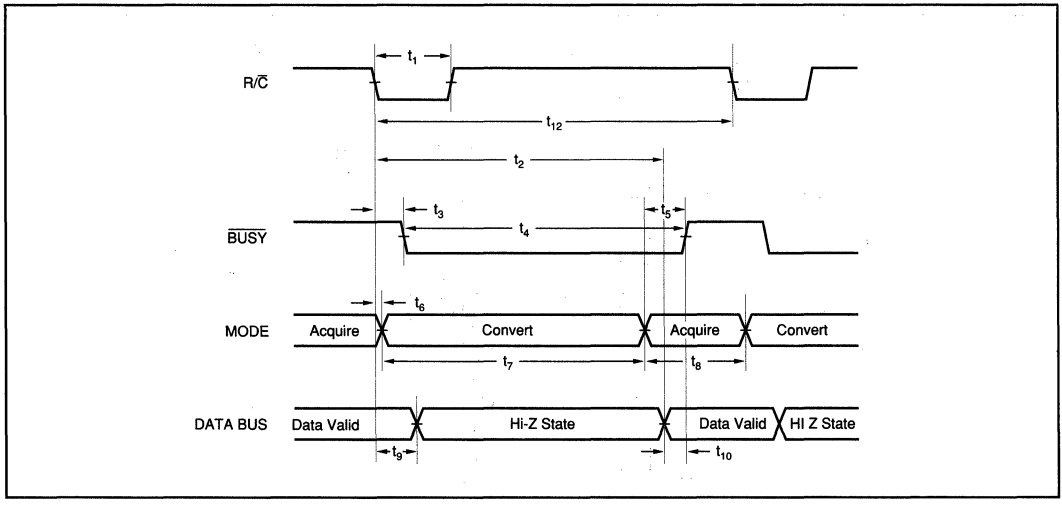


FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

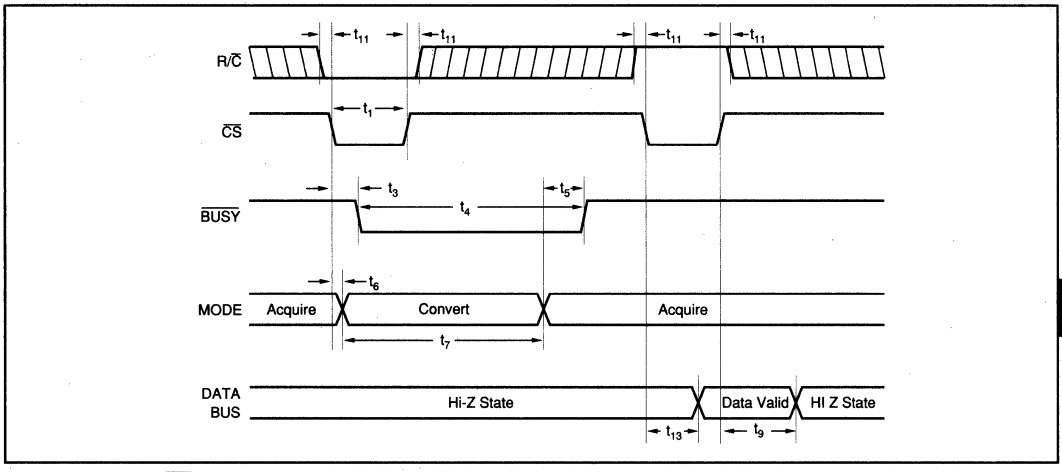


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

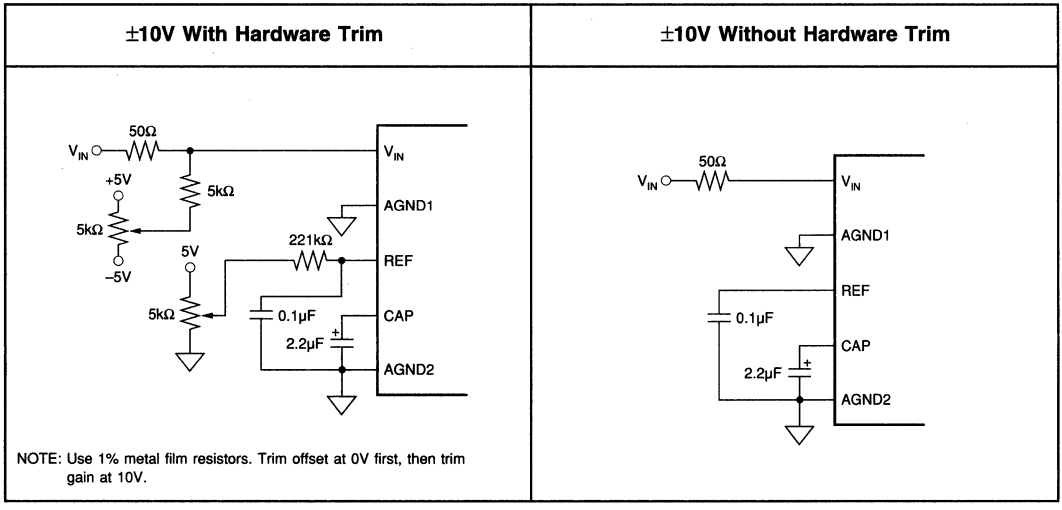


FIGURE 4. Circuit Diagram With and Without External Resistors.

CALIBRATION

The ADS7810 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

Hardware Calibration

To calibrate the offset and gain of the ADS7810, install the proper resistors and potentiometers as shown in Figure 4. The calibration range is ±50mV for the offset and ±135mV for the gain.

Software Calibration

To calibrate the offset and gain of the ADS7810, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistor. Refer to Table IV for range of gain errors with and without the external 50Ω resistor.

No Calibration

See Figure 4 for circuit connections. The 50Ω external resistor shown in Figure 4 may not be necessary in some applications. This resistor provides trim capability for the gain of the ADS7810. The nominal transfer function of the ADS7810 will be bound by the shaded region seen in Figure 5 with a typical offset of 0mV and a typical gain error of –1.6%. Refer to Table IV for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BPO	–40 < BPO < 40 –8 < BPO < 8	–40 < BPO < 40 –8 < BPO < 8	mV LSBs
Gain Error	–0.5 < error < 0.5	–2.5 < error < –1	% of FSR

TABLE IV. Offset and Gain Errors With and Without External Resistors.

REFERENCE

The ADS7810 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output of the buffer accessible on CAP (pin 4).

The internal reference has a 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 0.1µF capacitor should be connected as close to the REF pin as possible. The capacitor

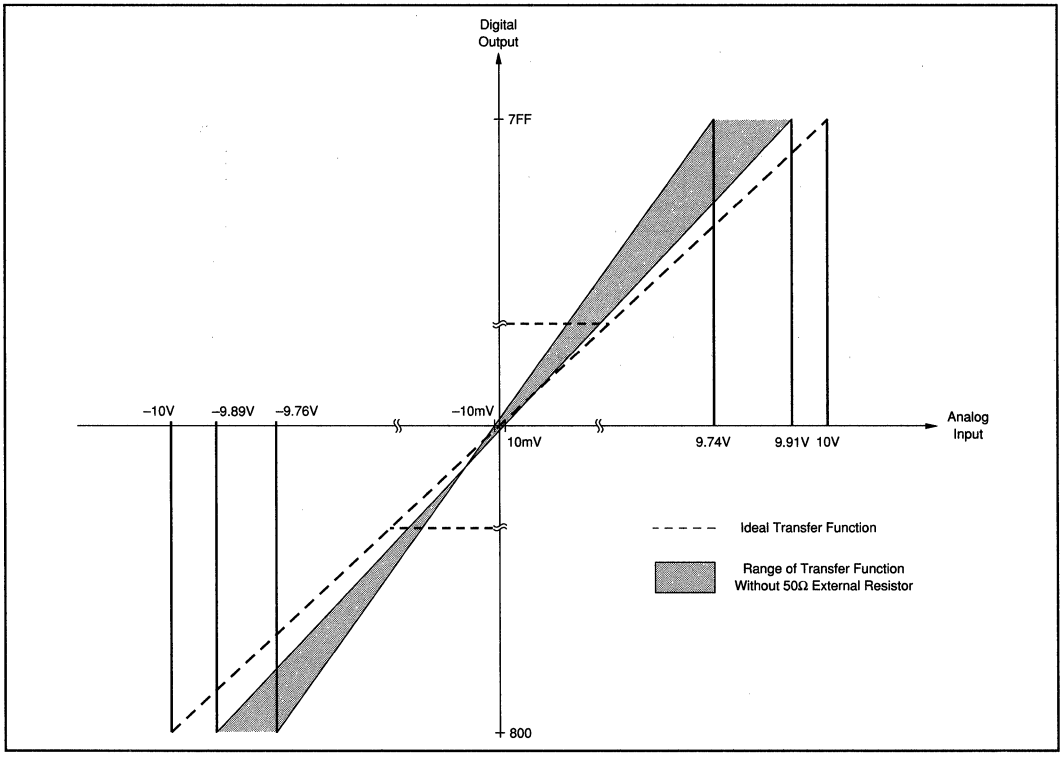


FIGURE 5. Bipolar Transfer Function Without External Resistors.

and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. The ADS7810 uses the majority of its power for analog and static circuitry. The ADS7810 should be considered as an analog component.

The +5V power for the ADS should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 21 and 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, simple +5V and –5V regulators can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, the V_{DIG} and V_{ANA} pins should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7810. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7810, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7810.

The resistive front end of the ADS7810 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7810 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7810 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

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ADS7811

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

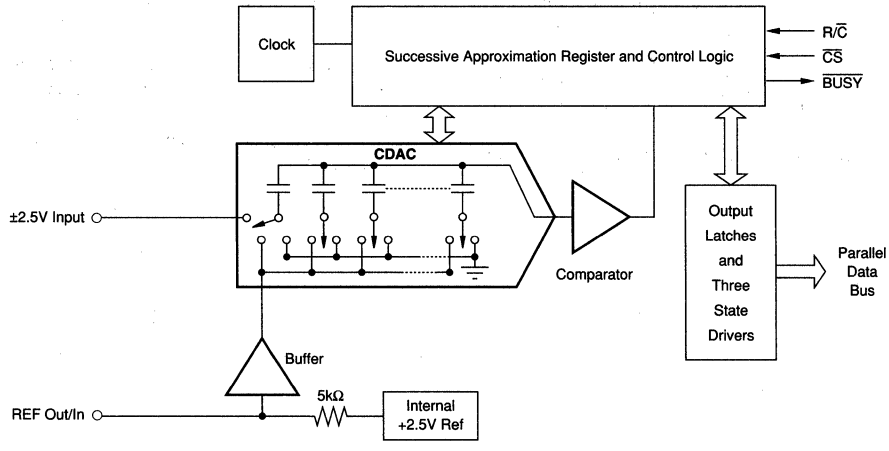
16-Bit 250kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- **250kHz SAMPLING RATE**
- **±2.5V INPUT RANGE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **FULL PARALLEL DATA OUTPUT WITH LATCHES**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**
- **86dB min SINAD WITH 100kHz INPUT**
- **INL: ±1.5 LSB max**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **DNL: 16 Bits "No Missing Codes"**

DESCRIPTION

The ADS7811 is a complete 16-bit sampling analog-to-digital converter using state-of-the art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers. The 28-pin ADS7811 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range. The ADS7811 is specified at a 250kHz sampling rate, and guaranteed over the full temperature range. A ±2.5V input range allows development of precision systems using only ±5V supplies.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = –25°C to +85°C, f_S = 250kHz, V_{DIG} = +V_{ANA} = +5V ±5%, and –V_{ANA} = –5V ±5%, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7811P, U			ADS7811PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Range			±2.5V			*		V
Impedance			100			*		MΩ
Capacitance			50			*		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			4.0			*	µs
Throughput Rate		250			*			kHz
DC ACCURACY								
Integral Linearity Error			±3			±1.5	±3	LSB[1]
No Missing Codes		14			15			Bits
Transition Noise[2]			1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity								
(V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V,		±4			*		LSB
	–5.25V < –V_{ANA} < –4.75V		±4			*		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 100kHz	90			96			dB[5]
Total Harmonic Distortion	f_{IN} = 100kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 100kHz	84			86			dB
	–60dB Input		28			30		dB
Signal-to-Noise	f_{IN} = 100kHz	84			86			dB
Full Power Bandwidth[6]			1			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step		600			*		ns
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.8		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 16 bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 200µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				65			*	ns
Bus Relinquish Time				65			*	ns

SPECIFICATIONS (CONT)

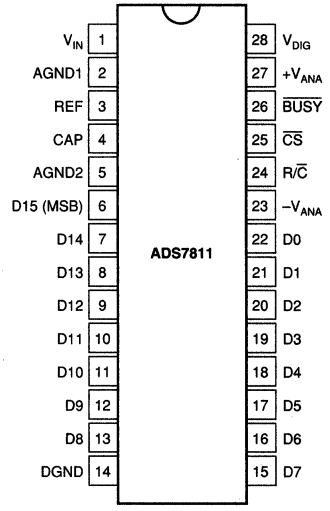
At T_A = –25°C to +85°C, f_S = 250kHz, V_{DIG} = $+V_{ANA}$ = +5V ±5%, and $-V_{ANA}$ = –5V ±5%, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7811P, U			ADS7811PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}		+4.75	+5	+5.25	*	*	*	V
$+V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$-V_{ANA}$		–5.25	–5	–4.75	*	*	*	V
Power Dissipation	f_S = 250kHz		160	250			*	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	*		*	°C
Storage		–55		+125	*		*	°C

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±2.5V input ADS7811, one LSB is 76µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±2.5V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

PIN CONFIGURATION

Top View **DIP/SOIC**



PIN #	NAME	DESCRIPTION
1	V_{IN}	Analog Input. Full-scale input range is ±2.5V.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	REF	Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 0.1µF ceramic capacitor.
4	CAP	Reference compensation capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2	Analog ground.
6	D15 (MSB)	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND	Digital Ground.
15	D7	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	$-V_{ANA}$	Analog negative supply input. Nominally –5V. Decouple to analog ground with 0.1µF ceramic and 10µF tantalum capacitors.
24	R/$\overline{C}$	Read/convert input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits.
25	$\overline{CS}$	Chip select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits.
26	$\overline{BUSY}$	Busy output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition.
27	$+V_{ANA}$	Analog positive supply input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}	Digital supply input. Nominally +5V. Connect directly to pin 27. Decouple to digital ground with 0.1µF ceramic and 10µF tantalum capacitors.

TABLE I. Pin Assignments.

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ADS7814

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

14-Bit 300kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

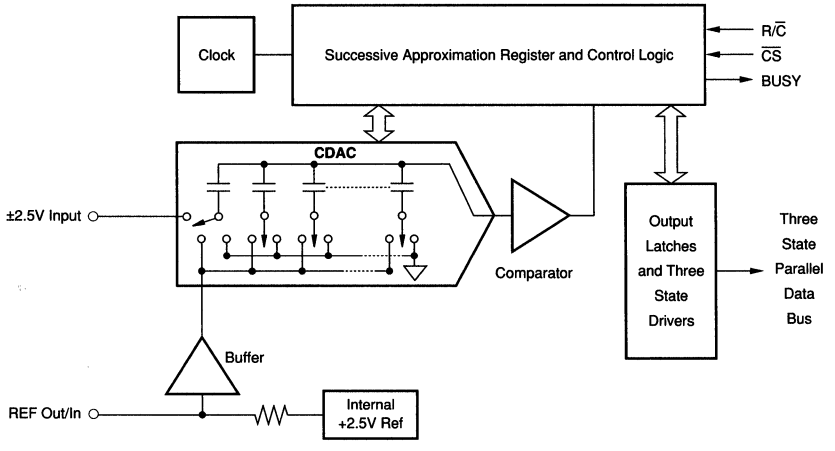
FEATURES

- **300kHz SAMPLING RATE**
- **±2.5V INPUT RANGE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **FULL PARALLEL DATA OUTPUT WITH LATCHES**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**
- **82dB min SINAD WITH 100kHz INPUT**
- **INL: ±2.0LSB max**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **DNL: 14 Bits "No Missing Codes"**

DESCRIPTION

The ADS7814 is a monolithic CMOS 14-bit analog-to-digital converter using state-of-the-art CMOS structures. It contains a 14-bit, capacitor-based, SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7814 is available in a 28-pin plastic DIP and SOIC, both fully specified for operation over the industrial –40°C to +85°C temperature range. The ADS7814 is specified at a 300kHz sampling rate, and guaranteed over the full temperature range. A ±2.5V input range allows development of precision systems using only ±5V supplies.



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SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 300kHz, V_{DIG} = $+V_{ANA}$ = +5V, ±5%, $-V_{ANA}$ = –5V, ±5%, using internal reference, unless otherwise specified.

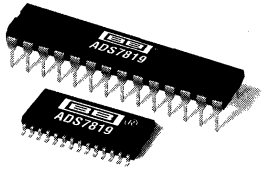
PARAMETER	CONDITIONS	ADS7814P, U			ADS7814PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				14			*	Bits
ANALOG INPUT								
Voltage Range			±2.5			*		V
Impedance			100			*		MΩ
Capacitance			50			*		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			3.33			*	µs
Throughput Rate		300			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±2	LSB[1]
No Missing Codes		13			14			Bits
Transition Noise[2]			0.2			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity								
(V_{DIG} = V_{ANA} = V_S)	+4.75V < V_D < +5.25V		±4			*		LSB
	+5.25V < V_{ANA} < –4.75V		±4			*		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 100kHz	88			90			dB[5]
Total Harmonic Distortion	f_{IN} = 100kHz			–88			–90	dB
Signal-to-(Noise+Distortion)	f_{IN} = 100kHz	80			82			dB
	–60dB Input		22			24		dB
Signal-to-Noise	f_{IN} = 100kHz	80			82			dB
Full Power Bandwidth[6]			1			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step		600			*		ns
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			1			*		µA
(Must use external buffer)								
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.8		V_D +0.3	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 14 bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 200µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				65			*	ns
Bus Relinquish Time				65			*	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}		+4.75	+5	+5.25	*	*	*	V
$+V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$-V_{ANA}$		–5.25	–5	–4.75	*	*		V
Power Dissipation	f_S = 300kHz		160	250			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C

NOTES: (1) LSB means Least Significant Bit. For the 14-bit, ±2.5V input ADS7814, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±2.5V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

PIN #	NAME	DESCRIPTION
1	V_{IN}	Analog Input. Full-scale input range is ±2.5V.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	REF	Reference Input/Output. Outputs internal reference of +2.5V nominal. Must be buffered externally to maintain ADS7811 accuracy. Can also be driven by external system reference. In both cases, connect to ground with a 0.1µF ceramic capacitor.
4	CAP	Reference Compensation Capacitor. 2.2µF tantalum to ground.
5	AGND2	Analog Ground.
6	DNC	Do Not Connect. Make no connection to this pin.
7	DNC	Do Not Connect. Make no connection to this pin.
8	D13 (MSB)	Data Bit 13. Most significant bit (MSB of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND	Digital Ground.
15	D7	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	Data Bit 0. Least significant bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	$-V_{ANA}$	Analog negative supply input. Nominally –5V. Decouple to analog ground with 0.1µF ceramic and 10µF tantalum capacitors.
24	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ inputs the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits.
25	$\overline{CS}$	Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits.
26	$\overline{BUSY}$	Busy output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises or another conversion will start, without time for signal acquisition.
27	$+V_{ANA}$	Analog Positive Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 27. Decouple to digital ground with 0.1µF ceramic and 10µF tantalum capacitors.

TABLE I. Pin Assignments.

BURR-BROWN®



ADS7819

12-Bit 800kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

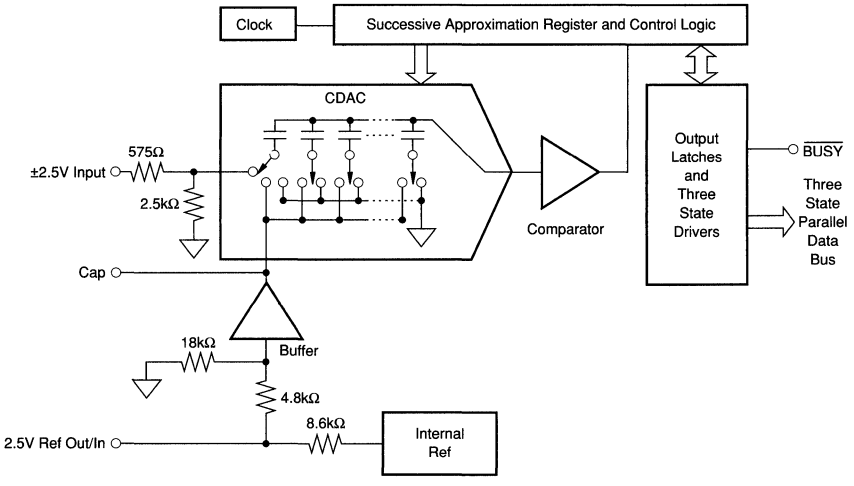
- 1.25µs THROUGHPUT TIME
- STANDARD ±2.5V INPUT RANGE
- 70dB min SINAD WITH 250kHz INPUT
- ±3/4 LSB max INL AND ±1 LSB max DNL
- INTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/ LATCHES
- 28-PIN 0.3" PDIP AND SOIC

DESCRIPTION

The ADS7819 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7819 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a ±2.5V input range and inherent overvoltage protection up to ±25V.

The 28-pin ADS7819 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = –40°C to +85°C, f_S = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7819P, U			ADS7819PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±2.5			*		V
Impedance			3.1			*		kΩ
Capacitance			5			*		pF
THROUGHPUT SPEED								
Conversion Time			940			*		ns
Complete Cycle	Acquire & Convert			1250			*	ns
Throughput Rate		800			*			kHz
DC ACCURACY								
Integral Linearity Error				±1			±0.75	LSB[1]
Differential Linearity Error				±1			*	LSB
No Missing Codes			Guaranteed			*		
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3, 4]				±0.5			±0.25	%
Full Scale Error Drift			±12			*		ppm/°C
Full Scale Error[3, 4]	Ext. 2.5000V Ref			±0.5			*	%
Full Scale Error Drift	Ext. 2.5000V Ref		±12			*		ppm/°C
Bipolar Zero Error[3]				±8			±4	LSB
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity								
($+V_{DIG} = +V_{ANA} = V_D$)	+4.75V < V_D < +5.25V			±5			*	LSB
	–5.25V < $-V_{ANA}$ < –4.75V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 250kHz	74	84		77	85		dB[5]
Total Harmonic Distortion	f_{IN} = 250kHz		–82	–74		–83	–77	dB
Signal-to-(Noise+Distortion)	f_{IN} = 250kHz	68	71		70	*		dB
Signal-to-Noise	f_{IN} = 250kHz	68	71		70	*		dB
Usable Bandwidth[6]			1.5			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			20			*		ns
Aperture Jitter			10			*		ps
Transient Response	FS Step		180			*		ns
Overvoltage Recovery[7]			250			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference DC Source Current (External load should be static)			100			*		µA
Internal Reference Drift			6					ppm/°C
External Reference Voltage Range For Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		V_D + 0.3	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 12-bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+2.8			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF
DIGITAL TIMING								
Bus Access Time				62			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

At T_A = –40°C to +85°C, f_S = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7819P, U			ADS7819PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
$+V_{DIG} = +V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$-V_{ANA}$		–5.25	–5	–4.75	*	*	*	V
$+I_{DIG}$			+16			*		mA
$+I_{ANA}$			+16			*		mA
$-I_{ANA}$			–13			*		mA
Derated Performance								
$+V_{DIG} = +V_{ANA}$		+4.5	+5	+5.5	*	*	*	V
$-V_{ANA}$		–5.5	–5	–4.5	*	*	*	V
Power Dissipation	f_S = 800kHz		225	275			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±2.5V input ADS7819, one LSB is 1.22mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±2.5V input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} ..... ±25V
REF ..... $+V_{ANA}$ +0.3V to AGND2 –0.3V
CAP ..... Indefinite Short to AGND2
Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
$+V_{ANA}$ ..... +7V
$+V_{DIG}$ to $+V_{ANA}$ ..... +0.3V
$+V_{DIG}$ 7V
$-V_{ANA}$ ..... –7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING AND PACKAGE INFORMATION

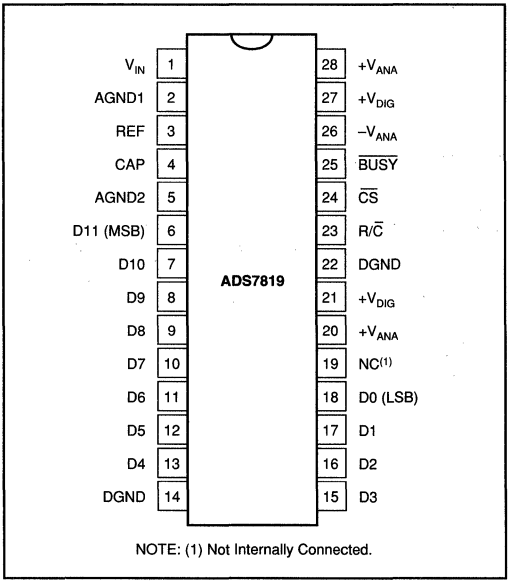
MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7819P	±1	68	–40°C to +85°C	28-Pin Plastic DIP	246
ADS7819PB	±0.75	70	–40°C to +85°C	28-Pin Plastic DIP	246
ADS7819U	±1	68	–40°C to +85°C	28-Pin SOIC	217
ADS7819UB	±0.75	70	–40°C to +85°C	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN ASSIGNMENTS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V.
2	AGND1		Analog Ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor.
4	CAP		Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V.
5	AGND2		Analog Ground.
6	D11 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
7	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
8	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
9	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
10	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
11	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
12	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
13	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
14	DGND		Digital Ground.
15	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
16	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
17	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
18	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
19			Not internally connected.
20	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28.
21	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28.
22	DGND		Digital ground.
23	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits.
24	$\overline{CS}$	I	Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits.
25	$\overline{BUSY}$	O	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
26	$-V_{ANA}$		Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
27	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28.
28	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.

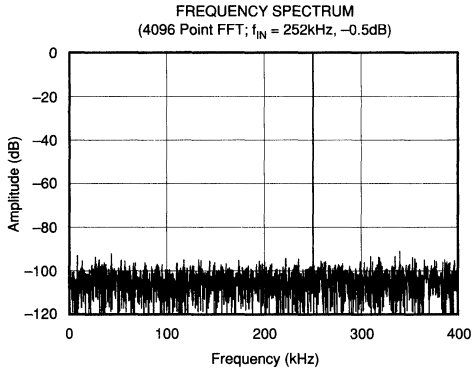
PIN CONFIGURATION

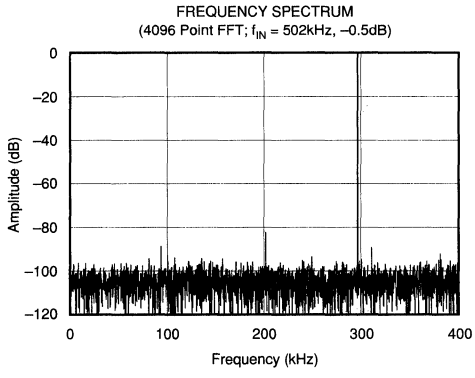


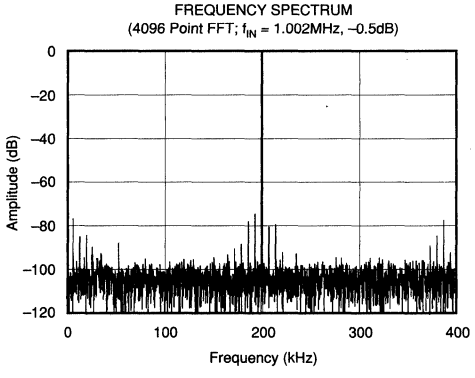
NOTE: (1) Not Internally Connected.

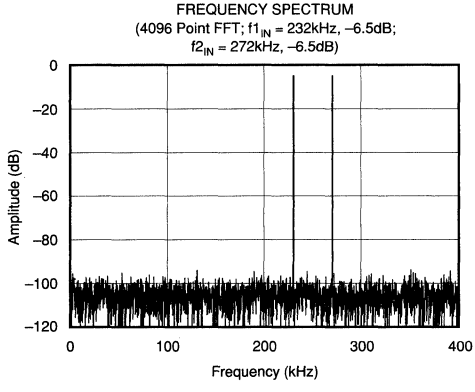
TYPICAL PERFORMANCE CURVES

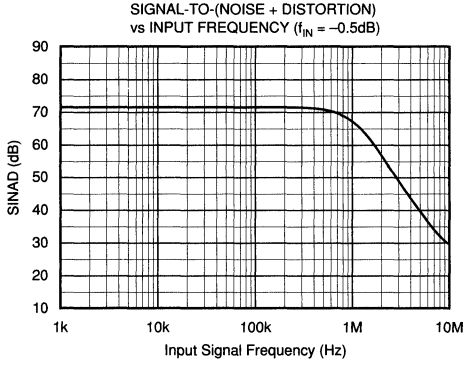
T = +25°C, f_S =800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = −5V, using internal reference and the input 50Ω resistors as shown in Figure 4b, unless otherwise specified.

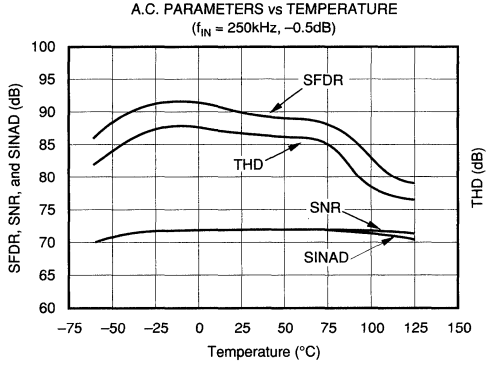






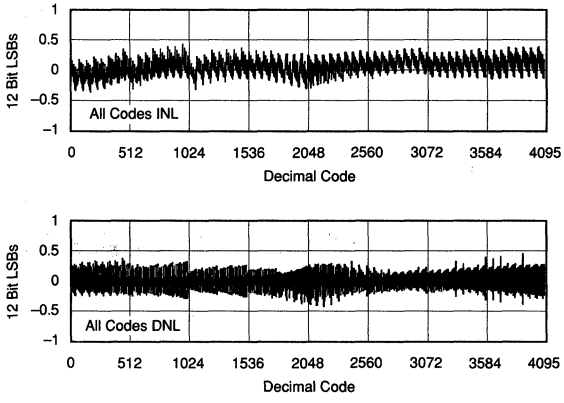


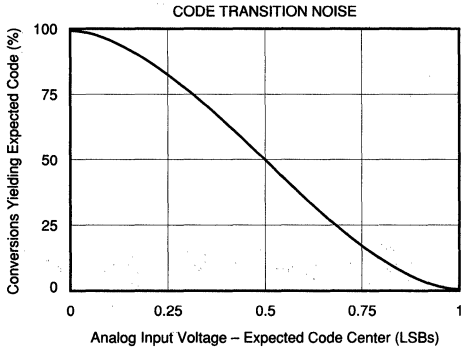


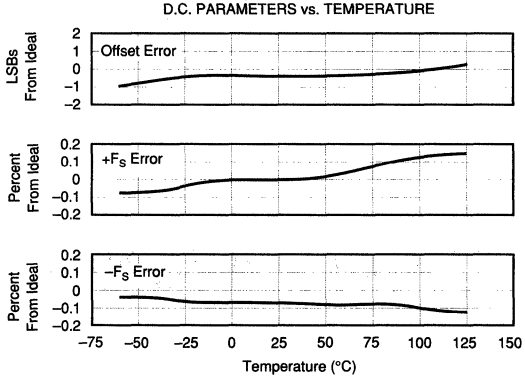


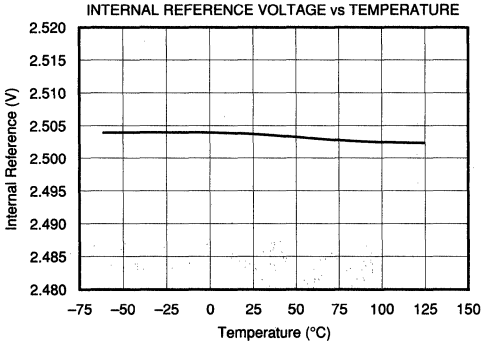
TYPICAL PERFORMANCE CURVES (CONT)

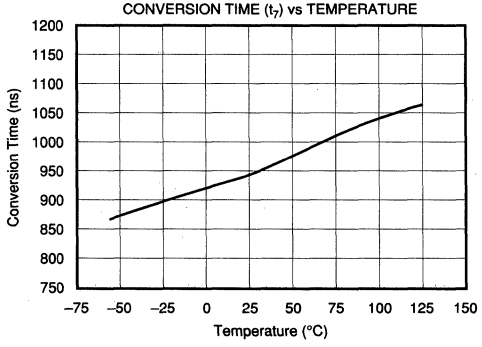
T = +25°C, f_S =800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistors as shown in Figure 4b, unless otherwise specified.











BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7819. Taking R/$\overline{C}$ (pin 23) LOW for 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on D11 (pin 6). $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	↑	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register but the output pins D11-D0 are tri-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table I. Control Line Functions for 'read' and 'convert'.

The ADS7819 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns puts the sample/hold of the ADS7819 in the hold state and starts a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7819 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal. Refer to Table I for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 and 3 for timing parameters.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
Full Scale Range	±2.5V	BINARY TWO'S COMPLEMENT	
Least Significant Bit (LSB)	1.22mV	BINARY CODE	HEX CODE
+Full Scale (2.5V – 1LSB)	2.499V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–1.22mV	1111 1111 1111	FFF
–Full Scale	–2.5V	1000 0000 0000	800

TABLE II. Ideal Input Voltages and Output Codes.

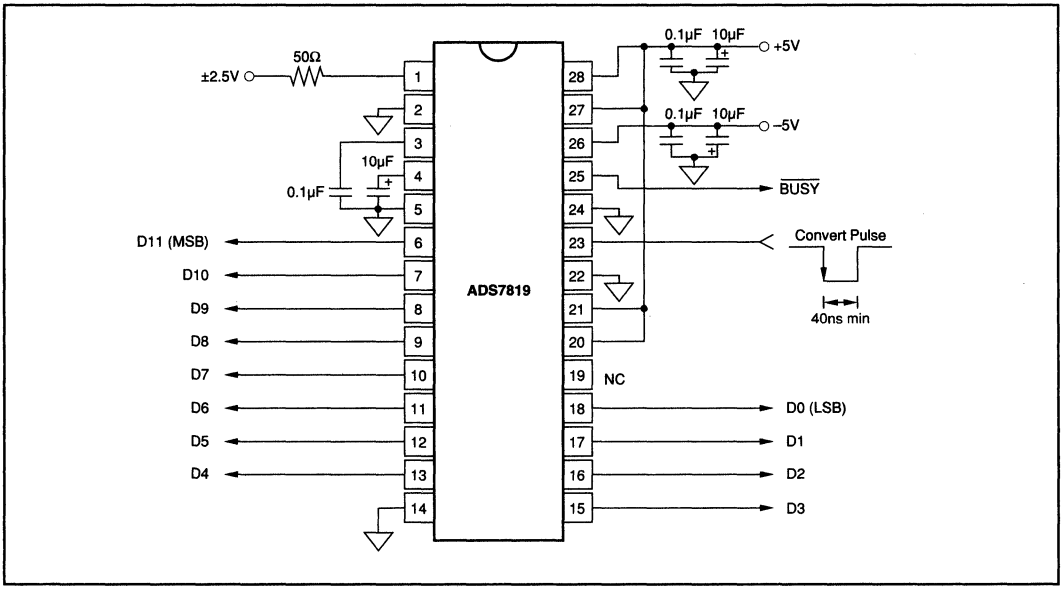


FIGURE 1. Basic Operation

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the **Reading Data** section and refer to Table I for control line functions for 'read' and 'convert' modes.

READING DATA

The ADS7819 outputs full parallel data in Binary Two's Complement data format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on D11-D0 (pins 6-13 and 15-18). Refer to Table II for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table III and Figures 2 and 3.

Note: For best performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feed through degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

INPUT RANGES

The ADS7819 has a ±2.5V input range. Figures 4a and 4b show the necessary circuit connections for the ADS7819 with and without external hardware trim. Offset and full scale error(1) specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4b. This external resistor makes it possible to trim the offset ±12mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain errors will be corrected in software or if they are negligible in regards to the particular application. See the **Calibration** section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external 50Ω resistor. The input resistor divider network provides inherent over-voltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

Note: The values shown for the internal resistors are for reference only. The exact values can vary by ±30%. This is true of all resistors internal to the ADS7819. Each resistive divider is trimmed so that the proper division is achieved.

NOTE: (1) Full scale error includes offset and gain errors and is measured at both +FS and –FS.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	Data Valid Delay After Start of Conversion		965	1100	ns
t_3	$\overline{BUSY}$ Delay From Start of Conversion		70	125	ns
t_4	$\overline{BUSY}$ LOW		960	1085	ns
t_5	$\overline{BUSY}$ Delay After End of Conversion		90		ns
t_6	Aperture Delay		20		ns
t_7	Conversion Time		940	1030	ns
t_8	Acquisition Time		180	220	ns
t_7 & t_8	Throughput Time		1120	1250	ns
t_9	Bus Relinquish Time	10	50	83	ns
t_{10}	$\overline{BUSY}$ Delay After Data Valid	20	65	100	ns
t_{11}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{12}	Time Between Conversions	1250			ns
t_{13}	Bus Access Time	10	30	62	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

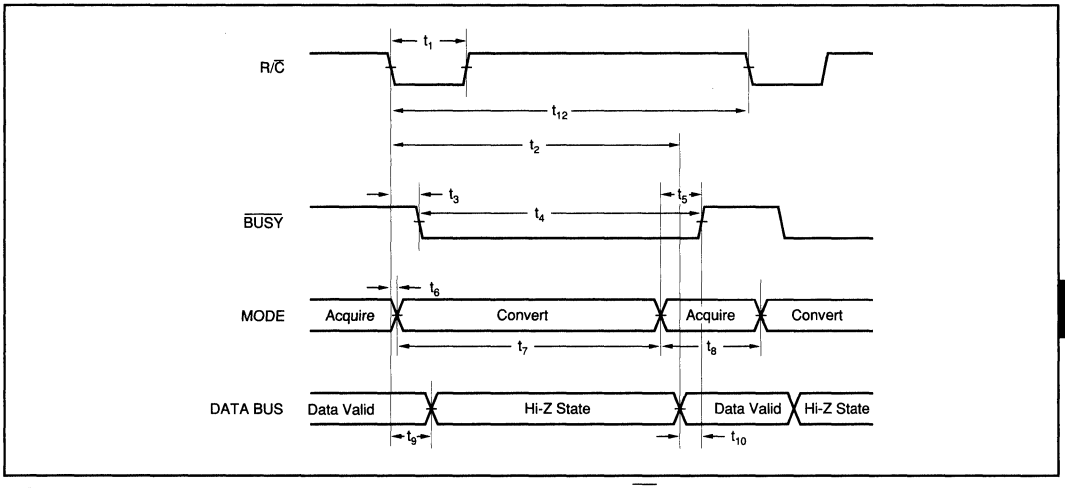


FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

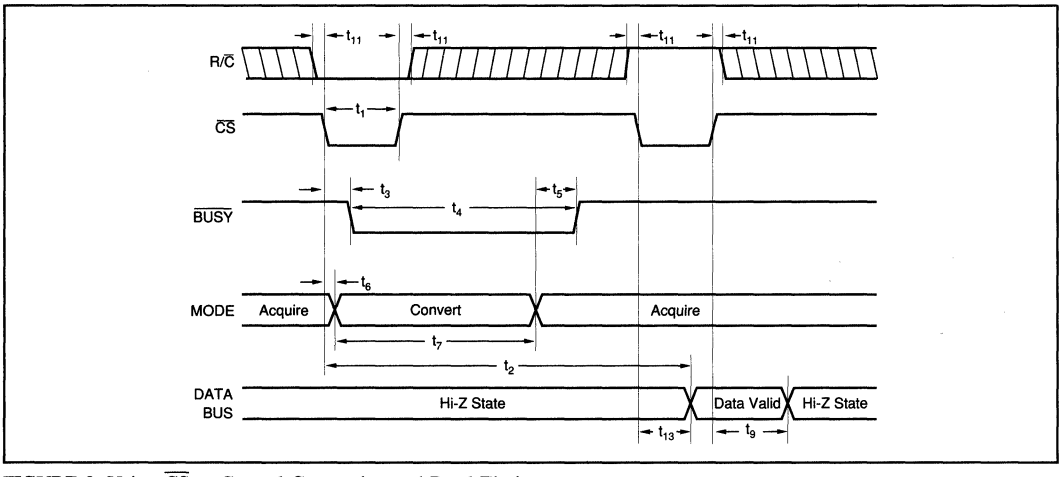


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

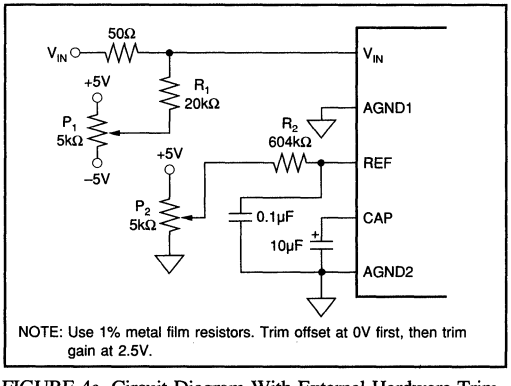


FIGURE 4a. Circuit Diagram With External Hardware Trim.

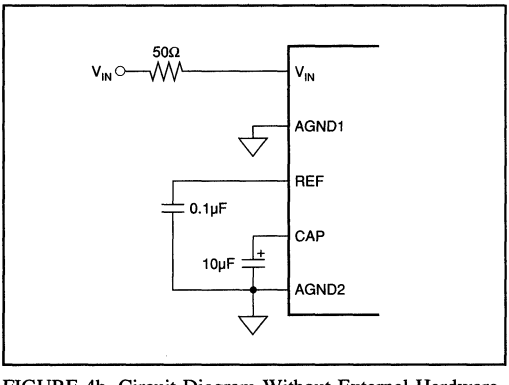


FIGURE 4b. Circuit Diagram Without External Hardware Trim.

CALIBRATION

The ADS7819 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain.

Hardware Calibration

To calibrate the offset and gain of the ADS7819, install the proper resistors and potentiometers as shown in Figure 4a. The calibration range is ±12mV for bipolar zero and ±30mV for full scale.

Potentiometer P_1 and resistor R_1 form the offset adjust circuit and P_2 and R_2 the gain adjust circuit. The exact values are not critical. R_1 and R_2 should not be made any larger than the value shown. They can easily be made smaller to provide increased adjustment range. Reducing these below 15% of the indicated values could begin to adversely affect the operation of the converter.

P_1 and P_2 can also be made larger to reduce power dissipation. However, larger resistances will push the useful adjustment range to the edges of the potentiometer. P_1 should probably not exceed 20kΩ and P2 100kΩ in order to maintain reasonable sensitivity.

Software Calibration

To calibrate the offset and gain of the ADS7819, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistor.

No Calibration

See Figure 4b for circuit connections. Note that the actual voltage dropped across the 50Ω resistor is nearly two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be taken into consideration when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external 50Ω resistor shown in Figure 4b may not be necessary in some applications. This resistor provides trim capability for the offset and compensates for a slight gain adjustment internal to the ADS7819. Not using the 50Ω resistor will cause a small gain error but will have no effect on the inherent offset error. Figure 5 shows typical transfer function characteristics with and without the 50Ω resistor in the circuit.

REFERENCE

The ADS7819 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally and output on CAP (pin 4).

The internal reference has a 6 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade.)

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 0.1µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

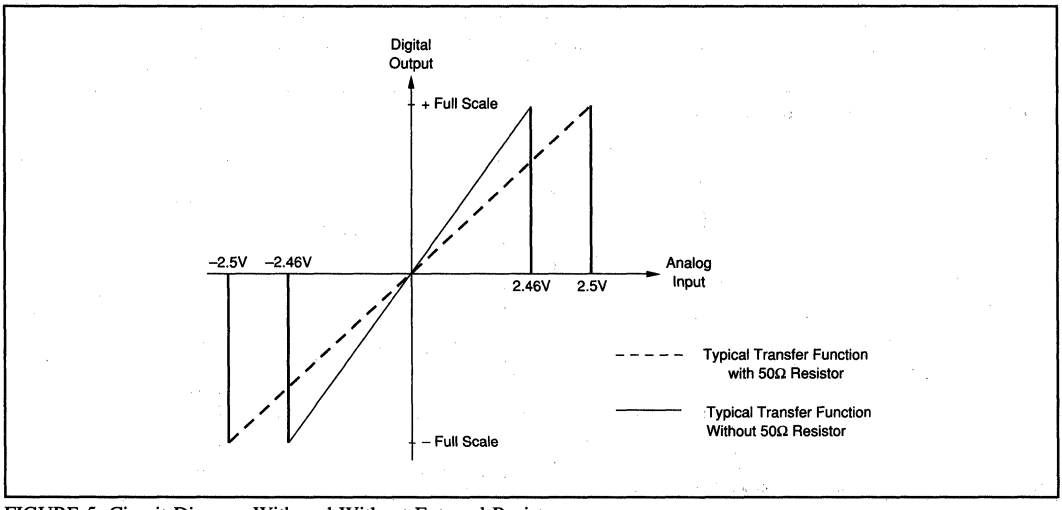


FIGURE 5. Circuit Diagram With and Without External Resistors.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 10µF tantalum capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 10µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

The ADS7819 uses the majority of its power for analog and static circuitry, and it should be considered as an analog component. For optimum performance, tie the analog and digital +5V power pins to the same +5V power supply and tie the analog and digital grounds together.

For best performance, the ±5V supplies can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If ±12V or ±15V supplies are present, simple regulators can be used. The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting $+V_{DIG}$ (pin 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic.

Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7819. DGND (pin 22) is the digital supply ground. AGND2 (pin 5) is the analog supply ground. AGND1 (pin 2) is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7819, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7819.

The resistive front end of the ADS7819 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7819 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7819 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

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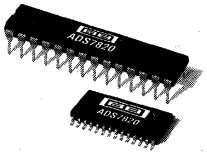


ADS7820

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

12-Bit 10µs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

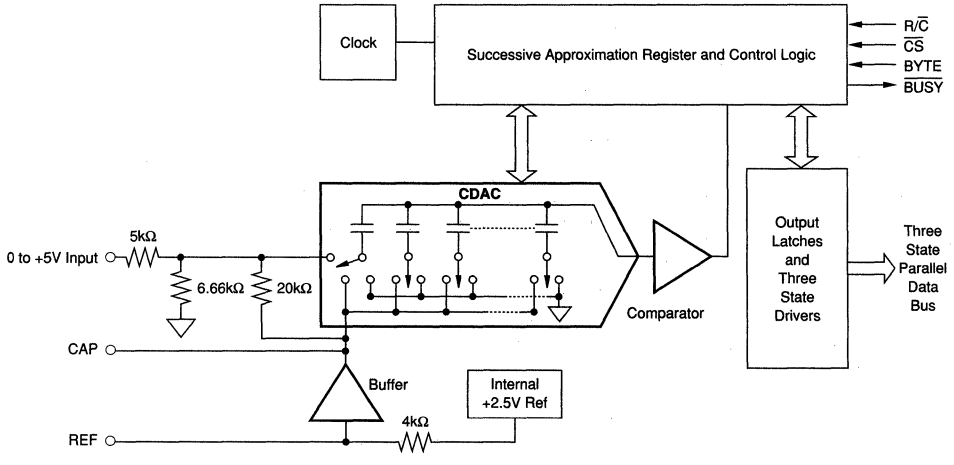
- **100kHz min SAMPLING RATE**
- **0 to +5V INPUT RANGE**
- **72dB min SINAD WITH 45kHz INPUT**
- **±1/2 LSB max INL AND DNL**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 16-BIT ADS7821**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **FULL PARALLEL DATA OUTPUT**
- **100mW max POWER DISSIPATION**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7820 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7820 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a 0 to +5V input range, with power dissipation under 100mW.

The 28-pin ADS7820 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7820P/U MIN	ADS7820P/U TYP	ADS7820P/U MAX	ADS7820PB/UB MIN	ADS7820PB/UB TYP	ADS7820PB/UB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			0 to +5			*		V
Impedance			10			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			5.7	8		*	*	µs
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±0.9			±0.45	LSB[1]
Differential Linearity Error				±0.9			±0.45	LSB
No Missing Codes			Guaranteed			*		Bits
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Offset Error				±10			*	mV
Offset Error Drift			±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 45kHz	80			*			dB[5]
Total Harmonic Distortion	f_{IN} = 45kHz			–80			*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 45kHz	70			72			dB
Signal-to-Noise	f_{IN} = 45kHz	70			72			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 12 bits				
Data Coding				Straight Binary				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7820P/U			ADS7820PB/UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
$+I_{DIG}$			0.3			*		mA
$+I_{ANA}$			16			*		mA
Power Dissipation	f_S = 100kHz			100			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, 0 to +5V input ADS7820, one LSB is 1.22mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer as shown in Figure 4b. (4) Full scale error is the worst case of Full Scale untrimmed deviation from ideal last code transition divided by the transition voltage and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} ..... ±20V
REF ..... $+V_{ANA}$ +0.3V to AGND2 –0.3V
CAP ..... Indefinite Short to AGND2
Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7820P	Plastic DIP	246
ADS7820PB	Plastic DIP	246
ADS7820U	SOIC	217
ADS7820UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

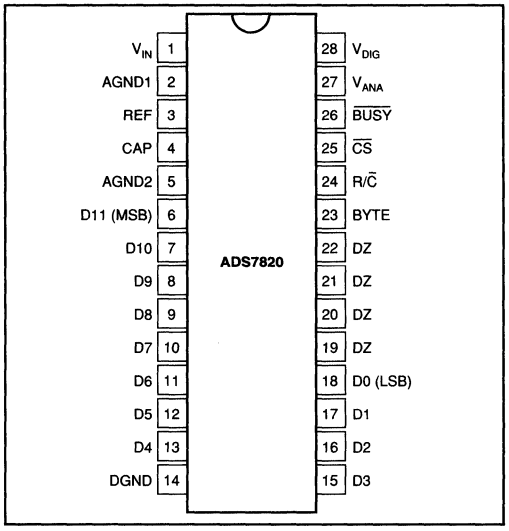
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7820P	±0.9	70	–40°C to +85°C	Plastic DIP
ADS7820PB	±0.45	72	–40°C to +85°C	Plastic DIP
ADS7820U	±0.9	70	–40°C to +85°C	SOIC
ADS7820UB	±0.45	72	–40°C to +85°C	SOIC

PIN CONFIGURATION



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		5000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		5.7	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		5		µs
$t_7 + t_8$	Throughput Time		7.5	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE I. Conversion Timing.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_{IN}	Analog Input. Full-scale input range is 0 to +5V.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	REF	Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 2.2µF Tantalum capacitor.
4	CAP	Reference Buffer Capacitor. 2.2µF Tantalum to ground.
5	AGND2	Analog Ground.
6	D11 (MSB)	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D10	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D9	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D8	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D7	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D6	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D5	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D4	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND	Digital Ground.
15	D3	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D2	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D1	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D0 (LSB)	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	DZ	Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	DZ	Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	DZ	Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	DZ	Data Zero. LOW when $\overline{CS}$ LOW and R/$\overline{C}$ HIGH. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	Byte Select. With BYTE LOW, data will be output as indicated above, causing pin 6 (D11) to output the MSB, and pin 18 (D0) to output the LSB. Pins 19 to 22 will output LOWs. With BYTE HIGH, the top and bottom 8 bits of data will be switched, so that pin 6 outputs data bit 3, pin 9 outputs data bit 0 (LSB), pin 10 to 13 output LOWs, pin 15 outputs data bit 11 (MSB) and pin 22 outputs data bit 4.
24	R/$\overline{C}$	Read/Convert input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits.
25	$\overline{CS}$	Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits.
26	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be high when $\overline{BUSY}$ rises, or another conversion will start, without time for signal acquisition.
27	V_{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
28	V_{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full Scale Range	0 to +5V		
Least Significant Bit (LSB)	1.22mV		
Full Scale	4.99878V	1111 1111 1111	FFF
Midscale	2.5V	1000 0000 0000	800
One LSB below Midscale	2.49878V	0111 1111 1111	7FF
Zero Scale	0V	0000 0000 0000	0

Table II. Ideal Input Voltages and Output Codes.

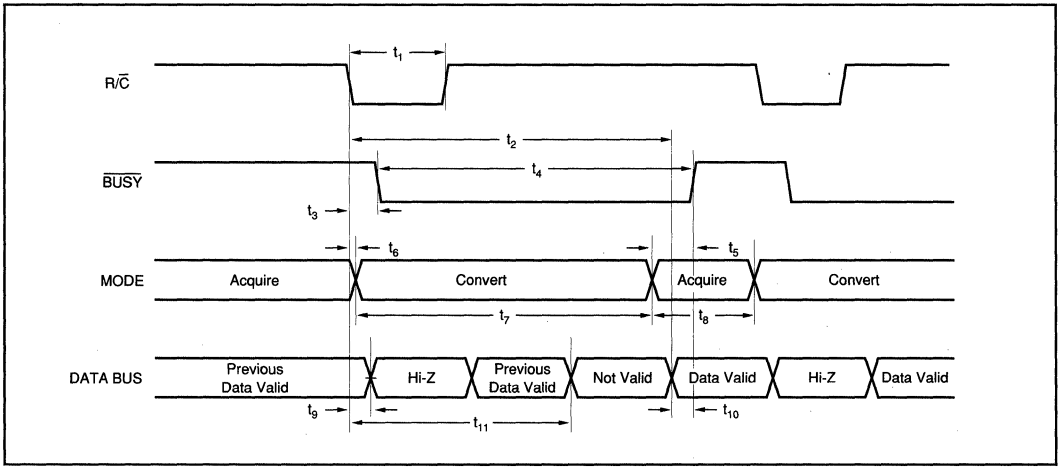


FIGURE 1. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

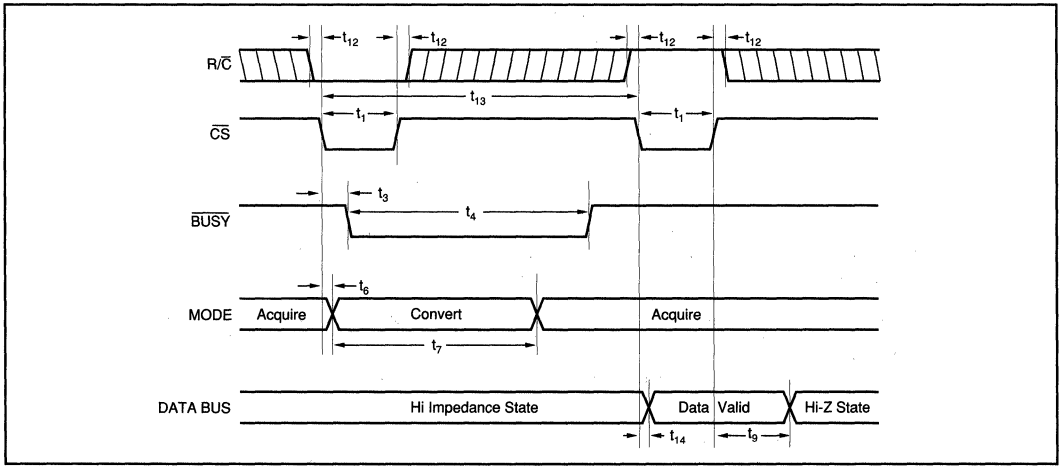


FIGURE 2. Using $\overline{CS}$ to Control Conversion and Read Timing.

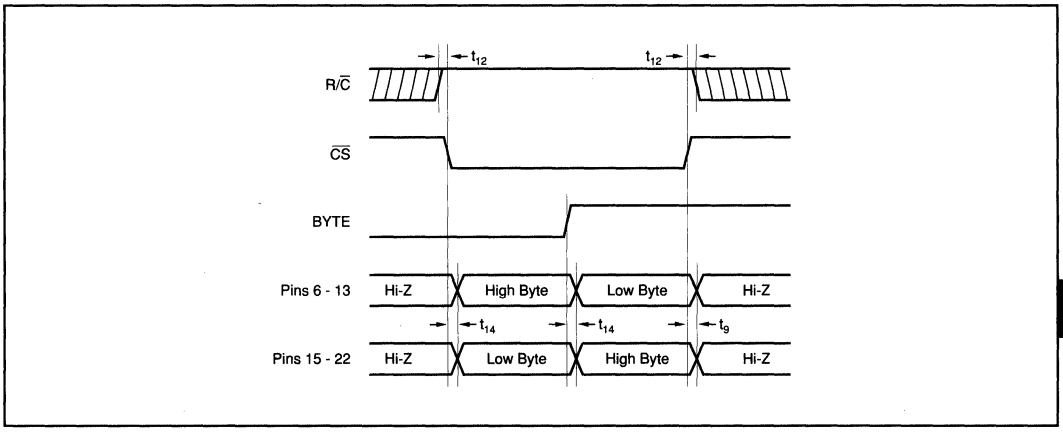


FIGURE 3. Using $\overline{CS}$ and BYTE to Control Data Bus.

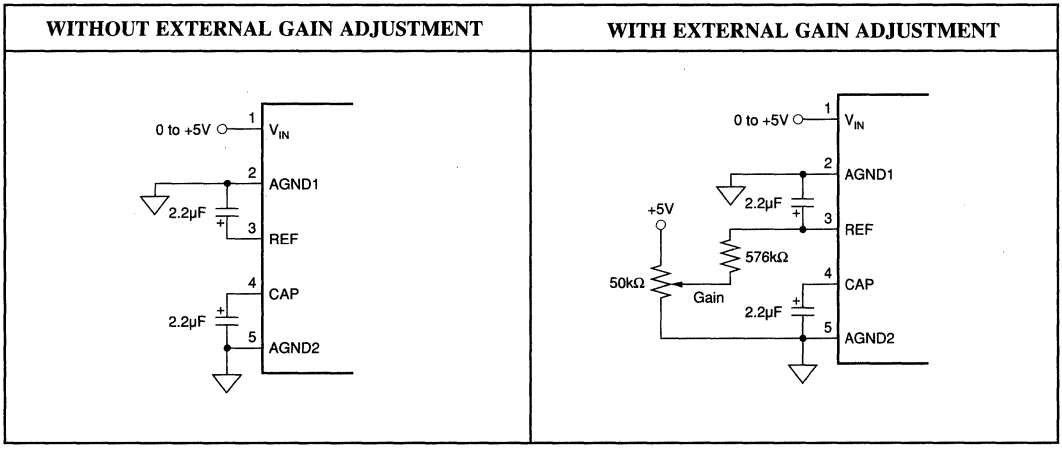


FIGURE 4. Circuit Diagram With and Without External Gain Adjustment.

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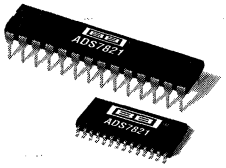


ADS7821

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

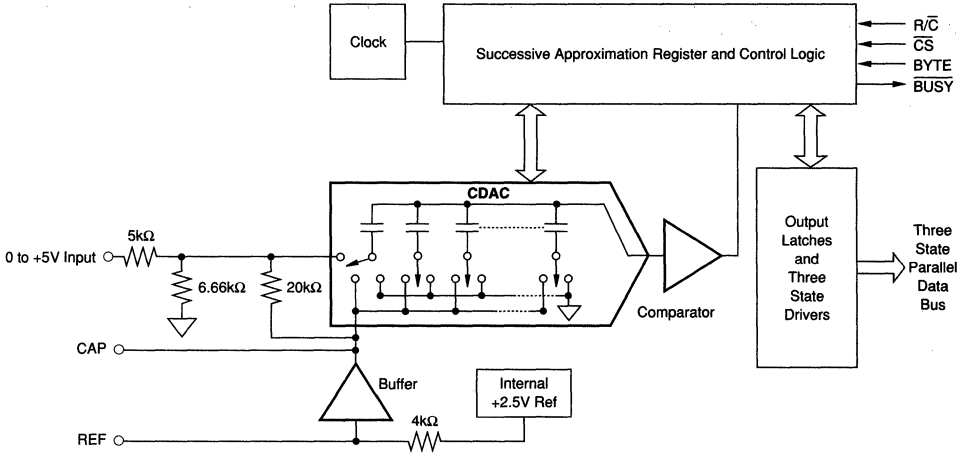
- 100kHz min SAMPLING RATE
- 0 to +5V INPUT RANGE
- 86dB min SINAD WITH 20kHz INPUT
- DNL: 16-bits "No Missing Codes"
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7820
- USES INTERNAL OR EXTERNAL REFERENCE
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 28-PIN 0.3" PLASTIC DIP AND SOIC

DESCRIPTION

The ADS7821 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7821 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide a 0 to +5V input range, with power dissipation under 100mW.

The 28-pin ADS7821 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the –25°C to +85°C range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7821P, U			ADS7821PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges			0 to +5			*		V
Impedance			10			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			7.6	8		*	*	µs
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±4			±3	LSB[1]
No Missing Codes		15			16			Bits
Transition Noise[2]			0.9			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Offset Error				±10			*	mV
Offset Error Drift			±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	20kHz	90			96			dB[5]
Total Harmonic Distortion	20kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	20kHz	83			86			dB
	–60dB Input		28			30		dB
Signal-to-Noise	20kHz	83			86			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 16 bits				
Data Coding				Straight Binary				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7821P, U			ADS7821PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation	f_S = 100kHz			100			*	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, 0 to +5V input ADS721, one LSB is 76µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer as shown in Figure 6a. (4) Full scale error is the worst case of Full Scale untrimmed deviation from ideal last code transition divided by the transition voltage and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	±20V
REF	+V_{ANA} +0.3V to AGND2 –0.3V
CAP	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to +V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7821P	Plastic DIP	246
ADS7821PB	Plastic DIP	246
ADS7821U	SOIC	217
ADS7821UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

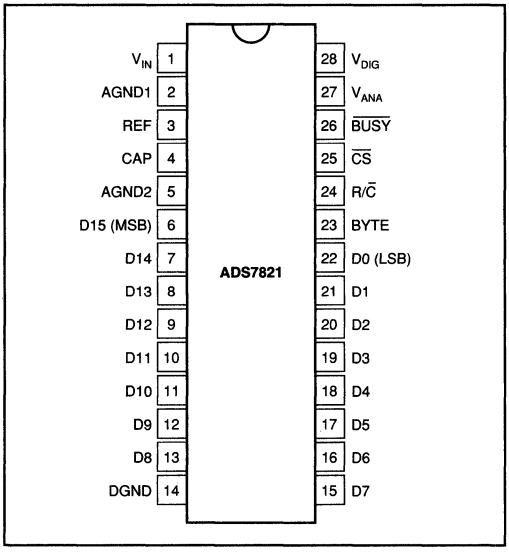
ORDERING INFORMATION

MODEL	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7821P	±4	83	–25°C to +85°C	Plastic DIP
ADS7821PB	±3	86	–25°C to +85°C	Plastic DIP
ADS7821U	±4	83	–25°C to +85°C	SOIC
ADS7821UB	±3	86	–25°C to +85°C	SOIC

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Swaps Pins 6 through 13 with Pins 15 through 22 when HIGH. See Figures 2 and 5.
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION



BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7821 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns (5µs max) will initiate a conversion. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Straight Binary with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7821 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7821 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7821 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 3 through 5 for timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. However, the output will become active whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 3 and 4 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".

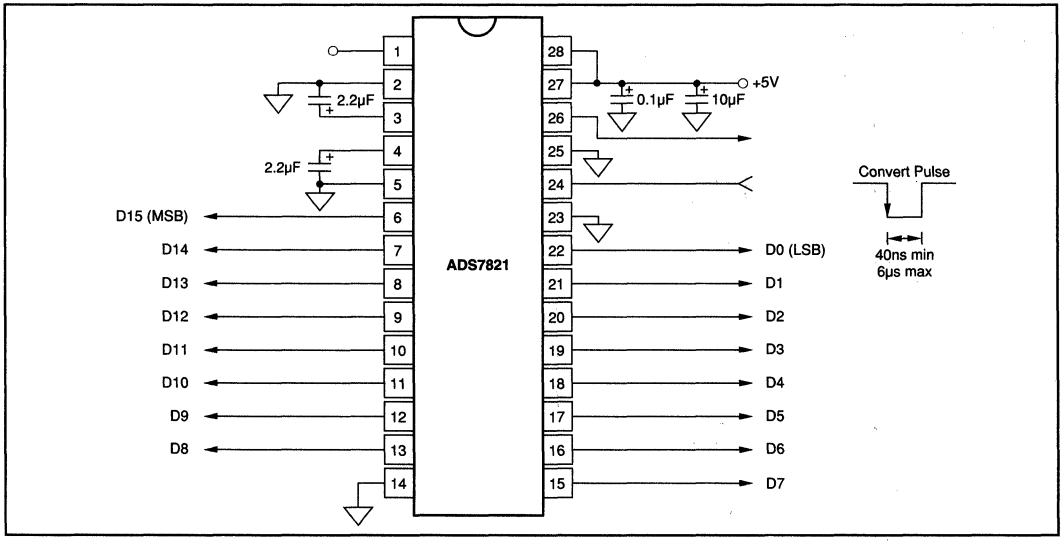


FIGURE 1. Basic Operation.

READING DATA

The ADS7821 outputs full or byte-reading parallel data in Straight Binary data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full Scale Range	0 to +5V		
Least Significant Bit (LSB)	76µV		
Full Scale	4.999924V	1111 1111 1111 1111	FFFF
Midscale	2.5V	1000 0000 0000 0000	8000
One LSB below Midscale	2.499924V	0111 1111 1111 1111	7FFF
Zero Scale	0V	0000 0000 0000 0000	0000

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D15-D0 (pin 6-13 and 15-22). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 5µs after the start of conversion 'n'. Do not attempt to read data from 5µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tying $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		5000	ns
t_2	Data Valid Delay after Start of Conversion			8	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after Start of Conversion		5		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

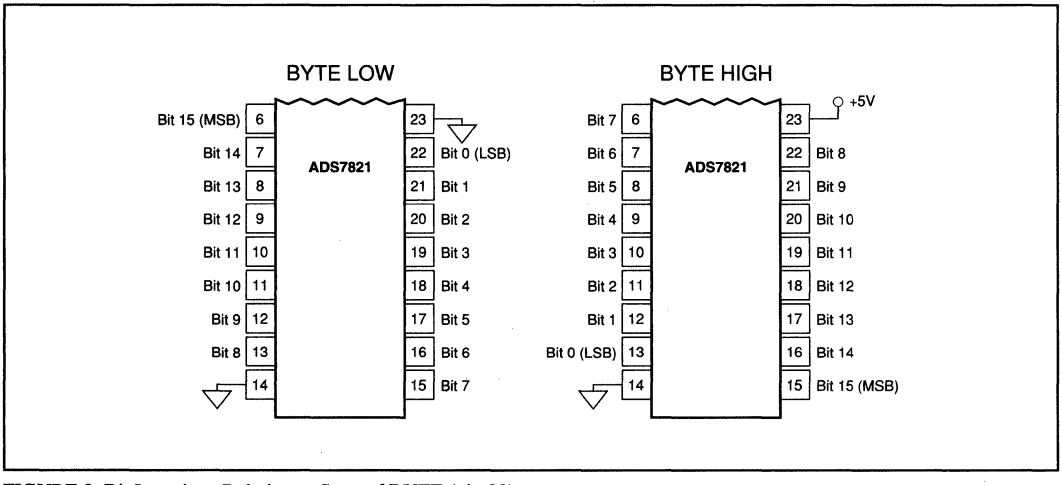


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

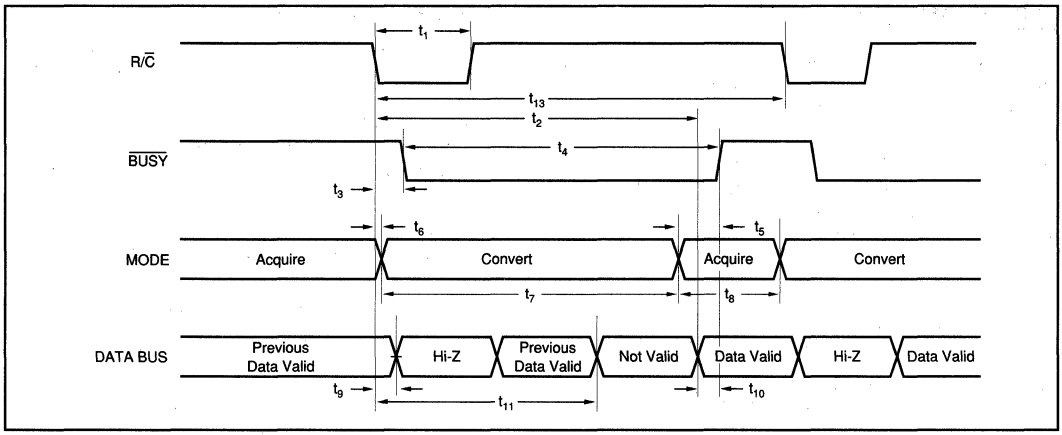


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

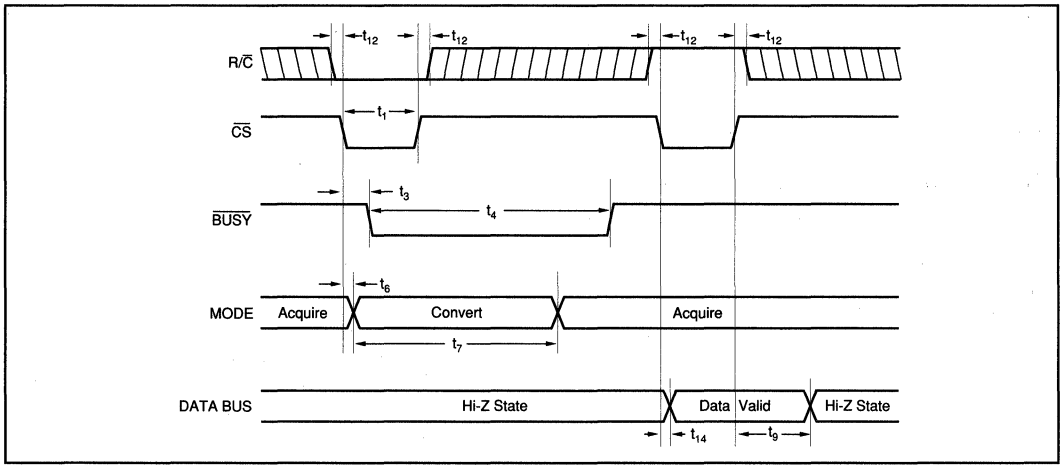


FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

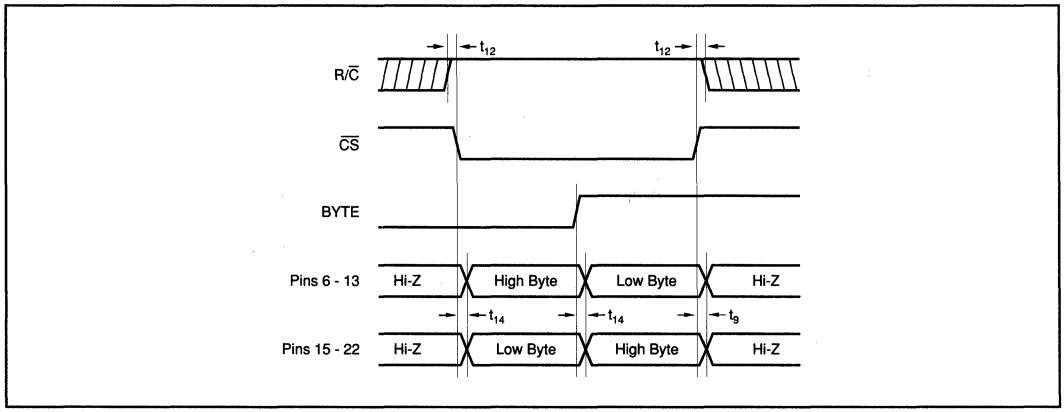


FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

INPUT RANGES

The ADS7821 offers a 0 to +5V input range. Figure 6 shows the necessary circuit connections for the ADS7821 with and without hardware gain trim. Offset and full scale error[1] specifications are tested and guaranteed with the circuit shown in Figure 6b. Adjustments for offset and gain are described in the **Hardware Calibration** section of this data sheet.

The nominal input impedance of 10kΩ results from the internal resistor network shown on the front page of the product data sheet. The input resistor divider network provides inherent overvoltage protection guaranteed to at lease ±20V.

NOTE: (1) Full scale error includes offset and gain errors.

HARDWARE CALIBRATION

To calibrate the gain of the ADS7821, install the proper resistor and potentiometer as shown in Figure 6a. The calibration range is ±60mV.

There is no inherent offset calibration method provided by the ADS7821. The offset adjustment can be accomplished by summing in a small offset to the circuitry prior to the ADS7821.

The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

REFERENCE

The ADS7821 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to directly drive external loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a static load. Static loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7821. Use of an external buffer is recommended for loads requiring more than 2mA. Do not attempt to directly drive any dynamic load with the output voltage on CAP. This will cause performance degradation of the converter.

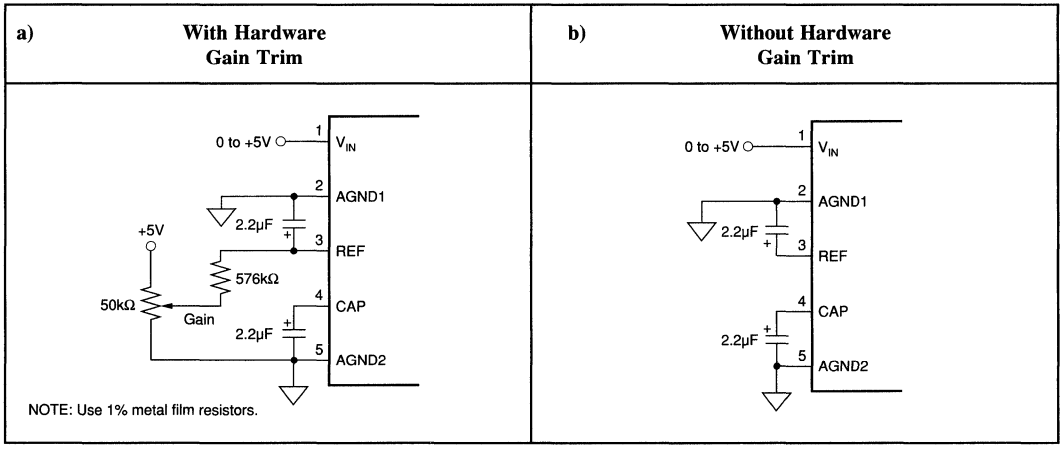


FIGURE 6. Circuit Diagram With and Without External Gain Trim.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7821 uses 90% of its power for the analog circuitry. The ADS7821 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7821. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7821, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. Any op amp sufficient for the signal in an application should be sufficient to drive the ADS7821.

The resistive front end of the ADS7821 also provides a guaranteed ±20V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7821 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7821 has an internal LSB size of 38µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

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ADS7824

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

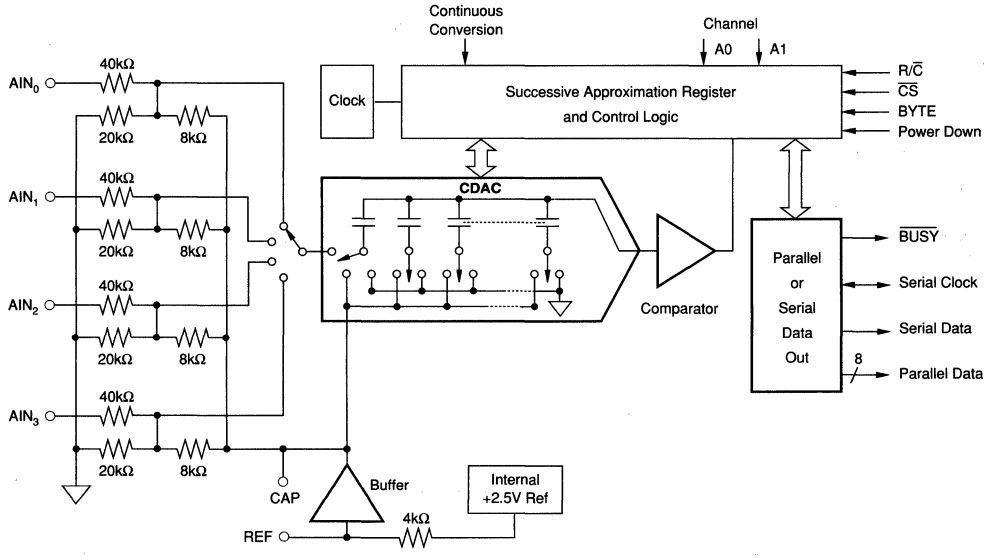
4 Channel, 12-Bit Sampling CMOS A/D Converter

FEATURES

- 25µs max SAMPLING AND CONVERSION
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7825
- PARALLEL AND SERIAL DATA OUTPUT
- 28-PIN 0.3" PLASTIC DIP AND SOIC
- ±0.5 LSB max INL AND DNL
- 50mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- ±10V INPUT RANGE, FOUR CHANNEL MULTIPLEXER
- CONTINUOUS CONVERSION MODE

DESCRIPTION

The ADS7824 can acquire and convert 12 bits to within ±0.5 LSB in 25µs max while consuming only 50mW max. Laser-trimmed scaling resistors provide the standard industrial ±10V input range and channel-to-channel matching of ±0.1%. The ADS7824 is a low-power 12-bit sampling A/D with a four channel input multiplexer, S/H, clock, reference, and a parallel/serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. The 28-pin ADS7824 is available in a plastic 0.3" DIP and in a SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, $V_{S1} = V_{S2} = V_S$ = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7824P, U			ADS7824PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±10V			*		V
Impedance	Channel On or Off		45.7			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Acquisition Time				5			*	µs
Multiplexer Settling Time	Includes Acquisition			5			*	µs
Complete Cycle (Acquire and Convert)				25			*	µs
Complete Cycle (Acquire and Convert)	CONTC = +5V			50			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error			±0.15	±1		*	±0.5	LSB[1]
Differential Linearity Error			±0.15	±1		*	±0.5	LSB
No Missing Codes			Guaranteed			*		
Transition Noise[2]			0.1			*		LSB
Full Scale Error[3,4]	Internal Reference			±0.5			±0.25	%
Full Scale Error Drift	Internal Reference		±7			±5		ppm/°C
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±2			*		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Channel-to-Channel Mismatch				0.1			*	%
Power Supply Sensitivity	+4.75 < V_S < +5.25			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range[5]	f_{IN} = 1kHz	80	90		*	*		dB
Total Harmonic Distortion	f_{IN} = 1kHz		–90	–80		*	*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz	70	73		72	*		dB
Signal-to-Noise	f_{IN} = 1kHz	70	73		72	*		dB
Channel Separation[6]	f_{IN} = 1kHz	100	120		*	*		dB
–3dB Bandwidth			TBD			*		MHz
Useable Bandwidth[7]			TBD			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response[8]	FS Step		5			*		µs
Overvoltage Recovery[9]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format		Parallel in two bytes; Serial				*		
Data Coding		Binary Two's Complement				*		
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_S			±5			*	µA
Output Capacitance	High-Z State			15			15	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{S1} = V_{S2} = V_S = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

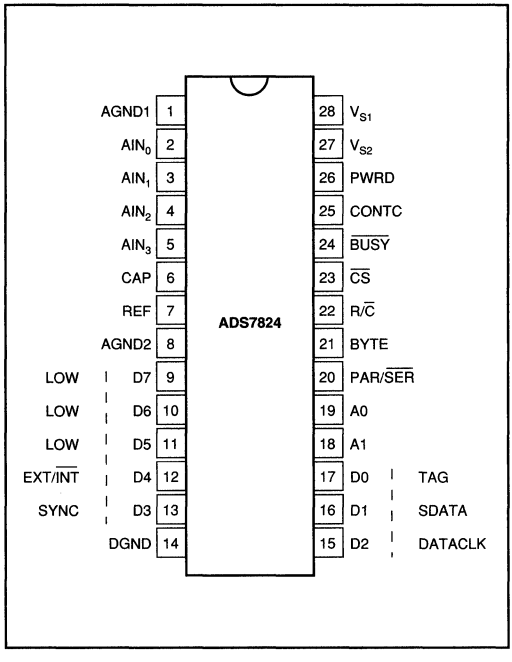
PARAMETER	CONDITIONS	ADS7824P, U			ADS7824PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	PAR/$\overline{SER}$ = +5V			83			*	ns
Bus Relinquish Time	PAR/$\overline{SER}$ = +5V			83			*	ns
Data Clock	PAR/$\overline{SER}$ = 0V							
Internal Clock (Output only when transmitting data)	EXT/$\overline{INT}$ LOW	0.5		1.5	*		*	MHz
External Clock (Can run continually)	EXT/$\overline{INT}$ HIGH	0.1		10	*		*	MHz
POWER SUPPLIES								
V_{S1} = V_{S2} = V_S		+4.75	+5	+5.25	*	*	*	V
Power Dissipation	f_S = 40kHz			50			*	mW
	PWRD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7824, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) A full scale sinewave input on one channel will be attenuated by this amount on the other channels. (7) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (8) The ADS7824 will accurately acquire any input step if given a full acquisition period after the step. (9) Recovers to specified performance after 2 x FS input overvoltage, and normal acquisitions can begin.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: AIN_0, AIN_1, AIN_2, AIN_3	±25V
REF	(AGND2 –0.3V) to (V_S + 0.3V)
CAP	Indefinite Short to AGND2, Momentary Short to V_S
V_{S1} and V_{S2} to AGND2	7V
V_{S1} to V_{S2}	±0.3V
Difference between AGND1, AGND2 and DGND	±0.3V
Digital Inputs and Outputs	–0.3V to (V_S + 0.3V)
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Maximum Input Current to Any Pin	100mA

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN #	NAME	I/O	DESCRIPTION
1	AGND1		Analog Ground. Used internally as ground reference point.
2	AIN_0		Analog Input Channel 0. Full-scale input range is ±10V. See Table I.
3	AIN_1		Analog Input Channel 1. Full-scale input range is ±10V. See Table I.
4	AIN_2		Analog Input Channel 2. Full-scale input range is ±10V. See Table I.
5	AIN_3		Analog Input Channel 3. Full-scale input range is ±10V. See Table I.
6	CAP		Internal Reference Output Buffer. 2.2µF Tantalum to ground.
7	REF		Reference Input/Output. Outputs +2.5V nominal. If used externally, must be buffered to maintain ADS7824 accuracy. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
8	AGND2		Analog Ground.
9	D7	O	Parallel Data Bit 7 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
10	D6	O	Parallel Data Bit 6 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
11	D5	O	Parallel Data Bit 5 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
12	D4	I/O	Parallel Data Bit 4 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, a LOW level input here will transmit serial data on SDATA from the previous conversion using the internal clock; a HIGH input here will transmit serial data using an external clock input on DATACLK. See Table II.
13	D3	O	Parallel Data Bit 3 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
14	DGND		Digital Ground.
15	D2	I/O	Parallel Data Bit 2 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, this will output the internal conversion clock if a LOW is input on D4; will be an input for an external data transmission clock if D4 is HIGH. See Table II.
16	D1	O	Parallel Data Bit 1 if PAR/$\overline{SER}$ HIGH; SDATA serial data output if PAR/$\overline{SER}$ LOW. See Table II.
17	D0	I/O	Parallel Data Bit 0 if PAR/$\overline{SER}$ HIGH; TAG data input if PAR/$\overline{SER}$ LOW. See Table II.
18	A1	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table II.
19	A2	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table II.
20	PAR/$\overline{SER}$	I	Select Parallel or Serial Output. If HIGH, parallel data will be output on D0 thru D7. If LOW, serial data will be output on SDATA. See Table II.
21	BYTE	I	Byte Select. Only used with parallel data, when PAR/$\overline{SER}$ HIGH. Determines which byte is available on D0 thru D7. Changing BYTE with $\overline{CS}$ LOW and R/$\overline{C}$ HIGH will cause the data bus to change accordingly. LOW selects the 8 MSBs; HIGH selects the 4 LSBs.
22	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH.
23	$\overline{CS}$	I	Chip Select. Internally OR'd with R/$\overline{C}$. With CONTC LOW and R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH.
24	$\overline{BUSY}$	O	Busy Output. Falls when conversion is started; remains LOW until the conversion is completed and the data is latched into the output register. In parallel output mode or in internal clock serial mode, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
25	CONTC	I	Continuous Conversion Input. If LOW, conversions will occur normally when initiated using $\overline{CS}$ and R/$\overline{C}$; if HIGH, acquisition and conversions will take place continually, cycling through all four input channels, as long as $\overline{CS}$, R/$\overline{C}$ and PWRD are LOW. See Table II.
26	PWRD	I	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output register. In the continuous conversion mode, the multiplexer address channel is reset to channel 0
27	V_{S2}		Supply Input. Nominally +5V. Connect directly to pin 27. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
28	V_{S1}		Supply Input. Nominally +5V. Connect directly to pin 28.

ADS7824 TIMING AND CONTROL

A1	A0	CHANNEL SELECTED	DESCRIPTION OF OPERATION
0	0	AIN_0	Channel to be converted during conversion n + 1 is latched when conversion n is initiated. The selected input starts being acquired as soon as conversion n is done.
0	1	AIN_1	
1	0	AIN_2	
1	1	AIN_3	

TABLE Ia. A0 and A1 Inputs (CONTC LOW.)

A1	A0	DATA AVAILABLE FROM CHANNEL	CHANNEL TO BE OR BEING CONVERTED	DESCRIPTION OF OPERATION
0	0	AIN_3	AIN_0	Channel being acquired or converted is output on these address lines. Data is valid for the previous channel. These lines are updated when $\overline{BUSY}$ rises.
0	1	AIN_0	AIN_1	
1	0	AIN_1	AIN_2	
1	1	AIN_2	AIN_3	

TABLE Ib. A0 and A1 Outputs (CONTC HIGH.)

INPUTS						OUTPUTS								
$\overline{CS}$	R/$\overline{C}$	BYTE	CONTC	PWRD	$\overline{BUSY}$	D7	D6	D5	D4	D3	D2	D1	D0	COMMENTS
1	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
X	0	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
0	1	0	X	X	X	B11 (MSB)	B10	B9	B8	B7	B6	B5	B4	Results from last completed conversion.
0	1	1	X	X	X	B3	B2	B1	B0 (LSB)	LOW	LOW	LOW	LOW	Results from last completed conversion.
0	1	X	X	X	↑	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	Data will change at the end of a conversion.

TABLE IIa. Read Control for Parallel Data (PAR/SER = 5V.)

$\overline{CS}$	R/$\overline{C}$	CONTC	PWRD	$\overline{BUSY}$	D7, D6, D5 LOW	D4 EXT/$\overline{INT}$	D3 SYNC	D2 DATACLK	D1 SDATA	D0 TAG	COMMENTS
Input	Input	Input	Input	Output	Output	Input	Output	I/O	Output	Input	
1	X	X	X	X	Hi-Z	LOW	Hi-Z	Output, Hi-Z	Hi-Z	X	
X	0	X	X	X	Hi-Z	LOW	Hi-Z	Output, Hi-Z	Hi-Z	X	
0	↓	0	X	1	LOW	LOW	LOW	Output	Output	X	Starts transmission of data from previous conversion on SDATA synchronized to 16 pulses output on DATACLK.
↓	0	0	X	1	LOW	LOW	LOW	Output	Output	X	Starts transmission of data from previous conversion on SDATA synchronized to 16 pulses output on DATACLK.
0	1	0	X	X	LOW	HIGH	LOW	Input	Output	Input	The level output on SDATA will be the level input on TAG 16 DATACLK input cycles earlier.
0	1	0	X	↑	LOW	HIGH	LOW	Input	Output	Input	At the end of the conversion, when $\overline{BUSY}$ rises, data from the conversion will be shifted into the output registers. If a clock is being input on DATACLK, valid data will be lost.
0	↑	0	X	1	LOW	HIGH	LOW	Input	Output	X	Initiates transmission of a HIGH pulse on SYNC followed by data from last completed conversion on SDATA synchronized to the input on DATACLK.
↓	1	0	X	1	LOW	HIGH	LOW	Input	Output	X	Initiates transmission of a HIGH pulse on SYNC followed by data from last completed conversion on SDATA synchronized to the input on DATACLK.
0	0	1	0	↓	LOW	LOW	LOW	Output	Output	X	Starts transmission of data from previous conversion on SDATA synchronized to 16 pulses output on DATACLK
↓	1	X	X	X	LOW	HIGH	Output	Input	Output	X	SDATA becomes active. Inputs on DATACLK shift out data.
0	↑	X	X	X	LOW	HIGH	Output	Input	Output	X	SDATA becomes active. Inputs on DATACLK shift out data.
↓	0	1	X	X	LOW	LOW	LOW	Output	Output	X	Restarts continuous conversion mode. Data starts being transmitted when $\overline{BUSY}$ next rises.
0	↓	1	X	X	LOW	LOW	LOW	Output	Output	X	Restarts continuous conversion mode. Data starts being transmitted when $\overline{BUSY}$ next rises.

TABLE IIb. Read Control for Serial Data (PAR/SER = 0V.)

CONTC	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	PWRD	A0 and A1	OPERATION
0	X	X	X	X	Inputs	Initiating conversion n latches in the levels input on A0 and A1 to select the channel for conversion n + 1
0	X	X	0	0	Inputs	Conversion in process. New convert commands ignored.
0	0	↓	1	0	Inputs	Initiates conversion on channel selected at start of previous conversion.
0	↓	0	1	0	Inputs	Initiates conversion on channel selected at start of previous conversion.
0	X	X	X	1	Inputs	All analog functions powered down. Conversions in process or initiated will yield meaningless data.
1	X	X	X	X	Outputs	The end of conversion n (when $\overline{BUSY}$ rises) increments the internal channel latches and outputs the channel address for conversion n + 1 on A0 and A1.
1	X	X	0	0	Outputs	Conversion in process
1	0	↓	1	0	Outputs	Restarts continuous conversion process on next input channel.
1	↓	0	1	0	Outputs	Restarts continuous conversion process on next input channel.
1	X	X	X	1	Outputs	All analog functions powered down. Conversions in process or initiated will yield meaningless data. Resets selected input channel for next conversion to IN_0.

TABLE III. Conversion Control.

BASIC OPERATION

Figure 1 shows the simple circuit required to operate the ADS7824, converting a single input channel. Taking R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output registers are updated. With BYTE (pin 21) in the LOW state, the eight MSB's will be output in Binary Two's Complement with the MSB (BIT 11) at pin 9. By bringing BYTE HIGH, the four LSB's will be output with the LSB (BIT 0) at pin 12 (See Table IIa). $\overline{BUSY}$ going HIGH can be used to latch the MSB data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

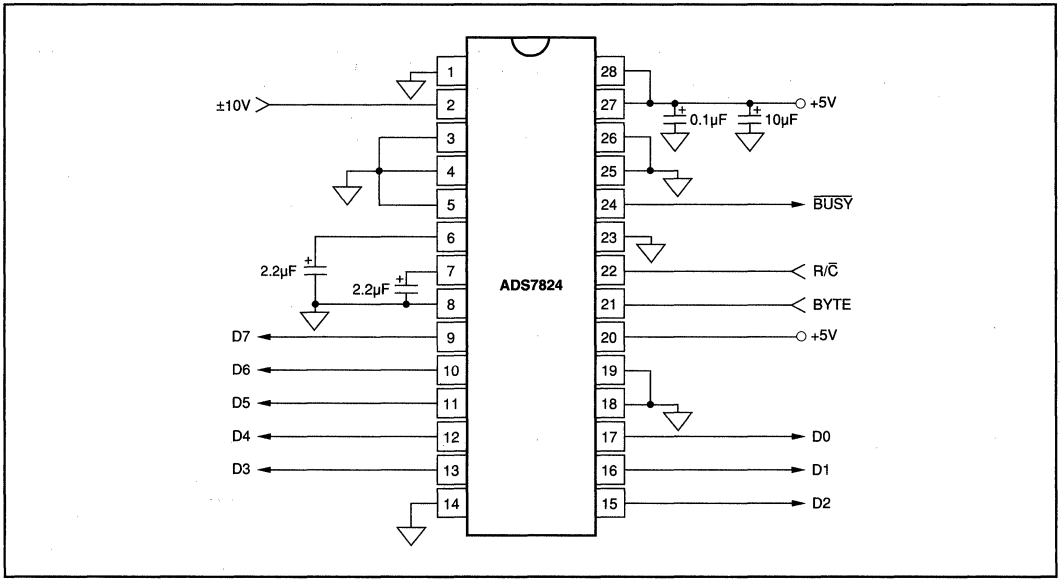


FIGURE 1. Basic Circuit Configuration.

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ADS7825

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

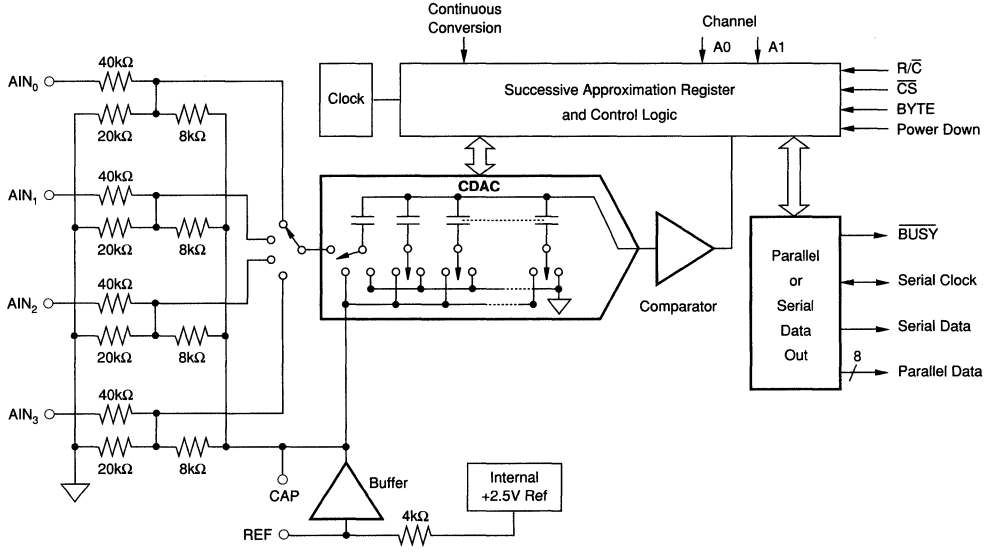
4 Channel, 16-Bit Sampling CMOS A/D Converter

FEATURES

- 25µs max SAMPLING AND CONVERSION
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7824
- PARALLEL AND SERIAL DATA OUTPUT
- 28-PIN 0.3" PLASTIC DIP AND SOIC
- ±2.0 LSB max INL
- 50mW max POWER DISSIPATION PLUS
- 50µW POWER DOWN MODE
- ±10V INPUT RANGE, FOUR CHANNEL MULTIPLEXER
- CONTINUOUS CONVERSION MODE

DESCRIPTION

The ADS7825 can acquire and convert 16 bits to within ±2.0 LSB in 25µs max while consuming only 50mW max. Laser-trimmed scaling resistors provide the standard industrial ±10V input range and channel-to-channel matching of ±0.1%. The ADS7825 is a low-power 16-bit sampling A/D with a four channel input multiplexer, S/H, clock, reference, and a parallel/serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. The 28-pin ADS7825 is available in a plastic 0.3" DIP and in a SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



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SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, $V_{S1} = V_{S2} = V_S$ = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7825P, U			ADS7825PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Range			±10V			*		V
Impedance	Channel On or Off		45.7			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Acquisition Time				5			*	µs
Multiplexer Settling Time	Includes Acquisition			5			*	µs
Complete Cycle (Acquire and Convert)				25			*	µs
Complete Cycle (Acquire and Convert)	CONTC = +5V			50			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error				±3		*	±2.0	LSB[1]
No Missing Codes		15			16			
Transition Noise[2]			0.8			*		LSB
Full Scale Error[3,4]	Internal Reference			±0.5			±0.25	%
Full Scale Error Drift	Internal Reference		±7			±5		ppm/°C
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±2			*		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Channel-to-Channel Mismatch				0.1			*	%
Power Supply Sensitivity	+4.75 < V_S < +5.25			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range[5]	f_{IN} = 1kHz	90			*			dB
Total Harmonic Distortion	f_{IN} = 1kHz			–90			*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz	83			86			dB
Signal-to-Noise	f_{IN} = 1kHz	83			86			dB
Channel Separation[6]	f_{IN} = 1kHz	100	120		*	*		dB
–3dB Bandwidth			TBD			*		MHz
Useable Bandwidth[7]			TBD			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response[8]	FS Step		5			*		µs
Overvoltage Recovery[9]			1			*		µs
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format		Parallel in two bytes; Serial				*		
Data Coding		Binary Two's Complement				*		
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_S			±5			*	µA
Output Capacitance	High-Z State			15			15	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{S1} = V_{S2} = V_S = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

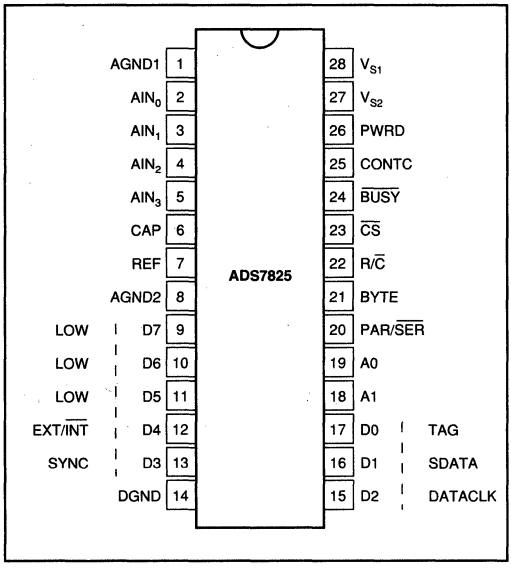
PARAMETER	CONDITIONS	ADS7825P, U			ADS7825PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	PAR/$\overline{SER}$ = +5V			83			*	ns
Bus Relinquish Time	PAR/$\overline{SER}$ = +5V			83			*	ns
Data Clock	PAR/$\overline{SER}$ = 0V							
Internal Clock (Output only when transmitting data)	EXT/$\overline{INT}$ LOW	0.5		1.5	*		*	MHz
External Clock (Can run continually)	EXT/$\overline{INT}$ HIGH	0.1		10	*		*	MHz
POWER SUPPLIES								
V_{S1} = V_{S2} = V_S		+4.75	+5	+5.25	*	*	*	V
Power Dissipation	f_S = 40kHz			50			*	mW
	PWRD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7825, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) A full scale sinewave input on one channel will be attenuated by this amount on the other channels. (7) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (8) The ADS7825 will accurately acquire any input step if given a full acquisition period after the step. (9) Recovers to specified performance after 2 x FS input overvoltage, and normal acquisitions can begin.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: AIN_0, AIN_1, AIN_2, AIN_3	±25V
REF	(AGND2 –0.3V) to (V_S + 0.3V)
CAP	Indefinite Short to AGND2, Momentary Short to V_S
V_{S1} and V_{S2} to AGND2	7V
V_{S1} to V_{S2}	±0.3V
Difference between AGND1, AGND2 and DGND	±0.3V
Digital Inputs and Outputs	–0.3V to (V_S + 0.3V)
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Maximum Input Current to Any Pin	100mA

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN #	NAME	I/O	DESCRIPTION
1	AGND1		Analog Ground. Used internally as ground reference point.
2	AIN_0		Analog Input Channel 0. Full-scale input range is ±10V. See Table I.
3	AIN_1		Analog Input Channel 1. Full-scale input range is ±10V. See Table I.
4	AIN_2		Analog Input Channel 2. Full-scale input range is ±10V. See Table I.
5	AIN_3		Analog Input Channel 3. Full-scale input range is ±10V. See Table I.
6	CAP		Internal Reference Output Buffer. 2.2µF Tantalum to ground.
7	REF		Reference Input/Output. Outputs +2.5V nominal. If used externally, must be buffered to maintain ADS7825 accuracy. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
8	AGND2		Analog Ground.
9	D7	O	Parallel Data Bit 7 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
10	D6	O	Parallel Data Bit 6 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
11	D5	O	Parallel Data Bit 5 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
12	D4	I/O	Parallel Data Bit 4 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, a LOW level input here will transmit serial data on SDATA from the previous conversion using the internal clock; a HIGH input here will transmit serial data using an external clock input on DATACLK. See Table II.
13	D3	O	Parallel Data Bit 3 if PAR/$\overline{SER}$ HIGH; LOW if PAR/$\overline{SER}$ LOW. See Table II.
14	DGND		Digital Ground.
15	D2	I/O	Parallel Data Bit 2 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, this will output the internal conversion clock if a LOW is input on D4; will be an input for an external data transmission clock if D4 is HIGH. See Table II.
16	D1	O	Parallel Data Bit 1 if PAR/$\overline{SER}$ HIGH; SDATA serial data output if PAR/$\overline{SER}$ LOW. See Table II.
17	D0	I/O	Parallel Data Bit 0 if PAR/$\overline{SER}$ HIGH; TAG data input if PAR/$\overline{SER}$ LOW. See Table II.
18	A1	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table II.
19	A2	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table II.
20	PAR/$\overline{SER}$	I	Select Parallel or Serial Output. If HIGH, parallel data will be output on D0 thru D7. If LOW, serial data will be output on SDATA. See Table II.
21	BYTE	I	Byte Select. Only used with parallel data, when PAR/$\overline{SER}$ HIGH. Determines which byte is available on D0 thru D7. Changing BYTE with $\overline{CS}$ LOW and R/$\overline{C}$ HIGH will cause the data bus to change accordingly. LOW selects the 8 MSBs; HIGH selects the 8 LSBs.
22	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH.
23	$\overline{CS}$	I	Chip Select. Internally OR'd with R/$\overline{C}$. With CONTC LOW and R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH.
24	$\overline{BUSY}$	O	Busy Output. Falls when conversion is started; remains LOW until the conversion is completed and the data is latched into the output register. In parallel output mode or in internal clock serial mode, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
25	CONTC	I	Continuous Conversion Input. If LOW, conversions will occur normally when initiated using $\overline{CS}$ and R/$\overline{C}$; if HIGH, acquisition and conversions will take place continually, cycling through all four input channels, as long as $\overline{CS}$, R/$\overline{C}$ and PWRD are LOW. See Table II.
26	PWRD	I	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output register. In the continuous conversion mode, the multiplexer address channel is reset to channel 0
27	V_{S2}		Supply Input. Nominally +5V. Connect directly to pin 27. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
28	V_{S1}		Supply Input. Nominally +5V. Connect directly to pin 28.

ADS7825 TIMING AND CONTROL

A1	A0	CHANNEL SELECTED	DESCRIPTION OF OPERATION
0	0	AIN_0	Channel to be converted during conversion n + 1 is latched when conversion n is initiated. The selected input starts being acquired as soon as conversion n is done.
0	1	AIN_1	
1	0	AIN_2	
1	1	AIN_3	

TABLE Ia. A0 and A1 Inputs (CONTC LOW.)

A1	A0	DATA AVAILABLE FROM CHANNEL	CHANNEL TO BE OR BEING CONVERTED	DESCRIPTION OF OPERATION
0	0	AIN_3	AIN_0	Channel being acquired or converted is output on these address lines. Data is valid for the previous channel. These lines are updated when $\overline{BUSY}$ rises.
0	1	AIN_0	AIN_1	
1	0	AIN_1	AIN_2	
1	1	AIN_2	AIN_3	

TABLE Ib. A0 and A1 Outputs (CONTC HIGH.)

INPUTS						OUTPUTS								
$\overline{CS}$	R/$\overline{C}$	BYTE	CONTC	PWRD	$\overline{BUSY}$	D7	D6	D5	D4	D3	D2	D1	D0	COMMENTS
1	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
X	0	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
0	1	0	X	X	X	B11 (MSB)	B10	B9	B8	B7	B6	B5	B4	Results from last completed conversion.
0	1	1	X	X	X	B3	B2	B1	B0 (LSB)	LOW	LOW	LOW	LOW	Results from last completed conversion.
0	1	X	X	X	↑	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	↑↓	Data will change at the end of a conversion.

TABLE IIa. Read Control for Parallel Data (PAR/SER = 5V.)

$\overline{CS}$	R/$\overline{C}$	CONTC	PWRD	$\overline{BUSY}$	D7, D6, D5 LOW	D4 EXT/$\overline{INT}$	D3 SYNC	D2 DATACLK	D1 SDATA	D0 TAG	COMMENTS
Input	Input	Input	Input	Output	Output	Input	Output	I/O	Output	Input	
1	X	X	X	X	Hi-Z	LOW	Hi-Z	Output, Hi-Z	Hi-Z	X	
X	0	X	X	X	Hi-Z	LOW	Hi-Z	Output, Hi-Z	Hi-Z	X	
0	↓	0	X	1	LOW	LOW	LOW	Output	Output	X	Starts transmission of data from previous conversion on SDATA synchronized to 16 pulses output on DATACLK.
↓	0	0	X	1	LOW	LOW	LOW	Output	Output	X	Starts transmission of data from previous conversion on SDATA synchronized to 16 pulses output on DATACLK.
0	1	0	X	X	LOW	HIGH	LOW	Input	Output	Input	The level output on SDATA will be the level input on TAG 16 DATACLK input cycles earlier.
0	1	0	X	↑	LOW	HIGH	LOW	Input	Output	Input	At the end of the conversion, when $\overline{BUSY}$ rises, data from the conversion will be shifted into the output registers. If a clock is being input on DATACLK, valid data will be lost.
0	↑	0	X	1	LOW	HIGH	LOW	Input	Output	X	Initiates transmission of a HIGH pulse on SYNC followed by data from last completed conversion on SDATA synchronized to the input on DATACLK.
↓	1	0	X	1	LOW	HIGH	LOW	Input	Output	X	Initiates transmission of a HIGH pulse on SYNC followed by data from last completed conversion on SDATA synchronized to the input on DATACLK.
0	0	1	0	↓	LOW	LOW	LOW	Output	Output	X	Starts transmission of data from previous conversion on SDATA synchronized to 16 pulses output on DATACLK
↓	1	X	X	X	LOW	HIGH	Output	Input	Output	X	SDATA becomes active. Inputs on DATACLK shift out data.
0	↑	X	X	X	LOW	HIGH	Output	Input	Output	X	SDATA becomes active. Inputs on DATACLK shift out data.
↓	0	1	X	X	LOW	LOW	LOW	Output	Output	X	Restarts continuous conversion mode. Data starts being transmitted when $\overline{BUSY}$ next rises.
0	↓	1	X	X	LOW	LOW	LOW	Output	Output	X	Restarts continuous conversion mode. Data starts being transmitted when $\overline{BUSY}$ next rises.

TABLE IIb. Read Control for Serial Data (PAR/SER = 0V.)

CONTC	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	PWRD	A0 and A1	OPERATION
0	X	X	X	X	Inputs	Initiating conversion n latches in the levels input on A0 and A1 to select the channel for conversion n + 1
0	X	X	0	0	Inputs	Conversion in process. New convert commands ignored.
0	0	↓	1	0	Inputs	Initiates conversion on channel selected at start of previous conversion.
0	↓	0	1	0	Inputs	Initiates conversion on channel selected at start of previous conversion.
0	X	X	X	1	Inputs	All analog functions powered down. Conversions in process or initiated will yield meaningless data.
1	X	X	X	X	Outputs	The end of conversion n (when $\overline{BUSY}$ rises) increments the internal channel latches and outputs the channel address for conversion n + 1 on A0 and A1.
1	X	X	0	0	Outputs	Conversion in process
1	0	↓	1	0	Outputs	Restarts continuous conversion process on next input channel.
1	↓	0	1	0	Outputs	Restarts continuous conversion process on next input channel.
1	X	X	X	1	Outputs	All analog functions powered down. Conversions in process or initiated will yield meaningless data. Resets selected input channel for next conversion to IN_0.

TABLE III. Conversion Control.

BASIC OPERATION

Figure 1 shows the simple circuit required to operate the ADS7825, converting a single input channel. Taking R/$\overline{C}$ (pin 22) LOW for a minimum of 40ns will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the output registers are updated. With BYTE (pin 21) in the LOW state, the eight MSB's will be output in Binary Two's Complement with the MSB (BIT 15) at pin 9. By bringing BYTE HIGH, the eight LSB's will be output with the LSB (BIT 0) at pin 17 (See Table IIa). $\overline{BUSY}$ going HIGH can be used to latch the MSB data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

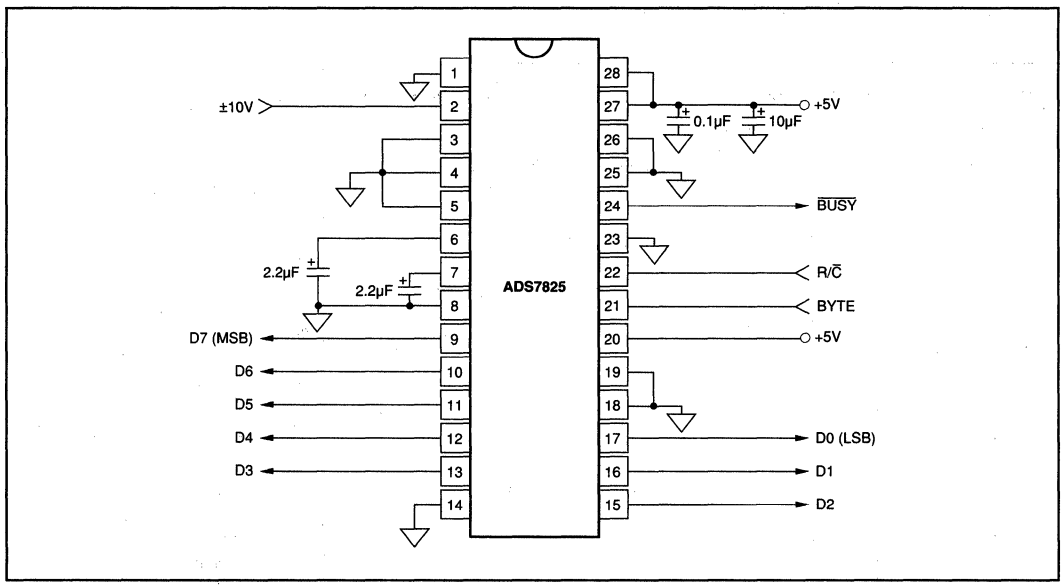


FIGURE 1. Basic Circuit Configuration.

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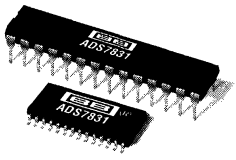


ADS7831

12-Bit 600kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- 600kHz THROUGHPUT RATE
- STANDARD ±2.5V INPUT RANGE
- 69dB min SINAD WITH 250kHz INPUT
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/LATCHES
- FULLY SPECIFIED –40°C TO +85°C
- 15MHz –3dB BANDWIDTH
- 28-PIN 0.3" PDIP AND SOIC

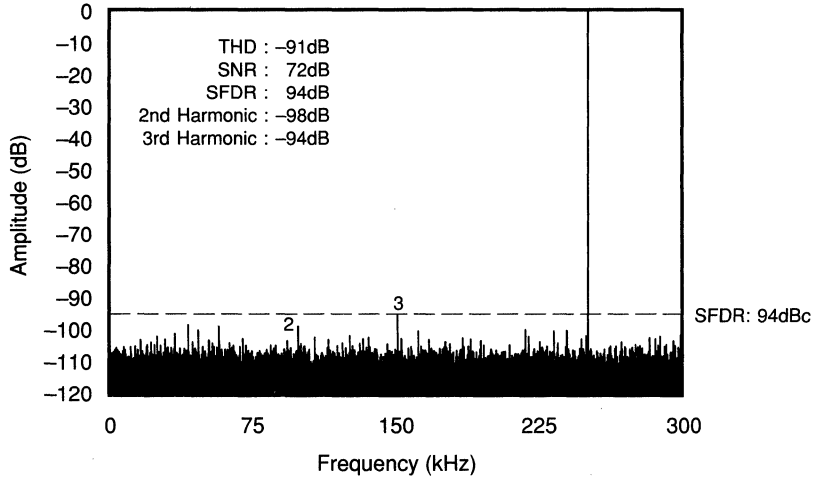
DESCRIPTION

The ADS7831 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7831 is specified at a 600kHz sampling rate, and guaranteed over the full temperature range. A ±2.5V input range and excellent Nyquist performance provide an optimum solution in ±5V supply systems.

The 28-pin ADS7831 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

FREQUENCY SPECTRUM
(16384 Point FFT; f_{IN} = 250kHz, –0.5dB)



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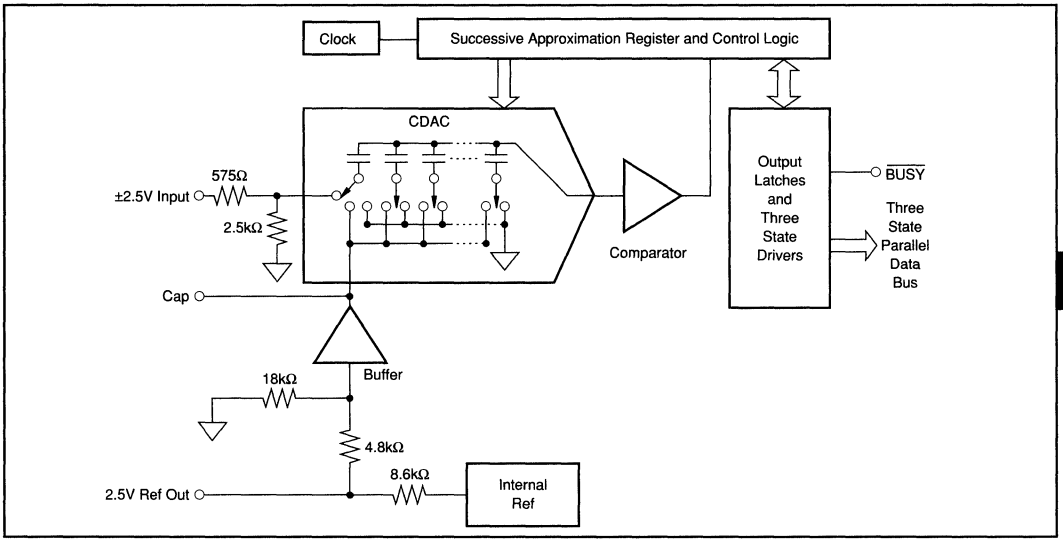
SPECIFICATIONS

At T_A = –40°C to +85°C, f_S = 600kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7831P, U MIN	ADS7831P, U TYP	ADS7831P, U MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Range			±2.5		V
Impedance			3.1		kΩ
Capacitance			5		pF
THROUGHPUT SPEED					
Conversion Time			1.3		µs
Complete Cycle	Acquire & Convert			1.66	µs
Throughput Rate		600			kHz
DC ACCURACY					
Integral Linearity Error				±1	LSB(1)
Differential Linearity Error				±1	LSB
No Missing Codes			Guaranteed		
Total Unadjusted Error(2, 3)				±10	LSB
(Includes Bipolar Zero Error and Full Scale Error)					
Power Supply Sensitivity					
($+V_{DIG} = +V_{ANA} = V_D$)	+4.75V < V_D < +5.25V –5.25V < $-V_{ANA}$ < –4.75V			±5	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 250kHz	77	87		dB(4)
Total Harmonic Distortion	f_{IN} = 250kHz		–85	–77	dB
Signal-to-(Noise+Distortion)	f_{IN} = 250kHz	69	71		dB
Signal-to-Noise	f_{IN} = 250kHz	69	72		dB
Usable Bandwidth(5)			1.6		MHz
Full-Power Bandwidth			15		MHz
SAMPLING DYNAMICS					
Aperture Delay			20		ns
Aperture Jitter			10		ps
Transient Response	FS Step		200		ns
Overvoltage Recovery(6)			250		ns
REFERENCE					
Reference Voltage		2.45	2.5	2.55	V
Reference DC Source Current			100		µA
(External load should be static)					
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.4		V_D + 0.3	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA
DIGITAL OUTPUTS					
Data Format			Parallel 12-bits		
Data Coding			Binary Two's Complement		
V_{OL}	I_{SINK} = 1.6mA			+0.4	V
V_{OH}	I_{SOURCE} = 500µA	+2.8			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5	µA
Output Capacitance	High-Z State			15	pF
DIGITAL TIMING					
Bus Access Time				62	ns
Bus Relinquish Time				83	ns
POWER SUPPLIES					
Specified Performance					
$+V_{DIG} = +V_{ANA}$		+4.75	+5	+5.25	V
$-V_{ANA}$		–5.25	–5	–4.75	V
$+I_{DIG}$			+16		mA
$+I_{ANA}$			+16		mA
$-I_{ANA}$			–12		mA
Power Dissipation	f_S = 600kHz		220	275	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance (θ_{JA})					
Plastic DIP			75		°C/W
SOIC			75		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±2.5V input ADS7831, one LSB is 1.22mV. (2) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometers. (3) Total unadjusted error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. (4) All specifications in dB are referred to a full-scale ±2.5V input. (5) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. 6) Recovers to specified performance after 2 x FS input over voltage.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	±25V
REF	$+V_{ANA}$ +0.3V to AGND2 –0.3V
CAP	Indefinite Short to AGND2
	Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
$+V_{ANA}$	+7V
$+V_{DIG}$ to $+V_{ANA}$	+0.3V
$+V_{DIG}$	7V
$-V_{ANA}$	–7V
Digital Inputs	–0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

PACKAGE AND ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7831P	28-Pin Plastic DIP	246
ADS7831U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

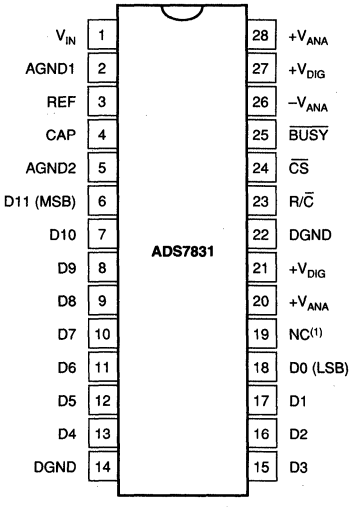
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN ASSIGNMENTS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V.
2	AGND1		Analog Ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor.
4	CAP		Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V.
5	AGND2		Analog Ground.
6	D11 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
7	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
8	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
9	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
10	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
11	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
12	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
13	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
14	DGND		Digital Ground.
15	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
16	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
17	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
18	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
19			Not internally connected.
20	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28.
21	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28.
22	DGND		Digital ground.
23	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits.
24	$\overline{CS}$	I	Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits.
25	$\overline{BUSY}$	O	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
26	$-V_{ANA}$		Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
27	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28.
28	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.

PIN CONFIGURATION

Top View **DIP/SOIC**

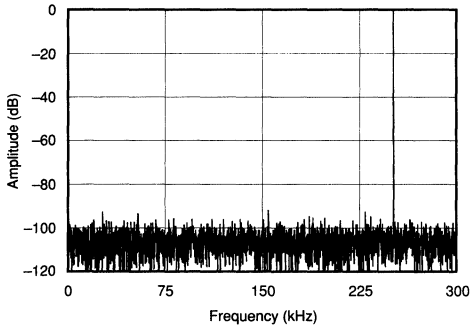


NOTE: (1) Not Internally Connected.

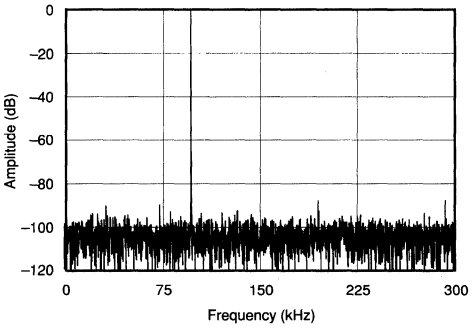
TYPICAL PERFORMANCE CURVES

T = +25°C, f_S =600kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

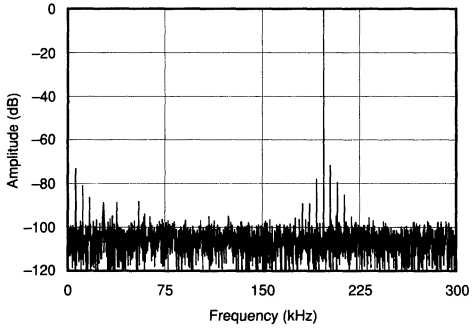
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 252kHz, –0.5dB)



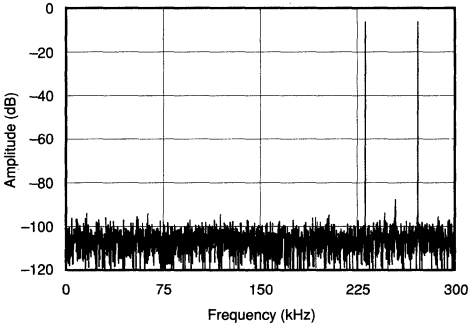
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 502kHz, –0.5dB)



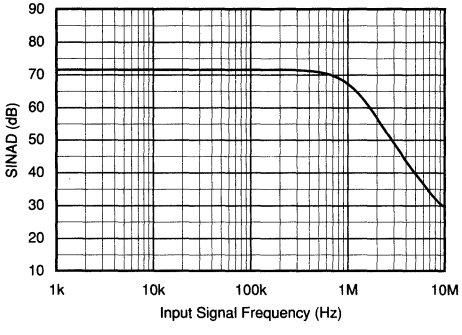
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1.002MHz, –0.5dB)



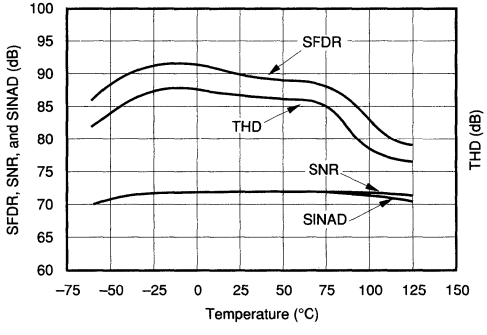
FREQUENCY SPECTRUM
(4096 Point FFT; $f1_{IN}$ = 232kHz, –6.5dB;
$f2_{IN}$ = 272kHz, –6.5dB)



SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = –0.5dB)

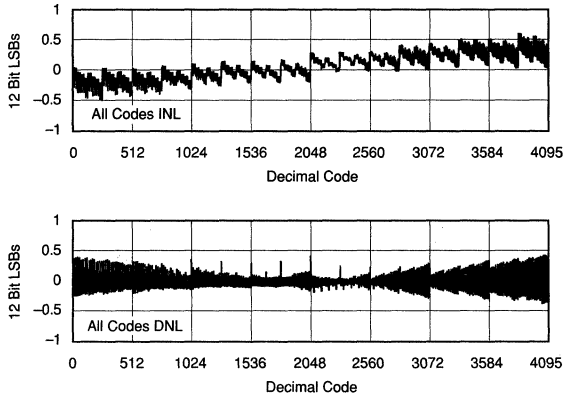


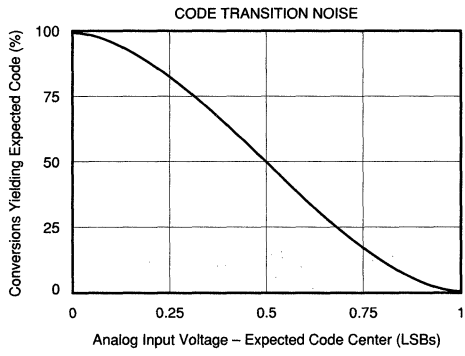
A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 250kHz, –0.5dB)

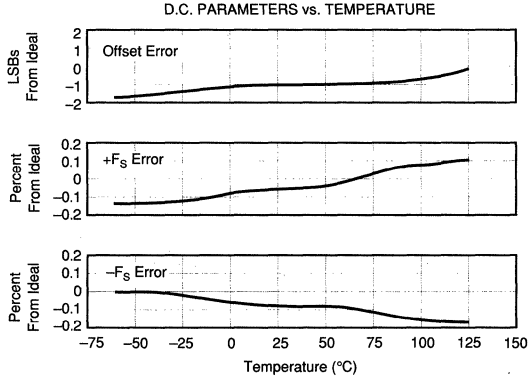


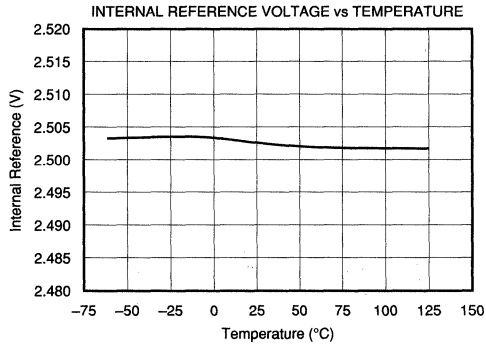
TYPICAL PERFORMANCE CURVES (CONT)

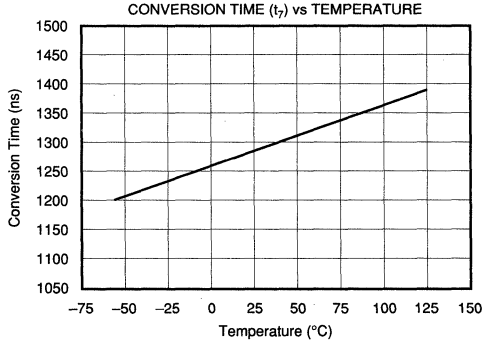
T = +25°C, f_S =600kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.











BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7831. Taking R/$\overline{C}$ (pin 23) LOW for 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on D11 (pin 6). $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7831 will begin tracking the input signal at the end of the conversion. Allowing 1.66µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7831 in the hold state and starts a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7831 will begin tracking the input signal at the end of the conversion. Allowing 1.66µs between convert commands assures accurate acquisition of a new signal. Refer to Table I for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 and 3 for timing parameters.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the **Reading Data** section and refer to Table I for control line functions for 'read' and 'convert' modes.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	↑	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register, but the output pins D11-D0 remain tri-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table I. Control Line Functions for 'read' and 'convert'.

DESCRIPTION	ANALOG INPUT	DIGITAL INPUT	
Full Scale Range	±2.5V	BINARY TWO'S COMPLEMENT	
Least Significant Bit (LSB)	1.22mV	BINARY CODE	HEX CODE
+Full Scale (2.5V – 1LSB)	2.499V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–1.22mV	1111 1111 1111	FFF
–Full Scale	–2.5V	1000 0000 0000	800

TABLE II. Ideal Input Voltages and Output Codes.

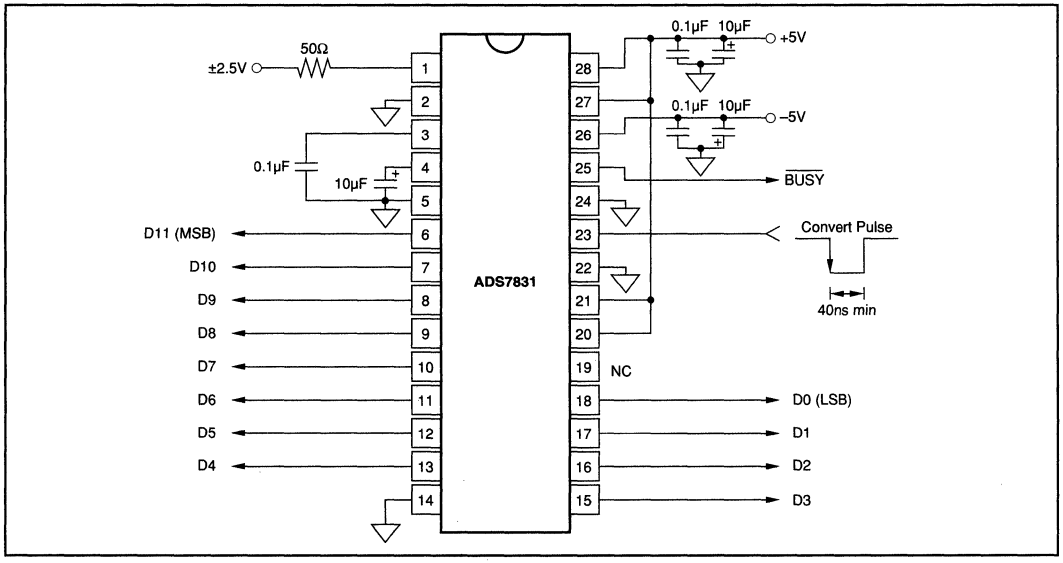


FIGURE 1. Basic Operation

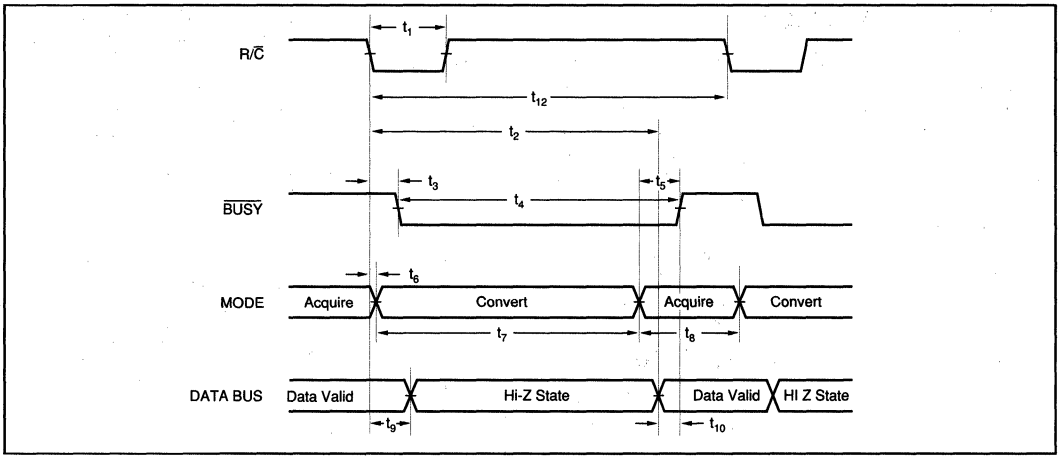


FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

READING DATA

The ADS7831 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on D11-D0 (pins 6-13 and 15-18). Refer to Table II for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table III and Figures 2 and 3.

Note: For best performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feed through degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

ANALOG INPUT

The ADS7831 has a ±2.5V input range. Figures 4a and 4b show the necessary circuit connections for the ADS7831 with and without external trim. Offset and full scale error(1) specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4b. This external resistor makes it possible to trim the offset ±12mV using R_1 and P_1 as shown in Figure 4a. This resistor may be left out if the offset and gain errors will be corrected in software or if they are negligible in regards to the particular application. See the **Calibration** section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on page 3 of this data sheet and the external 50Ω resistor. The input resistor divider network provides inherent over-voltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

Note: The values shown for the internal resistors are for reference only. The exact values can vary by ±30%. This is true of all resistors internal to the ADS7831. Each resistive divider is trimmed so that the proper division is achieved.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	Data Valid Delay After Start of Conversion		1310	1460	ns
t_3	$\overline{BUSY}$ Delay From Start of Conversion		75	125	ns
t_4	$\overline{BUSY}$ LOW		1300	1440	ns
t_5	$\overline{BUSY}$ Delay After End of Conversion		90		ns
t_6	Aperture Delay		20		ns
t_7	Conversion Time		1285	1400	ns
t_8	Acquisition Time		200	250	ns
t_7 & t_8	Throughput Time		1485	1650	ns
t_9	Bus Relinquish Time	10	55	83	ns
t_{10}	$\overline{BUSY}$ Delay After Data Valid	20	65	100	ns
t_{11}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{12}	Time Between Conversions	1660			ns
t_{13}	Bus Access Time	10	30	62	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

CALIBRATION

The ADS7831 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain.

Hardware Calibration

To calibrate the offset and gain of the ADS7831, install the proper resistors and potentiometers as shown in Figure 4a. The calibration range is ±12mV for the offset and ±30mV for full scale.

Potentiometer P_1 and resistor R_1 form the offset adjust circuit and P_2 and R_2 the gain adjust circuit. The exact values are not critical. R_1 and R_2 should not be made any larger than the value shown. They can easily be made smaller to provide increased adjustment range. Reducing these below 15% of the indicated values could begin to adversely affect the operation of the converter.

P_1 and P_2 can also be made larger to reduce power dissipation. However, larger resistances will push the useful adjustment range to the edges of the potentiometer. P_1 should probably not exceed 20kΩ and P2 100kΩ in order to maintain reasonable sensitivity.

Software Calibration or No Calibration

The ADS7831 does not require external resistors for its basic operation. However, the component is designed to be used with an external 50Ω resistor on the input, and the specifications apply to this condition. If this resistor is not used, the only specification that will be affected is total unadjusted error.

With the 50Ω resistor, the nominal input voltage range is ±2.5V and the total unadjusted error is ±10LSBs guaranteed. Without the 50Ω resistor, the nominal input voltage range will be ±2.46V and the total unadjusted error is not guaranteed. While it will typically be much less, the total unadjusted error could be as high as ±20LSBs.

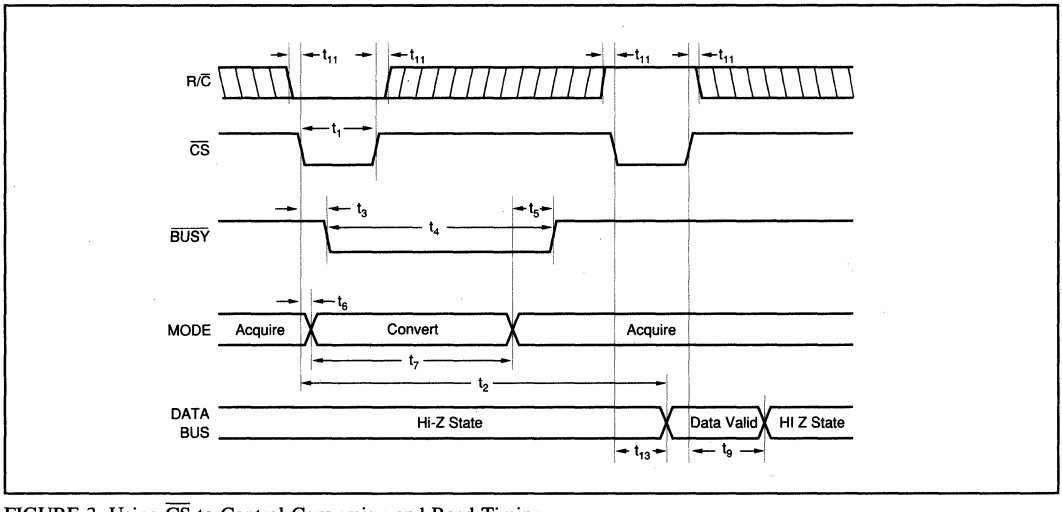


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

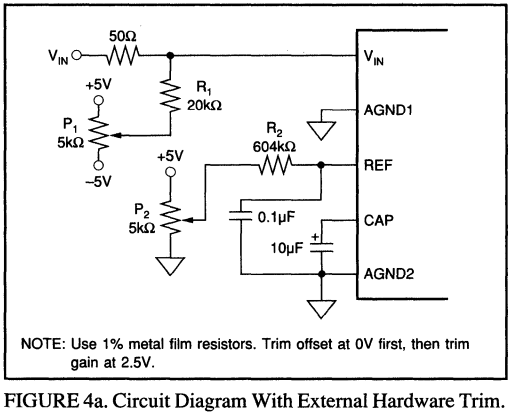


FIGURE 4a. Circuit Diagram With External Hardware Trim.

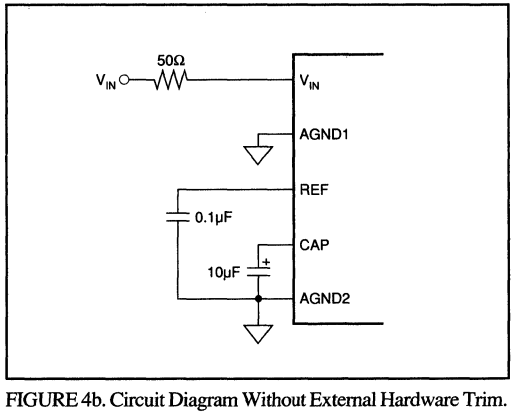


FIGURE 4b. Circuit Diagram Without External Hardware Trim.

REFERENCE

REF

REF (pin 3) is the output for the internal 2.5V reference. A 0.1µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 10µF capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 2.2µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 10µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

The ADS7831 uses the majority of its power for analog and static circuitry and it should be considered as an analog component. For optimum performance, tie the analog and digital +5V power pins to the same +5V power supply and tie the analog and digital grounds together.

For best performance, the ±5V supplies can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If ±12V or ±15V supplies are present, simple regulators can be used. The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic.

Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7831. DGND (pin 22) is the digital supply ground. AGND2 (pin 5) is the analog supply ground. AGND1 (pin 2) is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7831, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7831.

The resistive front end of the ADS7831 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7831 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7831 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

BURR-BROWN®

ADS7833

10-Channel, 12-Bit DATA ACQUISITION SYSTEM

FEATURES

- 3 SIMULTANEOUS SAMPLED CHANNELS
- 3 SYNCHRONIZED 12-BIT ADCs
- 6.6µs THROUGHPUT RATE
- FULLY DIFFERENTIAL MUX INPUTS
- DIGITALLY SELECTABLE INPUT RANGES
- ±5V POWER SUPPLIES
- SERIAL DIGITAL INPUT/OUTPUTS
- 2 SIMULTANEOUS SAMPLED AUXILIARY CHANNELS
- DIRECT INTERFACE TO MOTOROLA'S DSP56004/7

APPLICATIONS

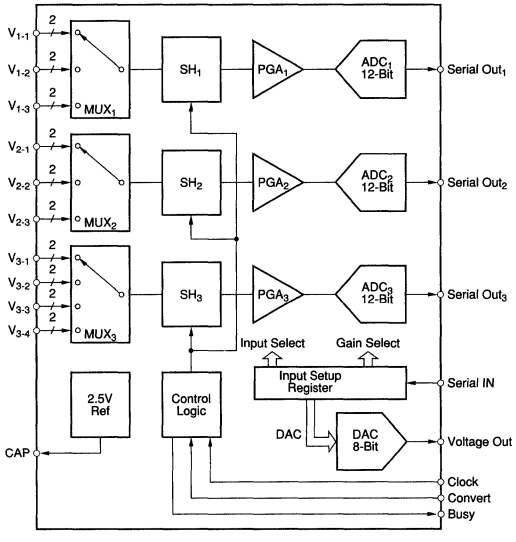
- AC MOTOR SPEED CONTROLS
- THREE PHASE POWER CONTROL
- UNINTERRUPTABLE POWER SUPPLIES
- VIBRATION ANALYSIS
- PC DATA ACQUISITION
- MEDICAL INSTRUMENTATION

DESCRIPTION

The ADS7833 consists of three 12-bit analog-to-digital converters preceded by three simultaneously operating sample-hold amplifiers, and multiplexers for 10 differential inputs. The ADCs have simultaneous serial outputs for high speed data transfer and data processing.

The ADS7833 also offers a programmable gain amplifier with programmable gains of 1.0V/V, 1.25V/V, 2.5V/V, and 5.0V/V. Channel selection and gain selection are selectable through the serial input control word. The high through put rate is maintained by simultaneously clocking in the 13-bit input control word for the next conversion while the present conversions are clocked out.

The part also contains an 8-bit digital-to-analog converter whose digital input is supplied as part of the input control word.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, and T_A = –40°C to +85°C, using internal reference, f_{CLOCK} = 2.1MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	ADS7833N MIN	ADS7833N TYP	ADS7833N MAX	UNITS
RESOLUTION		12			Bit
ANALOG INPUT					
Full Scale Voltage, Differential	G = 1.0V/V		±2.5		V
	G = 1.25V/V		±2.0		V
	G = 2.5V/V		±1.0		V
	G = 5.0V/V		±0.5		V
Common-Mode Voltage		±0.5	See Table VII		V
Impedance			10^{12}		Ω
Capacitance			20		pF
THROUGHPUT SPEED					
Conversion Time	CLK = 2.1MHz			6.1	µs
Complete Cycle	Acquire and Convert			6.6	µs
Throughput Rate		150	200		kHz
SAMPLING DYNAMICS					
S/H Droop Rate			0.1		µV/µs
S/H Acquisition Time			0.5		µs
S/H Aperture Delay			50		ns
S/H Aperture Jitter			50		ps
Sampling Skew, Channel-to-Channel			3		ns
DC ACCURACY					
Integral Linearity - Synchronous			±0.5	±2	LSB
Differential Linearity - Synchronous			±0.5		LSB
No Missing Codes		12			Bits
Integral Linearity - Asynchronous			0.5	±3	LSB
Differential Linearity - Asynchronous			0.5	±3	LSB
Full Scale Error	G = 1.0V/V			2	% of FSR
Full Scale Error Other Gains				4	% of FSR
Full Scale Error Drift	G = 1.0V/V		±10	±100	ppm/°C
	G = 2.5V/V		±10	±100	ppm/°C
Zero Error - Synchronous	G = 1.0V/V		±0.5	±15	LSB
Zero Error - Asynchronous			±0.5	±20	LSB
Zero Error Drift	G = 1.0V/V		±0.5		ppm/°C
AC ACCURACY					
Total Harmonic Distortion					
f_{IN} = 1kHz			92		dB
f_{IN} = 1MHz			72		dB
CMR	V_{CM} = 1V, f_{CM} = 1MHz		40		dB
REFERENCE					
Internal Reference Voltage			2.5		V
Internal Reference Accuracy			±0.25		%
Internal Reference Drift			±10		ppm/°C
Internal Reference Source Current			10		µA
External Reference Voltage Range for Specified Linearity		2.25	2.5	2.75	V
External Reference Current Drain			10		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		0		1.5	V
V_{IH}		+3.5		+5	V
I_{IL}				±10	µA
I_{IH}				±10	µA
Input Capacitance	At All Digital Input Pins			15	pF
DIGITAL OUTPUTS					
Data Format			12-Bit Serial		
Data Coding			BTC		
V_{OL}	I_{SINK} = 1.6mA	0		0.4	V
V_{OH}	I_{SOURCE} = 500µA	4.2		5	V
Leakage Current				±5	µA
Output Capacitance	At All Digital Output Pins			15	pF

SPECIFICATIONS (CONT)

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V, and T_A = –40°C to +85°C, using internal reference, f_{CLOCK} = 2.1MHz.

ANALOG-TO-DIGITAL CONVERTER CHANNELS

PARAMETER	CONDITIONS	ADS7833N MIN	ADS7833N TYP	ADS7833N MAX	UNITS
POWER SUPPLIES	Specified Performance				
V_{ANA+}		+4.75	+5.0	+5.25	V
V_{ANA-}		–4.75	–5.0	–5.25	V
V_{DIG+}		+4.75	+5.0	+5.25	V
V_{DIG-}		–4.75	–5.0	–5.25	V
I_{ANA+}			15	25	mA
I_{ANA-}			8	10	mA
I_{DIG+}			3	5	mA
I_{DIG-}			1	2	mA
Power Dissipation			125		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Derated Performance		–55		+125	°C
Storage		–65		+150	°C

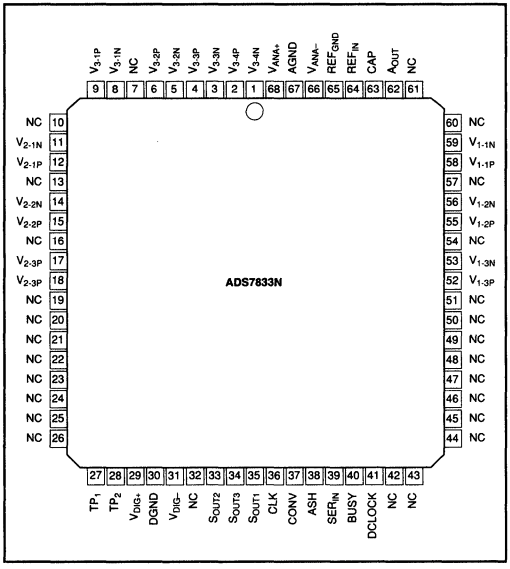
DIGITAL-TO-ANALOG CONVERTER

PARAMETER	CONDITIONS	ADS7833N MIN	ADS7833N TYP	ADS7833N MAX	UNITS
RESOLUTION		8-Bits			
Output Range		0		+2.5	V
Output Settling Time	To 0.5LSB			1	µs
Linearity Error				±1	LSB
Differential Linearity				±1	LSB
Output Current		200			
Offset Error			±1	10	mV
Full Scale Error				2	%

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage	±25V
Ground Voltage Difference: AGND and DGND	±0.3V
Power Supply Voltages:	
V_{ANA+}	+7V
V_{ANA-}	–7V
V_{DIG+}	+7V
V_{DIG-}	–7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

PIN CONFIGURATION



CONVERSION AND DATA TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	A/D Conversion Time	6.6	4.0		µs
CLK	A/D Conversion Clock	2.1	2.8		MHz
t_1	Setup Time for Conversion Before Rising Edge of Clock	50			ns
t_2	Hold Time for Conversion After Rising Edge of Clock	50			ns
t_3	Setup Time for Serial Out			25	ns
t_4	Setup Time for Serial Input	30			ns
t_5	Hold Time for Serial Input	30			ns

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7833N	68 Lead PLCC	312

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

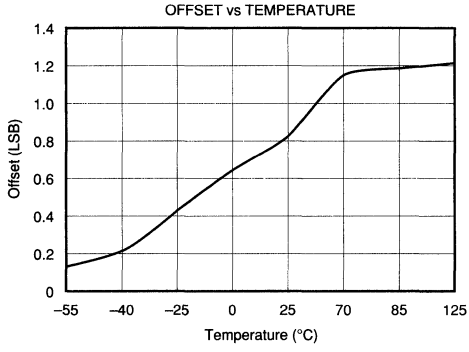
PIN DEFINITIONS

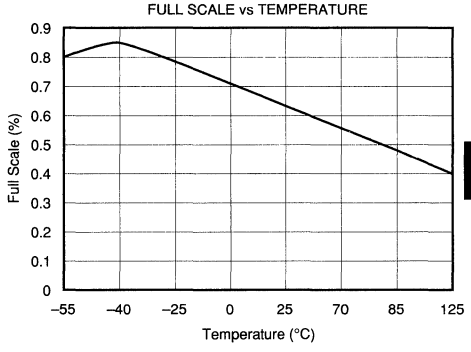
PIN NO	NAME	TYPE[1]	DESCRIPTION	PIN NO	NAME	TYPE[1]	DESCRIPTION
1	V_{3-4N}	AI	Voltage Input, Channel 3, Mux I/P 4, Negative Side	35	S_{OUT1}	DO	Serial Digital Output, Channel 1
				36	CLK	DI	Clock for A/D Converters
2	V_{3-4P}	AI	Voltage Input, Channel 3, Mux IP 4, Positive Side	37	CONV	DI	Start A/D Converters. When CONV goes to "0" (low) the next rising edge of CLK starts the conversion.
3	V_{3-3N}	AI	Voltage Input, Channel 3, Mux I/P 3, Negative Side	38	ASH	DI	Digital Control for Asynchronous Sample Hold. If signal is "1" (high), signals are sampled.
4	V_{3-3P}	AI	Voltage Input, Channel 3, Mux I/P 3, Positive Side				
5	V_{3-2N}	AI	Voltage Input, Channel 3, Mux I/P 2, Negative Side	39	SER_{IN}	DI	Serial Digital Input for Input Control Word
				40	BUSY	DO	A/D Converters Busy. Busy if signal is "0" (low).
6	V_{3-2P}	AI	Voltage Input, Channel 3, Mux I/P 2, Positive Side	41	DCLOCK	DO	A Delayed and Truncated Version of the CLK Signals. It is Delayed 50ns from the CLK Signal and Stays Low after 13 DCLOCK Cycles.
7	NC	—	No Connection				
8	V_{3-1N}	AI	Voltage Input, Channel 3, Mux I/P 1, Negative Side				
				42	NC	—	No Connection
9	V_{3-1P}	AI	Voltage Input, Channel 3, Mux I/P 1, Positive Side	43	NC	—	No Connection
				44	NC	—	No Connection
10	NC	—	No Connection	45	NC	—	No Connection
11	V_{2-1N}	AI	Voltage Input, Channel 2, Mux I/P 1, Negative Side	46	NC	—	No Connection
				47	NC	—	No Connection
12	V_{2-1P}	AI	Voltage Input, Channel 2, Mux I/P 1, Positive Side	48	NC	—	No Connection
				49	NC	—	No Connection
13	NC	—	No Connection	50	NC	—	No Connection
14	V_{2-2N}	AI	Voltage Input, Channel 2, Mux I/P 2, Negative Side	51	NC	—	No Connection
				52	V_{1-3P}	AI	Voltage Input, Channel 1, Mux I/P 3, Positive Side
15	V_{2-2P}	AI	Voltage Input, Channel 2, Mux I/P 2, Positive Side	53	V_{1-3N}	AI	Voltage Input, Channel 1, Mux I/P 3, Negative Side
16	NC	—	No Connection				
17	V_{2-3N}	AI	Voltage Input, Channel 2, Mux I/P 3, Negative Side.	54	NC	—	No Connection
				55	V_{1-2P}	AI	Voltage Input, Channel 1, Mux I/P 2, Positive Side
18	V_{2-3P}	AI	Voltage Input, Channel 2, Mux I/P 3, Positive Side	56	V_{1-2N}	AI	Voltage Input, Channel 1, Mux I/P 2, Negative Side
19	NC	—	No Connection				
20	NC	—	No Connection	57	NC	—	No Connection
21	NC	—	No Connection	58	V_{1-1P}	AI	Voltage Input, Channel 1, Mux I/P 1, Positive Side
22	NC	—	No Connection				
23	NC	—	No Connection	59	V_{1-1N}	AI	Voltage Input, Channel 1, Mux I/P 1, Negative Side
24	NC	—	No Connection				
25	NC	—	No Connection	60	NC	—	No Connection
26	NC	—	No Connection	61	NC	—	No Connection
27	TP1	—	Test Point 1, Make No Connection	62	A_{OUT}	AO	Output of DAC
28	TP2	—	Test Point 2, Make No Connection	63	CAP	AO	Decoupling Point for Internal Reference
29	V_{DIG+}	P	Digital Supply Voltage, +5V	64	REF_{IN}	AI	Input Pin for External Reference
30	DGND	P	Digital Supply Voltage, Ground	65	REF_{GND}	P	Ground Pin for External Reference
31	V_{DIG-}	P	Digital Supply Voltage, –5V	66	V_{ANA-}	P	Analog Supply Voltage, –5V
32	NC	—	No Connection	67	AGND	P	Analog Supply Voltage, Ground
33	S_{OUT2}	DO	Serial Digital Output, Channel 2	68	V_{ANA+}	P	Analog Supply Voltage, +5V
34	S_{OUT3}	DO	Serial Digital Output, Channel 3				

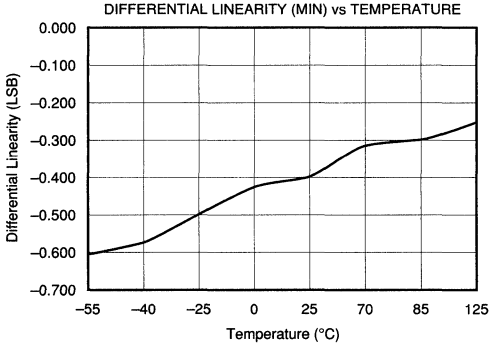
NOTE: (1) AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, P is Power Supply Connection.

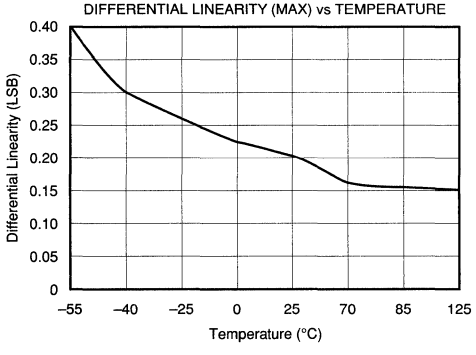
TYPICAL PERFORMANCE CURVES

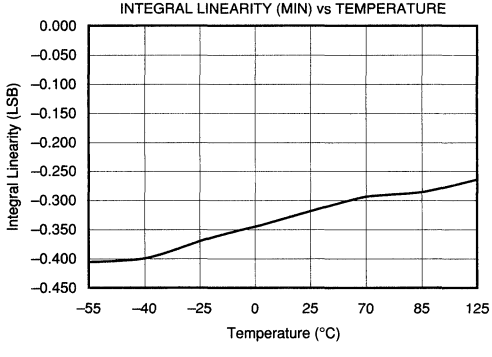
At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V and T_A = 25°C, using internal reference, f_{CLOCK} = 2.1MHz.

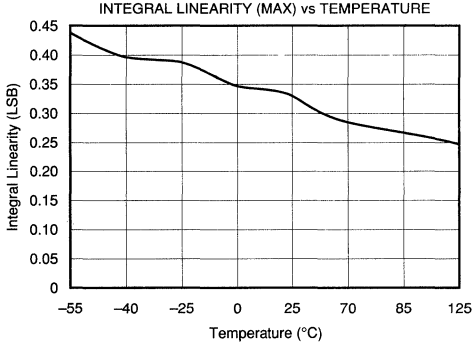






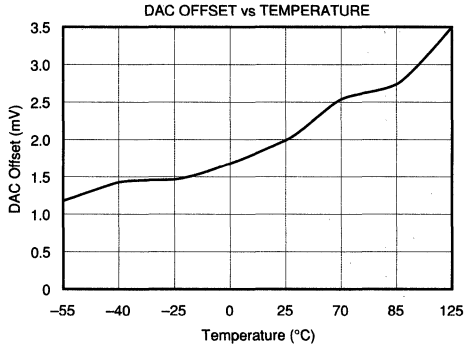


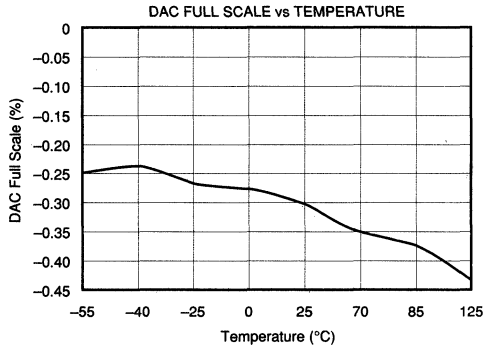




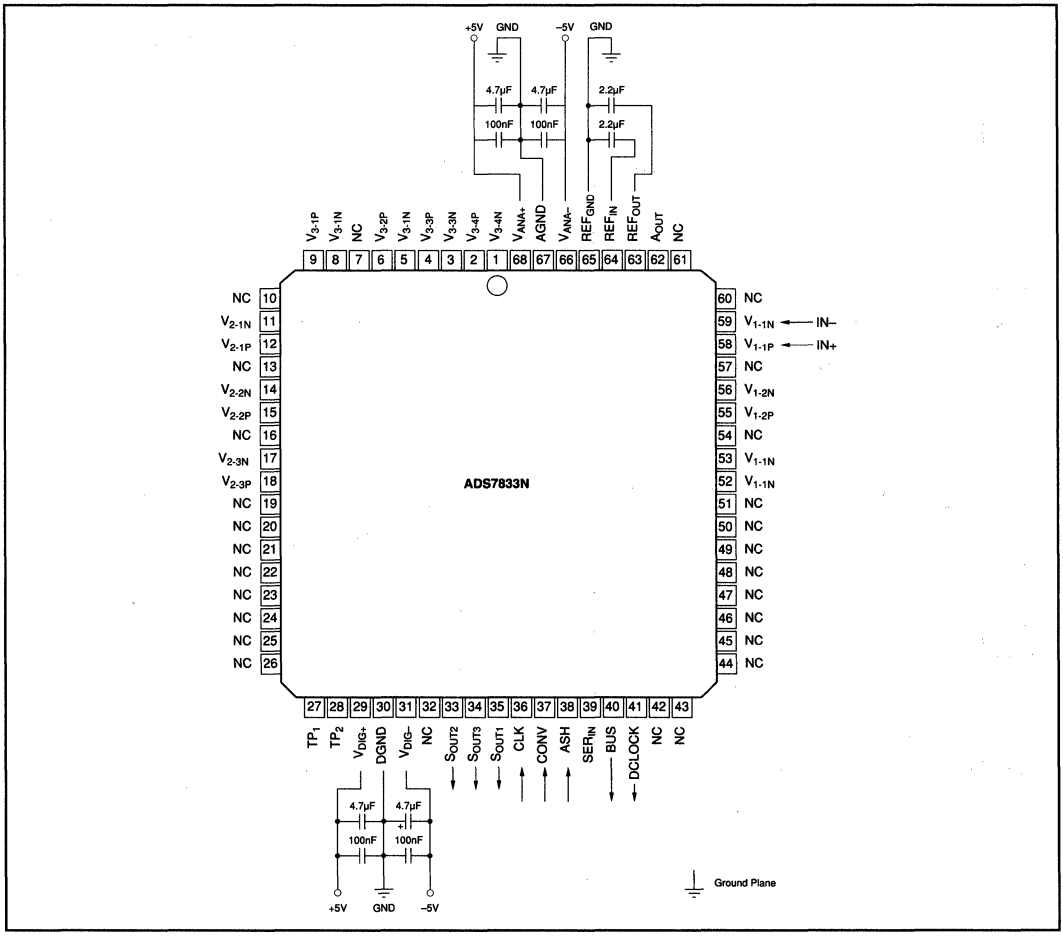
TYPICAL PERFORMANCE CURVES (CONT)

At V_{ANA+} = +5V, V_{ANA-} = –5V, V_{DIG+} = +5V, V_{DIG-} = –5V and T_A = 25°C, using internal reference, f_{CLOCK} = 2.1MHz.





BASIC CIRCUIT CONFIGURATION



FUNCTIONAL DESCRIPTION

(See Figure 1)

ADCs AND PGAs

The ADS7833 contains three signal channels each with a 12-bit analog-to-digital converter output. The ADCs operate synchronously and their serial outputs occur simultaneously. (Table VI gives the analog input/digital output relationships). The ADCs are preceded by programmable gain amplifiers. (Table II gives gain select information). For channels one and two, the PGAs are effective for all three analog inputs. For the third channel, only the V_{3-1} input is gain changed by the PGA. Inputs V_{3-2}, V_{3-3}, and V_{3-4} are connected to ADC_3 at a fixed gain of 1V/V regardless of the Gain Select value.

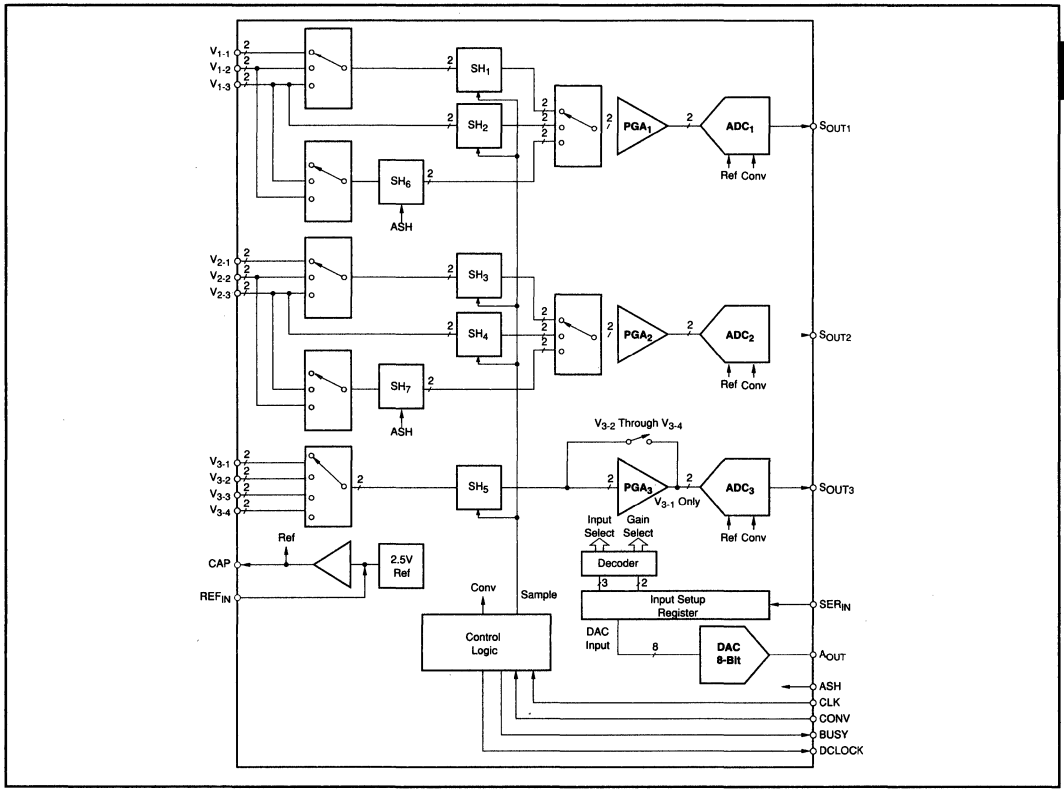


FIGURE 1. Functional Diagram.

SAMPLE HOLDS

The ADS7833 contains seven sample holds. Five of them (SH_1 through SH_5) sample simultaneously and have their sample/hold timing internally synchronized. (The timing is shown in Figure 2).

Three of the sample holds (SH_1, SH_3, and SH_5) are connected to the input multiplexers so that they can provide simultaneous sampling for all of their channels inputs. In addition, SH_2 and SH_4 simultaneously sample the third input of their channels (V_{1-3} and V_{2-3}, respectively). This is useful in motor control applications where V_{1-2} and V_{1-3} are the quadrature inputs for one position sensor, and V_{2-2} and V_{2-3} are the quadrature inputs for a second position sensor (see Figure 6). In that application, it is desirable to sample the quadrature inputs of a given position sensor at the same time (even though they are converted on successive conversion cycles) (see Table III), so that their values are captured at the same shaft position.

The ADS7833 also has the capability for limited asynchronous sampling. The sampling of SH_6 and SH_7 is controlled asynchronously by the control signal ASH (see Table III). This allows two inputs each on channel 1 and channel 2 (see Table IV) to be sampled asynchronously from the timing of the other sample holds. This can be useful in motor control applications where the two inputs for each channel come from a position sensor and it is desired to sample based on position sensor timing rather than system clock timing.

MULTIPLEXERS

The ADS7833 also contains several multiplexers that are used to select the desired analog inputs and connect the proper sample hold outputs to the PGAs and ADCs. The MUXs are driven by a decoder which receives its inputs from the Input Setup Register. (See Table III and Table IV for information on input channel selection). The input multiplexers can take full differential input signals (see Figure 3 and Table VII). The analog signals stay differential through the sample holds and the PGAs all the way to the inputs of the ADSs. This is done to provide the best possible high frequency noise rejection.

INPUT SETUP

As the ADCs are converting and transmitted their serial digital data for one conversion cycle, a setup word is being received to be used for the next conversion cycle. The 13-bit word is supplied at the SER_{IN} pin (see Figure 1), and is stored in the buffered Input Setup Register. The Input Select and Gain Select portions of the word are decoded and determine the state of the multiplexers and PGAs (see CONFIGURABLE PARAMETERS section).

DIGITAL-TO-ANALOG CONVERTER

An 8-bit DAC provides 256 output voltage levels from 0V to 2.5V (see Table V for input/output relationships). The DAC is controlled by the DAC Input portion of the input setup word. The DAC Input portion of the word is strobed into the DAC at the end of the conversion cycle (14th CLK pulse in Figure 2).

VOLTAGE REFERENCE

The ADS7833 contains an internal 2.5V voltage reference. It is available externally through an output buffer amplifier. If it is desired to use an external reference, one may be connected at the REF_{IN} pins. This then overrides the internal 2.5V reference, is connected to the ADCs and is available buffered at the CAP pin.

OTHER DIGITAL INPUTS AND OUTPUTS

Sampling and conversion is controlled by the CONV input (see Figure 2). The ADS7833 is designed to operate from an external clock supplied at the CLK input. This allows the conversion to be done synchronously with system timing so that transient noise effects can be minimized. The CLK signal may run continuously or may be supplied only during convert sequences. The BUSY and DCLOCK signals are internally generated and are supplied to make interfaces with microprocessors easier (see Figures 2, 4, and 6).

CONFIGURABLE PARAMETERS

Configurable parameters are:

- PGA Gain
- Input multiplexer and sample/hold selection
- DAC output voltage

Configuration information for these parameters is contained in the SER_{IN} word (See Figure 2). As one conversion is taking place, the configuration for the next conversion is being loaded into the buffered Input Setup Register via the SER_{IN} word. Table I shows information regarding these parameters.

CLOCK POSITIONS(1)	DESCRIPTION	FUNCTIONS
2-9	DAC $Input_{0-7}$	Sets DAC Output Voltage
10-11	Gain $Select_{0-1}$	Sets PGA Gains
12-14	Input $Select_{0-2}$	Determines Multiplexers Conditions
NOTE: (1) See Figure 2. "Clock Pulse Reference No."		

TABLE I. Description of Configurable Parameters.

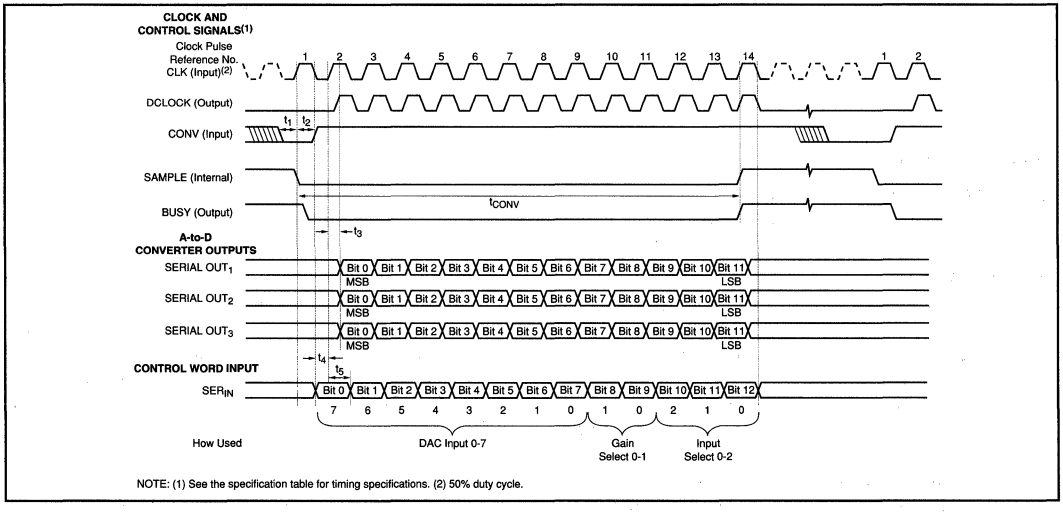


FIGURE 2. Timing Diagram.

PGA GAIN

The PGA gain is determined by the Gain Select portion (bits 8 and 9) in the SER_{IN} word (see Figure 2). There is one gain input that sets the same gain for all three PGAs. The gain values and allowable full scale inputs are shown in Table II.

For channels one and two the PGAs set the gain for all three analog inputs. For the third channel, only the V_{3-1} input is gain changed by the PGA. Inputs V_{3-2}, V_{3-3} and V_{3-4} are connected to ADC_3 at a fixed gain of 1V/V regardless of the Gain Select value.

GAIN SELECT$_{0-1}$	GAIN SETTING	FULL SCALE INPUT
0_H	5.0V/V	±0.5V
1_H	2.5V/V	±1.0V
2_H	1.25V/V	±2.0V
3_H	1.0V/V	±2.5V

TABLE II. Gain Select Information.

INPUT MULTIPLEXER AND SAMPLE HOLD SELECTION

The Input Select portion of the SER_{IN} word (bits 10, 11 and 12) (see Figure 2) are decoded and determine the open/closed condition of the multiplexer switches. This in turn determines which input signals are connected to the sample holds and which sample holds are connected to the PGAs/ADCs.

INPUT SIGNALS FOR PGAs/ADCs

Table III shows the relationships between the value of Input Select$_{0-2}$ and the signals that are converted.

INPUT SELECT$_{0-2}$		ANALOG SIGNAL CONNECTED TO PGA_X/ADC_X		
HEX CODE	BINARY CODE	PGA_1/ADC_1	PGA_2/ADC_2	PGA_3/ADC_2
0_H	000	Undefined	Undefined	V_{3-4}
1_H	001	V_{1-X} via SH_6(1)	V_{2-X} via SH_7(1)	V_{3-4}
2_H	010	V_{1-3} via SH_1	V_{2-3} via SH_3	V_{3-3}
3_H	011	V_{1-3} via SH_2	V_{2-3} via SH_4	V_{3-3}
4_H	100	V_{1-2}	V_{2-2}	V_{3-2}
5_H	101	V_{1-2}	V_{2-2}	V_{3-2}
6_H	110	V_{1-2}	V_{2-2}	V_{3-2}
7_H	111	V_{1-1}	V_{2-1}	V_{3-1}

NOTE: (1) See Table IV for Operation.

TABLE III. Input Controls for Synchronous Sample Holds.

Input Select = 7_H—Synchronously sample and convert input signals V_{1-1}, V_{2-1}, and V_{3-1}.

Input Select = 4_H, 5_H, 6_H—Synchronously sample and convert input signals V_{1-2}, V_{2-2}, and V_{3-2}. These codes also cause SH_2 and SH_4 to sample their inputs. Values 4_H, 5_H, 6_H have different effects on the inputs to SH_6 and SH_7 (see Table IV).

Input Select = 3_H—Convert V_{1-3} via SH_2, V_{2-3} via SH_4, and V_{3-3} (V_{1-3} and V_{2-3} are from the value sampled in a preceding conversion cycle with Input Select = 4_H, 5_H or 6_H).

Input Select = 2_H—Convert V_{1-3} via SH_1, V_{2-3} via SH_3, and V_{3-3} (V_{1-3} is sampled on SH_2 in this conversion cycle).

Input Select = 1_H—Input V_{3-4} is converted by PGA_3/ADC_3. The output of the asynchronous sample holds, SH_6 and SH_7, are converted by PGA_1/ADC_1 and PGA_2/ADC_2, respectively. Note that the inputs to SH_6 and SH_7 are determined by previous Input Select values (see Table IV). Thus, to properly convert the output of one of the asynchronous sample holds it is first necessary to choose its input with a previous conversion cycle. Also, the output of SH_6 or SH_7 will only be converted if ASH goes low before the CONV command is received.

Input Select = 0_H—V_{3-4} is converted by PGA_3/ADC_3. The inputs to PGA_1/ADC_1 and PGA_2/ADC_2 are undefined.

CONVERSIONS FROM THE ASYNCHRONOUS SAMPLE HOLDS

Decoding the Input Select value also determines which inputs are applied to the two asynchronously controlled sample holds SH_6 and SH_7. (See Table IV.) One of the three possible inputs is selected by the Input Select value being 4, 5, or 6.

The "No Effect" states indicate that these values of Input Select have no effect on the multiplexers at the input of SH_6 and SH_7. When one of the "No Effect" values of Input Select is presented, the multiplexers will not be changed (i.e., their condition is determined by the last 4, 5, or 6 value of Input Select that existed prior to the "No Effect" state).

Note that Input Select = 1_H presents the output of SH_6 and SH_7 ($1ASH_X$ and $2ASH_X$) to PGA_1/ADC_1 and PGA_2/ADC_2, respectively (see Table III). Therefore, in order to properly convert the asynchronous sampled signals, it is first necessary to choose an input signal (Input Select equal 5 or 6 in Table IV) with one load/convert cycle and then convert the sample hold output (Input Select = 4 in Table III) in a following conversion cycle.

INPUT SELECT$_{0-2}$		ANALOG SIGNAL CONNECTED TO	
HEX CODE	BINARY CODE	SH_6	SH_7
0_H	000	No Effect	No Effect
1_H	001	No Effect	No Effect
2_H	010	No Effect	No Effect
3_H	011	No Effect	No Effect
4_H	100	Open	Open
5_H	101	V_{1-3}	V_{2-3}
6_H	110	V_{1-2}	V_{1-2}
7_H	111	No Effect	No Effect

TABLE IV. Input Controls for Asynchronous Sample Holds.

DAC OUTPUT VOLTAGE

The value of the DAC output voltage is determined by the DAC Input portion of the SER_{IN} word (bits 0 through 7—see Figure 2). The 8-bit DAC has 256 possible output voltages from 0V to +2.49V. The value of 1 LSB is 0.0098V.

ANALOG-TO-DIGITAL CONVERTERS

ARCHITECTURE

The ADCs are 12-bit, successive approximation types implemented with a switched capacitor circuitry.

SPEED

The clock for the ADC conversion is supplied externally at the CLK pin. Maximum clock frequency for specified accuracy is 2.1MHz. This results in a complete conversion cycle (S/H acquisition and A/D conversion) of 6.6µs.

INPUT/OUTPUT

The ADS7833 is designed for bipolar input voltages and uses a binary two's complement digital output code. A programmable gain function is associated with each ADC. This changes the full scale analog input range and the analog resolution of the converter. Details are shown in Table VI.

DIFFERENTIAL AND COMMON-MODE INPUT VOLTAGES

The ADS7833 is designed with full differential signal paths all the way from the multiplexer inputs through to the input of the ADCs. This was done to provide superior high frequency noise rejection.

DIGITAL INPUT DAC $INPUT_{0-7}$		ANALOG OUTPUT
HEX CODE	BINARY CODE	
00_H	0000 0000	0V
01_H	0000 0001	+0.0098V
•	•	•
•	•	•
•	•	•
FF_H	1111 1111	+2.499

TABLE V. DAC Input/Output Relationships.

As is common with most differential input semiconductor devices, there are compound restrictions on the combination of differential and common-mode input voltages. This matter is made slightly more complicated by the fact that most of the analog inputs are capable of being affected by the programmable gain function. The possible differential and single ended configurations are shown in Figures 3a and 3b.

The maximum differential and common mode restrictions are shown in Table VII.

GAIN SELECT CODE	0	1	2	3
Gain	5.0V/V	2.5V/V	1.25V/V	1.0V/V
Full Scale Range (V_D with V_{CM} = 0)	±0.5V	±1.0V	±2.0V	±2.5V
Largest Positive Common Mode Voltage, V_{CM}+	+2.7V	+2.4V	+1.9V	+1.6V
Largest Negative Common Mode Voltage, V_{CM}–	–2.7V	–2.4V	–1.9V	–1.6V

TABLE VII. Differential and Common Mode Voltage Restrictions.

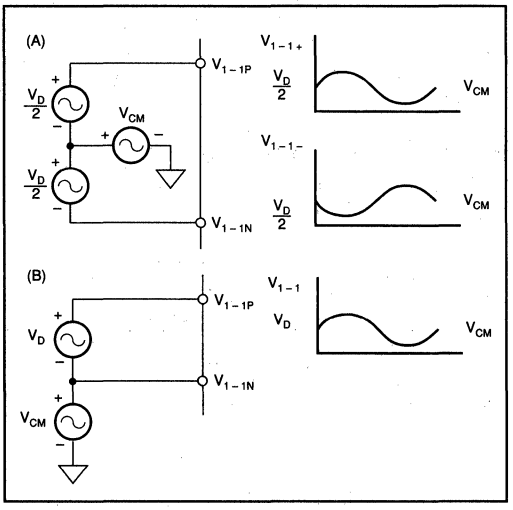


FIGURE 3. (a) Differential Signal Source, and (b) Single Ended Signal Source.

DESCRIPTION	ANALOG INPUT				DIGITAL OUTPUT	
GAIN SELECT CODE	0	1	2	3		
GAIN	5V/V	2.5V/V	1.25V/V	1.0V/V	BINARY TWO'S COMPLIMENT FORMAT	
FULL SCALE RANGE	±0.5V	±1.0V	±2.0V	±2.5V	HEX CODE	BINARY CODE
+Full Scale (FS –1LSB)	+0.49976	+0.9995V	+1.999V	+2.499	$7FF_H$	0111 1111 1111
One Bit above Mid-Scale	+0.244mV	+0.488mV	+0.976mV	+1.22mV	001H	0000 0000 0001
Mid-Scale	0V	0V	0V	0V	000_H	0000 0000 0000
One Bit Below Mid-Scale	–0.244V	–0.488mV	–0.976mV	–1.22mV	FFF_H	1111 1111 1111
–Full Scale	–0.500V	–1.000V	–2.000V	–2.500V	800_H	1000 0000 0000

NOTE: The programmable gain function applies to all three input channels for ADC_1 and ADC_2. However, the programmable gain function only applies to the first input (V_{3-1}) for ADC_3. The other three inputs (V_{3-2}, V_{3-3}, and V_{3-4}) are not affected by the GAIN SEL input. They operate at a fixed gain of 1V/V and thus have a fixed ±2.5V full scale input range.

TABLE VI. Analog Input - Digital Output Relationships.

MICROPROCESSOR INTERFACE

The internal logic of the ADS7833 is designed for easy control and data interface with microprocessors. Figure 4 shows the interface for loading the input control word from the microprocessor data bus into the serial input of the ADS7833.

Table VIII provides a sample assembly code and Figure 4 shows the connection diagram for connecting an ADS7833 to the DSP56004N—or DSP56007 a Motorola Digital Signal Processor. This configuration allows for full control of the ADS7833 as well as receiving all three conversion results simultaneously. The start of conversion is generated by the DSP56004 as well as the sample time of the asynchronous sample/holds.

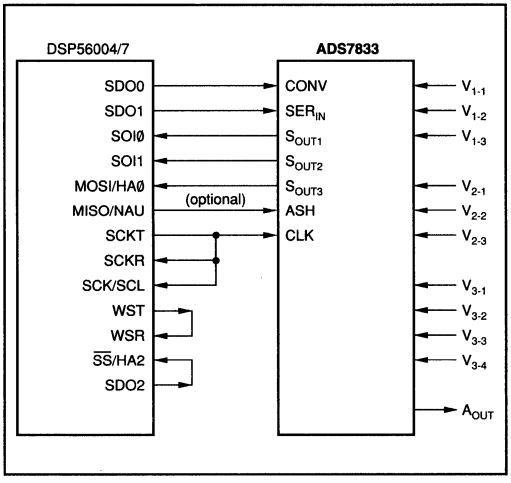


FIGURE 4. Microprocessor Interface for Motorola DSP56004/7.

While this is one of the most useful, the DSP56004/7 is flexible enough to allow various other configurations. These will free up the serial outputs for use with other serial peripherals, such as DACs.

TYPICAL ISOLATED ANALOG INPUT

Figure 5 shows an ISO130 used to isolate the current measurement in a motor speed control application. This amplifier is well suited for this application because of its high transient immunity (l0kV/µs). Its differential output feature is well suited to the differential input of the ADS7833. Keeping the signal transmission differential helps to preserve the high frequency noise rejection of the system.

A unique characteristic of the ISO130 is that it has a common mode output voltage of approximately 2.39V. To accept this level of CMV, the ADS7833 must be operated at a gain of 5V/V (±0.5V full scale differential input). (See Figure 3 and Table VII). Since the ISO130 has a gain of 8V/V, the maximum value of V_{SENSE} is 62.5mV. Thus, the value of R_{SENSE} is chosen to scale V_{SENSE} to this maximum value.

POWER-UP INITIALIZATION

When power is applied to the ADS7833, two conversion cycles are required for initialization and valid digital data is transmitted on the third cycle.

The first conversion after power is applied is performed with indeterminate configuration values in the double buffer output of the Input Setup Register. The second conversion cycle loads the desired values into the register. The third conversion uses those values to perform proper conversions and output valid digital data from each of the ADCs.

```
        movep   #>$0,x:$ffe4        ; Disable SAI transmit port
        movep   #>$0,x:$ffe1        ; Disable SAI receive port
        movep   #>$0,x:$fff1        ; Disable SHI port
        ;
        movep   #>$dfff00,x:$ffe5   ; Convert command
        movep   #>$101f00,x:$ffe6   ; DAC to midscale, G=1V/V, Channel 1 all ADCs
        movep   #>$0,x:$ffe7        ; For SS pin-enables SHI at proper time
        movep   #>$10d,x:$ffe0      ; Divide by 1 pre, divide by 13-96kHz conv @ 40MHz
        movep   #>$3,x:$ffe1        ; Enable SAI recv (rsng edge, MSB 1st, 16-bits, slave)

        movep   #>$2001,x:$fff0     ; Set narrow spike filter, CPOL=0, CPHA=1
        movep   #>$5,x:$fff1        ; Enable SHI (slave, no fifo, 16-bits)
        movep   #>$f,x:$ffe4        ; Enable SAI trans (rsng edge, MSB 1st, 16-bits, mstr)
        ;
wait    btst    #14,x:$ffe1         ; Look for a receive flag (left or right)
        jcs     data
        btst    #15,x:$ffe1
        jcc     wait
data    movep   x:$ffe2,x0          ; Get Sout1
        move    x0,x:$00            ; Save it
        movep   x:$ffe3,x0          ; Get Sout2
        move    x0,x:$01            ; Save it
        move    x:$fff3,x0          ; Get Sout3
        movep   x0,x:$02            ; Save it
```

TABLE VIII. Sample Code for Motorola DSP56004/7.

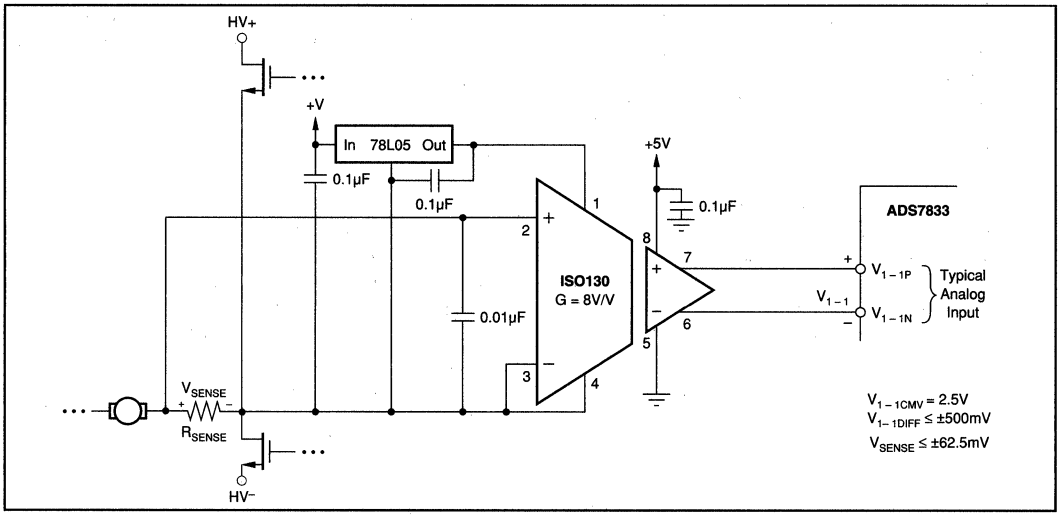


FIGURE 5. Typical Isolated Differential Analog Input.

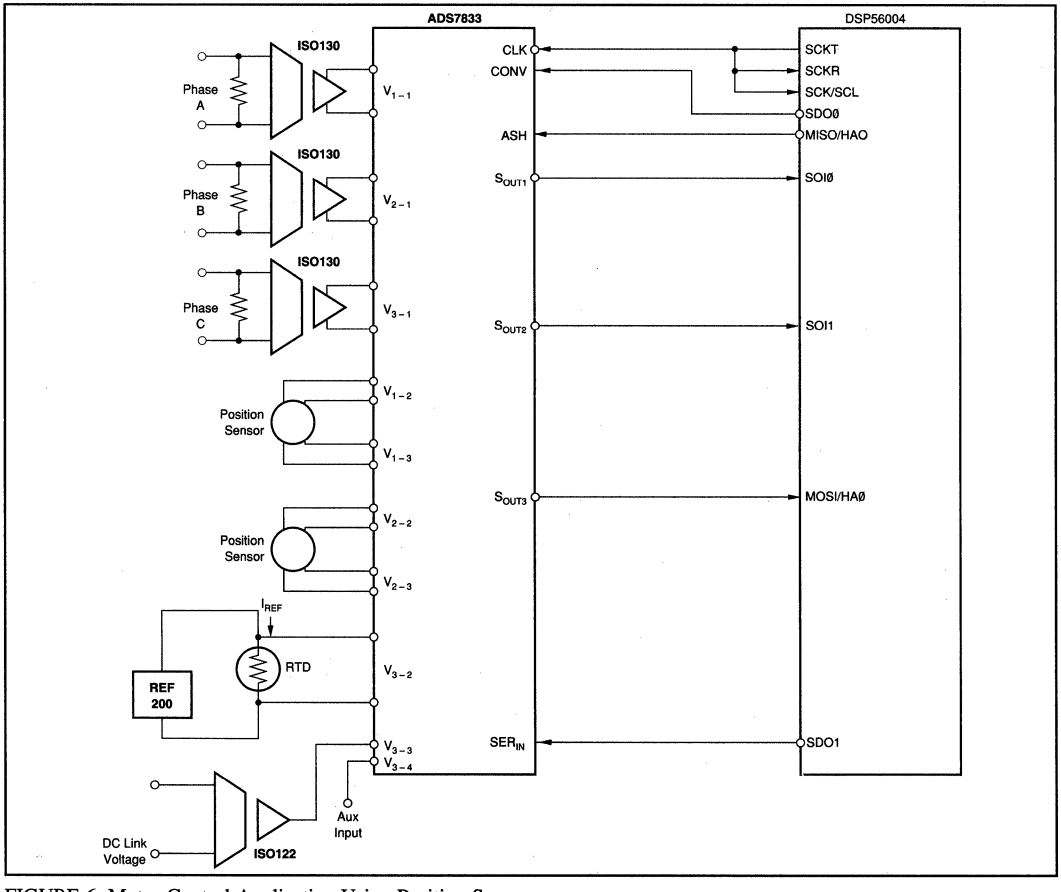


FIGURE 6. Motor Control Application Using Position Sensors.

BURR - BROWN®

AFE1103E

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

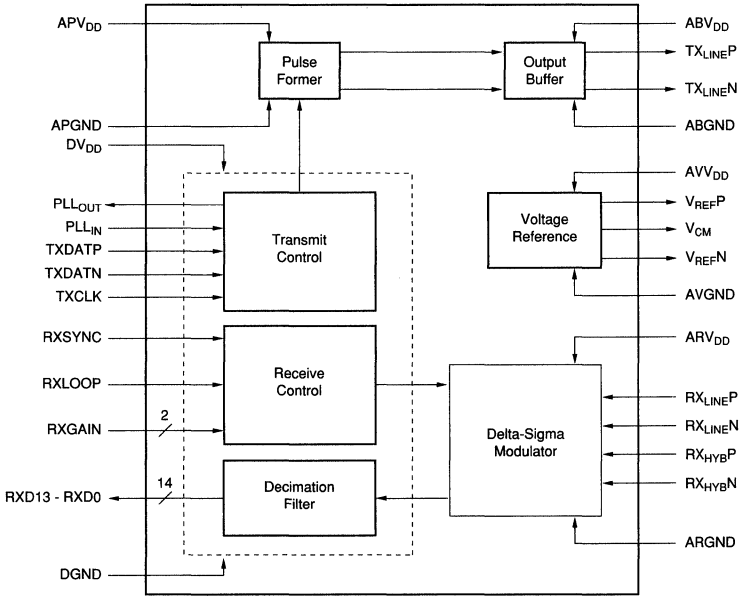
HDSL ANALOG FRONT END

FEATURES

- COMPLETE HDSL ANALOG INTERFACE
- T1 AND E1 OPERATION
- SINGLE CHIP SOLUTION
- SECOND SOURCED BY BROOKTREE Bt8921
- 2B1Q PULSE GENERATOR
- +5V ONLY, 300mW POWER DISSIPATION
- 48-PIN SSOP
- –40°C TO +85°C OPERATION

DESCRIPTION

Burr-Brown's HDSL Analog Front End greatly reduces the size and cost of an HDSL system by providing all of the active analog circuitry needed to connect the Brooktree Bt8952 HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the Bt8952. The HDSL Analog Interface is a monolithic device fabricated on 0.6µCMOS. It operates on a single +5V supply (using only 300mW). It is housed in a 48-pin SSOP package. This unit is second sourced by Brooktree's Bt8921.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

Typical at 25°C, V_{DD} = +5VDC, f_{MC} = 48X, V_{REF} = +2.5V, unless otherwise specified.

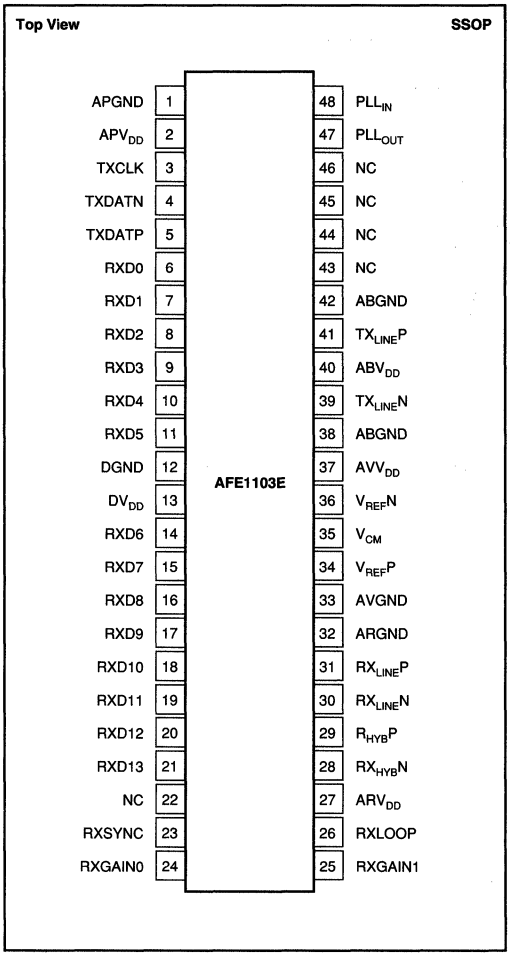
PARAMETER	COMMENTS	AFE1103E MIN	AFE1103E TYP	AFE1103E MAX	UNITS
RECEIVE CHANNEL					
Receive Clock Rate, f_R	48x Symbol Rate	TBD		28.032	MHz
T1 Mode			18.816		MHz
E1 Mode			28.032		MHz
ANALOG INPUTS					
Number of Inputs	Differential		2		
Line Input	G = 1				
Hybrid Input	G = 1				
Input Voltage Range	Balanced Differential	–3.5		+3.5	V
Input Impedance	All Inputs		40		kΩ
Input Capacitance			TBD		
Input Matching				±2	%
Common-Mode Voltage			V_{DD}/2		
A/D CONVERTER					
Resolution	No Missing Codes	13			Bits
Integral Linearity(1)	13-Bit LSB			±1	LSB
Differential Linearity(1)	13-Bit LSB			±0.8	LSB
Programmable Gain	Four Gains Between 0dB and +9dB	0		+9	dB
Settling Time for Gain Change			6		Symbol Periods
Gain + Offset Error	–40°C to +85°C		5		%FSR(2)
Output Data Coding	Offset Binary				
Output Data Rate	f_R/48				
T1 Mode			392		kHz
E1 Mode			584		kHz
SINAD(3)		70			dB
TRANSMIT CHANNEL					
Transmit Clock Rate, f_T		TBD		584	kHz
T1 Mode			392		kHz
E1 Mode			584		kHz
T1 Transmit –3dB Point	Bellcore TA-NWT-3017 Compliant		196		kHz
T1 Rate Power Spectral Density	(4), See Performance Curve				
T1 Average Power	(1), (4), 0 to 784kHz, R_L = 65Ω	13		14	dBm
E1 Transmit –3dB Point	ETSI DTR/TM 3017 Compliant		292		kHz
E1 Rate Power Spectral Density	(4), See Performance Curve				
E1 Average Power	(1), (4), 0 to 1.168MHz, R_L = 65Ω	13		14	dBm
Output Voltage Range	Balanced Differential, R_L = 28Ω	±3.1	±3.3	±3.5	V
Output Current		125			mA
Common-Mode Voltage			V_{DD}/2		
Output Impedance	DC to 1MHz, (1)			2	Ω
Linearity	At Output Symbol Peak, (5)			0.012	%FSR
Harmonic Distortion	3kHz, 3.4V Peak Sine Wave Output, R_L = 28Ω			–65	dB
HDSL Transformer Ratio	T1 or E1 Rates	1:2			
Phase Locked Loop					
Frequency Change Range			100		ppm
DIGITAL INTERFACE					
Input Levels	HCMOS and TTL Compatible				
Output Levels	HCMOS Drive Compatible	10			Loads
RX Interface	Offset Binary Coding				
t_{RX1}	Available Setup Time	50			ns
t_{RX2}	RXD13 - RXD0 to RXSYNC Hold Time	10			ns
Transmit Interface					
t_{TX1}	TXCLK Period	1.7		TBD	µs
t_{TX2}	TXCLK Pulse Width	50			ns
t_{TX3}	TXCLK to TXDAT Edge Allowable Error	0		200	ns
POWER					
Power Supply Voltage	Specification		5		V
Power Supply Voltage	Operating Range	4.75		5.25	V
Power Dissipation in Operation	V = +5VDC T1 or E1 Mode, R_L = 65Ω, (4)		300		mW
PSRR	Power Supply Rejection	65			dB
TEMPERATURE RANGE					
Operating(1)		–40		+85	°C

NOTES: (1) Guaranteed by design and characterization. (2) FSR is Full Scale Range. (3) Signal to Noise plus distortion; production tested with full scale 8kHz and 250kHz input at 584kHz output data rate. (4) With a pseudo-random code sequence of HDSL pulses; 13.5dBm applied to transformer (27dBm output from $TX_{LINE}P$ and $TX_{LINE}N$). (5) Power output and output linearity guaranteed by measuring voltage levels of each of the four symbol outputs.

PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	Ground	APGND	Analog Ground for PLL
2	Power	APV_{DD}	Analog Supply (+5V) for PLL
3	Input	TXCLK	Symbol Clock (QCLK from Bt8952) (392kHz for T1, 584kHz for E1)
4	Input	TXDATN	XMITB Line from Bt8952
5	Input	TXDATP	XMIT Line from Bt8952
6	Output	RXD0	ADC Output Bit-0 (RCV 2 from Bt8952)
7	Output	RXD1	ADC Output Bit-1 (RCV 3 from Bt8952)
8	Output	RXD2	ADC Output Bit-2 (RCV 4 from Bt8952)
9	Output	RXD3	ADC Output Bit-3 (RCV 5 from Bt8952)
10	Output	RXD4	ADC Output Bit-4 (RCV 6 from Bt8952)
11	Output	RXD5	ADC Output Bit-5 (RCV 7 from Bt8952)
12	Ground	DGND	Digital Ground
13	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
14	Output	RXD6	ADC Output Bit-6 (RCV 8 from Bt8952)
15	Output	RXD7	ADC Output Bit-7 (RCV 9 from Bt8952)
16	Output	RXD8	ADC Output Bit-8 (RCV 10 from Bt8952)
17	Output	RXD9	ADC Output Bit-9 (RCV 11 from Bt8952)
18	Output	RXD10	ADC Output Bit-10 (RCV 12 from Bt8952)
19	Output	RXD11	ADC Output Bit-11 (RCV 13 from Bt8952)
20	Output	RXD12	ADC Output Bit-12 (RCV 14 from Bt8952)
21	Output	RXD13	ADC Output Bit-13 (RCV 15 from Bt8952)
22	NC	NC	Connection to Ground recommended
23	Input	RXSYNC	ADC Sync Signal (RCVCLK from Bt8952) (392kHz for T1, 584kHz for E1)
24	Input	RXGAIN0	Receive Gain Control Bit-0
25	Input	RXGAIN1	Receive Gain Control Bit-1
26	Input	RXLOOP	Loopback Control Signal (loopback is enabled by positive signal)
27	Power	ARV_{DD}	Analog Supply (+5V)
28	Input	$RX_{HYB}N$	Negative Input from Hybrid Network
29	Input	$RX_{HYB}P$	Positive Input from Hybrid Network
30	Input	$RX_{LINE}N$	Negative Line Input
31	Input	$RX_{LINE}P$	Positive Line Input
32	Ground	ARGND	Analog Ground
33	Ground	AVGND	Analog Ground
34	Output	$V_{REF}P$	Positive Reference Output
35	Output	V_{CM}	Common-Mode Voltage (buffered)
36	Output	$V_{REF}N$	Negative Reference Output
37	Power	AVV_{DD}	Analog Supply (+5V)
38	Ground	ABGND	Analog Ground
39	Output	$TX_{LINE}N$	Negative Line Output
40	Power	ABV_{DD}	Output Buffer Supply (+5V)
41	Output	$TX_{LINE}P$	Positive Line Output
42	Ground	ABGND	Output Buffer Ground
43	NC	NC	Connection to Ground Recommended
44	NC	NC	Connection to Ground Recommended
45	NC	NC	Connection to Ground Recommended
46	NC	NC	Connection to Ground Recommended
47	Output	PLL_{OUT}	PLL Filter Output
48	Input	PLL_{IN}	PLL Filter Input

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	TBD V
Differential Input Voltage	TBD V
Output Short Circuit to ground (+25°C)	Continuous
Junction Temperature (T_J)	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
AFE1103E	48-Pin Plastic SSOP	333	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

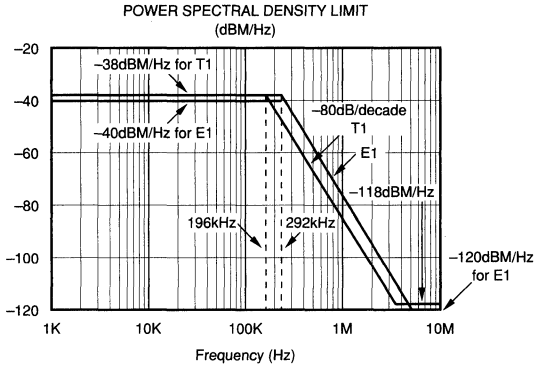
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

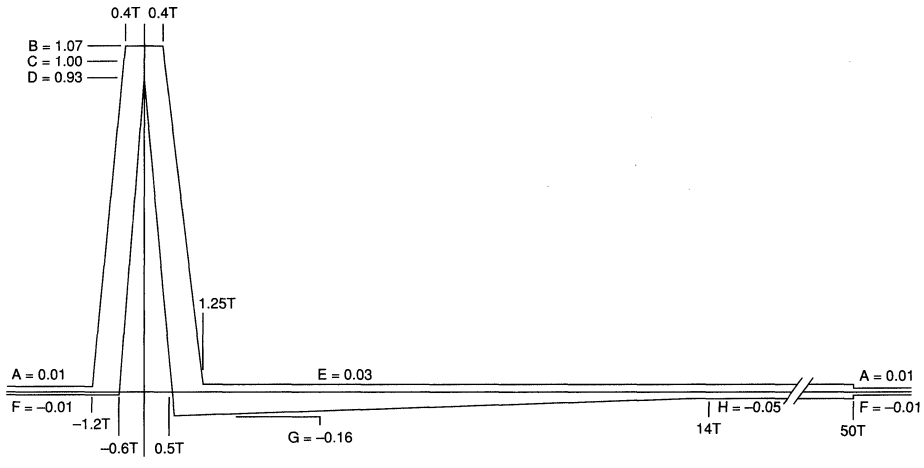
TYPICAL PERFORMANCE CURVES

Output of HDSL Pulse Transformer

Typical at 25°C, V_{DD} = +5VDC, f_{MC} = 48X, V_{REF} = +2.5V, unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at Output of HDSL Transformer.



NORMALIZED LEVEL		QUATERNARY SYMBOLS			
		+3	+1	–1	–3
A	0.01	0.0264	0.0088	–0.0088	–0.0264
B	1.07	2.8248	0.9416	–0.9416	–2.8248
C	1.00	2.6400	0.8800	–0.8800	–2.6400
D	0.93	2.4552	0.8184	–0.8184	–2.4552
E	0.03	0.0792	0.0264	–0.0264	–0.0792
F	–0.01	–0.0264	–0.0088	0.0088	0.0264
G	–0.16	–0.4224	–0.1408	0.1408	0.4224
H	–0.05	–0.1320	–0.0440	0.0440	0.1320

CURVE 2. Transmitted Pulse Template Measured at HDSL Transformer Output.

THEORY OF OPERATION

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data from the XMIT and XMITB outputs of the Bt8952 and generates a 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 for E1 mode and in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210 for T1 mode. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion). In addition to providing a low-impedance output, the line driver will also provide a smoothing filter function for the switched-capacitor pulse former output. This device operates at both T1 and E1 rates.

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first order analog crosstalk reduction. A programmable gain amplifier with gains of 0dB to +9dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces 13 bits of resolution with ±1LSB integral linearity at output rates up to 584kHz. The basic operation of the AFE1103 is illustrated in Figure 1 shown below.

The receive channel operates by summing the two differential inputs, one from the line (RX_{LINE}) and the other from the compromise hybrid (RX_{HYB}). The connection of these two inputs so that the hybird signal is subtracted from the line signal is described in the paragraph below titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is 1. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through 9dB. The ADC converts the signal to a 14-bit digital word, RXD13-RXD0.

RXLOOP INPUT

RXLOOP is the loopback control signal. When enabled, the $RX_{LINE}P$ and $RX_{LINE}N$ inputs are disconnected from the AFE. The $RX_{HYB}P$ and $RX_{HYB}N$ inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to RXLOOP.

ECHO CANCELLATION IN THE AFE

The RX_{HYB} input is designed to be subtracted from the RX_{LINE} input for first order echo cancellation. To accomplish this, note that the RX_{LINE} input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the RX_{HYB} input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

RECEIVE DATA CODING

The data from the receive channel A/D converter is coded in offset binary.

ANALOG INPUT	OUTPUT CODE (RXD13 - RXD0)
Positive Full Scale	1111111111111
Negative Full Scale	0000000000000

RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, RXGAIN1 and RXGAIN0. The resulting gain between 0dB and +9dB is shown below.

RXGAIN1	RXGAIN0	GAIN
0	0	0dB
0	1	3dB
1	0	6dB
1	1	9dB

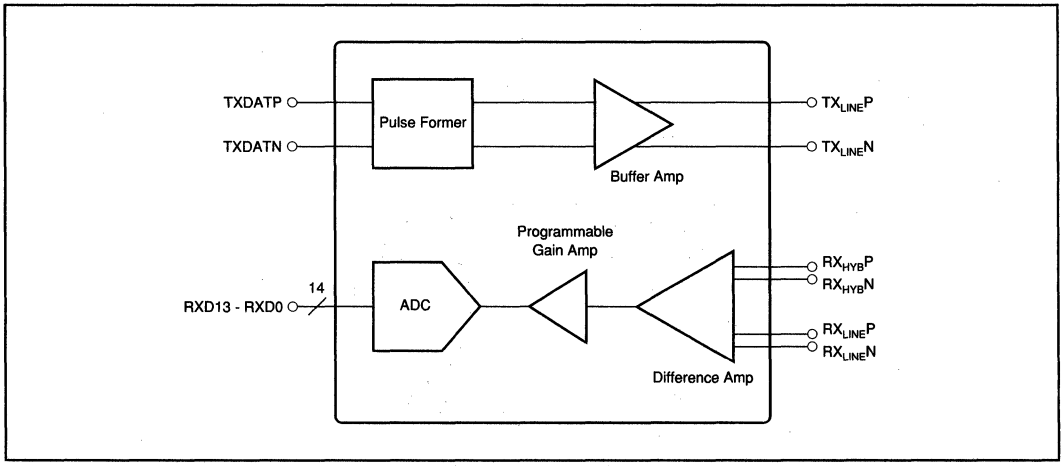


FIGURE 1. Functional Block Diagram of AFE1103.

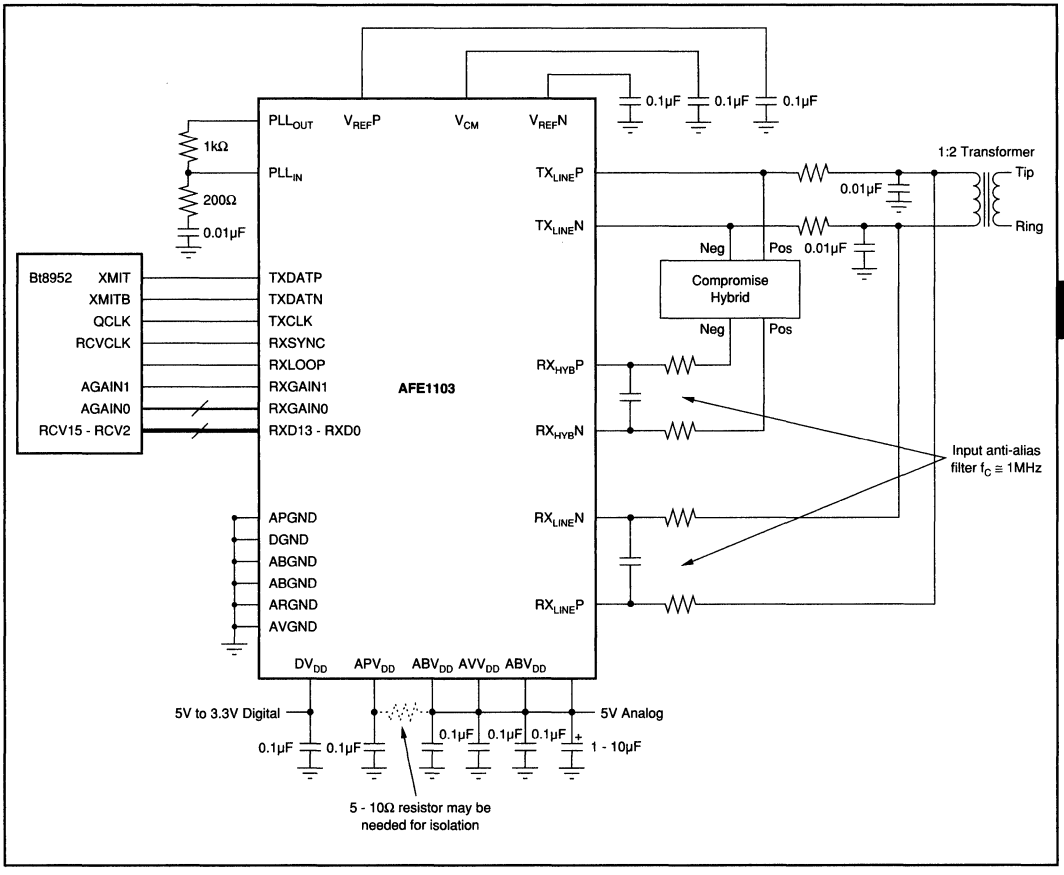


FIGURE 2. Basic Connection Diagram.

RX_{HYB} AND RX_{LINE} INPUT ANTI-ALIASING FILTERS

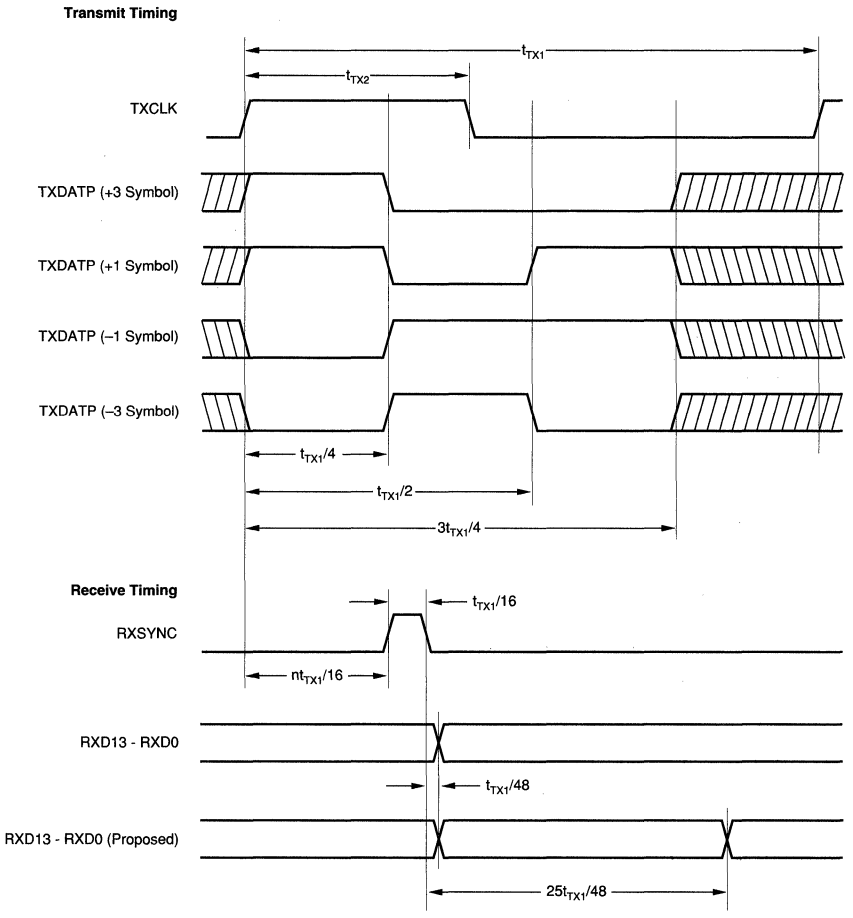
The –3dB frequency of the input anti-aliasing filter for the RX_{LINE} and RX_{HYB} differential inputs should be about 1MHz. Suggested values for the filter are 500Ω for each of the two input resistors and 150pF for the capacitor. Together the two 500Ω resistors and the 150pF capacitor result in a 3dB frequency of just over 1MHz. The 500Ω input resistors will result in a minimal voltage divider loss with the input impedance of the AFE1103.

RX_{HYB} AND RX_{LINE} INPUT BIAS VOLTAGE

The transmitter output on the TX_{LINE} pins is centered at midscale, 2.5V. Therefore, the RX_{LINE} input signal is centered at 2.5V in the circuit shown in Figure 2 above.

Inside the AFE1103, the RX_{HYB} and RX_{LINE} signals are subtracted as described in the paragraph on echo cancellation above. This means that the RX_{HYB} inputs need to be centered at 2.5V just as the RX_{LINE} signal is centered at 2.5V. V_{CM} (Pin 35) is a 2.5V voltage source. The external compromise hybrid must be designed so that the signal into the R_{HYB} inputs is centered at 2.5V. If the compromise hybrid circuit is AC coupled to the RX_{HYB} inputs, an external pull-up resistor to V_{CM} may be needed to center the input at 2.5V.

If V_{CM} pull-up resistors are used, we recommend resistors in the range of 100kΩ so that the pull-up resistors have a small effect on the rest of the circuit and a small current is used from V_{CM}.



NOTES: (1) Any transmit sequence not shown will result in a zero symbol. (2) All transitions are specified relative to the leading edge of TXCLK. (3) Maximum allowable error for any edge is $\pm t_{TX1}/96$ ($\pm t_{TX1}/96$ = ±17.8ns at E1 rate; ±26.6ns at T1 rate). (4) RXSYNC can shift to one of 16 discrete delay times from the leading edge of TXCLK. (5) RXDATA is valid within 15ns of the specified transition time.

FIGURE 3. Timing Diagram.

BURR-BROWN®

AFE1104E

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

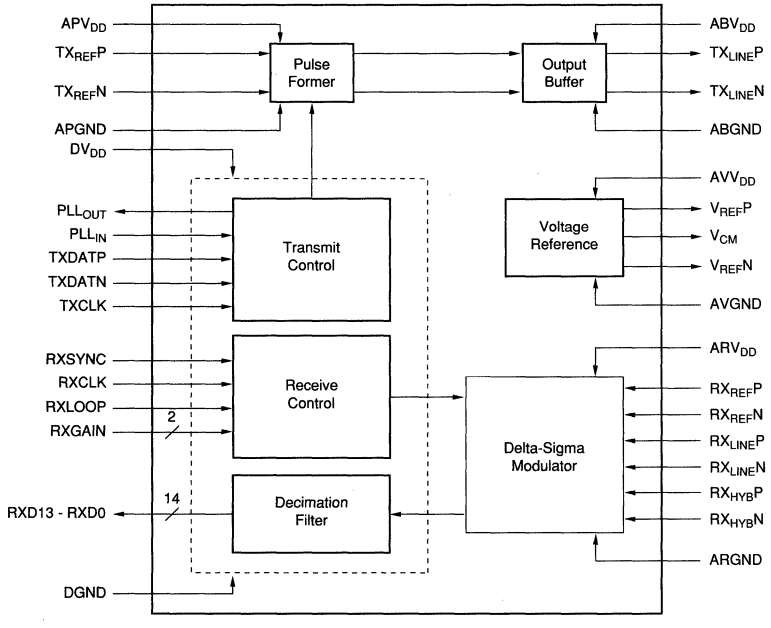
HDSL ANALOG FRONT END

FEATURES

- COMPLETE HDSL ANALOG INTERFACE
- T1 AND E1 OPERATION
- SINGLE CHIP SOLUTION
- 2B1Q PULSE GENERATOR
- +5V ONLY
- 300mW POWER DISSIPATION
- 48-PIN SSOP
- –40°C TO +85°C OPERATION

DESCRIPTION

Burr-Brown's HDSL Analog Front End greatly reduces the size and cost of an HDSL system by providing all of the active analog circuitry needed to connect PairGain Technologies SPAROW HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the SPAROW. The HDSL Analog Interface is a monolithic device fabricated on 0.6µCMOS. It operates on a single +5V supply (using only 300mW). It is housed in a 48-pin SSOP package.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

Typical at 25°C, V_{DD} = +5VDC, f_{MC} = 48X, V_{REF} = +2.5V, unless otherwise specified.

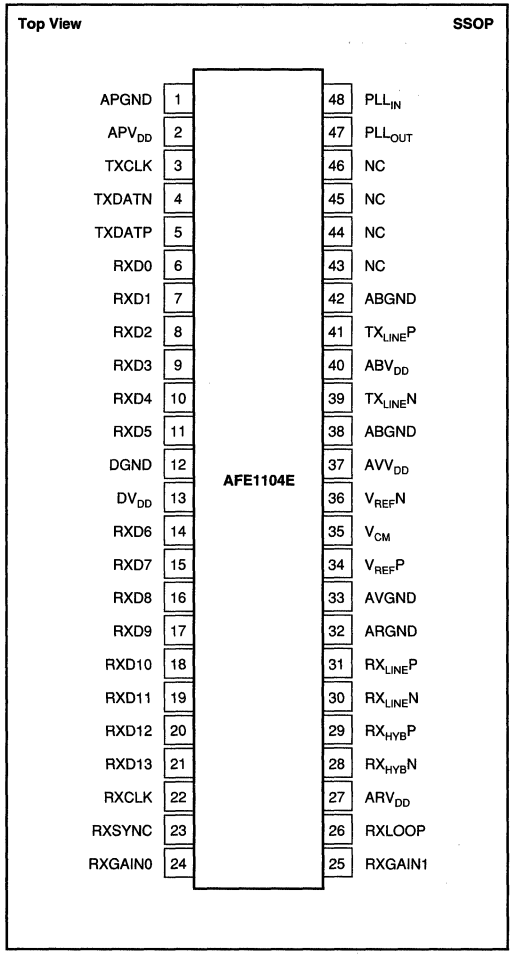
PARAMETER	COMMENTS	AFE1104E MIN	AFE1104E TYP	AFE1104E MAX	UNITS
RECEIVE CHANNEL					
Receive Clock Rate, f_{RX}	48x Symbol Rate	TBD		28.032	MHz
T1 Mode			18.816		MHz
E1 Mode			28.032		MHz
ANALOG INPUTS					
Number of Inputs	Differential		2		
Hybrid Tip	G = –1				
Hybrid Ring	G = +1				
Line Input	G = 1				
Hybrid Input	G = 1				
Input Voltage Range	Balanced Differential	–3.5		+3.5	V
Input Impedance	All Inputs		40		kΩ
Input Capacitance			TBD		
Input Matching				±2	%
Common Mode Voltage			$V_{DD}/2$		
A/D CONVERTER					
Resolution	No Missing Codes	13			Bits
Integral Linearity[1]	13-Bit LSB			±1	LSB
Differential Linearity[1]	13-Bit LSB			±0.8	LSB
Programmable Gain	Four Gains Between 0dB and +9dB	0		+9	dB
Settling Time for Gain Change			6		Symbol Periods
Gain + Offset Error	–40°C to +85°C		5		%FSR[2]
Output Data Rate	$f_{RX}/48$				
T1 Mode			392		kHz
E1 Mode			584		kHz
SINAD[3]		70			dB
TRANSMIT CHANNEL					
Transmit Clock Rate, f_{TX}		TBD		584	kHz
T1 Mode			392		kHz
E1 Mode			584		kHz
T1 Transmit –3dB Point	Bellcore TA-NWT-3017 Compliant		196		kHz
T1 Rate Power Spectral Density	See Performance Curve, [4]				
T1 Average Power	DC to 784kHz, R_L = 65Ω, [1], [4], [5], [6]	13		14	dBm
E1 Transmit –3dB Point	ETSI RTR/TM-03036 Compliant		292		kHz
E1 Rate Power Spectral Density	See Performance Curve, [4]				
E1 Average Power	DC to 1.168MHz, R_L = 65Ω, [1], [4], [5], [6]	13		14	dBm
Output Voltage Range	Balanced Differential, R_L = 28Ω	±3.1	±3.3	±3.5	V
Output Current		125			mA
Common-Mode Voltage			$V_{DD}/2$		
Output Impedance	DC, [3]		2	5	Ω
Linearity	At Output Symbol Peak, [4]			0.012	%FSR
Harmonic Distortion	3kHz, 3.4V Peak Sine Wave Output, R_L = 28Ω			–65	dB
HDSL Transformer Ratio	T1 or E1 Rates	1:2			
DIGITAL INTERFACE[3]					
Input Levels	HCMOS and TTL Compatible				
Output Levels	HCMOS Drive Compatible	10			Loads
Receive Interface					
t_{RX1}	RXCLK Period	40			ns
	RXCLK Duty Cycle	45		55	%
t_{RX2}	RXSYNC to RXCLK Setup Time	10			ns
t_{RX3}	RXSYNC to RXCLK Hold Time	10			ns
t_{RX4}	RXCLK to RXD13 - RXD0 Delay			50	ns
Transmit Interface					
t_{TXBAUD}	TXCLK Period	1.7			µs
t_{TXPW}	TXCLK Pulse Width	50			ns
t_{TXSSW}	TXDAT Sub-Symbol Width	320			ns
t_{TXSSE}	TXCLK to TXDAT Sub-Symbol Edge		$t_{TXBAUD}/96$		
	Allowable Error	–10		+10	ns
POWER					
Power Supply Voltage	Specification		5		V
Power Supply Voltage	Operating Range	4.75		5.25	V
Power Dissipation in Operation	V = +5VDC T1 or E1 Mode, R_L = 65Ω, [4]		300		mW
PSRR	Power Supply Rejection	65			dB
TEMPERATURE RANGE					
Operating[1]		–40		+85	°C

NOTES: (1) Guaranteed by design and characterization. (2) FSR is Full Scale Range. (3) Signal to Noise plus distortion; production tested with full scale 8kHz and 250kHz input at 584kHz output data rate. (4) With a pseudo-random code sequence of HDSL pulses; 13.5dBm applied to transformer (27dBm output from $TX_{LINE}P$ and $TX_{LINE}N$). (5) Power output and output linearity guaranteed by measuring voltage levels of each of the four symbol outputs. (6) HDSL transformer ratio of 1:2 into a line impedance of 135Ω.

PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	Ground	APGND	Analog Ground for PLL
2	Power	APV_{DD}	Analog Supply (+5V) for PLL
3	Input	TXCLK	Transmit Symbol Clock (392kHz for T1, 584kHz for E1)
4	Input	TXDATN	DAC– Line from SPAROW
5	Input	TXDATP	DAC+ Line from SPAROW
6	Output	RXD0	ADC Output Bit-0
7	Output	RXD1	ADC Output Bit-1
8	Output	RXD2	ADC Output Bit-2
9	Output	RXD3	ADC Output Bit-3
10	Output	RXD4	ADC Output Bit-4
11	Output	RXD5	ADC Output Bit-5
12	Ground	DGND	Digital Ground
13	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
14	Output	RXD6	ADC Output Bit-6
15	Output	RXD7	ADC Output Bit-7
16	Output	RXD8	ADC Output Bit-8
17	Output	RXD9	ADC Output Bit-9
18	Output	RXD10	ADC Output Bit-10
19	Output	RXD11	ADC Output Bit-11
20	Output	RXD12	ADC Output Bit-12
21	Output	RXD13	ADC Output Bit-13
22	Input	RXCLK	A/D Clock (18.816MHz for T1, 24.96MHz for E1)
23	Input	RXSYNC	ADC Sync Signal (392kHz for T1, 584kHz for E1)
24	Input	RXGAIN0	Receive Gain Control Bit-0
25	Input	RXGAIN1	Receive Gain Control Bit-1
26	Input	RXLOOP	Loopback Control Signal (loopback is enabled by positive signal)
27	Power	ARV_{DD}	Analog Supply (+5V)
28	Input	$RX_{HYB}N$	Negative Input from Hybrid Network
29	Input	$RX_{HYB}P$	Positive Input from Hybrid Network
30	Input	$RX_{LINE}N$	Negative Line Input
31	Input	$RX_{LINE}P$	Positive Line Input
32	Ground	ARGND	Analog Ground
33	Ground	AVGND	Analog Ground
34	Output	$V_{REF}P$	Positive Reference Output
35	Output	V_{CM}	Common-Mode Voltage (buffered)
36	Output	$V_{REF}N$	Negative Reference Output
37	Power	AVV_{DD}	Analog Supply (+5V)
38	Ground	ABGND	Analog Ground
39	Output	$TX_{LINE}N$	Transmit Line Output Negative
40	Power	ABV_{DD}	Output Buffer Supply (+5V)
41	Output	$TX_{LINE}P$	Transmit Line Output Positive
42	Ground	ABGND	Output Buffer Ground
43	NC	NC	Connection to Ground Recommended
44	NC	NC	Connection to Ground Recommended
45	NC	NC	Connection to Ground Recommended
46	NC	NC	Connection to Ground Recommended
47	Output	PLL_{OUT}	Transmit PLL Filter Output Connection
48	Input	PLL_{IN}	Transmit PLL Filter Input Connection

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	TBD V
Differential Input Voltage	TBD V
Output Short Circuit to ground (+25°C)	Continuous
Junction Temperature (T_J)	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
AFE1104E	48-Pin Plastic SSOP	333	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

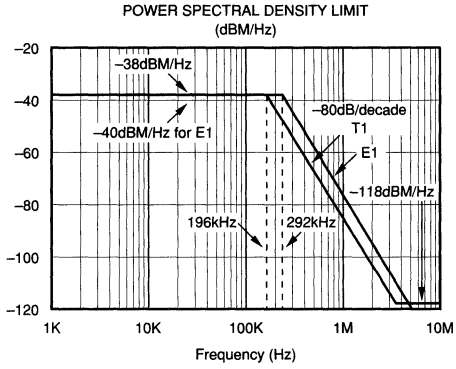
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

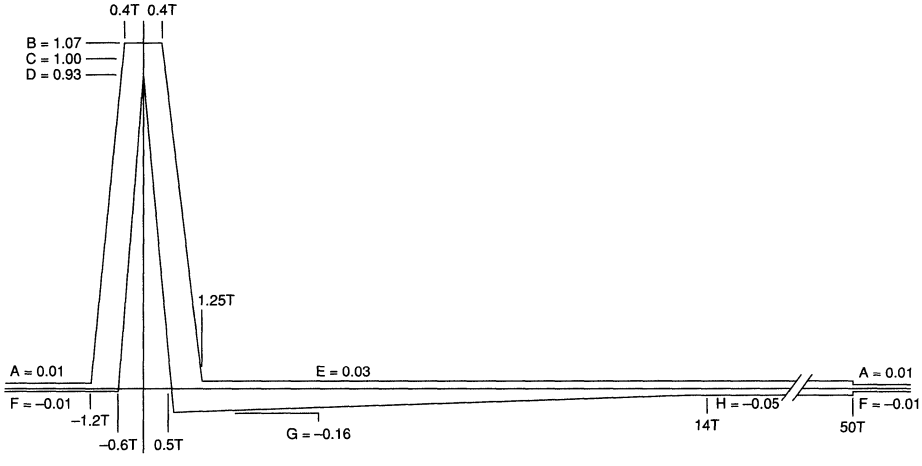
TYPICAL PERFORMANCE CURVES

Output of HDSL Pulse Transformer

Typical at 25°C, V_{DD} = +5VDC, f_{MC} = 48X, V_{REF} = +2.5V, unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at Output of HDSL Transformer.



NORMALIZED LEVEL		QUATERNARY SYMBOLS			
		+3	+1	–1	–3
A	0.01	0.0264	0.0088	–0.0088	–0.0264
B	1.07	2.8248	0.9416	–0.9416	–2.8248
C	1.00	2.6400	0.8800	–0.8800	–2.6400
D	0.93	2.4552	0.8184	–0.8184	–2.4552
E	0.03	0.0792	0.0264	–0.0264	–0.0792
F	–0.01	–0.0264	–0.0088	0.0088	0.0264
G	–0.16	–0.4224	–0.1408	0.1408	0.4224
H	–0.05	–0.1320	–0.0440	0.0440	0.1320

CURVE 2. Transmitted Pulse Template Measured at HDSL Transformer Output.

THEORY OF OPERATION

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data from SPAROW'S DAC+ and DAC– lines and generates a 2B1Q output waveform. In the T1 mode, the output meets the pulse mask and power spectral density requirements defined in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion). In addition to providing a low-impedance output, the line driver will also provide a smoothing filter function for the switched-capacitor pulse former output. This device operates at both T1 and E1 rates.

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier that can be used with an external compromise hybrid for first order analog crosstalk reduction. A programmable gain amplifier with gains of 0dB to +9dB is also included. The delta sigma modulator operating at a 48X oversampling ratio produces 13 bits of resolution with ±1LSB integral linearity at output rates up to 584kHz. The basic operation of the AFE1104 is illustrated in Figure 1 shown below.

The receive channel operates by summing the two differential inputs, one from the line (RX_{LINE}) and the other from the compromise hybrid (RX_{HYB}). The connection of these two inputs so that the hybird signal is subtracted from the line signal is described in the paragraph below titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is 1. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through 9dB. The ADC converts the signal to a 14-bit digital word, RXD13 - RXD0.

RXLOOP INPUT

RXLOOP is the loopback control signal. When enabled, the $RX_{LINE}P$ and $RX_{LINE}N$ inputs are disconnected from the AFE. The $RX_{HYB}P$ and $RX_{HYB}N$ inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to RXLOOP.

ECHO CANCELLATION IN THE AFE

The RX_{HYB} input is designed to be subtracted from the RX_{LINE} input for first order echo cancellation. To accomplish this, note that the RX_{LINE} input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the RX_{HYB} input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

RECEIVE DATA CODING

The data from the receive channel A/D converter is in two's complement code.

ANALOG INPUT	OUTPUT CODE (RXD13 - RXD0)
Positive Full Scale	01111111111111
Mid Scale	00000000000000
Negative Full Scale	10000000000000

RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, RXGAIN1 and RXGAIN0. The resulting gain between 0dB and +6dB is shown below.

RXGAIN1	RXGAIN0	GAIN
0	0	0dB
0	1	3dB
1	0	6dB
1	1	9dB

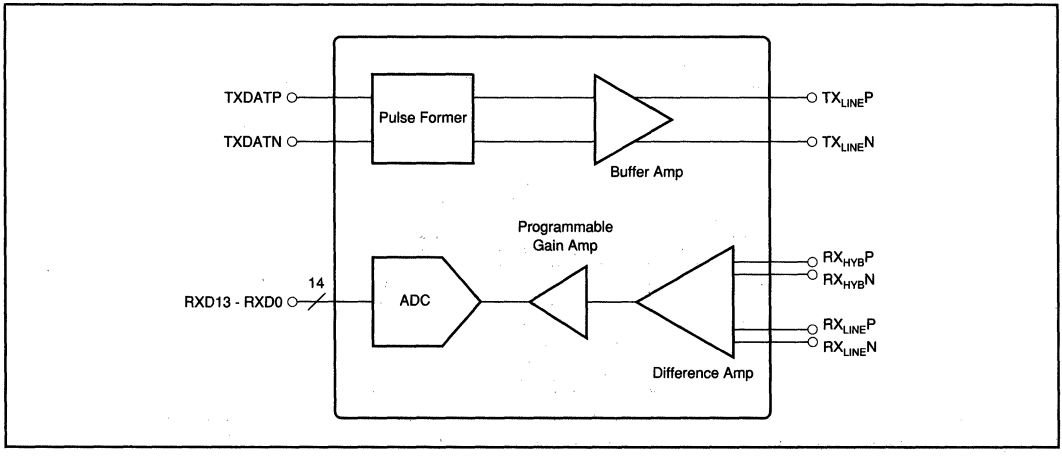


FIGURE 1. Functional Block Diagram of AFE1104.

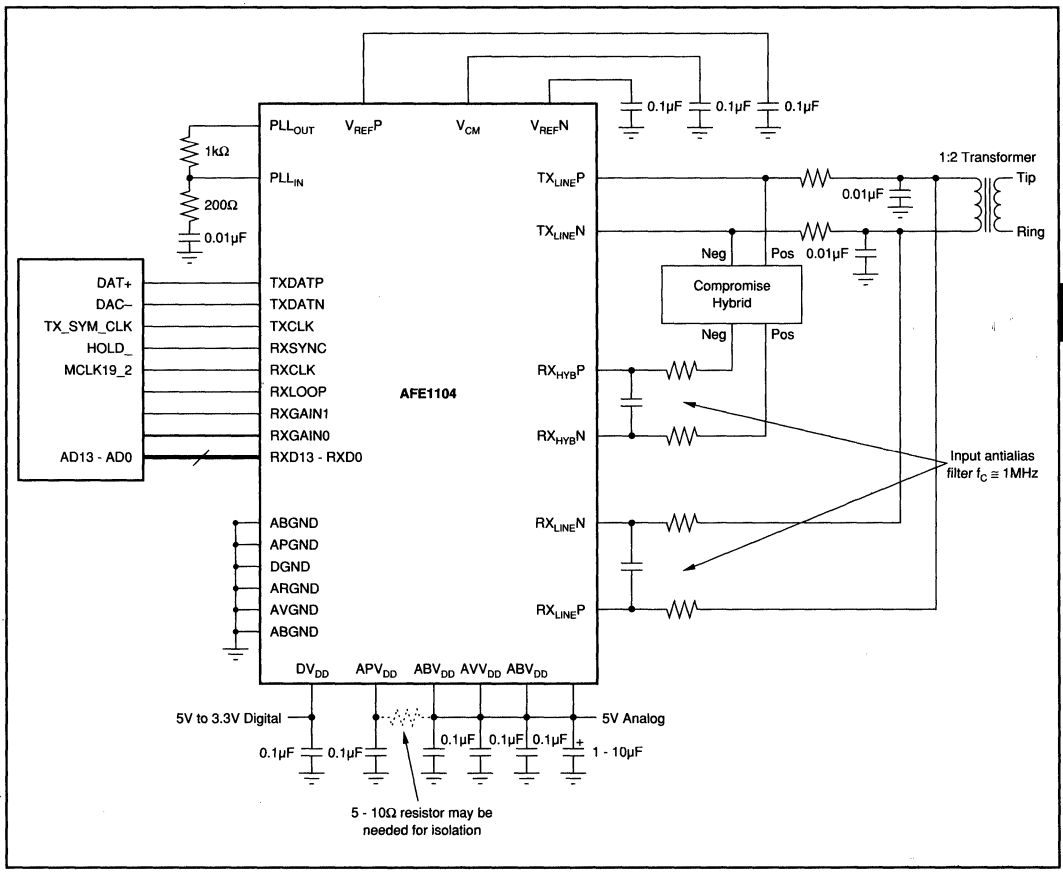


FIGURE 2. Basic Connection Diagram.

RX_{HYB} AND RX_{LINE} INPUT ANTI-ALIASING FILTERS

The –3dB frequency of the input anti-aliasing filter for the RX_{LINE} and RX_{HYB} differential inputs should be about 1MHz. Suggested values for the filter are 500Ω for each of the two input resistors and 150pF for the capacitor. Together the two 500Ω resistors and the 150pF capacitor result in a 3dB frequency of just over 1MHz. The 500Ω input resistors will result in a minimal voltage divider loss with the input impedance of the AFE1104.

RX_{HYB} AND RX_{LINE} INPUT BIAS VOLTAGE

The transmitter output on the TX_{LINE} pins is centered at midscale, 2.5V. Therefore, the RX_{LINE} input signal is centered at 2.5V in the circuit shown in Figure 2 above.

Inside the AFE1104, the RX_{HYB} and RX_{LINE} signals are subtracted as described in the paragraph on echo cancellation above. This means that the RX_{HYB} inputs need to be centered at 2.5V just as the RX_{LINE} signal is centered at 2.5V. V_{CM} (Pin 35) is a 2.5V voltage source. The external compromise hybrid must be designed so that the signal into the RX_{HYB} inputs is centered at 2.5V. If the compromise hybrid circuit is AC coupled to the RX_{HYB} inputs, an external pull-up resistor to V_{CM} may be needed to center the input at 2.5V.

If V_{CM} pull-up resistors are used, we recommend resistors in the range of 100kΩ so that the pull-up resistors have a small effect on the rest of the circuit and a small current is used from V_{CM}.

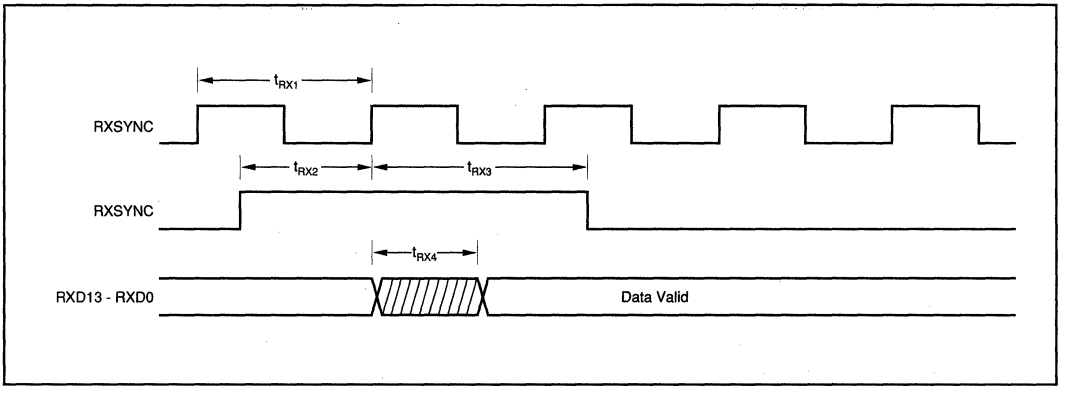
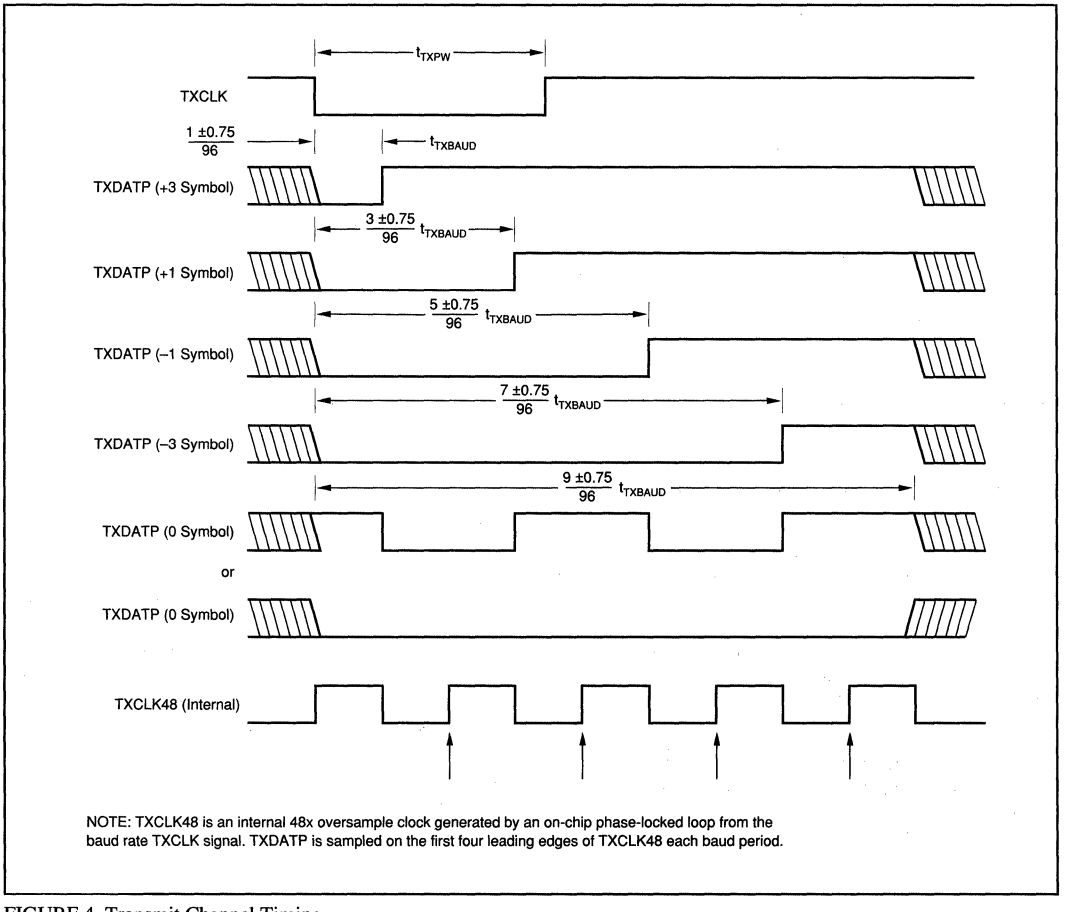


FIGURE 3. Receive Channel Timing.



NOTE: TXCLK48 is an internal 48x oversample clock generated by an on-chip phase-locked loop from the baud rate TXCLK signal. TXDATP is sampled on the first four leading edges of TXCLK48 each baud period.

FIGURE 4. Transmit Channel Timing.

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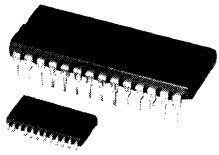


DDC101

20-BIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- MONOLITHIC CHARGE INPUT ADC
- DIGITAL FILTER NOISE REDUCTION: 0.9ppm, rms
- DIGITAL ERROR CORRECTION: CDS
- CONVERSION RATE: Up to 15kHz
- USER FRIENDLY EVALUATION FIXTURE

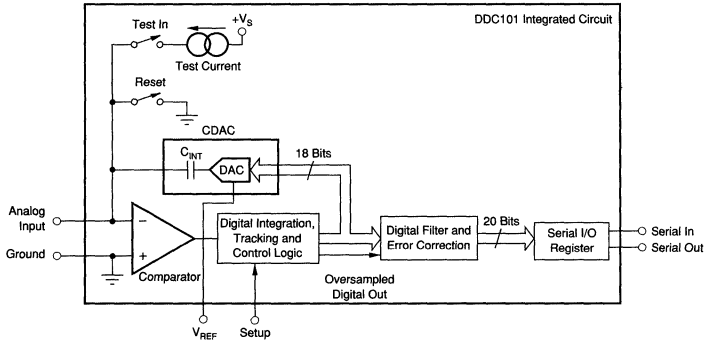
APPLICATIONS

- DIRECT PHOTOSENSOR DIGITIZATION
- PRECISION INSTRUMENTATION
- INFRARED PYROMETRY
- PRECISION PROCESS CONTROL
- CT SCANNER DAS
- CHEMICAL ANALYZERS

DESCRIPTION

The DDC101 is a precision, wide dynamic range, charge digitizing A/D converter with 20-bit resolution. Low level current output devices, such as photosensors, can be directly connected to its input. The most stringent accuracy requirements of many unipolar output sensor applications occur at low signal levels. To meet this requirement, Burr-Brown developed the adaptive delta modulation architecture of the DDC101 to provide linearly improving noise and linearity errors as the input signal level decreases. The DDC101 combines the functions of current-to-voltage conversion, integration, input programmable gain amplification, A/D conversion, and digital filtering to produce precision, wide dynamic range results. The input signal can be a low level current connected directly into the unit or a voltage connected through a user selected resistor. Although the DDC101 is optimized for unipolar signals, it can also accurately digitize bipolar input signals. The patented delta modulation topology combines charge integration and digitization functions. Oversampling and digital filtering reduce system noise dramatically. Correlated Double Sampling (CDS) captures and eliminates steady state and conversion cycle dependent offset and switching errors that are not eliminated with conventional analog circuits.

The DDC101 block diagram is shown below. During conversion, the input signal is collected on the internal integration capacitance for a user determined integration period. A high precision, autozeroed comparator samples the analog input node. Tracking logic updates the internal high resolution D/A converter at a 2MHz rate to maintain the analog input at virtual ground. A user programmable digital filter oversamples the tracking logic's output. The digital filter passes a low noise, high resolution digital output to the serial I/O register. The serial outputs of multiple DDC101 units can be easily connected together in series or parallel if desired to minimize interconnections.



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2 ..... Specifications
3 ..... Pin Descriptions
4 ..... Timing Diagrams
5 ..... Discussion of Specifications
6 ..... Detailed Theory of Operation
7 ..... Applications Information
8 ..... Mechanical

SECTION 1
BASIC THEORY OF OPERATION

The basic function of the DDC101 is illustrated in the Simplified Equivalent Circuit shown in Figure 1. The operation is equivalent to the functions performed by a very high quality, low bias current switched integrator followed by a precision floating point programmable gain amplifier and ending with a high resolution A/D converter.

The second block diagram, Figure 2, shows the DDC101 circuit architecture which implements these functions monolithically. During each conversion, the input signal current is collected on the internal integration capacitance, C_{INT}, as charge for a user determined integration period, T_{INT}. As the integration capacitor collects input charge, the tracking logic updates the internal high resolution D/A converter at a 2MHz rate to maintain the analog input node at virtual ground.

The digital filter oversamples the tracking logic's output at the beginning and end of each integration period to produce two oversampled data points. The DDC101 measures the charge accumulated in the integration and performs correlated double sampling (CDS) by subtracting these two data points. CDS eliminates integration cycle dependent errors such as charge injection, offset voltage, and reset noise since these errors are measured with the signal at each of the two data points. The number of oversamples, and thus the frequency response of the digital filter, is user programmable.

The digital filter passes a low noise, high resolution digital output to the serial I/O register. Since the timing control of the serial I/O register is independent of the DDC101 conversion process, the outputs of multiple DDC101 units can be connected together in series or parallel to minimize interconnections.

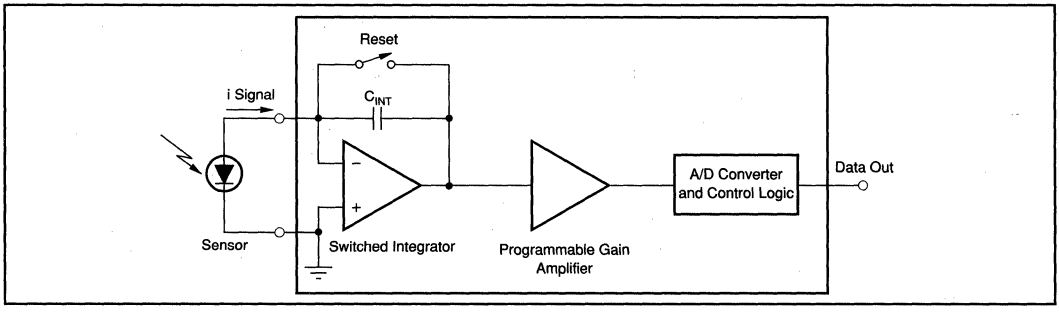


FIGURE 1. Simplified Equivalent Circuit of DDC101 to Illustrate Function.

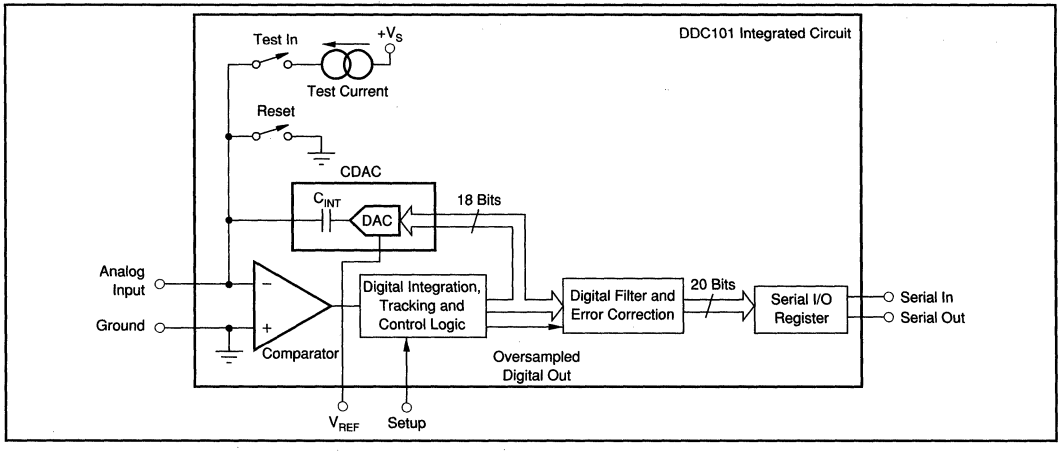


FIGURE 2. DDC101 Block Diagram.

An internal test current source is provided for basic functionality testing and diagnostics. This approximately 100nA current source is pin activated and sums with the external input current.

Figure 3 shows a more detailed circuit configuration of the DDC101. The single integration capacitor, C_{INT}, and the D/A converter have been replaced with a high resolution Capacitor Digital-to-Analog Converter (CDAC). By switching between ground and V_{REF} the binary weighted capacitor array of the CDAC accumulates the input signal's charge to keep the comparator input at virtual ground.

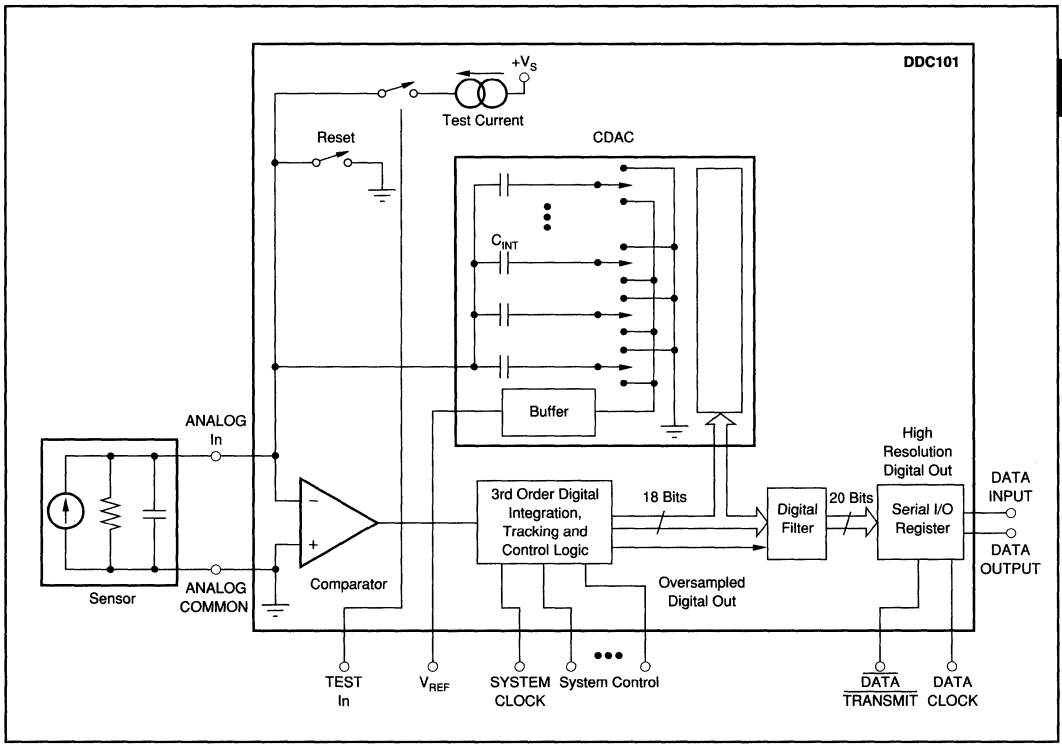


FIGURE 3. DDC101 Detailed Circuit Diagram.

SECTION 2
SPECIFICATIONS

ELECTRICAL

All specifications with unipolar current input range, T_{INT} = 1ms, correlated double sampling enabled, System Clock = 2MHz, V_{REF} = –2.5V, T_A = +25°C and V_S = ±5VDC, unless otherwise noted.

PARAMETER	CONDITIONS	DDC101 MIN	DDC101 TYP	DDC101 MAX	UNITS
INPUTS					
Charge Input[6]					
Unipolar Input Range	BTC Output Code	–1.95		500	pC/Integration
Bipolar Input Range	BTC Output Code	–251.95		250	pC/Integration
Input Current	Unipolar or Bipolar Range			7.8	µA
Current Input Range Examples[10]					
Unipolar Input Range	T_{INT} = 100µs	–0.0195		5	µA
Unipolar Input Range	T_{INT} = 1ms	–1.95		500	nA
Bipolar Input Range	T_{INT} = 100µs	–2.5195		2.5	µA
Bipolar Input Range	T_{INT} = 1ms	–251.95		250	nA
Voltage Input Examples[10]					
Unipolar Input Range[2]	R_{IN} = 10MΩ, T_{INT} = 1ms	–0.0195		5	V
Bipolar Input Range[2]	R_{IN} = 10MΩ, T_{INT} = 1ms	–2.5195		2.5	V
DYNAMIC CHARACTERISTICS					
Conversion Time		64		256 x 10^6	µs
Integration Time		64		10^6	µs
System Clock Input		0.5		2	MHz
ACCURACY					
Unipolar Mode Noise					
Noise, Low Level Current Input[1]	C_{SENSOR} = 0pF, L = 8		0.9		ppm of FSR, rms[3]
Noise, Low Level Current Input[1]	C_{SENSOR} = 0pF, L = 1		1.6		ppm of FSR, rms
Noise, Low Level Current Input[1]	C_{SENSOR} = 100pF, L = 1		2.1	3	ppm of FSR, rms
Noise, Low Level Current Input[1]	C_{SENSOR} = 500pF, L = 1		4.2		ppm of FSR, rms
Noise, Voltage Input[1, 2]	R_{IN} ≥ 20MΩ		1.9		ppm of FSR, rms
Differential Linearity Error					
Unipolar Input Range	Entire Range		±0.005% Reading ±0.5ppm FSR, max		
	0.1% FSR Input			±0.00006	% of FSR
	1% FSR Input			±0.00010	% of FSR
	10% FSR Input			±0.00055	% of FSR
Unipolar or Bipolar Input Range				±0.0015	% of FSR
Integral Linearity Error					
Unipolar Input Range[11]	Entire Range		±0.0244% Reading ±2.5ppm FSR, max		
	0.1% FSR Input			±0.00028	% of FSR
	1% FSR Input			±0.00050	% of FSR
	10% FSR Input			±0.0027	% of FSR
Unipolar or Bipolar Input Range[11]				±0.003	% of FSR
No Missing Codes					
Unipolar Input Range			18		Bits
Bipolar Input Range			16		Bits
Input Bias Current	T_A = +25°C		3	10	pA
DC Gain Error			±0.5	±2	% of FSR
Output Offset Error[8]			±0.5		ppm of FSR
Input Offset Voltage[8]			±0.5	±2	mV
External Voltage Reference, V_{REF}			–2.5		VDC
Internal Test Signal			100		nA
Internal Test Signal Accuracy			±20		nA
Gain Sensitivity to V_{REF}	V_{REF} = 2.5V ±0.1V		1:1		
PSRR		80	90		dB
PERFORMANCE OVER TEMPERATURE					
Output Offset Drift[8]	not including bias current drift		0		µV/°C
Input Offset Voltage Drift[8]			1		µV/°C
Input Bias Current Drift	+25°C to +45°C		0.1	0.5	pA/°C
Input Bias Current	T_A = +85°C		8	40	pA
Gain Drift[4]			±15		ppm/°C
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +5µA	+2.0		+V_{CC}	V
V_{IL}	I_{IL} = +5µA	–0.3		+0.8	V
V_{OH}	I_{OH} = 2 TTL Loads	+2.4		+V_{CC}	V
V_{OL}	I_{OL} = 2 TTL Loads	0.0		0.4	V
Data Clock					
Data I/O				8	MHz
SETUP Code I/O[9]				4	MHz
Data Format					
Straight Binary	Unipolar or Bipolar Range		20		Bits
Two's Complement	Unipolar or Bipolar Range		21		Bits

SPECIFICATIONS (CONT)

ELECTRICAL

All specifications with unipolar current input range, T_{INT} = 1ms, correlated double sampling enabled, System Clock = 2MHz, V_{REF} = –2.5V, T_A = +25°C and V_S = ±5VDC, unless otherwise noted.

PARAMETER	CONDITIONS	DDC101 MIN	DDC101 TYP	DDC101 MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Operation(5)		±4.75	±5	±5.25	VDC
Quiescent Current, Positive Supply	V_S+ = +5VDC, V_{DD}+ = +5VDC		15.6	19.5	mA
Analog, V_S+			8.9		mA
Digital, V_{DD}+			6.7		mA
Quiescent Current, Negative Supply	V_S– = –5VDC		18.0	22.5	mA
Operating Power			170		mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Input = low level (less than 1% of Full Scale); Full Scale I_{IN} = 500nA; T_{INT} = 1ms; Unipolar Input Range; Acquisition Time = 16 clock cycles, Oversampling = 128. (2) Voltage input is converted through user provided input resistor, R_{IN}. (3) FSR is Full Scale Range. (4) Gain Drift does not include the drift of the external reference. (5) V_{DD}+ must be less than or equal to V_S+. See Section 7 for recommended connections. (6) Straight Binary output code has slightly different Charge Range. See Section 6. (8) Input offset voltage is nulled by autozero circuitry and causes no output error. See Section 6 (Internal Error Correction). (9) This is the maximum clock frequency at which SETUP codes can be written to and read from the DDC101. (10) For other input current and voltage configurations, see Discussion of Specifications and Detailed Theory of Operation sections. (11) A best-fit straight line method is used to determine linearity. Two different best-fit straight lines are used for the two unipolar integral linearity specifications. Acquisition Time = 16 clock cycles, Oversampling = 128.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DDC101P	28-Pin DIP	215
DDC101U	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs
- Input Current ..... 100mA, momentary
- Input Current ..... 10mA, continuous
- Input Voltage ..... V_S+ +0.5V to V_S– –0.5V

Power Supply
- V_S+ ..... + 7V
- V_S– ..... –7V
- V_{DD}+ ..... must be ≤ V_S+

Maximum Junction Temperature ..... +165°C

ORDERING INFORMATION

MODEL	PACKAGE	THERMAL RESISTANCE (θ_{JA}) (°C/W)
DDC101P	28-Pin DW DIP	100
DDC101U	24-Pin SOIC	100

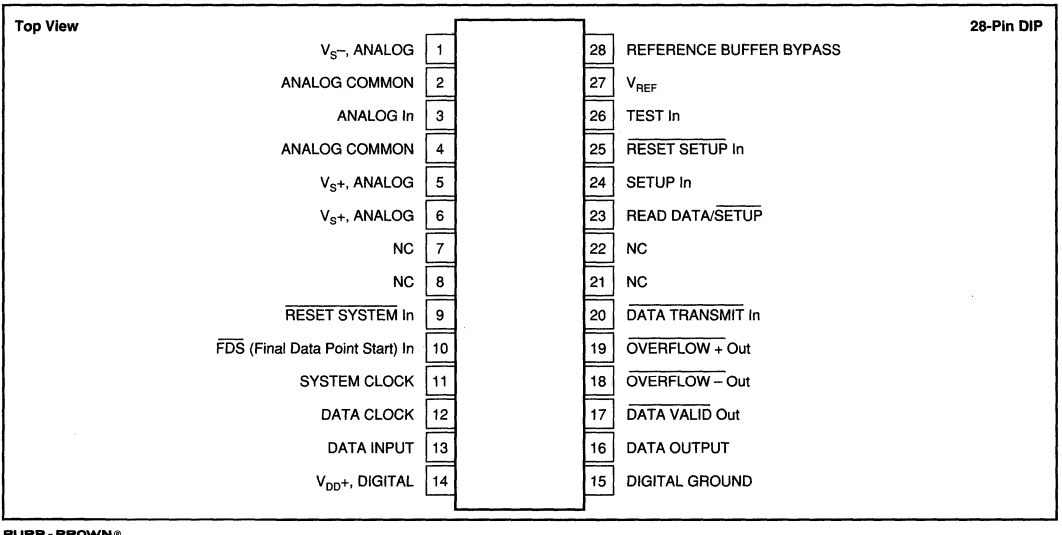
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

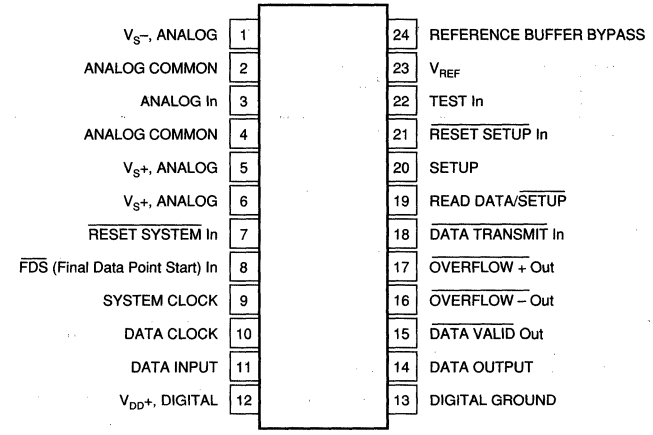
PIN CONFIGURATION

Top View — 28-Pin DIP



PIN CONFIGURATION

Top View **24-Pin SOIC**



SECTION 3
PIN DESCRIPTIONS

SOIC PIN NUMBER	DIP PIN NUMBER	NAME	DESCRIPTION
1	1	V_S–, ANALOG	Negative analog power supply voltage, –5VDC.
2	2	ANALOG COMMON	Analog ground point.
3	3	ANALOG INPUT	Input for low level current signal. Photosensor can be directly connected to this input. With a resistor in series, DDC101 will convert a voltage input.
4	4	ANALOG COMMON	Analog ground point.
5	5	V_S+, ANALOG	Positive analog power supply voltage, +5VDC. Hardwire to pin 6.
6	6	V_S+, ANALOG	Positive analog power supply voltage, +5VDC. Hardwire to pin 5.
7	9	RESET SYSTEM In	This input resets DDC101, but does not reset the SETUP register. The DDC101 system is reset when this pin is active; reset action is removed when the pin is inactive.
8	10	FDS In	This is Final Data point Start input. This input is the basic user control of the integration and conversion timing. When it becomes active, the DDC101 starts collection of the M, final data point samples. The beginning of the next integration time is exactly M system clock periods after the Final Data point Start command when operating in the continuous mode.
9	11	SYSTEM CLOCK	This clock input sets the basic sampling rate of the DDC101. The DDC101 is specified with a clock speed of 2MHz. The clock speed can be 0.5MHz to 2.0MHz.
10	12	DATA CLOCK	This clock input controls the data transfer rate for the serial DATA INPUT and DATA OUTPUT ports. The DATA CLOCK is independent of the SYSTEM CLOCK. This allows the DATA CLOCK to be operated at higher or lower speeds than the SYSTEM CLOCK. For best noise performance, data should not be transmitted and the DATA CLOCK should not be active during the initial and final data point collection. If data is being transmitted during the initial and final data point collection periods, the DATA CLOCK should be synchronized to the SYSTEM CLOCK, to minimize added noise. DATA CLOCK can be connected to SYSTEM CLOCK, so that the same clock is used for both; however, for best noise performance, the DATA CLOCK input should be active only when data is transmitted.
11	13	DATA INPUT	This input can be used to "daisy chain" the output of several DDC101s together to minimize wiring. The output register of the DDC101 acts as a shift register to pass through the output of previously connected DDC101 units. In this way, multiple DDC101 units can convert simultaneously then sequence the data out serially on the same data line with one common control line and one common data line for all DDC101 units.
12	14	V_{DD}+, DIGITAL	Digital power supply, +5VDC. V_{DD}+ must be less than or equal to V_S+.
13	15	DIGITAL GROUND	Digital ground point.
14	16	DATA OUTPUT	This output provides serial digital data clocked out at user controlled DATA CLOCK rate. Output data format is a 21-bit binary two's complement word or a 20-bit straight binary word. The data word is transmitted MSB first. When DATA TRANSMIT is not active DATA OUTPUT tri-states.
15	17	DATA VALID	This output is activated when conversion is complete and remains active until the DATA TRANSMIT input is activated.
16 17	18 19	OVERFLOW– OVERFLOW+	The OVERFLOW output signals each provide an open collector output so that the overflow outputs from several DDC101s can easily be connected (wire ORed) together to a common pull-up resistor. They are activated when the input is beyond the acceptable range during conversion. Specifically, they are activated when the internal D/A converter input or digital filter exceeds full scale. They are Cleared at the end of conversion 1/2 clock cycle after DATA VALID high. DATA VALID can be used to capture OVERFLOW data into an external register.

PIN DESCRIPTIONS (CONT)

SOIC PIN NUMBER	DIP PIN NUMBER	NAME	DESCRIPTION
18	20	$\overline{\text{DATA TRANSMIT}}$ In	This input controls the transmission of data from the serial I/O register of the DDC101. It can be activated anytime after $\overline{\text{DATA VALID}}$ out becomes active. It must remain active until all data has been collected from the serial I/O register(s) of all DDC101s in the data path.
19	23	READ DATA/ $\overline{\text{SETUP}}$ In	This input can be used to read back the current SETUP data. When this input is held high, the output from DATA OUTPUT is the data collected by the DDC101. When this input is pulled low, an internal shift register is loaded with the current SETUP data on the rising edge of DATA CLOCK. This SETUP data shift register is logically connected between DATA INPUT and DATA OUTPUT pins and can be read in the same way that the data output is read. SETUP data read back does not invalidate data already stored in the DDC101's serial I/O register or data being collected by the DDC101, although digital noise concerns should be considered as discussed in DATA CLOCK.
20	24	SETUP In	This input pin controls the DDC101 SETUP. A 12-bit digital word transmitted into this pin controls Acquisition Time, K, Oversampling, M, Multiple Integrations, L, Input Range and Output Data Format. The DDC101 reads the SETUP code at this pin after the $\overline{\text{RESET SETUP}}$ input transitions from active to inactive. The SETUP code is read into the SETUP register on the 12 positive data clock transitions following that transition.
21	25	$\overline{\text{RESET SETUP}}$	Resets SETUP register only, does not reset balance of DDC101. The DDC101 reads SETUP input data after this input transitions from active (reset) to inactive.
22	26	TEST In	This is a digital input that controls the connection of an internal DC current source to the DDC101's input. TEST In exercises the DDC101 and is intended to test for functionality only. The typical test input current is 100nA±20nA. The quiescent current of the DDC101 increases by approximately 1mA when TEST In is active. When TEST is HIGH, the internal current source is ON and current is flowing into the DDC101 input. When TEST is LOW, the current source is disconnected from the input.
23	27	V_{REF}	An external –2.5V reference must be connected to the REFERENCE In pin. Use of an external reference allows multiple DDC101s to use the same system reference for optimum channel matching. The external reference should be filtered to minimize noise contribution (see Figure 24).
24	28	REFERENCE BUFFER BYPASS	An external capacitor of 10µF should be connected to this node to provide proper operation of the internal D/A converter. The REFERENCE In pin is connected to an internal reference buffer amplifier. The internal reference buffer drives the internal CDAC. This buffer output is not intended for external use.
—	7	NC	No connection in 28-pin DIP.
—	8	NC	No connection in 28-pin DIP.
—	21	NC	No connection in 28-pin DIP.
—	22	NC	No connection in 28-pin DIP.

SECTION 4
TIMING CHARACTERISTICS

All specifications with Unipolar input range, T_{INT} = 1ms, Current Input, Correlated Double Sampling enabled, Sys Clock = 2MHz, V_{REF} = –2.5V, T_A = +25°C and V_S = ±5VDC, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	$\overline{\text{FDS}}$ Setup	30			ns
t_2	$\overline{\text{FDS}}$ width, Continuous Conversion	50		(M–1) Clocks+t_1+100ns	ns
t_3	$\overline{\text{FDS}}$ width, Asynchronous Conversion	M Clocks+t_1			ns
t_4	$\overline{\text{FDS}}$ HIGH to start of next integration, Asynchronous Conversion		50		ns
t_5	Setup time for $\overline{\text{RESET SETUP}}$ HIGH to DATA CLOCK HIGH	60			ns
t_6	Setup time for Setup Codes data valid before rising edge of DATA Clock	30			ns
t_7	Hold time for Setup Codes data valid after rising edge of DATA Clock	30			ns
t_8	Propagation delay from rising edge of SYSTEM CLOCK to $\overline{\text{DATA VALID}}$ LOW		50		ns
t_9	Propagation delay from $\overline{\text{DATA TRANSMIT}}$ LOW to $\overline{\text{DATA VALID}}$ HIGH		35		ns
t_{10}	Setup time for DATA CLOCK LOW to $\overline{\text{DATA TRANSMIT}}$ LOW	30			ns
t_{11}	Propagation delay from $\overline{\text{DATA TRANSMIT}}$ LOW to valid data out		30		ns
t_{12}	Hold time that Data output is valid after falling edge of DATA CLOCK	10			ns
t_{13}	Propagation delay from $\overline{\text{DATA TRANSMIT}}$ HIGH to Data Output tri-stated			40	ns
t_{14}	Propagation delay from falling edge of SYSTEM CLOCK to $\overline{\text{OVERFLOW}}$+ and $\overline{\text{OVERFLOW}}$– cleared	25			ns
t_{15}	SYSTEM CLOCK pulse width HIGH	240			ns
t_{16}	SYSTEM CLOCK pulse width LOW	240			ns
t_{17}	$\overline{\text{DATA VALID}}$ LOW to $\overline{\text{DATA TRANSMIT}}$ LOW, Single DDC101	30		(LxN–21) Clocks	ns

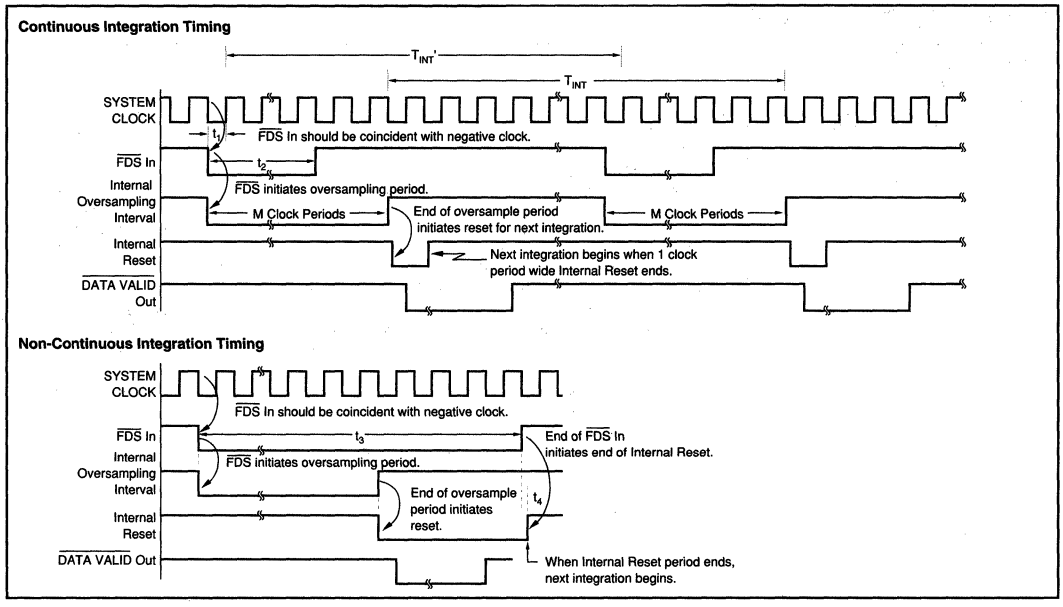


FIGURE 4. Conversion Timing Diagrams.

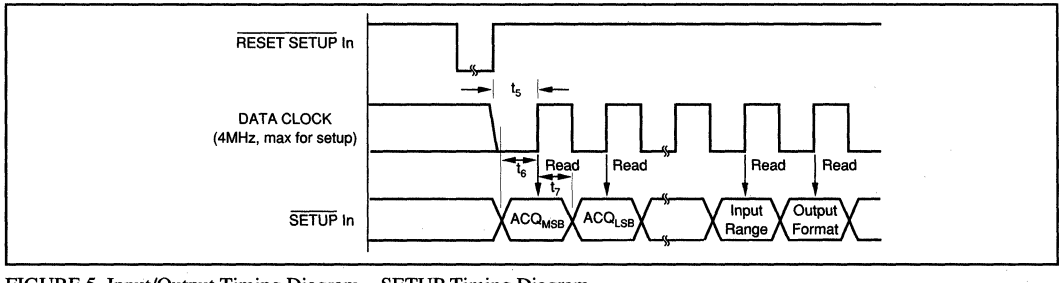


FIGURE 5. Input/Output Timing Diagram—SETUP Timing Diagram.

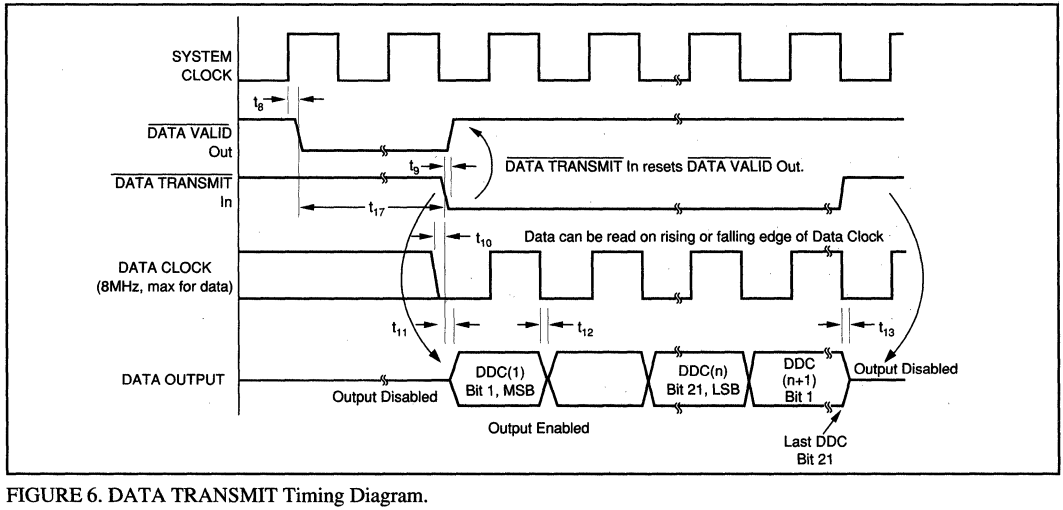


FIGURE 6. DATA TRANSMIT Timing Diagram.

TIMING DIAGRAMS (CONT)

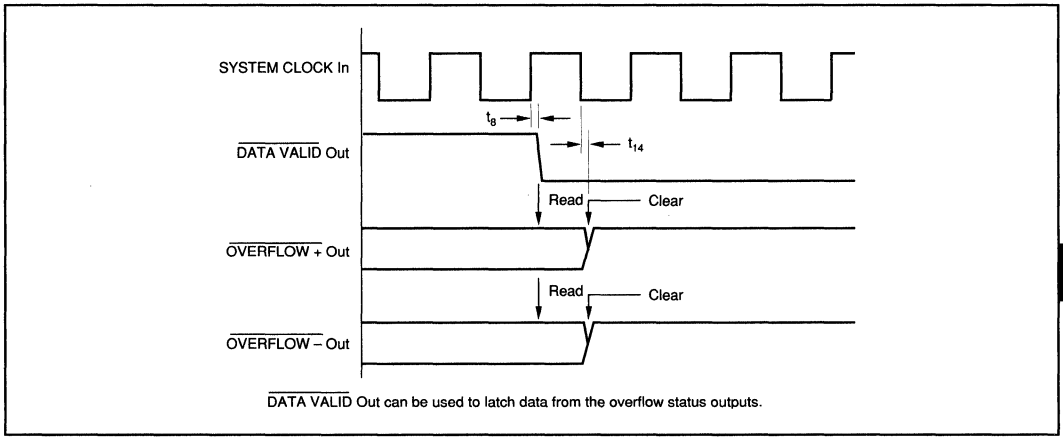


FIGURE 7. OVERFLOW Out Monitoring Timing Diagram.

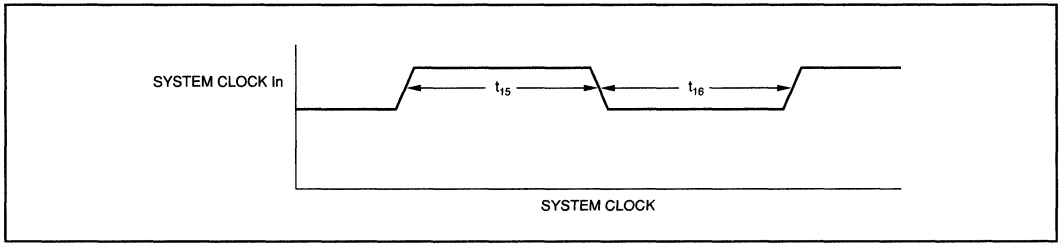


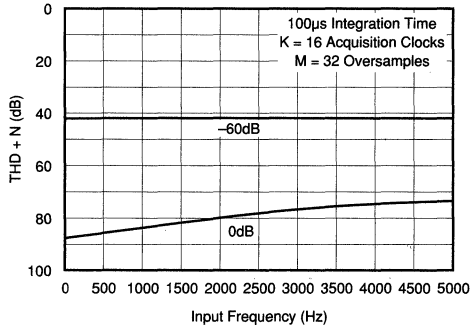
FIGURE 8. System Clock Timing.

TYPICAL PERFORMANCE CURVES

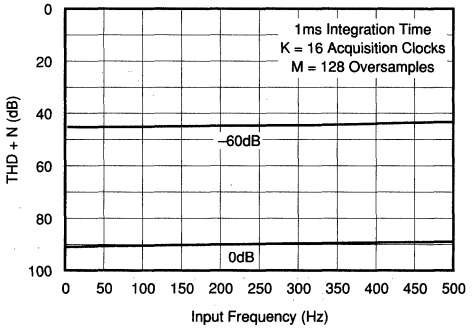
ELECTRICAL

System Clock = 2MHz, V_S = ±5VDC, V_{REF} = –2.5V, L = 1 Integration/Conversion, and T_A = +25°C, unless otherwise noted.

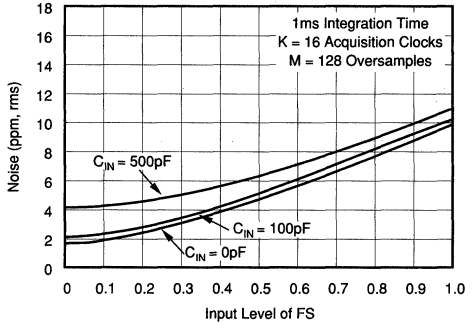
SINAD AT 10kHz CONVERSION, UNIPOLAR INPUT



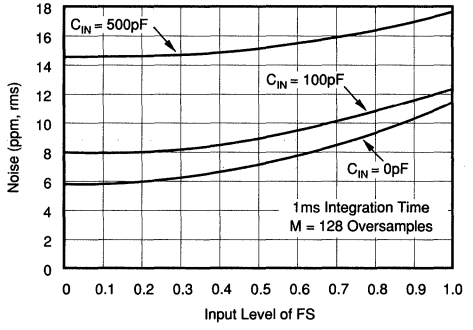
SINAD AT 1kHz CONVERSION, UNIPOLAR INPUT



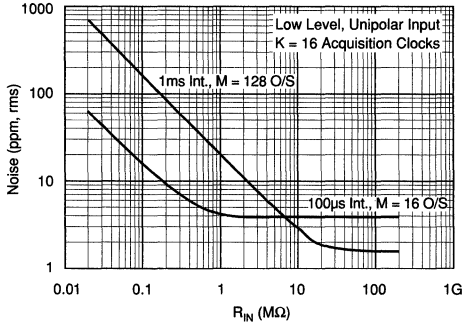
NOISE vs INPUT LEVEL (UNIPOLAR) WITH CDS



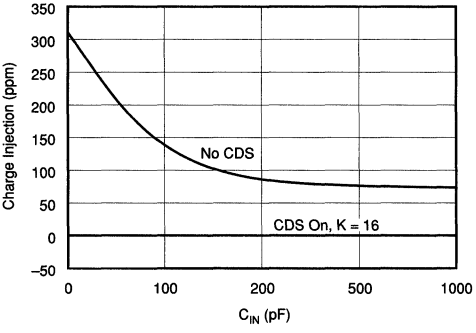
NOISE vs INPUT LEVEL (UNIPOLAR) WITHOUT CDS



NOISE vs RESISTOR VALUE



CHARGE INJECTION vs INPUT CAPACITANCE

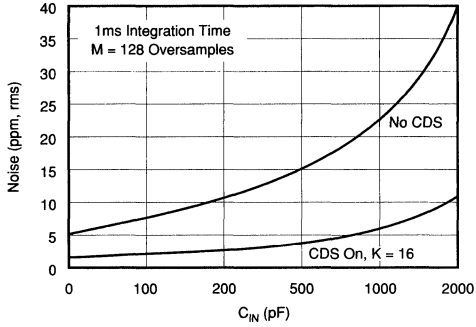


TYPICAL PERFORMANCE CURVES (CONT)

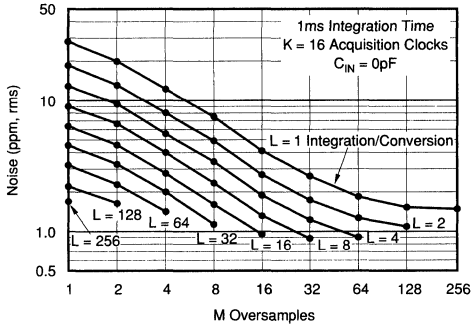
ELECTRICAL

System Clock = 2MHz, V_S = ±5VDC, V_{REF} = –2.5V, L = 1 Integration/Conversion, and T_A = +25°C, unless otherwise noted.

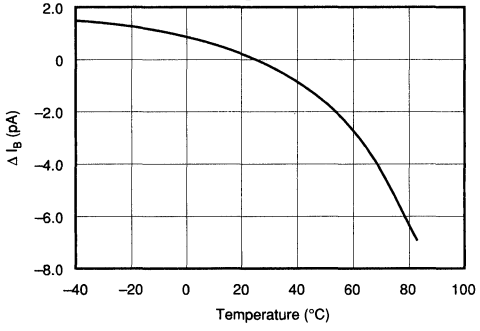
NOISE vs INPUT CAPACITANCE, UNIPOLAR INPUT



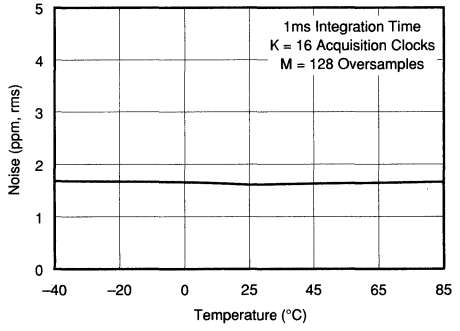
NOISE vs OVERSAMPLING, UNIPOLAR INPUT



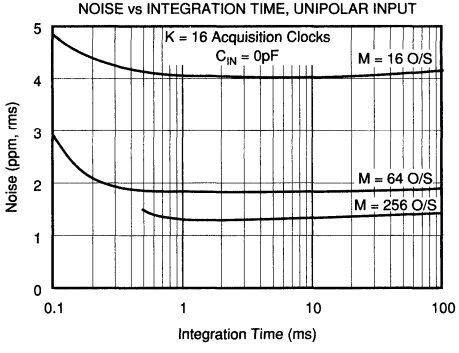
CHANGE IN I_B vs TEMPERATURE



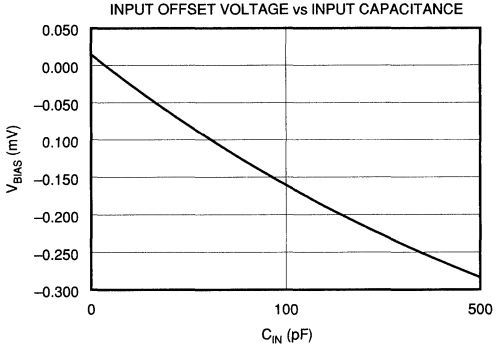
NOISE vs TEMPERATURE, UNIPOLAR INPUT



NOISE vs INTEGRATION TIME, UNIPOLAR INPUT



INPUT OFFSET VOLTAGE vs INPUT CAPACITANCE

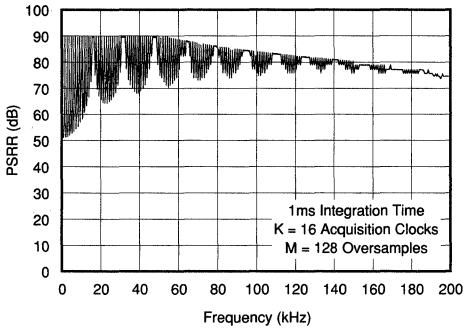


TYPICAL PERFORMANCE CURVES (CONT)

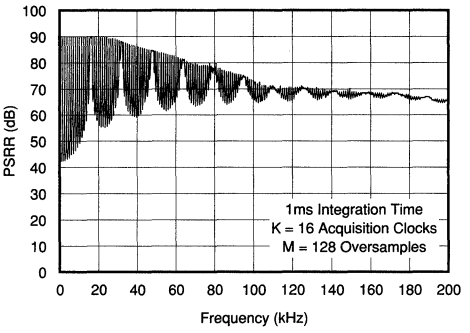
ELECTRICAL

System Clock = 2MHz, V_S = ±5VDC, V_{REF} = –2.5V, L = 1 Integration/Conversion, and T_A = +25°C, unless otherwise noted.

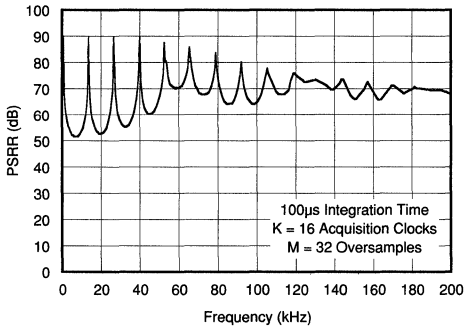
NEGATIVE PSRR vs FREQUENCY



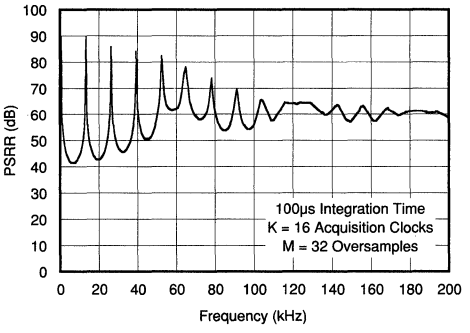
POSITIVE PSRR vs FREQUENCY



NEGATIVE PSRR vs FREQUENCY



POSITIVE PSRR vs FREQUENCY



SECTION 5
DISCUSSION OF SPECIFICATIONS

INPUT

The DDC101 is a charge digitizing A/D converter. Low level current output sources, such as a photosensors, can be directly connected to its input. The input signal can also be a voltage connected through a user selected resistor.

CHARGE INPUT

The maximum charge that can be captured in one integration by the DDC101 is 500pC. In the unipolar input range mode, the maximum positive charge that can be collected in one integration is 500pC. The DDC101 has a small negative range in the unipolar mode of –1.95pC. This small negative underrange is included to allow for a small amount of leakage current from the user's PC board and sensor. In the bipolar input range, the maximum positive charge that can be collected is +250pC. The maximum negative charge that can be collected is –251.95pC.

In addition to the normal mode of one integration per conversion, DDC101 can be configured by the user for 1 to 256 integrations per conversion. When the multiple integrations per conversion mode is chosen, the DDC101 DSP circuitry internally averages multiple integration cycles to provide one conversion result. This result has lower noise because it is the average of multiple integrations. In this mode, the maximum total charge that can be captured by the DDC101 in 256 integrations is 128,000pC.

TEST CURRENT INPUT

An internal DC test current can be connected under user control to the DDC101's input. The test current is nominally 100nA and will be summed with any applied external input signal. It is derived by a resistive network from the positive power supply. The test current is intended to test for functionality only. The TEST In pin of the DDC101 controls the current. When TEST is HIGH, the internal current source is ON and current is flowing into the DDC101 input. When TEST is LOW, the current source is disconnected from the input. With TEST active, positive power supply current increases by approximately 1mA.

FULL SCALE RANGE

The full scale range (FSR), which is referenced in the specification table, is the difference between the positive full scale charge and the negative full scale charge for the DDC101 in one integration cycle. Specifications such as noise and linearity, which are specified in percent or ppm of FSR, are referring to a value of 500pC for both unipolar and bipolar input ranges.

The full scale input current for a given integration time will result in a full scale input charge. As an example for unipolar input range, an input current of 0.5µA integrated for 1ms will result in the full scale charge of 500pC. For voltage inputs, the input resistor is chosen to achieve the proper full scale input current. As an example, for a 5V full scale input, a 10MΩ input resistor is selected to achieve a full scale input current of 0.5µA (1ms integration time).

Noise of 1.6ppm of FSR is equal to 1.6ppm x 500pC = 0.8fC or 1.6ppm x 0.5µA = 0.8pA or 1.6ppm x 5V = 8µV. Thus, in this instance, noise is 1.6pA or 8µV.

For the unipolar input range, the following table shows the full scale input current required for different integration times to collect 500pC of charge and the equivalent current values for 2 and 5ppm of FSR.

T_{INT}	I_{FS}	2ppm	5ppm
50ms	10nA	0.02pA	0.5pA
5ms	100nA	0.2pA	1pA
1ms	500nA	1pA	2.5pA
500µs	1µA	2pA	5pA
100µs	5µA	10pA	25pA

TABLE I. Integration Time (T_{INT}) and Full Scale Current (I_{FS}) for Full Scale 500pC Integration.

CURRENT INPUT

The maximum average input current that can be captured by the DDC101 is ±7.8µA. This current will result in an integration time of 64µs for unipolar input range and 32µs for bipolar input range. For longer integration times, the average input current must be less.

The maximum input current is limited by the slew and update rate of the internal tracking logic and CDAC. The largest input current that the DDC101 can accurately track is 7.8µA. Input currents larger than 7.8µA and high speed current input pulses can be accurately captured and digitized by the DDC101 with an external input or sensor capacitance on the DDC101 input. The average current during a complete integration cycle cannot exceed 7.8µA. Likewise, the total charge input must not exceed 500pC unipolar, 250pC bipolar during the integration time.

An external user provided input capacitance, C_S, as shown in Figure 9a, will capture the input signal charge if the input current limit is temporarily exceeded during the integration cycle. The DDC101 will then transfer the charge completely to C_{INT} based upon conservation of charge. An additional

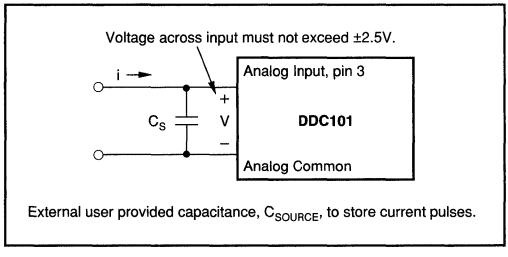


FIGURE 9a. Current Pulse Input Capture.

constraint is, the voltage that appears at the DDC101 input, must not exceed 2.5V. If this voltage is exceeded, charge may be lost and the integration result may be invalid. The input voltage can be calculated:

$$i(t) = C_S \frac{dv}{dt}$$

or

$$V = \frac{1}{C_S} \int i(t)dt$$

therefore,

$$V = i \frac{t}{C_S}.$$

As an example, with a user supplied input capacitance of 100pF, a current pulse of 100µA for 2µs could be stored without exceeding 2.5V applied to the input:

$$V = (100\mu A) \bullet \frac{2\mu s}{100pF} = 2V.$$

The current pulse must occur completely during part of one DDC101 integration time, and the DDC101 must still have time to discharge the input capacitance to ground at a maximum rate of 7.8µA before the DDC101 is triggered (through the FDS input) to end the integration. In addition, the total charge integrated must be 500pC or less for the unipolar range. A current pulse of 100µA for 2µs creates 200pC of charge.

VOLTAGE INPUT SPECIFICATIONS

The DDC101 is a charge digitizing device. With a user provided input resistor, the DDC101 can digitize voltage inputs. All of the general charge/current input specifications apply to the voltage input situation. The specification table shows the typical noise of the DDC101 including the effects of a 20MΩ input resistor, R_{IN}.

The input of the DDC101 is a virtual ground. A voltage input causes a current, i, to flow into the input through R_{IN} as shown in Figure 9b. The maximum input current is determined by the integration time selected. Table II shows the maximum input voltage based upon several selections of input current and input resistor for unipolar input range. The accuracy of the input resistor will add directly to the DC Gain Error of the DDC101; the drift of the input resistor will add directly to the Gain Drift of the DDC101.

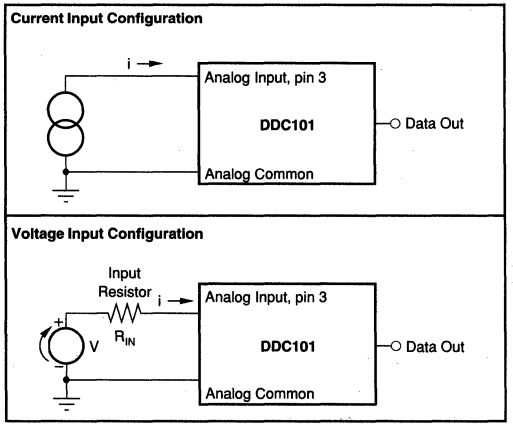


FIGURE 9b. DDC101 Input Configurations.

Note that the DDC101 output noise decreases as R_{IN} increases. This is because the DDC101 noise gain decreases and the input resistance current noise decreases as R_{IN} increases. This effect is shown in the "Noise vs Resistor Value" typical performance curve.

	INPUT RESISTOR, R_{IN}		
INTEGRATION TIME	**1ms**	**500µs**	**100µs**
Full Scale Input Current	0.5µA	1µA	5µA
Full Scale Voltage			
50mV	100kΩ	50kΩ	10kΩ
500mV	1MΩ	500kΩ	100kΩ
5V	10MΩ	5MΩ	1MΩ
50V	100MΩ	50MΩ	10MΩ

TABLE II. Example of Input Resistor Values Unipolar Input Range.

UNIPOLAR LINEARITY ERRORS

Due to innovative design techniques, the absolute level of linearity error of the DDC101 improves as the input signal level decreases when used in the unipolar input mode. Therefore, in unipolar input mode, the integral linearity of the DDC101 is specified as a small base error plus a percentage of reading error or as a percentage of full scale range. A best-fit straight line method is used to determine integral linearity. Two different best-fit straight lines are used for the two unipolar integral linearity specifications. For bipolar input mode, linearity is specified only as a percentage of full scale range.

To illustrate the improvement in unipolar mode linearity error, Figure 10 shows the maximum unipolar integral linearity error (ILE) of the DDC101 as a function of the input signal level. The maximum integral linearity error is ±0.0244% of reading ±2.5ppm of FSR. Thus, the maximum ILE for an input level of 1% of FSR is 0.0005%FSR.

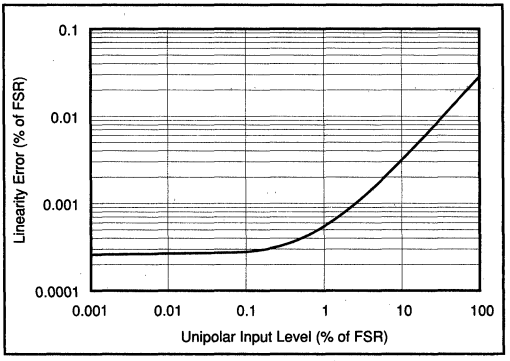


FIGURE 10. Maximum Unipolar Integral Linearity Error Relative to Full-Scale, Converted From % of Reading Specification.

NOISE

The noise of the DDC101 improves as the input signal level decreases, thus very low level signals can be resolved. Noise is shown in the specification table for low level inputs. For unipolar input range, the DDC101 noise at low level inputs is dominated by comparator noise gained to the output; at full scale inputs, the noise is dominated by D/A converter noise. The noise at low low level inputs is a function of input capacitance; the noise at full scale is relatively independent of input capacitance. For bipolar input operation, the noise is dominated by D/A converter noise and is higher than the full scale unipolar noise.

BIPOLAR INPUT ACCURACY

Linearity—As a bipolar input device, the linearity of the DDC101 is specified as a percentage of full scale range that does not improve with lower input signal levels. Performance is generally limited by the linearity of the unit when operated in the bipolar input mode.

Noise—In general, noise is not as important as linearity when determining total error. The output noise of the DDC101 in the bipolar mode peaks at midscale (zero input signal level). Output noise is lower for inputs above and below zero.

RESET CHARGE ERROR

The reset charge error (typically less than 250fC) is an offset error that could result from offset voltage, charge injection and kT/C errors. The DDC101 eliminates the effects of reset charge errors with correlated double sampling.

DC BIAS VOLTAGE

The DDC101 generates a small bias voltage (typically 500μV) at the input. This voltage is impressed on any sensor that is connected to the input. The DC bias voltage is the actual virtual ground voltage of the DDC101. The DDC101 input comparator circuitry includes an autozero circuit which eliminates this offset internally so that it does not produce an output error.

GAIN SENSITIVITY TO V_{REF}

The DDC101 gain is dependent upon the external reference voltage, V_{REF}. A change in the value of V_{REF} will be seen as a directly proportional change in the gain of the DDC101.

FREQUENCY RESPONSE

The DDC101 is a sampling system whose transfer function has three separate frequency components. These components are multiplied together to make the total frequency characteristic of the DDC101. The three components are:

1. Basic Integration
   This is the characteristic sin(x)/x response of the basic integration function. This response is controlled by the integration time of the DDC101.
2. Oversampling
   This is the low pass filter characteristic of the digital filter's oversampling. This response reduces the broadband noise in the input signal and the DDC101. Broadband noise decreases as the number of oversamples increases.
3. Multiple Integrations
   This is the low pass filter characteristic that results when the digital filter is used to average multiple integrations. This will determine the primary response of the DDC101 if two or more integrations are internally averaged.

See Section 6 for more details.

SECTION 6
DETAILED THEORY OF OPERATION

INTEGRATION CYCLE

An integration cycle, as illustrated in Figure 11, includes the Acquisition Time, Initial Data Point Sampling, Tracking Interval, and Final Data Point Sampling. The Acquisition Time is K clock periods. The first clock cycle of the Acquisition Time is used to reset the integrating capacitor, C_{INT}, to zero from the previous integration. The balance of the Acquisition Time insures that the DDC101 system is accurately tracking the input signal prior to initial data point acquisition. Close-ups of the Reset and Acquisition time are shown in Figures 12 and 13.

The Initial Data Point is then sampled M times. The Integration cycle time consists primarily of the Tracking Interval during which time the DDC101 "tracks" the integration of the input signal. The Tracking Interval is followed by the measurement of the Final Data Point with the same user selected number of samples, M. M and K are user selectable. The entire integration cycle consists of N clock periods as controlled by the user.

The DDC101 operates in continuous and non-continuous integration modes. In the continuous mode, one integration follows another with no delay from the end of one integration to the beginning of the next conversion. In the non-continuous mode, each new integration is started separately under user control.

The Final Data point Start (FDS) input is the primary user control of the integration cycle. The FDS input controls the end of one integration cycle and the start of the next integration cycle in both the continuous and non-continuous integration modes. Measurement of the M final data point samples begins when the FDS input is activated.

CONTINUOUS INTEGRATION MODE

In the continuous integration mode, the "Final Data Point Start" command (using the FDS pin) initiates the measurement of the M final data point samples. The next integration cycle begins immediately after the final data point sampling

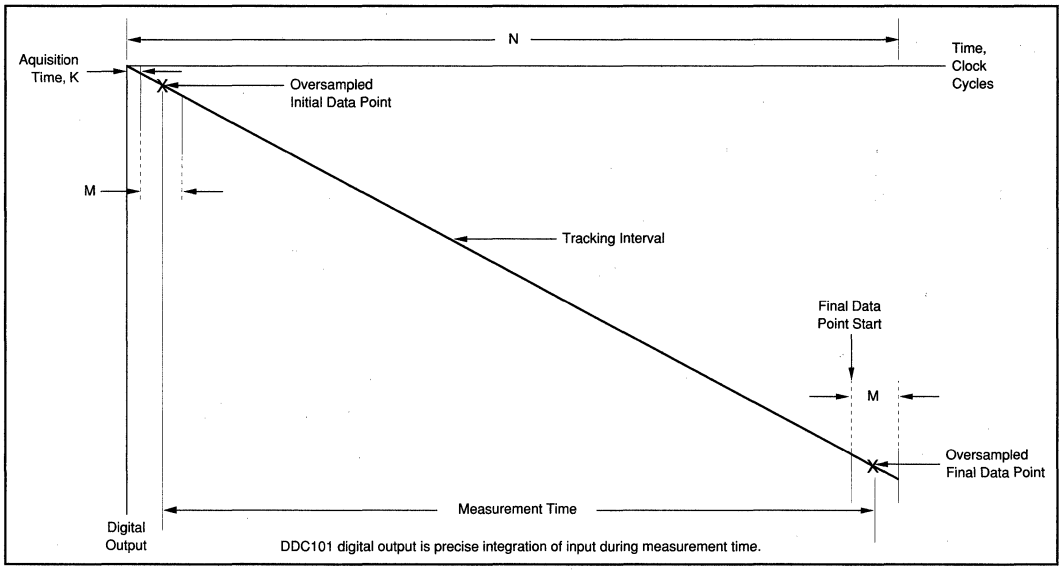


FIGURE 11. Equivalent Integrator Output for Single Integration.

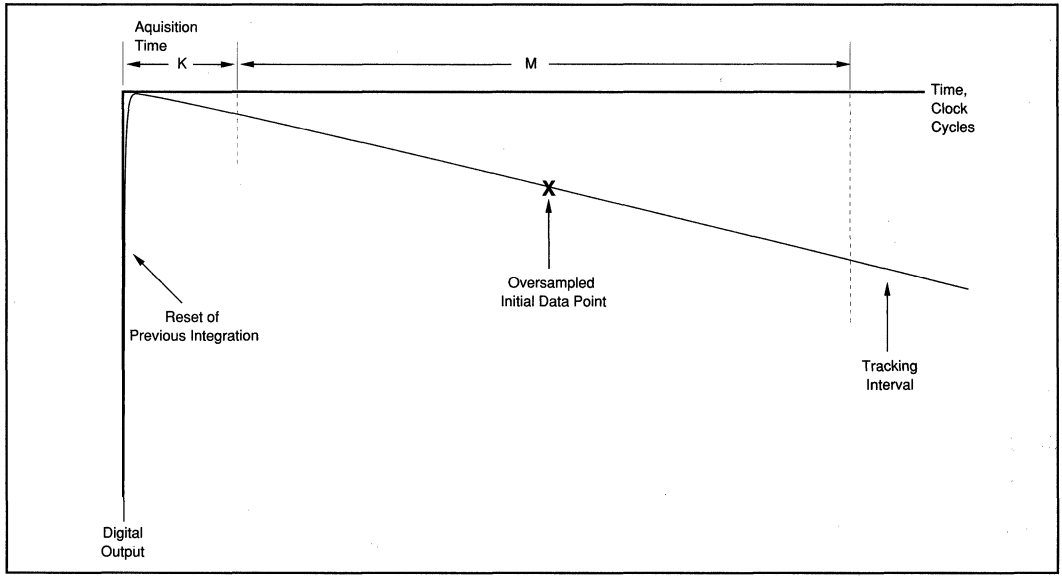


FIGURE 12. Close-up of Initial Oversampled Data Point for DDC101.

has been completed; this occurs M clock periods after the FDS transition to "ON". Acquisition, Initial Data Point and Tracking for the next integration follow automatically. The DDC101 continues in the Tracking mode until the next FDS command initiates the measurement of the M final data point samples. An FDS command is needed for each integration cycle. In the continuous integration mode, the FDS pulse width must be less than M clock periods. If the FDS pulse is held low past this time of M clock periods, the DDC101 will reset as for non-continuous mode (see also Figure 4).

In the continuous mode of operation, the tracking logic of the DDC101 "remembers" the integration rate of the previous integration and begins the next integration at the rate of the previous integration. This allows faster acquisition of the signal for the next integration.

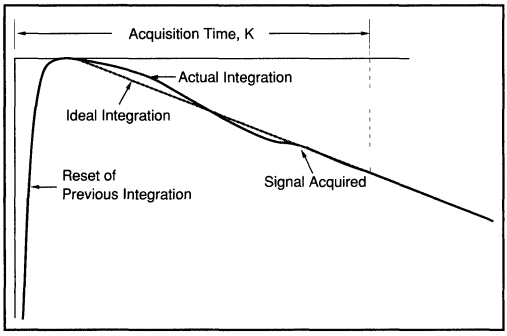


FIGURE 13. Close-up of Reset and Acquisition Time for DDC101.

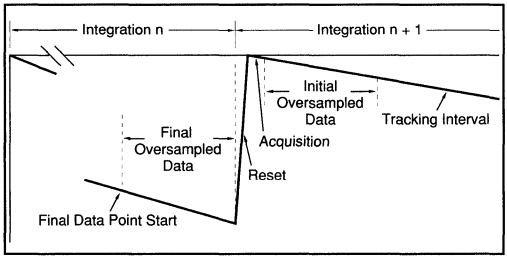


FIGURE 14. Close-up of End of One Integration Cycle and Beginning of Next.

NON-CONTINUOUS INTEGRATION MODE

For the non-continuous integration mode, FDS controls the start of the M final data point samples and the end of integration as discussed above. In this mode, however, FDS is also used to control the start of a new integration cycle asynchronously with the end of the previous integration. When FDS transitions to "ON", the collection of the M final data point samples begins. At the end of each integration, the DDC101 automatically resets the integration capacitance. If FDS remains "ON" past the end of integration, the DDC101 will stay in the integration reset state until FDS transitions to "OFF". Holding FDS "ON" past the end of integration will also reset the DDC101's tracking logic to zero integration rate.

In non-continuous integration mode, the initial data point measurement may be less accurate since the DDC101's internal tracking logic is reset at the beginning of the integration and tracking may not be accurate for the initial data point measurement. In this situation, Correlated Double Sampling (CDS) operation may not be advantageous.

INTERNAL ERROR CORRECTION

The DDC101 uses CDS techniques to gain optimum performance. CDS removes internal DDC101 errors which occur for a given integration cycle such as, charge injection, kT/C, and DDC101 offset errors. Correlated Double Sampling is user selectable. It is recommended for most continuous measurement applications.

Correlated Double Sampling is implemented in the DDC101 by subtracting the Initial Data Point from the Final Data Point. Thus, the error correction is updated automatically for each integration. When operating in the unipolar input range, CDS functions with either output data format—straight binary or binary two's complement. When operating in the bipolar input range, CDS functions with binary two's complement output data format only.

The errors that CDS removes are charge injection, kT/C and DDC101 input voltage offset. These errors are very difficult to eliminate in equivalent analog circuits. Charge injection errors result from charge that is transferred through the reset switch into the integration capacitor. kT/C errors are switching errors due to the noise of the resistance of the reset switch. DDC101 voltage offset errors are due to input offset of the input comparator. Both initial offset and offset drift with time and temperature are corrected since the correction is performed each integration cycle.

SINGLE CYCLE INTEGRATION

The DDC101 acquires charge (q) by integrating input current (i) for a specific time (T). That is,

$$q = \int_{O}^{T} i\,dt$$

The DDC101 acquires up to 500pC of full scale charge per integration cycle in the unipolar input range, and approximately ±250pC of full scale charge in the bipolar input range. Therefore, for the DDC101, maximum values can be calculated.

Unipolar Input Range	Bipolar Input Range
$500pC = I_{FS} \times T_{INT}$	$\pm 250pC = \pm I_{FS} \times T_{INT}$

Where I_{FS} is the full scale input current and T_{INT} is the integration time of the DDC101. Examples of I_{FS} and T_{INT} that equal 500pC and ±250pC are shown in the following tables.

The maximum average input current that the DDC101 can integrate is 7.8µA. This results in a minimum integration time of 64µs for unipolar inputs and 32µs for bipolar inputs. Further flexibility is possible with multiple integration cycles per conversion as described in the following text.

INPUT RANGE

Unipolar Input Range

For the unipolar input range, the range of charge for each integration cycle is from positive full scale of +500pC to a slightly negative charge of –1/256 (approximately –0.4%) of the positive full scale charge. This is +500pC to –1.95pC. The negative charge measurement capability allows for low level PC board parasitic leakages.

Bipolar Input Range

For the bipolar input range, the range of charge for each integration cycle is from positive full scale of +250pC to negative full scale of –251.95pC.

I_{FS}	T_{INT}
1nA	500ms
10nA	50ms
100nA	5ms
1µA	500µs
5µA	100µs
7.8µA	64µs

TABLE III. Input Current vs Integration Time Examples for Maximum Charge. Unipolar input range maximum charge = 500pC.

$\pm I_{FS}$	T_{INT}
1nA	250ms
10nA	25ms
100nA	2.5ms
1µA	250µs
2.5µA	100µs
7.8µA	32µs

TABLE IV. Input Current vs Integration Time Examples for Maximum Charge. Bipolar input range maximum charge = ±250pC.

MULTIPLE INTEGRATIONS PER CONVERSION CYCLE

If more than 500pC, unipolar (or ±250pC, bipolar) of charge must be integrated in one conversion cycle, the DDC101 can be user programmed for multiple integrations per conversion cycle. This feature can be used to provide for longer conversion periods for a specific input current other than shown in the previous table. The integration cycles forming a conversion cycle may be continuous or non-continuous. The number of integrations per conversion cycle, L, can be 1, 2, 4, 8, 16, 32, 64, 128, or 256. The multiple integrations are automatically averaged in the DDC101 so that one conversion result is output per total conversion cycle. Note that each integration requires individual control by the FDS signal. For example, if L = 4, then four FDS signals per conversion are required.

FINAL DATA POINT CONFIGURATION LIMITS

In each conversion cycle, the maximum number of final data points which can be collected is 256. This means that at the extremes, the DDC101 can be setup to perform one integration cycle with 256 oversamples, or the DDC101 can be setup to perform 256 integration cycles with one sample per integration cycle. The total number of integrations, L, multiplied by the number of samples per final data point, must be 256 or less. As an example, if 16 integration cycles, L, are used, the number of samples per final data point must be 16 or less.

NOTE: When CDS is used, the initial data points impose no additional conversion sampling limitations.

FREQUENCY RESPONSE

The DDC101 charge digitizing A/D Converter is a sampled system whose frequency response has three separate components. These components are multiplied together to make the total frequency characteristic of the DDC101. The three frequency response components are shown below. Each individual component has a sinc (sinx/x) frequency response function.

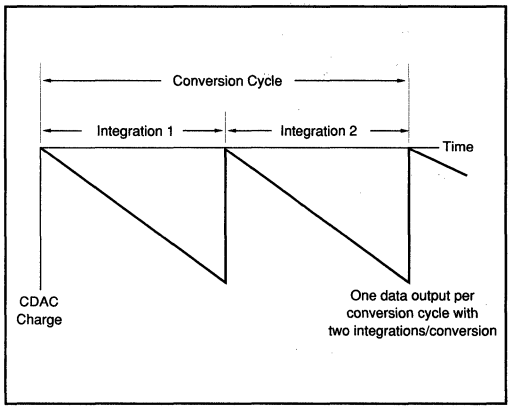


FIGURE 15. Conversion Cycle with Two Integrations.

INTEGRATIONS PER CONVERSION	I_{FS}	CONVERSION TIME	MAX CHARGE/ CONVERSION
L = 1	10nA	50ms	500pC
L = 2	10nA	100ms	1000pC
L = 4	10nA	200ms	2000pC
L = 8	10nA	400ms	4000pC
L = 16	10nA	800ms	8000pC
L = 32	10nA	1.6s	16000pC
L = 64	10nA	3.2s	32000pC
L = 128	10nA	6.4s	64000pC
L = 256	10nA	12.8s	128000pC

TABLE V. Integrations/Conversion vs Conversion Time. Example for multiple integrations with unipolar input range.

1. Basic Integration
   This is the characteristic sin(x)/x response of the basic integration function. This response is controlled by the measurement time of the DDC101, T_{MEAS}; see Figure 16.
2. Oversampling
   This is the low pass filter characteristic of the digital filter's oversampling. This response reduces the broadband noise in the input signal of the DDC101. Broadband noise decreases as the number of oversamples increases. This response is controlled by the number of oversamples, M; see Figure 17.
3. Multiple Integrations
   This is the low pass filter characteristic that results when the digital filter is used to average multiple integrations. This will determine the primary response of the DDC101 if two or more integrations are internally averaged. This response is controlled by the total conversion time of the DDC101; see Figure 18.

Input frequencies are multiplied by the DDC101 frequency response. The Nyquist frequency is $f_{CONV}/2$, where f_{CONV} is the DDC101 conversion rate. The highest frequency that can be reconstructed from the output data is $f_{CONV}/2$. Input frequencies above Nyquist are multiplied by the DDC101 frequency response and are then aliased into DC to $f_{CONV}/2$.

Basic Integration Frequency Response

The sin(x)/x basic integration characteristic is controlled by the digital filter's measurement time (T_{MEAS}). The measurement frequency, f_{MEAS} is $1/T_{MEAS}$. The input frequency response of the DDC101 is down –3dB at $f_{MEAS}/2.26$ with a null at f_{MEAS}. Subsequent nulls are at harmonics $2f_{MEAS}$, $3f_{MEAS}$, $4f_{MEAS}$, etc. as shown in the frequency response curve below. This characteristic is often used to eliminate known interference by setting f_{MEAS} or a harmonic to exactly the frequency of the interference. Table VI illustrates the frequency characteristics of the DDC101 integration function for various measurement times. As an example, for N = 2272, K = 16, and M = 256: $T_{MEAS} = (N-M-K)/f_{CLK}$ = (2272-256-16)/2MHz = 1ms and f_{MEAS} = 1kHz. T_{INT} = 2272/2MHz = 1.14ms; $f_{CONV} = 1/T_{INT}$ = 880Hz.

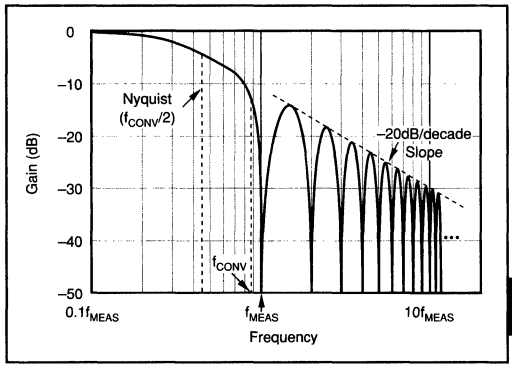


FIGURE 16. Basic Integration Frequency Response.

MEASUREMENT TIME	–3dB FREQUENCY	f_{MEAS}
100µs	4.42kHz	10kHz
1ms	442Hz	1kHz
10ms	44.2Hz	100Hz
16.66ms	26.5Hz	60Hz
20ms	22.1Hz	50Hz

TABLE VI. Basic Integration Frequency Response Examples.

Oversampling Frequency Response

The M oversamples of the initial and the final data points create an oversampling sin(x)/x type of low pass filter response. The oversampling function reduces broadband noise of the input signal and the DDC101. Broadband noise is reduced approximately in proportion to the square root of the number of oversamples, M. As an example, a conversion with 128 oversamples will have approximately 1/2 the noise of a conversion with 32 oversamples ($\sqrt{32/128} = \sqrt{1/4} = 1/2$) The oversampling low pass filter response creates a null at $f_{OS} = 1/T_{OS}$. The oversample time, T_{OS}, is M/f_{CLK}. For M = 256 and f_{CLK} = 2MHz, f_{OS} is approximately 7.8kHz. Subsequent nulls are at harmonics $2f_{OS}$, $3f_{OS}$, $4f_{OS}$, etc. The –3dB point is at $f_{OS}/2.26$. Table VII illustrates the DDC101 oversampling frequency characteristics with approximate values for f_{OS} and the –3dB frequency. An oversampling frequency response graph is shown below in Figure 17. This figure shows the frequency response for M = 256 oversamples with an f_{CLK} of 2MHz . The slope of the attenuation curve decreases at approximately 20dB/decade.

OVERSAMPLES (M)	–3dB FREQUENCY	f_{OS}
256	3.5kHz	7.8kHz
128	6.9kHz	15.6kHz
64	13.9kHz	31.2kHz
16	55kHz	125kHz

TABLE VII. Oversample Frequency Response Examples.

Normalized DDC101 Frequency Response

The normalized frequency response, H(f), of the DDC101 that is applied to the input signal consists of the product of the three frequency response components:

$$H(f) = \underbrace{\frac{\sin\left(\pi f\left(N-M-K\right)/f_{CLK}\right)}{\pi f\left(N-M-K\right)/f_{CLK}}}_{\text{Basic Integration}} \bullet \underbrace{\frac{\sin\left(\pi f M/f_{CLK}\right)}{M\sin\left(\pi f/f_{CLK}\right)}}_{\text{Oversampling}} \bullet \underbrace{\frac{\sin\left(\pi f LN/f_{CLK}\right)}{L\sin\left(\pi f N/f_{CLK}\right)}}_{\text{Multiple Integrations}} \bullet \underbrace{e^{-j\pi f(LN-K-1)/f_{CLK}}}_{\text{Linear Phase}}$$

Where:

f	is the signal frequency
f_{CLK}	is the system clock frequency, typically 2MHz
N	is the total number of clock periods in each integration time, $T_{INT} = N/f_{CLK}$, T_{INT} is the DDC101 CDAC's integration time
M	is the number of oversamples in one oversampled data point
K	is the number of clocks used in the acquisition time
$(N-M-K)/f_{CLK}$	is the digital filters measurement time, T_{MEAS}, ($T_{MEAS} = T_{INT} - (M+K)/f_{CLK}$)
M/f_{CLK}	is the oversample time, T_{OS}
LN/f_{CLK}	is the total conversion time for multiple integrations, T_{CONV}

The DDC101's transfer response has a linear phase characteristic as indicated by the exponential term.

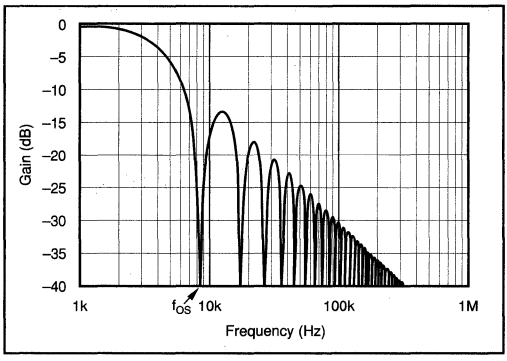


FIGURE 17. Oversampling Frequency Response for M = 256 (f_{CLK} = 2MHz).

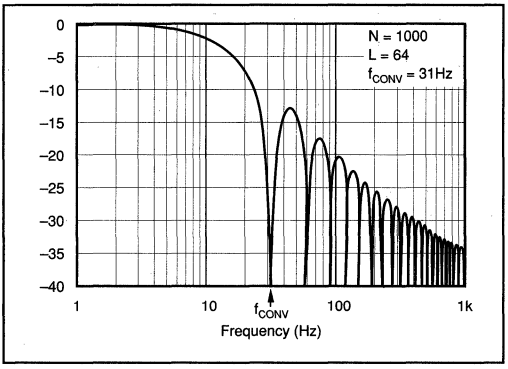


FIGURE 18. A Multiple Integration Frequency Response Example.

Multiple Integration Frequency Response

If the DDC101 is operated in the multiple integrations per conversion mode of operation, an additional sin(x)/x type low pass filter is created. The filter creates an initial null frequency at the conversion frequency, f_{CONV} of the DDC101 and at multiples of f_{CONV}. The –3dB point for this filter is also at $f_{CONV}/2.26$. The conversion time, T_{CONV}, is the sum of the integration times for multiple integrations that are averaged together by the DDC101. $T_{CONV} = LN/f_{CLK}$. $f_{CONV} = 1/T_{CONV}$. If multiple integrations per conversion are used, this filter will be the dominant low frequency filter of the DDC101. Table VIII shows examples of the conversion time and frequency for different parameter selections. Figure 18 shows an example of the frequency response due to Multiple Integrations. In the case of Figure 18, the integration time is 500µs (N = 1000 clock periods) and L = 64 integrations per conversion.

INTEGRATION TIME	L	CONVERSION TIME	–3dB FREQUENCY	f_{CONV}
1ms	2	2ms	221Hz	500Hz
1ms	8	8ms	55Hz	125Hz
1ms	16	16ms	27.5Hz	62.5Hz
1ms	64	64ms	6.9Hz	15.6Hz
1ms	256	256ms	1.73Hz	3.91Hz
10ms	2	20ms	22.1Hz	50.0Hz
10ms	8	80ms	5.5Hz	12.5Hz
10ms	16	160ms	2.75Hz	6.25Hz
10ms	64	640ms	0.69Hz	1.56Hz
10ms	256	2560ms	0.173Hz	0.39Hz

TABLE VIII. Multiple Integration Time Examples.

System Noise implications

The noise at the digital output of the DDC101 consists of system noise that is included in the analog input signal and noise from the DDC101.

DDC101 Noise—The noise of the DDC101 includes low frequency and broadband noise. The low frequency noise is reduced by the integrating function and the CDS function of the DDC101. This is reflected in the basic integration frequency response and in the multiple integration frequency response. The broadband electronic noise is reduced primarily by the oversampling function of the DDC101

Signal Noise—The noise of the input signal is filtered and reduced in a manner similar to the DDC101 noise reduction through the integrating and oversampling functions of the DDC101.

Figures 19 and 20 show the frequency response of the DDC101 for the product of the basic integration and oversampling frequency response for two different values of M. In both examples, the integration time is 1ms, the only difference is in the number of oversamples, M; for Figure 19, M = 256 oversamples was used; for Figure 20, M = 32 oversamples was used. The first null frequency is f_{MEAS} and subsequent nulls are at multiples of f_{MEAS}. The first example with the larger number of oversamples (M = 256) clearly reduces high frequency noise more than the second example with M = 32.

For M = 256, f_{OS} is 7.8kHz, f_{MEAS} is 1.16kHz, and the –3dB frequency is 507Hz. For M = 32, f_{OS} is 62.4kHz, f_{MEAS} is 1.02kHz and the –3dB frequency is 453Hz.

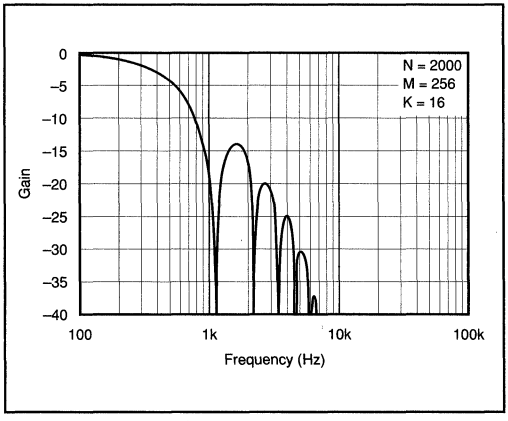


FIGURE 19. Product of Frequency Response of Basic Integration and Oversampling: 1ms Integration Time, 256 Oversamples.

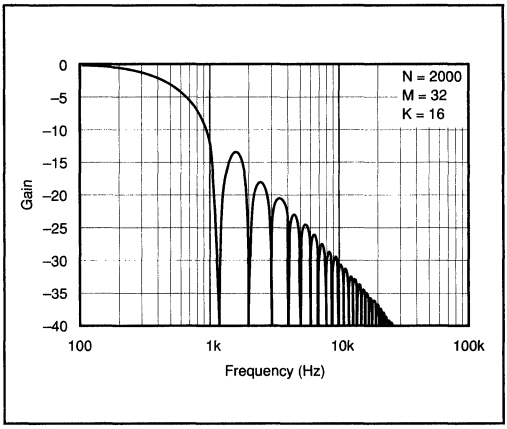


FIGURE 20. Product of Frequency Response of Basic Integration and Oversampling; 1ms Integration Time, 32 Oversamples.

Figure 21 shows the frequency response of the DDC101 and an ideal integrator with the same integration time. In this comparison, the DDC101 has greater bandwidth to the first null, but it also has greater out of band attenuation which reduces broadband noise significantly. If desired, the frequency response of the ideal integrator can be produced by passing the DDC101 output through an external digital filtering function which has the frequency response from DC to Nyquist of

$$\frac{\sin(\pi f T_{INT})}{\pi f T_{INT}} \bullet \frac{\pi f T_{MEAS}}{\sin(\pi f T_{MEAS})} \bullet \frac{M \sin(\pi f / f_{CLK})}{\sin(\pi f M / f_{CLK})} .$$

This has the effect of further attenuating undesired signals (noise) outside the "passband", further increasing the signal-to-noise ratio of the DDC101 and closely emulating the ideal integrator's signal accumulation characteristics.

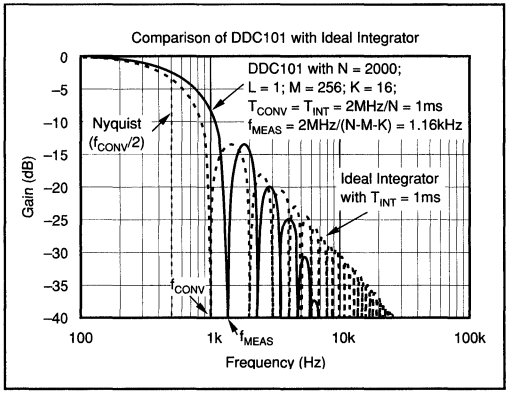


FIGURE 21. Comparison of DDC101 with Ideal Integrator.

SYSTEM SETUP

After power up, the Reset System and FDS signal inputs should be held low (active), while the SETUP register is loaded by the user. After the SETUP register is loaded, the Reset System input should transition to inactive while the FDS input remains active. The FDS should transition to inactive at the start of operation. Thereafter, Reset System should stay inactive and the FDS should be used to control each integration cycle.

SETUP INPUT

Software Control

Many of the options of the DDC101 are set through a serial bit stream transmitted by the user into the SETUP Input pin. The 12-bit word transmitted into the SETUP Input is used to set the following four options, in sequence:

1. Acquisition Time Control, K	2 bits
2. Oversampling Control Samples/Integration, M	4 bits
3. Multiple Integration Control Integrations/Conversion, L	4 bits
4. Unipolar or Bipolar Input Range	1 bit
5. Output Format	1 bit
Total for SETUP	12 bits

See Figure 5: SETUP Timing Diagram.

Acquisition Time Control, K

This signal sets the acquisition time (K clock periods) and controls the use of Correlated Double Sampling. The acquisition time occurs at the start of each new integration. The acquisition time control can be set to four options: "no CDS", 1, 16 or 32 clock periods. For typical continuous integration applications, K = 16 is recommended. The acquisition time always begins with one clock period for reset. This reset clock period is followed by 0, 15 or 31 clock periods for signal acquisition. Correlated Double Sampling is activated if the initial acquisition time is set to 1, 16 or 32 clock periods. Correlated Double Sampling is disabled and the Initial Data Point is not acquired if "no CDS" is selected.

K	RESET CLOCKS	ACQUISITION CLOCKS	CDS
"No CDS"	1	0	Disabled
1	1	0	Enabled
16	1	15	Enabled
32	1	31	Enabled

TABLE IX. Acquisition Time Control, K.

When Correlated Double Sampling is activated, the DDC101 acquires the initial data point for error correction as part of each conversion. At the end of the conversion cycle, the initial data point is subtracted from the final data point. The errors that are corrected with CDS are charge injection, kT/C noise, and DDC101 voltage offset. When Correlated Double Sampling is deactivated, the initial data point is not taken.

When operating in the unipolar input range, CDS functions with either output data format—straight binary or binary two's complement. When operating in the bipolar input range, CDS functions correctly only with binary two's complement output data format.

Oversampling Control Samples/Integration, M

This control sets the number of samples, M, used by the DDC101 to oversample the initial and final data points. M can be set for these values: 1, 2, 4, 8, 16, 32, 64, 128, 256. Broadband noise in the conversion is reduced roughly in proportion to the square root of M. Therefore, a conversion with 128 oversamples will have 1/2 the broadband noise of a conversion with 32 oversamples. See the previous frequency response discussion.

Multiple Integration Control, L

This control sets the number of integrations per conversion cycle, L. It is used to reduce the data rate, increase the magnitude of the input signal range, and/or reduce the noise. The product of L and M must be 256 or less.

Output Format

Two output formats are available for either the unipolar or bipolar input ranges:

Binary Two's Complement (BTC) and Straight Binary.

UNIPOLAR INPUT RANGE

For Binary Two's Complement, output data format, the output word is a 21-bit Two's Complement word. The first bit is the sign bit followed by the Most Significant Bit (MSB), etc. The output range is +100%FS to –0.4%FS, where FS is 500pC.

CODE	INPUT SIGNAL	
0 1111 1111 1111 1111 1111	+100%FS	+500pC
0 1111 1111 1111 1111 1110	+100%FS –1LSB	
0 0000 0000 0000 0000 0001	+1SLB	
0 0000 0000 0000 0000 0000	Zero	0pC
1 1111 1111 1111 1111 1111	–1LSB	
1 1111 1111 0000 0000 0000	–0.4%FS	–1.95pC

TABLE X. BTC Code Table—Unipolar Input Range.

For Straight Binary output data format, the output is a 20-bit straight binary word. The first bit is the Most Significant Bit (MSB), etc. The output range is +99.6%FS to –0.4%FS in which +99.6%FS represents positive full scale and –0.4%FS represents the minimum input.

CODE	INPUT SIGNAL	
1111 1111 1111 1111 1111	+99.6%FS	498.05pC
1111 1111 1111 1111 1110	+99.6%FS –1LSB	
0000 0001 0000 0000 0001	+1LSB	
0000 0001 0000 0000 0000	Zero	
0000 0000 0000 0000 0000	–0.4%FS	–1.95pC

TABLE XI. Straight Binary Code Table — Unipolar Input Range.

BIPOLAR INPUT RANGE

For Binary Two's Complement, output data format, the output word is a 21-bit Two's Complement word. The first bit is the sign bit followed by the Most Significant Bit (MSB), etc. The output range is +100%FS to –100.8%FS, where FS is 250pC. For the bipolar input range, the output code table changes with the use of Correlated Double Sampling (CDS). (There is no difference with or without CDS in the output code table when using the unipolar input range.)

CODE	INPUT SIGNAL	
0 1111 1111 1111 1111 1111	+100%FS	+250pC
0 1111 1111 1111 1111 1110	+100%FS –1LSB	
0 1000 0000 0000 0000 0001	+1LSB	
0 1000 0000 0000 0000 0000	Zero	0pC
0 0111 1111 1111 1111 1111	–1LSB	
0 0000 0000 0000 0000 0001	–100%FS + 1SLB	
0 0000 0000 0000 0000 0000	–100%FS	–250pC
1 1111 1111 0000 0000 0000	–100.8%FS	–251.95pC

TABLE XII. BTC Code Table — Bipolar Input Range without CDS.

CODE	INPUT SIGNAL	
0 0111 1111 1111 1111 1111	+100%FS	+250pC
0 0111 1111 1111 1111 1110	+100%FS – 1LSB	
0 0000 0000 0000 0000 0001	+1LSB	
0 0000 0000 0000 0000 0000	Zero	0pC
1 1111 1111 1111 1111 1111	–1LSB	
1 1000 0000 0000 0000 0001	–100%FS + 1LSB	
1 1000 0000 0000 0000 0000	–100%FS	–250pC
1 0111 1111 0000 0000 0000	–100.8%FS	–251.95pC

TABLE XIII. BTC Code Table — Bipolar Input Range with CDS.

For Straight Binary output data format with the bipolar input range, the output is a 20-bit straight binary word. The first bit is the Most Significant Bit (MSB), etc. The output range is +100%FS to –100%FS in which +100%FS represents positive full scale and –100%FS represents the negative full scale. *When using the straight binary output data format in bipolar input range, do not use CDS. This will cause a negative overflow to occur.*

CODE	INPUT SIGNAL	
1111 1111 1111 1111 1111	+100%FS	+250pC
1111 1111 1111 1111 1110	+100%FS – 1LSB	
1000 0000 0000 0000 0001	+1LSB	
1000 0000 0000 0000 0000	Zero	0pC
0111 1111 1111 1111 1111	–1LSB	
0000 0000 0000 0000 0000	–100%FS	–250pC

TABLE XIV. Straight Binary Code Table — Bipolar Input Range without CDS.

SETUP INPUT CODE

Acquisition Time Control—K - 2 bits

CODE	RESULT
00	1 Reset clock period, 0 clock period Acquisition Time, CDS disabled, no initial data point,
01	1 Reset clock period, 0 clock period Acquisition Time
10[1]	1 Reset clock period, 15 clock period Acquisition Time
11	1 Reset clock period, 31 clock period Acquisition Time

NOTE: (1) Recommended for continuous integration mode.

Oversampling Control
Samples/Integration—M - 4 bits

CODE	SAMPLES PER INTEGRATION
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1XXX	256

Multiple Integration Control
Integrations/Conversion—L - 4 bits

CODE	INTEGRATIONS PER CONVERSION
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1XXX	256

Input Range - 1 bit

CODE	INPUT RANGE
0	Unipolar
1	Bipolar

Output Format - 1 bit

CODE	OUTPUT FORMAT
1	Binary Two's Complement
0	Straight Binary

SECTION 7
APPLICATIONS INFORMATION

BASIC PRINTED CIRCUIT BOARD LAYOUT

As with any precision circuit, careful printed circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pin. Digital signals should be kept as far from the analog input signals as possible on the PC board.

Leakage currents between PC board traces can exceed the input bias current of the DDC101 if care is not taken. A circuit board "guard" pattern for the analog input pin and for the PC board trace that connects to the analog input pin is recommended. The guard pattern reduces leakage effects by surrounding the analog input pin and trace with a low impedance analog ground. Leakage currents from other portions of the circuit will flow harmlessly to the low impedance analog ground rather than into the analog input of the DDC101. Analog ground pins are placed on either side of the analog input pin in the DDC101 package to allow convenient layout of guard patterns. Figure 22 illustrates the use of guard patterns to protect the analog input.

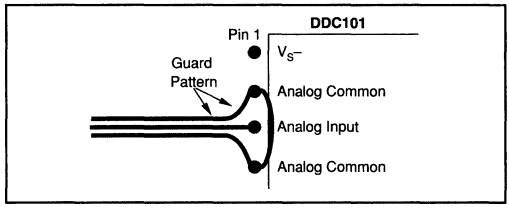


FIGURE 22. PC Board Layout Showing "Guard" Traces Surrounding Analog Input Pin and Traces.

Power Supplies

The ±5VDC supplies of the DDC101 should be bypassed with 10µF solid tantalum capacitors and 0.1µF ceramic capacitors. The supplies should each have a 10µF solid tantalum capacitor at a central point on the PC board. Each of the DDC101 power supply lines (V_S+, V_S-, $V_{DD}+$) should have a separate 0.1µF ceramic capacitor placed as close to the DDC101 package as possible.

The digital power supply voltage, $V_{DD}+$ must be equal to or less than the analog power supply voltage, V_S+. The analog power supply, V_S+, is connected to pins 5 and 6, these pins should be hardwired together on the printed circuit board at the pins for best performance.

$V_{DD}+$ should be as quiet as possible with minimal noise coupling. It is particularly important to eliminate noise from $V_{DD}+$ that is non-synchronous with DDC101 operation. Figure 23 illustrates two acceptable ways to supply $V_{DD}+$ power to the DDC101. The first case shows two separate +5VDC supplies for $V_{DD}+$ and V_S+. The second case shows the $V_{DD}+$ power supply derived from the V_S+ supply as used on the DDC101 Evaluation Fixture Device Under Test (DUT) board.

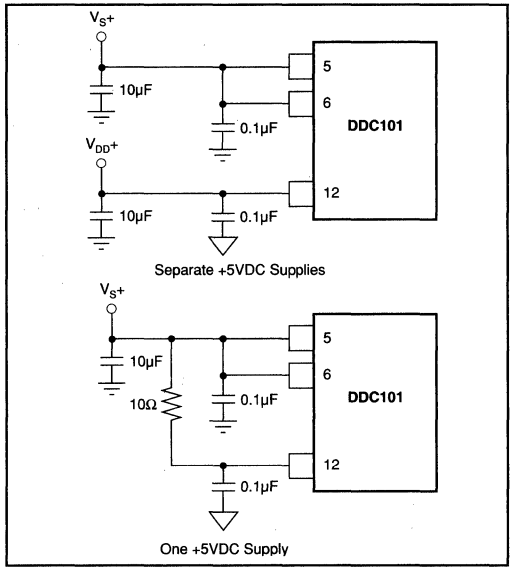


FIGURE 23. Positive Supply Connection Options.

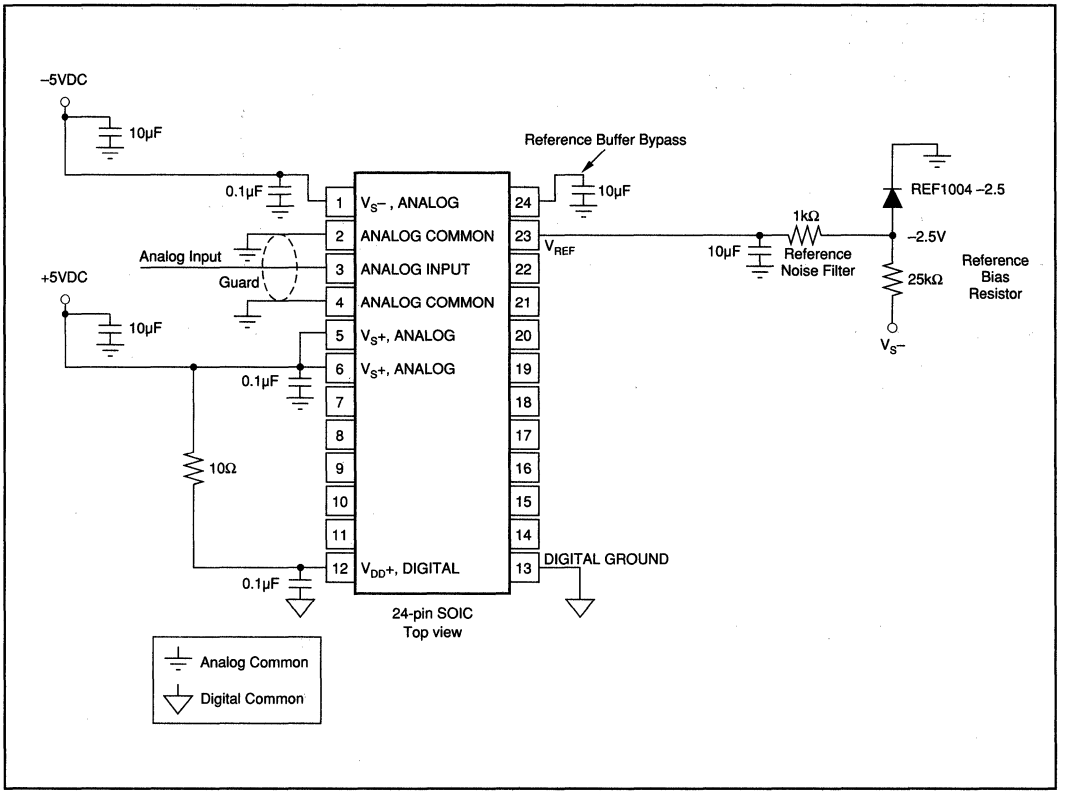


FIGURE 24. Example of Basic DDC101 Circuit Connections, SOIC Package.

Reading Data Output

Data from the previous conversion can be read any time after the $\overline{\text{DATA VALID}}$ output is activated and before the end of the next conversion. Data is held in an internal serial shift register until the end of the next conversion. The data must be completely read before the end of the next conversion or it will be overwritten with new data.

Recommended Setup

The following Setup parameters are recommended, in general, for use with the DDC101 with integration times of 1ms or longer. Multiple integrations per conversion, where practical, will provide lowest noise as illustrated in the typical performance curves.

Measurement Time Calculation

FUNCTION	RECOMMENDED
Acquisition Clocks, K	16
Oversamples, M	128
CDS	Enabled

A Continuous Integration Cycle consists of the Acquisition Time, Initial Data Point Collection, Tracking Interval, and Final Data Point Collection. The user can select these functions as illustrated in Table XV.

The time between "Final Data point Start" commands is the Integration Time, T_{INT}. The Measurement Time, T_{MEAS}, is the Integration time reduced by the Acquisition Time and by the Oversampling Time, T_{OS}.

$$T_{MEAS} = T_{INT} - T_{ACQ} - T_{OS}.$$

When CDS is used; T_{OS}, the oversampling time, is the time required to collect a data point (M clock periods). Each group of samples is averaged with the result at the midpoint of each sample group. Therefore, with CDS, T_{OS} = M clock periods. This is shown in Figure 25.

Two calculations of the Measurement Time are shown

FUNCTION	CLOCK CYCLES	USER CONTROLLED
Acquisition Time, K	1, 16, 32	Yes
Initial Data Point Samples, M(1)	1, 2, 4, 8, 16, 32,64, 128, 256	Yes
Tracking Interval	Variable	Yes
Final Data Point Samples, M(1)	1, 2, 4, 8, 16, 32, 64, 128, 256	Yes

NOTE: (1) Will be the same in CDS mode, initial Data Point Samples = 0 in non-CDS mode.

TABLE XV. Components of Integration Cycle.

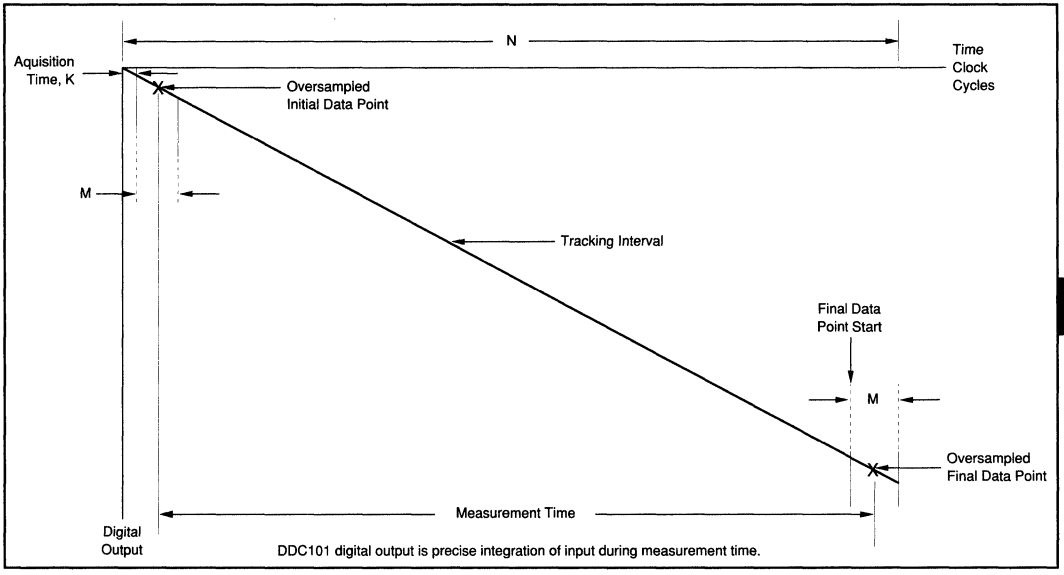


FIGURE 25. DDC101 Equivalent Integrator Output for Single Integration with CDS.

FUNCTION	USER SETTING (Clock Cycles)	TIME	MEASUREMENT (Calculated)
Integration Time (T_{INT})		1ms	
Acquisition Time K (T_{ACQ})	16	8µs	
Initial Data Point Samples, M	128	64µs	
Measurement Time			928µs
Final Data Point Samples, M	128	64µs	

TABLE XVI. Measurement Time with CDS.

FUNCTION	USER SETTING (Clock Cycles)	TIME	MEASUREMENT (Calculated)
Integration Time (T_{INT})		1ms	
Acquisition Time, K (T_{ACQ}) "No CDS"	1	0.5µs	
Initial Data Point Samples	None	0µs	
Measurement Time			967.5µs
Final Data Point Samples, M	128	64µs	

TABLE XVII. Measurement Time without CDS.

below: one with Correlated Double Sampling (CDS) and the other without CDS. Each example assumes that the recommended system clock frequency of 2MHz is used and that the time between "Final Data point Start" commands, (the integration time, T_{INT}) is 1ms.

Example with CDS. The Measurement Time with CDS is calculated as the Integration Time (T_{INT}) of 1ms less T_{ACQ} and T_{OS}. T_{OS}, the oversampling time, is 1/2 of the Initial Data Point time plus 1/2 the Final Data Point time since each group of samples is averaged with the result at the midpoint of each sample group.

Therefore, the Measurement Time = 1ms –(8 + 32 + 32)µs
= 928µs.

Example without CDS. The Measurement Time without CDS is calculated as the Total Integration Time (T_{INT}) of 1ms less T_{ACQ} and T_{OS}. T_{OS}, the oversampling time, is 1/2 of the Final Data Point time since this group of samples is averaged with the result at the midpoint of the sample group.

Therefore, the Measurement Time = 1ms –(0.5 + 32)µs
= 967.5µs.

Input Current Calculation

The following formula calculates the input current from the actual DDC output:

With CDS:

$$i = \frac{500pC \bullet \left[\frac{DDC\,output}{2^{20}}\right]}{T_{MEAS}}$$

$$i = \frac{500pC \bullet \left[\frac{DDC\,output}{2^{20}}\right]}{T_{INT} - K\ clock\ periods - M\ clock\ periods}$$

Without CDS:

$$i = \frac{500pC \bullet \left[\frac{DDC\,output}{2^{20}}\right]}{T_{MEAS}}$$

$$i = \frac{500pC \bullet \left[\frac{DDC\,output}{2^{20}}\right]}{T_{INT} - K\ clock\ periods - M/2\ clock\ periods}$$

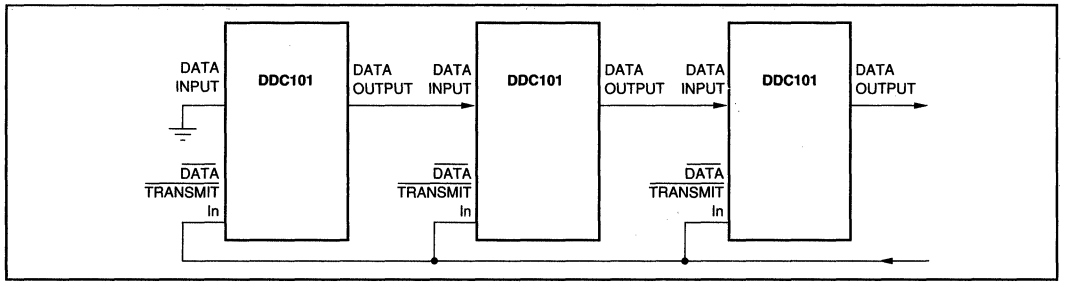


FIGURE 26. Daisy Chained DDC101s.

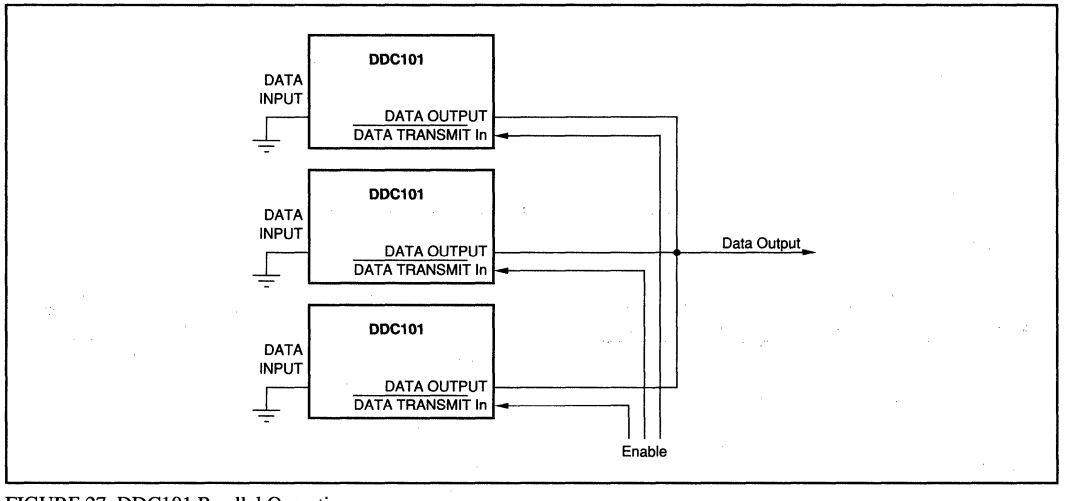


FIGURE 27. DDC101 Parallel Operation.

MULTIPLE DDC101 OPERATION

Multiple DDC101 units can be connected in serial or parallel configuration as illustrated in Figures 26 and 27.

DATA OUTPUT can be used with DATA INPUT to "daisy chain" the output of several DDC101 units together to minimize wiring; in this mode of operation, the serial data output is shifted through multiple DDC101s (Figure 26).

DATA OUTPUT is in a high impedance state until $\overline{\text{DATA TRANSMIT}}$ In is active. In this way, several DDC101 units can be connected in parallel to be enabled by the $\overline{\text{DATA TRANSMIT}}$ In line (Figure 27).

DDC101 EVALUATION FIXTURE

The DEM-DDC101P-C Evaluation Fixture is highly recommended for initial evaluation of the DDC101. It is designed for ease of use. The only additional equipment required to do a complete evaluation of the performance of the DDC101 is an IBM compatible PC with EGA or VGA graphics, a parallel interface port, a laser printer (optional), a ±5VDC power supply, and a signal source.

The DEM-DDC101P-C software is mouse compatible and retrieves data from up to 32 DDC101s in an easy to read, graphical format on the screen. The DEM-DDC101P-C Evaluation Fixture includes a PC Interface Board (with necessary parts), a DDC101 Board, a 25-pin ribbon connector and a 34-pin ribbon connector. The PC Interface Board makes timing commands and access to and from the DDC101 test board possible through the provided PC software. Data sheet, LI-439, provides complete information describing the evaluation fixture.

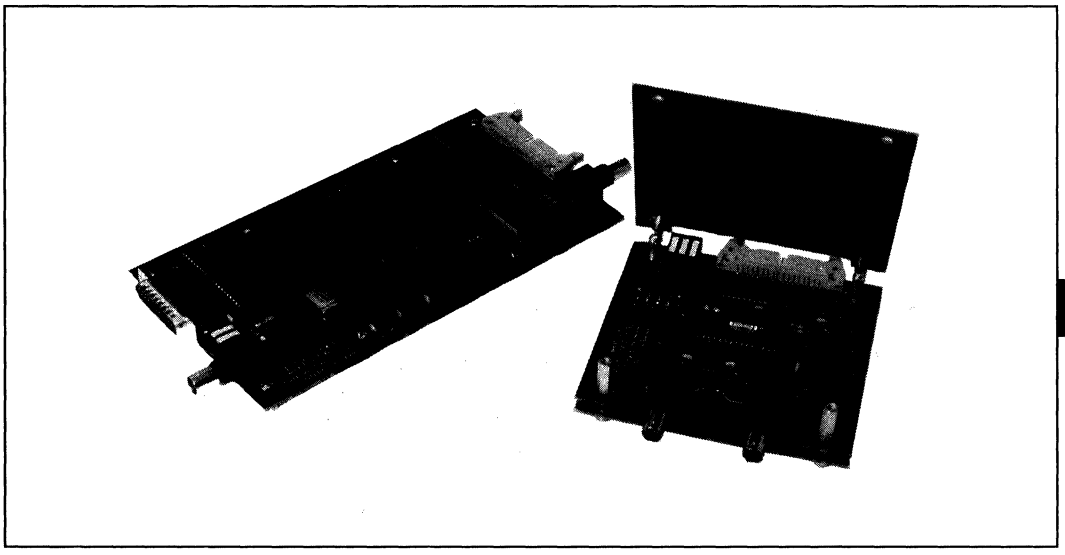


FIGURE 28. Photo of DEM-DDC101P-C Evaluation Fixture.

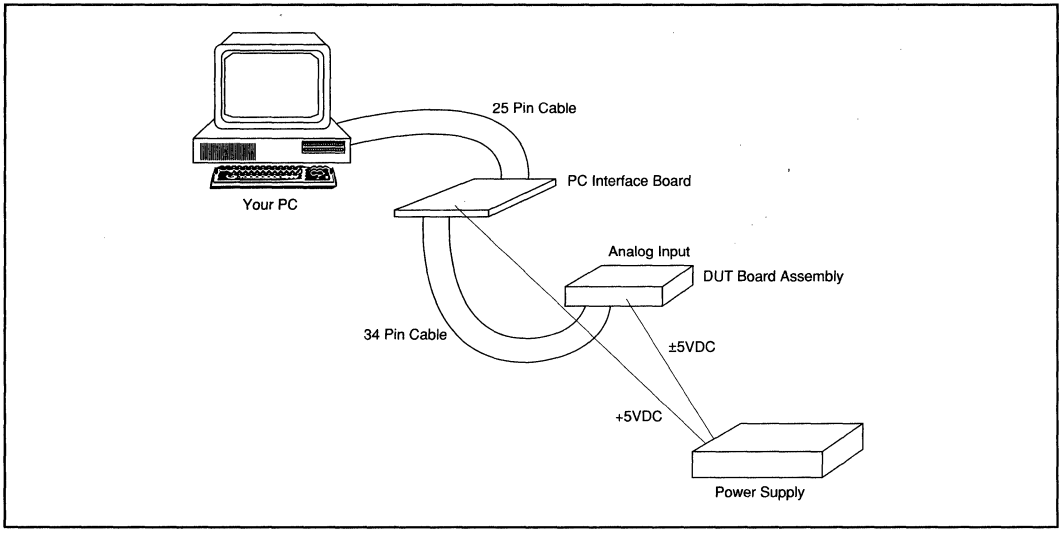


FIGURE 29. DEM-DDC101P-C Evaluation Fixture Connection Diagram.

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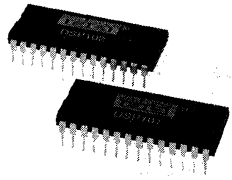


DSP101
DSP102

DSP-Compatible Sampling Single/Dual ANALOG-TO-DIGITAL CONVERTERS

FEATURES

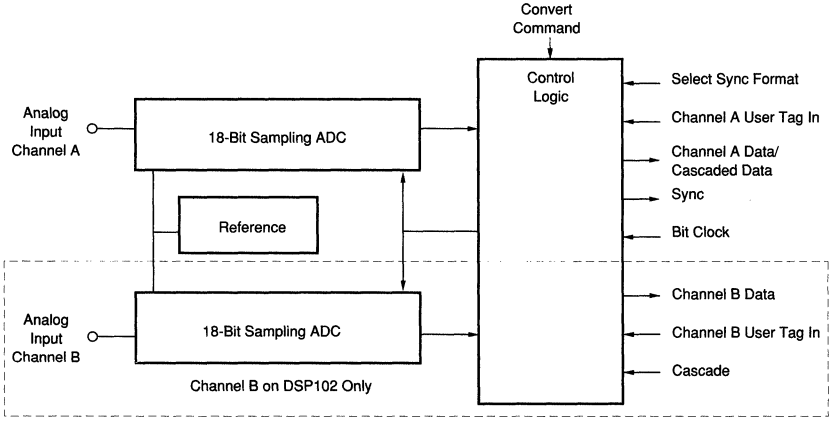
- **ZERO-CHIP INTERFACE TO STANDARD DSP ICs: AD, AT&T, MOTOROLA, TI**
- **SINGLE CHANNEL: DSP101**
- **DUAL CHANNEL: DSP102**
  Two Serial Outputs or Cascade to Single 32-Bit Word
- **SAMPLING RATE TO 200kHz**
- **DYNAMIC SPECIFICATIONS:**
  Signal/(Noise + Distortion) = 88dB;
  Spurious-Free Dynamic Range = 94dB;
  THD = –91dB
- **SERIAL OUTPUT DATA COMPATIBLE WITH 16-, 24-, AND 32-BIT DSP IC FORMATS**

DESCRIPTION

The DSP101 and DSP102 are high performance sampling analog-to-digital converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide full sampling and conversion at rates up to 200kHz.

The DSP101 offers a single conversion channel, with 18 bits of serial data output, allowing the user to drive 16-bit, 24-bit, or 32-bit DSP ports. The DSP102 offers two complete conversion channels, with either two full 18-bit output ports, or a mode to cascade two 16-bit conversions into a 32-bit port as one word.

Both the DSP101 and DSP102 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1068C

SPECIFICATIONS

ELECTRICAL

At T_A = 0°C to 70°C, ±2.75V input signal, sampling frequency (f_S) = 200kHz, V_{A+} = V_D = +5V, V_{A-} = –5V, 16MHz external clock on OSC1, CLKOUT tied to CLKIN, 8MHzdata transfer clock on XCLK, data analysis band-limited to 20kHz, unless otherwise specified.

PARAMETER	CONDITIONS	DSP101JP DSP102JP MIN	DSP101JP DSP102JP TYP	DSP101JP DSP102JP MAX	DSP101KP DSP102KP MIN	DSP101KP DSP102KP TYP	DSP101KP DSP102KP MAX	UNITS
RESOLUTION				18			*	Bits
ANALOG INPUT								
Voltage Range			±2.75V			*		V
Impedance			1			*		kΩ
Capacitance			20			*		pF
THROUGHPUT SPEED								
Complete Cycle	Acquisition + Conversion			5			*	µs
Throughput Rate		200			*			kHz
AC ACCURACY(1)								
Signal-to-(Noise + Distortion) Ratio	f_{IN} = 1kHz	83	86		86	88		dB(2)
	f_{IN} = 1kHz (–60dB)		32			*		dB
	f_{IN} = 25kHz		82			*		dB
Total Harmonic Distortion	f_{IN} = 1kHz		–90	–86		–91	–89	dB
Spurious-Free Dynamic Range	f_{IN} = 1kHz	89	92		92	94		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 1kHz	84	88		87	89		dB
DC ACCURACY								
Gain Error				±5			*	%
Gain Error Mismatch	DSP102 Channels			±2			*	%
Integral Linearity	±2.75V Input Range		Sufficient to meet AC Accuracy Specifications					
Differential Linearity	±2.75V Input Range		Sufficient to meet AC Accuracy Specifications					
Integral Linearity Error	±0.7V Input Range		±0.003			*		%
Differential Linearity Error	±0.7V Input Range		±0.002			*		%
No Missing Codes	±0.7V Input Range		14			*		Bits
Bipolar Zero Error (3)			±2					mV
Bipolar Zero Mismatch (3)	DSP102 Channels		±2					mV
Power Supply Sensitivity	–5.25V < V_{A-} < –4.75V		–60			*		dB
	+4.75V < V_{A+}, V_{D+} < +5.25V		–60			*		dB
SAMPLING DYNAMICS								
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps, rms
Transient Response			1			*		µs
Overvoltage Recovery			5			*		µs
DIGITAL INPUTS								
Logic Levels (Except OSC1)								
V_{IL}	I_L = ±10µA	0		+0.8	*		*	V
V_{IH}	I_H = ±10µA	+2.4		+5	*		*	V
OSC1 Clock			74HC Compatible					
Frequency				16				MHz
Data Transfer Clock (XCLK)								
Frequency		0.1		12	*		*	MHz
Duty Cycle		40	50	60	*		*	%
Conversion Clock (CLKIN)								
Frequency		0.5		5.33	*		*	MHz
Duty Cycle		25	33	55	*	*	*	%
DIGITAL OUTPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded 32-bit Mode					
Coding			Binary Two's Complement					
Logic Levels (Except OSC2)								
V_{OL}	I_{SINK} = 4mA	0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 4mA	+2.4		+5	*		*	V
OSC2			Can only be used to drive crystal oscillator.					
Conversion Clock (CLKOUT)								
Drive Capability		±2mA			*			mA
POWER SUPPLIES								
Rated Voltage								
V_{A+}		+4.75	+5	+5.25	*	*	*	V
V_{A-}		–5.25	–5	–4.75	*	*	*	V
V_D		+4.75	+5	+5.25	*	*	*	V
Power Consumption	XCLK = OSC1 = 12MHz		250	425		*	*	mW
Supply Current	XCLK = OSC1 = 12MHz							
I_{A+}			30	45		*	*	mA
I_{A-}			–18	–25		*	*	mA
I_D			5	15		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		–65		+125	*		*	°C

NOTES: (1) All dynamic specifications are based on 2048-point FFTs, using four-term Blackman-Harris window. (2) All specifications in dB are referred to a full-scale input, ±2.75Vp-p. (3) Adjustable to zero with external potentiometer.

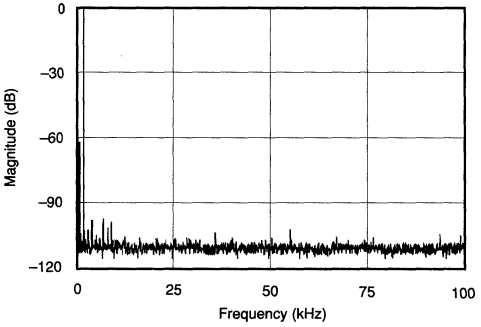
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_A+ = V_{D+} = +5V, V_A- = V_D- = –5V, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = 80f_S = 16MHz, XCLK = 40f_S = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

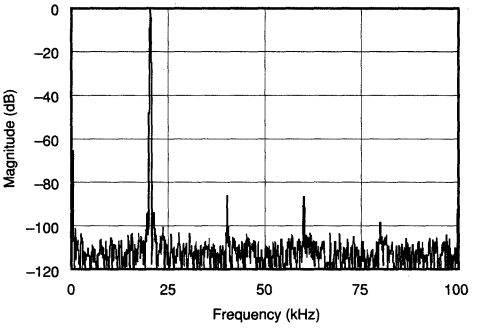
SINAD means Signal-to-(Noise + Distortion) Ratio.
SNR means Signal-to-Noise Ratio excluding harmonics thru the 8th.

THD means Total Harmonic Distortion thru 8th harmonic.
SFDR means Spurious Free Dynamic Range, including harmonics.

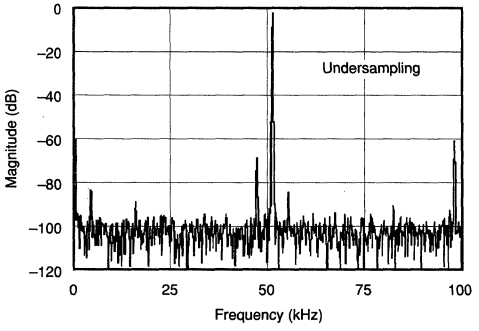
FREQUENCY SPECTRUM of ±2.75V, 1kHz INPUT
(Average of 12 FFTs, No Window Used)



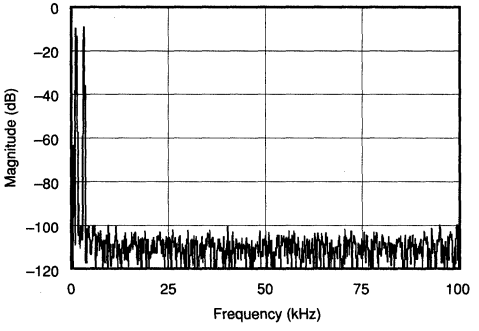
FREQUENCY SPECTRUM of ±2.75V, 20kHz INPUT
(Using Four-Term Blackman-Harris Window)



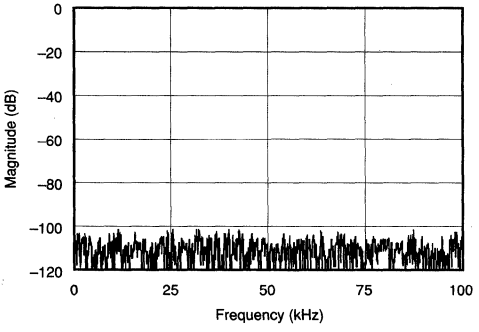
FREQUENCY SPECTRUM of ±2.75V, 451kHz INPUT
(Using Four-Term Blackman-Harris Window)



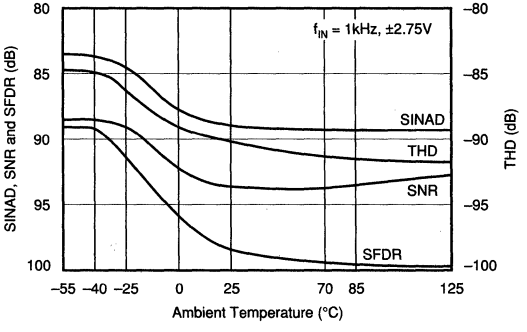
INTERMODULATION DISTORTION WITH 1kHz AND 3kHz INPUTS
(Using Four-Term Blackman-Harris Window)



DSP102 CHANNEL SEPARATION ON CHANNEL B WITH
±2.75V, 1kHz INPUT ON CHANNEL A



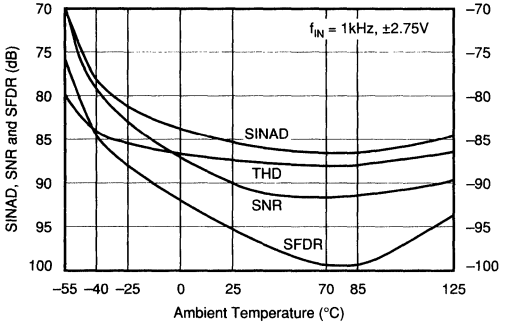
DYNAMIC PERFORMANCE vs TEMPERATURE



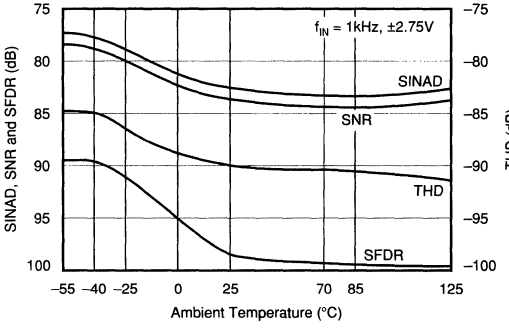
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{A+} = V_{D+} = +5V, V_{A-} = V_{D-} = –5V, Sampling Frequency f_S = 200kHz; External Clock Input at OSC1 = 80f_S = 16MHz, XCLK = 40f_S = 8MHz; Using 2048 Point FFT; Data analysis limited to 0 to 20kHz band; Unless otherwise specified.

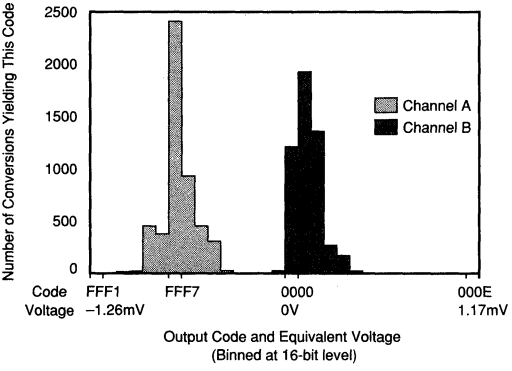
DYNAMIC PERFORMANCE vs TEMPERATURE
(f_S = 180kHz Asychronous to 12.288MHz
Crystal Between OSC1 and OSC2)



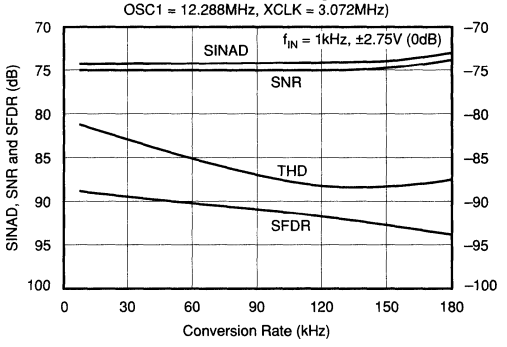
DYNAMIC PERFORMANCE vs TEMPERATURE
(Data Analysis Over Full 0 to 100kHz Band)



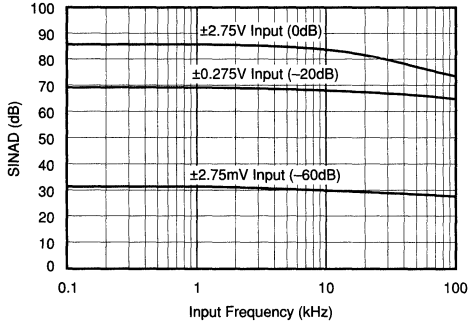
HISTOGRAM OF 5k CONVERSION RESULTS ON DSP102
(Both Inputs Grounded)



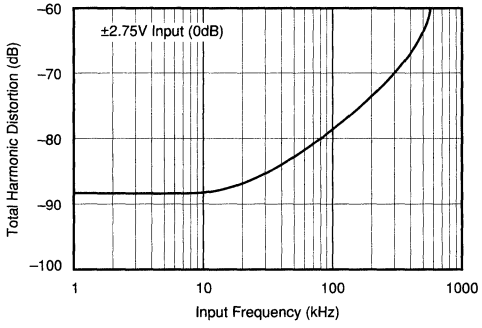
DYNAMIC PERFORMANCE vs CONVERSION RATE
(Data Analysis over Full 0 to f_S/2 Band,
OSC1 = 12.288MHz, XCLK = 3.072MHz)



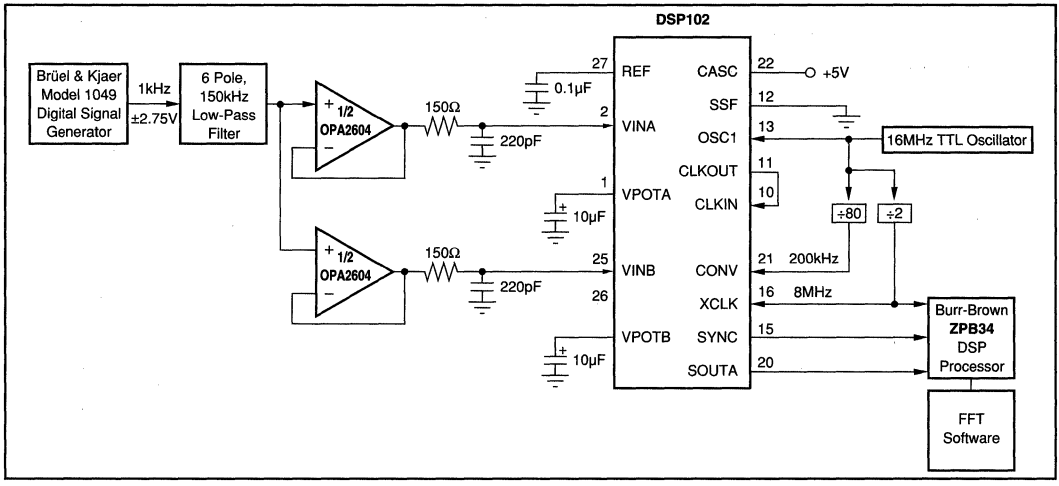
SINAD vs INPUT FREQUENCY
(Data Analysis over Full 0 to 100kHz Band)



TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



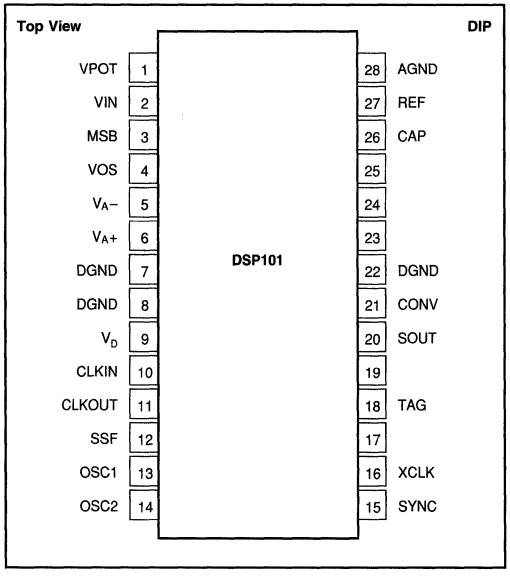
TYPICAL DSP102 FFT SETUP



ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A– to Analog Common	–7V
V_D to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Analog Input Voltage	±5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}, Plastic DIP	50°C/W

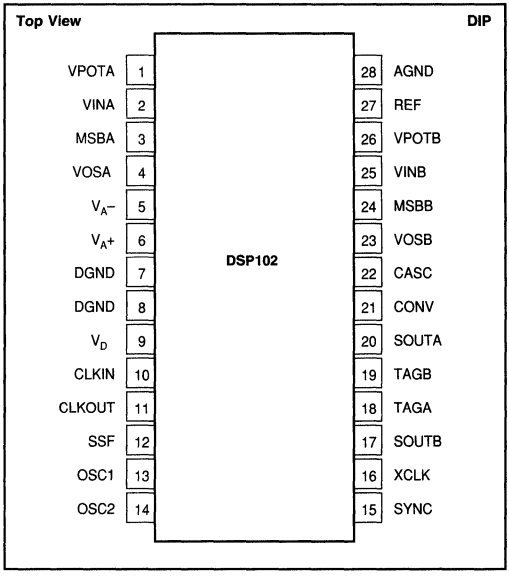
DSP101 PIN CONFIGURATION



DSP101 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOT	Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V.
2	VIN	Analog In.
3	MSB	MSB Adjust In.
4	VOS	VOS Adjust In.
5	V_A–	–5V Analog Power.
6	V_A+	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input/External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17		No Internal Connection.
18	TAG	User Tag In. Data clocked into this pin is appended to the conversion results on SOUT. See timing diagram (Figure 1).
19		No Internal Connection.
20	SOUT	Serial Data Out. MSB first, Binary Two's Complement format.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	DGND	Digital Ground.
23		No Internal Connection.
24		No Internal Connection.
25		No Internal Connection.
26	CAP	Bypass Capacitor. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.7V.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND. Voltage on this pin is approximately 3.8V.
28	AGND	Analog Ground.

DSP102 PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DSP101JP	28-Pin Plastic DIP	215
DSP101KP	28-Pin Plastic DIP	215
DSP102JP	28-Pin Plastic DIP	215
DSP102KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	NUMBER OF CHANNELS	SIGNAL-TO-(NOISE + DIST.) RATIO dB min
DSP101JP	1	83
DSP101KP	1	86
DSP102JP	2	83
DSP102KP	2	86

DSP102 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	VPOTA	Channel A Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V.
2	VINA	Channel A Analog In.
3	MSBA	Channel A MSB Adjust In.
4	VOSA	Channel A VOS Adjust In.
5	V_{A-}	–5V Analog Power.
6	V_{A+}	+5V Analog Power.
7	DGND	Digital Ground.
8	DGND	Digital Ground.
9	V_D	+5V Digital Power.
10	CLKIN	Conversion Clock In.
11	CLKOUT	Conversion Clock Out. Can drive multiple DSP101/DSP102s to synchronize conversion.
12	SSF	Select Synch Format In. If HIGH, SYNC will be active High. If LOW, SYNC will be active Low. See timing diagram (Figure 1).
13	OSC1	Oscillator Point 1 Input / External Clock In. If using external clock, drive with 74HC logic levels. Connect to DGND if not used.
14	OSC2	Oscillator Point 2 Output. Provides drive for crystal oscillator. Make no electrical connection if using external clock.
15	SYNC	Data Synchronization Out. Active High when SSF is HIGH; active Low when SSF is LOW.
16	XCLK	Data Transfer Clock In.
17	SOUTB	Channel B Serial Data Out. MSB first, Binary Two's Complement format.
18	TAGA	Channel A User Tag In. Data clocked into this pin is appended to the conversion results of SOUTA. See timing diagram (Figure 1).
19	TAGB	Channel B User Tag In. Data clocked into this pin is appended to the conversion results of SOUTB. See timing diagram (Figure 1).
20	SOUTA	Channel A Serial Data Out. MSB first, Binary Two's Complement format. If CASC is HIGH, 32 bits of data output, with first 16 bits being Channel A data.
21	CONV	Convert Command In. Falling edge puts converter into hold state, initiates conversion, and transmits previous conversion results to DSP IC with appropriate SYNC pulse.
22	CASC	Select Cascade Mode In. If HIGH, DSP102 transmits a 32-bit word on SOUTA, with the first 16 bits being data on Channel A. If LOW, DSP102 transmits data for both channels simultaneously.
23	VOSB	Channel B VOS Adjust In.
24	MSBB	Channel B MSB Adjust In.
25	VINB	Channel B Analog In.
26	VPOTB	Channel B Trim Reference Out. 10µF Tantalum to AGND. Voltage on this pin is approximately 2.75V.
27	REF	Reference Bypass. 0.1µF Ceramic to AGND. Voltage on this pin is approximately 3.8V.
28	AGND	Analog Ground.

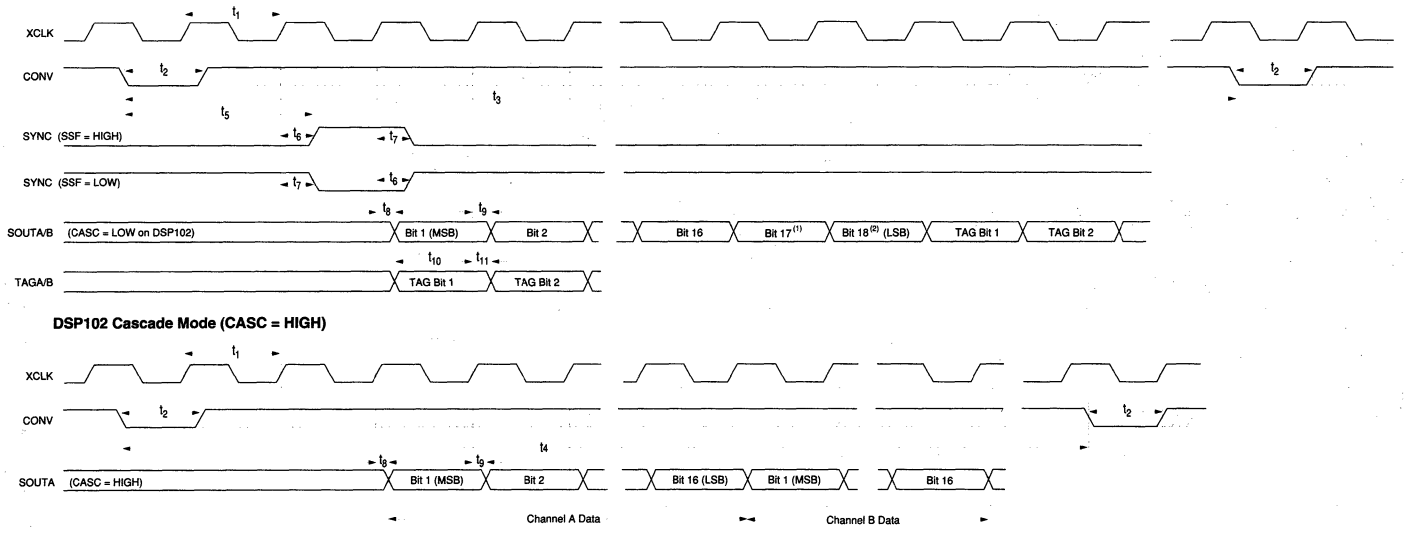
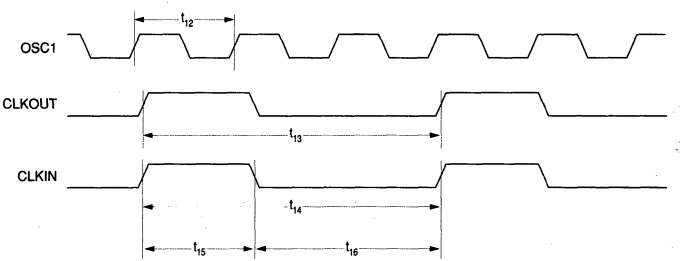


FIGURE 1. DSP101 and DSP102 Timing.

SYMBOL	DESCRIPTION (C_L = 50pF)	MIN	MAX	UNITS
t_1	XCLK period. Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP102)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP102)	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising		15	ns
t_8	SOUTA/B Data Valid Delay from XCLK Rising		15	ns
t_9	SOUTA/B Data Valid After from XCLK Rising	10		ns
t_{10}	TAGA/B Data Setup before XCLK Rising	20		ns
t_{11}	TAGA/B Data Hold after XCLK Rising		0	ns
t_{12}	OSC1 Period.(2) Duty Cycle 50% ± 10%	62	667	ns
t_{13}	CLKOUT Period. Duty Cycle 33% ± 10%	3 t_{12}		ns
t_{14}	CLKIN Period. Duty Cycle 33% ± 20%	186	2000	ns
t_{15}	CLKIN HIGH	62	1050	
t_{16}	CLKIN LOW	84	1340	

Conversion Clock Timing (2)



NOTES: (1) When using a DSP IC in a 16-bit mode, these data bits will be ignored by the processor. (2) f_{OSC1} must be at least 72 times faster than the conversion rate. (t_3, $t_4 \geq 72\ t_{12}$)

THEORY OF OPERATION

The DSP101 and DSP102 are sampling analog-to-digital converters optimized for handling dynamic signals. They have complete logic interface circuitry for ease of use with standard digital signal processing ICs, and transmit data words in a serial stream. The successive approximation conversion architecture is combined with an inherently sampling switched capacitor array to provide maximum user flexibility over sampling and conversion timing.

The DSP101 and DSP102 are pipelined internally. When the user gives a convert command at time (t), two actions are initiated. First, the internal sample/holds are switched to the hold state, and a conversion cycle is initiated. At the same time, the DSP101 or DSP102 transmits a synchronization pulse and starts shifting out the conversion results from the previous convert command at (t-1) using the system bit clock. The data from the conversion at time (t) is shifted out of the converter after the next convert command is received.

Both the DSP101 and the DSP102 are 18-bit A/Ds internally. When the DSP IC is programmed to accept 16-bit word lengths, the processor will ignore the last two data bits transmitted from the DSP101 or DSP102. A Cascade Mode on the DSP102 can be invoked to transmit data for both conversion channels over a single serial line as a 32-bit word. In this mode, the first 16 bits of data transmitted after the Sync pulse contain data from channel A, followed by 16 bits of information from channel B, allowing a single 32-bit word to contain data for both channels.

A unique Tag feature allows additional digital data to be appended to the conversion results, so that a single data word contains conversion results plus other signal information, such as gain settings or multiplexer channel settings in front of the converter.

The DSP101 and DSP102 are high-resolution A/D converters complete with sampling capability and on-board references. They can acquire and convert analog signals at up to a 200kHz sampling rate. Both operate from ±5V supplies, and have full-scale analog input ranges of ±2.75V.

BASIC OPERATION

Figure 2 shows the minimum connections required to operate the DSP101. The falling edge of a convert command on pin 21 puts the internal sampling capacitor array into the hold state. The falling edge on pin 21 also starts the process to initiate a conversion and transmit data from the previous conversion, synchronizing both appropriately to the 10MHz clock input on pin 13. Figure 1 shows the timing relationship between the convert command, the output data, and the synchronization pulse.

In this basic system, the 10MHz clock is used both to generate a 3.33MHz conversion clock and as the data transfer bit clock for outputting data. Per Figure 1, there must be at least 72 clock pulses on pin 13 between convert commands, so that this circuit can sample and convert at up to 138kHz.

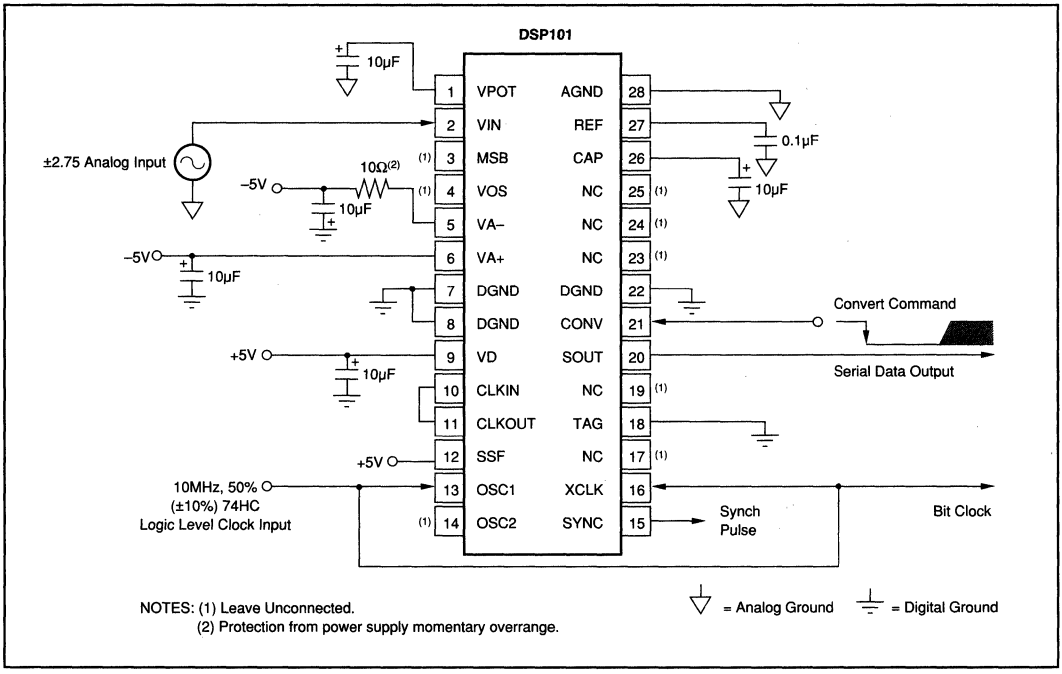


FIGURE 2. DSP101 Basic Operation.

The convert command at pin 21 causes a Sync pulse to be output on pin 15, followed by the data from the previous conversion output on pin 20. The Sync pulse will be HIGH for one bit clock cycle, since pin 12 is tied HIGH. (A LOW Sync pulse will be output on pin 15 if pin 12 is tied LOW.) Data is serially transmitted in an MSB-first data stream, in Binary Two's Complement format. Both the Sync pulse (pin 15) and the data stream (pin 20) are synchronized to the bit clock (at pins 13 and 16), with the timing relationships shown in Figure 1.

After the 18 bits of data from the previous conversion have been transmitted, pin 20 will continue to clock out LOWs until a new convert command restarts the process, since pin 18 (the Tag input) is grounded. If pin 18 is tied HIGH, pin 20 will clock out HIGHs between conversion cycles.

CONVERSION

A falling edge on pin 21 (CONV) puts the internal sampling capacitors in the hold state with minimum aperture jitter, initiates a conversion synchronized to the conversion clock, and outputs the data from the previous conversion with an appropriate Sync pulse. On the DSP102, a single convert command simultaneously samples both channels. The timing relationship between the convert command, Sync and the output data is shown in Figure 1. Both Sync and the output data are synchronized to XCLK, the system bit clock. Following a convert command falling edge, pin 21 must be held LOW at least 50ns.

Convert commands can be sent to the DSP101 and DSP102 completely asynchronous to other clocks in the system. This allows external events to be used to trigger conversions.

From Figure 1, it can be seen that two different clocking conditions must be considered in determining the minimum acceptable time between convert commands. First, there need to be a minimum of 24 XCLK periods between convert commands, to allow internal synchronization and transmission of Sync and the data. (In the Cascade Mode on the DSP102, there need to be at least 40 XCLK periods between convert commands, to allow transmission of the 32-bit data words.) When used with DSP processors programmed for data words longer than 16 bits, the transmission time to the processor may determine the minimum time between convert commands.

The second limitation on convert commands is the requirement that the internal analog-to-digital converter be given enough time to complete a conversion, shift the data to the output register, and acquire a new sample. This condition is met by having a minimum of 24 CLKIN periods between convert commands, or a minimum of 72 clock cycles on OSC1, if it is used to generate the conversion clock (CLKOUT driving CLKIN).

SIGNAL ACQUISITION

After a conversion is completed, the DSP101 or DSP102 will switch back to the sampling mode. With at least 24 CLKIN periods between convert commands, the A/D will have had sufficient time to acquire a new input sample to full rated accuracy.

DATA FORMAT AND INPUT LEVELS

The DSP101 and DSP102 output serial data, MSB first, in Binary Two's Complement format. In the Cascade Mode on the DSP102, the serial data will first contain 16 bits of data for channel A, MSB-first, followed by channel B data, again MSB-first. The analog input levels that generate specific output codes are shown in Table I.

As with all standard A/Ds, the first output transition will occur at an analog input voltage 1/2 LSB above negative full scale (–2.75V + 1/2 LSB) and the last transition will occur 3/2 LSB below positive full scale (+2.75V – 3/2 LSB.) See Figure 3.

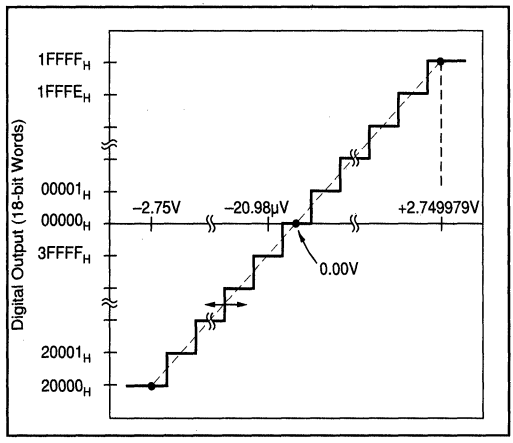


FIGURE 3. Analog Input to Digital Output Diagram.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT (BINARY TWO'S COMPLEMENT) BINARY CODE	16-BIT WORDS (HEX)	18-BIT WORDS (HEX)
Least Significant Bit (LSB = $\frac{5.5V}{2^n}$)				
16-bit Words	84µV			
18-bit Words	21µV			
Input Range	±2.75V			
+ Full Scale (2.75V–1LSB)	+2.749916V +2.749979V	011...111	7FFF	1FFFF
Bipolar Zero (Midscale)	0V	000...000	0000	00000
One LSB below Bipolar Zero	–84µV –21µV	111...111	FFFF	3FFFF
– Full Scale	–2.75V	100...000	8000	20000

TABLE I. Ideal Input Voltage vs Output Code.

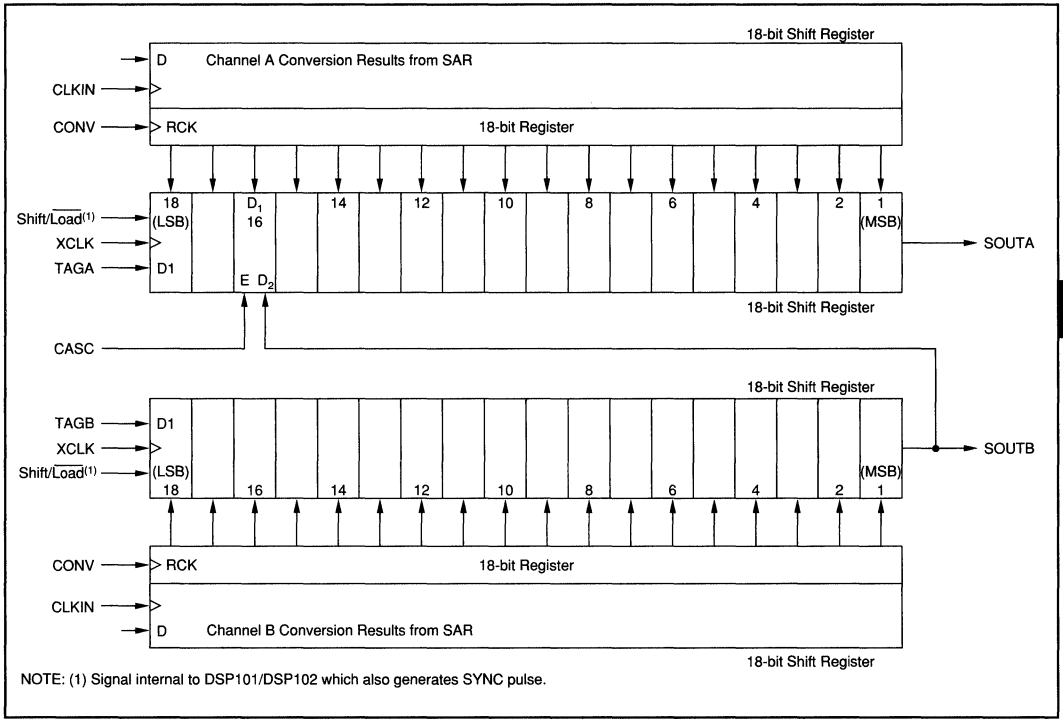


FIGURE 4. Output Structure of DSP102.

DATA TRANSFER

The internal A/Ds generate 18 bits of data, transmitting the data MSB first. When read by a DSP IC programmed to accept 16 bits of data, the first 16 MSB bits of data from the DSP101, or each channel of the DSP102, will be shifted into the processor's input shift register, and the last two least significant bits of data from the A/D will be ignored, although they will still be present on the serial data line. When the DSP processor is programmed to accept words of more than 16-bit length (typically 24-bit or 32-bit), the DSP101 and DSP102 will transmit the full 18-bit conversion results, after which the information input on the TAG input (or TAGA and TAGB on the DSP102) will be appended to the output word. (See Tag Feature below.)

In the Cascade Mode, the DSP102 will first transmit the 16 MSBs from channel A, followed by the full 18 bits from channel B, although DSP processors programmed to accept 32 bits of data will ignore the final two bits of information on Channel B. See the DSP102 Cascade Mode section below for details of the Cascade mode.

DATA SYNCHRONIZATION

A convert command both initiates a conversion and starts the process for transmitting data from the previous conversion. Convert commands can come at any time, completely asynchronous to the conversion clock or the bit clock, and the conversion clock may also be independent of the bit clock. The DSP101 and DSP102 internally synchronize the output data, Sync pulse, and Tag inputs to the bit clock.

While the convert command, conversion clock and bit clock can be asynchronous, system performance is usually enhanced by synchronizing all of them to a system master clock, whenever the application permits. This minimizes changes in digital loads and currents when the critical S/H transition and A/D bit decisions are occurring. Within the DSP101 and DSP102 themselves, running asynchronous convert commands, conversion clocks and bit clocks typically degrades performance only several dB, as shown in the various typical performance curves, but the system board design can easily have more effect.

When a convert command is received, the internal logic generates an appropriate Sync pulse, synchronized to XCLK, as shown in Figure 1. The output Sync pulse will be active High or active Low depending on whether a HIGH or a LOW, respectively, is input at SSF (pin 12).

The convert command also causes the conversion results from the previous conversion to be loaded into the output shift register, synchronous to XCLK. Figure 4 shows the operation of the internal data shift registers on the DSP102. The DSP101 is basically similar, but includes only the top of the figure, showing the SOUTA path.

During the internal successive approximation conversion process, the conversion results are shifted into the input shift registers of the output stage on the DSP102. A new convert command latches that data into the 18-bit parallel latches shown. The internal signal that also generates the Sync pulse, labeled "Shift/Load" in Figure 4, synchronously loads the conversion data into the output shift register on the rising edge of XCLK. The conversion results are then clocked out of the shift register on subsequent rising edges of XCLK.

DATA TRANSFER CLOCK

XCLK is the data transfer clock, or bit clock, for the system, and is an input for the DSP101 or DSP102. This input is TTL- and 74HC-level compatible. The serial data and SYNC outputs are synchronized internally to this clock, with data valid on the rising edge of XCLK, per the timing shown in Figure 1. Data input on pin 18 (TAG) on the DSP101, or on pins 18 and 19 on the DSP102 (TAGA and TAGB), will be clocked into the output shift register on the rising edge of XCLK, as discussed in the Tag Feature section.

CONVERSION CLOCK

The analog-to-digital converter sections in the DSP101 and DSP102 were designed to provide accurate conversions under worst case conditions of supplies, temperatures, etc. In order to achieve a full 200kHz sampling capability, they were designed to use a 33% duty cycle conversion clock (CLKIN on pin 10) as shown in Figure 1. The clock is LOW long enough for internal analog circuitry to settle sufficiently between bit decisions to insure rated accuracy. Bit decisions in the A/D are then made on the rising edge of CLKIN.

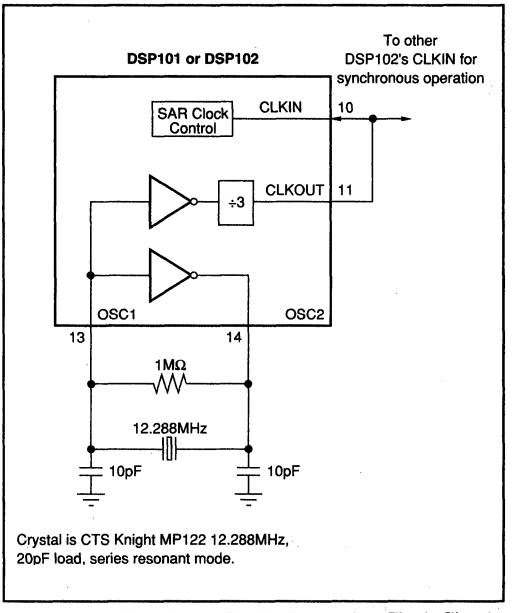
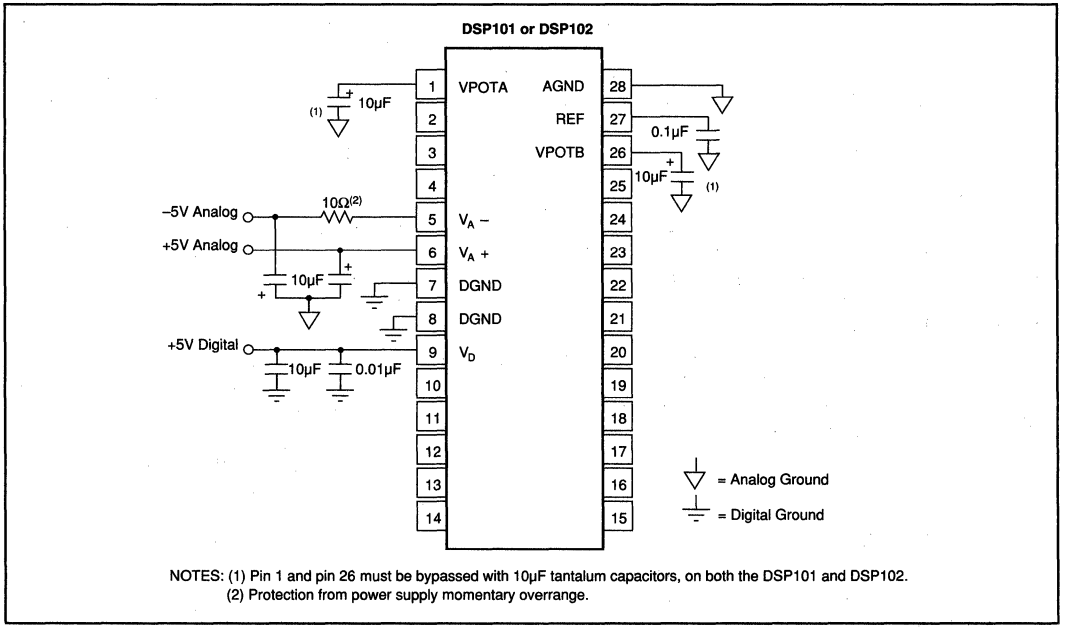


FIGURE 5. DSP101 or DSP102 Conversion Clock Circuit.



NOTES: (1) Pin 1 and pin 26 must be bypassed with 10µF tantalum capacitors, on both the DSP101 and DSP102.
(2) Protection from power supply momentary overrange.

FIGURE 6. DSP101 or DSP102 Power Supply Connections.

When a convert command is received, the DSP101 or DSP102 immediately switches the sampling capacitors to the hold state, and then internally gates the conversion clock to the A/D appropriately. Allowing a minimum of 24 CLKIN pulses between conversions insures that there is sufficient time for complete, accurate conversions, and allows the input sampling capacitor to fully acquire the next sample, regardless of the timing between the convert command and CLKIN.

In most applications, CLKIN (pin 10) can be driven from a 50% duty cycle clock without performance degradation. During characterization of the DSP101 and DSP102, the performance of a number of parts was measured under various conditions with a 4.8MHz, 50% duty cycle input to CLKIN at a full 200kHz conversion rate without noticeable degradation.

OSCILLATOR INPUTS AND CLKOUT

The DSP101 or DSP102 can generate a 33% duty cycle conversion clock output on CLKOUT (pin 11). This is accomplished by dividing by three a clock from either an external 74HC-level clock or from a crystal oscillator. CLKOUT can deliver ±2mA, and can be used to drive multiple DSP101 or DSP102 CLKINs. See Figure 1 for the timing relationship between OSC1 and CLKOUT.

To use an external 74HC-level clock, drive the clock into OSC1 (pin 13), and leave OSC2 (pin 14) unconnected.

To use a crystal oscillator to generate the conversion clock, refer to Figure 5. Connect the oscillator between OSC1 and OSC2. OSC2 provides the drive for the crystal oscillator. This pin cannot be used elsewhere in the system.

If CLKOUT is not used, both it and OSC2 should be left unconnected, and OSC1 should be grounded.

TAG FEATURE

Figure 4 shows the implementation of the TAG feature on the DSP101 and DSP102. When a convert command is received, the internal Shift/Load signal loads conversion result data into the output shift register synchronous to XCLK. Between convert commands, the information input on TAG (on the DSP101) or on TAGA and TAGB (on the DSP102) will be clocked into the output shift register on the rising edges of XCLK. Since this is an 18-bit shift register, the data input on the Tag lines will be output on SOUT (DSP101) or SOUTA and SOUTB (DSP102) delayed by 18 bit clocks.

The Tag Feature can be used in various ways. The Tag inputs can be tied HIGH or LOW to differentiate between two converters in a system. As discussed in the Applications section below, the Tag feature can be used to append to the serial output data word information on multiplexer channel address, or other digital data related to the input signal (such as the setting on a programmable gain amplifier.) Another option would be to daisy-chain multiple DSP101 or DSP102 converters, linking the serial output of one to the Tag input of the next. This can simplify the transmission of data from multiple A/Ds over a single optical isolation channel.

DSP102 CASCADE MODE

If pin 22 (CASC) is tied HIGH, the DSP102 will be in the Cascade Mode. In this mode, when a convert command is received, the DSP102 will transmit a 32-bit data word on pin

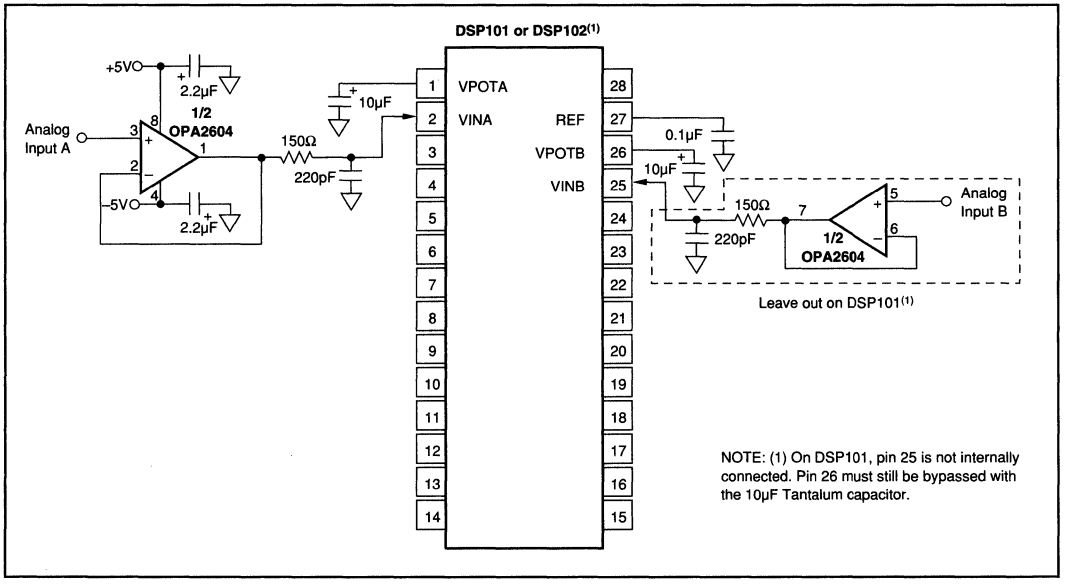


FIGURE 7. DSP101 or DSP102 Input Buffering.

20 (SOUTA) containing data for both input channels in two 16-bit words. Referring to Figure 1, the first 16 bits of data will be the results for channel A, followed by 16 bits of information for channel B. The data will be transferred MSB first. A convert command at time (t) will initiate the transmission of the results of the conversion initiated at time (t – 1).

From the descriptions above of the internal shift registers shown in Figure 4, it can be seen that the DSP102 in the Cascade Mode actually continues to shift out data after the 32nd bit of the data word. The next two bits clocked out will be the last two data bits from the full 18-bit conversion on channel B, after which the information output on SOUTA will be the information clocked into TAGB 35 bit clock cycles earlier.

In the Cascade mode on the DSP102, SOUTB will still output channel B conversion data and tag data as usual.

ANALOG PERFORMANCE

LINEARITY

The DSP101 and DSP102 are optimized for signal processing applications with wide dynamic range requirements. Linearity is trimmed for best performance in the range around 0V, which is critical for handling low amplitude signals. The DSP101 and DSP102 typically have integral and differential non-linearity below ±0.003% in the input range of ±0.7V, with there being no missing codes at the 14-bit level in this range. Over the full ±2.75V input range, the largest non-linearities are centered around the bit #2 transition points at +1.375V and –1.375V levels.

NOISE AND BIPOLAR ZERO ERROR

The equivalent input noise and bipolar zero error of the DSP101 and DSP102 is shown in the typical performance section for both channels on a DSP102. The inputs to both channels were grounded, and the results of 5,000 conversions was recorded. The data shown is binned at the 16-bit level. The noise results from all sources in the circuit, including clocks, reference noise, etc.

In a theoretically ideal converter with no offset and no noise, the results of all 5,000 conversion for each channel would lie in the bin corresponding to bipolar zero, code 0000. The typical DSP101 or DSP102 will have offset errors in the range of 1 to 2mV, and the two channels on the DSP102 will be matched closer than 2mV. The DSP102 shown in the typical performance section has the worst offset, –0.8mV, on channel A, with channel B being less than 1mV different, and the three sigma noise on either channel being less than 250µV.

INPUT BANDWIDTH

From the typical performance curves, it can be seen that there is very little degradation in Signal-to-(Noise + Distortion) for input signals up to 100kHz. The wideband sampling input typically maintains a 60dB Signal-to-(Noise + Distortion) Ratio undersampling 500kHz input signals.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP101 and DSP102, system design problems such as ground path resistance, contact resistance and power supply quality become very important.

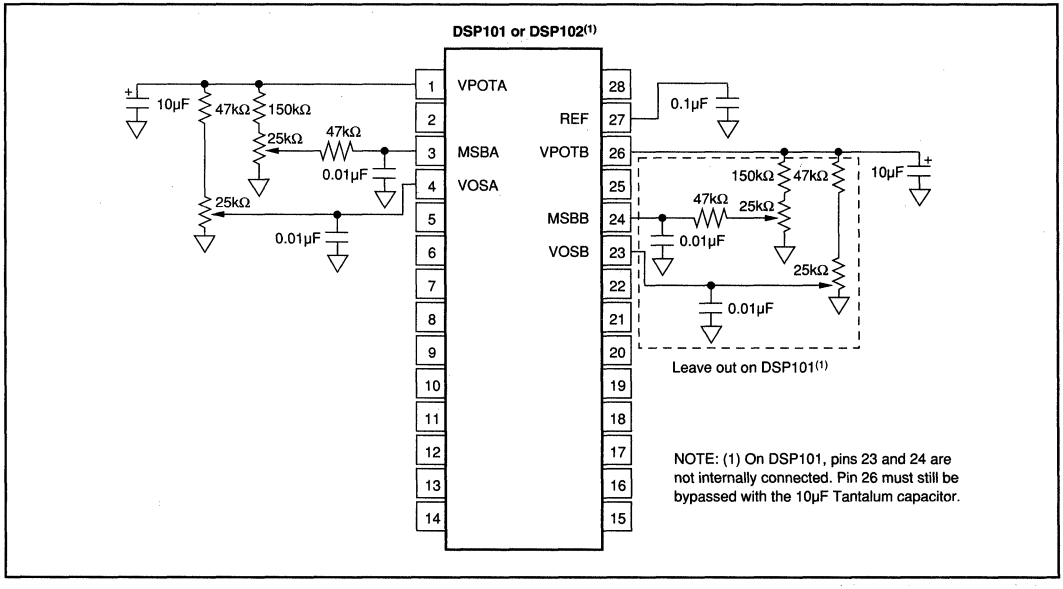


FIGURE 8. DSP101 or DSP102 Optional MSB and Offset Adjust.

Optimal dynamic performance is achieved by soldering the parts directly into boards, to keep the A/Ds as close as possible to ground. The use of sockets will often degrade AC performance. Zero-Insertion-Force sockets are particularly poor because longer lead lengths create inductance.

Short traces on the board, and bypass capacitors as close as possible to the A/D, will further improve dynamic performance.

GROUNDS

To achieve the maximum performance from the DSP101 or DSP102, care should be taken to minimize the effect of changes in current flowing in the system grounds, particularly while bit decisions are being made in the successive approximation converter's comparator. Pin 28 (AGND) on both the DSP101 and the DSP102 is the most critical, and care should be taken to make this pin as close as possible to the same potential as the system analog ground.

Whenever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 84μV at the 16-bit level, and one-quarter of that at the 18-bit level, the currents switched in a typical DSP system can easily corrupt the accuracy of the A/Ds unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figure 6. For optimum performance of any high resolution A/D, all of the supplies should be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-on.

INPUT SIGNAL CONDITIONING

To avoid introducing distortion, the DSP101 and DSP102 analog inputs must be driven by a source with low impedance over the input bandwidth needed in the application. Op amps such as the NE5532 or Burr-Brown's OPA2604 work well over audio bandwidths. Figure 7 shows an appropriate input driver circuit. The 150Ω and 220pF shown on the input help reduce the dynamic load on the input signal conditioning amp in front of the A/D, since all switched capacitor array architectures exhibit fast changes in input current load as the input sampling switch is opened and closed. These dynamic changes in the load can affect any signal conditioning circuit at the input. Other R and C combinations can be

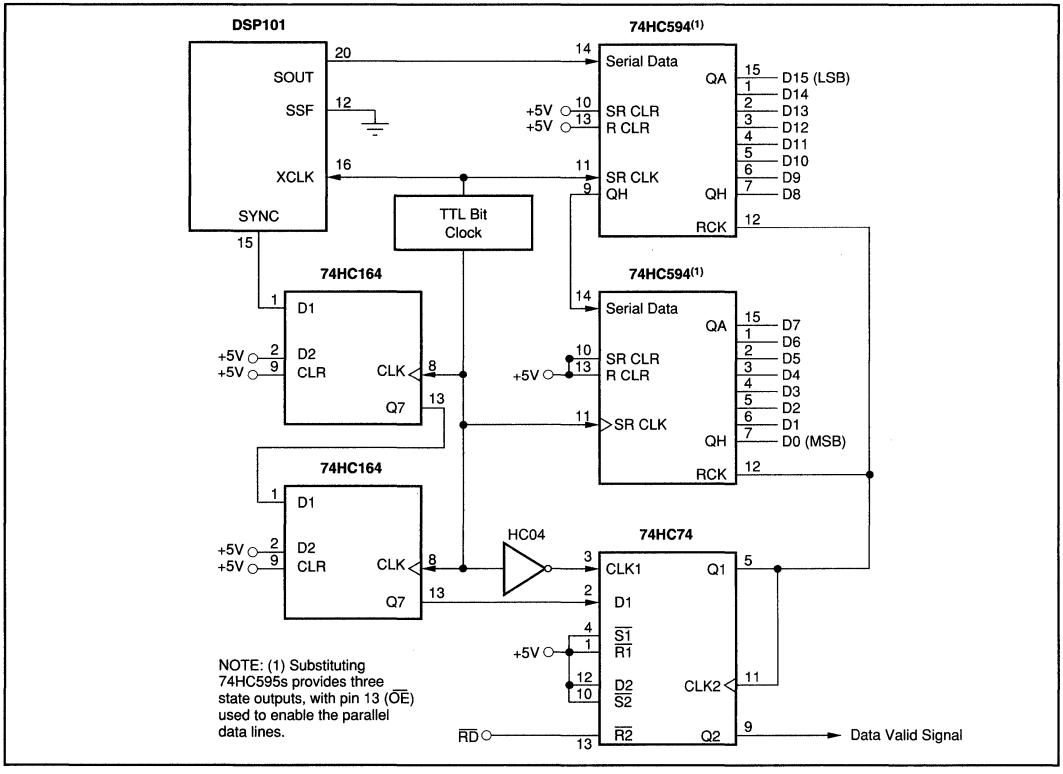


FIGURE 9. Driving a 16-bit Parallel Port from the DSP101.

used, but the resistor should not exceed 200Ω, or the output settling time of the signal conditioning amplifier may be too long.

EXTERNAL ADJUSTMENTS

All of the specifications for the DSP101 and DSP102, plus the typical performance curves, are based on the performance of these A/Ds without external trims. In most applications, external trims are not required.

OFFSET ADJUST

Where required by specific applications, offsets can be adjusted using the circuit of Figure 8. When not adjusted, VOS (pin 4) on the DSP101, and VOSA (pin 4) and VOSB (pin 23) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01µF capacitors, as close as possible to the A/D.

To trim offset, one alternative is to ground the analog input while converting continually. Then adjust the trimpot (on VOS for the DSP101, on VOSA and VOSB for the DSP102) until the output code is toggling between the codes FFFF and 0000 (Hex) at the 16-bit level (3FFFF and 00000 at the 18-bit level). This will center the offset at 1/2 LSB below 0V, which is respectively –42µV or –10µV at the 16- and 18-bit levels.

The offset can also be adjusted by providing a sine wave to the A/D input. Using FFT, or even simple averaging of several thousand conversion results at a time, the trimpots can be adjusted until there is no DC offset of the signal.

Grounding the input, or providing the sine wave, as far in front of the A/D as possible allows offset from intervening signal conditioning components to be also corrected by this procedure.

MSB ADJUST

In most applications, adjustment of the Most Significant Bit weight will not be required. When not adjusted, MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, should be left open. If these pins are connected to traces on the board, they should be bypassed to ground with 0.01µF capacitors, as close as possible to the A/D.

MSB (pin 3) on the DSP101, and MSBA (pin 3) and MSBB (pin 24) on the DSP102, are internally connected to a resistor divider network that is used to laser-trim the weight

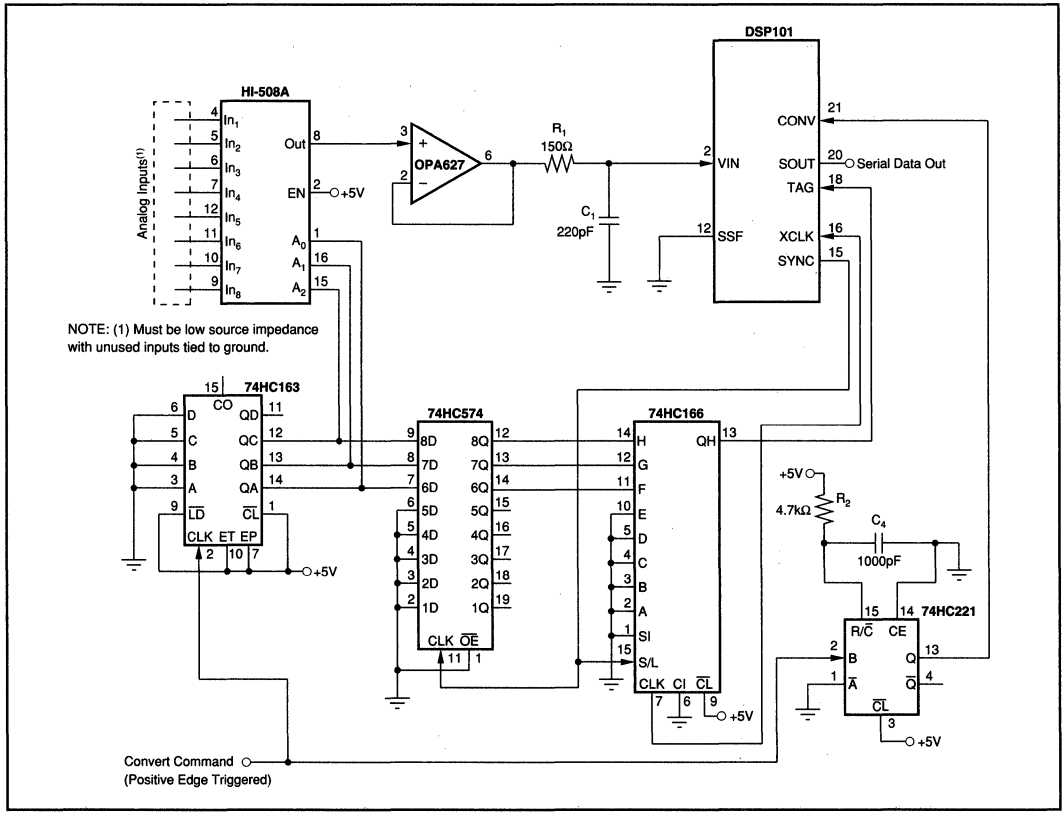


FIGURE 10. A Complete Eight-Channel Analog Input System Using the DSP202 and the HI-508A.

of the MSB capacitor in the CDAC. These pins are nominally at +100mV after laser-trimming during manufacturing. They can handle external inputs up to about one diode drop below ground (–0.6V) before internal clamping circuitry is triggered.

Figure 8 shows an appropriate circuit for adjusting the weight of the most significant bit to minimize differential non-linearity at the critical major-carry transition. To adjust, provide a small amplitude sine wave to the selected A/D input pin while converting continually, and adjust for maximum Signal-to-(Noise + Distortion) ratio, using appropriate signal analysis software.

GAIN ADJUST

If circuit gain needs to be adjusted in hardware, rather than in system software, appropriate trimpots should be included in the analog signal conditioning section in front of the DSP101 or DSP102. No specific gain adjust circuitry is included in the parts.

APPLICATIONS

INTERFACING DSP101 TO PARALLEL PORTS

Figure 9 shows a circuit for converting the serial output data from the DSP101 into 16 bits of parallel data, within the timing constraints of the serial bit-stream from the DSP101. In many applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

This circuit adds an additional pipeline delay to the conversion data, so that the parallel data from a conversion at time (t) is valid one conversion cycle plus 17 XCLK clocks later (at t+1 plus 17 times XCLK). A convert command at time (t+1) generates a Sync and begins transmitting serial data from SOUT. The serial data is shifted into the 74HC594 shift registers, and Sync is shifted through the 74HC164 shift registers. The Q1 output of the 74HC74 dual D-type flip-flops clocks the conversion data into the output register of the 74HC594s, and triggers a data valid signal on its Q2 output. The user can then read the data at any time before the next conversion is started, and the Read signal will reset the data valid output from Q2.

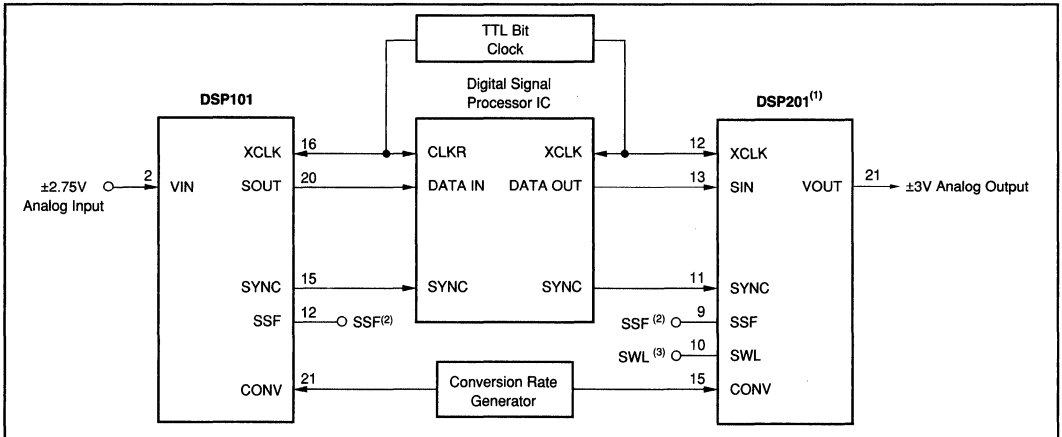
In many systems, galvanic isolation of signals is required. Using opto-couplers on the serial data lines in Figure 9 allows a fully isolated system to be built using a DSP101 and only three couplers across the barrier (for serial data, XCLK and SYNC.)

MULTIPLEXING INPUTS TO THE DSP101

Figure 10 shows a complete circuit for sequentially scanning eight analog input channels with a single DSP101, and using the Tag feature on the DSP101 to append the multiplexer channel address to the serial output conversion results.

The circuit in Figure 10 includes the required digital logic and timing logic. The 74HC163 counter provides the scan sequence to the Burr-Brown HI-508A analog multiplexer. In order to allow the HI-508A enough time to switch to the next channel and settle before the DSP101 begins a conversion, a 74HC221 one-shot introduces a 3µs delay for the DSP101 convert command input.

The Burr-Brown OPA627 provides a low impedance source for the DSP101, buffering it from the output impedance of



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	SSF(2)	SWL(3)
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

(1) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.

FIGURE 11. Analog Input and Analog Output System.

the multiplexer. This unity-gain buffer minimizes distortion, taking full advantage of the resolution and bandwidth of the DSP101.

The 74HC574D register delays the multiplexer address data by one conversion before appending the channel data to the serial conversion results from the DSP101. This attaches the channel address to the correct conversion results. Since the channel scanning shown in Figure 10 is sequential, this delay latch could be left out and software could recognize that the time (t) conversion results have the MUX address from the time (t-1) conversion appended. However, for systems using non-sequential scan lists, this delay latch is essential to maintain the conversion data and channel address integrity.

The 74HC166 synchronous loading shift register loads the channel address tag data into the shift register on the rising edge of the bit clock, in conjunction with the Sync output of the DSP101. The channel address tag data is then clocked into the DSP101 Tag input (pin 18) by the bit clock, while the conversion data is clocked out the other end of the DSP101 shift register (discussed in another section of this data sheet.)

Figure 10 was developed and tested using a Burr-Brown ZPB34 DSP board, which contains an AT&T DSP32C, so that the SYNC output is programmed to be active LOW. The circuit needs to be modified for DSP processors from ADI, TI, and Motorola, which use active HIGH Sync pulses. For these processors, tie SSF (pin 12) on the DSP101 HIGH, and use a 74HC04 hex inverter to invert the Sync signal to the 74HC574 and 74HC166.

The same basic circuit can be duplicated to drive two channels in a DSP102, or can be easily modified for more or less than eight channels of analog input.

USING DSP101 AND DSP102 WITH TEXAS INSTRUMENTS DSP ICS

Figures 11 thru 17 show various ways to use the DSP101 and DSP102 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are

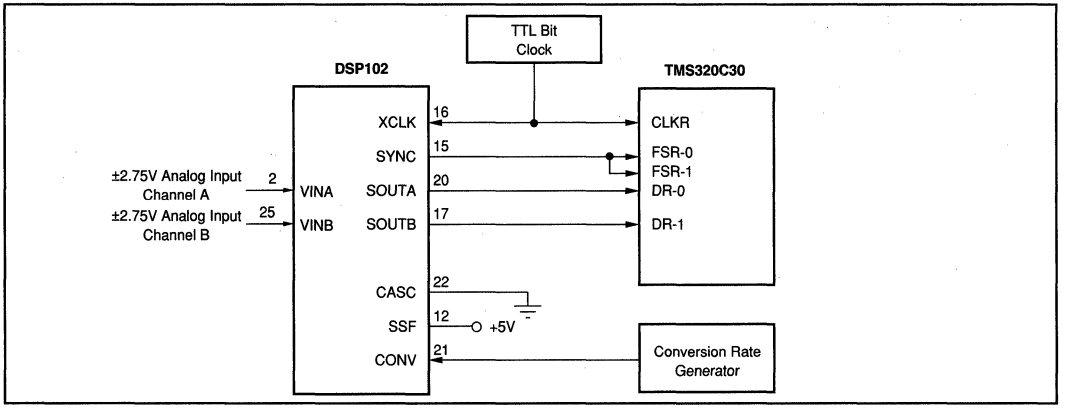


FIGURE 12. Using DSP102 with TMS320C30.

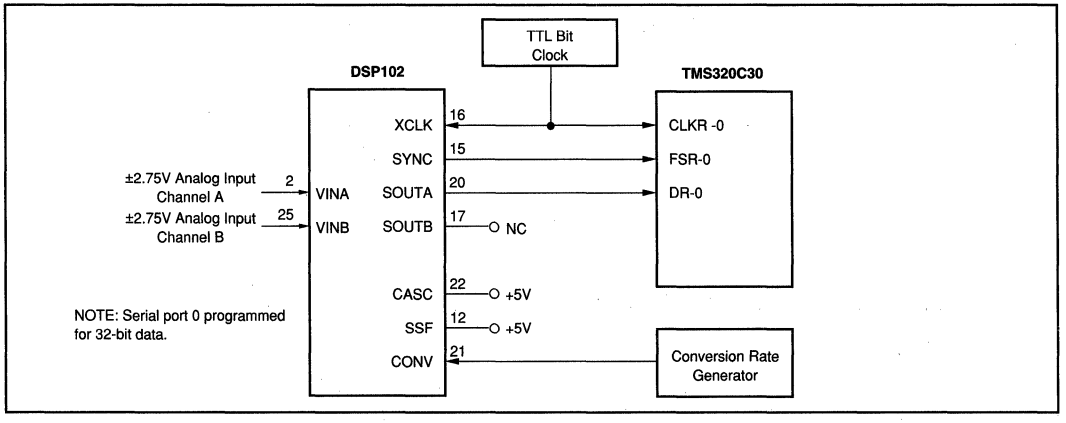
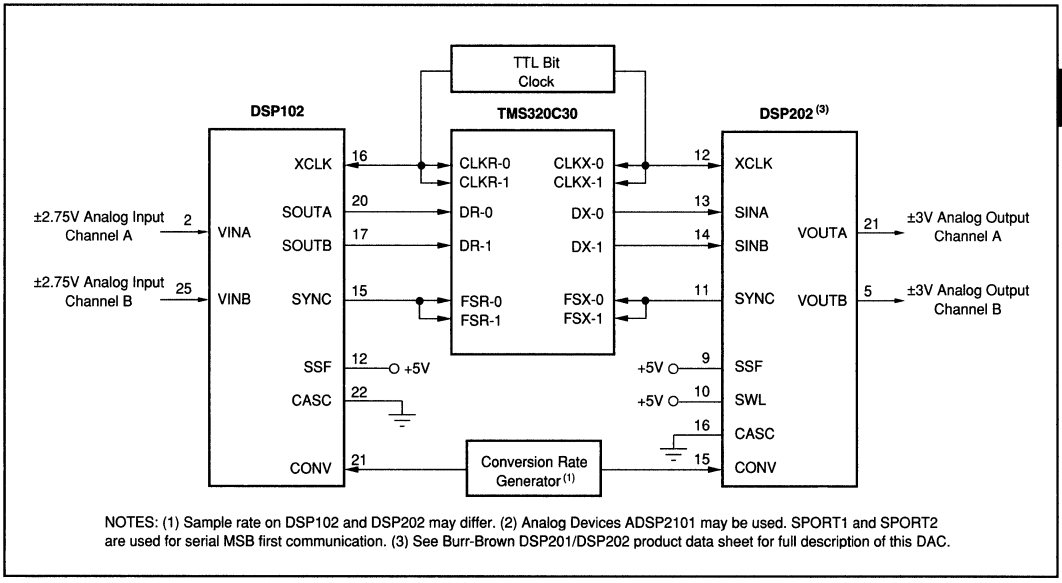


FIGURE 13. Using DSP102 with TMS320C30 in Cascade Mode.

based on using the TME320Cxx in the mode where SSF (Select Synch Format, pin 12) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP101 or DSP102 after receiving a convert command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing the basic operation of the A/Ds.

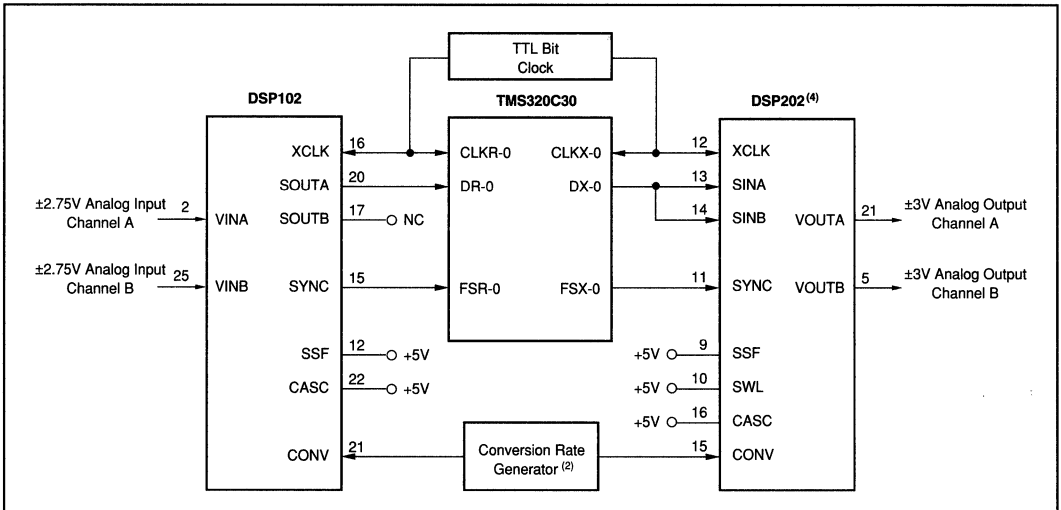
In all cases, the DSP101 and DSP102 will transmit data MSB-first, and the TMS320Cxx needs to be programmed for this.

Figure 11 shows a circuit for using the TMS320C25 or TMS320C30 in a complete analog input and analog output system using the DSP101 along with the Burr-Brown DSP201 D/A.



NOTES: (1) Sample rate on DSP102 and DSP202 may differ. (2) Analog Devices ADSP2101 may be used. SPORT1 and SPORT2 are used for serial MSB first communication. (3) See Burr-Brown DSP201/DSP202 product data sheet for full description of this DAC.

FIGURE 14. Two-Channel Analog Input and Output System with TMS320C30.



NOTES: (1) Program TMS320C30 for 32-bit mode. (2) Sample rate on DSP102 and DSP202 may differ. (3) DSP32C may be used in this mode. (4) See Burr-Brown DSP201/202 product data sheet for full description of this DAC.

FIGURE 15. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.

USING TMS320C31 TO GENERATE ALL CONTROL SIGNALS

Figure 17 shows a circuit for using the TMS320C31 with a DSP102 and a Burr-Brown DSP202 D/A to provide a two channel analog I/O system. The flexibility of the TMS320C31 allows it to generate the data transfer clock (XCLK) and the Convert Command, minimizing additional circuitry and synchronizing the timing signals to the processor's master clock. In this circuit, the DSP102 and DSP202 are used in their Cascade modes, transmitting and receiving two channels of data in a single 32-bit word. (See the Cascade Mode section above.)

Table II shows how to set up the circuit in Figure 17 for a 44.1kHz conversion rate for both channels of the DSP102 A/D and both channels of the DSP202 D/A. Both inputs and outputs will be simultaneously converted.

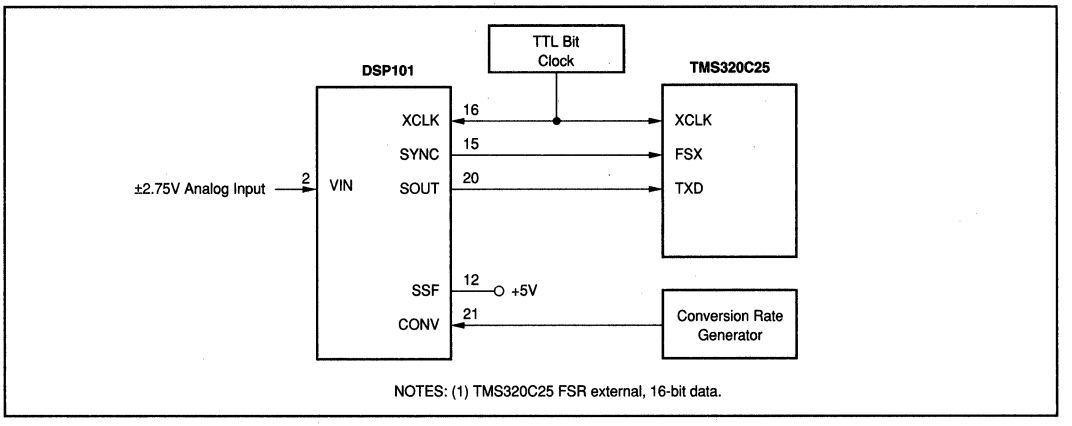


FIGURE 16. Using DSP101 with TMS320C25.

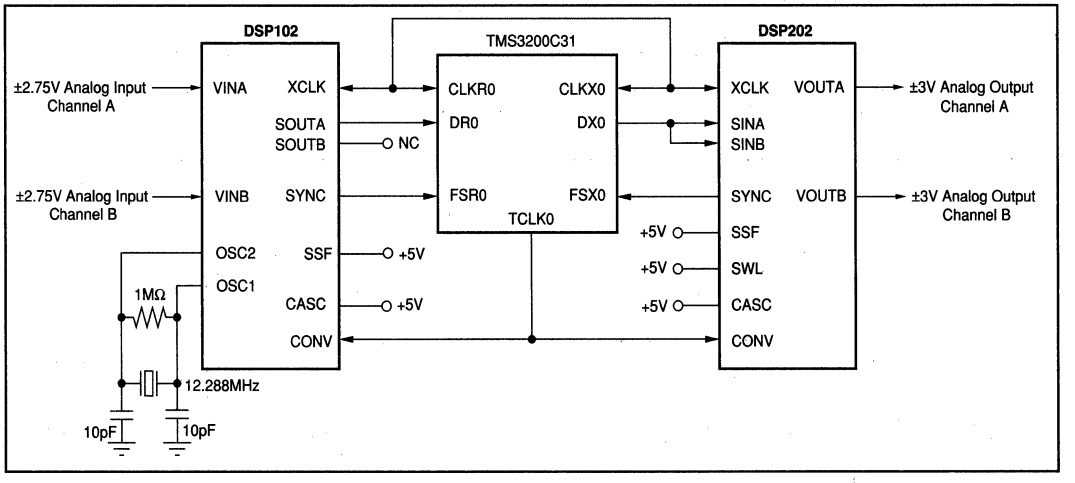


FIGURE 17. Two Channel Analog I/O Using TMS320C31.

SERIAL PORT	
Port Global Control Register	0x0EBC040
FSX/DX/CLKX Port Control Register	0x00000111
FSR/DR/CLKR Port Control Register	0x00000111
Receive/Transmit Timer Control Register	0x0000000F
TIMER	
Timer Global Control Register	0x000002C1
Timer Period Register	0x000000B5
NOTE: Assumes TMS320C31 has 32MHz Master Clock.	

TABLE II. TMS320C31 Register Settings for 44.1kHz Conversion Rate in Figure 17.

USING DSP101 AND DSP102 WITH MOTOROLA DSP ICS

Figure 18 shows how to use the DSP101 with a Motorola DSP56001. Using the DSP102 requires using two DSP56001s. The DSP56001 needs to be programmed to receive data MSB-first with SYNC in the Bit Mode.

SSF (pin 12) needs to be tied HIGH for using either the DSP101 or the DSP102 with DSP56001s. This will cause the DSP101 or DSP102 to transmit an appropriate active High synchronization pulse on SYNC (pin 15) after a convert command is received by the A/D. Timing is shown in Figure 1.

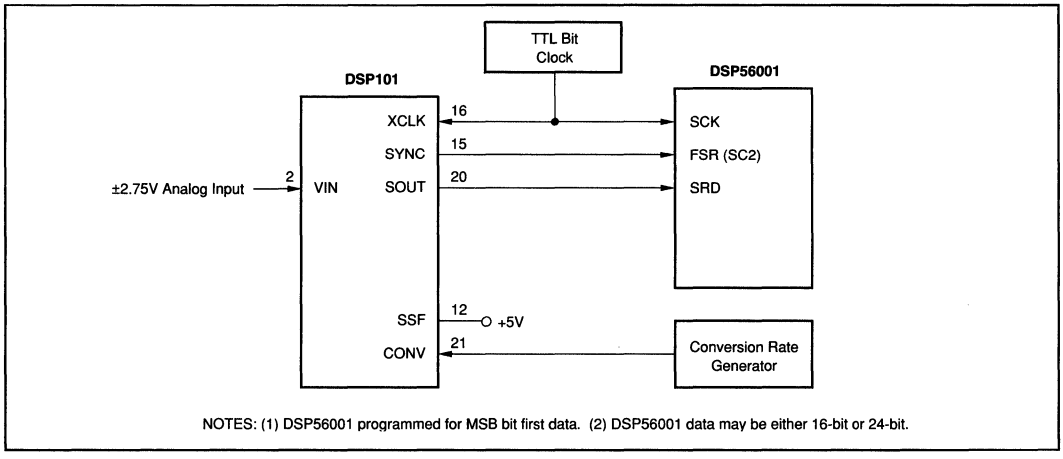
USING DSP101 AND DSP102 WITH AT&T DSP ICS

Figures 11, 19, 20, and 21 show how to use the DSP101 and DSP102 with the DSP16 and DSP32C in different modes. The AT&T processors need to be programmed to accept data MSB-first, and the DSP101 or DSP102 needs to have SSF (pin 12) tied LOW, so that an appropriate active Low synchronization pulse will be transmitted by the A/D after a convert command is received.

Figures 19 and 20 show the DSP32C and DSP16 respectively used with the DSP101 to handle a single analog input channel.

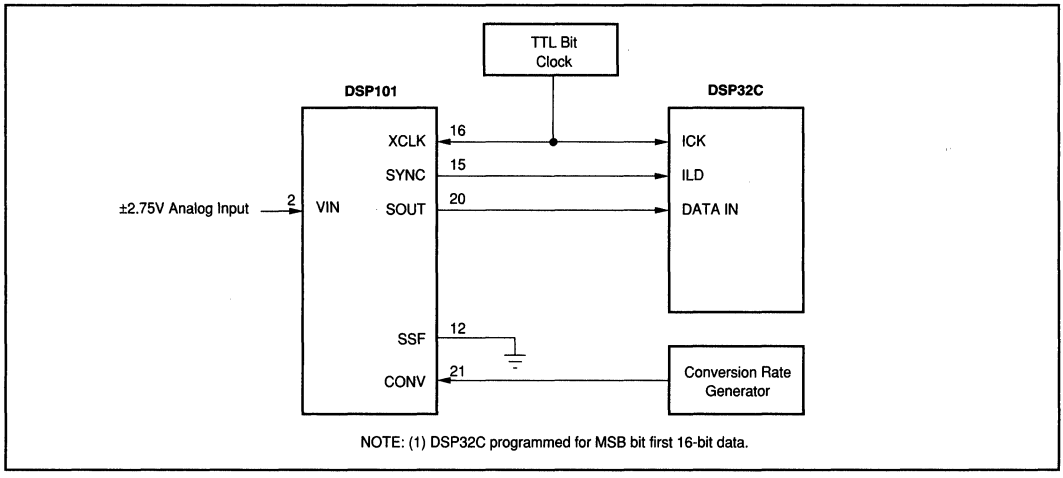
Figure 21 shows how to transmit to a single DSP32C conversion results from both DSP102 channels in a single 32-bit word, using the Cascade mode on the A/D.

Figure 11 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP101 and a Burr-Brown DSP201 D/A.



NOTES: (1) DSP56001 programmed for MSB bit first data. (2) DSP56001 data may be either 16-bit or 24-bit.

FIGURE 18. Using DSP101 with DSP56001.



NOTE: (1) DSP32C programmed for MSB bit first 16-bit data.

FIGURE 19. Using DSP101 with DSP32C.

USING DSP101 AND DSP102 WITH ADI DSP ICS

When using the DSP101 or DSP102 with the fixed-point ADSP21xx series, the processors need to be programmed to receive data MSB-first.

Figure 22 shows how to use the DSP102 with an ADSP2101 to provide a two-channel simultaneous sampling system.

Figure 23 shows the connections required to generate an analog input channel using an ADSP2105 with the DSP101.

The same basic circuit can be used to connect a DSP101 to the ADSP2101.

Figure 11 indicates how to build a complete analog I/O system using either the ADSP2101 or the ADSP2105 with a DSP101 and a Burr-Brown DSP201 D/A.

The two serial ports on the ADSP2101 can also be used with the DSP102 and the Burr-Brown DSP202 D/A to make two complete analog I/O channels, as indicated in footnote 2 of Figure 14.

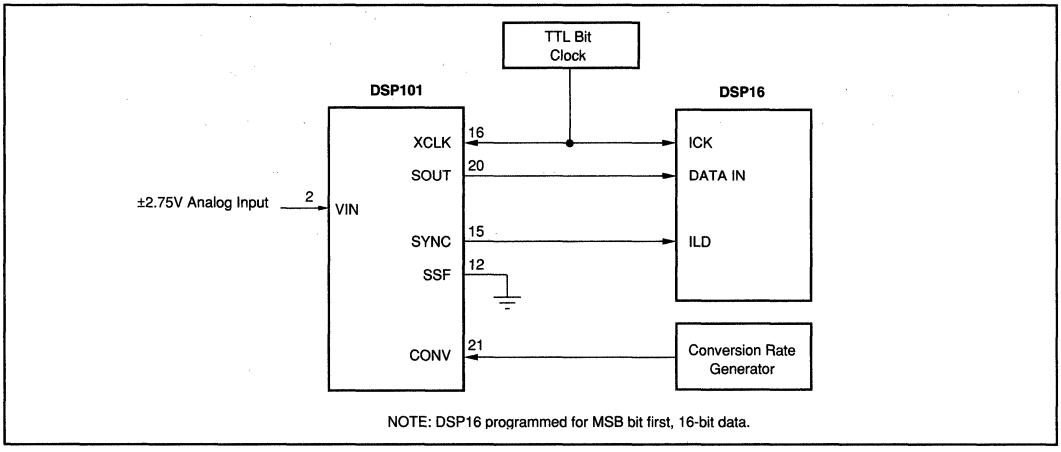


FIGURE 20. Using DSP101 with DSP16.

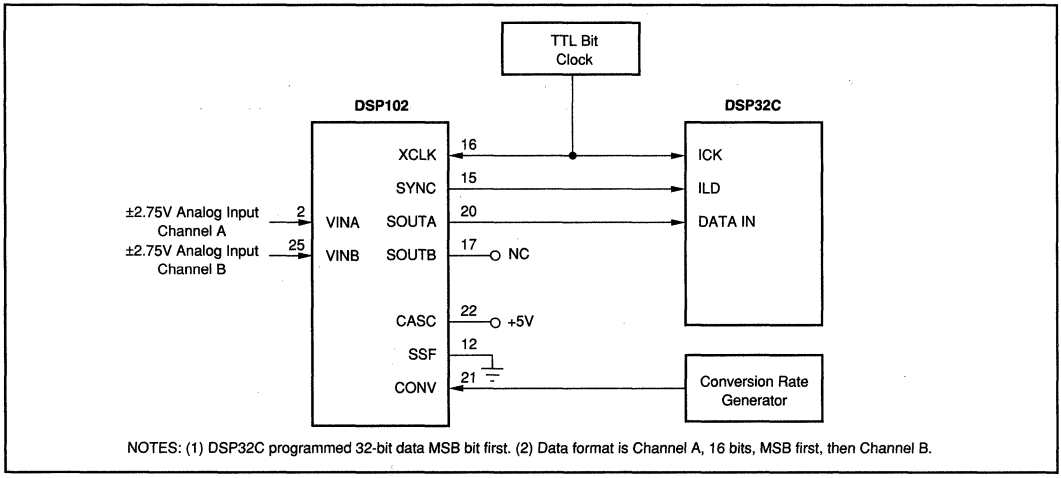


FIGURE 21. Using DSP102 with DSP32C in Cascade Mode.

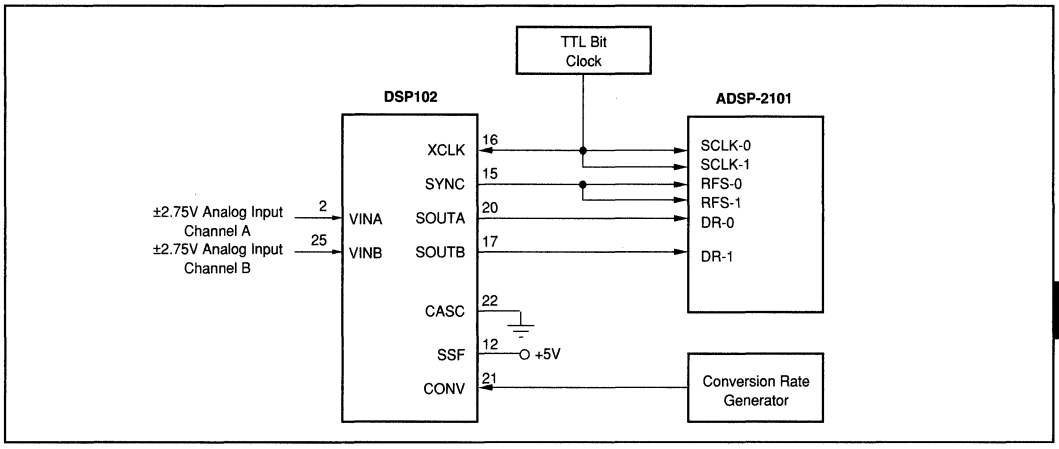


FIGURE 22. Using DSP102 with ADSP-2101.

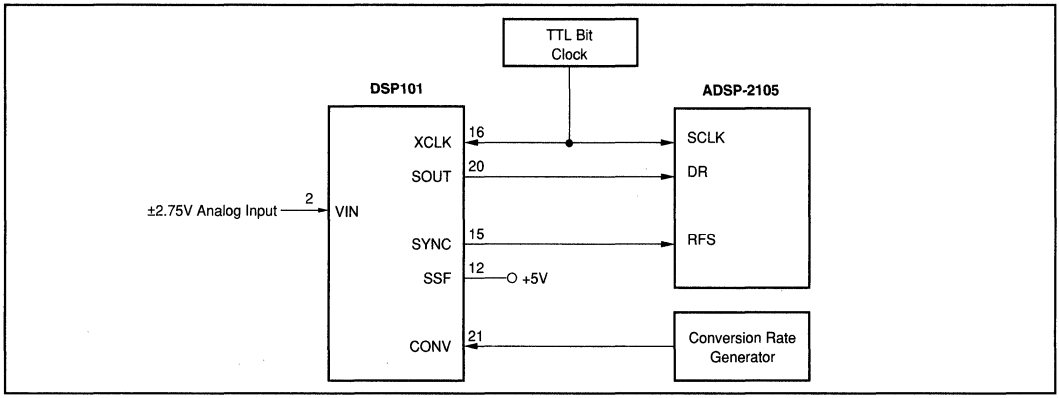


FIGURE 23. Using DSP101 with ADSP-2105.

DEM-DSP102/202 EVALUATION BOARD

An evaluation fixture, the DEM-DSP102/202, is available to simplify evaluation of the DSP101 and DSP102, and the companion digital-to-analog converters, the single DSP201 and dual DSP202. The DEM-DSP102/202 comes complete with a socketed DSP102 and DSP202, a breadboard area, TTL I/O headers and differential line drivers for data transfer options, a complete clocking circuit for the conversion clock and bit clock, and analog filter modules. The board makes it easy to go from design concept to working prototype of a DSP-based system, offering two complete analog I/O channels.

Contact your local Burr-Brown representative for a full data sheet on the DEM-DSP102/202.

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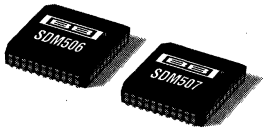


SDM506/507

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

16-Channel Single Ended Input/ 8-Channel Differential Input 16-BIT DATA ACQUISITION SYSTEMS

FEATURES

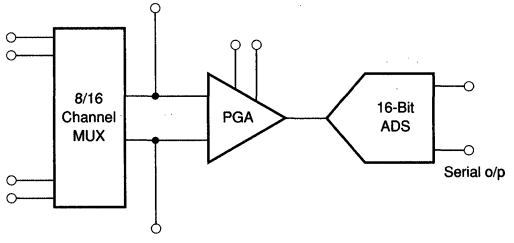
- 16-BIT RESOLUTION
- 100kHz THROUGHPUT
- PROGRAMMABLE GAINS (1, 10, 100, 1000)
- SERIAL OUTPUT DATA
- 16 SINGLE-ENDED INPUTS: SDM506
- 8 DIFFERENTIAL INPUTS: SDM507
- OVERVOLTAGE PROTECTION
- ANALOG INPUTS: 70Vp-p
- 44-PIN PLCC PACKAGE
- TEMPERATURE RANGE: –40°C to +85°C
- LOWER POWER: 450mW

DESCRIPTION

The SDM506/507 are complete 16-bit data acquisition systems with input multiplexer, serial output, and programmable gains of 1, 10, 100, and 1000. The SDM506 has 16 single-ended inputs and the SDM507 has 8 differential inputs.

All these features are contained within a space-saving 44-pin plastic-leaded chip carrier providing the ideal data aquisition solution when space is at a premium.

The SDM506/507 will accept unipolar or bipolar voltage inputs in the range 0V to +4V, 0V to +5V, 0V to +10V, ±3.33V, ±5V and ±10V. For low level signals, dynamic range can be increased by using the programmable gain amplifier. Input overvoltage protection on the analog input channels provide fault-free operation for input voltages up to ±35V.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

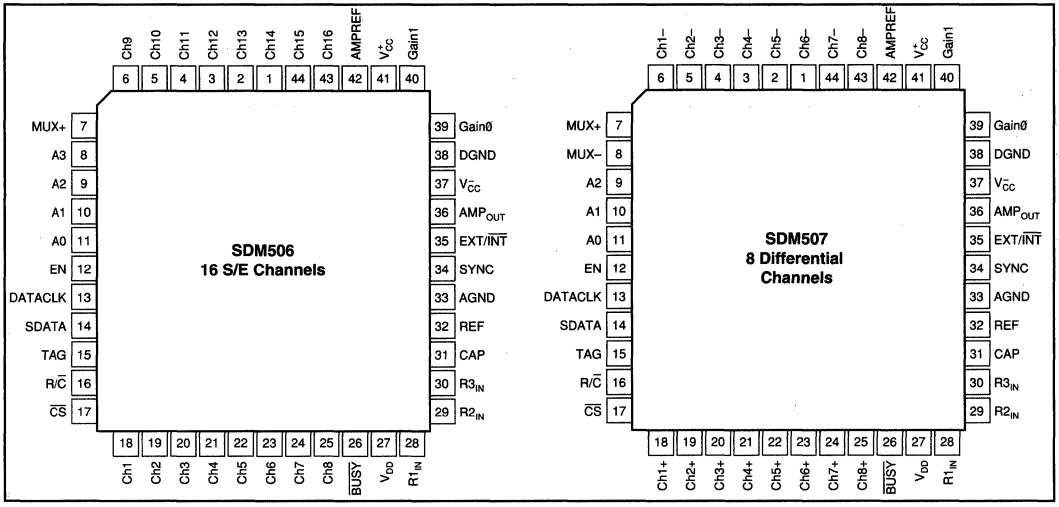
SPECIFICATIONS—PRELIMINARY

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, ±V_{CC} = ±15V, ±10V input range, and G = 1 using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	SDM506/507 MIN	SDM506/507 TYP	SDM506/507 MAX	UNITS
RESOLUTION				16	Bits
ANALOG INPUT			±10, ±5, ±3.33		V
Voltage Ranges			0-10, 0-5, 0-4		V
Input Impedance: On Channel	10^{10}		10		GΩ
Off Channel	10^{10}		10		GΩ
Input Capacitance: On Channel	20		20		pF
Off Channel	20		20		pF
THROUGHPUT SPEED					
Conversion Time			7.6	8	µs
Complete Cycle	Acquire and Convert			10	µs
Throughput Rate		100			kHz
DC ACCURACY					
Integral Linearity Error				8	LSB(1)
Differential Linearity Error				+3, –2	LSB
No Missing Codes		15			Bits
Transition Noise(2)			1.3		LSB
Full Scale Error(3, 4)				±1	%
Full Scale Error Drift			±10		ppm/°C
Full Scale Error(3, 4)	Ext. 2.50V Ref		±1		%
Full Scale Error Drift	Ext. 2.50V Ref		±5		ppm/°C
Bipolar Zero Error(3)			±13	±25	mV
Bipolar Zero Error Drift			±5		ppm/°C
Power Supply Sensitivity	+4.75V < V_D < +5.25V			±8	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 45kHz		87		dB
Total Harmonic Distortion	f_{IN} = 45kHz		–87		dB
Signal-to-(Noise and Distortion)	f_{IN} = 45kHz		80		dB
	–60dB Input		30		dB
Signal-to-Noise	f_{IN} = 45kHz		80		dB
Full-Power Bandwidth(6)			250		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			Sufficient to Meet AC Specs		
Transient Response	FS Step			2	µs
Overvoltage Recovery(7)			5		µs
REFERENCE					
Internal Reference Voltage		2.48	2.5	2.52	V
Internal Reference Source Current	Must Use External Buffer		1		µs
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.50V Ref			100	µA
DIGITAL INPUTS					
Logic Levels:					
V_{IL}		–0.3		+0.8	V
V_{IH}		+4.0		V_D +0.3V	V
I_{IL}				±10	µA
I_{IH}				±10	µA
DIGITAL OUTPUTS					
Data Format			Serial 16 Bits		
Data Coding			Binary Two's Complement		
V_{OL}	I_{SINK} = 1.6mA			+0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V
Leakage Current	High-Z-State, V_{OUT} = 0V to V_{DIG}			±5	µA
Output Capacitance	High-Z-State			15	pF
POWER SUPPLIES					
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{CC}		±11.4		±18	V
I_{DIG}			0.3		mA
I_{ANA}			16		mA
V_{CC}			7		mA
Power Dissipation, f_S = 100kHz				450	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, θ_{JA}					
Plastic PLCC			75		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input SDM506/507, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figures 10 and 11. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Analog Inputs:	
$R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
CAP	V_{ANA} +0.3V to A_{GND} –0.3V
REF	Indefinite Short to A_{GND}, Momentary Short to V_{ANA}
Analog Input Overvoltage:	
CH1-CH16 V_{CC+}	+20V
V_{CC-}	–20V
Supplies:	
V_{DIG}	+7V
V_{ANA}	+7V
V_{CC}	±18V
V_{DIG} to V_{ANA}	±0.3V
DGND to AGND	±0.3V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
SDM506	44-Pin PLCC	329	–40°C to +85°C
SDM507	44-Pin PLCC	329	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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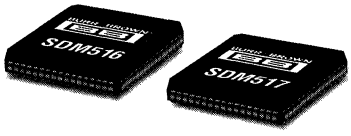


SDM516/517

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

16-Channel Single-Ended Input 16-Bit 100kHz Parallel Output DATA ACQUISITION SYSTEM

FEATURES

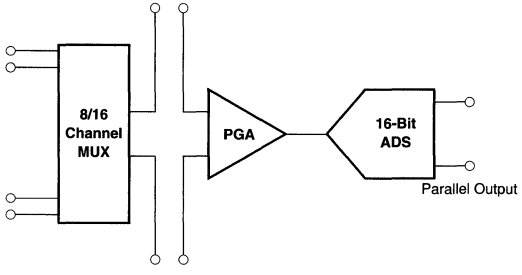
- 16-BIT RESOLUTION
- 100kHz THROUGHPUT
- PROGRAMMABLE GAINS (1, 10, 100, 1000)
- 16-, or 18-BIT DATA BUS INTERFACE
- 16 SINGLE-ENDED INPUTS: SDM516
- 8 DIFFERENTIAL INPUTS: SDM517
- OVERVOLTAGE PROTECTION
- ANALOG INPUTS: 70Vp-p
- 68-PIN PLCC PACKAGE

DESCRIPTION

The SDM516/517 are 16-channel, single-ended and 8-channel differential data acquistion systems with 16-bit resolution, parallel outputs and programmable gains of 1, 10, 100 and 1,000.

All these features are contained within a space-saving 68-pin plastic leaded chip carrier providing the ideal data acquisition solution when space is at a premium.

The SDM516/517 will accept industry standard ±10V analog inputs. For low level signals, dynamic range can be increased by using the programmable gain amplifier. Input overvoltage protection on the analog input channels provide fault-free operation for input voltages up to ±35V.



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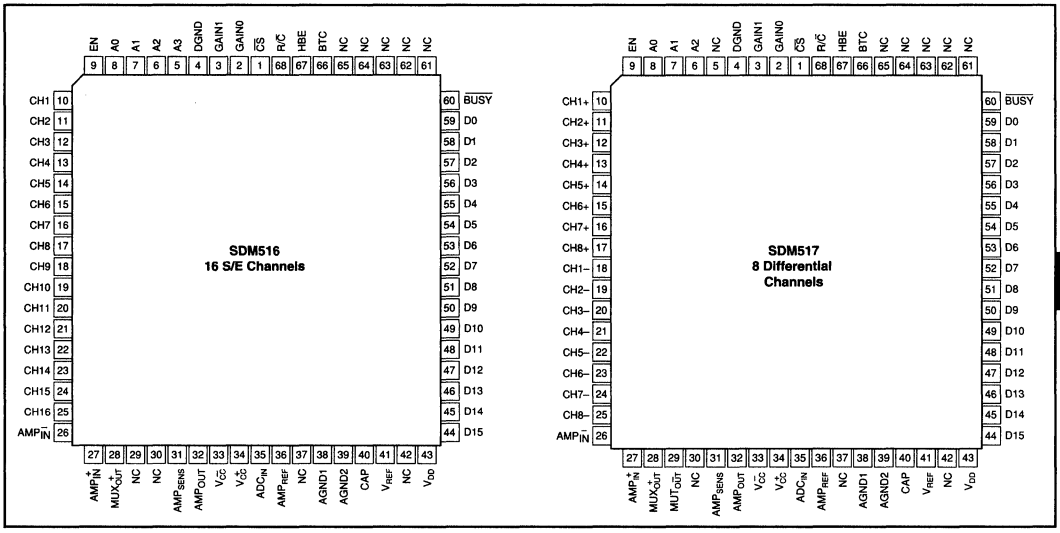
SPECIFICATIONS—PRELIMINARY

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, ±V_{CC} = ±15V, ±10V input range, and G = 1 using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	SDM516/517 MIN	SDM516/517 TYP	SDM516/517 MAX	UNITS
RESOLUTION				16	Bits
ANALOG INPUT					
Voltage Ranges			±10		V
Input Impedance: On Channel	10^{10}		10		GΩ
Off Channel	10^{10}		10		GΩ
Input Capacitance: On Channel	20		20		pF
Off Channel	20		20		pF
THROUGHPUT SPEED					
Conversion Time			7.6	8	µs
Complete Cycle	Acquire and Convert			10	µs
Throughput Rate		100			kHz
DC ACCURACY					
Integral Linearity Error		6		8	LSB(1)
Differential Linearity Error				+3, –2	LSB
No Missing Codes		15			Bits
Transition Noise(2)			1.3		LSB
Full Scale Error(3,4)				±1	%
Full Scale Error Drift			±10		ppm/°C
Full Scale Error(3,4)	Ext. 2.50V Ref		±1		%
Full Scale Error Drift	Ext. 2.50V Ref		±5		ppm/°C
Bipolar Zero Error(3)			±13	±25	mV
Bipolar Zero Error Drift			±5		ppm/°C
Power Supply Sensitivity	+4.75V < V_D < +5.25V			±8	LSB
V_{DIG} = V_{ANA} = V_D	10V < ±V_{CC} < 15V			±1	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 45kHz		87		dB
Total Harmonic Distortion	f_{IN} = 45kHz		87		dB
Signal-to-(Noise and Distortion)	f_{IN} = 45kHz		80		dB
	–60dB Input		30		dB
Signal-to-Noise	f_{IN} = 45kHz		80		dB
Full-Power Bandwidth(6)			250		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			Sufficient to Meet AC Specs		
Transient Response	FS Step			2	µs
Overvoltage Recovery(7)			5		µs
REFERENCE					
Internal Reference Voltage		2.48	2.5	2.52	V
Internal Reference Source Current	Must Use External Buffer		1		µs
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.50V Ref			100	µA
DIGITAL INPUTS					
Logic Levels:					
V_{IL}		–0.3		+0.8	V
V_{IH}		+4.0		V_D +0.3V	V
I_{IL}				±10	µA
I_{IH}				±10	µA
DIGITAL OUTPUTS					
Data Format			16-Bit Parallel		
Data Coding					
V_{OL}	I_{SINK} = 1.6mA			+0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V
Leakage Current	High-Z-State, V_{OUT} = 0V to V_{DIG}			±5	µA
Output Capacitance	High-Z-State			15	pF
POWER SUPPLIES					
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{CC}		±11.4		±18	V
I_{DIG}			0.3		mA
I_{ANA}			16		mA
V_{CC}			7		mA
Power Dissipation	f_S = 100kHz			450	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, θ_{JA}					
Plastic PLCC			75		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input SDM516/517, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 9. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Analog Inputs:
- $R1_{IN}$ ..... ±25V
- $R2_{IN}$ ..... ±25V
- $R3_{IN}$ ..... ±25V
- CAP ..... V_{ANA} +0.3V to A_{GND} –0.3V
- REF ..... Indefinite Short to A_{GND}, Momentary Short to V_{ANA}

Analog Input Overvoltage:
- CH1-CH16 V_{CC+} ..... +20V
- V_{CC-} ..... –20V

Supplies:
- V_{DIG} ..... +7V
- V_{ANA} ..... +7V
- V_{CC} ..... ±18V
- V_{DIG} to V_{ANA} ..... ±0.3V
- DGND to AGND ..... ±0.3V

Digital Inputs ..... –0.3V to V_{DIG} +0.3V
Maximum Junction Temperature ..... +165°C
Lead Temperature (soldering, 10s) ..... +300°C

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
SDM516	68-Pin PLCC	312	–40°C to +85°C
SDM517	68-Pin PLCC	312	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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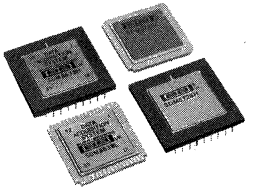


SDM862
SDM863
SDM872
SDM873

16 Single Ended/8 Differential Input 12-BIT DATA ACQUISITION SYSTEMS

FEATURES

- COMPLETE 12-BIT DATA ACQUISITION SYSTEM IN A MINIATURE PACKAGE
- INPUT RANGES SELECTABLE FOR UNIPOLAR OR BIPOLAR OPERATION
- THROUGHPUT RATES:

	862/3	872/3
8-BIT ACCURACY:	45kHz	67kHz
12-BIT ACCURACY:	33kHz	50kHz

- SELECTABLE GAINS OF 1, 10, AND 100
- FULL MICROPROCESSOR COMPATIBLE INTERFACE
- GUARANTEED NO MISSING CODES OVER TEMPERATURE
- SURFACE-MOUNT OR PIN GRID ARRAY PACKAGE OPTIONS
- HIGH RELIABILITY SCREENED VERSIONS AVAILABLE
- FULL SPECIFICATION OVER THREE TEMPERATURE RANGES: 0 to +70°C, –25 to +85°C, –55 to +125°C
- EVERY UNIT SUPPLIED WITH ELECTRICAL TEST DATA

APPLICATIONS

- INDUSTRIAL PROCESS MONITORING
- AIRBORNE SYSTEMS MONITORING
- ENGINE MONITORING
- POWER PLANT MONITORING
- SECURITY SYSTEMS MONITORING
- AUTOMATIC TEST EQUIPMENT

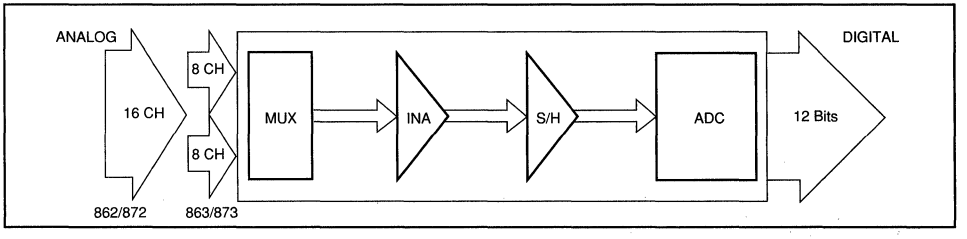
DESCRIPTION

16 Single-Ended Inputs:	SDM862	SDM872
8 Differential Inputs:	SDM863	SDM873
33kHz Throughput Rate:	SDM862	SDM863
50kHz Throughput Rate:	SDM872	SDM873

The SDM components are complete, pin-compatible, data acquisition systems housed in a hermetically sealed 1"-square leadless chip carrier or a 1.1"-square pin grid array. The small package outlines and low power consumption provide an ideal data acquisition solution when space is at a premium.

The devices comprise of an input multiplexer, instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and three-state buffers.

The SDM family will accept unipolar or bipolar voltage inputs in the range 0 to +10V, ±5V and ±10V. For low-level signals, jumper-selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. System integration is simplified by the microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter.



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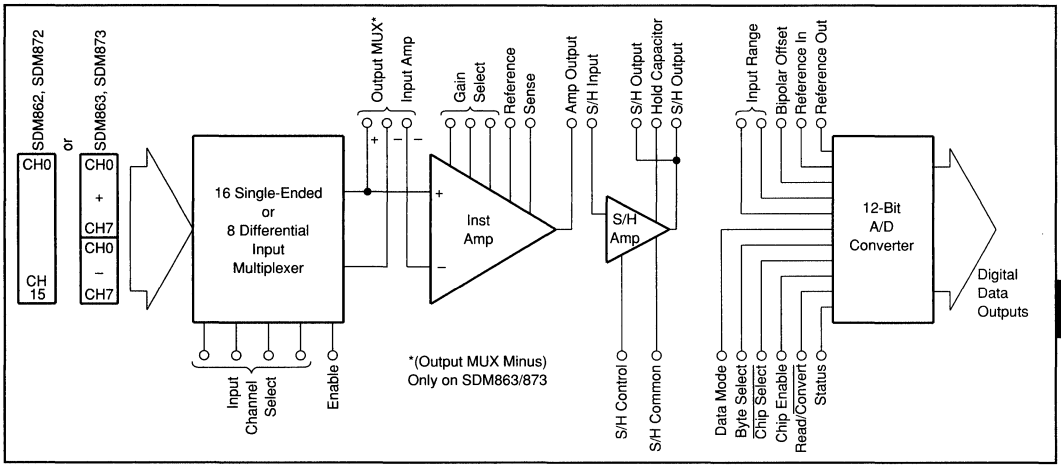


SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF. **All grades are burned-in at +125°C for 48 hours min.**

PARAMETER	SDM862/863/872/873 J, A, R MIN	TYP	MAX	SDM862/863/872/873 K, B, S MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Bipolar			±5, ±10				V
Unipolar			0-10				V
Input Impedance: On Channel		10^{10}			*		Ω
Off Channel		10^{10}			*		Ω
Input Capacitance: On Channel		20			*		pF
Off Channel		20			*		pF
CMRR (20VDC to 1kHz)	80	85		*	*		dB
Crosstalk (20Vp-p, 1kHz) (1)		–85	–80		*	*	dB
Feedthrough (at 1kHz) (1)		–85	–80		*	*	dB
Offset (channel to channel) G = 1 (2)		30	100		*	*	µV
Input Bias Current/Channel		1	5		*	*	nA
Input Voltage Range (3)	+10	+11		*	*		V
	–10	–15		*	*		V
DIGITAL (7, 8)							
MUX Input Channel Select: Logic '1'		5	30		*	*	µA
Logic '0'		5	30		*	*	µA
MUX Input: Logic High	4.0			*			V
Logic Low			0.8			*	V
S/H Command: Logic '1'		0.2			*		nA
Logic '0'		5	30		*	*	µA
ADC Section: Logic '1'			10			*	µA
Logic '0'			10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Integral Linearity (4)			±0.024			±0.012	%FSR
Differential Linearity (4)			±0.024			*	%FSR
No Missing Codes		Over Operating Temperature Range					
Gain Error (5): G = 1			0.5			*	%
G = 100		0.9			*		%
Unipolar Offset Error (5)		16			*		mV
Bipolar Offset Error (5)			50			*	mV
Noise Error							
(Measured at S/H Output) G = 1		0.5	1		*	*	mVp-p
Droop Rate		50	500		*	*	µV/ms
Temperature Coefficients:							
Unipolar Offset			20			15	ppm of FSR/°C
Bipolar Offset			30			25	ppm of FSR/°C
Full-Scale Calibration			60			35	ppm of FSR/°C

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF.

PARAMETERS	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM TIMINGS							
ADC Conversion Time: SDM862/SDM863	9	20	25	*	*	*	µs
SDM872/SDM873	9	12	15	*	*	*	µs
S/H Aperture Delay		50			*		ns
S/H Aperture Uncertainty		2			*		ns
TIMING							
Throughput (Serial Mode)							
SDM862/SDM863			22			*	kHz
SDM872/SDM873			28			*	kHz
(Overlap Mode):							
SDM862/SDM863			33			*	kHz
SDM872/SDM873			50			*	kHz
MULTIPLEXER (6)							
Switching Time (between channels)		+1.5			*		µs
Settling Time (10V step to 0.02%)		2.5			*		µs
Enable Time 'ON'		1	2		*	*	µs
'OFF'		0.25	0.5		*	*	µs
INSTRUMENTATION AMPLIFIER (6)							
Settling Time (20V step to 0.01%)							
G = 1		5	12.5		*	*	µs
G = 10		3	7.5		*	*	µs
G = 100		4	7.5		*	*	µs
Slew Rate	12	17		*	*		V/µs
S/H AMPLIFIER (6)							
Acquisition (10V step to 0.01%)		5			*		µs
Aperture Delay		50			*		ns
Hold Mode Settling Time		1.5			*		µs
Slew Rate		10			*		V/µs
OUTPUT							
DIGITAL DATA							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (Sink = 1.6mA)			+0.4			*	V
Logic 1 (Source = 500µA)	+2.4			*			V
Leakage (Data Bits Only), High-Z State	–5	0.1	+5	*	*	*	µA
POWER SUPPLY REQUIREMENTS							
Rated Voltage: Analog (±V_{CC})	14.25	15	15.75	*	*	*	VDC
Digital (V_{DD})	4.5	5	5.5	*	*	*	VDC
Supply Drain: +15V		13	22		*	*	mA
–15V		22	30		*	*	mA
+5V		11	15		*	*	mA
Power Dissipation		580	855		*	*	mW
TEMPERATURE RANGE							
Operating Temperature Range							
JH, KH/JL, KL	0		70	*		*	°C
AH, BH/AL, BL	–25		+85	*		*	°C
RH, SH/RL, SL	–55		+125	*		*	°C
Storage Temperature Range	–65		+150	*		*	°C

* Specification same as SDM862/863/872/873J, A, R grades.

NOTES: (1) Measured at the same and hold output. (2) Measured with all input channels grounded. (3) The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed. (4) Applicable over full operating temperature range. NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE. (5) Adjustable to zero using external potentiometer or select-on-test resistor. (6) Specifications are at +25°C and measured at 50% level of transition. (7) When using TTL drivers a 1kΩ pull-up resistor should be used. (8) Muxes operate in a break-before-make manner.

DIGITAL TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tdsc	Status Delay from CE		100	200	ns
thec	CE Pulse Width	50	30		ns
tssc	$\overline{CS}$ to CE Setup	50	20		ns
thsc	$\overline{CS}$ Low During CE High	50	20		ns
tsrc	R/$\overline{C}$ to CE Setup	50	0		ns
thrc	R/$\overline{C}$ Low During CE High	50	20		ns
tsac	Byte Select to CE Setup	0	0		ns
thac	Byte Selected Valid During CE High	50	20		ns
tc 86X	Conversion Time: 12 Bit Cycle	9	20	25	µs
	8 Bit Cycle	6	13	17	µs
tc 87X	Conversion Time: 12 Bit Cycle	9	12	15	µs
	8 Bit Cycle	6	8	10	µs
READ MODE					
tdd	Access Time from CE		75	150	ns
thd	Data Valid after CE Low	25	35		ns
thl	Output Float Delay		100	150	ns
tssr	$\overline{CS}$ to CE Setup	50	0		ns
tsrr	R/$\overline{C}$ to CE Setup	0	0		ns
tsar	Byte Select to CE Setup	50	25		ns
thsr	$\overline{CS}$ Valid after CE Low	0	0		ns
thrr	R/$\overline{C}$ High after CE Low	0	0		ns
thar	Byte Select Valid after CE Low	50	25		ns
ths 86X	Status Delay after Data Valid	100	500	1000	ns
ths 87X	Status Delay after Data Valid	100	300	600	ns

ABSOLUTE MAXIMUM RATINGS[1]

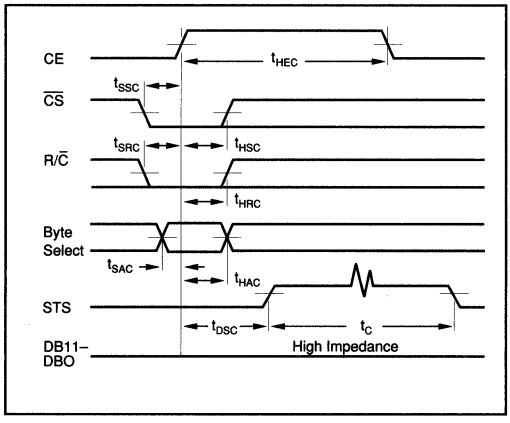
$+V_{CC}$ to ACOM	–0.5V to +16V
$-V_{CC}$ to ACOM	+0.5 to –16V
$+V_{DD}$ to DCOM	–0.5V to +7.0V
Analog Input Signal Range	$+V_{CC}$ +20V to $-V_{CC}$ –20V
Digital Input Signal	–0.5V to $+V_{DD}$
ACOM to DCOM	±1V

NOTE: (1) Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functions operation under any of these conditions is not necessarily implied.

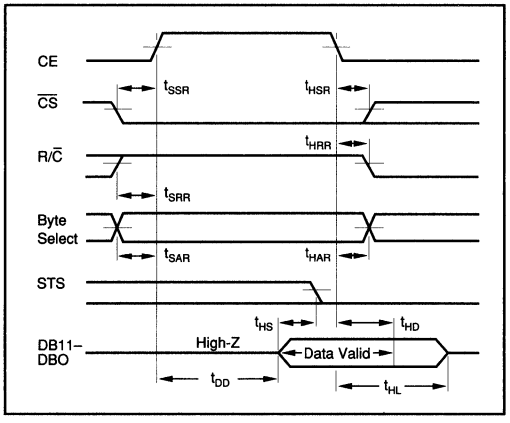
/QM HIGH RELIABILITY SCREENING

High Power Internal Visual Inspection	Burr-Brown Spec. QC2010
Stabilization Bake	24Hr at +150°C
Temperature Cycling	10 Cycles –65°C to +150°C
Constant Acceleration	30kG, Y1 axis
Hermeticity Fine Leak	Helium 5 x 10^{-8}cc/s
Hermeticity Gross Leak	Fluorocarbon
Burn-In	160Hr at +125°C

CONVERSION CYCLE TIMING



READ CYCLE TIMING



ORDERING INFORMATION[1]

Model	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)	Model	Input	LCC, PGA Package	Accuracy (% FSR)	Throughput	Temperature Range (°C)
SDM862J	16SE	L,H	±0.024	33kHz	0 to +70	SDM863J	8DIF	L, H	±0.024	33kHz	0 to +70
SDM862K	16SE	L,H	±0.012	33kHz	0 to +70	SDM863K	8DIF	L, H	±0.012	33kHz	0 to +70
SDM862A	16SE	L,H	±0.024	33kHz	–25 to +85	SDM863A	8DIF	L, H	±0.024	33kHz	–25 to +85
SDM862B	16SE	L,H	±0.012	33kHz	–25 to +85	SDM863B	8DIF	L, H	±0.012	33kHz	–25 to +85
SDM862R	16SE	L,H	±0.024	33kHz	–55 to +125	SDM863R	8DIF	L, H	±0.024	33kHz	–55 to +125
SDM862S	16SE	L,H	±0.012	33kHz	–55 to +125	SDM863S	8DIF	L, H	±0.012	33kHz	–55 to +125
SDM872J	16SE	L,H	±0.024	50kHz	0 to +70	SDM873J	8DIF	L,H	±0.024	50kHz	0 to +70
SDM872K	16SE	L,H	±0.012	50kHz	0 to +70	SDM873K	8DIF	L,H	±0.012	50kHz	0 to +70
SDM872A	16SE	L,H	±0.024	50kHz	–25 to +85	SDM873A	8DIF	L,H	±0.024	50kHz	–25 to +85
SDM872B	16SE	L,H	±0.012	50kHz	–25 to +85	SDM873B	8DIF	L,H	±0.012	50kHz	–25 to +85
SDM872R	16SE	L,H	±0.024	50kHz	–55 to +125	SDM873R	8DIF	L,H	±0.024	50kHz	–55 to +125
SDM872S	16SE	L,H	±0.012	50kHz	–55 to +125	SDM873S	8DIF	L,H	±0.012	50kHz	–55 to +125

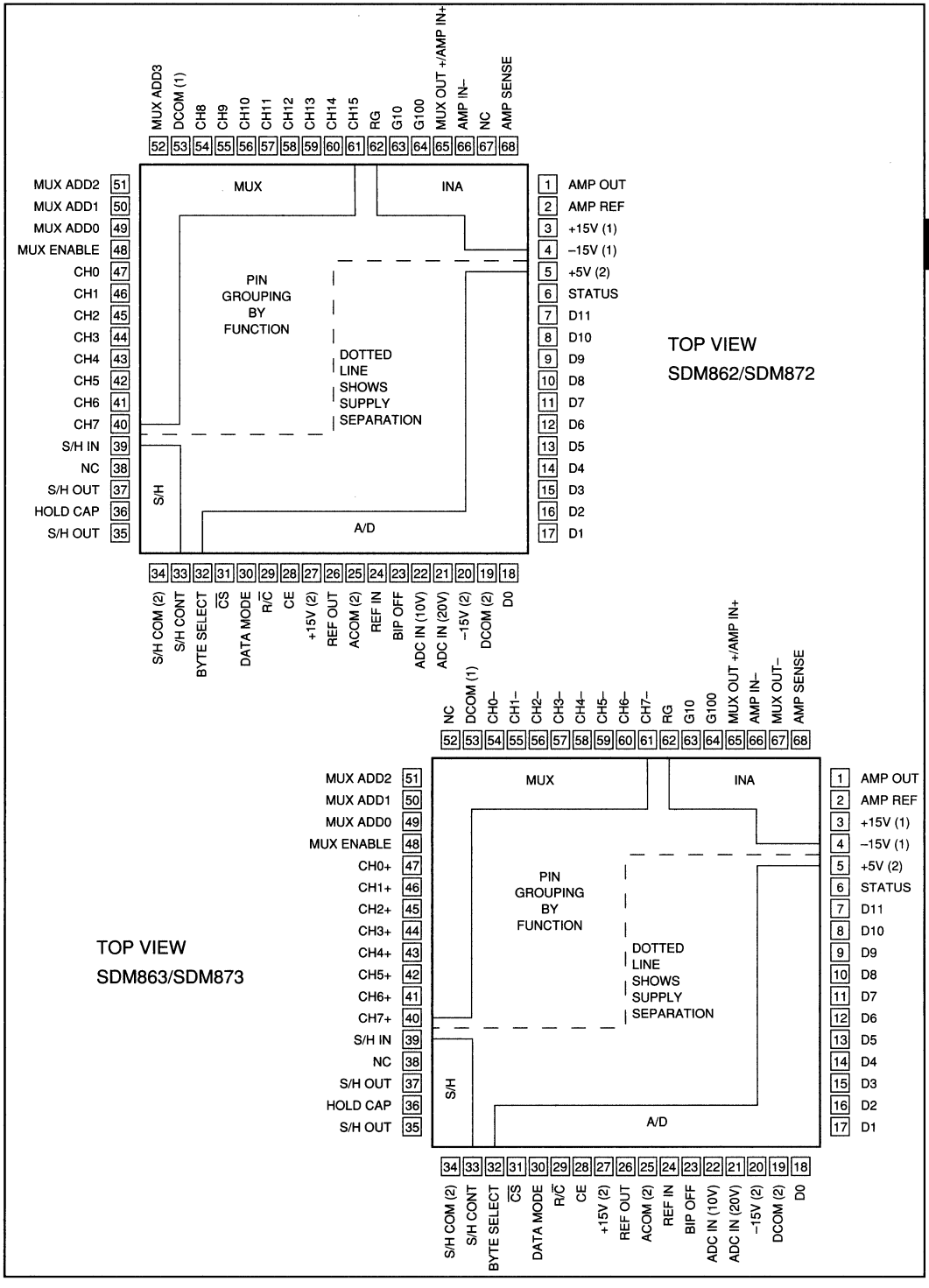
NOTE: (1) 16 single-ended inputs, LCC package, with accuracy of 0.24% FSR. Temp Range of 0°C to +70°C and throughput of 33kHz = SDM862JL.

PACKAGE INFORMATION

MODEL	DESCRIPTION	PACKAGE DRAWING NUMBER[1]
PC862/863-1	LCC (Socketed) Evaluation PCB[2]	907
PC862/863-2	PGA Evaluation PCB	906

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Socket is MC0068-1.

PIN CONFIGURATIONS



PIN DESIGNATION	DEFINITION	COMMENTS SDM8X2 = SDM862 OR SDM872
CH0 to CH15 CH0 to CH7 (+, –) (PINS 40 to 47, 54 to 61)	Channel Inputs	Analog Inputs (Total 16) for single-ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT+/AMP IN+ (PIN 65)	MULTIPLEXER "HI" OUTPUT	On the SDM8X2 this is the multiplexer output. On the SDM8X3 it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUXOUT (Pin 67)	MULTIPLEXER "LO" OUTPUT	This pin is used on the SDM8X3 only. It should be connected to the negative input of the instrumentation amplifier.
AMP IN (Pin 66)	Negative input of instrumentation amplifier	On the SDM8X2 this should be connected to analog common. On the SDM8X3 it should be connected to Muxout—(Pin 67).
AMP OUT (Pin 1)	Output of instrumentation amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE (Pin 68)	Output sense line of instrumentation amplifier	This pin will normally be connected direct to AMP OUT (Pin 1).
AMP REF (Pin 2)	Reference for amplifier output	This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to optimize system accuracy.
S/H OUT (Pins 35/37)	Output of sample/hold amplifier	Two pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.
HOLD CAP (Pin 36)	Connection for hold capacitor on S/H amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using Pins 35 and 37.
ADC IN (20V); ADC IN (10V) (Pins 21, 22)	Inputs to A/D converter	Connect to S/H amplifier output. Use appropriate pin for desired range.
RG, G10, G100 (Pins 62, 63, 64)	Gain settling pins on instrumentation amplifier	For Gain = 1, no connections. For Gain = 10, connect G10 to RG. For Gain = 100, connect G100 to RG.
REF OUT (PIN 26)	10V Reference voltage	This is the reference voltage for the A/D converter.
REF IN, BIP OFF (Pins 24, 23)	Reference input and offset input to A/D converter	Connect trim potentiometers (or select-on-test resistors) to these pins for unipolar or bipolar operation as shown in Figures 12, 13.
S/H IN (Pin 39)	Input to sample/hold amplifier	Connect to amp out (Pin 1).
MUX ENABLE (Pin 48)	Multiplex enable/disable	Logic '1' on this pin will enable a selected channel on the internal multiplexer. Logic '0' de-selects all channels.
MUX ADD0 to MUX ADD3 (Pins 49 to 52)	Address inputs for channel selection	These address lines select a particular channel as specified in Figure 24.
S/H CONT (Pin 33)	Track/Hold control on S/H amplifier	Logic '1' holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.
S/H COM (Pin 34)	Reference for S/H logic control	Connect to digital common.
D0 to D11 (Pins 7 to 18)	3-state digital outputs	The 12- or 8-bit result of a conversion is available as output on these pins (D0-LSB, D11-MSB).
STATUS (Pin 6)	Status of A/D conversion	This output is at logic '1' while the internal A/D converter is carrying out a conversion. This pin may be used to directly control the S/H amplifier.
CE (Pin 28)	Chip enable	This input must be at logic '1' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
$\overline{CS}$ (Pin 31)	Chip select	This input must be at logic '0' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
R/$\overline{C}$ (Pin 29)	Read/convert	Data can be read when this pin is logic '1' or a conversion can be initiated when this pin is logic '0'. This pin is typically connected to the R/$\overline{W}$ control line of a microprocessor-based system (see Figures 10, 17, 18, 19, 20).
DATA MODE (Pin 30)	Select 12- or 8-Bit Data	When data mode is at logic '1' all 12 output data bits are enabled simultaneously. When data mode is at logic '0' MSBs and LSBs are controlled by byte select (Pin 32).
BYTE SELECT (Pin 32)	Byte address, short cycle	When reading output data, byte select at logic '0' enables the 8 MSBs. Byte select at logic '1' enables the 4 LSBs. The 4 LSBs can therefore be connected to four of the MSB lines for inter-connection to an 8-bit bus. In start convert mode, logic '0' enables a 12-bit conversion while logic '1' will short cycle the conversion to 8 bits (see Figure 10).
+15V(1), +15V(2)(Pins 3, 27)	Power Supply	Connect to +15V supply using decoupling as indicated in Figures 15, 16.
–15V(1), –15V(2)(Pins 4, 20)	Power Supply	Connect to –15V supply using decoupling as indicated in Figures 15, 16.
ACOM(2) (Pin 25)	Analog Common	Analog common connection. Note that a common (including digital common) should be connected together at one point close to the device.
DCOM (1) (Pin 53)	Reference for MUX logic control.	Connect to digital common.
+5V (Pin 5)	Logic power supply	Connect to +5V digital supply line with decoupling as in Figures 15, 16.
DCOM(2) (Pin 19)	Reference for A/D converter control lines	Connect to S/H common at one point close to device.
NC (Pin 38)	No internal connection	

SYSTEM DESCRIPTION

The SDM comprises four circuit elements—an input-protected multiplexer, an instrumentation amplifier, a sample/hold amplifier, and an analog-to-digital converter.

INSTALLATION

MULTIPLEXER

The SDM family has a choice of input multiplexers (MUX).

SDM862 and SDM872: 16 single-ended inputs
SDM863 and SDM873: 8 differential inputs

On all models, the analog inputs may be expanded using the enable control. See Figure 1. When the enable is at a logic "0," the internal MUX is disabled, allowing additional multiplexers to be connected in parallel. The limiting factor for the number of additional multiplexers is the cumulative effect of leakage current flowing in the signal source impedance, causing offset errors.

Differential inputs will generally eliminate the noise associated with common system grounds, but care must be taken to ensure that neither of the differential inputs exceed the maximum input range. Otherwise, signal distortion will result. A return path for the input bias currents must always be provided. This prevents the charging of stray capacitances in applications using floating sources, such as transformers and thermocouples. Multiplexer inputs are protected from overvoltage, as indicated in the electrical specifications, and should be current limited to 20mA.

Where high-speed operation is required and channels require rapid sampling, then it is important to buffer the inputs against the effect of current sharing between the MUX output capacitance and the input filter capacitance. See Figure 2.

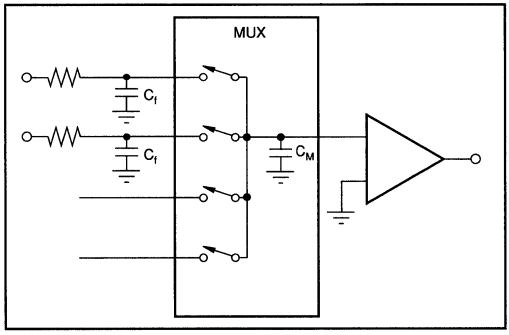


FIGURE 2. Filter and MUX Capacitance.

All data acquisition systems using a MUX require consideration of the errors that may be introduced by MUX output capacitance. The applications information explains this more fully in the input filtering section.

Shown in Figure 3 is an application that demonstrates the flexibility of signal conditioning and gives the opportunity to use a higher bandwidth filter. Diodes shown are low leakage types (1na). The low output impedance of the amplifiers reduces the time taken to charge MUX capacitance C_M.

INSTRUMENT AMPLIFIER

The instrument amplifier (INA) presents a very high input impedance to the signal source, eliminating gain errors introduced by voltage divider action between the source output impedance and SDM input impedance. Where the differential models are used, the INA performs the differential to single-ended conversion required to drive the sample/hold amplifier. Gains may be set by using external jumpers, to values of 1 (no jumper), 10 and 100. For gains other than these presets, the following formula may be used to find an external resistor value to add in series with the G = 10 or G = 100 jumpers.

$$R_{ext} = \frac{40k\Omega}{G-1} - Ri$$

Where Ri = 4444Ω, G = 10 input.
404Ω, G = 100 input.

It should be noted that the internal gain set resistors have a ±20% tolerance and ±20ppm/°C drift.

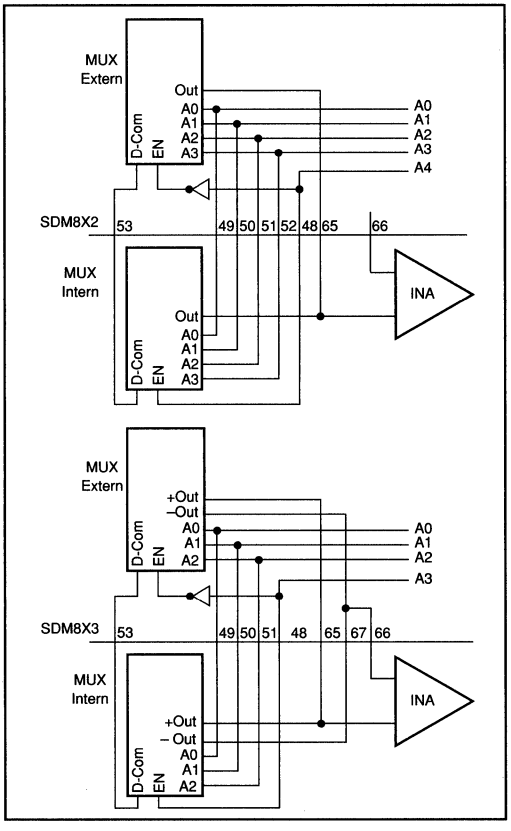


FIGURE 1. External Multiplexer Connections for Differential and Single-Ended Operation.

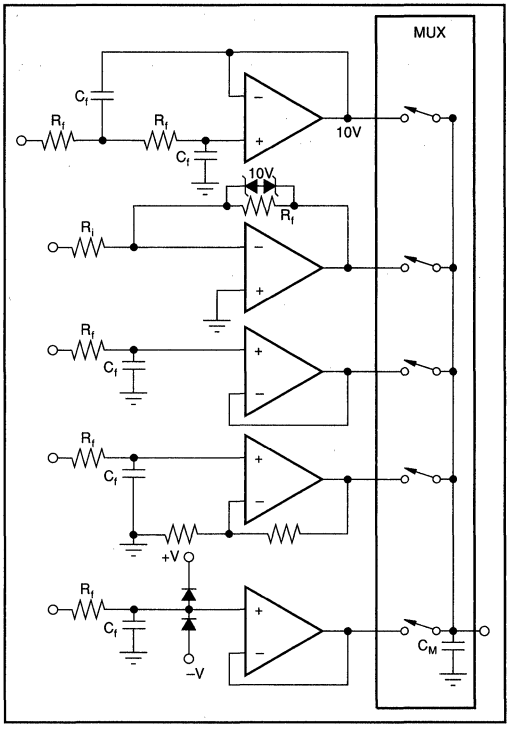


FIGURE 3. Example Application Illustrating Flexible Signal Conditioning.

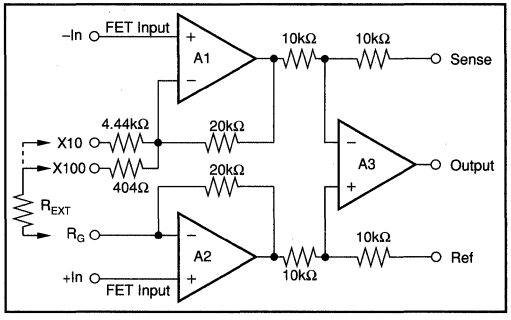


FIGURE 4. Use External Gain Set Resistor.

Where it is necessary to keep the input amplifiers from saturating or increasing the overall gain, then the gain of the output amplifier can be increased from unity by using the circuit in Figure 5.

The values of the resistors in Figure 5 are in the following table.

O/P GAIN	R_1 and R_3 Ω	R_2 Ω
2	1200	2740
5	1000	511
10	1500	340

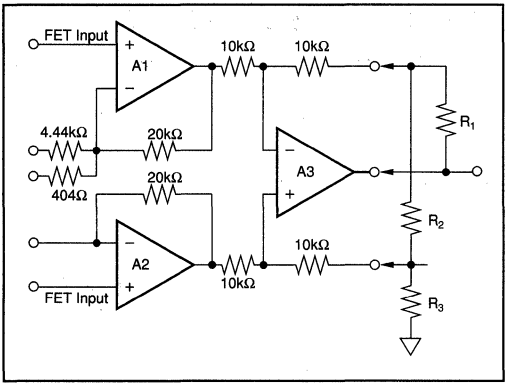


FIGURE 5. Increasing Output Amplifier Gain.

Matching of R_1 and R_3 is required to maintain high common-mode rejection (CMR), R_2 sets the gain and may be varied without effect on CMR.

To ensure that the effects of temperature are minimized when altering the gain with external components, it is very important to use low tempco resistors. When connecting the output sense, ensure that series resistance is minimized because resistance present will degrade CMR.

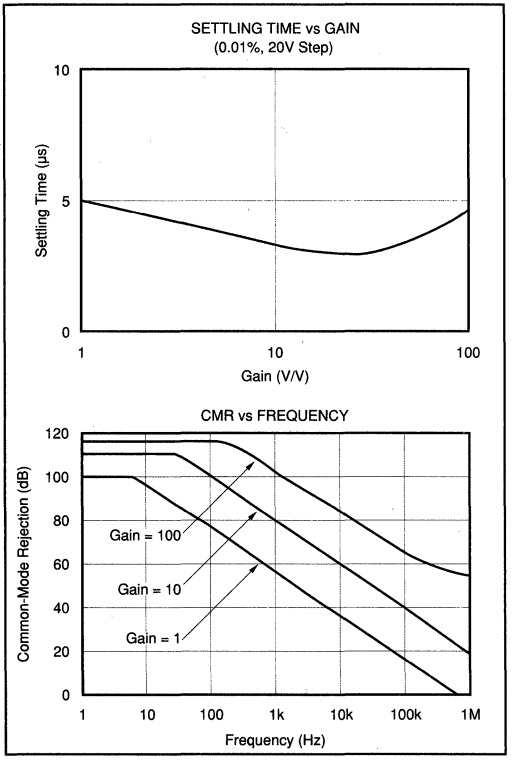


FIGURE 6. Typical INA Settling Time and CMR.

Some applications may require programmable gains. This may be realized with Figure 7.

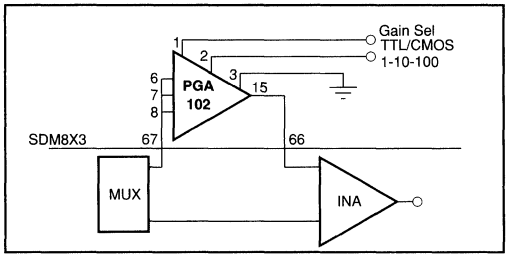


FIGURE 7. Setting Programmable Gains.

SAMPLE/HOLD AMPLIFIER

The Sample/Hold amplifier (S/H) is used to track the incoming signal and "hold" the required instantaneous value so that it does not change while the ADC is carrying out its conversion. Timing for the S/H may be derived from the STATUS output of the ADC, with care being taken to comply with the SDM timing considerations.

Capacitors with high insulation resistance and low dielectric absorption such as Teflon™, polystyrene or polypropylene should be used as storage elements. (Polystyrene should not be used above +80°C.) Teflon™ is recommended for high temperature operation. Care should be taken in the printed circuit layout to minimize stray capacitance and leakage currents from the capacitor to minimize charge offset and droop errors. The use of a guard ring driven by the S/H output around the pin connecting to the hold capacitor is recommended. (Refer to the application board layout for an example of this.)

The value of the external hold capacitor determines the droop rate, charge offset and acquisition time of the S/H, Figure 8. Droop rate for the SDM is specified with a hold capacitor value of 4700pf. There is a trade-off between acquisition time and droop rate, as the hold capacitor is increased in value it takes longer to charge, and hence there is a corresponding increase in acquisition time and reduction in droop rate. The droop rate is determined by the amount of leakage present in the SDM, board leakage and the dielectric absorption of the hold capacitance. The hold capacitor is also a compensation element for the S/H and should not be reduced below 2nf for good stability. The offset error in sample mode is not affected by the hold capacitor. However, during the transition to hold mode there is approximately 5pC of charge injected into the hold capacitor, causing an offset error that has been nulled for use with a 5nf hold capacitor. Any other value for the hold capacitor will cause a minor but fixed hold mode offset to be introduced, and is proportional to the change in value from 5nf. Therefore, the SDM should be offset nulled with the S/H in hold mode.

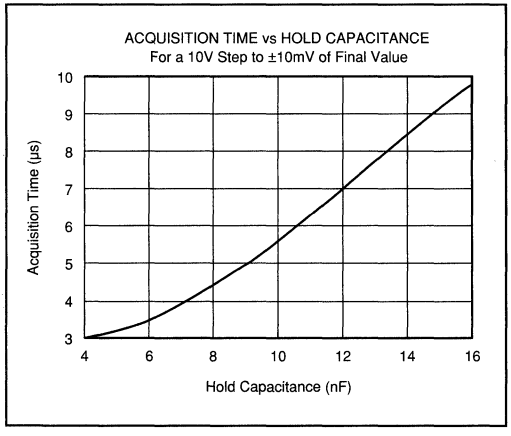


FIGURE 8. Acquisition Time vs Hold Capacitance for a 10V Step Settling to ±10mV of Final Value.

ANALOG-TO-DIGITAL CONVERTER

This circuit element converts the analog voltage presented by the sample/hold amplifier to a digital number in binary format under control of the digital signals detailed in Figure 9. The converter can convert unipolar and bipolar signals in the range 10V and 20V. It can be calibrated to remove gain and offset errors from the entire system. The converter contains its own clock, voltage reference, and microprocessor interface with 3-state outputs. The converter will normally be used to digitize signals to 12-bit resolution, but it can be short-cycled to provide 8-bit resolution at higher speed. The digital output is compatible with 8- or 16-bit data buses, the data format being selected by control signals as detailed in Figure 9.

CE	$\overline{CS}$	R/$\overline{C}$	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
∧	0	0	X	0	Initiate 12-bit conversion
∧	0	0	X	1	Initiate 8-bit conversion
1	∨	0	X	0	Initiate 12-bit conversion
1	∨	0	X	1	Initiate 8-bit conversion
1	0	∨	X	0	Initiate 12-bit conversion
1	0	∨	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

FIGURE 9. Control Input Truth Table.

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure). Thus, with the SDM connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV

below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Figure 13).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

The SDM is guaranteed to have no missing codes to 12-bit resolution over it's respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An SDM connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The SDM specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition 7FFH to 800H.

Bipolar offset error for the SDM is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

OPERATING INSTRUCTIONS

OPERATING MODES

The SDM can operate in one of two modes, namely serial and overlap, as shown in Figure 10. In serial mode, control of the device is such that a multiplexer channel X is first selected, time is then allowed for the instrumentation amplifier to settle, the sample/hold amplifier is set to HOLD mode and finally a conversion is carried out. This procedure is then repeated for channel Y. Faster throughput can be obtained using overlap mode. While a conversion is being

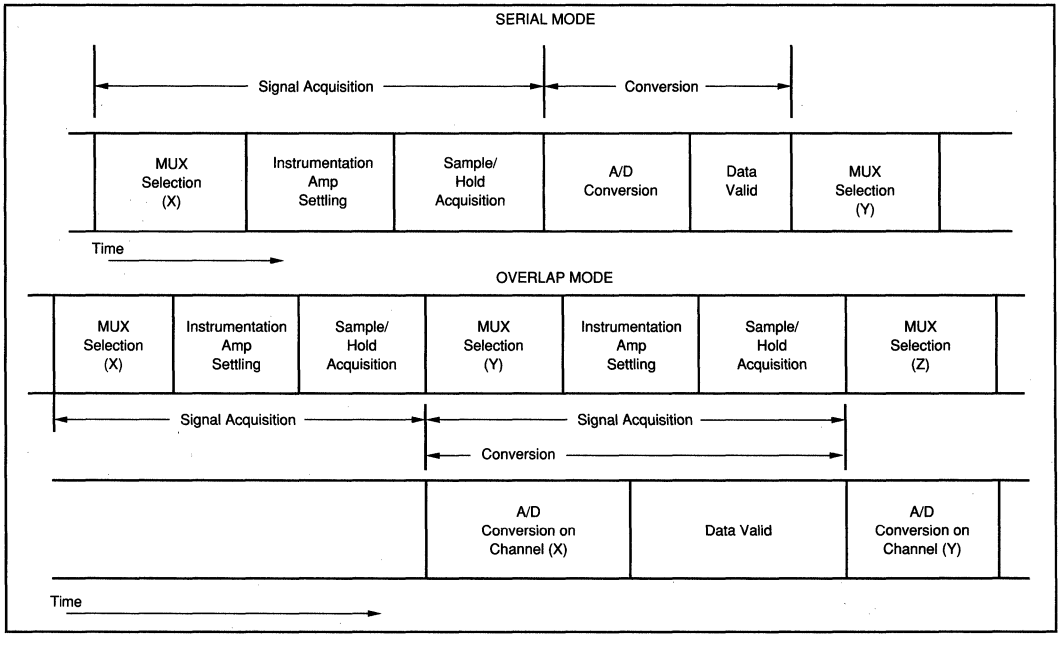


FIGURE 10. Serial and Overlap Modes of Operation.

carried out by the ADC on a voltage from channel X held on the sample/hold, channel Y is selected and the multiplexer and instrumentation amplifier allowed to settle. In this way, the total throughput time is limited only by the sum of the sample/hold acquisition time and the ADC conversion time.

CALIBRATION – UNIPOLAR

If adjustment of unipolar offset and gain are not required, then the gain set potentiometer in Figure 11 (Unipolar operation) may be replaced with a 50Ω, 1% metal film resistor, and the offset network replaced with a connection from pin 23 to ground.

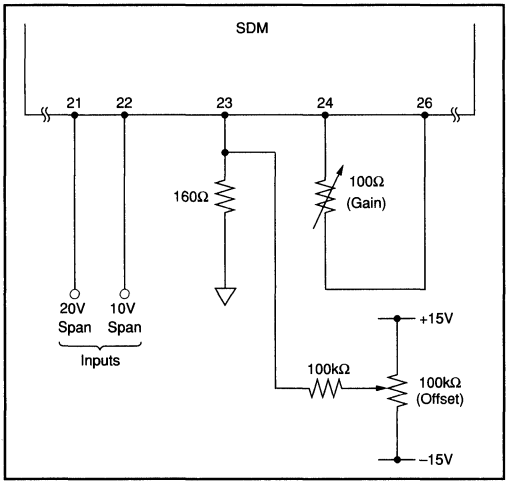


FIGURE 11. Unipolar Calibration.

CALIBRATION - BIPOLAR

If adjustment of bipolar offset and gain are not required then the gain set and offset potentiometers in Figure 12 (Bipolar operation) may both be replaced with 50Ω, 1% metal film resistors.

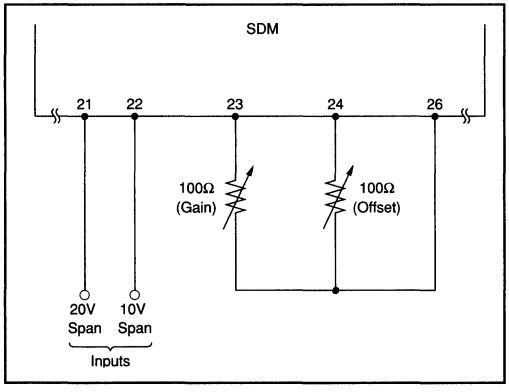


FIGURE 12. Bipolar Calibration.

CALIBRATION - GENERAL

The input voltage ranges of the ADC are 0-10V, ±5V and ±10V. Calibration in all ranges is achieved by adjusting the offset and gain potentiometers (indicated in Figures 11 and 12) such that the 000 to 001 code transition takes place at +1/2LSB from full-scale negative (–FS) and the FFE to FFF transition takes place at –3/2LSB from full-scale positive (+FS). The procedure is therefore to select the required range from Figure 13, apply the specified (–FS+1/2LSB) voltage to any selected input channel and adjust the offset potentiometer for the 000 to 001 transition. The (+FS–3/2LSB) voltage should then be applied to the same channel and the gain potentiometer adjusted for the FFE to FFF transition. The offset should always be made before the gain adjustment.

FULL-SCALE RANGE	000 TO 001 TRANSITION VOLT.	FFE TO FFF TRANSITION VOLT.	1LSB EQUALS
0–10V	+0.0012V	+9.9963V	2.44mV
±5V	–4.9988V	+4.9963V	2.44mV
±10V	–9.9976V	+9.9927V	4.88mV

FIGURE 13. Code Transition Ranges.

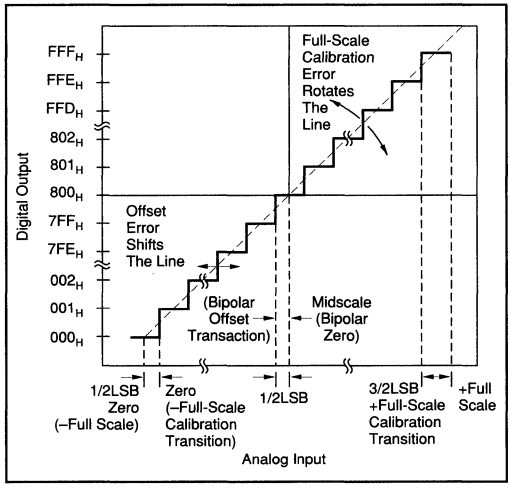


FIGURE 14. SDM Transfer Characteristic Terminology.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

It should be noted that the multiplexer/instrumentation amplifier section and sample/hold plus ADC section of the SDM have separate power connections. This is to enable more flexible grounding techniques to be implemented, Figures 15, 16. It also facilitates the use of independent decoupling of the analog front-end power supply, and the ADC plus associated digital circuitry power supply if desired. In this way, a separately decoupled analog front-end can be made to be substantially more immune to power supply noise generated by the ADC circuitry than if the

power supplies to the two sections were directly connected. This feature is important where low-level signals are in use or high input signal noise immunity is desired.

The output section has three grounds:

Pin 25 Analog Common, A/D Converter
Pin 34 S/H Amp Digital Input Reference
Pin 19 Digital Common, A/D Converter

The input section has one ground:

Pin 53 Common for digital MUX-inputs and power supply decoupling.

All grounds have to be interconnected externally to the SDM, and it is recommended that all grounds are connected via one track to a single point as close as possible to the SDM. To check that the grounding structure is correct, the ground tracking should be sketched and a grounding "tree" should result whereby all grounds route to a central point.

In general, layout should be such that analog and digital tracks are separated as much as possible with coupling between analog and digital lines minimized by careful lay-out. For instance, if the lines must cross they should do so at right angles to each other. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

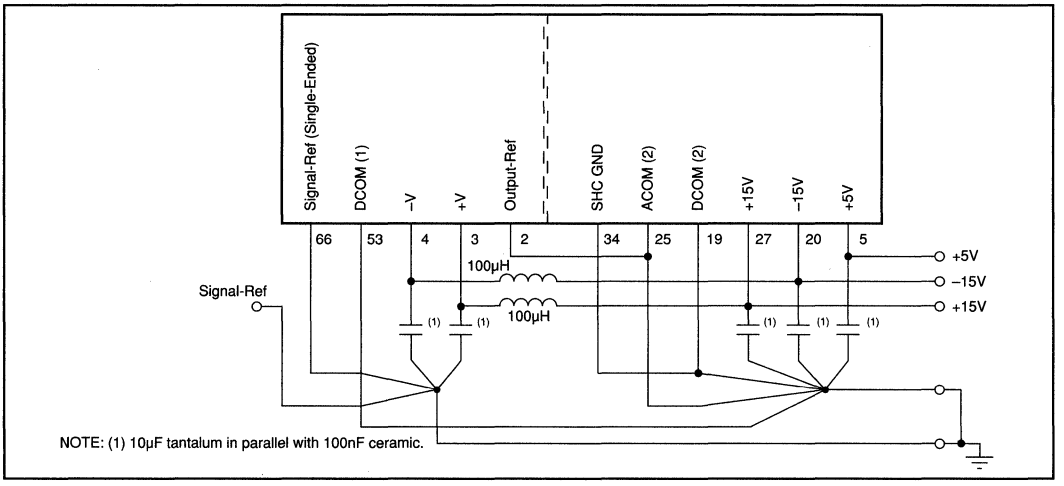


FIGURE 15. Recommended Decoupling of Power Supplies.

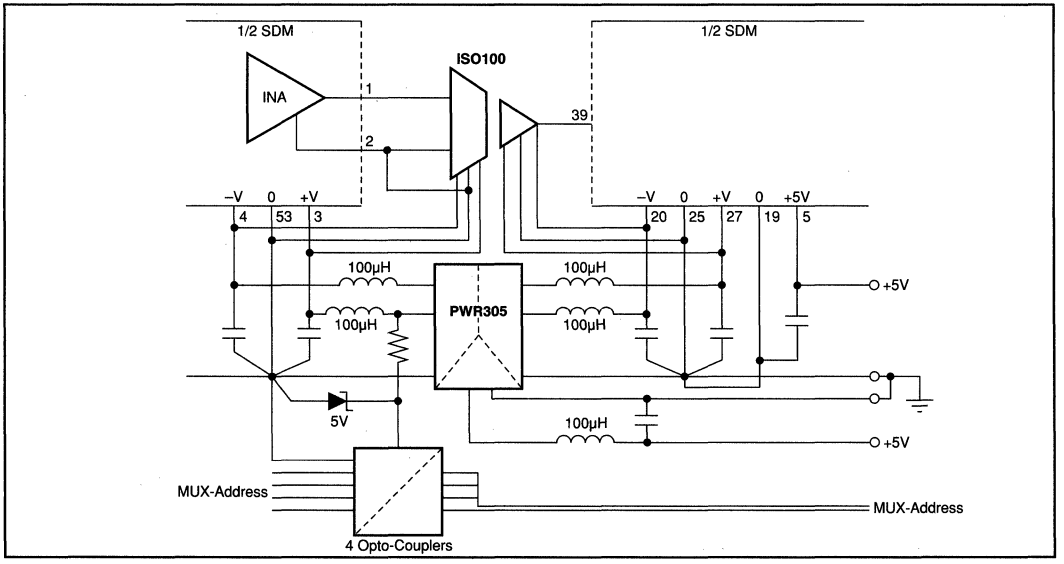


FIGURE 16. Galvanic Isolation Between Analog and Digital Signals.

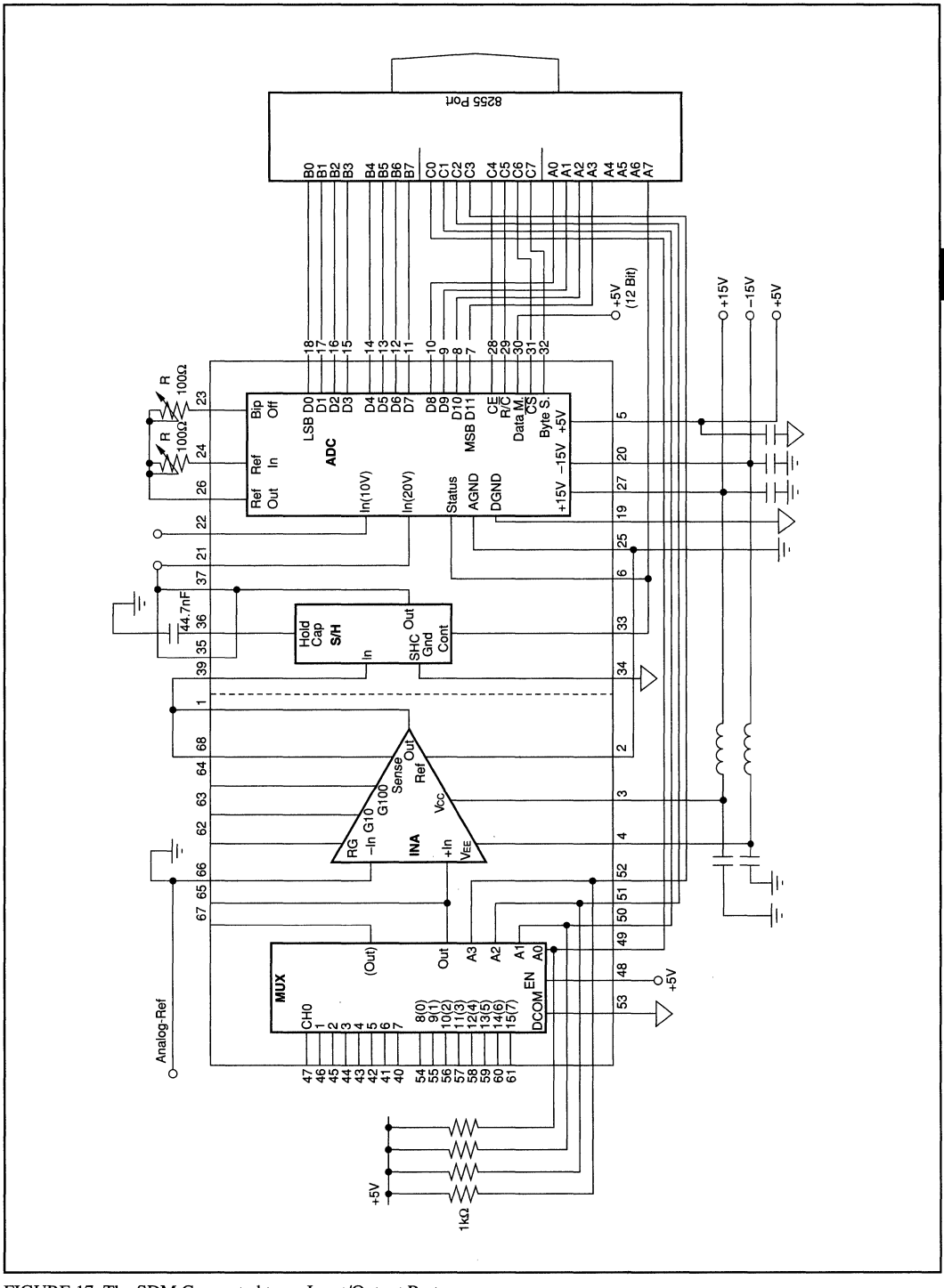


FIGURE 17. The SDM Connected to an Input/Output Port.

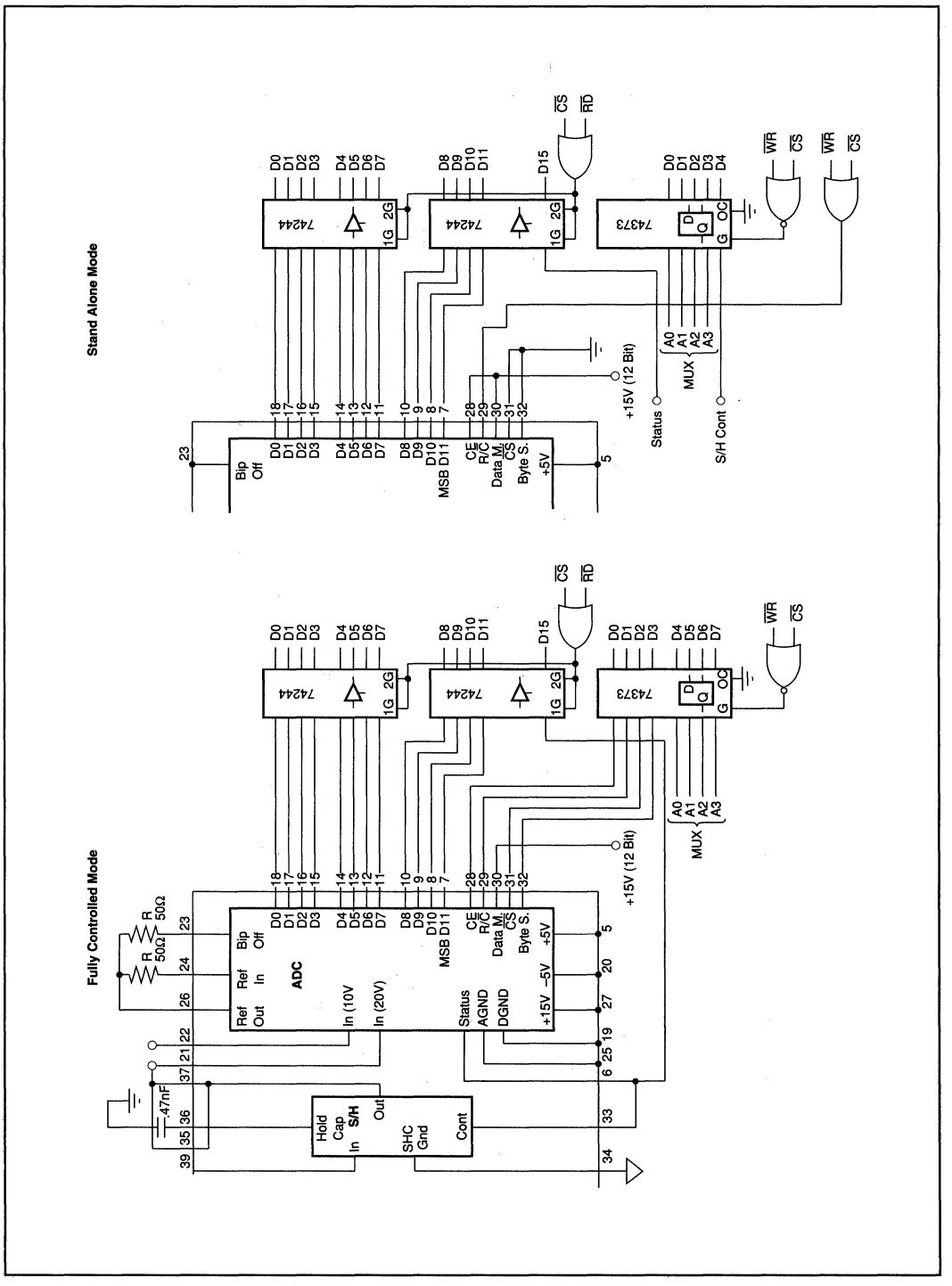


FIGURE 18. The SDM Connected to a 16-Bit-BUS.

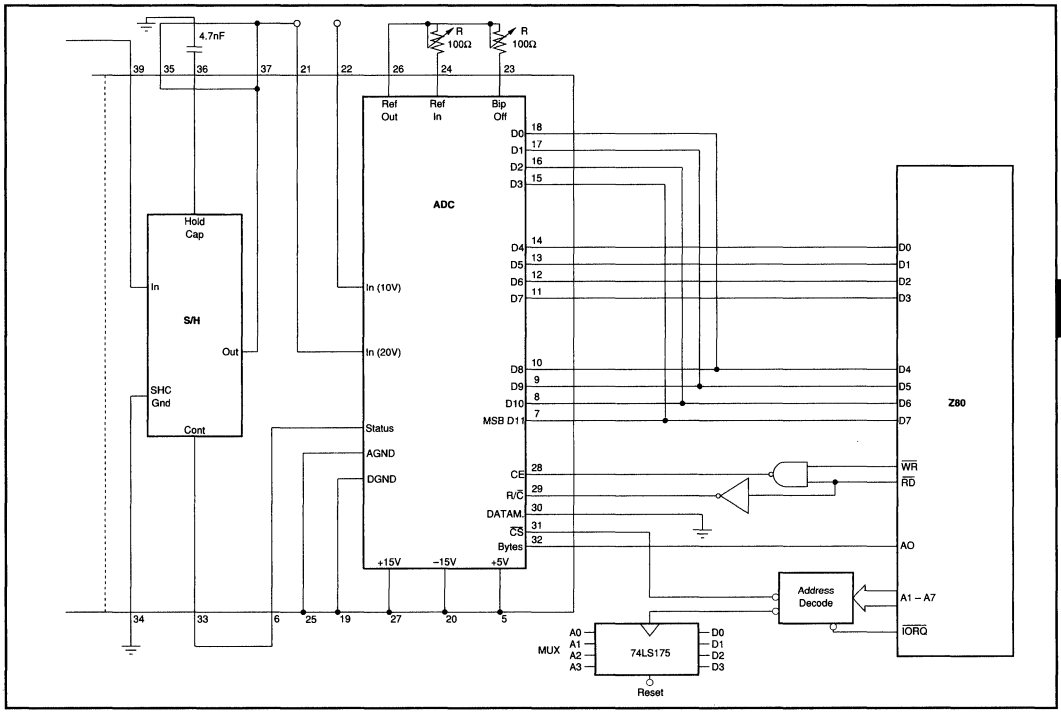


FIGURE 19a. SDM on the Z80 Interface.

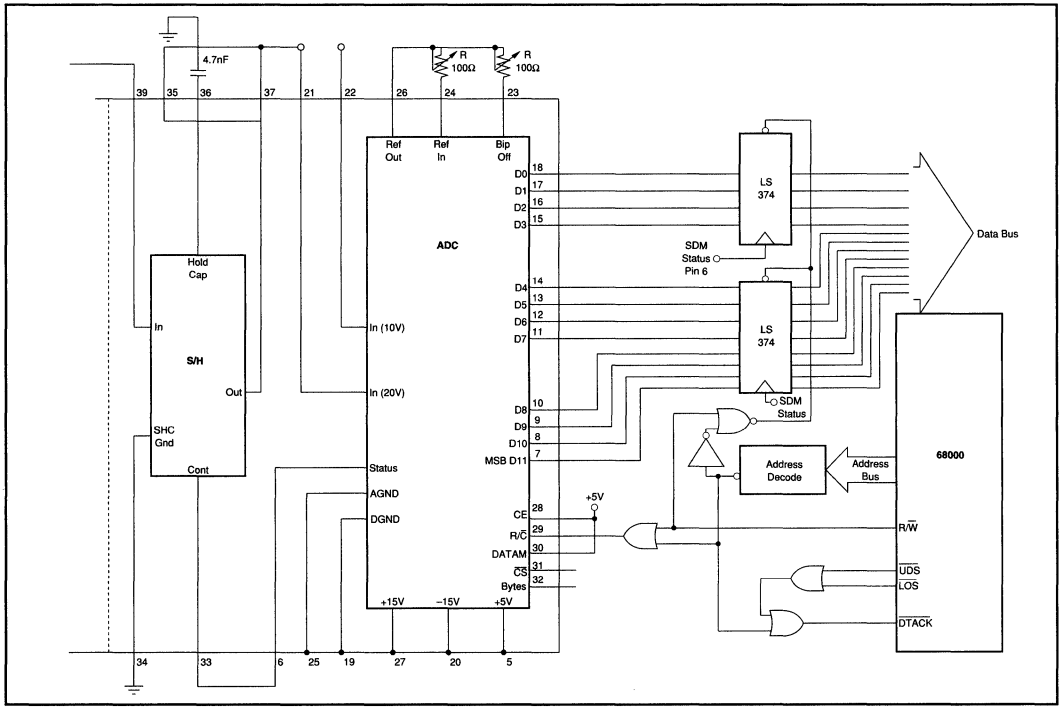


FIGURE 19b. 68000/SDM Interface.

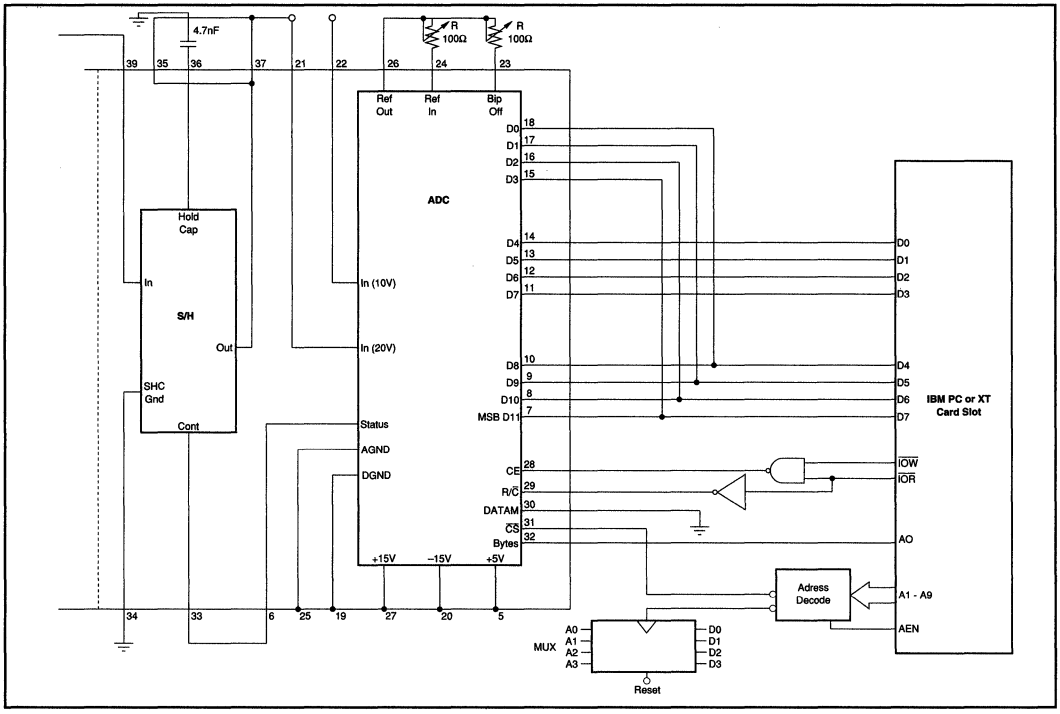


FIGURE 19c. IBM PC SDM Interface.

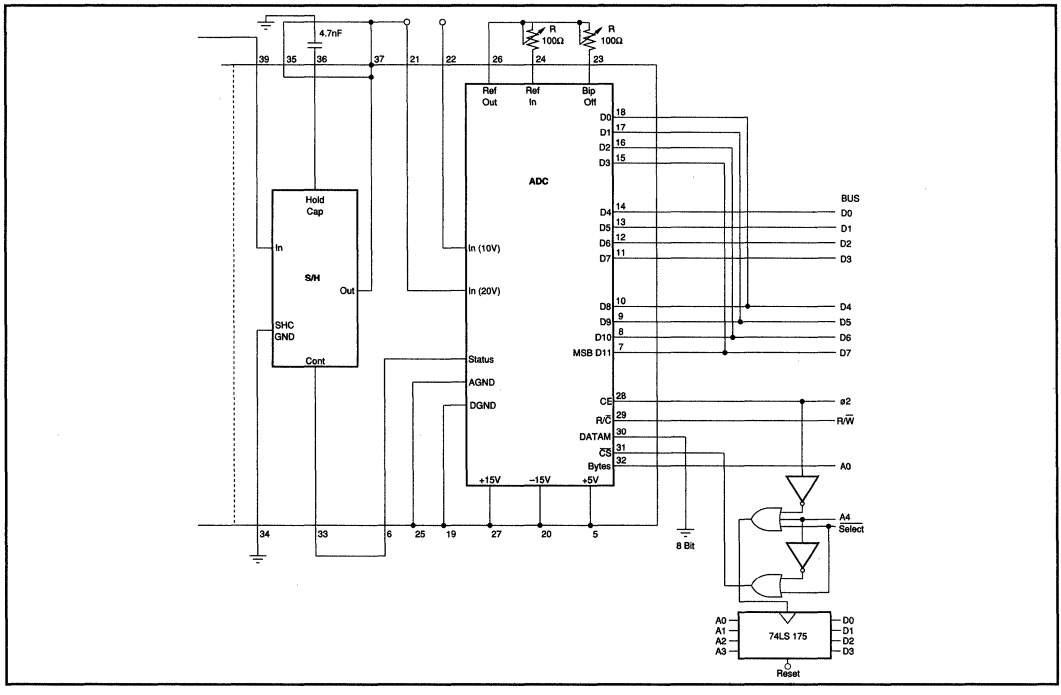


FIGURE 20. SDM on the 6502 BUS.

CONTROLLING THE SDM

The Burr-Brown SDM family can be easily interfaced to most microprocessor systems, as shown in Figures 17-20. The microprocessor may control each conversion, or the converter may operate in a stand-alone mode controlled only by the R/$\overline{C}$ input.

STAND-ALONE OPERATION

The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and BYTE SELECT are connected to LOW and CE and DATA MODE are connected to HIGH. The output data are presented as 12-bit words.

Conversion is initiated by a High-to-Low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In each case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 21 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 22 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table I lists timing specifications for stand-alone operation.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS} 86X	STS Delay After Data Valid	300	500	1000	ns
t_{HS} 87X		100	300	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE I. Stand-Alone Mode Timing.

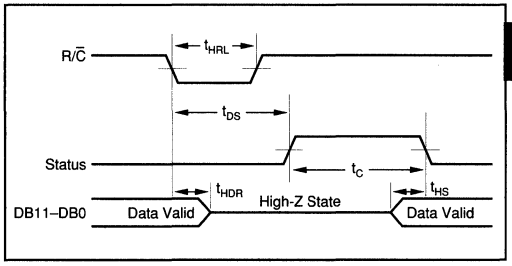


FIGURE 21. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

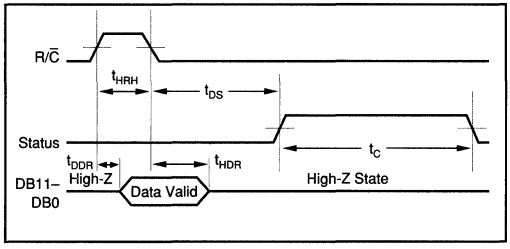


FIGURE 22. R/$\overline{C}$ Pulse High—Outputs Enabled Only Where R/$\overline{C}$ is High.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the BYTE SELECT input, which is latched upon receipt of a conversion start transition. BYTE SELECT is latched because it is also involved in enabling the output buffers. No other control inputs are latched. If BYTE SELECT is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if BYTE SELECT is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1).

Conversion Start

A conversion is initiated by a transition on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$)—refer to Figure 9. The last of the three to reach the required state start the conversion and thus all three may be dynamically controlled. If necessary, they may change state simultaneously, and the nominal delay time is independent of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Conversion Cycle Timing of the Digital Specifications.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SDM	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 23. 12-Bit Data Format for 8-Bit Systems (connected as Figures 18 and 19).

The STATUS output indicates the state of the converter by being high only during a conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore, data is not valid. During this period additional transitions of the three control inputs will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if BYTE SELECT changes state after the beginning of conversion, any additional start conversion transition will latch the new state of BYTE SELECT, possibly resulting in an incorrect conversion length (8 bit versus 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four conditions are met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. In this condition the data lines are enabled according to the state of the inputs DATA MODE and BYTE SELECT. See Read Cycle Timing for timing relationships and specification.

In most applications the DATA MODE input will be hardwired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When DATA MODE is high, all 12 outputs lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus and the state of the BYTE SELECT is ignored.

When DATA MODE is low, the data is presented in the form of two 8-bit bytes, with selection of each byte by the state of BYTE SELECT during the read cycle.

The BYTE SELECT input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When BYTE SELECT is low, the byte addressed contains the 8MSBs. When BYTE SELECT is high, the byte addressed contains the 4LSBs from the conversion followed by four zeros that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 23. The design of the SDM guarantees that the BYTE SELECT input may be toggled at any time without damage to the output buffers occurring.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the status output has gone low. In those situations requiring the fastest possible access to the data, the read may be started as much as (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Read Cycle Timing for these timing relationships.

APPLICATIONS INFORMATION

ASSEMBLY OF SURFACE MOUNT PACKAGES

There are several assembly methods for the LCC versions of the SDM8XX. The associated advantages and disadvantages of three methods are outlined below.

1. DIRECT SURFACE MOUNT ONTO PCB

ADVANTAGES	DISADVANTAGES
Ease of assembly Low cost Low weight Small footprint size	Difficult to inspect solder joints Difficult to clean Choice of board material important in wide temperature range applications

In wide temperature applications it is important to match the coefficients of thermal expansion of the board and the SDM8XXL. Below is a list of materials and their approximate coefficients of linear thermal expansion.

MATERIAL	(ppm/°C)
Alumina (96%) - SDM Package	6-7
Copper-clad-Invar (50% Cu)	9
(30% Cu)	6
(10% Cu)	3
Epoxy-Kevlar (60% Kevlar)	6
Polyimide-Kevlar (40% Kevlar)	6
Beryllia	5
Polyimide-glass (x-axis)	12
(y-axis)	14

Kevlar™ E.I. du Pont de Nemours & Co.

2. ATTACHMENT OF SURFACE MOUNT EDGE CLIPS

ADVANTAGES	DISADVANTAGES
Ease of Inspection Easy cleaning Thermal expansion taken up by the flexing of the edge clips	Extra cost Extra assembly

ASSEMBLY

The edge clips are attached to the edges of the SDM8XXL as in Figure 24 before the device is mounted on to the board.

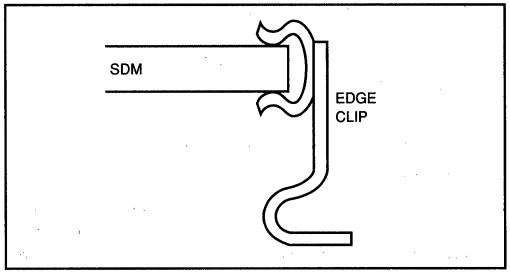


FIGURE 24. Edge Clip Assembly.

SUPPLIERS OF EDGE CLIPS

USA	USA
DIE-TECH INC., R.D. 1, Sipe Road, York Haven, PA 17370 USA PHONE: (717) 938-6771	NAS Electronics, 381 Park St., Hackensack, NJ 07602 USA PHONE: (201) 343-3156
EUROPE	**EUROPE**
SEMI-DICE (UK) Ltd, Buckingham House, Mineral Lane, Chesham, Bucks. HP5 2AU UK PHONE: 0494 771275	NASBRIT Ltd, Wester Goudi Ind. Est. Dundee DD2 4UX UK PHONE: 0382 622222

3. SURFACE MOUNT SOCKET

ADVANTAGES	DISADVANTAGES
Board thermal expansion not so critical Ease of component replacement	Cost Extra height (if critical)

Below is the name and address of a supplier of a 68-pin surface mountable socket.

The part number is: Socket 212-068-012
Spring cover CCS-004

USA	EUROPE
Methode Electronics INC, Interconnect Products Div. 1700 Hick Road, Rolling Meadows, TX 75050 USA PHONE: (312) 392-3500	Lucas Methode Connectors Ltd, Halifax Road Ingrow Bridge, Keighley, Yorkshire BD21 5HR UK PHONE: 0535 603282

General Comments

The advantages and disadvantages of all the methods mentioned above are for general use of surface mount components. Every user will find that the importance of these factors will depend on his application and situation.

EVALUATION BOARD

For the engineer who wishes to evaluate the SDM family, Burr-Brown has designed printed circuit boards on a single 'Eurocard' (shown here for LCC only). These boards enable the design engineer to experiment with various accuracy improvement techniques which are described below. Special consideration has been given to the grounding and circuit layout techniques required when dealing with 12-bit analog signals.

The printed circuit board has been designed so that the solutions to several of the problems likely to be encountered by the user can be examined.

It should not be thought that every user is required to adopt all of the techniques used on the circuit board. In many applications very few external components will be required. However, in following the application guidelines illustrated by the circuitry and accompanying notes, the designer will be able to select and adapt the solutions most suited to their won particular application or problem area.

Provisions for the following are made on the LCC PC board:

—68 pin LCC socket (Burr-Brown Part No. MC0068).
—8 differential or 16 single-ended inputs.
—Input filtering with overvoltage protection for each channel.
—Socket for quad D-type flip-flop 74175 (MUX address latches).
—7 additional I.C. sockets for easy interfacing to various BUS systems (connection by wire wrap techniques).
—2 voltage regulators (15V).
—LC power supply decoupling.

The layout pays particular attention to the requirements when operating with precision analog signals. This requires strict separation of the analog and digital areas. Analog and digital commons are totally separated and connected together only at the commons of the supply voltage. All common lines are low resistance and low inductance.

SUPPLY VOLTAGES

In order to avoid coupling between the external supply voltage 15V supplies, 2 voltage regulators (78M15, 79L15) are provided on the PC board. The unregulated supply voltage may vary from ±17V to ±25V.

The MUX/INA section and SHC/ADC section of the SDM have separate supply lines which can be inductively decoupled. This is recommended in order to suppress the high frequency noise which comes from the ADC during conversion.

The power supply rejection of the instrumentation amplifier reduces with increasing frequency. If high frequency noise on the supplies is not decoupled it will be injected into the signal path and cause errors. This effect can be particularly pronounced when using the 'overlap' mode since the instru-

SDM862/872						SDM863/873				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8			–		
H	L	L	H	H	9			–		
H	L	H	L	H	10			–		
H	L	H	H	H	11			–		
H	H	L	L	H	12			–		
H	H	L	H	H	13			–		
H	H	H	L	H	14			–		
H	H	H	H	H	15			–		

FIGURE 25. Channel Select Truth Table.

mentation amplifier is settling to a new analog value while the ADC is still carrying out the previous conversion.

The digital supply voltage is +5V and is also LC-filtered.

All supply lines are bypassed with a 10µF tantalum and a 100nF ceramic capacitor situated **as close as possible** to the package.

If the voltage regulators for the ±15V are not used, small inductors for decoupling of the supply voltages are recommended. If inductors are not fitted a dynamic ground loop will be created from supply lines via bypass capacitors to analog common.

INPUT PROTECTION

The multiplexer is protected up to an input voltage which can exceed the supply voltage by a maximum of 20V. This means, that with ±15V supply voltage, the input voltage can be ±35V without damage. This is also the case when the supply voltages are switched off (0V). The maximum input voltage can then be ±20V. For higher overvoltage protection a series resistor has to be used. The current via the multiplexer should be limited to 20mA absolute maximum, 1mA is preferred. For example, a 10kΩ series resistor would give an additional 10V overprotection.

For much higher overvoltages (e.g. 100V), high value series resistors cannot be used as offset errors would result. In practice, a combination of series resistors and diodes is used. The diodes are connected to ±15V and will conduct whenever the input voltage exceeds the ±15V supply voltage. The diodes are selected by signal source impedance, as well as filter resistance, as the diode leakage current across the series resistor can cause offset and linearity errors. In this circuit, IN4148 together with 10kΩ are used.

INPUT FILTER

Processor noise can be induced in the analog ground. Input filtering is therefore recommended for analog data acquisition. Such high frequency noise signals can cause dynamic overload of the instrumentation amplifier resulting in nonlinear behavior. This leads directly to digitizing errors.

The design of the filter takes into account the characteristics of the SDM and of the signal source.

The following points have to be considered:

—The stray capacitance, output capacitance of the multiplexer and input capacitance of the instrument amplifier (up to 80pf in some cases) has to be discharged in order to minimize errors caused by 'charge sharing.'

—The series resistor limits the current in the protection diodes, but it also has to be selected for the required filter time constant.

—The noise rejection of the filter has to be >80db in order to satisfy a 12-bit A/D conversion.

As well as considering the above, different calculations have to be carried out for single and differential input signals.

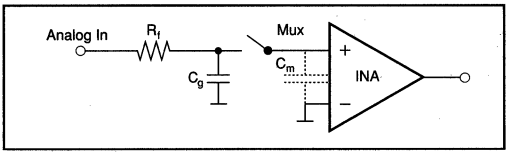


FIGURE 26.

Single-Ended Measurement

R_f limits the maximum input current through the protection diodes. In this case, R_f has been chosen as 10kΩ and together with the capacitor C_g, forms the input filter time constant (C_g = 0.47µF). The time constant must be chosen according to the requirements of the input signal bandwidth and noise rejection. The multiplexer capacitance (C_m) is discharged mainly by C_g. This means C_g has to be sufficiently large compared with C_m or charged via R_f prior to resampling of the signal.

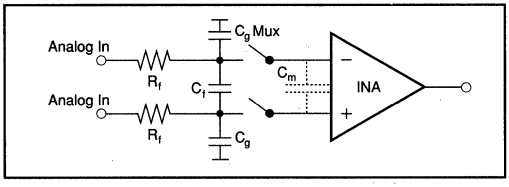


FIGURE 27.

Differential Measurement

Capacitor C_f, is used for limiting the input signal frequency. The bandwidth is calculated as follows:

$$F_f = \frac{1}{4\pi R_f C_f} \quad \text{IF } C_f >> C_g$$

When selecting the value of C_f, it should be noted that C_m has to be discharged when switching the multiplexer channels. This means that the voltage error of C_f (induced by 'charge sharing' with C_m) has to be smaller than 1LSB. Therefore, C_f should have a minimum value of a 0.47µF. The resistors R_f, together with the source impedance, have to be sufficiently small in order to recharge C_f prior to signal sampling. This prevents errors in the signal value caused by the charge stored on C_m by the previously selected channel.

The 2 capacitors C_g form together with R_f a common-mode filter. This filter greatly improves accuracy in a noisy environment (decrease of common-mode rejection of instrumentation amplifier with increasing frequency).

For good common-mode filter operation, both time constants R_f and C_g should match each other within 2%. Additional errors will be induced by a mismatch.

Selected values are: C_f = 0.47µF, C_g = 10nF, R_f = 10kΩ. The filter reduces the signal slew rate so that the instrumentation amplifier can follow the voltage variation of the signal with the noise component eliminated.

In general, all measurements which require more than a gain of 10 should be done in differential mode. Single ended

measurements should be limited to applications where current sources are measured via shunts or where signal voltages in the range of some volts are available.

Bus-Interface

As the outputs of the SDM are BUS compatible, only a few ICs are necessary to interface to various BUS systems. For such interfacing, 20-pin IC sockets are provided. Wiring is by wire wrap to the BUS connector.

Setting of Various Modes

Circuit Board positions are provided for the connection of 'jumpers' as follows:

J1, J2—ADC analog input volt age settings.
J3—Set for differential (SDM8X3) or single ended (SMD8X2) operation.
J4—Instrumentation amplifier gain settings.

(a) 16 input channels, single ended:
—Use SDM8X2
—Consider single-ended filtering
—Connect J3 (pin 66) to common

(b) Differential inputs
—Use SDM8X3
—Consider differential filtering
—Connect J3 (pin 67) to pin 67

(c) Analog input

±10V	Connect J1 to pin 21
	Connect J2 to pot P2 (100Ω)
±5V	Connect J1 to pin 22
	Connect J2 to pot P2 (100Ω)
0 to +10V:	Connect J1 to pin 22
	Connect J2 to junction of R_1/R_2

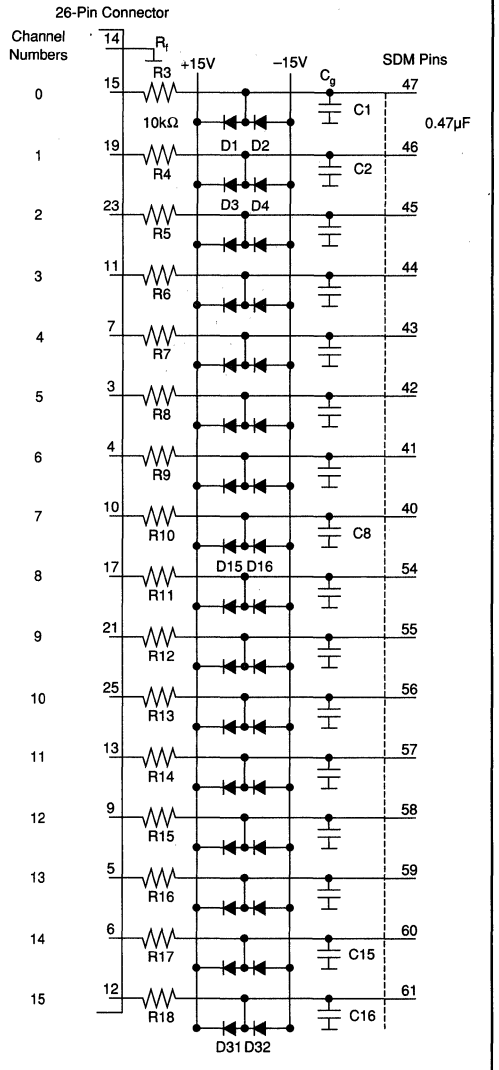
(d) Gain of instrumentation amplifier

G = 1	Jumper J4 open
G = 10	Jumper J4 to pin 63
G = 100	Jumper J4 to pin 64

Other gains: use additional resistor between pin 62 and pin 63 (see section on Instrumentation Amplifier) as low tempco resistor is recommended in order to minimize gain drift.

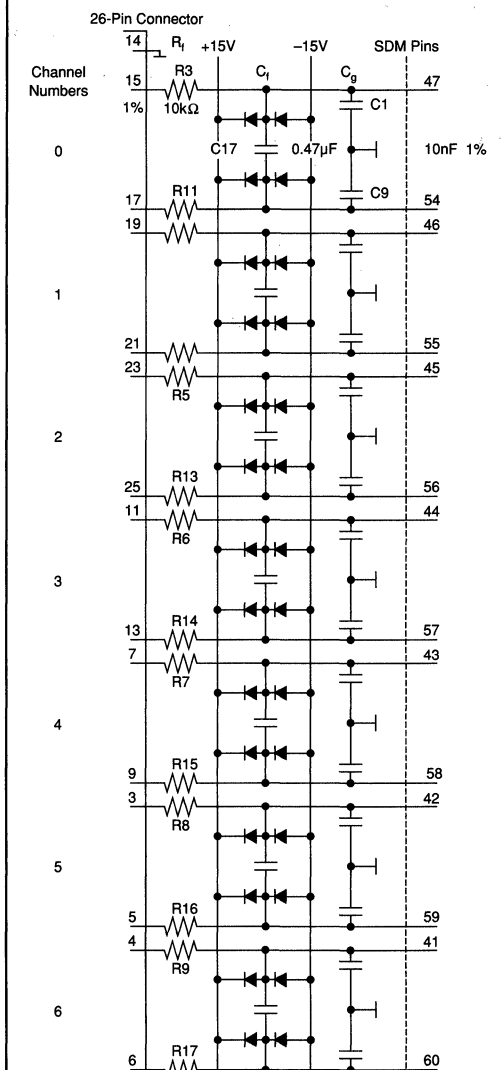
INPUT FILTER AND PROTECTION CIRCUITRY

SINGLE-ENDED



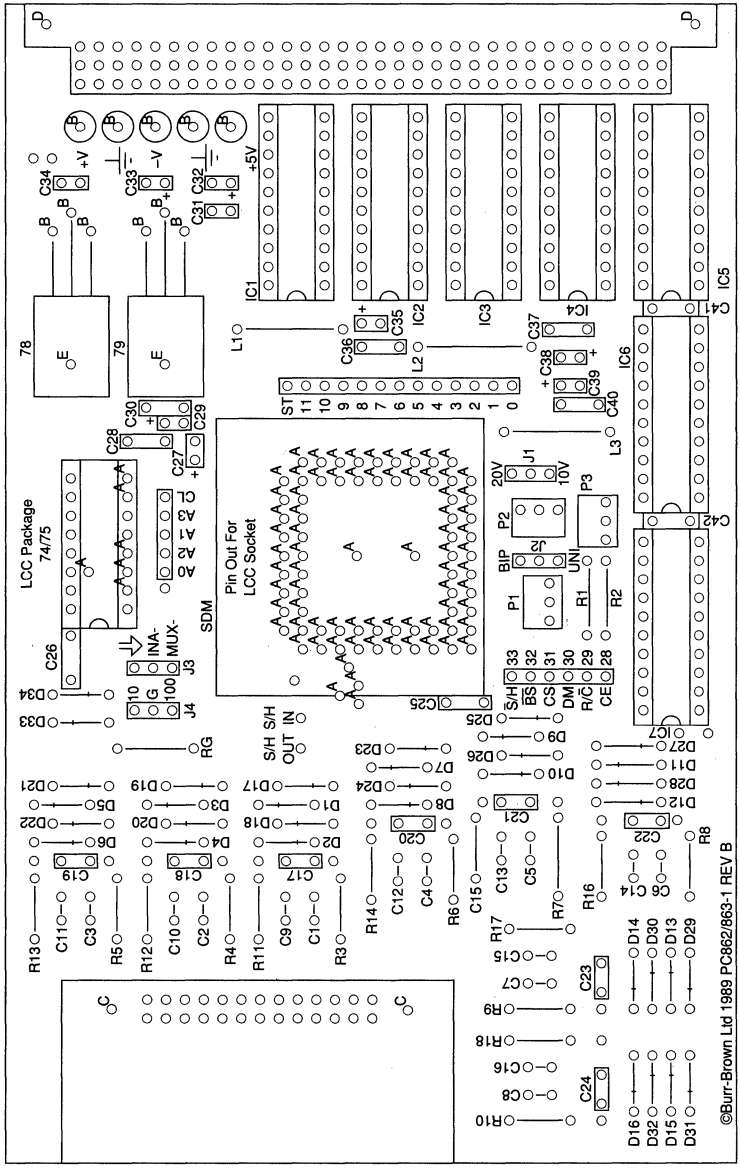
Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

DIFFERENTIAL



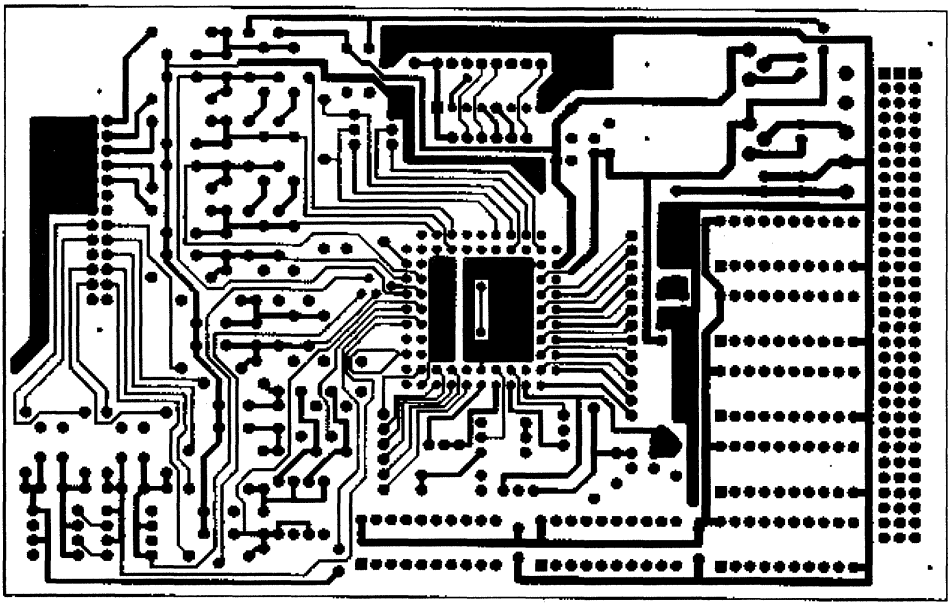
Pins 1, 2, 8, 14, 16, 18, 20, 22, 24 and 26 are Connected to Common

PCB COMPONENT LAYOUT

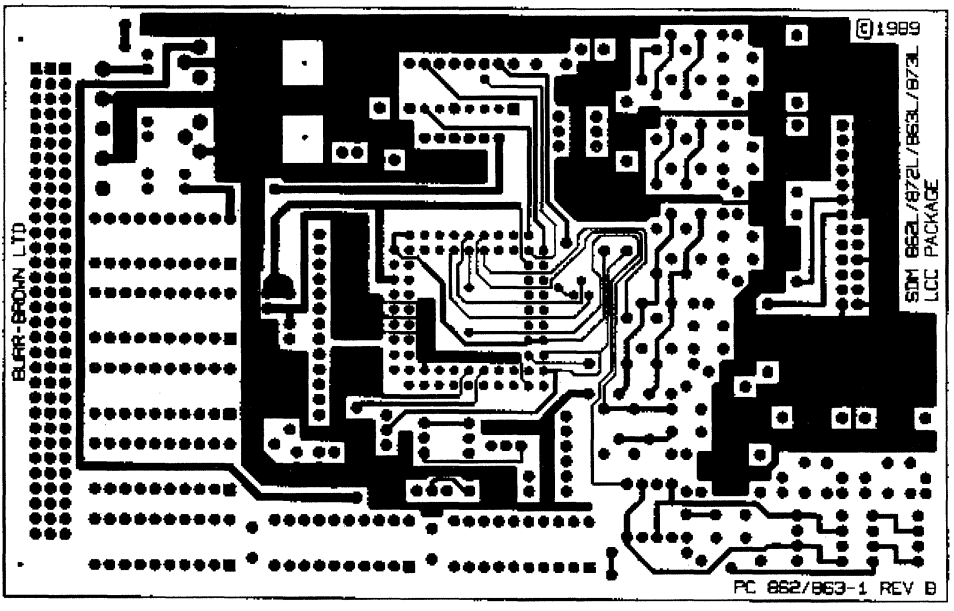


NOTE: (1) NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2
(2) NOT DRAWN TO SCALE

P.C.B. LAYOUT

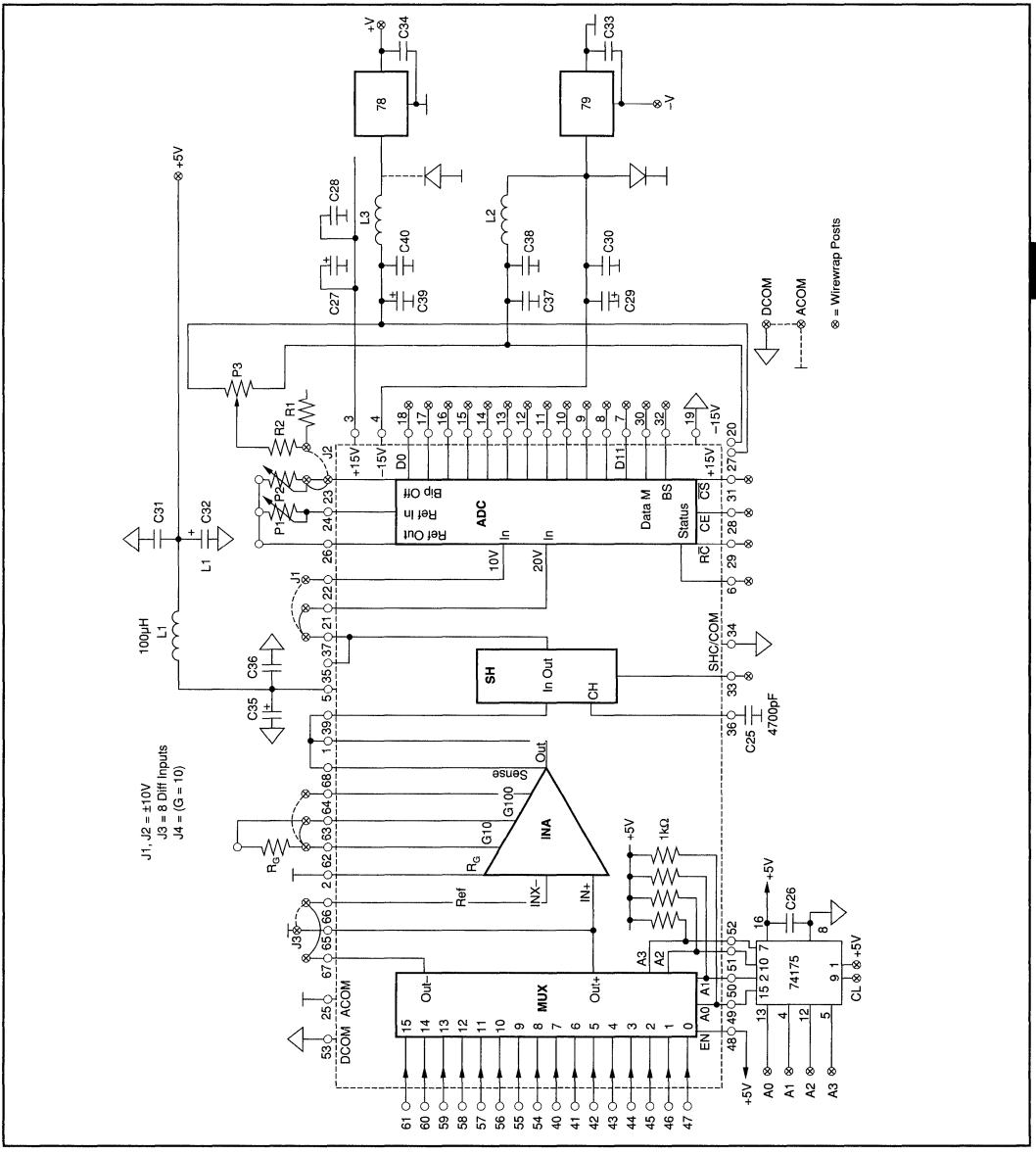


NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2



NOTE: NOT SUITABLE FOR PGA PACKAGE SEE PC862/863-2

CIRCUIT DIAGRAM—SDM PC BOARD



P.C.B. COMPONENTS PARTS LIST

R1	100Ω	C26	10nF Ceramic	P3	100kΩ **0–10V Range Only**
R2	100kΩ — For 0–10V Settling	C27, C29, C35	10µF Tantalum (Decoupling)	L1...L3	100µH (Decoupling)
R3...R18	10kΩ 1%	C32, C38, C39		D1...D32	1N4148 (Input Protection Diodes)
C1...C16	0.47µF—Single Ended Input Mode	C28, C30, C31	100nF Ceramic (Decoupling)	D33, D34	1N4007
	10nF 1%—Differential Input Mode	C36, C37, C40		78	MC78M15CG
C17...C24	0.47µF—Differential Input Mode	C33, C34	0.33µF Tantalum	79	MC79L15CG
C25	4.700pF (Polypropylene, Polystyrene or Teflon™)	P1	100Ω	**74175**	74LS175
		P2	100Ω **±5V, ±10V Range Only**	LCC Socket	MC0068

UNLESS OTHERWISE MARKED—RESISTORS ARE 1/4W, 5%, CAPACITORS ARE 10%

Teflon™ E.I. du Pont de Nemours & Co.

3 Digital-to-Analog Converters

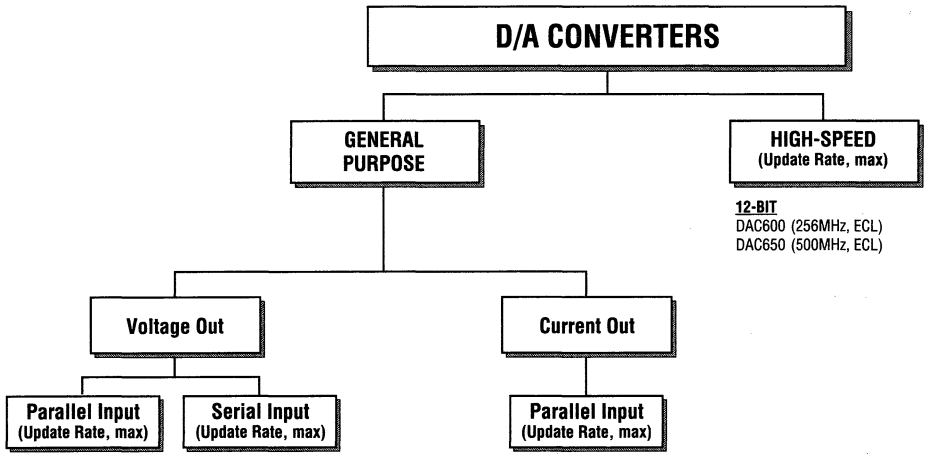
Burr-Brown offers a wide range of Digital-to-Analog (D/A) converters designed to meet critical requirements for industrial, audio and waveform-generation applications.

Industrial instrumentation D/As with 12-, 16-, and 18-bit resolutions are available in industry standard pinouts. There are also new smaller size, lower-power D/As specified over the extended industrial temperature range, –40°C to +85°C. Dual and Quad D/As are also available in the product line.

DAC714 is a new 16-bit monolithic D/A converter with internal reference and programmable output. Operating with ±12V supplies, **DAC714** is capable of supporting 10MHz input data rates and serial data output for cascaded serial bus connections. It is available in 16-pin plastic 0.3" DIP and 16-lead wide-body plastic SOIC packages.

DAC715 is a new monolithic 16-bit D/A converter with a high-speed 16-bit parallel double-buffered bus interface. It is ideal for industrial process control, robotics, and motion controllers.

DAC716 is a complete monolithic D/A converter that includes a +10V temperature compensated voltage reference, current-to-voltage amplifier, high-speed synchronous serial interface, a serial output which allows cascading multiple converters, and an asynchronous clear function which immediately sets the output voltage to zero.



* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Product	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range	Description
DAC56	16	±0.012	1.5*	±3V	Serial Input, Flexible Bus Interface
DAC80	12	±0.012	0.3, 3*	±1mA, –2mA; +5V, +10V, ±5V, ±10V	Industry Standard, General Purpose, Flexible Bus Interface
DAC667	12	±0.006	4	±2.5V, ±5V, ±10V, +5V, +10V	Industry Standard Pinout, Flexible Bus Interface
DAC700	16	±0.0015	1	–2mA	General Purpose
DAC701	16	±0.0015	8	+10V	General Purpose
DAC702	16	±0.0015	1	±1mA	General Purpose
DAC703	16	±0.0015	8	±10V	General Purpose
DAC707	16	±0.003	8	±10V	16-Bit Parallel, Bus Interface
DAC708	16	±0.003	1	±1mA, –2mA	Serial/8-bit Parallel, Bus Interface
DAC709	16	±0.003	8	±5V, ±10V, +10V	Serial/8-bit Parallel, Bus Interface
DAC712	16	±0.003	12	±10V	16-Bit Parallel, Bus Interface
DAC714	16	±0.003	10	±10V	Serial Interface, Bus Interface
DAC715	**16**	**±0.003**	**10**	**0 to 10V**	**Parallel, Double Buffered**
DAC716	***16***	***±0.003***	***10***	***0 to 10V***	***Serial, Low Noise Reference***
DAC729	18	±0.00075	5	±1mA, –2mA; +5V, +10V, ±5V, ±10V	Very High Resolution
DAC725	16	±0.003	8	±10V	Dual, Serial/8-bit Parallel, Bus Interface
DAC811	12	±0.006	4	±5V, ±10V, +10V	Flexible Bus Interface
DAC813	12	±0.006	4	±5V, ±10V, +10V	Small, Low Cost, Flexible Bus Interface
DAC1600	16	±0.003	8*	±10V	Lowest Cost
DAC2813	12	±0.006	6	±10, 0 to 10	Dual, 12-bit Port, Flexible Bus Interface
DAC2814	12	±0.012	10	$+V_S$ –1.4V (max), $-V_S$ +1.4V (min)	Dual, Multiplying Serial Port, Flexible Bus Interface
DAC2815	12	±0.012	10	$+V_S$ –1.4V (max), $-V_S$ +1.4V (min)	Dual Multiplying 8-bit Port, Flexible Bus Interface
DAC4813	12	±0.012	6	±10V	QUAD, 12-bit Port, Flexible Bus Interface
DAC4814	12	±0.012	10	$+V_S$ –1.4V (max), $-V_S$ +1.4V (min)	QUAD, Multiplying Serial Port, Flexible Bus Interface
DAC4815	12	±0.012	10	$+V_S$ –1.4V (max), $-V_S$ +1.4V (min)	QUAD, Multiplying 8-bit Port, Flexible Bus Interface
DAC7528	8	±0.012	0.18	0 to 1mA	Dual Multiplying DAC, Flexible Bus Interface
DAC7541A	12	±0.012	1	0 to 1mA	Industry Standard, Bus Interface
DAC7545	12	±0.012	2	0 to 1mA	Industry Standard w/Latch, Bus Interface
DAC7800	12	±0.012	0.8	0 to 1mA	Octal, Serial Interface, with Bus Interface
DAC7801	12	±0.012	0.8	0 to 1mA	8-bit Port Interface, with Bus Interface
DAC7802	12	±0.012	0.8	0 to 1mA	12-bit Port Interface, with Bus Interface
DAC8043	12	±0.012	0.25*	0 to 1mA	Single w/Bus, with Bus Interface

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

DIGITAL SIGNAL PROCESSING

Product	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Comments
DSP201	18	±0.006	NS	±3	DSP-Compatible Digital Interface, Single
DSP202	18	±0.006	NS	±3	DSP-Compatible Digital Interface, Dual

HIGH SPEED

Product	Resolution (Bits)	Max Update Rate	SFDR, f_O = 1MHz (V_{OUT} = FS)	Output Range	Input Format	Power Supply (V)	Package	Max Power Dissipation (mW)
DAC600	12	256MHz	–74dB SFDR	–1V, –20mA	Parallel	–5.2	68 PLCC	1.3W
DAC650	12	500MHz	–70dB SFDR	±1V, ±20mA	Parallel	±15, ±5	68 LEAD	2.0W

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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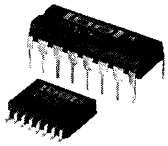


DAC56

Monolithic 16-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  Internal Voltage Reference
  ±3V Output Operational Amplifier
  Pinout Allows I_{OUT} (±1.0mA) Option
  No external components required
- 0.012% LINEARITY ERROR MAX
- 12-BIT MONOTONICITY GUARANTEED OVER 0°C TO +70°C
- ±5V TO ±12V POWER SUPPLY
- SETTLING TIME: V_{OUT} = 1.5µs; I_{OUT} = 350ns
- SERIAL DATA INPUT: Binary Two's Complement
- 16-PIN PLASTIC DIP AND SOIC

APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS LEVEL SETTING
- CLOSED-LOOP SERVO-CONTROL
- AUTO-CALIBRATION CIRCUIT FOR A/D BOARDS
- UP-GRADE REPLACEMENT FOR MULTIPLYING D/A
- X-Y PLOTTER
- DSP PROCESSOR BOARDS

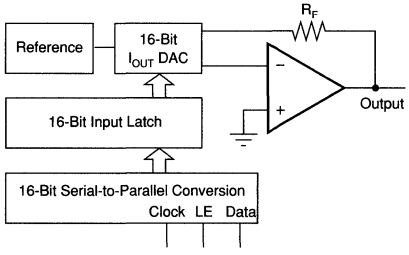
DESCRIPTION

The DAC56 is a complete 16-bit monolithic D/A converter. Completely self-contained with a stable, low noise, internal zener voltage reference; high-speed current switches; a resistor ladder network; and a low noise output operational amplifier all on a single monolithic chip. The DAC56 operates over a wide power supply range from ±5V to ±12V.

Differential linearity error (DLE) is guaranteed to meet specifications without external adjustment. However, provisions for an externally adjustable circuit controlling the MSB error, the differential linearity error at bipolar zero, makes the DLE at BPZ essentially zero and provides for high system performance. The I/V amplifier stage includes an output current limiting circuit to protect both amplifier and load from excessive current. This assures the user of high system reliability.

A high-speed interface is capable of clocking in data at a rate of 10MHz max, and its interface logic contains a serial data clock (input), serial data (input) and latch-enable (input). Serial data is clocked MSB first into a 16-bit register and then latched into a 16-bit parallel register.

The DAC56 is packaged in a 16-pin plastic DIP and 16-pin SOIC.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

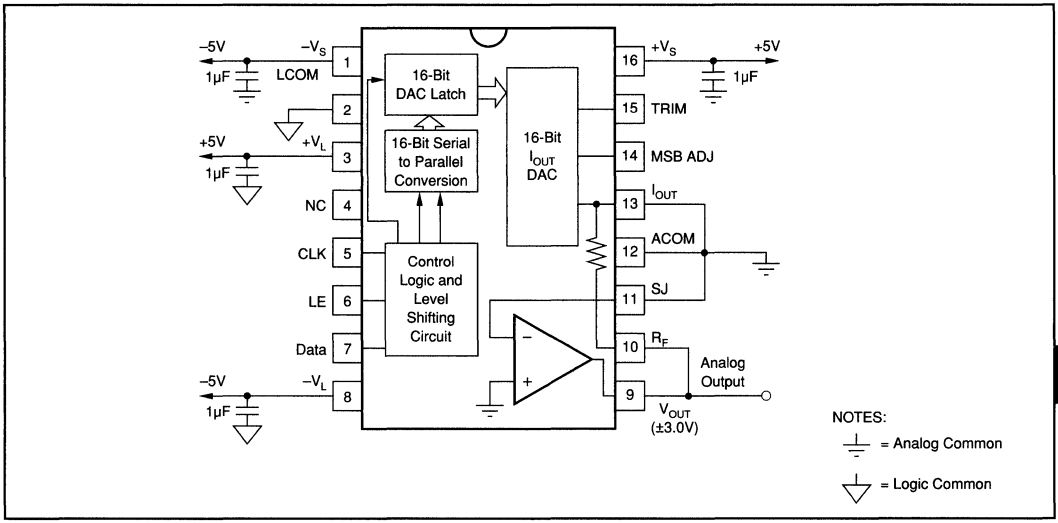
ELECTRICAL

All specifications at +25°C, and power supply voltage of ±5V unless otherwise noted.

PARAMETER	CONDITIONS	DAC56 MIN	DAC56 TYP	DAC56 MAX	UNITS
DIGITAL INPUT					
Resolution			16		Bits
Digital Input Level: (1) V_{IH}		+2.4		$+V_L$	V
V_{IL}		0		+0.8	V
$I_{IH} \cdot V_I = +2.7V$				+1	µA
$I_{IL} \cdot V_I = +0.4V$				–50	µA
Input Clock Frequency		10			MHz
ACCURACY					
Integral Linearity Error				±0.012	% of FSR(3)
Differential Linearity Error				±0.024	% of FSR
Gain Error				±1.5	% of FSR
Bipolar Zero Error				±0.5	% of FSR
Monotonicity	0°C to +70°C			12	Bits
TEMPERATURE DRIFT	0°C to +70°C				
Gain Drift			±60		ppm of FSR/°C
Bipolar Zero Drift			±20		ppm of FSR/°C
Linearity Drift				±0.012	% of FSR
Differential Linearity Drift				±0.024	% of FSR
POWER SUPPLY SENSITIVITY	$\pm V_S = \pm V_L = \pm 5VDC$				
Gain			±0.0045		% of FSR/%V
Bipolar Zero			±0.0015		% of FSR/%V
SETTLING TIME	to ±0.006% of FSR				
Voltage Output					
6V Step			1.5		µs
1LSB			1		µs
Current Output					
1mA Step	10 to 100Ω Load		350		ns
	1kΩ Load(3)		350		ns
Slew Rate			12		V/µs
ANALOG OUTPUT					
Voltage Output Configuration					
Bipolar Range		±2.66	±3.0	±3.34	V
Output Current		±8			mA
Output Impedance			0.1		Ω
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Range			±1		mA
Output Impedance			1.2		kΩ
WARMUP TIME		1			min
POWER SUPPLY REQUIREMENTS(4)					
Supply Voltage					
$+V_S$ and $+V_L$		+4.75	+5.00	+13.2	V
$-V_S$ and $-V_L$		–4.75	–5.00	–13.2	V
Supply Drain (No Load)					
+V ($+V_S$ and $+V_L = +5V$)			+10	+17	mA
–V ($-V_S$ and $-V_L = -5V$)			–25	–35	mA
+V ($+V_S$ and $+V_L = +12V$)			+12		mA
–V ($-V_S$ and $-V_L = -12V$)			–27		mA
Power Dissipation					
V_S and $V_L = \pm 5V$			175	260	mW
V_S and $V_L = \pm 12V$			468		mW
TEMPERATURE RANGE					
Specification		0		70	°C
Storage		–60		100	°C

NOTES: (1) Logic input levels are TTL-/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for DAC56 in the V_{OUT} mode. (3) Measured with an active clamp to provide a low impedance for approximately 200ns. (4) All specifications assume $+V_S$ connected to $+V_L$ and $-V_S$ connected to $-V_L$. If supplies are connected separately, $-V_L$ must not be more negative than $-V_S$ to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	$-V_S$	Analog Negative Supply
2	LCOM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	ACOM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC56P	16-Pin Plastic DIP	802
DAC56U	16-Pin SOIC	803

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±15VDC
Input Logic Voltage	–1V to $+V_S/+V_L$
Power Dissipation	850mW
Operating Temperature	–25°C to +70°C
Storage Temperature	–80°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

OPERATING INSTRUCTIONS

The accuracy of a D/A converter is described by the transfer function as shown in Figure 1. Digital input to analog output converter relationships are shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift is due to the drift of the internal reference zener diode with temperature or time.

The converter is designed so that these drifts are in opposite directions. This way the bipolar zero voltage is virtually unaffected by variations in the reference voltage.

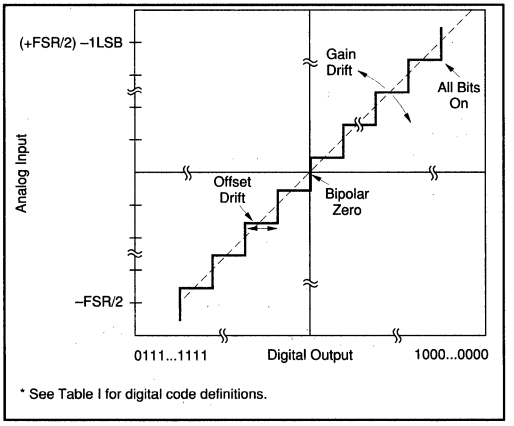


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
$7FFF_H$	+ Full Scale	+2.999908	–0.999970
8000_H	– Full Scale	–3.000000	+1.000000
0000_H	Bipolar Zero	0.000000	0.000000
$FFFF_H$	Zero –1LSB	–0.000092	+0.030500µA

TABLE I. Digital Input to Analog Output Relationship.

DIGITAL INPUT CODES

The DAC56 accepts serial input data (MSB first) in Binary Two's Complement form—Refer to Table I for input/output relationships.

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added as shown in the Connection Diagram (Figure 2), for optimum performance and noise rejection.

These capacitors (1µF tantalum recommended) should be connected as close as possible to the converter.

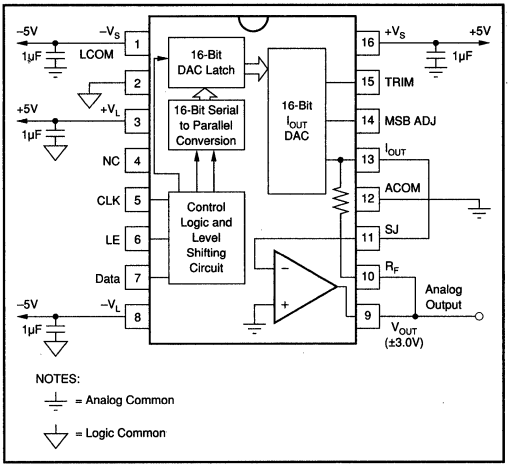


FIGURE 2. Connection Diagram.

MSB ERROR ADJUSTMENT (OPTIONAL)

Differential linearity error at all codes of the DAC56 is guaranteed to meet specifications without an external adjustment. However, if adjustment of the differential linearity error at bipolar zero is desired, it can be trimmed essentially to zero using the circuit as shown in Figure 3.

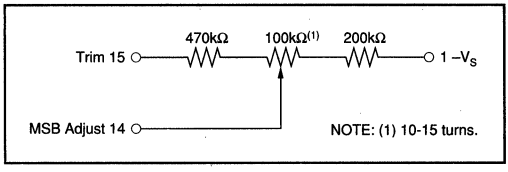
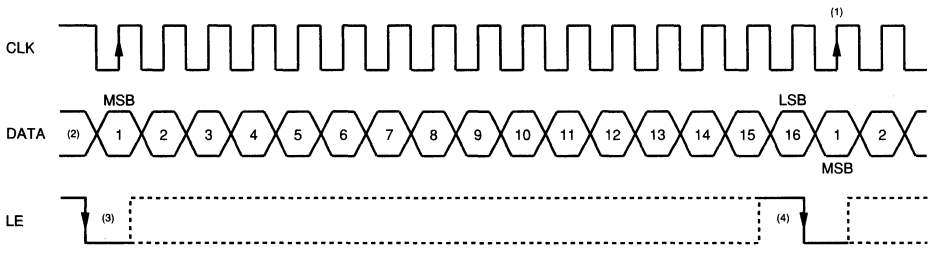


FIGURE 3. MSB Adjustment Circuit.

After allowing ample warm-up time (5 to 10 minutes) to assure stable operation, select the input code $FFFF_H$. Measure the output voltage using a 6-1/2 digit voltmeter and record the measurement. Change the digital input code to 0000_H. Adjust the 100kΩ potentiometer (TCR of 100ppm per °C or less is recommended) to make the output voltage read 1LSB more than the voltage reading of the previous code (ex. 1LSB = 92µV at FSR = 6V).

If the MSB adjustment circuit is not used, pins 14 and 15 should be left open.



NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 4. Input Timing Diagram.

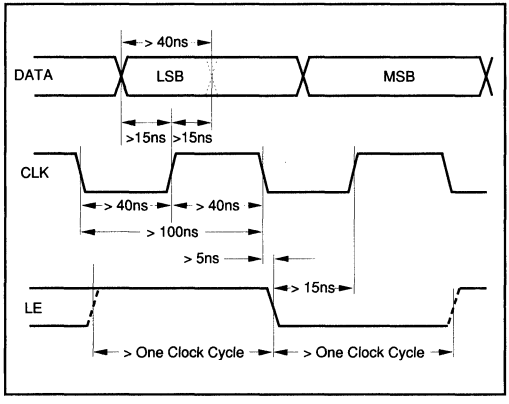


FIGURE 5. Input Timing Relationships.

INPUT TIMING CONSIDERATIONS

Figures 4 and 5 refer to the input timing required to interface the inputs of DAC56 to a serial input data stream. Serial data is accepted in Binary Two's Complement with the MSB being loaded first. Data is clocked in on positive going clock (CLK, pin 5) edges and is latched into the DAC input register on negative going latch enable (LE, pin 6) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are those that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

Figure 4 gives the general input format required for the DAC56. Figure 5 shows the specific relationships between the various signals and their timing constraints.

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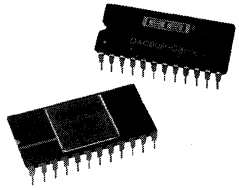


DAC80
DAC80P

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **INDUSTRY STANDARD PINOUT**
- **FULL ±10V SWING WITH V_{CC} = ±12VDC**
- **DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE**
- **GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES**
- **±1/2LSB MAXIMUM NONLINEARITY: 0°C to +70°C**
- **SETTLING TIME: 4µs max to ±0.01% of Full Scale**
- **GUARANTEED MONOTONICITY: 0°C to +70°C**
- **TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic**

DESCRIPTION

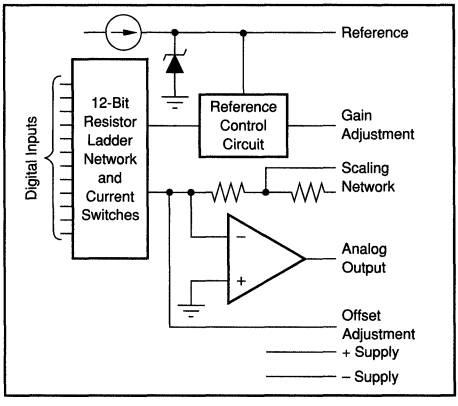
This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80 first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with voltage output only.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H.



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SPECIFICATIONS

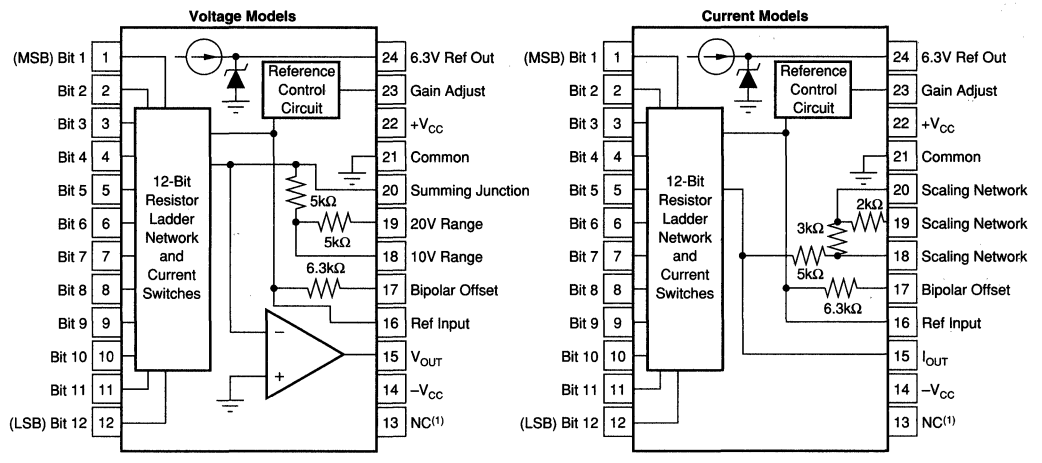
ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

PARAMETER	DAC80 MIN	DAC80 TYP	DAC80 MAX	UNITS
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (0°C to +70°C)(1):				
V_{IH} (Logic "1")	+2		+16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	µA
I_{IL} (V_{IN} = +0.4V)			–180	µA
ACCURACY (at +25°C)				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4	LSB
Gain Error(2)		±0.1	±0.3	%
Offset Error(2)		±0.05	±0.15	% of FSR(3)
DRIFT (0°C to +70°C)(4)				
Total Bipolar Drift (includes gain, offset, and linearity drifts)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C(5)				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.06	±0.12	% of FSR
Gain: Including Internal Reference		±10	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	±3/4	LSB
Linearity Error 0°C to +70°C		±1/4	±1/2	LSB
Monotonicity Guaranteed	0		+70	°C
CONVERSION SPEED, V_{OUT} Models				
Settling Time to ±0.01% of FSR				
For FSR Change (2kΩ || 500pF Load)				
with 10kΩ Feedback		3	4	µs
with 5kΩ Feedback		2	3	µs
For 1LSB Change		1		µs
Slew Rate	10			V/µs
CONVERSION SPEED, I_{OUT} Models				
Settling Time to ±0.01% of FSR				
For FSR change: 10Ω to 100Ω Load		300		ns
1kΩ Load		1		µs
ANALOG OUTPUT, V_{OUT} Models				
Ranges		±2.5, ±5, ±10, +5, +10		V
Output Current(6)	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration(7)		Indefinite		
ANALOG OUTPUT, I_{OUT} Models				
Ranges: Bipolar	±0.96	±1.0	±1.04	mA
Unipolar	–1.96	–2.0	–2.04	mA
Output Impendance: Bipolar	2.6	3.2	3.7	kΩ
Unipolar	4.6	6.6	8.6	kΩ
Compliance	–2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
External Current (constant load)			2.5	mA
Drift vs Temperature		±10	±20	ppm/°C
Output Impedance		1		Ω
POWER SUPPLY SENSITIVITY				
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±11.4		±16.5	VDC
Supply Drain (no load): $+V_{CC}$		8	12	mA
$-V_{CC}$		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480	mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	–25		+85	°C
Storage: Plastic DIP	–60		+100	°C
Ceramic DIP	–65		+150	°C

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range. (7) Short circuit current is 40mA, max.

FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS



NOTE: (1) Logic supply applied to this pin has no effect.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V to +18V
$-V_{CC}$ to Common	0V to –18
Digital Data Inputs to Common	–1V to +18V
Reference Output to Common	$\pm V_{CC}$
Reference Input to Common	$\pm V_{CC}$
Bipolar Offset to Common	$\pm V_{CC}$
10V Range R to Common	$\pm V_{CC}$
20V Range R to Common	$\pm V_{CC}$
External Voltage to DAC Output	–5V to +5V
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	100°C/W
Ceramic DIP	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC80P	24-Pin Plastic DIP	167
DAC80	24-Pin Ceramic DIP	125

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

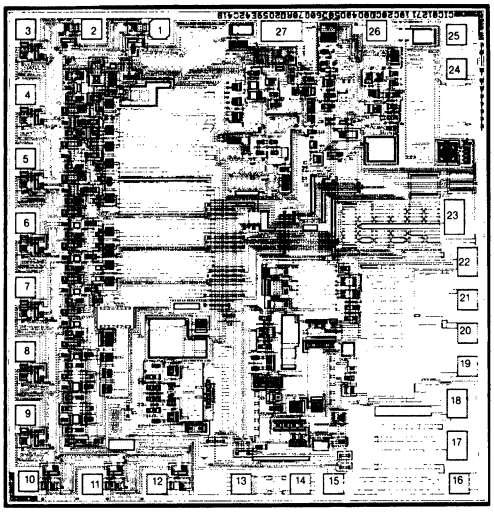
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "–BI" to the base model number.

ORDERING INFORMATION

MODEL	PACKAGE	OUTPUT
DAC80-CBI-I	Ceramic DIP	Current
DAC80Z-CBI-I	Ceramic DIP	Current
DAC80-CBI-V	Ceramic DIP	Voltage
DAC80Z-CBI-V	Ceramic DIP	Voltage
DAC80P-CBI-V	Plastic DIP	Voltage
BURN-IN SCREENING OPTION		
MODEL	**PACKAGE**	**BURN-IN TEMP. (160h)(1)**
DAC80-CBI-V-BI	Ceramic DIP	+125°C
DAC80P-CBI-V-BI	Plastic DIP	+125°C

NOTE: (1) Or equivalent combination. See text.

DICE INFORMATION



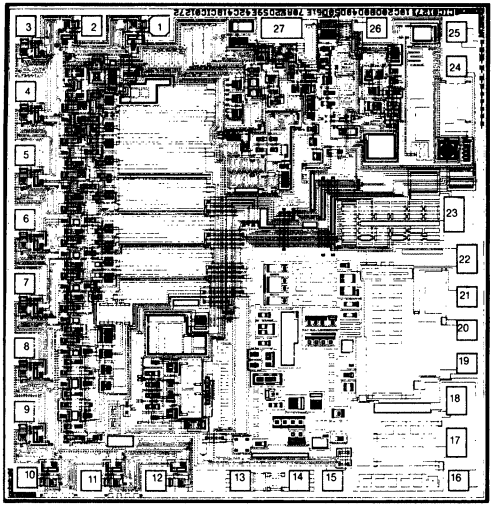
DAC80KD-V DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB)	15	$-V_{CC}$
2	Bit 2	16	V_{OUT}
3	Bit 3	17	Ref In
4	Bit 4	18	Bipolar Offset
5	Bit 5	19	Scale 10V FSR
6	Bit 6	20	Scale 20V FSR
7	Bit 7	21	NC
8	Bit 8	22	Sum Junct
9	Bit 9	23	COM
10	Bit 10	24	COM
11	Bit 11	25	$+V_{CC}$
12	Bit 12 (LSB)	26	Gain Adjust
13	NC	27	6.3V Ref Out
14	NC		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	118 x 121 ± 5	3.0 x 3.07 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum



DAC80KD-I DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB)	15	$-V_{CC}$
2	Bit 2	16	I_{OUT}
3	Bit 3	17	Ref In
4	Bit 4	18	Bipolar Offset
5	Bit 5	19	Scale 10V FSR
6	Bit 6	20	Scale 20V FSR
7	Bit 7	21	Scale
8	Bit 8	22	NC
9	Bit 9	23	COM
10	Bit 10	24	COM
11	Bit 11	25	$+V_{CC}$
12	Bit 12 (LSB)	26	Gain Adjust
13	NC	27	6.3V Ref Out
14	NC		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	118 x 121 ± 5	3.0 x 3.07 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	CSB Complementary Straight Binary	COB Complementary Offset Binary	CTC[1] Complementary Two's Complement
000000000000	+Full Scale	+Full Scale	–1LSB
011111111111	+1/2 Full Scale	Zero	–Full Scale
100000000000	1/2 Full Scale –1LSB	–1LSB	–Full Scale
111111111111	Zero	–Full Scale	Zero

NOTE: (1) Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE I. Digital Input Codes.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C, and +70°C; 2) calculating the gain error with respect to the 25°C value, and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C, and 70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

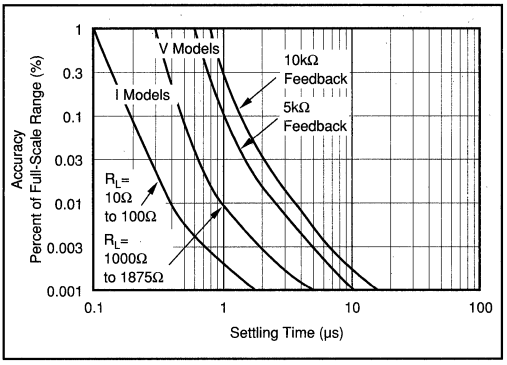


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to –2V (see Figures 11 and 12).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage range of ±1V and 0 to –2V (see Figures 11 and 12).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input

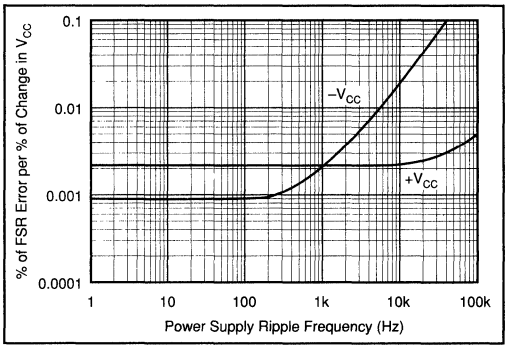


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

(pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC80 digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC80 directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1µF tantalum) should be located close to the DAC80.

±12V OPERATION

All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, minimum, over the entire V_{CC} range.

No bleed resistor is needed from $+V_{CC}$ to pin 24, as was needed with prior hybrid Z versions of DAC80. Existing ±12V applications that are being converted to the monolithic DAC80 must omit the resistor to pin 24 to insure proper operation.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

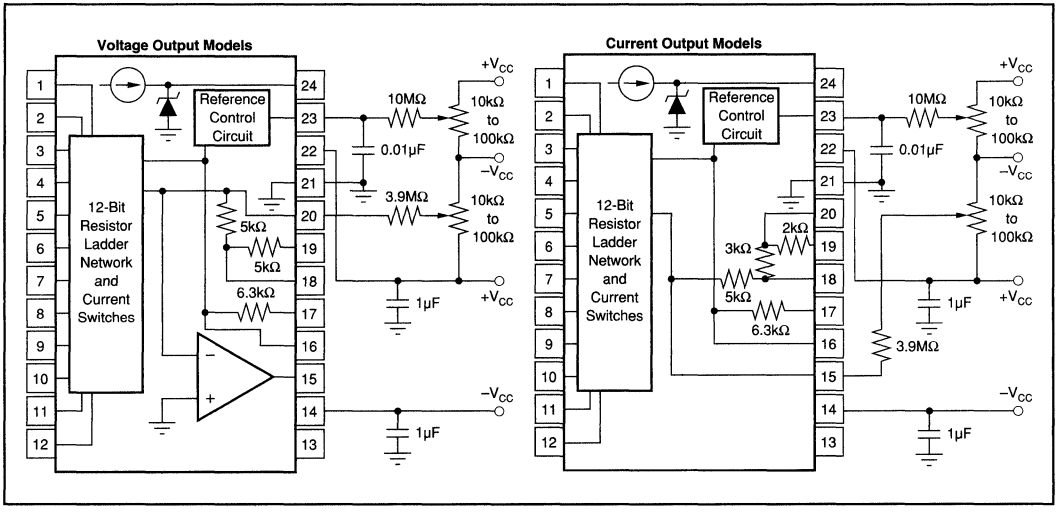


FIGURE 3. Power Supply and External Adjustment Connection Diagrams.

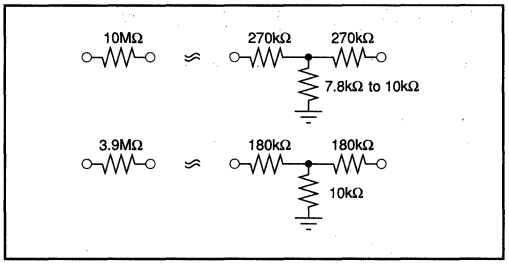


FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC80 must change the gain trim resistor on pin 23 from 33MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001µ1F to 0.01µF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

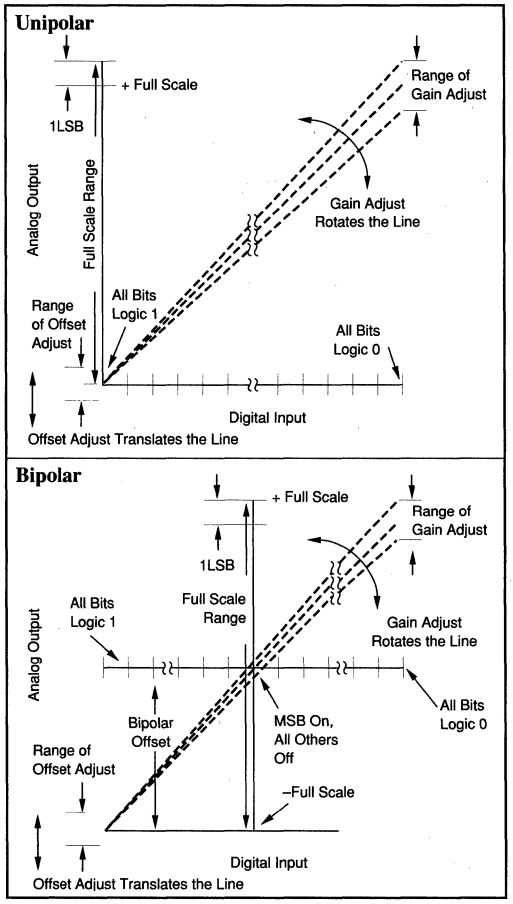


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is –10V. See Table II for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

	ANALOG OUTPUT			
DIGITAL INPUT	VOLTAGE(1)		CURRENT	
MSB LSB ↓ ↓	0 to +10V	±10V	0 to –2mA	±1mA
000000000000	+9.9976V	+9.9951V	–1.9995mA	–0.9995mA
011111111111	+5.0000V	0.0000V	–1.0000mA	0.0000mA
100000000000	+4.9976V	–0.0049V	–0.9995mA	+0.0005mA
111111111111	0.0000V	–10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488µA	0.488µA

NOTE: (1) To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE II. Digital Input/Analog Output.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V, ±5V, or ±2.5V; or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

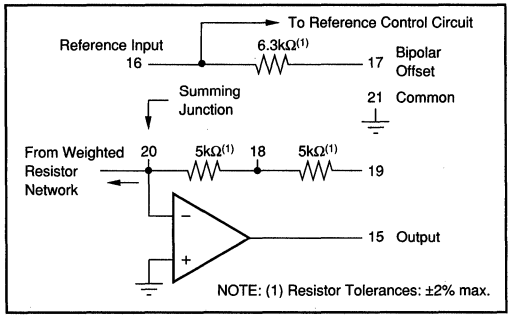


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4µs for the 20V range and 3µs for the 10V range.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

TABLE III. Output Voltage Range Connections for Voltage Models.

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

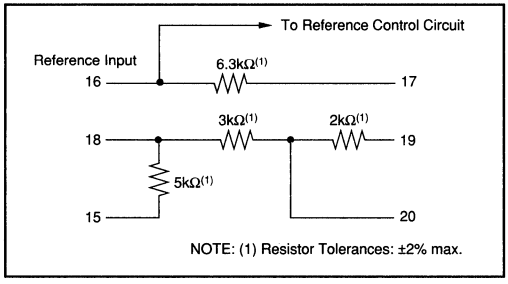


FIGURE 7. Internal Scaling Resistors.

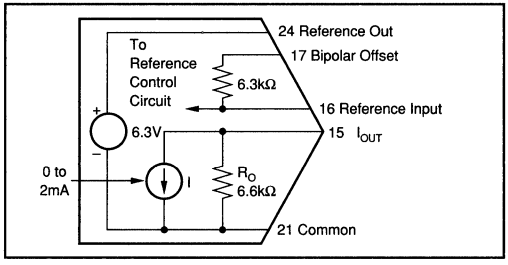


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

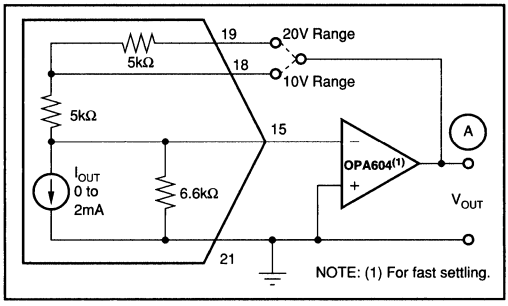


FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

TABLE IV. Voltage Range of Current Output.

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} value of ±1mA for bipolar voltage ranges and –2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

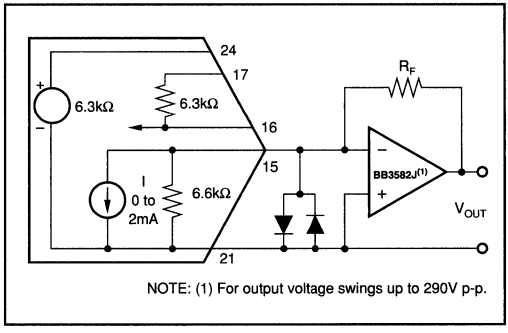


FIGURE 10. External Op-Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

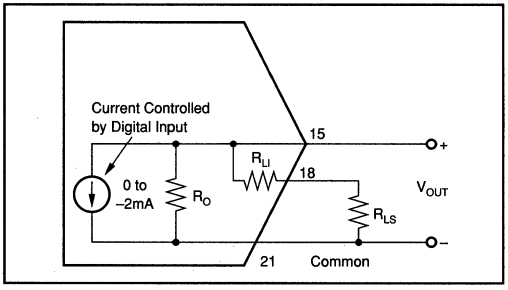


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to 20 and pin 18 to 19). By choosing R_{LS} = 210Ω, R_L = 1178Ω. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to –2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ in parallel with 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing R_{LS} = 225Ω, R_L = 1455Ω. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

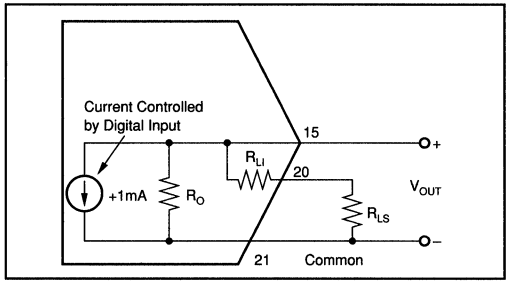


FIGURE 12. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

BURR-BROWN®

DAC600

DEMO BOARD AVAILABLE
See Appendix A

12-Bit 256MHz Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- 256MHz UPDATE RATE
- –73dB HARMONIC DISTORTION AT 10MHz
- LASER TRIMMED ACCURACY: 1/2LSB
- –5.2V SINGLE POWER SUPPLY
- EDGE-TRIGGERED LATCH
- LOW GLITCH: 5.6pVs
- WIDEBAND MULTIPLYING REFERENCE INPUT
- 50Ω OUTPUT IMPEDANCE

APPLICATIONS

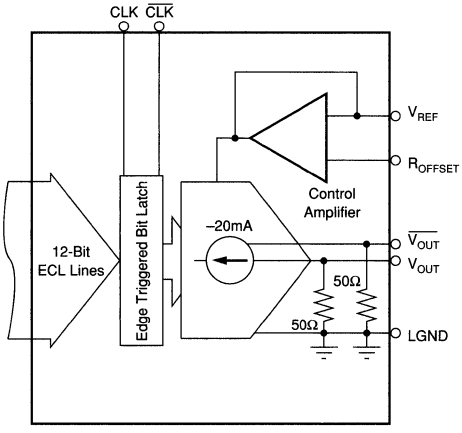
- DIRECT DIGITAL SYNTHESIS
- ARBITRARY WAVEFORM GENERATION
- HIGH RESOLUTION GRAPHICS
- COMMUNICATIONS LOCAL OSCILLATORS
  Spread Spectrum/Frequency Hopping
  Base Stations
  Digitally Tuned Receivers

DESCRIPTION

The DAC600 is a monolithic, high performance digital-to-analog converter for high frequency waveform generation. The internal segmentation and latching minimize output glitch energy and maximizes AC performance. Resistor laser trimming provides for excellent DC linearity.

The ECL compatibility provides for low digital noise at high update rates. The complementary 50Ω outputs and low output capacitance simplifies transmission line design and filtering at the output.

The DAC600 combines precision thin film and bipolar technology to create a high performance, cost effective solution for modern waveform synthesis.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C V_{REF} = +1.0V, V_{EEA} = V_{EED} = –5.2V, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	DAC600AN MIN	DAC600AN TYP	DAC600AN MAX	DAC600BN MIN	DAC600BN TYP	DAC600BN MAX	UNITS
DIGITAL INPUTS									
Logic	12 Parallel Input Lines, ECL								
Resolution					12			*	Bits
ECL Logic Input Levels: V_{IL}	Logic "0"	Full	–1.48	–1.95	–2	*	*	*	V
I_{IL}		Full			2			*	µA
V_{IH}	Logic "1"	Full	–1.1	–0.75	0	*	*	*	V
I_{IH}		Full			200			*	µA
DIGITAL TIMING									
Input Data Rate		Full	DC		256	*		*	MHz
CLK Pulse Width High or Low		Full	1.95			*			ns
Set-up Time		Full	1.5	1.0		*	*		ns
Hold Time (Referred to CLK)		Full	1.9	1.7		*	*		ns
Propagation Delay		Full		2			*		ns
ANALOG OUTPUT									
Bipolar Output Current	R_L = 0Ω	Full	19	20	21	*	*	*	mA
Output Resistance		Full	47.5	50	52.5	49	*	51	Ω
Output Capacitance		Full		15			*		pF
CONTROL AMPLIFIER									
Input Resistance		Full		800			*		Ω
Full Power Bandwidth	–3dB	Full		10			*		MHz
Offset		+25°C		0	±1		0	±0.5	mV
Input Reference Range		Full	100mV		±1.25	*		*	V
TRANSFER CHARACTERISTICS									
Integral Linearity Error[1]: $V_{OUT\ NOT}$	Best Fit Straight Line	+25°C		±0.012	±0.024		±0.006	±0.012	%FSR
$V_{OUT\ NOT}$		Full		±0.024	±0.036		±0.012	±0.024	%FSR
V_{OUT}		+25°C			±0.1			±0.1	%FSR
Differential Linearity Error[1]: $V_{OUT\ NOT}$		+25°C			±0.024			±0.012	%FSR
$V_{OUT\ NOT}$		Full			±0.036			±0.024	%FSR
V_{OUT}		+25°C			±0.1%			±0.1%	%FSR
12-Bit Monotonicity		+25°C		Guaranteed			Guaranteed		
		Full		Typical			Guaranteed		
Output Offset Current: $V_{OUT\ NOT}$	Bits 1-12 HIGH	+25°C		75	150		50	100	µA
$V_{OUT\ NOT}$		Full		57	150		50	100	µA
Gain Error[2]		+25°C		±0.5	±1.5		±0.5	±1.0	%
		Full		±1.3	±2.0		±1.1	±2.0	%
Output Leakage Current	V_{REF} = 0V, Bits 1-12 LOW, $V_{OUT\ NOT}$	+25°C		10	75		5	50	µA
TIME DOMAIN PERFORMANCE									
Glitch Energy	Major Carry	+25°C		5.6			*		pVs
Fall Time	90% to 10%	+25°C		510			*		ps
Rise Time	10% to 90%	+25°C		770			*		ps
Settling Time[3]									
±0.1% FSR	Major Carry, 1 LSB Change	Full		4			*		ns
±0.024% FSR		Full		15			*		ns
DYNAMIC PERFORMANCE									
Spurious Free Dynamic Range[4]									
f_O = 1MHz	f_{CLOCK} = 50MHz	+25°C		74		70	77		dBFS[3]
f_O = 10MHz	f_{CLOCK} = 50MHz	+25°C		71		65	73		dBFS
f_O = 1MHz	f_{CLOCK} = 100MHz	+25°C		72		70	75		dBFS
f_O = 10MHz	f_{CLOCK} = 100MHz	+25°C		71		66	70		dBFS
f_O = 20MHz	f_{CLOCK} = 100MHz	+25°C		63		59	62		dBFS
f_O = 10MHz	f_{CLOCK} = 200MHz	+25°C		66		66	70		dBFS
f_O = 20MHz	f_{CLOCK} = 200MHz	+25°C		58		64	67		dBFS
f_O = 50MHz	f_{CLOCK} = 200MHz	+25°C		52		50	55		dBFS
Output Noise	Bits 1-12 HIGH	+25°C		10.6			*		nV/√Hz
POWER SUPPLIES									
Supply Voltages: V_{EE}		Full	–4.5	–5.2	–5.5	*	*	*	V
Supply Currents: I_{EEA}	Pins 33 and 34	Full	30	46	60	*	*	*	mA
I_{EED}	Pins 5 and 55	Full	110	150	190	*	*	*	mA
Power Consumption	Operating	Full		900mW	1.3		*	*	W
TEMPERATURE RANGE									
Specification: DAC600AN, BN	Ambient	Full	–40		+85	*		*	°C
θ_{JA}				30			*		°C/W

NOTES: (1) Linearity tests are measured into a virtual ground (op amp). (2) Gain error in % is calculated by: GE (%) = $\frac{V_{MEASURED}\ (FS) - V_{IDEAL}\ (FS)\ X\ 100}{V_{IDEAL}\ (FS)}$
(3) Settling time is influenced by the load due to fast edge speeds. Use good transmission line techniques for best results. (4) Spurious free dynamic range is measured from the fundamental frequency to any harmonic or non-harmonic spurs within the bandwidth $f_{CLK}/2_C$, unless otherwise specified.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE (AMBIENT)
DAC600AN, BN	68-Pin Plastic QUAD	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

V_{EEA}	0.3 to –7
V_{EED}	0.3 to –7
Logic Inputs	0 to –5.5V
Reference Input Voltage	0 to +1.25V
Reference Input Current	0 to 1.56mA
Case Temperature	–40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC600AN, BN	68-Pin Plastic QUAD	312-1

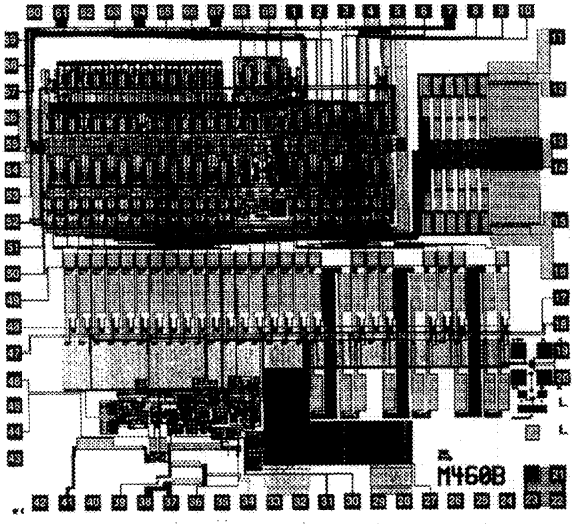
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION	PIN NO	DESIGNATION	DESCRIPTION
1	BYPASS	Disables Latching of Data	35	V_{REF2}	Analog Reference Voltage Center Tap
2	CLK	CLOCK	36	NC	
3	CLKNOT	CLOCKNOT	37	NC	
4	DGND	Digital Ground	38	V_{REF}	Analog Reference Voltage
5	DV_{EE}[1]	–5.2V Supply	39	V_{REF}	Analog Reference Voltage
6	Bit 9		40	NC	
7	Bit 10		41	NC	
8	Bit 11		42	R_{OFFSET}	Offset Compensation
9	Bit 12	LSB	43	NC	
10	NC		44	BYPASS	0.1µF Bypass to Ground
11	NC		45	NC	
12	NC		46	NC	
13	V_{OUT}	DAC Output	47	ALTCOMPC	Control Amp PTAT Reference Compensation[2]
14	V_{OUT}	DAC Output	48	AGND	Analog Signal Ground
15	LGND	Ladder Ground	49	NC	
16	LGND	Ladder Ground	50	LBIAS	Ladder Bias Alternate Compensation[2]
17	V_{OUTNOT}	DAC Output Complement	51	NC	
18	V_{OUTNOT}	DAC Output Complement	52	NC	
19	NC		53	NC	
20	AGND	Analog Ground	54	Bit 1	MSB
21	NC		55	DV_{EE}	Digital –5.2V Supply
22	NC		56	DGND	Digital Signal Ground
23	NC		57	DGND	Digital Signal Ground
24	NC		58	Bit 2	
25	NC		59	Bit 3	
26	BYPASS	0.1µF Bypass to Ground	60	Bit 4	
27	NC		61	NC	
28	ALTCOMPIB	PTAT-IB Reference Compensation[2]	62	Bit 5	
29	AGND	Analog Ground	63	DGND	Digital Ground
30	AGND	Analog Ground	64	Bit 6	
31	NC		65	Bit 7	
32	LOOPCRNT	DAC Reference Alt. Loop Current (Connect to AGND)	66	DGND	Digital Ground
			67	Bit 8	
33	V_{EE}[1]	–5.2V Supply	68	NC	
34	V_{EE}[1]	–5.2V Supply			

NC: no connect
NOTE: (1) Pins 5 and 55 typically draw 150mA of current. Pins 33 and 34 combined typically draw 46mA. (2) Connect bypass capacitor to V_{EE}.

DICE INFORMATION



DAC600 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bypass	36	NC
2	CLK	37	V_{REF}
3	CLKNOT	38	V_{REF}
4	DGND	39	NC
5	DV_{EE}	40	NC
6	Bit 9	41	R_{OFFSET}
7	NC	42	NC
8	Bit 10	43	NC
9	Bit 11	44	NC
10	Bit 12	45	NC
11	V_{OUT}	46	ALTCOMPC
12	V_{OUT}	47	AGND
13	LGND	48	NC
14	LGND	49	LBIAS
15	V_{OUTNOT}	50	NC
16	V_{OUTNOT}	51	NC
17	NC	52	NC
18	AGND	53	Bit 1 (MSB)
19	NC	54	DV_{EE}
20	NC	55	DGND
21	NC	56	DGND
22	NC	57	Bit 2
23	NC	58	Bit 3
24	NC	59	Bit 4
25	NC	60	NC
26	NC	61	NC
27	ALTCOMPIB	62	NC
28	AGND	63	Bit 5
29	AGND	64	DGND
30	NC	65	Bit 6
31	LOOPCRNT	66	Bit 7
32	AV_{EE}	67	DGND
33	AV_{EE}	68	Bit 8
34	V_{REF2}	69	NC
35	NC		

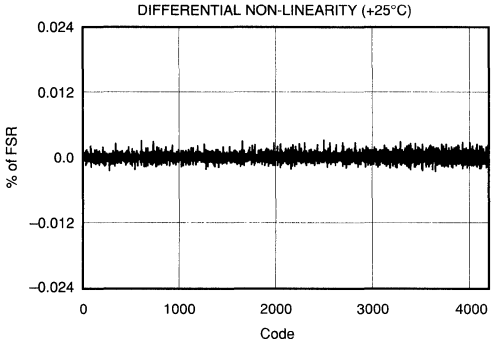
Substrate Bias: Negative Supply $-V_{CC}$.
NC = Do not connect.

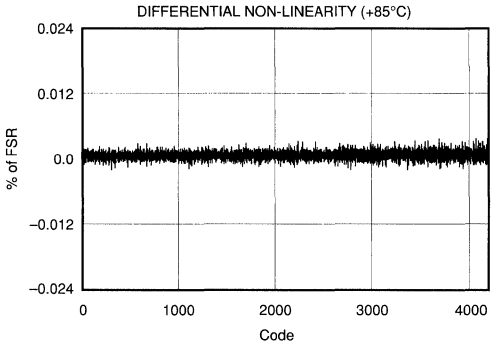
MECHANICAL INFORMATION

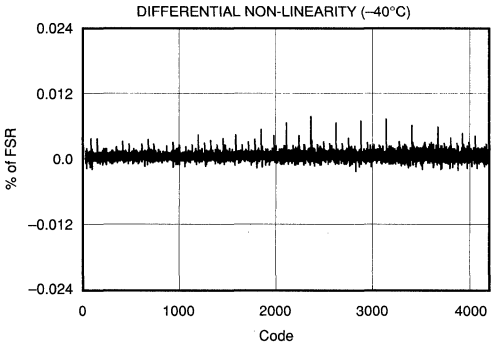
	MILS (0.001")	MILLIMETERS
Die Size	160 x 140 ±5	4.06 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	
Metallization	Gold	

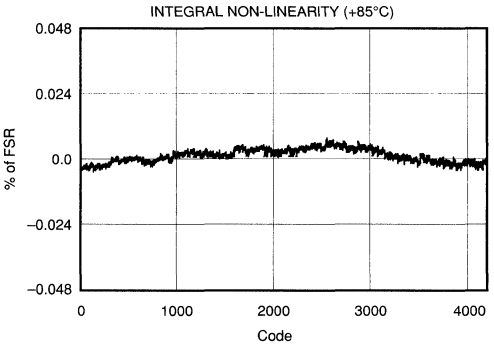
TYPICAL PERFORMANCE CURVES

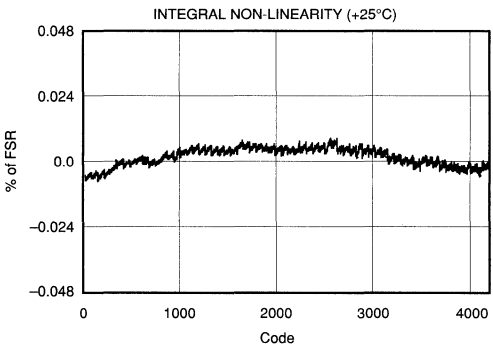
AT T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

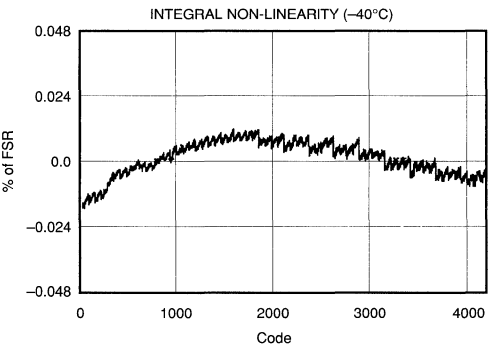








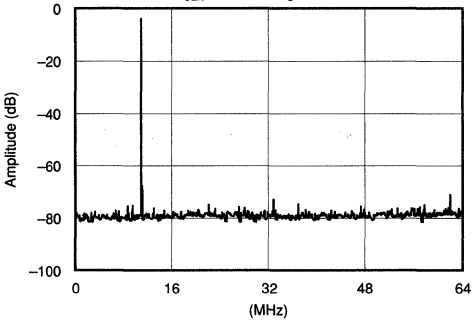




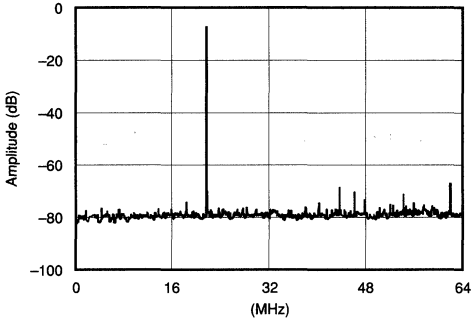
TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

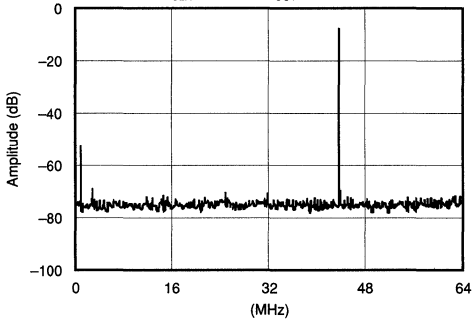
OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_O = 11MHz



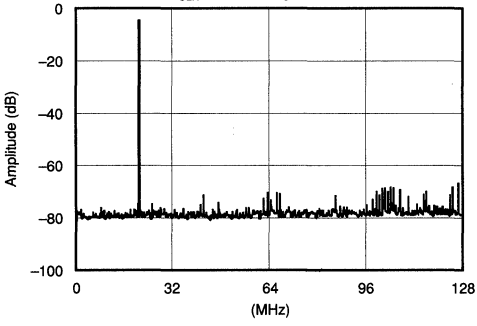
OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_O = 21.9MHz



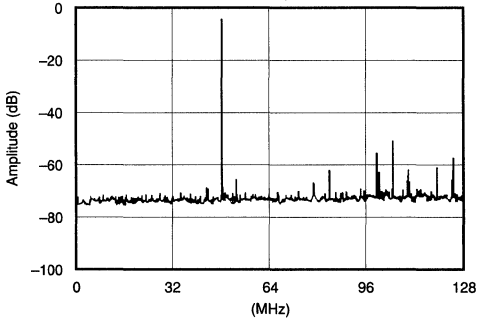
OUTPUT SPECTRUM AT
f_{CLK} = 128MHz, f_{OUT} = 41.5MHz



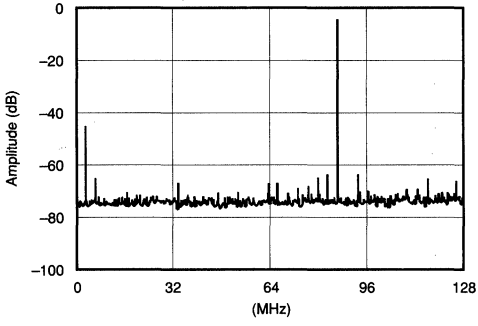
OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 33.8MHz



OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 55.3MHz



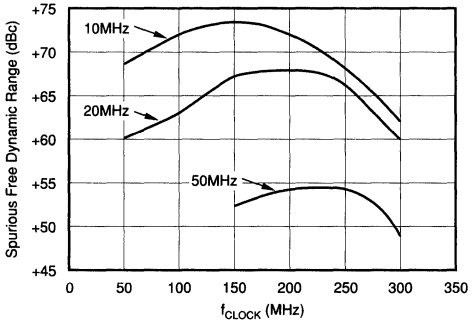
OUTPUT SPECTRUM AT
f_{CLK} = 256MHz, f_O = 83.1MHz



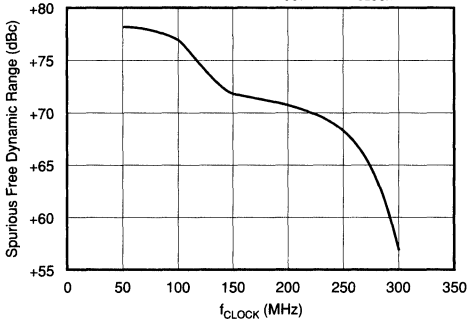
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

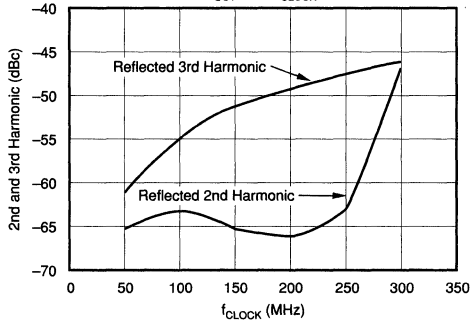
SPURIOUS FREE DYNAMIC RANGE vs CLOCK FREQUENCY



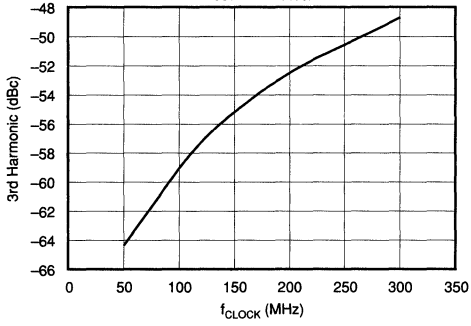
SPURIOUS FREE DYNAMIC RANGE vs CLOCK FREQUENCY ($f_{OUT} \approx 1/16\ f_{CLOCK}$)



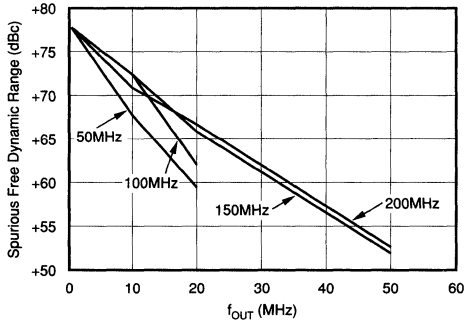
HARMONIC DISTORTION vs CLOCK FREQUENCY ($f_{OUT} \approx 1/3\ f_{CLOCK}$)



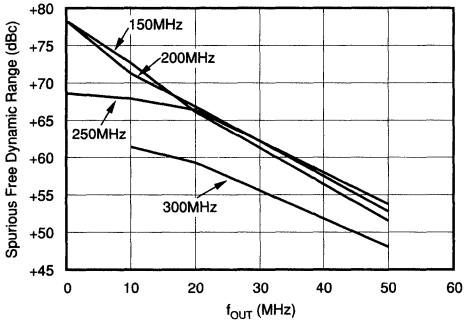
3RD HARMONIC vs CLOCK FREQUENCY ($f_{OUT} \approx 1/4\ f_{CLOCK}$)



SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY



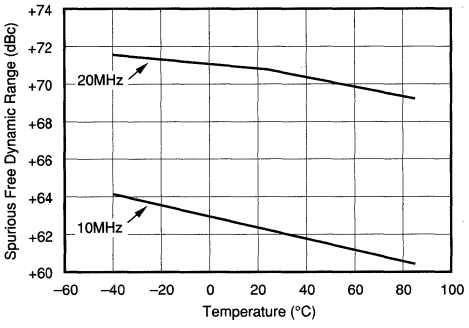
SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY



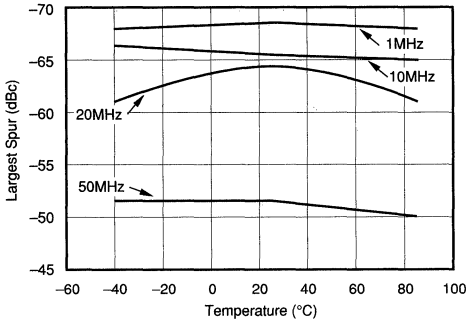
TYPICAL PERFORMANCE CURVES (CONT)

At T_{CASE} = +25°C, V_{REF} = +1.0V, measured at $V_{OUT\ NOT}$. Spurious free dynamic range includes all harmonic or non-harmonic spurs in the bandwidth $f_{CLK}/2$, unless otherwise noted.

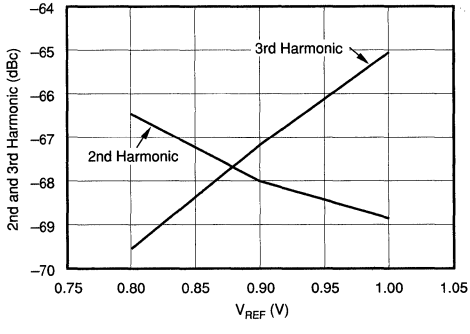
SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



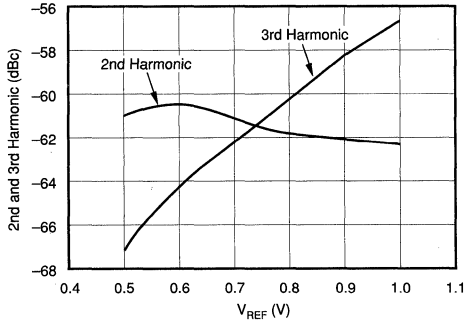
SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



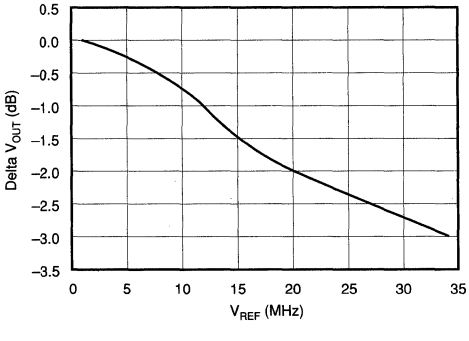
REFERENCE VOLTAGE vs DISTORTION (f_{CLK} = 128MHz, f_{OUT} = 21.9MHz)



HARMONIC DISTORTION vs REFERENCE VOLTAGE ($f_{OUT} \approx 1/4\ f_{CLOCK}$)

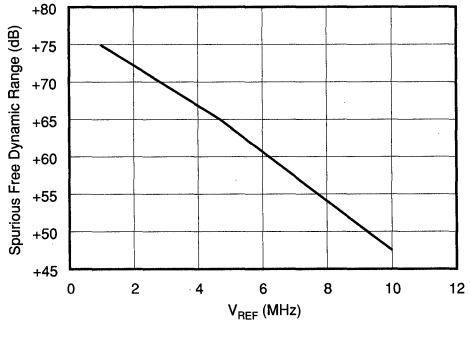


REFERENCE CONTROL AMPLIFIER FREQUENCY RESPONSE



V_{REF} Amplitude +0.75V DC 100mVp-p AC
(All Bits on, 47pF Pin 35)

SPURIOUS FREE DYNAMIC RANGE vs REFERENCE FREQUENCY



V_{REF} Amplitude +0.75V DC 100mVp-p AC
(All Bits on, 47pF Pin 35)

THEORY OF OPERATION

The DAC600 employs a familiar architecture where input bits switch on the appropriate current sources (Figure 1.) Bits 1-4 are decoded into 15 segments after the first set of latches. The edge triggered master-slave latches are driven by an internal clock buffer. Current sources for bits 5 and 6 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 7-12 are properly scaled and fed to the laser trimmed R-2R ladder.

Decoding of bits 1-4 into 15 segments and synchronizing the data with a master/slave register reduces glitching. If the BYPASS input is low, data is transferred to the output on the positive going edge of the clock. If BYPASS is high, data is transferred to the output regardless of clock state. All digital inputs are ECL compatible.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder. With all of the current sources off, the output voltage is at 0V. With all current sources on (–20mA), the output voltage is at –1V. Transfer function information is given in Tables I and II.

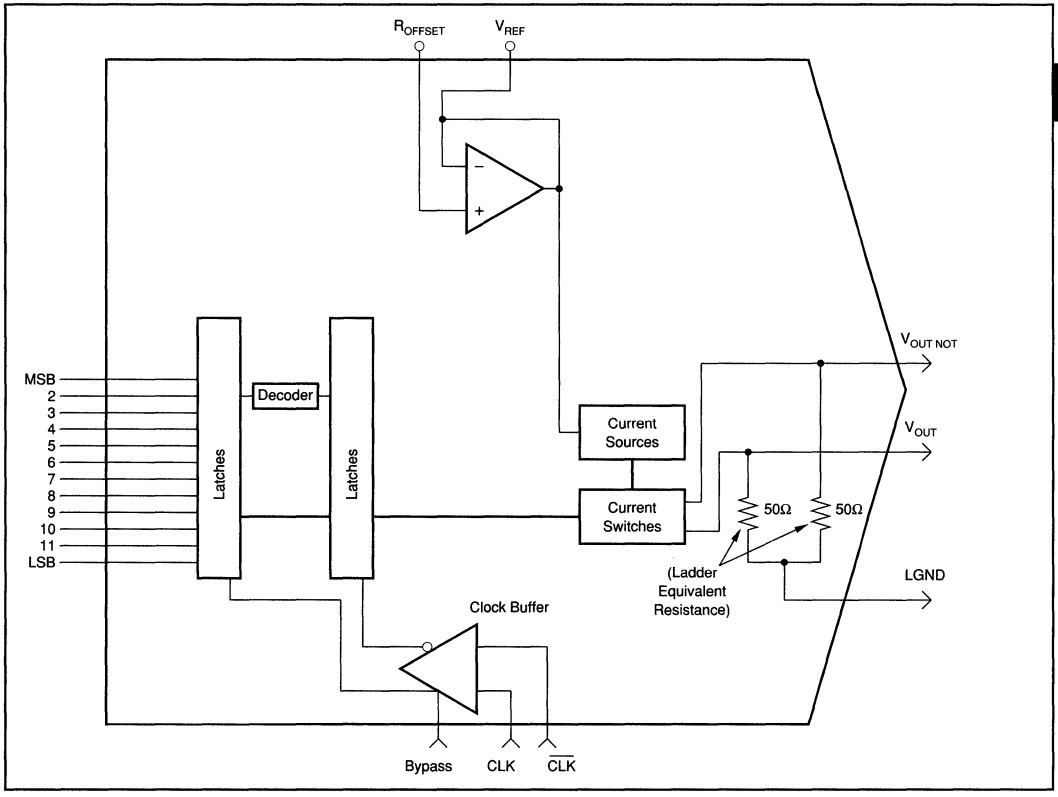


FIGURE 1. Basic DAC600 Architecture.

INPUT BITS 1 2 3 4 5 6 7 8 9 10 11 12	OUTPUT VOLTAGES V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0	0V	–0.999756V
0 0 0 0 0 0 0 0 0 0 0 1	–244µV	0.999512V
•	•	
•	•	
•	•	
•	•	
1 0 0 0 0 0 0 0 0 0 0 0	–0.5	–0.499756
1 1 1 1 1 1 1 1 1 1 1 1	–0.999756V	0

TABLE I. Input Code vs Output Voltage Relationships.

BIT	VOLTAGE (No External Load, V_{OUT})
1	–0.5
2	–0.25
3	–0.125
4	–62.5mV
5	–31.25mV
6	–15.625mV
7	–7.8125mV
8	–3.9063mV
9	–1.9531mV
10	–976µV
11	–488µV
12 (LSB)	–244µV

TABLE II. Nominal Bit Weight Values.

There is also a complementary $V_{OUT\ NOT}$ output that allows for a differential output signal. The full scale complementary outputs (V_{OUT} and $V_{OUT\ NOT}$) can be simply modeled as –20mA in parallel with 50Ω. This gives an output swing of 0.5Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

The V_{REF} pin should be supplied by a +1.0V reference that is capable of supplying a nominal current of 1.25mA. An alternative would be the use of a 1.25mA current source. A low drift reference will minimize gain drift. A recommended reference circuit is given in Figure 2 as shown in the Typical Performance Curves, lowering the reference voltage to +0.8V will typically improve the Spurious Free Dynamic Range by a few dB.

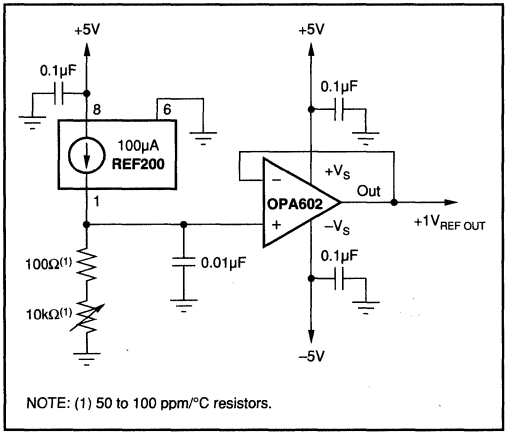


FIGURE 2. A Low Drift External Reference Circuit.

A low-cost alternative reference circuit is shown in Figure 3. This circuit uses the Burr-Brown REF1004-2.5 micropower voltage reference. Gain drift is dependent upon the temperature coefficient of the 1.2kΩ resistor. A TC of < 10ppm/°C is recommended.

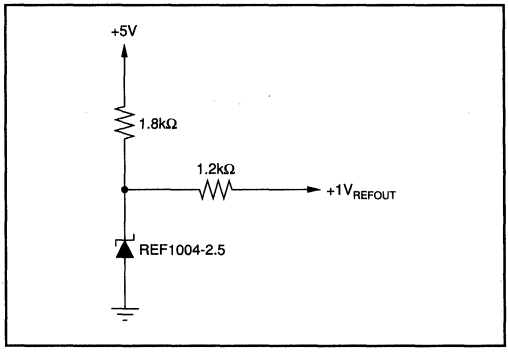


FIGURE 3. Low Cost External Reference Circuit.

The DAC600 can also accept a wideband multiplying reference input. The full power bandwidth of this reference is approximately 30MHz. Care must be taken not to exceed the minimum and maximum input reference voltage levels which are 100mV and +1.25V respectively (refer to the absolute maximum ratings section). In the multiplying reference mode, the 0.4µF bypass capacitor on LBIAS and the 0.1µF on pin 35 need to be removed. A 47pF capacitor to ground needs to be connected to pin 35 (Figure 4.)

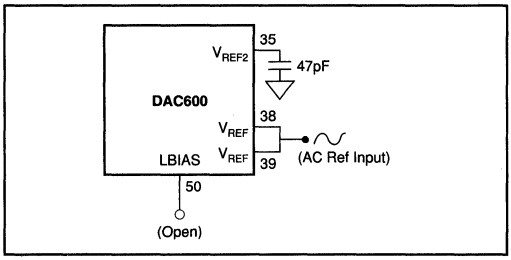


FIGURE 4. Connections for a Multiplying Reference Input.

TIMING

The DAC600 has an internal latch that is triggered on the rising edge of the clock when the BYPASS pin is set LOW. This master-slave mode of operation will assure that the 12 bits will arrive at the current sources with a minimum of data skew. Therefore, this mode is recommended for the vast majority of applications. Observing the minimum set-up and hold time recommendations will ensure proper data latching, refer to Figure 5 for complete timing specifications.

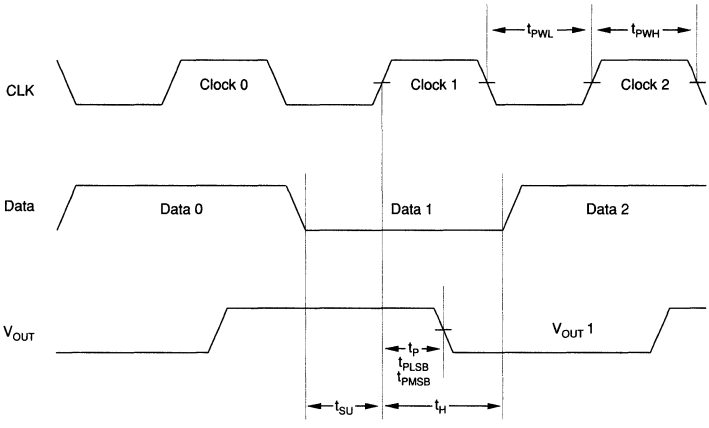
When BYPASS is set HIGH, the DAC600 will operate in the transparent mode. In this mode, both the master and slave registers are transparent and changes in input data ripple directly to the output. Since the four MSBs have a decoder delay, these bits arrive at the output approximately 600 picoseconds later than the lower 8 LSBs. Because this data skew causes glitch, this mode is not recommended for optimum AC performance.

The DAC600 has a differential ECL clock input. This clock input can also be driven by a single ended clock if desired by trying the CLKNOT input to an external voltage of –1.3V. Using a differential clock provides much improved digital feedthrough immunity, however.

DRIVING THE DAC600

The DAC600 inputs will most likely be driven by high speed ECL gate outputs. These outputs should be terminated using standard high speed transmission line techniques. Consult an ECL handbook for proper methods of termination.

Termination resistors should not be connected to the analog ground plane close to the DAC600. The fast changing digital bit currents will cause noise in the analog ground plane under this layout scheme. These fast changing digital currents should be steered away from the sensitive DAC600



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		2		ns
t_{SU}	Setup time DATA must remain stable before CLK.	1.5	1.0		ps
t_H	Hold time DATA must remain stable after CLK.	1.9	1.7		ns
t_{PWL}	CLK pulse width low (50% to 50%).	1.95			ns
t_{PWH}	CLK pulse width high (50% to 50%).	1.95			ns
t_{PMSB}	Propagation delay, MSBs, transparent mode only.		2.1		ns
t_{PLSB}	Propagation delay, LSBs, transparent mode only.		1.5		ns

FIGURE 5. Timing Diagram.

analog ground plane. For speeds of up to 256MHz, series termination with 47Ω resistors will be adequate (Figure 6). This termination technique will greatly lessen the issue of termination currents coupling into the analog ground plane. This is shown in the typical DAC600 connection diagram (Figure 7.)

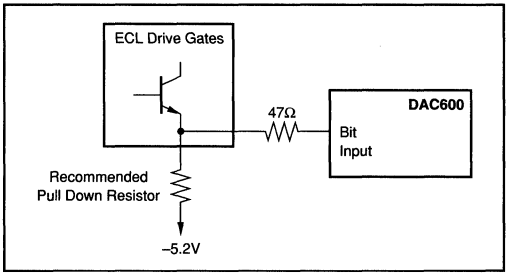


FIGURE 6. Series Bit Termination.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. All of the ground pins (both analog and digital) should be connected directly to the analog ground plane at the DAC600.

Wide busses for the power paths are recommended as good general practice. External bypassing is recommended. A 10µF ceramic capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

ALTCOMPB and ALTCOMPC should be bypassed with 0.1µF capacitors connected to V_{EEA}. When not used in the multiplying mode LBIAS should be bypassed with a 0.4µF capacitor connected to V_{EEA}. The heat spreader (pins 26 and 44) should be bypassed with a 0.1µF capacitor.

MAXIMIZING PERFORMANCE

In addition to optimizing the layout and ground of the DAC600, there are other important issues to consider when optimizing the performance of this DAC in various AC applications.

The DAC600 includes an internal 50Ω output impedance to simplify output interfacing to a 50Ω load. Because some loads may be a complex impedance, care must be taken to match the output impedance with the load. Mismatching of impedances can cause reflections which will affect the measured AC performance parameters such as settling time, harmonic distortion, rise/fall times, etc. Often complex impedances can be matched by placing a variable 3 to 10pF capacitor at the output of the DAC to ground. Also, probing the output of the DAC can present a complex impedance.

The typical performance curves of Spurious Free Dynamic Range vs various combinations of clock rate and/or input frequency should give a general idea of the spectral performance of the DAC under system specific clock and output frequencies. For variable frequency DDS and ARB applications, having a programmable frequency bandpass (smart) filter at the output of the DAC can greatly improve system

spur and noise performance by filtering out unwanted spur and noise spectra. Even with a programmable bandpass filter, care should be taken to update the DAC at greater than 4 times per cycle to (1) minimize the 2nd and 3rd harmonic magnitudes by having the output slew excessively between any successive clock and (3) to keep the 2nd harmonic and other even order harmonics from folding back close to the fundamental under the condition f_{OUT} = 1/3 f_{CLK} and (3) to keep the 3rd harmonic and other harmonics from folding back close to the fundamental under the condition f_{OUT} = 1/4 f_{CLK}. The making use of the high update rate of the DAC600 helps to lessen the problems of large harmonics "folding back" into the passband.

For DDS applications, often the DAC itself is the limit in Spurious Free Dynamic Range (SFDR) performance. However, due to the high linearity of the DAC600, low frequency spurious performance may be limited by the digital truncation error of the phase accumulator/ROM combination. Most vendors supplying a combination of phase accumulator and ROM specify the SFDR of their digital algorithm.

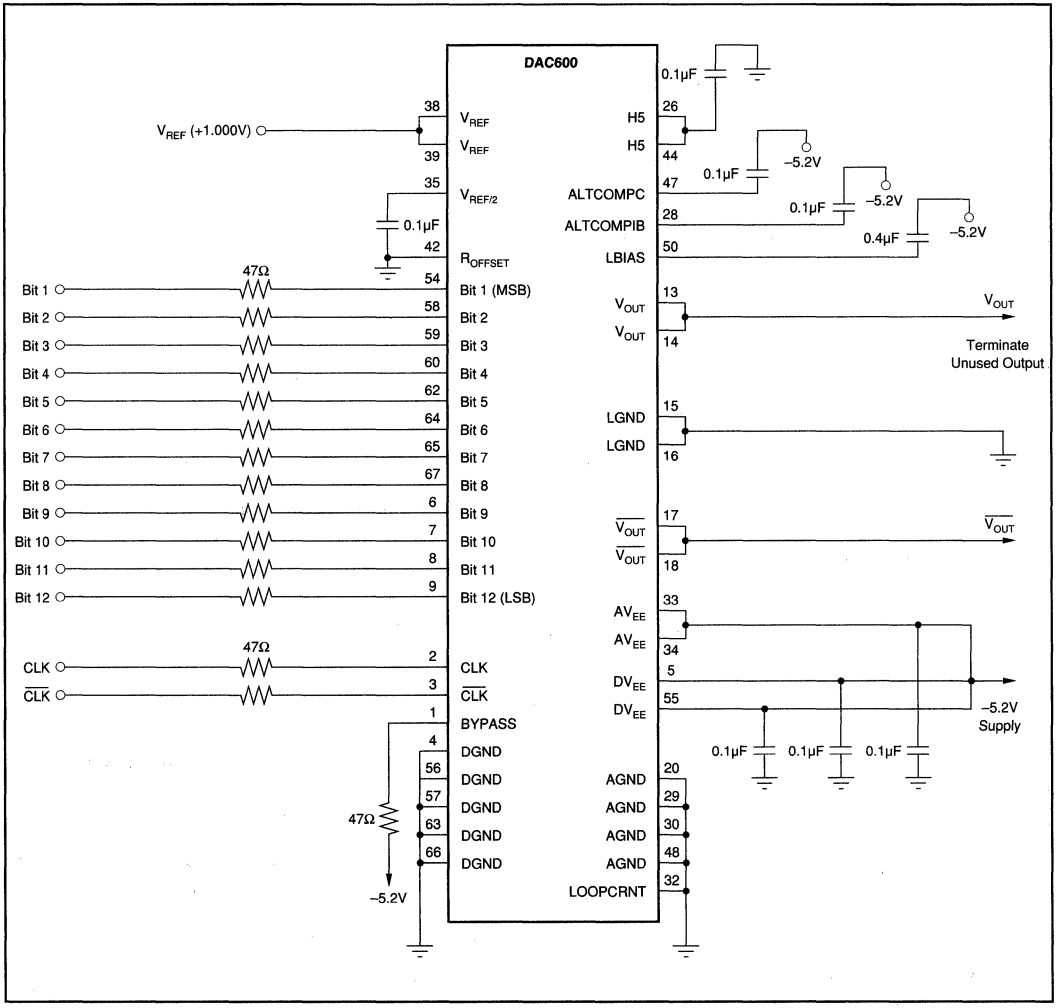
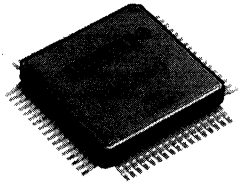


FIGURE 7. Typical DAC600 Connection Diagram.

BURR - BROWN®



DAC650

DEMO BOARD AVAILABLE
See Appendix A

12-Bit 500MHz DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- 500MHz UPDATE RATE
- GUARANTEED SPURIOUS PERFORMANCE
- LOW GLITCH
- FAST SETTLING
- INTERNAL EDGE-TRIGGERED LATCH
- LASER TRIMMED ACCURACY
- INTERNAL REFERENCE
- CLEAN LOW-NOISE OUTPUT

APPLICATIONS

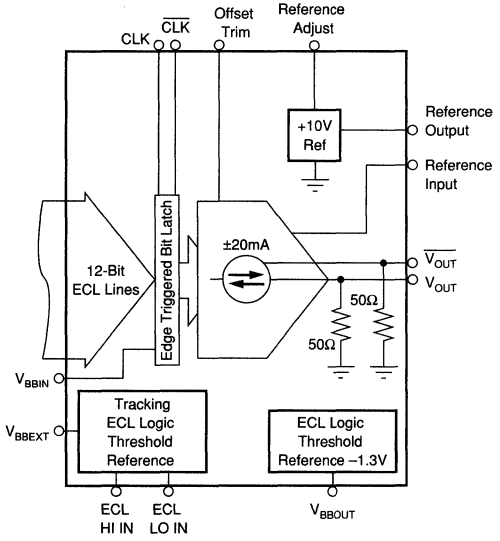
- DIRECT DIGITAL SYNTHESIS
- ARBITRARY WAVEFORM GENERATION
- HIGH RESOLUTION GRAPHICS
- COMMUNICATIONS LOCAL OSCILLATORS
  Spread Spectrum
  Base Stations
  Digitally Tuned Receivers
- HIGH-SPEED MODEMS

DESCRIPTION

The DAC650 is a high performance 12-bit digital to analog converter for high frequency waveform generation. It is complete with an internal low drift reference and edge-triggered data latch. The internal segmentation and latching provide for minimal output glitch energy.

The ECL compatibility provides for low digital noise at high update rates. The 50Ω output resistance and low output capacitance simplify transmission line design and filtering at the output. Complementary outputs are offered for increased performance while driving transformers or differential amplifiers.

The DAC650 combines precision thin film and bipolar technology with high speed gallium arsenide to create a high performance, cost effective solution for modern waveform synthesis systems.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

Over full specified temperature range, using the internal +10V reference and rated supplies, unless otherwise noted.

PARAMETER	CONDITIONS	DAC650JL MIN	DAC650JL TYP	DAC650JL MAX	DAC650KL MIN	DAC650KL TYP	DAC650KL MAX	UNITS
TEMPERATURE RANGE								
Specification: DAC650JL, KL[1]	Ambient	0		+70	*		*	°C
θ_{CA}			27			*		°C/W
θ_{JC}			13			*		°C/W
DIGITAL INPUTS								
Logic	12 Parallel Input Lines			ECL Compatible				
Resolution				12			*	Bits
ECL Logic Input Levels[2]: V_{IL}	Logic "0"	–1.475	–1.8	–2	*	*	*	V
I_{IL}			1.0	10		*	*	µA
V_{IH}	Logic "1"	–1.115	–0.8	–0.6	*	*	*	V
I_{IH}			1.0	10		*	*	µA
Logic Threshold Voltage		–1.2	–1.3	–1.4	*	*	*	V
DIGITAL TIMING								
Input Data Rate		DC		500	*		*	MHz
CLK Pulse Width Low		1.0			*			ns
Set-Up Time		2.0	1.8		*	*		ns
Hold Time (Referred to CLK)		–500	–600		*	*		ps
Propagation Delay			1.5			*		ns
ANALOG OUTPUT								
Bipolar Output Current	$R_L = 0\Omega$		±20			*		mA
Bipolar Output Voltage	$R_L = \infty$		±1.0			*		V
Output Resistance	V_{OUT}, $\overline{V_{OUT}}$ to Ground	49	50	51	*	*	*	Ω
Output Resistance Drift			50			*		ppm/°C
Output Capacitance			5			*		pF
TRANSFER CHARACTERISTICS								
Integral Linearity Error	Best Fit Straight Line		±0.018	±0.036		±0.012	±0.024	%FSR
Differential Linearity Error	+25°C		±0.018	±0.036		±0.08	±0.024	%FSR
	Over Temperature		±0.018	±0.036		±0.012	±0.024	%FSR
Monotonicity			Typical			Guaranteed		
Bipolar Gain Error	Output Voltage, $R_L = \infty$		±0.5	±1.0		±0.5	±1.0	%FSR
Bipolar Offset Error	Output Voltage, $R_L = \infty$		±0.5	±1.0		±0.25	±0.5	%FSR
TIME DOMAIN PERFORMANCE								
Glitch Energy	Major Carry		20			*		pV-s
Output Rise Time	10% to 90%		300			*		ps
Output Fall Time	90% to 10%		350			*		ps
Settling Time[3]: ±0.1%FSR	Major Carry, 1LSB Change		2.0			*		ns
REFERENCES								
V_{BB} Input Range (Pin 1)		–1.4	–1.3	–1.2	*	*	*	V
$V_{BB\ INT}$ Reference (Pin 68)		–1.4	–1.3	–1.2	*	*	*	V
$V_{BB\ EXT}$ Tracking Reference (Pin 67)	$ECL_{HI\ IN} = -0.8V$, $ECL_{LO\ IN} = -1.8V$	–1.4	–1.3	–1.2	*	*	*	V
Internal Reference Voltage (Ref Out)		9.95	10	10.05	*	*	*	V
Ref in Resistance			4950			*		Ω
Ref in Operating Voltage Range		4.5	10.0	11.0	*	*	*	V
DYNAMIC PERFORMANCE								
Spurious Free Dynamic Range[4]								
f_O = 1MHz, f_{CLK} = 100MHz	+25°C, Span = DC to $f_{CLK}/2$	65	68		68	70		dBc[5]
f_O = 10MHz, f_{CLK} = 100MHz	+25°C, Span = DC to $f_{CLK}/2$	59	63		62	65		dBc
f_O = 30MHz, f_{CLK} = 200MHz	+25°C, Span = DC to $f_{CLK}/2$	50	52		53	56		dBc
f_O = 80MHz, f_{CLK} = 200MHz	+25°C, Span = DC to $f_{CLK}/2$	47	50		50	52		dBc
f_O = 80MHz, f_{CLK} = 500MHz	+25°C, Span = DC to 150MHz	49	55		52	58		dBc
f_O = 100MHz, f_{CLK} = 500MHz	+25°C, Span = 50MHz to 150MHz	51	56		54	59		dBc
Output Noise	Full Scale Sine Wave Output		1.0			*		µV/√Hz
POWER SUPPLIES								
Supply Voltages: $+V_{CC}$	Operating, T_{MIN} to T_{MAX}	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–15.75	–15	–14.25	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD2}$		–5.46	–5.2	–4.94	*	*	*	V
Power Supply Rejection	All Supplies, ±5% Change		0.05	0.08		*	*	%/%
Supply Currents: $+I_{CC}$	Operating		10	13		*	*	mA
$-I_{CC}$			–47	–50		*	*	mA
$+I_{DD1}$			53	57		*	*	mA
$-I_{DD2}$			–191	–245		*	*	mA
Power Consumption	Operating		2.0	2.6		*	*	W

NOTE: (1) Extended temperature range devices are available, inquire. (2) V_{BBIN} (Pin 1) connected to $V_{BB\ INT}$ (Pin 68). (3) Settling time is influenced by load due to fast edge speeds. Use good transmission line techniques for best results. (4) Spurious Free Dynamic Range includes both harmonic and non-harmonic related spurs in the bandwidth indicated. (5) dBc is "dB referred to the fundamental amplitude."

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE (AMBIENT)
DAC650JL, KL	68-Pin Ceramic, Gullwing Leads	0°C to +70°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC650JL, KL	68-Pin Ceramic Gullwing	256

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
Logic Input	+0.5V to –5.5V
Case Temperature	–40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PIN DEFINITIONS

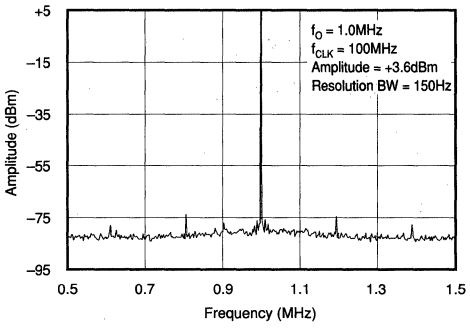
PIN NO	DESIGNATION	DESCRIPTION	PIN NO	DESIGNATION	DESCRIPTION
1	V_{BB}	Sets Logic Threshold for Bits 1-12	35	AGND	Ground for Analog Output Current
2	Bit 1	MSB	36	AGND	
3	Bit 2		37	AGND	
4	Bit 3		38	AGND	
5	Bit 4		39	$\overline{V_{OUT}}$	Complementary Output Voltage
6	Bit 5		40	$\overline{V_{OUT}}$	
7	Bit 6		41	$\overline{V_{OUT}}$	
8	Bit 7		42	AGND	
9	Bit 8		43	AGND	
10	Bit 9		44	AGND	
11	Bit 10		45	V_{OUT}	Output Voltage
12	Bit 11		46	V_{OUT}	
13	Bit 12	LSB	47	V_{OUT}	
14	V_{EE}	Logic Power (–5.2V Nominal)(1)	48	AGND	
15	V_{EE}		49	AGND	
16	CLK	Clock	50	AGND	
17	CLK_{NOT}	Not Clock	51	AGND	
18	DNC	Do Not Connect	52	–15V	–15V Supply
19	V_{EE}		53	–15V	
20	V_{EE}		54	PWR GND	Ground for Analog Supplies
21	V_{EE}		55	+5V	+5V Supply
22	V_{EE}		56	+5V	+5V Supply
23	V_{EE}		57	V_{OS} ADJ	Offset Adjust
24	V_{EE}		58	PWR GND	Ground for Analog Supplies
25	V_{EE}		59	Ref_{ADJ}	Reference Out Adjust
26	V_{EE}		60	Ref_{OUT}	Reference Out (+10V, Buffered)
27	DGND	Ground for Logic	61	Ref_{IN}	Reference In (4.950kΩ)
28	DGND		62	+15V	+15V Supply
29	DGND		63	PWR GND	Ground for Analog Supplies
30	DGND		64	–5.2V Analog	Analog Power (–5.2V Nominal)(1)
31	DGND		65	ECL LO_{IN}	External ECL LOW input (optional)
32	DGND		66	ECL HI_{IN}	External ECL HI input (optional)
33	DGND		67	V_{BBEXT}	The buffered mean of LO_{EXT} and HI_{EXT}
34	DGND		68	V_{BBINT}	Internally generated –1.3V reference

NOTE: (1) Both the –5.2V Logic and –5.2V analog pins should be powered from a common supply.

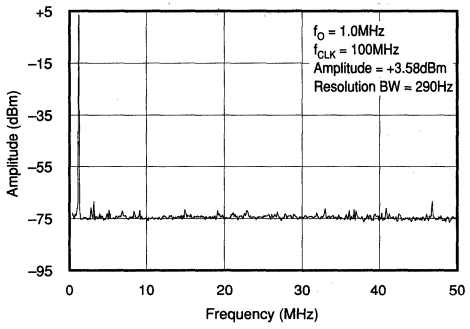
TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

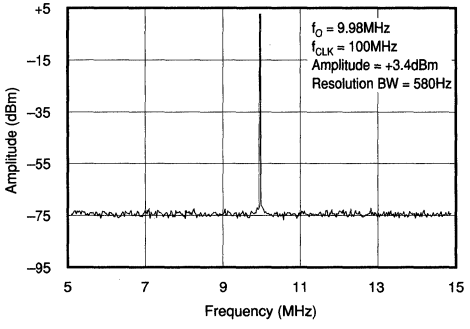
OUTPUT SPECTRUM



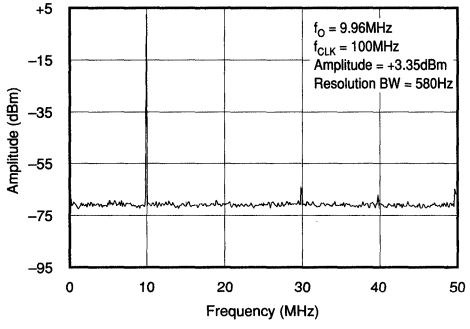
OUTPUT SPECTRUM



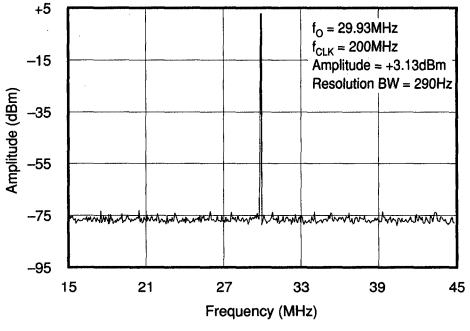
OUTPUT SPECTRUM



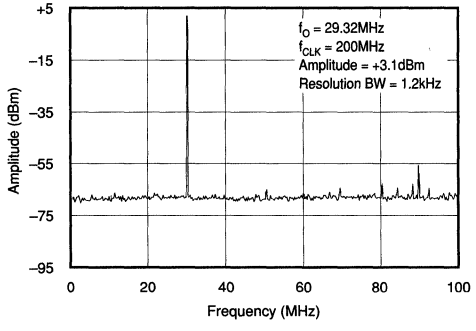
OUTPUT SPECTRUM



OUTPUT SPECTRUM

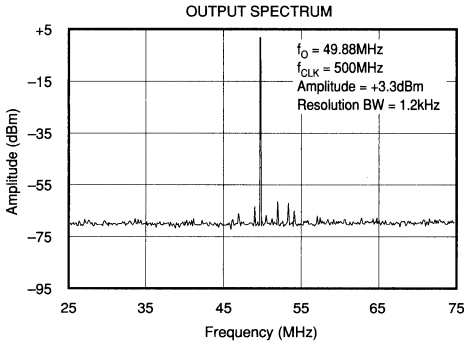


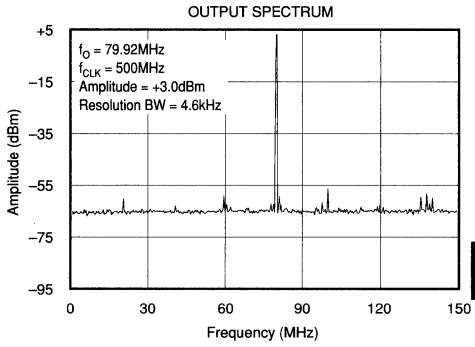
OUTPUT SPECTRUM

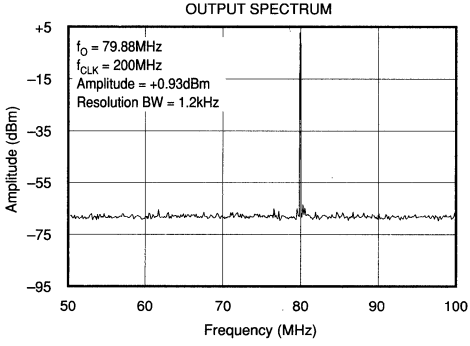


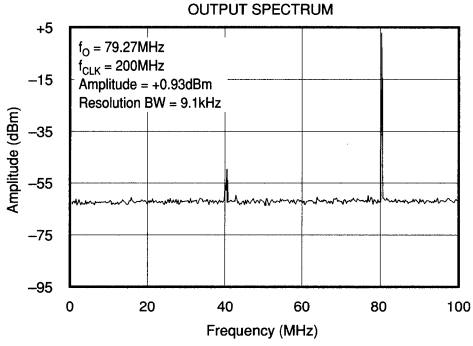
TYPICAL PERFORMANCE CURVES (CONT)

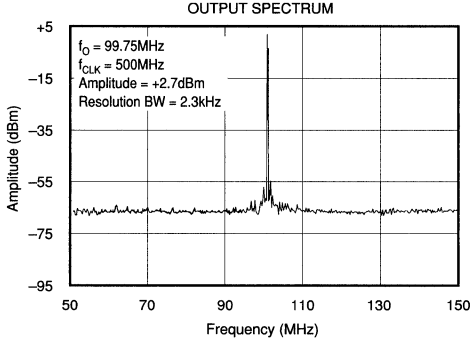
T_A = +25°C unless otherwise noted.







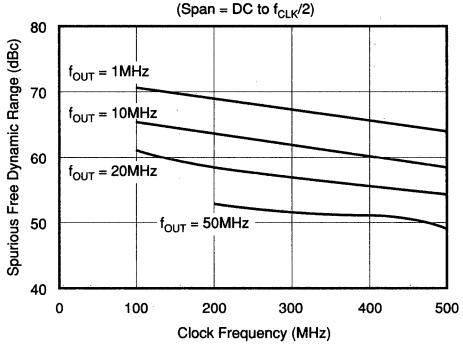




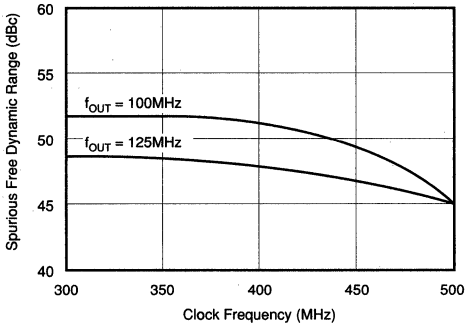
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C unless otherwise noted.

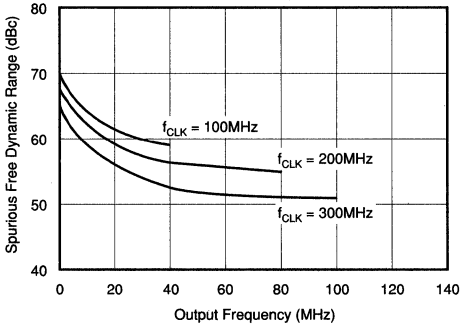
SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY
(Span = DC to $f_{CLK}/2$)



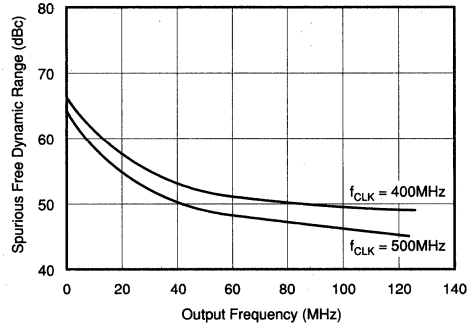
SPURIOUS FREE DYNAMIC RANGE
vs CLOCK FREQUENCY
(Span = DC to 200MHz)



SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY
(Span = DC to $f_{CLK}/2$)



SPURIOUS FREE DYNAMIC RANGE
vs OUTPUT FREQUENCY
(Span = DC to 200MHz)



TECHNOLOGY OVERVIEW

The DAC650 uses a unique design approach to achieve very fast settling time and high resolution. This mixed-technology design uses two active chips: one gallium arsenide and the other silicon.

The GaAs MESFET die is used for those circuits which determine speed. This includes the latches, data decoders, and current switches. A silicon die with thin film is used for those circuits which determine accuracy, such as the precision references and current sources. The precision R-2R resistor ladders are laser trimmed to further increase the accuracy of the DAC650. A block diagram of the DAC650 is shown in Figure 1.

THEORY OF OPERATION

The DAC650 employs a familiar architecture where input bits switch on the appropriate current sources. Bits 1-3 are decoded into 7 segments before the first set of latches. A similar delay is given for the 9 least significant bits to minimize data skew. The edge triggered master-slave latches are driven by an internal clock buffer. This buffer placement has matched the clock lines to each of the 32 latches, thus minimizing output glitch energy.

There are 7 current sources for bits 1 to 3. Current sources for bits 4-8 are scaled down in binary fashion. These current sources are switched directly to the output of the R-2R ladder. Bits 9-12 are fed to the laser trimmed R-2R ladder for proper scale-down. The segmentation further minimizes output glitch which can cause spectral degradation.

The output current sees 50Ω of output impedance from the equivalent resistance of a R-2R ladder (100Ω) in parallel with 100Ω (Figure 1). With all of the current sources off, the output voltage is at +1V. With all current sources on (–40mA), the output voltage is at –1V. There is also a complementary $\overline{V_{OUT}}$ output that allows for a differential output signals. The full scale complementary outputs (V_{OUT} and $\overline{V_{OUT}}$) can be simply modeled as ±20mA in parallel with 50Ω. This gives an output swing of 1Vp-p with an external 50Ω load.

REFERENCE/GAIN ADJUSTMENT

A precision +10V reference is included in the DAC650. A 50Ω resistor should be connected between REF_{IN} and REF_{OUT} for the specified unadjusted gain. This internal reference has been laser trimmed to minimize offset and gain drift. Alternatively, an external reference may be used. Multiple DACs may be run from one master reference by connecting a 50Ω resistor from each REF_{IN} to the master REF_{OUT}. A 100Ω potentiometer may be used in place of the 50Ω resistor in order to provide a ±1% gain adjustment range (Figure 2).

A wider adjustment range of ±20% may be achieved by connecting a 10kΩ potentiometer from REF_{OUT} to ground, with the wiper connected to the REF_{ADJ} pin. Adjusting the output to more than 40mA full scale may degrade high frequency performance and reliability due to higher current densities and operating temperature. Alternatively, lower full scale currents will affect operation because there is less current available to charge internal and external capacitances.

It should be noted that the gain adjust techniques mentioned above affect the current output and thus the voltage output from the DAC650. The voltage output will also be affected by an external load acting in parallel with the 50Ω output impedance.

OFFSET ADJUST

The offset may be adjusted by connecting a potentiometer between the +5V supply and ground with the wiper connected to the offset adjust pin. The voltage on this pin with no connection is about 2V, with an equivalent impedance of 1.6kΩ. A 10kΩ potentiometer will give the necessary adjustment range. The full scale range of the DAC output may be offset so it is not symmetrical around zero, but the full scale range must also be adjusted so that the output swing does not exceed ±1V. Connecting the offset adjust pin to ground gives a unipolar output of 0 to –2V (with no load) or 0 to –1V (with a 50Ω load). This also reduces the current requirements for the +5V supply by 20mA.

DIGITAL INPUTS, LOGIC THRESHOLDS, and TERMINATION

The input logic levels and clock levels are ECL compatible. The data inputs are single ended ECL and the clock input is differential.

The internal impedance of the data and clock inputs is a high impedance (FET gate), and is clamped to the digital supply and ground to protect against ESD damage. ESD precautions should still be used when handling the DAC650.

The inputs will most likely be driven by high-speed ECL gate outputs. These outputs should be terminated using standard high-speed transmission line techniques. Consult an ECL handbook for proper methods of termination.

Termination resistors should not be connected to the analog ground plane close to the DAC650. The fast changing digital bit currents will cause noise in the analog ground plane under this layout scheme. These fast changing digital currents should be steered away from the sensitive DAC650 analog ground plane. For speeds of up to 256MHz, series termination with 47Ω resistors will be adequate (Figure 3). This termination technique will greatly lessen the issue of termination currents coupling into the analog ground plane. Above 256MHz, parallel termination of the transmission line at the package pin may be required for clean digital input.

The input data threshold level is set by connecting the appropriate voltage (–1.2V to –1.4V) to pin 1. The actual level may be provided 3 ways:

(1) The user connects the DAC650's internal –1.3V threshold reference directly to pin 1. This simple connection provides excellent noise margins for ECL levels.

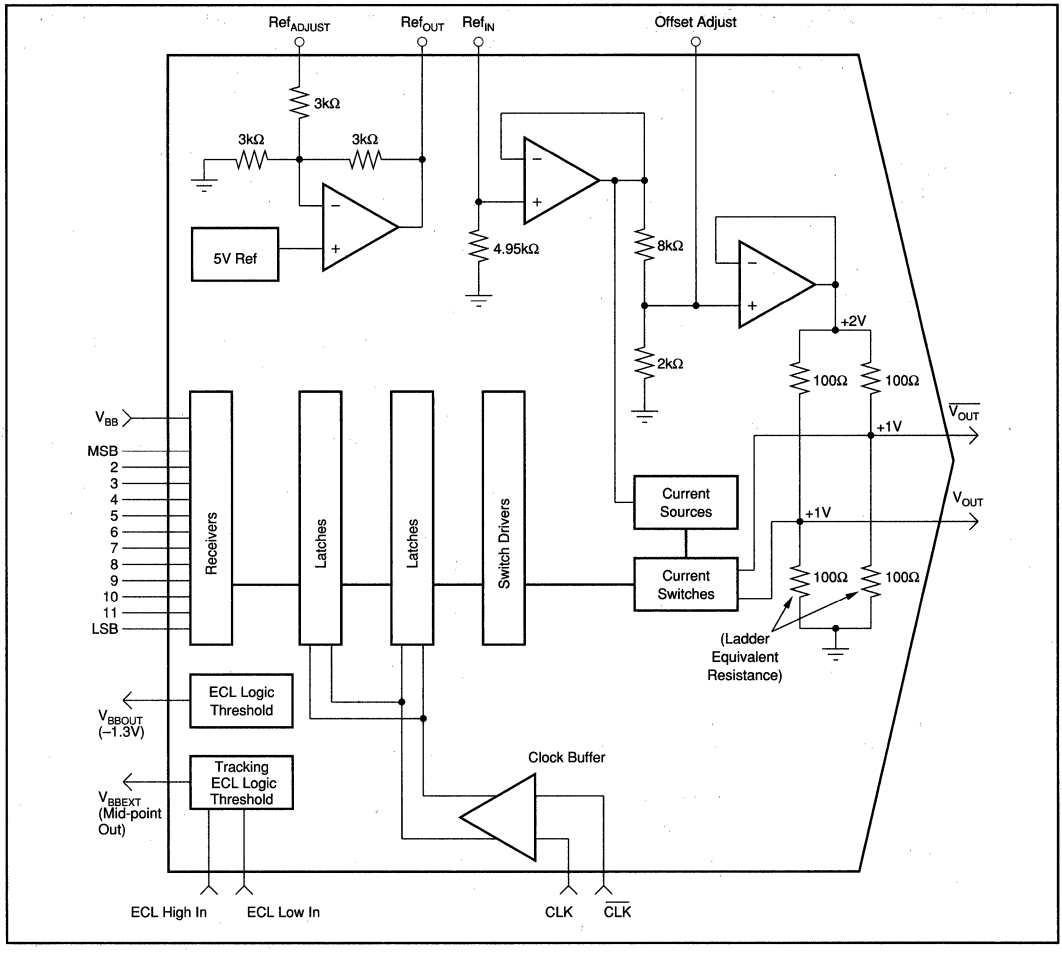


FIGURE 1. Functional Block Diagram of the DAC650.

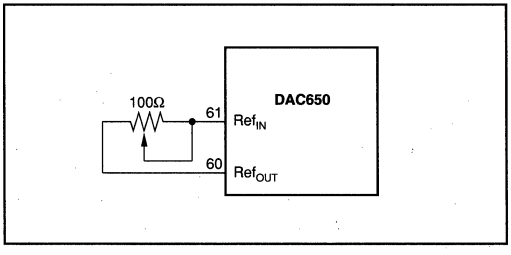


FIGURE 2. Using a Potentiometer for ±1% Gain Adjust.

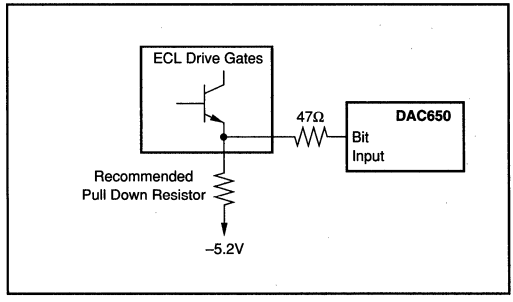


FIGURE 3. Series Bit Termination.

(2) An external V_{BB} system reference is applied to pin 1. This technique may allow data threshold levels to track the system over supply and temperature variations.

(3) The internal tracking ECL threshold reference (pin 67) is applied to pin 1. The output of the tracking ECL threshold reference is simply the average of two externally applied levels. These levels are a system logic low (pin 65) and system logic high (pin 66). This technique may provide increased noise margin for systems with levels slightly different from ECL. Leave pins 65-67 open if this option is not used.

TIMING

The DAC650 has an internal edge triggered latch. The output changes on the positive edge of CLK. This master-slave latching will assure that the 12 bits will arrive at the bit switches with a minimum of data skew. Data must have adequate setup and hold time for proper operation (refer to Figure 4). Note that the Hold time is negative. Therefore the data may change before the rising edge of clock and still be valid.

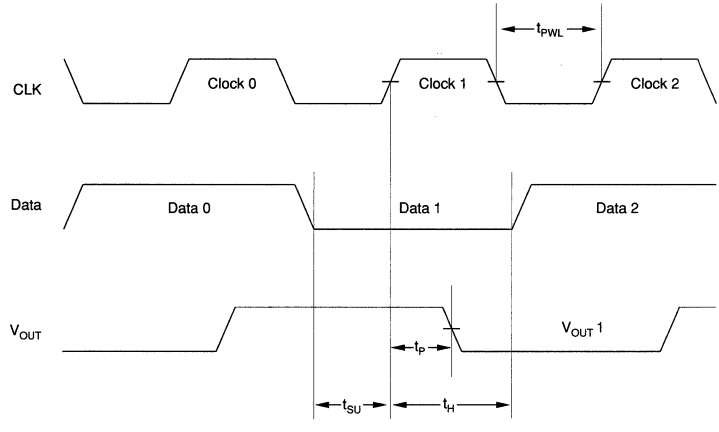
The DAC650 has a differential ECL clock input. This clock input can also be driven by a single-ended clock if desired by tying the $\overline{CLK}$ input to an external voltage of –1.3V. Using a true differential clock provides much improved digital feedthrough immunity, however.

DATA IN/VOUT CORRESPONDENCE

The each full scale output of the DAC650 may be modeled as either ±20mA current source in parallel with 50Ω or a ±1V voltage source in series with 50Ω. The nominal current and voltage bit weights are given in Table I and the input code vs output voltage relationships are given in Table II.

Transmission line techniques at the output are also recommended to minimize ringing and glitching. Ideally, both of the outputs should see the same termination, including any delay between the DAC650 and the load.

Since the outputs V_{OUT} and $\overline{V_{OUT}}$ are equal in magnitude but opposite in sign, they are ideal for driving RF transformers (Figures 5). The primary may be connected between the two outputs. The secondary may be floating or referenced to ground. This results in a 2X signal power and some cancellation of clock feedthrough, glitching, and distortion. Figures 6 and 7 give recommended output amplifiers.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_P	Propagation delay. 50% of CLK to 50% of V_{OUT}.		1.5		ns
t_{SU}	Setup time DATA must remain stable before CLK.	2.0	1.8		ns
t_H	Hold time DATA must remain stable after CLK.	–500	–600		ps
t_{PWL}	CLK pulse width low (50% to 50%).	1.0			ns

FIGURE 4. Timing Diagram for the DAC650.

If only one output is used, the unused output should be terminated identically. If the terminations cannot be identical and the unused output must be unterminated, the termination for the used output should be as close as possible to the DAC650.

LAYOUT AND POWER SUPPLIES

A multilayer PC board with a solid ground and power planes is recommended. An example of a typical circuit configuration is given in Figures 8. The DAC650 has multiple ground pins to minimize pin impedances. All of the ground pins (analog and digital both) should be connected directly to the analog ground plane at the DAC650.

Wide busses for the power paths are recommended as good general practice. There are several internal power supply bypass capacitors, but external bypassing is still recommended. A 10µF tantalum capacitor in parallel with a 0.01µF chip capacitor will be sufficient in most applications.

Pin 64, Analog V_{EE}, should be connected to the same supply as the digital V_{EE} pins (–5.2V).

BIT	VOLTAGE (No External Load)	CURRENT
1	1V	20mA
2	.5V	10mA
3	0.25V	5mA
4	0.125V	2.5mA
5	62.5mV	1.25mA
6	31.25mV	625µA
7	15.625mV	312.5µA
8	7.8125mV	156.25µA
9	3.9063mV	78.125µA
10	1.9531mV	39.06µA
11	976µV	19.53µA
12 (LSB)	488µV	9.76µA

TABLE I. Nominal Bit Weight Values.

INPUT BITS 1 2 3 4 5 6 7 8 9 10 11 12	V_{OUT}	NV_{OUT}
0 0 0 0 0 0 0 0 0 0 0 0	+1.000	–1 + 488µV
0 0 0 0 0 0 0 0 0 0 0 1	+1 – 488µV	–1 + 976µV
0 0 0 0 0 0 0 0 0 0 1 0	+1 – 976µV	–1 + 1.464mV
•		
•		
•		
•		
0 1 0 0 0 0 0 0 0 0 0 0	0.50	–0.50 + 488µV
1 0 0 0 0 0 0 0 0 0 0 0	0.000	+488µV
1 1 1 1 1 1 1 1 1 1 1 1	–1 + 488µV	+1.000

TABLE II. Input Code vs Output Voltage Relationships.

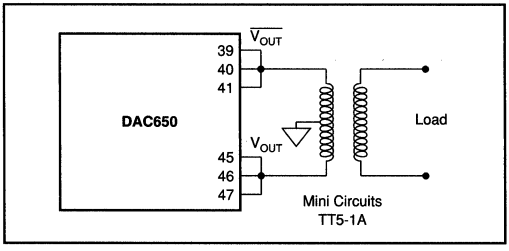


FIGURE 5. Using an RF Transformer at the Output of the DAC650. Filtering the Outputs Before the Transformer Improves the Performance in Some Applications.

MAXIMIZING PERFORMANCE

The DAC650 has been designed to give a very clean analog output with minimal noise, overshoot, and ringing. In addition to optimizing the layout and ground of the DAC650, there are other important issues to consider when optimizing the performance of this DAC in various AC applications.

The DAC650 includes an internal 50Ω output impedance to simplify output interfacing to a 50Ω load. Because some loads may be a complex impedance, care must be taken to match the output impedance with the load. Mismatching of impedances can cause reflections which will affect the measured AC performance parameters such as settling time, harmonic distortion, rise/fall times, etc. Often complex impedances can be matched by placing a variable 3 to 10pF capacitor at the output of the DAC to ground. Also, probing the output can present a complex impedance.

The typical performance curves of Spurious Free Dynamic Range vs various combinations of clock rate and/or input frequency should give a general idea of the spectral performance of the DAC under system specific clock and output frequencies. We have defined Spurious Free Dynamic Range as any harmonic or non-harmonic spurs in the indicated bandwidth . In phase lock loop applications, the harmonics often fall outside the loop bandwidth of the PLL. In these cases, as well as cases where the output is filtered, Spurious

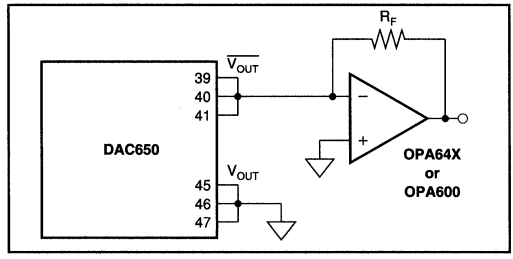


FIGURE 6. A High Speed Single Ended Amplifier at the Output. The Gain is $-R_F/50\Omega$.

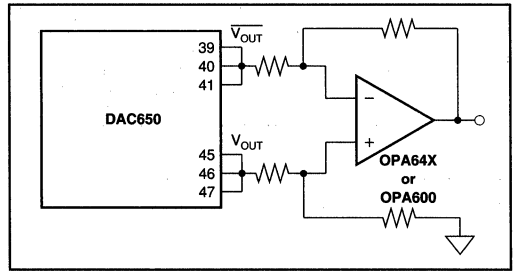


FIGURE 7. A High Speed Differential Amplifier at the Output.

Free Dynamic Range will generally be much better due to the harmonics falling outside the passband. Even with a bandpass filter, updating the DAC at greater than 4 times per cycle will (1) minimize the 2nd and 3rd harmonic magnitudes by having the output slew excessively between any successive clock and (2) will keep the ($f_{CLK} - 2f_O$) spur and other even order spurs from folding back close to the fundamental under the condition $f_{OUT} = 1/3f_{CLK}$ and (3) will keep the ($f_{CLK} - 3f_O$) spur and other spurs from folding back close to the fundamental under the condition $f_{OUT} = 1/4f_{CLK}$. Making use of the high update rate of the DAC650 helps to lessen the problems of harmonics "folding back" into the passband.

EVALUATION BOARD

The high frequency signals used in operating the DAC650 can cause difficult layout problems. It is especially difficult to build a high-performance prototype board using the DAC650. It is recommended that an evaluation fixture be used for prototyping. An evaluation fixture includes a DAC650 soldered to the PC board. Both grades are available for the evaluation fixture.

ORDERING INFORMATION

MODEL	DESCRIPTION
DEM-DAC650J-E	Evaluation Board with DAC650JL Attached
DEM-DAC650K-E	Evaluation Board with DAC650KL Attached
DEM-DAC650 PDS	Data Sheet for DAC650 Evaluation Board

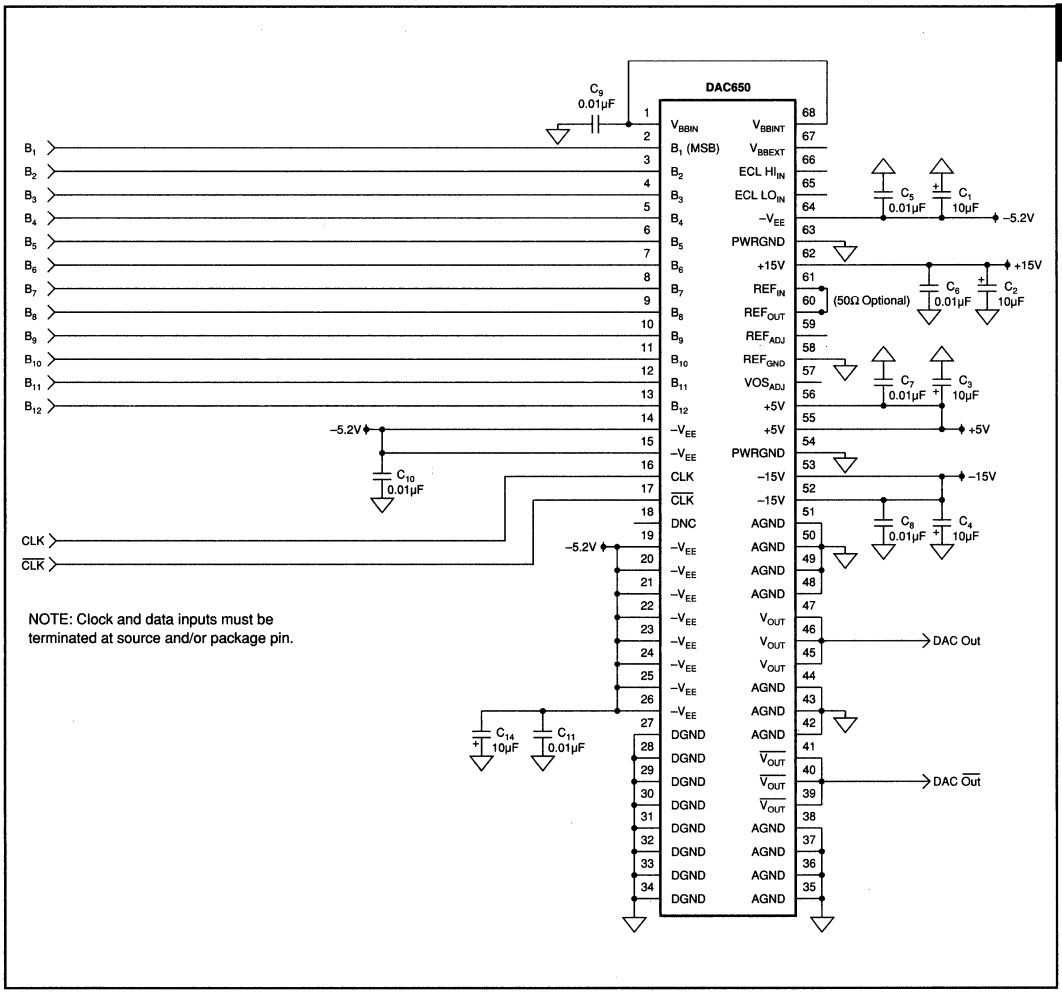


FIGURE 8. Typical DAC650 Connection Diagram.

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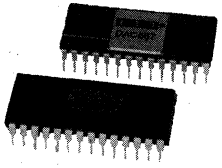


DAC667

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

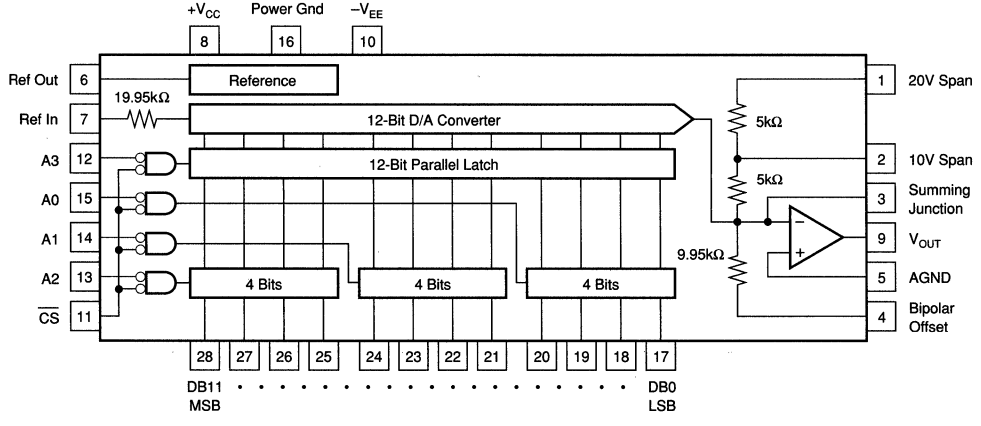
- ±1/2LSB MAX NONLINEARITY OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- MICROCOMPUTER INTERFACE: Double-Buffered Latch
- VOLTAGE OUTPUT: ±10V, ±5V, +10V With ±12V to ±15V Supplies
- LOW POWER DISSIPATION: 345mW typ
- PIN COMPATIBLE WITH AD667

DESCRIPTION

The DAC667 is a complete monolithic integrated circuit microprocessor-compatible 12-bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

A double-buffered latch facilitates microcomputer interfacing to 4-, 8-, 12-, or 16-bit data buses. The input buffer latch holds the 12-bit data until it is transferred to an internal 12-bit D/A converter latch, giving precise timing control over an analog output change.

The DAC667 is specified to ±1/4LSB maximum linearity error (B and K grades) at +25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range. The DAC667 is available in two performance grades and in 28-pin, 0.6" wide plastic and ceramic DIP package types.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted.

PARAMETER	DAC667JP MIN	DAC667JP TYP	DAC667JP MAX	DAC667KP MIN	DAC667KP TYP	DAC667KP MAX	UNITS
DIGITAL INPUTS							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	0		+0.8	*		*	V
I_{IH} (VI_H = 5.5V)		3	10		*	*	µA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3			*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10			*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load, C_F = 0)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = −11.4 to −16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
−11.4 to −16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating	−40		+85	*		*	°C
Storage	−65		+125	*		*	°C

* Same as specification for DAC667JP.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground	0V to +18V
V_{EE} to Power Ground	0V to −18V
Digital Inputs (Pins 11–15, 17–28) to Power Ground	−1V to +7V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span Resistor to Reference Ground	±12V
20V Span Resistor to Reference Ground	±24V
Ref Out, V_{OUT} (Pins 6, 9)	Indefinite Short to Power Ground, Momentary Short To V_{CC}
Power Dissipation	1000mW

TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

All models, T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V.

ELECTRICAL (CONT)

T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted.

PARAMETER	DAC667AH MIN	DAC667AH TYP	DAC667AH MAX	DAC667BH MIN	DAC667BH TYP	DAC667BH MAX	UNITS
DIGITAL INPUT							
Resolution			12			*	Bits
Logic Levels (TTL Compatible, T_{MIN} to T_{MAX})[1]							
V_{IH} (Logic 1)	+2		+5.5	*		*	V
V_{IL} (Logic 0)	+0		+0.8	*		*	V
I_{IH} (V_{IH} = 5.5V)		3	10		*	*	µA
I_{IL} (V_{IL} = 0.8V)		1	5		*	*	µA
ACCURACY							
Linearity Error at +25°C		±1/4	±1/2		±1/8	±1/4	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error at +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_A = T_{MIN} to T_{MAX}		Monotonicity Guaranteed			*		LSB
Gain Error[2]		±0.1	±0.2		*	*	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		*	*	LSB
Bipolar Zero[2]		±0.05	±0.1		*	*	% of FSR
DRIFT							
Differential Linearity		±2			*		ppm of FSR/°C
Gain (Full Scale), T_A = +25°C to T_{MIN} or T_{MAX}		±5	±30		*	±15	ppm of FSR/°C
Unipolar Offset, T_A = +25°C to T_{MIN} or T_{MAX}		±1	±3			*	ppm of FSR/°C
Bipolar Zero, T_A = +25°C to T_{MIN} or T_{MAX}		±5	±10			*	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ || 500pF Load)							
With 10kΩ Feedback		3	4		*	*	µs
With 5kΩ Feedback		2	3		*	*	µs
For LSB Change		2			*		µs
Slew Rate	8			*			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit Current			40			*	mA
REFERENCE OUTPUT	9.9	10	10.1	*	*	*	V
External Current	0.1	1		*	*		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5VDC		5	10		*	*	ppm of FS/%
V_{EE} = –11.4 to –16.5VDC		5	10		*	*	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			*		V
Range[4]	±11.4		±16.5	*		*	V
Supply Current							
+11.4 to +16.5VDC		14	17		*	*	mA
–11.4 to –16.5VDC		9	12		*	*	mA
TEMPERATURE RANGE							
Specification	–25		+85	*		*	°C
Operating	–40		+85	*		*	°C
Storage	–65		+150	*		*	°C

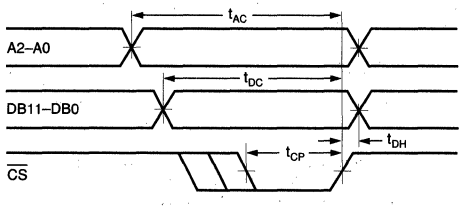
* Same as specification for DAC667AH.

NOTES: (1) The digital input specifications are 100% tested at +25°C and over the full temperature range. (2) Adjustable to zero. (3) FSR means full scale range and is 20V for ±10V range and 10V for the ±5V range. (4) ±10V full scale output can be achieved using ±11.4 supplies.

TIMING DIAGRAMS

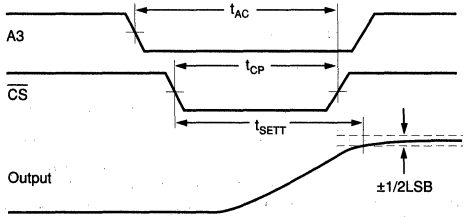
Write Cycle #1

Load first rank from Data Bus; A3 = 1.



Write Cycle #2

Load second rank from first rank; A2, A1, A0 = 1.



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC667JP	28-Pin Plastic DIP	215
DAC667KP	28-Pin Plastic DIP	215
DAC667AH	28LD Side-Brazed Ceramic DIP	149
DAC667BH	28LD Side-Brazed Ceramic DIP	149

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE (°C)	LINEARITY ERROR, max at 25°C	GAIN TC, max (ppm/°C)
DAC667JP	Plastic DIP	0 to +70	±1/2LSB	±30
DAC667KP	Plastic DIP	0 to +70	±1/4LSB	±15
DAC667AH	Ceramic DIP	–25 to +85	±1/2LSB	±30
DAC667BH	Ceramic DIP	–25 to +85	±1/4LSB	±15

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all ones and all zeros). DAC667 linearity error is specified at ±1/4LSB max at +25°C for B and K grades, and ±1/2LSB max for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. All grades of the DAC667 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Gain drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar offset drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar offset drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

Bipolar zero drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar zero drift is expressed in parts per million of full scale range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for FSR output changes of 20V (10kΩ feedback) and 10V (5kΩ feedback), and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

OPERATION

DAC667 is a monolithic integrated-circuit 12-bit D/A converter. It is complete with 12-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface as shown in the front-page diagram.

INTERFACE LOGIC

The bus interface logic of the DAC667 consists of four independently addressable latches in two ranks. The first rank consists of three four-bit input latches which can be loaded directly from a 4-, 8-, 12- or 16-bit microprocessor/microcontroller bus. These latches hold data temporarily while a complete 12-bit word is assembled before loading it into the second rank of latches. This double buffered organization prevents the generation of spurious analog output values while the complete word is being assembled.

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When the control signals return to logic 1, the data is latched. A truth table for the control signals is presented in Table I.

$\overline{CS}$	A3	A2	A1	A0	OPERATION
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable Four LSBs of First Rank
0	1	1	0	1	Enable Four Middle Bits of First Rank
0	1	0	1	1	Enable Four MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent
X = Don't care.					

TABLE I. DAC667 Truth Table.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the timing specifications on page 2 are met.

LOGIC INPUT COMPATIBILITY

The DAC667 digital inputs are TTL compatible (1.4V switching level) with a low leakage, high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

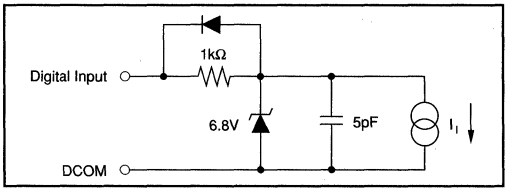


FIGURE 1. Equivalent Digital Input Circuit.

DAC667 data inputs will float to logic 1 and control inputs will float to logic 0 if left open. It is recommended that any unused inputs be connected to power common to improve noise immunity.

INPUT CODING

The DAC667 accepts positive-true binary input codes.

Input coding for unipolar analog output is straight binary (USB), where all zeros (000_{HEX}) on the data inputs gives a zero analog output and all ones (FFF_{HEX}) gives an analog output 1LSB below full scale.

Input coding for bipolar analog outputs is bipolar offset binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

The DAC667 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

INTERNAL/EXTERNAL REFERENCE USE

DAC667 contains a +10V reference which is trimmed to typically ±0.2% and tested and guaranteed to ±1%. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 50Ω. A trim potentiometer with a nominal value of 100Ω can be used to provide adjustment to zero gain error. If an external 10.000V reference is used, it may be necessary to increase the trim range slightly.

The reference output may be used to drive external loads, sourcing up to 5mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the converter will vary.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. The DAC667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range, a CMOS multiplying D/A is a better choice.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of offset and gain adjustments to a unipolar- and a bipolar-connected DAC667. Offset should be adjusted first to avoid interaction of adjustments.

Offset Adjustment

For unipolar (USB) operation, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) operation, apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. See Table II for calibration values and codes.

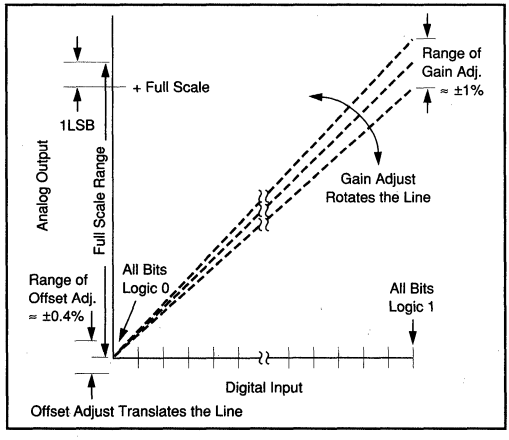


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

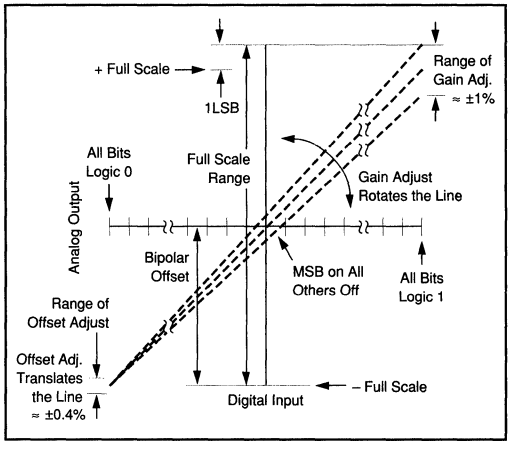


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Gain Adjustment

For either unipolar or bipolar operation, apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for calibration values.

DIGITAL INPUT	ANALOG OUTPUT				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FFF_{HEX}	+4.9987V	+9.9976V	+2.4987V	+4.9976V	+9.9951V
800_{HEX}	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+2.4987V	+4.9976V	–0.0013V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	0.0000V	–2.5000V	–5.0000V	–10.0000V
1LSB	1.22mV	2.44mV	1.22mV	2.44mV	4.88mV

TABLE II. Calibration Values.

SETTLING TIME PERFORMANCE

The switches, reference and output amplifier of the DAC667 are designed for optimum settling time performance (Figure 4). Figure 4a shows the full scale range step response, V_{OUT} –10V to +10V to –10V, for data input 000_{HEX} to FFF_{HEX} to 000_{HEX}. Figure 4b shows the settling time response at plus full scale (+10V) for an output transition from –10V to +10V. Figure 4c shows the settling time response at minus full scale (–10V) for an output transition from +10V to –10V. Figure 4d shows the major carry glitch response for input code transitions $7FF_{HEX}$ to 800_{HEX} and for 800_{HEX} to $7FF_{HEX}$.

Unlike the Analog Devices AD667, the Burr-Brown DAC667 does not require an external capacitor (C_f = 20pF) across R_{SPAN} to eliminate overshoot. Using the 20pF with the Burr-

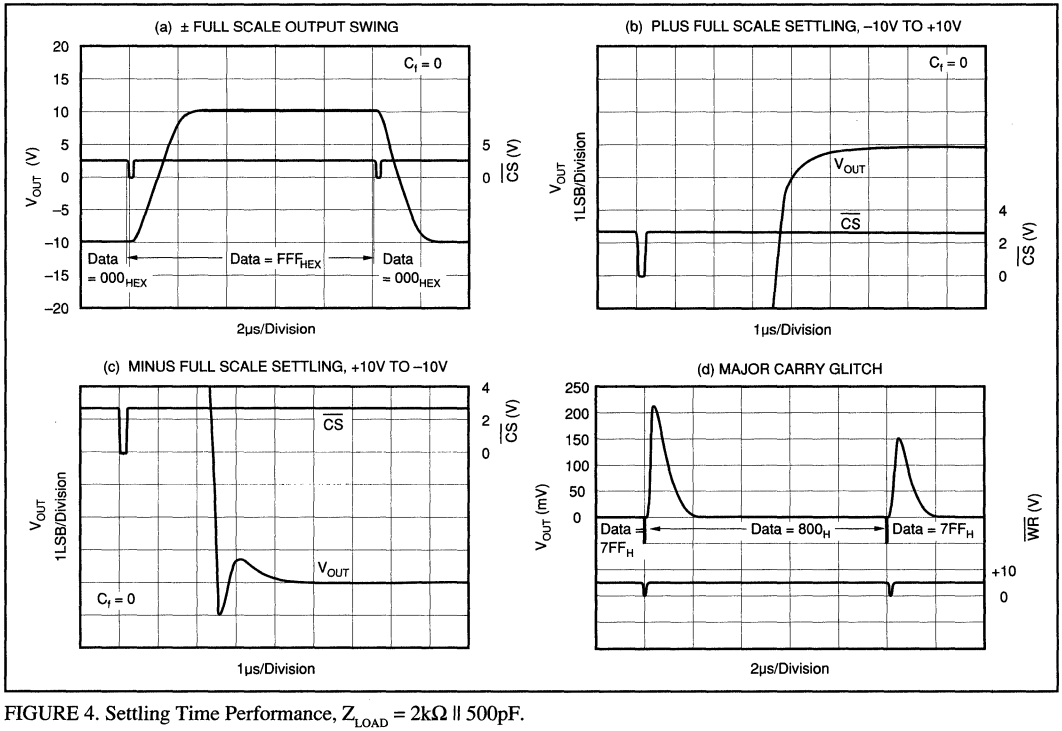


FIGURE 4. Settling Time Performance, Z_{LOAD} = 2kΩ || 500pF.

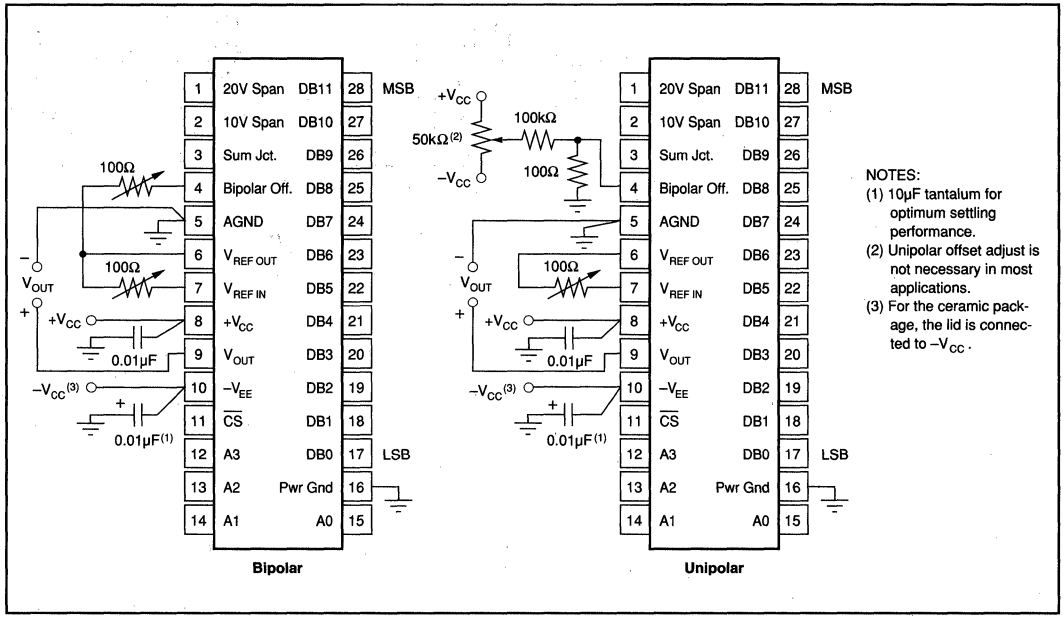


FIGURE 5. Power Supply, Gain and Offset Connections.

Brown DAC667 increases the settling time about one microsecond. The DAC667 settling time is specified at 7µs maximum. The AD667 is specified at 4µs maximum.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the metal lid of the ceramic-packaged DAC667 is connected to $-V_{EE}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Best settling performance occurs using a 1µF to 10µF tantalum capacitor at $-V_{EE}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{EE}$ as well as at $+V_{CC}$. The capacitors should be located close to the DAC667 package.

DAC667 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both power ground (pin 16) and analog ground (AGND, pin 5) be connected directly to a ground plane under the package. If a ground plane is not used, connect the AGND and power ground pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\,OUT}$ is the AGND pin, it is also important to connect the load directly to the AGND pin.

The change in current in the AGND pin due to an input data word change from 000_{HEX} to FFF_{HEX} is only 1mA.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

The DAC667 output amplifier can provide ±10V output swing while operating on ±11.4V supplies. The Analog Devices AD667 requires a minimum of ±12.5V to achieve an output swing of ±10V.

Internal scaling resistors provided in the DAC667 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. Refer to Figures 6, 7 and 8. Connections for various output ranges are shown in Table III.

The internal feedback resistors (5kΩ) and the bipolar offset resistor (9.95kΩ) are trimmed to an absolute tolerance of about ±10%.

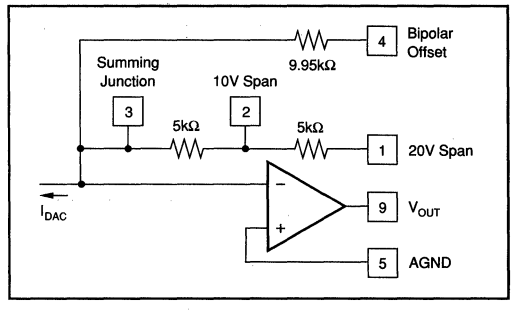


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 9 TO	CONNECT PIN 1 TO	CONNECT PIN 2 TO	CONNECT PIN 4 TO
±10V	Offset Binary	1	9	NC	6 (Through 50Ω fixed or 100Ω trim resistor.)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (Through 50Ω fixed or 100Ω trim resistor.)
±2.5V	Offset Binary	2	3	9	6 (Through 50Ω fixed or 100Ω trim resistor.)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (Or optional trim. See Figure 7.)
0 to +5V	Straight Binary	2	3	9	5 (Or optional trim. See Figure 7.)

TABLE III. Output Voltage Range Connections.

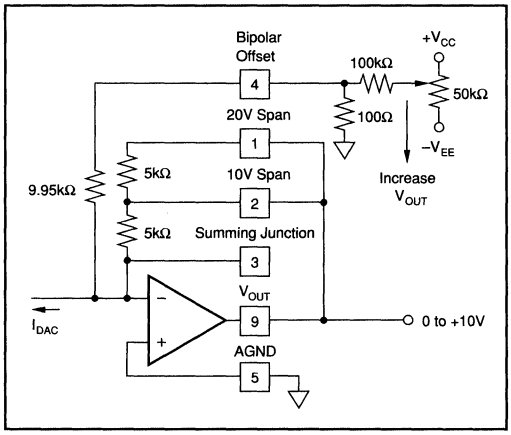


FIGURE 7. 0 to +10V Unipolar Voltage Output.

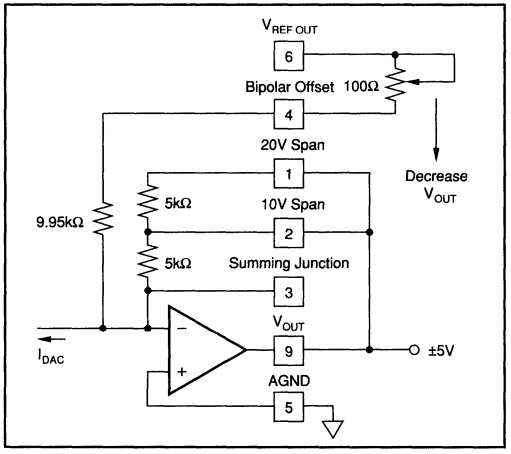


FIGURE 8. ±5V Bipolar Voltage Output.

MICROCOMPUTER BUS INTERFACING

8-BIT BUS INTERFACE

The DAC667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats. Data formats for 8-bit buses are illustrated in Figure 9.

DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4
DB3	DB2	DB1	DB0	X	X	X	X

(a) Left-Justified

X	X	X	X	DB11	DB10	DB9	DB8
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

(b) Right-Justified

FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

Whenever a 12-bit D/A is loaded from an 8-bit bus, two bytes are required. If the software program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the four most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

Figure 10 shows an addressing scheme for use with a DAC-667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the DAC667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

Right-justified data can also be accommodated as shown in Figure 11. The DAC667 still occupies two adjacent locations in the processor's memory map. Location X01 loads the eight LSBs and location X10 loads the four MSBs and updates the output.

12- AND 16-BIT BUS INTERFACES

For operation with 12- and 16-bit buses, all four address lines (A0 through A3) are connected to logic 0, and the latch is enabled by $\overline{CS}$ asserted low. The DAC667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the DAC667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering. See Figure 12.

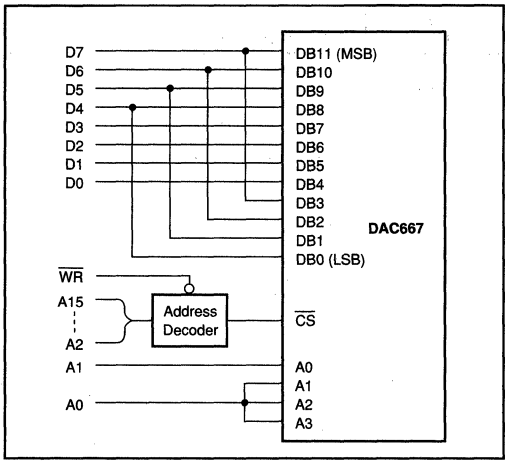


FIGURE 10. Left-Justified 8-Bit Bus Interface.

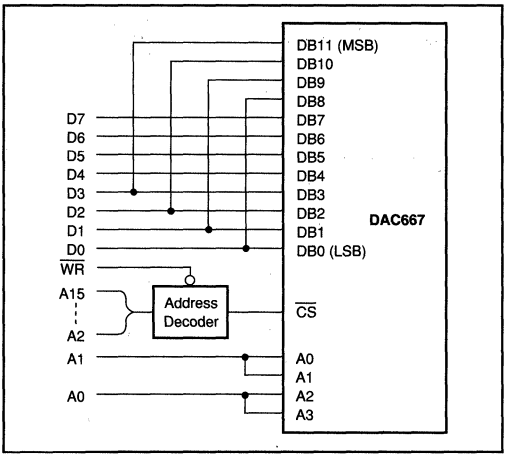


FIGURE 11. Right-Justified 8-Bit Bus Interface.

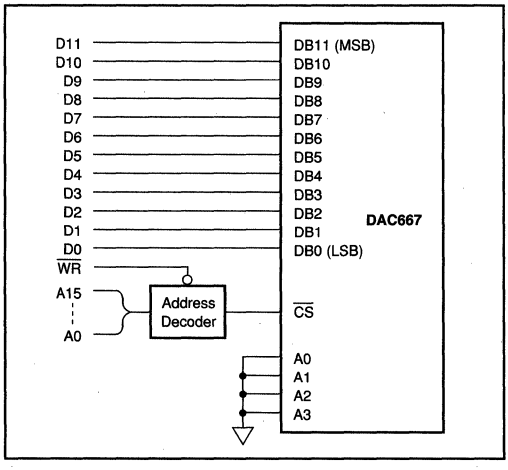
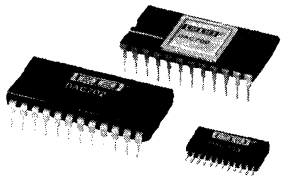


FIGURE 12. Connections for 12- and 16-Bit Bus Interface.

BURR-BROWN®



DAC700/702
DAC701/703

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

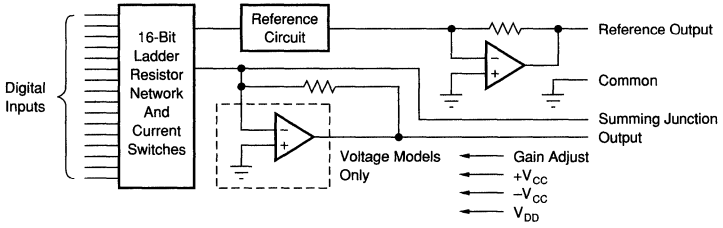
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.0015% of FSR max
  Differential Linearity Error ±0.003% of FSR max
- MONOTONIC (at 15 bits) OVER FULL SPECIFICATION TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- DUAL-IN-LINE PLASTIC AND HERMETIC CERAMIC AND SOIC

DESCRIPTION

The DAC70X family comprise of complete 16-bit digital-to-analog converters that includes a precision buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range, but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to –2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC700 and DAC702 are also pin-compatible with the DAC70 model family. In addition, the DAC703 is offered in a 24-pin SOIC package for surface mount applications.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

PARAMETER	DAC702/703J			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT													
DIGITAL INPUT													
Resolution			16			*			*			*	Bits
Digital Inputs [1]													
V_{IH}	+2.4		$+V_{CC}$	*		*	*		*	*		*	V
V_{IL}	–1.0		+0.8	*		*	*		*	*		*	V
I_{IH}, V_I = +2.7V			+40			*			*			*	µA
I_{IL}, V_I = +0.4V		–0.35	–0.5		*	*		*	*		*	*	mA
TRANSFER CHARACTERISTICS													
ACCURACY[2]													
Linearity Error[4]		±0.0015	±0.006		*	±0.003		*	*		±0.00075	±0.0015	% of FSR[3]
Differential Linearity Error[4]		±0.003	±0.012		*	±0.006		*	*		±0.0015	±0.003	% of FSR
Differential Linearity Error at Bipolar Zero (DAC702/703)[4]					±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR
Gain Error[5]		±0.07	±0.30		*	±0.15		±0.05	±0.10		*	*	%
Zero Error[5, 6]		±0.05	±0.10		*	*		*	*		*	*	% of FSR
Monotonicity Over Spec. Temp Range	13			14			*			15			Bits
DRIFT (over specification temperature range)													
Total Error Over Temperature Range (all models)[7]		±0.08			*	±0.15		±0.05	±0.10		*	*	% of FSR
Total Full Scale Drift:													
DAC700/701		±10			*	±30		±8.5	±18		±6	±13	ppm of FSR/°C
DAC702/703		±10			*	±25		±7	±15		*	*	ppm of FSR/°C
Gain Drift (all models)		±10	±30		*	±25		±7	±15		±5	±10	ppm/°C
Zero Drift:													
DAC700/701					±2.5	±5		±1.5	±3		*	*	ppm of FSR/°C
DAC702/703		±5	±15		*	±12		±4	±10		±2.5	±5	ppm of FSR/°C
Differential Linearity Over Temp.[4]			±0.012			+0.009, –0.006			*			+0.006, –0.003	% of FSR
Linearity Error Over Temp.[4]			±0.012			±0.006			*			±0.003	% of FSR
SETTLING TIME (to ±0.003% of FSR)[8]													
DAC701/703 (V_{OUT} Models)													
Full Scale Step, 2kΩ Load		4			*	8		*	*		*	*	µs
1LSB Step at Worst-Case Code[9]		2.5			*			*			*		µs
Slew Rate		10			*			*			*		V/µs
DAC700/702 (I_{OUT} Models)													
Full Scale Step (2mA), 10 to 100Ω Load		350			*	1000		*	*		*	*	ns
1kΩ Load		1			*	3		*	*		*	*	µs
OUTPUT													
VOLTAGE OUTPUT MODELS													
DAC701 (CSB Code)					0 to +10			*					V
DAC703 (COB Code)		±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance		0.15			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		
CURRENT OUTPUT MODELS													
DAC700 (CSB Code)[10]					0 to –2			*			*		mA
Output Impedance[10]					4			*			*		kΩ
DAC702 (COB Code)[10]		±1			*			*			*		mA
Output Impedance[10]		2.45			*			*			*		kΩ
Compliance Voltage		±2.5			*			*			*		V

ELECTRICAL (CONT)

PARAMETER	DAC702/703J MIN	DAC702/703J TYP	DAC702/703J MAX	DAC700/701/702/703K MIN	DAC700/701/702/703K TYP	DAC700/701/702/703K MAX	DAC700/701/702/703B, S MIN	DAC700/701/702/703B, S TYP	DAC700/701/702/703B, S MAX	DAC700/701/702/703L, C MIN	DAC700/701/702/703L, C TYP	DAC700/701/702/703L, C MAX	UNITS
REFERENCE VOLTAGE													
Voltage		+6.3		+6.0	+6.3	+6.6	+6.24	+6.3	+6.36	*	*	*	V
Source Current Available for External Loads		+2.5		+1.5	*		*	*		*	*		mA
Temperature Coefficient		±10			*	±25		*	±15		*	*	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	13.5	15	16.5	*	*	*	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+16.5	*	*	*	*	*	*	*	*	*	V
Current (No Load):													
DAC700/702													
(I_{OUT} Models)													
$+V_{CC}$		+10	+25		*	*		*	*		*	*	mA
$-V_{CC}$		−13	−25		*	*		*	*		*	*	mA
V_{DD}		+4	+8		*	*		*	*		*	*	mA
DAC701/703													
(V_{OUT} Models)													
$+V_{CC}$		+16	+30		*	*		*	*		*	*	mA
$-V_{CC}$		−18	−30		*	*		*	*		*	*	mA
V_{DD}		+4	+8		*	*		*	*		*	*	mA
Power Dissipation:													
(V_{DD} = +5.0V)[11]													
DAC700/702		365			*	790		*	630		*	*	mW
DAC701/703		530			*	940		*	780		*	*	mW
Power Supply Rejection:													
$+V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*		*	*	% of FSR/%V_{DD}
TEMPERATURE RANGE													
Specification:													
B, C Grades							−25		+85	*		*	°C
S Grades							−55		+125				°C
J, K, L Grades	0		+70	*		*				0		+70	°C
Storage: Ceramic				−60		+150	*		*	*		*	°C
Plastic, SOIC	−60		+100	*		*							°C

* Specification same as model to the left.

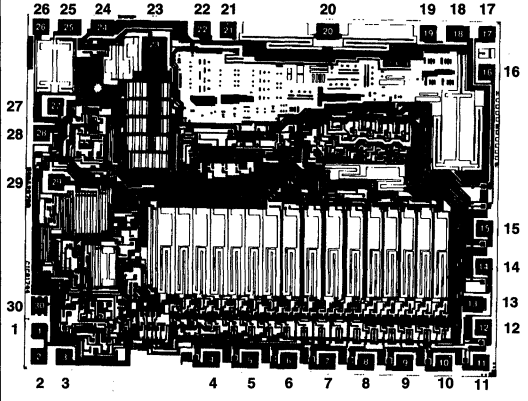
NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0.0015% of FSR for the LH and CH grades, ±0.003% of FSR for the BH grade and ±0.006% of FSR for the KG grade. (2) DAC700 and DAC702 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC702) and the 0 to +2mA range (DAC700). (4) ±0.0015% of full-scale range is equivalent to 1LSB in 15-bit resolution. ±0.003% of full-scale range is equivalent to 1LSB in 14-bit resolution. ±0.006% of full-scale range is equivalent to 1LSB in 13-bit resolution. (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the zero point. (6) Error at input code $FFFF_H$ for DAC700 and DAC701, $7FFF_H$ for DAC702 and DAC703. (7) With gain and zero errors adjusted to zero at +25°C. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Tolerance on output impedance and output current is ±30%. (11) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V, +18V
$-V_{CC}$ to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to R_F (DAC700/702)	±18V
External Voltage Applied to D/A Output (DAC701/703)	−5V to +5V
V_{OUT} (DAC701/703)	Indefinite Short to Common
Power Dissipation	1W
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DICE INFORMATION



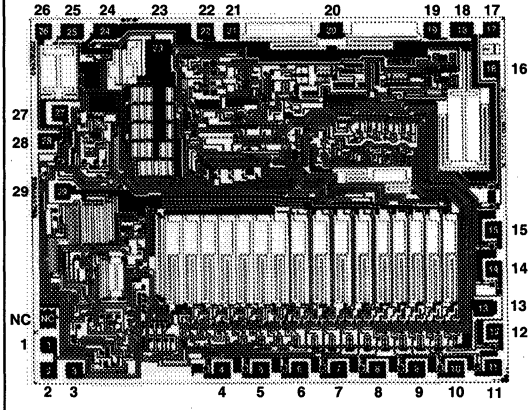
DAC702KD DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} –10kΩ
4	Bit 4 Input	19	No Connection
5	Bit 5 Input	20	R_{FB} –10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	–15V Supply	28	Reference Output
14	Bit 13 Input	29	–15V Supply
15	Bit 14 Input	30	Zener Test Point
			Do Not Use

Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	153 x 120	3.89 x 3.05
Die Thickness	20 Mils	0.5
Min. Pad Size	4 x 4	0.1 x 0.1
Metalization		Aluminum



DAC703KD DIE TOPOGRAPHY

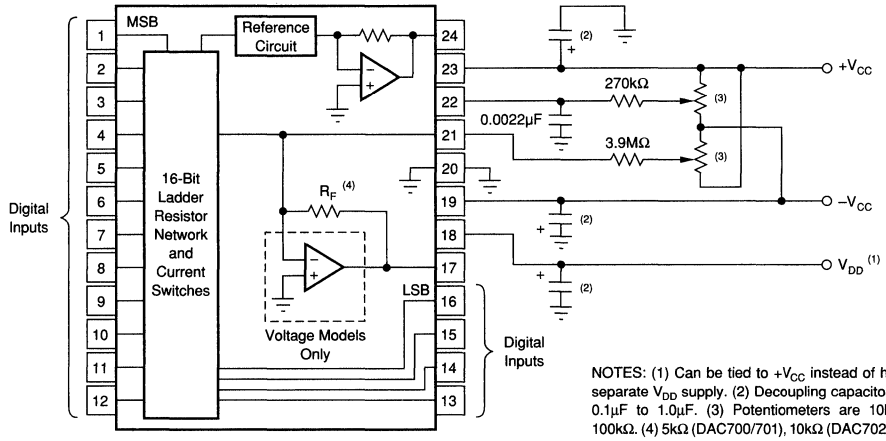
PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB) Input	16	Bit 15 Input
2	Bit 2 Input	17	Bit 16 Input
3	Bit 3 Input	18	R_{FB} –10kΩ
4	Bit 4 Input	19	Voltage Output
5	Bit 5 Input	20	R_{FB} –10kΩ
6	Bit 6 Input	21	+5V Supply
7	Bit 7 Input	22	Digital Ground
8	Bit 8 Input	23	Analog Ground
9	Bit 9 Input	24	Current Output
10	Bit 10 Input	25	Bipolar Offset
11	Bit 11 Input	26	Gain Adjust
12	Bit 12 Input	27	+15V Supply
13	–15V Supply	28	Reference Output
14	Bit 13 Input	29	–15V Supply
15	Bit 14 Input	30	Zener Test Point
			Do Not Use

Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	153 x 120	3.89 x 3.05
Die Thickness	20 Mils	0.5
Min. Pad Size	4 x 4	0.1 x 0.1
Metalization		Aluminum

CONNECTION DIAGRAMS



NOTES: (1) Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply. (2) Decoupling capacitors are 0.1µF to 1.0µF. (3) Potentiometers are 10kΩ to 100kΩ. (4) 5kΩ (DAC700/701), 10kΩ (DAC702/703).

PIN ASSIGNMENTS

PIN #	ALL PACKAGES	
	DAC700/702	DAC701/703
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Reference Output	+6.3V Reference Output

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC702JP	24-Pin Plastic DIP	167
DAC703JP	24-Pin Plastic DIP	167
DAC702KP	24-Pin Plastic DIP	167
DAC703KP	24-Pin Plastic DIP	167
DAC700KH	24-Pin Ceramic DIP	165
DAC701KH	24-Pin Ceramic DIP	165
DAC702KH	24-Pin Ceramic DIP	165
DAC703KH	24-Pin Ceramic DIP	165
DAC700BH	24-Pin Ceramic DIP	165
DAC701BH	24-Pin Ceramic DIP	165
DAC702BH	24-Pin Ceramic DIP	165
DAC703BH	24-Pin Ceramic DIP	165
DAC700LH	24-Pin Ceramic DIP	165
DAC701LH	24-Pin Ceramic DIP	165
DAC702LH	24-Pin Ceramic DIP	165
DAC703LH	24-Pin Ceramic DIP	165
DAC700CH	24-Pin Ceramic DIP	165
DAC701CH	24-Pin Ceramic DIP	165
DAC702CH	24-Pin Ceramic DIP	165
DAC703CH	24-Pin Ceramic DIP	165
DAC702SH	24-Pin Ceramic DIP	165
DAC703SH	24-Pin Ceramic DIP	165
DAC703JU	24-Pin SOIC	239
DAC703KU	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	OUTPUT CONFIGURATION	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (% of FSR)	GAIN DRIFT MAX (ppm/°C)
DAC702JP, DAC703JP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.006	±30
DAC702KP, DAC703KP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700KH, DAC701KH	Ceramic DIP	0 to –2mA, 0 to +10V	0°C to +70°C	±0.003	±25
DAC702KH, DAC703KH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700BH, DAC701BH	Ceramic DIP	0 to –2mA, 0 to +10V	–25°C to +85°C	±0.003	±15
DAC702BH, DAC703BH	Ceramic DIP	±1mA, ±10V	–25°C to +85°C	±0.003	±15
DAC700LH, DAC701LH	Ceramic DIP	0 to –2mA, 0 to +10V	0°C to +70°C	±0.0015	±10
DAC700CH, DAC701CH	Ceramic DIP	0 to –2mA, 0 to +10V	–25°C to +85°C	±0.0015	±10
DAC700SH, DAC701SH	Ceramic DIP	0 to –2mA, 0 to +10V	–55°C to +125°C	±0.003	±15
DAC702LH, DAC703LH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.0015	±10
DAC702CH, DAC703CH	Ceramic DIP	±1mA, ±10V	–25°C to +85°C	±0.0015	±10
DAC702SH, DAC703SH	Ceramic DIP	±1mA, ±10V	–55°C to +125°C	±0.003	±15
DAC703JU	Plastic SOIC	±10V	0°C to +70°C	±0.006	±30
DAC703KU	Plastic SOIC	±10V	0°C to +70°C	±0.003	±25

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC700/701/702/703 accept complementary digital input codes in either binary format (CSB, unipolar or COB, bipolar). The COB models DAC702/703 may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

DIGITAL INPUT CODES	ANALOG OUTPUT		
	DAC700/701 Complementary Straight Binary (CSB)	DAC702/703 Complementary Offset Binary (COB)	DAC702/703 Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	–1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	– Full Scale
8000_H	+1/2 Full Scale –1LSB	–1LSB	+ Full Scale
$FFFF_H$	Zero	– Full Scale	Bipolar Zero

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential linearity error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than –1LSB (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC700/701/702/703 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $FFFF_H$ (DAC700 and DAC701) applied to the digital inputs over the specified temperature range. For the bipolar models, zero is measured at $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to zero volts (DAC703) or zero milliamps (DAC702) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (DAC703) or 10V (DAC701) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

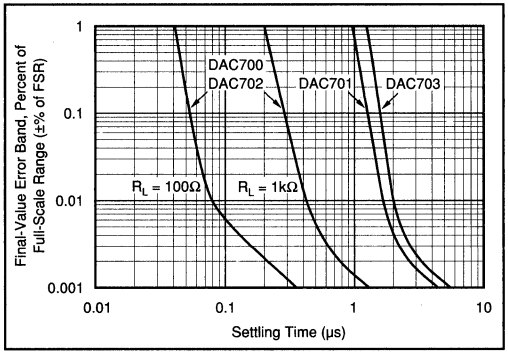


FIGURE 1. Final-Value Error Band vs Full-Scale Range Settling Time.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

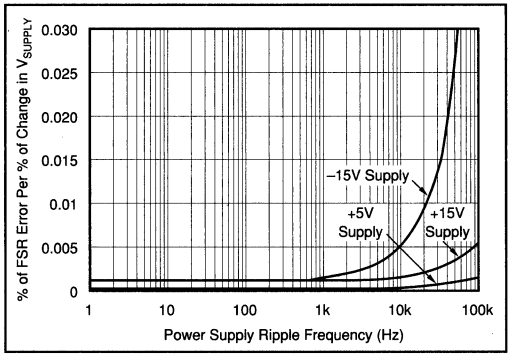


FIGURE 2. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage, available to the user, has a tolerance of ±5% (KH models) and ±1% (BH models). A minimum of 1.5mA is available for external loads. Since the output impedance of the reference output is typically 1W, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001µF to 0.01µF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

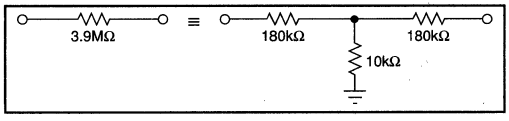


FIGURE 3. Equivalent Resistances.

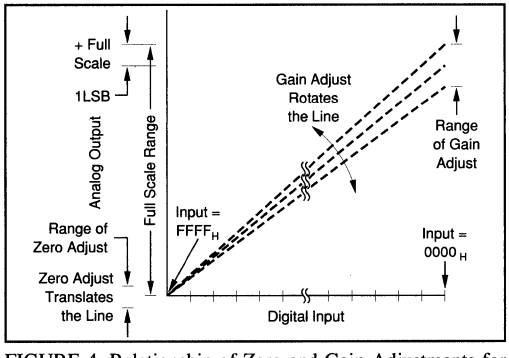


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC700 and DAC701.

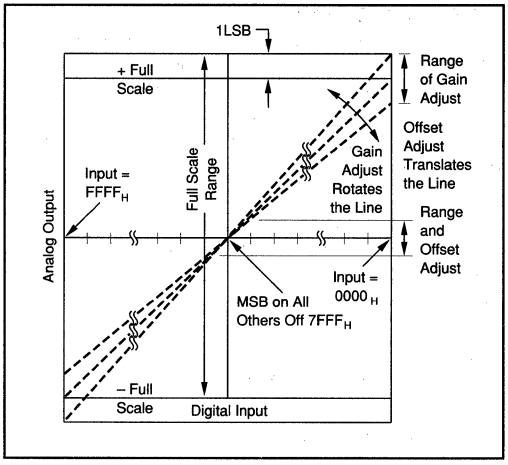


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC702 and DAC703.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a 10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{L\,MIN}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\,MIN}$ is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC700 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20µA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 (R_4 x 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models (DAC700 or DAC702) with external precision output op amps. By sensing the output voltage at the load resistor (ie, by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

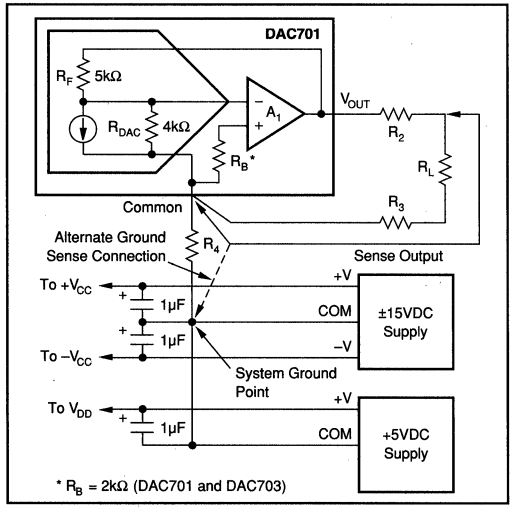


FIGURE 6. Output Circuit for Voltage Models.

VOLTAGE OUTPUT MODELS							
		ANALOG OUTPUT					
		DAC701 UNIPOLAR			DAC703 BIPOLAR		
DIGITAL INPUT CODE		16-BIT	15-BIT	14-BIT	16-BIT	15-BIT	14-BIT
1LSB	(μV)	153	305	610	305	610	1224
0000_H	(V)	+9.99985	+9.99969	+9.99939	+9.99960	+9.99939	+9.99878
$FFFF_H$	(V)	0	0	0	–10.0000	–10.0000	–10.0000
ANALOG OUTPUT MODELS							
		ANALOG OUTPUT					
		DAC700 UNIPOLAR			DAC702 BIPOLAR		
DIGITAL INPUT CODE		16-BIT	15-BIT	14-BIT	16-BIT	15-BIT	14-BIT
1LSB	(μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H	(mA)	–1.99997	–1.99994	–1.99988	–0.99997	–0.99994	–0.99988
$FFFF_H$	(mA)	0	0	0	+1.00000	+1.00000	+1.00000

TABLE II. Digital Input and Analog Output Relationships.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

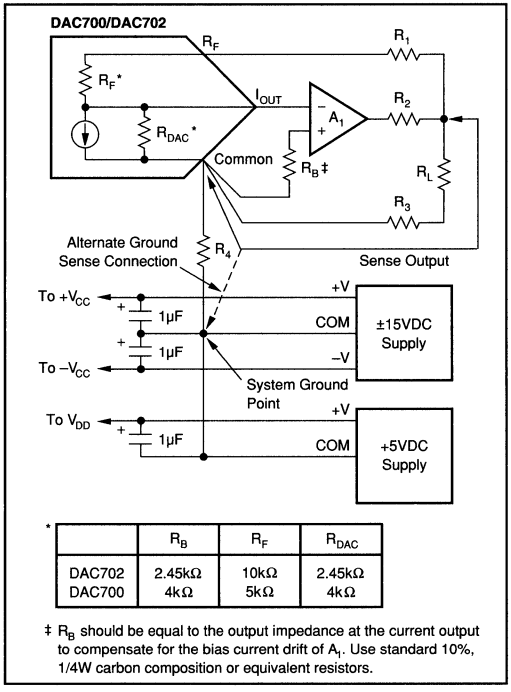


FIGURE 7. Preferred External Op Amp Configuration.

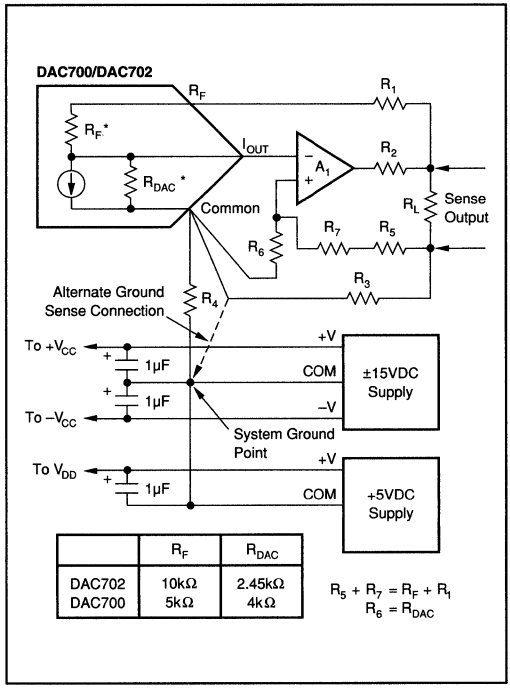


FIGURE 8. Differential Sensing Output Op Amp Configuration.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/AS

DAC700 and DAC702 are current output devices and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

DAC700 or DAC702 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the DAC700 and DAC702 ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and –2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

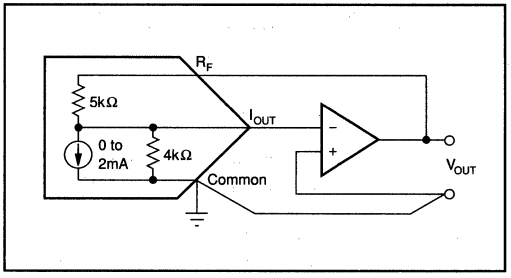


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

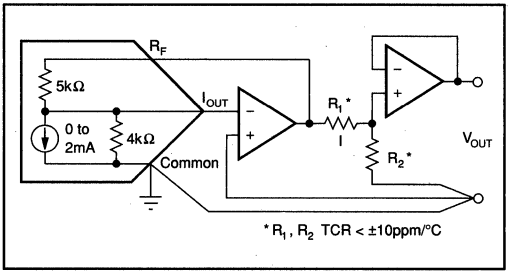


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

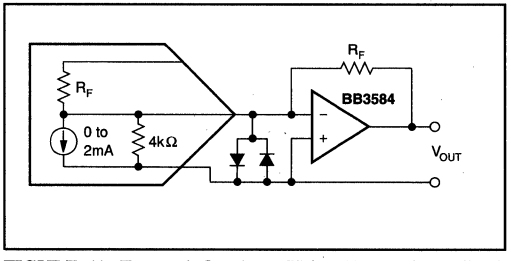


FIGURE 11. External Op Amp Using External Feedback Resistors.

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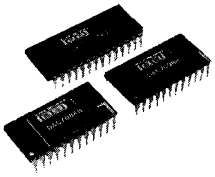


DAC707
DAC708/709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

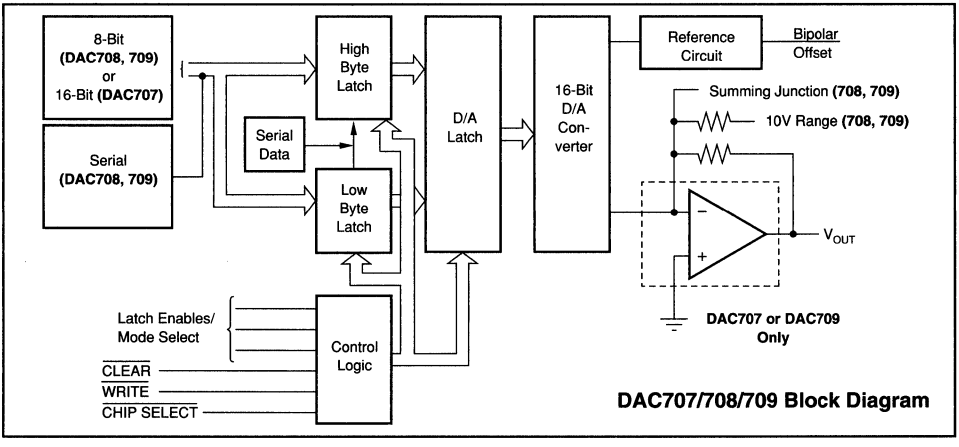
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY: Linearity Error ±0.003% of FSR max Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)

DESCRIPTION

The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first).

The DAC707 is designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC707 has bipolar voltage output and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and for the DAC707, and DAC709, a voltage output amplifier. All models are available with an optional burn-in screening.



DAC707/708/709 Block Diagram

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP MIN	DAC707JP TYP	DAC707JP MAX	DAC707/708/709KH, DAC707KP MIN	DAC707/708/709KH, DAC707KP TYP	DAC707/708/709KH, DAC707KP MAX	DAC707/708/709BH, SH MIN	DAC707/708/709BH, SH TYP	DAC707/708/709BH, SH MAX	UNITS
INPUT										
DIGITAL INPUT										
Resolution			16			*			*	Bits
Bipolar Input Code (all models)		Binary Two's Complement			*			*		
Unipolar Input Code[1] (DAC708/709 only)					Unipolar Straight Binary			*		
Logic Levels[2]: V_{IH}	+2.0		+5.5	*		*	*		*	V
V_{IL}	–1.0		+0.8	*		*	*		*	V
I_{IH} (V_I = +2.7V)			1			*			*	µA
I_{IL} (V_I = +0.4V)			1			*			*	µA
TRANSFER CHARACTERISTICS										
ACCURACY[3]										
Linearity Error		±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.0045	±0.012		±0.003	±0.006		*	*	% of FSR
at Bipolar Zero[5, 6]					±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.30		*	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		*	*		*	*	% of FSR
Monotonicity Over Spec Temp Range	13			14			14			Bits
Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$		±0.0015	±0.006		*	*		*	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*	% of FSR/%V_{DD}
DRIFT (Over Spec Temp Range[3])										
Total Error Over Temp Range[8]		±0.08			*	±0.15		*	±0.10	% of FSR
Total Full Scale Drift		±10			*	±25		*	±15	ppm of FSR/°C
Gain Drift		±10	±30		*	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)					±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±15		*	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			±0.012			+0.009, –0.006			*	% of FSR
Linearity Error Over Temp[5]			±0.012			±0.006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[9]										
Voltage Output Models										
Full Scale Step (2kΩ load)		4			*	8		*	8	µs
1LSB Step at Worst Case Code[10]		2.5			*	4		*	4	µs
Slew Rate		10			*			*		V/µs
Current Output Models										
Full Scale Step (2mA): 10 to 100Ω Load					350			*		ns
1kΩ Load					1			*		µs
OUTPUT										
VOLTAGE OUTPUT MODELS										
Output Voltage Range										
DAC709: Unipolar (USB Code)					0 to +10			*		V
Bipolar (BTC Code)					±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*			*		V
Output Current	±5			*			*			mA
Output Impedance		0.15			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*		
CURRENT OUTPUT MODELS										
Output Current Range (±30% typ)										
DAC708: Unipolar (USB Code)					0 to –2			*		mA
Bipolar (BTC Code)					±1			*		mA
Unipolar Output Impedance (±30% typ)					4.0			*		kΩ
Bipolar Output Impedance (±30% typ)					2.45			*		kΩ
Compliance Voltage					±2.5			*		V

ELECTRICAL (CONT)

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP			DAC707/708/709KH, DAC707KP			DAC707/708/709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS										
Voltage (all models): $+V_{CC}$	+13.5	+15	+16.5	*	*	*	*	*	*	V
$-V_{CC}$	−13.5	−15	−16.5	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	V
Current (No Load, +15V Supplies)										
Current Output Models: $+V_{CC}$					+10	+25		*	*	mA
$-V_{CC}$					−13	−25		*	*	mA
V_{DD}					+5	+10		*	*	mA
Voltage Output Models: $+V_{CC}$		+16	+30		*	*		*	*	mA
$-V_{CC}$		−18	−30		*	*		*	*	mA
V_{DD}		+5	+10		*	*		*	*	mA
Power Dissipation (±15V supplies)										
Current Output Models					370	800		*	*	mW
Voltage Output Models		535			*	950		*	*	mW
TEMPERATURE RANGE										
Specification: BH Grades							−25		+85	°C
JP, KP, KH Grades	0		+70	*		*				°C
SH Grades							−55		+125	°C
Storage: Ceramic				−65		+150	−65		+150	°C
Plastic	−60		+100	*		*				°C

*Specification same as for models in column to the left.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution, ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) With gain and zero errors adjusted to zero at +25°C. (9) Maximum represents the 3σ limit. Not 100% tested for this parameter. (10) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC707JP	28-Pin Plastic DBL Wide DIP	215
DAC707KP	28-Pin Plastic DBL Wide DIP	215
DAC707BH	28LD Side Brazed Hermetic Dip	144
DAC707KH	28LD Side Brazed Hermetic DIP	144
DAC707SH	28LD Side Brazed Hermetic DIP	144
DAC708BH	24LD Side Brazed Hermetic DIP	165
DAC708KH	24LD Side Brazed Hermetic DIP	165
DAC708SH	24LD Side Brazed Hermetic DIP	165
DAC709BH	24LD Side Brazed Hermetic DIP	165
DAC709KH	24LD Side Brazed Hermetic DIP	165
DAC709SH	24LD Side Brazed Hermetic DIP	165

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
$+V_{CC}$ to COMMON ..... 0V, +18V
$-V_{CC}$ to COMMON ..... 0V, −18V
Digital Data Inputs to COMMON ..... −0.5V, V_{DD} +0.5
DC Current any input ..... ±10mA
Reference Out to COMMON ..... Indefinite Short to COMMON
V_{OUT} (DAC707, DAC709) ..... Indefinite Short to COMMON
External Voltage Applied to R_F (pin 13 or 14, DAC708) ..... ±18V
External Voltage Applied to D/A Output
(pin 1, DAC707; pin 14, DAC709) ..... ±5V
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

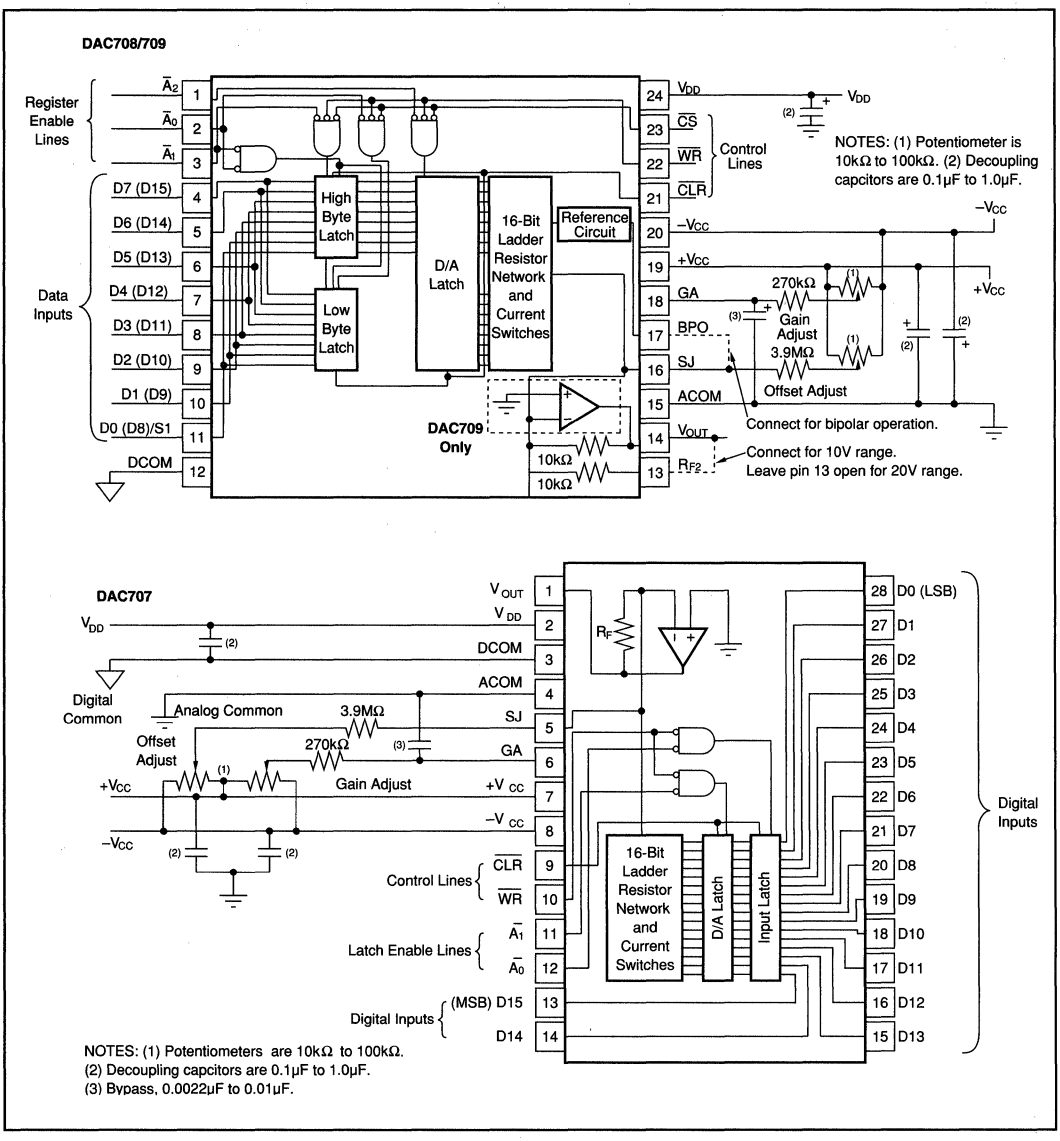
MODEL	TEMPERATURE RANGE	INPUT CONFIG	OUTPUT CONFIG
DAC707JP	0°C to +70°C	16-bit port	±10V output
DAC707JP-BI(1)	0°C to +70°C	16-bit port	±10V output
DAC707KP	0°C to +70°C	16-bit port	±10V output
DAC707KP-BI(1)	0°C to +70°C	16-bit port	±10V output
DAC707KH	0°C to +70°C	16-bit port	±10V output
DAC707KH-BI(1)	0°C to +70°C	16-bit port	±10V output
DAC707BH	−25°C to +85°C	16-bit port	±10V output
DAC707BH-BI(1)	−25°C to +85°C	16-bit port	±10V output
DAC707SH	−55°C to +125°C	16-bit port	±10V output
DAC707SH-BI(1)	−55°C to +125°C	16-bit port	±10V output
DAC708KH	0°C to +70°C	8-bit port	±1mA output
DAC708BH	−25°C to +85°C	8-bit port	±1mA output
DAC708SH	−55°C to +125°C	8-bit port	±1mA output
DAC709KH	0°C to +70°C	8-bit port	±10V output
DAC709BH	−25°C to +85°C	8-bit port	±10V output
DAC709SH	−55°C to +125°C	8-bit port	±10V output

NOTE: (1) 25 piece minimum order.

DESCRIPTION OF PIN FUNCTIONS

DAC707		Pin	DAC708/709	
DESIGNATOR	**DESCRIPTION**	**#**	**DESIGNATOR**	**DESCRIPTION**
V_{OUT}	Voltage output for DAC707 (±10V)	1	A_2	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	A_0	Latch enable for "low byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital common	3	A_1	Latch enable for "high byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ	Summing junction of the internal output op amp for the DAC707. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (–15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
$\overline{CLR}$	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
$\overline{WR}$	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
$\overline{A_1}$	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
$\overline{A_0}$	Enable for input latch (Active low)	12	DCOM	Digital common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (–15V)
D7	Data bit 7	21	$\overline{CLR}$	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

CONNECTION DIAGRAMS



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

Digital Input Codes	ANALOG OUTPUT	
	Unipolar Straight Binary[1] (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale –1LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	–1LSB
8000_H	+1/2 Full Scale	–Full Scale

NOTES: (1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (–Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of –1LSB maximum (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain Drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero Drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted). This code corresponds to zero volts (DAC707 and DAC709) or zero milliamps (DAC708) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

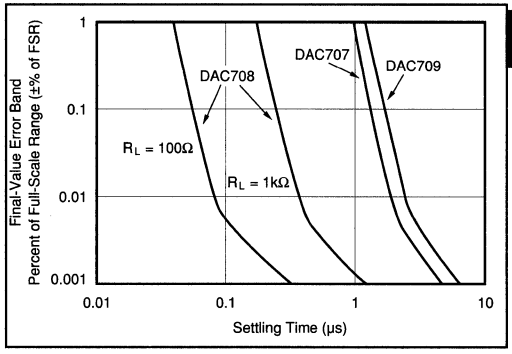


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter

output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

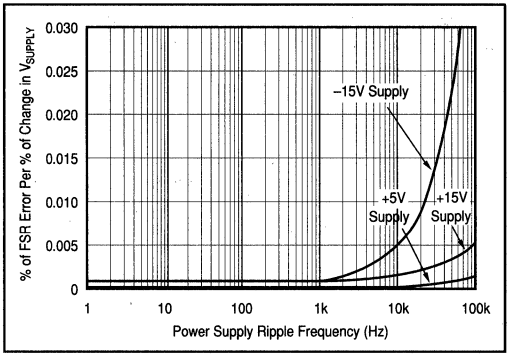


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001µF to 0.01µF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

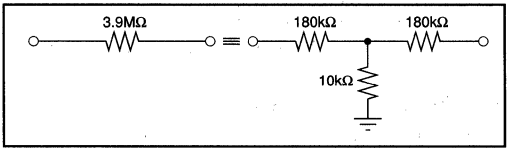


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustments circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

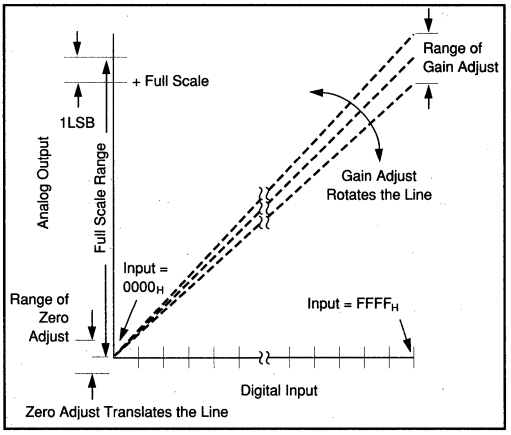


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

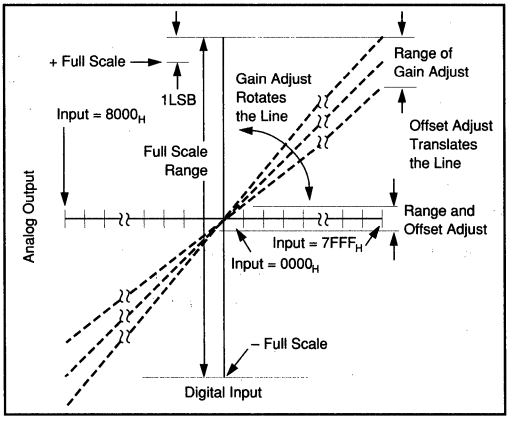


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC707 and DAC708/709

VOLTAGE OUTPUT MODELS												
Digital Input Code	Analog Output			Units	Digital Input Code	Analog Output						Units
	Unipolar, 0 to +10V[1]					Bipolar, ±10V			Bipolar, ±5V			
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	µV	One LSB	305	610	1224	153	305	610	µV
$FFFF_H$	+9.99985	+9.99969	+9.99939	V	7FFFH	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000_H	0	0	0	V	8000H	−10.0000	−10.0000	−10.0000	−5.0000	−5.0000	−5.0000	V

CURRENT OUTPUT MODELS									
Digital Input Code	Analog Output			Units	Digital Input Code	Analog Output			Units
	Unipolar, 0 to −2mA[1]					Bipolar, ±1mA			
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0.031	0.061	0.122	µA	One LSB	0.031	0.061	0.122	µA
$FFFF_H$	−1.99997	−1.99994	−1.99988	mA	$7FFF_H$	−0.99997	−0.99994	−0.99988	mA
0000_H	0	0	0	mA	8000_H	+1.00000	+1.00000	+1.00000	mA

NOTE: (1) MSB assumed to be inverted externally.

TABLE II. Digital Input and Analog Output Voltage/Current Relationships.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A}_0$, $\overline{A}_1$, and $\overline{A}_2$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A}_0$ and $\overline{A}_1$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A}_2$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A}_2$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

DAC707

The DAC707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A}_0$. The D/A latch is enabled by $\overline{A}_1$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

LOGIC TIMING - Parallel or Serial Data Input		Over Temperature ns, min	ns, max
T_{DW}	Data valid to end of $\overline{WR}$	80	
T_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
T_{AW}	$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ valid to end of $\overline{WR}$	80	
T_{WP}	Write pulse width	80	
T_{DH}	Data hold after end of $\overline{WR}$	0	

TIMING DIAGRAM

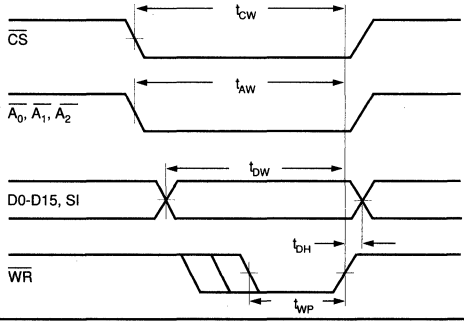


FIGURE 6. Logic Timing Diagram.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

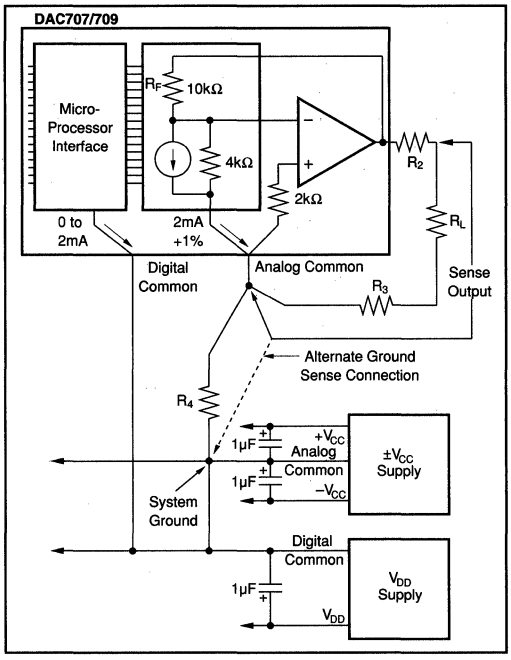


FIGURE 7. DAC707/709 Bipolar Output Circuit (Voltage Out).

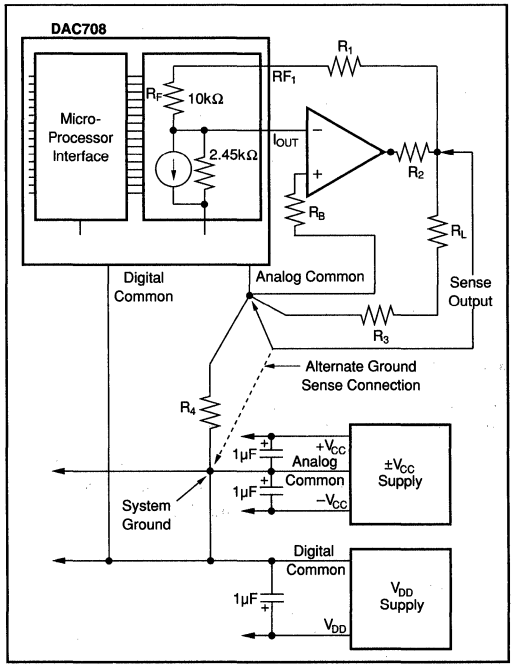


FIGURE 8. DAC708 Bipolar Output Circuit (with External Op Amp).

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

Figures 8 and 9 show two methods of connecting the current output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

In many applications it is impractical to sense the output voltage at ANALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10µA to 20µA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

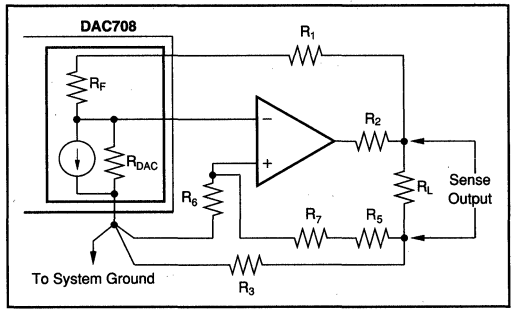


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

BURN-IN SCREENING

Burn-in screening is an option available for the DAC707. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Model	Temp. Range	Burn-In Screening
DAC707JP-BI	0°C to 70°C	100°C
DAC707KP-BI	0°C to 70°C	100°C
DAC707KH-BI	–25°C to +85°C	125°C
DAC707BH-BI	–25°C to +85°C	125°C
DAC707SH-BI	–55°C to +125°C	125°C

All units are tested after burn-in to ensure that grade specifications are met.

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The $\overline{WR}$ input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 $\overline{WR}$ pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

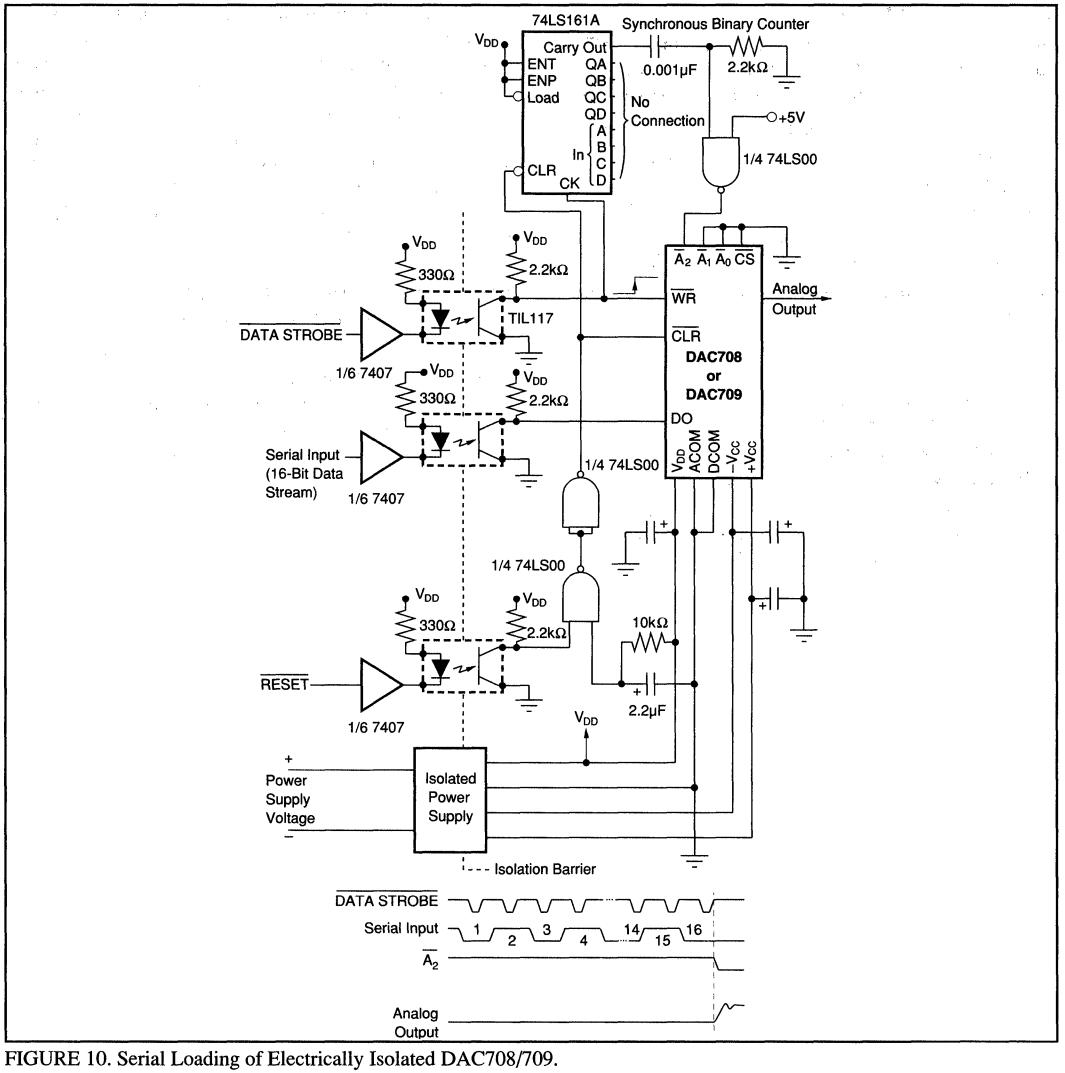


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

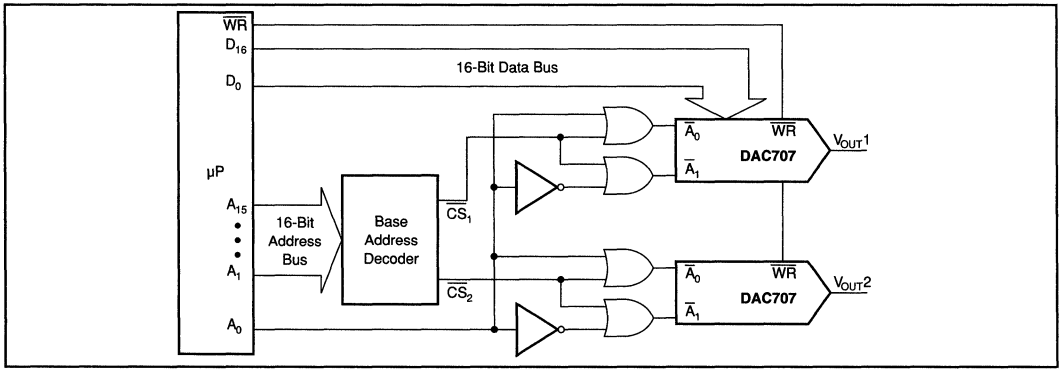


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

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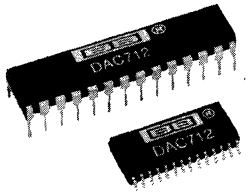


DAC712

16-BIT DIGITAL-TO-ANALOG CONVERTER WITH 16-BIT BUS INTERFACE

FEATURES

- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: ±10V
- 13-, 14-, AND 15-BIT LINEARITY GRADES
- 15-BIT MONOTONIC OVER TEMPERATURE (K GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES

DESCRIPTION

DAC712 is a complete 16-bit resolution D/A converter.

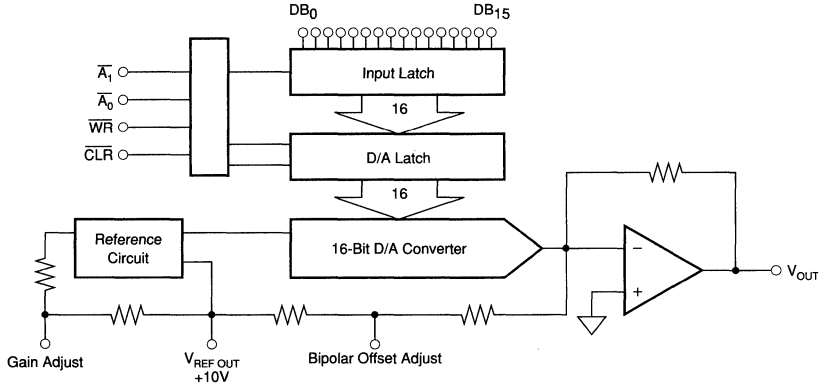
DAC712 has a precision +10V temperature compensated voltage reference, ±10V output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to bipolar zero.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC712 is available in two linearity error performance grades: ±4LSB DAC712P and U, ±2LSB DAC712PB, PK or UB, UK. DAC712 is specified at power supply voltages of ±12V and ±15V.

DAC712 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. The DAC712P, U, PB, UB are specified over the –40°C to +85°C temperature range and the DAC712UK, PK are specified over the 0°C to +70°C range.



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SPECIFICATIONS

ELECTRICAL

At T_A = 25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = −12V and −15V, unless otherwise noted.

PARAMETER	DAC712P, U			DAC712PB, UB			DAC712PK, UK			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT										
RESOLUTION		16			*			*		Bits
DIGITAL INPUTS										
Input Code	Binary Two's Complement				*			*		
Logic Levels[1]										
V_{IH}	+2.0		$+V_{CC}-1.4$	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH} (V_I = +2.7V)			±10			*			*	µA
I_{IL} (V_I = +0.4V)			±10			*			*	µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error			±4			±2			±2	LSB
T_{MIN} to T_{MAX}			±8			±4			±2	LSB
Differential Linearity Error			±4			±2			±2	LSB
T_{MIN} to T_{MAX}			±8			±4			±2	LSB
Monotonicity Over Temp	13			14			15			Bits
Gain Error[3]			±0.1			±0.1			*	%
T_{MIN} to T_{MAX}			±0.2			±0.15			*	%
Bipolar Zero Error[3]			±0.1			*			*	% FSR[2]
			±20			*			*	mV
T_{MIN} to T_{MAX}			±0.2			±0.15			*	% FSR
			±40			±30			*	mV
Power Supply Sensitivity Of Full Scale:			±0.003			*			*	% FSR/% V_{CC}
			±30			*			*	ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE										
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)[4]										
20V Output Step		6			*	10		*	*	µs
1 LSB Output Step[5]		4			*			*		µs
Output Slew Rate		10			*			*		V/µs
Total Harmonic Distortion + Noise										
0dB, 1001Hz, f_S = 100kHz		0.005			*			*		%
−20dB, 1001Hz, f_S = 100kHz		0.03			*			*		%
−60dB, 1001Hz, f_S = 100kHz		3.0			*			*		%
SINAD										
1001Hz, f_S = 100kHz		87			*			*		dB
Digital Feedthrough[5]		2			*			*		nV-s
Digital-to-Analog Glitch Impulse[5]		15			*			*		nV-s
Output Noise Voltage (Includes Reference)		120			*			*		nV/√Hz
ANALOG OUTPUT										
Output Voltage Range										
$+V_{CC}$, $-V_{CC}$ = ±11.4V	±10			*			*			V
Output Current	±5			*			*			mA
Output Impedance		0.1			*			*		Ω
Short Circuit to ACOM										
Duration		Indefinite			*			*		
REFERENCE VOLTAGE										
Voltage	+9.975	+10.000	+10.025	*	*	*	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	*		*	V
Output Resistance		1			*			*		Ω
Source Current	2			*			*			mA
Short Circuit to ACOM, Duration		Indefinite			*			*		
POWER SUPPLY REQUIREMENTS										
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	V
$-V_{CC}$	−11.4	−15	−16.5	*	*	*	*	*	*	V
Current (No Load, ±15V Supplies)										
$+V_{CC}$		13	15		*	*		*	*	mA
$-V_{CC}$		22	25		*	*		*	*	mA
Power Dissipation[6]		525	600		*	*		*	*	mW
TEMPERATURE RANGES										
Specification										
All Grades	−40		+85	*		*	0		+70	°C
Storage	−60		+150	*		*	*		*	°C
Thermal Coefficient θ_{JA}										
DIP Package		75			*			*		°C/W
SOIC Package		75			*			*		°C/W

*Specifications are the same as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V, +17V
$-V_{CC}$ to COMMON	0V, −17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	−1V to $+V_{CC}$ −0.7V
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC712P	Plastic DIP	246
DAC712U	Plastic SOIC	217
DAC712PB	Plastic DIP	246
DAC712UB	Plastic SOIC	217
DAC712PK	Plastic DIP	246
DAC712UK	Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

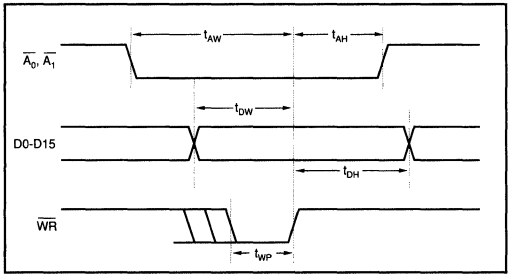
MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX at +25°C
DAC712P	Plastic DIP	−40°C to +85°C	±4LSB
DAC712U	Plastic SOIC	−40°C to +85°C	±4LSB
DAC712PB	Plastic DIP	−40°C to +85°C	±2LSB
DAC712UB	Plastic SOIC	−40°C to +85°C	±2LSB
DAC712PK	Plastic DIP	0°C to +70°C	±2LSB
DAC712UK	Plastic SOIC	0°C to +70°C	±2LSB

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

TIMING DIAGRAM



TIMING SPECIFICATIONS

T_A = −40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V.

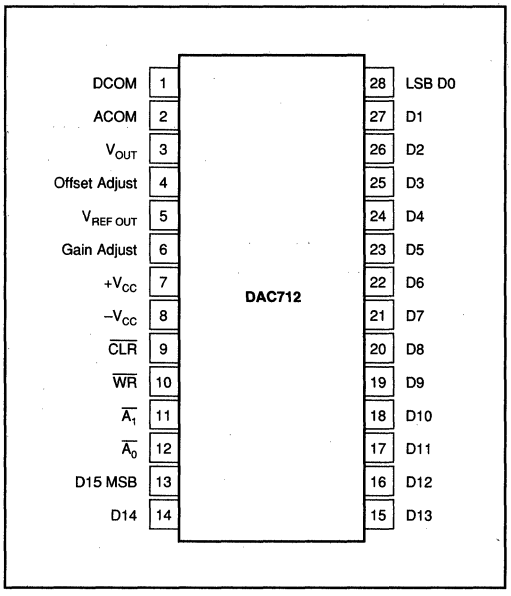
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	50		ns
t_{AW}	$\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$	50		ns
t_{AH}	$\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$	10		ns
t_{DH}	Data Hold after end of $\overline{WR}$	10		ns
t_{WP}(1)	Write Pulse Width	50		ns
t_{CP}	CLEAR Pulse Width	200		ns

NOTES: (1) For single-buffered operation, t_{WP} is 80ns min. Refer to page 10.

TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	1 → 0 → 1	1	Load Input Latch
1	0	1 → 0 → 1	1	Load D/A Latch
1	1	1 → 0 → 1	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

PIN CONFIGURATION



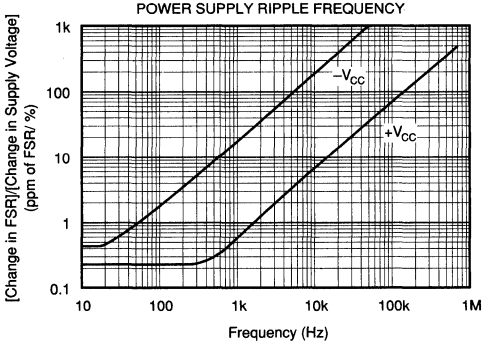
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Power Supply return for digital currents.
2	ACOM	Analog Supply Return.
3	V_{OUT}	±10V D/A Output.
4	Off Adj	Offset Adjust (Bipolar).
5	$V_{REF\ OUT}$	Voltage Reference Output.
6	Gain Adj	Gain Adjust.
7	$+V_{CC}$	+12V to +15V Supply.
8	$-V_{CC}$	−12V to −15V Supply.
9	$\overline{CLR}$	CLEAR. Sets D/A output to BIPOLAR ZERO (Active Low).
10	$\overline{WR}$	Write (Active Low).
11	$\overline{A_1}$	Enable for D/A latch (Active Low).
12	$\overline{A_0}$	Enable for Input latch (Active Low).
13	D15	Data Bit 15 (Most Significant Bit).
14	D14	Data Bit 14.
15	D13	Data Bit 13.
16	D12	Data Bit 12.
17	D11	Data Bit 11.
18	D10	Data Bit 10.
19	D9	Data Bit 9.
20	D8	Data Bit 8.
21	D7	Data Bit 7.
22	D6	Data Bit 6.
23	D5	Data Bit 5.
24	D4	Data Bit 4.
25	D3	Data Bit 3.
26	D2	Data Bit 2.
27	D1	Data Bit 1.
28	D0	Data Bit 0 (Least Significant Bit).

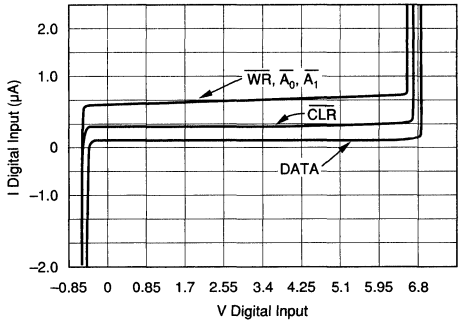
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

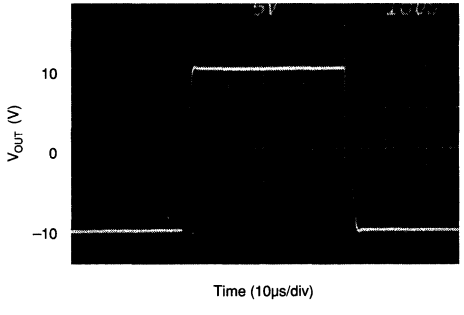
POWER SUPPLY REJECTION vs POWER SUPPLY RIPPLE FREQUENCY



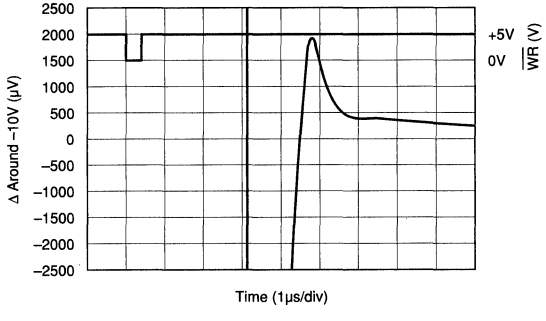
LOGIC vs V LEVEL



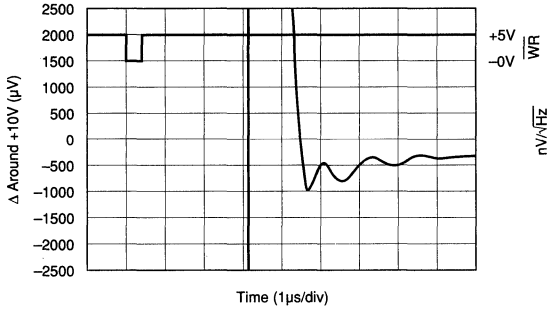
± FULL SCALE OUTPUT SWING



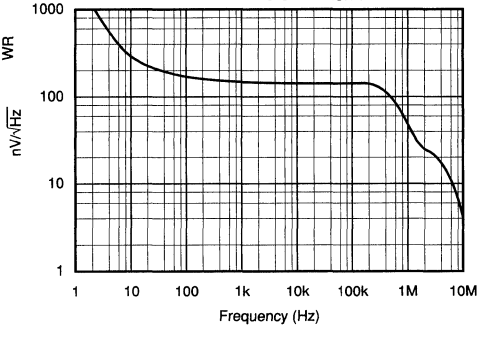
SETTLING TIME, +10V TO –10V



SETTLING TIME, –10V TO +10V



SPECTRAL NOISE DENSITY



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC712 is guaranteed over the specification temperature range to 13-, 14-, and 15 bits for performance grades DAC712P/U, DAC712PB/UB, and DAC712PK/UK, respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_{HEX}$ to 0000_{HEX}, and 0000_{HEX} to $FFFF_{HEX}$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from $7FFF_{HEX}$ to 8000_{HEX}.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC712 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

DAC712 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a bipolar zero output.

LOGIC INPUT COMPATIBILITY

DAC712 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic "0" and control inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC712 is designed to accept positive-true binary two's complement (BTC) input codes which are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of $7FFF_{HEX}$ gives a plus full scale output, 8000_{HEX} gives a minus full scale output, and 0000_{HEX} gives bipolar zero output.

INTERNAL REFERENCE

DAC712 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

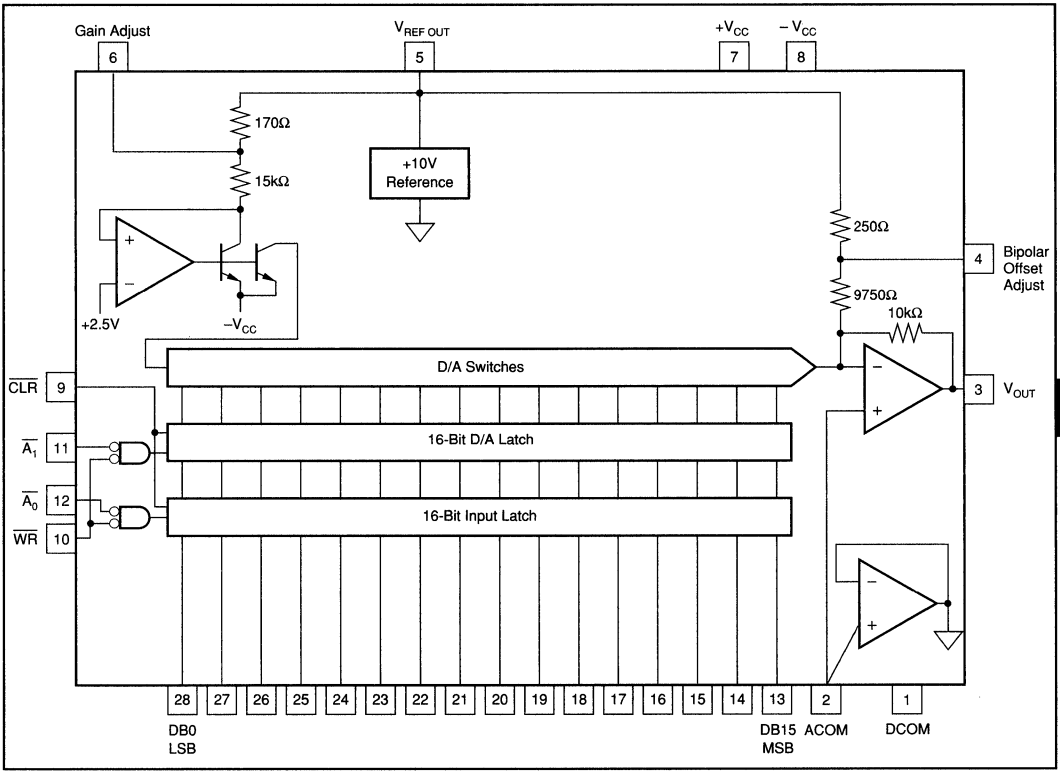


FIGURE 1. DAC712 Block Diagram.

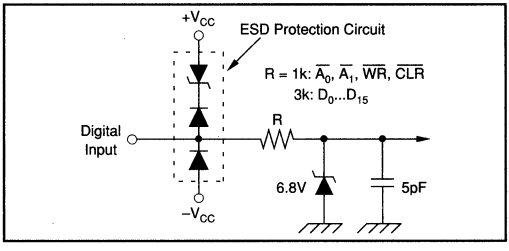


FIGURE 2. Equivalent Circuit of Digital Inputs.

OUTPUT VOLTAGE SWING

The output amplifier of DAC712 is committed to a ±10V output range. DAC712 will provide a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

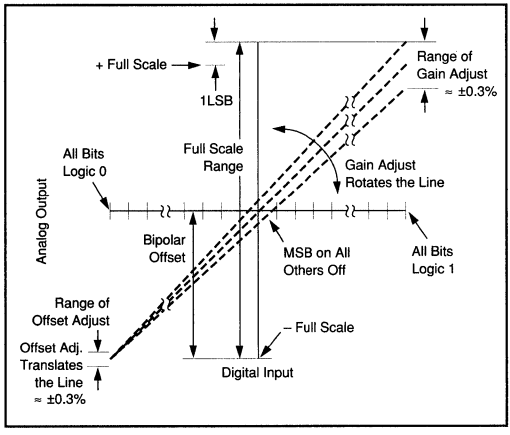


FIGURE 3. Relationship of Offset and Gain Adjustments.

Offset Adjustment

Apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for –10V.

DAC712 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 305µV		
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V)	DESCRIPTION
$7FFF_H$	+9.999695	+ Full Scale –1LSB
4000_H	+5.000000	3/4 Scale
0001_H	+0.000305	BPZ + 1LSB
0000_H	0.000000	Bipolar Zero (BPZ)
$FFFF_H$	–0.000305	BPZ – 1LSB
$C000_H$	–5.000000	1/4 Scale
8000_H	–10.00000	Minus Full Scale

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milli-inch wide printed circuit conductor 60 milli-inches long will result in a voltage drop of 150µV.

The analog output of DAC712 has an LSB size of 305µV (–96dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC712's noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

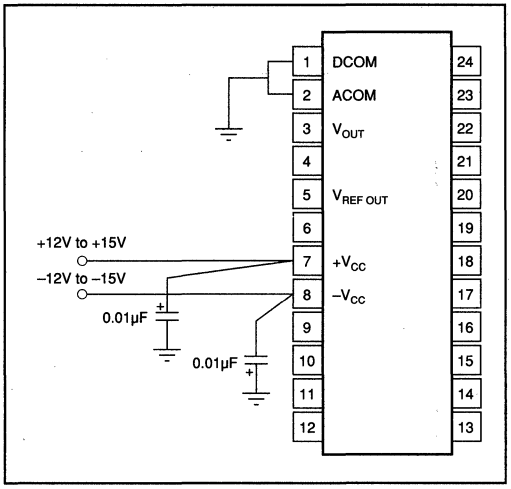


FIGURE 4. Power Supply Connections.

DAC712 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC712s are used or if DAC712 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because

there is no change in DAC712 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC712 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC712 output amplifier is connected internally for the ±10V bipolar (20V) output range. That is, the bipolar offset resistor is connected to an internal reference voltage and the 20V range resistor is connected internally to V_{OUT}. DAC712 cannot be connected by the user for unipolar operation.

DIGITAL INTERFACE

BUS INTERFACE

DAC712 has 16-bit double-buffered data bus interface with control lines for easy interface to interface to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.

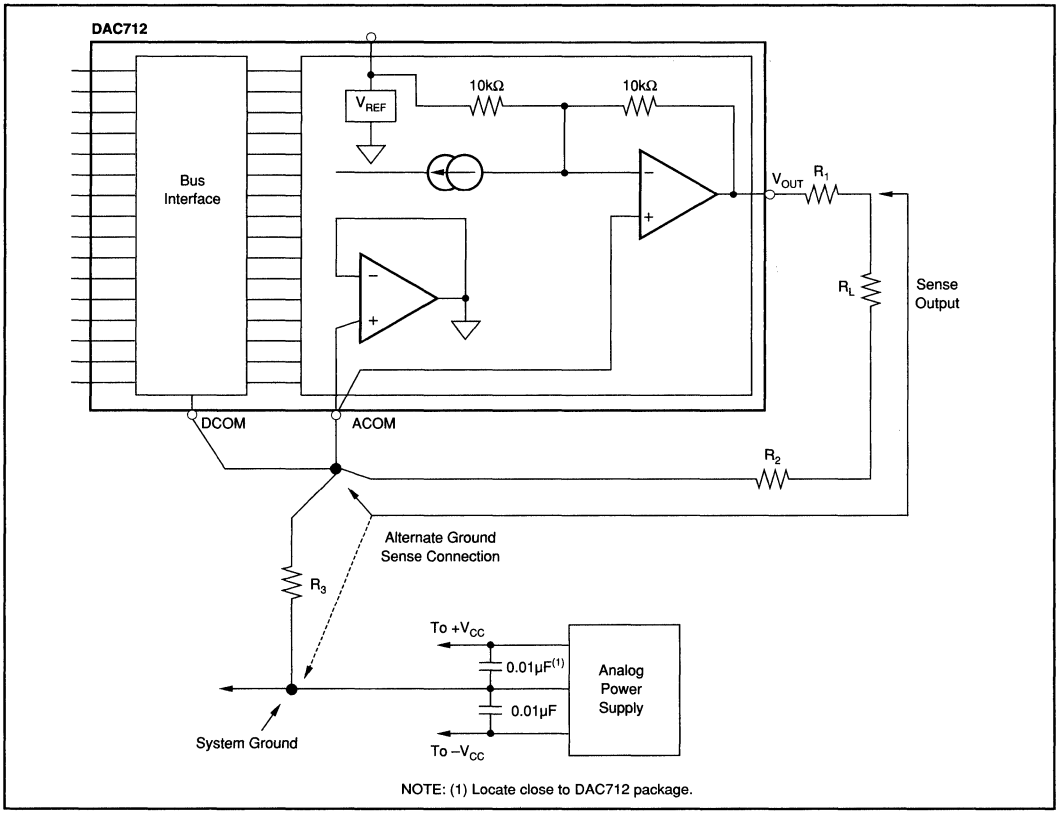


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

$\overline{A_0}$ is the enable control for the DATA INPUT LATCH. $\overline{A_1}$ is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by $\overline{A_0}$, and $\overline{A_1}$. Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

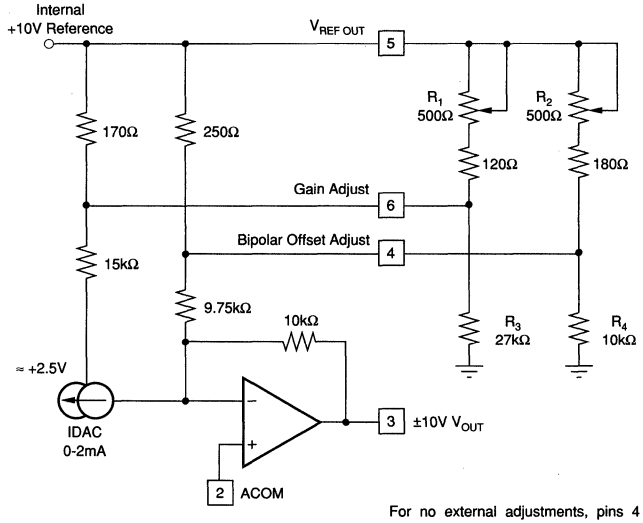
$\overline{CLR}$ sets the INPUT DATA LATCH to all zero and the D/A LATCH to a code that gives bipolar 0V at the D/A output.

SINGLE-BUFFERED OPERATION

To operate the DAC712 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting $\overline{A_0}$ to DCOM. If $\overline{A_1}$ is not used to enable the D/A, it should be connected to DCOM also. For this mode of operation, the width of $\overline{WR}$ will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

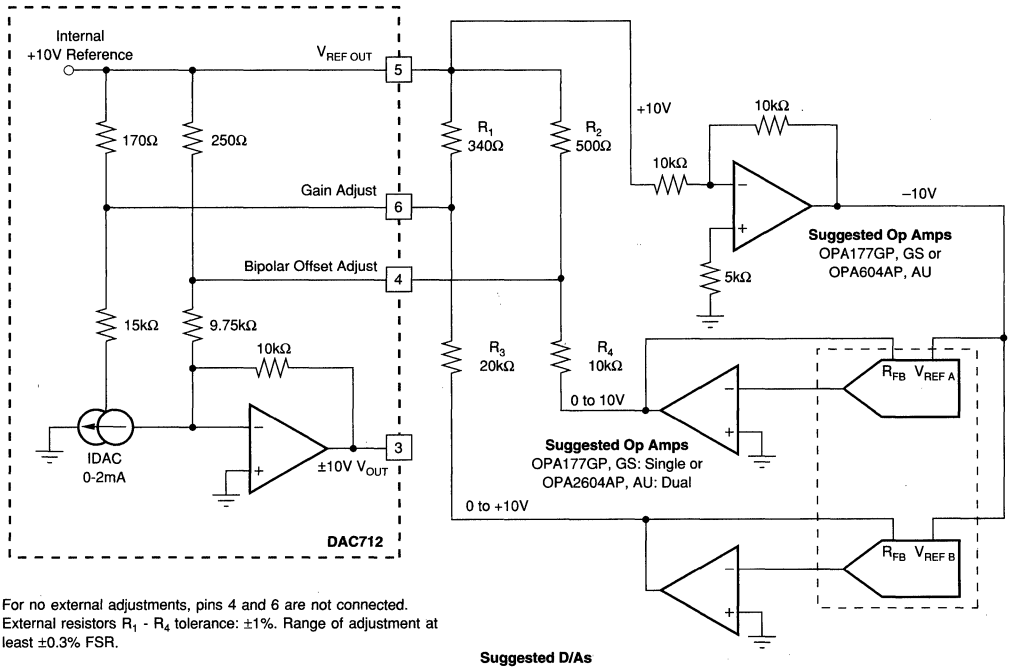
TRANSPARENT INTERFACE

The digital interface of the DAC712 can be made transparent by asserting $\overline{A_0}$, $\overline{A_1}$, and $\overline{WR}$ LOW, and asserting $\overline{CLR}$ HIGH.



For no external adjustments, pins 4 and 6 are not connected. External resistors R_1 - R_4 are standard ±1% values. Range of adjustment at least ±0.3% FSR.

FIGURE 6. Manual Offset and Gain Adjust Circuits.



For no external adjustments, pins 4 and 6 are not connected.
External resistors R_1 - R_4 tolerance: ±1%. Range of adjustment at least ±0.3% FSR.

Suggested D/As
CMOS
DAC7800: Dual: Serial Input, 12-bit Resolution
DAC7801: Dual: 8-bit Port Input, 12-bit Resolution
DAC7802: Dual: 12-bit Port Input, 12-bit Resolution
DAC7528: Dual: 8-bit Port Input, 8-bit Resolution
DAC7545: Dual: 12-bit Port Input, 12-bit Resolution
DAC8043: Single: Serial Input, 12-bit Resolution

BIPOLAR (complete)
DAC813 (Use 11-bit resolution for 0V to +10V output. No op amps required).

FIGURE 7. Gain and Offset Adjustment Using D/A Converters.

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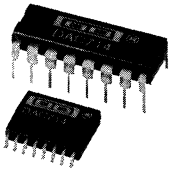


DAC714

16-Bit DIGITAL-TO-ANALOG CONVERTER With Serial Data Interface

FEATURES:

- SERIAL DIGITAL INTERFACE
- VOLTAGE OUTPUT: ±10V, ±5V, 0 to +10V
- ±1 LSB INTEGRAL LINEARITY
- 16-BIT MONOTONIC OVER TEMPERATURE
- PRECISION INTERNAL REFERENCE
- LOW NOISE: 120nV/√Hz Including Reference
- 16-LEAD PLASTIC AND CERAMIC SKINNY DIP AND PLASTIC SOIC PACKAGES

DESCRIPTION

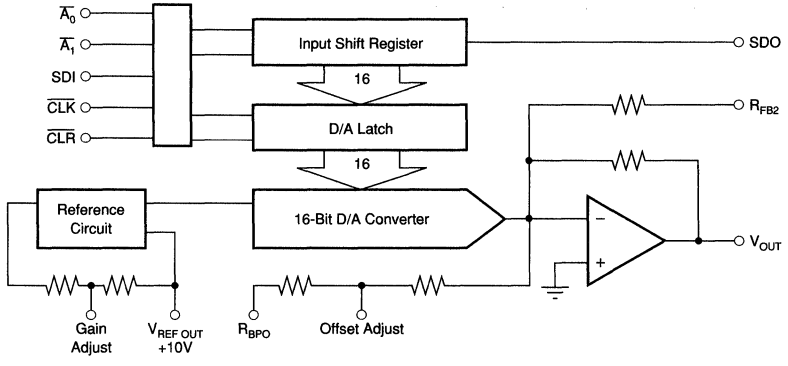
DAC714 is a complete monolithic D/A converter. A precision +10V temperature compensated voltage reference, ±10V voltage output amplifier and serial interface.

The serial digital interface is fast, 50ns max minimum write pulse width, and has a RESET function.

GAIN and BIPOLAR OFFSET adjustment are arranged so that they can be set by external D/A converters as well as by potentiometers.

DAC714 is packaged in a 16-pin plastic and ceramic skinny-DIP and in a 16-lead wide-body plastic SOIC.

The DAC714P, U, HB, and HC are specified over the –40°C to +85°C range and the DAC714HL is specified over the 0°C to +70°C range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

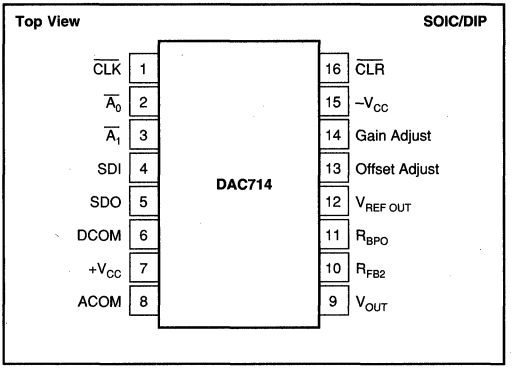
SPECIFICATIONS

At T_A = +25°C, +V_{CC} = +12V and +15V, –V_{CC} = –12V, and –15V, unless otherwise noted.

	DAC714P, U			DAC714HB			DAC714HC			DAC714HL			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error			±4			±2			±1			±1	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±2	LSB
Differential Linearity Error			±4			±2			±1			±1	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±1	LSB
Monotonicity	14			15			16			16			Bits
Monotonicity Over Spec Temp Range	13			14			15			16			Bits
Gain Error[3]			±0.1			±0.1			±0.1			±0.1	%
T_{MIN} to T_{MAX}			±0.25			±0.25			±0.25			±0.25	%
Unipolar/Bipolar Zero Error[3]			±0.1			±0.1			±0.1			±0.1	% of FSR[2]
T_{MIN} to T_{MAX}			±0.2			±0.2			±0.2			±0.2	% of FSR
Power Supply Sensitivity of Gain			±0.003			±0.003			±0.003			±0.003	%FSR/%V_{CC}
			±30			±30			±30			±30	ppm FSR/%V_{CC}
DYNAMIC PERFORMANCE													
Settling Time													
(to ±0.003%FSR, 5kΩ || 500pF Load)[4]													
20V Output Step		6	10		6	10		6	10		6	10	µs
1LSB Output Step[5]		4			4			4			4		µs
Output Slew Rate		10			10			10			10		V/µs
Total Harmonic Distortion													
0dB, 1001Hz, f_S = 100kHz		0.005			0.005			0.005			0.005		%
–20dB, 1001Hz, f_S = 100kHz		0.03			0.03			0.03			0.03		%
–60dB, 1001Hz, f_S = 100kHz		3.0			3.0			3.0			3.0		%
SINAD: 1001Hz, f_S = 100kHz		87			87			87			87		dB
Digital Feedthrough[5]		2			2			2			2		nV–s
Digital-to-Analog Glitch Impulse[5]		15			15			15			15		nV–s
Output Noise Voltage (includes reference)		120			120			120			120		nV/√Hz
ANALOG OUTPUT													
Output Voltage Range													
+V_{CC}, –V_{CC} = ±11.4V	±10			±10			±10			±10			V
Output Current	±5			±5			±5			±5			mA
Output Impedance		0.1			0.1			0.1			0.1		Ω
Short Circuit to ACOM Duration		Indefinite			Indefinite			Indefinite			Indefinite		
REFERENCE VOLTAGE													
Voltage	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	+9.975	+10.000	+10.025	V
T_{MIN} to T_{MAX}	+9.960		+10.040	+9.960		+10.040	+9.960		+10.040	+9.960		+10.040	V
Output Resistance		1			1			1			1		Ω
Source Current	2			2			2			2			mA
Short Circuit to ACOM Duration		Indefinite			Indefinite			Indefinite			Indefinite		
INTERFACE													
RESOLUTION		16			16			16			16		Bits
DIGITAL INPUTS													
Serial Data Input Code													
Logic Levels[1]						Binary Two's Complement							
V_{IH}	+2.0		(V_{CC} –1.4)	+2.0		(V_{CC} –1.4)	+2.0		(V_{CC} –1.4)	+2.0		(V_{CC} –1.4)	V
V_{IL}	0		+0.8	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_I = +2.7V)			±10			±10			±10			±10	µA
I_{IL} (V_I = +0.4V)			±10			±10			±10			±10	µA
DIGITAL OUTPUT													
Serial Data													
V_{OL} (I_{SINK} = 1.6mA)	0		+0.4	0		+0.4	0		+0.4	0		+0.4	V
V_{OH} (I_{SOURCE} = 500µA), T_{MIN} to T_{MAX}	+2.4		+5	+2.4		+5	+2.4		+5	+2.4		+5	V
POWER SUPPLY REQUIREMENTS													
Voltage													
+V_{CC}	+11.4	+15	+16.5	+11.4	+15	+16.5	+11.4	+15	+16.5	+11.4	+15	+16.5	V
–V_{CC}	–11.4	–15	–16.5	–11.4	–15	–16.5	–11.4	–15	–16.5	–11.4	–15	–16.5	V
Current (No Load, ±15V Supplies)[6]													
+V_{CC}		13	16		13	16		13	16		13	16	mA
–V_{CC}		22	26		22	26		22	26		22	26	mA
Power Dissipation[7]			625			625			625			625	mW
TEMPERATURE RANGES													
Specification													
All Grades	–40		+85	–40		+85	–40		+85	0		+70	°C
Storage	–60		+150	–60		+150	–60		+150	–60		+150	°C
Thermal Coefficient, θ_{JA}		75			75			75			75		°C/W

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst-case Binary Two's Complement code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. (6) During power supply turn on, the transient supply current may approach 3x the maximum quiescent specification. (7) Typical (i.e. rated) supply voltages times maximum currents.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	$\overline{CLK}$	Serial Data Clock
2	$\overline{A_0}$	Enable for Input Register (Active Low)
3	$\overline{A_1}$	Enable for D/A Latch (Active Low)
4	SDI	Serial Data Input
5	SDO	Serial Data Output
6	DCOM	Digital Supply Ground
7	$+V_{CC}$	Positive Power Supply
8	ACOM	Analog Supply Ground
9	V_{OUT}	D/A Output
10	R_{FB2}	±10V Range Feedback Output
11	R_{BPO}	Bipolar Offset
12	$V_{REF\ OUT}$	Voltage Reference Output
13	Offset Adjust	Offset Adjust
14	Gain Adjust	Gain Adjust
15	$-V_{CC}$	Negative Power Supply
16	$\overline{CLR}$	Clear

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to Common	0V to +17V
$-V_{CC}$ to Common	0V to –17V
$+V_{CC}$ to $-V_{CC}$	34V
ACOM to DCOM	±0.5V
Digital Inputs to Common	–1V to (V_{CC} –0.7V)
External Voltage Applied to BPO and Range Resistors	±V_{CC}
$V_{REF\ OUT}$	Indefinite Short to Common
V_{OUT}	Indefinite Short to Common
SDD	Indefinite Short to Common
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR max at +25°C	TEMPERATURE RANGE
DAC714P	Plastic DIP	±4 LSB	–40°C to +85°C
DAC714U	Plastic SOIC	±4 LSB	–40°C to +85°C
DAC714HB	Ceramic DIP	±2 LSB	–40°C to +85°C
DAC714HC	Ceramic DIP	±1 LSB	–40°C to +85°C
DAC714HL	Ceramic DIP	±1 LSB	0°C to +70°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC714P	Plastic DIP	180
DAC714U	Plastic SOIC	211
DAC714H	Ceramic DIP	129

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{CLK}	Data Clock Period	100		ns
t_{CL}	Clock LOW	50		ns
t_{CH}	Clock HIGH	50		ns
t_{A0S}	Setup Time for $\overline{A_0}$	50		ns
t_{A1S}	Setup Time for $\overline{A_1}$	50		ns
t_{AOH}	Hold Time for $\overline{A_0}$	0		ns
t_{A1H}	Hold Time for $\overline{A_1}$	0		ns
t_{DS}	Setup Time for DATA	50		ns
t_{DH}	Hold Time for DATA	10		ns
t_{DSOP}	Output Propagation Delay	140		ns
t_{CP}	Clear Pulsewidth	200		ns

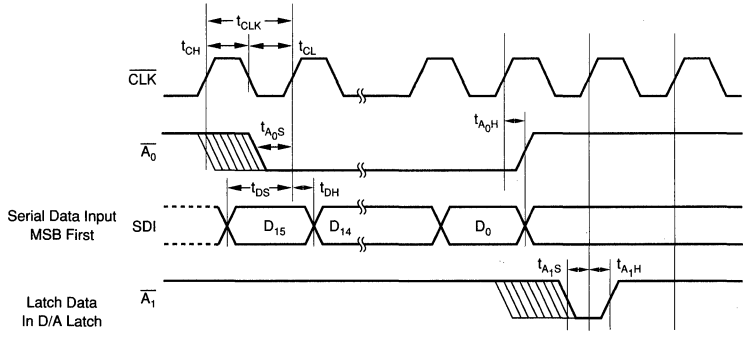
TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{CLK}$	$\overline{CLR}$	DESCRIPTION
0	1	1 → 0 → 1	1	Shift Serial Data into SDI
1	0	1 → 0 → 1	1	Load D/A Latch
1	1	1 → 0 → 1	1	No Change
0	0	1 → 0 → 1	1	Two Wire Operation(1)
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

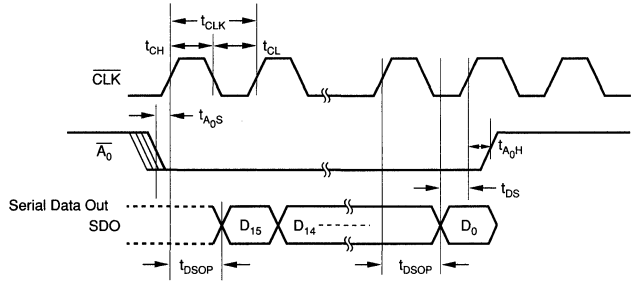
NOTES: X = Don't Care. (1) All digital input changes will appear at the output.

TIMING DIAGRAMS

Serial Data In



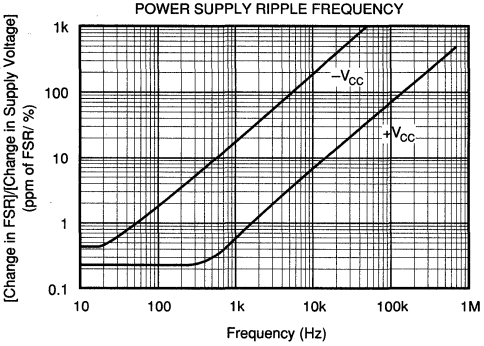
Serial Data Out



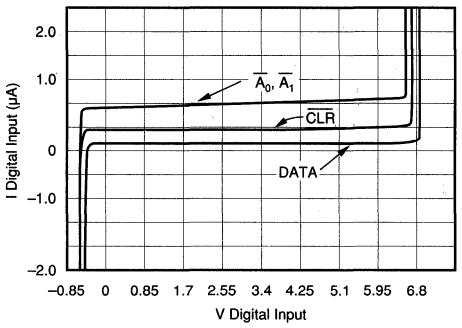
TYPICAL PERFORMANCE CURVES

AT T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

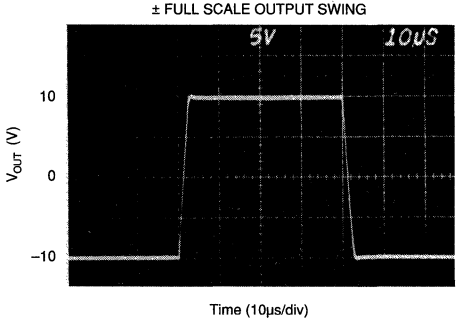
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



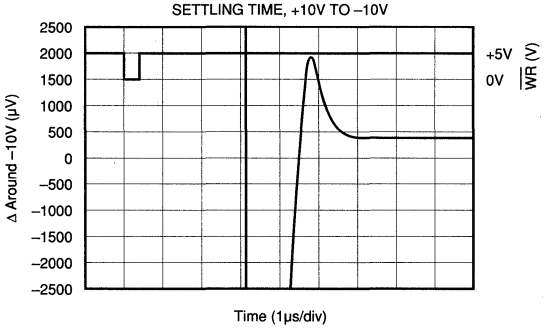
LOGIC vs V LEVEL



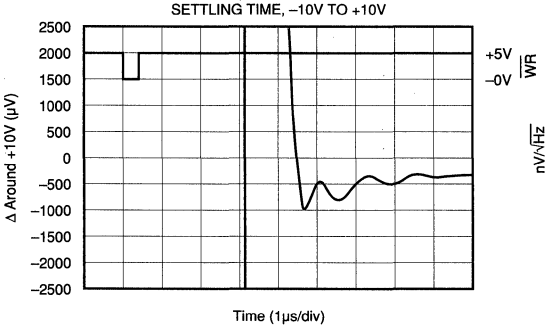
± FULL SCALE OUTPUT SWING



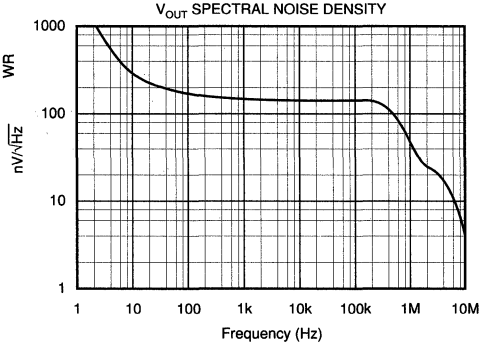
SETTLING TIME, +10V TO –10V



SETTLING TIME, –10V TO +10V



V_{OUT} SPECTRAL NOISE DENSITY



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC714 is guaranteed over the specification temperature range to 16 bits.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_{HEX}$ to 0000_{HEX}, and 0000_{HEX} to $FFFF_{HEX}$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from 0000_{HEX} to $FFFF_{HEX}$.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC714 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and a serial interface.

INTERFACE LOGIC

DAC714 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a bipolar zero output.

LOGIC INPUT COMPATIBILITY

DAC714 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic "0" and control inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC714 is designed to accept positive-true binary two's complement (BTC) input codes with the MSB first which are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of $7FFF_{HEX}$ produces a plus full scale output, 8000_{HEX} produces a minus full scale output, and 0000_{HEX} produces bipolar zero output.

INTERNAL REFERENCE

DAC714 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

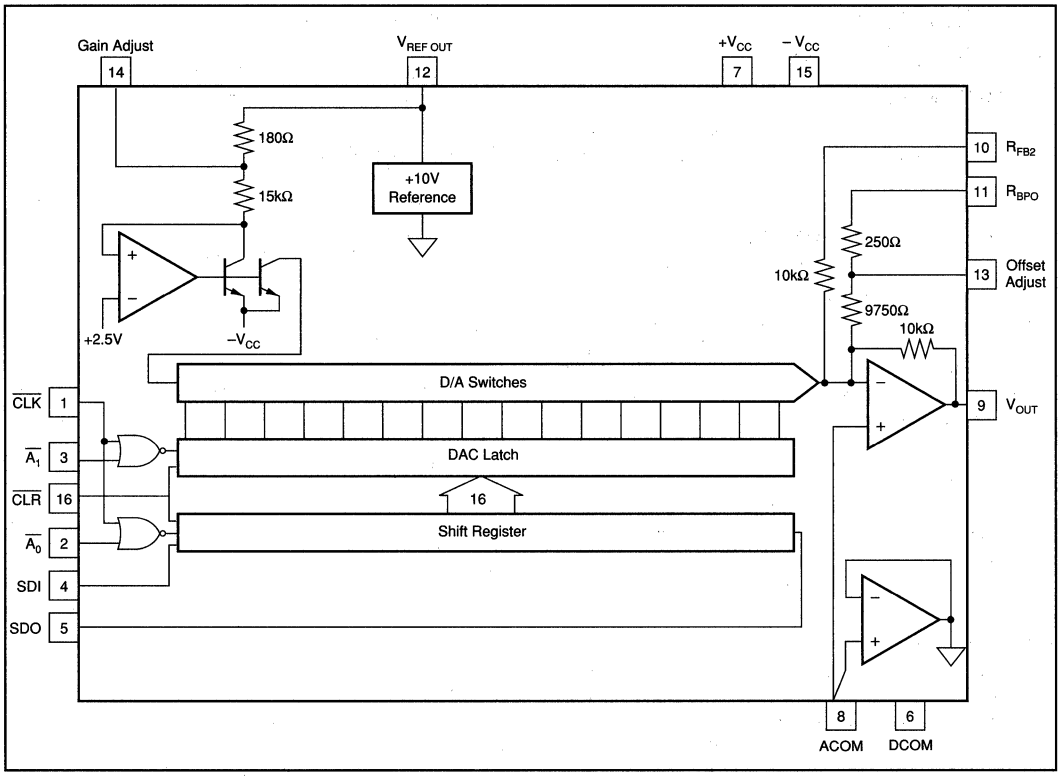


FIGURE 1. DAC714 Block Diagram.

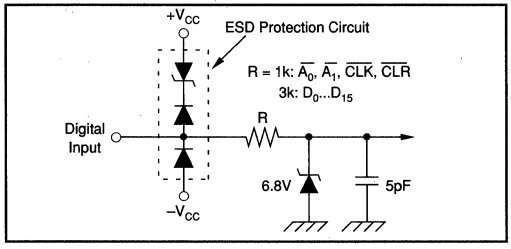


FIGURE 2. Equivalent Circuit of Digital Inputs.

OUTPUT VOLTAGE SWING

The output amplifier of DAC714 is designed to achieve a ±10V output range. DAC714 will provide a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

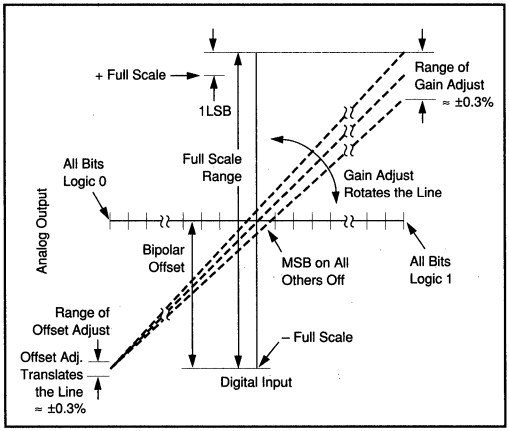


FIGURE 3. Relationship of Offset and Gain Adjustments.

Offset Adjustment

Apply the digital input code, 8000H, that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for –10V (or 0V unipolar).

DAC714 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 305μV			
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V) BIPOLAR 20V RANGE	ANALOG OUTPUT (V) UNIPOLAR 10V RANGE	DESCRIPTION
$7FFF_H$	+9.999695	+9.999847	+ Full Scale –1LSB
4000_H	+5.000000	+7.500000	3/4 Scale
0001_H	+0.000305	+5.000153	BPZ + 1LSB
0000_H	0.000000	+5.000000	Bipolar Zero (BPZ)
$FFFF_H$	–0.000305	+4.999847	BPZ – 1LSB
$C000_H$	–5.000000	+2.500000	1/4 Scale
8000_H	–10.00000	0.000000	Minus Full Scale

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

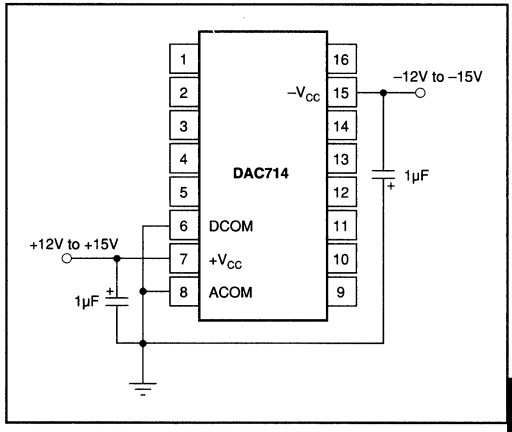


FIGURE 4. Power Supply Connections.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305μV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300μV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milliinch wide printed circuit conductor 60 milliinches long will result in a voltage drop of 150μV.

The analog output of DAC714 has an LSB size of 305μV (–96dB) in the bipolar mode. The rms noise floor of the D/A should remain below this level in the frequency range of interest. The DAC714's output noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10μF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01μF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

DAC714 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5μA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC714s are used or if DAC714 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because there is no change in DAC714 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC714 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC714 output amplifier is connected internally for 20V output range. That is, the 20V range resistor is connected internally to V_{OUT}, for other ranges and configurations, see Figures 6 and 7.

DIGITAL INTERFACE

SERIAL INTERFACE

The DAC714 has a serial interface with two data buffers which can be used for either synchronous or asynchronous updating of multiple D/A converters. $\overline{A0}$ is the enable control for the Data Input Latch. $\overline{A1}$ is the enable for the D/A Latch. $\overline{CLK}$ is used to strobe data into the latches enabled by $\overline{A0}$ and $\overline{A1}$. A $\overline{CLR}$ function is also provided and when enabled it sets the Data Latch to all zeros and the D/A Latch to a code that gives bipolar zero at the D/A output.

Multiple DAC714s can be connected to the same $\overline{CLK}$ and data lines in two ways. The output of the serial loaded data latch is available as SDO so that any number of DAC714s can be cascaded on the same input bit stream as shown in Figure 8 and 9. This configuration allows all D/A converters to be updated simultaneously and requires a minimum number of control signal inputs. These configurations do require 16N $\overline{CLK}$ cycles to load any given D/A converter, where N is the number of D/A converters.

The DAC714 can also be connected in parallel as shown in Figure 10. This configuration allows any D/A converter in the system to be updated in a maximum of 16 $\overline{CLK}$ cycles.

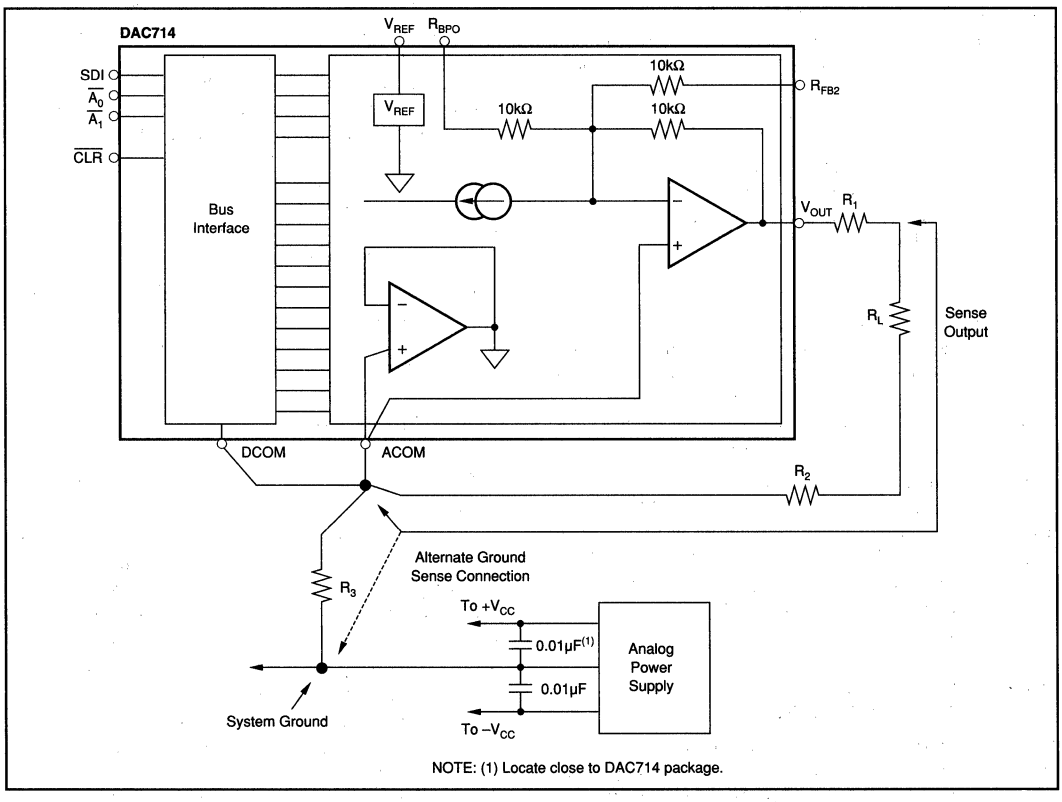


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

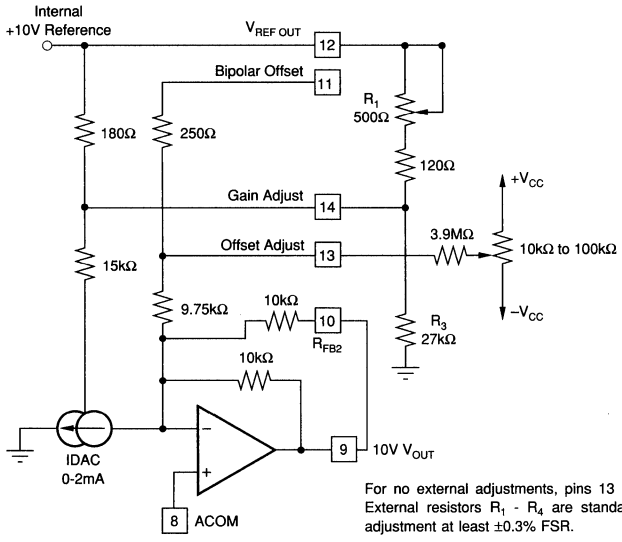


FIGURE 6a. Manual Offset and Gain Adjust Circuits; Unipolar Mode (0V to +10V output range).

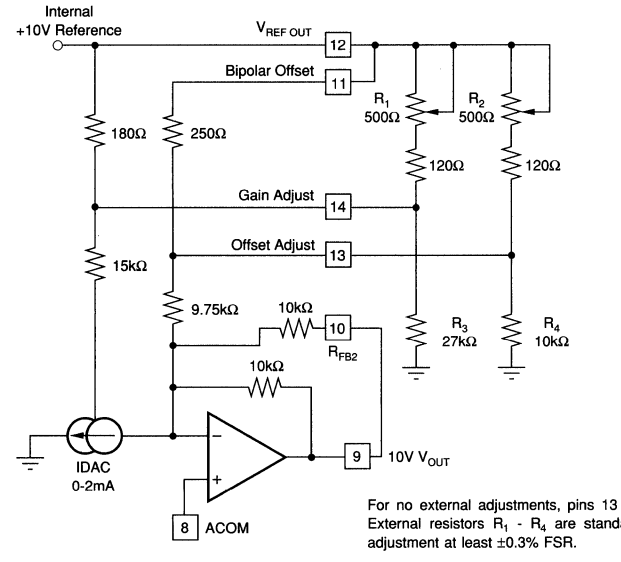
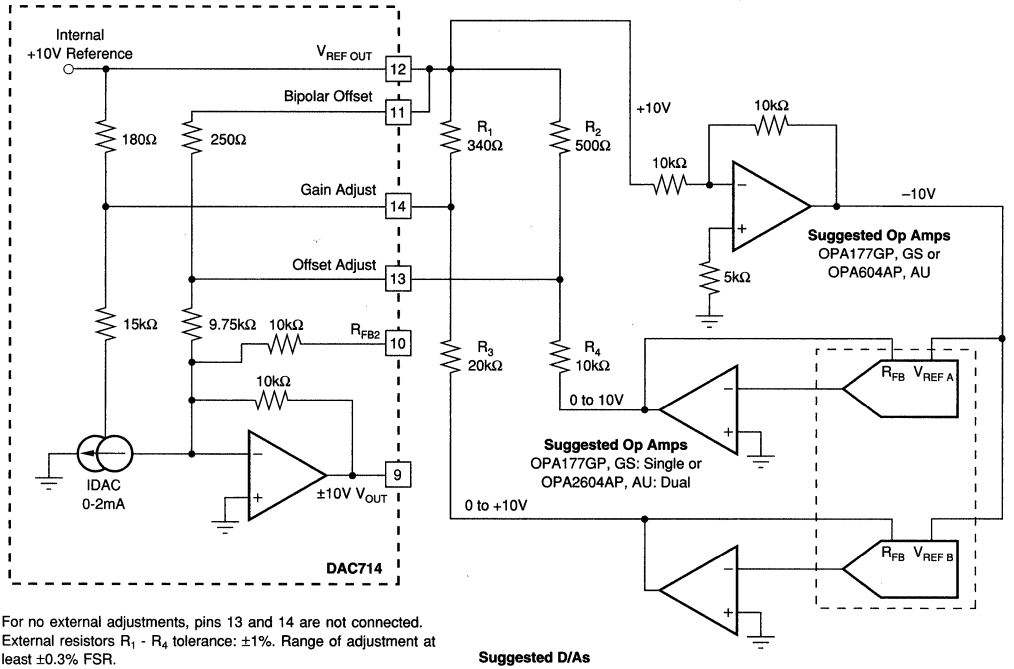


FIGURE 6b. Manual Offset and Gain Adjust Circuits; Bipolar Mode (–5V to +5V output range).



For no external adjustments, pins 13 and 14 are not connected.
External resistors R_1 - R_4 tolerance: ±1%. Range of adjustment at least ±0.3% FSR.

Suggested D/As

CMOS

DAC7800: Dual: Serial Input, 12-bit Resolution
DAC7801: Dual: 8-bit Port Input, 12-bit Resolution
DAC7802: Dual: 12-bit Port Input, 12-bit Resolution
DAC7528: Dual: 8-bit Port Input, 8-bit Resolution
DAC7545: Dual: 12-bit Port Input, 12-bit Resolution
DAC8043: Single: Serial Input, 12-bit Resolution

BIPOLAR (complete)

DAC813 (Use 11-bit resolution for 0V to +10V output. No op amps required).

FIGURE 7. Gain and Offset Adjustment in the Bipolar Mode Using D/A Converters (–10V to +10V output range).

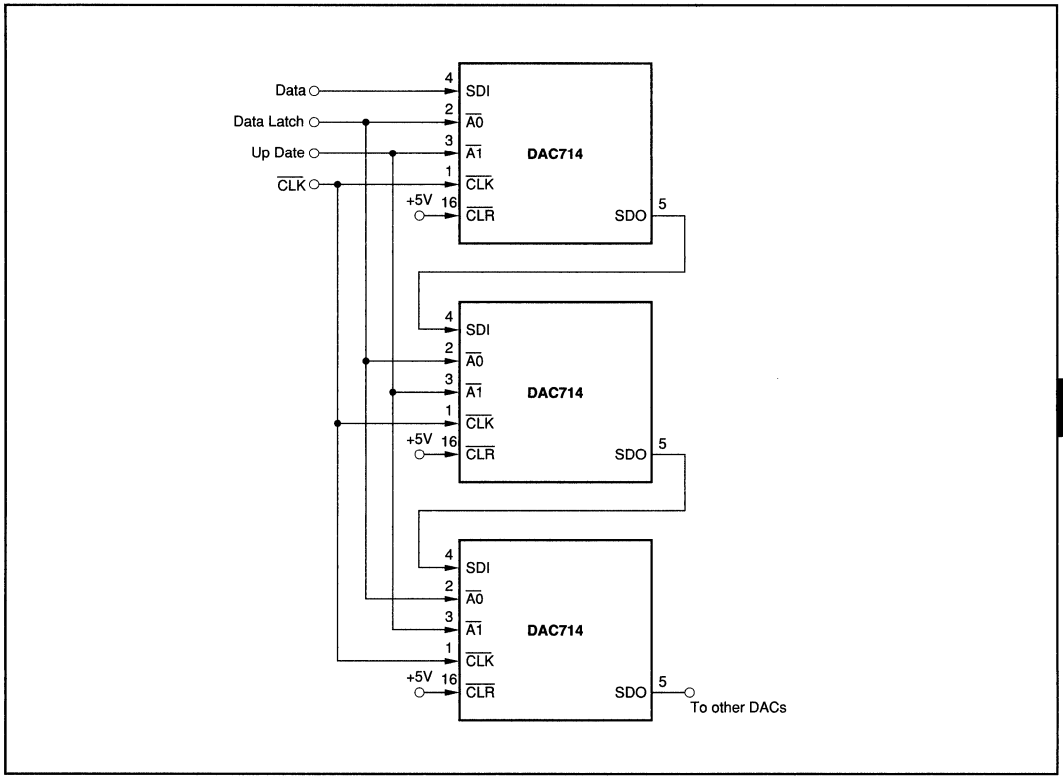


FIGURE 8a. Cascaded Serial Bus Connection with Synchronous Update.

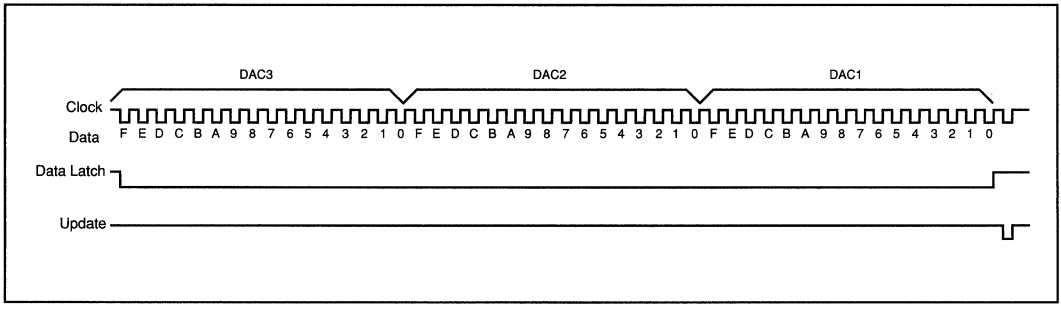


FIGURE 8b. Timing Diagram For Figure 8a.

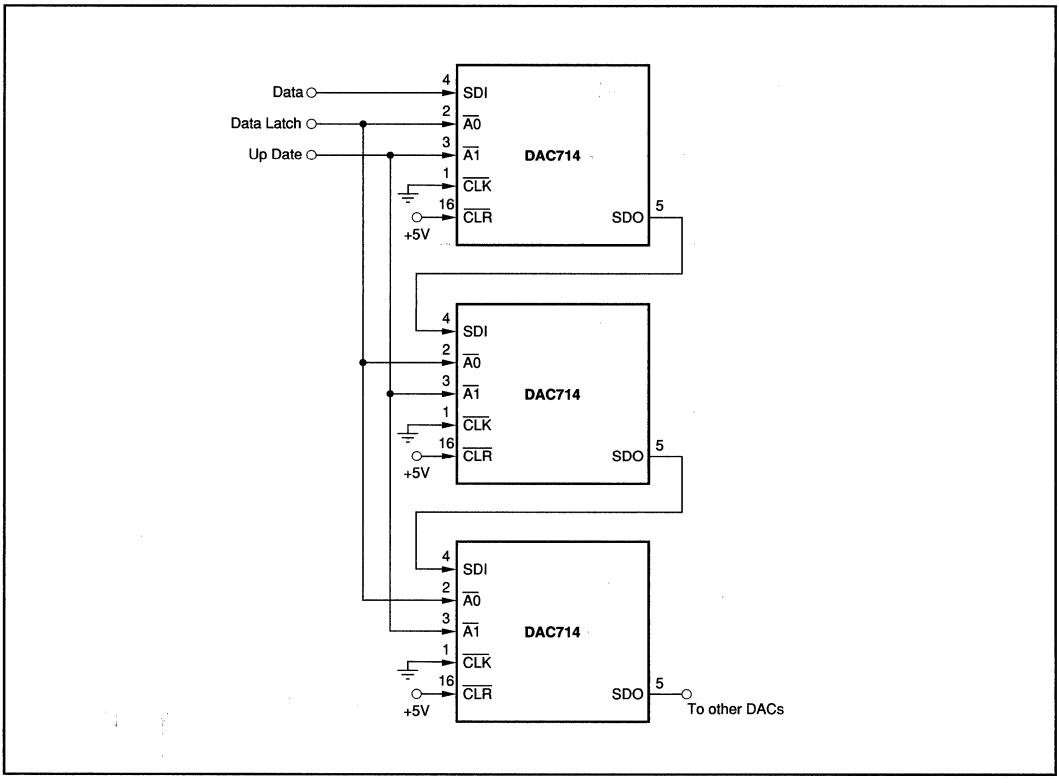


FIGURE 9a. Cascaded Serial Bus Connection with Asynchronous Update.

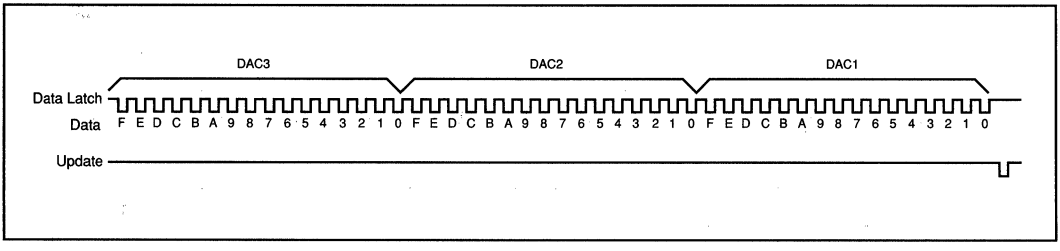


FIGURE 9b. Timing Diagram For Figure 9a.

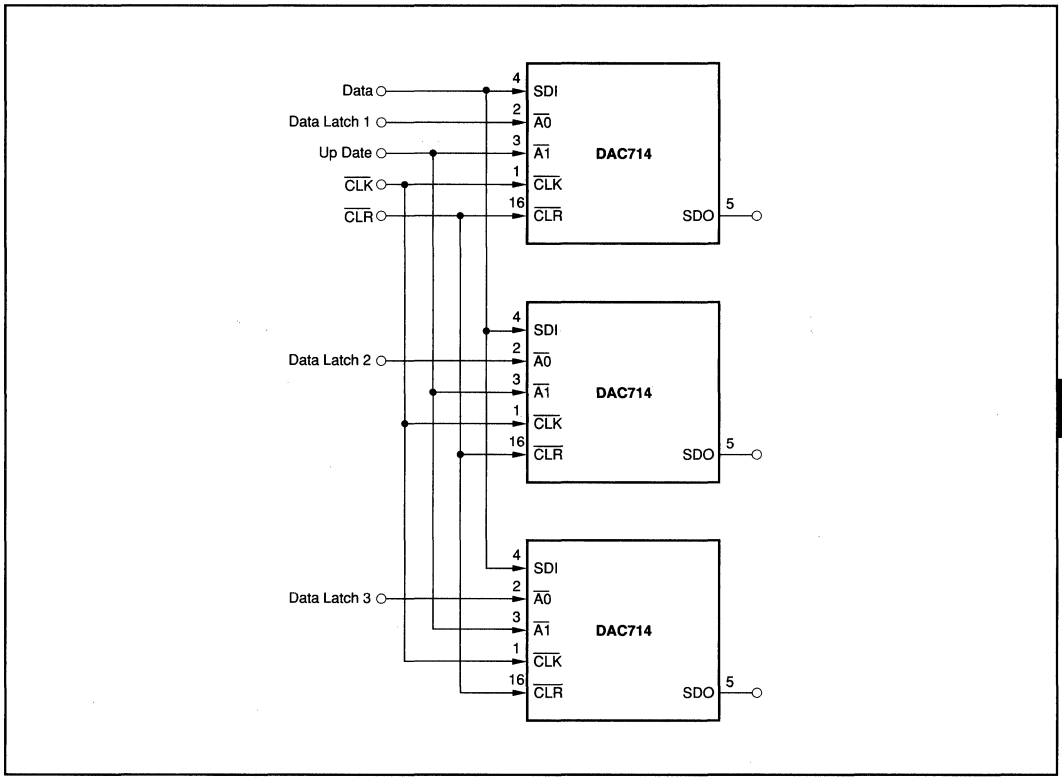


FIGURE 10a. Parallel Bus Connection.

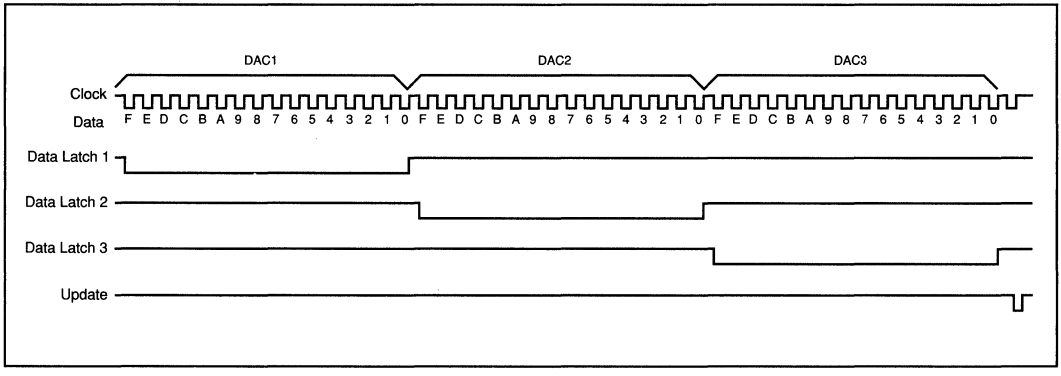


FIGURE 10b. Timing Diagram For Figure 10a.

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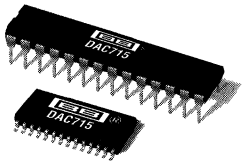


DAC715

16-Bit DIGITAL-TO-ANALOG CONVERTER with 16-Bit BUS Interface

FEATURES

- **HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE**
- **VOLTAGE OUTPUT: 0 to +10V**
- **13-, 14-, 15-BIT LINEARITY GRADES**
- **16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)**
- **POWER DISSIPATION: 600mW max**
- **GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters**
- **28-LEAD DIP AND SOIC PACKAGES**

DESCRIPTION

DAC715 is a complete 16-bit resolution D/A converter.

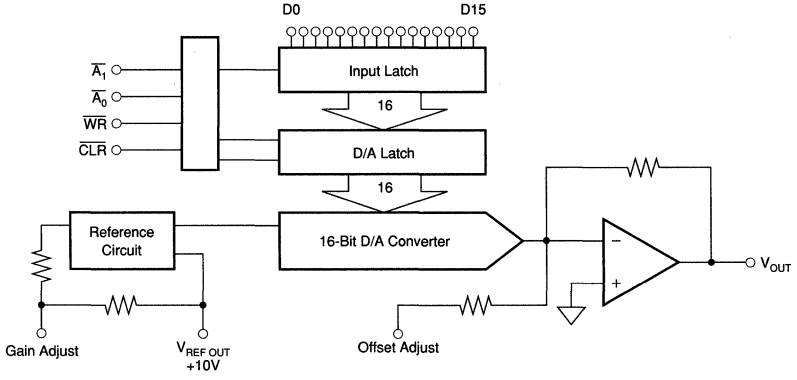
DAC715 has a precision +10V temperature compensated voltage reference, output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to half scale.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC715 is available in two linearity error performance grades: ±4LSB DAC715P and U, ±2LSB DAC715PB/PK/PL or UB/UK/UL. DAC715 is specified at power supply voltages of ±12V and ±15V.

DAC715 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. The DAC715P, DAC715U, DAC715PB, and DAC715UB are specified over the –40°C to +85°C temperature range, and the DAC715PK, DAC715UK, DAC715PL, and DAC715UL are specified from 0°C to +70°C.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, and after a 10-minute warm-up unless otherwise noted.

PARAMETER	DAC715P, U			DAC715PB, UB			DAC715PK, UK			DAC715PL, UL			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MAX	MIN	TYP	
INPUT													
RESOLUTION			16			*			*			*	Bits
DIGITAL INPUTS													
Input Code		Binary Two's Complement			*			*			*		
Logic Levels[1]: V_{IH}	+2.0		$+V_{CC}$ – 1.4	*		*	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	*		*	V
I_{IH} (V_I = +2.7V)			±10			*			*			*	µA
I_{IL} (V_I = +0.4V)			±10			*			*			*	µA
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error			±4			±2			±2			±2	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±2	LSB
Differential Linearity Error			±4			±2			±2			±1	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±1	LSB
Monotonicity Over Temp	13			14			15			16			Bits
Gain Error[3]			±0.1			±0.1			*			*	%
T_{MIN} to T_{MAX}			±0.2			±0.15			*			*	%
Offset Error[3]			±0.1			*			*			*	% FSR[2]
T_{MIN} to T_{MAX}			±0.2			*			*			*	% FSR
Power Supply Sensitivity Of Full Scale			±0.003			*			*			*	% FSR/%V_{CC}
			±30			*			*			*	PPM FSR/%V_{CC}
DYNAMIC PERFORMANCE													
Settling Time (to ±0.003%FSR, 5kΩ II 500pF Load)[4]													
10V Output Step		6	10		*	*		*	*		*	*	µs
1 LSB Output Step[5]		4			*			*			*		µs
Output Slew Rate		10			*			*			*		V/µs
Total Harmonic Distortion + Noise													
0dB, 1001Hz, f_S = 100kHz		0.005			*			*			*		%
–20dB, 1001Hz, f_S = 100kHz		0.03			*			*			*		%
–60dB, 1001Hz, f_S = 100kHz		3.0			*			*			*		%
SINAD													
1001Hz, f_S = 100kHz		87			*			*			*		dB
Digital Feedthrough[5]		2			*			*			*		nV-s
Digital-to-Analog Glitch Impulse[5]		15			*			*			*		nV-s
Output Noise Voltage (includes Reference)		120			*			*			*		nV√Hz
ANALOG OUTPUT													
Output Voltage Range													
$+V_{CC}$, $-V_{CC}$ = ±11.4V	0 to +10			*			*			*			V
Output Current	±5			*			*			*			mA
Output Impedance		0.1			*			*			*		Ω
Short Circuit to ACOM													
Duration		Indefinite			*			*			*		
REFERENCE VOLTAGE													
Voltage	+9.975	+10.000	+10.025	*	*	*	*	*	*	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*	*	*	*	*	*	*	*	*	V
Output Resistance		1			*			*			*		Ω
Source Current	2			*			*			*			mA
Short Circuit to ACOM, Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	–16.5	–15	–11.4	*	*	*	*	*	*	*	*	*	V
Current (no load, ±15V Supplies)													
$+V_{CC}$		13	15		*	*		*	*		*	*	mA
$-V_{CC}$		22	25		*	*		*	*		*	*	mA
Power Dissapation[6]		525	600		*	*		*	*		*	*	mW
TEMPERATURE RANGE													
Specification All Grades	–40		+85	*		*	0		+70	*		*	°C
Storage	–60		+150	*		*	*		*	*		*	°C
Thermal Resistance θ_{JA}													
DIP Package		75			*			*			*		°C/W
SOIC Package		75			*			*			*		°C/W

*Specifications are the same as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a 0 to +10V output, FSR = 10V. (3) Errors externally adjustable to zero. (4) Maximum represents greater than the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V, +17V
$-V_{CC}$ to COMMON	0V, –17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	–1V to $+V_{CC}$
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

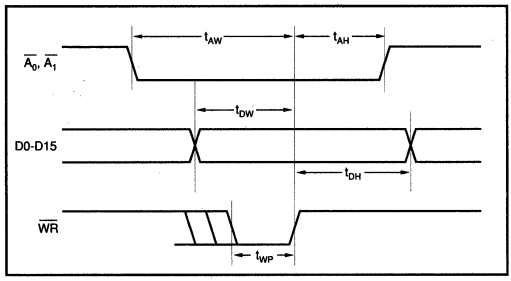
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC715P	Plastic DIP	246
DAC715U	Plastic SOIC	217
DAC715PB	Plastic DIP	246
DAC715UB	Plastic SOIC	217
DAC715PK	Plastic DIP	246
DAC715UK	Plastic SOIC	217
DAC715PL	Plastic DIP	246
DAC715UL	Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	DIFFERENTIAL LINEARITY ERROR MAX at +25°C
DAC715P	Plastic DIP	–40°C to +85°C	±4LSB
DAC715U	Plastic SOIC	–40°C to +85°C	±4LSB
DAC715PB	Plastic DIP	–40°C to +85°C	±2LSB
DAC715UB	Plastic SOIC	–40°C to +85°C	±2LSB
DAC715PK	Plastic DIP	0°C to 70°C	±2LSB
DAC715UK	Plastic SOIC	0°C to 70°C	±2LSB
DAC715PL	Plastic DIP	0°C to 70°C	±1LSB
DAC715UL	Plastic SOIC	0°C to 70°C	±1LSB

TIMING DIAGRAM



TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	50		ns
t_{AW}	$\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$	50		ns
t_{AH}	$\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$	10		ns
t_{DH}	Data Hold after end of $\overline{WR}$	10		ns
t_{WP}(1)	Write Pulse Width	50		ns
t_{CP}	CLEAR Pulse Width	200		ns

NOTES: (1) For single-buffered operation, t_{WP} is 80ns min. Refer to page 10.

TRUTH TABLE

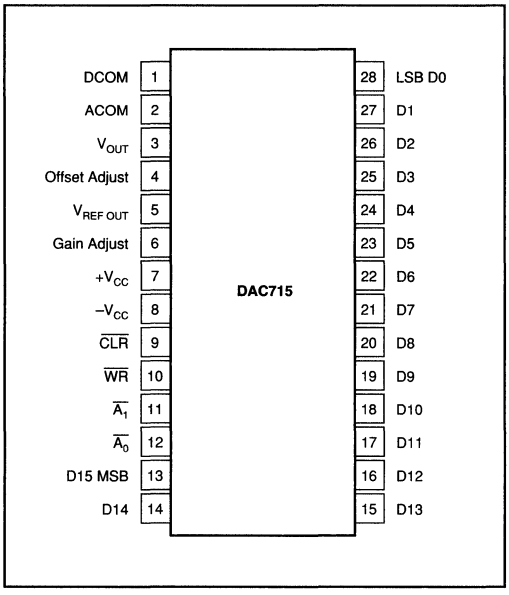
$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	1 → 0 → 1	1	Load Input Latch
1	0	1 → 0 → 1	1	Load D/A Latch
1	1	1 → 0 → 1	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



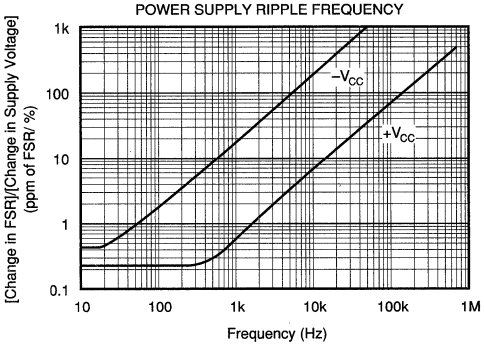
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Power Supply return for digital currents.
2	ACOM	Analog Supply Return.
3	V_{OUT}	0 to +10V D/A Output.
4	Offset Adjust	Offset Adjust.
5	$V_{REF\ OUT}$	Voltage Reference Output.
6	Gain Adjust	Gain Adjust.
7	$+V_{CC}$	+12V to +15V Supply.
8	$-V_{CC}$	–12V to –15V Supply.
9	$\overline{CLR}$	CLEAR. Sets D/A output to Half Scale (Active Low).
10	$\overline{WR}$	Write (Active Low).
11	$\overline{A_1}$	Enable for D/A latch (Active Low).
12	$\overline{A_0}$	Enable for Input latch (Active Low).
13	D15	Data Bit 15 (Most Significant Bit).
14	D14	Data Bit 14.
15	D13	Data Bit 13.
16	D12	Data Bit 12.
17	D11	Data Bit 11.
18	D10	Data Bit 10.
19	D9	Data Bit 9.
20	D8	Data Bit 8.
21	D7	Data Bit 7.
22	D6	Data Bit 6.
23	D5	Data Bit 5.
24	D4	Data Bit 4.
25	D3	Data Bit 3.
26	D2	Data Bit 2.
27	D1	Data Bit 1.
28	D0	Data Bit 0 (Least Significant Bit).

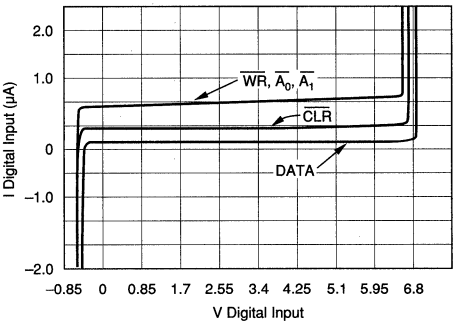
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_{CC} = ±15V unless otherwise noted.

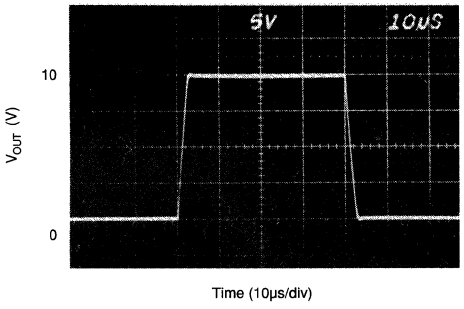
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



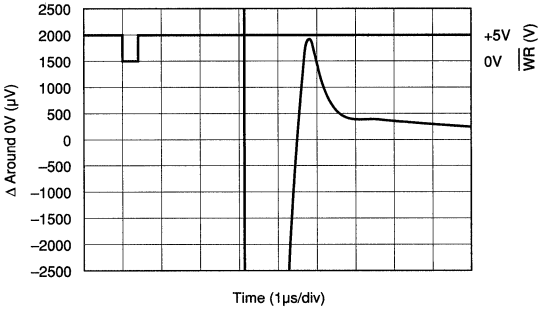
LOGIC vs V LEVEL



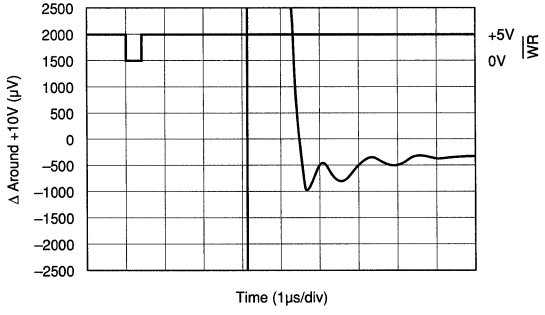
FULL SCALE OUTPUT SWING



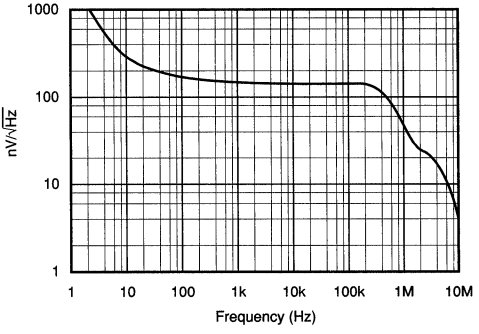
SETTLING TIME, +10V TO 0V



SETTLING TIME, 0V TO +10V



SPECTRAL NOISE DENSITY



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC715 is guaranteed over the specification temperature range to 13-, 14-, 15-, and 16-bits for performance grades DAC715P/U, DAC715PB/UB, DAC715PK/UK, and DAC715PL/UL respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 10V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_H$ to 0000_H, and 0000_H to $FFFF_H$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from $FFFF_H$ to 0000_H.

DIGITAL FEEDTHROUGH

When the D/A is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC715 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

DAC715 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a half scale output.

LOGIC INPUT COMPATIBILITY

DAC715 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic "0" and control inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC715 is designed to accept positive-true binary two's complement (BTC) input codes. For unipolar analog output configuration, a digital input of $7FFF_H$ gives a full scale output, 8000_H gives a zero output, and 0000_H gives half scale output.

INTERNAL REFERENCE

DAC715 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain of the converter will vary.

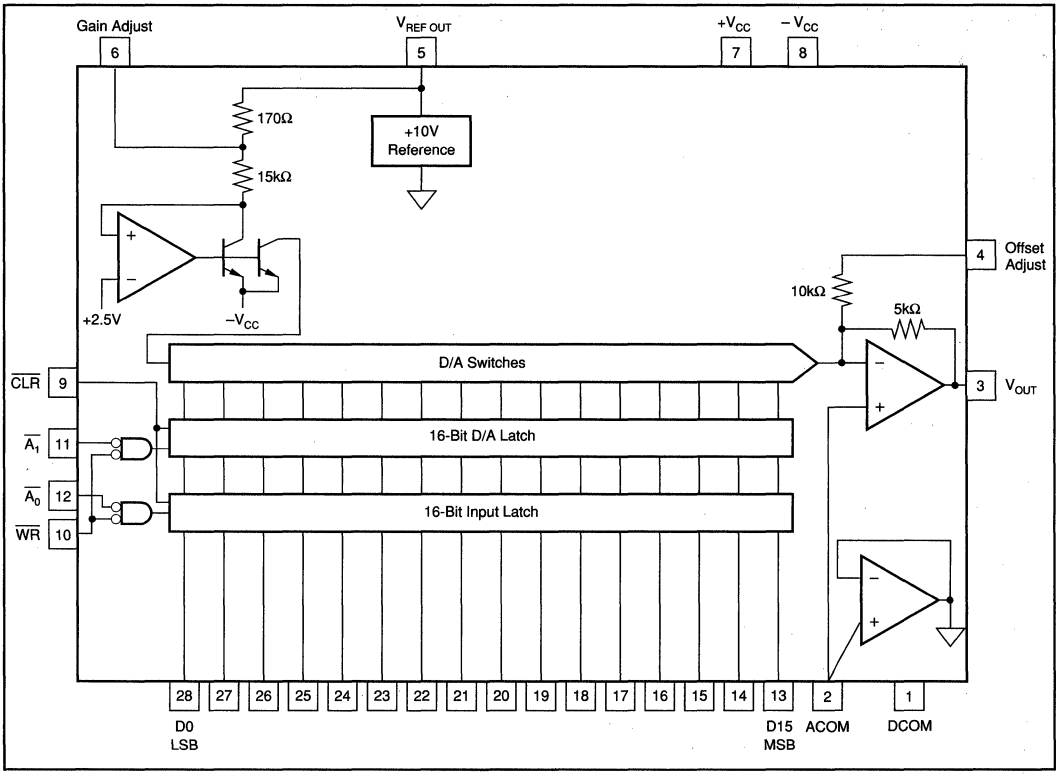


FIGURE 1. DAC715 Block Diagram.

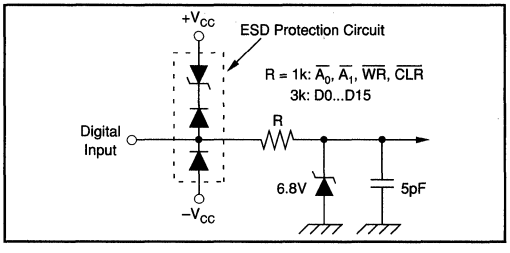


FIGURE 2. Equivalent Circuit of Digital Inputs.

OUTPUT VOLTAGE SWING

The output amplifier of DAC715 is committed to a 0 to +10V output range. DAC715 will provide a 0 to +10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a unipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

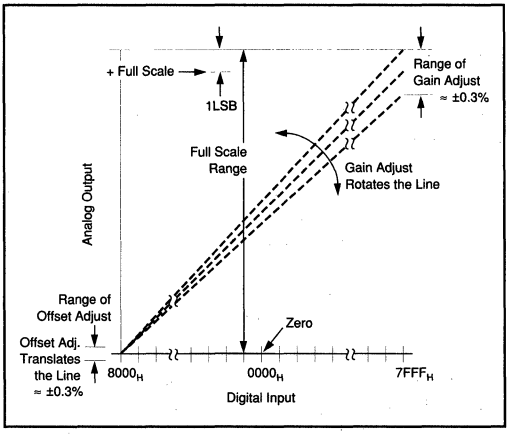


FIGURE 3. Relationship of Offset and Gain Adjustments.

Offset Adjustment

Apply the digital input code that produces zero output voltage and adjust the offset potentiometer or the offset adjust D/A converter for 0V.

DAC715 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 152µV		
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V)	DESCRIPTION
$7FFF_H$	9.999847	Full Scale –1LSB
4000_H	7.5	3/4 Scale
0001_H	5.000152	Half Scale + 1LSB
0000_H	5	Half Scale
$FFFF_H$	4.999847	Half Scale – 1LSB
$C000_H$	2.5	1/4 Scale
8000_H	0	Zero

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of 152µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milliinch wide printed circuit conductor 60 milliinches long will result in a voltage drop of 150µV.

The analog output of DAC715 has an LSB size of 152µV (–96dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC715's noise spectral density (which includes the noise contributed by the internal reference) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

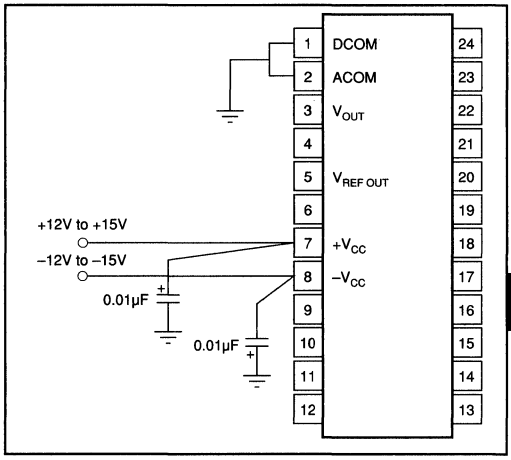


FIGURE 4. Power Supply Connections.

DAC715 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC715s are used or if DAC715 shares supplies with other components, connecting the ACOM and DCOM lines together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because

there is no change in DAC715 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC715 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, 0V.

DIGITAL INTERFACE

BUS INTERFACE

DAC715 has 16-bit double-buffered data bus interface with control lines for easy interface to interface to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.

$\overline{A_0}$ is the enable control for the DATA INPUT LATCH. $\overline{A_1}$ is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by $\overline{A_0}$, and $\overline{A_1}$. Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

$\overline{CLR}$ sets the INPUT DATA LATCH to zeros and the D/A LATCH to a code that gives half scale 5V at the D/A output.

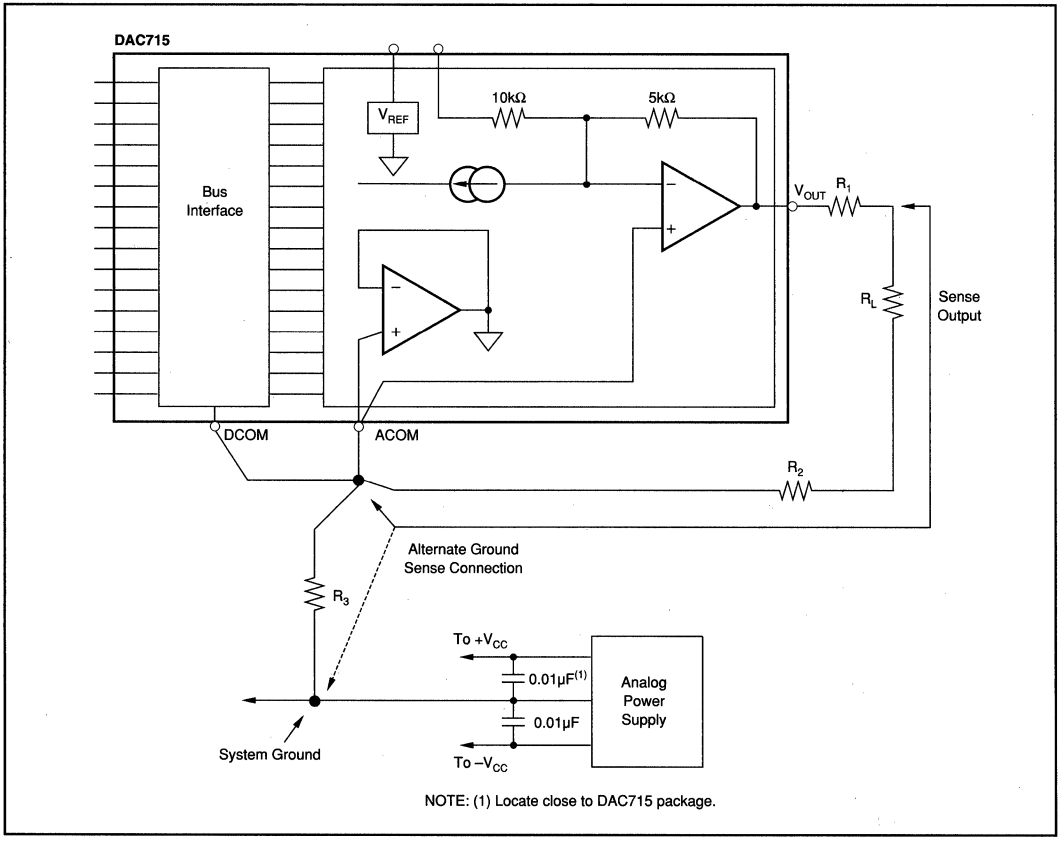


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

SINGLE-BUFFERED OPERATION

To operate the DAC715 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting $\overline{A_0}$ to DCOM. If $\overline{A_1}$ is not used to enable the D/A, it should be connected to DCOM also. For this mode of operation, the width of $\overline{WR}$ will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

TRANSPARENT INTERFACE

The digital interface of the DAC715 can be made transparent by asserting $\overline{A_0}$, $\overline{A_1}$, and $\overline{WR}$ LOW, and asserting $\overline{CLR}$ HIGH.

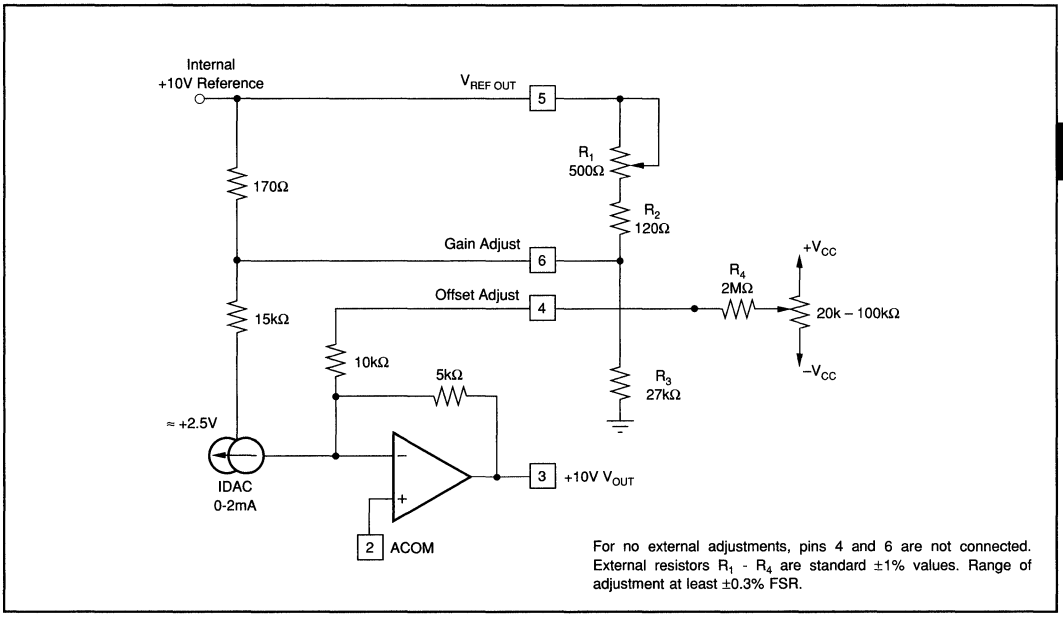


FIGURE 6. Manual Offset and Gain Adjust Circuits.

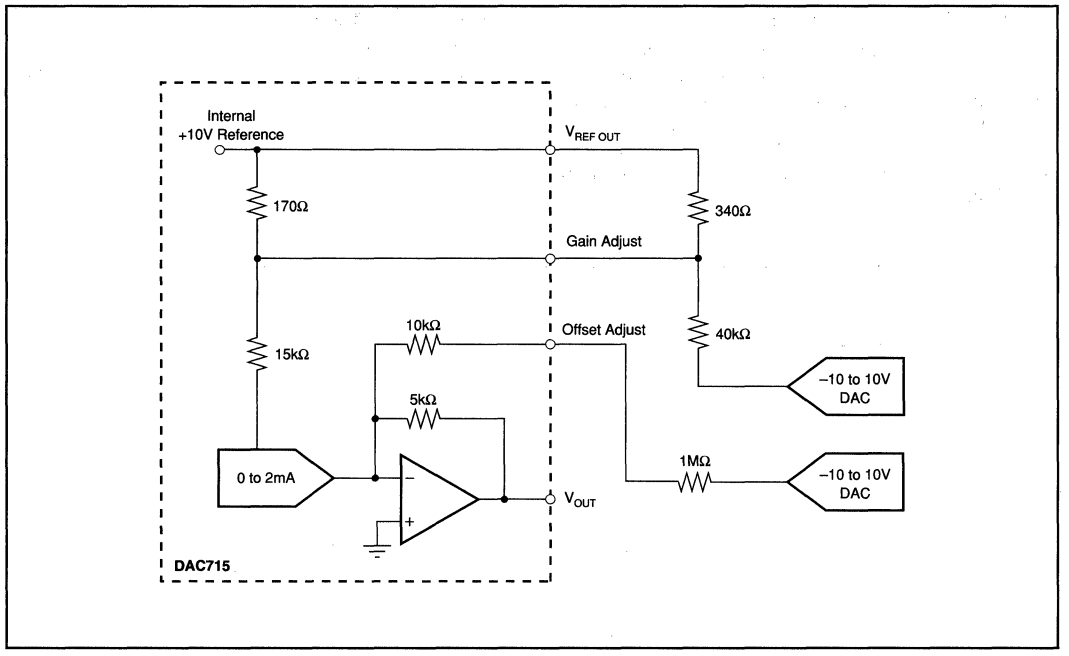


FIGURE 7. Gain and Offset Adjustment Using D/A Converters.

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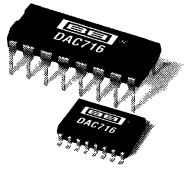


DAC716

16-Bit DIGITAL-TO-ANALOG CONVERTER with Serial Data Interface

FEATURES:

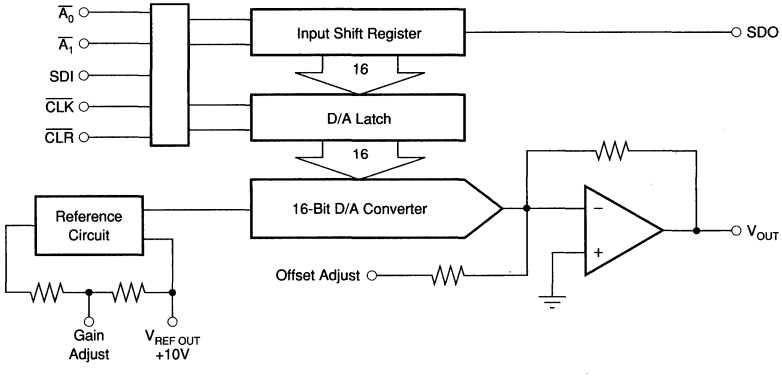
- SERIAL DIGITAL INTERFACE
- VOLTAGE OUTPUT: 0 to +10V
- ±2 LSB INTEGRAL LINEARITY
- 16-BIT MONOTONIC OVER TEMPERATURE
- PRECISION INTERNAL REFERENCE
- LOW NOISE: 120nV/√Hz Including Reference
- 16-LEAD PLASTIC SKINNY DIP AND PLASTIC SOIC PACKAGES

DESCRIPTION

The DAC716 is a complete monolithic D/A converter including a +10V temperature compensated voltage reference, current-to-voltage amplifier, a high-speed synchronous serial interface, a serial output which allows cascading multiple converters, and an asynchronous clear function which immediately sets the output voltage to zero.

The output voltage range is 0 to +10V while operating from ±12V to ±15V supplies, and the gain and bipolar offset adjustments are designed so that they can be set via external potentiometers or external D/A converters. The output amplifier is protected against short-circuiting to ground.

The 16-pin DAC716 is available in a plastic 0.3" DIP and a wide-body plastic SOIC package. The DAC716P, U, PB, and UB are specified over the –40°C to +85°C range while the DAC716UK, PK, UL, and PL are specified over the 0°C to +70°C range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

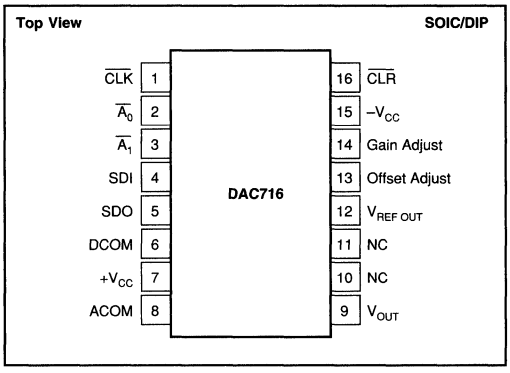
At T_A = +25°C, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, unless otherwise noted.

PARAMETER	DAC716P, U			DAC716PB, UB			DAC716PK, UK			DAC716PL, UL			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error			±4			±2			±2			±2	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±2	LSB
Differential Linearity Error			±4			±2			±1			±1	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±1	LSB
Monotonicity	14			15			16			16			Bits
Monotonicity Over Spec Temp Range	13			14			15			16			Bits
Gain Error[3]			±0.1			*			*			*	%
T_{MIN} to T_{MAX}			±0.25			*			*			*	%
Unipolar Zero Error[3]			±0.1			*			*			*	% of FSR[2]
T_{MIN} to T_{MAX}			±0.2			*			*			*	% of FSR
Power Supply Sensitivity of Gain			±0.003			*			*			*	%FSR/%V_{CC}
			±30			*			*			*	ppm FSR/%V_{CC}
DYNAMIC PERFORMANCE													
Settling Time													
(to ±0.003%FSR, 5kΩ || 500pF Load)[4]													
20V Output Step		6	10		*	*		*	*		*	*	µs
1LSB Output Step[5]		4			*			*			*		µs
Output Slew Rate		10			*			*			*		V/µs
Total Harmonic Distortion													
0dB, 1001Hz, f_S = 100kHz		0.005			*			*			*		%
−20dB, 1001Hz, f_S = 100kHz		0.03			*			*			*		%
−60dB, 1001Hz, f_S = 100kHz		3.0			*			*			*		%
SINAD: 1001Hz, f_S = 100kHz		87			*			*			*		dB
Digital Feedthrough[5]		2			*			*			*		nV–s
Digital-to-Analog Glitch Impulse[5]		15			*			*			*		nV–s
Output Noise Voltage (includes reference)		120			*			*			*		nV/√Hz
ANALOG OUTPUT													
Output Voltage Range													
$+V_{CC}$, $-V_{CC}$ = ±11.4V	+10			*			*			*			V
Output Current	±5			*			*			*			mA
Output Impedance		0.1			*			*			*		Ω
Short Circuit to ACOM Duration		Indefinite			*			*			*		
REFERENCE VOLTAGE													
Voltage	+9.975	+10.000	+10.025	*	*	*	*	*	*	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	*		*	*		*	V
Output Resistance		1			*			*			*		Ω
Source Current	2			*			*			*			mA
Short Circuit to ACOM Duration		Indefinite			*			*			*		
INTERFACE													
RESOLUTION		16			*			*			*		Bits
DIGITAL INPUTS													
Serial Data Input Code													
Logic Levels[1]						Straight Binary							
V_{IH}	+2.0		(V_{CC} −1.4)	*		*	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	*		*	V
I_{IH} (V_I = +2.7V)			±10			*			*			*	µA
I_{IL} (V_I = +0.4V)			±10			*			*			*	µA
DIGITAL OUTPUT													
Serial Data													
V_{OL} (I_{SINK} = 1.6mA)	0		+0.4	*		*	*		*	*		*	V
V_{OH} (I_{SOURCE} = 500µA), T_{MIN} to T_{MAX}	+2.4		+5	*		*	*		*	*		*	V
POWER SUPPLY REQUIREMENTS													
Voltage													
$+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	−11.4	−15	−16.5	*	*	*	*	*	*	*	*	*	V
Current (No Load, ±15V Supplies)[6]													
$+V_{CC}$		13	16		*	*		*	*		*	*	mA
$-V_{CC}$		22	26		*	*		*	*		*	*	mA
Power Dissipation[7]			625			*			*			*	mW
TEMPERATURE RANGES													
Specification													
All Grades	−40		+85	*		*	0		+70	*		*	°C
Storage	−60		+150	*		*	*		*	*		*	°C
Thermal Coefficient, θ_{JA}		75			*			*			*		°C/W

*Specifications are the same as the grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for 0 to +10V output, FSR = 10V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst-case Straight Binary code changes: 7FFF to 8000 and 8000 to 7FFF. (6) During power supply turn on, the transient supply current may approach 3x the maximum quiescent specification. (7) Typical (i.e. rated) supply voltages times maximum currents.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	$\overline{CLK}$	Serial Data Clock
2	$\overline{A_0}$	Enable for Input Register (Active Low)
3	$\overline{A_1}$	Enable for D/A Latch (Active Low)
4	SDI	Serial Data Input
5	SDO	Serial Data Output
6	DCOM	Digital Supply Ground
7	$+V_{CC}$	Positive Power Supply
8	ACOM	Analog Supply Ground
9	V_{OUT}	D/A Output
10	NC	No Connection
11	NC	No Connection
12	$V_{REF\ OUT}$	Voltage Reference Output
13	Offset Adjust	Offset Adjust
14	Gain Adjust	Gain Adjust
15	$-V_{CC}$	Negative Power Supply
16	$\overline{CLR}$	Clear

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to Common	0V to +17V
$-V_{CC}$ to Common	0V to –17V
$+V_{CC}$ to $-V_{CC}$	34V
ACOM to DCOM	±0.5V
Digital Inputs to Common	–1V to (V_{CC} –0.7V)
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to Common
V_{OUT}	Indefinite Short to Common
SDO	Indefinite Short to Common
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	DIFFERENTIAL LINEARITY ERROR T_{MIN} to T_{MAX}	TEMPERATURE RANGE
DAC716P	Plastic DIP	±8 LSB	–40°C to +85°C
DAC716U	Plastic SOIC	±8 LSB	–40°C to +85°C
DAC716PB	Plastic DIP	±4 LSB	–40°C to +85°C
DAC716UB	Plastic SOIC	±4 LSB	–40°C to +85°C
DAC716PK	Plastic DIP	±2 LSB	0°C to +70°C
DAC716UK	Plastic SOIC	±2 LSB	0°C to +70°C
DAC716PL	Plastic DIP	±1 LSB	0°C to +70°C
DAC716UL	Plastic SOIC	±1 LSB	0°C to +70°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC716P	Plastic DIP	180
DAC716U	Plastic SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +15V, $-V_{CC}$ = –15V.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{CLK}	Data Clock Period	100		ns
t_{CL}	Clock LOW	50		ns
t_{CH}	Clock HIGH	50		ns
t_{A0S}	Setup Time for $\overline{A_0}$	50		ns
t_{A1S}	Setup Time for $\overline{A_1}$	50		ns
t_{AOH}	Hold Time for $\overline{A_0}$	10		ns
t_{A1H}	Hold Time for $\overline{A_1}$	10		ns
t_{DS}	Setup Time for DATA	50		ns
t_{DH}	Hold Time for DATA	10		ns
t_{DSOP}	Output Propagation Delay	140		ns
t_{CP}	Clear Pulsewidth	200		ns

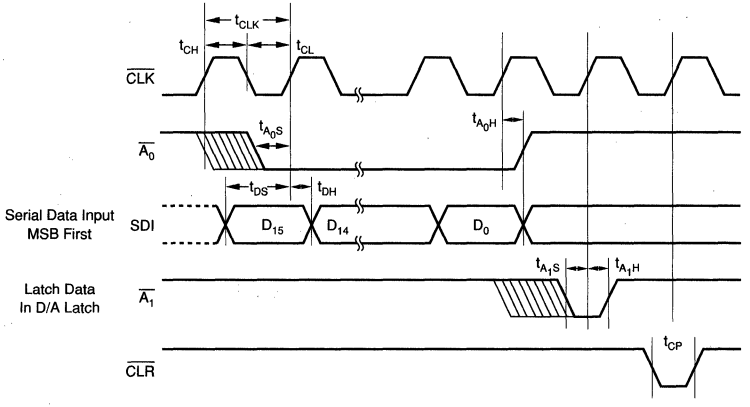
TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{CLK}$	$\overline{CLR}$	DESCRIPTION
0	1	1 → 0 → 1	1	Shift Serial Data into SDI
1	0	1 → 0 → 1	1	Load D/A Latch
1	1	1 → 0 → 1	1	No Change
0	0	1 → 0 → 1	1	Two Wire Operation(1)
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

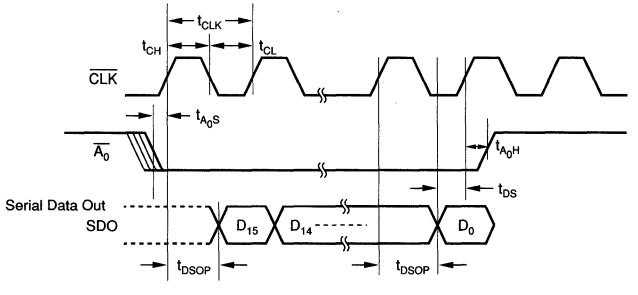
NOTES: X = Don't Care. (1) All digital input changes will appear at the D/A output.

TIMING DIAGRAMS

Serial Data In



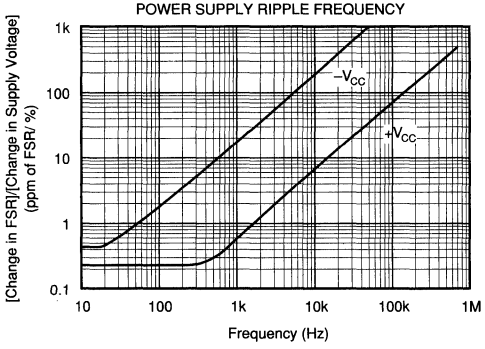
Serial Data Out



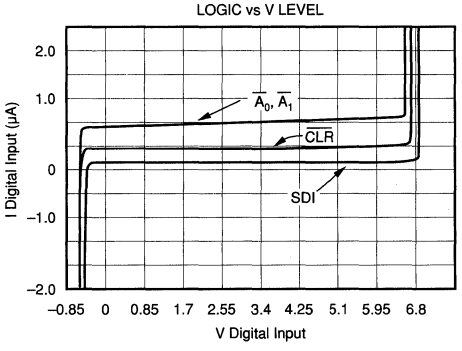
TYPICAL PERFORMANCE CURVES

AT T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

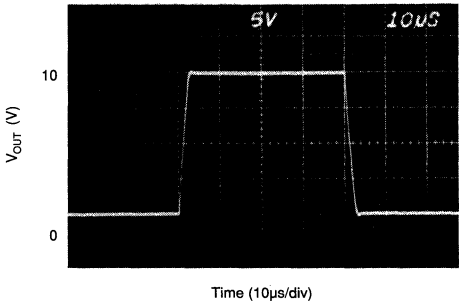
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



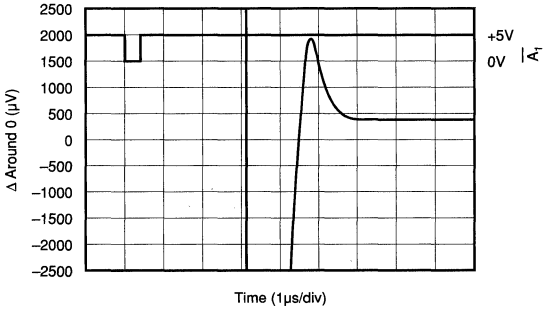
LOGIC vs V LEVEL



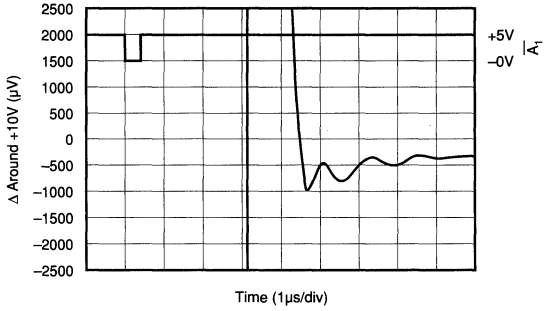
FULL SCALE OUTPUT SWING



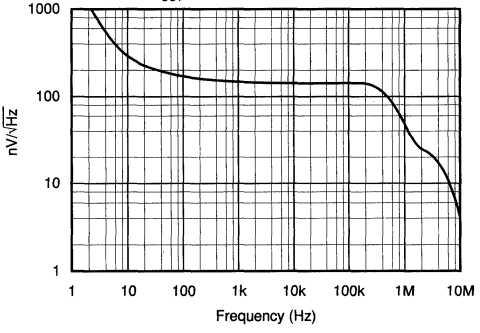
SETTLING TIME, +10V TO 0V



SETTLING TIME, 0V TO +10V



V_{OUT} SPECTRAL NOISE DENSITY



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of the L grade is guaranteed over the specification temperature range to 16 bits.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 10V and 1LSB. The 1LSB change is measured at the Major Carry (7FFF to 8000, and 8000 to 7FFF: Straight Binary codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from 8000 to 7FFF.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

The DAC716 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and a serial interface.

INTERFACE LOGIC

The DAC716 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic "0" will enter the latch. When the enable inputs return to logic "1", the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give an output voltage of 0V (code 0000).

LOGIC INPUT COMPATIBILITY

DAC716 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic "0" and control inputs will float to logic "0" if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

The DAC716 is designed to accept Straight Binary (SB) input codes. The serial input format is MSB first.

INTERNAL REFERENCE

DAC716 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and unipolar offset of the converter will vary.

OUTPUT VOLTAGE SWING

The output amplifier of DAC716 is designed to achieve a +10V output range. DAC716 will provide a +10V output swing while operating on ±11.4V or higher voltage supplies.

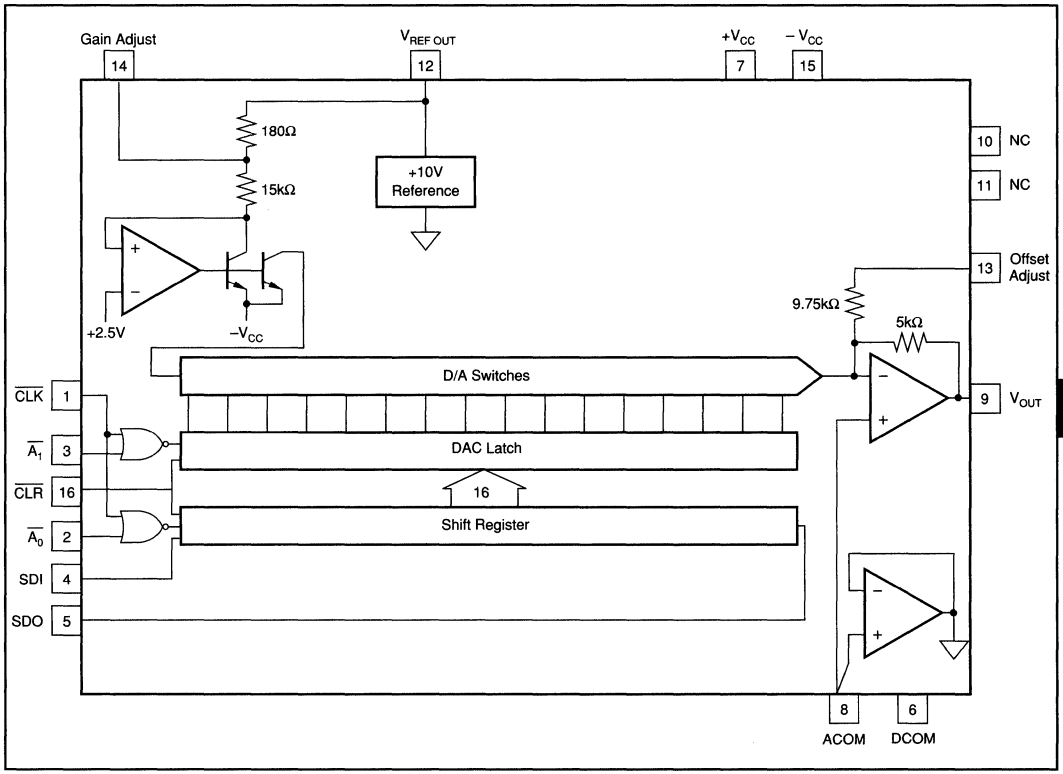


FIGURE 1. DAC716 Block Diagram.

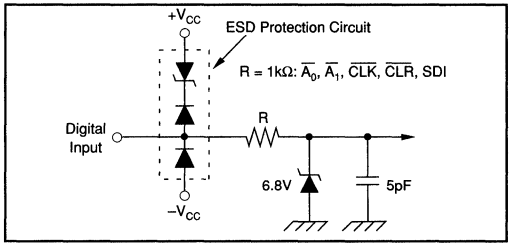


FIGURE 2. Equivalent Circuit of Digital Inputs.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a unipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

Offset Adjustment

Apply the digital input code, 0000, that produces 0V and adjust the offset potentiometer or the offset adjust D/A converter for 0V.

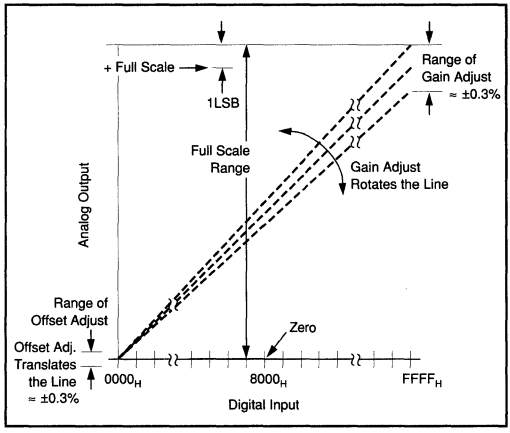


FIGURE 3. Relationship of Offset and Gain Adjustments.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

DAC716 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 152µV		
DIGITAL INPUT CODE STRAIGHT BINARY	ANALOG OUTPUT (V) UNIPOLAR 10V RANGE	DESCRIPTION
$FFFF_H$	+9.999695	+ Full Scale –1LSB
8000_H	+5.000000	Half Scale
0000_H	0.000000	Unipolar Zero

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

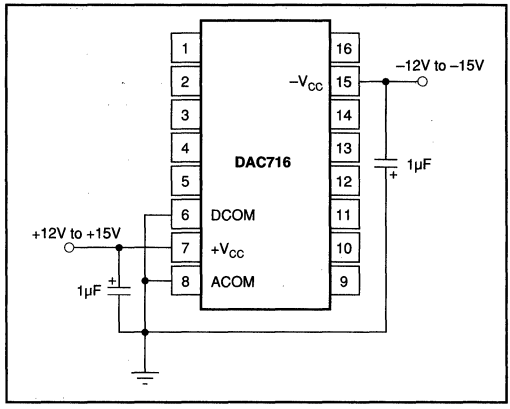


FIGURE 4. Power Supply Connections.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high precision of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of 152µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 0.1 inch wide printed circuit conductor 0.6 inches long will result in a voltage drop of 150µV.

The analog output of DAC716 has an LSB size of 152µV (–96dB). The rms noise floor of the D/A should remain below this level in the frequency range of interest. The DAC716's output noise spectral density (which includes the noise contributed by the internal reference) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

The DAC716 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC716s are used or if the DAC716 shares supplies with other components, connecting the ACOM and DCOM lines together at the power supplies only rather than at each chip, may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because there is no change in DAC716 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC716 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide a nominal OFFSET adjust and GAIN adjust resolution of 25µV and 15µV per LSB step, respectively.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, 0V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC716 output amplifier is connected internally for 10V output range.

DIGITAL INTERFACE

SERIAL INTERFACE

The DAC716 has a serial interface with two data buffers which can be used for either synchronous or asynchronous updating of multiple D/A converters. $\overline{A0}$ is the enable control for the Data Input Latch. $\overline{A1}$ is the enable for the D/A Latch. $\overline{CLK}$ is used to strobe data into the latches enabled by $\overline{A0}$ and $\overline{A1}$. A $\overline{CLR}$ function is also provided and when enabled it sets the Data Latch to all zeros and the D/A Latch to a code that gives bipolar zero at the D/A output.

Multiple DAC716s can be connected to the same $\overline{CLK}$ and data lines in two ways. The output of the serial loaded data latch is available as SDO so that any number of DAC716s can be cascaded on the same input bit stream as shown in Figure 8 and 9. This configuration allows all D/A converters to be updated simultaneously and requires a minimum number of control signal inputs. These configurations do require 16N $\overline{CLK}$ cycles to load any given D/A converter, where N is the number of D/A converters.

The DAC716 can also be connected in parallel as shown in Figure 10. This configuration allows any D/A converter in the system to be updated in a maximum of 16 $\overline{CLK}$ cycles.

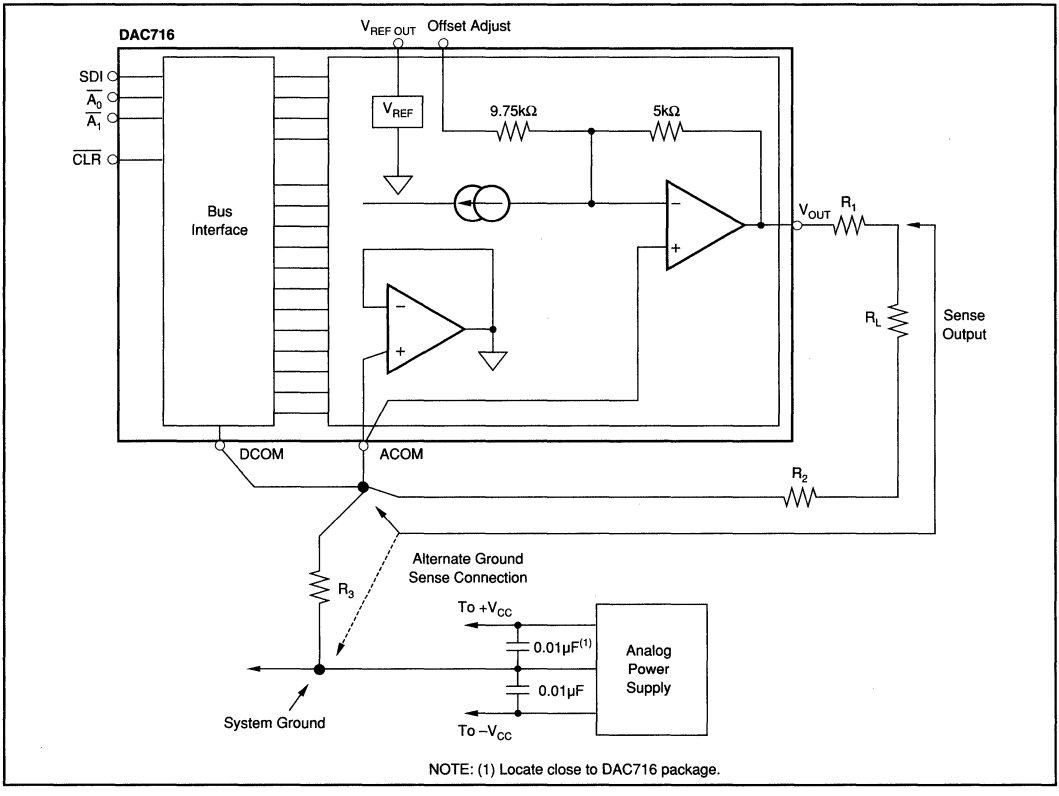


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

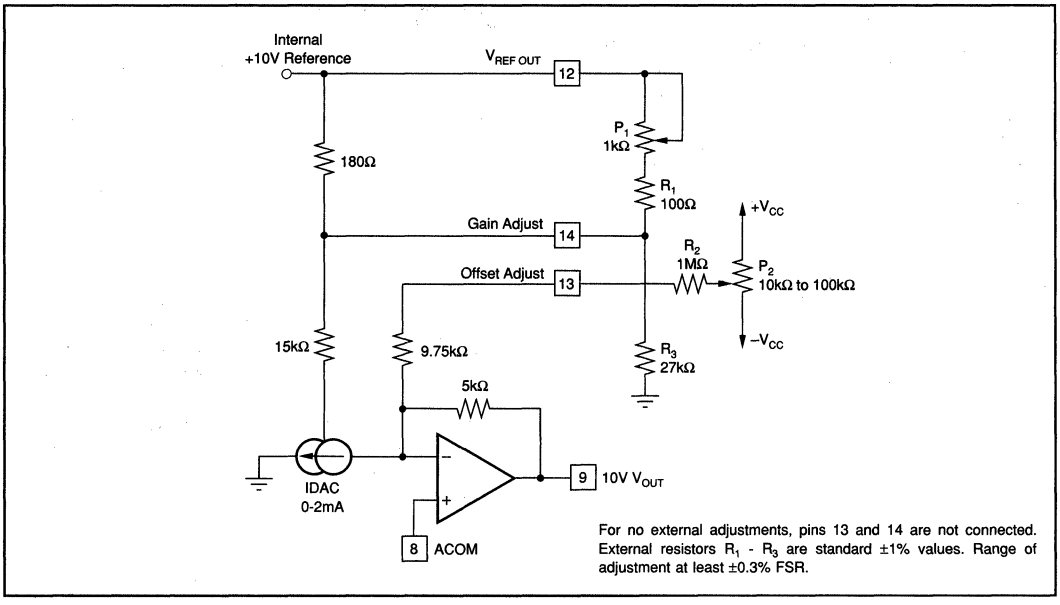


FIGURE 6. Manual Offset and Gain Adjust Circuits.

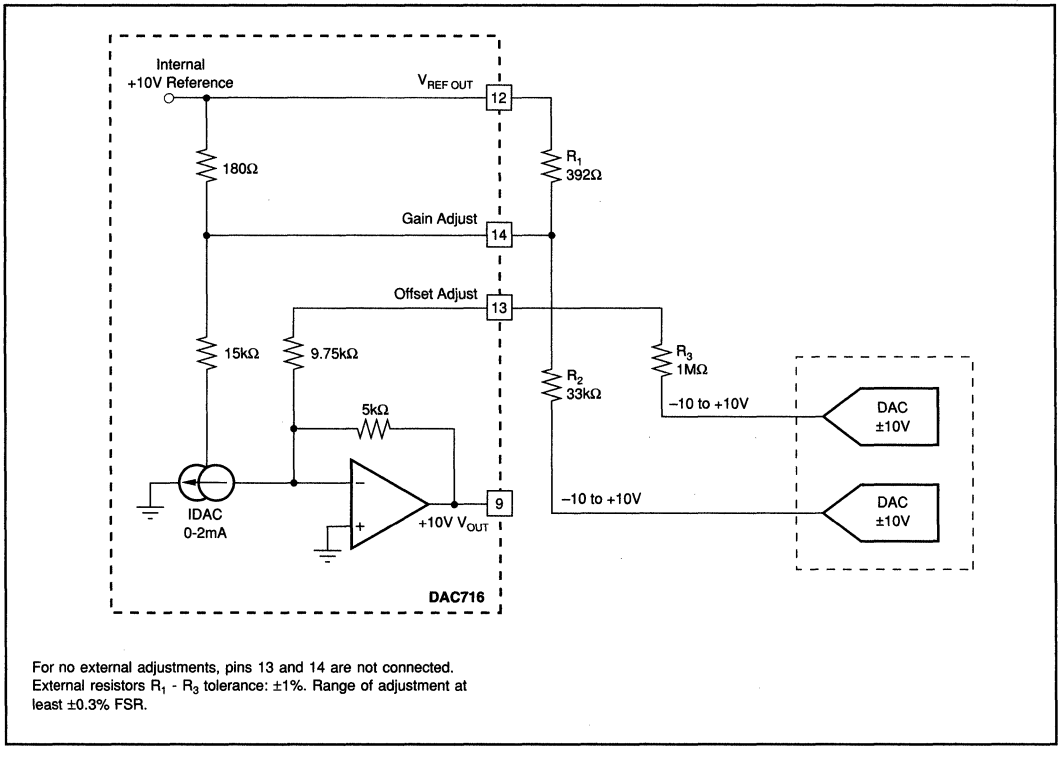


FIGURE 7. Gain and Offset Adjustment Using D/A Converters.

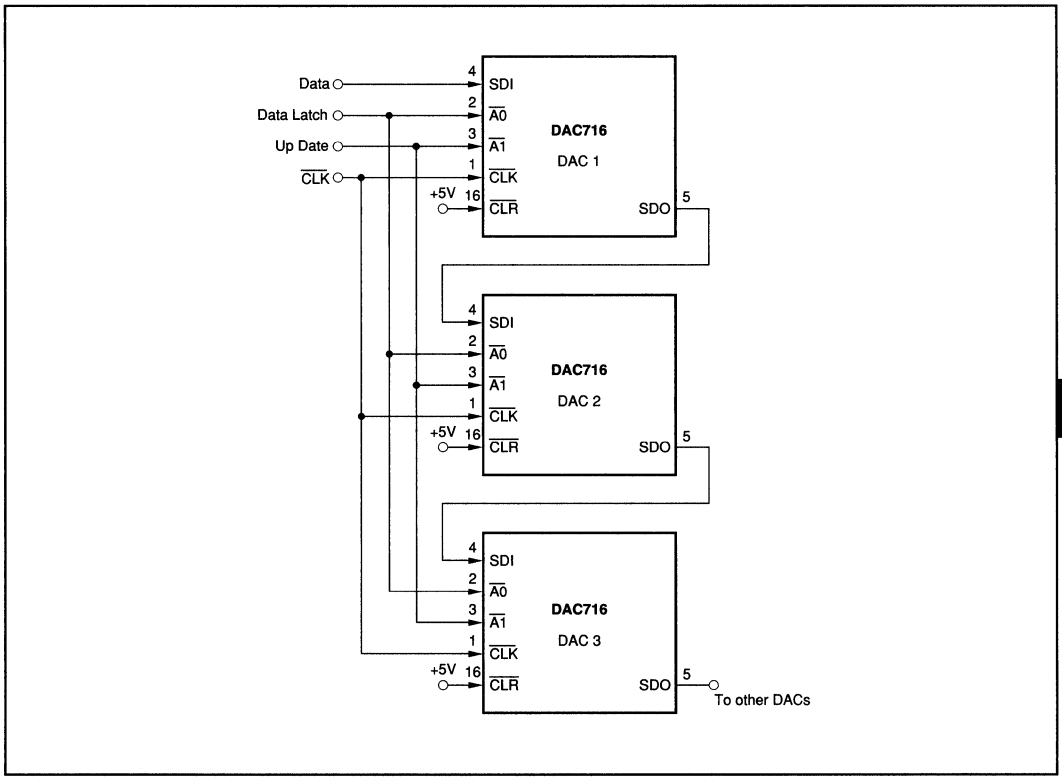


FIGURE 8a. Cascaded Serial Bus Connection with Synchronous Update.

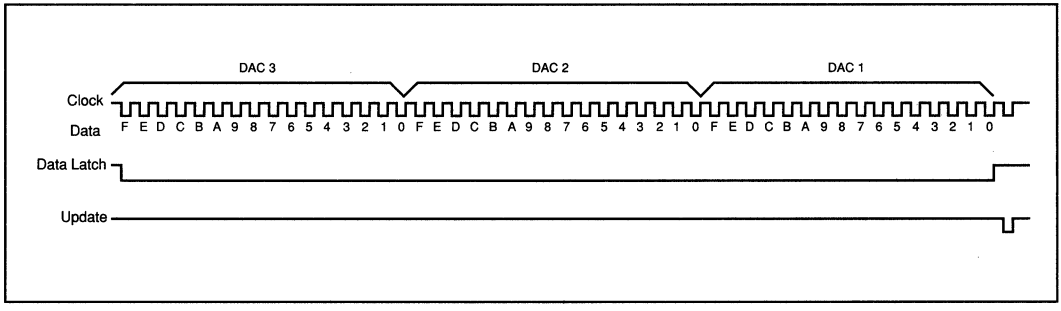


FIGURE 8b. Timing Diagram For Figure 8a.

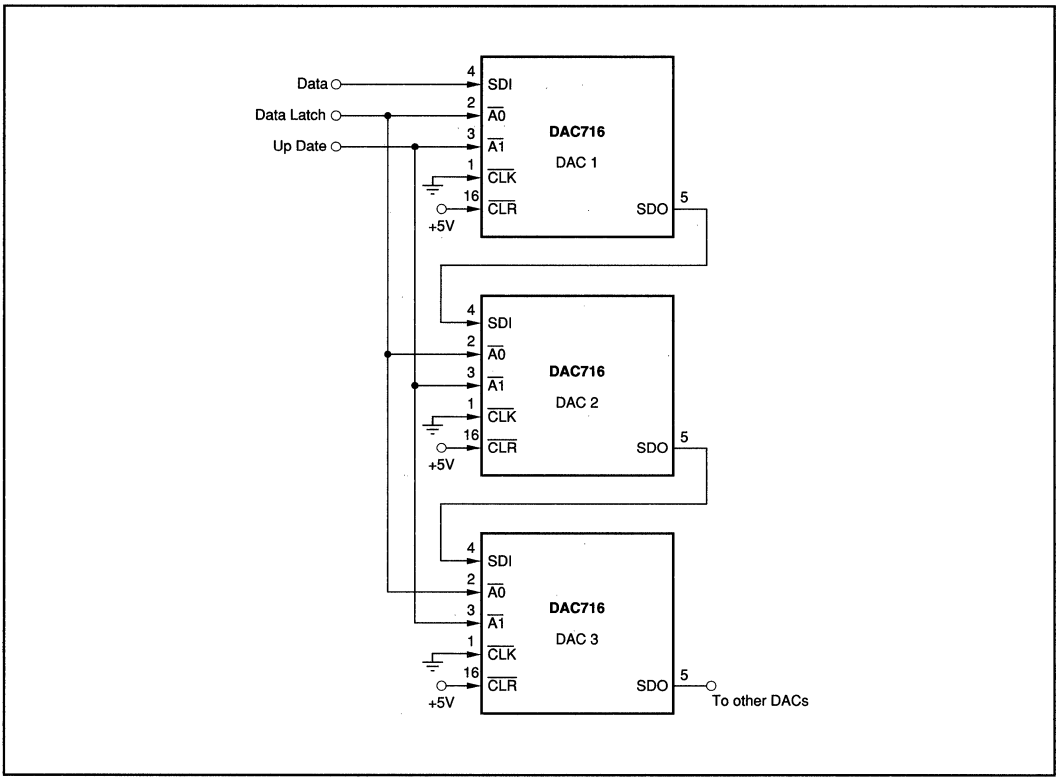


FIGURE 9a. Cascaded Serial Bus Connection with Asynchronous Update.

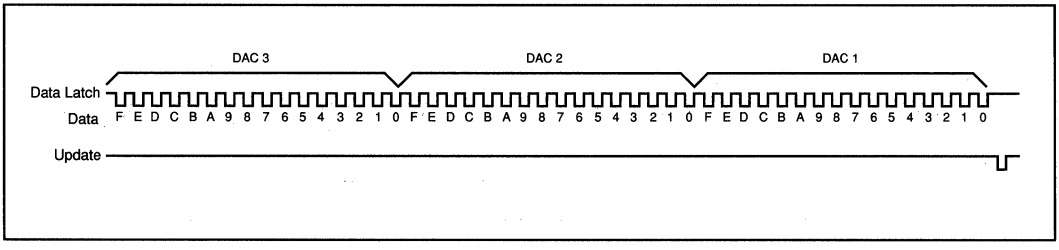


FIGURE 9b. Timing Diagram For Figure 9a.

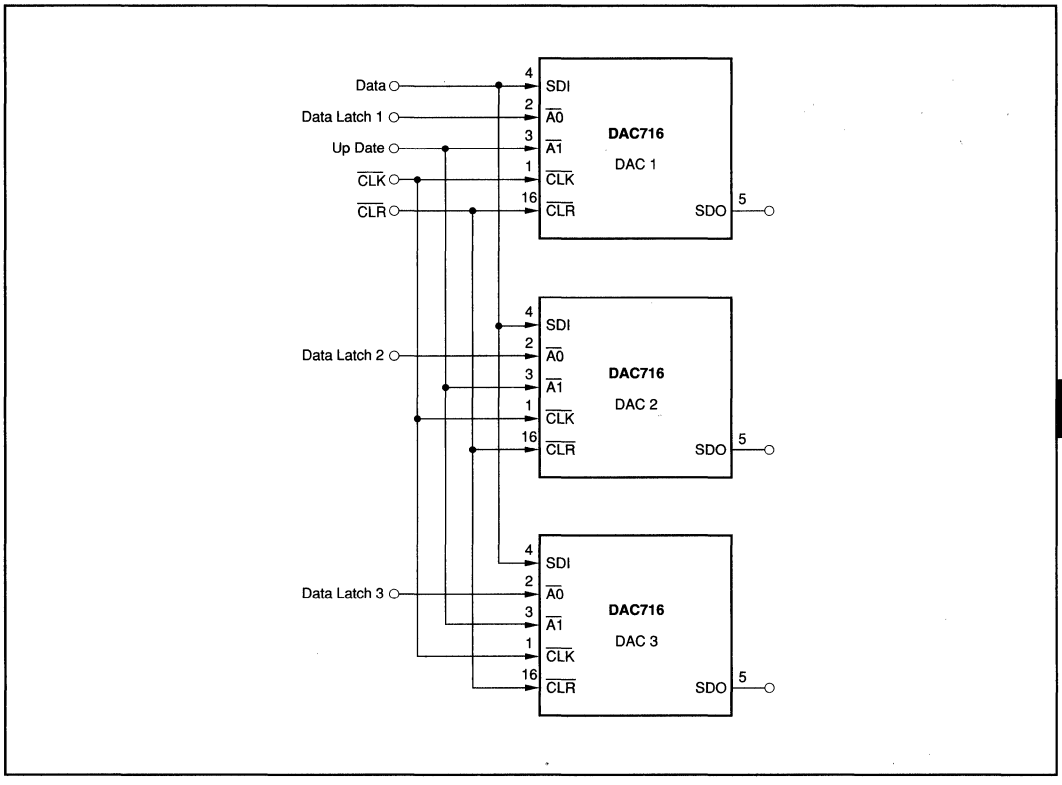


FIGURE 10a. Parallel Bus Connection.

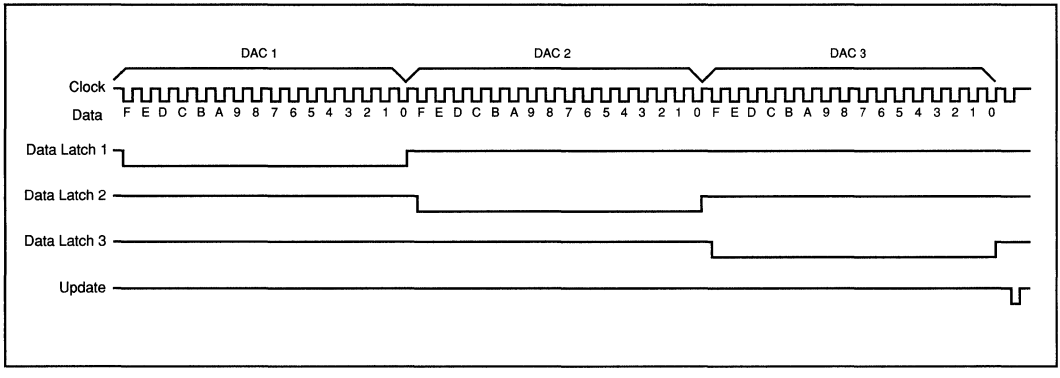


FIGURE 10b. Timing Diagram For Figure 10a.

BURR - BROWN®

DAC725

Dual 16-Bit DIGITAL-TO-ANALOG CONVERTER

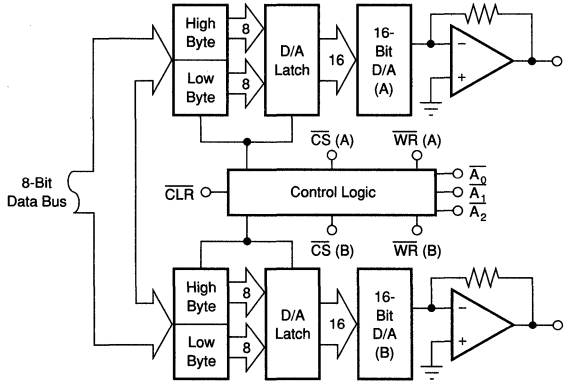
FEATURES

- **COMPLETE DUAL V_{OUT} DAC**
- **DOUBLE-BUFFERED INPUT REGISTER**
- **HIGH-SPEED DATA INPUT: Serial or Parallel**
- **HIGH ACCURACY: ±0.003% Linearity Error**
- **14-BIT MONOTONICITY OVER TEMPERATURE**
- **PLASTIC PACKAGE**
- **CLEAR INPUT TO SET ZERO OUTPUT**

DESCRIPTION

The DAC725 is a dual 16-bit DAC, complete with internal reference and output op amps. The DAC725 is designed to interface to an 8-bit microprocessor bus, but can also be interfaced to wider buses. The hybrid construction minimizes the digital feedthrough typically associated with products that combine the digital bus interface circuitry with high-accuracy analog circuitry.

The 16-bit data word is loaded into either of the DACs in two 8-bit bytes per 16-bit word. The versatility of the control lines allows the data word to be directed to either DAC, in any order. The voltage-out DACs are dedicated to a bipolar output voltage of ±10V. The output is immediately set to 0V when the Clear command is given. This feature, combined with the bus interfacing and complete DAC circuitry, makes the DAC725 ideal for automatic test equipment, power control, servo systems, and robotics applications.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

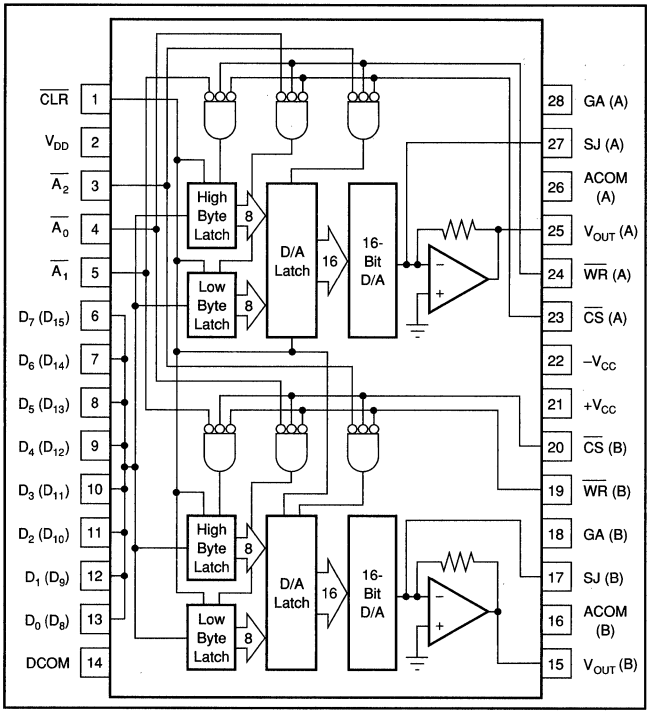
At T_A = +25°C, V_{CC} = ±15V, and after a 10-minute warm-up unless otherwise noted.

PARAMETER	DAC725JP MIN	DAC725JP TYP	DAC725JP MAX	DAC725KP MIN	DAC725KP TYP	DAC725KP MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Bipolar Input Code		Binary Twos Complement			*		
Logic Levels[1]: V_{IH}	+2		+5.5	*		*	V
V_{IL}	–1		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			1			*	µA
I_{IL} (V_I = +0.4V)			1			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.003	±0.006		±0.0015	±0.003	% of FSR[2]
Differential Linearity Error[3]		±0.0045	±0.012		0.003	±0.006	% of FSR
At Bipolar Zero: KP[3, 4]					±0.003	±0.006	% of FSR
Gain Error[5]		±0.07	±0.2		*	±0.15	%
Bipolar Zero Error[5]		±0.05	±0.1		*	*	% of FSR
Montonicity Over Specified Temp. Range	13			14			Bits
Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$		±0.0015	±0.006		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*	% of FSR/%V_{DD}
DRIFT (Over Specified Temperature Range)							
Gain Drift		±10			*	±25	ppm/°C
Bipolar Zero Drift		±5			*	±12	ppm of FSR/°C
Differential Linearity Over Temperature[3]		±0.0045	±0.012		±0.003	±0.006	% of FSR
Linearity Error Over Temperature[3]			±0.012			±0.006	% of FSR
SETTLING TIME (to ±0.003% of FSR)[6]							
20V Step (2kΩ load)		4			*	8	µs
1LSB Step at Worst-Case Code[7]		2.5			*	4	µs
Slew Rate		10			*		V/µs
OUTPUT							
Output Voltage Range[8]	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Current (No load, ±15V supplies): $+V_{CC}$		+29	+35		*	*	mA
$-V_{CC}$		–35	–40		*	*	mA
V_{DD}		+6	+10		*	*	mA
Power Dissipation (±15V supplies)		920	1175		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Storage	–60		+150	*		*	°C

*Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74HC and 54/74HTC compatible over the specification temperature range. (2) FSR means Full-Scale Range. For example, for ±10V output, FSR = 20V. (3) ±0.0015% of FSR is equal to 1LSB in 16-bit resolution. ±0.003% of FSR is equal to 1LSB in 15-bit resolution. ±0.006% of FSR is equal to 1LSB in 14-bit resolution. (4) Error at input code 0000_H (BTC). (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (6) Maximum represents the 3σ limit. Not tested for this parameter. (7) The bipolar worst-case code change is $FFFF_H$ to 0000_H (BTC). (8) Minimum supply voltage for ±10V output swing is approximately ±13V. Output swing for ±12V supplies is at least ±9V.

CONNECTION DIAGRAM



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	CLR	Clear line. Sets the D/A register to 0000_{HEX}, which gives bipolar zero on the D/A output.
2	V_{DD}	Logic supply (+5V).
3	$\overline{A_2}$	Latch enable for D/A latch (active low).
4	$\overline{A_0}$	Latch enable for "low byte" input (active low).
5	$\overline{A_1}$	Latch enable for "high byte" input (active low).
6	D_7 (D_{15}) (MSB)	Input for data bit 7 if enabling low byte (LB) latch, or data bit 15 if enabling the high byte (HB) latch.
7	D_6 (D_{14})	Input for data bit 6 if enabling LB latch, or data bit 14 if enabling HB latch.
8	D_5 (D_{13})	Data bit 5 (LB) or data bit 13 (HB).
9	D_4 (D_{12})	Data bit 4 (LB) or data bit 12 (HB).
10	D_3 (D_{11})	Data bit 3 (LB) or data bit 11 (HB).
11	D_2 (D_{10})	Data bit 2 (LB) or data bit 10 (HB).
12	D_1 (D_9)	Data bit 1 (LB) or data bit 9 (HB).
13	D_0 (D_8)	Data bit 0 (LB) or data bit 8 (HB).
14	DCOM	Digital common.
15	V_{OUT} (B)	Voltage output for DAC B.
16	ACOM (B)	Analog common for DAC B.
17	SJ (B)	Summing junction of the internal op amp for DAC B.
18	GA (B)	Gain adjust pin for DAC B.
19	$\overline{WR}$ (B)	Write control line for DAC B.
20	$\overline{CS}$ (B)	Chip select control line for DAC B.
21	$+V_{CC}$	Positive supply voltage (+15V).
22	$-V_{CC}$	Negative supply voltage (–15V).
23	$\overline{CS}$ (A)	Chip select control line for DAC A.
24	$\overline{WR}$ (A)	Write control line for DAC A.
25	V_{OUT} (A)	Voltage output for DAC A.
26	ACOM (A)	Analog common for DAC A.
27	SJ (A)	Summing junction of the internal op amp for DAC A.
28	GA (A)	Gain adjust pin for DAC A.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V, +15V
$+V_{CC}$ to COMMON	0V, +18V
$-V_{CC}$ to COMMON	0V, –18V
Digital Data Inputs to COMMON	–0.5V, V_{DD} + 0.5
DC Current any Input	±10mA
Reference Out to COMMON	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
External Voltage Applied to R_F	±18V
External Voltage Applied to D/A Output	±5V
Power Dissipation	2000mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
DAC725JP	±0.012	0°C to +70°C
DAC725KP	±0.006	0°C to +70°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC725JP	28-Pin Plastic DIP	215
DAC725KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC725 accepts positive-true binary twos complement input code, as shown in Table I. The data is loaded into either DAC, 8 bits at a time. The data may also be clocked into the device in a serial format.

DIGITAL INPUT CODES	ANALOG OUTPUT (Binary Two's Complement, Bipolar Operation, All Models)
$7FFF_H$	+ Full Scale
0000_H	Zero
$FFFF_H$	– 1LSB
8000_H	– Full Scale

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (minus full-scale point and plus full-scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of –1LSB maximum (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC725 is specified to be monotonic to 14 bits over the entire specification range.

DRIFT

Gain Drift

Gain drift is a measure of the change in full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by:

(1) testing the end point differences at t_{MIN}, +25°C and t_{MAX},

(2) calculating the gain error with respect to the +25°C value, and

(3) dividing by the temperature change.

The DAC725 is specified for Maximum Gain and Offset values at temperature. This tells the system designer the maximum that can be expected over temperature, regardless of room temperature values.

Zero Drift

Zero drift is a measure of change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. This code corresponds to 0V analog output.

The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

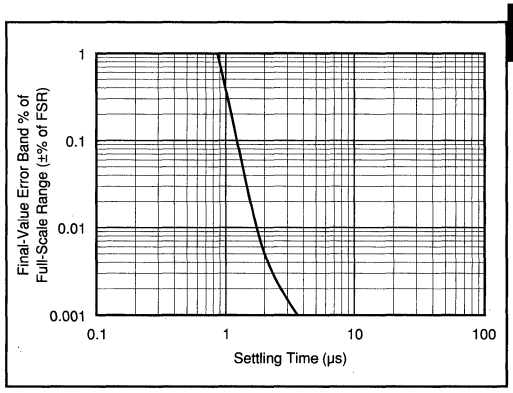


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V), and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. This is the worst-case point since all of the input bits change when going from one code to the next.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

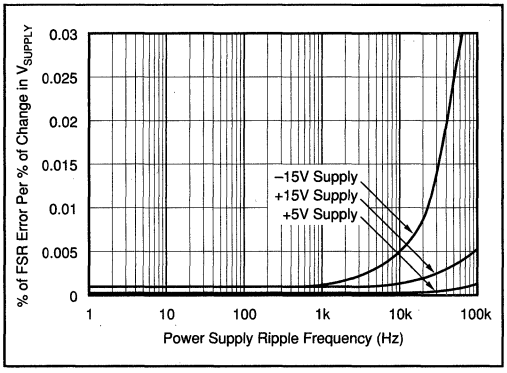


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF to 10µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001µF to 0.01µF low-leakage film capacitor should be connected from Gain Adjust to Analog Common to prevent noise pickup. Refer to Figure 4 for relationship of Offset and Gain adjustments.

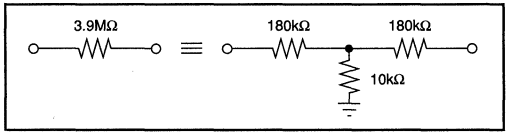


FIGURE 3. Equivalent Resistances.

Zero Adjustment

By loading the code 0000_H, the DAC will force 0V. Offset is adjusted by using the circuit of Figure 5. An alternate method would be to use the $\overline{CLR}$ control to set the DAC to 0V. Zero calibration should be made before gain calibration.

Gain Adjustment

To adjust the gain of the DAC725, set the DAC to $7FFF_H$ for both DACs. Adjust the gain of each DAC to obtain the full scale voltage of +9.99969V as shown in Table II.

DIGITAL INPUT CODE	BIPOLAR OUTPUT, ±10V			UNITS
	16 Bits	15 Bits	14 Bits	
One LSB	305	610	1224	µV
$7FFF_H$	+9.99969	+9.99939	+9.99878	V
8000_H	−10	−10	−10	V

TABLE II. Digital Input Codes.

INTERFACE LOGIC AND TIMING

The control logic functions are chip select ($\overline{CS}_A$ or $\overline{CS}_B$), write ($\overline{WR}_A$ or $\overline{WR}_B$), latch enable ($\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$), and clear ($\overline{CLR}$). These pins provide the control functions for the microprocessor interface. There is a write and a chip select for both DAC_A and for DAC_B channels. This allows the 8-bit data word to be latched from the data bus to the input latch or from the input latch to the DAC latch, of DAC_A, DAC_B, or both.

$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{WR}$ (A)	$\overline{CS}$ (A)	DESCRIPTION
1	1	0	0	0	DAC latch enabled, Channel A
1	0	1	0	0	Input latch high byte enabled, Channel A
1	0	0	0	0	High byte flows through to DAC, Channel A
0	1	1	0	0	Low byte latched from data bus, Channel A
0	1	0	0	0	Low byte flows through to DAC, Channel A
0	0	1	1	1	Serial input mode for byte latches
X	X	X	1	0	No data is latched
X	X	X	0	1	No data is latched

"1" or "0" indicates TTL Logic Level Channel A shown.

TABLE III. Truth Table of Data Transfers.

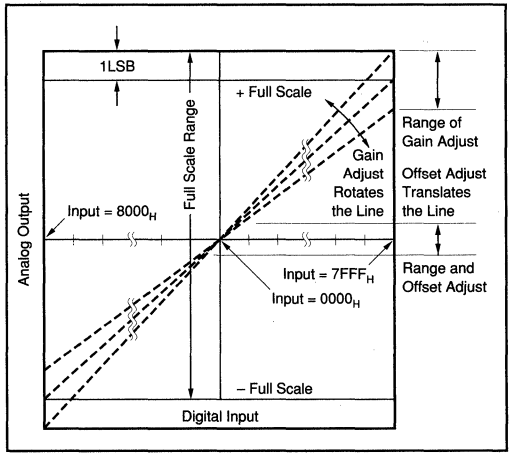


FIGURE 4. Relationship of Zero and Gain Adjustments for the DAC725.

The latch enable lines control which latch is being loaded. Line $\overline{A_1}$ in combination with $\overline{WR}$ and $\overline{CS}$ enables the high byte of the DAC channel to be latched through the byte latch. The $\overline{A_0}$ line, in conjunction with the $\overline{WR}$ and $\overline{CS}$, latches the data for the low byte. When $\overline{A_2}$, $\overline{CS}$, and $\overline{WR}$ are low at the same time, the data is latched through the D/A latch and the DAC changes output voltage. Each latch may be made transparent by maintaining its enable signal at logic "0".

The serial data mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are at logic low simultaneously. The data (MSB first) is clocked in to pin 13 with clock pulses on the $\overline{WR}$ pin. The data is then latched through to the DAC as a complete 16-bit word selected by $\overline{A_2}$.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the DAC latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the DAC.

The maximum clock rate of the latches is 10MHz. The minimum time between the write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode, the maximum rate at which data can be clocked into the input shift register is 10MHz. The timing of the control signals is given in Figure 6.

INTERVAL	DESCRIPTION	OVER TEMP. ns, min	OVER TEMP. ns, max
t_{DW}	Data valid to end of $\overline{WR}$	80	
t_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
t_{AW}	$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$ valid to end of $\overline{WR}$	80	
t_{WP}	Write pulse width	80	
t_{DH}	Data hold after end of $\overline{WR}$	0	

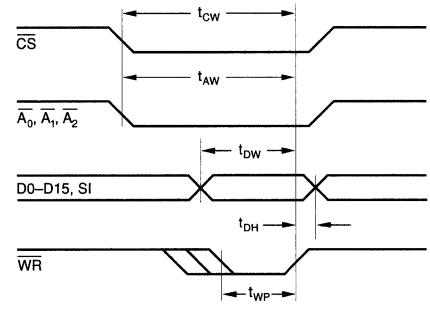


FIGURE 6. Logic Timing Diagram.

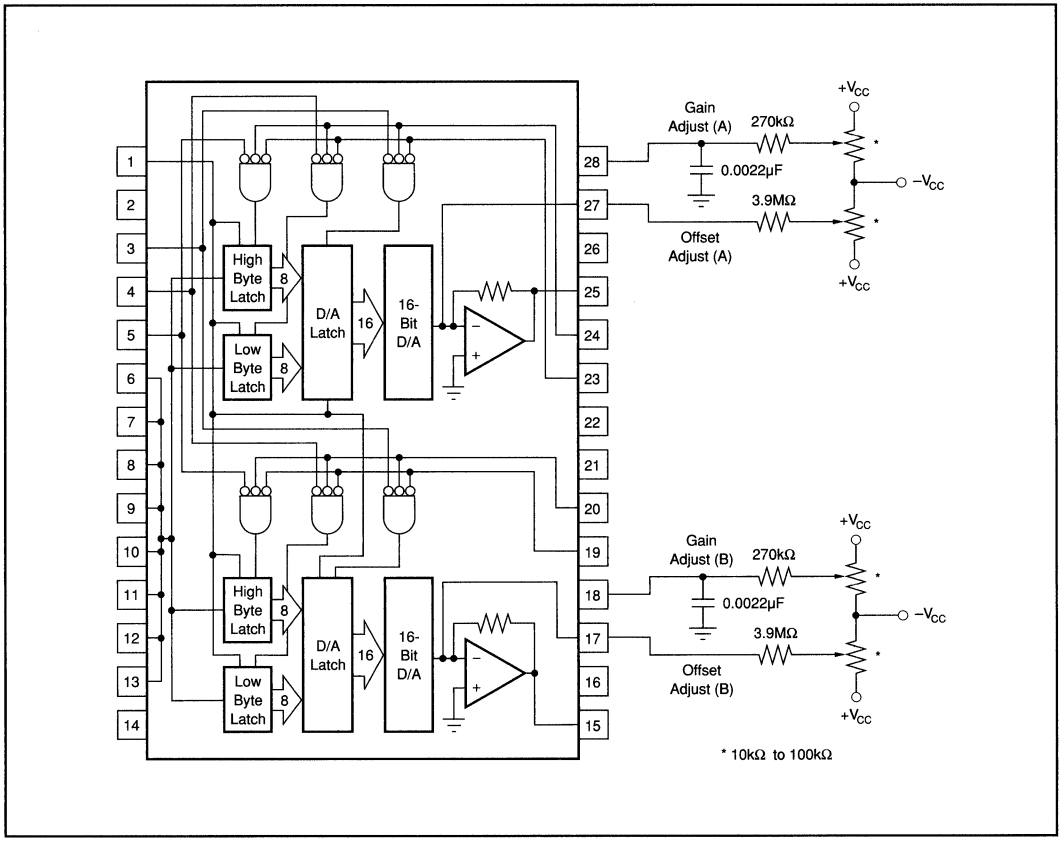


FIGURE 5. Connections for Gain and Offset Adjust.

INSTALLATION

Because of the extremely high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1oz copper-clad printed circuit board material is approximately 1/2mΩ per square mil. In the example above, a 10mil-wide conductor 60mil long would cause a 1LSB error in R_2 and R_3 of Figure 7.

In Figure 7, lead and contact resistances are represented as R_2 through R_6. As long as the load resistance (R_L) remains constant, the resistances of R_2 and R_3 will appear as gain errors when the output is sensed across the load. If the output is sensed at the DAC725 output terminal and the system analog common, R_2 and R_3 appear in series with R_L. R_4 has a current through it that varies by only 1% of the nominal 2mA current for all code combinations. This IR drop causes an offset error, and is calibrated out as an offset error.

The current through the digital common varies directly with the digital code that is loaded into the DAC. The current is not the same for each code. If this IR drop is allowed to modulate the analog common, there may be code-dependent errors in the analog output.

The IR drop across R_6 may cause accuracy problems if the analog commons of several circuits are "daisy chained" along the power supply analog common. All analog sense lines should be referenced to the system analog common.

APPLICATIONS

WAVEFORM GENERATION

The DAC725 has attributes that make it ideal for very low distortion waveform synthesis. Due to special design techniques, the feedthrough energy is much lower than that found in other D/A converters available today. In addition to the low feedthrough glitch energy, the input logic will operate with data rates of 10MHz. This makes the DAC725 ideal for waveform synthesis.

PROGRAMMABLE POWER SUPPLIES

The DAC725 is an excellent choice for programmable power supply applications. The DAC outputs may be programmed to track or oppose each other. If the load is floating, and can be driven differentially, the dynamic range will be 17 bits, because the full-scale range doubles for the same sized LSB. The clear line ($\overline{CLR}$) sets both DAC outputs to zero, and would be used at power-up to bring the system up in a safe state. The $\overline{CLR}$ line could also be used if an over-power state is sensed.

ISOLATION

The DAC725 can accept serial input data, which means that only six optoisolators are needed for two DACs. The data is clocked into the input latch using the $\overline{WR}$ pin. The 16-bit data word is latched into the DAC selected by $\overline{A_2}$. When $\overline{A_0}$ and $\overline{A_1}$ are simultaneously low, the serial mode is enabled.

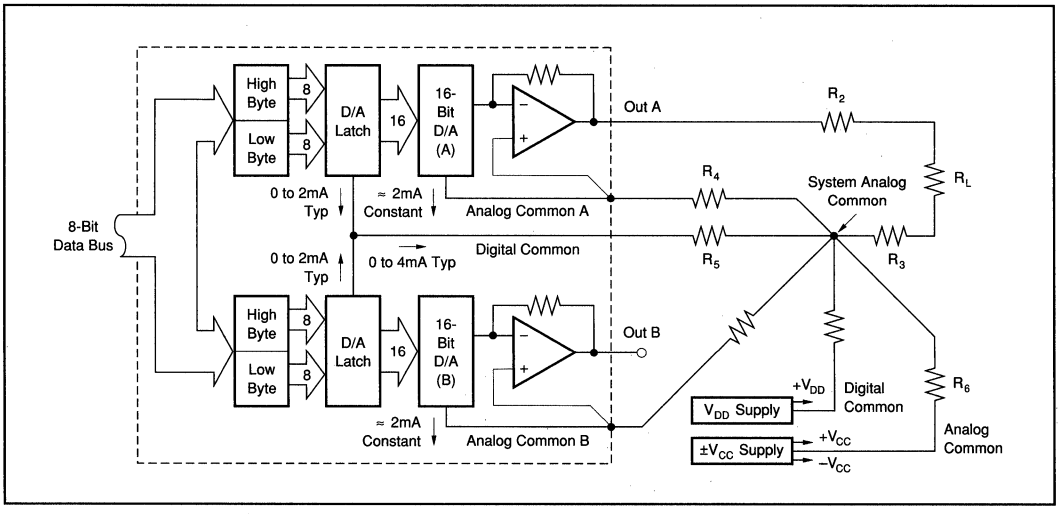


FIGURE 7. System Wiring Example.

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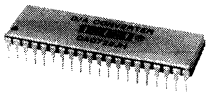
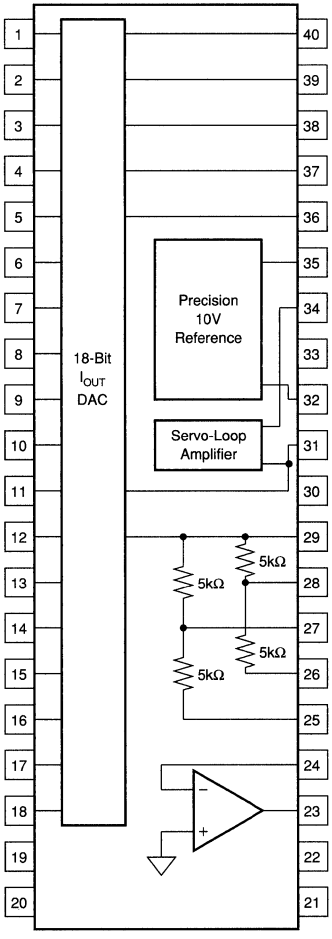


DAC729

Ultra-High Resolution 18-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT LINEARITY GUARANTEED (K Grade)
- USER ADJUSTABLE TO 18-BIT LINEARITY
- PRECISION INTERNAL REFERENCE
- FAST SETTLING, LOW NOISE INTERNAL OP AMP
- LOW DRIFT
- HERMETIC 40-PIN CERAMIC PACKAGE
- I_{OUT} OR V_{OUT} OPERATION



DESCRIPTION

The DAC729 sets the standard in very high accuracy digital-to-analog conversion. It is supplied from the factory at a guaranteed linearity of 16 bits, and is user-adjustable to 18-bit linearity (1LSB = FSR/262144).

To attain this high level of accuracy, the design takes advantage of Burr-Brown's thin-film monolithic DAC process, dielectric op amp process, hybrid capabilities, and advanced test and laser-trim techniques.

The DAC729 hybrid layout is specifically partitioned to minimize the effects of external load-current-induced thermal errors. The op amp design consists of a fast settling precision op amp with a current buffer within the feedback loop. This buffer isolates the load from the precision op amp, which results in a fast settling (8µs to 16 bits) output. The standard 40-pin package offers full hermeticity, contributing to the excellent reliability of the DAC729.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, using internal reference op amp, unless otherwise noted. COB = ±10V FSR, CSB = 0V to +10V FSR.

PARAMETER	DAC729JH MIN	DAC729JH TYP	DAC729JH MAX	DAC729KH MIN	DAC729KH TYP	DAC729KH MAX	UNITS
DIGITAL INPUT							
Resolution		18			*		Bits
Digital Inputs[1]: V_{IH}	+2.4		+V_L	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH}, V_{IN} = +2.7V			+5			*	µA
I_{IL}, V_{IN} = +0.4V			–300			*	µA
TRANSFER CHARACTERISTICS[2]							
ACCURACY							
Linearity Error[3]			±0.0015			±0.00076	% of FSR[4]
Differential Linearity Error			±0.003			±0.0015	% of FSR
Gain Error[5]		±0.05	±0.10		*	*	%
Offset Error:[5]Voltage, COB[6]		±5	±10		*	*	mV
CSB[6]		±3	±5		*	*	mV
Current, COB			±5			*	µA
CSB			±1			*	µA
Power Supply Sensitivity, Unipolar: ±15VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Bipolar Offset: ±15VDC		±0.0004	±0.0015		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Bipolar Gain: ±15VDC		±0.0005	±0.0015		*	*	% of FSR/%V_S
+5VDC		±0.0001	±0.0005		*	*	% of FSR/%V_S
Output Noise (10Hz to 100kHz), Voltage: Bipolar Offset		29			*		µVrms
Bipolar Gain		37			*		µVrms
Current: Bipolar Offset		2.9			*		nArms
Bipolar Gain		3			*		nArms
Monotonicity (0°C to +70°C)	15	16		16	17		Bits
Differential Linearity Adjustment Resolution[7]		18			*		Bits
DRIFT (Over Specification Temperature Range)							
Gain Drift (Excluding Reference Drift)		±3	±5		*	*	ppm/°C
Offset Drift (Excluding Reference Drift): COB (Bipolar)		±2	±5		*	*	ppm of FSR/°C
CSB (Unipolar)		±2	±3		*	*	ppm of FSR/°C
Linearity Error (at 0°C and +70°C)		±0.3	±1		±0.3	±0.5	ppm of FSR/°C
Differential Linearity Error (at 0°C and +70°C)		±0.5	±2		±0.5	±1	ppm of FSR/°C
STABILITY, LONG TERM (at +25°C)							
Gain (Exclusive of Reference)		±5			±5		ppm/1000hr
Offset: COB (Exclusive of Reference)		±5			±5		ppm of FSR/1000hr
CSB		±5			±5		ppm of FSR/1000hr
Linearity		±2			±2		ppm of FSR/1000hr
Reference		±5			±5		ppm/1000hr
OUTPUT							
VOLTAGE OUTPUT MODE							
Ranges: COB		±2.5, ±5, ±10			*		V
CSB		0 to +10, 0 to +5			*		V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
CURRENT OUTPUT MODE							
COB Ranges		±1			*		mA
Output Impedance		2.86			*		kΩ
CSB Ranges		0 to –2			*		mA
Output Impedance		4.0			*		kΩ
Output Current Tolerance			±0.1			*	% of FSR
Compliance Voltage		–1 to +5			*		V
SETTLING TIME (To ±0.00076% of FSR)[8]							
Voltage (Load = 2kΩ || 100pF): Full-Scale Step		5	8		*	*	µs
1LSB Step (Major Carry)[9]		4	7		*	*	µs
Slew Rate		20			*		V/µs
Switching Transient Peak		500			*		mV
Switching Transient Energy		0.45			*		V-µs
Current Full-Scale Step (2mA X 10Ω || 1pF)		300			*		ns

SPECIFICATIONS (CONT)

ELECTRICAL

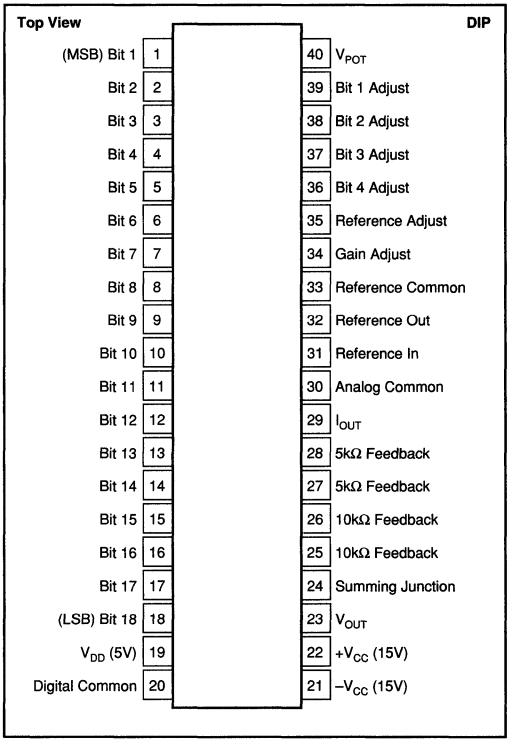
T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, using internal reference op amp, unless otherwise noted. COB = ±10V FSR, CSB = 0V to +10V FSR.

PARAMETER	DAC729JH MIN	DAC729JH TYP	DAC729JH MAX	DAC729KH MIN	DAC729KH TYP	DAC729KH MAX	UNITS
REFERENCE							
Output (pin 32) :Voltage	+9.990	+10.000	+10.010	*	*	*	V
Source Current[10]			+4			*	mA
Temperature Coefficient		±2	±4		*	*	ppm/°C
Short-Circuit Duration		Indefinite to Common			Indefinite to Common		
Power Supply Sensitivity		0.00025	0.003		*	*	%/V
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$	−16.5	−15	−13.5	*	*	*	V
V_{DD}	+4.75	+5	+5.25	*	*	*	V
Current: $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−45	−60		*	*	mA
V_{DD}		+18	+25		*	*	mA
Power Dissipation (Rated Supplies)		1.22	1.63		*	*	W
ENVIRONMENTAL SPECIFICATIONS							
Temperature Range: Specification	0		+70	*		*	°C
Storage	−60		+150	*		*	°C

* Specifications same as DAC729JH.

NOTES: (1) TTL- and CMOS-compatible. (2) Specified for V_{OUT} mode using the internal op amp. (3) ±0.00076% of full-scale range is 1/2LSB for 16-bit resolution. (4) FSR means full-scale range, 20V for ±10V range, etc. (5) Adjustable to zero error with an external potentiometer. (6) COB is complementary offset binary (bipolar); CSB is complementary straight binary (unipolar). (7) Using the MSB adjustment circuit, the user may improve the DAC linearity to 1/2LSB of this specification with gain and offset errors adjusted to zero at 25°C. (8) Maximum represents 3σ limit, not 100% production tested. (9) At the major carry; 20000 to $1FFFF_{HEX}$ and from 1FFFF to 20000_{HEX}. (10) Maximum with no degradation in specifications. External loads must be constant.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

V_{DD} to Common	0V to +7V
$+V_{CC}$ to Common	0V to +18V
$-V_{CC}$ to Common	0V to −18V
Digital Data Inputs (pins 1-18) to Common	−0.5V to V_{DD}
Reference Voltage In (pin 31)	+9V to +11V
Reference Out (pin 32) to Common	Indefinite Short to Common
External Voltage Applied to D/A Output (pin 29)	−5V to +5V
External Voltage Applied to Feedback Resistors (pins 25, 26, 27, 28)	−15V to +15V
V_{OUT} (pin 23)	Indefinite Short to Common
Power Dissipation	3000mW
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
DAC729JH	40-Pin Hermetic DIP	0°C to +70°C
DAC729KH	40-Pin Hermetic DIP	0°C to +70°C
DAC729KH-BI	40-Pin Hermetic DIP	0°C to +70°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC729JH	40-Pin Hermetic DIP	214
DAC729KH	40-Pin Hermetic DIP	214
DAC729KH-BI	40-Pin Hermetic DIP	214

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

BURN-IN SCREENING

Burn-in screening is an option available for the DAC729 family of products. Burn-in duration is 160 hours at 100°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met.

THEORY OF OPERATION

The DAC729 is an 18-bit digital-to-analog converter system, including a precision reference, low noise, fast settling operational amplifier, and an 18-bit current source/DAC chip contained in a hermetic 40-pin ceramic dual-in-line package. Refer to Figure 11 for a schematic diagram of the DAC729.

THE INTERNAL REFERENCE

The reference consists of a very low temperature coefficient closed-loop reference zener circuit that has been temperature-drift-compensated by laser-trimming a zener current to achieve less than 1ppm/°C temperature drift of V_{REF}.

By strapping pin 32 (Reference Out) to pin 31 (Reference In), the DAC will be properly biased from the internal reference. The internal reference may be fine adjusted using pin 35 as shown in Figure 7. The reference has an output buffer that will supply 4mA for use external to the DAC729. This load must remain constant because changing load on the reference may change the reference current to the DAC.

In systems where several components need to track the same system reference, the DAC729 may be used with an external 10V reference, however, the internal reference has lower noise (6μVp-p) and better stability than other references available.

THE OPERATIONAL AMPLIFIER

To support a DAC of this accuracy, the operational amplifier must have a maximum gain-induced error of less than 1/3LSB, independent of output swing (the op amp must be linear!) To support 15 bits (1/2-bit linearity), the op amp must have a gain of 130,000V/V. For 18 bits, the minimum gain is well over 500,000V/V. Since thermal feedback is the major limitation of gain for mono op amps, the amplifier was designed as a high gain, fast settling mono op amp, followed by a monolithic, unity-gain current buffer to isolate the thermal effects of external loads from the input stage gain transistors. The op amp and buffer are separated from the DAC chip, minimizing thermally-induced linearity errors in the DAC circuit. The op amp, like the reference, is not dedicated to the DAC729. The user may want to add a network, or select a different amplifier. The DAC729 internal op amp is intended to be the best choice for accuracy, settling time, and noise.

THE DAC CHIP

The heart of the DAC729 is a monolithic current source and switch integrated circuit. The absolute linearity, differential linearity, and the temperature performance of the DAC729 are the result of the design, which utilizes the excellent element matching of the current sources and switch transistors to each other, and the tracking of the current setting resistors to the feed back resistors. Older discrete designs cannot achieve the performance of this monolithic DAC design.

The two most significant bits are binarily weighted interdigitated current sources. The currents for bits 3 through 18 are scaled with both current source weighting and an R-2R ladder. The circuit design is optimized for low noise and low superposition error, with the current sources arranged to minimize both code-dependent thermal errors and IR drop errors. As a result, the superposition errors are typically less than 20μV.

The DAC chip is biased from a servo amplifier feeding into the base line of the current sources. This servo amplifier sets the collector current to be mirrored and scaled in the DAC chip current sources, as shown in Figure 11. The reference current for the servo is established by the reference voltage applied to pin 31 feeding an internal resistor (20kΩ) to the virtual ground of the servo amplifier.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC729 accepts complementary digital input codes in either binary format (CSB for Unipolar or COB for Bipolar; see Table I).

	DAC ANALOG OUTPUT			
DIGITAL INPUT	COB	20V FSR	CSB	10V FSR
00 0000 0000 0000 0000	+ Full Scale	9.999924V	+ Full Scale	9.999962V
11 1111 1111 1111 1111	– Full Scale	–10V	– Full Scale	0V

TABLE I. Digital Input Coding.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2 LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than –1LSB (–0.0015% for 16-bit resolution) insures monotonicity to 16 bits.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC729KH is specified to be monotonic to 16 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is measured by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C, and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $3FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full-scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Settling time includes the slew time of the op amp.

Voltage Output

Settling times are specified to ±0.00076% of FSR scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.00076% of FSR for a full-scale range change with an output load resistance of 10Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to the current output mode of operation. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified linearity.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter full-scale output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$), or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 1). It is specified for DC or low frequency changes. The typical performance curve in Figure 1 shows the effect of high frequency changes in power supply voltages using internal reference, DAC, and op amp.

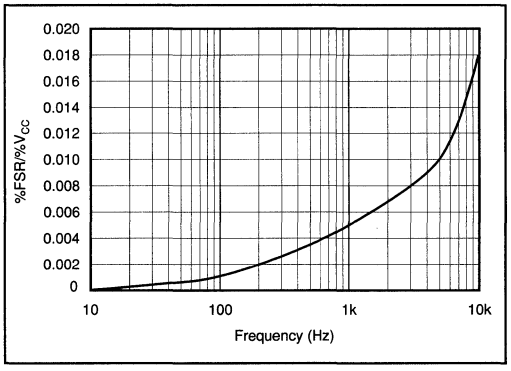


FIGURE 1. Power Supply Sensitivity vs Frequency Using Internal Reference and Op Amp.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in Figure 2. These capacitors (1µF to 10µF tantalum recommended) should be located at the DAC729.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC729 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001µF to 0.01µF capacitor should be connected from Gain Adjust (pin 34) to

common to shunt noise pickup. This capacitor should be a low leakage film type (such as Mylar™ or Teflon™).

Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. See Table II for corresponding codes and Figures 2 and 3 for offset adjustment connections. Offset adjust should be made prior to gain adjust.

Mylar™, Teflon™ E.I. du Pont de Nemours & Co.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and Figure 3 for gain adjustment connections.

OUTPUT RANGE	CODE	CONNECT PIN 23	CONNECT PIN 31	CONNECT PIN 24	GAIN ADJUST 16-BITS	GAIN ADJUST 18-BITS
±10V	COB	to Pin 25	to Pin 26	to Pin 29	9.9969V	9.99992V
±5V	COB	to Pin 27	to Pin 26	to Pin 29	4.9998V	9.99996V
±2.5V	COB	to Pin 27	to Pin 26	to Pins 29 & 25	2.4992V	2.49998V
0 to 10V	CSB	to Pins 25 & 26	N/C	to Pin 29	9.9998V	9.99996V
0 to 5V	CSB	to Pins 27 & 28	N/C	to Pin 29	4.9999V	4.99998V

TABLE II. Output Range Connections and Gain Adjust Voltage.

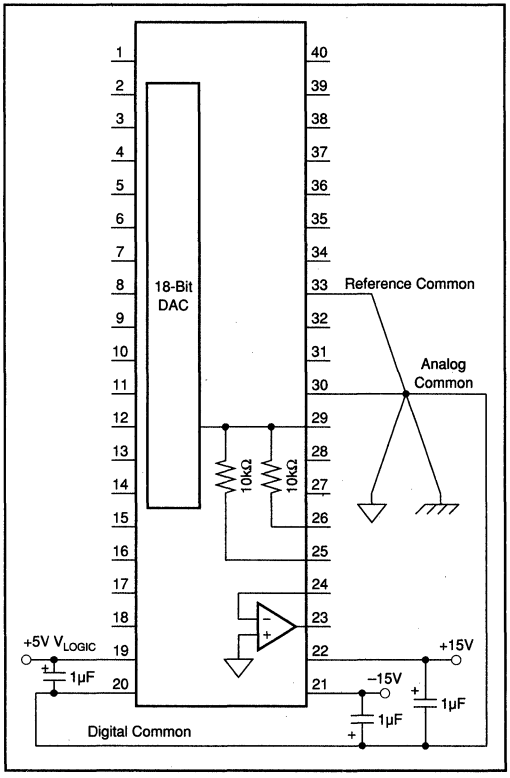


FIGURE 2. Ground Connections and Supply Bypass.

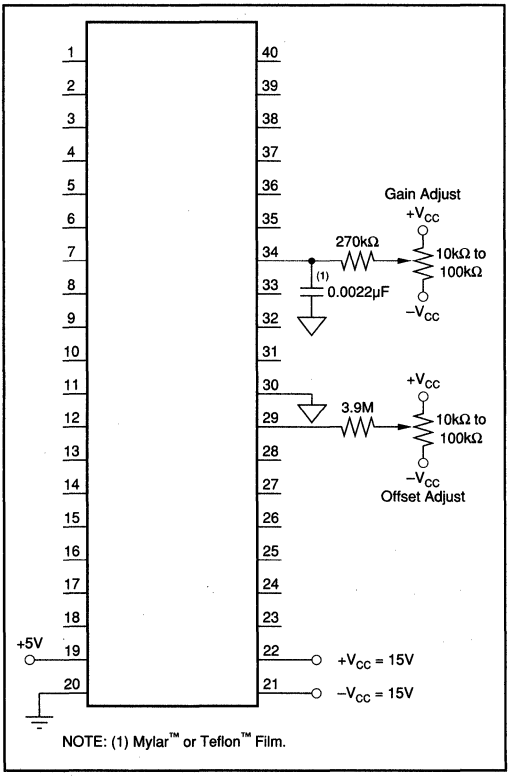


FIGURE 3. Gain and Offset Adjust Hook-Up.

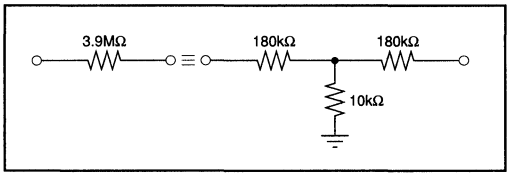


FIGURE 4. Equivalent Resistances.

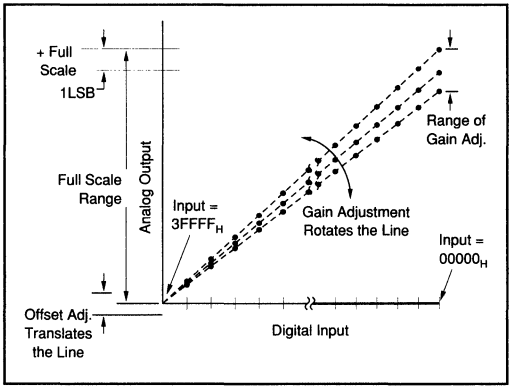


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

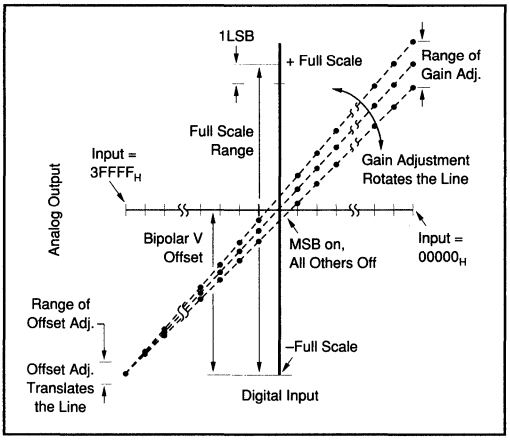


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

REFERENCE ADJUSTMENT

The internal reference may be fine adjusted using pin 35 as shown in Figure 7. Adjusting the reference has a similar effect on the DAC as gain adjust, except the transfer characteristic rotates around bipolar zero for a bipolar connection as shown in Figure 8.

LAYOUT/APPLICATIONS SUGGESTIONS

Obviously, the management of IR drops, power supply noise, thermal stability, and environmental noise becomes much more critical as the accuracy of the system increases. The DAC729 has been designed to minimize these applications problems to a large degree. The basics of "Kelvin sensing" and "holy point" grounding will be the most important considerations in optimizing the absolute accuracy of the system. Figure 9 shows the proper connection of the DAC with the holy-point ground and the Kelvin-sensed-output connection at the load.

The DAC729 has three separate supply common (ground) pins. Reference common (pin 33) carries the return current from the internal reference and the output I/V converter common. The current in pin 33 is stable and independent of code or load. Digital common (pin 20) carries the variable currents of the biasing circuits. Analog common (pin 30) is the termination of the R-2R ladder and also carries the "waste current" from the off side of the current switches. These three ground pins must be star connected to system ground for the DAC to bias properly and accurately. Good ground connections are essential, because an IR drop of just 39µV completely swamps out a 10V FSR 18-bit LSB.

When the application is such that the DAC must control loads of greater than ±5mA with rated accuracy, it is recommended that an external op amp or op amp buffer combination be used to dissipate the variable power external to the DAC729. This minimizes the temperature variations on the precision D/A converter. Figure 10 illustrates a method of connecting the external amplifier for ±10V operation, while using an external reference.

When driving loads to greater than ±10V, care must be taken that the internal resistors are never exposed to greater than ±10V, and that the summing junction is clamped to insure that the voltage never exceeds ±5V. Clamping the summing junction with diodes (parallel opposing connection) to ground will give the best transient response and settling times.

TRUE 18-BIT PERFORMANCE (Differential Linearity Adjustment)

To take full advantage of the DAC729's accuracy, the four MSBs have adjustment capabilities. A simplified schematic (Figure 11) shows the internal structure of the DAC current source and the adjustment input terminal. The suggested network for adjusting the linearity is shown in Figure 12. This circuit has nearly twice the range that is required for the DAC729JH. The range is intentionally narrow so as to minimize the effect of temperature drift or stability problems in the potentiometers. The potentiometers are biased in an identical fashion to the internal DAC current sources to minimize power supply sensitivity and drift over temperature. Low leakage capacitors such as Mylar or Teflon film are essential.

The linearity adjustment requires a digital voltmeter with 7 digits of resolution on the 10V range (1µV resolution) and excellent linearity. For the DAC, 1LSB of the 0V to 10V scale (10 FSR) is 38µV. To be 1/2LSB linear, the measurement must resolve 19µV. The meter must be properly calibrated and linear to 1ppm of range.

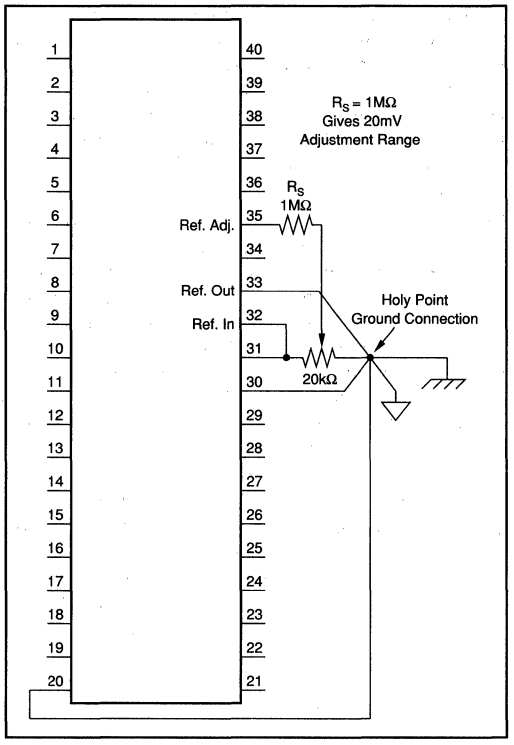


FIGURE 7. V_{REF} Adjust.

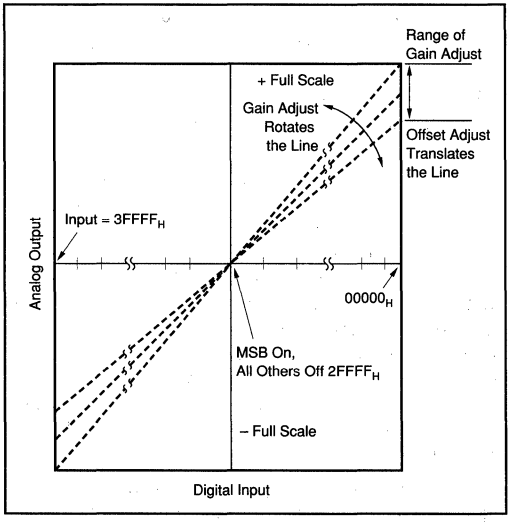


FIGURE 8. Effect of V_{REF} Adjust on a COB Connected DAC729.

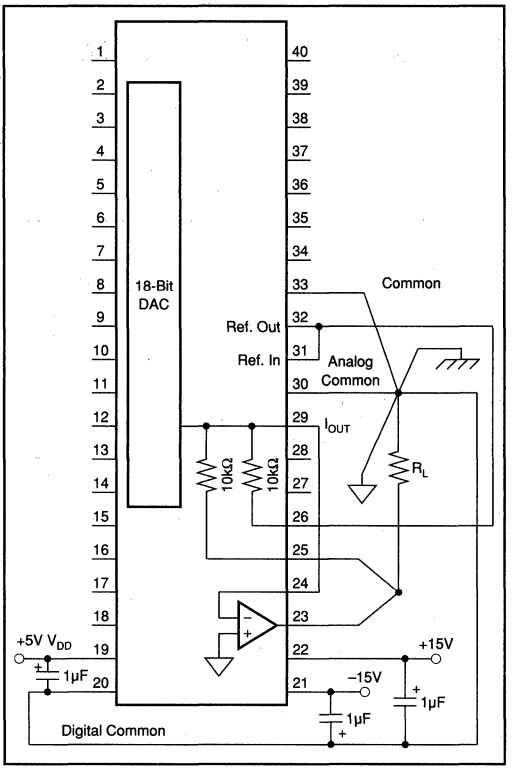


FIGURE 9. Typical Hook-Up Diagram with "Holy Point" Ground and Kelvin Sense Load, Using Internal Op Amp and Reference.

With the DAC connected for 0 to 10V output (Figure 13), the adjustment procedure is to set the DAC code and measure as follows:

FOURTH MSB ADJUSTMENT (Pin 36)

1. Set Code = 11 1100 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 11 1011 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 4th MSB potentiometer to make difference +38µV.
6. Repeat steps 1 through 5 to confirm.

THIRD MSB ADJUSTMENT (Pin 37)

1. Set Code = 11 1000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 11 0111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 3rd MSB potentiometer to make difference +38µV.
6. Repeat steps 1 through 5 to confirm.

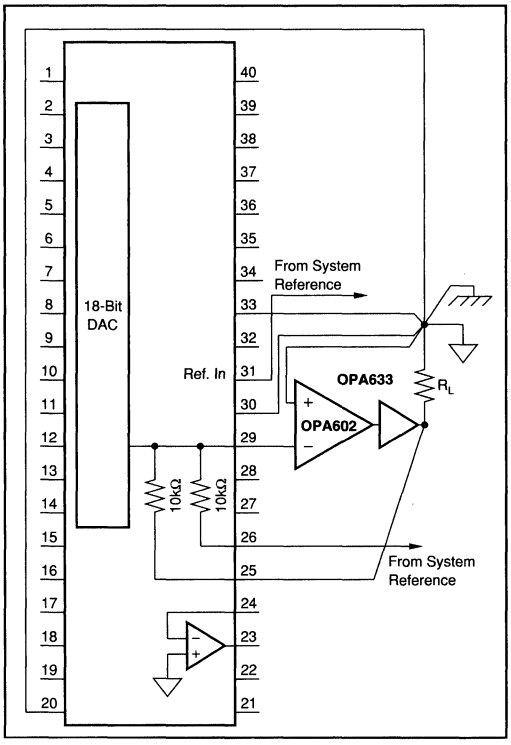


FIGURE 10. Using an External Op Amp with Buffer and External Reference for ±10V Output.

SECOND MSB ADJUSTMENT (Pin 38)

1. Set Code = 11 0000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 10 1111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 2nd MSB potentiometer to make difference +38µV.
6. Repeat steps 1 through 5 to confirm.

MSB ADJUSTMENT (Pin 39)

1. Set Code = 10 0000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 01 1111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust the MSB potentiometer to make difference +38µV.
6. Repeat steps 1 through 5 to confirm.

APPLICATIONS

The DAC729 is the DAC of choice for applications requiring very high resolution, accuracy, and wide dynamic range.

DIGITAL AUDIO

The excellent linearity and differential linearity are ideal for PCM professional audio and waveform generation applications.

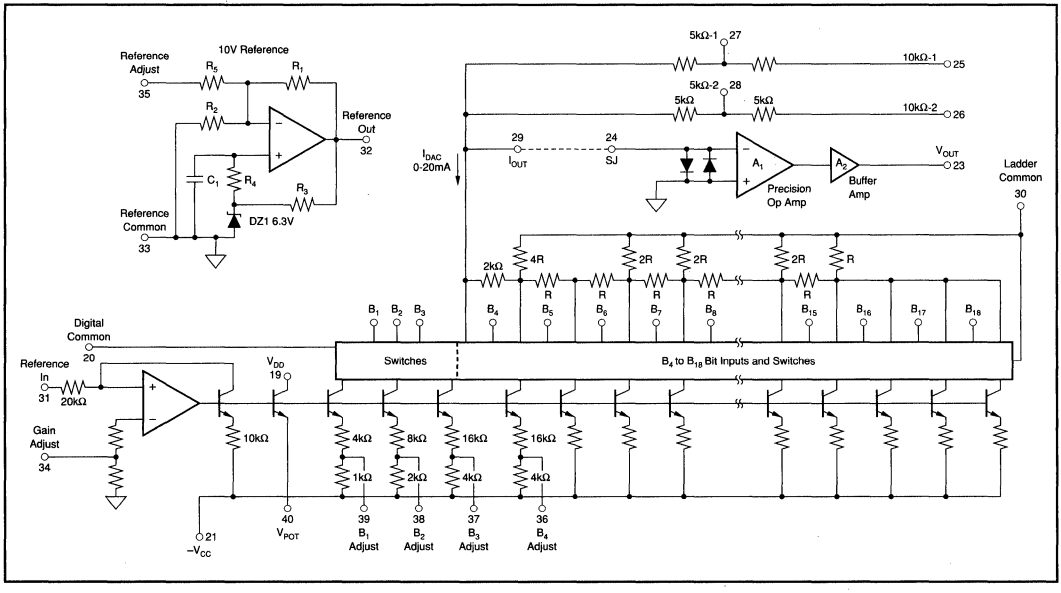


FIGURE 11. DAC729 Simplified Schematic.

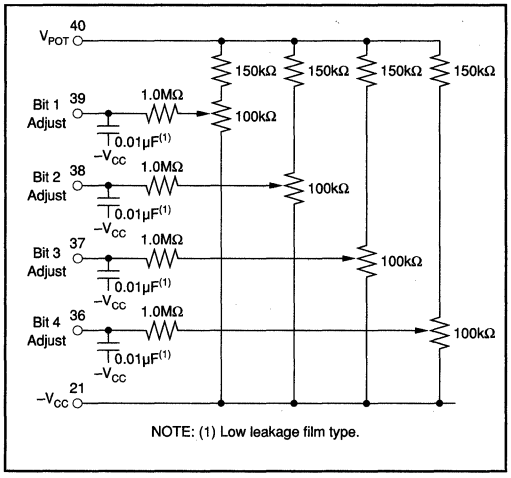


FIGURE 12. Differential Linearity Adjustment Circuit for the 4MSBs.

The DAC729 offers superb dynamic range. Dynamic range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range, usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6dB per bit. For the DAC729 the theoretical range is 108dB! The actual dynamic range is limited by noise (signal-to-noise) and linearity errors. The DAC729's 6µV typical noise floor, fast settling op amp, and adjustable 18-bit linearity minimize the limitation.

Total harmonic distortion (THD) is the measure of the magnitude and distribution of the linearity error, differential linearity error, noise, and quantization error. The THD is defined as the ratio of the square root of the sum of the squares of the harmonics to the values of the input fundamental frequency. The rms value of a DAC error can be shown to be

$$\varepsilon_{RMS} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the DAC729 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\varepsilon_{RMS}}{E_{RMS}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{RMS}} \quad X \times 100\% \quad (2)$$

where E rms is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

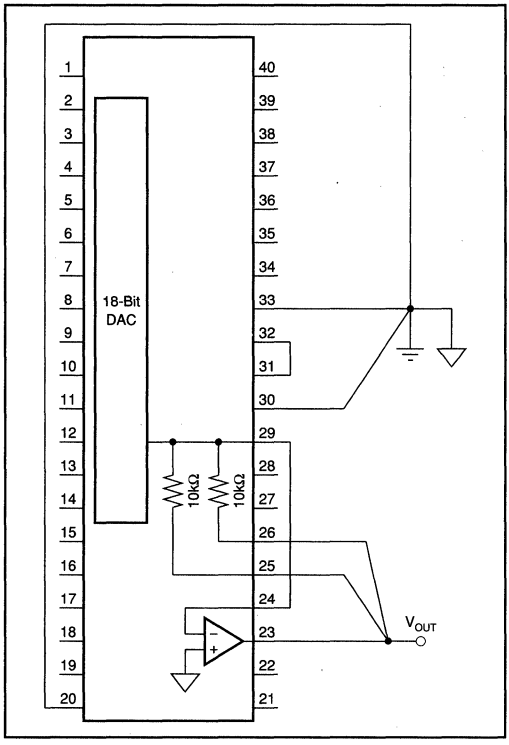


FIGURE 13. 0 to 10V FSR.

The DAC729 has demonstrated THD of 0.0009% at full scale (at 1kHz). This is the level of distortion that is desired to test other professional audio products, making the DAC729 ideal for professional audio test equipment.

The ability to adjust the linearity of the 4MSBs, the 18-bit resolution, fast settling and low noise give the DAC729 unmatched performance.

AUTOMATIC TEST EQUIPMENT

The pin functions of the DAC729 are convenient for use in automatic test equipment systems. The ability to use internal or external reference and internal or external op amp means versatility for the system designer. For example, in automatic test systems with several DACs and ADCs, it is desirable to operate all of the high accuracy converters from the same reference, improving the tracking characteristics of those components to one another. The reference in the DAC729 is a very stable precision reference, and is suitable for use as the system reference.

Test systems, and other large systems are the ideal application for a DAC of this accuracy, because the DAC will be calibrated in the environment in which it will be used. Since the environment is very stable, the manual calibration (Figure 12) may be adequate. However, highly automated systems will go to an automatic calibration routine. Replacing

the potentiometers in Figure 12 with V_{OUT} DACs, and using sample and difference measurements, the major carry bit weights can be measured, and external DACs used to adjust the differential linearity of the DAC729. A successive approximation routine yields the fastest calibration. The output voltage of the external DACs will have to be level shifted, as the bit adjustment potentiometer must be able to achieve $-V_{CC}$ to give the full adjust range.

Because the DAC729 feedback resistors have a tolerance of ±0.1%, the output range can be rescaled slightly with small-value fixed external resistors to give convenient ranges. A popular range is 0V to +10.24V which gives even 5mV steps at 11 bits. In this case, the LSB size is 39.06µV. Figure 14 shows how to connect two 240Ω resistors in series with the internal 10kΩ resistors to give a 0V to 10.24V full-scale range. Another convenient range might be 0V to +10.48576V which gives an even 40µV LSB step size.

THE HEART OF AN 18-BIT ADC

The DAC729 makes a good building block in ADC applications. The key to ADC accuracy is differential linearity of the DAC. The ability to adjust to 18-bit linearity, coupled with the fast settling time of the DAC729 makes the design cycle for an 18-bit successive approximation ADC much faster, and the production more consistent. Figure 15 shows the DAC as the heart of a successive approximation ADC. The clock and successive approximation register could be implemented in 7400 series TTL, as a simple gate-array or standard cell, or part of a local processor.

With the DAC out of the way, the comparator is the toughest part of the ADC design. To resolve an 18-bit LSB, and interface to a TTL-logic device, the comparator must have a gain of 500kV/V (5X actual) as well as low hysteresis, low noise, and low thermally induced offsets. With this much gain, a slow comparator may be desired to reduce the risk of instability.

The feedback resistors of the DAC are the input scaling resistors of the ADC. An OPA602 and an OPA633 make an excellent buffer for the input signal, giving a very high input impedance to the signal (minimizing IR drop) while maintaining the linearity.

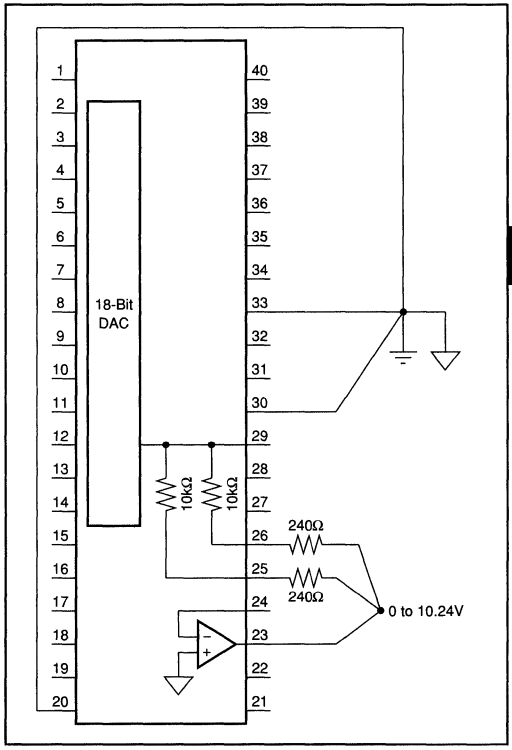


FIGURE 14. 0V to 10.24V Using Internal Op Amp and Internal Reference.

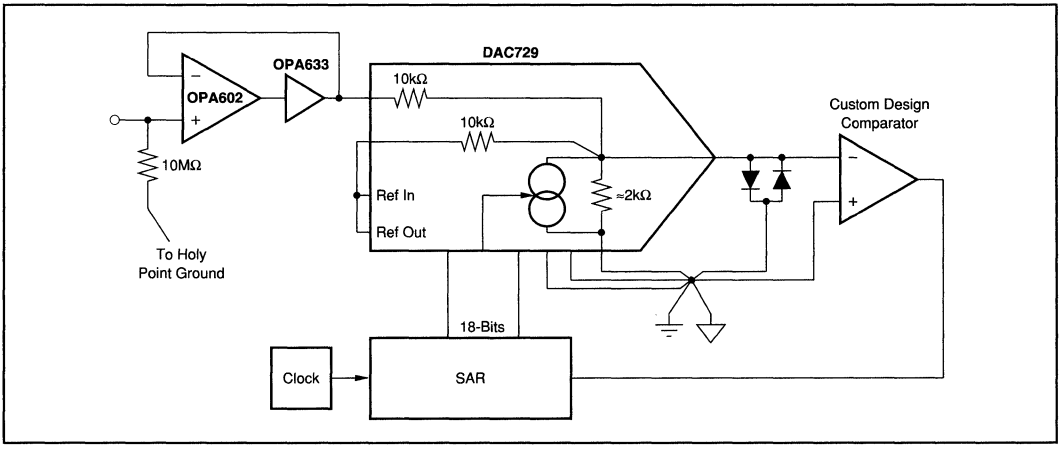


FIGURE 15. Block Diagram of an 18-Bit Resolution ±10V_{IN} ADC.

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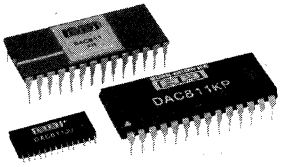


DAC811

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS

DESCRIPTION

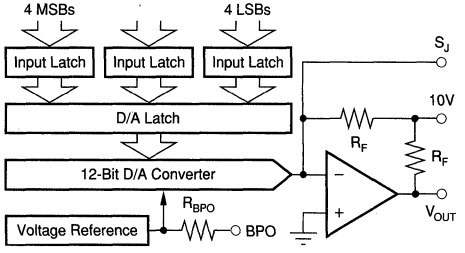
The DAC811 is a complete, single-chip integrated-circuit, microprocessor-compatible, 12-bit digital-to-analog converter. The chip combines a precision voltage reference, microcomputer interface logic, and double-buffered latch, in a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nibbles to permit interfacing to 4-, 8-, 12-, or 16-bit buses and to handle right-or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nibble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B, K, and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in six performance grades and three package types. DAC811J and K are specified over the temperature ranges of 0°C to +70°C; DAC811A and B are specified over –25°C to +85°C; DAC811R and S are specified over –55°C to +125°C. DAC811J and K are packaged in a reliable 28-pin plastic DIP or plastic SOIC package, while DAC811A, B, R and S are available in a 28-pin 0.6" wide dual-inline hermetically sealed ceramic side-brazed package (H package).



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

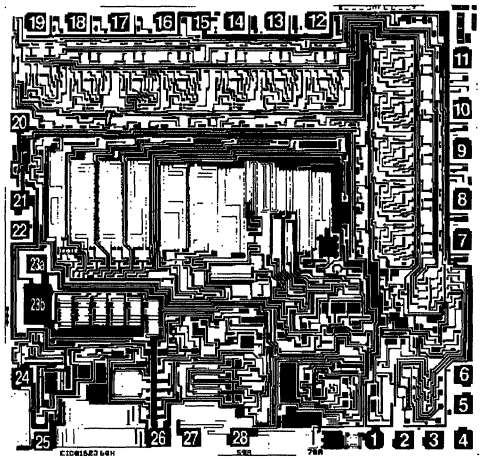
ELECTRICAL

T_A = +25°C. $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

PARAMETER	DAC811AH, JP, JU			DAC811BH, KP, KU			DAC811RH			DAC811SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT													
Resolution			12			*			*			*	Bits
Codes[1]		USB, BOB			*			*			*		
Digital Inputs Over Temperature Range[2]													
V_{IH}	+2		+15	*		*	*		*	*		*	VDC
V_{IL}	0		+0.8	*		*	*		*	*		*	VDC
I_{IH}, V_I = +2.7V			+10			*			*			*	µA
I_{IL}, V_I = +0.4V			±20			*			*			*	µA
Digital Interface Timing Over Temperature Range													
t_{WP}, $\overline{WR}$ Pulse Width	50			*			*			*			ns
t_{AW}1, $\overline{N_X}$ and $\overline{LDAC}$ Valid to End of $\overline{WR}$	50			*			*			*			ns
t_{DW}, Data Valid to End of $\overline{WR}$	80			*			*			*			ns
t_{DH}, Data Valid Hold Time	0			*			+10			*			ns
ACCURACY													
Linearity Error		±1/4	±1/2		±1/8	±1/4		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]		±0.1	±0.2		*	*		*	*		*	*	%
Offset Error[3, 4]		±0.05	±0.15		*	*		*	*		*	*	% of FSR[5]
Monotonicity		Guaranteed			*			*			*		
Power Supply Sensitivity: $+V_{CC}$		±0.001	±0.003		*	*		*	*		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.002	±0.006		*	*		*	*		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		*	*		*	*		*	*	% of FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)													
Gain		±10	±30		±10	±20		±15	±30		±15	±30	ppm/°C
Unipolar Offset		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			*			*			*		
SETTLING TIME[6] (to within ±0.01% of FSR of Final Value; 2kΩ load)													
For Full Scale Range Change, 20V Range		3	4		*	*		*	*		*	*	µs
10V Range		3	4		*	*		*	*		*	*	µs
For 1LSB Change at Major Carry[7]		1			*			*			*		µs
Slew Rate[6]	8	12		*	*		*	*		*	*		V/µs
ANALOG OUTPUT													
Voltage Range ($\pm V_{CC}$ = 15V)[8]: Unipolar		0 to +10			*			*			*		V
Bipolar		±5, ±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance (at DC)		0.2			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		
REFERENCE VOLTAGE													
Voltage	+6.2	+6.3	+6.4	*	*	*	*	*	*	*	*	*	V
Source Current Available for External Loads	+2			*			*			*			mA
Temperature Coefficient		±10	±30		±10	±20		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16.5	*	*	*	*	*	*	*	*	*	VDC
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	*	*	*	VDC
Current (no load): $+V_{CC}$		+16	+25		*	*		*	*		*	*	mA
$-V_{CC}$		−23	−35		*	*		*	*		*	*	mA
V_{DD}		+8	+15		*	*		*	*		*	*	mA
Potential at DCOM with Respect to ACOM[9]		±0.5			*				*			*	V
Power Dissipation		625	800		*	*		*	*		*	*	mW
TEMPERATURE RANGE													
Specification: J, K	0		+70	*		*	*		*	*		*	°C
A, B	−25		+85	*		*	*		*	*		*	°C
R, S	−65		+150	*		*	*		*	*		*	°C
							−55		+125	*		*	°C
Storage: J, K	−60		+100	*		*	*		*	*		*	°C
A, B, R, S	−65		+150	*		*	*		*	*		*	°C

* Specification same as model to immediate left.

NOTES: (1) USB = unipolar straight binary; BOB = bipolar offset binary. (2) TTL, LSTTL and 54/74 HC compatible. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means full scale range and is 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.



DAC811 DIE TOPOGRAPHY

MECHANICAL INFORMATION

	MILS (0.001")
Die Size	134 x 128
Min. Pad Size	4 x 4

Backside Bias: $-V_{CC}$

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	$+V_{DD}$	Logic supply, +5V.
2	$\overline{WR}$	Write, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	Load D/A converter, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	Nibble A, enables $\overline{WR}$ to load input latch A (the most significant nibble). Logic low enables.
5	$\overline{N_B}$	Nibble B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	Nibble C, enables $\overline{WR}$ to load input latch C (the least significant nibble). Logic low enables.
7	D_{11}	Data bit 12, MSB, positive true.
8	D_{10}	Data bit 11.
9	D_9	Data bit 10.
10	D_8	Data bit 9.
11	D_7	Data bit 8.
12	D_6	Data bit 7.
13	D_5	Data bit 6.
14	D_4	Data bit 5.
15	DCOM	Digital common, V_{DD} supply return.
16	D_0	Data bit 1, LSB.
17	D_1	Data bit 2.
18	D_2	Data bit 3.
19	D3	Data bit 4.
20	$+V_{CC}$	Analog supply input, +15V or +12V.
21	$-V_{CC}$	Analog supply input, –15V or –12V.
22	Gain Adj	To externally adjust gain.
23	ACOM	Analog common, $\pm V_{cc}$ supply return.
24	V_{OUT}	D/A converter voltage output.
25	10V Range	Connect to pin 24 for 10V range.
26	SJ	Summing junction of output amplifier.
27	BPO	Bipolar offset. Connect to pin 26 for bipolar operation.
28	Ref Out	6.3V reference output.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (Pins 2–14, 16–19) to DCOM	–0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
Ref Out	Indefinite Short to ACOM
External Voltage Applied to DAC Output	–5V to +5V
Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, θ_{J-A}: Plastic DIP and SOIC	100°C/W
Ceramic DIP	65°C/W

NOTE: Stresses above those listed above may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

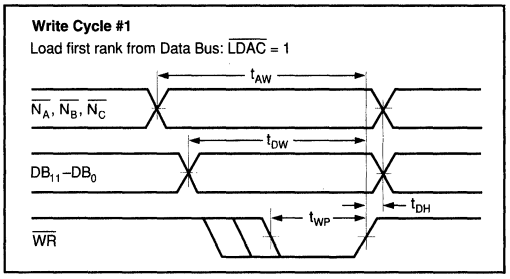
MODEL	PACKAGE	TEMPERATURE RANGE (°C)	LINEARITY ERROR, MAX AT +25°C	GAIN DRIFT (ppm/°C)
DAC811JP	Plastic DIP	0 to +70	±1/2LSB	30
DAC811JU	Plastic SOIC	0 to +70	±1/2LSB	30
DAC811KP	Plastic DIP	0 to +70	±1/4LSB	15
DAC811KU	Plastic SOIC	0 to +70	±1/4LSB	15
DAC811AH	Ceramic DIP	–25 to +85	±1/2LSB	30
DAC811BH	Ceramic DIP	–25 to +85	±1/4LSB	15
DAC811RH	Ceramic DIP	–55 to +125	±1/2LSB	30
DAC811SH	Ceramic DIP	–55 to +125	±1/4LSB	20

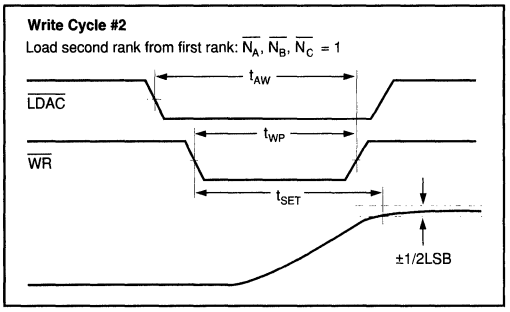
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC811AH	28-Pin Side-Brazed DIP	149
DAC811BH	28-Pin Side-Brazed DIP	149
DAC811RH	28-Pin Side-Brazed DIP	149
DAC811SH	28-Pin Side-Brazed DIP	149
DAC811JP	28-Pin Plastic DIP	215
DAC811KP	28-Pin Plastic DIP	215
DAC811JU	28-Pin SOIC	217
DAC811KU	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TIMING DIAGRAMS





DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive-true binary input codes. DAC811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB ↓ ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111	+ Full Scale	+ Full Scale	–1LSB
100000000000	+ 1/2 Full Scale	Zero	– Full Scale
011111111111	+ 1/2 Full Scale – 1LSB	–1LSB	+ Full Scale
000000000000	Zero	– Full Scale	Zero
* Invert MSB of the BOB code with external inverter to obtain BTC code.			

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all 1s and all 0s). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A, J, and R grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC811 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full scale range value (e.g., +FS minus –FS) at high temperature, +25°C, and low temperature, calculating the error with respect to the +25°C value, and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0s on the input over the specification temperature range. Offset is measured at high temperature, +25°C, and low temperature. The offset drift is the maximum change in offset referred to the +25°C value, divided by the temperature change. It is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.1V. The reference output may be used to drive external loads, sourcing at least 2mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

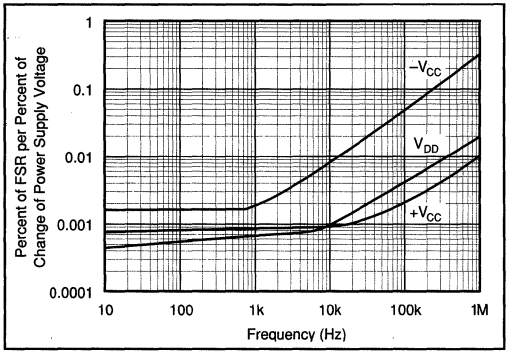


FIGURE 1. Power Supply Rejection vs Power Supply Ripple Frequency.

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$, and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic 0. When either $\overline{N_A}$, ($\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic 1, the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic 0.

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic 0. When either $\overline{LDAC}$ or $\overline{WR}$ are at logic 1, the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic 0.

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When any one of the control signals returns to logic 1, the data is latched. Table II is a truth table for all latches.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No operation
0	0	1	1	1	Enables input latch 4MSBs
0	1	0	1	1	Enables input latch 4 middle bits
0	1	1	0	1	Enables input latch 4LSBs
0	1	1	1	0	Loads D/A latch from input latches
0	0	0	0	0	Makes all latches transparent
"X" = Don't care.					

TABLE II. DAC813 Interface Logic Truth Table.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output, and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

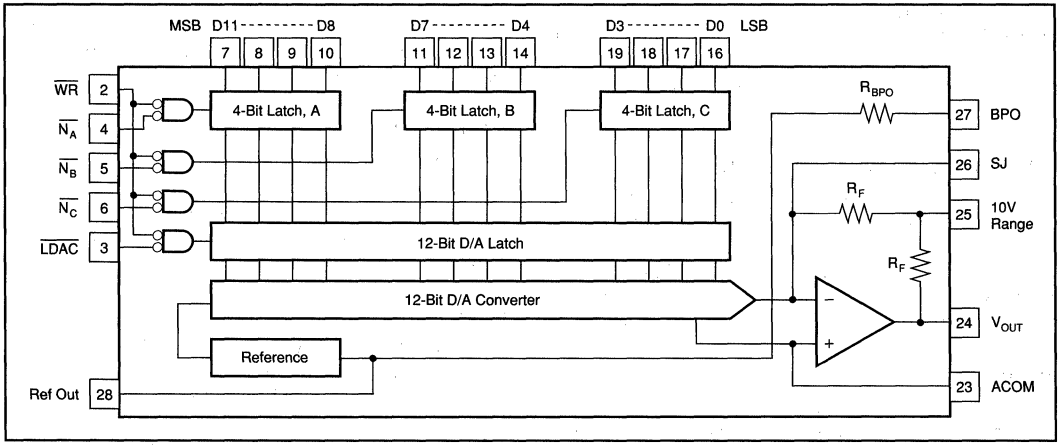


FIGURE 2. DAC811 Block Diagram.

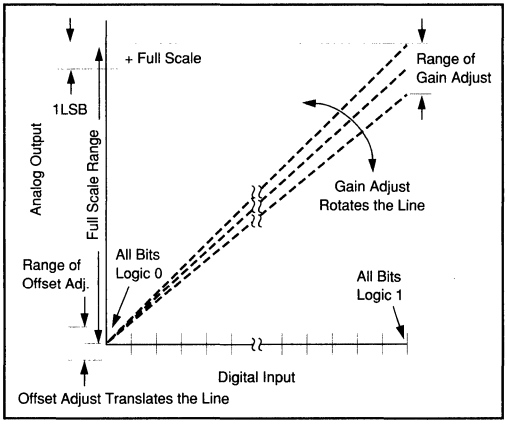


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

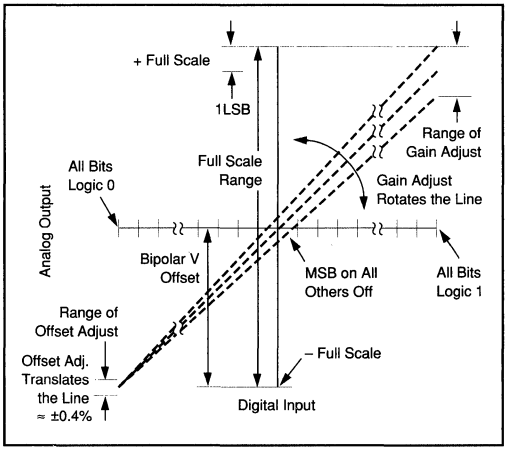


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT		
	0 to +10V	±5V	±10V
MSB LSB ↓ ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5V	0V	0V
011111111111	+4.9976V	–0.0024V	–0.0049V
000000000000	0V	–5V	–10V
LSB	2.4mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12VB supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TLL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B and 54/74C CMOS devices.

Resistors of 47kΩ should be placed in series with D0 through D11, $\overline{WR}$, $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ if edges are <10ns or if the logic input is driven below ground by undershoot.

INSTALLATION

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in Figure 5.

These capacitors (1µF tantalum recommended) should be located close to the DAC811.

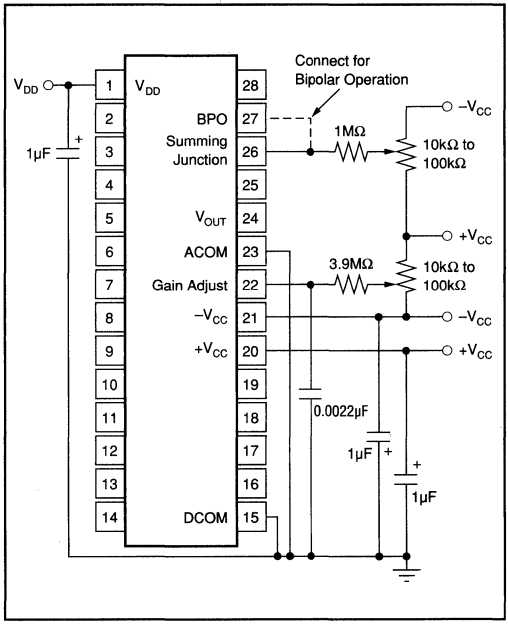


FIGURE 5. Power Supply, Gain, and Offset Potentiometer Connections.

DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The analog common (pin 23) and digital common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiometers should be 100ppm/°C or less. The 1MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001µF to 0.01µF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment. Excessive capacitance on the Gain Adjust or Offset Adjust pin may affect slew rate and settling time.

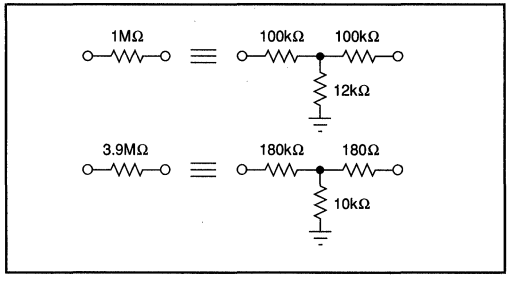


FIGURE 6. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or a unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.

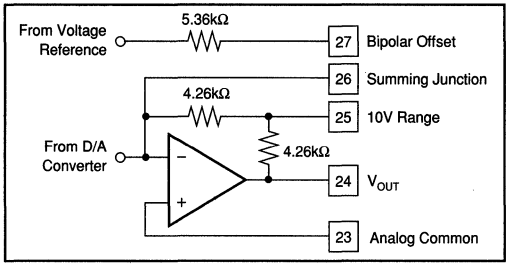


FIGURE 7. Output Amplifier Voltage Range Scaling Circuit.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 25 TO	CONNECT PIN 27 TO
0 to +10V	USB	24	23
±5	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

TABLE IV. Output Range Connections.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface to microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether. For instance, if half the memory space is unused, address line A15 of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each DAC811 occupies four address locations. A 74LS139 provides the two-to-four decoder and selects it with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. An 8205 decoder is an alternative to the 74LS139.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right-justified data formats, as illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 10 and 11 show an addressing scheme for right-justified and left-justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right-justified case, $X10_{16}$ loads the 8LSBs, and $X01_{16}$ loads the 4MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

Left-justified data is handled in a similar manner, shown in Figure 11. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.

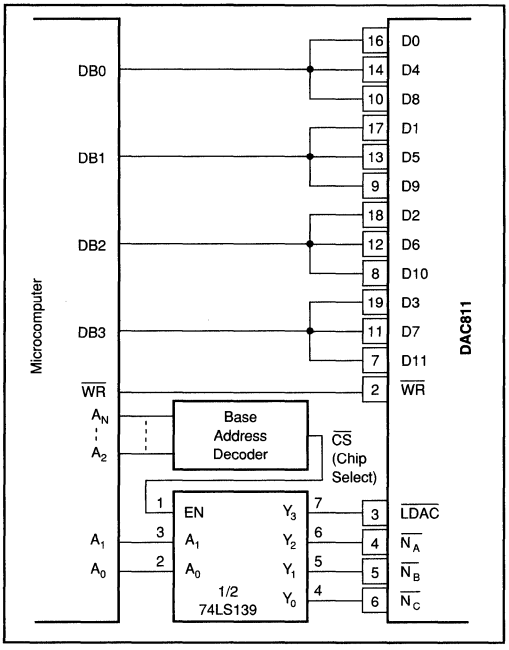


FIGURE 8. Addressing and Control for 4-Bit Microcomputer Interface.

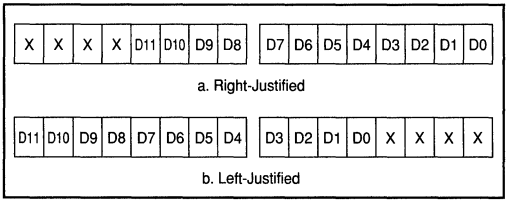


FIGURE 9. 12-Bit Data Format for 8-Bit Systems.

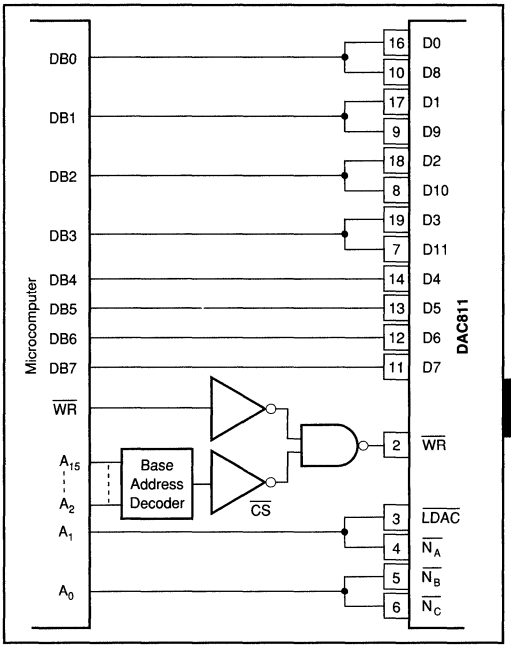


FIGURE 10. Right-Justified Data Bus Interface.

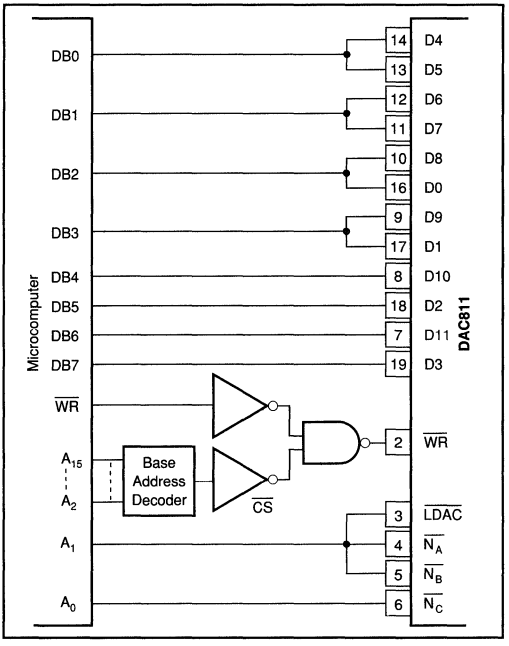


FIGURE 11. Left-Justified Data Bus Interface.

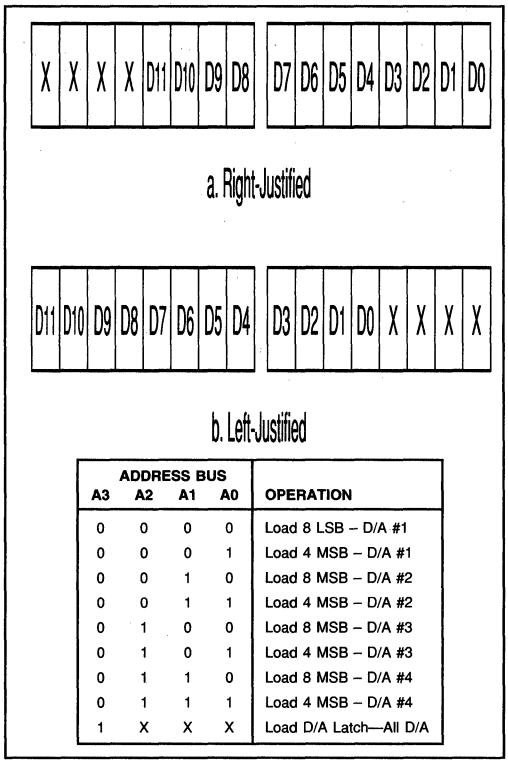
INTERFACING MULTIPLE DAC811s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 12 uses a 74LS138 decoder to decode a set of eight adjacent addresses, to load the input latches of four DAC811s. The example shows a right-justified data format.

A ninth address using A_3 causes all DAC811s to be updated simultaneously. If a particular DAC811 is always loaded last—for instance, D/A #4—A_3 is not needed, thus saving eight address spaces for other uses. Incorporate A_3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

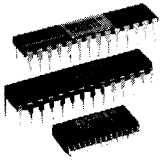
For this application, the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$ and $\overline{N_C}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC811, is selected by the address decoder and strobed by $\overline{WR}$.



ADDRESS BUS A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 MSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 MSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 MSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 12. Interfacing Multiple DAC811s to an 8-Bit Bus.

BURR-BROWN®



DAC813

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

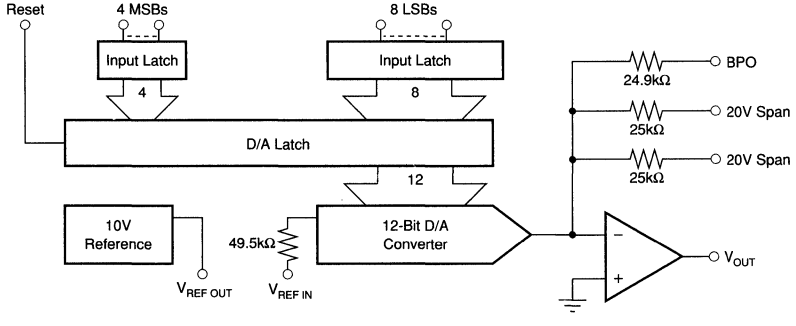
DESCRIPTION

The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to ±1/2LSB maximum linearity error (J, A grades) and ±1/4LSB (K, B grades). It is packaged in a 28-pin 0.3" wide ceramic DIP (–40°C to +85°C specification temperature range), 28-pin 0.3" wide plastic DIP and 28-lead plastic SO (0°C to +70°C).



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±12V or ±15V and load on V_{OUT} = 5kΩ || 500pF to common unless otherwise noted.

PARAMETER	CONDITIONS	DAC813AH, JP, JU, AU			DAC813BH, KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution				12			*	Bits
Codes[1]			USB, BOB			*		
Digital Inputs Over Temperature Range[2]								
V_{IH}[3]		+2		+5.5	*		*	VDC
V_{IL}		0		+0.8	*		*	VDC
DATA Bits, $\overline{WR}$, $\overline{Reset}$, $\overline{LDAC}$, $\overline{LMSB}$, $\overline{LLSB}$				±10			*	µA
I_{IH}	V_{IN} = +2.7V			±10			*	µA
I_{IL}	V_{IN} = +0.4V							
ACCURACY								
Linearity Error			±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error			±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[4]			±0.05	±0.2		*	*	%
Unipolar Offset Error[5]			±0.01	±0.02		*	*	% of FSR[7]
Bipolar Zero Error[6]			±0.02	±0.2		*	*	% of FSR
Monotonicity			Guaranteed			*		
Power Supply Sensitivity: $+V_{CC}$	20V Range		5	10		*	*	ppm of FSR/%
$-V_{CC}$			1	10		*	*	ppm of FSR/%
DRIFT	Over Specification							
Gain	Temperature Range		±5	±30		*	±15	ppm/°C
Unipolar Offset			±1	±3		*	±3	ppm of FSR/°C
Bipolar Zero			±3	±10		*	±5	ppm of FSR/°C
Linearity Error Over Temperature Range			±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range			Guaranteed			*		
SETTLING TIME[8] (To Within ±0.01% of FSR of Final Value; 5kΩ || 500pF load)								
For Full Scale Range Change	20V Range		4.5	6		*	*	µs
	10V Range		3.3	5		*	*	µs
For 1LSB Change at Major Carry[9]			2			*		µs
Slew Rate			10			*		V/µs
ANALOG OUTPUT								
Voltage Range: Unipolar	$\pm V_{CC} > \pm 11.4V$		0 to +10			*		V
Bipolar	$\pm V_{CC} > \pm 11.4V$		±5, ±10			*		V
Output Current		±5			*			mA
Output Impedance	At DC		0.2			*		Ω
Short Circuit to Common Duration			Indefinite			*		
REFERENCE VOLTAGE								
Voltage		+9.95	+10	+10.05	*	*	*	V
Source Current Available for External Loads		5			*			mA
Impedance			2			*		Ω
Temperature Coefficient			±5	±25		*	*	ppm/°C
Short Circuit to Common Duration			Indefinite			*		
POWER SUPPLY REQUIREMENTS								
Voltage: $+V_{CC}$		+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$		−11.4	−15	−16.5	*	*	*	VDC
Current: $+V_{CC} + V_L$	No Load		13	15		*	*	mA
$-V_{CC}$	No Load		−5	−7		*	*	mA
Potential at DCOM with Respect to ACOM[10]		−3		+3	*		*	V
Power Dissipation			270	330		*	*	mW
TEMPERATURE RANGE								
Specification: J, K		0		+70	*		*	°C
A, B		−40		+85	*		*	°C
Operating: J, K		−40		+85	*		*	°C
A, B		−55		+125	*		*	°C
Storage: J, K		−60		+100	*		*	°C
A, B		−65		+150	*		*	°C

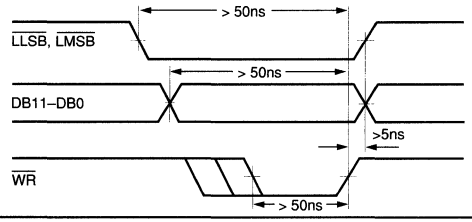
*Same as specification for DAC813AH, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (5) Error at input code 000_{HEX} for unipolar mode, FSR = 10V. (6) Error at input code 800_{HEX} for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (7) FSR means Full Scale Range and is 20V for the ±10V range. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

MINIMUM TIMING DIAGRAMS

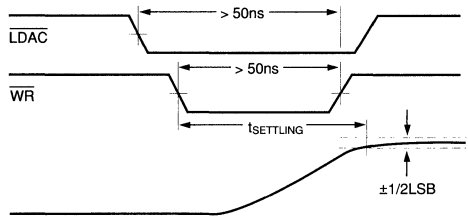
WRITE CYCLE #1

(Load first rank from Data Bus: $\overline{LDAC}$ = 1)



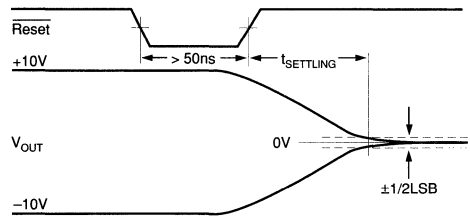
WRITE CYCLE #2

(Load second rank from first rank: $\overline{LLSB}$, $\overline{LMSB}$ = 1)



RESET COMMAND (Bipolar Mode)

$\overline{LLSB}$, $\overline{LMSB}$, $\overline{LDAC}$, $\overline{WR}$ = Don't Care



ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
DCOM with respect to ACOM	±4V
Digital Inputs (Pins 11–15, 17–28) to DCOM	–0.5V to $+V_{CC}$
External Voltage Applied to BPO Span Resistor	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to ACOM
V_{OUT}	Indefinite Short to ACOM
Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, θ_{J-A}: Plastic DIP and SOIC	130°C/W
Ceramic DIP	85°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

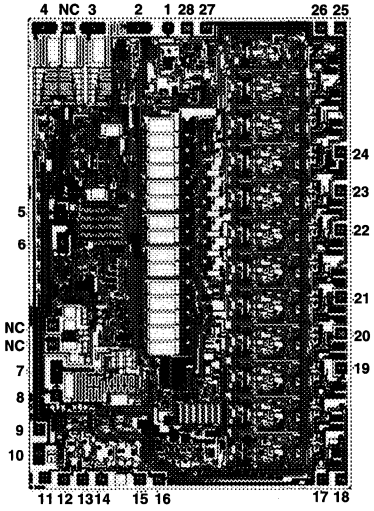
PIN	NAME	DESCRIPTION
1	$+V_L$	Positive supply pin for logic circuits. Connect to $+V_{CC}$.
2, 3	20V Range	Connect Pin 2 or Pin 3 to Pin 9 (V_{OUT}) for a 20V FSR. Connect both to Pin 9 for a 10V FSR.
4	BPO	Bipolar offset. Connect to Pin 6 ($V_{REF\ OUT}$) through 100Ω resistor or 200Ω potentiometer for bipolar operation.
5	ACOM	Analog common, $\pm V_{CC}$ supply return.
6	$V_{REF\ OUT}$	+10V reference output referred to ACOM.
7	$V_{REF\ IN}$	Connected to $V_{REF\ OUT}$ through a 1kΩ gain adjustment potentiometer or a 500Ω resistor.
8	$+V_{CC}$	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V_{OUT}	D/A converter voltage output.
10	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
11	$\overline{WR}$	Master enable for $\overline{LDAC}$, $\overline{LLSB}$, and $\overline{LMSB}$. Must be low for data transfer to any latch.
12	$\overline{LDAC}$	Load DAC. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	$\overline{Reset}$	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	$\overline{LMSB}$	Enable for 4-bit input latch of D_8-D_{11} data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path.
15	$\overline{LLSB}$	Enable for 8-bit input latch of D_0-D_7 data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DICE INFORMATION



DAC813 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	$+V_L$	15	$\overline{LLSB}$
2	20V Range	16	DCOM
3	20V Range	17	DB0 (LSB)
4	BPO	18	DB1
5	ACOM	19	DB2
6	$V_{REF\ OUT}$	20	DB3
7	$V_{REF\ IN}$	21	DB4
8	$+V_{CC}$	22	DB5
9	V_{OUT}	23	DB6
10	$-V_{CC}$	24	DB7
11	$\overline{WR}$	25	DB8
12	$\overline{LDAC}$	26	DB9
13	$\overline{Reset}$	27	DB10
14	$\overline{LMSB}$	28	DB11 (MSB)

Substrate Bias: $-V_{CC}$
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	204 x 140 ±5	5.18 x 3.56 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C	GAIN DRIFT (ppm/°C)
DAC813AU	Plastic SOIC	–40°C to +85°C	±1/2LSB	±30
DAC813JP	Plastic DIP	0°C to +70°C	±1/2LSB	±30
DAC813JU	Plastic SOIC	0°C to +70°C	±1/2LSB	±30
DAC813KP	Plastic DIP	0°C to +70°C	±1/4LSB	±15
DAC813KU	Plastic SOIC	0°C to +70°C	±1/4LSB	±15
DAC813AH	Ceramic DIP	–40°C to +85°C	±1/2LSB	±30
DAC813BH	Ceramic DIP	–40°C to +85°C	±1/4LSB	±15

PACKAGE INFORMATION

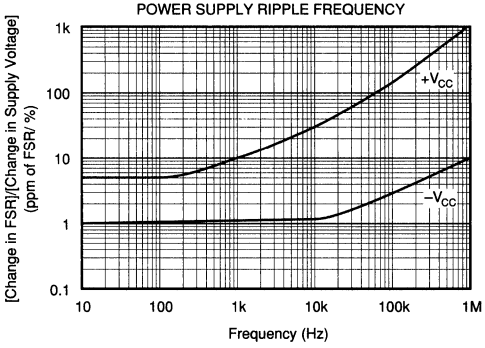
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC813AH	28-Pin Hermetic Side-Brazed DIP	247
DAC813BH	28-Pin Hermetic Side-Brazed DIP	247
DAC813AP	28-Pin Plastic DIP	246
DAC813KP	28-Pin Plastic DIP	246
DAC813AU	28-Pin Plastic SOIC	217
DAC813JU	28-Pin Plastic SOIC	217
DAC813KU	28-Pin Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

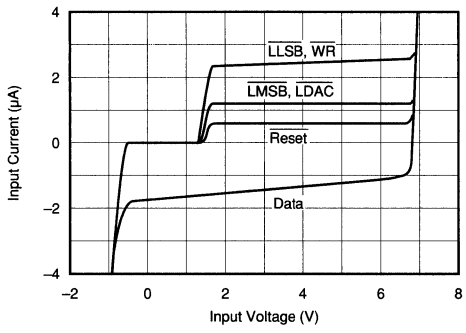
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

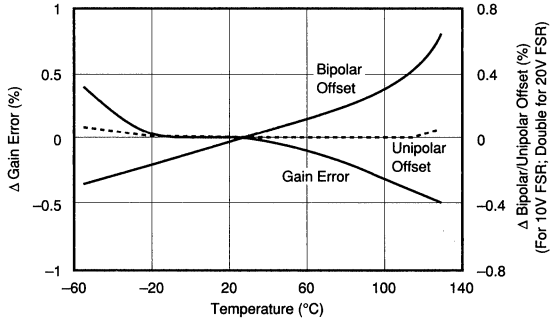
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



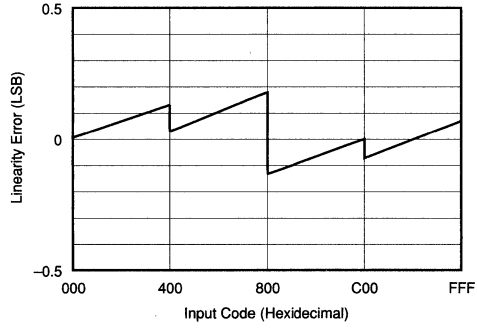
DIGITAL INPUT CURRENT
vs INPUT VOLTAGE



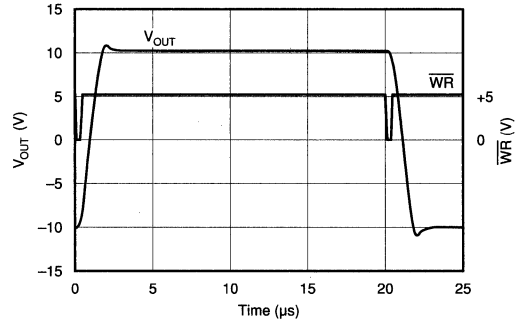
CHANGE OF GAIN AND OFFSET ERROR
vs TEMPERATURE



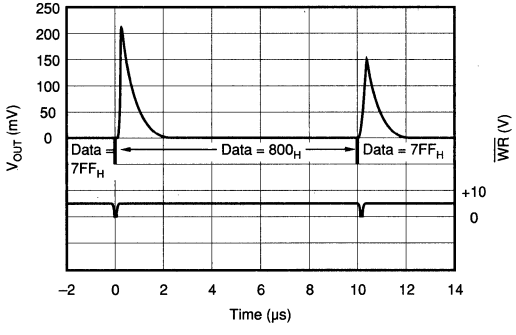
INTEGRAL LINEARITY ERROR



± FULL SCALE OUTPUT SWING

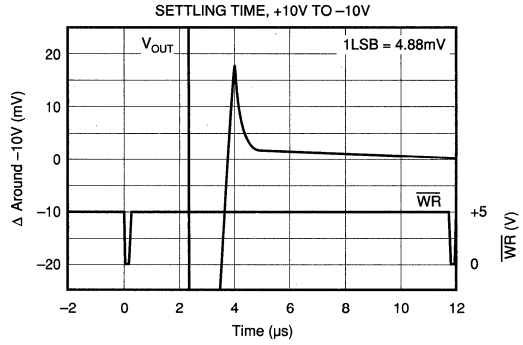


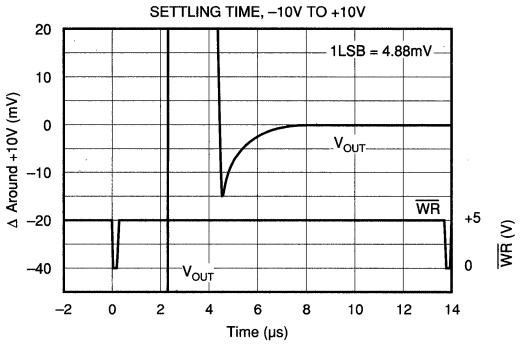
MAJOR CARRY GLITCH



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
FFF_{HEX}	+ Full Scale	+ Full Scale	Zero – 1LSB
800_{HEX}	+ 1/2 Full Scale	Zero	– Full Scale
$7FF_{HEX}$	+ 1/2 Full Scale – 1LSB	Zero – 1LSB	+ Full Scale
000_{HEX}	Zero	– Full Scale	Zero
* Invert MSB of BOB code with external inverter to obtain BTC code.			

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar Offset Drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.012% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of ±50mV. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 500Ω. The connection can be made through an optional 1kΩ trim resistor to provide adjustment to zero

gain error. The reference output may be used to drive external loads, sourcing at least 5mA. This current should be constant, otherwise the gain of the converter will vary.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a ppm of FSR output change per percent of change in either $+V_{CC}$ or $-V_{CC}$ about the nominal voltages expressed in ppm of FSR/%. The first performance curve on page 5 shows typical power supply rejection versus power supply ripple frequency.

OPERATION

DAC813 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

INTERFACE LOGIC

Input latches hold data temporarily while a complete 12-bit word is assembled before loading into the D/A latch. This double-buffered organization prevents the generation of spurious analog output values. Each latch is independently addressable.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for the control signals is presented in Table II.

$\overline{WR}$	$\overline{LLSB}$	$\overline{LMSB}$	$\overline{LDAC}$	RESET	OPERATION
1	X	X	X	1	No operation
X	X	X	X	0	D/A latch set to 800_{HEX}
0	1	0	1	1	Enables 4 MSBs input latch
0	0	1	1	1	Enables 8 LSBs input latch
0	1	1	0	1	Loads D/A latch from input latches
0	0	0	0	1	Makes all latches transparent
"X" = Don't Care					

TABLE II. DAC813 Interface Logic Truth Table.

CAUTION: DAC813 was designed to use $\overline{WR}$ as the fast strobe. $\overline{WR}$ has a much faster logic path than $\overline{EN}_X$ (or $\overline{LDAC}$). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_X$ to strobe data into the latches, the DATA HOLD time will be long, approximately 15ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

LOGIC INPUT COMPATIBILITY

The DAC813 digital inputs are TTL, 5V CMOS compatible over the operating range of $+V_{CC}$. The input switching threshold remains at the TTL threshold over the supply range. An equivalent circuit of a digital input is shown in Figure 2.

The logic input current over temperature is low enough to permit driving the DAC813 directly from the outputs of 5V CMOS devices.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition,

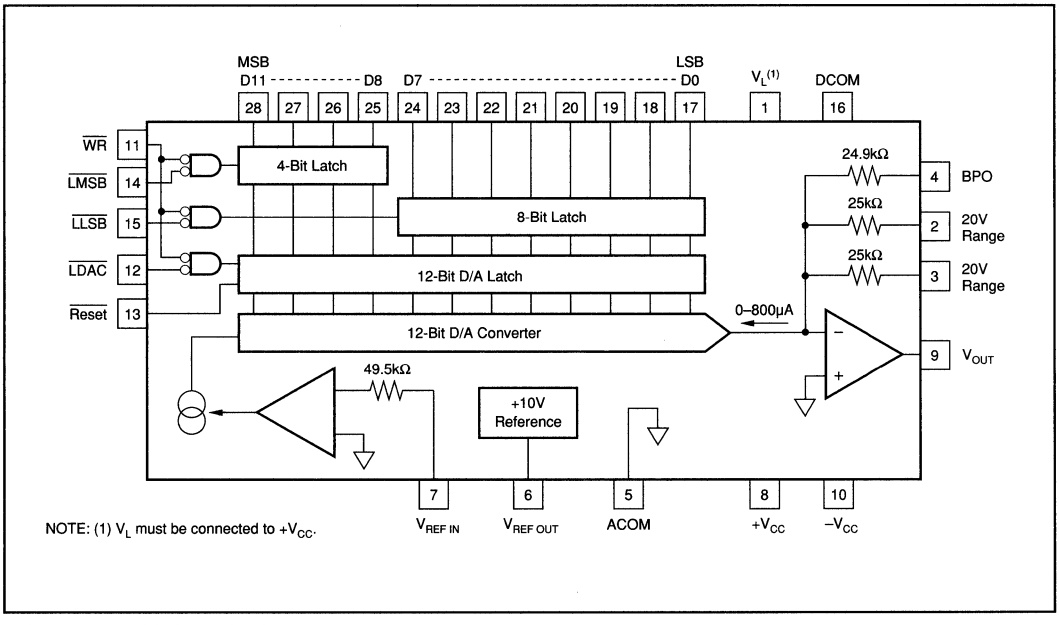


FIGURE 1. DAC813 Block Diagram.

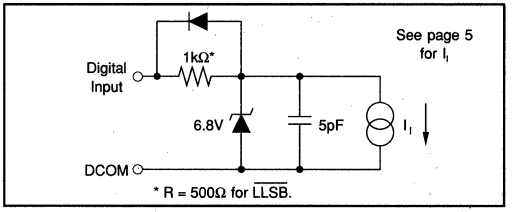


FIGURE 2. Equivalent Input Circuit for Digital Inputs.

the speed of the interface will be slower. A digital output driving a DATA input line of the DAC813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

RESET FUNCTION

When asserted low (<0.8V), $\overline{\text{RESET}}$ (Pin 13) forces the D/A latch to 800_{HEX} regardless of any other input logic condition. If the analog output is connected for bipolar operation (either ±10V or ±5V), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If $\overline{\text{RESET}}$ is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available $\overline{\text{Reset}}$ can be connected to $+V_{CC}$ through a 100kΩ to 1MΩ resistor to limit the input current.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	0 to +10V	±5V	±10V
FFF_{HEX}	+9.9976V	+4.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+4.9976V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	–5.0000V	–10.0000V
1LSB	2.44mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to $-V_{CC}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Optimum settling performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$ and at least a 0.01µF ceramic capacitor at $+V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well. The 0.01µF capacitors should be located close to the DAC813.

Pin 1 supplies internal logic and **must** be connected to $+V_{CC}$.

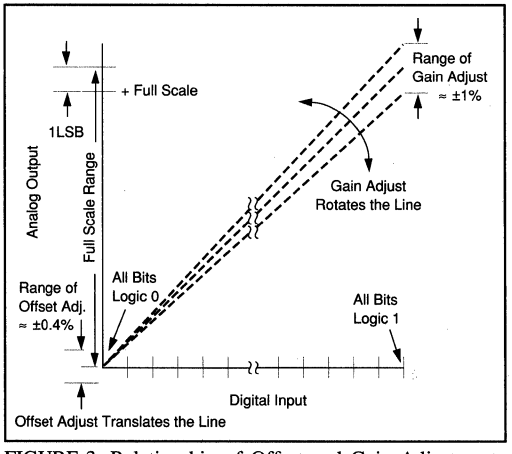


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

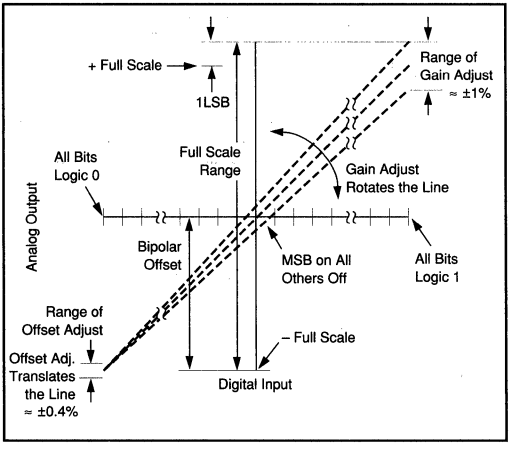


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

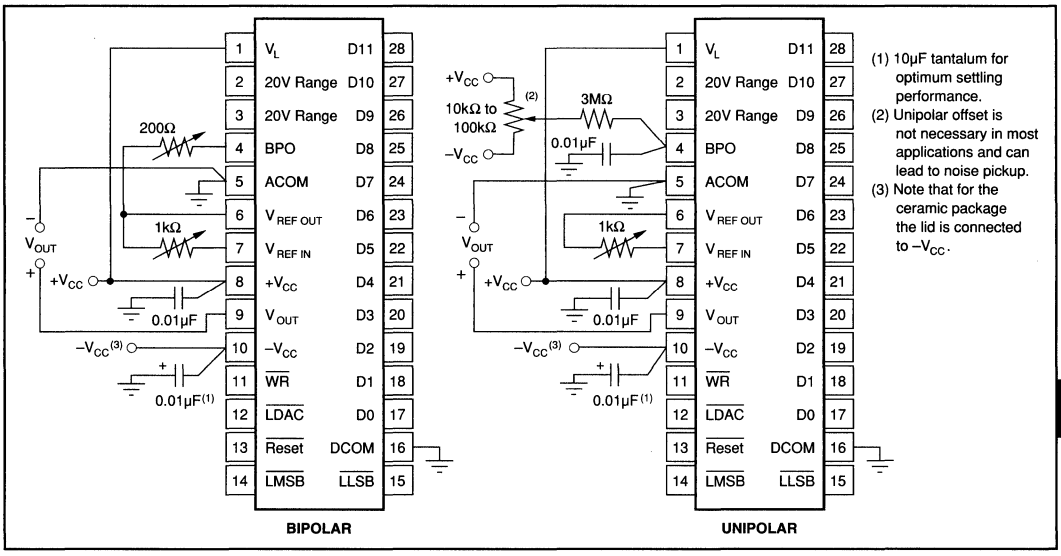


FIGURE 5. Power Supply, Gain, and Offset Connections.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 16) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from 000_{HEX} to FFF_{HEX} is only 800µA.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.

The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a 600Ω resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A 7.98kΩ resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A resistors.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{LMSB}$, $\overline{LLSB}$, and $\overline{LDAC}$ determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

8-BIT INTERFACE

The control logic of DAC813 permits interfacing to right-justified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. $X10_{HEX}$ loads the 8 LSBs and $X01_{HEX}$ loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{HEX}$ and $X11_{HEX}$ are not used.

INTERFACING MULTIPLE DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{LLSB}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{LMSB}$ and $\overline{LLSB}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by $\overline{WR}$.

Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

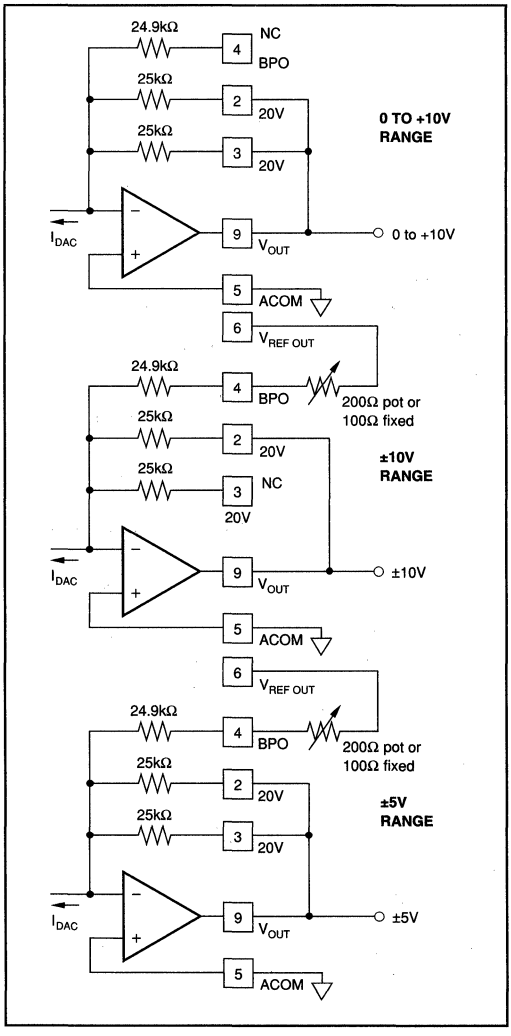


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

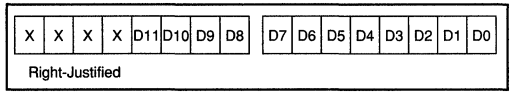


FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

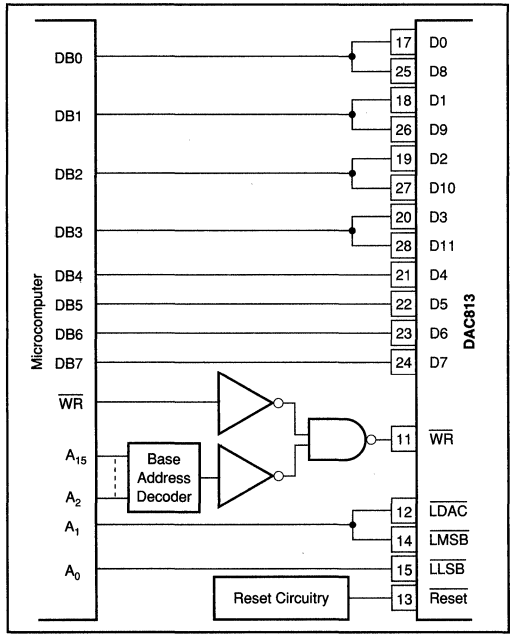
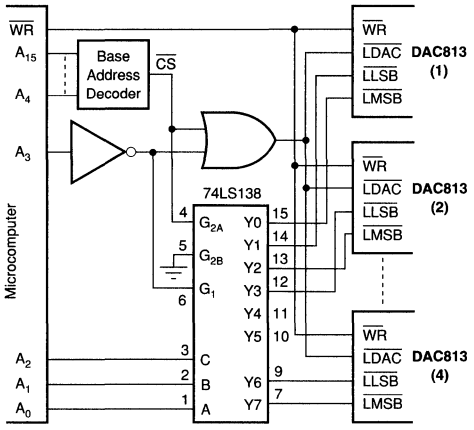


FIGURE 8. Right-Justified Data Bus Interface.



ADDRESS BUS A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 LSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 LSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 LSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.

BURR - BROWN®

DAC2813

DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

FEATURES

- COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS
- 12-BIT PORT INTERFACE
- ANALOG OUTPUT RANGE: ±10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- INTEGRAL LINEARITY ERROR: ±1/2LSB max
- ±12V to ±15V SUPPLIES
- 28-PIN PLASTIC DIP PACKAGE

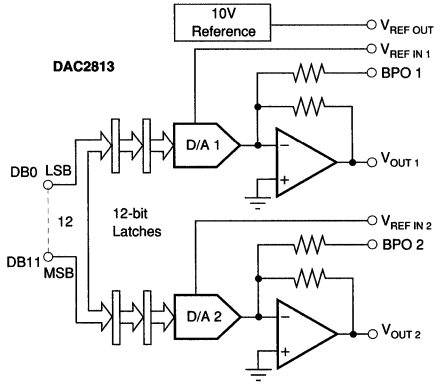
DESCRIPTION

DAC2813 is a complete dual 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC2813 output range resistors are internally connected for 20V full scale range. A 0 to 10V range can be connected using the bipolar offset resistor. Gain and bipolar offset of each D/A are adjustable with external trim potentiometers.

DAC2813 is available in one performance grade with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

PARAMETER	CONDITIONS	DAC2813AP MIN	DAC2813AP TYP	DAC2813AP MAX	UNITS
INPUTS					
DIGITAL INPUTS	Over Temperature Range		Bipolar Offset Binary		
Input Code (1)					
Logic Levels (2)					
V_{IH}		+2		+5.5(3)	V
V_{IL}		0		+0.8	V
Logic Input Currents					
DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$,$\overline{EN}_X$					
I_{IH}	V_I = +2.7V			±20	µA
I_{IL}	V_I = +0.4V			±20	µA
TRANSFER CHARACTERISTICS					
ACCURACY					
Linearity Error			±1/4	±1/2	LSB
Differential Linearity Error			±1/2	±1	LSB
Gain Error (5,6)			±0.05	±0.2	%
Bipolar Zero Error (5,7)			±0.05	±0.2	%FSR(4)
Power Supply Sensitivity					
Of Full Scale $+V_{CC}$			±5	±20	ppmFSR/%+V_{CC}
$-V_{CC}$			±1	±10	ppmFSR/%−V_{CC}
DRIFT	Over Specification Temperature Range				
Gain			±5	±30	ppm/°C
Bipolar Zero Drift			±5	±15	ppmFSR/°C
Linearity Error over Temperature			±1/2	±3/4	LSB
Monotonicity			Guaranteed		
DYNAMIC CHARACTERISTICS					
SETTLING TIME (8)	To within ±0.012%FSR of Final Value 5kΩ || 500pF Load				
Full Scale Range Change	20V Range		4.5	6	µs
1LSB Output Step (9) At Major Carry			2		µs
Slew Rate			10		V/µs
Crosstalk (10)	5kΩ Loads		0.1		LSB
OUTPUT					
Output Voltage Range	$\pm V_{CC} \geq$ ±11.4V			±10	V
Output Current		±5			mA
Output Impedance			0.2		Ω
Short Circuit to ACOM Duration			Indefinite		
REFERENCE VOLTAGE					
Voltage		+9.95	+10.00	+10.05	V
Source Current Available for External Loads		2			mA
Impedance			0.2		Ω
Temperature Coefficient			±5	±25	ppm/°C
Short Circuit to Common Duration			Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage:$+V_{CC}$		+11.4	+15	+16.5	V
$-V_{CC}$		−11.4	−15	−16.5	V
Current:	No Load $\pm V_{CC}$ = ±15V				
$+V_{CC}$			24	30	mA
$-V_{CC}$			12	14	mA
Power Dissipation			540	660	mW
Potential at DCOM with Respect to ACOM (11)		−3		+3	V
TEMPERATURE RANGES					
Specification		−40		+85	°C
Storage		−60		+100	°C
Thermal Resistance, θ_{JA},Plastic DIP			30		°C/W

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Adjustable to zero with external trim potentiometer. (6) Specified with 500Ω connected between $V_{REF\ OUT}$ and $V_{REF\ IN}$. (7) Error at input code 800_{HEX}. DAC2813 specified with 100Ω connected between$V_{REF\ OUT}$ and $V_{REF\ IN}$; and with 500Ω connected between $V_{REF\ OUT}$ and BPO. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) For the worst-case code change: $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (10) Crosstalk is defined as the change in any output as a result of any other output being driven from −10V to +10V at rated output current. (11) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
ACOM to DCOM	±4V
Digital Inputs to DCOM	−1V to $+V_{CC}$
External Voltage applied to BPO Resistor	±18V
$V_{REF\ OUT}$	Indefinite short to ACOM
V_{OUT}	Momentary to ±18V
Lead Temperature, soldering 10s	+300°C
Max Junction Temperature	165°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

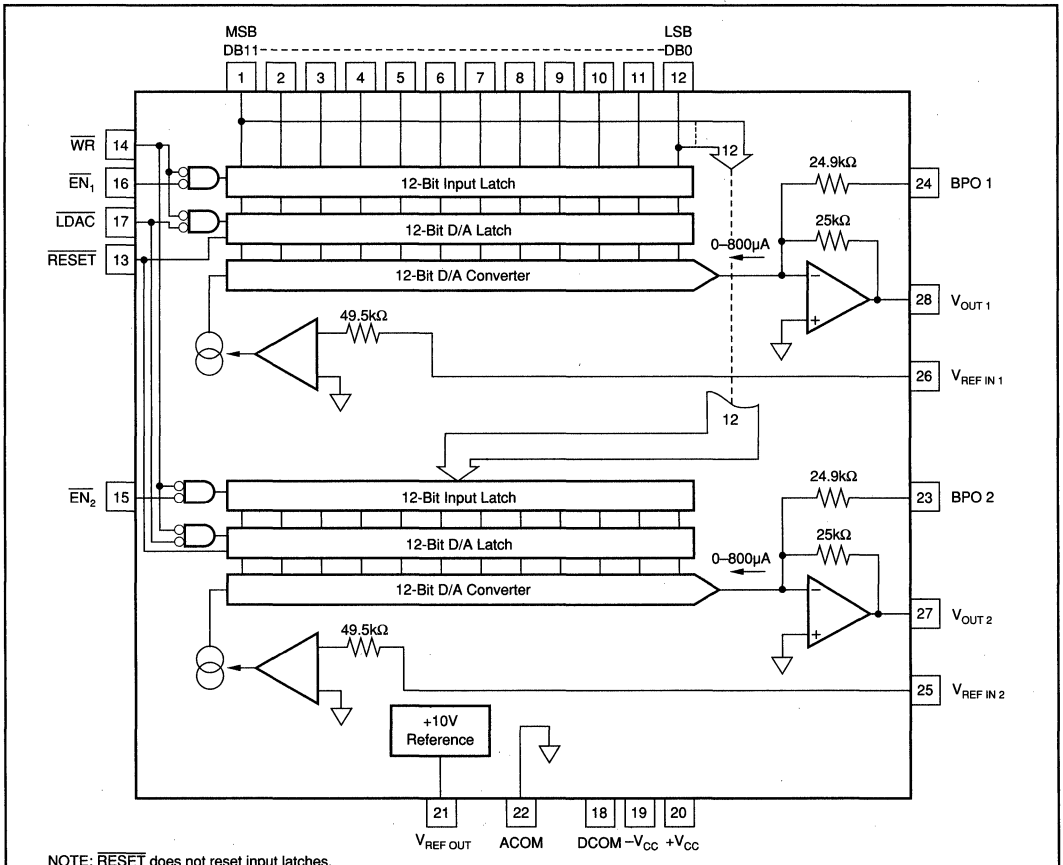
MODEL	PACKAGE	TEMPERATURE RANGE
DAC2813AP	28-Pin DBL Wide DIP	−40°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC2813AP	28-Pin DBL Wide DIP	167

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BLOCK DIAGRAM

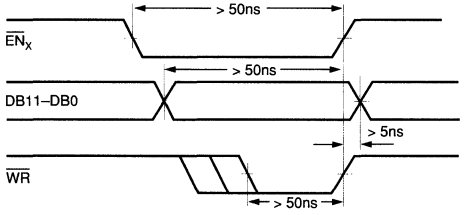


NOTE: $\overline{RESET}$ does not reset input latches.

TIMING DIAGRAMS

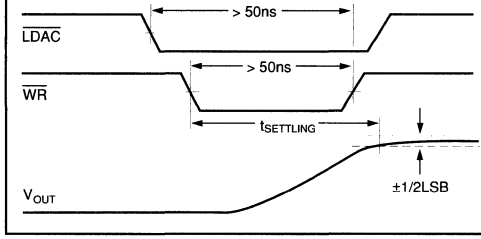
WRITE CYCLE #1

(Load first rank from Data Bus: $\overline{LDAC}$ = 1)



WRITE CYCLE #2

(Load second rank from first rank: $\overline{EN_X}$ = 1)



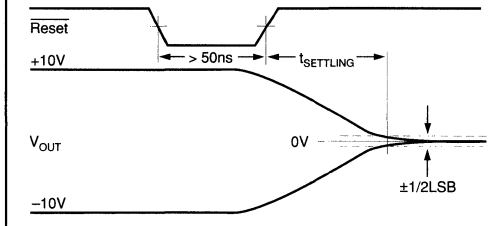
TRUTH TABLE

$\overline{WR}$	$\overline{EN1}$	$\overline{EN2}$	$\overline{LDAC}$	$\overline{RESET}$	OPERATION
X	X	X	X	0	Reset both D/A Latches. Does not reset input latches.
1	X	X	X	1	No Operation
X	1	1	1	1	No Operation
0	1	0	1	1	Load Data into First Rank for D/A 2
0	0	1	1	1	Load Data into First Rank for D/A 1
0	1	1	0	1	Load Second Rank from First Rank, both D/As
0	0	0	0	1	All Latches Transparent

"X" = Don't Care

RESET COMMAND (Bipolar Mode)

$\overline{EN_X}$, $\overline{LDAC}$, $\overline{WR}$ = Don't Care



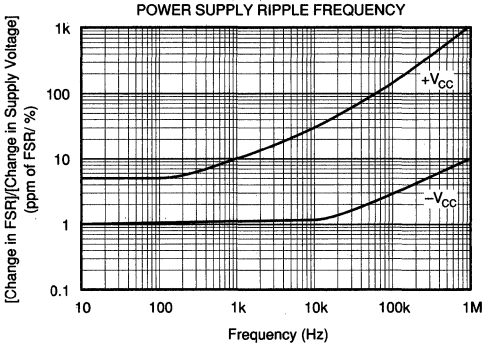
PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	DB11	DATA, MSB, positive true.
2	DB10	DATA
3	DB9	DATA
4	DB8	DATA
5	DB7	DATA
6	DB6	DATA
7	DB5	DATA
8	DB4	DATA
9	DB3	DATA
10	DB2	DATA
11	DB1	DATA
12	DB0	DATA, LSB.
13	$\overline{RESET}$	Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten an $\overline{LDAC}$-$\overline{WR}$ command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state.
14	$\overline{WR}$	Write strobe. Must be low for data transfer to any latch (except RESET).
15	$\overline{EN2}$	Enable for 12-bit input data latch of D/A 2. NOTE: This logic path is slower than the WR\ path.
16	$\overline{EN1}$	Enable for 12-bit input data latch of D/A 1. NOTE: This logic path is slower than the WR\ path.
17	$\overline{LDAC}$	Load DAC enable. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of both D/A converters.
18	DCOM	Digital common, logic currents return.
19	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
20	$+V_{CC}$	Analog supply input, nominally +12V or +15V referred to ACOM.
21	$V_{REF\ OUT}$	+10V reference output.
22	ACOM	Analog common, $+V_{CC}$, $-V_{CC}$ supply return.
23	BPO2	Bipolar offset. Connect to pin 21 ($V_{REF\ OUT}$) through a 100Ω resistor or through a 200 potentiometer for Bipolar Offset Adjust for D/A 2.
24	BPO1	Bipolar offset. Connect to pin 21 ($V_{REF\ OUT}$) through a 100Ω resistor or through a 200 potentiometer for Bipolar Offset Adjust or D/A 1.
25	$V_{REF\ IN\ 2}$	Connect to $V_{REF\ OUT}$ through 500Ω fixed resistor or through a 1kΩ gain adjustment potentiometer for D/A 2.
26	$V_{REF\ IN\ 1}$	Connect to $V_{REF\ OUT}$ through 500Ω fixed resistor or through a 1kΩ gain adjustment potentiometer for D/A 1.
27	$V_{OUT\ 2}$	D/A 2 analog output.
28	$V_{OUT\ 1}$	D/A 1 analog output.

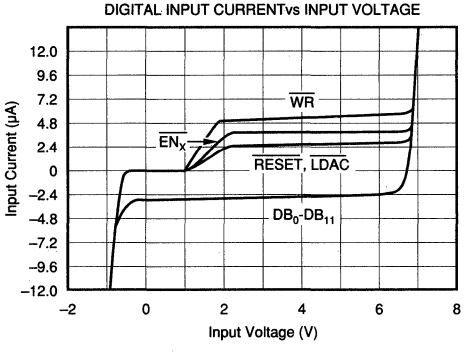
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

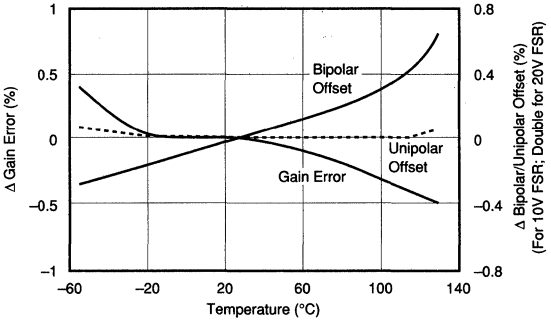
POWER SUPPLY REJECTION vs POWER SUPPLY RIPPLE FREQUENCY



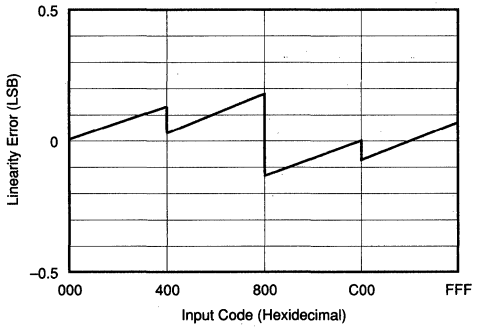
DIGITAL INPUT CURRENTvs INPUT VOLTAGE



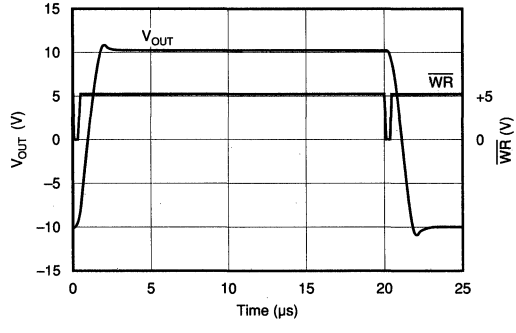
CHANGE OF GAIN AND OFFSET ERROR vs TEMPERATURE



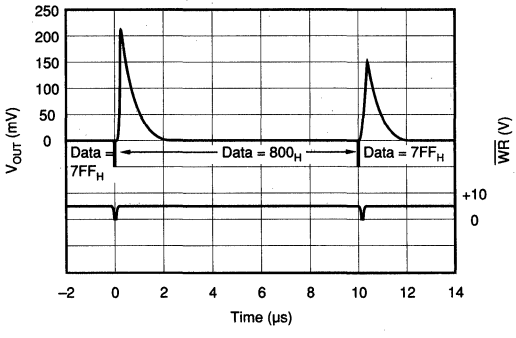
INTEGRAL LINEARITY ERROR



± FULL SCALE OUTPUT SWING

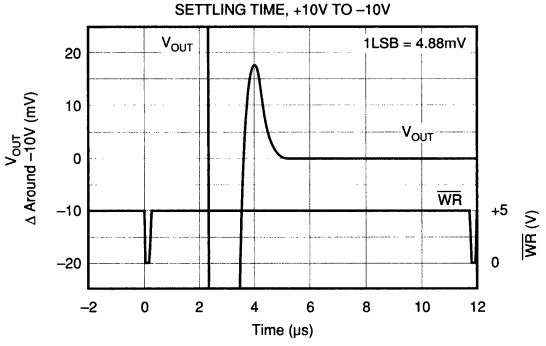


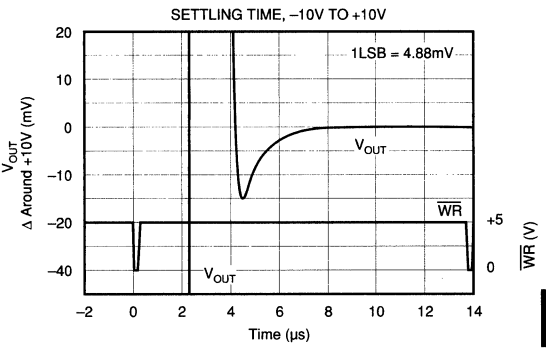
MAJOR CARRY GLITCH



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all "1s" and all "0s"). DAC2813 linearity error is ±1/2LSB max at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. DAC2813 is monotonic over their specification temperature range –40°C to +85°C.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Settling times are specified to ±0.01% of Full Scale Range (FSR) for two conditions: one for a FSR output change of 20V (25kΩ feedback) and one for a 1LSB change. The 1LSB change is measured at the Major Carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input code transition at which worst-case settling time occurs.

OPERATION

INTERFACE LOGIC

The bus interface logic of the DAC2813 consists of two independently addressable latches in two ranks for each D/A converter. The first rank consists of one 12-bit input latch which can be loaded directly from a 12- or 16-bit microprocessor/microcontroller bus. The input latch holds data temporarily before it is loaded into the second latch, the D/A latch. This double buffered organization permits simultaneous update of all D/As.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When the control signals return to logic "1", the data is latched.

CAUTION: DAC2813 was designed to use $\overline{WR}$ as the fast strobe. WR/ has a much faster logic path than $\overline{EN_X}$ (or LDAC). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN_X}$ to strobe data into the latches, the DATA

HOLD time will be long, approximately 20ns to 30ns and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

RESET FUNCTION

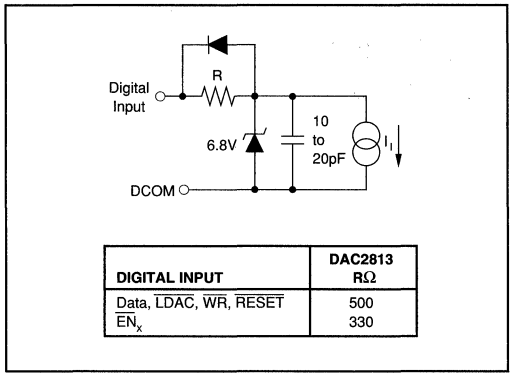
The Reset function resets only the D/A latch. Therefore, after a RESET, good data must be written to **all** the input latches before an $\overline{LDAC}$ – $\overline{WR}$ command is issued. Otherwise, old data or unknown data is present in the input latches and will be transferred to the D/A latch producing an analog output value that may be unwanted.

LOGIC INPUT COMPATIBILITY

DAC2813 digital inputs are TTL compatible (1.4V switching level) over the operating range of $+V_{CC}$. Each input has low leakage and high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC2813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition, the speed of the interface will be slower. A digital output driving a DATA input line of the DAC2813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

Unused CONTROL inputs should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available, the control inputs can be connected to $+V_{CC}$ through a 100kΩ resistor to limit the input current.



DIGITAL INPUT	DAC2813 RΩ
Data, $\overline{LDAC}$, $\overline{WR}$, $\overline{RESET}$	500
$\overline{EN_x}$	330

FIGURE 1. Equivalent Digital Input Circuit.

INPUT CODING

DAC2813 accepts positive-true binary input codes. Input coding for bipolar analog outputs is Bipolar Offset Binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

DAC2813 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

DAC2813 can be connected for 0 to +10V unipolar operation by using the BPO resistors, plus a 100Ω series resistor, in parallel with the internal feedback resistor. In this case, an input code of 000_{HEX} gives zero volt output, an input of FFF_{HEX} gives an output 1LSB below positive full scale.

INTERNAL/EXTERNAL REFERENCE USE

DAC2813 contains a +10V ±50mV voltage reference, $V_{REF\ OUT}$. $V_{REF\ OUT}$ is available to drive external loads sourcing up to 2mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the D/A converters will vary.

For DAC2813 $V_{REF\ OUT}$ must be connected to $V_{REF\ IN\ 1}$ and $V_{REF\ IN\ 2}$ through gain adjust resistors with a nominal value of 500Ω. Trim potentiometers with a nominal value of 1000Ω can be used to provide adjustment to zero gain error.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. However, DAC2813 is optimized for fixed-reference applications. If the reference voltage is expected to time-vary over a wide range, a CMOS multiplying D/A is a better choice.

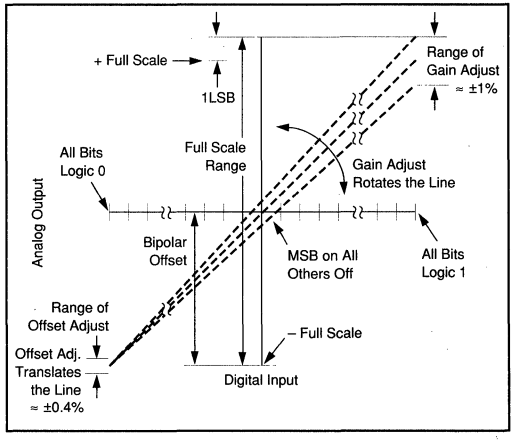


FIGURE 2. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT	
	UNIPOLAR 0 TO +10V	BIPOLAR ±10V
FFF_{HEX}	+9.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V
$7FF_{HEX}$	+4.9976V	–0.0049V
000_{HEX}	0.0000V	–10.0000V
1LSB	2.44mV	4.88mV

TABLE III. Analog Output Calibration Values.

GAIN AND OFFSET ADJUSTMENTS

Figure 2 illustrates the relationship of offset and gain adjustments to a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments.

Offset Adjustment

For bipolar analog output operation, apply digital input code 000_{HEX} to produce the maximum negative output and adjust the offset potentiometer for –10.000V. See Table III for calibration values and codes.

Gain Adjustment

For either unipolar or bipolar operation, apply digital input code FFF_{HEX} gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for calibration values.

INSTALLATION

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best settling time performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

DAC2813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both DIGITAL COMMON (DCOM) and ANALOG COMMON (ACOM) be connected directly to a ground plane under the package. If a ground place is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. The change in current in the ACOM pin due to an input date word change from 000_{HEX} to FFF_{HEX} is only 1mA for each D/A converter.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

DAC2813 output amplifiers provide a ±10V output swing while operating on supplies as low as ±12V ±5%.

DAC2813 is internally connected to provide ±10V output when the bipolar offset pins BPO1 and/or BPO2 are connected, through 100Ω resistors, to $V_{REF\ OUT}$. For a unipolar 0 to +10V output, the BPO resisitor, in series with a 100Ω external resistor, may be paralleled with the internal feedback resistor to provide the correct scaling. The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of ±2%.

12- AND 16-BIT BUS INTERFACES

DAC2813 data is latched into the input latches of each D/A by asserting low each ENx individually and transferring the data from the bus to each input latch by asserting WR low. All D/A outputs in each package are then updated simultaneously by asserting LDAC and WR low. Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

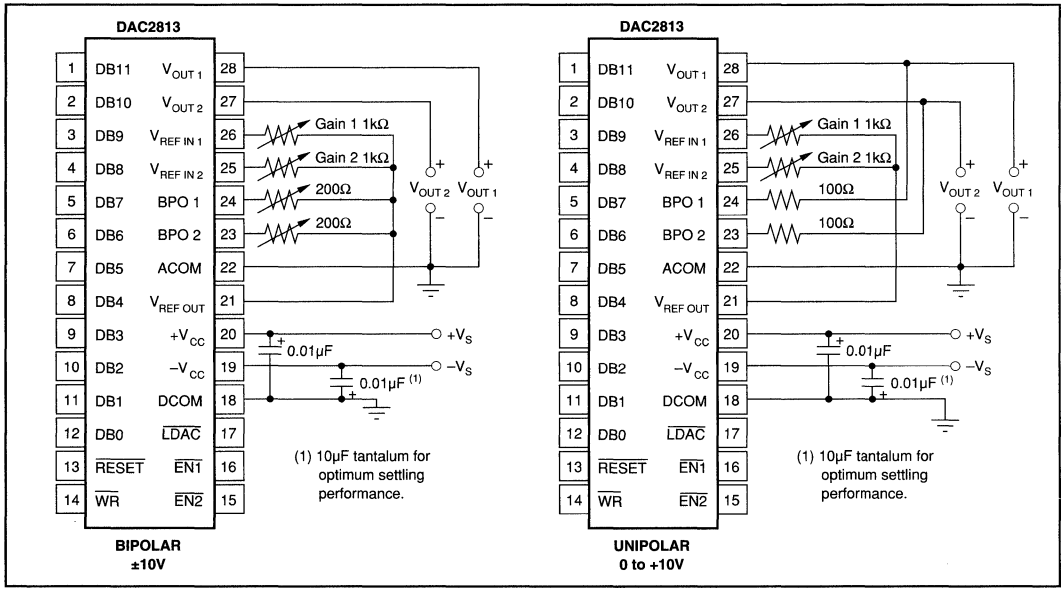


FIGURE 3. DAC2813 Power Supply, Output Range, Gain and Offset Adjust Connections. Unipolar output connected DAC2813s have Gain Adjust only.

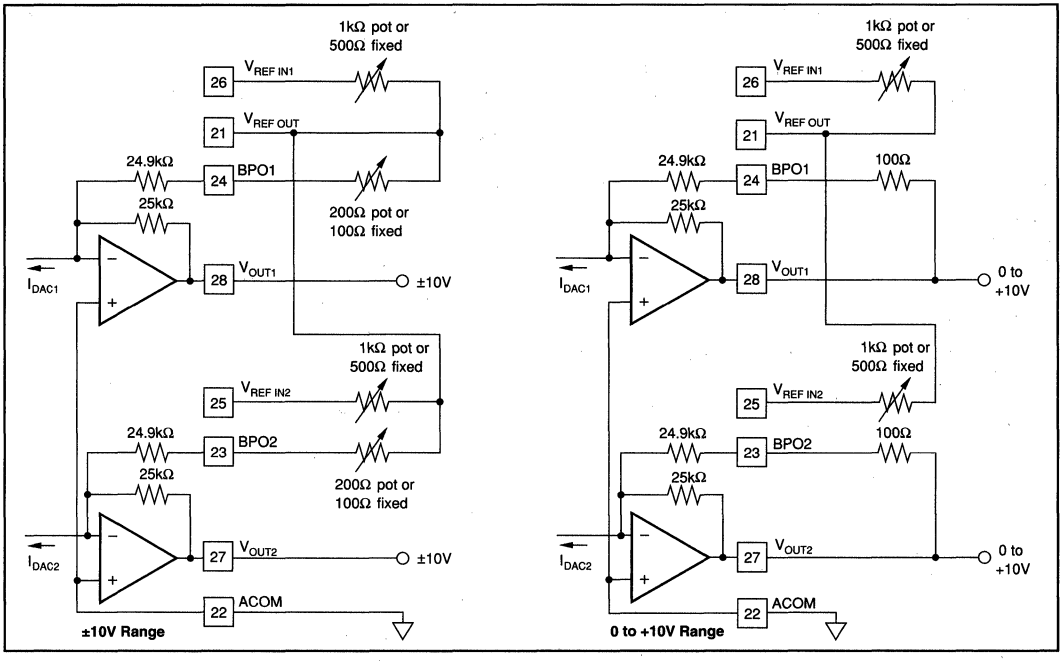


FIGURE 4. DAC2813 Output Amplifier Range Connnections.

BURR-BROWN®

DAC2814

DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (Serial Interface)

FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER: 300mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

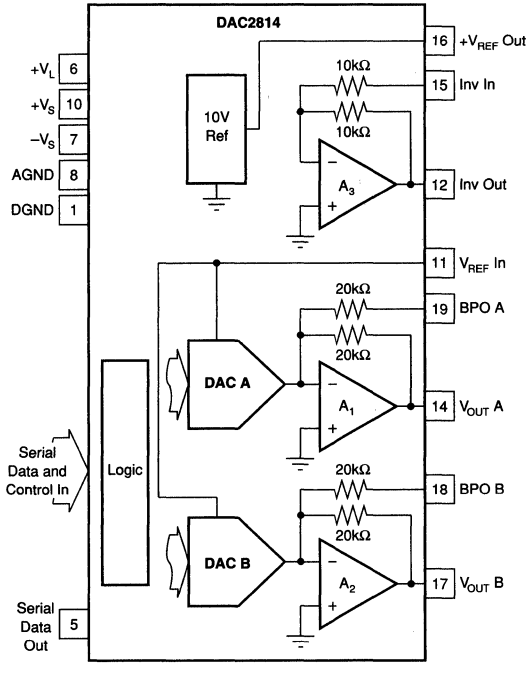
DESCRIPTION

The DAC2814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC2814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC B MSB first into a 24-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2814 is packaged in a 24-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2814AP MIN	DAC2814AP TYP	DAC2814AP MAX	DAC2814BP MIN	DAC2814BP TYP	DAC2814BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		+2		+5	*		*	V
V_{IL} (Input Low Voltage)		0		+0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
DIGITAL OUTPUT								
Data Out V_{OL}	I_{SINK} = 1.6mA	0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5	*		*	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C TO +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V V_L = +4.5V to +5.5V			30			*	ppmFSR/V
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+6.5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT (Code Dependent)			±2			*		mA
DIGITAL CROSSTALK	Full Scale Transition C_L= 100pF		3			*		nV-s
D/A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2814AP			DAC2814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+10	+13.5		*	*	mA
$-I_S$			–10	–13.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.2	1		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			5			*	mA
Total Power, All DACs			300	410		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC2814AP	24-Pin Plastic DIP	167
DAC2814BP	24-Pin Plastic DIP	167

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

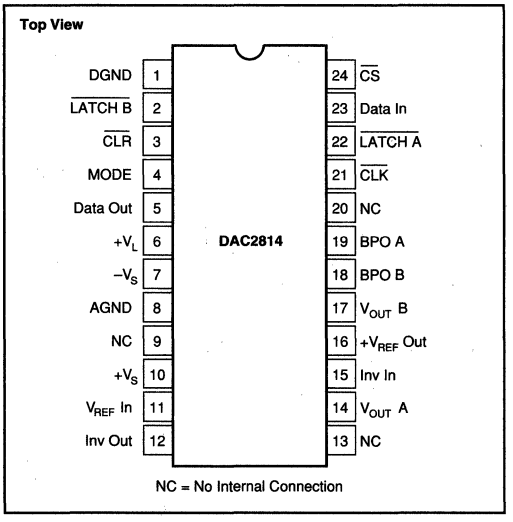
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN DESIGNATIONS

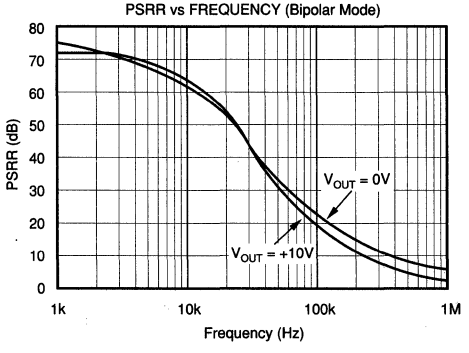
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	DGND	Digital common	24	$\overline{CS}$	Chip select enable, DAC A and DAC B
2	$\overline{LATCH\ B}$	Latch data update, logic input, DAC B	23	Data In	Serial data input
3	$\overline{CLR}$	Asychronous input reset to zero	22	$\overline{LATCH\ A}$	Latch data update, logic input, DAC A
4	MODE	Selection input for unipolar or bipolar reset to zero	21	$\overline{CLK}$	Clock input
5	Data Out	Serial data output	20	NC	No internal connection
6	$+V_L$	Positive logic power supply, +5V input	19	BPO A	Bipolar offset input, DAC A
7	$-V_S$	Negative analog power supply , –15V input	18	BPO B	Bipolar offset input, DAC B
8	AGND	Analog common	17	V_{OUT} B	Analog output voltage, DAC B
9	NC	No internal connection	16	$+V_{REF}$ Out	Reference voltage, +10V output
10	$+V_S$	Positive analog power supply, +15V input	15	Inv In	Inverter (A3) input
11	V_{REF} In	± Reference voltage input	14	V_{OUT} A	Analog output voltage, DAC A
12	Inv Out	Inverter (A3) output	13	NC	No internal connection

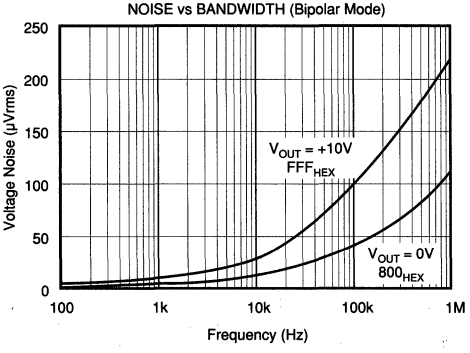
PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

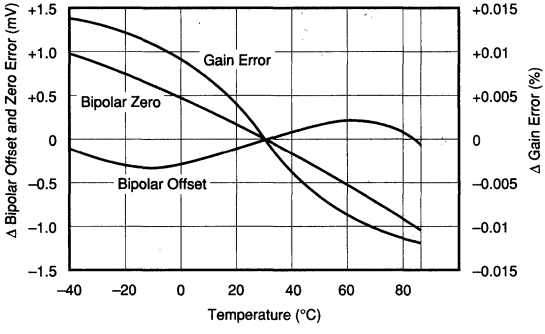




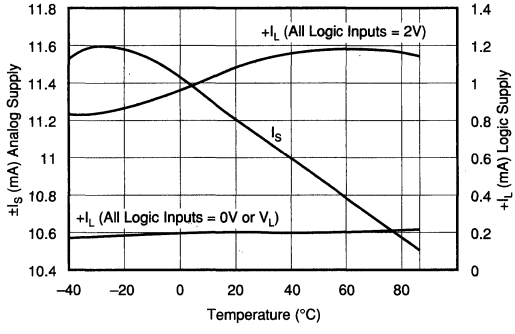
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

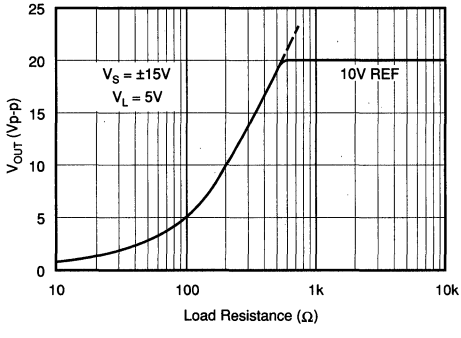
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



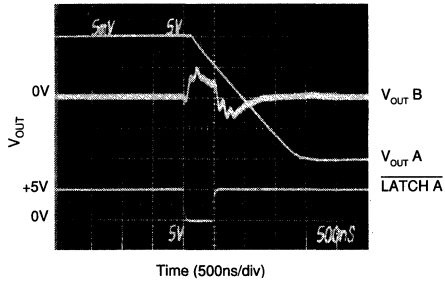
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



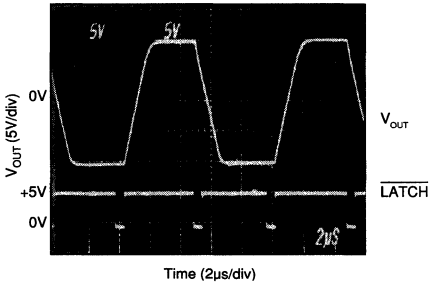
CROSSTALK (Bipolar Mode)



Time (500ns/div)

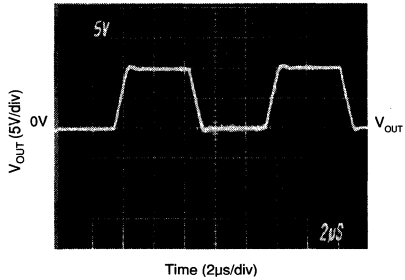
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{\text{LATCH}}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

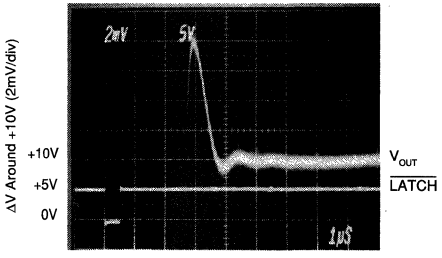


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

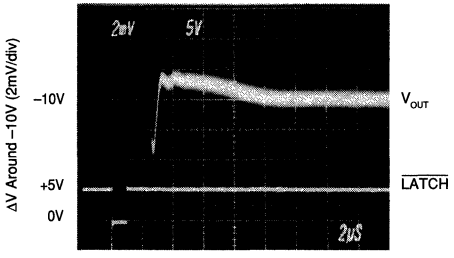
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



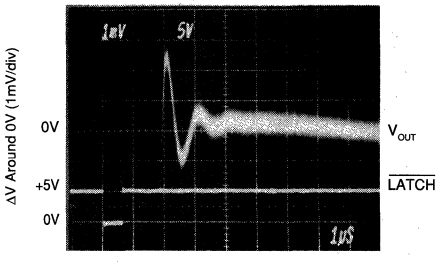
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



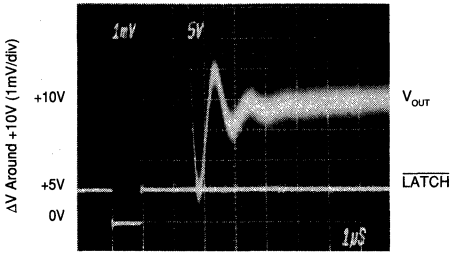
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



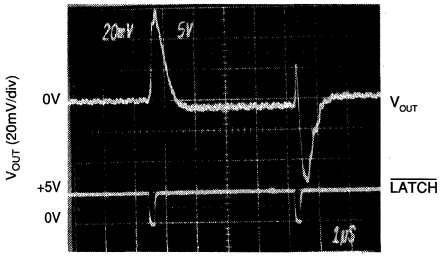
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



Time (1µs/div)

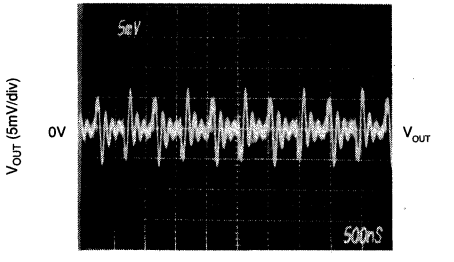
MAJOR CARRY GLITCH



Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



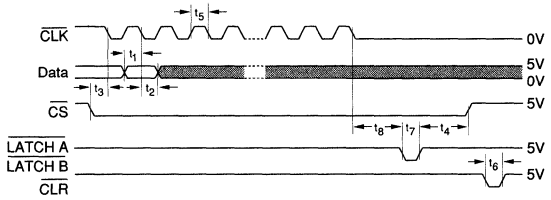
Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

V_L = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$ or $\overline{LATCH\ B}$	15ns



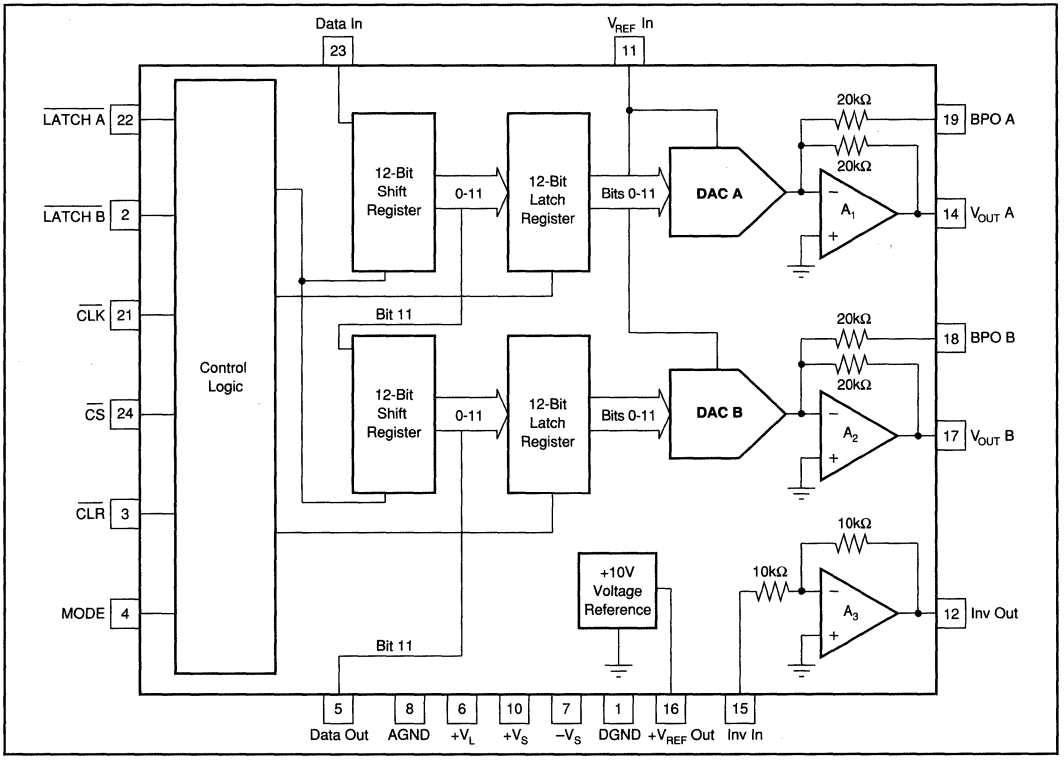
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V • $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	FUNCTION
X	1	↓	0	X	X	Data Clocked In
X	1	X	1	X	X	No Data Transfer
X	1	X	0	0	1	DAC A Register Updated
X	1	X	0	1	0	DAC B Register Updated
X	1	X	0	0	0	DAC A and DAC B Updated Together
0	0	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	Shift Registers Cleared = 000_{HEX}, DAC Registers = 800_{HEX}

NOTE: X = Don't care ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM , DAC2814 — Dual, 12-bit DAC, Serial Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2814 are TTL and 5V CMOS compatible. Input codes for the DAC2814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 24-bit shift register. DAC B MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. Both $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream.

By using separate signals for $\overline{\text{LATCH A}}$ and $\overline{\text{LATCH B}}$, it is possible to update either one of the two DACs every 12 clock cycles.

When $\overline{\text{CLR}}$ is brought low, the input shift registers are cleared to 000_{HEX}, while the DAC registers = 800_{HEX}. If $\overline{\text{LATCH}}$ is brought low after $\overline{\text{CLR}}$, the DACs are updated with 000_{HEX} resulting in –10V (Bipolar) or 0V (Unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

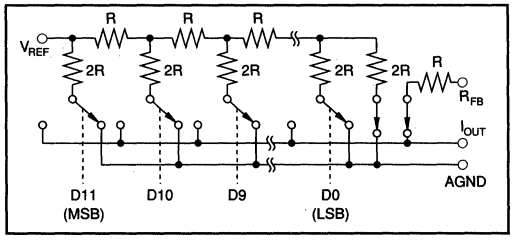


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

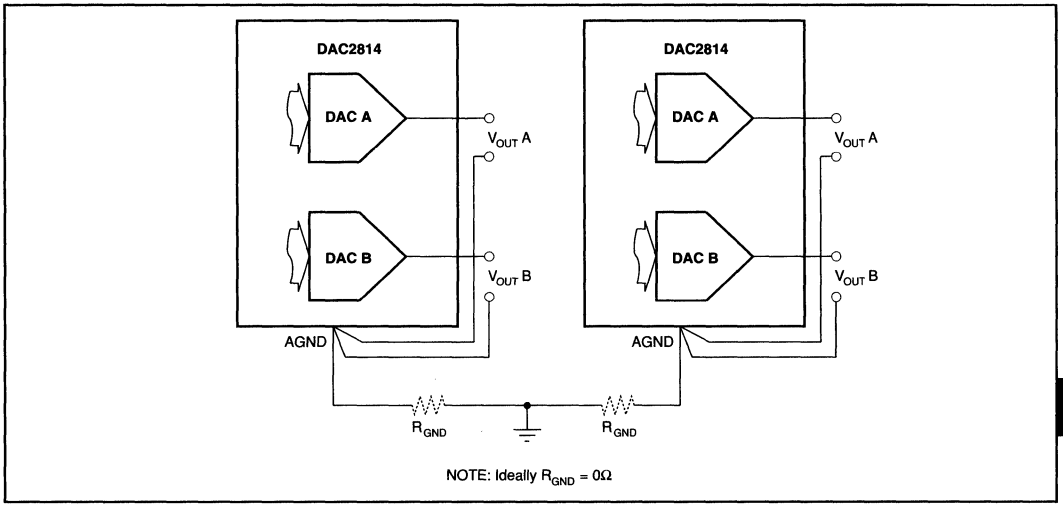


FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2814 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC2814s can be connected to the same $\overline{CLK}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC2814s can be cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 24N $\overline{CLK}$ cycles may be required to update any given DAC, where N = number of DAC2814s.

Parallel Bus Connection

Several DAC2814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 24 $\overline{CLK}$ cycles.

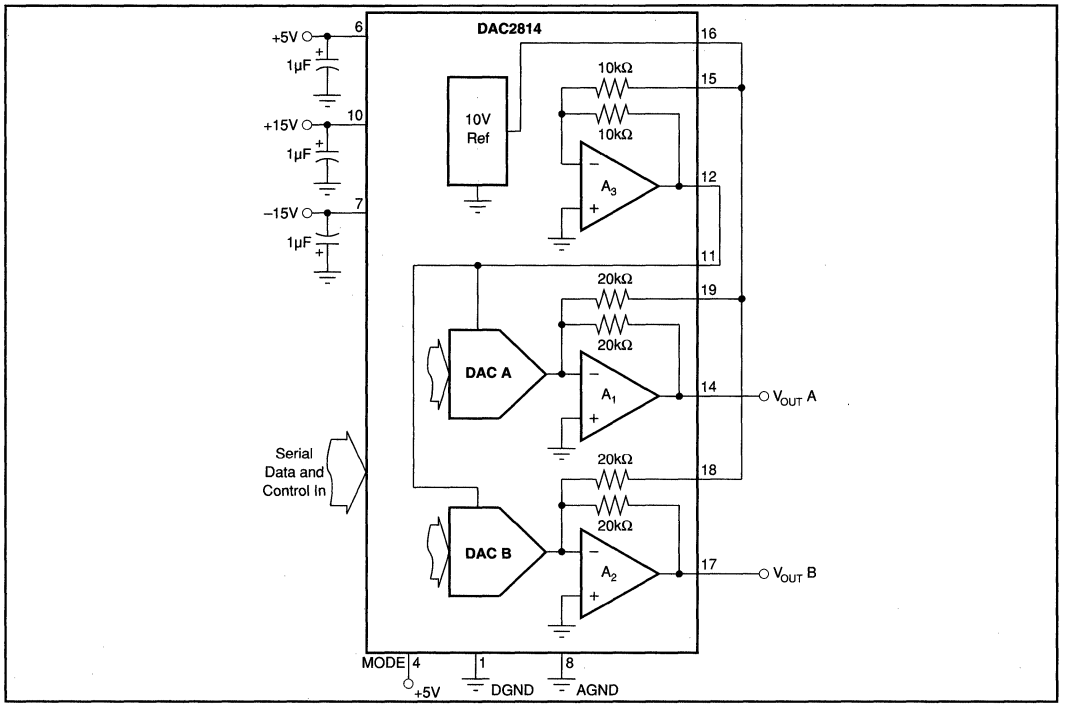


FIGURE 3. Analog Connections for ±10V DAC Output.

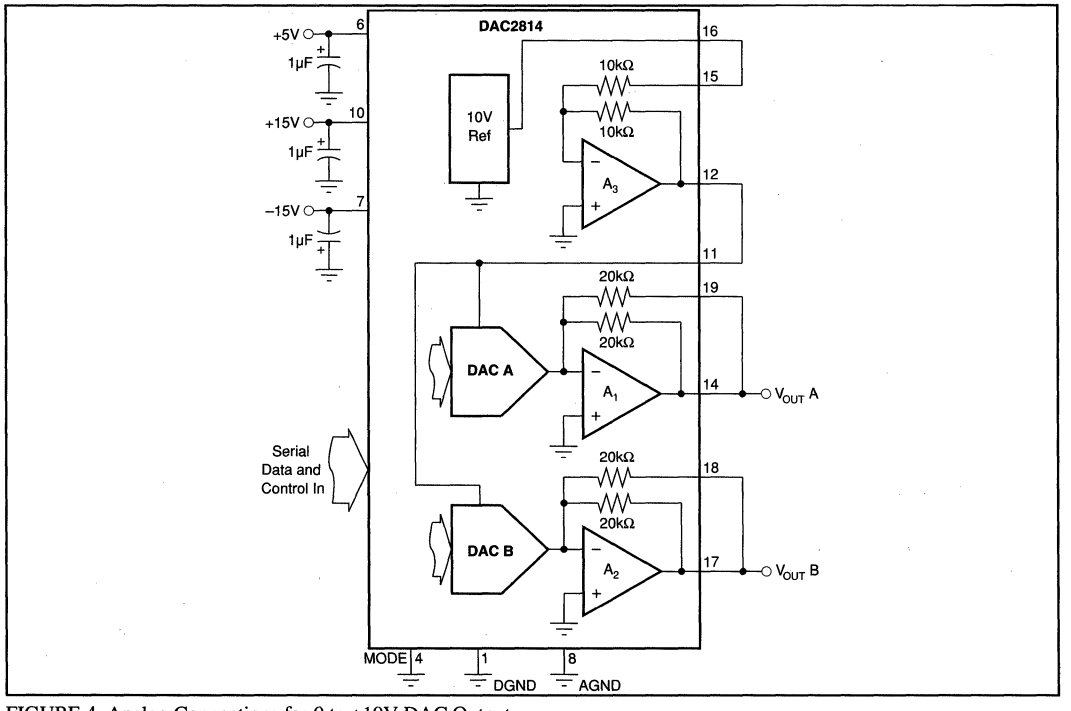


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

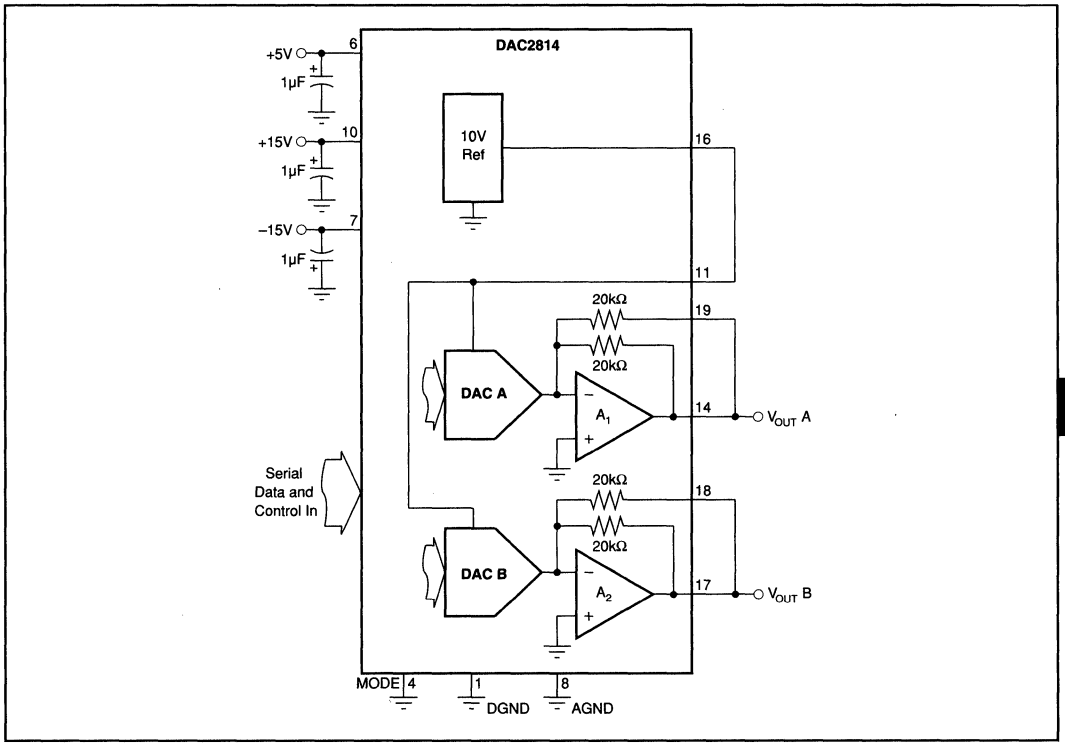


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

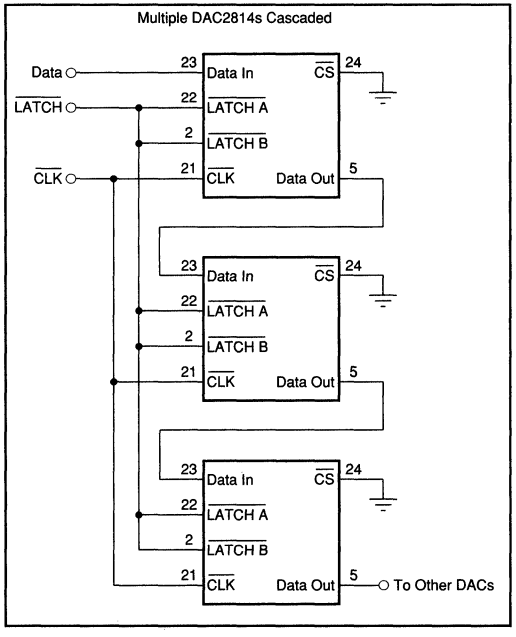


FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC packages.

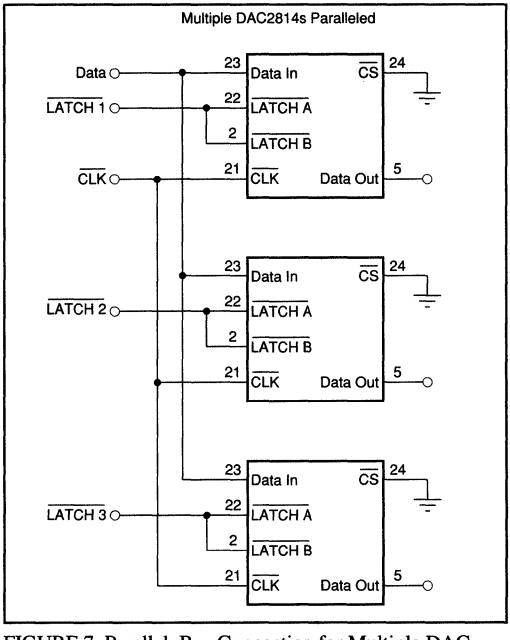


FIGURE 7. Parallel Bus Connection for Multiple DAC packages.

BURR - BROWN®

DAC2815

DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (8-Bit Port Interface)

FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER: 300mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

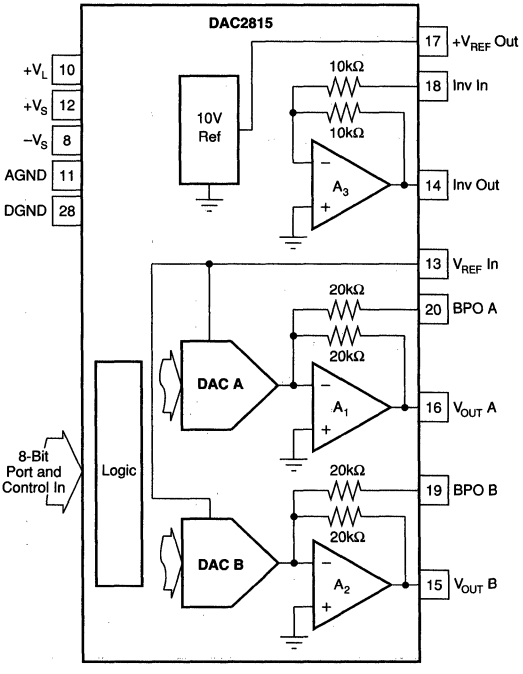
DESCRIPTION

The DAC2815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC2815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP MIN	DAC2815AP TYP	DAC2815AP MAX	DAC2815BP MIN	DAC2815BP TYP	DAC2815BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		2		5	*		*	V
V_{IL} (Input Low Voltage)		0		0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C TO +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V, V_L = +4.5V to +5.5V			30			*	ppmFSR/V
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+6.5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation (ΔV_{OUT} vs ΔI_{LOAD})				40			*	ppm/mA
Supply Regulation (ΔV_{OUT} vs ΔV_S)				±5			*	ppm/V
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT (Code Dependent)			±2			*		mA
DIGITAL CROSSTALK	Full Scale Transition C_L= 100pF		3			*		nV-s
D/A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP			DAC2815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+10	+13.5		*	*	mA
$-I_S$			–10	–13.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.2	1		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			5			*	mA
Total Power, All DACs			300	410		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC2815AP	28-Pin Plastic DIP	215
DAC2815BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V,–18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

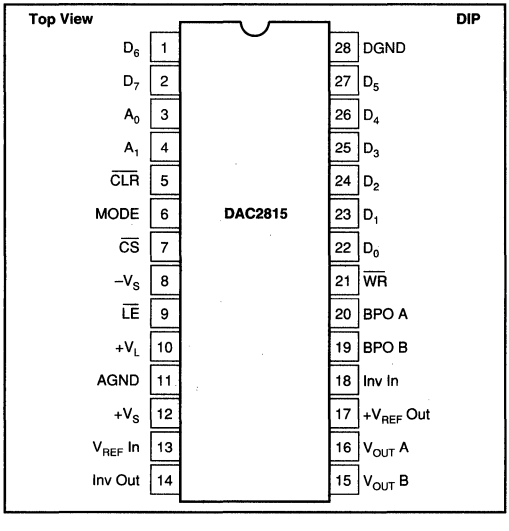
ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC2815AP	±1
DAC2815BP	±1/2

PIN DESIGNATIONS

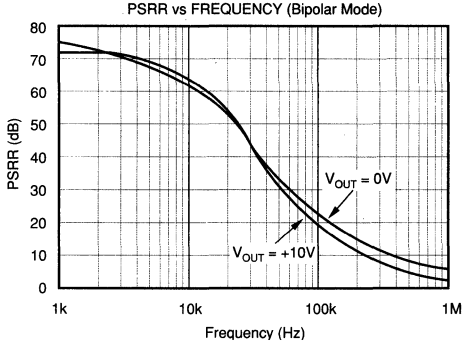
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	D_6	Data bit 6 input	28	DGND	Digital common
2	D_7	Data bit 7 input	27	D_5	Data bit 5 input
3	A_0	Address 0 input	26	D_4	Data bit 4 input
4	A_1	Address 1 input	25	D_3	Data bit 3 input
5	$\overline{CLR}$	Asychronous input reset to zero	24	D_2	Data bit 2 input
6	MODE	Selection input for unipolar or bipolar reset to zero	23	D_1	Data bit 1 input
7	$\overline{CS}$	Chip select enable, DAC A and DAC B	22	D_0	Data bit 0 input
8	$-V_S$	Negative analog power supply, –15V input	21	$\overline{WR}$	Write input, DAC A and DAC B
9	$\overline{LE}$	Latch data enable, DAC A and DAC B	20	BPO A	Bipolar offset input, DAC A
10	$+V_L$	Positive logic power supply, +5V input	19	BPO B	Bipolar offset input, DAC B
11	AGND	Analog common	18	Inv In	Inverter (A3) input
12	$+V_S$	Positive analog power supply, +15V input	17	$+V_{REF}$ Out	Reference voltage, +10V output
13	V_{REF} In	± Reference voltage input	16	V_{OUT} A	Analog output voltage, DAC A
14	Inv Out	Inverter (A_3) output	15	V_{OUT} B	Analog output voltage, DAC B

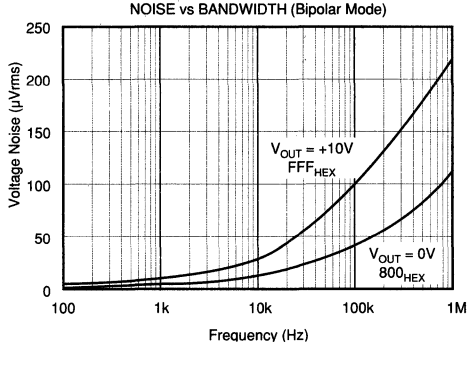
PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

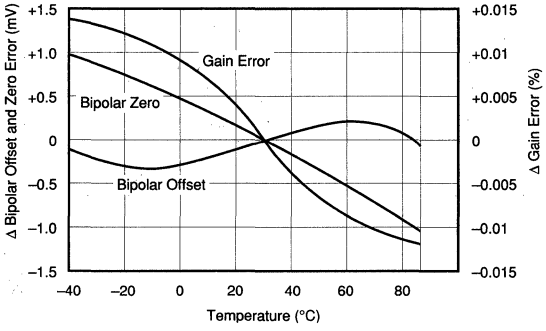




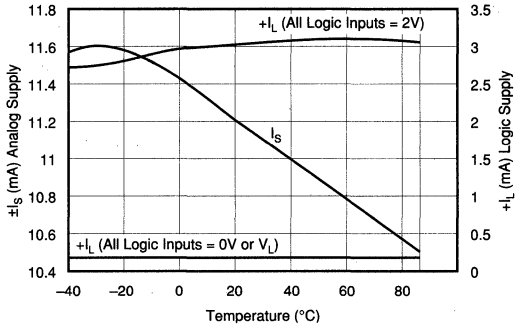
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

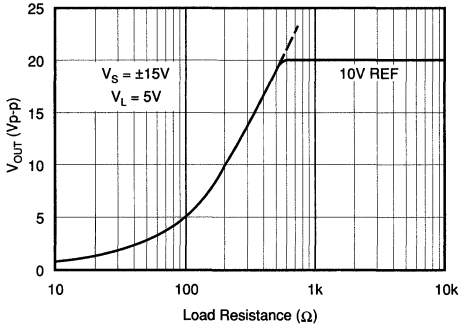
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



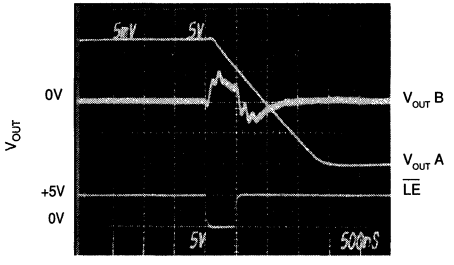
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



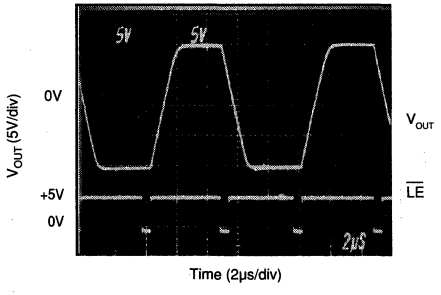
CROSSTALK (Bipolar Mode)



Time (500ns/div)

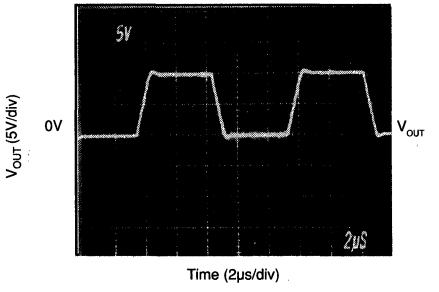
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{LE}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

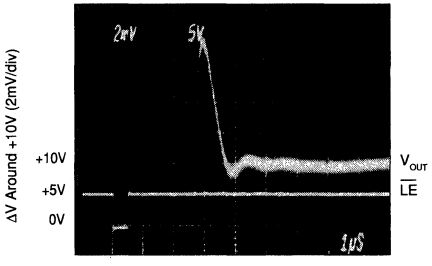


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

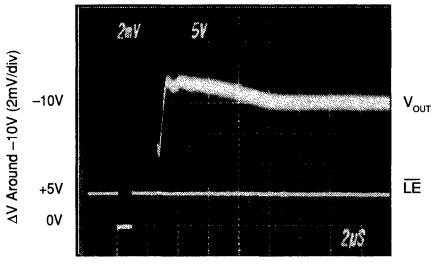
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



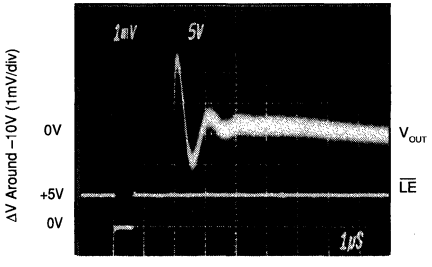
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



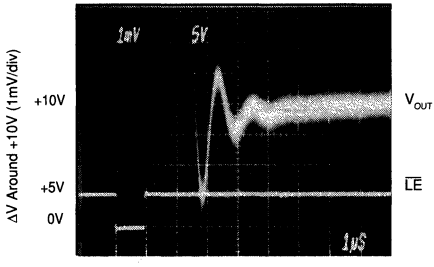
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



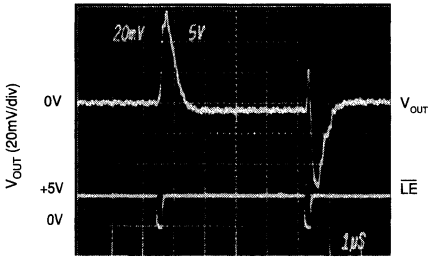
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



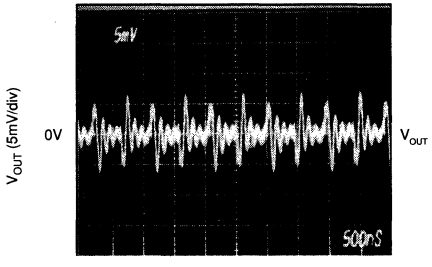
Time (1µs/div)

MAJOR CARRY GLITCH



Time (1µs/div)
NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH

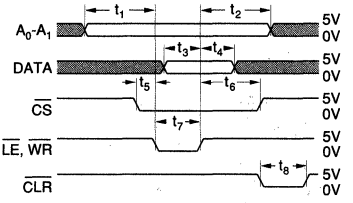


Time (500ns/div)
DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

$+V_L$ = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	10ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns



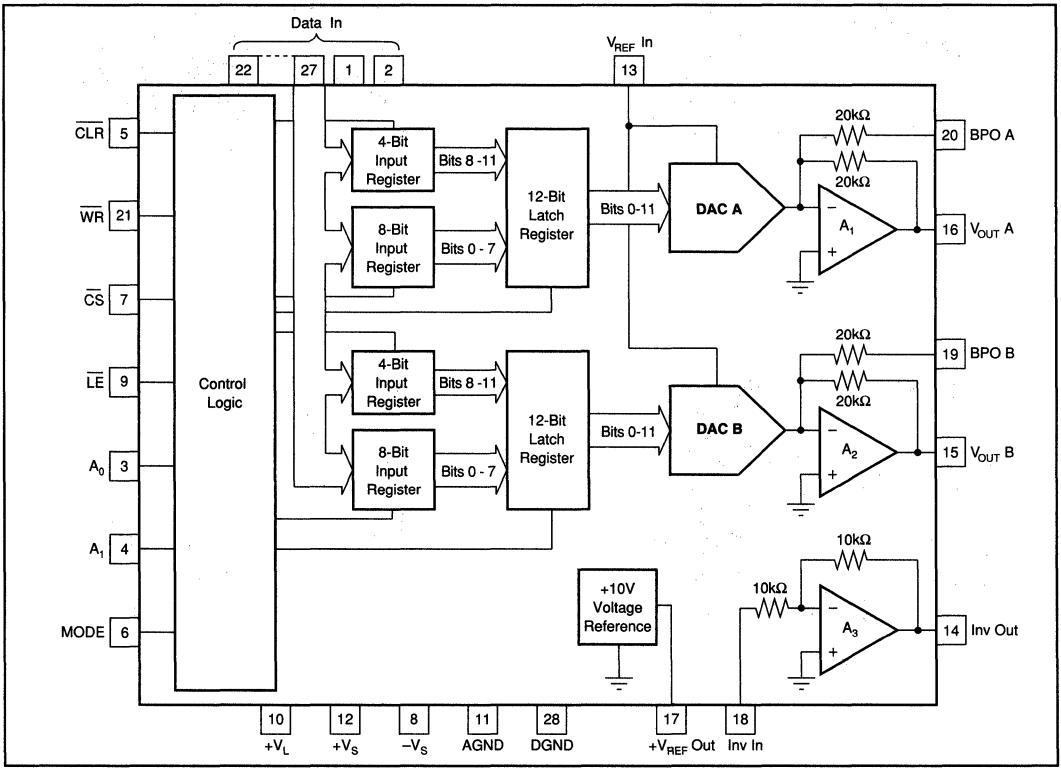
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_1	A_0	FUNCTION
X	1	1	0	0	0	0	DAC A LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	0	1	DAC A MS Input Register Loaded with D3-(MSB)-D0
X	1	1	0	0	1	0	DAC B LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	1	1	DAC B MS Input Register Loaded with D3-(MSB)-D0
X	1	0	0	1	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
X	1	0	0	0	X	X	DAC A, DAC B Registers are Transparent
X	1	X	1	X	X	X	No Data Transfer
X	1	1	X	1	X	X	No Data Transfer
0	0	X	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	X	Input Registers Cleared = 000_{HEX}, DAC Registers = 800_{HEX}

NOTE: X = Don't care.

FUNCTIONAL BLOCK DIAGRAM, DAC2815 — Dual 12-bit DAC, 8-bit Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2815 are TTL and 5V CMOS compatible. Input codes for the DAC2815 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in the unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. This data is latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bring $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. Both DACs are updated simultaneously.

When $\overline{CLR}$ is brought low, the input registers are cleared to 000_{HEX} (–10V), while the DAC registers = 800_{HEX}. If $\overline{LE}$ is brought low, the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of

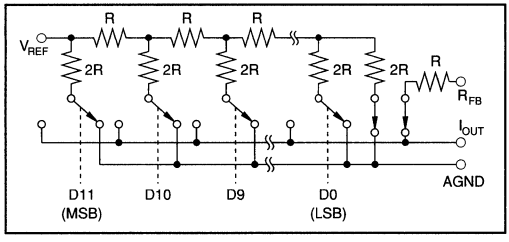


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

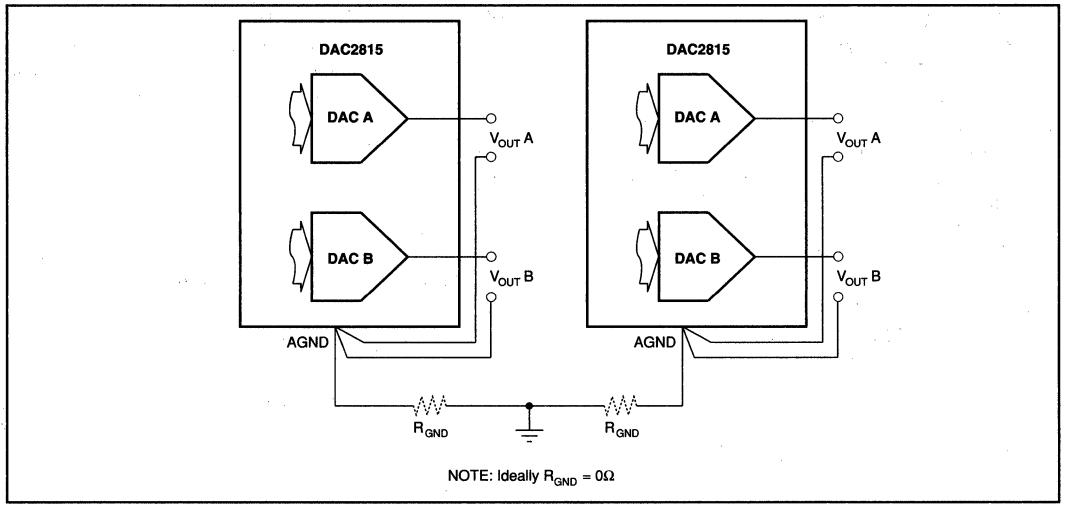


FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2815 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2815 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2815 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

DAC2815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 6. Only one $\overline{\text{LATCH}}$ signal is required for a system where all DAC2815s are updated simultaneously. If you want to update DAC2815s independently, use separate $\overline{\text{LATCH}}$ signals. The $\overline{\text{LATCH}}$ and $\overline{\text{WRITE}}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

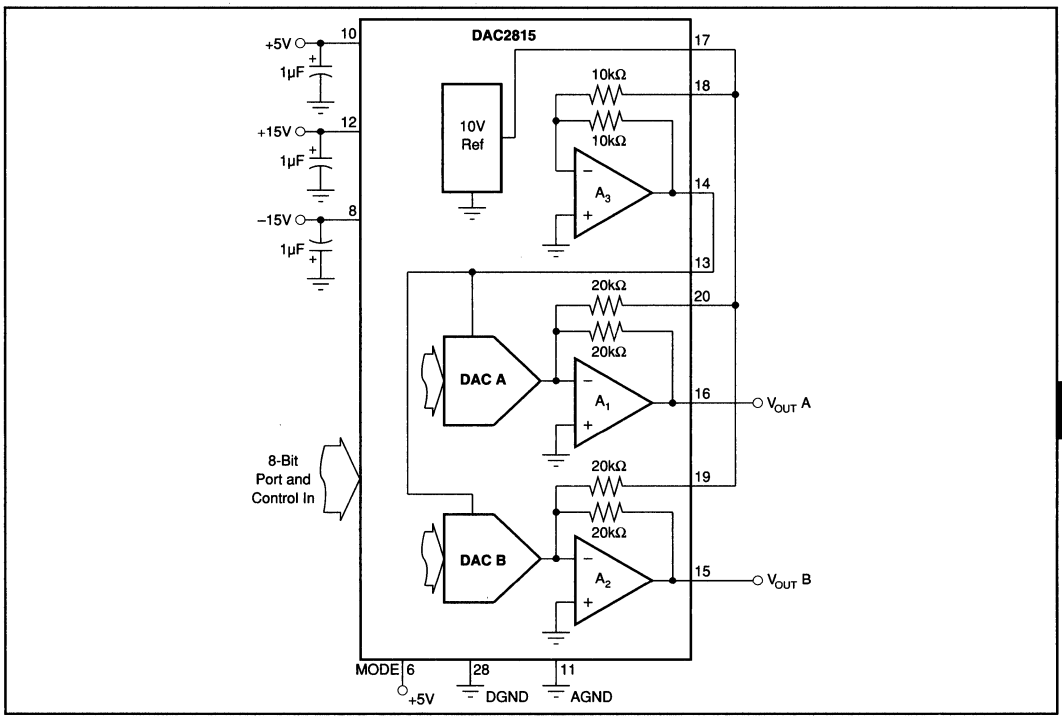


FIGURE 3. Analog Connections for ±10V DAC Output.

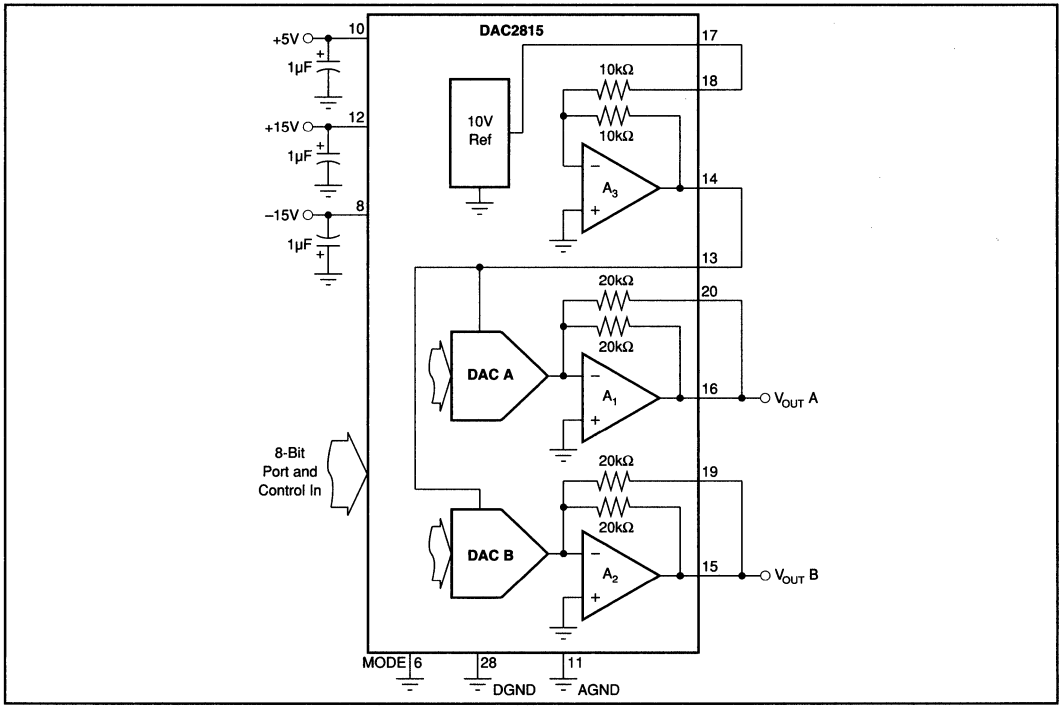


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

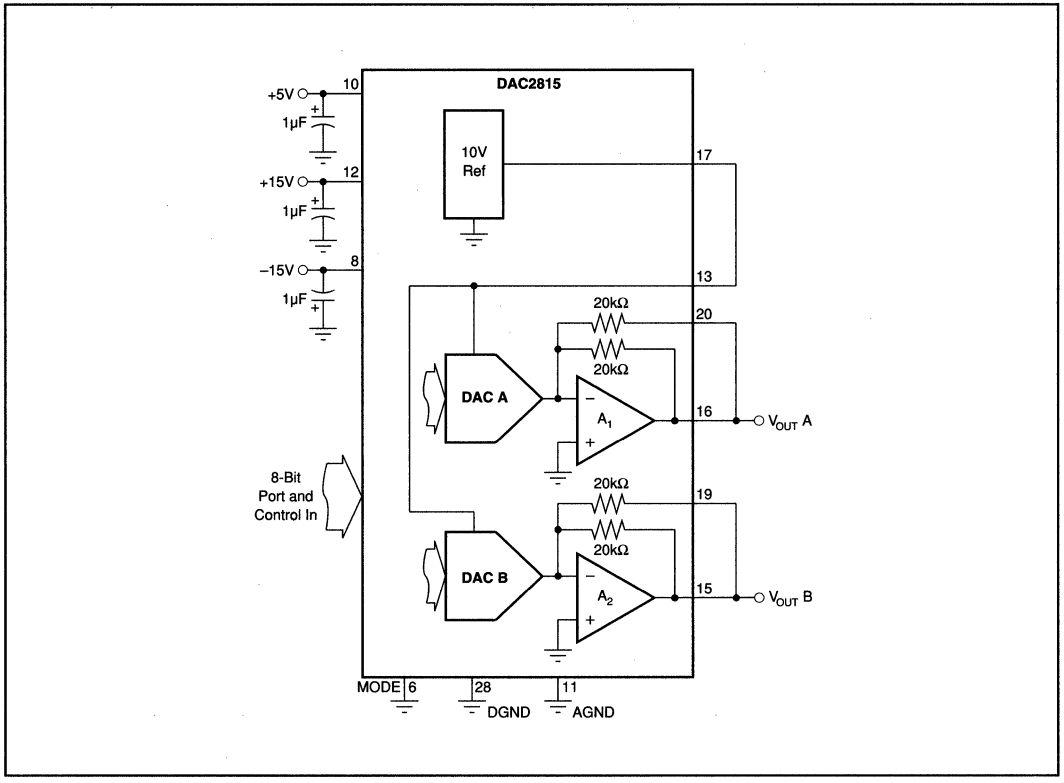


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

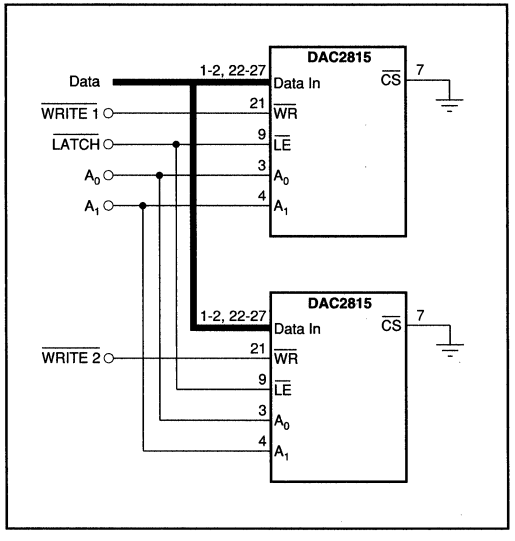


FIGURE 6. Logic Connection for Multiple DAC2815 Packages.

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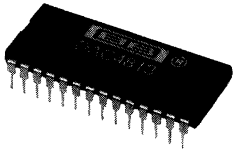


DAC4813

QUAD 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

FEATURES

- COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS
- 12-BIT PORT INTERFACE
- ANALOG OUTPUT RANGE: ±10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- INTEGRAL LINEARITY ERROR: ±1/2LSB max
- ±12V to ±15V SUPPLIES
- 28-PIN PLASTIC DIP PACKAGE

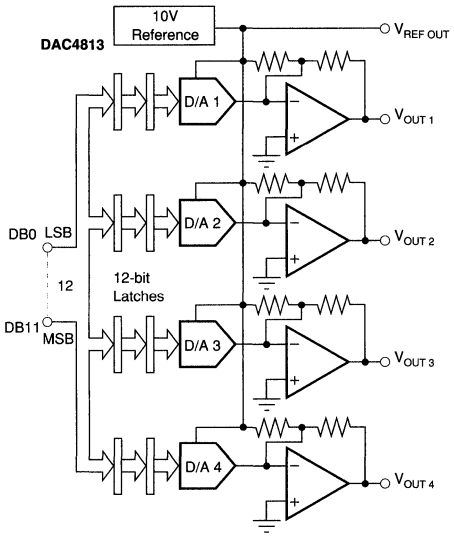
DESCRIPTION

DAC4813 is a complete quad 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC4813 D/A converters are committed to the ±10V output range only. Gain and offset are not externally adjustable.

DAC4813AP is available in one performance grade with a integral linearity error of 1/2LSB and 12-bit monotonicity guaranteed over temperature. It is packaged in 28-pin 0.6in. wide plastic DIP package and specified over –40°C to +85°C.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

PARAMETER	CONDITIONS	DAC4813 MIN	DAC4813 TYP	DAC4813 MAX	UNITS
INPUTS					
DIGITAL INPUTS	Over Temperature				
Input Code (1)	Range		Bipolar Offset Binary		
Logic Levels (2)					
V_{IH} (3)		+2		+5.5	V
V_{IL}		0		+0.8	V
Logic Input Currents					
DB0-DB11, $\overline{WR}$, $\overline{LDAC}$, $\overline{RESET}$,$\overline{EN}_X$					
I_{IH}	V_I = +2.7V			±40	µA
I_{IL}	V_I = +0.4V			±40	µA
TRANSFER CHARACTERISTICS					
ACCURACY					
Linearity Error			±1/4	±1/2	LSB
Differential Linearity Error			±1/2	±1	LSB
Gain Error			±0.05	±0.2	%
Bipolar Zero Error (5)			±0.05	±0.2	%FSR(4)
Power Supply Sensitivity					
Of Full Scale $+V_{CC}$			±5	±20	ppmFSR/%+V_{CC}
$-V_{CC}$			±1	±10	ppmFSR/%−V_{CC}
DRIFT	Over Specification Temperature Range				
Gain			±5	±30	ppm/°C
Bipolar Zero Drift			±5	±15	ppmFSR/°C
Linearity Error over Temperature			±1/2	±3/4	LSB
Monotonicity			Guaranteed		
DYNAMIC CHARACTERISTICS					
SETTLING TIME (6)	To within ±0.012%FSR of Final Value 5kΩ || 500pF Load				
Full Scale Range Change	20V Range		4.5	6	µs
1LSB Output Step (7) At Major Carry		2			µs
Slew Rate			10		V/µs
Crosstalk (8)	5kΩ Loads		0.2		LSB
OUTPUT					
Output Voltage Range	$\pm V_{CC} \geq \pm 11.4V$			±10	V
Output Current		±5			mA
Output Impedance			0.2		Ω
Short Circuit to ACOM Duration	at DC		Indefinite		
REFERENCE VOLTAGE					
Voltage		+9.95	+10.00	+10.05	V
Source Current Available for External Loads		2			mA
Impedance			0.2		Ω
Temperature Coefficient			±5	±25	ppm/°C
Short Circuit to Common Duration	at DC		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$		+11.4	+15	+16.5	V
$-V_{CC}$		−11.4	−15	−16.5	V
Current:	No Load $\pm V_{CC} = \pm 15V$				
$+V_{CC}$			48	60	mA
$-V_{CC}$			24	28	mA
Power Dissipation			1080	1320	mW
Potential at DCOM with Respect to ACOM (9)		−3		+3	V
TEMPERATURE RANGES					
Specification		−40		+85	°C
Storage		−60		+100	°C
Thermal Resistance, θ_{JA},Plastic DIP			30		°C/W

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) Error at input code 800_{HEX}. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) For the worst-case code change: $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (8) Crosstalk is defined as the change in any output as a result of any other output being driven from −10V to +10V at rated output current. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
ACOM to DCOM	±4V
Digital Inputs to DCOM	−1V to $+V_{CC}$
External Voltage applied to BPO Resistor	±18V
$V_{REF\ OUT}$	Indefinite short to ACOM
V_{OUT}	Momentary to ±18V
Lead Temperature, soldering 10s	+300°C
Max Junction Temperature	165°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

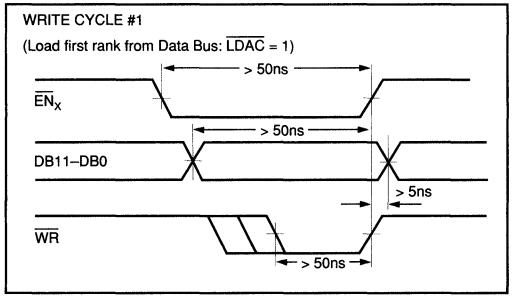
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC4813AP	28-Pin Plastic DBL Wide DIP	215

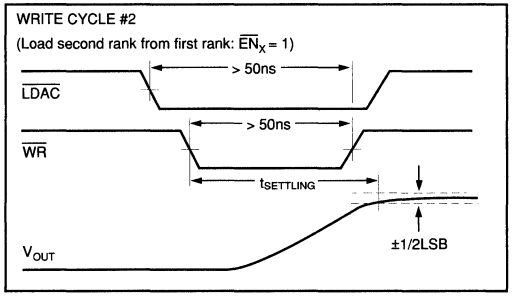
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

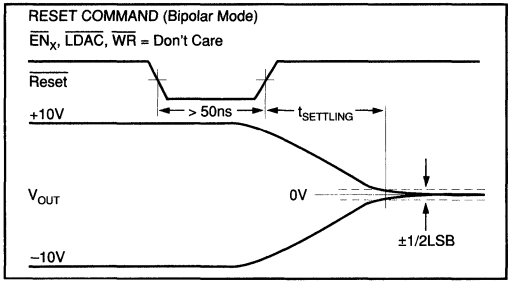
MODEL	PACKAGE	TEMPERATURE RANGE
DAC4813AP	Plastic DIP	−40°C to +85°C

TIMING DIAGRAMS





TIMING DIAGRAMS (CONT)



TRUTH TABLE

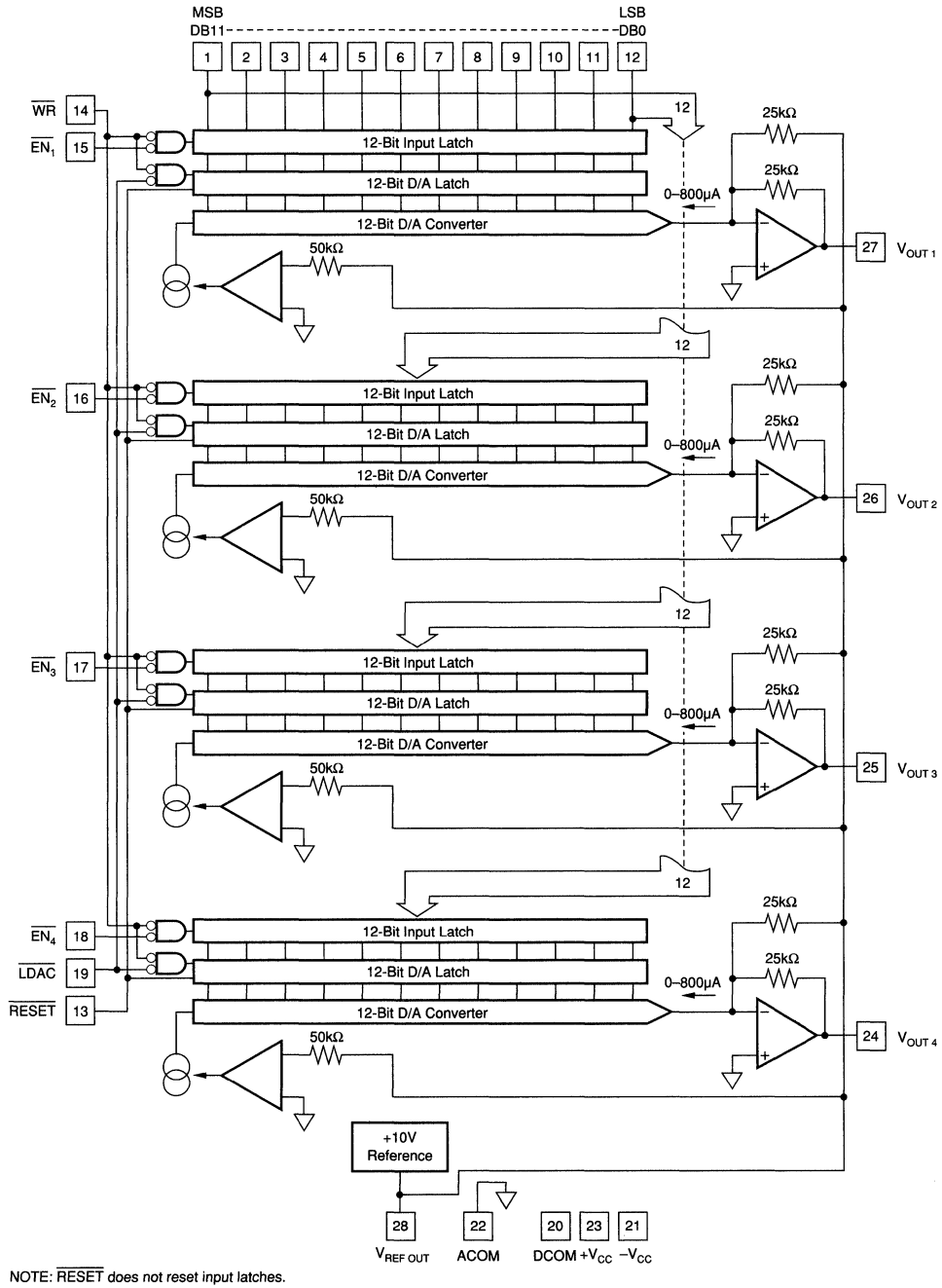
$\overline{WR}$	$\overline{EN1}$	$\overline{EN2}$	$\overline{EN3}$	$\overline{EN4}$	$\overline{LDAC}$	$\overline{RESET}$	OPERATION
X	X	X	X	X	X	0	Reset all D/A Latches
1	X	X	X	X	X	1	No Operation
X	1	1	1	1	1	1	No Operation
0	1	1	1	0	1	1	Load Data into First Rank for D/A 4
0	1	1	0	1	1	1	Load Data into First Rank for D/A 3
0	1	0	1	1	1	1	Load Data into First Rank for D/A 2
0	0	1	1	1	1	1	Load Data into First Rank for D/A 1
0	1	1	1	1	0	1	Load Second Rank from First Rank, All D/As
0	0	0	0	0	0	1	All Latches Transparent

"X" = Don't Care

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	DB11	DATA, MSB, positive true.
2	DB10	DATA
3	DB9	DATA
4	DB8	DATA
5	DB7	DATA
6	DB6	DATA
7	DB5	DATA
8	DB4	DATA
9	DB3	DATA
10	DB2	DATA
11	DB1	DATA
12	DB0	DATA, LSB.
13	$\overline{\text{RESET}}$	Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten by a $\overline{\text{LDAC}}$-$\overline{\text{WR}}$ command. RESET does not reset the input latch. After power–up and reset, input latches will be in an indeterminant state.
14	$\overline{\text{WR}}$	Write strobe. Must be low for data transfer to any latch (except RESET).
15	$\overline{\text{EN1}}$	Enable for 12-bit input data latch of D/A1. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
16	$\overline{\text{EN2}}$	Enable for 12-bit input data latch of D/A2. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
17	$\overline{\text{EN3}}$	Enable for 12-bit input data latch of D/A3. NOTE: This logic path is slower than the $\overline{\text{WR}}$ /path.
18	$\overline{\text{EN4}}$	Enable for 12-bit input data latch of D/A4. NOTE: This logic path is slower than the $\overline{\text{WR}}$/ path.
19	$\overline{\text{LDAC}}$	Load DAC enable. Must be low with $\overline{\text{WR}}$ for data transfer to the D/A latch and simultaneous update of all D/A converters.
20	DCOM	Digital common, logic currents return.
21	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
22	ACOM	Analog common, $+V_{CC}$, $-V_{CC}$ supply return.
23	$+V_{CC}$	Analog supply input, nominally +12V or +15V referred to ACOM.
24	$V_{OUT\ 4}$	D/A 4 analog output.
25	$V_{OUT\ 3}$	D/A 3 analog output.
26	$V_{OUT\ 2}$	D/A 2 analog output.
27	$V_{OUT\ 1}$	D/A 1 analog output.
28	$V_{REF\ OUT}$	+10V reference output.

BLOCK DIAGRAM

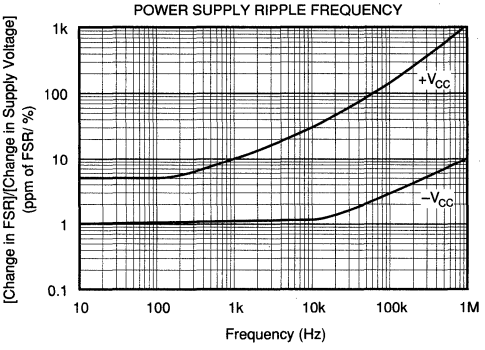


NOTE: $\overline{\text{RESET}}$ does not reset input latches.

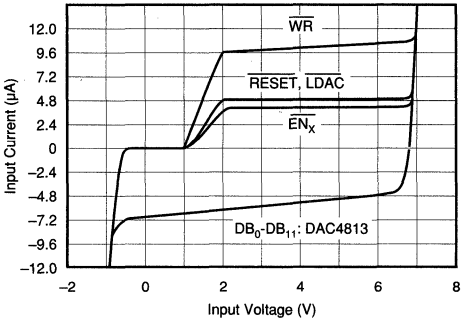
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

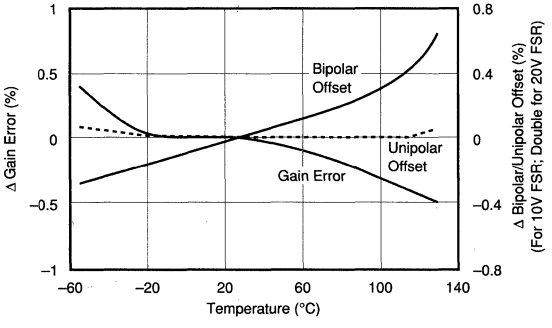
POWER SUPPLY REJECTION vs POWER SUPPLY RIPPLE FREQUENCY



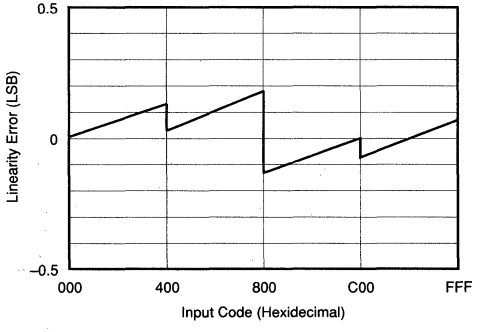
DIGITAL INPUT CURRENTvs INPUT VOLTAGE



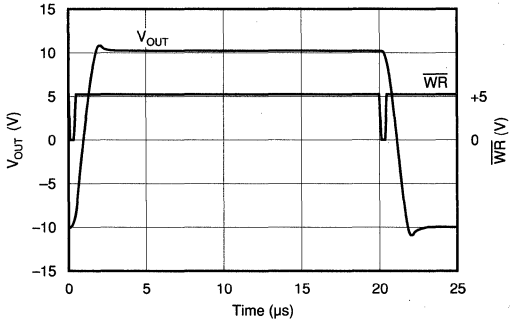
CHANGE OF GAIN AND OFFSET ERROR vs TEMPERATURE



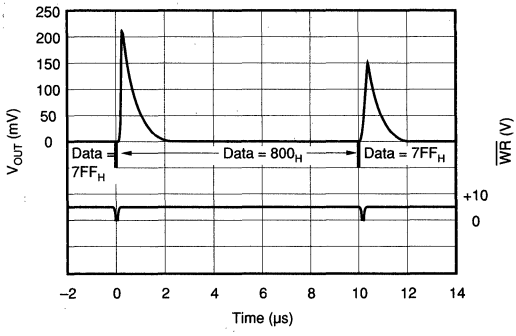
INTEGRAL LINEARITY ERROR



± FULL SCALE OUTPUT SWING

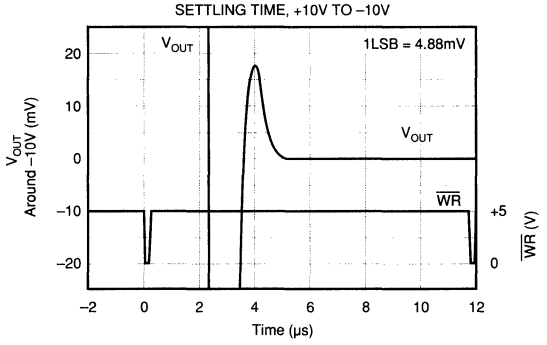


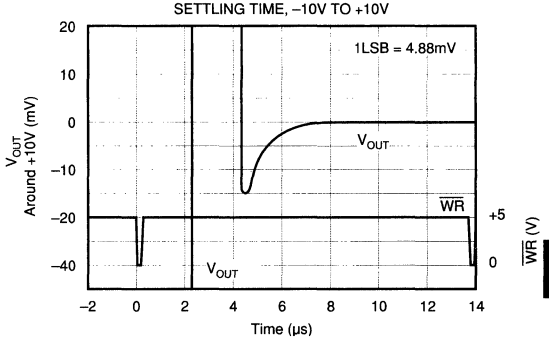
MAJOR CARRY GLITCH



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all "1s" and all "0s"). DAC4813 linearity error is ±1/2LSB max at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. DAC4813 is monotonic over their specification temperature range –40°C to +85°C.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Settling times are specified to ±0.01% of Full Scale Range (FSR) for two conditions: one for a FSR output change of 20V (25kΩ feedback) and one for a 1LSB change. The 1LSB change is measured at the Major Carry ($7FF_{HEX}$ to 800_{HEX}, and 800_{HEX} to $7FF_{HEX}$), the input code transition at which worst-case settling time occurs.

OPERATION

INTERFACE LOGIC

The bus interface logic of the DAC4813 consists of two independently addressable latches in two ranks for each D/A converter. The first rank consists of one 12-bit input latch which can be loaded directly from a 12- or 16-bit microprocessor/microcontroller bus. The input latch holds data temporarily before it is loaded into the second latch, the D/A latch. This double buffered organization permits simultaneous update of all D/As.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When the control signals return to logic "1", the data is latched.

CAUTION: DAC4813 was designed to use $\overline{WR}$ as the fast strobe. $\overline{WR}$ has a much faster logic path than $\overline{EN}_X$ (or $\overline{LDAC}$). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_X$ to strobe data into the latches, the DATA HOLD time will be long, approximately 20ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

RESET FUNCTION

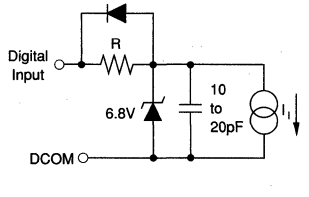
The Reset function resets only the D/A latch. Therefore, after a RESET, good data must be written to **all** the input latches before an $\overline{LDAC}$ – $\overline{WR}$ command is issued. Otherwise, old data or unknown data is present in the input latches and will be transferred to the D/A latch producing an analog output value that may be unwanted.

LOGIC INPUT COMPATIBILITY

DAC4813 digital inputs are TTL compatible (1.4V switching level) over the operating range of $+V_{CC}$. Each input has low leakage and high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC4813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition, the speed of the interface will be slower. A digital output driving a DATA input line of the DAC4813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

Unused control inputs should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available, the control inputs can be connected to $+V_{CC}$ through a 100kΩ resistor to limit the input current.



DIGITAL INPUT	DAC4813 RΩ
Data, $\overline{LDAC}$, $\overline{WR}$, $\overline{RESET}$	250
$\overline{EN_x}$	330

FIGURE 1. Equivalent Digital Input Circuit.

INPUT CODING

DAC4813 accepts positive-true binary input codes.

Input coding for bipolar analog outputs is Bipolar Offset Binary (BOB), where an input code of 000_{HEX} gives a minus full-scale output, an input of FFF_{HEX} gives an output 1LSB below positive full scale, and zero occurs for an input code of 800_{HEX}.

DAC4813 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

INTERNAL/EXTERNAL REFERENCE USE

DAC4813 contains a +10V ±50mV voltage reference, $V_{REF\,OUT}$. $V_{REF\,OUT}$ is available to drive external loads sourcing up to 2mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the D/A converters will vary.

Because of the lack of additional pins required for external reference inputs, $V_{REF\,OUT}$ is connected internally to all 4 D/A converters. $V_{REF\,OUT}$ is available for external use on pin 28.

GAIN AND OFFSET ADJUSTMENTS

DAC4813 has no Gain and Offset Adjustment option.

INSTALLATION

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added. Best settling time performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be ale to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

DAC4813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both DIGITAL COMMON (DCOM) and ANALOG COMMON (ACOM) be connected directly to a ground plane under the package. If a ground place is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\,OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. The change in current in the ACOM pin due to an input date word change from 000_{HEX} to FFF_{HEX} is only 1mA for each D/A converter.

OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

DAC4813 output amplifiers provide a ±10V output swing while operating on supplies as low as ±12V ±5%.

DAC4813 is fully committed to ±10V output ranges. Optional ranges are not pin programmable.

12- AND 16-BIT BUS INTERFACES

DAC4813 data is latched into the input latches of each D/A by asserting low each $\overline{ENx}$ individually and transferring the data from the bus to each input latch by asserting $\overline{WR}$ low. All D/A outputs in each package are then updated simultaneously by asserting $\overline{LDAC}$ and $\overline{WR}$ low.

Be sure to read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

BURR-BROWN®

DAC4814

Quad 12-Bit Digital-to-Analog Converter (Serial Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED SERIAL INTERFACE (10MHz CLOCK)
- LOW POWER: 600mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

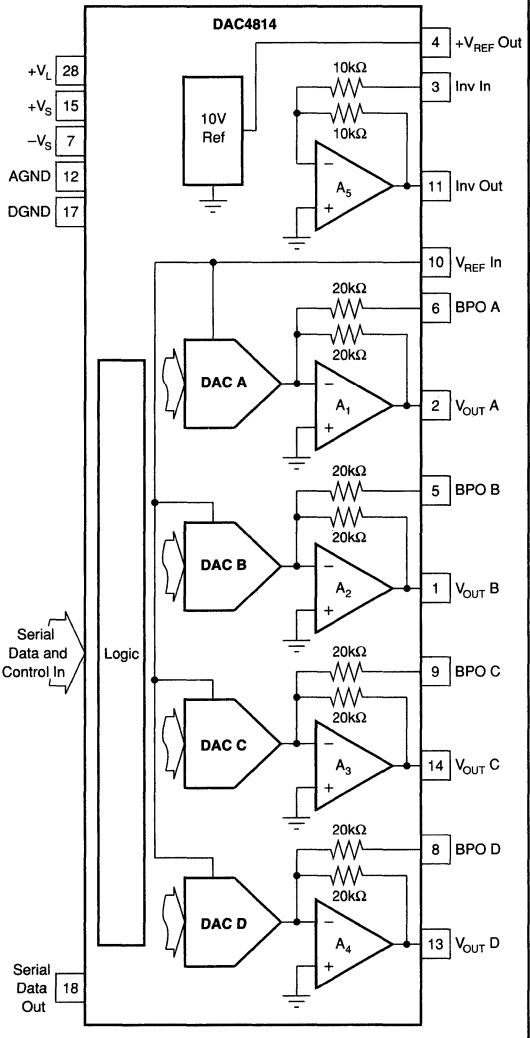
DESCRIPTION

The DAC4814 is one in a family of dual and quad 12-bit digital-to-analog converters. Serial, 8-bit, 12-bit interfaces are available.

The DAC4814 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC4814 has a high-speed serial interface capable of being clocked at 10MHz. Serial data are clocked DAC D MSB first into a 48-bit shift register, then strobed into each DAC separately or simultaneously as required. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC4814 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP MIN	DAC4814AP TYP	DAC4814AP MAX	DAC4814BP MIN	DAC4814BP TYP	DAC4814BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		+2		+5	*		*	V
V_{IL} (Input Low Voltage)		0		+0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
DIGITAL OUTPUT								
Data Out V_{OL}	I_{SINK} = 1.6mA	0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5	*		*	V
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C to +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			*	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+6.5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(Δ V_{OUT} vs Δ I_{LOAD})								
Supply Regulation				±5			*	ppm/V
(Δ V_{OUT} vs Δ V_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT (Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition C_L= 100pF		3			*		nV-s
D/A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4814AP			DAC4814BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+20	+24		*	*	mA
$-I_S$			–20	–25.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.4	2		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			10			*	mA
Total Power, All DACs			600	753		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed to but not tested.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V, –18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

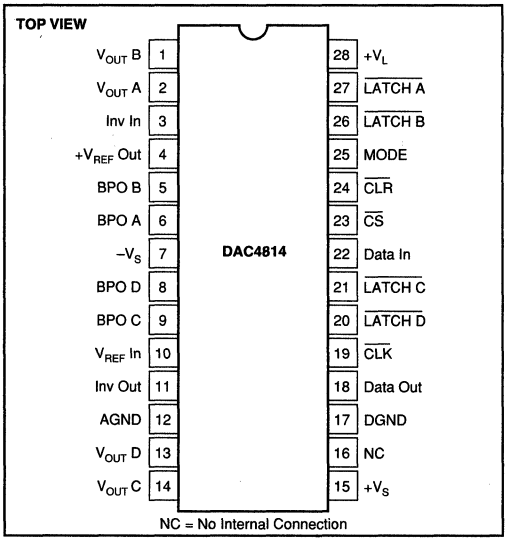
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC4814AP	28-Pin Plastic DBL Wide DIP	215
DAC4814BP	28-Pin Plastic DBL Wide DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN DESIGNATIONS

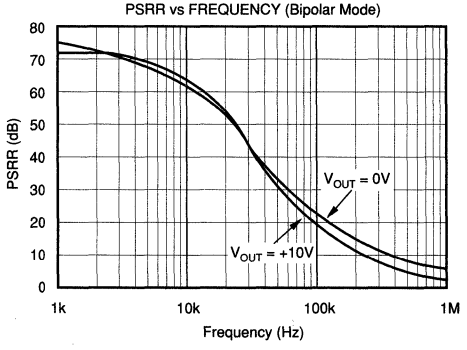
PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	$+V_L$	Positive logic power supply, +5V input
2	V_{OUT} A	Analog output voltage, DAC A	27	$\overline{\text{LATCH A}}$	Latch data update, logic input, DAC A
3	Inv In	Inverter (A_S) input	26	$\overline{\text{LATCH B}}$	Latch data update, logic input, DAC B
4	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	25	MODE	Selection input for unipolar or bipolar reset to zero
5	BPO B	Biplolar offset input, DAC B	24	$\overline{\text{CLR}}$	Asynchronous input reset to zero
6	BPO A	Bipolar offset input, DAC A	23	$\overline{\text{CS}}$	Chip select enable, DAC A, B, C, and D
7	$-V_S$	Negative analog power supply , –15V input	22	Data In	Serial data input
8	BPO D	Bipolar offset input, DAC D	21	$\overline{\text{LATCH C}}$	Latch data update, logic input, DAC C
9	BPO C	Bipolar offset input, DAC C	20	$\overline{\text{LATCH D}}$	Latch data update, logic input, DAC D
10	V_{REF} In	± Reference voltage input	19	$\overline{\text{CLK}}$	Clock input
11	Inv Out	Inverter (A_S) output	18	Data Out	Serial data output
12	AGND	Analog common	17	DGND	Digital common
13	V_{OUT} D	Analog output voltage, DAC D	16	NC	No internal connection
14	V_{OUT} C	Analog output voltage, DAC C	15	$+V_S$	Positive analog power supply, +15V input

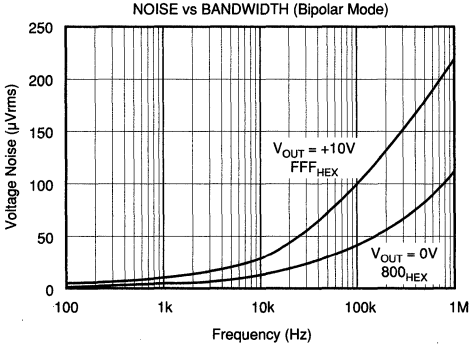
PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

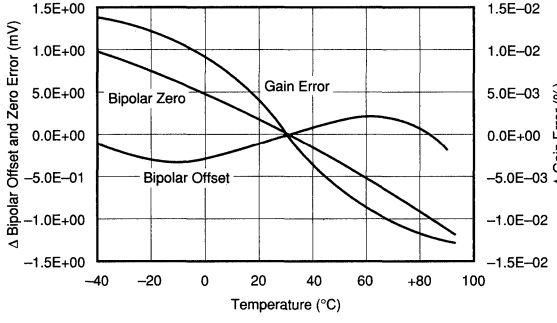




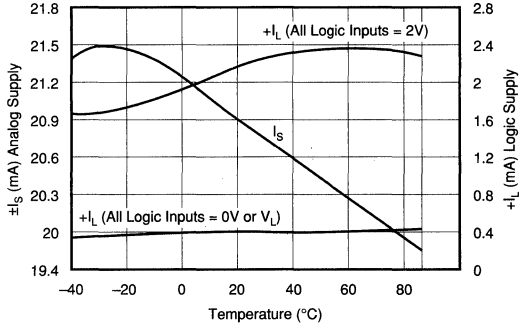
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

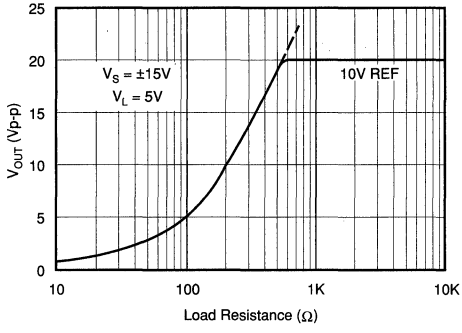
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



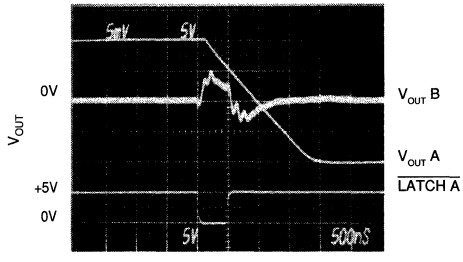
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



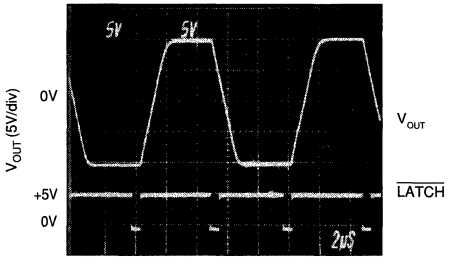
CROSSTALK (Bipolar Mode)



Time (500ns/div)

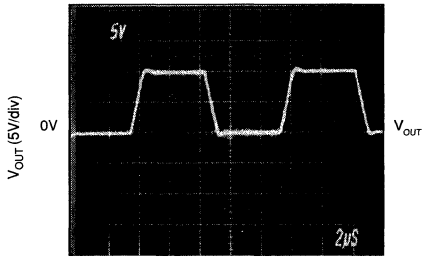
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{\text{LATCH}}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

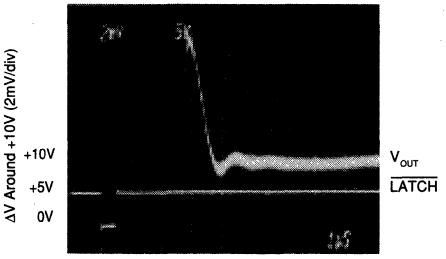


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

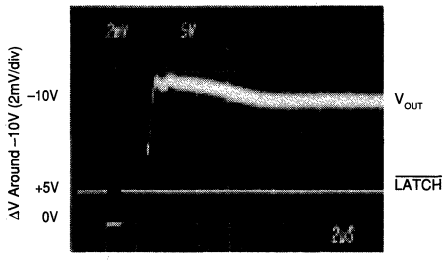
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



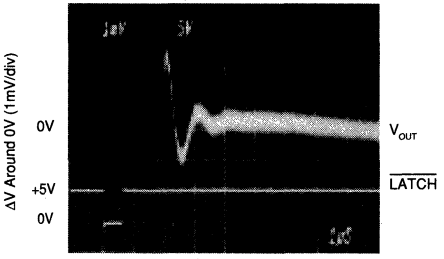
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



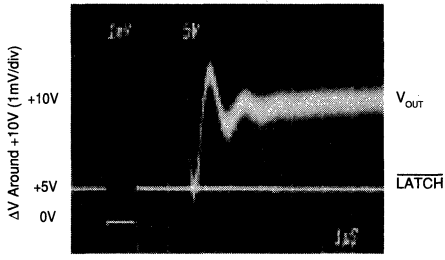
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



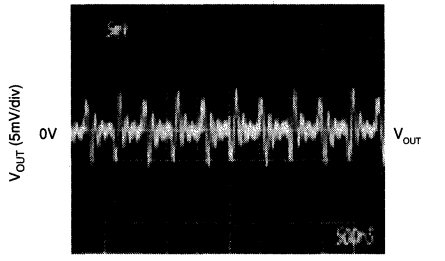
Time (1µs/div)

MAJOR CARRY GLITCH

Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



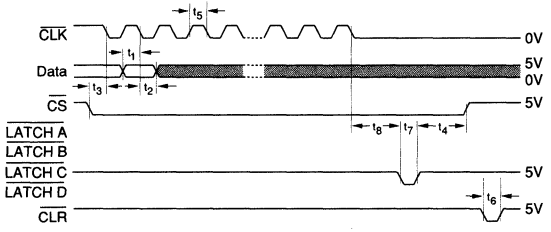
Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

V_S = ±15V, V_L = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Data Setup Time	15ns
t_2—Data Hold Time	15ns
t_3—Chip Select to $\overline{CLK}$, Latch, Data Setup Time	15ns
t_4—Chip Select to $\overline{CLK}$, Latch, Data Hold Time	40ns
t_5—$\overline{CLK}$ Pulse Width	40ns
t_6—Clear Pulse Width	40ns
t_7—Latch Pulse Width	40ns
t_8—$\overline{CLK}$ Edge to $\overline{LATCH\ A}$, $\overline{LATCH\ B}$, $\overline{LATCH\ C}$, or $\overline{LATCH\ D}$	15ns



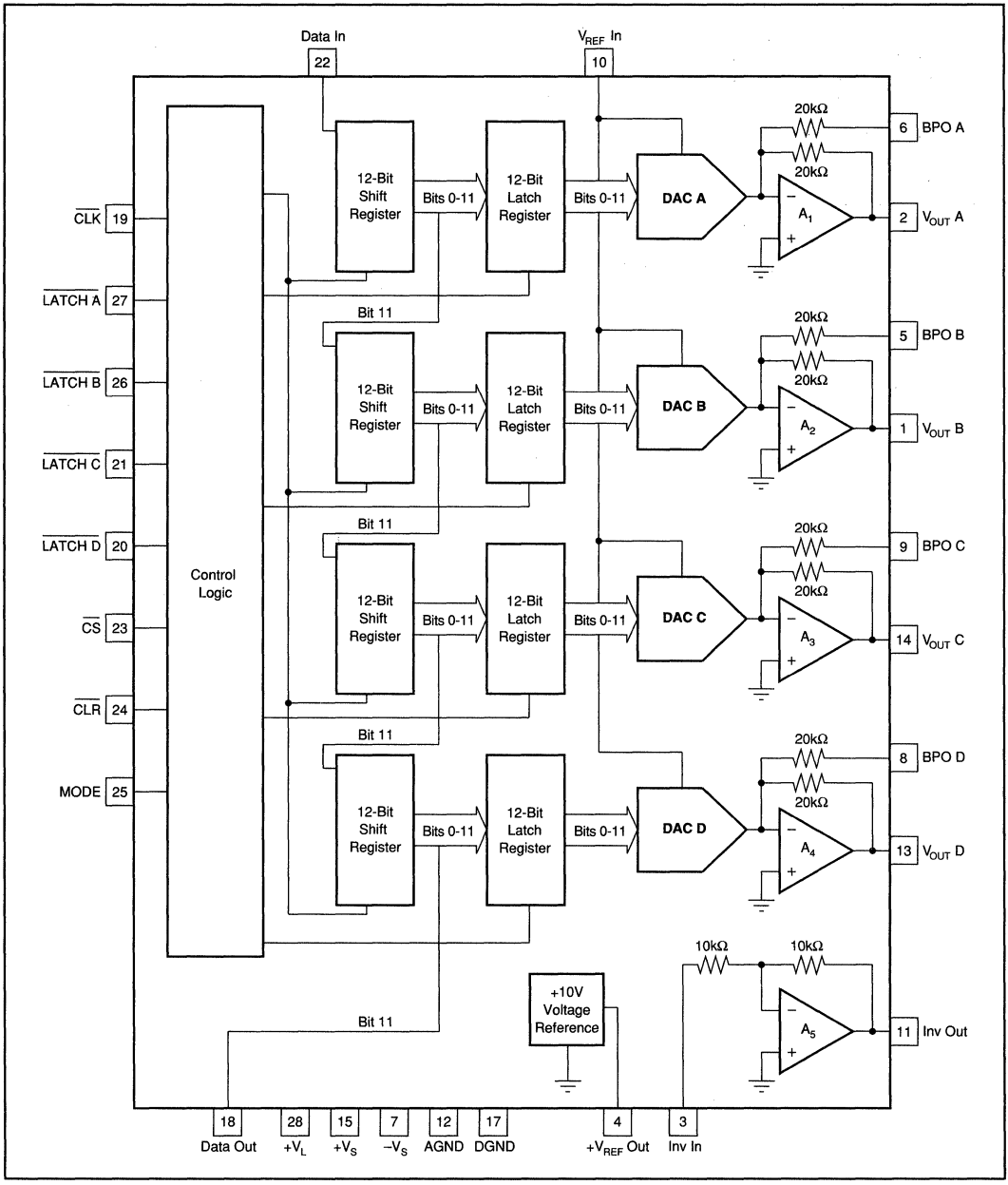
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V • t_R = t_F = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{CLK}$	$\overline{CS}$	$\overline{LATCH\ A}$	$\overline{LATCH\ B}$	$\overline{LATCH\ C}$	$\overline{LATCH\ D}$	FUNCTION
X	1	↓	0	X	X	X	X	Data clocked in
X	1	X	1	X	X	X	X	No data transfer
X	1	X	0	0	1	1	1	DAC A register updated
X	1	X	0	1	0	1	1	DAC B register updated
X	1	X	0	1	1	0	1	DAC C register updated
X	1	X	0	1	1	1	0	DAC D register updated
X	1	X	0	0	0	0	0	All DAC registers updated simultaneously
0	0	X	X	X	X	X	X	All registers cleared
1	0	X	X	X	X	X	X	Shift registers cleared = 000_{HEX}, DAC registers = 800_{HEX}

Note: X = Don't Care. ↓ = Falling edge triggered.

FUNCTIONAL BLOCK DIAGRAM, DAC4814 — Quad 12-bit DAC, Serial Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4814 are TTL and 5V CMOS compatible. Input codes for the DAC4814 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4814.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

DACs can be updated simultaneously or independently as required. Data are transferred on falling clock edges into a 48-bit shift register. DAC D MSB is loaded first. Data are transferred to the DAC registers when the $\overline{\text{LATCH}}$ signals are brought low. The data are latched when the $\overline{\text{LATCH}}$ signals are brought high. All $\overline{\text{LATCH}}$ signals may be tied together to allow simultaneous update of the DACs if required. The output of the DAC shift register is provided to allow cascading of several DACS on the same bit stream. By using separate signals for $\overline{\text{LATCH A}}$, $\overline{\text{LATCH B}}$, $\overline{\text{LATCH C}}$, and $\overline{\text{LATCH D}}$ it is possible to update one of the four DACs every 12 clock cycles.

When $\overline{\text{CLR}}$ is brought low, the input shift registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX}. If $\overline{\text{LATCH}}$ is brought low after $\overline{\text{CLR}}$, the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4814 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

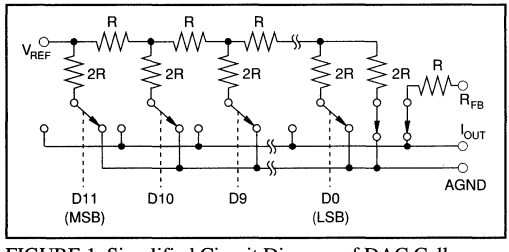


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC4814 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar output connect the DAC4814 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC4814 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

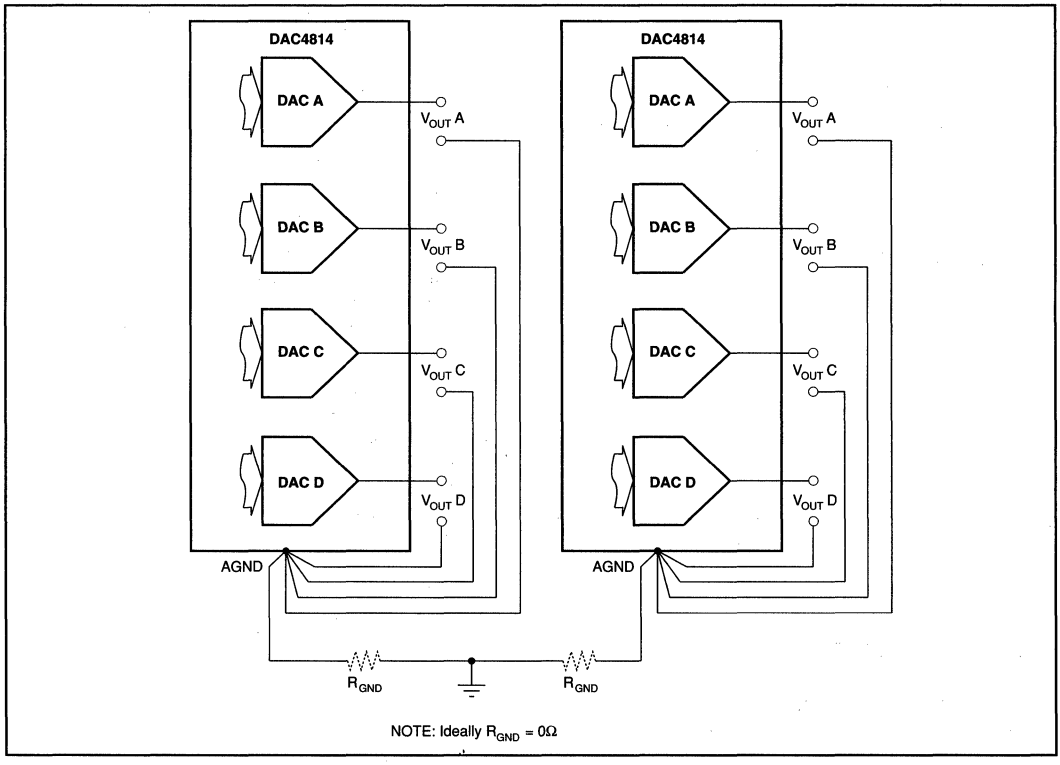


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

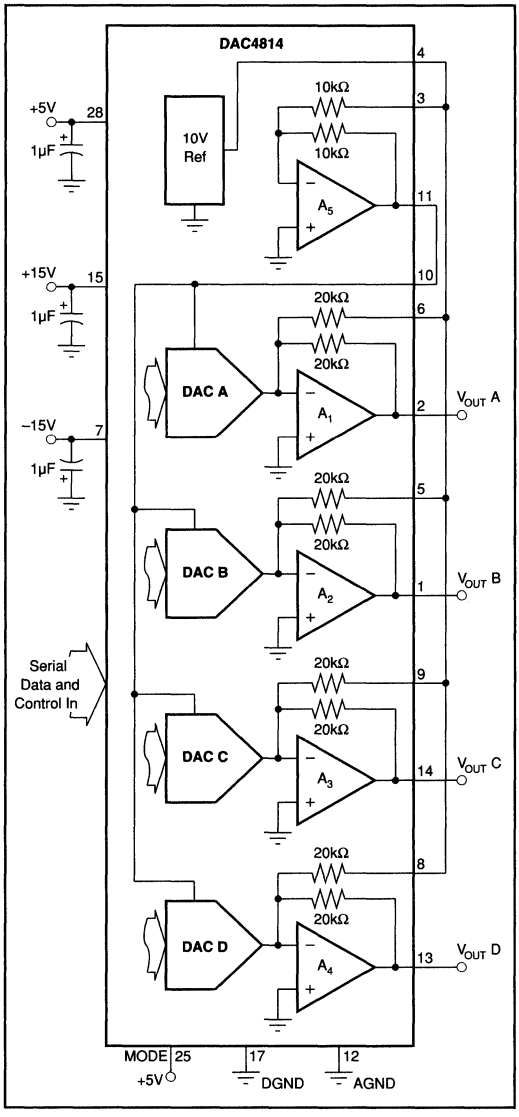


FIGURE 3. Analog Connections for ±10V DAC Output.

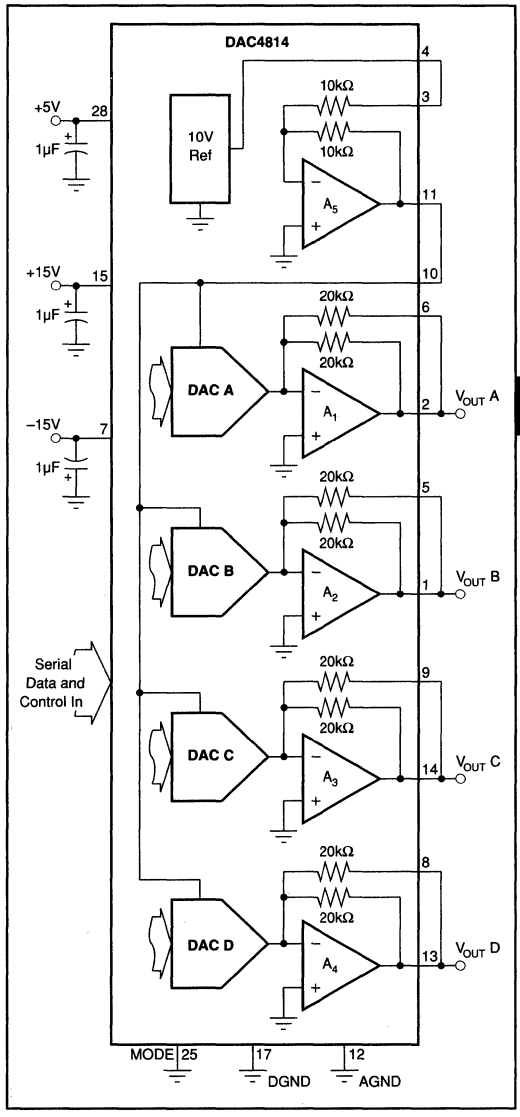


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC4814 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

Cascaded Bus Connection

Multiple DAC4814s can be connected to the same $\overline{CLK}$ and DATA input lines in two ways. Since the output of the DAC shift register is available, any number of DAC4814s can be cascaded on the same input bit stream as shown in Figure 6. This arrangement allows all DACs in the system to be updated simultaneously and requires a minimum number of control signal inputs. However, up to 48N $\overline{CLK}$ cycles may be required to update any given DAC, where N = number of DAC4814s.

Parallel Bus Connection

Several DAC4814s can also have their DATA inputs connected in parallel as shown in Figure 7. This allows any DAC in the system to be updated in a maximum of 48 $\overline{CLK}$ cycles.

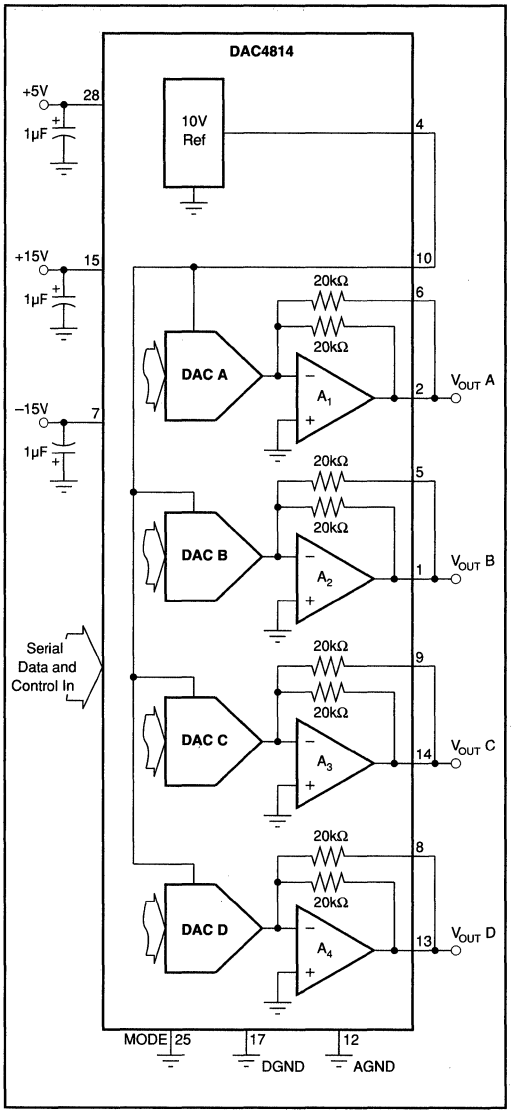


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

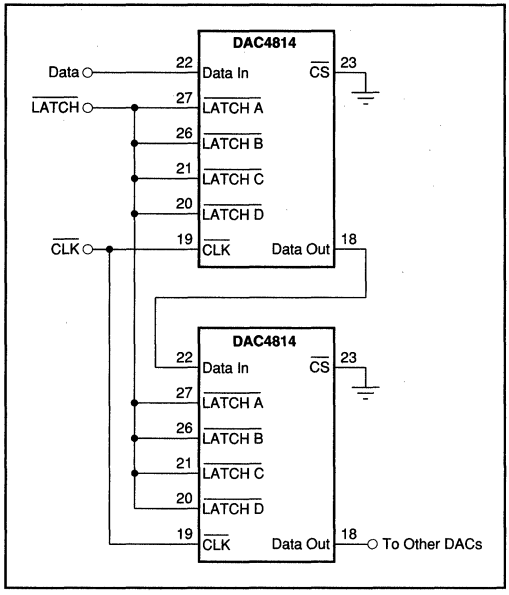


FIGURE 6. Cascaded Serial Bus Connection for Multiple DAC Packages.

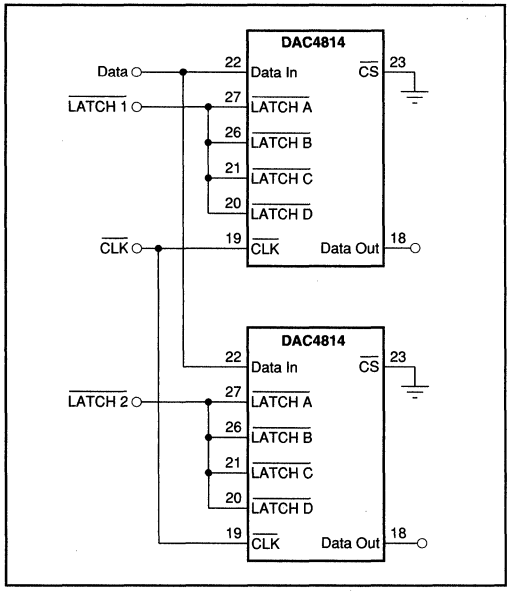


FIGURE 7. Parallel Bus Connection for Multiple DAC Packages.

BURR - BROWN®

DAC4815

Quad 12-Bit Digital-to-Analog Converter (8-Bit Port Interface)

FEATURES

- COMPLETE QUAD DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER, 600mW (150mW/DAC)
- LOW GAIN DRIFT, 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- BIPOLAR OUTPUT
- CLEAR/RESET TO BIPOLAR ZERO

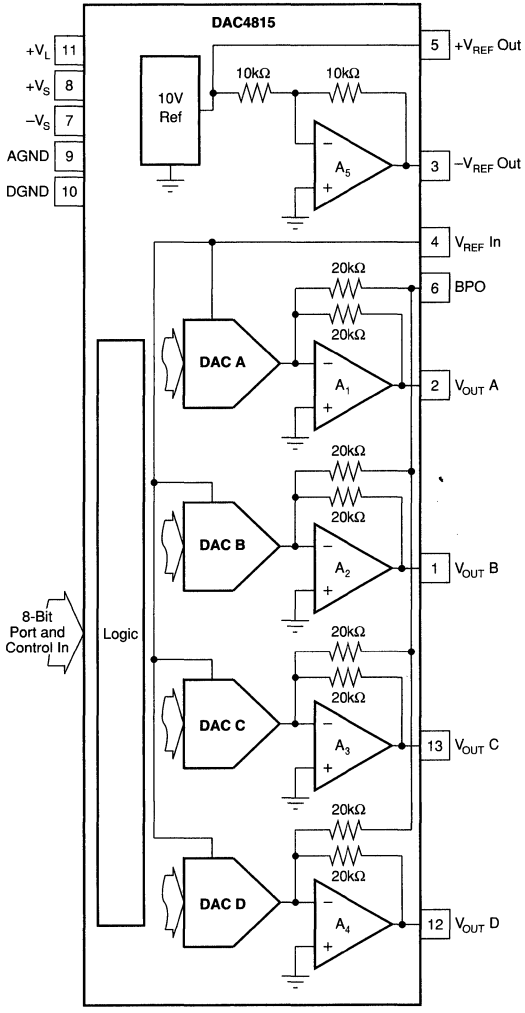
DESCRIPTION

The DAC4815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC4815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for bipolar ±10V output range.

The DAC4815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to bipolar zero. This feature is useful for power-on reset or system calibration. The DAC4815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC4815AP MIN	DAC4815AP TYP	DAC4815AP MAX	DAC4815BP MIN	DAC4815BP TYP	DAC4815BP MAX	UNITS
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		2		5	*		*	V
V_{IL} (Input Low Voltage)		0		0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		±1.5/–1				±1	LSB
Bipolar Zero Error			±20			±10	mV	
Gain Error	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V			30			*	ppmFSR/V
	V_L = +4.5V to +5.5V							
TEMPERATURE DRIFT								
Gain Drift			±5	±30		*	±20	ppm/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
–REFERENCE OUTPUT, Inverter								
–10V Reference		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			30			*		mA
REFERENCE INPUT								
Reference Input Resistance		1.75	2.5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		3.5	5		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[4]	C_L = 100pF							
Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT								
(Code Dependent)			±4			*		mA
DIGITAL CROSSTALK	Full Scale Transition		3			*		nV-s
	C_L= 100pF							
DIGITAL-TO-ANALOG GLITCH IMPULSE			30			*		nV-s
POWER SUPPLY								
$+V_S$ and $–V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+20	+24		*	*	mA
$–I_S$			–20	–25.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.4	2		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			10			*	mA
Total Power, All DACs			600	753		*	*	mW

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

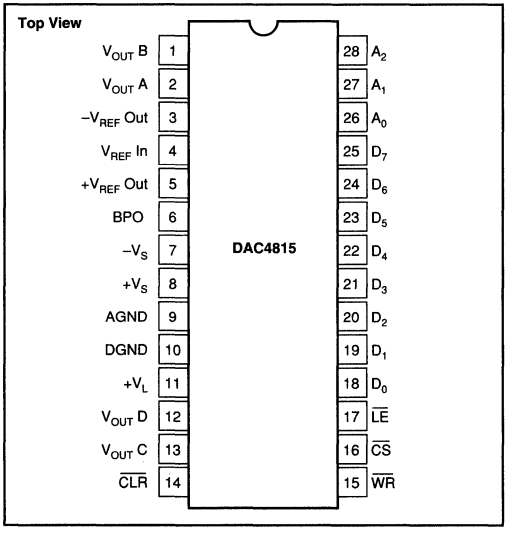
PARAMETER	CONDITIONS	DAC4815AP			DAC4815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes effect of voltage output DAC, voltage references. (4) Guaranteed but not tested.

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	V_{OUT} B	Analog output voltage, DAC B	28	A_2	Address line 2 input
2	V_{OUT} A	Analog output voltage, DAC A	27	A_1	Address line 1 input
3	$-V_{REF}$ Out	Negative reference voltage output (–10V output)	26	A_0	Address line 0 input
4	V_{REF} In	± Reference voltage input	25	D_7	Data bit 7 input
5	$+V_{REF}$ Out	Positive reference voltage output (+10V output)	24	D_6	Data bit 6 input
6	BPO	Bipolar offset input, DAC A, B, C, and D	23	D_5	Data bit 5 input
7	$-V_S$	Negative analog power supply, –15V input	22	D_4	Data bit 4 input
8	$+V_S$	Positive analog power supply, +15V input	21	D_3	Data bit 3 input
9	AGND	Analog common	20	D_2	Data bit 2 input
10	DGND	Digital common	19	D_1	Data bit 1 input
11	$+V_L$	Positive logic power supply, +5V input	18	D_0	Data bit 0 input
12	V_{OUT} D	Analog output voltage, DAC D	17	$\overline{LE}$	Latch data enable, DAC A, B, C, and D
13	V_{OUT} C	Analog output voltage, DAC C	16	$\overline{CS}$	Chip select enable, DAC A, B, C, and D
14	$\overline{CLR}$	Asynchronous input reset to zero	15	$\overline{WR}$	Write input, DAC A, B, C, and D

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V,–18V
AGND to DGND	±0.3V
Any digital input to GND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC4815AP	±1
DAC4815BP	±1/2

PACKAGE INFORMATION

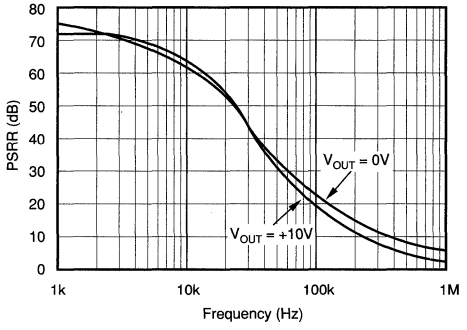
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC4815AP	28-Pin Plastic DIP	215
DAC4815BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

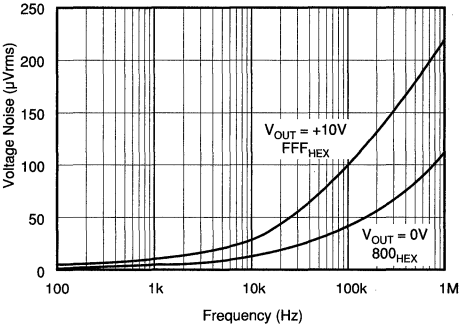
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

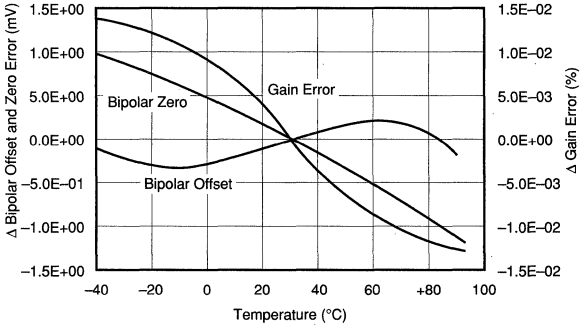
PSRR vs FREQUENCY (Bipolar Mode)



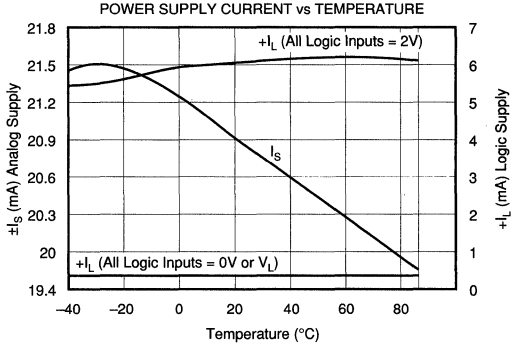
NOISE vs BANDWIDTH (Bipolar Mode)



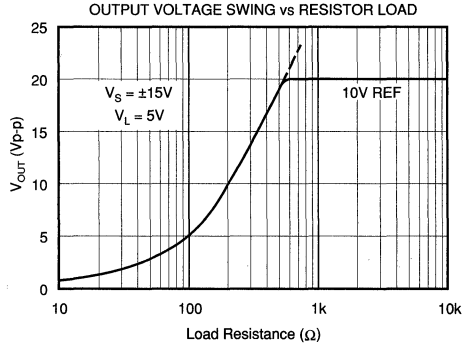
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



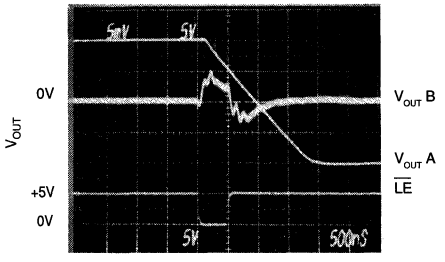
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



CROSSTALK (Bipolar Mode)



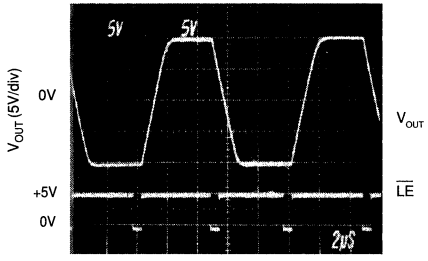
Time (500ns/div)

NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of $\overline{LE}$ signal.

TYPICAL PERFORMANCE CURVES (CONT)

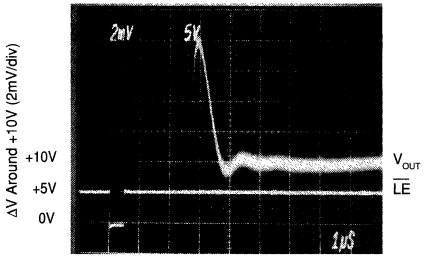
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

FULL-SCALE OUTPUT SWING
BIPOLAR (20V Step)



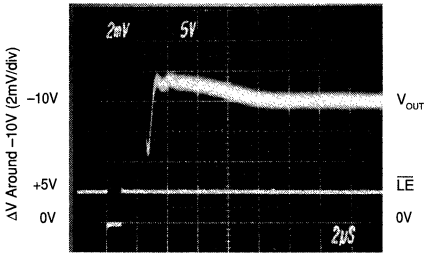
Time (2µs/div)

SETTLING TIME
BIPOLAR (–10V to +10V)



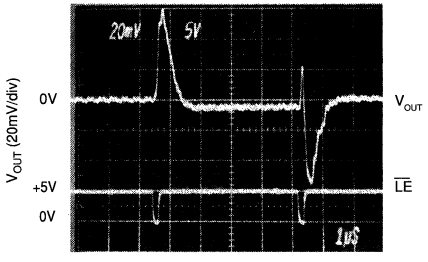
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



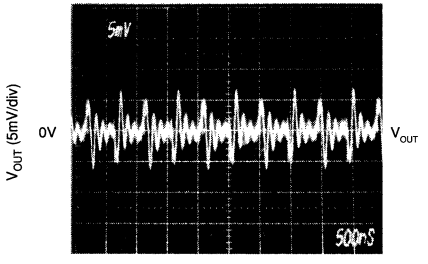
Time (2µs/div)

MAJOR CARRY GLITCH



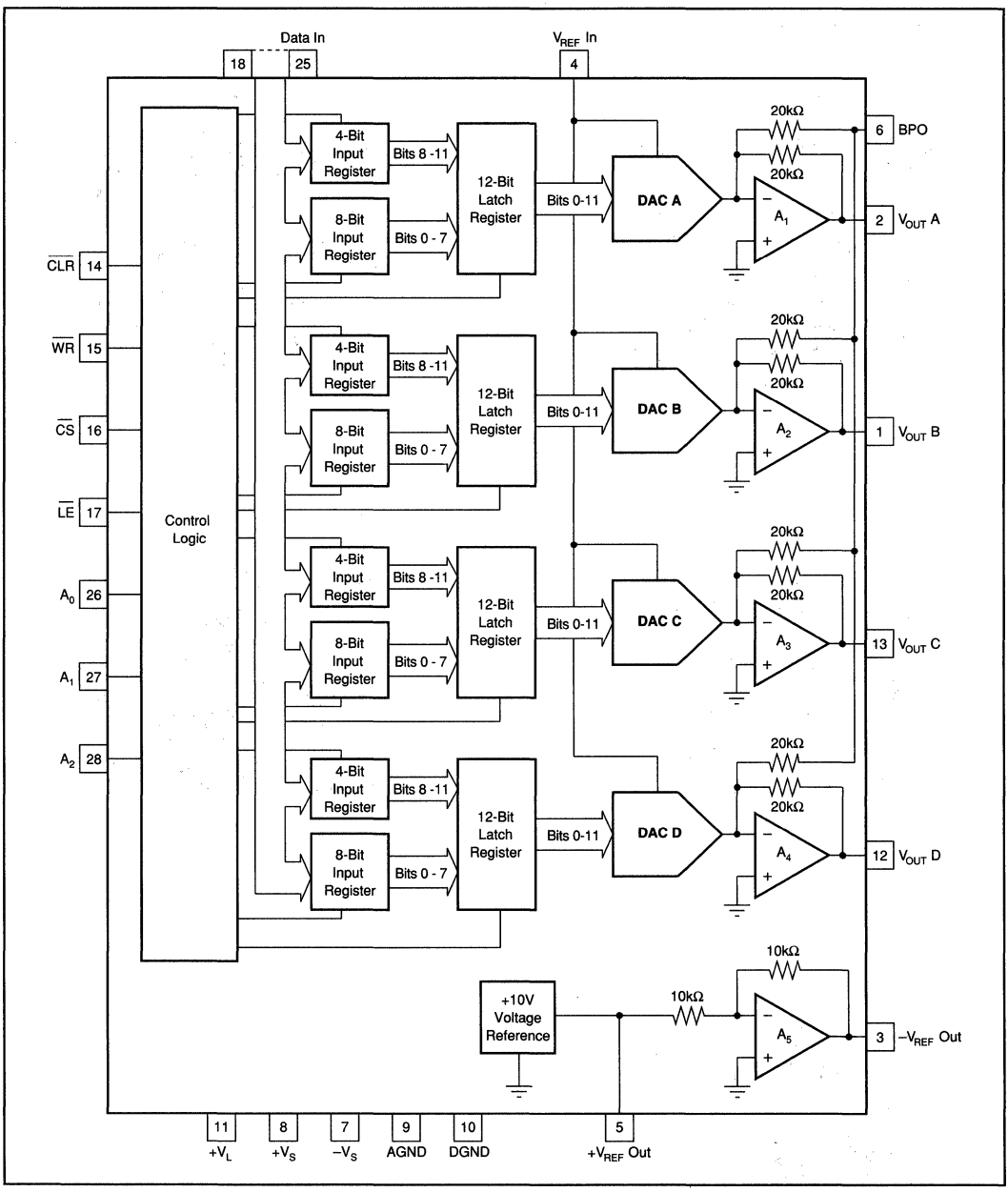
Time (1µs/div)
NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



Time (500ns/div)
DAC output noise due to activity on digital inputs with latch disabled.

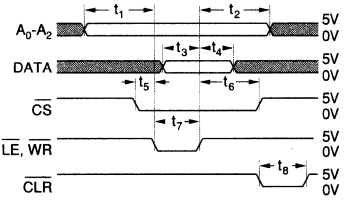
FUNCTIONAL BLOCK DIAGRAM, DAC4815 — Quad 12-bit DAC, 8-bit Port



TIMING CHARACTERISTICS

$+V_L$ = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	20ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns



NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_2	A_1	A_0	FUNCTION
1	1	0	0	0	0	0	DAC A LS input register loaded with D7-D0(LSB)
1	1	0	0	0	0	1	DAC A MS input register loaded with D3(MSB)-D0
1	1	0	0	0	1	0	DAC B LS input register loaded with D7-D0(LSB)
1	1	0	0	0	1	1	DAC B MS input register loaded with D3(MSB)-D0
1	1	0	0	1	0	0	DAC C LS input register loaded with D7-D0(LSB)
1	1	0	0	1	0	1	DAC C MS input register loaded with D3(MSB)-D0
1	1	0	0	1	1	0	DAC D LS input register loaded with D7-D0(LSB)
1	1	0	0	1	1	1	DAC D MS input register loaded with D3(MSB)-D0
1	0	0	1	X	X	X	All DAC registers updated simultaneously from input registers
1	0	0	0	X	X	X	All DAC registers are transparent
1	X	1	X	X	X	X	No data transfer
1	1	X	1	X	X	X	No data transfer
0	X	X	X	X	X	X	Input registers cleared = 000_{HEX}, DAC registers = 800_{HEX}

NOTE: X = Don't care.

DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC4815 are TTL and 5V CMOS compatible. Input codes for the DAC4815 are BOB (Bipolar Offset Binary). See Figure 3 for ±10V bipolar connection.

BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	BIPOLAR (BOB)
FFF_{HEX}	+Full Scale
800_{HEX}	Zero
$7FF_{HEX}$	Zero – 1 LSB
000_{HEX}	–Full Scale

INTEGRAL OR RELATIVE LINEARITY

This term, also know as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX}.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} - V_{MIN}$) from the ideal span of 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC4815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. The data are latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bringing $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. All DACs are updated simultaneously.

When $\overline{CLR}$ is brought low, the input registers are cleared to 000_{HEX} while the DAC registers = 800_{HEX}. If $\overline{LE}$ is brought low after $\overline{CLR}$ the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or OV (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the four DACs in the DAC4815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a –10V reference are shared by all DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

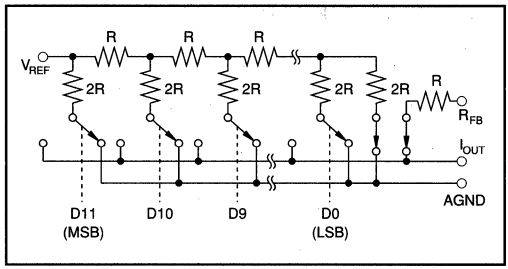


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

POWER SUPPLY CONNECTIONS

The DAC4815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

±10V OUTPUT RANGE CONNECTION

For a ±10V bipolar output connect the DAC4815 as shown in Figure 3.

CONNECTION TO DIGITAL BUS

DAC4815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 4. Only one $\overline{LATCH}$ signal is required for a system where all DAC4815s are updated simultaneously. If your want to update DAC4815s independently, use separate $\overline{LATCH}$ signals. The $\overline{LATCH}$ and $\overline{WRITE}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

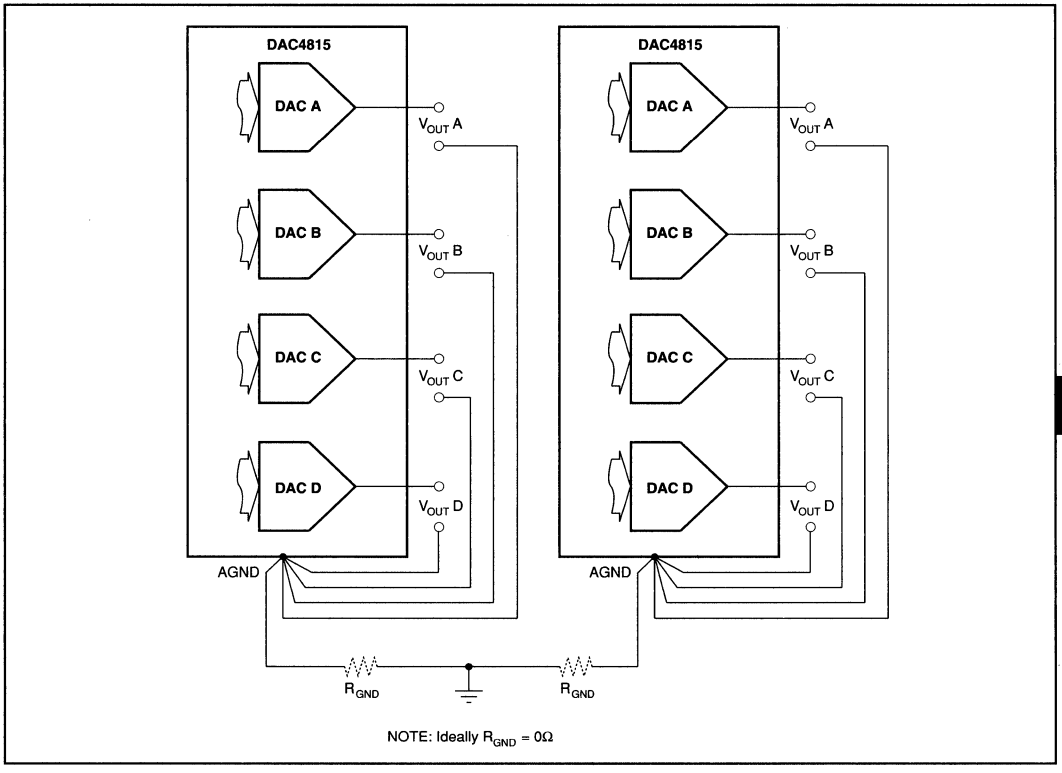


FIGURE 2. Recommended Ground Connections for Multiple DAC Packages.

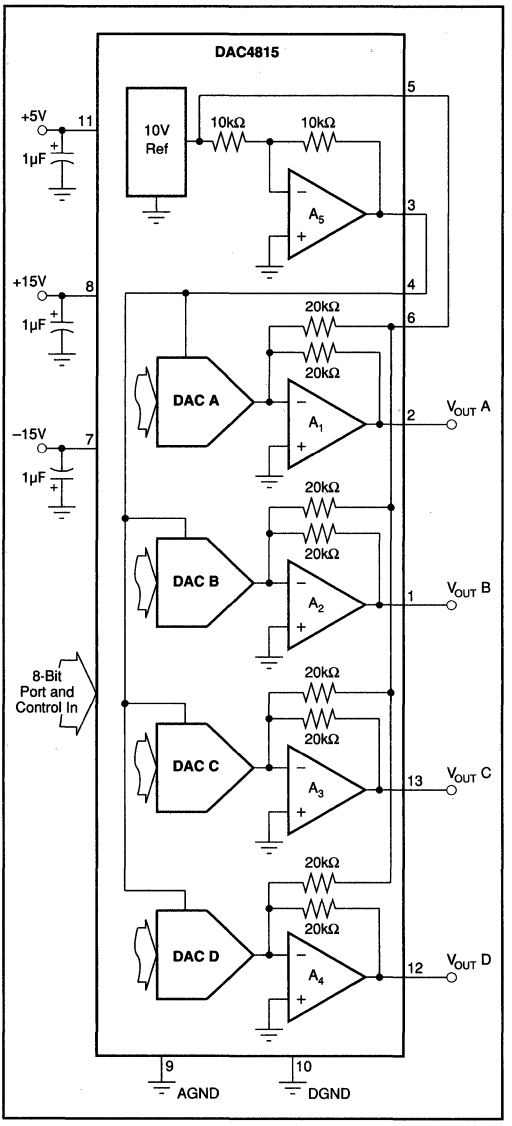


FIGURE 3. Analog Connections for ±10V DAC Output.

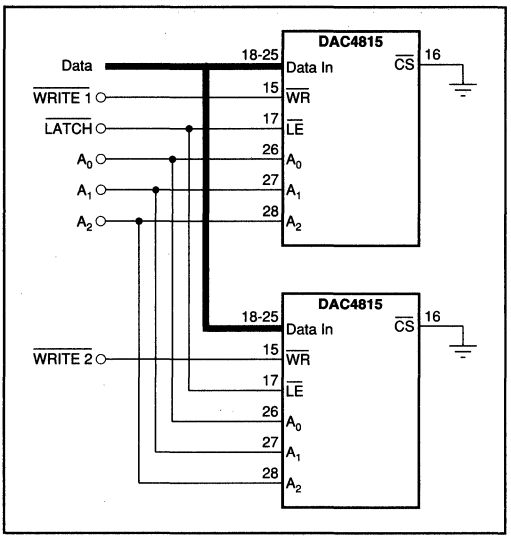


FIGURE 4. Logic Connections for Multiple DAC4815 Packages.

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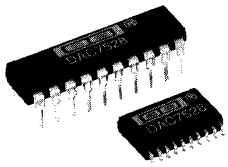


DAC7528

CMOS Dual 8-Bit Buffered Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

- DOUBLE BUFFERED DATA LATCHES
- SINGLE 5V SUPPLY OPERATION
- ±1/2 LSB LINEARITY
- FOUR-QUADRANT MULTIPLICATION
- DACs MATCHED TO 1%

APPLICATIONS

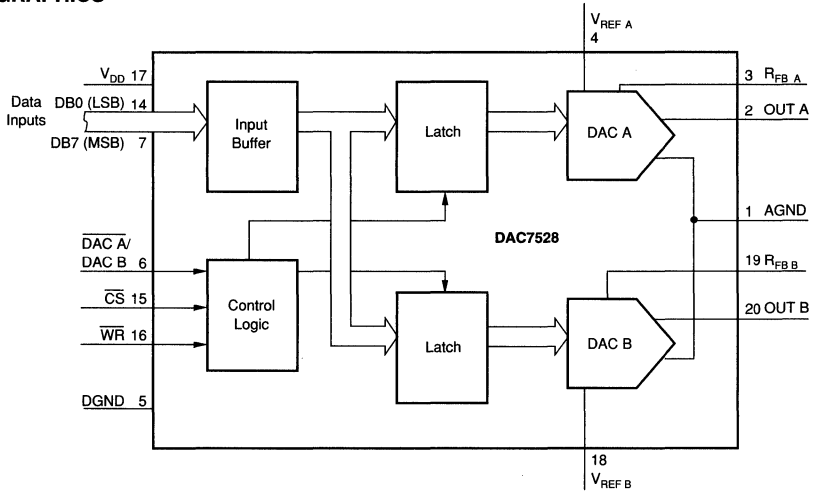
- DIGITALLY CONTROLLED FILTERS
- DISK DRIVES
- AUTO CALIBRATION
- MOTOR CONTROL SYSTEMS
- PROGRAMMABLE GAIN/ATTENUATION
- X-Y GRAPHICS

DESCRIPTION

The DAC7528 contains two, 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors.

Each DAC operates independently with separate reference input pins and internal feedback resistors. Excellent converter-to-converter matching is maintained.

The DAC7528 operates from a single +5V power supply. The inputs are TTL-compatible. Package options include 20-pin plastic DIP and SOIC.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

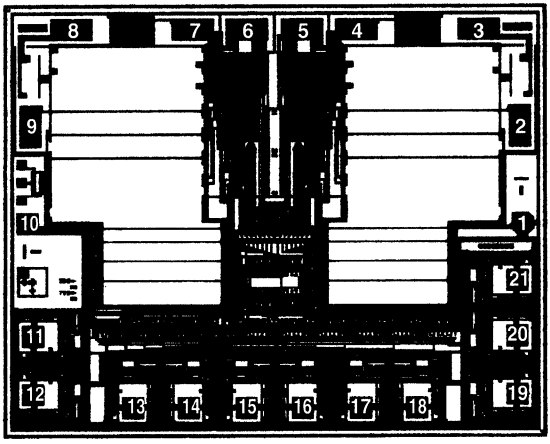
ELECTRICAL

At V_{DD} = +5V; $V_{REFA, B}$ = + 10V; I_{OUT} = GND = 0V: T = Full Temperature Range specification under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC7528P, U			DAC7528PB, UB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY (1)									
Resolution	N		8			8			Bits
Relative Accuracy	INL				±1			±1/2	LSB
Differential Nonlinearity	DNL	Guaranteed Monolithic Over Temp			±1			±1/2	LSB
FS Gain Error (2)		T_A = +25°C			±2			±1	LSB
		$T_A = T_{MIN}$ to T_{MAX}			±4			±2	LSB
Gain Tempco (2)(3)				±2	±35		–	–	ppm/°C
Supply Rejection	PSR	ΔV_{DD} = ±5%, T_A = +25°C		0.001	0.01		–	–	%FSR/%
		$T_A = T_{MIN}$ to T_{MAX}		0.001	0.01		–	–	%FSR/%
Output Leakage Current (OUTA)		DACA = 00_{16}, T_A = +25°C			±50			–	nA
		$T_A = T_{MIN}$ to T_{MAX}			±200			–	nA
Output Leakage Current (OUTB)		DACB = 00_{16}, T_A = +25°C			±50			–	nA
		$T_A = T_{MIN}$ to T_{MAX}			±200			–	nA
REFERENCE INPUT									
Input Resistance		(V_{REFA}, V_{REFB})	8	10	15	–	–	–	kΩ
Input Resistance Match		(V_{REFA}, V_{REFB})			±1			–	%
DYNAMIC PERFORMANCE (4)									
Output Current Settling Time to 1/2 LSB		Enable Pins Low T_A = +25°C			180			–	ns
		Load = 100Ω/13pF, $T_A = T_{MIN}$ to T_{MAX}			200			–	ns
Digital-to-Analog Propagation Delay		Enable Pins Low T_A= +25°C			80			–	ns
to 90% of Output		Load = 100Ω/13pF, $T_A = T_{MIN}$ to T_{MAX}			100			–	ns
Digital-to-Analog Impulse				125			–		nVs
AC Feedthrough		V_{REFA} = 20Vpp Sinewave, T_A = +25°C			–70				dB
(V_{REFA} to OUTA)		100kHz, V_{REFB} = 0V, $T_A = T_{MIN}$ to T_{MAX}			–65				dB
AC Feedthrough		V_{REFA} = 20Vpp Sinewave, T_A = +25°C			–70				dB
(V_{REFB} to OUTB)		100kHz, V_{REFB} = 0V, $T_A = T_{MIN}$ to T_{MAX}			–65				dB
Channel-to-Channel Isolation		V_{REFA} = 20Vpp Sinewave, 100kHz,		–90			–		dB
(V_{REFA} to OUTB)		V_{REFB} = 0V, Both DACs = FF_{16}							
Channel-to-Channel Isolation		V_{REFB} = 20Vpp Sinewave 100kHz,		–90			–		dB
(V_{REFB} to OUTA)		V_{REFA} = 0V, Both DACs = FF_{16}							
Digital Crosstalk		Measured With Code Transition 00_{16} to FF_{16}		30			–		nVs
Harmonic Distortion	THD	V_{IN} = 6Vrms at 1kHz		–85			–		dB
ANALOG OUTPUTS (4)									
OUTA capacitance	C_{OUTA}	DAC = 00_{16}			50			–	pF
		DAC = FF_{16}			120			–	pF
OUTB capacitance	C_{OUTB}	DAC = 00_{16}			50			–	pF
		DAC = FF_{16}			120			–	pF
DIGITAL INPUTS									
Input High Voltage	V_{IH}		2.4			–			V
Input Low Voltage	V_{IL}				0.8			–	V
Input Current	I_{IN}	T_A = +25°C			±1			–	µA
		$T_A = T_{MIN}$ to T_{MAX}			±10			–	µA
Input Capacitance (4)	C_{IN}	All Digital Inputs			10			–	pF
POWER REQUIREMENTS									
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}, T_A = +25°C			1			–	mA
		$T_A = T_{MIN}$ to T_{MAX}			1			–	mA
		Digital Inputs = 0V or V_{DD}, T_A = +25°C			100			–	µA
		$T_A = T_{MIN}$ to T_{MAX}			500			–	µA
SWITCHING CHARACTERISTICS (100% tested) See Timing Diagram									
Chip Select To Write Setup Time	t_{CS}	T_A = +25°C	200			–			ns
		$T_A = T_{MIN}$ to T_{MAX}	230			–			ns
Chip Select To Write Hold Time	t_{CH}	T_A = +25°C	20			–			ns
		$T_A = T_{MIN}$ to T_{MAX}	30			–			ns
DAC Select To Write Setup Time	t_{AS}	T_A = +25°C	200			–			ns
		$T_A = T_{MIN}$ to T_{MAX}	230			–			ns
DAC Select To Write Hold Time	t_{AH}	T_A = +25°C	20			–			ns
		$T_A = T_{MIN}$ to T_{MAX}	30			–			ns
Write Pulse Width	t_{WR}	T_A = +25°C	180			–			ns
		$T_A = T_{MIN}$ to T_{MAX}	200			–			ns
Data Setup Time	t_{DS}	T_A = +25°C	110			–			ns
		$T_A = T_{MIN}$ to T_{MAX}	130			–			ns
Data Hold Time	t_{DH}	T_A = +25°C	0			–			ns

NOTES: (1) Specifications apply to both DACs. (2) Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}. (3) Guaranteed, but not tested. (4) These characteristics are for design guidance only and are not subject to test.

DICE INFORMATION



DAC7528 TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION	PAD	FUNCTION
1	V_{DD}	8	$R_{FB\ A}$	15	DB4
2	$V_{REF\ B}$	9	$V_{REF\ B}$	16	DB3
3	$R_{FB\ B}$	10	DGND	17	DB2
4	OUTB	11	$\overline{DAC\ A}$/DAC B	18	DB1
5	AGNDB	12	DB7	19	DB0
6	AGNDA	13	DB6	20	$\overline{CS}$
7	OUTA	14	DB5	21	$\overline{WR}$

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	104 x 124	2.6 x 3.1
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10

PACKAGE INFORMATION

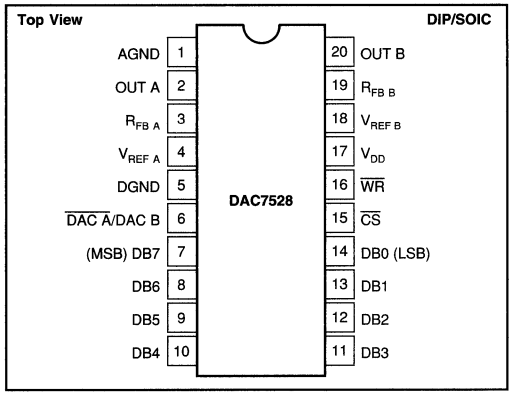
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC7528P	20-Pin Plastic DIP	222
DAC7528PB	20-Pin Plastic DIP	222
DAC7528U	20-Pin SOIC	221
DAC7528UB	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	INL	PACKAGE	TEMPERATURE RANGE
DAC7528P	±1LSB	20-Pin Plastic DIP	–40°C to +85°C
DAC7528PB	±1/2LSB	20-Pin Plastic DIP	–40°C to +85°C
DAC7528U	±1LSB	20-Pin SOIC	–40°C to +85°C
DAC7528UB	±1/2LSB	20-Pin SOIC	–40°C to +85°C

PIN CONFIGURATION



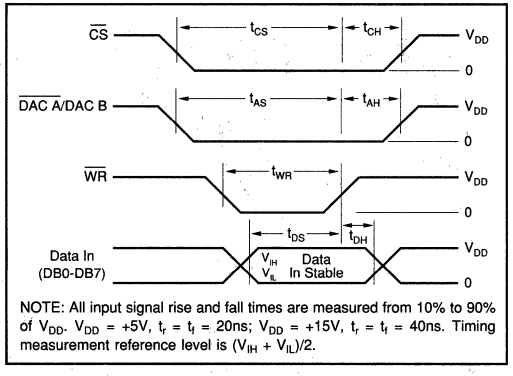
ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	0V, +7V
$V_{REFA, B}$ to GND	±25V
$R_{FA,B}$ to GND	±25V
Digital Input Voltage Range	–0.3V to V_{DD}
Output Voltage (pins 2, 20)	–0.3V to V_{DD}
Operating Temperature Range U,P	–40°C to +85°C
DICE	0°C to +70°C
Junction Temperature	+150°C
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
θ_{JA} U package	105°C/W
P package	85°C/W
θ_{JC} U package	60°C/W
P package	35°C/W

NOTES: θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for PDIP package.

CAUTION: (1) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except $V_{REFA, B}$ (pins 4 and 18) and $R_{FBA, B}$ (pins 3 and 19). (2) The digital control inputs are zener-protected: however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. (3) Use proper antistatic handling procedures. (4) Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

WRITE CYCLE TIMING DIAGRAM



NOTE: All input signal rise and fall times are measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

MODE SELECTION TABLE

$\overline{\text{DAC A/DAC B}}$	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

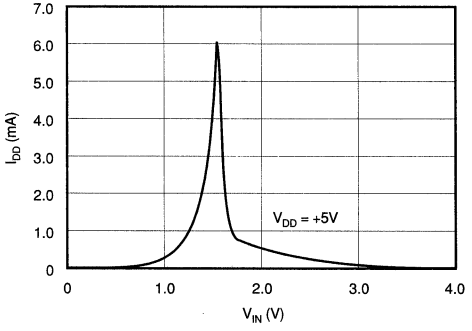
Digital Inputs: All digital inputs of the DAC7528 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. $R_{FB\ A}$, $V_{REF\ A}$, $R_{FB\ B}$, and $V_{REF\ B}$ show some sensitivity.

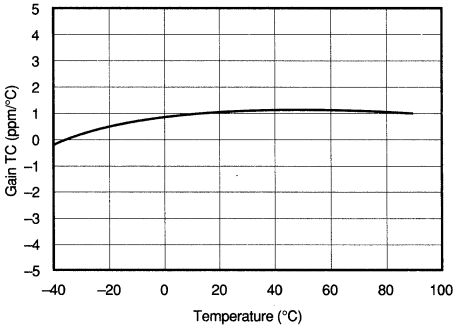
TYPICAL PERFORMANCE CURVES

At V_{DD} = +5V; $V_{REFA,B}$ = +10V; I_{OUT} = GND = 0V: T = Full Temperature Range Specification under Absolute Maximum Ratings unless otherwise noted.

SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



DAC7528 GAIN TC



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC7528 is $-(255/256)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figure 4.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT\ A}$ and $I_{OUT\ B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT\ A}$ or $I_{OUT\ B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

AC FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.195% of final value for a full scale step.

DIGITAL-TO-ANALOG IMPULSE

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC7528. The current from the $V_{REF\ A}$ pin is switched between $I_{OUT\ A}$ and AGND by 8 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at $V_{REF\ A}$ is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.

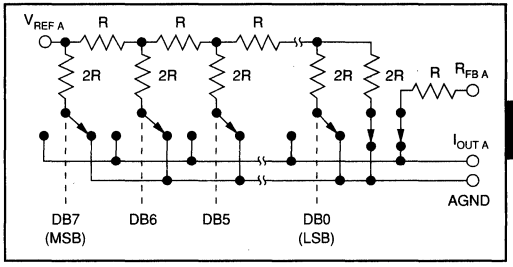


FIGURE 1. Equivalent Circuit for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB\ A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.

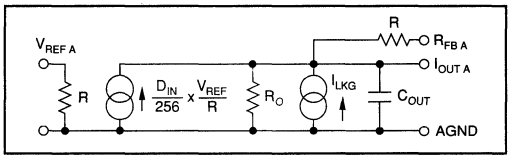


FIGURE 2. Simplified Circuit Diagram for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC7528 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC7528 is designed to operate on V_{DD} = +5V ±10%. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the D/A. AGND and DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pin of the DAC7528 as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC7528 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC7528 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is nonlinear with code, and the largest steps in R_O occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is $2VOS - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good nonlinearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC7528 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

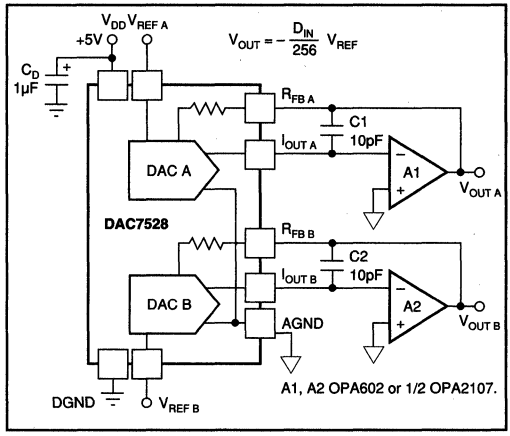


FIGURE 3. Unipolar Configuration 2 Quadrant Multiplication.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC7528 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R1–R3 and R4–R6 should be ratio-matched to 0.195% to ensure the specified gain error performance.

APPLICATION INFORMATION

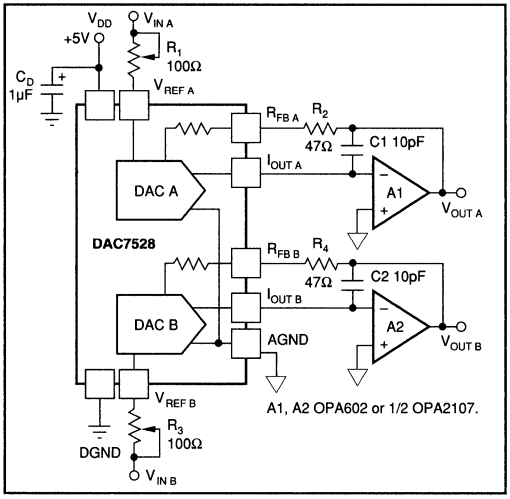


FIGURE 4. Unipolar Configuration with Gain Trim.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (255/256) = $-1/2V_{REF}$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	0V

TABLE I. Unipolar Output Code.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111	$+V_{REF}$ (127/128)
1000 0001	$+V_{REF}$ (1/128)
1000 0000	0V
0111 1111	$-V_{REF}$ (1/128)
0000 0000	$-V_{REF}$ (127/128)

TABLE II. Bipolar Output Code.

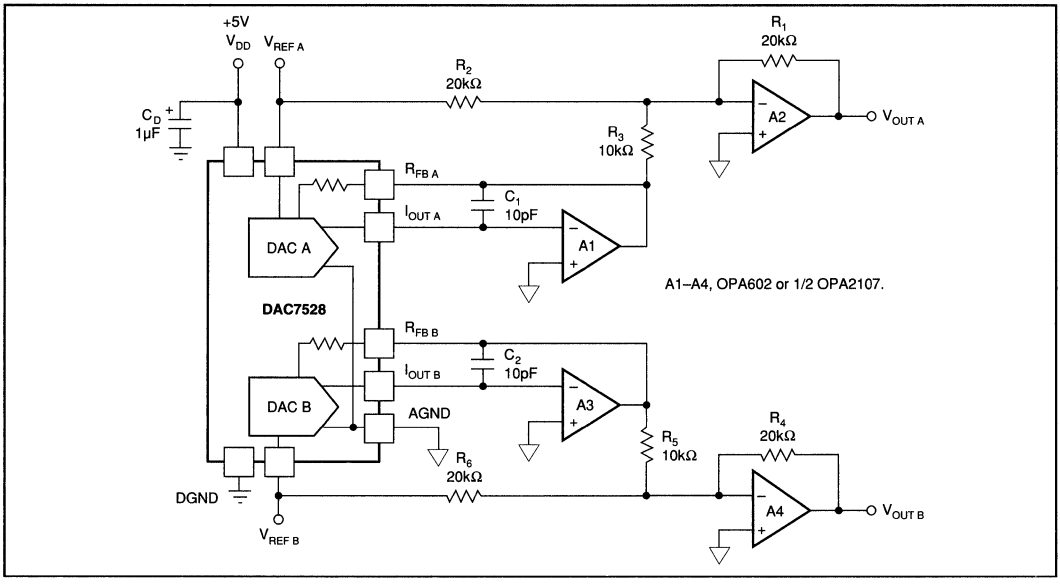
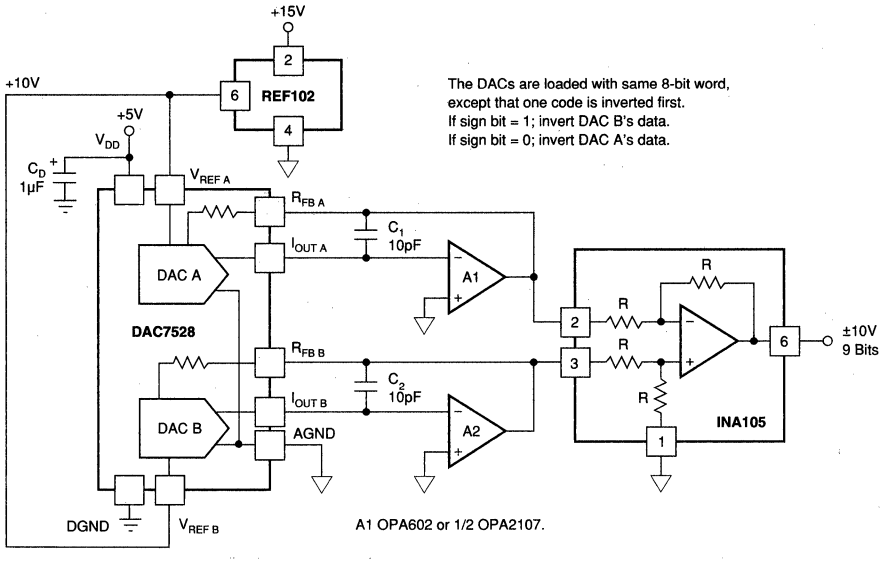


FIGURE 5. Bipolar Configuration 4 Quadrant Multiplication.

APPLICATIONS CIRCUIT: 8-BIT PLUS SIGN DAC



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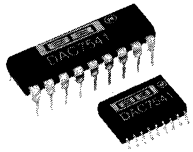


DAC7541A

Low Cost 12-Bit CMOS Four-Quadrant Multiplying DIGITAL-TO-ANALOG CONVERTER

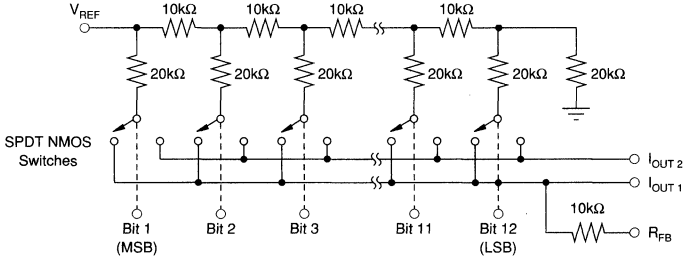
FEATURES

- FULL FOUR-QUADRANT MULTIPLICATION
- 12-BIT END-POINT LINEARITY
- DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- TTL-/CMOS-COMPATIBLE
- SINGLE +5V TO +15V SUPPLY
- LATCH-UP RESISTANT
- 7521/7541/7541A REPLACEMENT
- PACKAGES: Plastic DIP, Plastic SOIC
- LOW COST

DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature range.

DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to a standard 18-pin plastic package, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.



Digital Inputs (DTL-/TTL-/CMOS-compatible)
Logic: A switch is closed to $I_{OUT\,1}$ for its digital input in a "HIGH" state.

Switches shown for digital inputs "HIGH".

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C, $+V_{DD}$ = +12V or +15V, V_{REF} = +10V, $V_{PIN\,1} = V_{PIN\,2}$ = 0V, unless otherwise specified.

PARAMETER	DAC7541A GRADE	DAC7541A T_A = +25°C	DAC7541A $T_A = T_{MAX}, T_{MIN}$[1]	UNITS	TEST CONDITIONS/COMMENTS
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J	±1	±1	LSB max	±1LSB = ±0.024% of FSR.
	K	±1/2	±1/2	LSB max	±1/2LSB = ±0.012% of FSR.
Differential Non-linearity	J	±1	±1	LSB max	All grades guaranteed monotonic to 12 bits,
	K	±1/2	±1/2	LSB max	T_{MIN} to T_{MAX}.
Gain Error	J	±6	±8	LSB max	Measured using internal R_{FB} and includes effect
	K	±1	±3	LSB max	of leakage current and gain T.C.
					Gain error can be trimmed to zero.
Gain Temperature Coefficient					
(ΔGain/ΔTemperature)	ALL		5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current: Out_1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
Out_2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
REFERENCE INPUT					
Voltage (Pin 17 to GND)	All	–10/+10	–10/+10	V min/max	
Input Resistance (Pin 17 to GND)	All	7-18	7-18	kΩ min/max	
					Typical input resistance = 11kΩ.
					Typical input resistance temperature coefficient is –50ppm/°C.
DIGITAL INPUTS					
V_{IN} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	µA max	Logic inputs are MOS gates.
					I_{IN} typ (25°C) = 1nA
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
$\Delta Gain/\Delta V_{DD}$	All	±0.01	±0.02	% per % max	V_{DD} = +11.4V to +16V
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min to V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IN}.
	All	100	500	µA max	All digital inputs 0V or V_{DD}.

NOTES: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions. (2) Guaranteed by design but not production tested.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not production tested.
V_{DD} = +15V, V_{REF} = +10V except where stated, $V_{PIN\,1} = V_{PIN\,2}$ = 0V, output amp is OPA606 except where stated.

PARAMETER	DAC7541A GRADE	DAC7541A T_A = +25°C	DAC7541A $T_A = T_{MAX}, T_{MIN}$[1]	UNITS	TEST CONDITIONS/COMMENTS
PROPAGATION DELAY					
(from Digital Input change to 90% of					Out_1 Load = 100Ω, C_{EXT} = 13pF.
final Analog Output)	All	100	—	ns typ	Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	1000	—	nV-s typ	V_{REF} = 0V, all digital inputs 0V to V_{DD} or V_{DD} to 0V. Measured using OPA606 as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR					
(V_{REF} to Out_1)	All	1.0	—	mVp-p max	V_{REF} = ±10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME					
	All	0.6	—	µs typ	To 0.01% of Full Scale Range.
					Out_1 Load = 100Ω, C_{EXT} = 13pF.
	All	1.0	—	µs max	Digital Inputs: 0V to V_{DD} or V_{DD} to 0V.
OUTPUT CAPACITANCE					
$C_{OUT\,1}$ (Pin 1)	All	100	100	pF max	Digital Inputs = V_{IH}
$C_{OUT\,2}$ (Pin 2)	All	60	60	pF max	Digital Inputs = V_{IH}
$C_{OUT\,1}$ (Pin 1)	All	70	70	pF max	Digital Inputs = V_{IL}
$C_{OUT\,2}$ (Pin 2)	All	100	100	pF max	Digital Inputs = V_{IL}

NOTE: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions.

ABSOLUTE MAXIMUM RATINGS

V_{DD} (Pin 16) to Ground	+17V
V_{REF} (Pin 17) to Ground	+25V
V_{RFB} (Pin 18) to Ground	±25V
Digital Input Voltage (pins 4-15) to Ground	–0.4V, V_{DD}
$V_{PIN\ 1}$, $V_{PIN\ 2}$ to Ground	–0.4V, V_{DD}
Power Dissipation (any package):	
To +75°C	450mW
Derates above +75°C	–6mW/°C
Lead Temperature (soldering, 10s)	+300°C
Storage Temperature: Plastic Package	+125°C

NOTE: Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

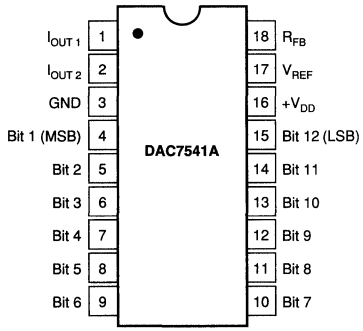
BURN-IN SCREENING

Burn-in screening is an option available for the models in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

PIN CONNECTIONS

Top View — DIP/SOIC



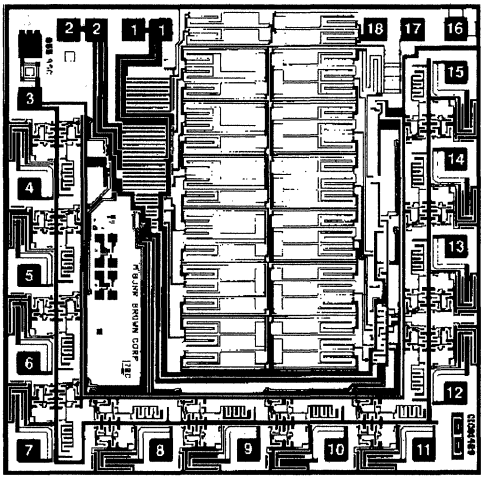
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7541JP	Plastic DIP	218
DAC7541KP	Plastic DIP	218
DAC7541JU	Plastic SOIC	219
DAC7541KU	Plastic SOIC	219
DAC7541JP-BI	Plastic DIP	218
DAC7541KP-BI	Plastic DIP	218

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB)
DAC7541AJP	Plastic DIP	0°C to +70°C	±1	±6
DAC7541AKP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7541AJU	Plastic SOIC	0°C to +70°C	±1	±6
DAC7541AKU	Plastic SOIC	0°C to +70°C	±1/2	±1
BURN-IN SCREENING OPTION See text for details.				
MODEL	**PACKAGE**	**TEMPERATURE RANGE**	**RELATIVE ACCURACY (LSB)**	**BURN-IN TEMP. (160 Hours)[1]**
DAC7541AJP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC7541AKP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C



DIE TOPOLOGY DAC7541A

PAD	FUNCTION	PAD	FUNCTION
1	I_{OUT1}	10	Bit 7
2	I_{OUT2}	11	Bit 8
3	GND	12	Bit 9
4	Bit 1 (MSB)	13	Bit 10
5	Bit 2	14	Bit 11
6	Bit 3	15	Bit 12 (LSB)
7	Bit 4	16	$+V_{DD}$
8	Bit 5	17	V_{REF}
9	Bit 6	18	$R_{FEEDBACK}$

Substrate Bias: Isolated.
NC: No Connection.

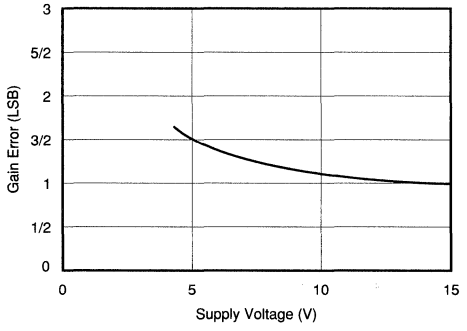
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	104 x 105 ±5	2.64 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

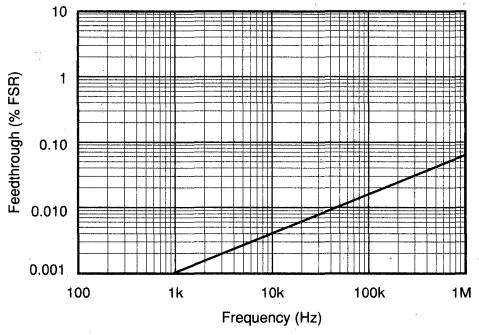
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V, unless otherwise noted.

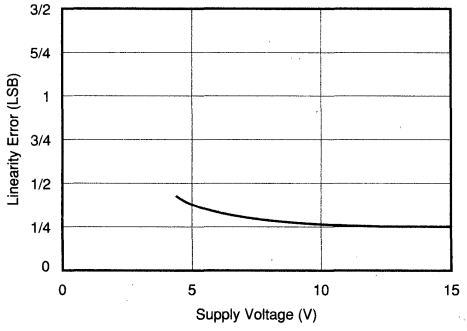
GAIN ERROR vs SUPPLY VOLTAGE



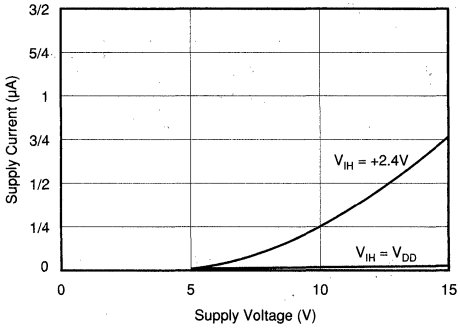
FEEDTHROUGH ERROR vs FREQUENCY



LINEARITY vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line between zero and full scale.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, from one adjacent output state to the next. A differential nonlinearity specification of ±1.0LSB guarantees monotonicity.

GAIN ERROR

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7541A is $-(4095/4096)$ X (V_{REF}). Gain error may be adjusted to zero using external trims.

OUTPUT LEAKAGE CURRENT

The measure of current which appears at Out_1 with the DAC loaded with all zeros, or at Out_2 with the DAC loaded with all ones.

MULTIPLYING FEEDTHROUGH ERROR

This is the AC error output due to capacitive feedthrough from V_{REF} to Out_1 with the DAC loaded with all zeros. This test is performed at 10kHz.

OUTPUT CURRENT SETTLING TIME

This is the time required for the output to settle to a tolerance of ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

PROPAGATION DELAY

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the measure of the area of the glitch energy measured in nV-seconds. Key contributions to glitch energy are digital word-bit timing differences, internal circuitry timing differences, and charge injected from digital logic.

MONOTONICITY

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7541A is guaranteed monotonic to 12 bits.

POWER SUPPLY REJECTION

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

The DAC7541A is a 12-bit multiplying D/A converter consisting of a highly stable thin-film R-2R ladder network and 12 pairs of current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the DAC7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity.

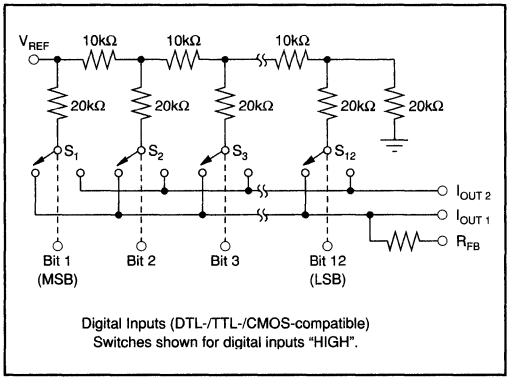


FIGURE 1. Simplified DAC Circuit.

EQUIVALENT CIRCUIT ANALYSIS

Figures 2 and 3 show the equivalent circuits for all digital inputs low and high, respectively. The reference current is switched to $I_{OUT\,2}$ when all inputs are low and $I_{OUT\,1}$ when inputs are high. The I_L current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant one-bit current drain through the ladder terminal.

DYNAMIC PERFORMANCE

Output Impedance

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\,1}$ terminal may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output

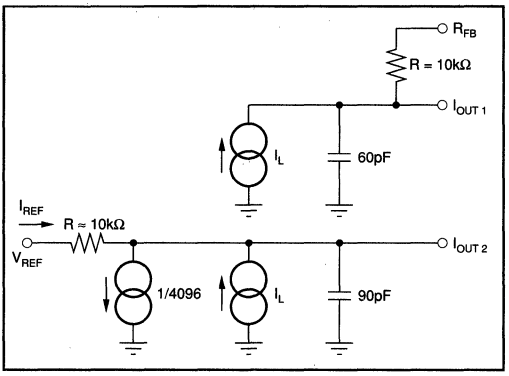


FIGURE 2. DAC7541A Equivalent Circuit (All inputs LOW).

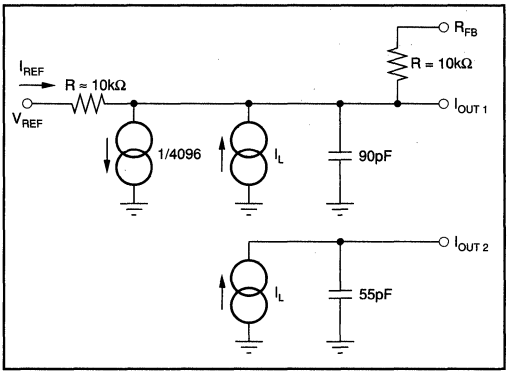


FIGURE 3. DAC7541A Equivalent Circuit (All inputs HIGH).

amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically dampen the output. See Figures 4 and 6.

APPLICATIONS

OP AMP CONSIDERATIONS

The input bias current of the op amp flows through the feedback resistor, creating an error voltage at the output of the op amp. This will show up as an offset through all codes of the transfer characteristics. A low bias current op amp such as the OPA606 is recommended.

Low offset voltage and V_{OS} drift are also important. The output impedance of the DAC is modulated with the digital code. This impedance change (approximately 10kΩ to 30kΩ) is a change in closed-loop gain to the op amp. The result is that V_{OS} will be multiplied by a factor of one to two depending on the code. This shows up as a linearity error. Offset can be adjusted out using Figure 4. Gain may be adjusted using Figure 5.

UNIPOLAR BINARY OPERATION (Two-Quadrant Multiplication)

Figure 4 shows the analog circuit connections required for unipolar binary (two-quadrant multiplication) operation. With a DC reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an AC reference voltage or current, the circuit provides two-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I.

BINARY INPUT	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0V

TABLE I. Unipolar Codes.

C_1 phase compensation (10 to 25pF) in Figure 4 may be required for stability when using high speed amplifiers. C_1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at Out_1.

R_1 in Figure 5 provides full scale trim capability—load the DAC register to 1111 1111 1111, adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096). Alternatively, full scale can be adjusted by omitting R_1 and R_2 and trimming the reference voltage magnitude.

BIPOLAR FOUR-QUADRANT OPERATION

Figure 6 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

BINARY INPUT	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Codes.

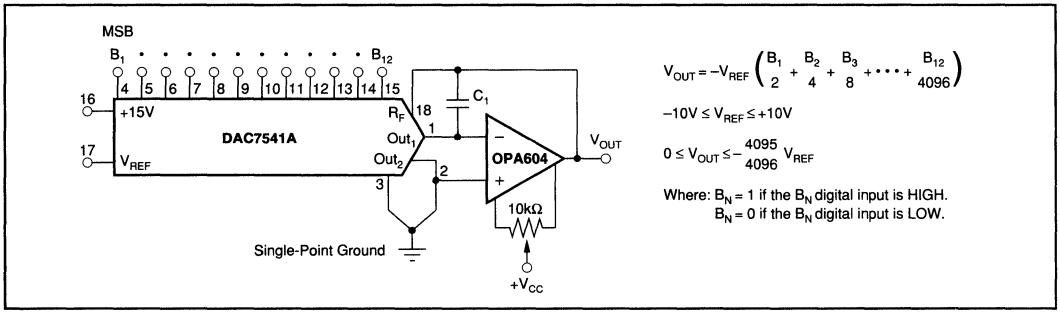


FIGURE 4. Basic Connection With Op Amp V_{OS} Adjust: Unipolar (two-quadrant) Multiplying Configuration.

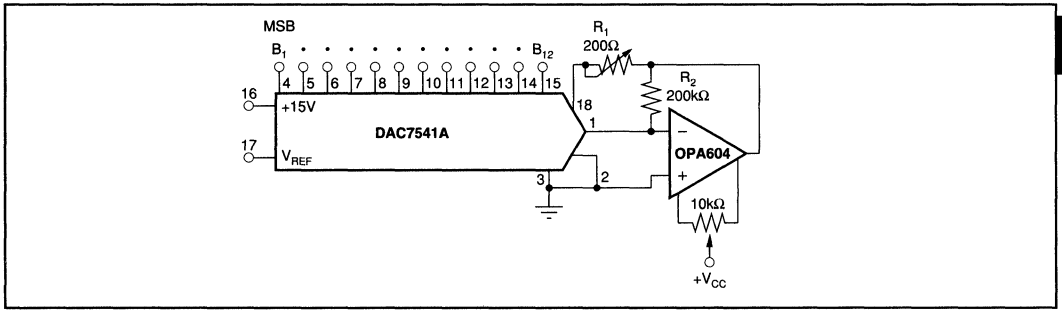


FIGURE 5. Basic Connection With Gain Adjust (allows adjustment up or down).

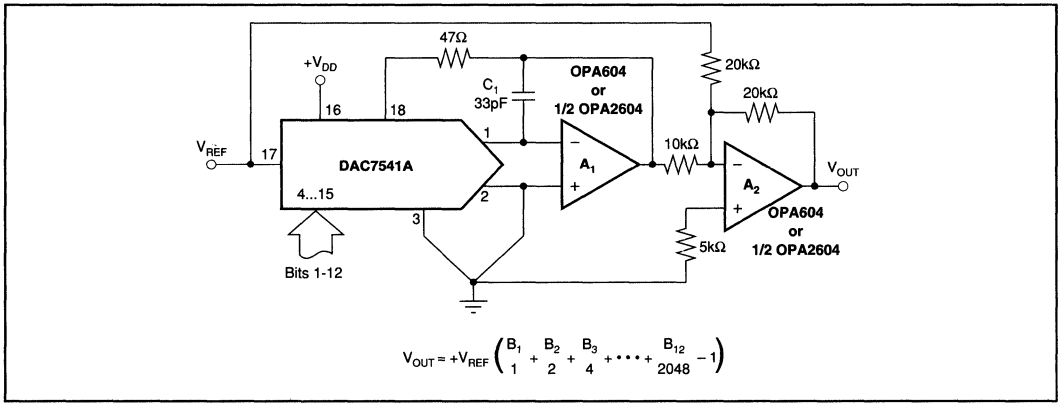


FIGURE 6. Bipolar Four-Quadrant Multiplier.

DIGITALLY CONTROLLED GAIN BLOCK

The DAC7541A may be used in a digitally controlled gain block as shown in Figure 7. This circuit gives a range of gain from one (all bits = one) to 4096 (LSB = one). The transfer function is:

$$V_{OUT} = \frac{-V_{IN}}{\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \bullet\bullet\bullet + \frac{B_{12}}{4096}\right)}$$

All bits off is an illegal state, as division by zero is impossible (no op amp feedback). Also, errors increase as gain increases, and errors are minimized at major carries (only one bit on at a time).

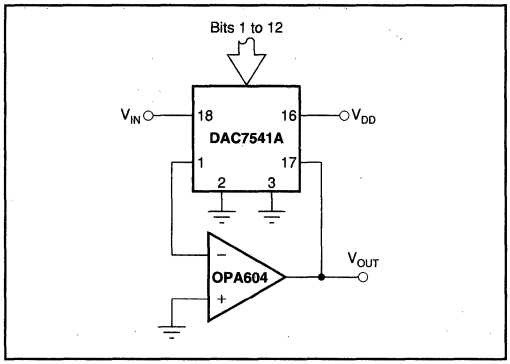


FIGURE 7. Digitally Programmable Gain Block.

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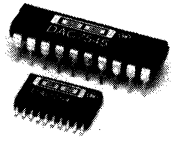


DAC7545

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER Microprocessor Compatible

FEATURES

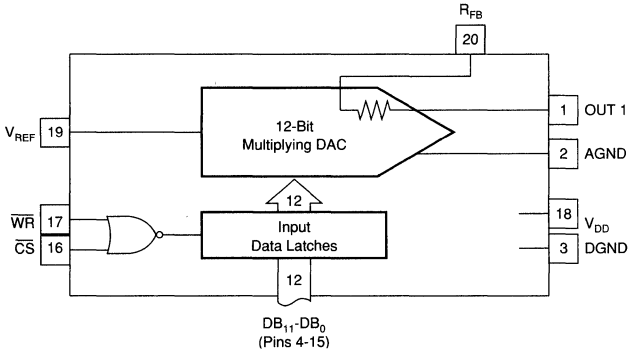
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2ppm/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- TTL/CMOS LOGIC COMPATIBLE
- LOW OUTPUT LEAKAGE: 10nA max
- LOW OUTPUT CAPACITANCE: 70pF max
- DIRECT REPLACEMENT FOR AD7545, PM-7545

DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin plastic DIP or 20-lead plastic SOIC packages. Devices are specified over the commercial.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and V_{DD} = +5V.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM, unless otherwise specified.

PARAMETER	GRADE	DAC7545 V_{DD} = +5V T_A = +25°C	DAC7545 V_{DD} = +5V T_{MAX}-T_{MIN}[1]	DAC7545 V_{DD} = +15V T_A = +25°C	DAC7545 V_{DD} = +15V T_{MAX}-T_{MIN}[1]	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Accuracy	J	±2	±2	±2	±2	LSB	
	K	±1	±1	±1	±1	LSB	
	L	±1/2	±1/2	±1/2	±1/2	LSB	
	GL	±1/2	±1/2	±1/2	±1/2	LSB	
Differential Nonlinearity	J	±4	±4	±4	±4	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	K	±1	±1	±1	±1	LSB	10-Bit Monotonic, T_{MIN} to T_{MAX}
	L	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
	GL	±1	±1	±1	±1	LSB	12-Bit Monotonic, T_{MIN} to T_{MAX}
Gain Error (with internal R_{FB})[2]	J	±20	±20	±25	±25	LSB	D/A register loaded with FFF_H.
	K	±10	±10	±15	±15	LSB	Gain error is adjustable using
	L	±5	±6	±10	±10	LSB	the circuits in Figures 2 and 3.
	GL	±1	±2	±6	±7	LSB	
Gain Temperature Coefficient[3] (ΔGain/ΔTemperature)	All	±5	±5	±10	±10	ppm/°C for V_{DD} = +5	Typical value is 2ppm/°C
DC Supply Rejection[3] (ΔGain/ΔV_{DD})	All	0.015	0.03	0.01	0.02	%/%	ΔV_{DD} ±5%
Output Leakage Current at Out 1	J, K, L, GL	10	50	10	50	nA	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	µs	To 1/2LSB. Out_1 Load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V
Propagation Delay[3] (from digital input change to 90% of final analog output)	All	300		250		ns	Out_1 Load = 100Ω. C_{EXT} = 13pF[4]
Glitch Energy	All	400		250		nV-s[5]	V_{REF} = ACOM
AC Feedback at I_{OUT} 1	All	5	5	5	5	mVp-p[5]	V_{REF} = ±10V, 10kHz Sine Wave
REFERENCE INPUT							
Input Resistance (pin 19 to AGND)	All	7	7	7	7	kΩ[6]	Input resistance TC = 300ppm/°C[5]
		25	25	25	25	kΩ	
AC OUTPUTS							
Output Capacitance[3]: $C_{OUT\,1}$	All	70	70	70	70	pF	DB_0-DB_{11} = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
$C_{OUT\,2}$	All	200	200	200	200	pF	DB_0-DB_{11} = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	13.5	13.5	V[6]	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	1.5	1.5	V	
I_{IN} (Input Current)[7]	All	±1	±10	±1	±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[3]: DB_0-DB_{11}	All	5	5	5	5	pF	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF	V_{IN} = 0V
SWITCHING CHARACTERISTICS[8]							
Chip Select to Write Setup Time, t_{CS}	All	280	380	180	200	ns[6]	See Timing Diagram
		200	270	120	150	ns[5]	
Chip Select to Write Hold Time, t_{CH}	All	0	0	0	0	ns[6]	
Write Pulse Width, t_{WR}	All	250	400	160	240	ns[6]	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns[5]	
Data Setup Time, t_{DS}	All	140	210	90	120	ns[6]	
		100	150	60	80	ns[5]	
Data Hold Time, t_{DH}	All	10	10	10	10	ns[6]	
POWER SUPPLY, I_{DD}							
	All	2	2	2	2	mA	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	µA	All Digital Inputs 0V or V_{DD}
	All	10	10	10	10	µA[5]	All Digital Inputs 0V or V_{DD}

NOTES: (1) Temperature ranges—J, K, L, GL: 0°C to +70°C. (2) This includes the effect of 5ppm max, gain TC. (3) Guaranteed but not tested. (4) DB_0-DB_{11} = 0V to V_{DD} or V_{DD} to 0V. (5) Typical. (6) Minimum. (7) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA. (8) Sample tested at +25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise noted.

V_{DD} to DGND	–0.3V, +17
Digital Input to DGND	–0.3V, V_{DD}
V_{RFB}, V_{REF}, to DGND	±25V
$V_{PIN\ 1}$ to DGND	–0.3V, V_{DD}
AGND to DGND	–0.3V, V_{DD}
Power Dissipation: Any Package to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature:	
Commercial J, K, L, GL	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

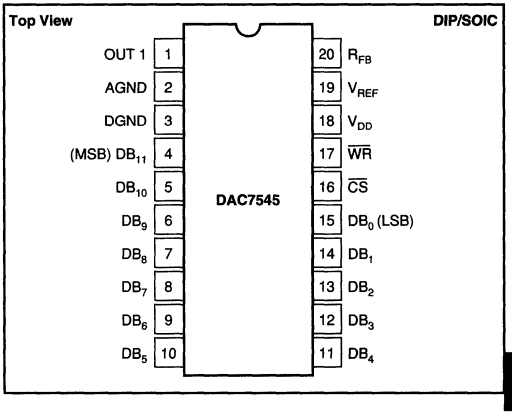
NOTE: Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONNECTIONS



PACKAGE INFORMATION

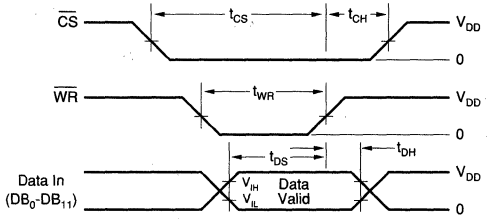
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7545JP	20-Pin PDIP	222
DAC7545KP	20-Pin PDIP	222
DAC7545LP	20-Pin PDIP	222
DAC7545GLP	20-Pin PDIP	222
DAC7545JU	20-Pin SOIC	221
DAC7545KU	20-Pin SOIC	221
DAC7545LU	20-Pin SOIC	221
DAC7545GLU	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

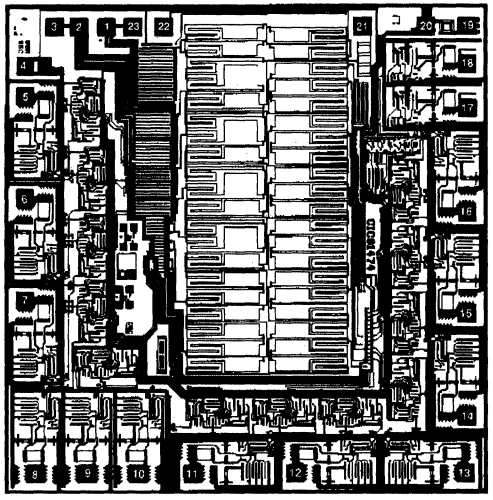
MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB) V_{DD} = +5V
DAC7545JP	Plastic DIP	0°C to +70°C	±2	±20
DAC7545KP	Plastic DIP	0°C to +70°C	±1	±10
DAC7545LP	Plastic DIP	0°C to +70°C	±1/2	±5
DAC7545GLP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7545JU	Plastic SOIC	0°C to +70°C	±2	±20
DAC7545KU	Plastic SOIC	0°C to +70°C	±1	±10
DAC7545LU	Plastic SOIC	0°C to +70°C	±1/2	±5
DAC7545GLU	Plastic SOIC	0°C to +70°C	±1/2	±1

WRITE CYCLE TIMING DIAGRAM



Mode Selection	
Write Mode	**Hold Mode**
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to Data Bus (DB_0-DB_{11}) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB_0-DB_{11}) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES: V_{DD} = +5V, $t_R = t_F$ = 20ns. V_{DD} = +15V, $t_R = t_F$ = 40ns. All inputs signal rise and fall times measured from 10% to 90% of V_{DD}. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.



DAC7545 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	OUT 1	13	DB_3
2	AGND	14	DB_2
3	AGND	15	DB_1 (LSB)
4	DGND	16	DB_0
5	DB11	17	$\overline{CS}$
6	DB10	18	$\overline{WR}$
7	DB9	19	$\overline{XYR}$
8	DB8	20	V_{DD}
9	DB7	21	V_{REF}
10	DB6	22	R_{FB}
11	DB_5	23	OUT_1
12	DB_4		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	136 x 134 ±5	3.45 x 3.40 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as end point linearity) describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale have been adjusted.

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7545 is $-(4095/4096)(V_{REF})$. Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The current which appears at OUT 1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error

The AC output error due to capacitive feedthrough from V_{REF} to OUT 1 with the DAC loaded with all zeros. This test is performed using a 10kHz sine wave.

Output Current Settling Time

The time required for the output to settle within ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

The delay of the internal circuitry is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-to-Analog Glitch Impulse

The area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND and an OPA600 as the output op amp and G_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7545 is guaranteed monotonic to 12 bits, except the J grade is specified to be 10-bit monotonic.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of the digital-to-analog converter portion of the DAC7545. The current from the V_{REF} pin is switched from OUT 1 to AGND by the FET switch. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.

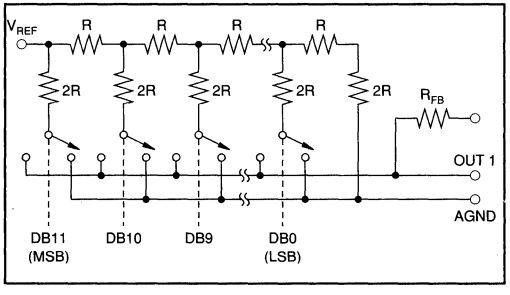


FIGURE 1. Simplified DAC Circuit of the DAC7545.

The output capacitance of the DAC7545 is code dependent and varies from a minimum value (70pF) at code 000H to a maximum (200pF) at code FFFH.

The input buffers are CMOS inverters, designed so that when the DAC7545 is operated from a 5V supply (V_{DD}), the logic threshold is TTL-compatible. Being simple CMOS inverters, there is a range of operation where the inverters operate in the linear region and thus draw more supply current than normal. Minimizing this transition time through the linear region and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

UNIPOLAR OPERATION

Figure 2 shows the DAC7545 connected for unipolar operation. The high-grade DAC7545 is specified for a 1LSB gain error, so gain adjust is typically not needed. However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC7545JP, the gain error is specified to be ±25LSB. A range of adjustment of ±37LSB will be adequate. The equation below results in a value of 458Ω for the potentiometer (use 500Ω).

$$R_1 = \frac{R_{LADDER}}{4096} (3 \times \text{Gain Error})$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 2 may be used with input voltages up to ±20V as long as the output amplifier is biased to handle the excursions. Table I represents the analog output for four codes into the DAC for Figure 2.

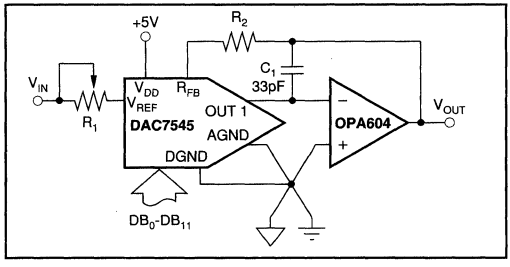


FIGURE 2. Unipolar Binary Operation.

BINARY CODE	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 V

TABLE I. Unipolar Codes.

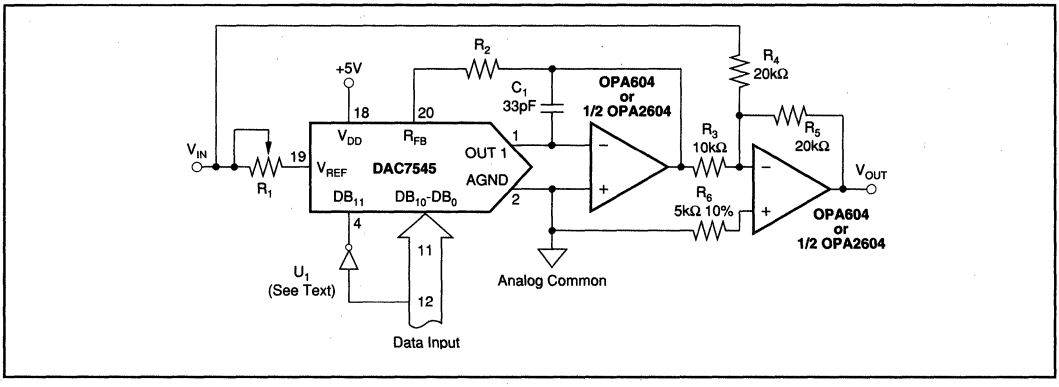


FIGURE 3. Bipolar Operation (Two's Complement Code).

BIPOLAR OPERATION

Figure 3 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter, U_1, on the MSB line converts two's complement input code to offset binary code. If the inversion is done in software, U_1 may be omitted.

R_3, R_4, and R_5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R_3 value to R_4 causes both offset and full-scale error. Mismatch of R_5 to R_4 and R_3 causes full-scale error.

DATA INPUT	ANALOG OUTPUT
MSB LSB	
0111 1111 1111	$+V_{IN}$ (2047/2048)
0000 0000 0001	$+V_{IN}$ (1/2048)
0000 0000 0000	0 V
1111 1111 1111	$-V_{IN}$ (1/2048)
1000 0000 0000	$-V_{IN}$ (2048/2048)

TABLE II. Two's Complement Code Table for Circuit of Figure 3.

DIGITALLY CONTROLLED GAIN BLOCK

Figure 4 shows a circuit for digitally controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC7545. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback, and a saturated op amp output.

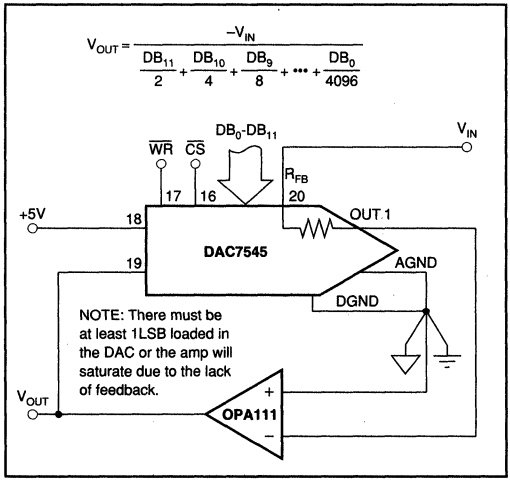


FIGURE 4. Digitally Controlled Gain Block.

APPLICATIONS HINTS

CMOS DACs, such as the DAC7545, exhibit a code-dependent out resistance. The effect of this is a code-dependent differential nonlinearity at the amplifier output which depends on the offset voltage, V_{OS}, of the amplifier. Thus linearity depends upon the potential of OUT 1 and AGND being exactly equal to each other. Usually the DAC is connected to an external op amp with its noninverting input connected to AGND. The op amp selected should have a low input bias current and low V_{OS} and V_{OS} drift over temperature. The op amp offset voltage should be less than $(25 \times 10^{-6})(V_{REF})$ over operating conditions. Suitable op amps are the Burr-Brown OPA37 and the OPA627 for fixed reference applications and low bandwidth requirement. The OPA37 has low V_{OS} and will not require an offset trim. For wide bandwidth, high slew rate, or fast settling applications, the Burr-Brown OPA604 or 1/2 OPA2604 are recommended.

Unused digital inputs should be connected to V_{DD} or to DGND. This prevents noise form triggering the high impedance digital input. It is suggested that the unused digital inputs also be given a path to ground or V_{DD} through a 1MΩ resistor to prevent the accumulation of static charge if the PC card is unplugged from the system. In addition, in systems where the AGND to DGND connection is on a backplane, it is recommended that two diodes be connected in inverse parallel between AGND and DGND.

INTERFACING TO MICROPROCESSORS

The DAC7545 can be directly interfaced to either an 8- or 16-bit microprocessor through its 12-bit wide data latch using the $\overline{CS}$ and $\overline{WR}$ controls.

An 8-bit processor interface is shown in Figure 5. It uses two memory addresses, one for the lower 8 bits and one for the upper 4 bits of data into the DAC via the latch.

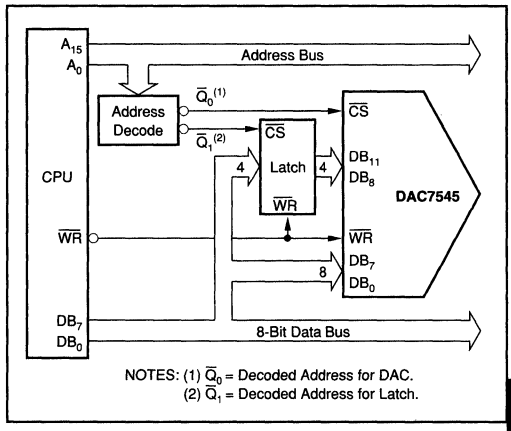


FIGURE 5. 8-Bit Processor Interface.

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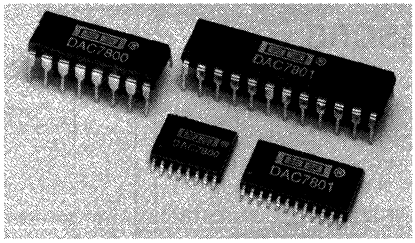


DAC7800
DAC7801
DAC7802

Dual Monolithic CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- TWO D/As IN A 0.3" WIDE PACKAGE
- SINGLE +5V SUPPLY
- HIGH SPEED DIGITAL INTERFACE:
  Serial—DAC7800
  8 + 4-Bit Parallel—DAC7801
  12-Bit Parallel—DAC7802
- MONOTONIC OVER TEMPERATURE
- LOW CROSSTALK: –94dB min
- FULLY SPECIFIED OVER –40°C TO +85°C

APPLICATIONS

- PROCESS CONTROL OUTPUTS
- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN CIRCUITS
- AUTO-CALIBRATION CIRCUITS

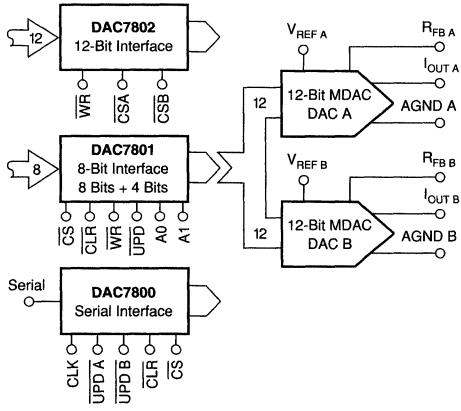
DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of –40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each D/A separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single D/A register for each D/A. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{DD} = +5VDC, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, T_A = –40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7800/7801/7802K			DAC7800/7801/7802L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Resolution		12			*			Bits
Relative Accuracy				±1			±1/2	LSB
Differential Nonlinearity				±1			*	LSB
Gain Error	Measured Using $R_{FB\ A}$ and $R_{FB\ B}$. All Registers Loaded with All 1s.			±3			±1	LSB
Gain Temperature Coefficient[1]			2	5		*	*	ppm/°C
Output Leakage Current	T_A = +25°C		0.005	10		*	*	nA
	T_A = –40°C to +85°C		3	150		*	*	nA
REFERENCE INPUT								
Input Resistance		6	10	14	*	*	*	kΩ
Input Resistance Match			0.5	3		*	2	%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)		2			*			V
V_{IL} (Input Low Voltage)				0.8			*	V
I_{IN} (Input Current)	T_A = +25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8	10		*	*	pF
POWER SUPPLY								
V_{DD}		4.5		5.5	*		*	V
I_{DD}			0.2	2		*	*	mA
Power Supply Rejection	V_{DD} from 4.5V to 5.5V			0.002			*	%/%

* Same specification as for DAC7800/7801/7802K.

AC PERFORMANCE

OUTPUT OP AMP IS OPA602.

At V_{DD} = +5VDC, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, T_A = +25°C unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7800/7801/7802K			DAC7800/7801/7802L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CURRENT SETTLING TIME	To 0.01% of Full Scale R_L = 100Ω, C_L = 13pF		0.4	0.8		*	*	µs
DIGITAL-TO-ANALOG GLITCH IMPULSE	$V_{REF\ A}$ = $V_{REF\ B}$ = 0V R_L = 100Ω, C_L = 13pF		0.9			*		nV-s
AC FEEDTHROUGH	f_{VREF} = 10kHz		–75	–72		*	*	dB
OUTPUT CAPACITANCE	DAC Loaded with All 0s		30	50		*	*	pF
	DAC Loaded with All 1s		70	100		*	*	pF
CHANNEL-TO-CHANNEL ISOLATION								
$V_{REF\ A}$ to $I_{OUT\ B}$	$f_{VREF\ A}$ = 10kHz $V_{REF\ B}$ = 0V, Both DACs Loaded with 1s	–90	–94		*	*		dB
$V_{REF\ B}$ to $I_{OUT\ A}$	$f_{VREF\ B}$ = 10kHz $V_{REF\ A}$ = 0V, Both DACs Loaded with 1s	–90	–101		*	*		dB
DIGITAL CROSSTALK	Full Scale Transition R_L = 100Ω, C_L = 13pF		0.9			*		nV-s

NOTE: (1) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

At T_A = +25°C unless otherwise noted.

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	–0.3, V_{DD}
Digital Input to DGND	–0.3, V_{DD} + 0.3
$V_{REF\ A}$, $V_{REF\ B}$ to AGND	±25V
$V_{REF\ A}$, $V_{REF\ B}$ to DGND	±25V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND	–0.3, V_{DD}
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7800KP	16-Pin PDIP	180
DAC7800LP	16-Pin PDIP	180
DAC7800KU	16-Pin SOIC	211
DAC7800LU	16-Pin SOIC	211
DAC7801KP	24-Pin DIP	243
DAC7801LP	24-Pin DIP	243
DAC7801KU	24-Pin SOIC	239
DAC7801LU	24-Pin SOIC	239
DAC7802KP	24-Pin DIP	243-3
DAC7802LP	24-Pin DIP	243-3
DAC7802KU	24-Pin SOIC	239
DAC7802LU	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure.

Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

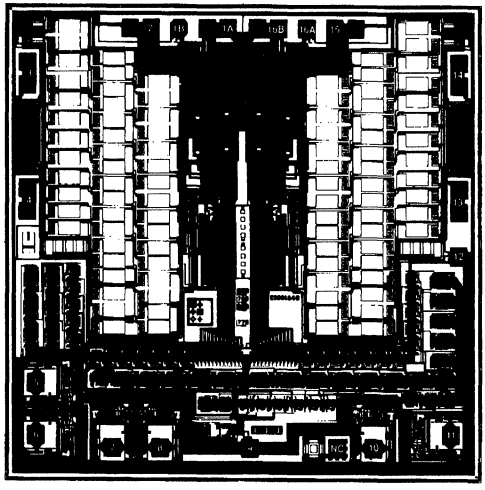
Digital Inputs: All digital inputs of the DAC780X family incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. AGND, I_{OUT}, and R_{FB} show some sensitivity. Failure to observe ESD handling procedures could result in catastrophic device failure.

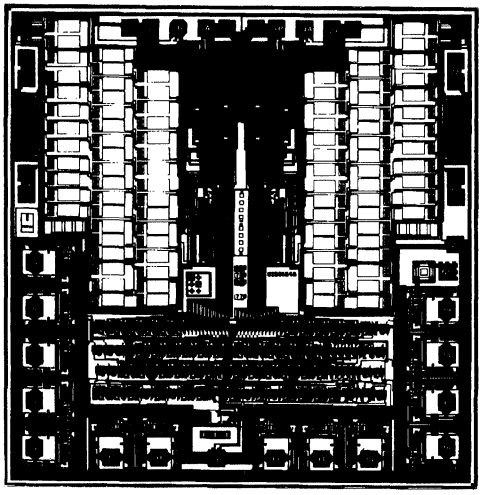
ORDERING INFORMATION

MODEL	RELATIVE ACCURACY	GAIN ERROR	PACKAGE
DAC7800KP	±1LSB	±3LSB	16-Pin DIP
DAC7800KU			16-Lead SO
DAC7800LP	±1/2LSB	±1LSB	16-Pin DIP
DAC7800LU			16-Lead SO
DAC7801KP	±1LSB	±3LSB	24-Pin DIP
DAC7801KU			24-Lead SO
DAC7801LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7801LU			24-Lead SO
DAC7802KP	±1LSB	±3LSB	24-Pin DIP
DAC7802KU[1]			24-Lead SO
DAC7802LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7802LU			24-Lead SO

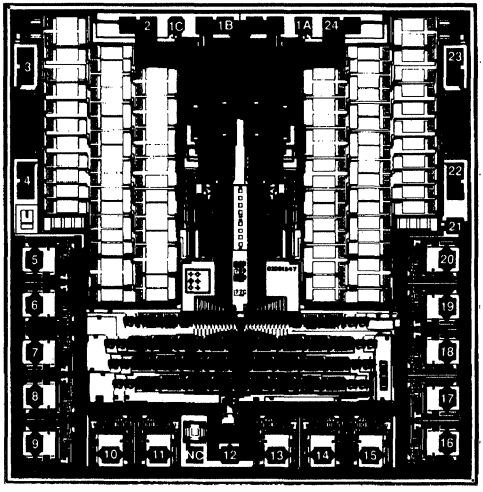
DICE INFORMATION



DAC7800 DIE TOPOGRAPHY



DAC7801 DIE TOPOGRAPHY



DAC7802 DIE TOPOGRAPHY

MECHANICAL INFORMATION

DAC7800	MILS (0.001")	MILLIMETERS
Die Size	131 x 136 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

Substrate Bias: $+V_{DD}$

DAC7801	MILS (0.001")	MILLIMETERS
Die Size	131 x 134 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metallization		Aluminum

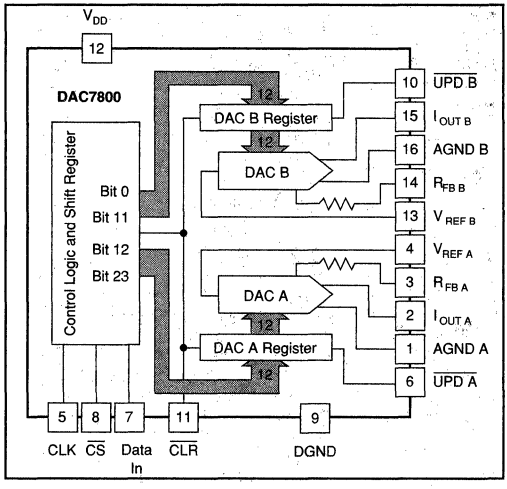
Substrate Bias: $+V_{DD}$

DAC7802	MILS (0.001")	MILLIMETERS
Die Size	131 x 121 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

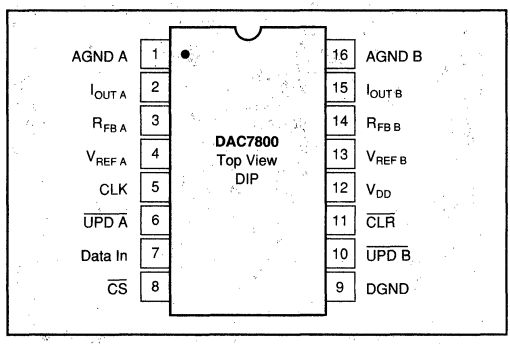
Substrate Bias: $+V_{DD}$

DAC7800

BLOCK DIAGRAM



PIN CONFIGURATION

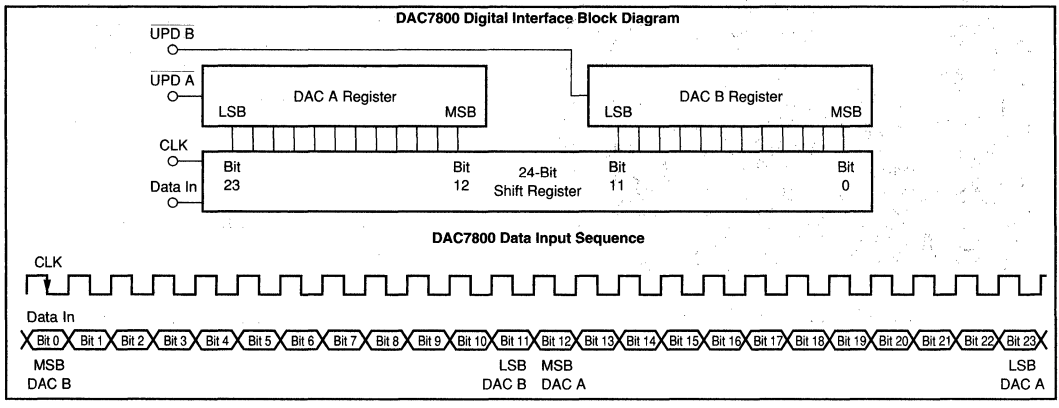


LOGIC TRUTH TABLE

CLK	UPD A	UPD B	CS	CLR	FUNCTION
X	X	X	X	0	All register contents set to 0's (asynchronous).
X	X	X	1	X	No data transfer.
↓	X	X	0	1	Input data is clocked into input register (location Bit 23) and previous data shifts.
X	0	1	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A.
X	1	0	0	1	Input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.
X	0	0	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A, and input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.

X = Don't care. ↓ means falling edge triggered.

DATA INPUT FORMAT

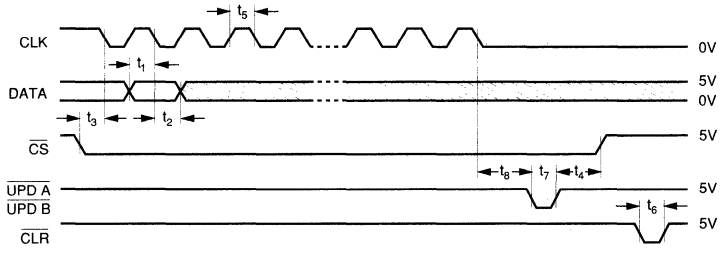


DAC7800 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = –40°C to +85°C.

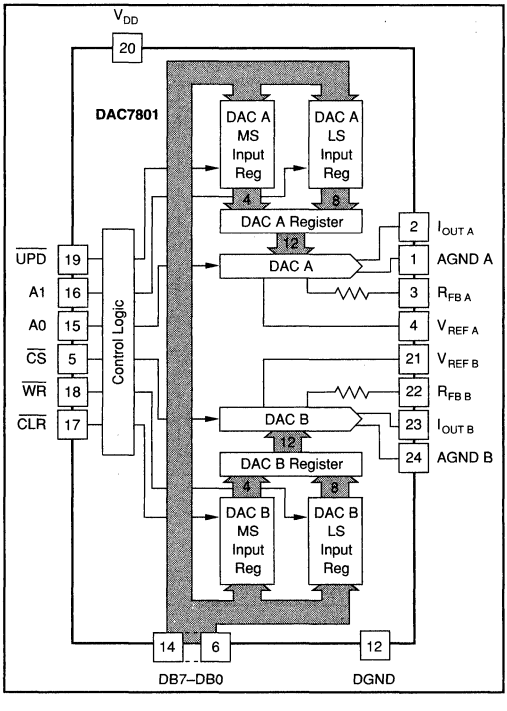
PARAMETER	MINIMUM
t_1 — Data Setup Time	15ns
t_2 — Data Hold Time	15ns
t_3 — Chip Select to CLK, Update, Data Setup Time	15ns
t_4 — Chip Select to CLK, Update, Data Hold Time	40ns
t_5 — CLK Pulse Width	40ns
t_6 — Clear Pulse Width	40ns
t_7 — Update Pulse Width	40ns
t_8 — CLK Edge to $\overline{UPD\ A}$ or $\overline{UPD\ B}$	15ns



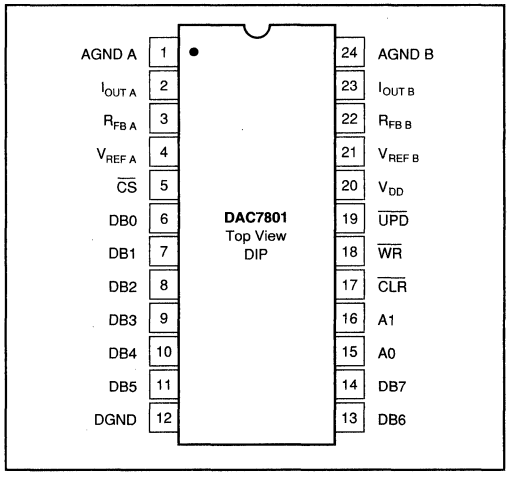
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. t_R = t_F = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7801

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)–DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)–DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

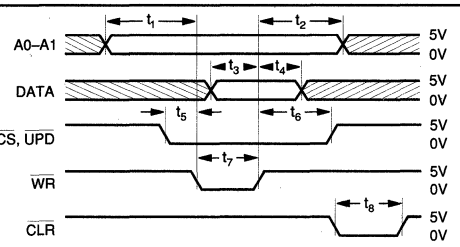
X = Don't care.

DAC7801 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10V, T_A = –40°C to +85°C.

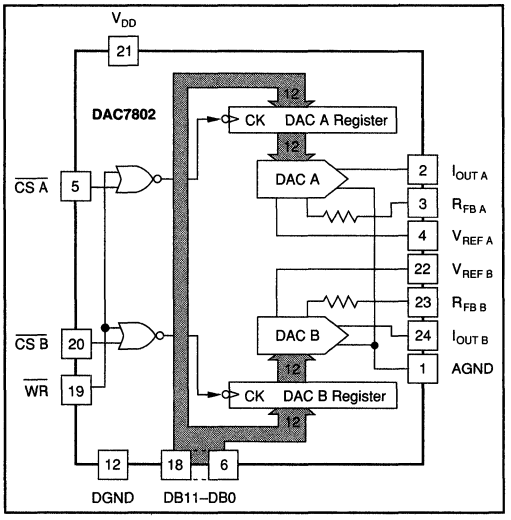
PARAMETER	MINIMUM
t_1 — Address Valid to Write Setup Time	10ns
t_2 — Address Valid to Write Hold Time	10ns
t_3 — Data Setup Time	30ns
t_4 — Data Hold Time	10ns
t_5 — Chip Select or Update to Write Setup Time	0ns
t_6 — Chip Select or Update to Write Hold Time	0ns
t_7 — Write Pulse Width	40ns
t_8 — Clear Pulse Width	40ns



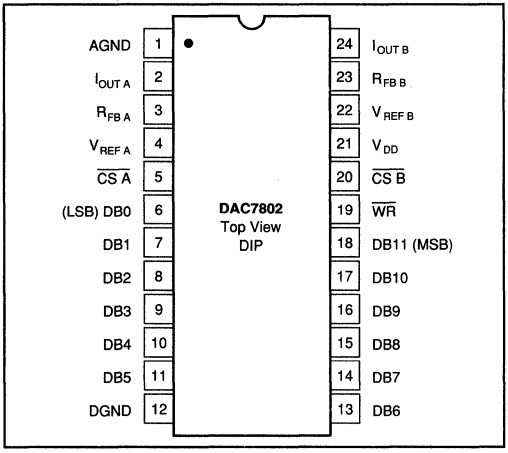
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. t_R = t_F = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7802

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

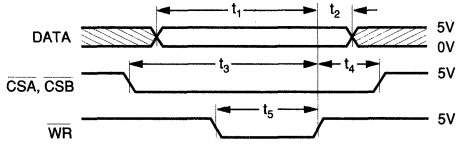
$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

X = Don't care. ↓ means rising edge triggered.

TIMING CHARACTERISTICS

At V_{DD} = +5V, and T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1 - Data Setup Time	20ns
t_2 - Data Hold Time	15ns
t_3 - Chip Select to Write Setup Time	30ns
t_4 - Chip Select to Write Hold Time	0ns
t_5 - Write Pulse Width	30ns

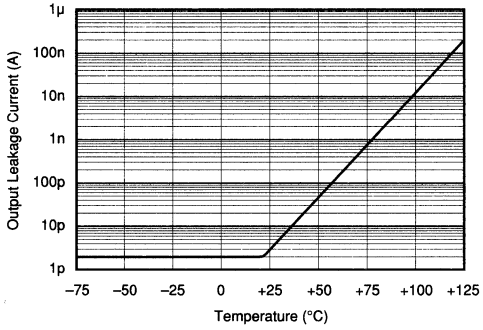


NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. t_R = t_F = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

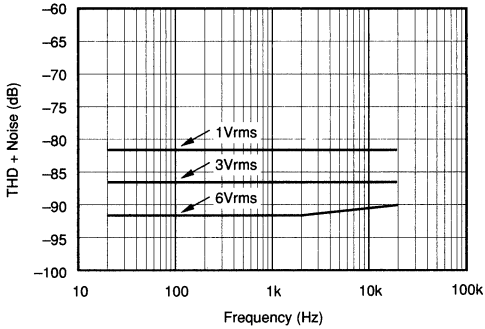
TYPICAL PERFORMANCE CURVES

OUTPUT OP AMP IS OPA602.
T_A = +25°C, V_{DD} = +5V.

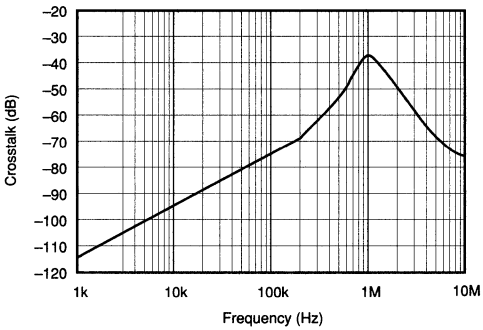
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



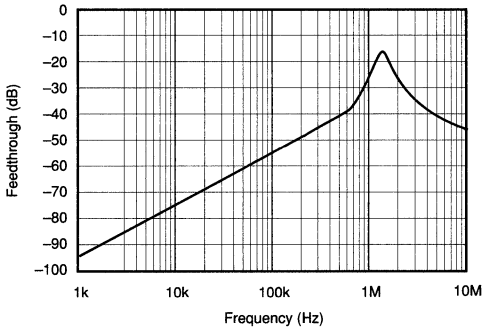
THD + NOISE vs FREQUENCY



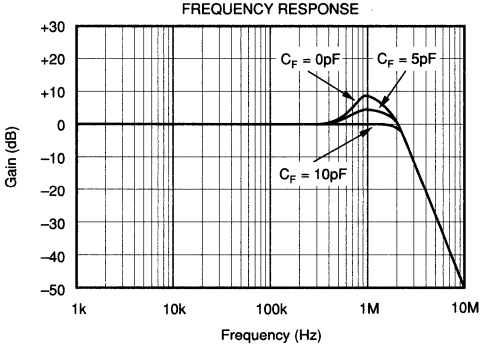
CHANNEL-TO-CHANNEL ISOLATION vs FREQUENCY



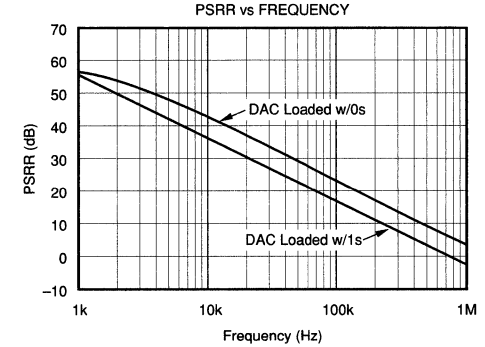
FEEDTHROUGH vs FREQUENCY



FREQUENCY RESPONSE



PSRR vs FREQUENCY



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC780X is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figures 5 and 7.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT\,A}$ and $I_{OUT\,B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT\,A}$ or $I_{OUT\,B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.01% of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC780X. The current from the $V_{REF\,A}$ pin is switched between $I_{OUT\,A}$ and AGND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.

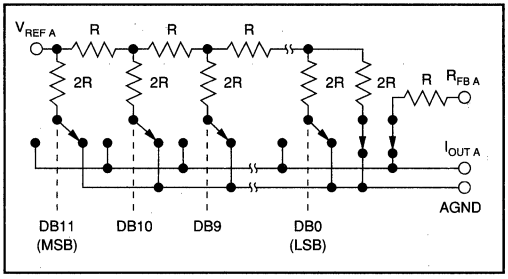


FIGURE 1. Simplified Circuit Diagram for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB\,A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.

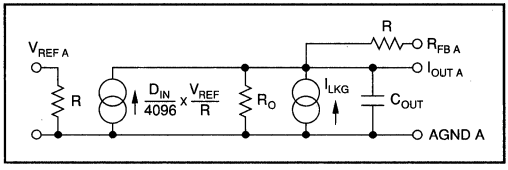


FIGURE 2. Equivalent Circuit for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC780X incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC780X are designed to operate on $V_{DD} = +5V \pm 10\%$. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the D/A. AGND and

DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pins of the DAC780X as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC780X directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC780X should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is nonlinear with code, and the largest steps in R_O occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good nonlinearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC780X in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC780X in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table III.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE II. Unipolar Output Code.

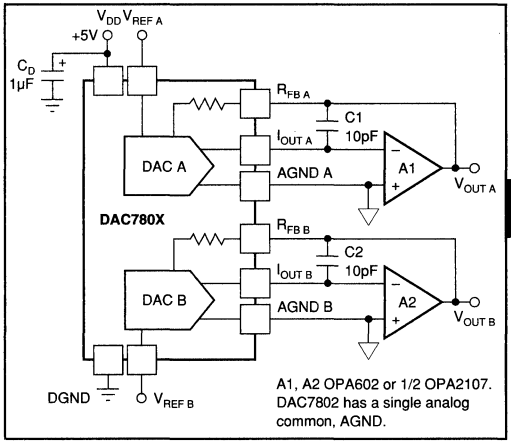


FIGURE 3. Unipolar Configuration.

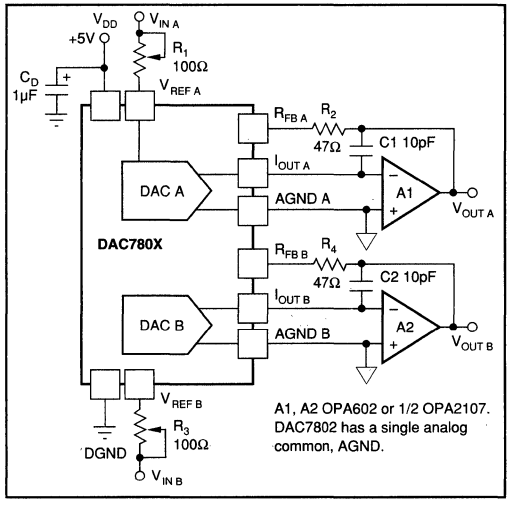


FIGURE 4. Unipolar Configuration with Gain Trim.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R5–R7 and R8–R10 should be ratio-matched to 0.01% to ensure the specified gain error performance.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 6 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE III. Bipolar Output Code.

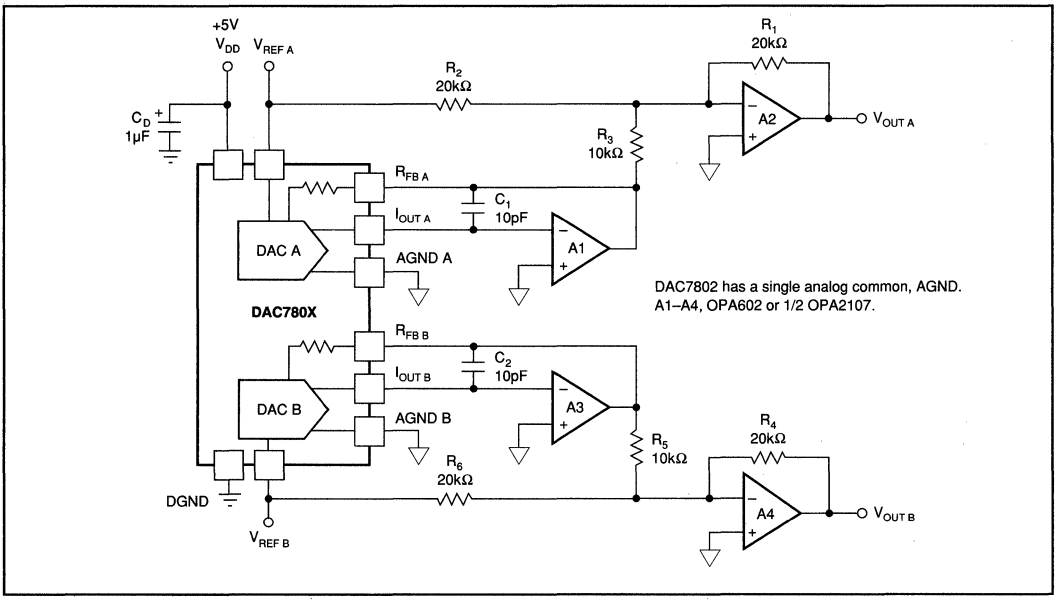


FIGURE 5. Bipolar Configuration.

APPLICATIONS

12-BIT PLUS SIGN DACS

For a bipolar DAC with 13 bits of resolution, two solutions are possible. As shown in Figure 7, the addition of a precision difference amplifier and a high speed JFET switch provides a 12-bit plus sign voltage-output DAC. When the switch selects the op amp output, the difference amplifier serves as a non-inverting output buffer. If the analog ground side of the switch is selected, the output of the difference amplifier is inverted.

Another option, shown in Figure 8, also produces a 12-bit plus sign output without the additional switch and digital control line.

DIGITALLY PROGRAMMABLE ACTIVE FILTER

DAC780X are shown in Figure 9 in a digitally programmable active filter application. The design is based on the state-variable filter, Burr-Brown UAF42, an active filter topology that offers stable and repeatable filter characteristics.

DAC1 and DAC2 can be updated in parallel with a single word to set the center frequency of the filter. DAC 4, which makes use of the uncommitted op amp in UAF42, sets the Q of the filter. DAC3 sets the gain of the filter transfer function without changing the Q of the filter. The reverse is also true.

The center frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance of the D/A (typical value, 10kΩ) and C the internal capacitor value (1000pF) of the UAF42. External capacitors can be added to lower the center frequency of the filter. But the highest center frequency for this circuit will be about 16kHz because the effective series resistance of the D/A cannot be less than 10kΩ.

Note that the ladder resistance of the D/A may vary from device to device. Thus, for best tracking, DAC2 and DAC3 should be in the same package. Some calibration may be necessary from one filter to another.

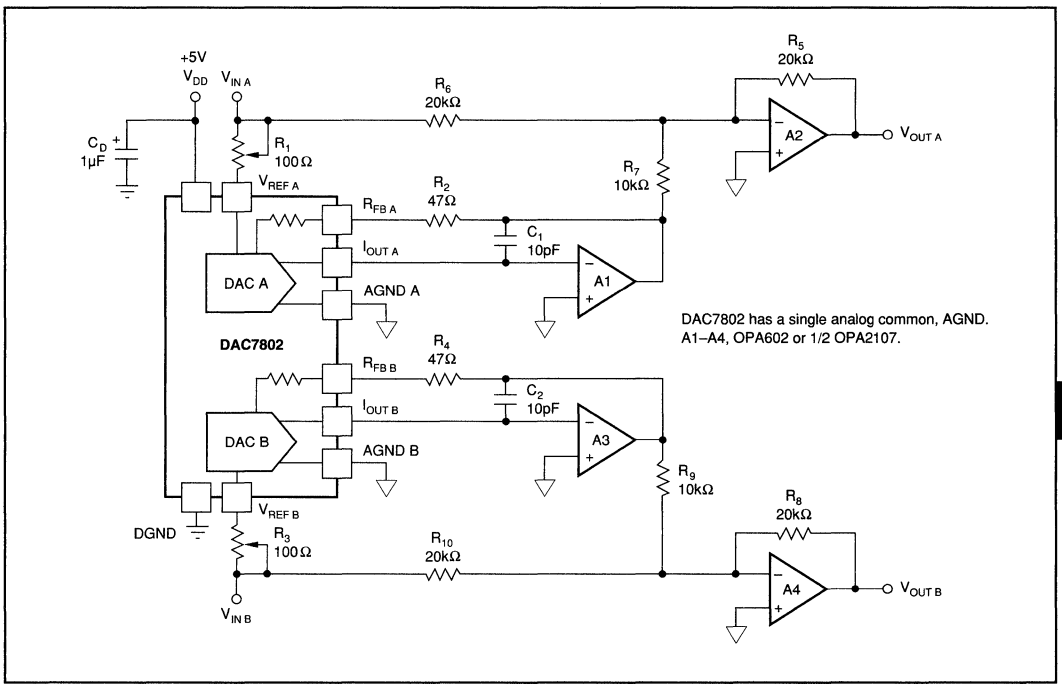


FIGURE 6. Bipolar Configuration with Gain Trim.

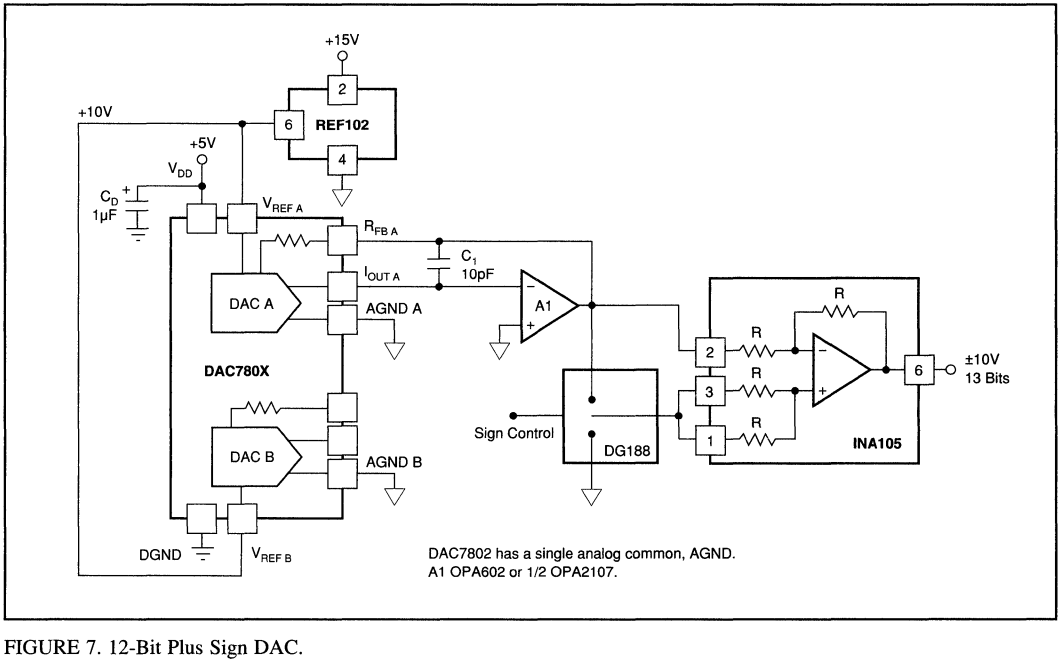


FIGURE 7. 12-Bit Plus Sign DAC.

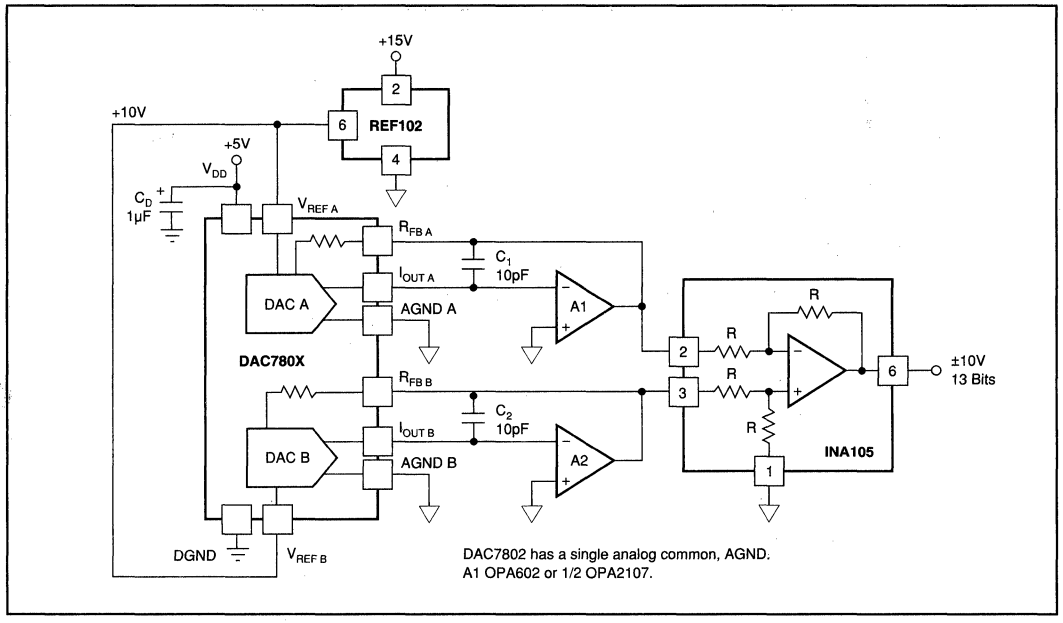


FIGURE 8. 13-Bit Bipolar DAC.

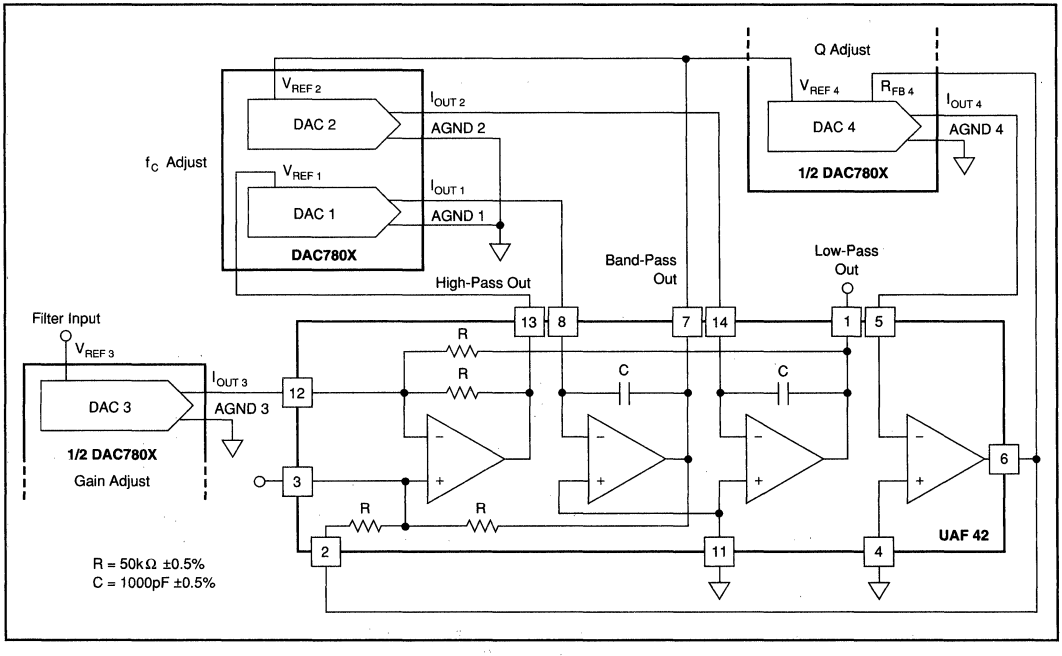


FIGURE 9. Digitally Programmable Universal Active Filter.

BURR - BROWN®

DAC8043

CMOS 12-Bit Serial Input Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT ACCURACY IN 8-PIN MINI-DIP AND 8-PIN SOIC
- FAST 3-WIRE SERIAL INTERFACE
- LOW INL AND DNL: ±1/2 LSB max
- GAIN ACCURACY TO ±1LSB max
- LOW GAIN TEMPCO: 5ppm/°C max
- OPERATES WITH +5V SUPPLY
- TTL/CMOS COMPATIBLE
- ESD PROTECTED

APPLICATIONS

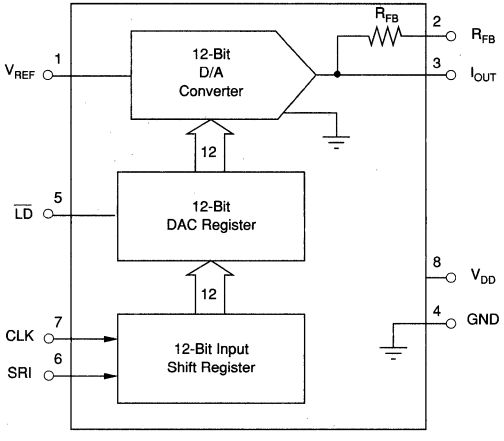
- AUTOMATIC CALIBRATION
- MOTION CONTROL
- MICROPROCESSOR CONTROL SYSTEMS
- PROGRAMMABLE AMPLIFIER/ ATTENUATORS
- DIGITALLY CONTROLLED FILTERS

DESCRIPTION

The DAC8043 is a 12-bit current output multiplying digital-to-analog converter (DAC) that is packaged in a space saving surface mount 8-pin SOIC and an 8-pin Mini-DIP. Its 3-wire serial interface saves additional circuit board space which results in low power dissipation. When used with microprocessors having a serial port, the DAC8043 minimizes the digital noise feedthrough from its input to output. The serial port can be used as a dedicated analog bus and kept inactive while the DAC8043 is in use. Serial interfacing reduces the complexity of opto or transformer isolation applications.

The DAC8043 contains a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial input (SRI) data is clocked into the input register on the rising edge of the clock (CLK) pulse. When the new data word had been clocked in, it is loaded into the DAC register by taking the $\overline{LD}$ input low. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043 operates from a single +5V power supply which makes the DAC8043 an ideal low power, small size, high performance solution for several applications.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8043P, U			DAC8043PC, UC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution	N		12			12			Bits
Nonlinearity[1]	INL				±1			±1/2	LSB
Differential Nonlinearity[2]	DNL				±1			±1/2	LSB
Gain Error[3]	FSE	T_A = +25°C			±2			±1	LSB
		T_A = Full Temp Range			±2			±2	LSB
Gain Tempco[5]	TC_{FSE}				±5			±5	ppm/°C
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		±0.0006	±0.002		±0.0006	±0.002	%/%
Output Leakage Current[4]	I_{LKG}	T_A = +25°C			±5			±5	nA
		T_A = Full Temp Range			±100			±25	nA
Zero Scale Error[7, 12]	I_{ZSE}	T_A = +25°C			0.03			0.03	LSB
		T_A = Full Temp Range			0.60			0.15	LSB
Input Resistance[8]	R_{IN}		7	11	15	7	11	15	kΩ
AC PERFORMANCE									
Output Current Settling Time[5, 6]	t_S	T_A = +25°C		0.25	1		0.25	1	µs
Digital-to-Analog Glitch		V_{REF} = 0V		2	20		2	20	nVs
Energy[5, 10]	Q	I_{OUT} = Load = 100Ω							
		C_{EXT} = 13pF							
		DAC Register Loaded Alternately with all 0s and all 1s							
Feedthrough Error[5, 11]	FT	V_{REF} = 20Vp-p at f = 10kHz		0.7	1		0.7	1	mVp-p
(V_{REF} to I_{OUT})		Digital Input = 0000 0000 0000							
		T_A = +25°C							
Total Harmonic Distortion[5]	THD	V_{REF} = $6V_{RMS}$ at 1kHz		–85			–85		dB
		DAC Register Loaded with all 1s							
Output Noise Voltage Density[5, 13]	e_N	10Hz to 100kHz			17			17	$nV/\sqrt{Hz}$
		Between R_{FB} and I_{OUT}							
DIGITAL INPUTS									
Digital Input High	V_{IH}		2.4			2.4			V
Digital Input Low	V_{IL}				0.8			0.8	V
Input Leakage Current[9]	I_{IL}	V_{IN} = 0V to +5V			±1			±1	µA
Input Capacitance[5, 11]	C_{IN}	V_{IN} = 0V			8			8	pF
ANALOG OUTPUTS									
Output Capacitance[5]	C_{OUT}	Digital Inputs = V_{IH}			110			110	pF
		Digital Inputs = V_{IL}			80			80	pF
TIMING CHARACTERISTICS[5, 14]									
Data Setup Time	t_{DS}	T_A = Full Temperature Range	40			40			ns
Data Hold Time	t_{DH}	T_A = Full Temperature Range	80			80			ns
Clock Pulse Width High	t_{CH}	T_A = Full Temperature Range	90			90			ns
Clock Pulse Width Low	t_{CL}	T_A = Full Temperature Range	120			120			ns
Load Pulse Width	t_{LD}	T_A = Full Temperature Range	120			120			ns
LSB Clock into Input Register									
to Load DAC Register Time	t_{ASB}	T_A = Full Temperature Range	0			0			ns
POWER SUPPLY									
Supply Voltage	V_{DD}		4.75	5	5.25	4.75	5	5.25	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}			500			500	µA
		Digital Inputs = 0V or V_{DD}			100			100	µA

NOTES: (1) ±1/2 LSB = ±0.012% of Full Scale. (2) All grades are monotonic to 12-bits over temperature. (3) Using internal feedback resistor. (4) Applies to I_{OUT}; All digital inputs = 0V. (5) Guaranteed by design and not tested. (6) I_{OUT} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_S = propagation delay (t_{PD}) + 9τ where τ = measured time constant of the final RC decay. (7) V_{REF} = +10V, all digital inputs = 0V. (8) Absolute temperature coefficient is less than ±50ppm/°C. (9) Digital inputs are CMOS gates: I_{IN} is typically 1nA at +25°C. (10) V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V. (11) All digital inputs = 0V. (12) Calculated from worst case R_{REF}: I_{ZSE} (in LSBs) = (R_{REF} X I_{LKG} X 4096)/V_{REF}. (13) Calculations from en = $\sqrt{4K\ TRB}$ where: K = Boltzmann constant, J/°K, R = resistance, Ω. T = Resistor temperature, °K, B = bandwidth, Hz. (14) Tested at V_{IN} = 0V or V_{DD}.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	0V, +7V
V_{REF} to GND	±25V
V_{RFB} to GND	±25V
Digital Input Voltage Range	–0.3V to V_{DD}
Output Voltage (Pin 3)	–0.3 V to V_{DD}
Operating Temperature Range	
AD	0°C to +70°C
P, PC, U, UC	–40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	–65°C to + 150°C
Lead Temperature (soldering, 10s)	+300° C
θ_{JA}(1)	
U Package	+100°C/W
P Package	+96°C/W
θ_{JC}	
U Package	+42°C/W
P Package	+37°C/W

NOTE: (1) θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for PDIP packages.

CAUTION: 1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2). 2. The digital control inputs are ESD protected: however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. 3. Use proper anti-static handling procedures. 4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ORDERING INFORMATION

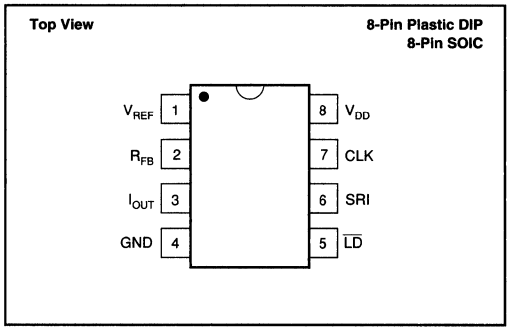
MODEL	INL	TEMPERATURE RANGE	PACKAGE
DAC8043P	1LSB	–40°C to +85°C	8-pin Plastic DIP
DAC8043PC	1/2LSB	–40°C to +85°C	8-pin Plastic DIP
DAC8043U	1LSB	–40°C to +85°C	8-pin SOIC
DAC8043UC	1/2LSB	–40°C to +85°C	8-pin SOIC

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC8043P	8-Pin PDIP	006
DAC8043PC	8-Pin PDIP	006
DAC8043U	8-Pin SOIC	182
DAC8043UC	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

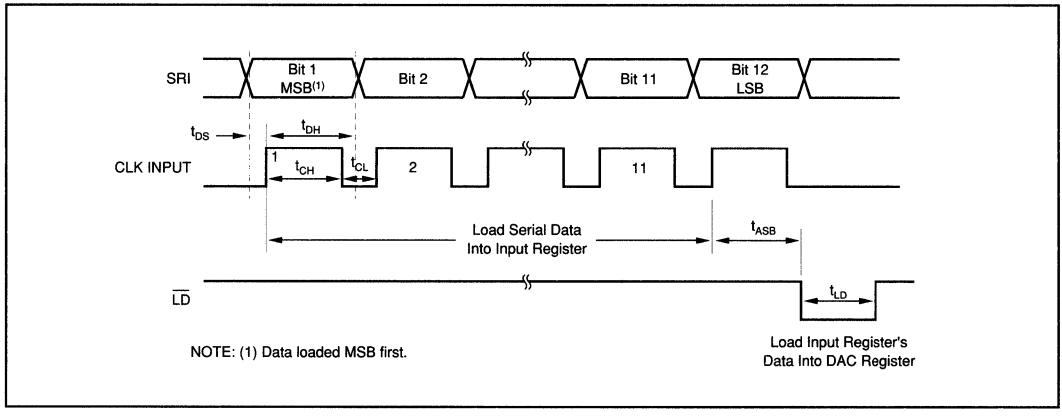
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

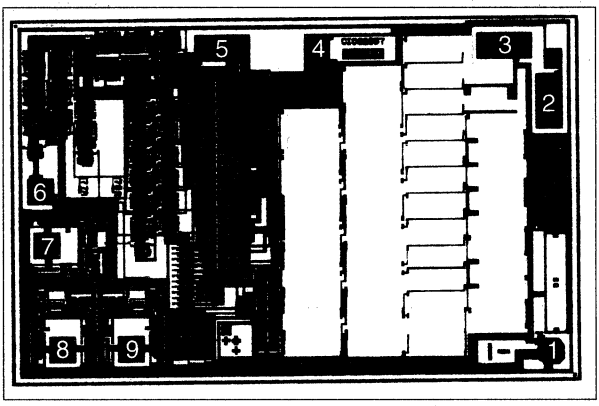
Digital Inputs: All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. V_{REF} and R_{FB} show some sensitivity.

WRITE CYCLE TIMING DIAGRAM



DICE INFORMATION



DAC8043 DIE TOPOGRAPHY

PAD	FUNCTION
1	V_{DD}
2	V_{REF}
3	R_{FB}
4	I_{OUT}
5	AGND
6	DGND
7	$\overline{LD}$
8	SRI
9	CLK

Substrate Bias: $+V_{DD}$.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	70x 110 ±5	1.78 x 2.79 ±0.13
Die Thickness	14 ±3	0.35 ±3
Min. Pad Size	4 x 4	0.1 x 0.1
Metallization		Aluminum
Backing		Chrome Silver

WAFER TEST LIMITS

At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = +25°C.

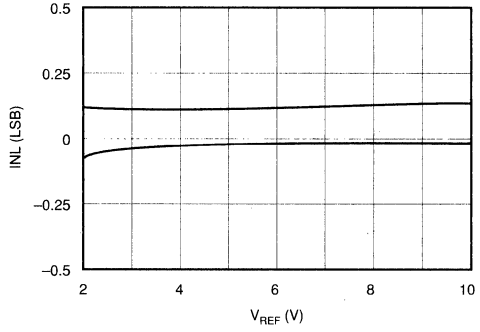
PARAMETER	SYMBOL	CONDITIONS	LIMIT	DAC8043 UNITS
STATIC ACCURACY				
Resolution	N		12	Bits min
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Gain Error	G_{FSE}	Using Internal Feedback Resistor	±2	LSB max
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% max
Output Leakage Current (I_{OUT})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA max
REFERENCE INPUT				
Input Resistance	R_{IN}		7/15	kΩ min/max
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V min
Digital Input LOW	V_{IL}		0.8	V max
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	µA max
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	500	µA max
		Digital Inputs = 0V to V_{DD}	100	µA max

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

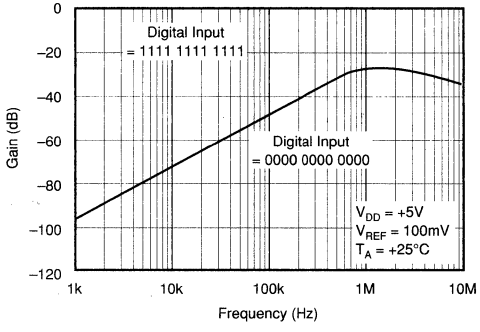
TYPICAL PERFORMANCE CURVES

At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

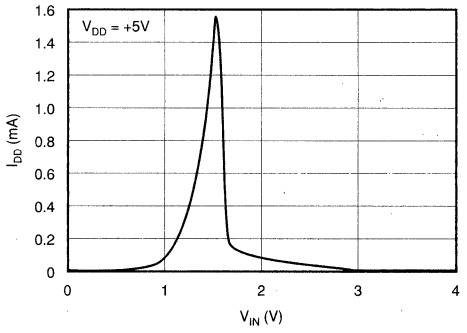
LINEARITY ERROR vs REFERENCE VOLTAGE



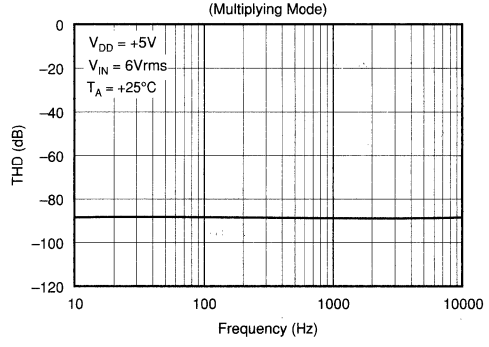
GAIN vs FREQUENCY



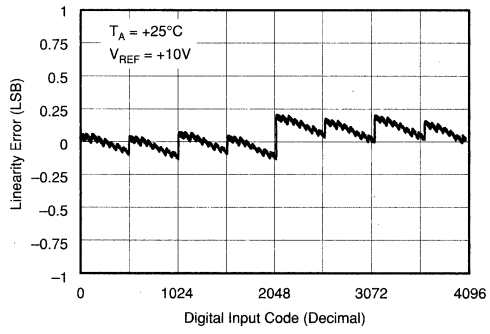
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



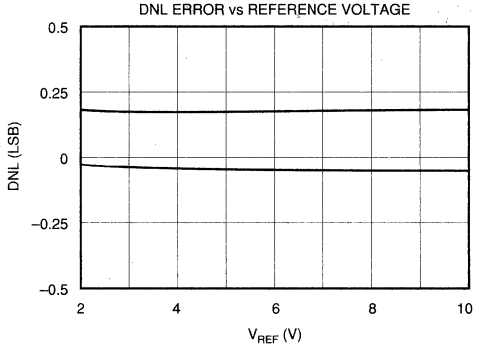
TOTAL HARMONIC DISTORTION vs FREQUENCY
(Multiplying Mode)



LINEARITY ERROR vs DIGITAL CODE



DNL ERROR vs REFERENCE VOLTAGE



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC8043 is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figure 4.

OUTPUT LEAKAGE CURRENT

The current which appears at I_{OUT} with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from I_{OUT} to GND.

FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.01% of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of a DAC8043. The current from the V_{REF} pin is switched between I_{OUT} and GND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.

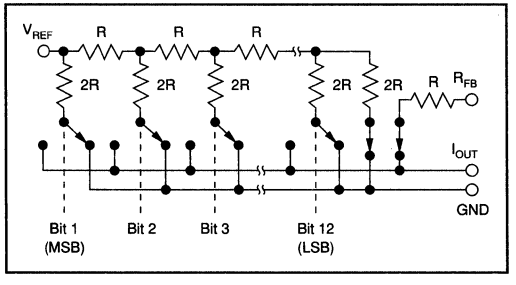


FIGURE 1. Simplified Circuit Diagram for the DAC.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, R_{FB}, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for the DAC. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 80pF to 110pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.

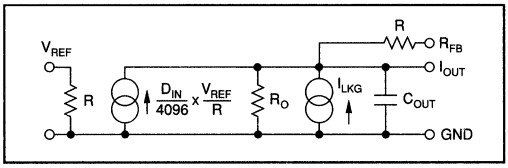


FIGURE 2. Equivalent Circuit for the DAC.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC8043 is designed to operate on V_{DD} = +5V ±5%. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the D/A. Output op amp analog common (+ input) should be connected as near to the GND pins of the DAC8043 as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Coupling from any of the digital control or data lines might degrade the glitch performance. Solder the DAC8043 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC8043 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is nonlinear with code, and the largest steps in R_O occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is

$$2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3.$$

Thus, to maintain good nonlinearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC8043 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistor R2 induces a positive gain error greater than worst-case initial negative gain error. Trim resistor R1 provides a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC8043 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602 or a dual amplifier such as the OPA2107. C1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R1–R2 should be ratio-matched to 0.01% to ensure the specified gain error performance.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE I. Unipolar Output Code.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Output Code.

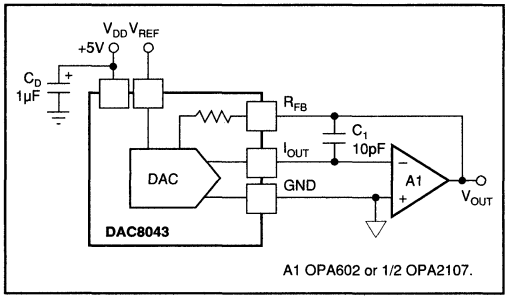


FIGURE 3. Unipolar Configuration.

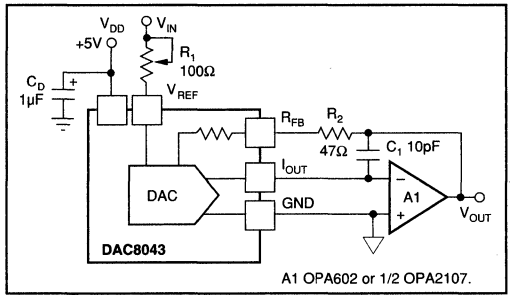


FIGURE 4. Unipolar Configuration with Gain Trim.

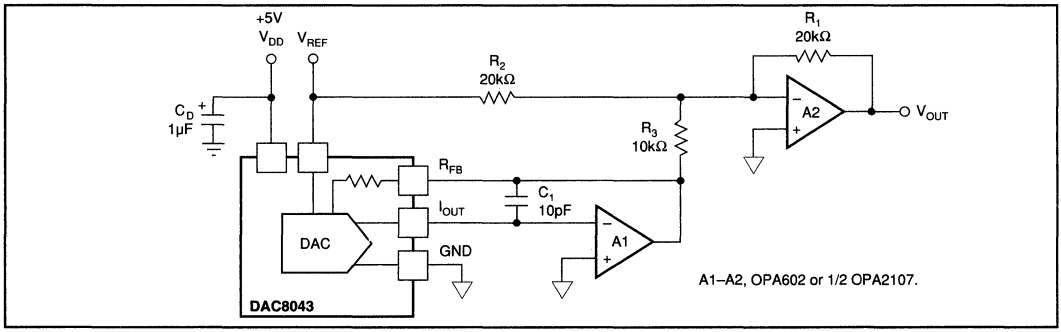


FIGURE 5. Bipolar Configuration.

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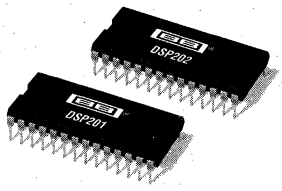


DSP201
DSP202

DSP-Compatible Single/Dual DIGITAL-TO-ANALOG CONVERTERS

FEATURES

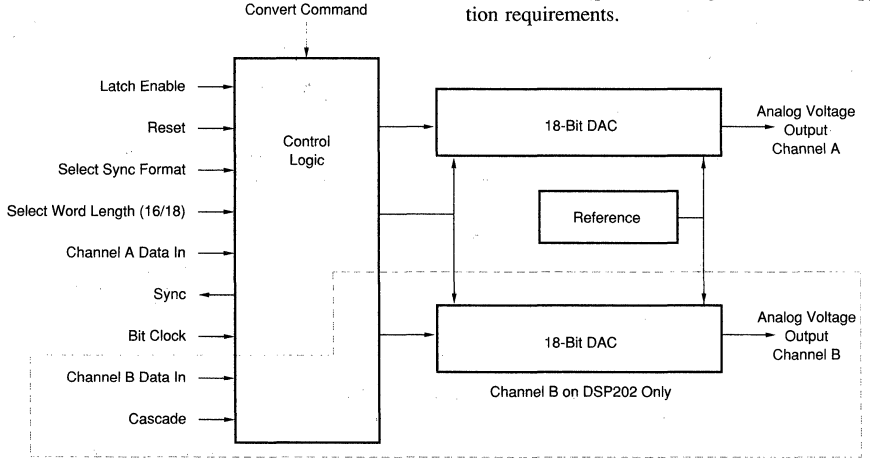
- **ZERO-CHIP INTERFACE TO DSP ICs: AD, AT&T, MOTOROLA, TI**
- **SINGLE CHANNEL: DSP201**
- **DUAL CHANNEL: DSP202 Two Serial Inputs or Cascade from Single 32-Bit Word**
- **UPDATE RATE TO 500kHz**
- **DYNAMIC SPECIFICATIONS: Signal/(Noise + Distortion) = 90dB; THD = –92dB**
- **USER SELECTABLE 16-BIT OR 18-BIT DATA WORDS**

DESCRIPTION

The DSP201 and DSP202 are high performance digital-to-analog converters designed for simplicity of use with modern digital signal processing ICs. Both are complete with all interface logic for use directly with DSP ICs, and provide analog output voltages updated at up to 500kHz.

The DSP201 offers a single complete voltage output channel, accepting either 16 bits or 18 bits of input data, and can be driven by 16-bit, 24-bit, or 32-bit serial ports. The DSP202 offers two complete voltage output channels, with either two separate input ports, or a mode to drive both output channels from a single 32-bit word.

Both the DSP201 and DSP202 are packaged in standard, low-cost 28-pin plastic DIP packages. Each is offered in two performance grades to match application requirements.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = 0°C to 70°C, Output Update Frequency, f_S, = 400kHz, V_{A+} = V_{D+} = +5V, V_{A-} = V_{D-} = –5V, unless otherwise specified.

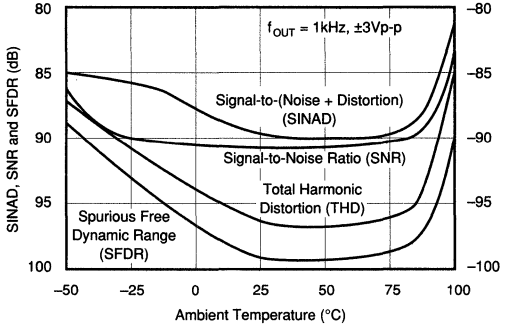
PARAMETER	CONDITIONS	DSP201JP DSP202JP MIN	DSP201JP DSP202JP TYP	DSP201JP DSP202JP MAX	DSP201KP DSP202KP MIN	DSP201KP DSP202KP TYP	DSP201KP DSP202KP MAX	UNITS
RESOLUTION				18			*	Bits
DYNAMIC RANGE			108			*		dB
ANALOG OUTPUT								
Voltage Range	R_L = 375Ω		±3		*			V
Impedance			0.1			*		Ω
Current	R_L = 375Ω		±8			*		mA
Slew Rate	R_L = 1.5kΩ, C_L = 100pF		15			*		V/µs
Settling Time to 0.006% for Full-Scale Step	R_L = 1.5kΩ, C_L = 100pF		2.5			*		µs
THROUGHPUT SPEED (1)								
Update Rate	CASC = LOW on DSP202	500			*			kHz
DSP202 in Cascade Mode	CASC = HIGH	300						kHz
AC ACCURACY (2, 3)								
Signal to (Noise + Distortion) Ratio	f_{OUT} = 1kHz	82	86		88	90		dB(4)
	f_{OUT} = 1kHz (–60dB)		30			32		dB
	f_{OUT} = 10kHz	80	86		86	90		dB
Total Harmonic Distortion	f_{OUT} = 1kHz		–90	–85		–92	–88	dB
Channel Separation on DSP202	f_{OUT} = 1kHz to 100kHz		105			*		dB
DC ACCURACY								
Integral Nonlinearity Error			±0.006			±0.004		%
Differential Nonlinearity Error			±0.006			±0.004		%
Bipolar Zero Error (5)			±10			*		mV
Bipolar Zero Error Drift			20			*		ppm FSR/°C
Bipolar Zero Mismatch (5)	DSP202 Channels		5			*		mV
Gain Error			1	3		*	*	%
Gain Error Drift			100			*		ppm/°C
Gain Error Mismatch	DSP202 Channels		1	3		*	*	%
Digital Feedthrough	ENABLE = HIGH		–105			*		dB
Power Supply Sensitivity	–5.1 < V_{A-}, V_{D-} < –4.9		–60			*		dB
	+4.9 < V_{A+}, V_{D+} < +5.1		–60			*		dB
DIGITAL INPUTS								
Format			Serial; MSB first; 16/18-bit and Cascaded					
Coding			Binary Twos Complement					
Logic Levels								
V_{IL}	I_{IL} = ±10µA	0		+0.8	*		*	V
V_{IH}	I_{IH} = ±10µA	+2.4		+5	*		*	V
Data Transfer Clock								
Frequency				12	*		*	MHz
Duty Cycle		40	50	60	*	*	*	%
DIGITAL OUTPUTS								
V_{OL}	I_{OL} = 4mA	0		+0.4	*		*	V
V_{OH}	I_{OH} = 4mA	+2.4		+5	*		*	V
POWER SUPPLIES								
Rated Voltage								
V_{A+}		+4.75	+5	+5.25	*	*	*	V
V_{A-}		–5.25	–5	–4.75	*	*	*	V
V_{D+}		+4.75	+5	+5.25	*	*	*	V
V_{D-}		–5.25	–5	–4.75	*	*	*	V
Current								
I_{A+}			18			*		mA
I_{A-}			17			*		mA
I_{D+}			13			*		mA
I_{D-}			25			*		mA
Power Consumption			365	450		*	*	mW
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		–40		+125	*		*	°C

NOTES: (1) The data transfer clock must be at least 24 times the update rate for the standard mode, and 40 times the update rate in the DSP202 Cascade Mode. (2) All dynamic specifications are based on 2048-point FFTs. (3) Data for the 1kHz test is bandlimited to 0 to 20kHz. Data for the 10kHz test is bandlimited to 0 to 40kHz. (4) All specifications in dB are referred to a full-scale output, ±3Vp-p. (5) Adjustable to zero with external potentiometer.

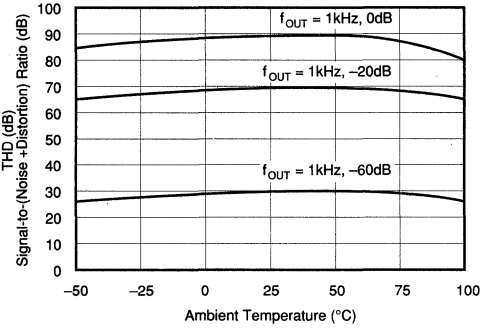
TYPICAL PERFORMANCE CURVES

T_A = +25°C; Update Frequency, f_S = 400kHz; $V_A+ = V_D+ = +5V$; $V_A- = V_D- = 5V$; SWL = HIGH; CASC = LOW; Output Bandwidth Limited to 20kHz; unless otherwise noted.

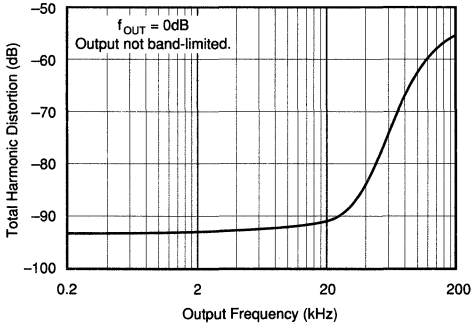
DYNAMIC PERFORMANCE vs TEMPERATURE



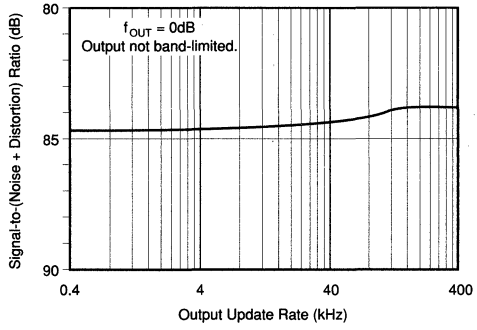
SIGNAL-TO-(NOISE + DISTORTION) RATIO vs TEMPERATURE AND AMPLITUDE



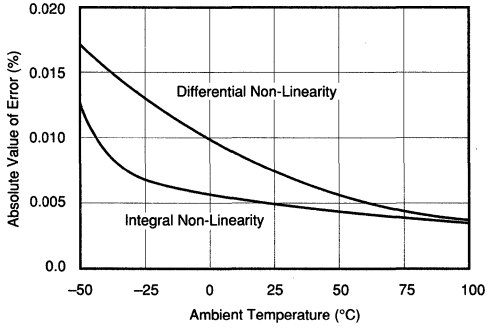
TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY



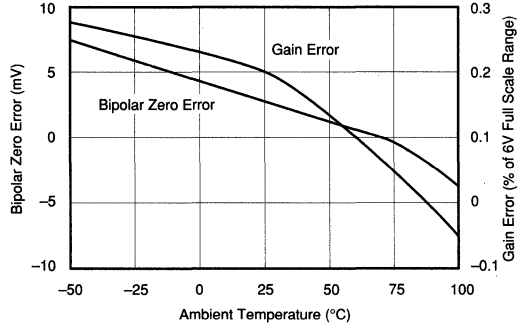
SIGNAL-TO-(NOISE + DISTORTION) vs OUTPUT UPDATE RATE



INTEGRAL AND DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE (For Worst-Case Codes.)



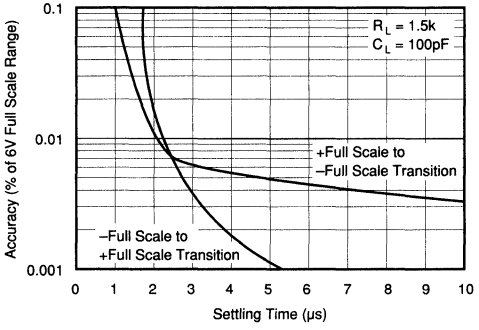
BIPOLAR ZERO ERROR AND GAIN ERROR vs TEMPERATURE



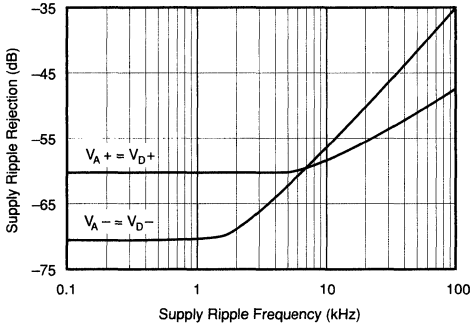
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C; Update Frequency, f_S = 400kHz; $V_A+ = V_D+ = +5V$; $V_A- = V_D- = 5V$; SWL = HIGH; CASC = LOW; Output Bandwidth Limited to 20kHz; unless otherwise noted.

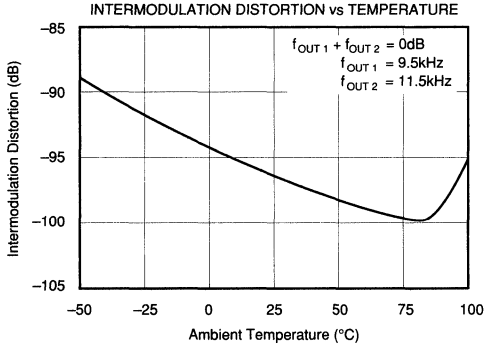
OUTPUT VOLTAGE SETTLING TIME



POWER SUPPLY REJECTION vs SUPPLY RIPPLE FREQUENCY



INTERMODULATION DISTORTION vs TEMPERATURE



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DSP201JP	28-Pin Plastic DIP	215
DSP201KP	28-Pin Plastic DIP	215
DSP202JP	28-Pin Plastic DIP	215
DSP202KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	NUMBER OF CHANNELS	SIGNAL-TO-(NOISE + DIST.) RATIO, dB min
DSP201JP	1	82
DSP201KP	1	88
DSP202JP	2	82
DSP202KP	2	88

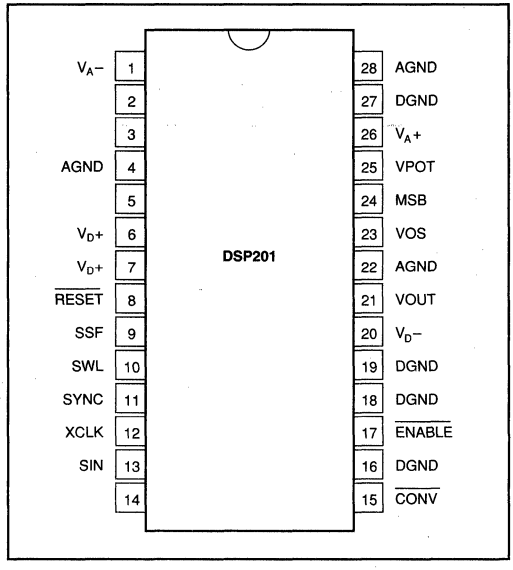
ELECTROSTATIC DISCHARGE SENSITIVITY

The DSP201 and DSP202 are ESD (electrostatic discharge) sensitive devices, and normal standard precautions should be taken. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ABSOLUTE MAXIMUM RATINGS

V_A+ to Analog Common	+7V
V_A- to Analog Common	–7V
V_D+ to Digital Common	+7V
V_D- to Digital Common	–7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_D + 0.5V
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	50°C/W

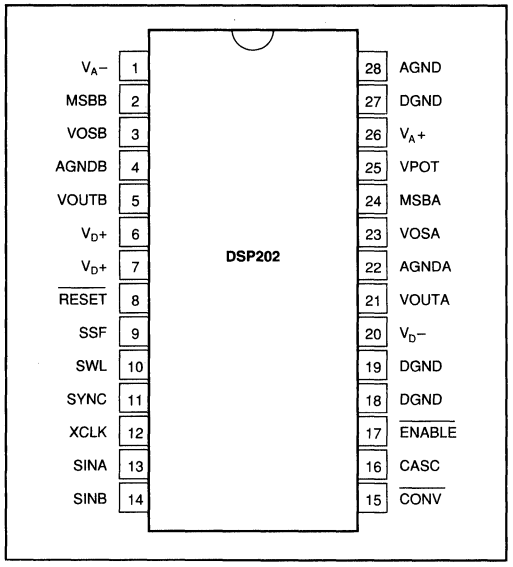
DSP201 PIN CONFIGURATION



DSP201 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2		No Internal Connection.
3		No Internal Connection.
4	AGND	Analog Ground.
5		No Internal Connection.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{RESET}$	Reset. If LOW, DAC output will be 0V after two convert commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two convert commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP201 accepts first 16 bits of data. If LOW, DSP201 accepts first 18 bits of data.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SIN	Serial Data In. MSB first, Binary Two's Complement format.
14		No Internal Connection.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	DGND	Digital Ground.
17	$\overline{ENABLE}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUT	Voltage Out.
22	AGND	Analog Ground.
23	VOS	VOS Adjust In.
24	MSB	MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustment.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

DSP202 PIN CONFIGURATION



DSP202 PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	V_A-	–5V Analog Power.
2	MSBB	Channel B MSB Adjust In.
3	VOSB	Channel B VOS Adjust In.
4	AGNDB	Channel B Analog Ground.
5	VOUTB	Channel B Voltage Out.
6	V_D+	+5V Digital Power.
7	V_D+	+5V Digital Power.
8	$\overline{RESET}$	Reset. If LOW, DAC output will be 0V after two Convert Commands, and will remain there as long as the Reset input is LOW. If HIGH, normal operation proceeds. Two Convert Commands are required after Reset goes from LOW to HIGH before the output will relate to the input word.
9	SSF	Select Sync Format In. Tie HIGH for use with Motorola and TI DSP ICs. Tie LOW for use with AT&T DSP ICs.
10	SWL	Select Word Length In. If HIGH, DSP202 accepts first 16 bits of data. If LOW, DSP202 accepts first 18 bits of data. Must be HIGH if CASC is HIGH.
11	SYNC	Data Synchronization Output. Active HIGH when SSF is HIGH, active LOW when SSF is LOW.
12	XCLK	Data Transfer Clock Input.
13	SINA	Channel A Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINB and to DSP IC output.
14	SINB	Channel B Serial Data In. MSB first, Binary Two's Complement format. In Cascade Mode, connect to SINA and to DSP IC output.
15	CONV	Convert Command In. DAC is updated on falling edge, and initiates clocking new data in.
16	CASC	Select Cascade Mode In. If HIGH, DSP202 accepts a 32-bit word, and uses the first 16 bits to update channel A, and the second 16 bits to update channel B. In Cascade Mode, SINA and SINB are connected together. If CASC is LOW, data is strobed into both channels on each clock cycle.
17	$\overline{ENABLE}$	Latch Enable In. If LOW, DAC output will be latched with new data word on falling edge of Convert Command. If HIGH, Convert Commands will be ignored.
18	DGND	Digital Ground.
19	DGND	Digital Ground.
20	V_D-	–5V Digital Power.
21	VOUTA	Channel A Voltage Out.
22	AGNDA	Channel A Analog Ground.
23	VOSA	Channel A VOS Adjust In.
24	MSBA	Channel A MSB Adjust In.
25	VPOT	Trim Reference Out for MSB adjustments.
26	V_A+	+5V Analog Power.
27	DGND	Digital Ground.
28	AGND	Analog Ground.

THEORY OF OPERATION

The DSP201 and DSP202 are basic voltage output digital-to-analog converters with complete logic interface circuitry for ease of use with standard digital signal processing ICs. Data words are transmitted from the DSP IC on its serial port, leaving the DSP IC parallel ports free for digital communication.

The DSP201 and DSP202 are pipelined internally. When the user gives a convert command at time t, two actions are initiated. First, the data stored in the internal shift registers following the previous convert command (at t – 1) is used to update the output D/A converters immediately. Second, the DSP201 or DSP202 transmits a synchronization pulse to the DSP IC and starts clocking new data into the shift register using the system Bit Clock. This data is then used to update the D/As when the t + 1 convert command is received.

Both the DSP201 and DSP202 are 18-bit D/As internally. On-chip logic can be programmed to use 18-bits of data to update the D/A outputs, or can be programmed to update the D/A based on 16-bit data words. Additionally, the logic in the DSP202 can accept a 32-bit data word (the Cascade Mode), and update both D/A channels simultaneously with 16 bits each. All of these modes can be hard-wired or logic-controlled externally, so that no extra overhead on the part of the DSP IC is required.

In the 16-bit modes, the DSP201 and DSP202 will append zeros to the 16-bits transferred to each of the internal D/As, which are full 18-bit converters. The 18-bit word-length mode can be used with DSP ICs programmed for either 24-bit or 32-bit output words, in which case the DSP201 or DSP202 will clock in the first 18-bits of data after the synchronization pulse, and ignore additional information on the serial line. When programmed to accept 16-bit words, the DSP201 and DSP202 can be used with DSP ICs programmed to output 16-, 24-, or 32-bit words, and will ignore additional information after the first 16 bits on the serial line.

The DSP201 and DSP202 are complete voltage output D/A converters, with on-chip references and output amplifiers to drive ±3V into 375Ω loads. State-of-the-art bipolar technologies are used in the D/A section to maximize the output update rate, to maximize dynamic performance, and to eliminate glitch problems. Advanced plastic packaging methods makes this performance attainable economically.

BASIC OPERATION

DATA FORMAT AND OUTPUT LEVELS

The DSP201 and DSP202 accept serial data, MSB first, in standard Binary Two's Complement format. The length of the data words can be selected as shown below, and the D/A output level generated by a specific input code is shown in Table I.

As with all standard D/As, the output ranges from negative full scale (–3V) to 1 LSB below positive full scale (+3V – 1LSB). The bipolar output amplifiers are designed to drive 375Ω loads at full speed and accuracy.

UPDATING THE OUTPUT

With $\overline{\text{ENABLE}}$ (pin 17) LOW, the falling edge of a Convert Command arriving on CONV (pin 15) will immediately update the D/A outputs with the data stored in the internal shift registers following the previous Convert Command. The Convert Command can be asynchronous to any other signals or clocks without reducing accuracy, although system accuracy is often enhanced by synchronizing digital signals.

For a full-scale change in the input code, the output will typically settle to within ±0.006% of its final level within 2.5µs. The slew rate of the output amplifier is typically 15V/µs, for a full power bandwidth close to 800kHz. All of the specifications and typical performance curves are achieved with a full 400kHz update rate, unless otherwise specified. The DSP201 and DSP202 are guaranteed operational to a full 500kHz update rate, which exceeds the maximum Bit Clock rate for most standard DSP ICs.

DATA TRANSFER

Data is transmitted serially to the DSP201 or DSP202, and is clocked into the internal shift registers on the rising edge of the external Data Transfer Clock or Bit Clock (XCLK input on pin 12.) This clock can be as fast as 12MHz. The Data Transfer Clock can tolerate duty cycles from 40% to 60%.

As indicated in the timing diagrams in Figure 1, either 16- or 18-bits of data will be clocked into the DSP201 or DSP202, or 32-bits will be clocked into the DSP202 in the

INPUT CODE			OUTPUT VOLTAGE	
BINARY	16-BIT MODE AND DSP202 CASCADE MODE	HEX 18-BIT MODE	16-BIT MODE AND DSP202 CASCADE MODE	18-BIT MODE
0111...1111	7FFF	1FFFF	+2.999908V	2.999977V
0000...0000	0000	00000	0V	0V
1111...1111	FFFF	3FFFF	–92µV	–23µV
1000...0000	8000	20000	–3.000000V	–3.000000V
Theoretical LSB Size			91.6µV	22.9µV

TABLE I. Output Voltage vs Input Code.

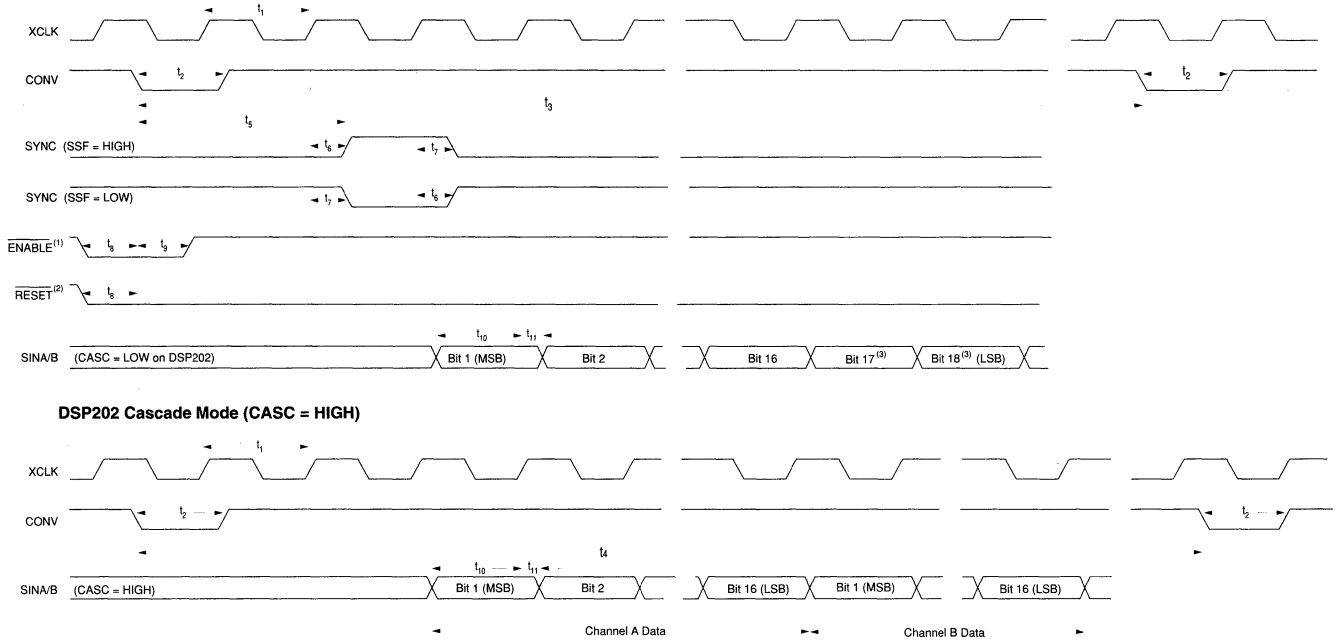


FIGURE 1. DSP201 and DSP202 Timing.

INTERVAL	DESCRIPTION	MIN	MAX	UNITS
t_1	XCLK period; Duty Cycle 50% ±10%	83		ns
t_2	Convert Command LOW Time	50		ns
t_3	Convert Period (CASC = LOW on DSP202)	24		t_1
t_4	Convert Period (CASC = HIGH on DSP202	40		t_1
t_5	SYNC Active Delay after Convert Falling Edge)	t_1 +40	2 t_1	ns
t_6	SYNC LOW to HIGH Delay from XCLK Rising; C_L = 50pF		15	ns
t_7	SYNC HIGH to LOW Delay from XCLK Rising; C_L = 50pF		15	ns
t_8	$\overline{\text{ENABLE}}$ Setup before Convert Falling Edge(1)	50		ns
t_9	$\overline{\text{ENABLE}}$ Hold after Convert Falling Edge(1)	50		ns
t_8	$\overline{\text{RESET}}$ Setup before Convert Falling Edge	50		ns
t_{10}	SINA/B Data Setup before XCLK Rising	20		ns
t_{11}	SINA/B Data Hold after XCLK Rising		0	ns

NOTES: (1) Normally tied LOW so that previously transmitted data is used to update DAC output on falling edge of CONV. $\overline{\text{ENABLE}}$ HIGH prevents the DAC from being updated. (2) $\overline{\text{RESET}}$ must be held LOW for two complete Convert Command cycles, and $\overline{\text{ENABLE}}$ must be LOW. (3) Optional data bits. Clocked into DAC register only if SWL is LOW.

Cascade Mode, but internal digital overhead requires additional Data Transfer Clock cycles before a new Convert Command can be sent. The minimum time between Convert Commands is 24 times the Data Transfer Clock period for either the DSP201 or the DSP202 in standard modes, and 40 times the Data Transfer clock period for the DSP202 in the Cascade Mode. There is no maximum time between Convert Commands.

These additional clock cycles are used to set up the internal shift registers and logic, and are included in the specifications for maximum update rate. This means a 12MHz Bit Clock can achieve the maximum specified update rate of 500kHz.

DATA SYNCHRONIZATION

The DSP201 and DSP202 have internal logic to generate a synchronization pulse (SYNC on pin 11) to signal the host processor to transmit data. The synchronization pulse is sent when a Convert Command is received, and the SYNC output changes on the rising edge of XCLK. Timing is shown in Figure 1.

The synchronization pulse can be programmed to be either active High or active Low, depending on the logic level input on SSF (Select Sync Format on pin 9.) If SSF is LOW, SYNC will be normally HIGH, and will transmit a LOW pulse after a Convert Command is received. If SSF is HIGH, SYNC will be normally LOW, and will transmit a HIGH pulse after a Convert Command is received. The SYNC pulse will be as wide as one clock cycle on the Data Transfer Clock input on XCLK (pin 12.)

SELECTING WORD LENGTH

If the Select Word Length input (SWL, pin 10) is HIGH, the DSP201 or DSP202 will accept 16 bits of data after a Convert Command, with the timing shown in Figure 1. After these 16 bits, additional data on SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) will be ignored. Transparent to the user, the internal shift register will append two zeroes to the 16-bit data words before updating the D/As on the next Convert Command.

If SWL is LOW, the DSP201 or DSP202 will clock 18 bits of data into the internal shift register after a Convert Command, with the timing shown in Figure 1. Subsequent data on SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) will be ignored.

In the 16-bit mode, an increment of 1 LSB will change the D/A output by approximately 91.6μV (the 6V full scale range divided by 2^{16}), while an LSB in the 18-bit mode will change the output approximately 22.9μV ($6V/2^{18}$).

The DSP201 and DSP202 analog performance is tested in production using the 16-bit mode (with SWL HIGH), and the typical performance curves were generated using the 16-bit mode. Verification is made during final test that the 18-bit mode functions, but the extra resolution of these last two bits is not used when testing the analog performance.

DSP202 CASCADE MODE

If CASC on the DSP202 (pin 16) is HIGH, the Cascade Mode is implemented. In this mode, SINA (pin 13) and SINB (pin 14) are strapped together and connected to the serial output port of an appropriate DSP IC or other data word source. A Convert Command initiates the transfer of a 32-bit word to the DSP202.

In the Cascade Mode, care must be taken to make sure SWL (pin 10) is HIGH.

LATCH ENABLE

If $\overline{\text{ENABLE}}$ (pin 17) is LOW, the D/A outputs will be latched with new data on the falling edge of the Convert Command. Taking $\overline{\text{ENABLE}}$ HIGH causes the DSP201 or DSP202 to ignore Convert Commands. With $\overline{\text{ENABLE}}$ HIGH when a Convert Command arrives at time t, data latched in the internal shift register after the Convert Command at t – 1 is not latched to the D/As, but a new synchronization pulse is still generated and the data in the shift register is overwritten. This feature allows multiple DSP201s or DSP202s to share a single DSP IC and still be independently updated.

RESET

Taking $\overline{\text{RESET}}$ (pin 8) LOW will cause the D/As to output 0V after two Convert Commands are received. The two Convert Commands clear out the internal shift registers, and data input on the serial input lines will be ignored while $\overline{\text{RESET}}$ is low. This facilitates designing an analog output system that goes into a known, benign state either at power-up, after fault conditions or during a calibration cycle. $\overline{\text{ENABLE}}$ (pin 17) must be LOW when resetting the DSP201 or DSP202 outputs to 0V.

After $\overline{\text{RESET}}$ is taken HIGH, two Convert Commands are required before the output will relate to the input data. Also, $\overline{\text{ENABLE}}$ must be LOW for the data to be latched to the D/As. The first Convert Command again latches the outputs at 0V, and the second Convert Command drives the output to the level determined by the data clocked in after the first Convert Command.

A $\overline{\text{RESET}}$ command after power up is not required for proper operation of the DSP201 or DSP202.

LAYOUT CONSIDERATIONS

Because of the high resolution, linearity and speed of the DSP201 and DSP202, system design problems such as ground path resistance, contact resistance and power supply quality become very important.

GROUNDS

To achieve the maximum performance from the DSP201 or DSP202, care should be taken to minimize the effect of current flows in the system grounds that may corrupt the output voltages generated by the D/As. Pin 22 on the DSP201 and pins 4 and 22 on the DSP202 are the most

critical internal grounds, and care should be taken especially at these points to make them as close as possible to the same potential as the system analog ground. The design of the DSP201 and DSP202 insures that these pins will have minimal current flowing through them.

Internally, power currents are directed to the digital grounds (pins 18, 19, and 27) for internal digital currents, which are primarily switching currents, and to the analog grounds (pin 28, plus pin 4 on the DSP201) for analog currents, which are primarily from the internal current switches and the output amplifier. Pin 16 on the DSP201 is used internally as a logic level, and injects essentially no current into the ground.

Wherever possible, it is strongly recommended that separate analog and digital ground planes be used. With an LSB level of 92µV in 16-bit modes, and one quarter of that in 18-bit modes, the currents switched in a typical DSP system (processor, memory, etc.) can easily corrupt the output accuracy of the D/A's unless great care is taken to analyze and design for current flows.

POWER SUPPLY DECOUPLING

All of the supplies should be decoupled to the appropriate grounds using tantalum capacitors in parallel with ceramic capacitors, as shown in Figures 2 and 3. For optimum performance of any high resolution D/A, all of the supplies need to be as clean as possible. If separate digital and analog supplies are available in a system, care should be taken to insure that the difference between the analog and the digital supplies is not more than 0.5V for more than a few hundred milliseconds, as may occur at power-on.

Separate –5V analog and digital supplies are not needed. These pins are kept separate internally to minimize coupling. Drive pin 20 from the –5V analog supply, and make sure that the decoupling shown in Figure 2 or 3 are placed as close as possible to the D/As.

CALIBRATION AND ADJUSTMENT OPTIONAL EXTERNAL OFFSET AND MSB TRIMS

All of the specifications for the DSP201 and DSP202, plus the typical performance curves, are based on the performance of these D/As without external trims. In most applications, external trims are not required.

If external trims are not used, pins 23, 24, and 25 on the DSP201 should be left open, as should pins 2, 3, 23, 24 and 25 on the DSP202. These pins should not be decoupled with capacitors or tied to any specific potential, or the noise on the D/A outputs may increase.

ADJUSTING OFFSET

Where required by specific applications, offsets can be trimmed using the circuits in Figure 2 (DSP201) or Figure 3 (DSP202.) As with all standard D/As, offset on the DSP201 and DSP202 means the difference of the output from the ideal negative full scale value. The DSP201 and DSP202 use a current switching D/A architecture, and the current from this is internally amplified to produce a ±3V output range. Negative full scale output thus results from having all of the internal current switches turned off. Offset on the DSP201 and DSP202 should not be confused with the delta from 0V with an input code of 0000...0000 (0000 hex for 16-bit Modes, 00000 hex for 18-bit Modes). This is often described as bipolar zero error, and includes the effects of both offset and gain error.

To trim the offsets, first latch the D/As with 1000...0000 (8000 hex or 20000 hex). Then adjust the offset adjustment pots to produce an output of –3.000000V.

ADJUSTING THE MSB WEIGHT

The MSB adjustment circuitry shown in Figure 2 for the DSP201 and in Figure 4 for the DSP202 basically change the weight of the MSB by adding to or subtracting from the current controlled by the internal MSB switch.

Depending on the application, the MSB adjustments can be made in one of three different ways to optimize the system performance using the DSP201 or DSP202. For dynamic performance, the MSB can be adjusted to minimize distortion of either a full-scale or low level sine-wave output. For applications stressing differential linearity, the 0000...0000 (0000 hex or 00000 hex) to 1000...0000 (FFFF hex or 3FFFF hex) transition can be trimmed to change the output of the D/As precisely 1 LSB (92µV in the 16-bit Mode or 23µV in the 18-bit Mode.)

To adjust for minimum distortion of full-scale sinewaves, strobe the inputs to the DSP201 or DSP202 with codes representing ideal full scale sine waves, then trim the MSB adjustment circuit to minimize distortion, as measured by either a distortion analyzer or by digitizing the output with an appropriate A/D and running FFT analyses.

In many audio applications, it is more appropriate to adjust for minimum distortion with low level sinewave outputs. This minimizes zero-crossover error, which can be a concern in high-end audio systems. To do this, strobe the inputs to the DSP201 or DSP202 with codes representing ideal low-level sine waves (–60dB from full scale works well), and then trim the MSB adjustment circuit to minimize distortion, again using a distortion analyzer or FFT analyses to check the results of the trims.

The MSB adjustment circuits can also be used to trim the D/A outputs directly for the transition from 0000...0000 (0000 hex or 00000 hex) to 1111...1111 (FFFF hex or 3FFFF hex), eliminating differential linearity error at the major carry. Ideally, this transition of the digital input code should cause the D/A outputs to change 92µV in the 16-bit Mode or 23µV in the 18-bit Mode. A simple way to make this adjustment is to continually load alternately the codes 1111...1111 (FFFF hex or 3FFFF hex) and 0000...0000 (0000 hex or 00000 hex) into the DSP201 or DSP202. An amplifier with sufficient gain can then drive an oscilloscope input, and the transition output step can be adjusted.

An alternative for calibrating on a bench is to tie SIN (DSP201 pin 13) or SINA and SINB (DSP202 pins 13 and 14) HIGH, and provide a Bit Clock and periodic Convert Commands. This loads 1111...1111 ($FFFF_{HEX}$ or $3FFFF_{HEX}$), driving the output to 1LSB below 0V. Then periodically bring $\overline{RESET}$ (pin 8) LOW for at least two Convert Commands, which is the equivalent of loading all 0s, so the output is 0V. Now the output can be adjusted for an ideal transition step.

ADJUSTING BIPOLAR ZERO ERROR

If it is important in a specific application to adjust bipolar zero error, the user should first adjust the MSB trim circuits, and then use the offset adjust circuits to adjust the outputs to 0V with input codes of all 0s (0000...0000; 0000 hex or 00000 hex.) In this case, it is not possible to also trim offset at –Full Scale, as described above.

GAIN ERROR

Gain error on the DSP201 or DSP202 cannot be directly adjusted. If required in a specific application, gain can be trimmed out at the system level by adjusting the gain used in an output amplifier stage, such as would be used in any active output filter. In this case, the bipolar zero error should be adjusted first as discussed above. Then, the gain on the output amplifier should be adjusted to minimize the deviation from ideal for –Full Scale (1000...000; 8000 hex or 20000 hex) and +Full Scale (0111...1111; 7FFF hex or 1FFFF hex.)

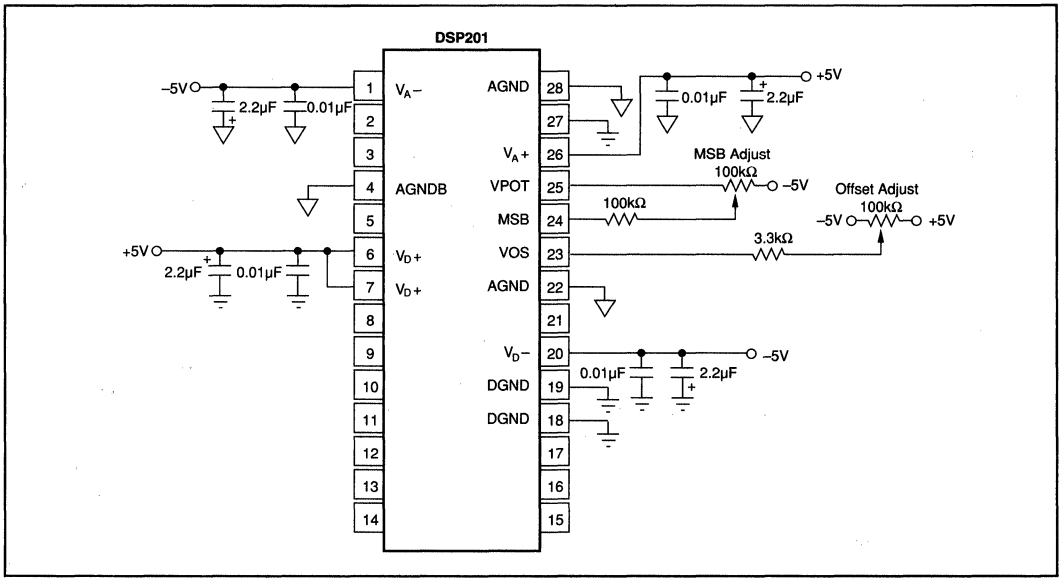


FIGURE 2. DSP201 Power Supply Connections and Optional Adjust Circuits.

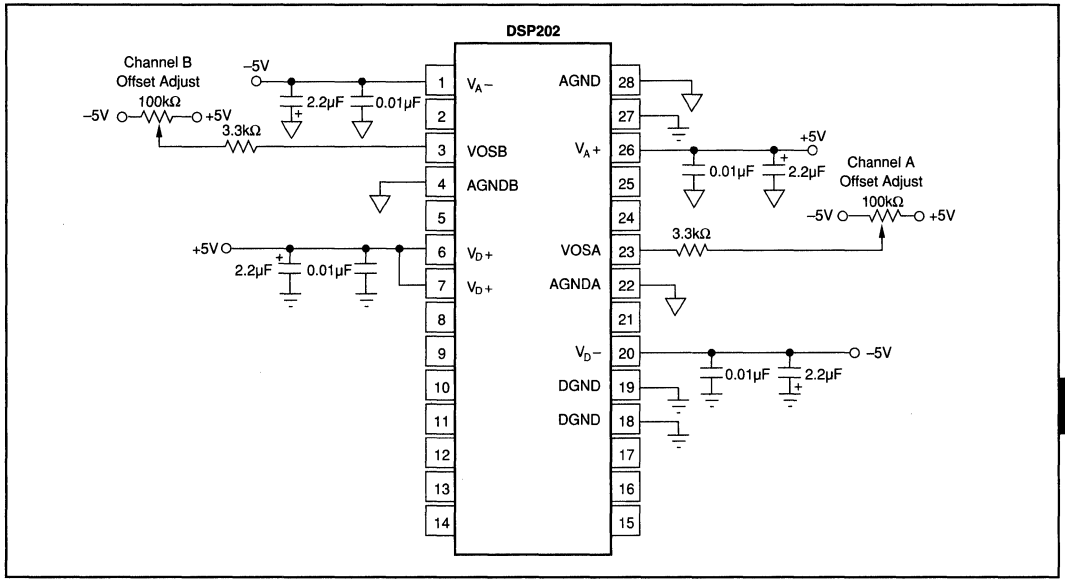


FIGURE 3. DSP202 Power Supply Connections and Optional Offset Voltage Adjustment.

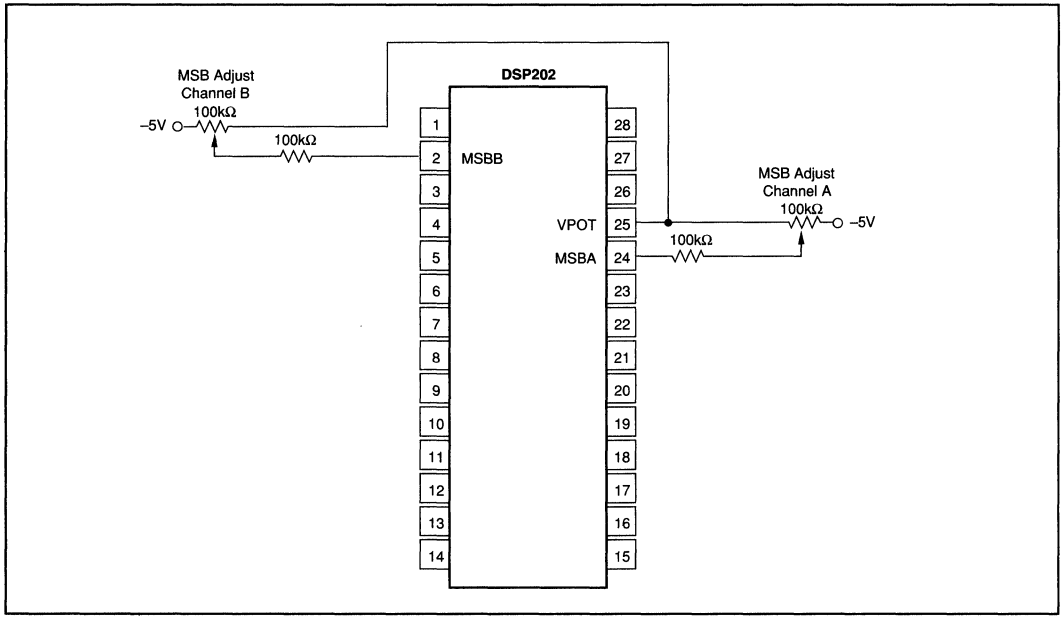


FIGURE 4. DSP202 Optional MSB Adjust Circuit.

APPLICATIONS

USING PARALLEL PORTS WITH THE DSP201 OR DSP202

Figure 5 shows a circuit for converting parallel outputs into the serial data stream required by the DSP201, and meets the requirements for timing signals. Doubling this circuit allows the DSP202 to be driven from a 32-bit parallel port. In most applications, this circuit can be easily incorporated into gate arrays or other programmed logic circuits already used in the system, since the extra gate count is not high.

DEGLITCHING

Particularly in high resolution D/A converters, changing input codes may cause glitching on the output that excessively corrupts the dynamic purity of an output signal. The DSP201 and DSP202 are designed to minimize output glitching, and all of the performance specifications and typical performance curves are based on tests with no extra deglitching circuitry. In particular, the guaranteed Signal-to-(Noise + Distortion) performance would be impossible to attain with any significant glitching.

COMPLETE ANALOG INPUT/OUTPUT SYSTEM

The DSP201 or DSP202 can be paired with the Burr-Brown DSP101 or DSP102 analog-to-digital converter to provide both analog input and analog output for a complete digital signal processing system. The DSP101 and DSP102 are respectively single and dual channel 200kHz sampling A/Ds with easy to use interfacing logic that complement the DSP201 and DSP202. Figure 6 shows a single channel analog input and output system based on a DSP201 and a DSP101, and the minimal connections required to interface to a DSP IC. A pair of channels can be implemented using a single DSP202 and a single DSP102, either with two separate DSP ICs, with a single DSP IC with dual serial input and output channels, or a single DSP IC capable of 32-bit words in the Cascade Mode.

For maximum flexibility in system design, the DSP201 or DSP202 D/As can be updated at a different rate than the conversion rate used on the DSP101 or DSP102 A/Ds, and either or both of these rates can be asynchronous to the clocks used with the DSP IC.

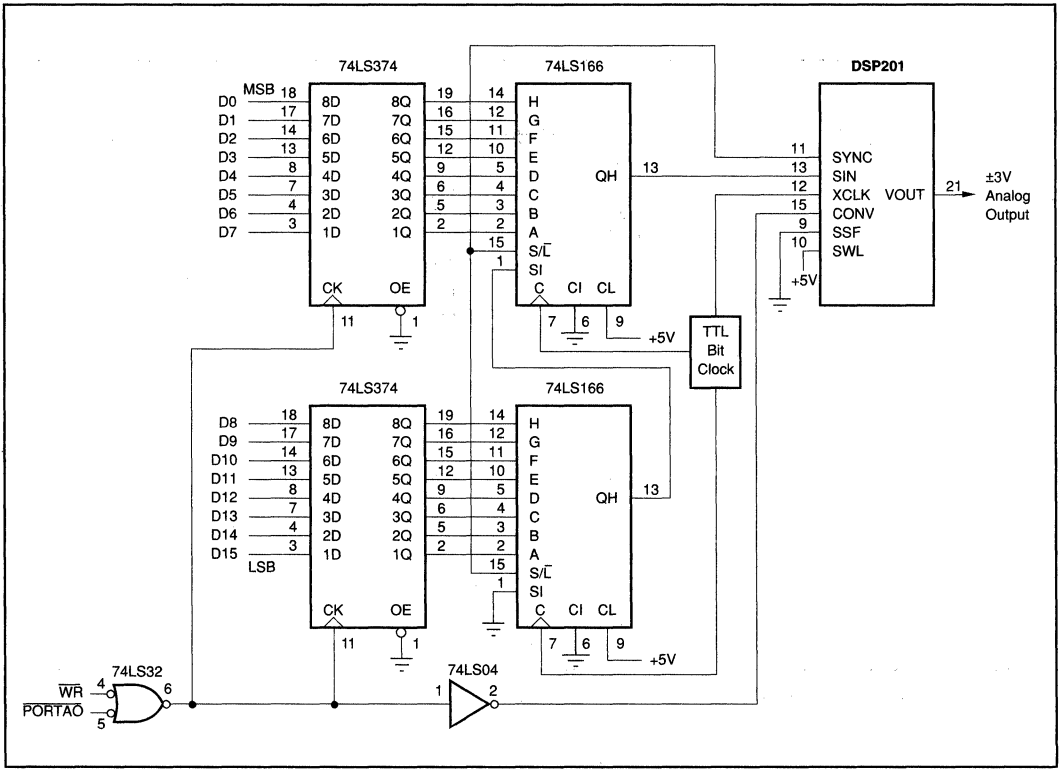
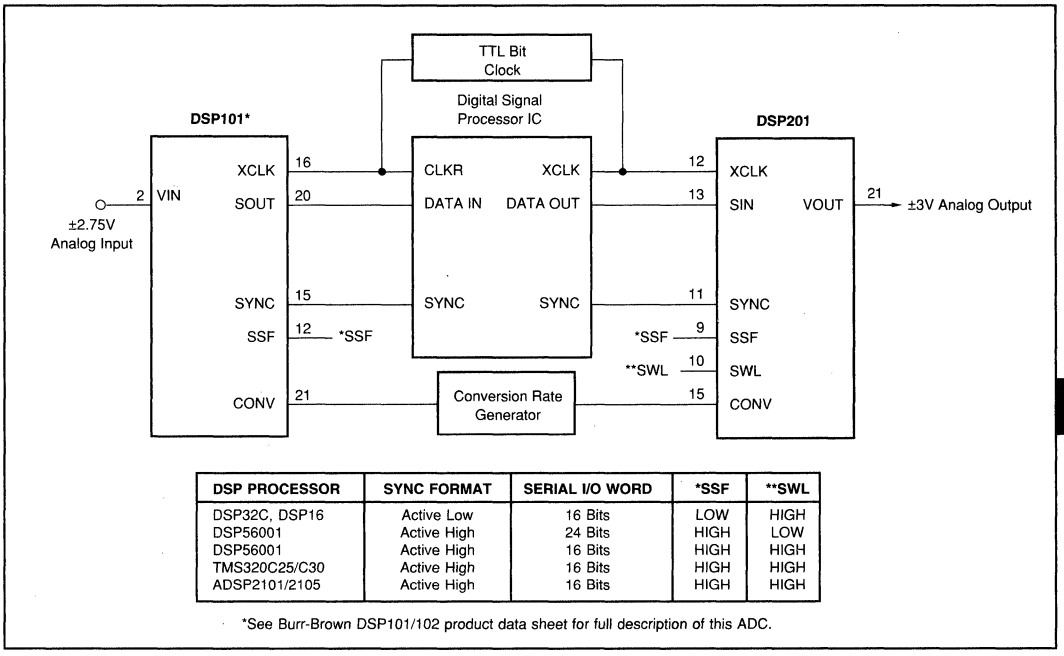


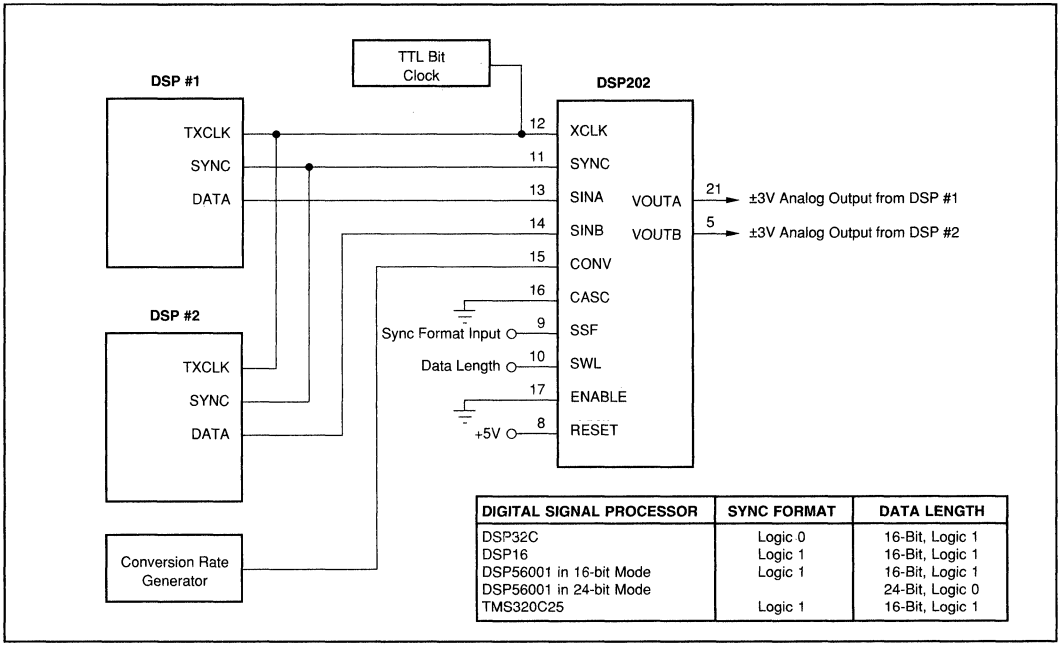
FIGURE 5. Driving the DSP201 from a 16-Bit Parallel Port.



DSP PROCESSOR	SYNC FORMAT	SERIAL I/O WORD	*SSF	**SWL
DSP32C, DSP16	Active Low	16 Bits	LOW	HIGH
DSP56001	Active High	24 Bits	HIGH	LOW
DSP56001	Active High	16 Bits	HIGH	HIGH
TMS320C25/C30	Active High	16 Bits	HIGH	HIGH
ADSP2101/2105	Active High	16 Bits	HIGH	HIGH

*See Burr-Brown DSP101/102 product data sheet for full description of this ADC.

FIGURE 6. Analog Input and Analog Output System.



DIGITAL SIGNAL PROCESSOR	SYNC FORMAT	DATA LENGTH
DSP32C	Logic 0	16-Bit, Logic 1
DSP16	Logic 1	16-Bit, Logic 1
DSP56001 in 16-bit Mode	Logic 1	16-Bit, Logic 1
DSP56001 in 24-bit Mode		24-Bit, Logic 0
TMS320C25	Logic 1	16-Bit, Logic 1

FIGURE 7. DSP202 with Dual DSP ICs.

USING DSP201 AND DSP202 WITH TEXAS INSTRUMENTS DSP ICS

Figures 6 thru 12 show various ways to use the DSP201 and DSP202 with DSP ICs from the Texas Instruments TMS320Cxx series. For simplicity, all of these circuits are based on using the TMS320Cxx in the mode where SSF (Select Synch Format, pin 9) is tied HIGH, so that there is an active High synchronization pulse generated by the DSP201 or DSP202 after receiving a Convert Command. The synchronization pulse can be changed to active Low simply by making SSF LOW, where appropriate, without changing basic operation of the D/As. The timing for either synchronization mode is shown in Figure 1.

In all cases, the DSP201 and DSP202 expect to receive the data with the MSB first, and the TMS320Cxx needs to be programmed for this.

Figure 6 shows a circuit for using the TMS320C25 to generate a complete analog input and analog output system using the DSP201 plus the Burr-Brown DSP101 A/D.

Figure 7 shows how to use two TMS320C25 chips to drive the two channels of the DSP202.

The TMS320C30 has dual serial I/O ports, which can be used to drive the dual inputs on the DSP202, as shown in Figure 8. This circuit can maximize the update rate for the channels. Since the TMS320C30 can also output 32-bit words, both channels of the DSP202 can be updated from a single serial output port on the TMS320C30, using the cascade mode as shown in Figure 9.

Figures 10 and 11 show complete two-channel analog input and analog output systems consisting of three basic chips, the TMS320C30 plus a DSP202 dual D/A and a Burr-Brown DSP102 dual A/D. Figure 10 makes use of the dual serial I/O ports on the TMS320C30, and is shown with the DSP202 in the 16-bit Mode, which maximizes the possible throughput rate on the system. Figure 11 makes use of the 32-bit word length mode in the TMS320C30 and the Cascade Mode on both the DSP202 and the DSP102 to provide two full analog I/O channels over a single serial I/O port on the TMS320C30. Thus, up to four complete, separate analog I/O channels could be operated using a single TMS320C30, by making use of the second serial port.

Figure 12 shows how to use a TMS320C25 to update the analog output of the DSP201.

USING DSP201 AND DSP202 WITH MOTOROLA DSP ICS

Figure 13 shows how to use the DSP201 with a Motorola DSP56001. Using the DSP202 requires using two DSP56001s, as indicated in Figure 7.

The DSP56001 needs to be programmed for transmission of the MSB bit first with SYNC in the Bit Mode. If the DSP56001 is programmed for 16-bit data words, SWL (pin 10) on the DSP201 or DSP202 needs to be tied HIGH to select the 16-bit Mode. In the DSP56001 24-bit mode, the DSP201 or DSP202 can be programmed to accept data lengths of 16-bits (with SWL HIGH) or 18-bits (with SWL LOW), and will ignore the trailing bits on the serial line.

For use with the Motorola DSP56001, SSF (pin 9) on the DSP201 or DSP202 needs to be tied HIGH. This will cause the DSP201 or DSP202 to transmit an appropriate active High synchronization pulse on SYNC (pin 11) after a Convert Command is received by the DSP201 or DSP202. Timing is shown in Figure 1.

Even though the DSP201 or DSP202 require a minimum of 24 Bit Clock pulses between convert commands, the maximum update rate for the D/As using a 5MHz Bit Clock will still be over 200kHz (5MHz / 24 = 208.3kHz.)

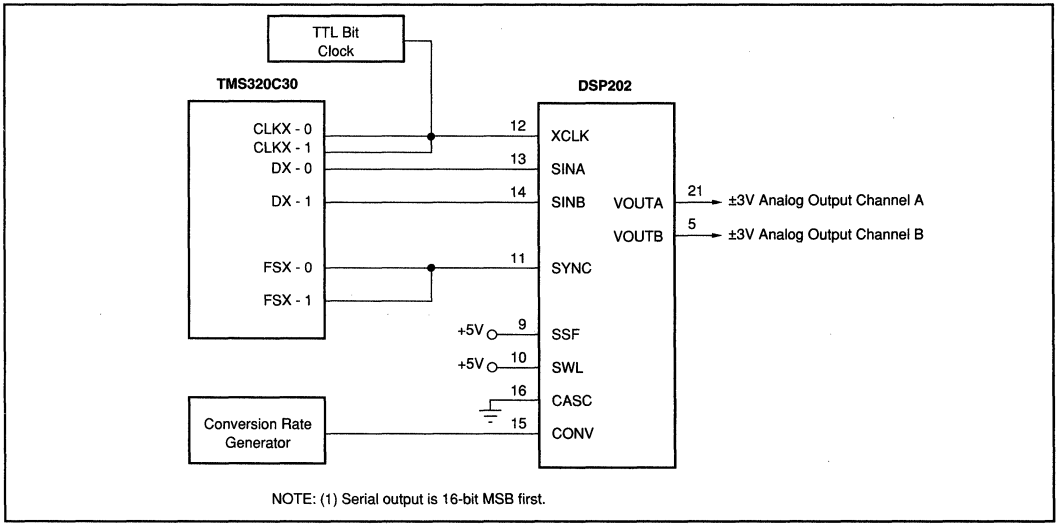


FIGURE 8. Using DSP202 with TMS320C30's Dual SIO.

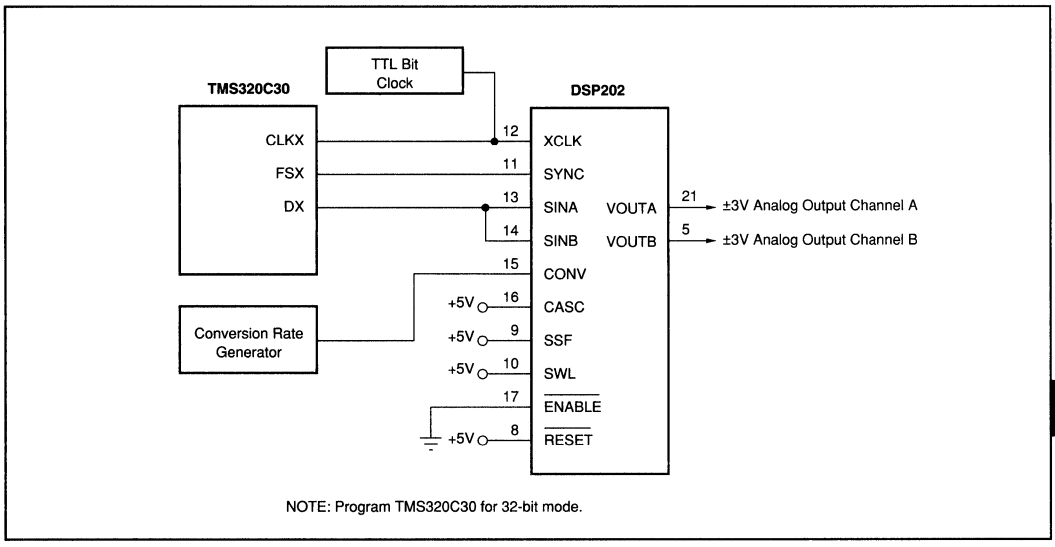


FIGURE 9. Using DSP202 with TMS320C30 in Cascade Mode.

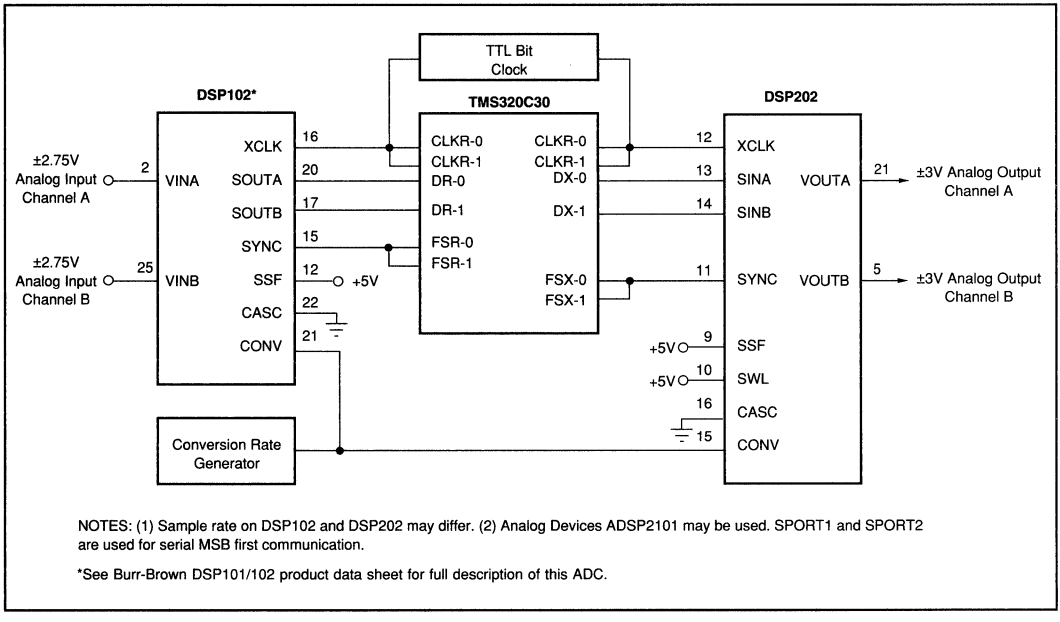
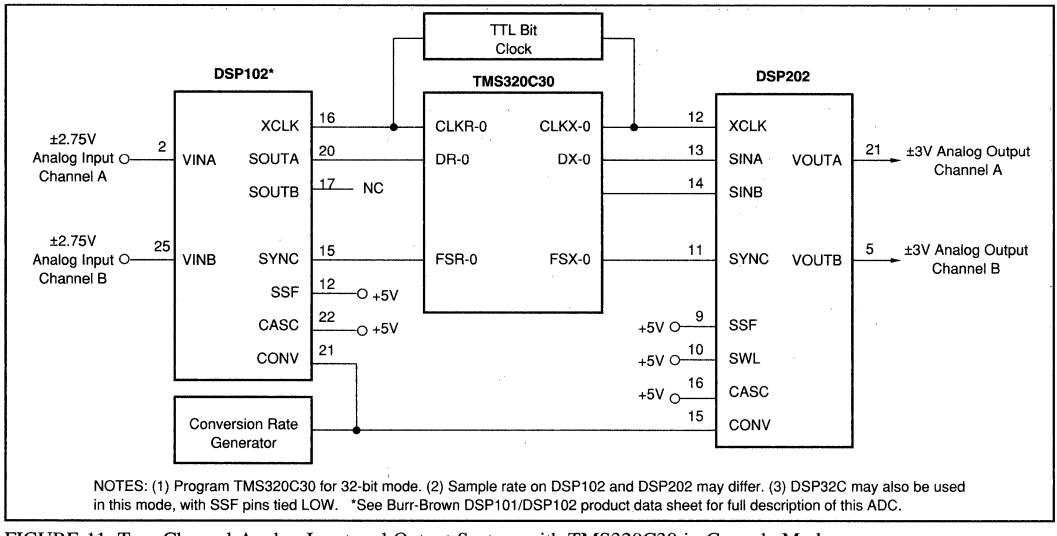
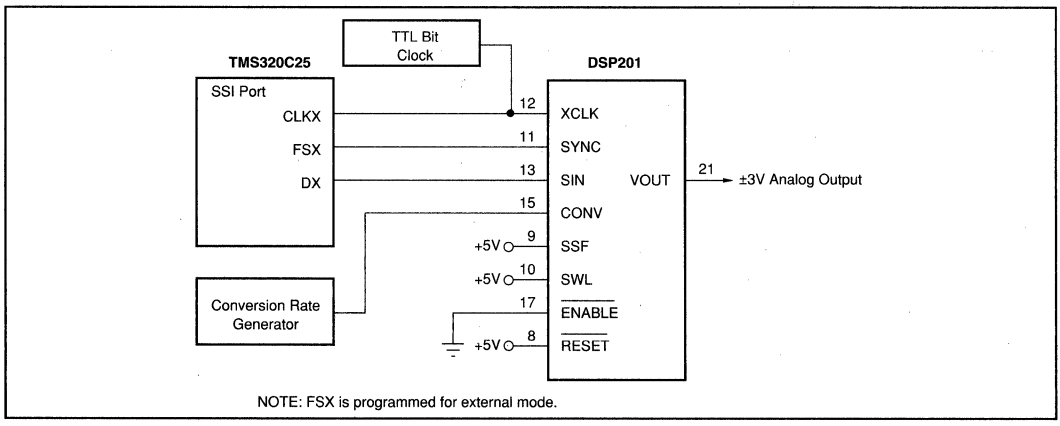


FIGURE 10. Two-Channel Analog Input and Output System with TMS320C30.



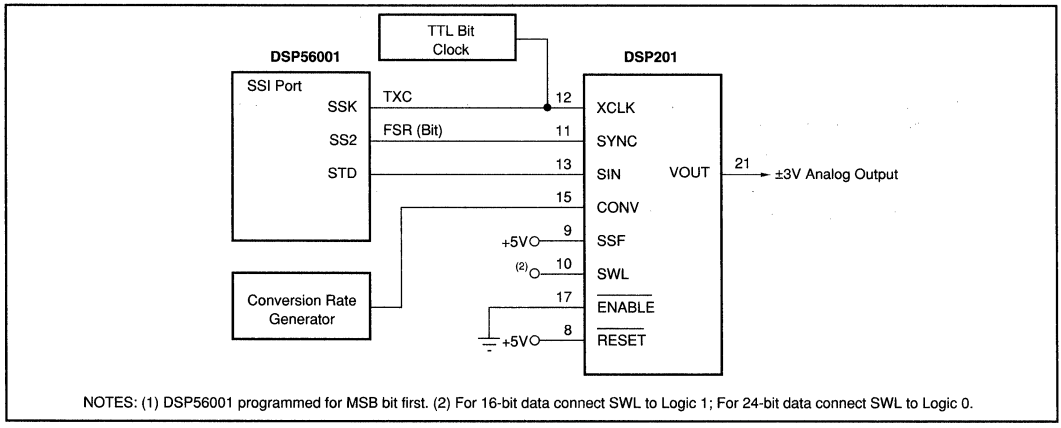
NOTES: (1) Program TMS320C30 for 32-bit mode. (2) Sample rate on DSP102 and DSP202 may differ. (3) DSP32C may also be used in this mode, with SSF pins tied LOW. *See Burr-Brown DSP101/DSP102 product data sheet for full description of this ADC.

FIGURE 11. Two-Channel Analog Input and Output System with TMS320C30 in Cascade Mode.



NOTE: FSX is programmed for external mode.

FIGURE 12. Using DSP201 with TMS320C25.



NOTES: (1) DSP56001 programmed for MSB bit first. (2) For 16-bit data connect SWL to Logic 1; For 24-bit data connect SWL to Logic 0.

FIGURE 13. Using DSP201 with DSP56001.

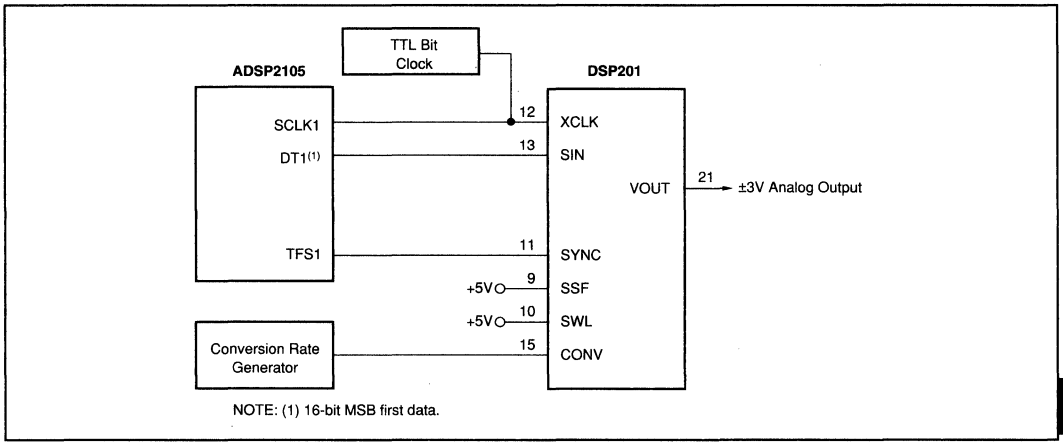


FIGURE 14. Using DSP201 with ADSP-2105.

USING DSP201 AND DSP202 WITH ADI DSP ICS

When using the DSP201 or DSP202 with the ADSP2101 or ADSP2105, the processors need to be programmed to transmit the data with the MSB first.

Figure 14 shows the connections required to generate an analog output channel using an ADSP2105 with the DSP201. The same basic circuit can also be used to connect a DSP201 to the ADSP2101.

Figure 6 indicates how to build a complete analog input and analog output system using either the ADSP2101 or ADSP2105 with a DSP201 and a Burr-Brown DSP101 A/D.

The two serial ports on the ADSP2101 can also be used with the DSP202 to make two complete analog output channels as noted in footnote 2 of Figure 10.

USING DSP201 AND DSP202 WITH AT&T DSP ICS

Figures 15, 16 and 17 show how to use the DSP201 and DSP202 with the DSP16 and DSP32C in different modes. The DSP IC needs to be programmed to transmit data with the MSB first, and the DSP201 or DSP202 needs to have SSF (Select Sync Format on pin 9) tied LOW so that the D/As will output an appropriate active Low synchronization pulse after a Convert Command is received.

Figures 15 and 17 show the DSP32C and DSP16 respectively used with the DSP201 in the 16-bit Mode to generate a single analog output channel. With a 12MHz Bit Clock and the 24 Bit Clock cycles required by the DSP201 and DSP202 between Convert Commands, the output of Figure 15 can be updated at a full 500kHz (12MHz/24 = 500kHz.)

Figure 16 shows how to drive two analog output channels from a single 32-bit serial port on the DSP32C, using the Cascade Mode on the DSP202. With a 12MHz Bit Clock and the 40 Bit Clock cycles required between Convert Commands by the DSP for internal logic overhead, this circuit can update two separate analog outputs at 300kHz each from a single serial port (12MHz/40 = 300kHz.)

Figure 6 indicates how to build a complete analog input and analog output system using a DSP32C or DSP16 with a DSP201 and a Burr-Brown DSP101 A/D.

Figure 7 shows a two channel analog output system using a single DSP202 with two DSP32Cs or two DSP16s.

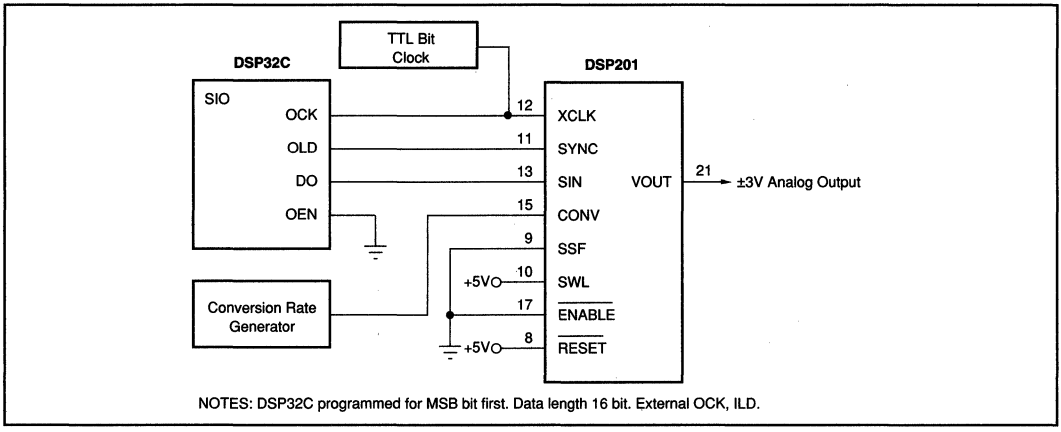


FIGURE 15. Using DSP201 with DSP32C with 16-Bit Data Words.

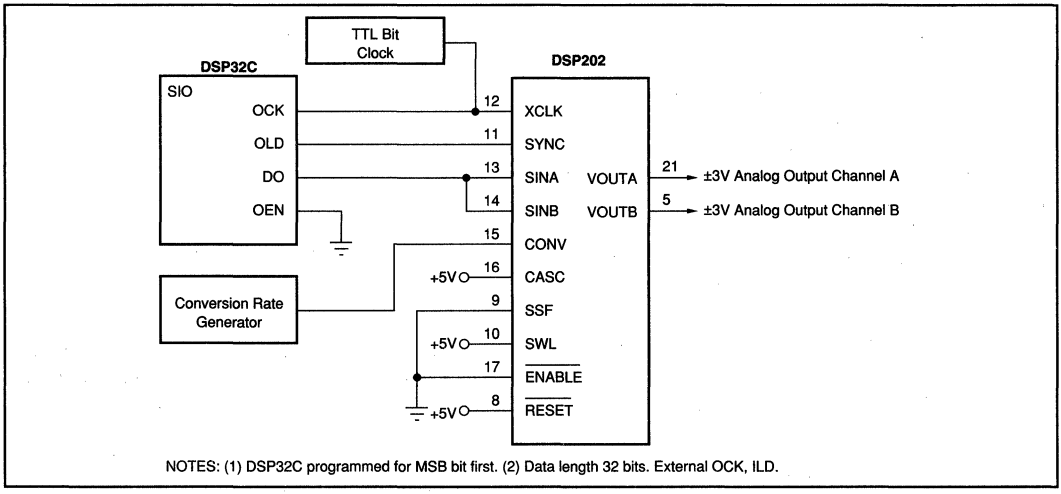


FIGURE 16. Using DSP202 with DSP32C in Cascade Mode.

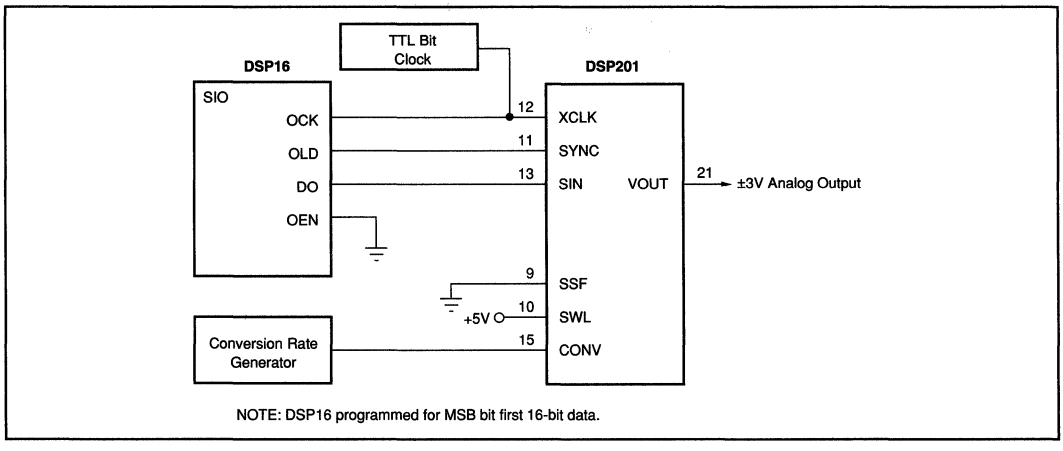


FIGURE 17. Using DSP201 with DSP16.

4 Digital Interface Products

DIGITAL COUPLER

Product	Isolation Voltage Cont Peak (Vrms)	Isolation Voltage Pulse Test Peak (V)	Leakage Current 240VAC 60Hz (μA)	Data Rate (MBd)	Power Consumption Per Channel max (mW)	Ext Power Req	Temp[1]	Pkg	Description
ISO150	1500	2400[2]	0.6	80	25	Yes	XInd	DIP, SOIC	Dual Isolated Transceiver
ISO485	1500	NS	NS	20	180 at 5MBit/s	Yes	XInd	DIP	RS-485 Transceiver

NOTES: (1) XInd = –40°C to +85°C. (2) Partial discharge test voltage, ac Vrms.

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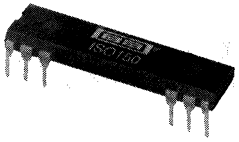


ISO150

Dual, Isolated, Bi-Directional DIGITAL COUPLER

FEATURES

- REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
- DATA RATE: 80M Baud, typ
- LOW POWER CONSUMPTION: 25mW Per Channel, max
- TWO CHANNELS, EACH BI-DIRECTIONAL, PROGRAMMABLE BY USER
- PARTIAL DISCHARGE TESTED: 2400Vrms
- CREEPAGE DISTANCE OF 16.5mm (DIP)
- LOW COST PER CHANNEL
- PLASTIC DIP AND SOIC PACKAGES

APPLICATIONS

- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- ISOLATED UART INTERFACE
- MULTIPLEXED DATA TRANSMISSION
- ISOLATED PARALLEL TO SERIAL INTERFACE
- TEST EQUIPMENT
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED LINE RECEIVER
- GROUND LOOP ELIMINATION

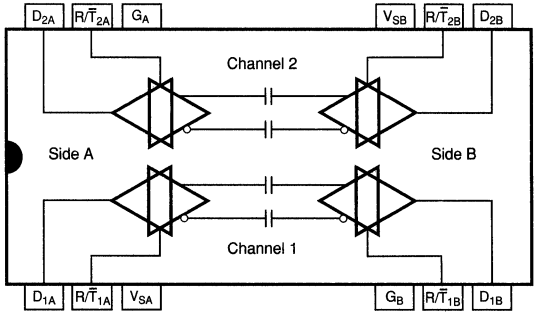
DESCRIPTION

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80MBaud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/µs.

ISO150 avoids the problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

ISO150 is available in a 24-pin DIP package and in a 28-lead SOIC. Both are specified for operation from –40°C to 85°C.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C and V_S = +5V, unless otherwise noted.

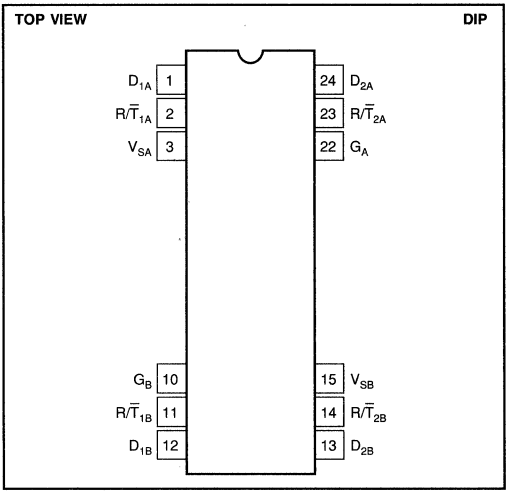
PARAMETER	CONDITION	ISO150AP, AU MIN	ISO150AP, AU TYP	ISO150AP, AU MAX	UNITS
ISOLATION PARAMETERS					
Rated Voltage, Continuous	60Hz	1500			Vrms
Partial Discharge, 100% Test(1)	1s, 5pC	2400			Vrms
Creepage Distance (External)					
DIP—"P" Package			16		mm
SOIC—"U" Package			7.2		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity(2)			1.6		kV/µs
Barrier Impedance			$>10^{14}$ || 7		Ω || pF
Leakage Current	240Vrms, 60Hz		0.6		µArms
DC PARAMETERS					
Logic Output Voltage, High, V_{OH}	I_{OH} = 6mA	V_S–1		V_S	V
Low, V_{OL}	I_{OL} = 6mA	0		0.4	V
Logic Output Short-Circuit Current	Source or Sink		30		mA
Logic Input Voltage, High(3)		2		V_S	V
Low(3)		0		0.8	V
Logic Input Capacitance			5		pF
Logic Input Current			<1		nA
Power Supply Voltage Range(3)		3	5	5.5	V
Power Supply Current(4)					
Transmit Mode	DC		0.001	100	µA
	50MBaud		14		mA
Receive Mode	DC		7.2	10	mA
	50MBaud		16		mA
AC PARAMETERS					
Data Rate, Maximum(5)	C_L = 50pF	50	80		MBaud
Data Rate, Minimum		DC			
Propagation Time(6)	C_L = 50pF	20	27	40	ns
Propagation Delay Skew(7)	C_L = 50pF		0.5	2	ns
Pulse Width Distortion(8)	C_L = 50pF		1.5	6	ns
Output Rise/Fall Time, 10% to 90%	C_L = 50pF		9	14	ns
Mode Switching Time					
Receive-to-Transmit			13		ns
Transmit-to-Receive			75		ns
TEMPERATURE RANGE					
Operating Range		–40		85	°C
Storage		–40		125	°C
Thermal Resistance, θ_{JA}			75		°C/W

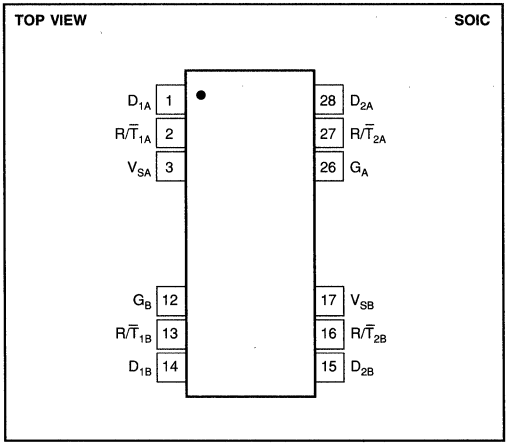
NOTES: (1) All devices receive a 1s test. Failure criterion is ≥5 pulses of ≥5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 0.4V hysteresis—see text. (4) Supply current measured with both tranceivers set for the indicated mode. Supply current varies with data rate—see typical curves. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from V_{IN} = 1.5V to V_O = 2.5V. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between progagation time of a rising edge and a falling edge.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–40°C to +125°C
Supply Voltages, V_S	–0.5 to 6V
Transmitter Input Voltage, V_I	–0.5 to V_S + 0.5V
Receiver Output Voltage, V_O	–0.5 to V_S + 0.5V
$R/\overline{T}_X$ Inputs	–0.5 to V_S + 0.5V
Isolation Voltage dV/dt, V_{ISO}	500kV/µs
D_X Short to Ground	Continuous
Junction Temperature, T_J	175°C
Lead Temperature (soldering, 10s)	260°C
1.6mm below seating plane (DIP package)	300°C

PIN CONFIGURATION





PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO150AP	24-Pin Single-Wide DIP	243-1
ISO150AU	28-Lead SOIC	217-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN DESCRIPTIONS

NAME	FUNCTION
D_{1A}	Data in or data out for transceiver 1A. $\overline{R}/T_{1A}$ held low makes D_{1A} an input pin.
$R/\overline{T}_{1A}$	Receive/Transmit switch controlling transceiver 1A.
V_{SA}	+5V supply pin for side A which powers transceivers 1A and 2A.
G_B	Ground pin for transceivers 1B and 2B.
$R/\overline{T}_{1B}$	Receive/Transmit switch controlling transceiver 1B.
D_{1B}	Data in or data out for transceiver 1B. $\overline{R}/T_{1B}$ held low makes D_{1B} an input pin.
D_{2B}	Data in or data out for transceiver 2B. $\overline{R}/T_{2B}$ held low makes D_{2B} an input pin.
$R/\overline{T}_{2B}$	Receive/Transmit switch controlling D_{2B}.
V_{SB}	+5V supply pin for side B which powers transceivers 1B and 2B.
G_A	Ground pin for transceivers 1A and 2A.
$R/\overline{T}_{2A}$	Receive/Transmit switch controlling transceiver 2A.
D_{2A}	Data in or data out for transceiver 2A. $\overline{R}/T_{2A}$ held low makes D_{2A} in input pin.

ELECTROSTATIC DISCHARGE SENSITIVITY

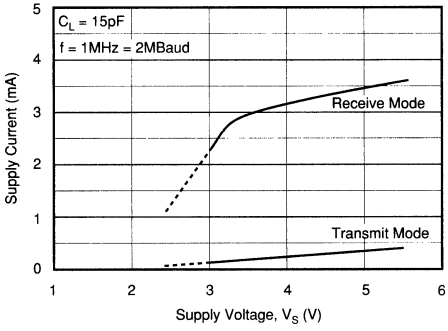
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

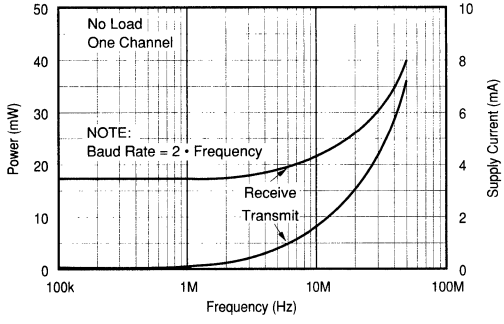
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +5V unless otherwise noted.

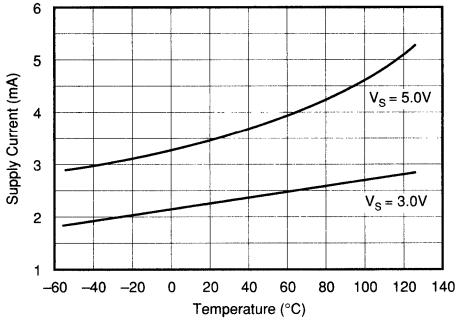
SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE



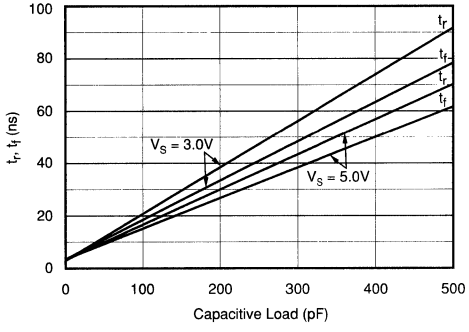
POWER CONSUMPTION PER CHANNEL vs FREQUENCY



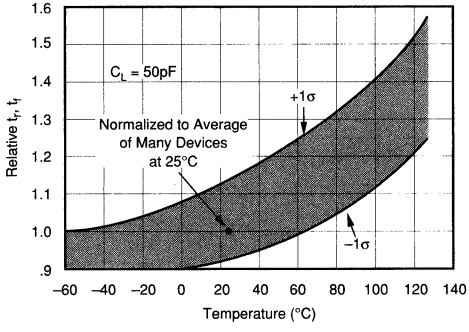
SUPPLY CURRENT PER CHANNEL vs TEMPERATURE



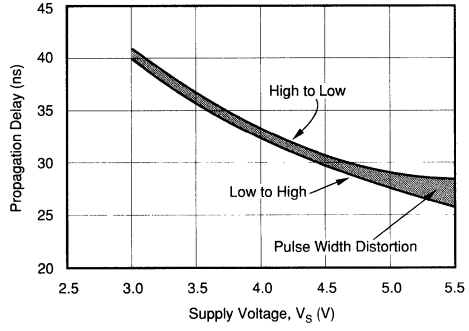
TYPICAL RISE AND FALL TIMES vs CAPACITIVE LOAD vs SUPPLY VOLTAGE



NORMALIZED RISE/FALL TIME vs TEMPERATURE



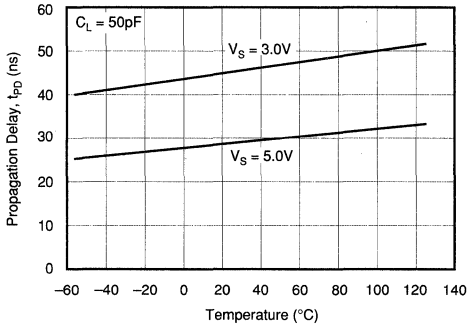
PROPAGATION DELAY vs SUPPLY VOLTAGE



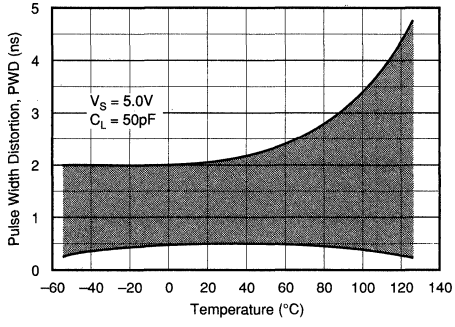
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = +5V, unless otherwise noted.

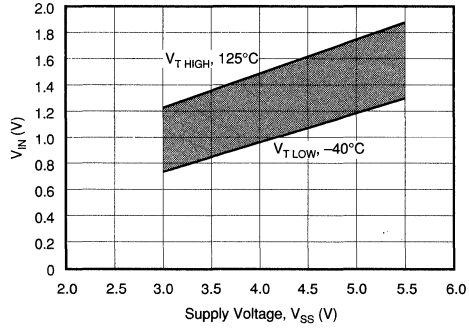
PROPAGATION DELAY vs TEMPERATURE



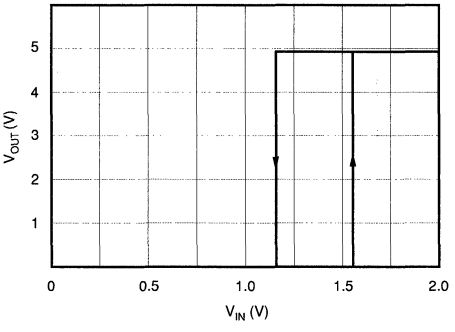
PULSE WIDTH DISTORTION vs TEMPERATURE



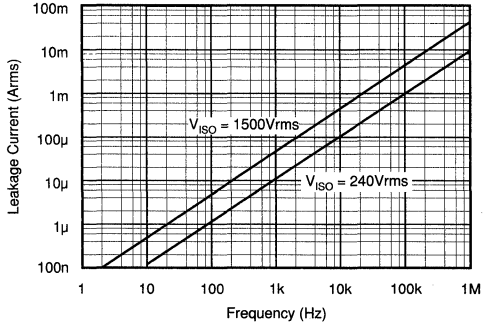
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



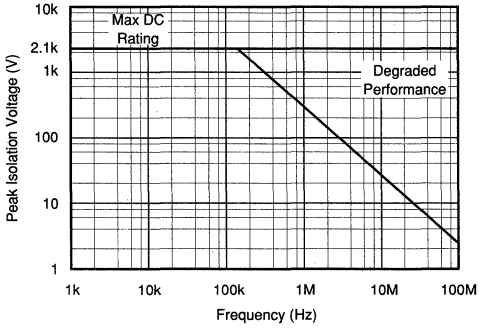
OUTPUT VOLTAGE vs LOGIC INPUT VOLTAGE



ISOLATION LEAKAGE CURRENT vs FREQUENCY

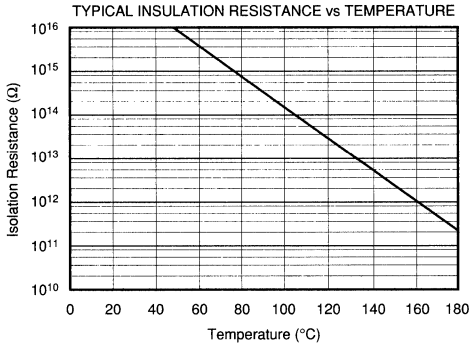


ISOLATION VOLTAGE vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = +5V, unless otherwise noted.



ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO150 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO150 is verified by partial discharge testing. 2400Vrms, 60Hz, is applied across the barrier for one second while measuring any tiny discharge currents that may flow through the barrier. These current pulses are produced by localized ionization within the barrier. This is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATIONS INFORMATION

Figure 1 shows the ISO150 connected for basic operation. Channel 1 is configured to transmit data from side B to A. Channel 2 is set for transmission from side A to B. The R/$\overline{T}$ pins for each of the four transceivers are shown connected to the required logic level for the transmission direction shown. The transmission direction can be controlled by logic signals applied to the R/$\overline{T}$ pins. Channel 1 and 2 can be independently controlled for the desired transmission direction.

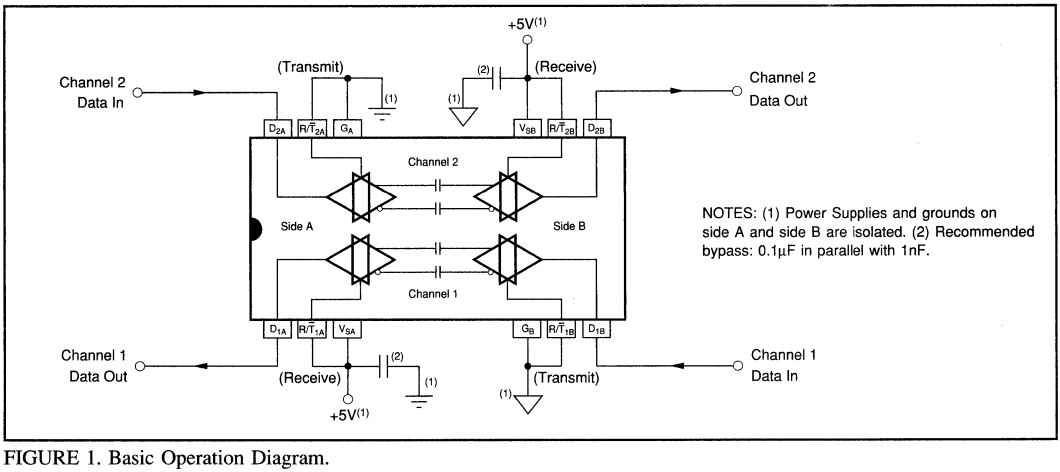


FIGURE 1. Basic Operation Diagram.

LOGIC LEVELS

A single pin serves as a data input or output, depending on the mode selected. Logic inputs are CMOS with thresholds set for TTL compatibility. The logic threshold is approximately 1.3V with 5V supplies and with approximately 400mV of hysteresis. Input logic thresholds vary with the power supply voltage. Drive the logic inputs with signals that swing the full logic voltage swing. The ISO150 will use somewhat greater quiescent current if logic inputs do not swing within 0.5V of the power supply rails.

In receive mode, the data output can drive 15 standard LS-TTL loads. It will also drive CMOS loads. The output drive circuits are CMOS.

POWER SUPPLY

Separate, isolated power supplies must be connected to side A and side B to provide galvanic isolation. Nominal rated supply voltage is 5V. Operation extends from 3V to 5.5V. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier.

The V_S pin for each side powers the transceivers for both channel 1 and 2. The specified supply current is the total of both transceivers on one side, both operating in the indicated mode. Supply current for one transceiver in transmit mode and one in receive mode can be estimated by averaging the specifications for transmit and receive operation. Supply current varies with the data transmission rate—see typical curves.

POWER-UP STATE

The ISO150 transmits information across the barrier only when the input-side data changes logic state. When a transceiver is first programmed for receive mode, or is powered-up in receive mode, its output is initialized "high". Subsequent changes of data applied to the input side will cause the output to properly reflect the input side data.

SIGNAL LOSS

The ISO150's differential-mode signal transmission and careful receiver design make it highly immune to voltage across the isolation barrier (isolation-mode voltage). Rapidly changing isolation-mode voltage can cause data errors. As the rate of change of isolation voltage is increased, there is a very sudden increase in data errors. Approximately 50% of ISO150s will begin to produce data errors with isolation-mode transients of 1.6kV/µs. This may occur as low as 500V/µs in some devices. In comparison, a 1000Vrms, 60Hz isolation-mode voltage has a rate of change of approximately 0.5V/µs.

Still, some applications with large, noisy isolation-mode voltage can produce data errors by causing the receiver output to change states. After a data error, subsequent changes in input data will produce correct output data.

PROPAGATION DELAY AND SKEW

Logic transitions are delayed approximately 27ns through the ISO150. Some applications are sensitive to data skew—the difference in propagation delay between channel 1 and channel 2. Skew is less than 2ns between channel 1 and channel 2. Applications using more than one ISO150 must allow for somewhat greater skew from device to device. Since all devices are tested for delay times of 20ns min to 40ns max, 20ns is the largest device-to-device data skew.

MODE CHANGES

The transmission direction of a channel can be changed "on the fly" by reversing the logic levels at the channel's $R/\overline{T}$ pins on both side A and side B. Approximately 75ns after the transceiver is programmed to receive mode its output is initialized "high", and will respond to subsequent input-side changes in data.

STANDBY MODE

Quiescent current of each transceiver circuit is very low in transmit mode when input data is not changing (1nA typical). To conserve power when data transmission is not required, program both side A and B transceivers for transmit mode. Input data applied to either transceiver is ignored by the other side. High speed data applied to either transceiver will increase quiescent current.

CIRCUIT LAYOUT

The high speed of the ISO150 and its isolation barrier require careful circuit layout. Use good high speed logic layout techniques for the input and output data lines. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier. Use low inductance connections. Ground planes are recommended.

Maintain spacing between side 1 and side 2 circuitry equal or greater than the spacing between the missing pins of the ISO150 (approximately 16mm for the DIP version). Sockets are not recommended.

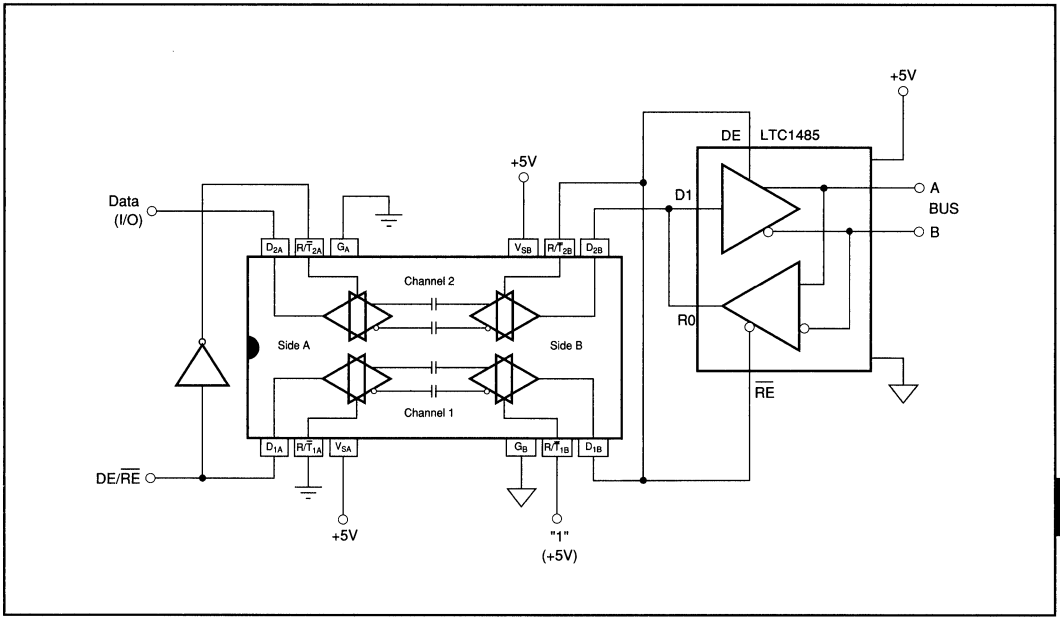


FIGURE 2. Isolated RS-485 Interface.

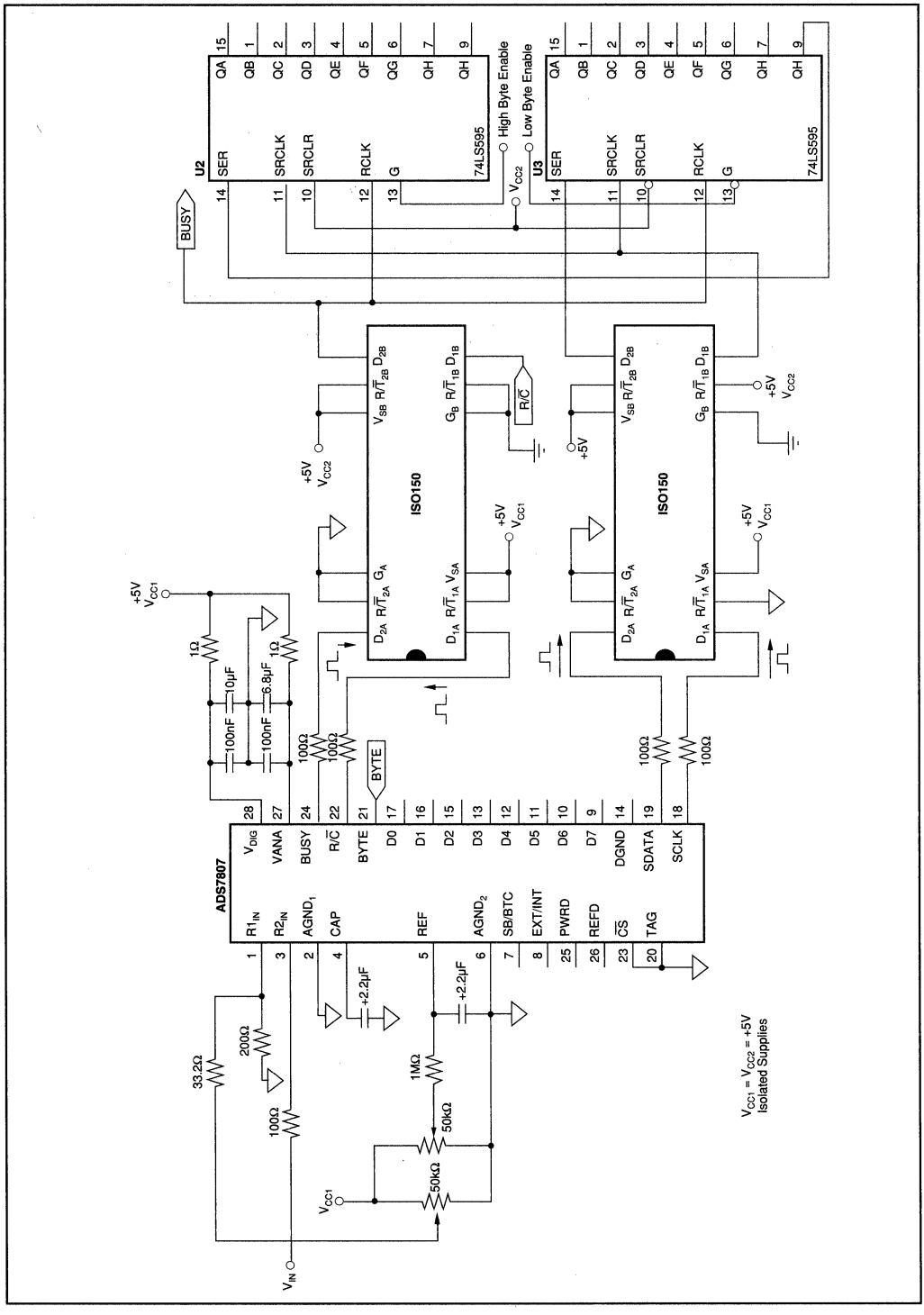


FIGURE 3. ISO150 and ADS7807 is Used to Reduce Circuit Noise in a Mixed Signal Application.

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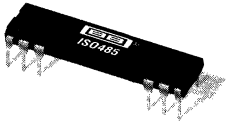


ISO485

Isolated RS-485 DIFFERENTIAL BUS TRANSCEIVER

FEATURES

- RS-485 AND RS-422 COMPATIBLE
- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- SINGLE-WIDE 24-PIN PLASTIC DIP
- EASY TO USE
- LOW POWER: 180mW typ at 5Mbit/s

APPLICATIONS

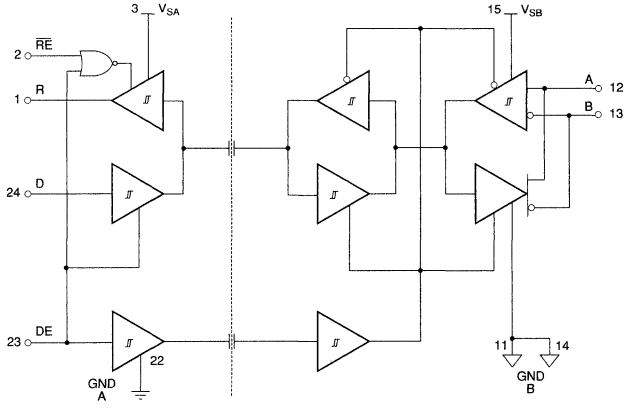
- MULTIPOINT DATA TRANSMISSION ON LONG BUS LINES IN NOISY ENVIRONMENTS

DESCRIPTION

The ISO485 differential, isolated bus transceiver uses Burr-Brown's capacitively coupled isolation technology to provide high-speed, low cost bus isolation. The ISO485 is designed for bi-directional data communication on multipoint bus transmission lines and meets EIA Standard RS-485 as well as EIA Standard RS-422A requirements.

The ISO485 uses high voltage 0.4pF capacitors instead of the LED and photodetector which are used in equivalent optocoupler solutions. As a consequence the part count of the isolated RS-485 channel is reduced from multiple optocoupler channels, an RS-485 transceiver chip and supporting circuitry to one ISO485. The capacitors in the ISO485 provide a high voltage barrier, 1500Vrms and greatly reduce current spikes on the power line.

The ISO485 combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5V power supply. The driver differential outputs and the receiver differential input/output bus ports are designed to offer minimum loading to the bus whenever the driver is disabled or V_S = 0V.



TRUTH TABLE

DE	$\overline{RE}$	RS-485 BUS
0	0	R_X
0	1	HIGH Z
1	0	HIGH Z
1	1	T_X

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C, V_S = 5V, unless otherwise specified.

PARAMETER	CONDITION	ISO485P MIN	ISO485P TYP	ISO485P MAX	UNITS
DRIVER DC CHARACTERISTICS					
Input Voltage					
High MIN				2	V
Low MAX		0.8			V
Input Current					
High-Level	V_{IN} = 2.4V			±1	µA
Low-Level	V_{IN} = 0.4V			±1	µA
Output Voltage	I_{OUT} = 0	0		5	V
Differential Output Voltage	$I_{OA} - I_{OB}$ = 0	1.5		5	V
	R_{LOAD} = 100Ω	2	2.5	5	V
	R_{LOAD} = 54Ω	1.5	2.5	5	V
Change In Magnitude of Differential Output Voltage	R_{LOAD} = 54Ω or 100Ω			±0.5	V
Common-Mode Output Voltage	R_{LOAD} = 54Ω or 100Ω			3	V
Change in Magnitude of Common-Mode Output Voltage	R_{LOAD} = 54Ω or 100Ω			±0.2	V
Output Current	V_{OUT} = 7V, output disabled			1	mA
	V_{OUT} = –7V, output disabled			–0.8	mA
Short-Circuit Output Current (1 sec max)	V_{OUT} = –7V		–250		mA
	V_{OUT} = 0V		–150		mA
	V_{OUT} = V_S		250		mA
	V_{OUT} = 12V		250		mA
DRIVER SWITCHING CHARACTERISTICS					
Propagation Delay Time, Low-to-High Level Output	R_{LOAD} = 54Ω			60	ns
Propagation Delay Time, High-to-Low Level Output	R_{LOAD} = 54Ω			60	ns
Input to Output Propagation Delay Skew	R_{LOAD} = 54Ω		10		ns
Output Rise Time	R_{LOAD} = 54Ω		10		ns
Output Fall Time	R_{LOAD} = 54Ω		10		ns
RECEIVER DC CHARACTERISTICS					
Differential-Input-Threshold Voltage					
High	V_{OUT} = 2.7V, I_{OUT} = –0.4mA			0.2	V
Low	V_{OUT} = 0.5V, I_{OUT} = 8mA	–0.2			V
Hysteresis			70		mV
High-Level Output Voltage	V_{ID} = 200mV, I_{OH} = 400µA	2.4			V
Low-Level Output Voltage	V_{ID} = 200mV, I_{OL} = 8mA			0.4	V
High-Impedance-State Output Current	V_{OUT} = 1.4V			±1	µA
Line Input Current	V_{IN} = 12V, other output = 0V		0.7		mA
	V_{IN} = –7V, other output = 0V		–0.6		mA
Enable-Input Current					
High	V_{IH} = 2.7V			1	µA
Low	V_{IL} = 0.4V			1	µA
Input Resistance		12			kΩ
Short-Circuit Output Current	1 sec max		40		mA
RECEIVER SWITCHING CHARACTERISTICS					
Propagation Delay Time, Low-to-High Level Output	V_{ID} = –1.5V to 1.5V, C_L = 15pF		35	60	ns
Propagation Delay Time, High-to-Low Level Output	V_{ID} = –1.5V to 1.5V, C_L = 15pF		30	60	ns
Input to Output Propagation Delay Skew			10		ns
Output Rise Time	R_L = 54Ω		8		ns
Output Fall Time	R_L = 54Ω		8		ns
TRANSCEIVER SPECIFICATIONS					
Maximum Data Rate		20	35		Mbits/s
Propagation Delay Driver to Receiver			75		ns
Driver Output Enable Time	R_L = 110Ω		155	200	ns
Driver Output Disable Time	R_L = 110Ω		185	280	ns
Propagation Delay Receiver to Driver			13		ns
Receiver Output Enable Time	C_L = 15pF		110	180	ns
Receiver Output Disable Time	C_L = 15pF		120	185	ns

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = 5V, unless otherwise specified.

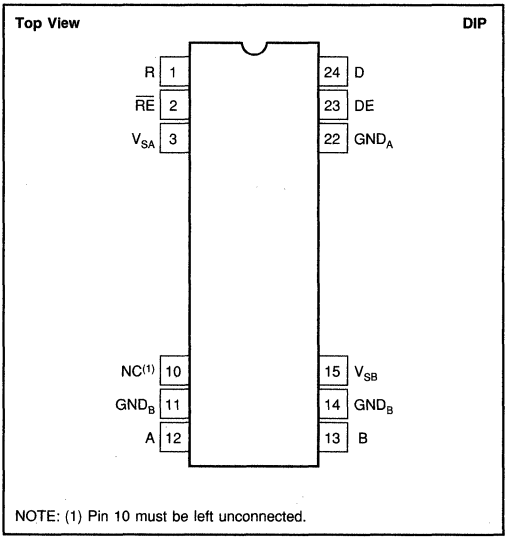
PARAMETER	CONDITION	ISO485P MIN	ISO485P TYP	ISO485P MAX	UNITS
TRANSCEIVER SPECIFICATIONS (CONT)					
Supply Voltage					
V_SA		3	5	5.5	V
V_SB		4.75	5	5.25	V
Supply Current	DE RE RS-485 BUS				
V_SA	0 0 Rx			5	mA
V_SA	0 1 HIGH Z			0.4	mA
V_SA	1 0 HIGH Z			0.4	mA
V_SA	1 1 Tx			0.4	mA
V_SB	0 0 Rx			55	mA
V_SB	0 1 HIGH Z			55	mA
V_SB	1 0 HIGH Z			51	mA
V_SB	1 1 Tx			51	mA
RECOMMENDED OPERATING CONDITIONS					
Voltage at Any Bus Terminal	(separately or common-mode)	–7		12	V
High-Level Driver Input Voltage		2			V
Low-Level Driver Input Voltage				0.8	V
Differential Receiver Input Voltage				±12	V
Output Current High-Level					
	Driver			–60	mA
	Receiver			–400	µA
Output Current Low-Level					
	Driver			60	mA
	Receiver			8	mA
TEMPERATURE RANGE					
Operating		–40		85	°C
Storage		–40		125	°C
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test[1]	1s, 5pC	2400			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity[2]			1.6		kV/µs
Barrier Impedance			$> 10^{14}$ || 7		Ω || pF
Leakage Current	240Vrms, 60Hz		0.6		µArms

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages, V_S	5.5V
Voltage at any bus terminal	−10 to 15V
Enable Input Voltage	0 to V_{CC} + 0.5V
Continuous total dissipation at 25°C free-air temp.	750mW
Lead solder temperature, 260°C for 10s, 1.6mm below seating plane	300°C
Junction Temperature	150°C
Package thermal transfer, θ_{JA}	75°C/W

PIN CONFIGURATION



NOTE: (1) Pin 10 must be left unconnected.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO485P	24-Pin Single-Wide DIP	243-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R	Data Received From Transmission Line
2	$\overline{RE}$	Receive Switch Controlling Receiving Of Data
3	V_{SA}	+5V Supply Pin For Side A
10	NC	This Pin MUST Be Left Unconnected
11	GND_B	Ground Pin For Side B. Also Connected To Pin 14
12	A	Data, Driver Out/Receiver In
13	B	Data, Driver Out/Receiver In
14	GND_B	Ground Pin For Side B. Also Connected To Pin 11
15	V_{SB}	+5V Supply Pin For Side B
22	GND_A	Ground Pin For Side A
23	DE	Driver Switch Controlling Output Of Data
24	D	Data To Be Transmitted

ELECTROSTATIC DISCHARGE SENSITIVITY

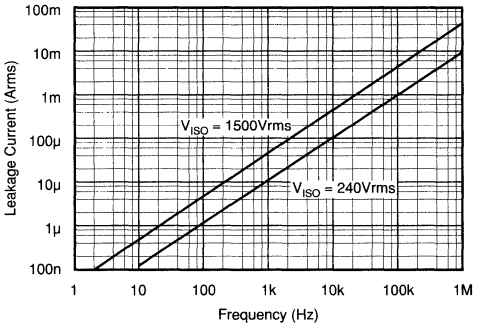
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

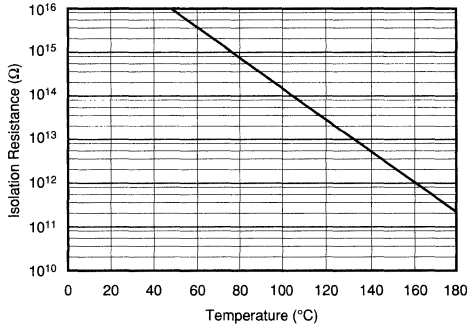
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, unless otherwise noted.

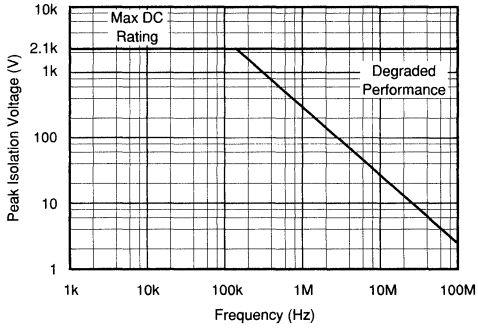
ISOLATION LEAKAGE CURRENT vs FREQUENCY



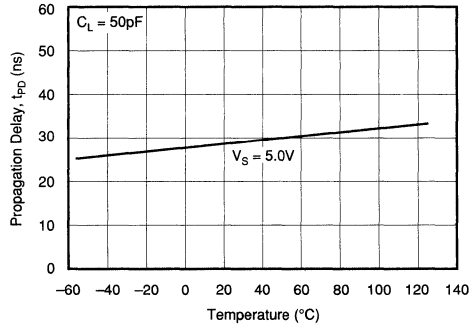
TYPICAL INSULATION RESISTANCE vs TEMPERATURE



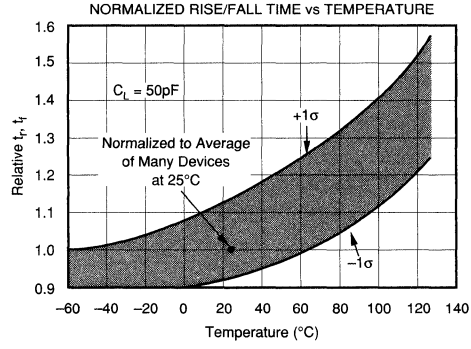
ISOLATION VOLTAGE vs FREQUENCY



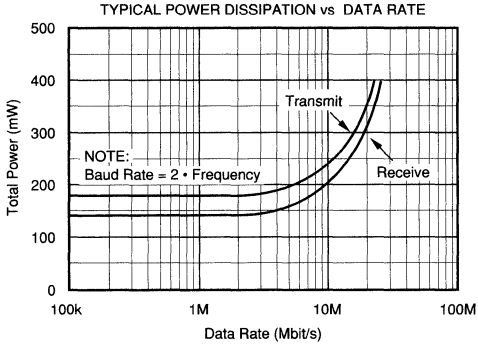
PROPAGATION DELAY vs TEMPERATURE



NORMALIZED RISE/FALL TIME vs TEMPERATURE



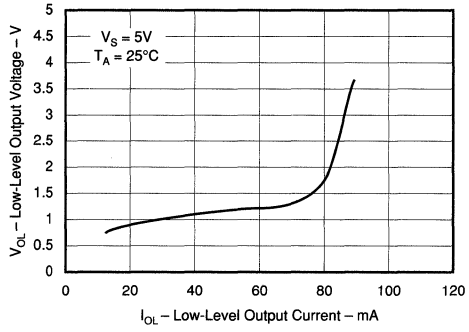
TYPICAL POWER DISSIPATION vs DATA RATE



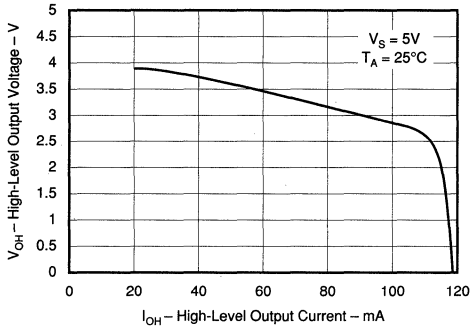
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

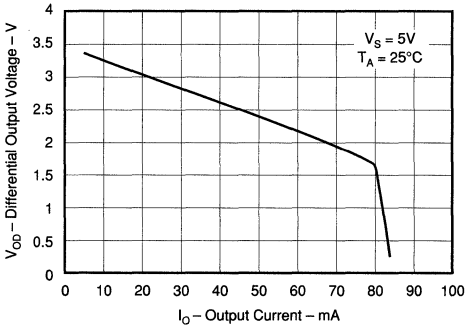
OUTPUT LOW VOLTAGE vs
DRIVER OUTPUT CURRENT



OUTPUT HIGH VOLTAGE vs
DRIVER OUTPUT CURRENT



OUTPUT VOLTAGE vs
DRIVER OUTPUT CURRENT



MODE OF OPERATION

The ISO485 is a differential, isolated transceiver for half duplex multi-point communication, and complies with the EIA Interface Standards summarized in Table I. The signals transmitted across the isolation barrier can achieve transmission rates up to 35Mbit/s typical. The barrier is designed to perform in harsh electrical environments without signal degradation, while providing high isolation and good transient immunity.

Referring to the block diagram on the front page, data present at the D input can be transmitted across the barrier when the data enable pin DE is a logic high. The data appears as a differential signal on the outputs A and B and within the output range 0V to +5V. The isolated side of the DE logic high also inhibits the isolated side of data read R. The input NOR gate arrangement prevents attempts to transmit and receive simultaneously. The truth table shows the conditions on the RS-485 bus for the possible states of DE and $\overline{RE}$.

ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO485 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO485 is verified by partial discharge testing. 2400Vrms, 50Hz, is applied across the barrier for one second while measuring any tiny discharge currents that may flow through the barrier. These current pulses are produced by localized ionization within the barrier. This is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATION EXAMPLE

Consider an RS-485 network in an industrial area. The system specifications are:

- Distance between master controller and the farthest outstation 50 meters.
- System data rate is to be 30Mbit/s.
- One daisy-chain cable will link the master controller to the outstations.

The main design considerations in implementing this system are:

- Line loading and termination
- Selection of correct cable for requirements
- Attenuation and distortion of the signal
- Fault protection and fail-safe operation

LOADING

RS-485 recommends a maximum of 32 unit loads on any one line: the unit loading being derived from the 12kΩ input impedance and the 12V maximum common-mode voltage. The ISO485 represents 1 unit load. We could, therefore, connect up to 31 outstations to the master controller and comply with the specification.

TERMINATION

When a signal starts to change at the output of a transmitter, the other end of the line will eventually see this change and a reflection will occur. If this reflection returns to the transmitter before the transmitted signal has reached its maximum value, the line may be considered as a "lumped parameter" model. In this case no termination is necessary because the line has a negligible effect on the system.

If the rise of the signal at the receiver T_{RISE} is much less than the time taken for the signal to go from transmitter to receiver and back again $2T_{PD}$ termination of the line is necessary. It is usual to terminate the line with its characteristic impedance, Z_O when the following rule applies:

$$2T_{PD} \geq 5T_{RISE} \quad (1)$$

For this installation we have selected an Alpha Wire Corporation cable, No. 6072C. The cables characteristics are shown in Figure 2. The rise time T_{RISE} at the receiver was measured between the 10% and 90% points.

$$T_{RISE} = 10ns \quad (2)$$

From Figure 1 we can see that the velocity of propagation V_P is given as 80%. Since this is the ratio of the signal speed in air, to the signal speed in the cable, we have

$$V_P = 3 \times 10^8 \times 0.8 = 2.4 \times 10^8 \text{ m/s} \quad (3)$$

therefore $T_{PD} = 1/V_P = 4.2\text{ns/m}$

For the cable $2T_{PD} = 4.2 \times 10^{-9} \times 50 \times 2 = 42\text{us}$

Equation 1 holds, therefore the line must be terminated with its characteristic impedance.

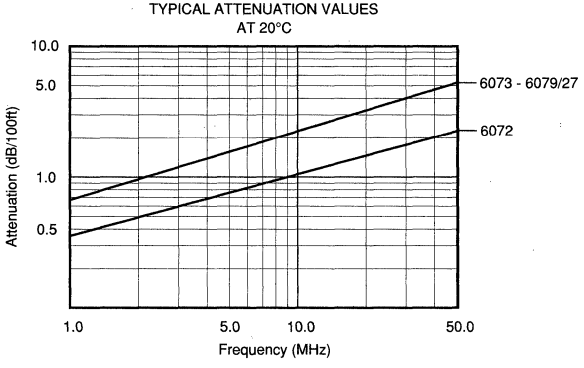
EYE PATTERNS AND Z_O

Eye patterns can be used to assess the signal distortion and noise on the transmission line. It is also a convenient method of determining the characteristic impedance of the line. The term 'eye' comes from the shape of the trace on the oscilloscope. See Figures 2 and 3.

The eye pattern was obtained using the non return zero pseudo-noise generator circuit shown in Figure 5. Figure 2 shows the effects of the termination resistor for the three cases: $Z_T > Z_O$, $Z_T = Z_O$, $Z_T < Z_O$ with $Z_T = Z_O$ the eye

pattern is clear. In practice a precision decade resistance box was used to determine the exact value of Z_T to use.

As the data rate is increased we can see from Figure 3 how the signal distortion also increases. From the graph in Figure 1 we can see that the specified attenuation figures given agree with those obtained by measurement; approximately –1.3db/100ft, at 30Mbit/s (15MHz).



TYPICAL ELECTRICAL CHARACTERISTICS

Capacitance

ALPHA WIRE CORP. NO.	CDR. to CDR.		CDR. to (CDR. AND SHIELD)		VP.	Z_0 at 1MHz,
	pF/ft	(pF/m)	pF/ft	pF/m)	%	Ω
6072C	8.7	(28, 5)	5.9	(52, 2)	80	150
6073C thru 6079/27C	12.5	(41, 0)	22.0	(72, 5)	80	150

FIGURE 1. Cable Characteristics.

PARAMETER		EIA-232	RS-432-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20k	100k	10M	10M
Maximum Common-Mode Voltage (V)		±25	±6	6 to –0.25	12 to –7
Driver Output	Loaded	±5	±3.6	±2	±1.5
Levels (V)	Unloaded	±15	±6	±5	±5
Driver Load (Ω)		3k to 7k	450 (min)	100 (min)	60 (min)
Driver Slew Rate		30V/µs (max)	External Control	NA	NA
Driver Output Short Circuit		500 to V_{CC}	150 to GND	150 to GND	150 to GND
Current Limit (mA)					250 to –7 or 12V
Driver Output Resistance	Power on	NA	NA	NA	12k
High Z state (Ω)	Power off	300	60k	60k	12k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3V	±200mV	±200mV	±200mV

TABLE I. Summary of EIA Interface Standards.

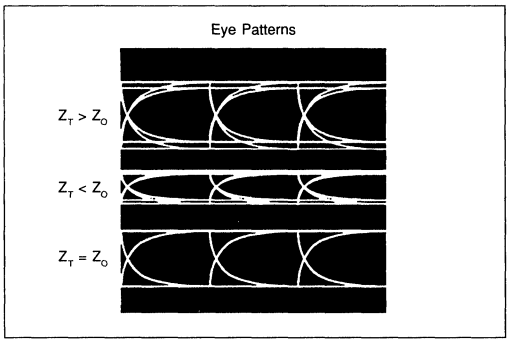


Figure 2. Eye Patterns.

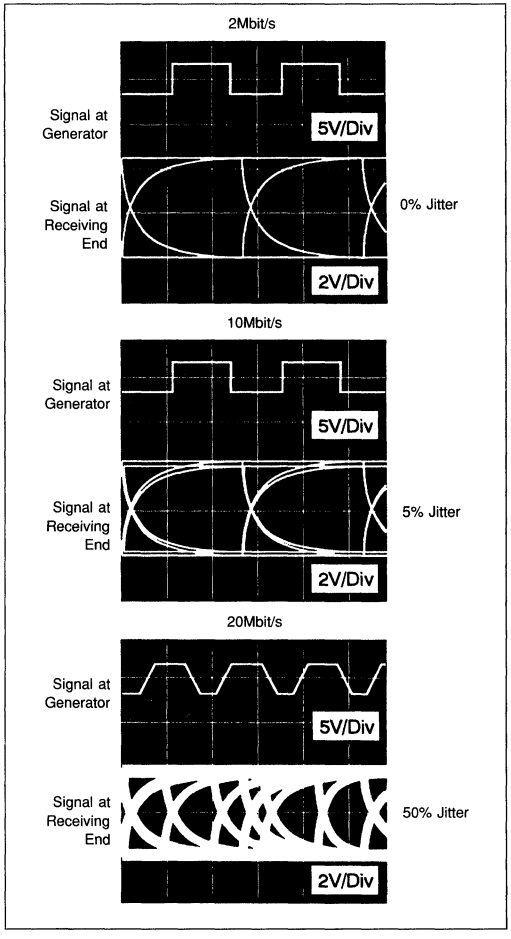


Figure 3. ISO485 Signal Distortion vs Data Rate.

STUB LENGTH

If the outstations are not to act as transmission lines, they too must meet the criteria determined by equation 1. They must be seen as a lumped parameter. As a rule-of-thumb, the transition time of the pulse from the transmitter, T_{RISE} should be ten times longer than the propagation delay, pd_{STUB} down the stub to the outstation.

$$T_{RISE} \geq 10pd_{STUB} \quad (4)$$

From $pd = 1/V_P \times \text{stub length}$

$$T_{RISE} \geq 10 \times 1/V_P \times \text{stub length}$$

$$16.5 \times 10^{-9} \geq 10 \times \frac{1}{3 \times 10^8 \times 0.8} \times \text{stub length}$$

Therefore stub length = 396mm (15.6") maximum

START-UP CIRCUIT

Because the ISO485 is a capacitively coupled device, it is possible to power up an indeterminate state. The circuit of Figure 4 ensures that the ISO485 powers up in the receive mode, thus avoiding any conflict on the transmission line.

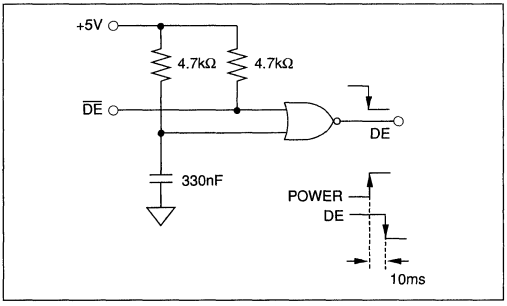


Figure 4. Start-up Circuit.

TRANSMIT/RECEIVE MODE

Because the ISO485 is a capacitively coupled device, indeterminate states can occur when the change from transmit to receive or, from receive to transmit is initiated. This is easily overcome by transmitting an edge prior to the data of interest. The four possible conditions which could happen are detailed in Figures 5a, 5b, 6a, and 6b. Thereafter, data is known and correct.

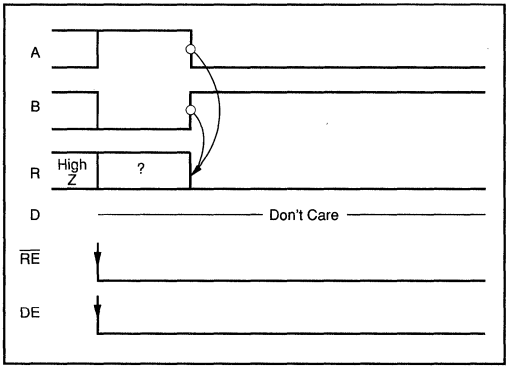


Figure 5a. Transmit to Receive.

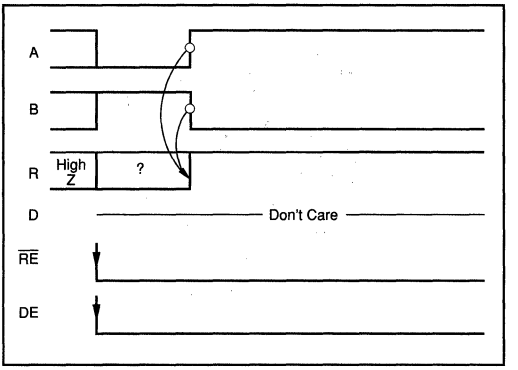


Figure 5b. Transmit to Receive.

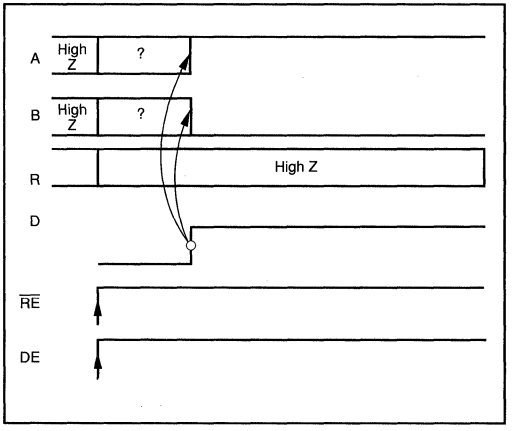


Figure 6a. Receive to Transmit

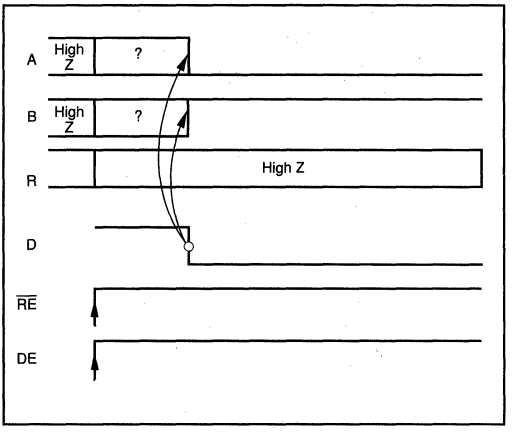


Figure 6b. Receive to Transmit.

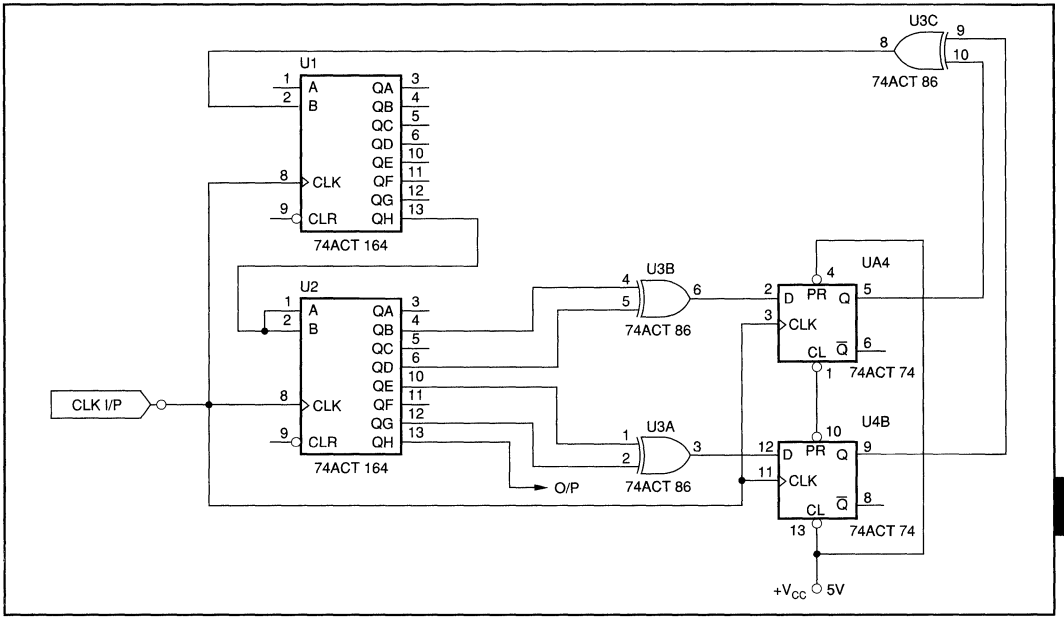
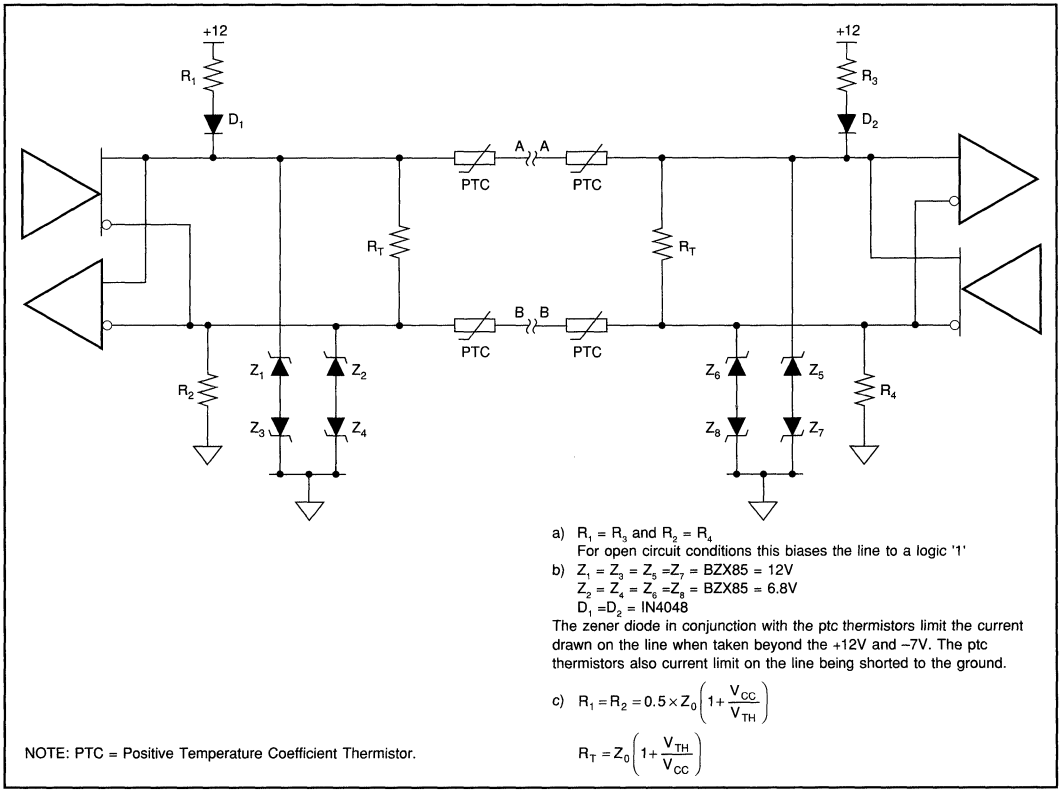


FIGURE 7. NRZ Psuedo-Noise Generator.



a) $R_1 = R_3$ and $R_2 = R_4$
For open circuit conditions this biases the line to a logic '1'

b) $Z_1 = Z_3 = Z_5 = Z_7$ = BZX85 = 12V
$Z_2 = Z_4 = Z_6 = Z_8$ = BZX85 = 6.8V
$D_1 = D_2$ = IN4048
The zener diode in conjunction with the ptc thermistors limit the current drawn on the line when taken beyond the +12V and –7V. The ptc thermistors also current limit on the line being shorted to the ground.

c) $R_1 = R_2 = 0.5 \times Z_0 \left(1 + \frac{V_{CC}}{V_{TH}}\right)$

$R_T = Z_0 \left(1 + \frac{V_{TH}}{V_{CC}}\right)$

NOTE: PTC = Positive Temperature Coefficient Thermistor.

FIGURE 8. RS-485 Line with Fail-Safe Protection.

5 Multiplexers

Burr-Brown analog multiplexers provide one of the most cost effective methods of achieving multiple-channel signal distribution. Single-ended and differential channel versions are available in both ceramic and plastic packages.

These high speed multiplexers are input protected and can withstand voltages of 70Vp-p without damaging the device. Full ±15V input range is provided on all devices.

MPC506	16 to 1 mux	single-ended
MPC507	8 to 1 mux	differential
MPC508	8 to 1 mux	single-ended
MPC509	4 to 1 mux	differential

ANALOG MULTIPLEXER
(Input, Settling Time, max)

16-CHANNEL
MPC506 (Single, 3.5µs)
MPC800 (Single, 800ns)

8-CHANNEL
MPC507 (Diff, 3.5µs)
MPC508 (Single, 3.5µs)

4-CHANNEL
MPC509 (Diff, 3.5µs)
MPC100 (Single, 450MHz)

2-CHANNEL
MPC104 (Single, 590MHz)
MPC102 (Single, 370MHz, Dual)

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

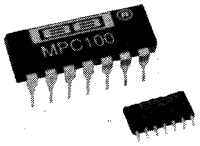
Product	Channels	Input Range (V)	On Resistance max (Ω)	Small Signal Bandwidth	Settling Time (to 0.01%)	Temp Range[1]	Pkg[2]	Description
MPC100AP	4-channel, single ended	±4.2	0.88M	450MHz	—	Ext	14-p PDIP	Buffered 4 x 1
MPC100AU	4-channel, single ended	±4.2	0.88M	450MHz	—	Ext	14-p SOIC	Buffered 4 x 1
MPC102AP	dual 2-channel, single ended	±3.6	0.88M	370MHz	—	Ext	14-p PDIP	Buffered Dual 2 x 1
MPC102AU	dual 2-channel, single ended	±3.6	0.88M	370MHz	—	Ext	14-p SOIC	Buffered Dual 2 x 1
MPC104AP	2-channel, single ended	±3.6	0.88M	590MHz	—	Ext	8-p PDIP	Buffered 2 x 1
MPC104AU	2-channel, single ended	±3.6	0.88M	590MHz	—	Ext	8-p SOIC	Buffered 2 x 1
MPC506AP	16-channel, single ended	±15	1.8k	—	3.5µs	Ext	28-p PDIP	Protected Inputs, CMOS
MPC506AG	16-channel, single ended	±15	1.8k	—	3.5µs	Ext	28-p CDIP	Protected Inputs, CMOS
MPC506AU	16-channel, single ended	±15	1.8k	—	3.5µs	Ext	29-p SOIC	Protected Inputs, CMOS
MPC507AP	8-channel, differential	±15	1.8k	—	3.5µs	Ext	28-p PDIP	Protected Inputs, CMOS
MPC507AG	8-channel, differential	±15	1.8k	—	3.5µs	Ext	28-p CDIP	Protected Inputs, CMOS
MPC507AU	8-channel, differential	±15	1.8k	—	3.5µs	Ext	28-p SOIC	Protected Inputs, CMOS
MPC508AP	8-channel, single ended	±15	1.8k	—	3.5µs	Ext	16-p PDIP	Protected Inputs, CMOS
MPC508AG	8-channel, single ended	±15	1.8k	—	3.5µs	Ext	16-p CDIP	Protected Inputs, CMOS
MPC508AU	8-channel, single ended	±15	1.8k	—	3.5µs	Ext	16-p SOIC	Protected Inputs, CMOS
MPC509AP	4-channel, differential	±15	1.8k	—	3.5µs	Ext	16-p PDIP	Protected Inputs, CMOS
MPC509AG	4-channel, differential	±15	1.8k	—	3.5µs	Ext	16-p CDIP	Protected Inputs, CMOS
MPC509AU	4-channel, differential	±15	1.8k	—	3.5µs	Ext	16-p SOIC	Protected Inputs, CMOS
MPC800KG	16 single or 8 differential	±15	750	—	800ns	Com	CDIP	High Speed, CMOS
MPC801KG	8 single or 4 differential	±15	750	—	800ns	Com	CDIP	High Speed, CMOS

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ext = –40°C to +85°C, Mil = –55°C to +125°C. (2) CDIP = Ceramic DIP, PDIP = Plastic DIP.

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

BURR-BROWN®



MPC100

Wide Bandwidth 4 x 1 VIDEO MULTIPLEXER

FEATURES

- **BANDWIDTH: 250MHz (1.4Vp-p)**
- **LOW INTERCHANNEL CROSSTALK: ≤60dB (30MHz, DIP); ≤70dB (30MHz, SO)**
- **LOW SWITCHING TRANSIENTS: +2.5/–1.2mV**
- **LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.05%, 0.01°**
- **LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±230µA**

APPLICATIONS

- **VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)**
- **RADAR SYSTEMS**
- **DATA ACQUISITION**
- **INFORMATION TERMINALS**
- **SATELLITE OR RADIO LINK IF ROUTING**

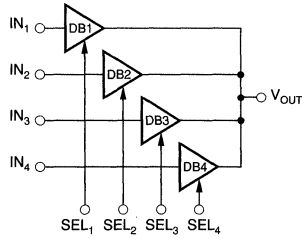
DESCRIPTION

The MPC100 is a very wide bandwidth 4 to 1 channel Video Signal Multiplexer which can be used in a wide variety of applications.

MPC100 is designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC100 make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC100 consists of four identical monolithic integrated open-loop buffer amplifiers, which are connected internally at the output. The unidirectional transmission path consists of bipolar complementary buffers, which offer extremely high output-to-input isolation. The MPC100 multiplexer enables one of the four input channels to connect to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL-input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 250MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in space-saving SO-14 and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)



TRUTH TABLE

SEL_1	SEL_2	SEL_3	SEL_4	V_{OUT}
0	0	0	0	HI-Z
1	0	0	0	IN_1
0	1	0	0	IN_2
0	0	1	0	IN_3
0	0	0	1	IN_4

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At V_{CC} = ±5V, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP, AU MIN	MPC100AP, AU TYP	MPC100AP, AU MAX	UNITS
INPUT OFFSET VOLTAGE	R_{IN} = 0, R_{SOURCE} = 0				
Initial			+10	±30	mV
vs Temperature			±30		µV/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V	–40	–80		dB
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		–50		dB
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–50		dB
Initial Matching	Between the Four Channels		±3		mV
INPUT BIAS CURRENT					
Initial			+4	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V		±380		nA/V
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		+1.0		µA/V
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–11.0		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	f_B = 20kHz to 10MHz		4.0		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/V_N • √5MHz		–98		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±4.2		V
TRANSFER CHARACTERISTICS	Voltage Gain				
	R_L = 1kΩ, V_{IN} = ±2V		0.982		V/V
	R_L = 10kΩ, V_{IN} = ±2.8V	0.98	0.992		V/V
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2.0		V_{CC}	V
Logic 0 Voltage		0		+0.8	V
Logic 1 Current	V_{SEL} = 5.0V		100	150	µA
Logic 0 Current	V_{SEL} = 0.8V		0.002	5	µA
SWITCHING CHARACTERISTICS	V_I = –0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_O = 1Vp-p		0.25		µs
SEL to Channel OFF Time	10% Point of V_O = 1Vp-p		0.25		µs
Switching Transient, Positive	Measured While Switching		+2.5		mV
Switching Transient, Negative	Between Two Grounded Channels		–1.2		mV
OUTPUT					
Voltage	V_{IN} = ±3V, R_L = 5kΩ	±2.8	±2.98		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6	±5	mA
	No Channel Selected		±230	±350	µA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			90		°C/W

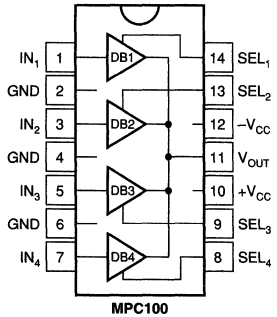
SPECIFICATIONS

At V_{CC} = ±5V, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP, AU MIN	MPC100AP, AU TYP	MPC100AP, AU MAX	UNITS
AC CHARACTERISTICS					
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH (–3dB)	V_O = 5.0Vp-p, C_{OUT} = 1pF V_O = 2.8Vp-p, C_{OUT} = 1pF V_O = 1.4Vp-p, C_{OUT} = 1pF		70 140 250		MHz MHz MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, C_{OUT} = 1pF		450		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_{IN} = 0.3Vp-p VDC = 0 to 0.7V VDC = 0 to 1.4V		 0.05 0.06		 % %
DIFFERENTIAL PHASE	f = 4.43MHz, V_{IN} = 0.3Vp-p VDC = 0 to 0.7V VDC = 0 to 1.4V		 0.01 0.02		 Degrees Degrees
GAIN FLATNESS PEAKING	V_O = 0.2Vp-p, DC to 30MHz V_O = 0.2Vp-p, DC to 100MHz		0.04 0.05		dB dB
HARMONIC DISTORTION Second Harmonic Third Harmonic	f = 30MHz, V_O = 1.4Vp-p, R_L = 1kΩ		 –53 –67		 dBc dBc
CROSSTALK MPC100AP All Hostile Off Isolation MPC100AU All Hostile Off Isolation	V_I = 1.4Vp-p, Figures 4 and 8 f = 5MHz, f = 30MHz, f = 5MHz, f = 30MHz, f = 5MHz, f = 30MHz, f = 5MHz, f = 30MHz		 –82 –60 –70 –71 –78 –70 –75 –76		 dB dB dB dB dB dB dB dB
TIME DOMAIN					
RISE TIME	V_O = 1.4Vp-p, Step 10% to 90% C_{OUT} = 1pF, R_{OUT} = 22Ω		 3.3		 ns
SLEW RATE	V_O = 2Vp-p C_{OUT} = 1pF C_{OUT} = 22pF C_{OUT} = 47pF		 650 460 320		 V/µs V/µs V/µs

CONNECTION DIAGRAM

Top View **SOIC/DIP**

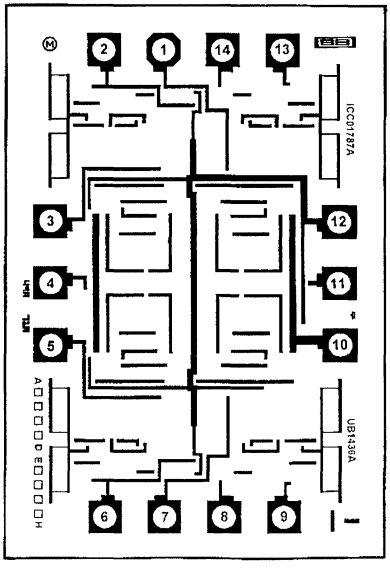


MPC100

FUNCTIONAL DESCRIPTION

IN_1-IN_4	Four analog input channels
GND	Analog input shielding grounds, connect to system ground
SEL_1-SEL_4	Channel selection inputs
V_{OUT}	Analog output; tracks selected channel
$-V_{CC}$	Negative supply voltage; typical –5VDC
$+V_{CC}$	Positive supply voltage; typical +5VDC

DICE INFORMATION



MPC100 DIE TOPOGRAPHY

PAD	FUNCTION
1	Input 1
2	Ground
3	Input 2
4	Ground
5	Input 3
6	Ground
7	Input 4
8	Select 4
9	Select 3
10	+5V Supply
11	Output
12	–5V Supply
13	Select 2
14	Select 1

Substrate Bias: Negative Supply
NC: No Connection
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	51 x 76, ±5	1.295 x 1.93, ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005 +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6V
Analog Input Voltage (IN_1 through IN_4)(1)	$\pm V_{CC}$, ±0.7V
Logic Input Voltage	–0.6V to $+V_{CC}$ +0.6V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Output Current	±6mA
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL_1 through SEL_4)(1)	–0.5V to $+V_{CC}$ +0.7V

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC100AP	14-Pin Plastic DIP	–40°C to +85°C
MPC100AU	SO-14 Surface Mount	–40°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC100AP	14-Pin Plastic DIP	010
MPC100AU	SO-14 Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

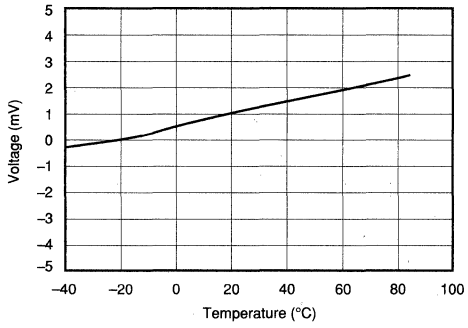
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

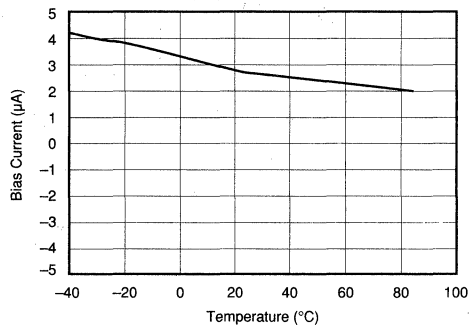
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

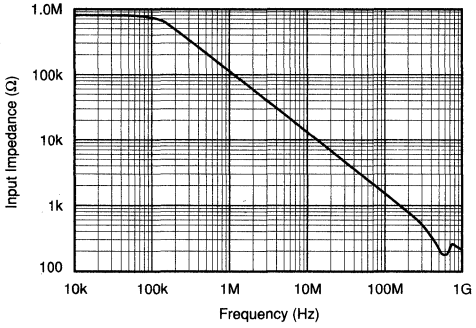
OFFSET VOLTAGE vs TEMPERATURE



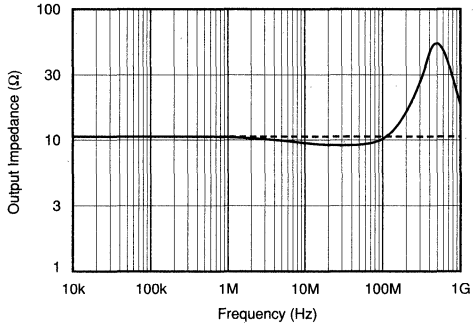
INPUT BIAS CURRENT vs TEMPERATURE



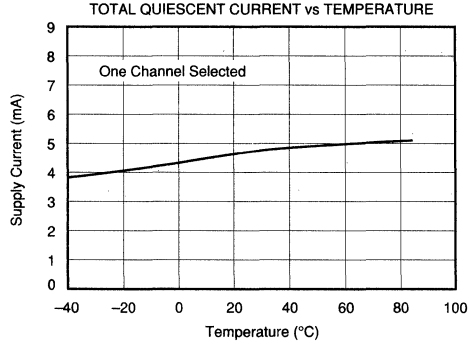
INPUT IMPEDANCE vs FREQUENCY



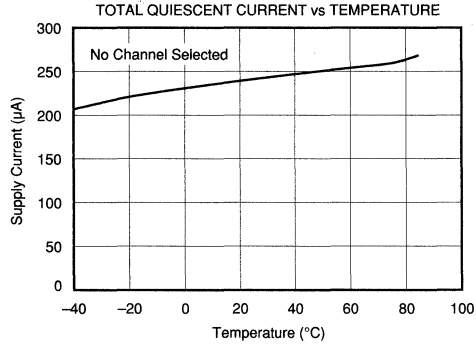
OUTPUT IMPEDANCE vs FREQUENCY



TOTAL QUIESCENT CURRENT vs TEMPERATURE



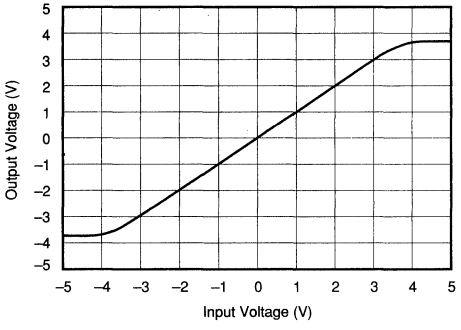
TOTAL QUIESCENT CURRENT vs TEMPERATURE



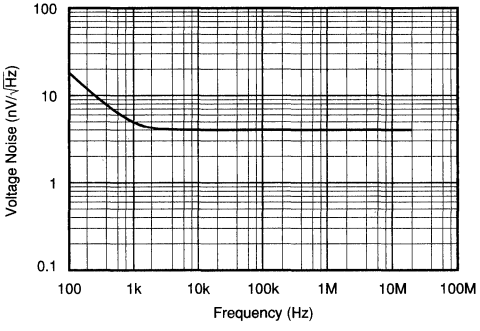
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

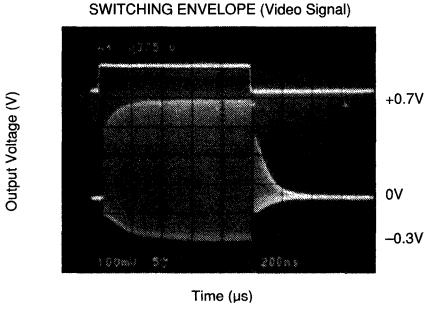
TRANSFER FUNCTION



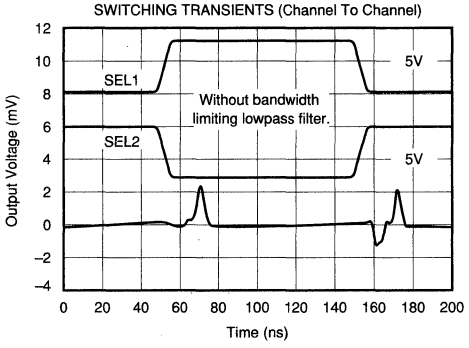
INPUT VOLTAGE NOISE SPECTRAL DENSITY



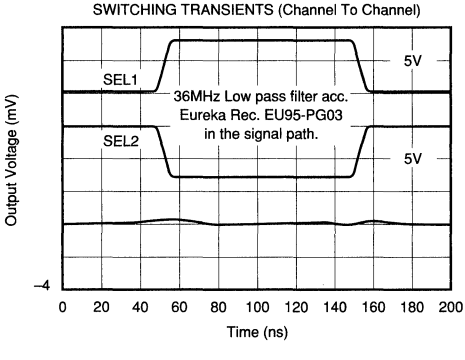
SWITCHING ENVELOPE (Video Signal)



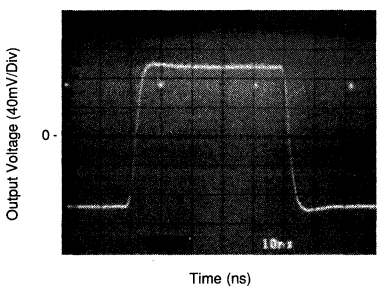
SWITCHING TRANSIENTS (Channel To Channel)



SWITCHING TRANSIENTS (Channel To Channel)



SMALL SIGNAL PULSE RESPONSE

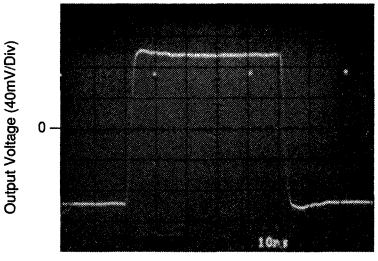


C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

TYPICAL PERFORMANCE CURVES (CONT)

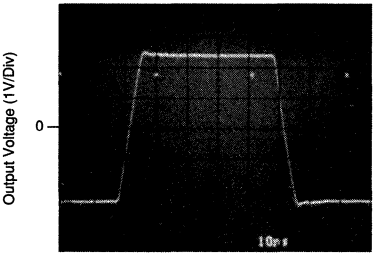
At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE



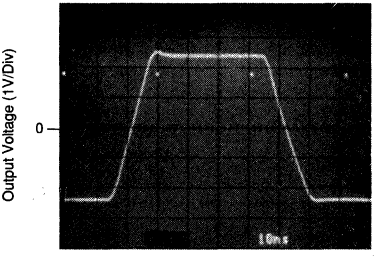
Time (ns)
C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

LARGE SIGNAL PULSE RESPONSE



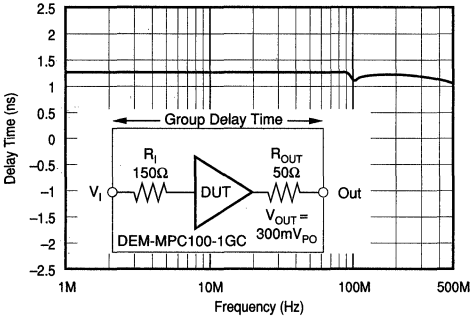
Time (ns)
C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

LARGE SIGNAL PULSE RESPONSE

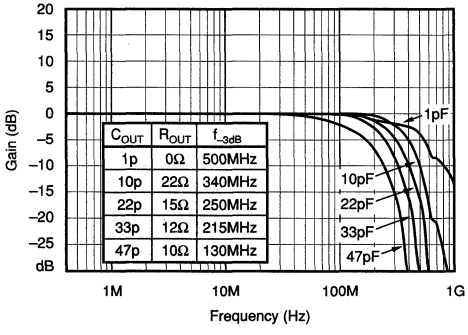


Time (ns)
C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

GROUP DELAY TIME vs FREQUENCY

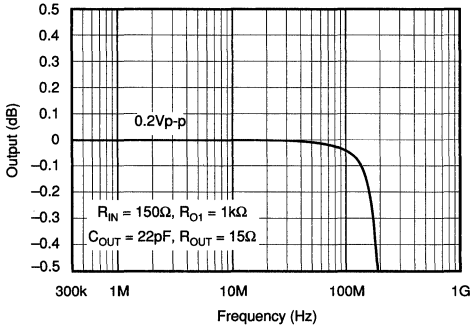


BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}



C_{OUT}	R_{OUT}	f_{-3dB}
1p	0Ω	500MHz
10p	22Ω	340MHz
22p	15Ω	250MHz
33p	12Ω	215MHz
47p	10Ω	130MHz

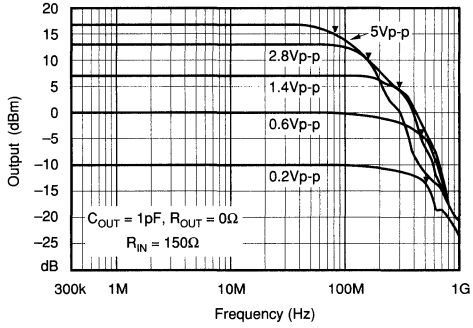
GAIN FLATNESS



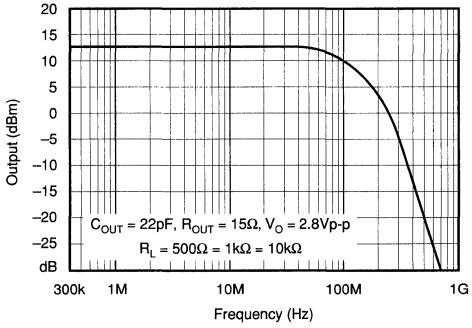
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

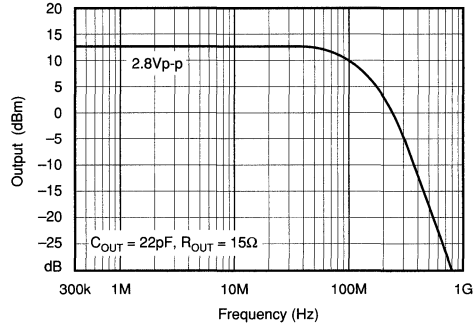
BANDWIDTH vs OUTPUT VOLTAGE



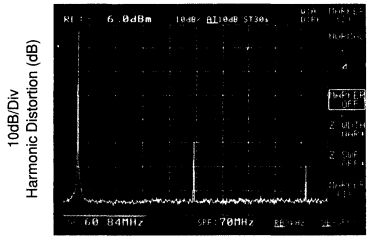
BANDWIDTH vs R_{LOAD}



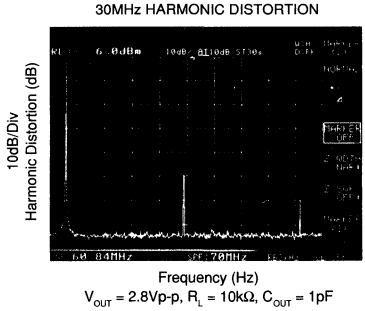
BANDWIDTH MATCHING (DB1...DB4)



30MHz HARMONIC DISTORTION



30MHz HARMONIC DISTORTION



APPLICATIONS INFORMATION

The MPC100 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

All pins on the MPC100 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown in Figure 1. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or less whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision buffer amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC100.

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC100 incorporates on-chip ESD protection diodes as shown in Figure 1. This eliminates the need for the user to add external protection diodes, performance.

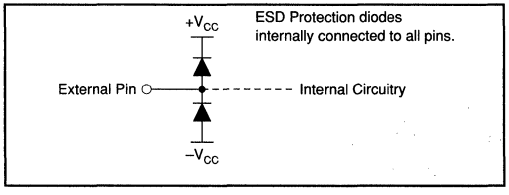


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC100 video multiplexer allows the user to connect any one of four analog input channels (IN_1-IN_4) to the output of the component and to switch between channels within less than 0.5µs. It consists of four identical unity-gain buffer amplifiers, which are connected together internally at the output. The open loop buffers consisting of complementary emitter followers applies no feedback, so their low frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form an unidirectional transmission path and thus provide high output-to-input isolation. Switching stages compatible to TTL level digital signals are provided for each buffer to select the input channel. When no channel is selected, the output of the device is high-impedance and allows the user to wire more MPC100s together to form switch multi-channel matrices.

If one channel is selected with a digital "1" at the corresponding SEL-input, the MPC100 acts as a buffer amplifier with high input impedance and low output impedance. The truth table on the front page describes the relationship between the digital inputs (SEL_1 to SEL_4) and the analog inputs (IN_1 to IN_4), and which signal is selected at the output.

The 2-4 address decoder and chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. It requires DC coupling and termination resistors when directly driven from a low impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 250MHz at an output voltage of 1.4Vp-p allows the design of large crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.05%) and phase (0.01°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the brightness (luminance) signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC100 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to

another causes the signal to mix at the output for a short time, but it interferes only minimally with the input signals. The transient peaks remain less than +2.5mV and –1.2mV. Subsequent equipment might interpret large negative output glitches as synchronization pulses. To remove this problem, the output must be clamped during the switching dead time. With the MPC100, the generated output transients are extremely small and clamping is unnecessary. The switching time between two channels is less than 0.5µs. This short time period allows easy switching during the vertical blanking time. The signal envelope during the transition from one channel to another rises and falls symmetrically and shows less overshooting or DC settling transients.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffers are always in off-state. One important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±230µA in off-state and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC100 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance or inductance.
- Make short and low inductance traces. The entire physical circuit layout should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection. Refer to the suggested layout shown in Figure 6.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended because they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile solderless sockets.
- Use low-inductance and surface-mounted components to achieve the best AC-performance.
- A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential.

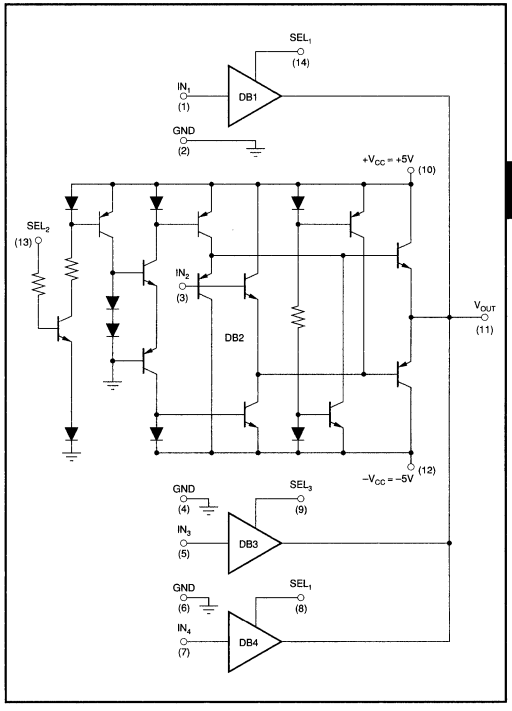


FIGURE 2. Simplified Circuit Diagram.

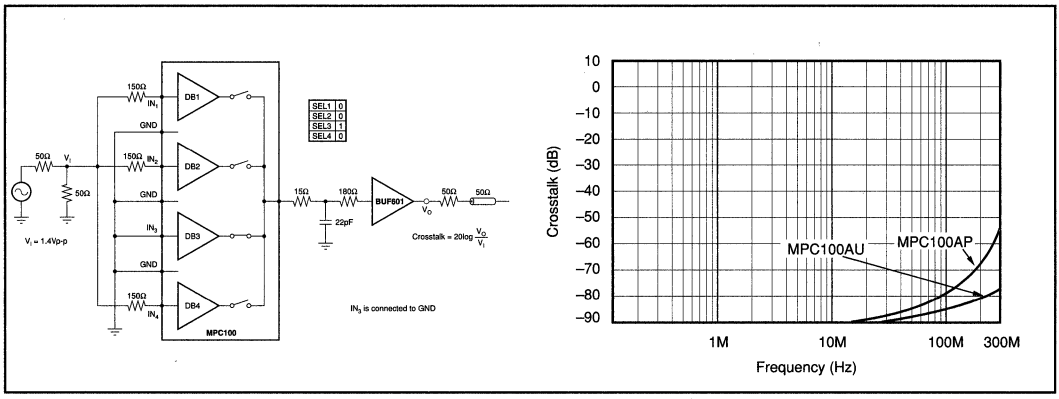


FIGURE 3. Channel Crosstalk—Grounded Input.

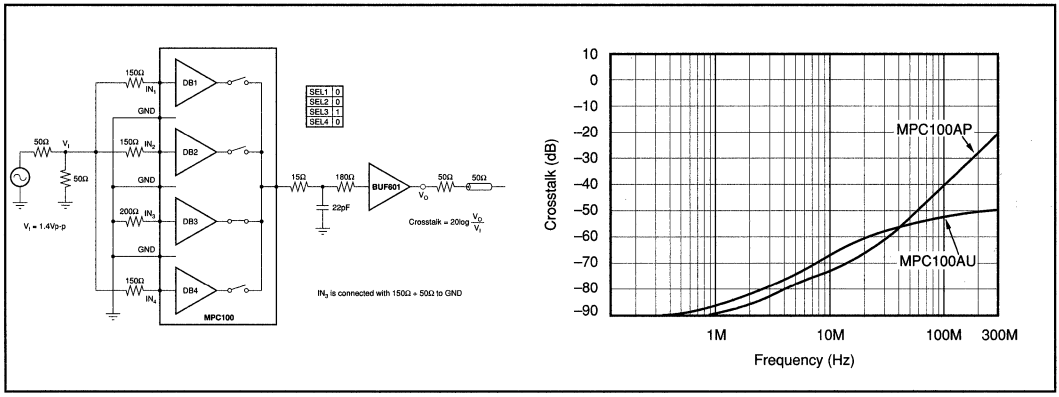


FIGURE 4. Channel Crosstalk—150Ω Input Resistor.

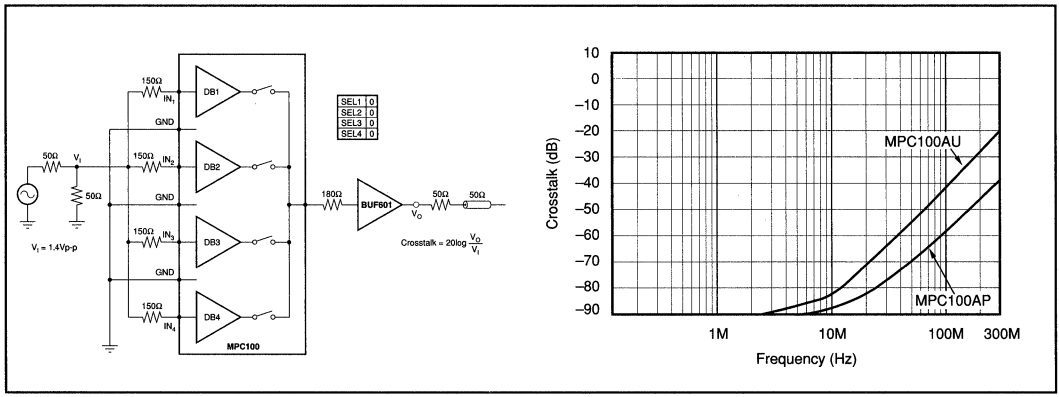
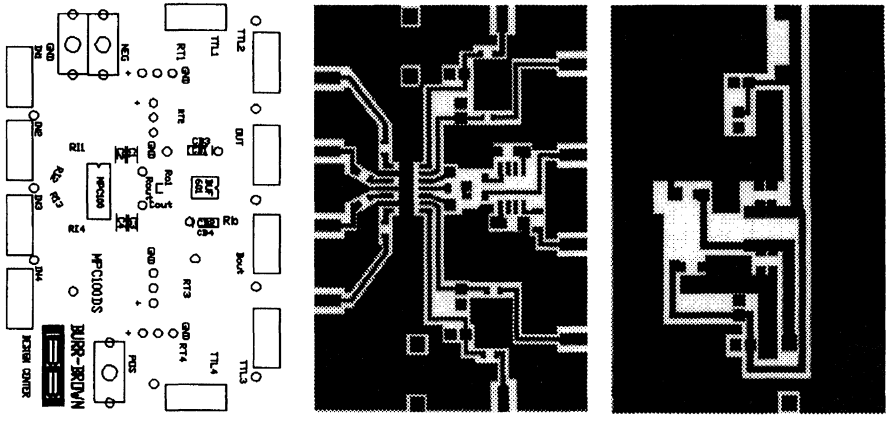


FIGURE 5. Off Isolation.



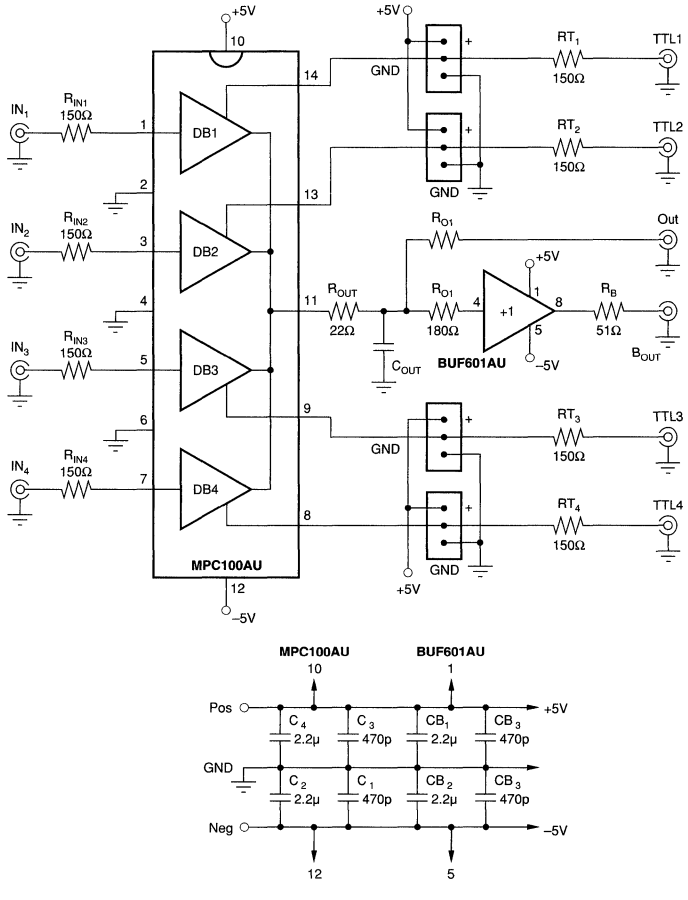


FIGURE 6. Test Circuit and Circuit Board Layout.

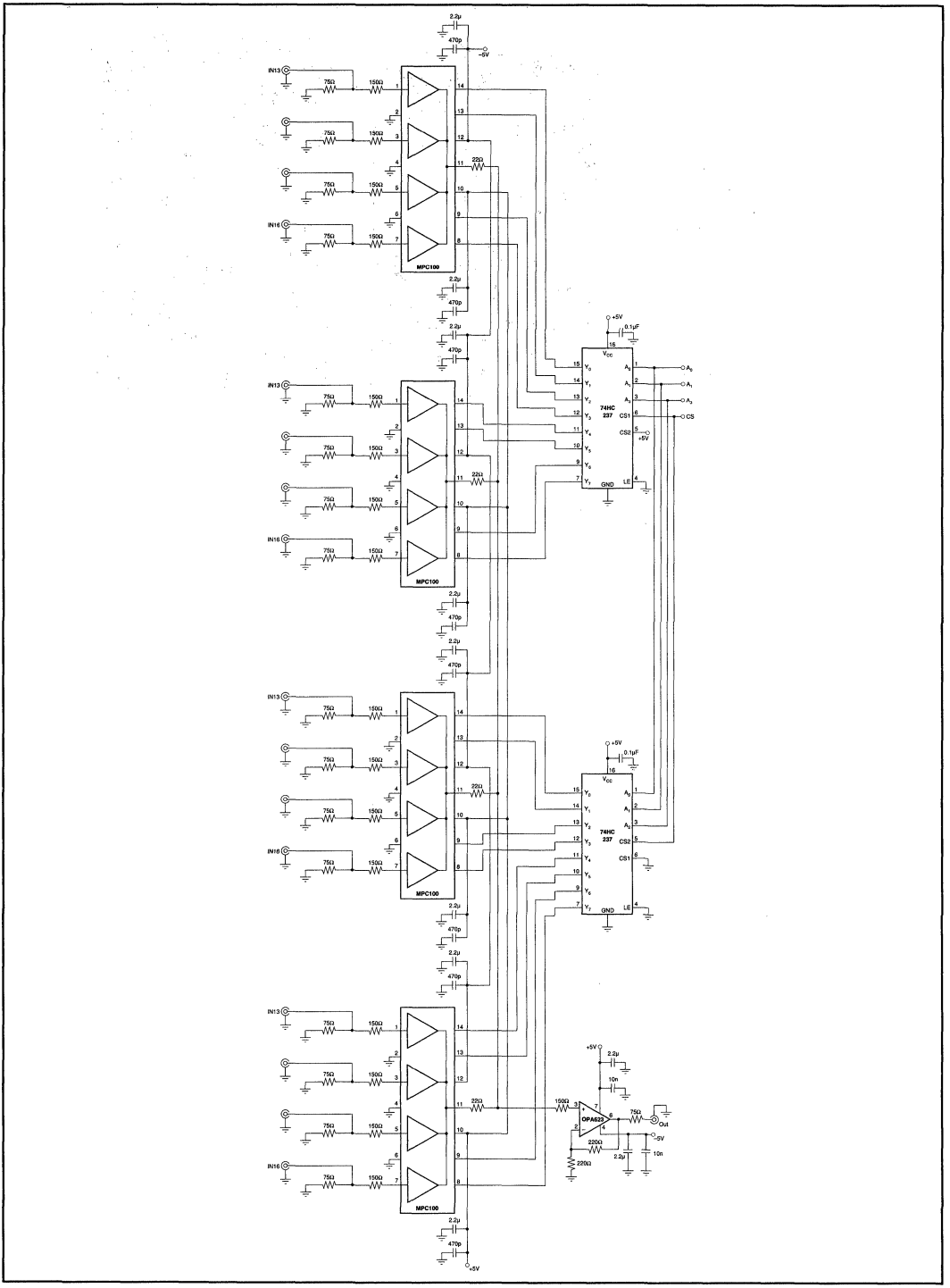
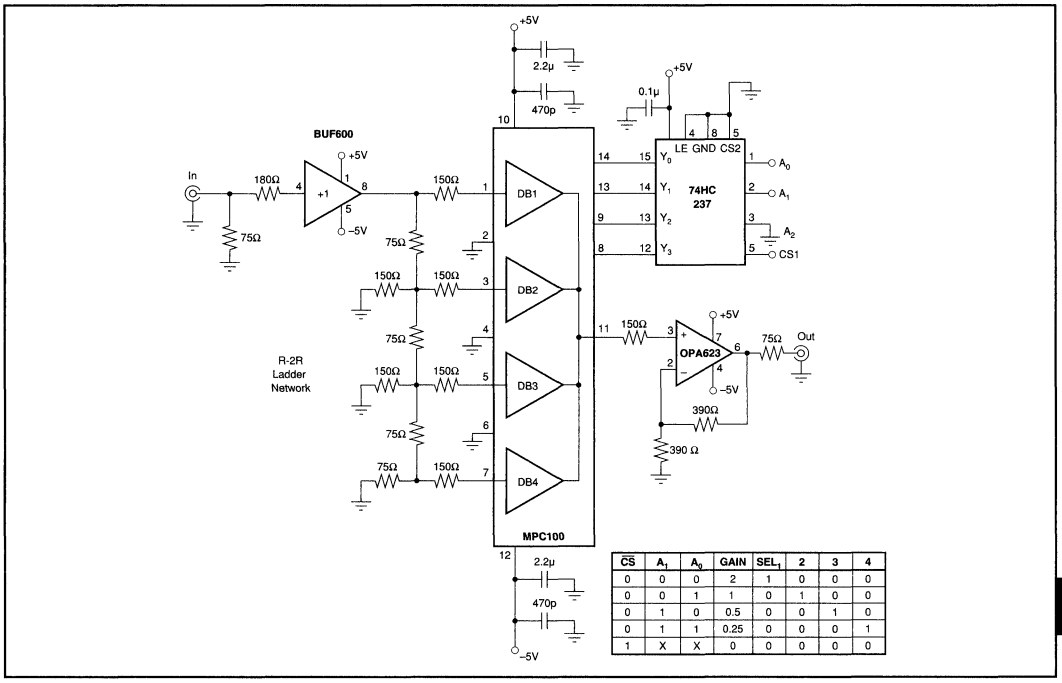


FIGURE 7. Video Distribution Field.



$\overline{CS}$	A_1	A_0	GAIN	SEL_1	2	3	4
0	0	0	2	1	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0.5	0	0	1	0
0	1	1	0.25	0	0	0	1
1	X	X	0	0	0	0	0

FIGURE 8. Digital Gain Control.

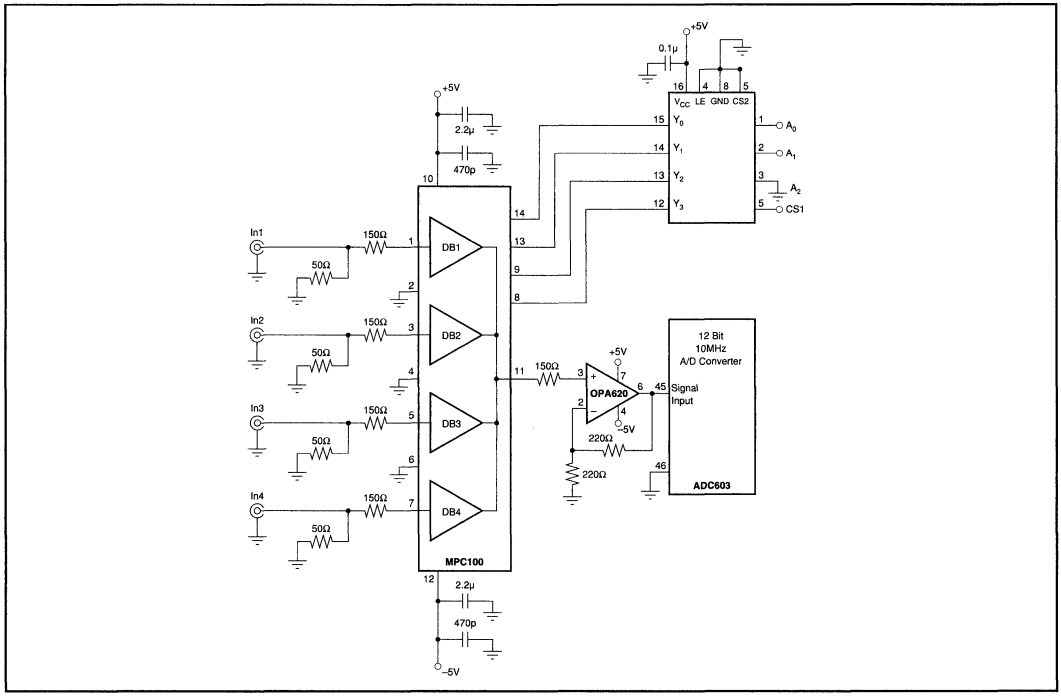


FIGURE 9. High Speed Data Acquisition System.

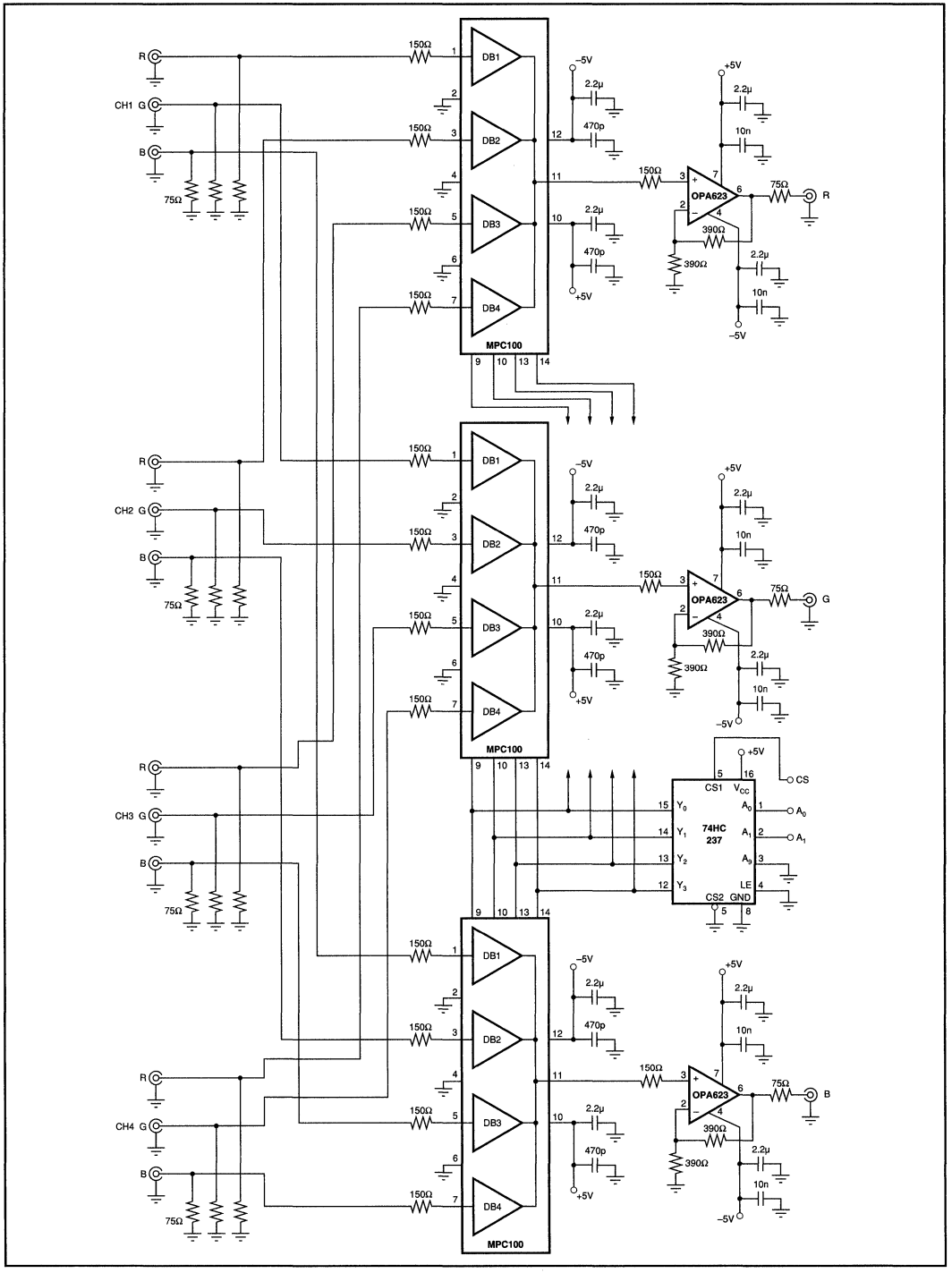


FIGURE 10. Distribution Field for High Resolution Graphic Cards, Cameras.

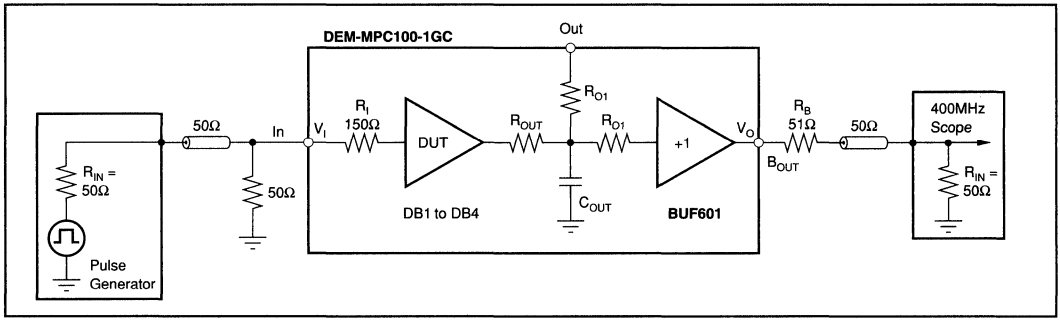


FIGURE 11. Test Circuit Pulse Response.

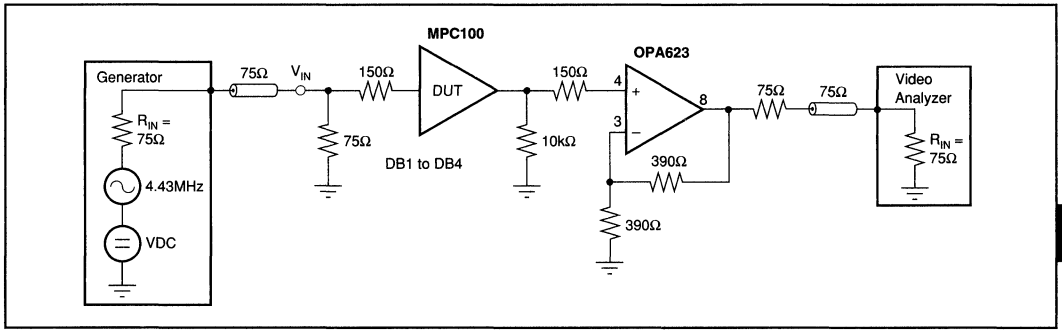


FIGURE 12. Test Circuit Differential Gain and Phase.

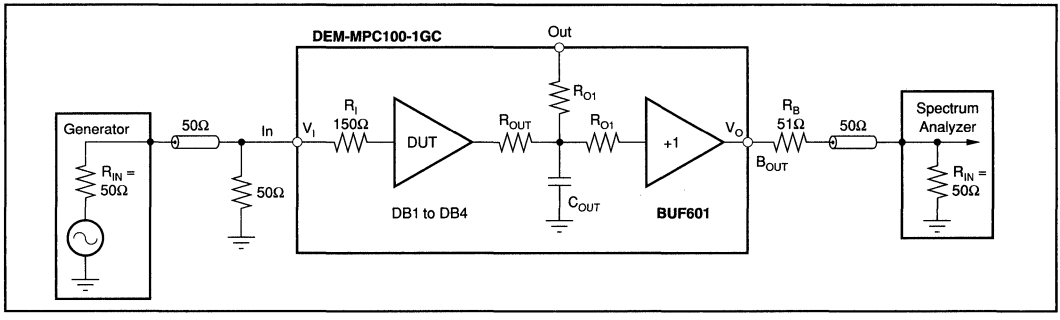


FIGURE 13. Test Circuit Frequency Response.

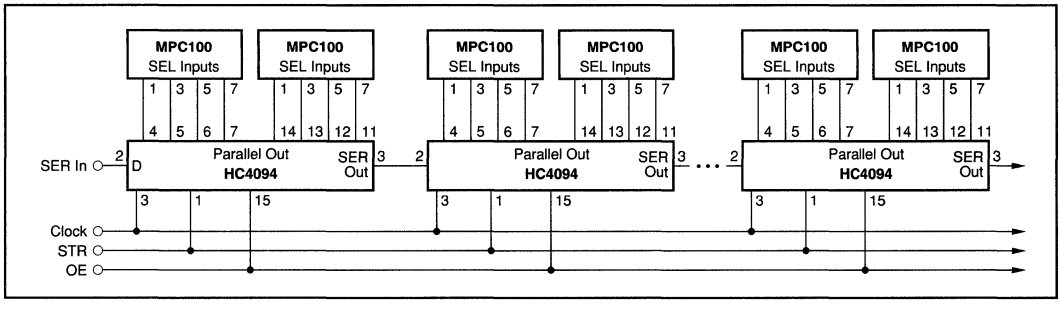
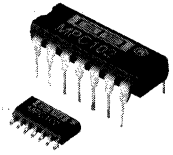


FIGURE 14. Serial Bus-Controlled Distribution Field.

BURR-BROWN®



MPC102

Wide-Bandwidth DUAL 2 x 1 VIDEO MULTIPLEXER

FEATURES

- **BANDWIDTH: 210MHz (1.4Vp-p)**
- **LOW INTERCHANNEL CROSSTALK: –68dB (30MHz, SO); –58dB (30MHz, DIP)**
- **LOW SWITCHING TRANSIENTS: +6mV/–8mV**
- **LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.02%, 0.02°**
- **LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±250µA**

APPLICATIONS

- **VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)**
- **RADAR SYSTEMS**
- **DATA ACQUISITION**
- **INFORMATION TERMINALS**
- **SATELLITE OR RADIO LINK IF ROUTING**

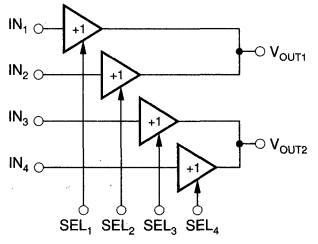
DESCRIPTION

The MPC102 is dual, wide-bandwidth, 2-to-1 channel video signal multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC102 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC102 consists of four identical monolithic, integrated, open-loop buffer amplifiers. Two buffer outputs are each connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC102 multiplexer enables the user to connect one of two input signals to the corresponding output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 14-pin SO and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)



TRUTH TABLE

SEL_1	SEL_2	SEL_3	SEL_4	V_{OUT1}	V_{OUT2}
0	0	0	0	HI-Z	HI-Z
1	0	0	0	IN_1	HI-Z
0	1	0	0	IN_2	HI-Z
0	0	1	0	HI-Z	IN_3
0	0	0	1	HI-Z	IN_4

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5V, R_L = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP, AU			UNITS
		MIN	TYP	MAX	
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE	R_{IN} = 0, R_{SOURCE} = 0				
Initial			14	±30	mV
vs Temperature			60		µV/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V	–40	–74		dB
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		–50		dB
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–50		dB
Initial Matching	All Four Buffers		±3		mV
INPUT BIAS CURRENT					
Initial			4	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V		±710		nA/V
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		0.26		µA/V
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		1.7		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 20kHz to 10MHz		4.0		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/(V_{IN} • √5MHz)		–98		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±3.6		V
TRANSFER CHARACTERISTICS					
Voltage Gain	R_L = 1kΩ, V_{IN} = ±2V		0.982		V/V
Voltage Gain	R_L = 10kΩ, V_{IN} = ±2.8V	0.98	0.992		V/V
RATED OUTPUT					
Voltage	V_{IN} = ±3V, R_L = 10kΩ	±2.8	±2.98		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2		V_{CC}	V
Logic 0 Voltage				+0.8	V
Logic 1 Current	V_{SEL} = 5.0V		100	150	µA
Logic 0 Current	V_{SEL} = 0.8V			5	µA
SWITCHING CHARACTERISTICS	V_{IN} = –0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_{OUT} = 1Vp-p		0.25		µs
SEL to Channel OFF Time	10% Point of V_{OUT} = 1Vp-p		0.25		µs
Switching Transient, Positive	Measured While Switching		6		mV
Switching Transient, Negative	Between Two Grounded Channels		–8		mV
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6	±5	mA
	No Channel Selected		±250	±350	µA
Rejection Ratio			–80		dB
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			90		°C/W

SPECIFICATIONS—AC CHARACTERISTICS (CONT)

At V_{CC} = ±5V, R_L = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP, AU MIN	MPC102AP, AU TYP	MPC102AP, AU MAX	UNITS
LARGE SIGNAL BANDWIDTH (–3dB)	V_{OUT} = 5.0Vp-p, C_{OUT} = 1pF		55		MHz
	V_{OUT} = 2.8Vp-p, C_{OUT} = 1pF		100		MHz
	V_{OUT} = 1.4Vp-p, C_{OUT} = 1pF		210		MHz
SMALL SIGNAL BANDWIDTH	V_{OUT} = 0.2Vp-p, C_{OUT} = 1pF		370		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_{IN} = 0.3Vp-p VDC = 0 to 0.7V		0.02		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_{IN} = 0.3Vp-p VDC = 0 to 0.7V		0.02		Degrees
GAIN FLATNESS PEAKING	V_{OUT} = 0.2Vp-p, DC to 30MHz		0.04		dB
	V_{OUT} = 0.2Vp-p, DC to 100MHz		0.05		dB
HARMONIC DISTORTION	f = 30MHz, V_{OUT} = 1.4Vp-p, R_L = 350Ω				
Second Harmonic			–64		dBc
Third Harmonic			–66		dBc
CROSSTALK	V_{IN} = 1.4Vp-p				
MPC102AP All Hostile	f = 5MHz,		–75		dB
	f = 30MHz,		–58		dB
Off Isolation	f = 5MHz,		–70		dB
	f = 30MHz,		–71		dB
MPC102AU All Hostile	f = 5MHz,		–78		dB
	f = 30MHz,		–68		dB
Off Isolation	f = 5MHz,		–75		dB
	f = 30MHz		–76		dB
TIME DOMAIN					
RISE/FALL TIME	V_{OUT} = 1.4Vp-p, Step 10% to 90% C_{OUT} = 1pF, R_{OUT} = 22Ω		2.5		ns
SLEW RATE	V_{OUT} = 1.4Vp-p				
	C_{OUT} = 1pF		500		V/µs
	C_{OUT} = 22pF		360		V/µs
	C_{OUT} = 47pF		260		V/µs

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6V
Analog Input Voltage (IN_1 through IN_4)	$\pm V_{CC}$, ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Output Current	±6mA
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL_1 through SEL_4)	–0.5V to $+V_{CC}$ +0.7V
Logic Voltage Input	–0.6V to $+V_{CC}$ +0.6V

ORDERING INFORMATION

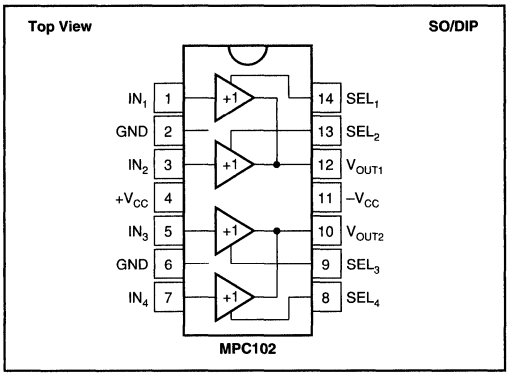
MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC102AP	14-Pin Plastic DIP	–40°C to +85°C
MPC102AU	14-Pin SOIC	–40°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC102AP	14-Pin DIP	010
MPC102AU	14-Pin SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

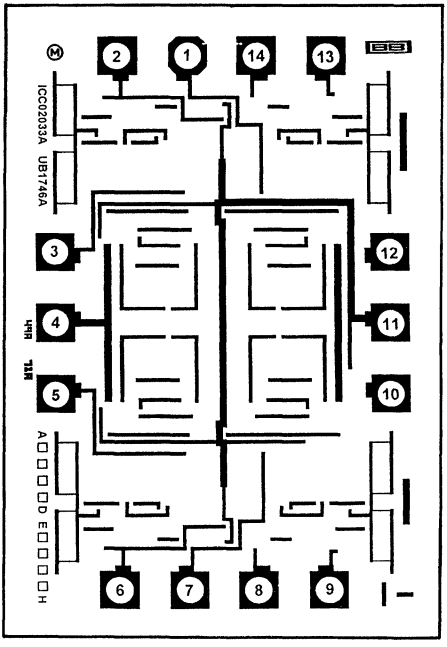
CONNECTION DIAGRAM



PIN DESCRIPTION

PIN	DESCRIPTION
IN_1, IN_2	Analog Inputs Channel 1 and 2
IN_3, IN_4	Analog Inputs Channel 3 and 4
GND	Analog Shielding Grounds, Connect to System Ground
SEL_1, SEL_2	Channel Selection Inputs
V_{OUT1}	Analog Output 1
V_{OUT2}	Analog Output 2
$-V_{CC}$	Negative Supply Voltage; typical –5VDC
$+V_{CC}$	Positive Supply Voltage; typical +5VDC

DICE INFORMATION



MPC102AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Input 1
2	Ground
3	Input 2
4	+5V Supply
5	Input 3
6	Ground
7	Input 4
8	Select 4
9	Select 3
10	Output 2
11	–5V Supply
12	Output 1
13	Select 2
14	Select 1

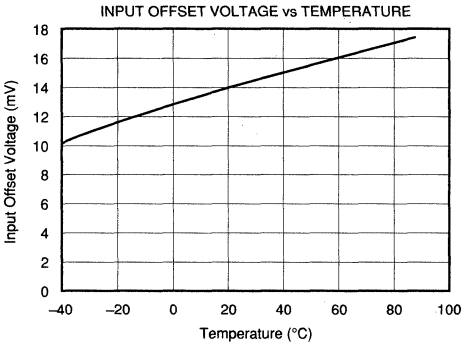
Substrate Bias: Negative Supply.
NC: No Connection.
Wire Bonding: Gold wire bonding is recommended.

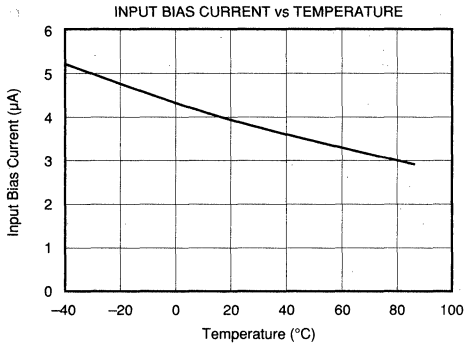
MECHANICAL INFORMATION

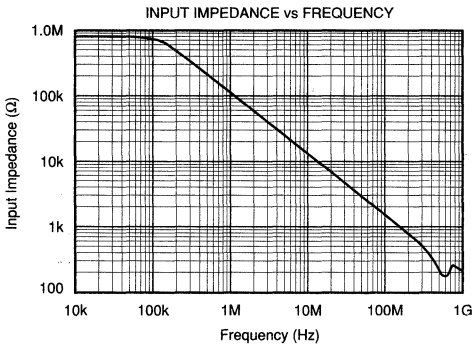
	MILS (0.001")	MILLIMETERS
Die Size	51 x 76 ±5	1.295 x 1.93 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

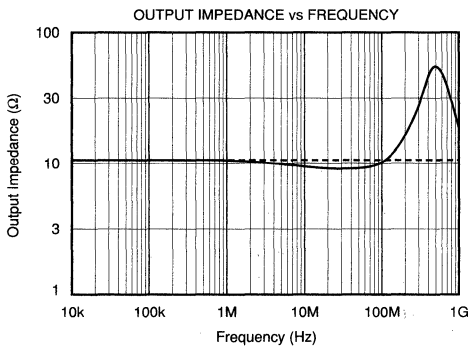
TYPICAL PERFORMANCE CURVES

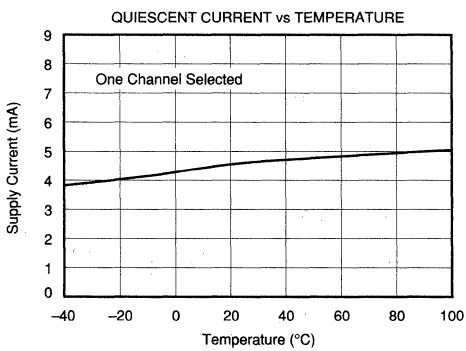
At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

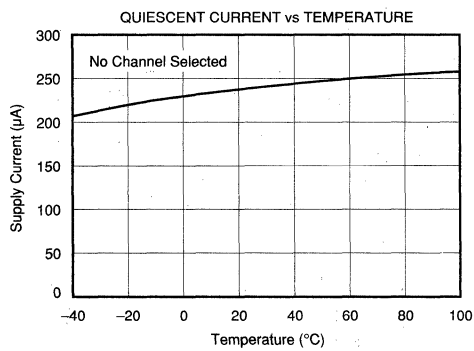








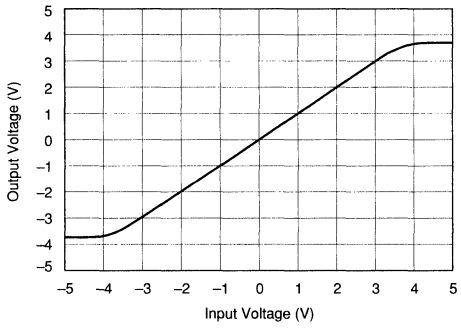




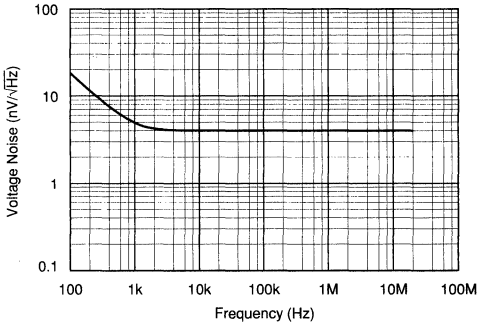
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

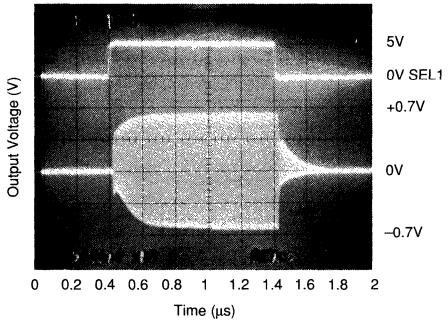
TRANSFER FUNCTION



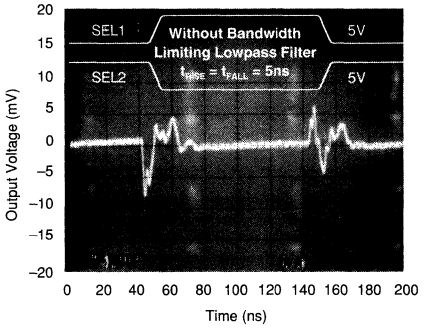
INPUT VOLTAGE NOISE SPECTRAL DENSITY

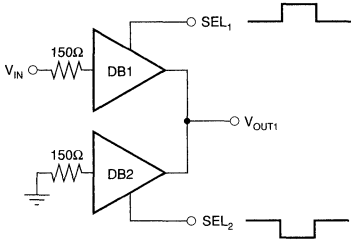


SWITCHING ENVELOPE
(Channel-to-Channel Switching)

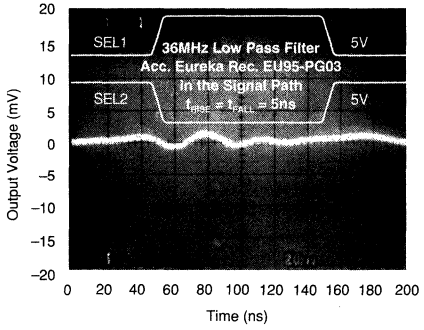


SWITCHING TRANSIENTS
(Channel-to-Channel)

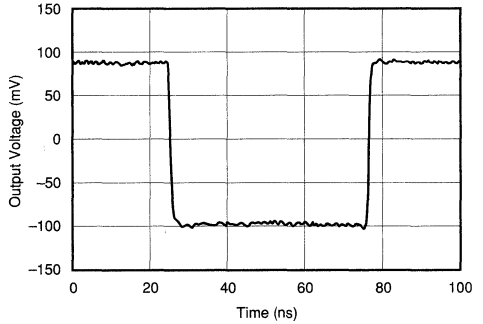




SWITCHING TRANSIENTS
(Channel-to-Channel)



SMALL SIGNAL PULSE RESPONSE

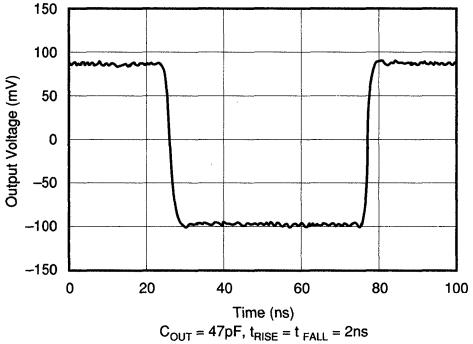


C_{OUT} = 1pF, $t_{RISE} = t_{FALL}$ = 2ns
(Generator), V_{IN} = 0.2Vp-p

TYPICAL PERFORMANCE CURVES (CONT)

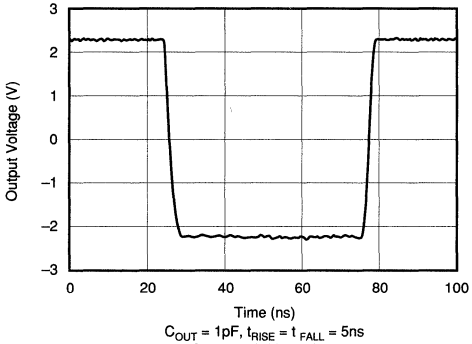
At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE



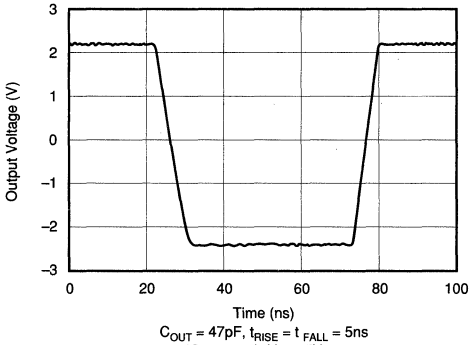
C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator), V_{IN} = 0.2Vp-p

LARGE SIGNAL PULSE RESPONSE



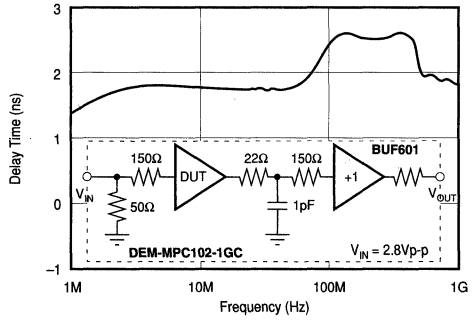
C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator), V_{IN} = 5Vp-p

LARGE SIGNAL PULSE RESPONSE

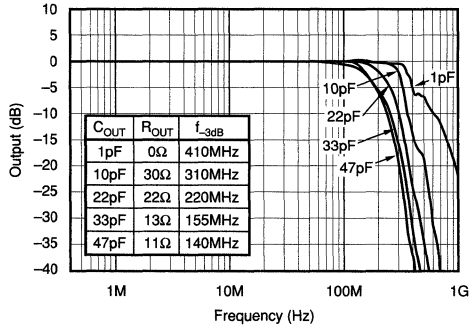


C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator), V_{IN} = 5Vp-p

GROUP DELAY TIME vs FREQUENCY

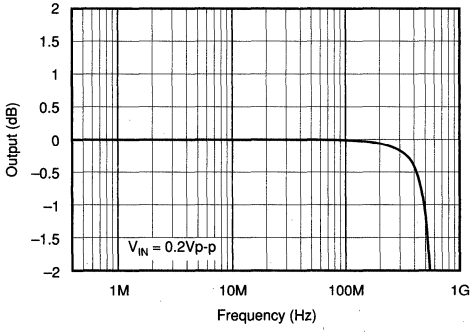


BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}



C_{OUT}	R_{OUT}	f_{-3dB}
1pF	0Ω	410MHz
10pF	30Ω	310MHz
22pF	22Ω	220MHz
33pF	13Ω	155MHz
47pF	11Ω	140MHz

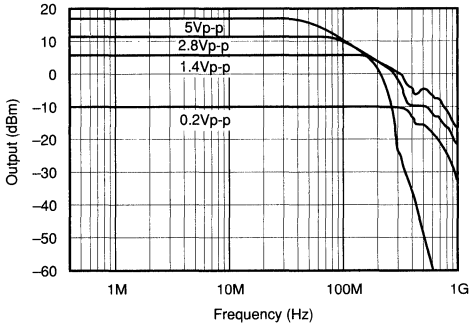
GAIN FLATNESS



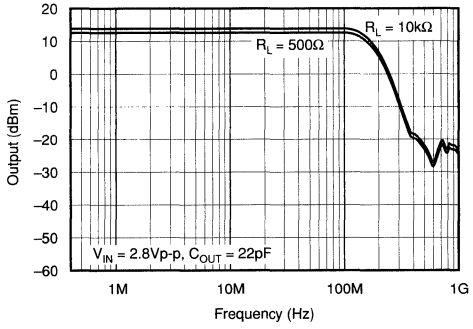
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

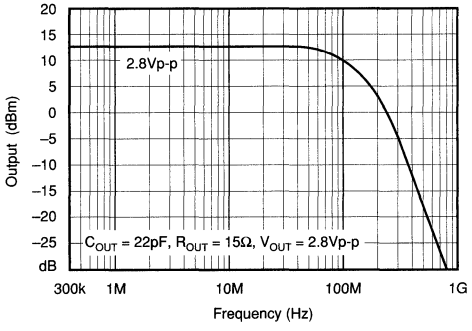
BANDWIDTH vs OUTPUT VOLTAGE



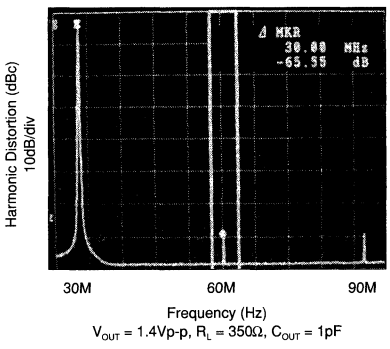
BANDWIDTH vs R_{LOAD}



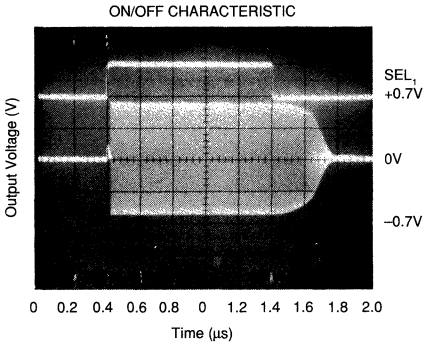
BANDWIDTH MATCHING (DB1...DB4)

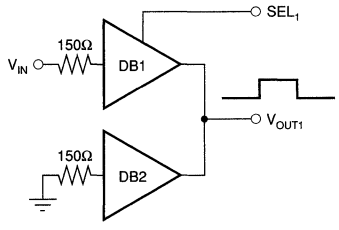


30MHz HARMONIC DISTORTION



ON/OFF CHARACTERISTIC





APPLICATIONS INFORMATION

The MPC102 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

As shown below, all pins on the MPC102 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the characteristics of the buffer amplifier input without necessarily destroying the device. In precision buffer amplifiers, such damage may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC102.

Static damage has been well-recognized as a problem for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC102 incorporates on-chip ESD protection diodes as shown in Figure 1. Thus the user does not need to add external protection diodes, which can add capacitance and degrade AC performance.

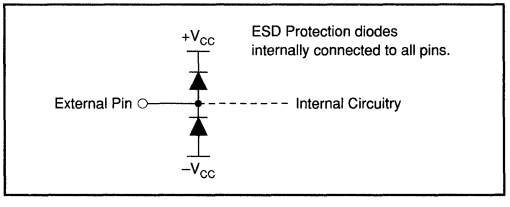


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC102 is a dual, 2 x 1, wide-band analog signal multiplexer. It allows the user to connect one of the two inputs (IN_1/IN_2 or IN_3/IN_4) to the corresponding output. The switching speed between two input channels is typically less than 300ns.

However, in contrast to signal switches using CMOS or DMOS transistors, the switching transients are very low at +6mV and –8mV. The MPC102 consists of four identical unity-gain buffer amplifiers. Two of the four amplifiers are connected together internally at the output. The open-loop buffer amps, which consist of complementary emitter followers, apply no feedback so their low-frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form a unidirectional transmission path, thus providing high output-to-input isolation. Switching stages compatible to TTL-level digital signals are provided for each buffer to select the input channel. When no channel is selected, the outputs of the device are high-impedance. This allows the user to wire several MPC102s together to create multichannel switch matrices.

Chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases bus-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. The buffers require DC coupling and termination resistors when driven directly from a low-impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated, high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. Bandwidth of over 210MHz at an output voltage of 1.4Vp-p allows the design of multi-channel crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.02%) and phase (0.02°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the luminance signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC102 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short time, but it interferes minimally with the input signals. The transient peaks remain less than +6mV and –8mV. The generated output transients are extremely small, so DC

clamping during switching between channels is unnecessary. DC clamping during the switching dead time is required to avoid synchronization by large negative output glitches in subsequent equipment.

The SEL-to-channel-ON time is typically 25ns and is always shorter than the typical SEL-to-channel-OFF time of 250ns. In the worst case, an ON/OFF margin of 150ns ensures safe switching even for timing spreads in the digital control latches. The short interchannel switching time of 300ns allows channel change during the vertical blanking time, even in high-resolution graphic or broadcast systems. As shown in the typical performance curves, the signal envelope during transition from one channel to another rises and falls symmetrically and shows less overshooting and DC settling effects.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Since most of the buffer amplifiers are in the off-state, one important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±250µA when no channel is selected and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC102 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance.
- Make short and low inductance traces. The entire circuit layout should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile solderless sockets.
- Use low-inductance and surface-mounted components for best ac-performance.
- A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential.

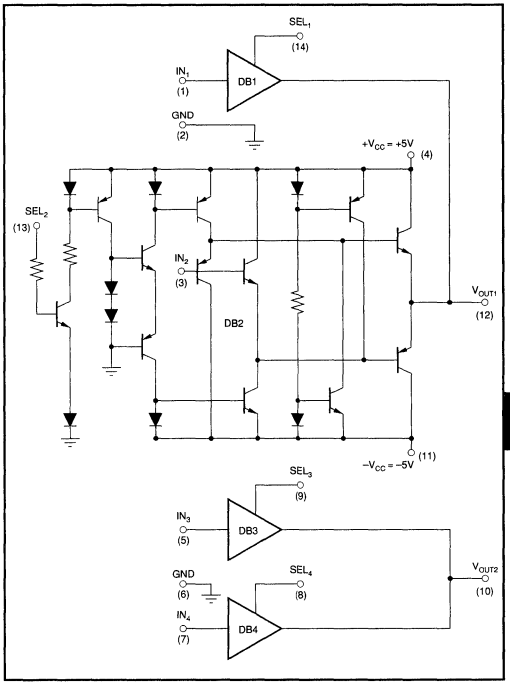


FIGURE 2. Simplified Circuit Diagram.

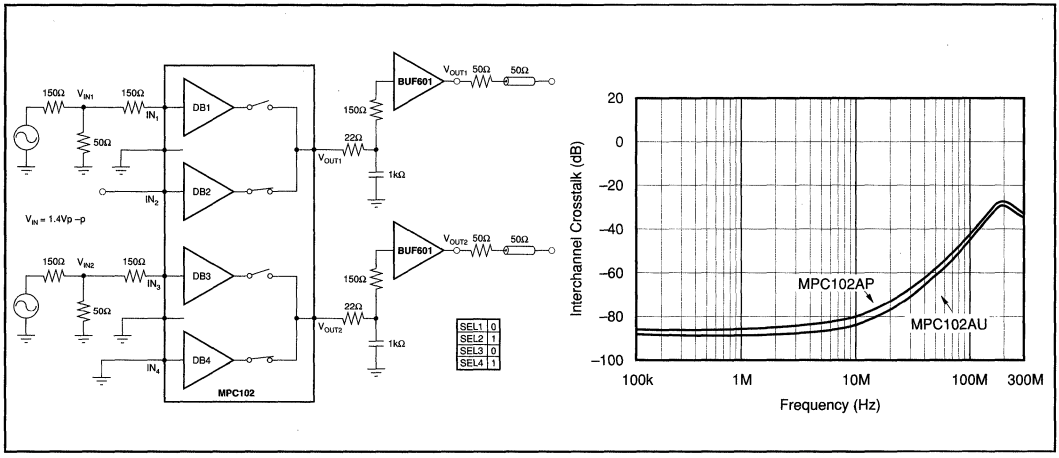


FIGURE 3. All Hostile Crosstalk – Grounded Input.

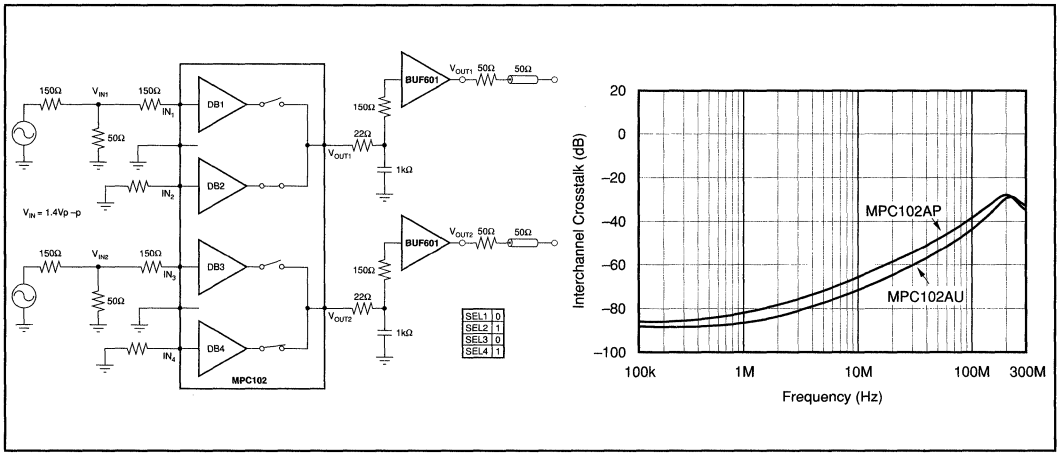


FIGURE 4. Off Isolation Crosstalk 150Ω Input.

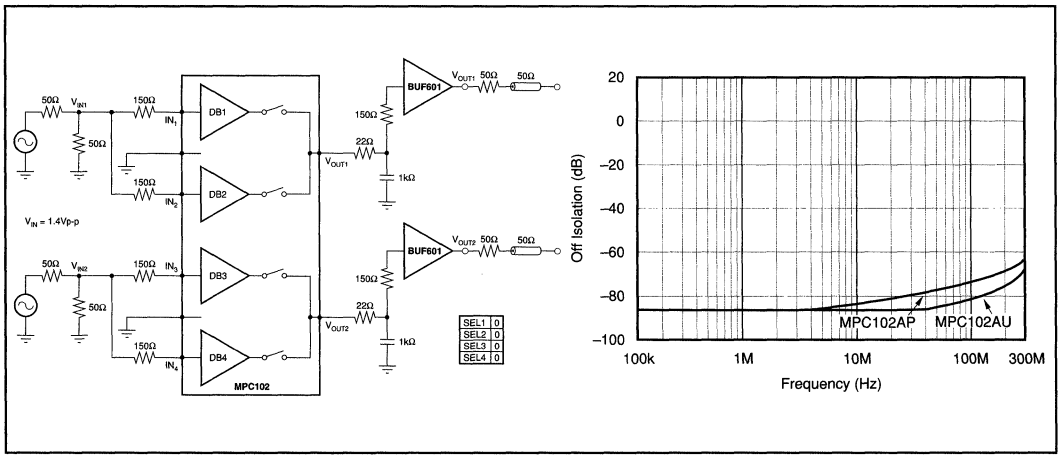
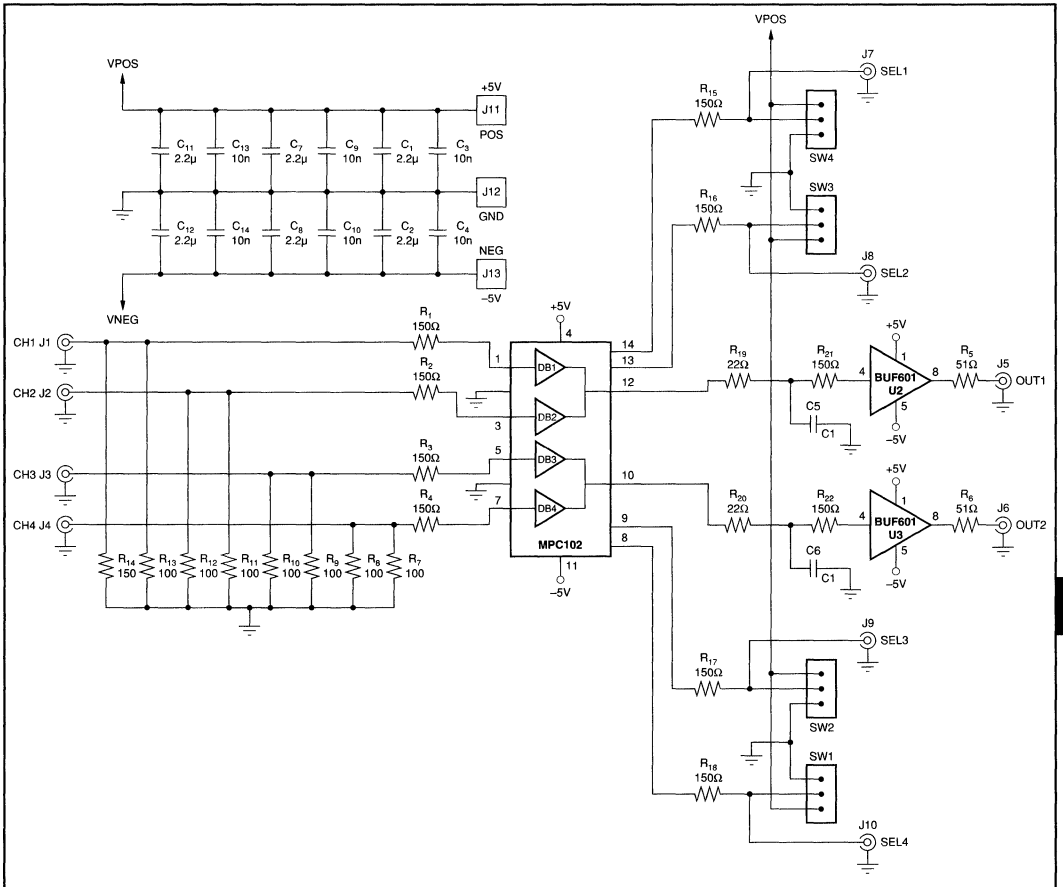


FIGURE 5. Off Isolation Crosstalk Test Circuit 2.



Component Side | Silk Screen | Solder Side

FIGURE 7. Test Circuit and Board Layout.

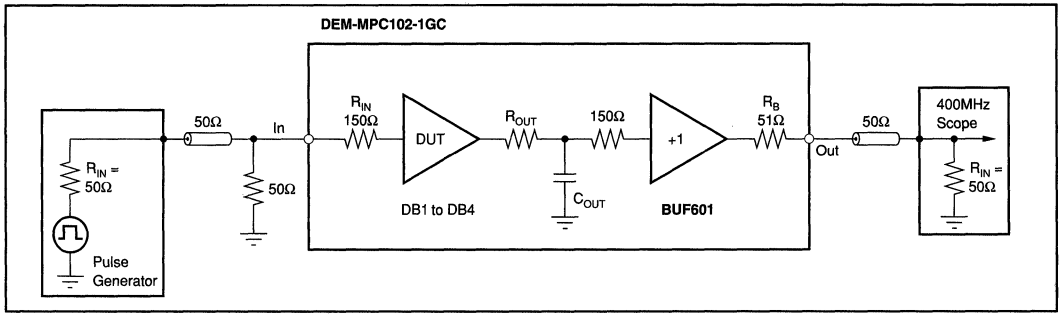


FIGURE 8. Test Circuit Pulse Response.

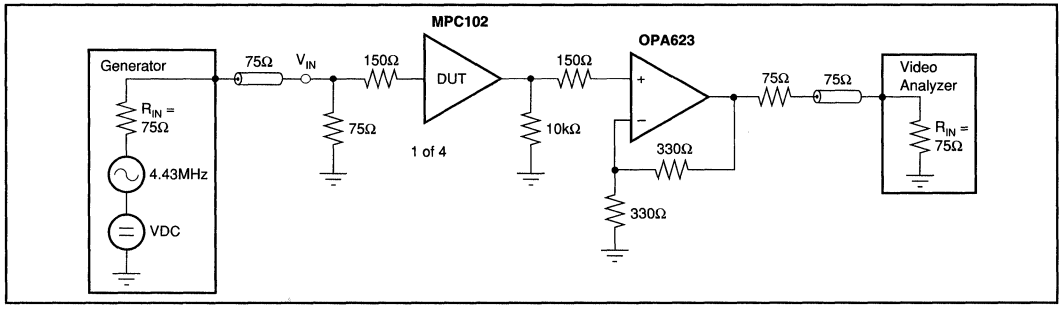


FIGURE 9. Test Circuit Differential Gain and Phase.

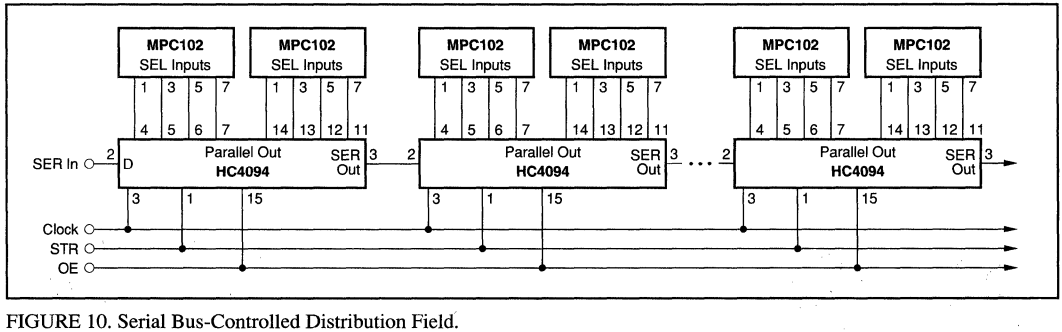


FIGURE 10. Serial Bus-Controlled Distribution Field.

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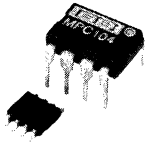


MPC104

Wide-Bandwidth 2 x 1 VIDEO MULTIPLEXER

FEATURES

- BANDWIDTH: 210MHz (1.4Vp-p)
- LOW INTERCHANNEL CROSSTALK: –79dB (30MHz, SO); –77dB (30MHz, DIP)
- LOW SWITCHING TRANSIENTS: +13mV/–4mV
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.03%, 0.01°
- LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±120µA

APPLICATIONS

- VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)
- RADAR SYSTEMS
- DATA ACQUISITION
- INFORMATION TERMINALS
- SATELLITE OR RADIO LINK IF ROUTING

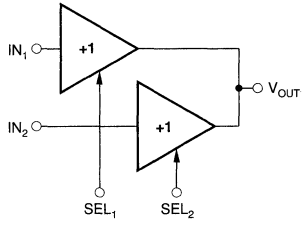
DESCRIPTION

The MPC104 is a wide-bandwidth, 2-to-1 channel video signal multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC104 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC104 consists of two identical monolithic, integrated, open-loop buffer amplifiers, which are connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC104 multiplexer enables the user to connect one of two input signals to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $5nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 8-pin SO and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)



TRUTH TABLE

SEL_1	SEL_2	V_{OUT}
0	0	HI-Z
1	0	IN_1
0	1	IN_2

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS–DC CHARACTERISTICS

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

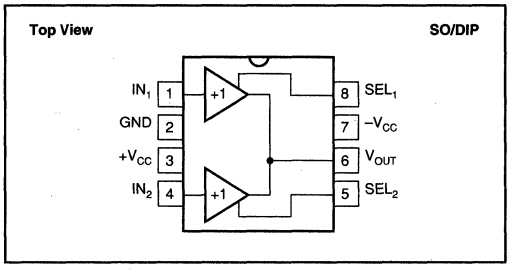
PARAMETER	CONDITIONS	MPC104AP, AU MIN	MPC104AP, AU TYP	MPC104AP, AU MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial			14	±30	mV
vs Temperature			60		µV/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V	–40	–80		dB
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		–50		dB
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–50		dB
Initial Matching	All Buffers		3		mV
INPUT BIAS CURRENT					
Initial			5	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V		±710		nA/V
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		0.26		µA/V
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		1.7		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 20kHz to 10MHz		5		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/V_N • √5MHz		–96		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±3.6		V
TRANSFER CHARACTERISTICS					
Voltage Gain	R_L = 1kΩ, V_{IN} = ±2V		0.982		V/V
	R_L = 10kΩ, V_{IN} = ±2.8V	0.98	0.992		V/V
RATED OUTPUT					
Voltage	V_{IN} = ±3V	±2.8	±2.97		V
Resistance	One Channel Selected		12.5		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.2		pF
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2		V_{CC} +0.6	V
Logic 0 Voltage				+0.8	V
Logic 1 Current	V_{SEL} = 5.0V	75	100	125	µA
Logic 0 Current	V_{SEL} = 0.8V		0.002	5	µA
SWITCHING CHARACTERISTICS	V_I = –0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_{OUT} = 1Vp-p		0.13		µs
SEL to Channel OFF Time	10% Point of V_{OUT} = 1Vp-p		0.17		µs
Switching Transient, Positive	(Measured While Switching		+13		mV
Switching Transient, Negative	Between Two Grounded Channels)		–4		mV
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected, Over Temperature		±4.6	±5.3	mA
	No Channel Selected, Over Temperature		±120	±175	µA
Rejection Ratio			–80		dB

SPECIFICATIONS– AC CHARACTERISTICS

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC104AP, AU			UNITS
		MIN	TYP	MAX	
LARGE SIGNAL BANDWIDTH (–3dB)	V_{OUT} = 5.0Vp-p, C_{OUT} = 1pF		55		MHz
	V_{OUT} = 2.8Vp-p, C_{OUT} = 1pF		101		MHz
	V_{OUT} = 1.4Vp-p, C_{OUT} = 1pF		210		MHz
SMALL SIGNAL BANDWIDTH	V_{OUT} = 0.2Vp-p, C_{OUT} = 1pF		590		MHz
GROUP DELAY TIME			550		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_{IN} = 0.3Vp-p				
	VDC = 0 to 0.7V		0.03		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_{IN} = 0.3Vp-p				
	VDC = 0 to 0.7V		0.01		Degrees
GAIN FLATNESS PEAKING	V_{OUT} = 0.2Vp-p, DC to 30MHz		0.05		dB
	V_{OUT} = 0.2Vp-p, DC to 100MHz		0.07		dB
HARMONIC DISTORTION	f = 30MHz, V_{OUT} = 1.4Vp-p				
Second Harmonic			–63		dBc
Third Harmonic			–65		dBc
CROSSTALK	V_{IN} = 1.4Vp-p				
MPC104AP All Hostile	f = 5MHz,		–90		dB
	f = 30MHz,		–77		dB
Off Isolation	f = 5MHz,		–93		dB
	f = 30MHz,		–81		dB
MPC104AU All Hostile	f = 5MHz,		–95		dB
	f = 30MHz,		–79		dB
Off Isolation	f = 5MHz,		–93		dB
	f = 30MHz		–86		dB
RISE/FALL TIME	V_{OUT} = 1.4Vp-p, Step 10% to 90%				
	C_{OUT} = 1pF, R_{OUT} = 22Ω		2.3		ns
SLEW RATE	V_{OUT} = 1.4Vp-p				
	C_{OUT} = 1pF		500		V/µs
	C_{OUT} = 22pF		360		V/µs
	C_{OUT} = 47pF		260		V/µs

CONNECTION DIAGRAM



PIN DESCRIPTION

PIN	DESCRIPTION
IN_1, IN_2	Analog Input Channels
GND	Analog Input Shielding Grounds, Connect to System Ground
SEL_1, SEL_2	Channel Selection Inputs
V_{OUT}	Analog Output; tracks selected channel
$-V_{CC}$	Negative Supply Voltage; typical –5VDC
$+V_{CC}$	Positive Supply Voltage; typical +5VDC

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6VDC
Analog Input Voltage (IN_1 through IN_2)	$\pm V_{CC}$, ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Output Current	±6mA
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL_1 through SEL_2)	–0.5V to $+V_{CC}$ +0.7V

PACKAGE INFORMATION

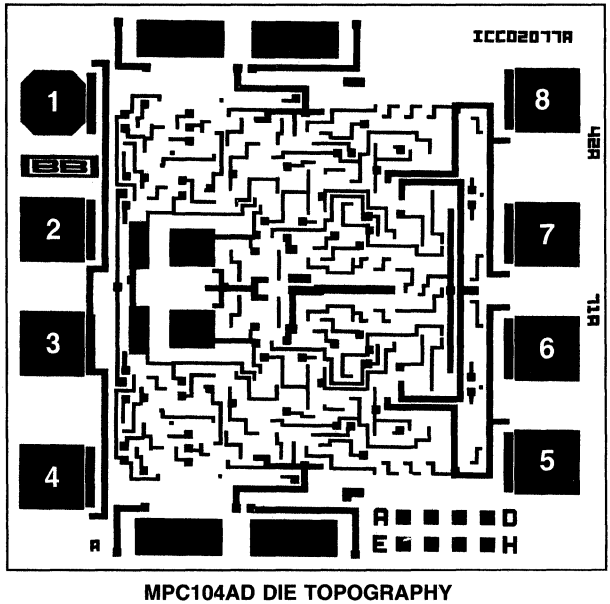
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC104AP	8-Pin DIP	006
MPC104AU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC104AP	8-Pin Plastic DIP	–40°C to +85°C
MPC104AU	8-Pin SOIC	–40°C to +85°C

DICE INFORMATION



MPC104AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Input 1
2	Ground
3	+5V Supply
4	Input 2
5	Select 2
6	Output
7	–5V Supply
8	Select 1

Substrate Bias: Negative Supply.
NC: No Connection.
Wire Bonding: Gold wire bonding is recommended.

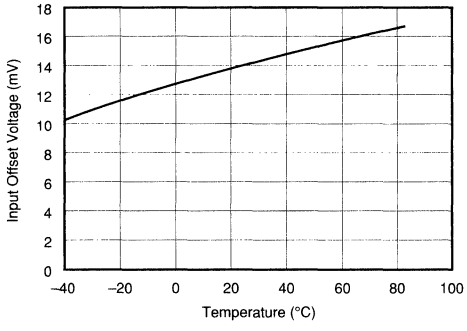
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	44 x 47 ±5	1.13 x 1.19 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

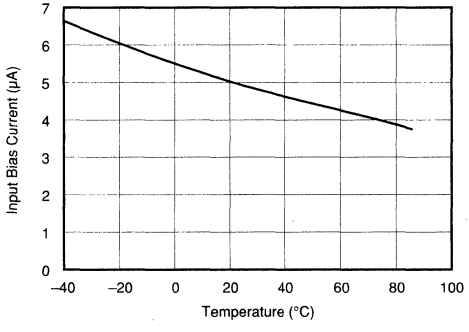
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

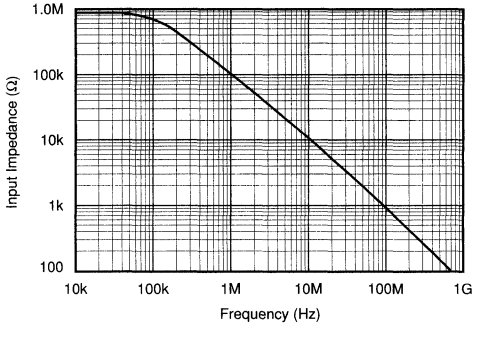
INPUT OFFSET VOLTAGE vs TEMPERATURE



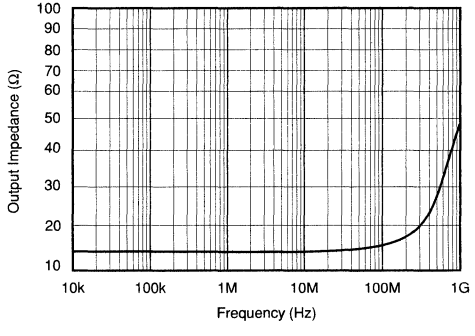
INPUT BIAS CURRENT vs TEMPERATURE



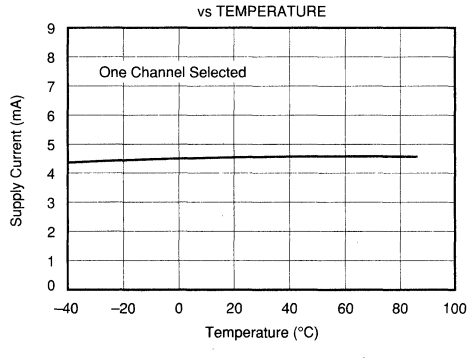
INPUT IMPEDANCE vs FREQUENCY



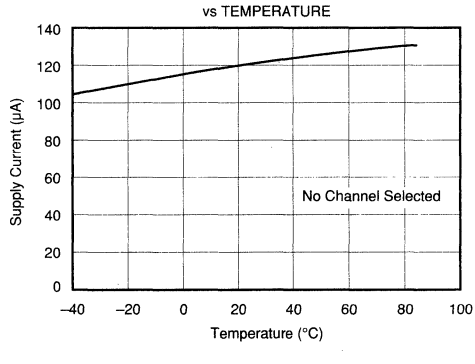
OUTPUT IMPEDANCE vs FREQUENCY



TOTAL POSITIVE QUIESCENT CURRENT vs TEMPERATURE



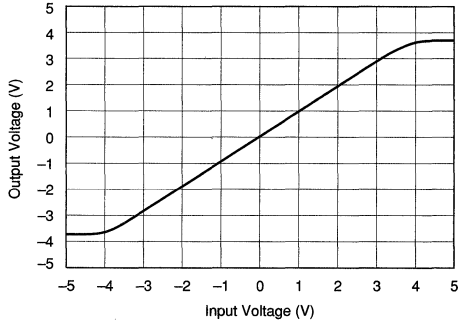
TOTAL POSITIVE QUIESCENT CURRENT vs TEMPERATURE



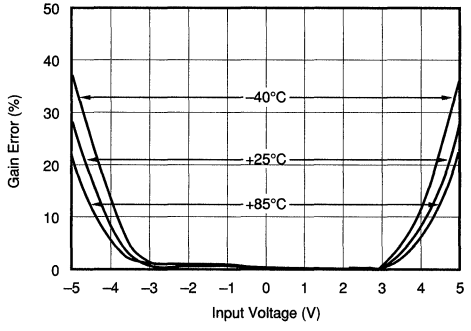
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

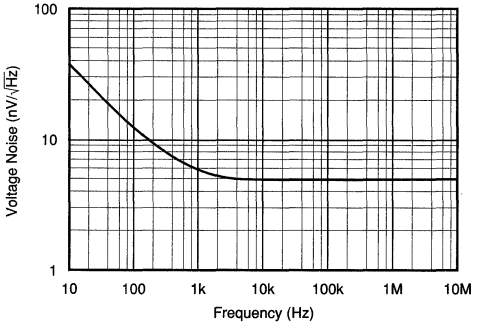
TRANSFER FUNCTION



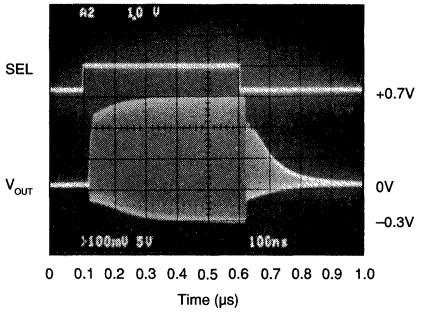
GAIN ERROR vs INPUT VOLTAGE

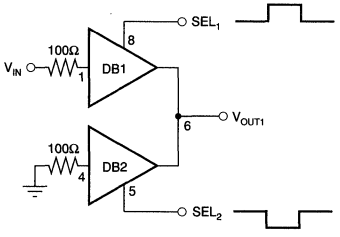


INPUT VOLTAGE NOISE SPECTRAL DENSITY

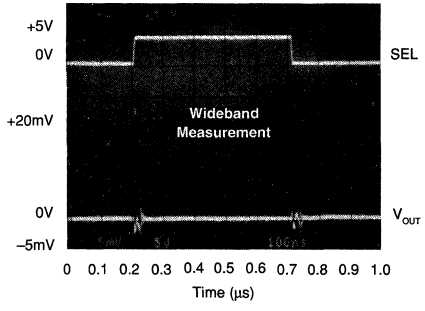


SWITCHING ENVELOPE
(Channel-to-Channel Switching)

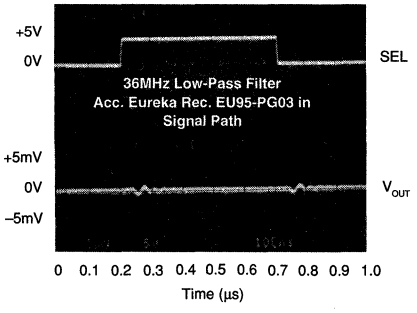




SWITCHING TRANSIENTS



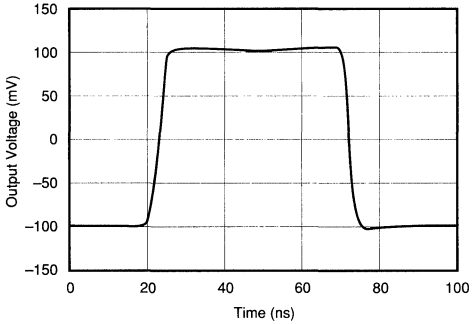
SWITCHING TRANSIENTS



TYPICAL PERFORMANCE CURVES (CONT)

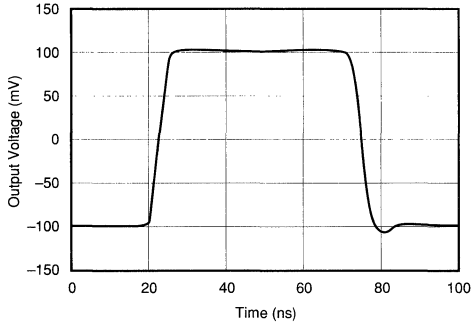
At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE



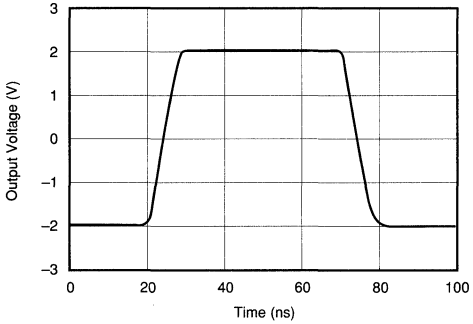
V_{IN} = 0.2Vp-p, C_{OUT} = 1pF
t_{RISE} = t_{FALL} = 2ns (Generator)

SMALL SIGNAL PULSE RESPONSE



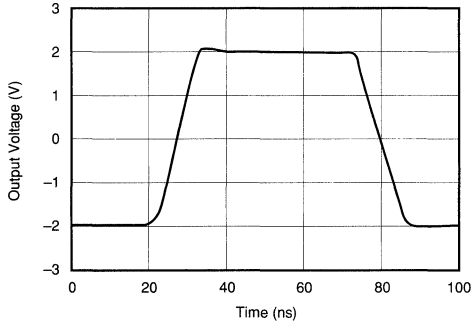
V_{IN} = 0.2Vp-p, C_{OUT} = 47pF
t_{RISE} = t_{FALL} = 2ns (Generator)

LARGE SIGNAL PULSE RESPONSE



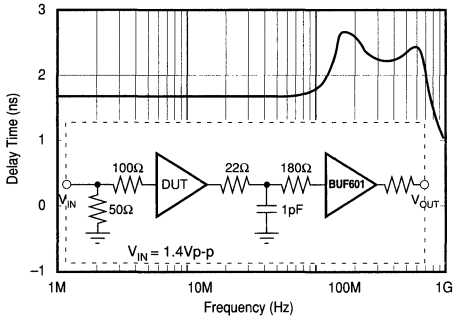
V_{IN} = 4Vp-p, C_{OUT} = 1pF
t_{RISE} = t_{FALL} = 2ns (Generator)

LARGE SIGNAL PULSE RESPONSE

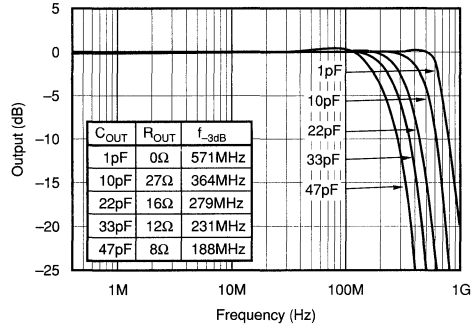


V_{IN} = 4Vp-p, C_{OUT} = 47pF
t_{RISE} = t_{FALL} = 2ns (Generator)

GROUP DELAY TIME vs FREQUENCY



BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}

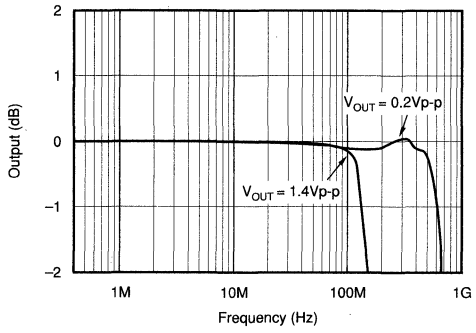


C_{OUT}	R_{OUT}	f_{-3dB}
1pF	0Ω	571MHz
10pF	27Ω	364MHz
22pF	16Ω	279MHz
33pF	12Ω	231MHz
47pF	8Ω	188MHz

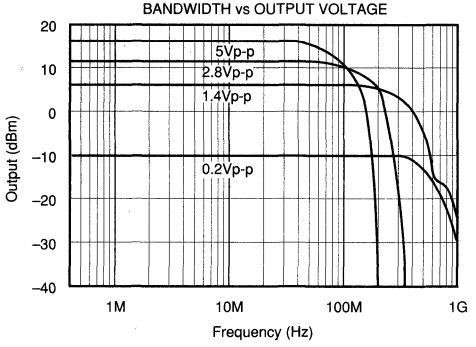
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 10kΩ, R_{IN} = 100Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

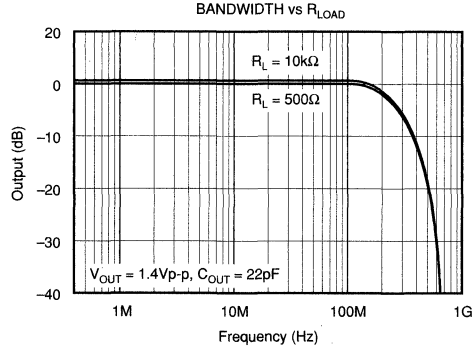
GAIN FLATNESS



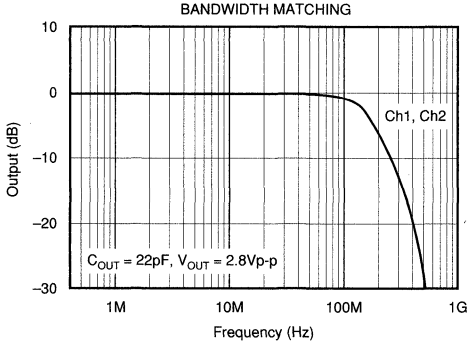
BANDWIDTH vs OUTPUT VOLTAGE



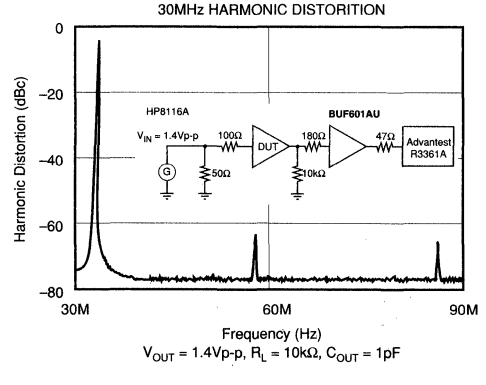
BANDWIDTH vs R_{LOAD}



BANDWIDTH MATCHING

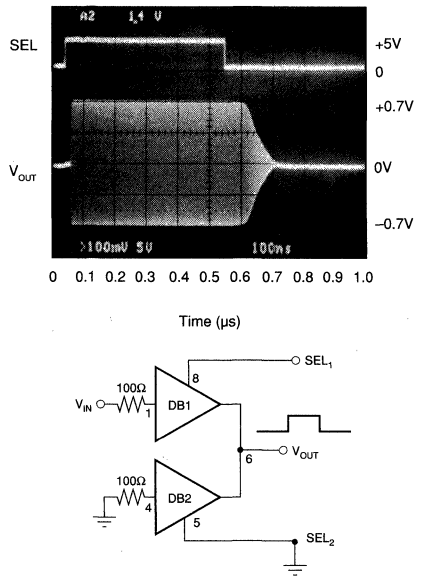


30MHz HARMONIC DISTORITION



V_{OUT} = 1.4Vp-p, R_L = 10kΩ, C_{OUT} = 1pF

ON/OFF CHARACTERISTIC



APPLICATIONS INFORMATION

The MPC104 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

As shown below, all pins on the MPC104 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the characteristics of the buffer amplifier input without necessarily destroying the device. In precision buffer amplifiers, such damage may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC104.

Static damage has been well-recognized as a problem for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC104 incorporates on-chip ESD protection diodes as shown in Figure 1. Thus the user does not need to add external protection diodes, which can add capacitance and degrade AC performance.

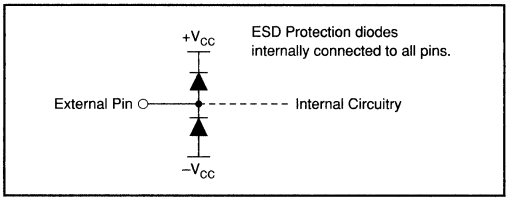


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC104 is a 2 x 1, wide-band analog signal multiplexer. It allows the user to connect one of the two inputs (IN_1/IN_2) to the output. The switching speed between two input channels is typically less than 300ns.

However, in contrast to signal switches using CMOS or DMOS transistors, the switching transients were kept very low at +13mV and –4mV. The MPC104 consists of two identical unity-gain buffer amplifiers, respectively connected together internally at the output. The open-loop buffer amps, which consist of complementary emitter followers, apply no feedback so their low-frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form a unidirectional transmission path, thus providing high output-to-input isolation. Switching stages compatible to TTL-level digital signals are provided for each buffer to select the input channel. When no channel is selected, the outputs of the device are high-impedance and allow the user to wire several MPC104s together to create multichannel switch matrices.

Chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. The buffers require DC coupling and termination resistors when driven directly from a low-impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated, high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 210MHz at an output voltage of 1.4Vp-p allows the design of multi-channel crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz, or in quality for high resolution graphic and imaging systems with 200MHz system bandwidth. The buffer amplifiers also offer low differential gain (0.03%) and phase (0.01°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the luminance signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.2pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC104 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short time, but it hardly interferes with the input signals. The transient peaks remain less than +13mV and –4mV. The generated output transients are extremely small, so DC clamping during switching between channels is unnecessary. DC clamping during the switching dead time is re-

quired to avoid synchronization by large negative output glitches in subsequent equipment.

The SEL-to-channel-ON time is typically 25ns and always shorter than the typical SEL-to-channel-OFF time of 250ns. In the worst case, an ON/OFF margin of 150ns ensures safe switching even for timing spreads in the digital control latches. The short interchannel switching time of 300ns allows channel change during the vertical blanking time, even in high-resolution graphic or broadcast systems. As shown in the typical performance curves, the signal envelope during transition from one channel to another rises and falls symmetrically and shows less overshooting and DC settling effects.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffer amplifiers are in the off-state. One important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±120µA when no channel is selected and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC104 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance or inductance.
- Make short and low inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.
- Use low-inductance and surface-mounted components. Circuits using all surface mount components with the MPC104 will offer the best AC-performance.
- A resistor (100Ω to 150Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

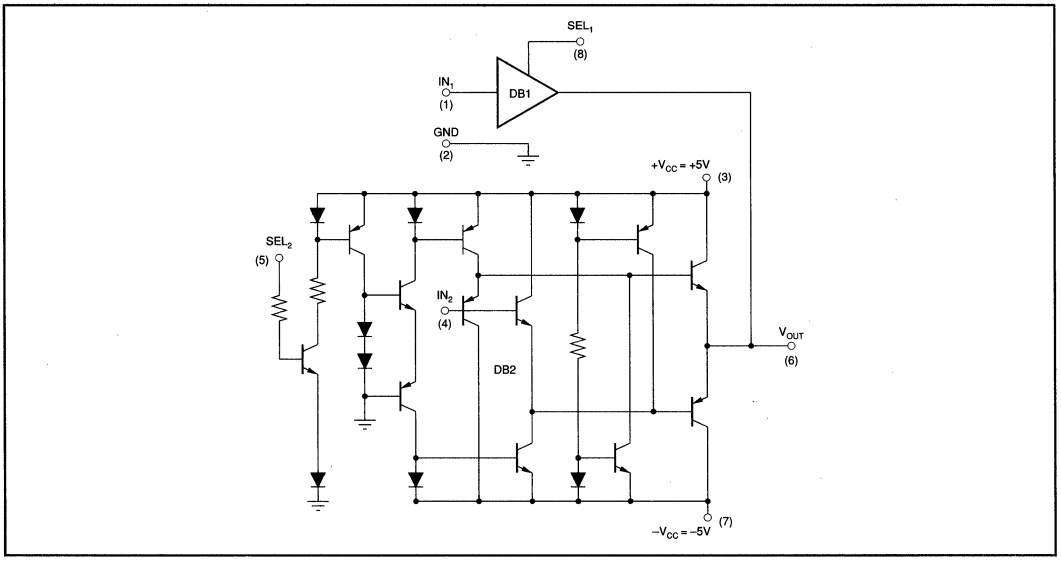
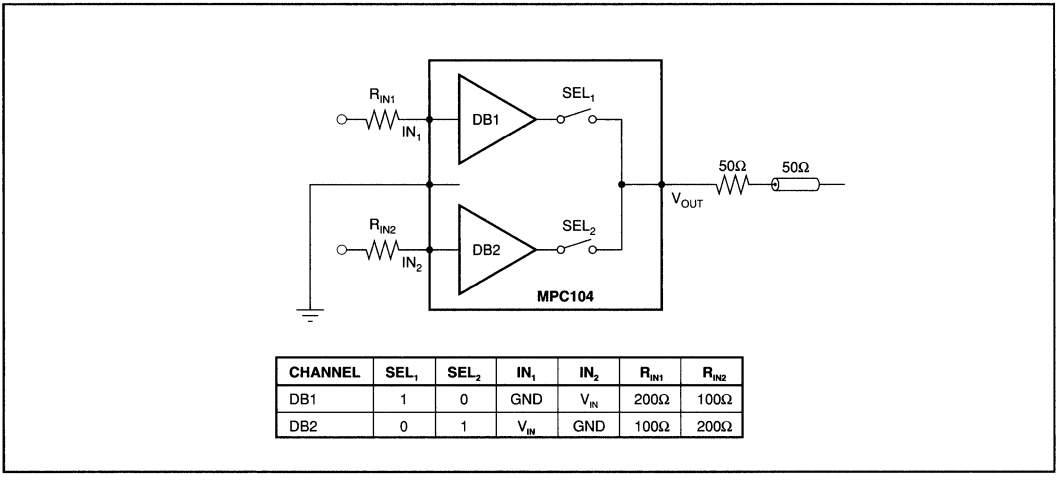
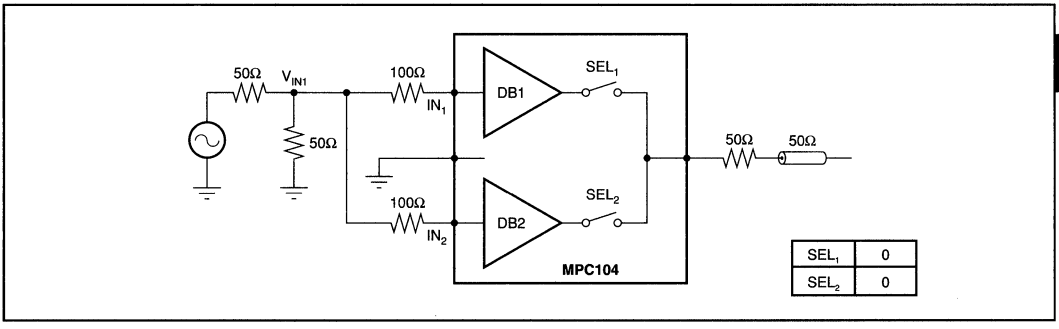


FIGURE 2. Simplified Circuit Diagram.



CHANNEL	SEL_1	SEL_2	IN_1	IN_2	R_{IN1}	R_{IN2}
DB1	1	0	GND	V_{IN}	200Ω	100Ω
DB2	0	1	V_{IN}	GND	100Ω	200Ω

FIGURE 3. All Hostile Crosstalk Test Circuit 1.



SEL_1	0
SEL_2	0

FIGURE 4. Off Isolation Crosstalk Test Circuit 2.

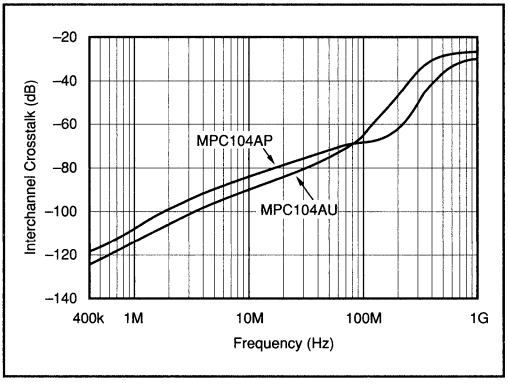


FIGURE 5. Interchannel Crosstalk.

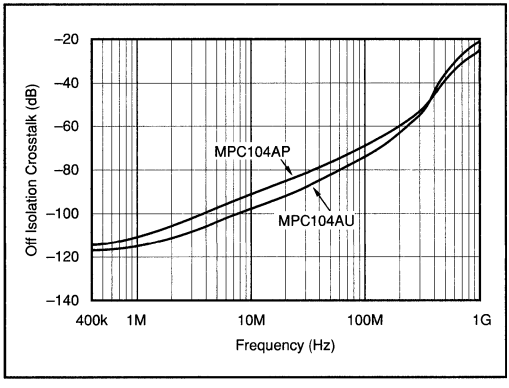


FIGURE 6. Off Isolation Crosstalk.

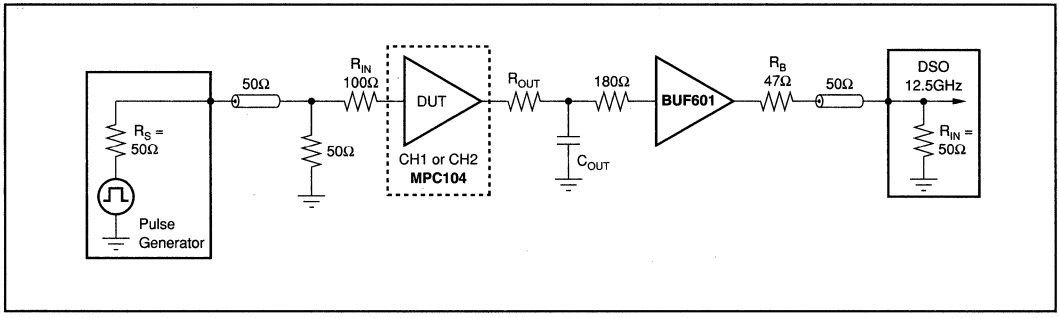


FIGURE 7. Test Circuit Pulse Response.

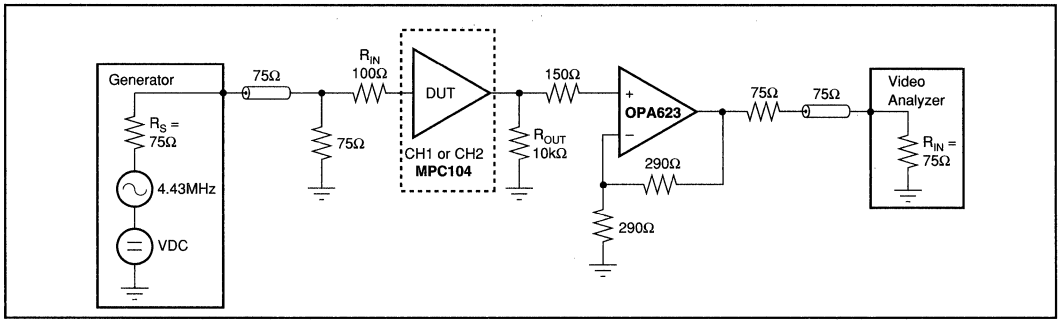


FIGURE 8. Test Circuit Differential Gain and Phase.

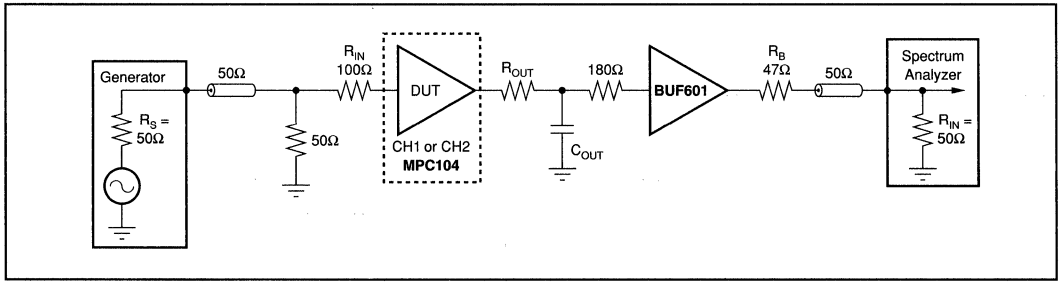


FIGURE 9. Test Circuit Frequency Response.

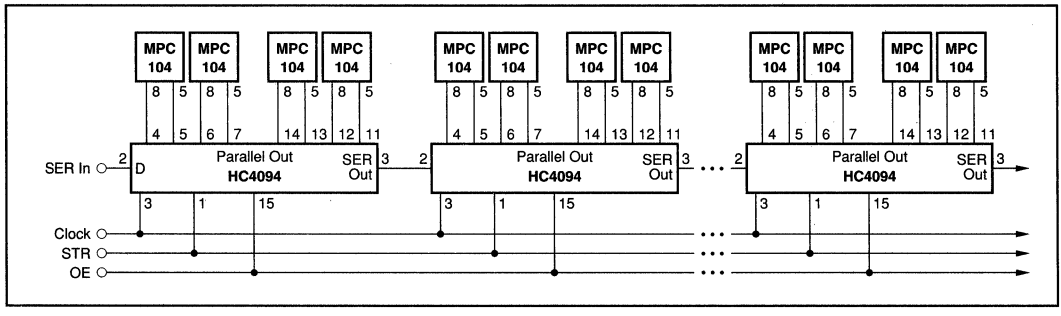


FIGURE 10. Serial Bus-Controlled Distribution Field.

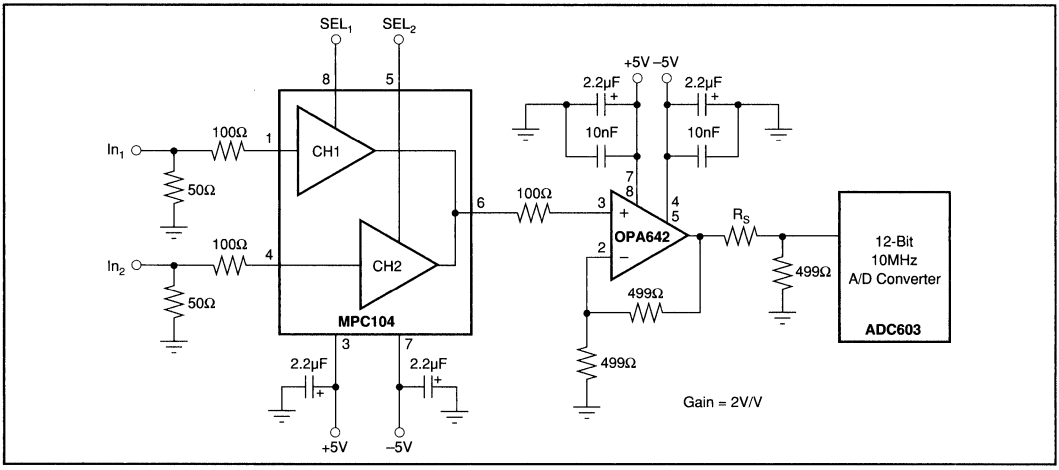


FIGURE 11. High-Speed Data Acquisition System.

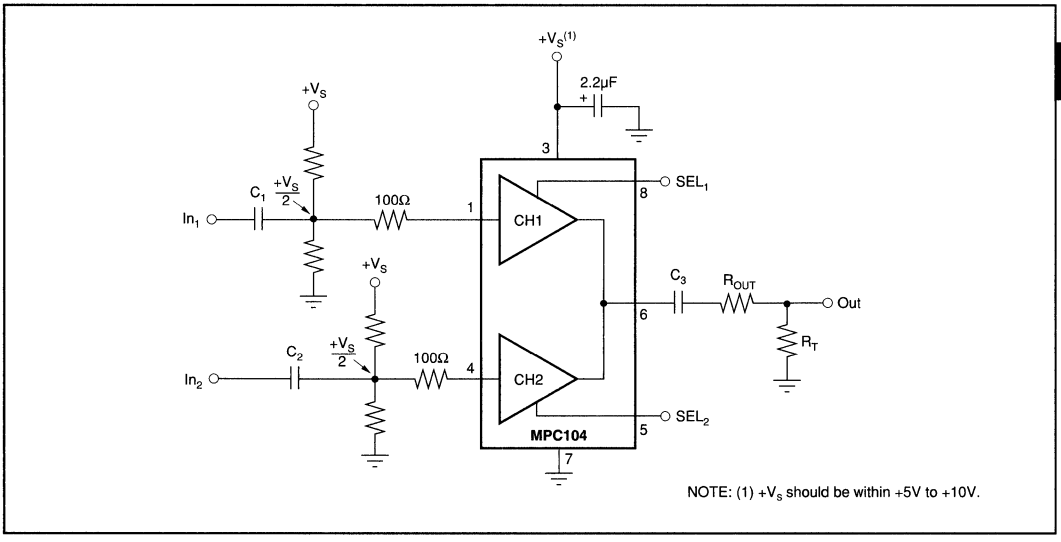


FIGURE 12. Single Supply Operation.

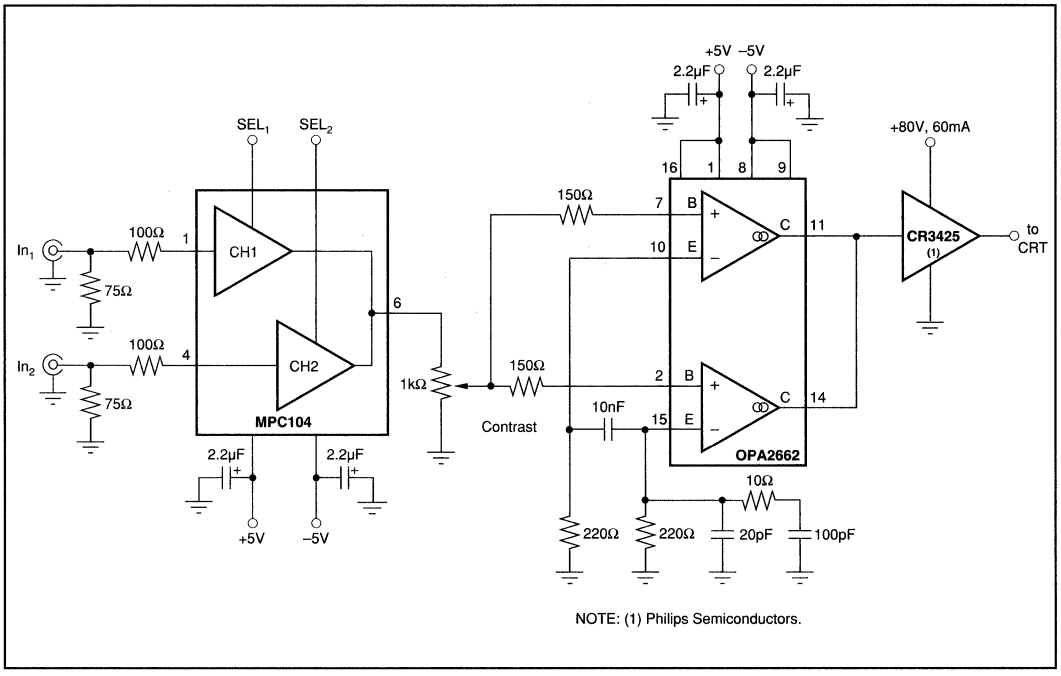


FIGURE 13. Input Multiplexer for a CRT Output Stage.

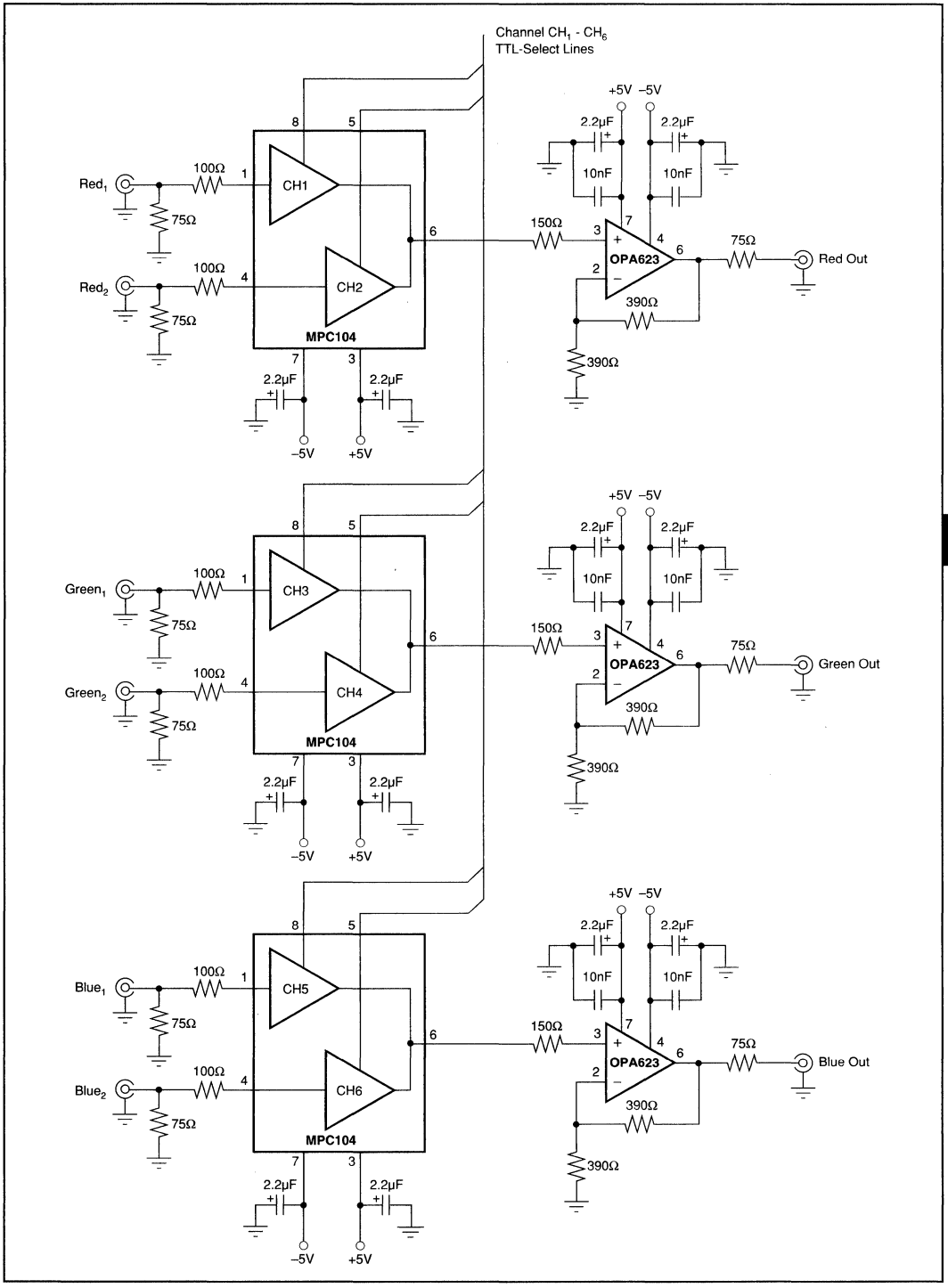


FIGURE 14. Input Multiplexer for RGB Video Signals.

BURR-BROWN®

MPC506A
MPC507A

Single-Ended 16-Channel/Differential 8-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- **ANALOG OVERVOLTAGE PROTECTION: 70Vp-p**
- **NO CHANNEL INTERACTION DURING OVERVOLTAGE**
- **BREAK-BEFORE-MAKE SWITCHING**
- **ANALOG SIGNAL RANGE: ±15V**
- **STANDBY POWER: 7.5mW typ**
- **TRUE SECOND SOURCE**

DESCRIPTION

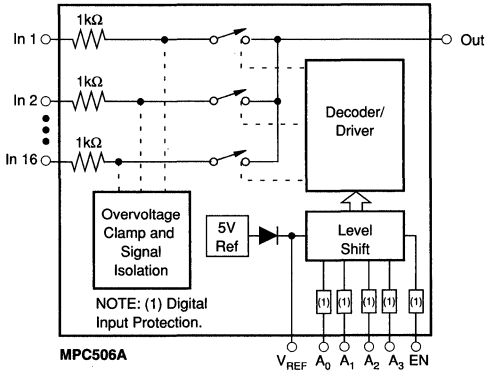
The MPC506A is a 16-channel single-ended analog multiplexer, and the MPC507A is an 8-channel differential multiplexer.

The MPC506A and MPC507A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

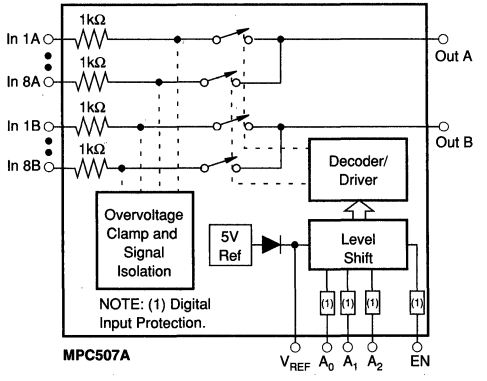
These features make the MPC506A and MPC507A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC506A and MPC507A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic or plastic DIP and plastic SOIC packages. Temperature range is –40/+85°C.

FUNCTIONAL DIAGRAMS



MPC506A



MPC507A

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

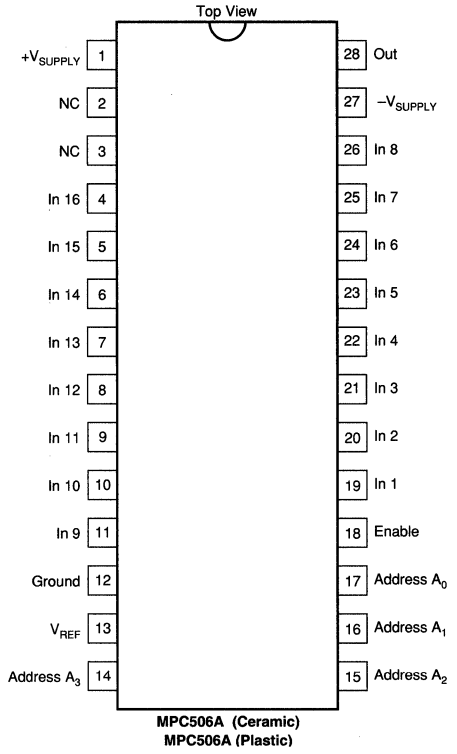
SPECIFICATIONS

Supplies = +15V, –15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V unless otherwise specified.

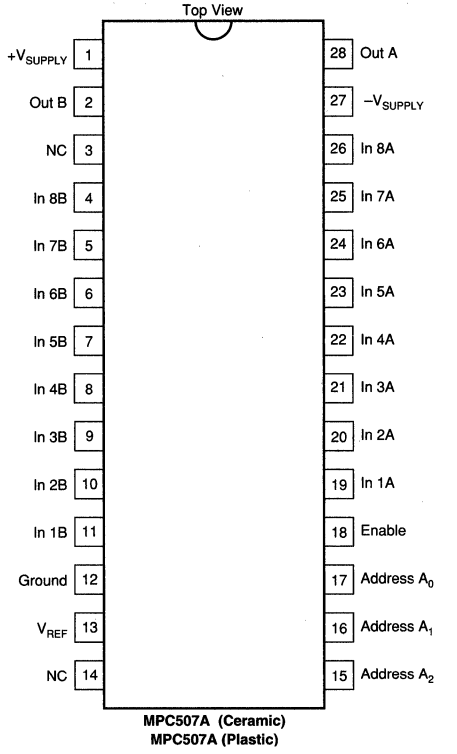
PARAMETER	TEMP	MPC506A/MPC507A MIN	MPC506A/MPC507A TYP	MPC506A/MPC507A MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS					
V_S, Analog Signal Range	Full	–15		+15	V
R_{ON}, On Resistance(1)	+25°C		1.3	1.5	kΩ
	Full		1.5	1.8	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.5		nA
	Full			10	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.2		nA
MPC506A	Full			5	nA
MPC507A	Full			5	nA
I_D (OFF) with Input Overvoltage Applied(2)	+25°C		4.0		nA
	Full				µA
I_D (ON), On Channel Leakage Current	+25°C		2		nA
MPC506A	Full			10	nA
MPC507A	Full			10	nA
I_{DIFF} Differential Off Output Leakage Current (MPC507A Only)	Full			10	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold	Full			0.8	V
V_{AH}, Input High Threshold(3)	Full	4.0			V
V_{AL}, MOS Drive(4)	+25°C			0.8	V
V_{AH}, MOS Drive(4)	+25°C	6.0			V
I_A, Input Leakage Current (High or Low)(5)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.3		µs
	Full			0.6	µs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		200		ns
	Full			500	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		250		ns
	Full			500	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.01%)	+25°C		3.5		µs
"OFF Isolation"(6)	+25°C	50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5		pF
C_D (OFF), Channel Output Capacitance: MPC506A	+25°C		50		pF
MPC507A	+25°C		25		pF
C_A, Digital Input Capacitance	25°C		5		pF
C_{DS}, (OFF), Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
I+, Current Pin 1(7)	Full		0.7	1.5	mA
I–, Current Pin 27(7)	Full		5	20	µA

NOTES: (1) V_{OUT} = ±10V, I_{OUT} = –100µA. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) V_{REF} = +10V. (5) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (6) V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = 7Vrms, f = 100kHz. Worst-case isolation occurs on channel 8 due to proximity of the output pins. (7) V_{EN}, V_A = 0V or 4.0V.

PIN CONFIGURATION



MPC506A (Ceramic)
MPC506A (Plastic)



MPC507A (Ceramic)
MPC507A (Plastic)

TRUTH TABLES

MPC506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

MPC507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC506AP	28-Pin Plastic	215
MPC506AG	28-Pin Ceramic	126
MPC506AU	28-Pin Plastic SOIC	217
MPC507AP	28-Pin Plastic	215
MPC507AG	28-Pin Ceramic	126
MPC507AU	28-Pin Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS[1]

Voltage between supply pins 44V
V_{REF} to ground, V+ to ground 22V
V– to ground 25V
Digital input overvoltage:
V_{EN}, V_A: V_{SUPPLY} (+) ..... +4V
V_{SUPPLY} (–) ..... –4V
or 20mA, whichever occurs first.
Analog input overvoltage:
V_S: V_{SUPPLY} (+) ..... +20V
V_{SUPPLY} (–) ..... –20V
Continuous current, S or D 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation* 2.0W
Operating temperature range ..... –40°C to +85°C
Storage temperature range ..... –65°C to +150°C

*Derate 20.0mW/°C above T_A = 70

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

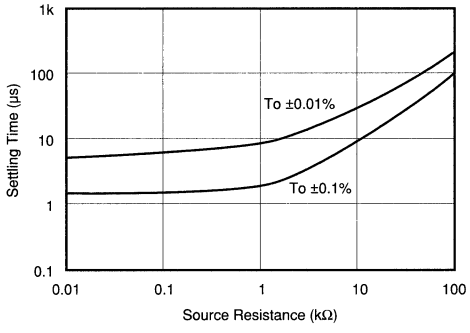
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	DESCRIPTION
MPC506AP	28-Pin Plastic DIP	–40°C to +85°C	16-Channel Single-Ended
MPC506AG	28-Pin Ceramic DIP	–40°C to +85°C	16-Channel Single-Ended
MPC506AU	28-Pin Plastic SOIC	–40°C to +85°C	16-Channel Single-Ended
MPC507AP	28-Pin Plastic DIP	–40°C to +85°C	8-Channel Differential
MPC507AG	28-Pin Ceramic DIP	–40°C to +85°C	8-Channel Differential
MPC507AU	28-Pin Plastic SOIC	–40°C to +85°C	8-Channel Differential

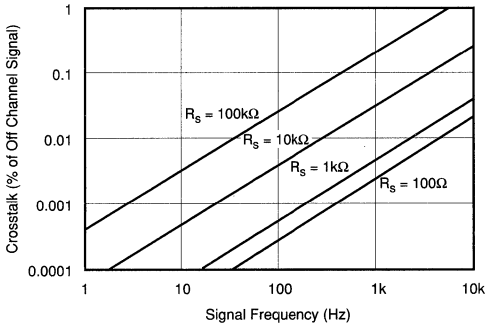
TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

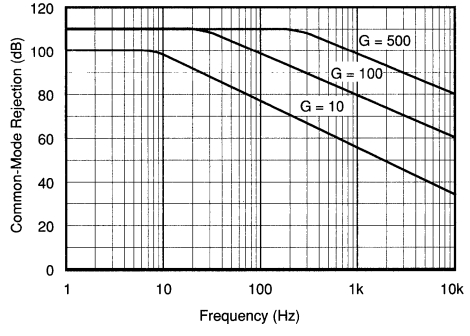
SETTLING TIME vs SOURCE RESISTANCE FOR 20V STEP CHANGE



CROSSTALK vs SIGNAL FREQUENCY



COMBINED CMR vs FREQUENCY MPC507A AND INA110



DISCUSSION OF SPECIFICATIONS

DC CHARACTERISTICS

The static or dc transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
dc offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedance of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- *Use sources with impedances as low as possible.* A 1000Ω source resistance will present less than 0.001% loading error and 10kΩ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1).

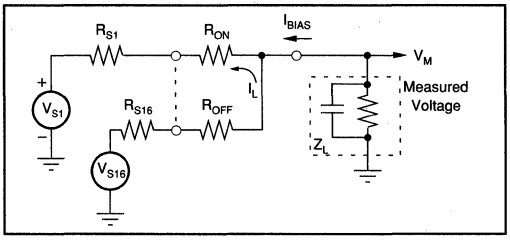


FIGURE 1. MPC506A Static Accuracy Equivalent Circuit.

Source and Multiplexer Resistive Loading Error

$$\in (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20μV if a 1kΩ source is used. In general, for the MPC506A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications.

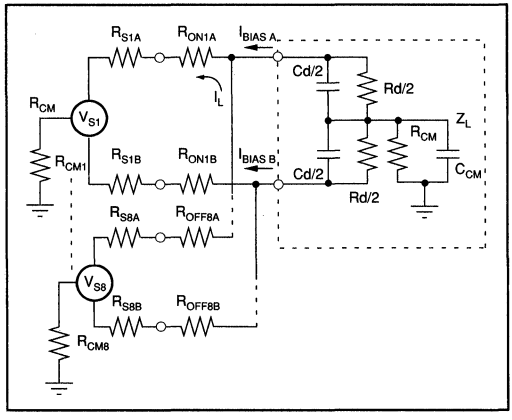


FIGURE 2. MPC507A Static Accuracy Equivalent Circuit.

Load (Output Device) Characteristics

- *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system dc common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC507A is used for multiplexing high-level signals of 1V to 10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation i = C (dV/dt), the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The trade-off for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\ dt$$

where i = C (dV/dt) of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

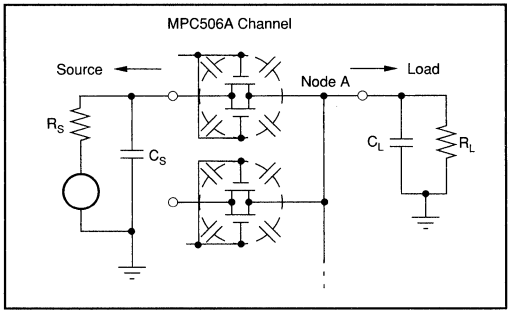


FIGURE 3. Settling Time Effects—MPC506A.

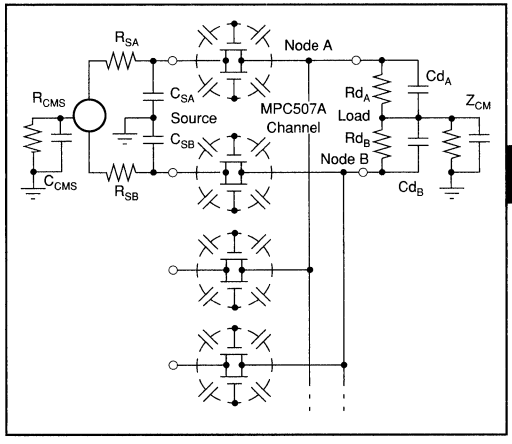


FIGURE 4. Settling and Common-Mode Effects—MPC507A

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the seven (MPC507A) or 15 (MPC506A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1000Hz sine wave applied to all off channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (MPC507A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC507A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC507A and Burr-Brown's INA110 instrumentation amplifier (G = 100) is 110dB at DC to 10Hz with a 6dB/octave roll-off to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown INA110 instrumentation amplifier connected for gains of 500, 100, and 10.

Factors which will degrade multiplexer and system DC CMR are:

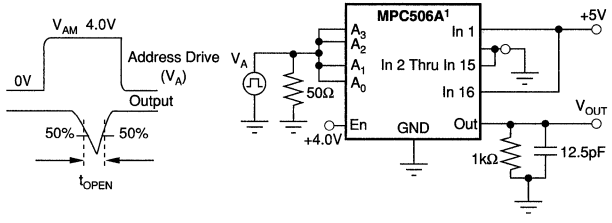
- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR roll-off is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

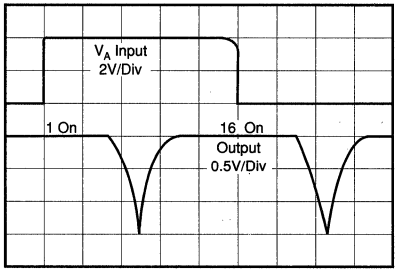
SWITCHING WAVEFORMS

Typical at +25°C, unless otherwise noted.

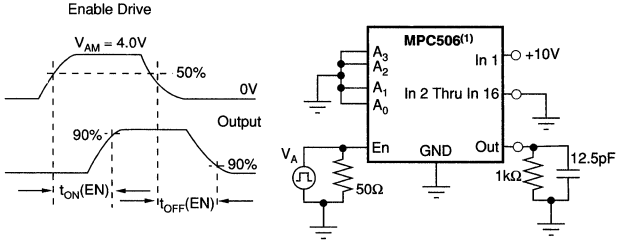
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



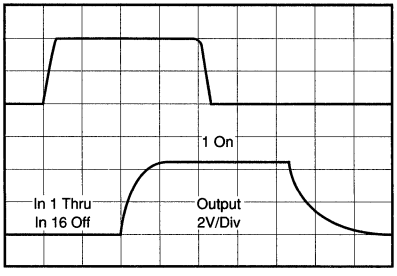
NOTE: (1) Similar connection for MPC507A.



ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))



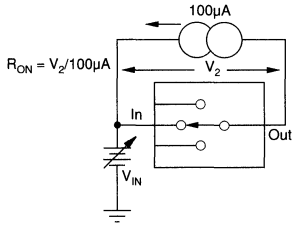
NOTE: (1) Similar connection for MPC507A.

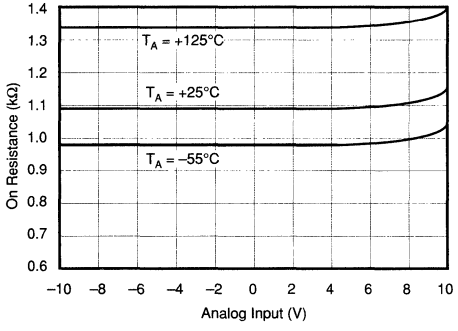


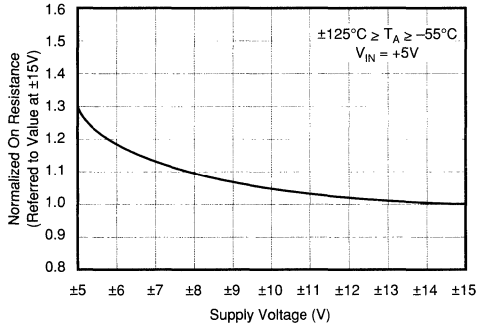
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

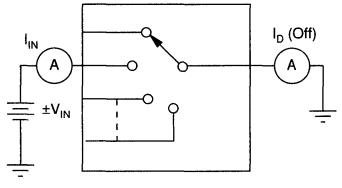
ON RESISTANCE vs INPUT SIGNAL, SUPPLY VOLTAGE

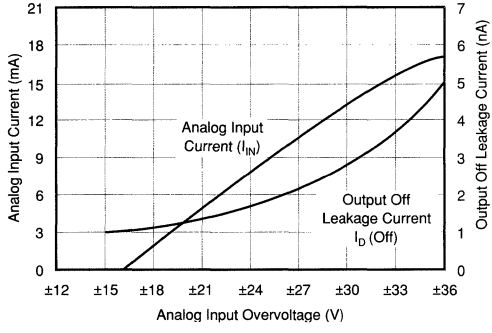






ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

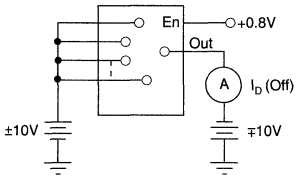


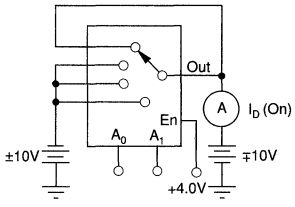


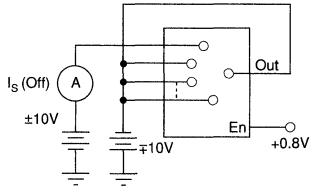
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

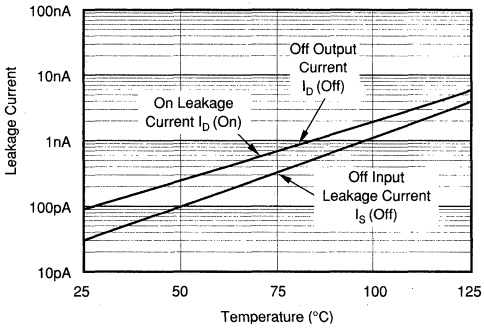
T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

LEAKAGE CURRENT vs TEMPERATURE



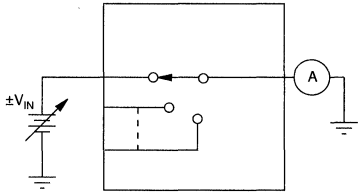


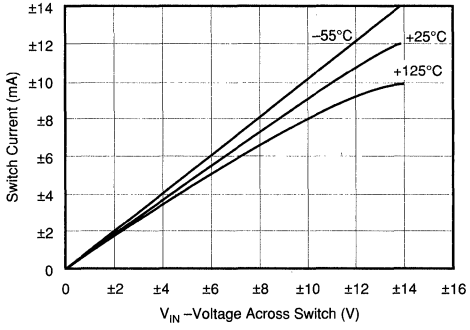




NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V. (Two measurements per device for I_D (Off): +10V/–10V and –10V/+10V).

ON-CHANNEL CURRENT vs VOLTAGE

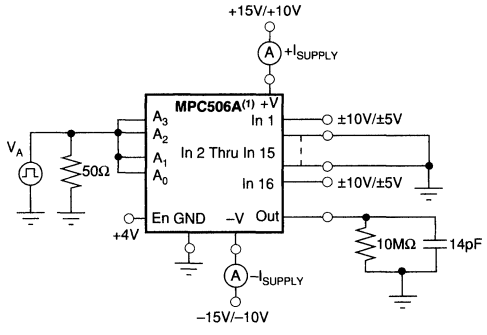




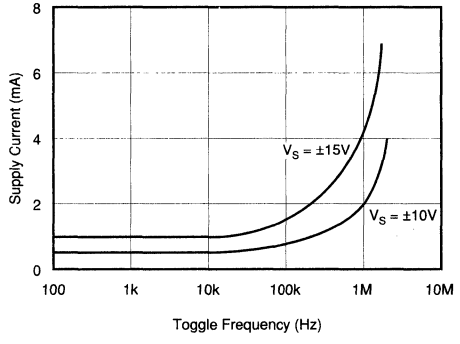
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

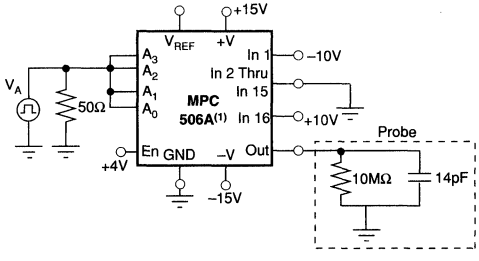
SUPPLY CURRENT vs TOGGLE FREQUENCY



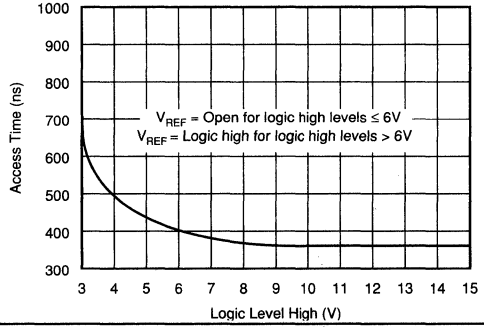
NOTE: (1) Similar connection for MPC507A.



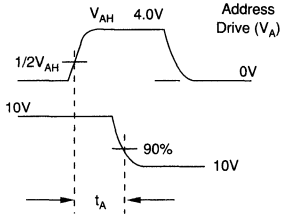
ACCESS TIME vs LOGIC LEVEL (High)

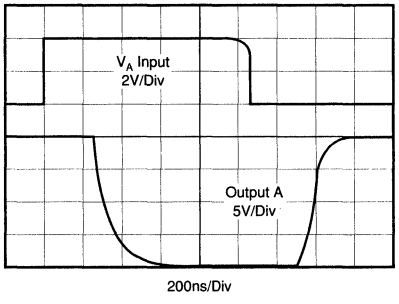


NOTE: (1) Similar connection for MPC507A.



ACCESS TIME WAVEFORM





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 3-bit (MPC507A or 4-bit MPC506A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15V and/or –15V supply voltage is absent or shorted to ground, the MPC507A and MPC506A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull up resistors are recommended (see Typical Performance Curves, Access Time).

To preserve common-mode rejection of the MPC507A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

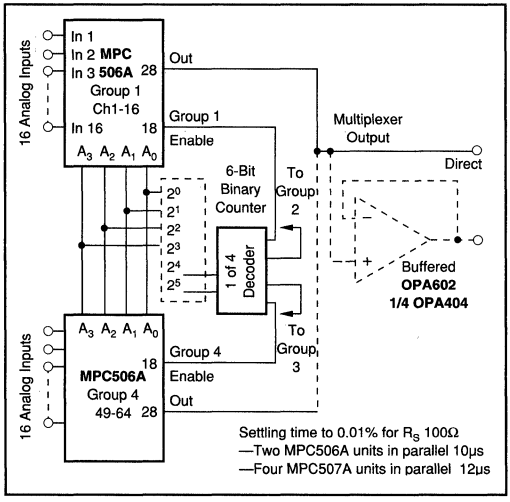


FIGURE 5. 64-Channel, Single-Tier Expansion.

CHANNEL EXPANSION

Single-Ended Multiplexer (MPC506A)

Up to 64 channels (four multiplexers) can be connected to a single node, or up to 256 channels using 17 MPC506A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

Differential Multiplexer (MPC507A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or an 8 x 8 configuration.

Single-Node Expansion

The 64x1 configuration is simply eight (MPC507A) units tied to a single node. Programming is accomplished with a 6-bit counter, using the 3LSBs of the counter to control Channel Address inputs A_0, A_1, A_2 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC507A multiplexers.

Two-Tier Expansion

Using an 8x8 two-tier structure for expansion to 64 channels, the programming is simplified. The 6-bit counter output does not require a 1-of-8 decoder. The 3LSBs of the counter drive the A_0, A_1 and A_2 inputs of the eight first-tier multiplexers and the 3MSBs of the counter are applied to the A_0, A_1, and A_2 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multitiered configuration.

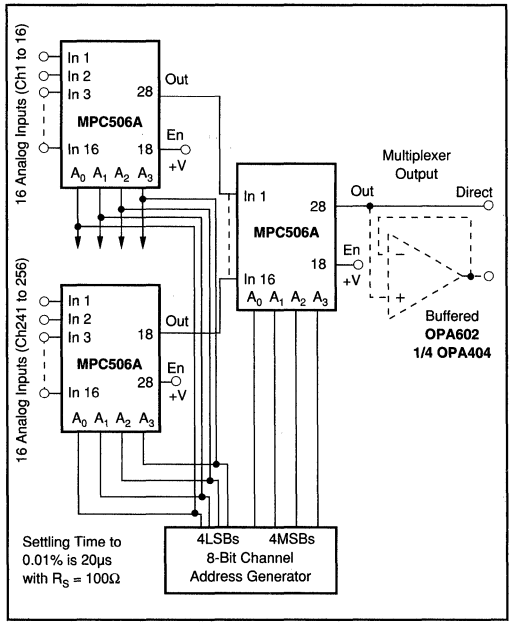


FIGURE 6. Channel Expansion up to 256 Channels Using 16x16 Two-Tiered Expansion

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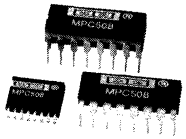


MPC508A
MPC509A

Single-Ended 8-Channel/Differential 4-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- ANALOG OVERVOLTAGE PROTECTION: 70Vp-p
- NO CHANNEL INTERACTION DURING OVERVOLTAGE
- BREAK-BEFORE-MAKE SWITCHING
- ANALOG SIGNAL RANGE: ±15V
- STANDBY POWER: 7.5mW typ
- TRUE SECOND SOURCE

DESCRIPTION

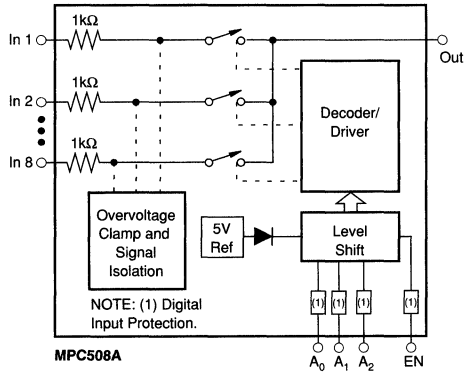
The MPC508A is an 8-channel single-ended analog multiplexer and the MPC509A is a 4-channel differential multiplexer.

The MPC508A and MPC509A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

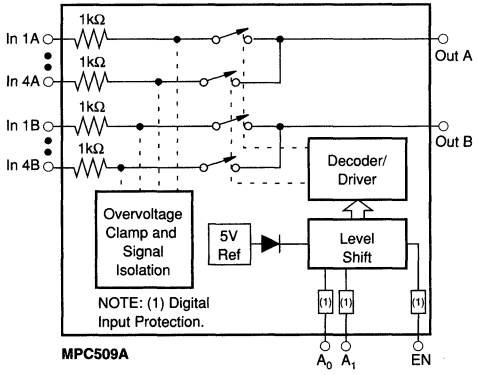
These features make the MPC508A and MPC509A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC508A and MPC509A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic or plastic DIP and plastic SOIC packages. Temperature range is –40°C to +85°C.

FUNCTIONAL DIAGRAMS



MPC508A



MPC509A

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

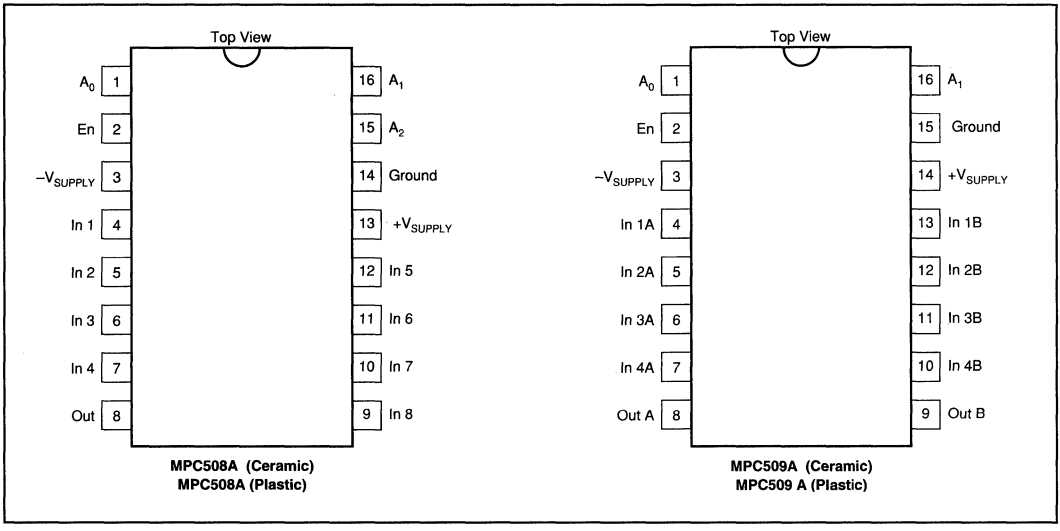
ELECTRICAL

Supplies = +15V, −15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V, unless otherwise specified.

PARAMETER	TEMP	MPC508A/509A MIN	MPC508A/509A TYP	MPC508A/509A MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS					
V_S, Analog Signal Range	Full	−15		+15	V
R_{ON}, On Resistance(1)	+25°C		1.3	1.5	kΩ
	Full		1.5	1.8	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.5		nA
	Full			10	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.2		nA
MPC508A	Full			5	nA
MPC509A	Full			5	nA
I_D (OFF) with Input Overvoltage Applied(2)	+25°C		4.0		nA
	Full				µA
I_D (ON), On Channel Leakage Current	+25°C		2		nA
MPC508A	Full			10	nA
MPC509A	Full			10	nA
I_{DIFF} Differential Off Output Leakage Current (MPC509A Only)	Full			10	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold Drive	Full			0.8	V
V_{AH}, Input High Threshold(3)	Full	4.0			V
I_A, Input Leakage Current (High or Low)(4)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.5		µs
	Full			0.6	µs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		200		ns
	Full			500	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		250		ns
	Full			500	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.01%)	+25°C		3.5		µs
"OFF Isolation"(5)	+25°C	50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5		pF
C_D (OFF), Channel Output Capacitance: MPC508A	+25°C		25		pF
MPC509A	+25°C		12		pF
C_A, Digital Input Capacitance	25°C		5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
I+, Current Pin 1(6)	Full		0.7	1.5	mA
I−, Current Pin 27(6)	Full		5	20	µA

NOTES: (1) V_{OUT} = ±10V, I_{OUT} = −100µA. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (5) V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = 7Vrms, f = 100kHz. Worst-case isolation occurs on channel 4 due to proximity of the output pins. (6) V_{EN}, V_A = 0V or 4.0V.

PIN CONFIGURATIONS



TRUTH TABLES

MPC508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

MPC509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

ABSOLUTE MAXIMUM RATINGS(1)

Voltage between supply pins 44V
V+ to ground 22V
V– to ground 25V
Digital input overvoltage V_{EN}, V_A:
V_{SUPPLY} (+) ..... +4V
V_{SUPPLY} (–) ..... –4V
or 20mA, whichever occurs first.
Analog input overvoltage V_S:
V_{SUPPLY} (+) ..... +20V
V_{SUPPLY} (–) ..... –20V
Continuous current, S or D 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation(2) 1.28W
Operating temperature range ..... –40°C to +85°C
Storage temperature range ..... –65°C to +150°C

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Derate 1.28mW/°C above T_A = +70°C.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	DESCRIPTION
MPC508AP	16-Pin Plastic DIP	–40°C to +85°C	8-Channel Single-Ended
MPC508AU	16-Pin Plastic SOIC	–40°C to +85°C	8-Channel Single-Ended
MPC508AG	16-Pin Ceramic DIP	–40°C to +85°C	8-Channel Single-Ended
MPC509AP	16-Pin Plastic DIP	–40°C to +85°C	4-Channel Differential
MPC509AU	16-Pin Plastic SOIC	–40°C to +85°C	4-Channel Differential
MPC509AG	16-Pin Ceramic DIP	–40°C to +85°C	4-Channel Differential

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC508/509AP	16-Pin Plastic DIP	180
MPC508/509AU	16-Pin Plastic SOIC	211
MPC508/509AG	16-Pin Ceramic	129

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DISCUSSION OF PERFORMANCE

DC CHARACTERISTICS

The static or dc transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error;
Multiplexer ON resistance error;
and, DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$, or greater, will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- *Use sources with impedances as low as possible.* 1000Ω source resistance will present less than 0.001% loading error and $10k\Omega$ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1).

Source and Multiplexer Resistive Loading Error

$$\epsilon(R_{S+}R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of $20\mu V$ if a $1k\Omega$ source is used. In general, for the MPC508A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications. Refer to Figure 2.

Load (Output Device) Characteristics

- *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system dc common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

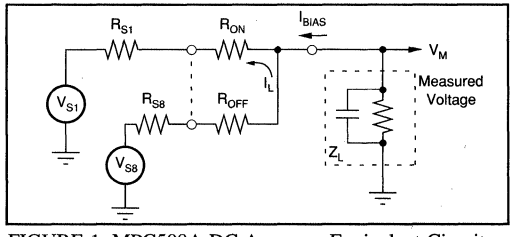


FIGURE 1. MPC508A DC Accuracy Equivalent Circuit.

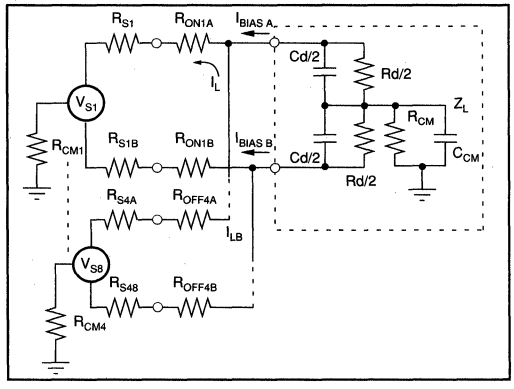


FIGURE 2. MPC509A DC Accuracy Equivalent Circuit.

Source Characteristics

- *The source impedance unbalance* will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- *Keep source impedances as low as possible* to minimize resistive loading errors.
- *Minimize ground loops.* If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC509A is used for multiplexing high-level signals of ±1V to ±10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation i = C (dV/dt), the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients, seen at the source and load, decrease proportionally as the capacitance of the load and source increase. The trade-off for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\ dt$$

where i = C (dV/dt) of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

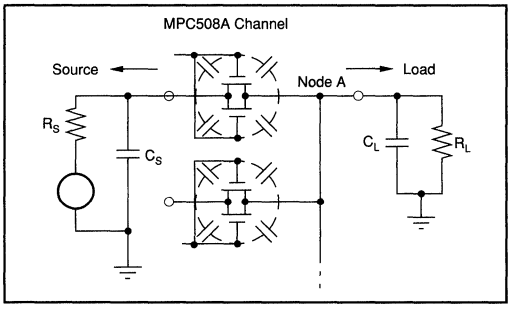


FIGURE 3. Settling Time Effects—MPC508A

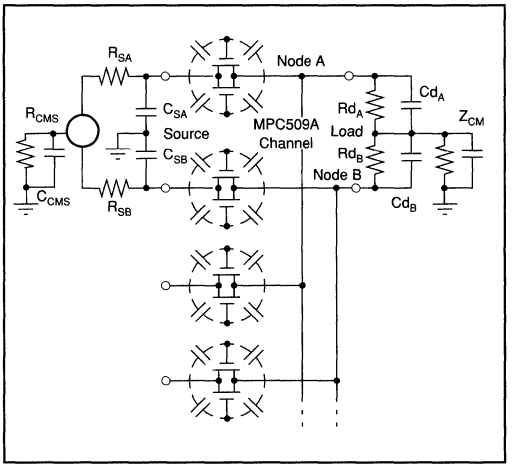


FIGURE 4. Settling and Common-Mode-Effects—MPC509A

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the three (MPC509A) or seven (MPC508A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1kHz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (MPC509A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC509A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC509A and Burr-Brown's INA110 instrumentation amplifier is 110dB at DC to 10Hz (G = 100) with a 6dB/octave roll off to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model INA110 instrumentation amplifier connected for gains of 10, 100, and 500.

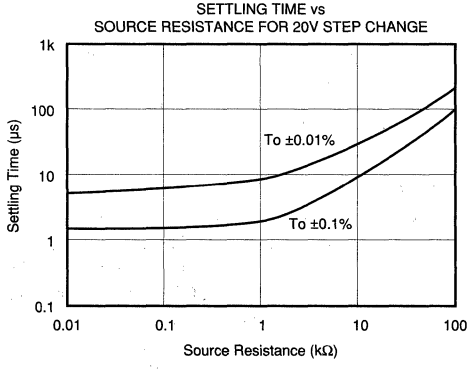
Factors which will degrade multiplexer and system DC CMR are:

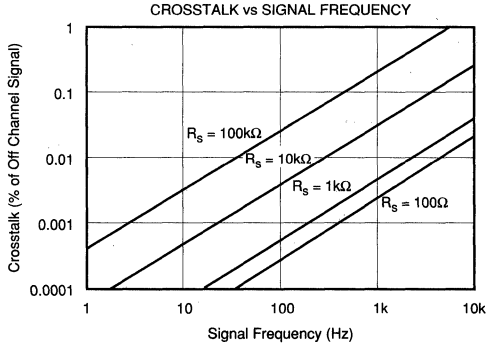
- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

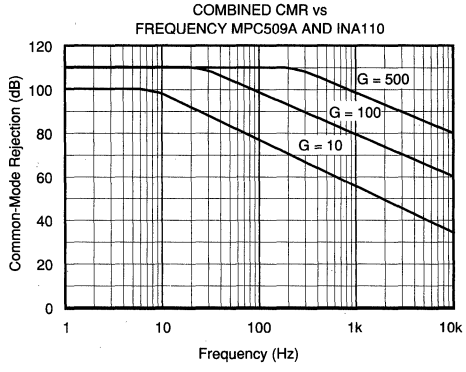
AC CMR roll off is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer-to-amplifier wiring must be minimized. Use twisted-shielded-pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.



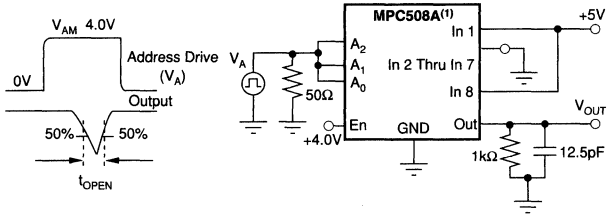


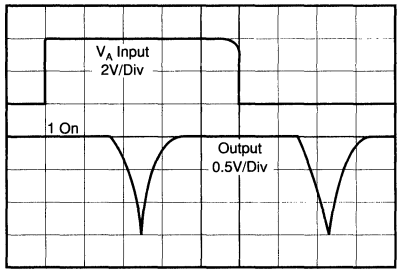


SWITCHING WAVEFORMS

TYPICAL AT +25°C UNLESS OTHERWISE NOTED.

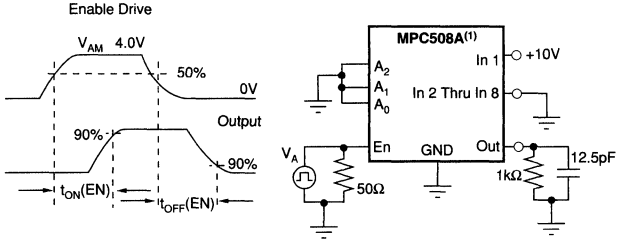
BREAK-BEFORE-MAKE DELAY (t_{OPEN})

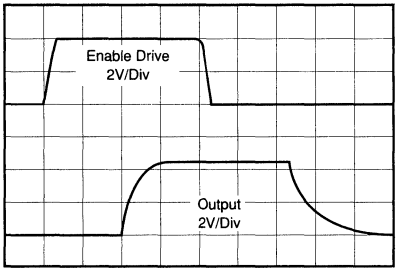




NOTE: (1) Similar connection for MPC509A.

ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))



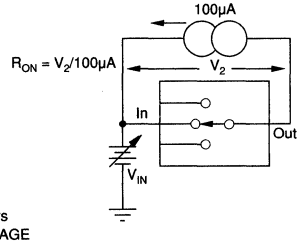


NOTE: (1) Similar connection for MPC509A.

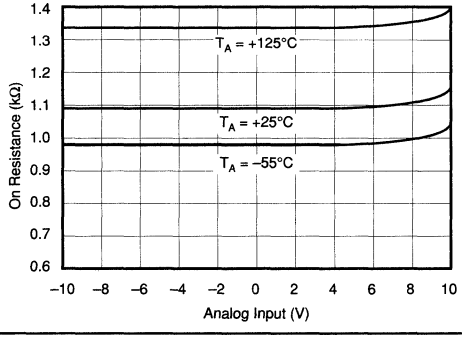
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless otherwise specified: T_A = +25, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V.

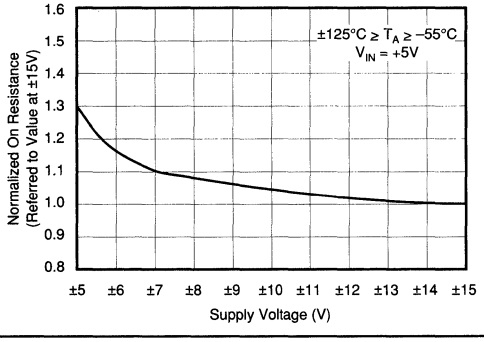
ON RESISTANCE vs ANALOG INPUT SIGNAL, SUPPLY VOLTAGE



ON RESISTANCE vs ANALOG INPUT VOLTAGE

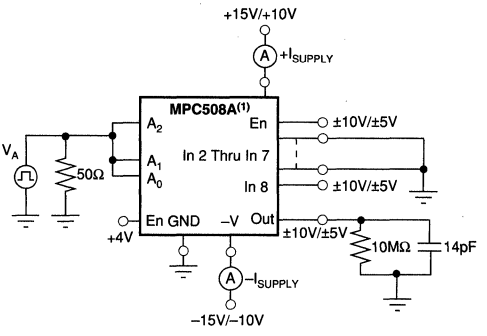


NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

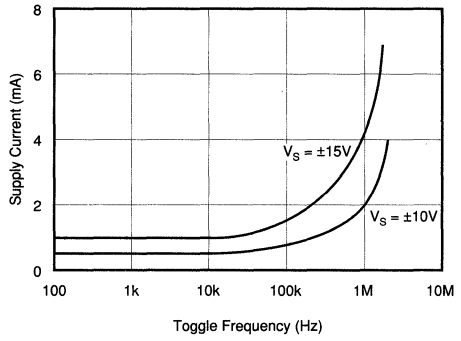


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

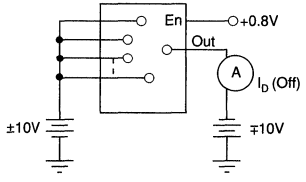
SUPPLY CURRENT vs TOGGLE FREQUENCY

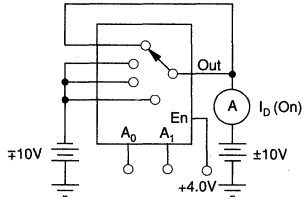


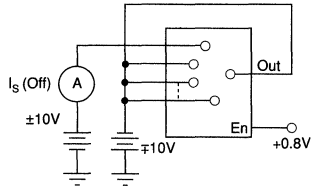
NOTE: (1) Similar connection for MPC509A.

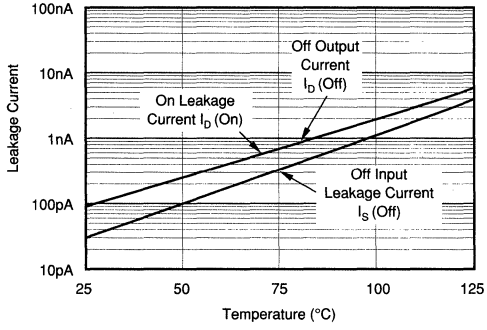


LEAKAGE CURRENT vs TEMPERATURE



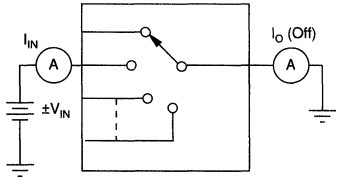


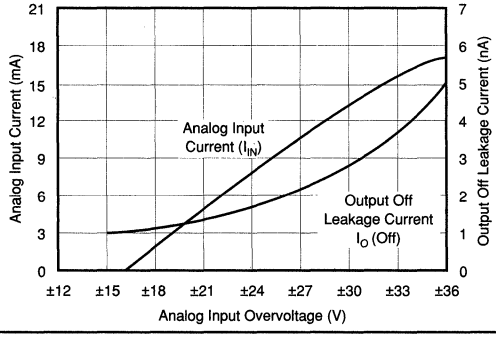




NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V.
(Two measurements per device for I_D (Off): +10V/–10V and –10V/+10V).

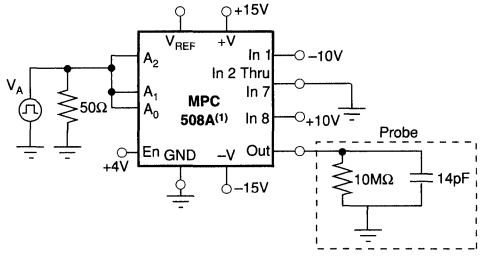
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



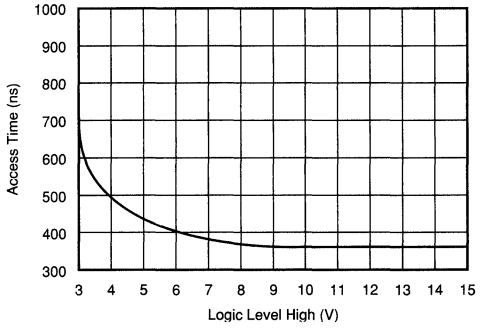


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

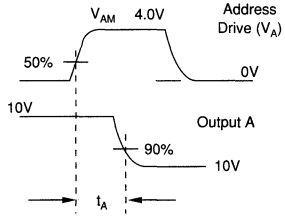
ACCESS TIME vs LOGIC LEVEL (High)

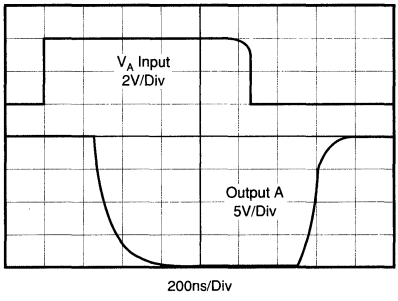


NOTE: (1) Similar connection for MPC509A.

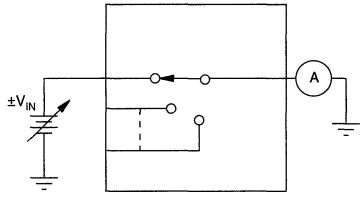


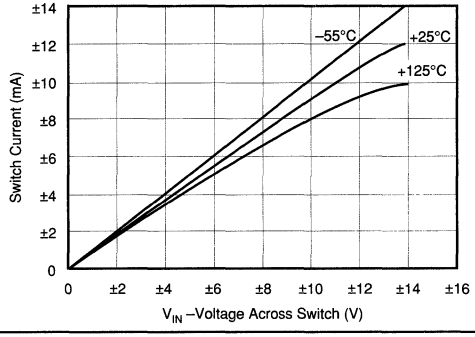
ACCESS TIME WAVEFORM





ON-CHANNEL CURRENT vs VOLTAGE





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 2-bit (MPC509A) or 3-bit (MPC508A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to $+V_{SUPPLY}$.

If the +15V and/or –15V supply voltage is absent or shorted to ground, the MPC509A and MPC508A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended.

To preserve common-mode rejection of the MPC509A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

Single-Ended Multiplexer (MPC508A)

Up to 32 channels (four multiplexers) can be connected to a single node, or up to 64 channels using nine MPC508A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

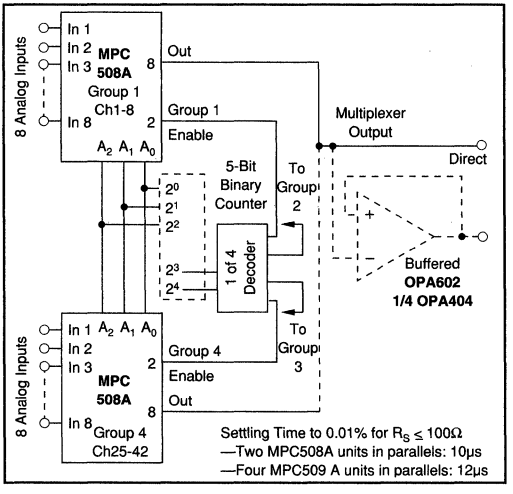


FIGURE 5. 32-Channel, Single-Tier Expansion.

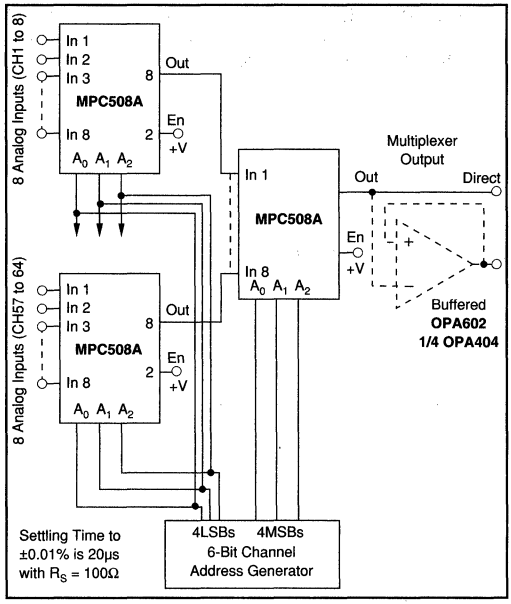


FIGURE 6. Channel Expansion Up to 64 Channels Using 8 x 8 Two-Tiered Expansion.

Differential Multiplexer (MPC509A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

Single-Node Expansion

The 32 x 1 configuration is simply eight (MPC509A) units tied to a single node. Programming is accomplished with a 5-bit counter, using the 2LSBs of the counter to control Channel Address inputs A_0 and A_1 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC509A multiplexers.

Two-Tier Expansion

Using a 4 x 4 two-tier structure for expansion to 16 channels, the programming is simplified. A 4-bit counter output does not require a 1-of-8 decoder. The 2LSBs of the counter drive the A_0 and A_1 inputs of the four first-tier multiplexers and the 2MSBs of the counter are applied to the A_0 and A_1 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

BURR-BROWN®

MPC800

ABRIDGED DATA SHEET

For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10463

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- **HIGH SPEED**
  100ns Access Time
  800ns Settling to 0.01%
  250ns Settling to 0.1%
- **USER-PROGRAMMABLE**
  16-Channel Single-Ended or
  8-Channel Differential
- **SELECTABLE TTL OR CMOS COMPATIBILITY**
- **WILL NOT SHORT SIGNAL SOURCES — Break-Before-Make Switching**
- **SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER**
- **28-PIN HERMETIC DUAL-IN-LINE PACKAGE**

DESCRIPTION

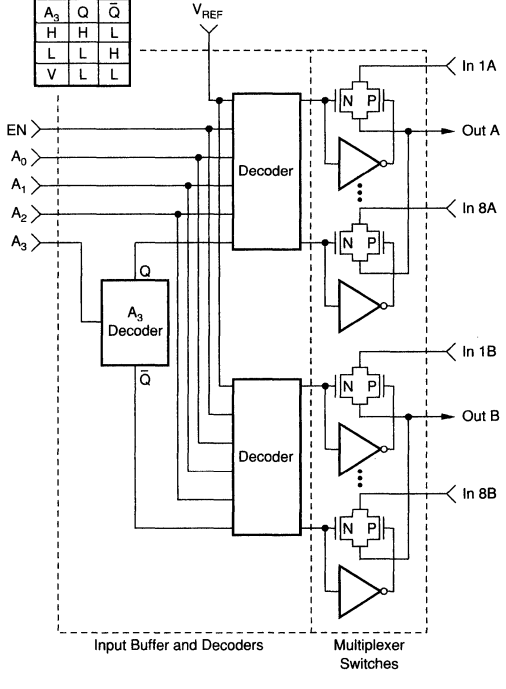
The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C.

A_3 Decoder		
A_3	Q	$\bar{Q}$
H	H	L
L	L	H
V	L	L



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

PARAMETER	MPC800KG MIN	MPC800KG TYP	MPC800KG MAX	UNITS
ANALOG INPUTS				
Voltage Range	–15		+15	V
Maximum Overvoltage	$-V_{CC}$ –2		$+V_{CC}$ +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range[1]	6		10	V
ON Characteristics[2]				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature		See Typical Performance Curves		
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.04		nA
Over Temperature Range		0.6	100	nA
ON Channel Leakage Drift		See Typical Performance Curves		
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.01		nA
Over Temperature Range		0.38	50	nA
OFF Channel Input Leakage Drift		See Typical Performance Curves		
OFF Channel Output Leakage		0.035		nA
Over Temperature Range		0.48	100	nA
OFF Channel Output Leakage Drift		See Typical Performance Curves		
Output Leakage (All channels disabled)[3]		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
–16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL[4]				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	µA
I_{AL}		4	25	µA
TTL Input Overvoltage	–6		6	V
CMOS				
Logic "0" (V_{AL})			$0.3V_{REF}$	V
Logic "1" (V_{AH})	$0.7V_{REF}$			V
CMOS Input Overvoltage	–2		$+V_{CC}$ +2	V
Address A_3 Overvoltage	$-V_{CC}$ –2		$+V_{CC}$ +2	V
Digital Input Capacitance		5		pF
Channel Select[5]				
Single-Ended		4-bit Binary Code One of 16		
Differential		3-bit Binary Code One of 8		
Enable		Logic "0" Inhibits All Channels		
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation[6]			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, –39		mA
At 100kHz Switching Speed		+25, –29		mA

SPECIFICATIONS (CONT)

ELECTRICAL

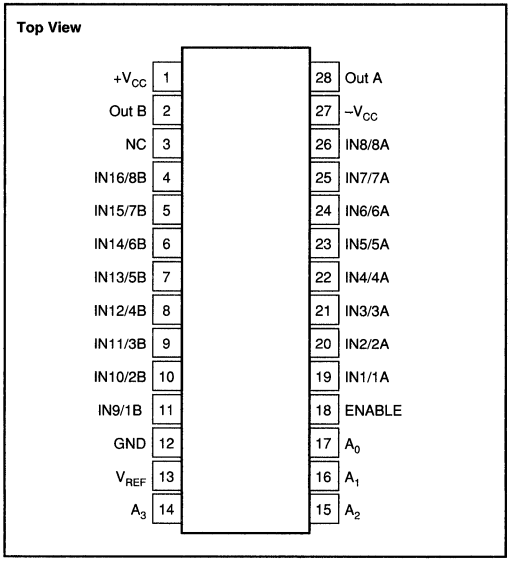
At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

PARAMETER	MPC800KG MIN	MPC800KG TYP	MPC800KG MAX	UNITS
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Crosstalk[7]		See Typical Performance Curves		
T_{OPEN} (Break-before-make delay)		20		ns
Access Time at +25°C		100	150	ns
Over Temperature Range		120	200	ns
Settling Time[8]				
to 0.1% (20mV)		250		ns
to 0.01% (2mV)		800		ns
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S		2.5		pF
OFF Channel Output Capacitance, C_O		18		pF
OFF Input to Output Capacitance, C_{DS}		0.02		pF
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	–65		+150	°C

NOTES: (1) Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility. (2) V_{IN} = ±10V, I_{OUT} = 100µA. (3) Single-ended mode. (4) Logic levels specified for V_{REF} (pin 13) open. (5) For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line. For differential operation connect A_3 to $-V_{CC}$. (6) Derate 8mW/°C above T_A = +75°C. (7) 10Vp-p sine wave on all unused channels. See Typical Performance Curves. (8) For 20V step input to ON channel, into 1kΩ load.

PIN CONFIGURATION

Top View



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPC800KG	Single-Wide Cerdip	–0°C to +75°C

PACKAGE INFORMATION

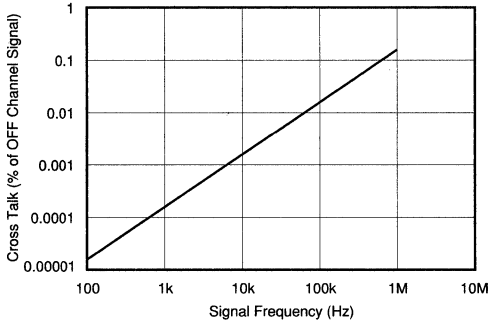
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
MPC800KG	28-Pin Single-Wide Cerdip	228

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

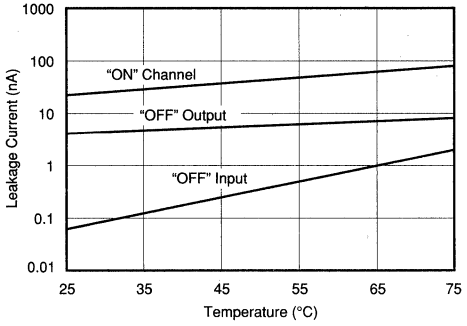
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

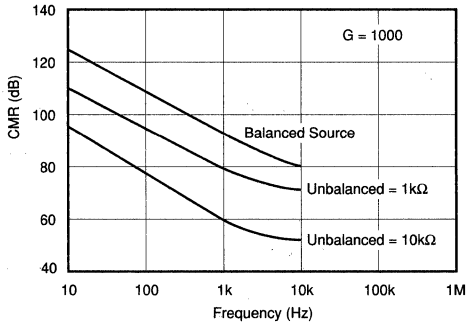
CROSS TALK vs SIGNAL FREQUENCY



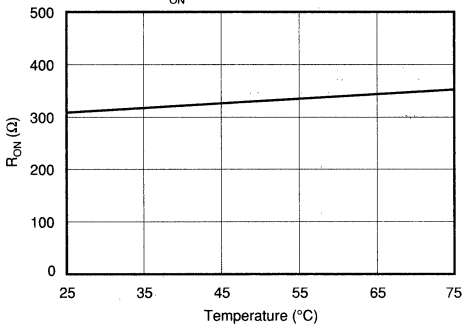
LEAKAGE CURRENTS vs TEMPERATURE



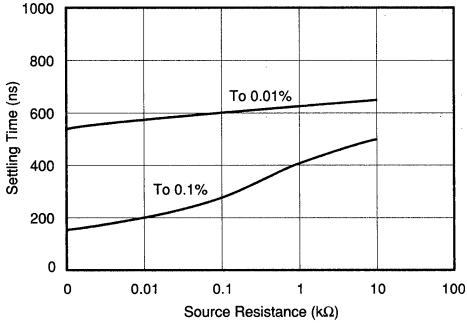
COMBINED CMR vs FREQUENCY
FOR MODEL 3630 AND MPC800



R_{ON} DRIFT vs TEMPERATURE



SETTLING TIME vs SOURCE RESISTANCE
(10V Step Change, R_L = 1kΩ)



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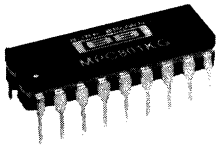


MPC801

ABRIDGED DATA SHEET

For Complete Data Sheet
Call Fax Line 1-800-548-6133
Request Document Number 10464

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- **HIGH SPEED**
  80ns Access Time
  800ns Settling to 0.01%
  250ns Settling to 0.1%
- **USER-PROGRAMMABLE**
  8-Channel Single-Ended or
  4-Channel Differential
- **SELECTABLE TTL OR CMOS COMPATIBILITY**
- **WILL NOT SHORT SIGNAL SOURCES — Break-Before-Make Switching**
- **SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER**
- **18-PIN HERMETIC DUAL-IN-LINE PACKAGE**

DESCRIPTION

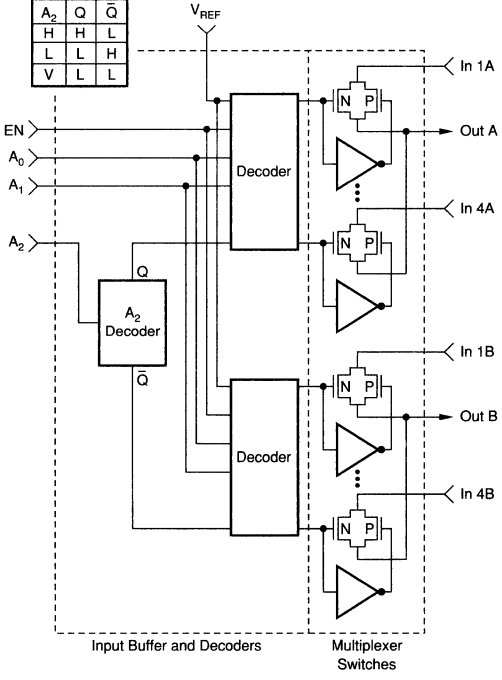
The MPC801 is a high speed multiplexer that is user-programmable for 8-channel single-ended operation or 4-channel differential operation and for TTL or CMOS compatibility.

The MPC801 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC801KG for operation from 0°C to +75°C.

A_2 Decode		
A_2	Q	$\bar{Q}$
H	H	L
L	L	H
V	L	L



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

PARAMETER	MPC801KG MIN	MPC801KG TYP	MPC801KG MAX	UNITS
ANALOG INPUTS				
Voltage Range	–15		+15	V
Maximum Overvoltage	$-V_{CC}$ –2		$+V_{CC}$ +2	V
Number of Input Channels				
Differential	4			
Single-Ended	8			
Reference Voltage Range[1]	6		10	V
ON Characteristics[2]				
ON Resistance (R_{ON}) at +25°C		500	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature		See Typical Performance Curves		
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.1		nA
Over Temperature Range		0.3	50	nA
ON Channel Leakage Drift		See Typical Performance Curves		
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.05		nA
Over Temperature Range		0.6	50	nA
OFF Channel Input Leakage Drift		See Typical Performance Curves		
OFF Channel Output Leakage		0.1		nA
Over Temperature Range		0.30	50	nA
OFF Channel Output Leakage Drift		See Typical Performance Curves		
Output Leakage				
(All channels disabled)[3]		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
–16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL[4]				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	µA
I_{AL}		4	20	µA
TTL Input Overvoltage	–6		6	V
CMOS				
Logic "0" (V_{AL})			$0.3V_{REF}$	V
Logic "1" (V_{AH})	$0.7V_{REF}$			V
CMOS Input Overvoltage	–2		$+V_{CC}$ +2	V
Address A_2 Overvoltage	$-V_{CC}$ –2		$+V_{CC}$ +2	V
Digital Input Capacitance		5		pF
Channel Select[5]				
Single-Ended		3-bit Binary Code One of 8		
Differential		2-bit Binary Code One of 4		
Enable		Logic "0" Inhibits All Channels		
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between				
Supply Pins			33	V
Total Power Dissipation		360		mW
Allowable Total Power Dissipation[6]			725	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+14, –12.5		mA
At 100kHz Switching Speed		+12.5, –12.5		mA

SPECIFICATIONS (CONT)

ELECTRICAL

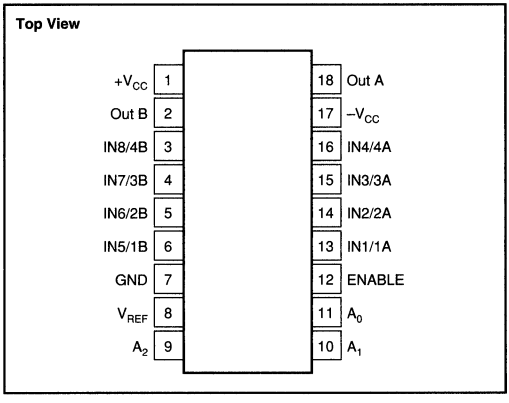
At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

PARAMETER	MPC801KG MIN	MPC801KG TYP	MPC801KG MAX	UNITS
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Crosstalk(7)		See Typical Performance Curves		
T_{OPEN} (Break-before-make delay)		20		ns
Access Time at +25°C		80	125	ns
Over Temperature Range		110	150	ns
Settling Time(8)				
to 0.1% (20mV)		250		ns
to 0.01% (2mV)		800		ns
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S		1.9		pF
OFF Channel Output Capacitance, C_O		10		pF
OFF Input to Output Capacitance, C_{DS}		0.02		pF
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	–65		+150	°C

NOTES: (1) Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility. (2) V_{IN} = ±10V, I_{OUT} = 100µA. (3) Single-ended mode. (4) Logic levels specified for V_{REF} (pin 8) open. (5) For single-ended operation, connect output A (pin 18) to output B (pin 2) and use A_2 (pin 9) as an address line. For differential operation connect A_2 to $-V_{CC}$. (6) Derate 8mW/°C above T_A = +75°C. (7) 10Vp-p sine wave on all unused channels. See Typical Performance Curves. (8) For 20V step input to ON channel, into 1kΩ load.

PIN CONFIGURATION

Top View



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPC801KG	Cerdip	0°C to +75°C

PACKAGE INFORMATION

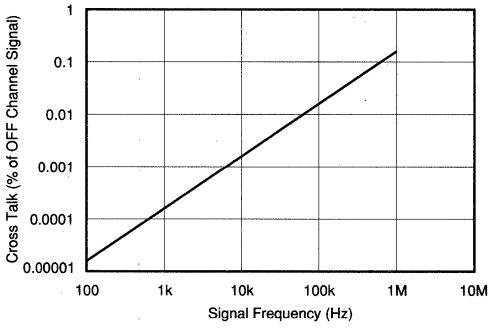
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC801KG	18-Pin Single-Wide Cerdip	266

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

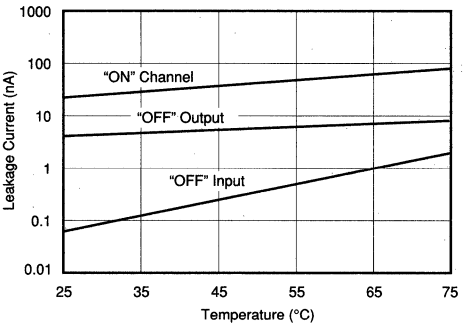
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted.

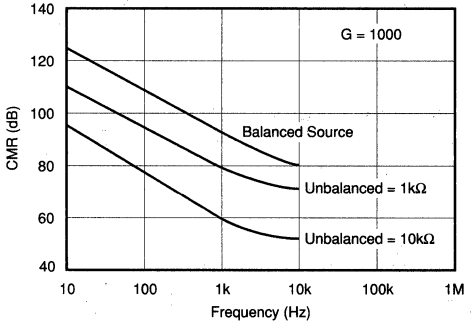
CROSS TALK vs SIGNAL FREQUENCY



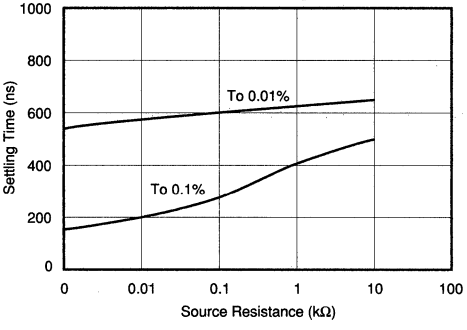
LEAKAGE CURRENTS vs TEMPERATURE



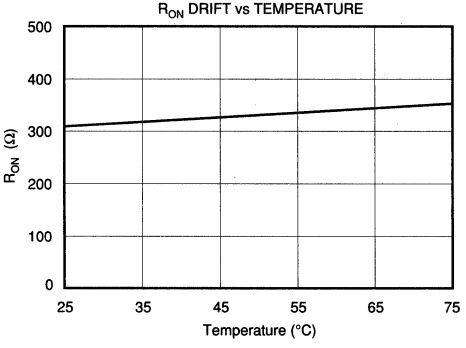
COMBINED CMR vs FREQUENCY
FOR MODEL 3630 AND MPC800



SETTLING TIME vs SOURCE RESISTANCE
(20V Step Change, R_L = 1kΩ)



R_{ON} DRIFT vs TEMPERATURE



6 Sample/Hold Amplifiers

Sample/hold amplifiers are a key part of an A/D conversion solution. While many new A/D converters have a self-contained sample/hold on the A/D chip, sample/hold amplifiers play a role in specialized applications such as multiple channel simultaneous sampling, and ultra-high speed sampling and multichannel output applications.

Use of a sample/hold increases the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal to be converter is captured at a specific instant in time.

SAMPLE/HOLD AMPLIFIERS
(Acquisition Time, max)

12-BIT
SHC605 (0.35µs)
SHC804 (0.35µs)
SHC803 (0.35µs)
SHC5320 (1.5µs)
SHC298 (10µs)

14-BIT
SHC76 (6µs)

WIDE-BAND
SHC615 (15ns)
SHC804 (0.35µs)
SHC605 (0.03µs)

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Product	Gain Error (%)	Offset Error (mV)	Charge Offset (mV)	Small Signal Bandwidth (MHz) (typ)	Acq Time to 0.01% (µs max)	Droop Rate (µV/µs)	Temp Range[1]	Input Range (Vp-p)	Pkg[2]	Description
SHC76	±0.02	±3	±6 typ	1.5	3	±1	Ind, Com, Mil	20	HMD	Fast, High Accuracy
SHC298	±0.01	±7	±25 max	0.125	10	±100,000	Com, Ind	23	PDIP, MC, SOIC	Lowest Cost Industry Std
SHC605	±0.1	±5	±20	200	0.02*	±8000	Ext	4.0	16-p SOIC	Low Cost
SHC615	0.1[3]	8 (typ)	—	750	15ns[3]	±33,000[3]	Xlind	2	PDIP, SOIC	Wideband DC Restoration Cir
SHC803	±0.1	±3	±10	16	0.35	±5	Ind	20	HMD	High Speed with Buffer
SHC804	±0.1	±3	±5	16	0.35	±5	Ind	20	HMD	High Speed
SHC5320	NA	±0.5	±1 typ	2	1.5	±0.5	Com, Mil	20	HCD, PDIP, SOIC	Low Cost, Fast Industry Std

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C, Ext = –40°C to +85°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) With 27pF external hold capacitor.

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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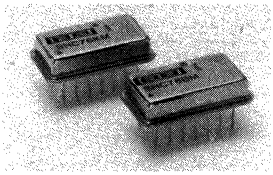


SHC76

SAMPLE/HOLD AMPLIFIER

FEATURES

- **FAST (6µs max) ACQUISITION TIME (14-bit)**
- **APERTURE JITTER: 400ps**
- **POWER DISSIPATION: 300mW**
- **COMPATIBLE WITH HIGH RESOLUTION A/D CONVERTERS ADC76, PCM75, AND ADC71**

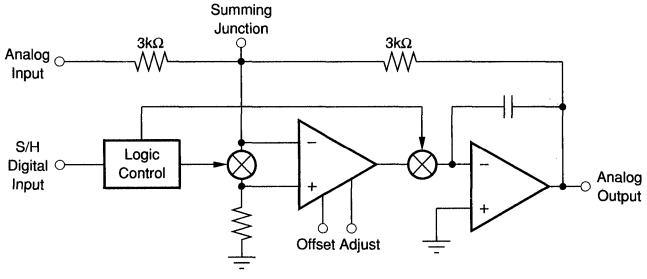
DESCRIPTION

The SHC76 is a fast, high-accuracy hybrid sample/hold circuit suitable for use in high-resolution data acquisition systems.

The SHC76 is complete with internal hold capacitor and incorporates an internal compensation network which minimizes sample-to-hold charge offset. The SHC76 is configured as a unity-gain inverter.

High-resolution converters such as the ADC76 and ADC71 are compatible with SHC76 in forming complete, 14-bit accurate analog-to-digital conversion systems.

The SHC76 comes in a 14-pin single-wide hermetic metal DIP. Power supply requirements are specified from ±14.5V to ±15.5V with guaranteed operation from ±11.4V to ±18V. Input voltage range is ±10V. The SHC76 is available in two temperature ranges: KM, for 0°C to +70°C; and BM, for –25°C to +85°C operation.



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SPECIFICATIONS

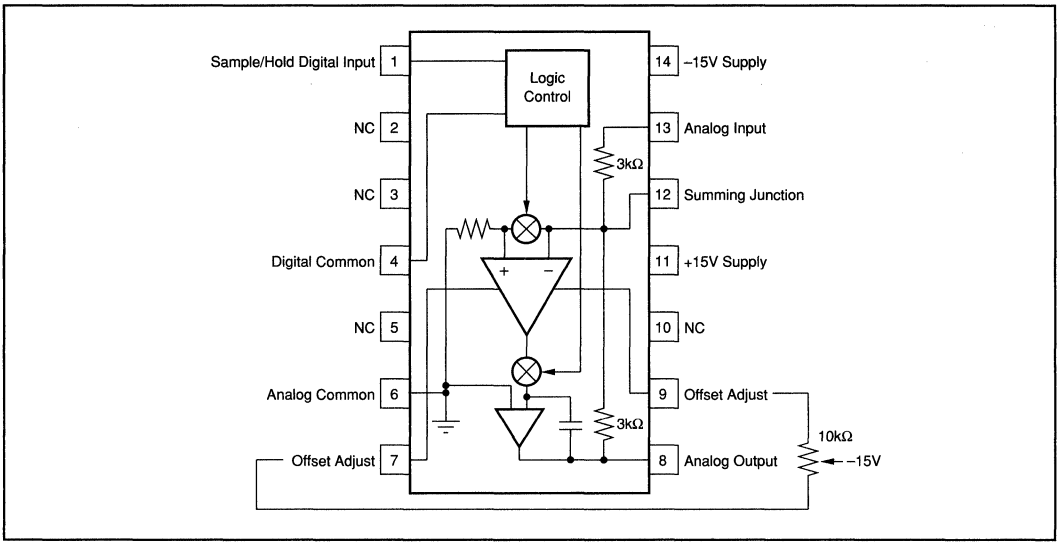
ELECTRICAL

Typical at +25°C, and nominal power supply voltage of ±15V, unless otherwise noted.

PARAMETER	SHC76KM, BM MIN	SHC76KM, BM TYP	SHC76KM, BM MAX	UNITS
ANALOG INPUTS				
Voltage Range	±10			V
Overvoltage, no damage			±15	V
Impedance		3000		Ω
DIGITAL INPUT				
(TTL-Compatible)				
Track Mode, Logic "1"	2		5.5	V
Hold Mode, Logic "0"	0		0.8	V
I_{IH}, V_{IH} = 2.4V			400	µA
I_{IL}, V_{IL} = 0.4V			1000	µA
ANALOG OUTPUT				
Voltage		±10		V
Current		5		mA
Short-Circuit Current		20		mA
Impedance		1		Ω
DC ACCURACY/STABILITY				
Gain		–1.00		V/V
Gain Error		±0.01	±0.02	%
Gain Nonlinearity				
(±10V Output Track)		±0.001		%
Gain Temperature Coefficient		1	5	ppm/°C
Offset Voltage(1)			±3	mV
Output Offset at T_{MIN}, T_{MAX} (Track)		±6		mV
TRACK MODE DYNAMICS				
Freqency Response				
Small Signal (–3dB)		1.5		MHz
Full Power Bandwidth		0.5		MHz
Slew Rate		30		V/µs
Noise in Track Mode				
(DC to 1.0MHz)		200		µVrms
TRACK-TO-HOLD SWITCHING				
Aperture Time		30		ns
Aperture Uncertainty (Jitter)		0.4		ns
Offset Step (Pedestal)		±2	±4	mV
Pedestal at Temperature				
KM Grade		±4		mV
BM Grade		±6		mV
Switching Transient				
Amplitude		200		mV
Settling to 1mV		0.5	2	µs
Settling to 0.3mV		1	3	µs
HOLD MODE DYNAMICS				
Droop Rate		0.1	1	µV/µs
Droop Rate at T_{MAX}			100	µV/µs
Feedthrough Rejection				
(10Vp-p, 20kHz)	74	86		dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
To ±0.01% of 20V		1.5	3	µs
To ±0.003% of 20V		4	6	µs
POWER REQUIREMENTS				
Nominal Voltages for Rated				
Performance	±14.5	±15	±15.5	V
Operating Range(2)	±11.4		±18	V
Power Supply Rejection		100		µV/V
Supply Current: $+V_S$		15	20	mA
$–V_S$		–4	–10	mA
Power Dissipation		300	500	mW
TEMPERATURE RANGE				
Operating: KM Grade	0		+70	°C
BM Grade	–25		+85	°C
Storage	–55		+125	°C

NOTES: (1) Adjustable to zero with external circuit. (2) Operating to derated performance with $V_{IN} < V_S$ –5V.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals	40V
Input Voltage	Actual Supply Voltage
Differential Input Voltage	±24V
Digital Input Voltage	–0.5V to +5.5V
Output Current Continuous[2]	±20mA
Internal Power Dissipation	500mW
Storage Temperature Range	$-65°C < T_A < +150°C$
Output Short-Circuit Duration[3]	Momentary to Common
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC76KM	14-Pin Single-Wide, Hermetic Metal DIP	107
SHC76BM	14-Pin Single-Wide, Hermetic Metal DIP	107

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
SHC76KM	14-Pin Single-Wide, Hermetic Metal DIP	0°C to +70°C
SHC76BM	14-Pin Single-Wide, Hermetic Metal DIP	–25°C to +85°C

PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Digital Input	8	Analog Output
2	No Connection	9	Offset Adjust
3	No Connection	10	No Connection
4	Digital Ground	11	+15V Supply
5	No Connection	12	Summing Junction
6	Analog Ground	13	Analog Input
7	Offset Adjust	14	–15V Supply

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

This is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

GAIN ERROR

The difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

DROOP RATE

The voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

FEEDTHROUGH

The amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

APERTURE DELAY TIME

The time required to switch from Sample-to-Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

APERTURE UNCERTAINTY TIME

The nonrepeatibility of aperture delay time.

ACQUISITION TIME

The time required for the sample/hold output to settle within a given error band of its final value when the sample/hold is switched from Hold-to-Sample.

CHARGE OFFSET (PEDESTAL)

The output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

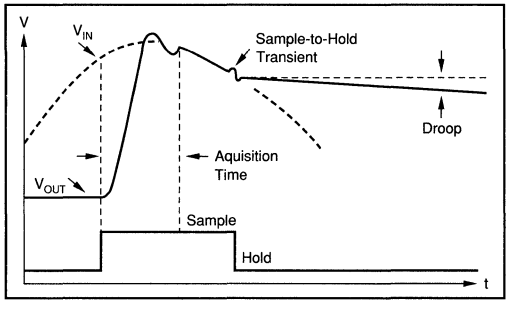


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

SAMPLE-TO-HOLD SWITCHING TRANSIENT

The switching transient which appears on the output when the sample/hold is switched from Sample-to-Hold. Both the magnitude and the settling time of the transient are specified.

SAMPLED DATA ACQUISITION SYSTEM CALCULATIONS

The rated accuracy of an A/D converter in combination with the aperture uncertainty of a sample/hold determine the maximum theoretical input slew rate (frequency) of a given sampled data system.

Sine Wave $f_{MAX} = (2^{-N} \text{ FSR}) \div (2\pi \text{ A t})$
A = max Input Signal Amplitude (peak-to-peak)
FSR = Full-Scale Range of A/D Converter
t = Aperture Uncertainty of S/H (jitter)
N = Number of Bits Accuracy

Given below are the maximum input frequencies of two A/D converters in conjunction with the SHC76:

SHC76 13-bit Sine Wave f_{MAX} =
$(0.000122 \cdot 20V) \div (2 \cdot \pi \cdot 20V \cdot 0.4ns) = 48.6kHz$

SHC76 14-bit Sine Wave f_{MAX} =
$(0.000061 \cdot 20V) \div (2 \cdot \pi \cdot 20V \cdot 0.4ns) = 24.3kHz$

The maximum throughput rate is determined by adding all critical conversion process times together. Throughput rate cannot exceed the maximum input frequency determined by the accuracy and jitter specs without degrading system performance. Two samples per period of a sine wave are required to satisfy the Nyquist sampling theorem. A low-pass filter is required to cut off frequencies higher than the maximum throughput frequency to prevent aliasing errors from occurring.

Throughput f_{MAX} (2 samples) =
1 ÷ [2 (S/H acquisition time + S/H settling time
+ A/D conversion time)]

Table I is a listing of various A/D throughput rates using the SHC76 S/H amplifier (assuming two samples per period).

CONVERTER	ACCURACY (Bits)	CONVERSION SPEED (µs)	RESOLUTION (Bits)	THROUGHPUT F_{MAX} (kHz)
ADC76KG	14	17	16	19.2
	14	16	15	20.0
	14	15	14	20.8
ADC76JG	13	17	16	23.8
	13	16	15	25.0
	13	15	14	26.3
ADC71KG	14	57	16	7.58
	14	54	15	7.94
	14	50	14	8.47
ADC71JG	13	57	16	8.20
	13	54	15	8.62
	13	50	14	9.26

TABLE I. A/D Converter Throughput Rates.

APPLICATIONS

Figures 2 and 3 show the SHC76 in combination with an ADC76 and ADC71 to provide 14-bit accurate A/D conversion systems.

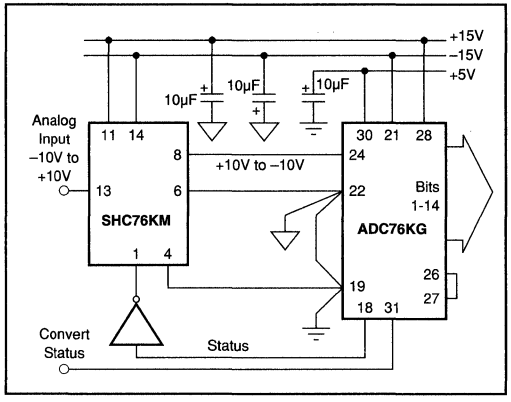


FIGURE 2. A 20kHz A/D Conversion System (14-bit accurate).

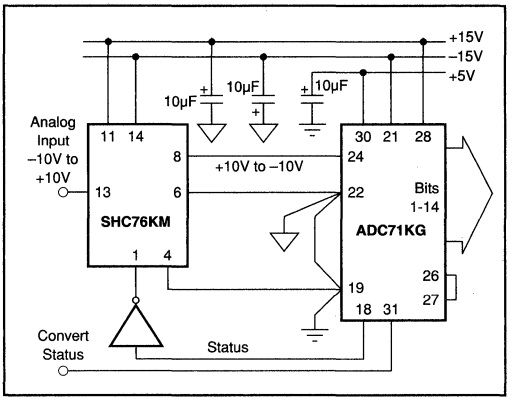
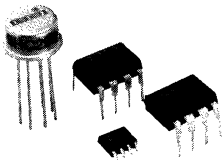


FIGURE 3. A 8.47kHz A/D Conversion System (14-bit accurate).

BURR-BROWN®

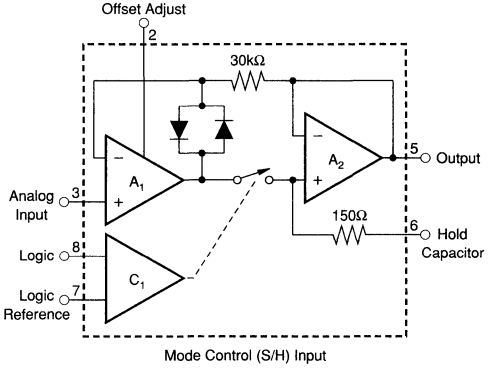


SHC298
SHC298A

Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10µs ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20µVrms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL-CMOS-COMPATIBLE LOGIC INPUT



DESCRIPTION

The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6µs acquisition time. Droop rates less than 5mV/min are possible with a 1µF holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from ±5V to ±18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample on the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from –25°C to +85°C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0°C to +70°C.

The SHC298AJP, specified over 0°C to +70°C, is available in an 8-pin plastic DIP. The SHC298A grade features improved gain and offset error, improved drift over temperature, and faster acquisition time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, –11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

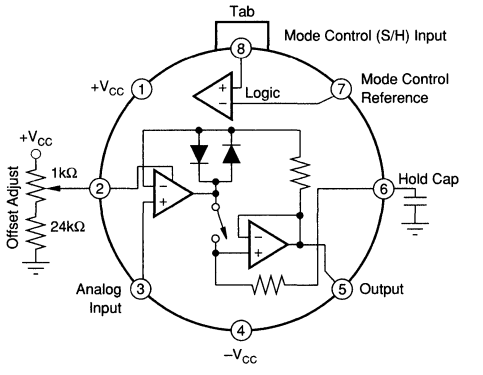
PARAMETER	SHC298AM, JP, JU			SHC298AJP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT							
Resistance		10^{10}			*		Ω
Bias Current[1]		10	50		*	25	nA
DIGITAL INPUT	Pin 7		Pin 8		Circuit State		
Mode Control Truth Table	0V		+2.4V		Sample (Track)		
	0V		+0.8V		Hold		
	+2.4V		+2.8V		Hold		
	+0.8V		+2.8V		Sample (Track)		
Mode Control and Mode Control Reference Input Current			10				µA
Differential Logic Threshold	0.8	1.4	2.4				V
TRANSFER CHARACTERISTICS							
ACCURACY (+25°C)							
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015		*	*	% of 20V
Gain		+1			*		V/V
Gain Error		±0.004	±0.010		±0.001	±0.005	%
Input Voltage Offset (adjust to zero)[1]		±2	±7		±1	±2	mV
Droop Rate[1]		±30	±200		*	±100	µV/ms
Charge Offset[2]		±15	±25		*	*	mV
Noise (rms) 10Hz to 100kHz		10	20		*	*	µV
Power Supply Rejection		±25	±100		*	*	µV/V
ACCURACY DRIFT							
Gain Drift		3	4		1	2	ppm/°C
Input Offset Drift		15	70		*	25	µV/°C
Charge Offset Drift, C = 1000pF		50	150		*	*	µV/°C
Charge Offset Drift, C = 10,000pF		20	50		*	*	µV/°C
Droop Rate at T_J = +85°C		1	10		*	*	mV/ms
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth, C = 1000pF	75	125		*	*		kHz
Full Power Bandwidth, C = 10,000pF	10	16		*	*		kHz
Output Slew Rate, C = 1000pF	7	10		*	*		V/µs
Output Slew Rate, C = 10,000pF	1.4	2		*	*		V/µs
Aperture Time : Negative Input Step		200	250		*	*	ns
Positive Input Step		150	200		*	*	ns
Acquisition Time (C = 1000pF): to ±0.01%, 10V Step		6	10		*	*	µs
to ±0.01%, 20V Step		8	12		*	*	µs
to ±0.1%, 10V Step		5	9		4	6	µs
to ±0.1%, 20V Step		7	11		*	*	µs
Sample/Hold Transient: Peak Amplitude		160			*		mV
Settling to 1mV		1	1.5		*	*	µs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015		±0.004	±0.0075	% of 20V
OUTPUT							
ANALOG OUTPUT							
Voltage Range	±11.5			*			V
Current Range	±2			*			mA
Impedance (in Hold Mode)	0.5	4		*	*	Ω	
POWER SUPPLY							
Rate Voltage		15			*		VDC
Range	±5		±18	*		*	VDC
Current[1]		±4.5	±6.5		*	*	mA

* Same as specifications for SHC298AM, JP, JU.

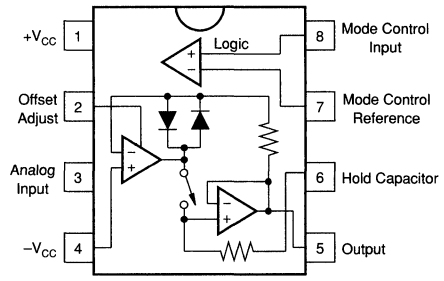
NOTES: (1) These parameters guaranteed over a supply voltage range of ±5V to = ±18V. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

PIN CONFIGURATIONS

Top View **TO-99**



Top View **Plastic DIP/Small Outline**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Package Limitation)	500mV
Junction Temperature, $T_{J\ MAX}$	
AM	125°C
JP, JU	100°C
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range	–65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage[1]	+7V, –30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10s
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

PACKAGE/ORDERING INFORMATION

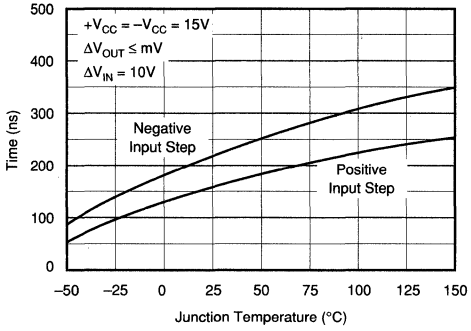
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE
SHC298AM	TO-99	001	–25°C to +85°C
SHC298JP	8-Pin Plastic DIP	006	0°C to +70°C
SHC298JU	8-Lead SOIC	182	0°C to +70°C
SHC298AJP	8-Pin Plastic DIP	006	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

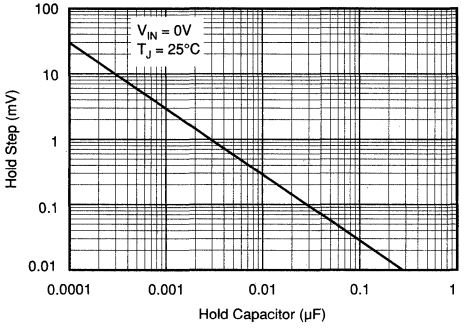
TYPICAL PERFORMANCE CURVES

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

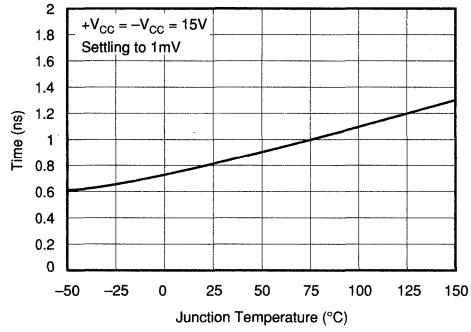
APERTURE TIME



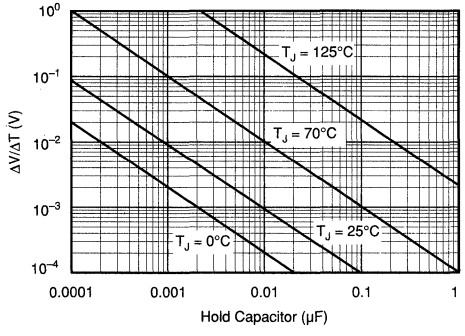
CHARGE OFFSET



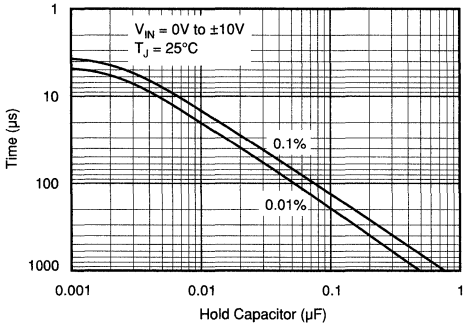
SAMPLE-TO-HOLD TRANSIENT SETTLING TIME



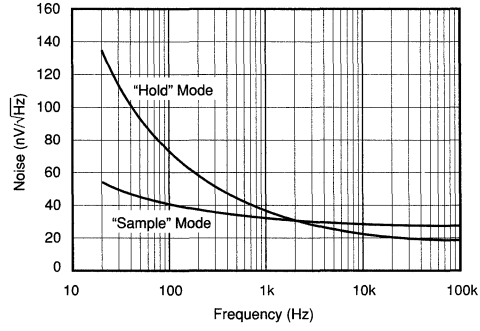
OUTPUT DROOP RATE



ACQUISITION TIME



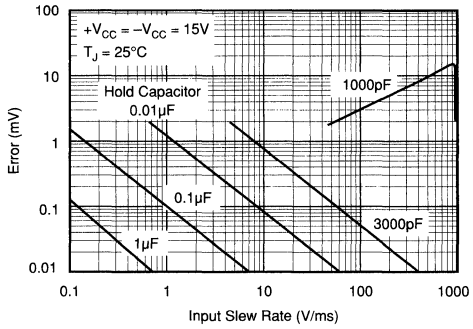
OUTPUT NOISE



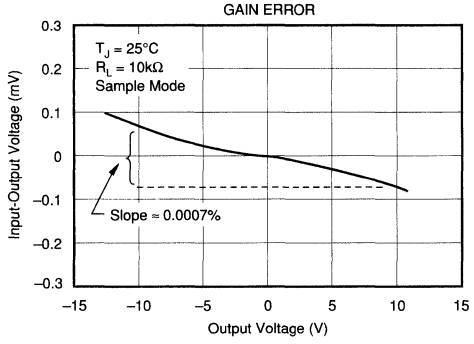
TYPICAL PERFORMANCE CURVES (CONT)

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

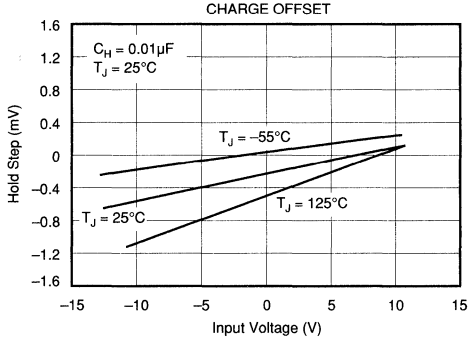
DYNAMIC SAMPLING ERROR



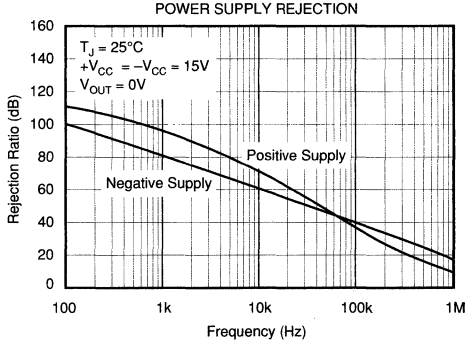
GAIN ERROR



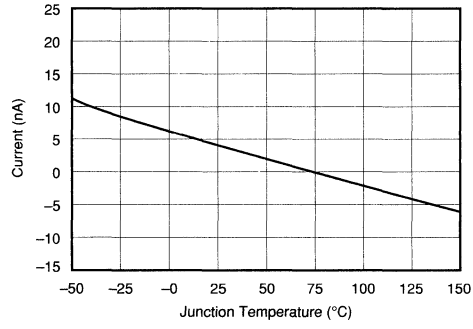
CHARGE OFFSET



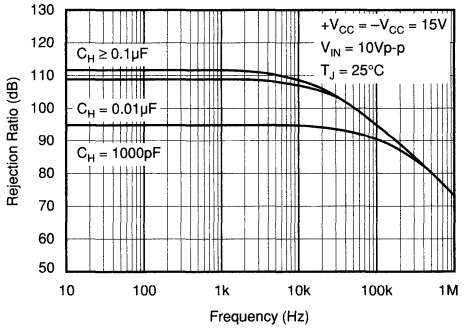
POWER SUPPLY REJECTION



INPUT BIAS CURRENT

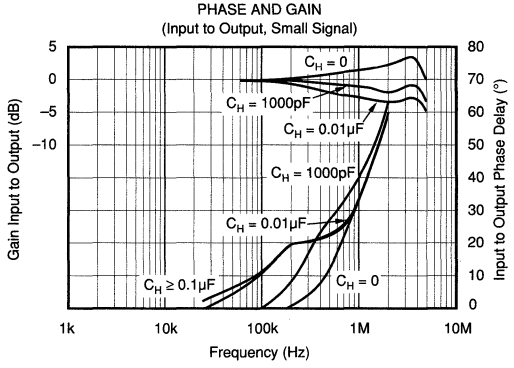


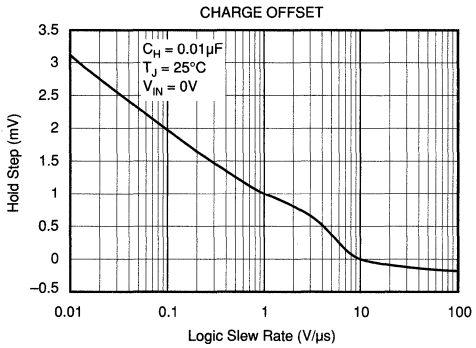
FEEDTHROUGH REJECTION RATIO



TYPICAL PERFORMANCE CURVES (CONT)

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1ms of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10µs acquisition time, and 1ms Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between input and output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

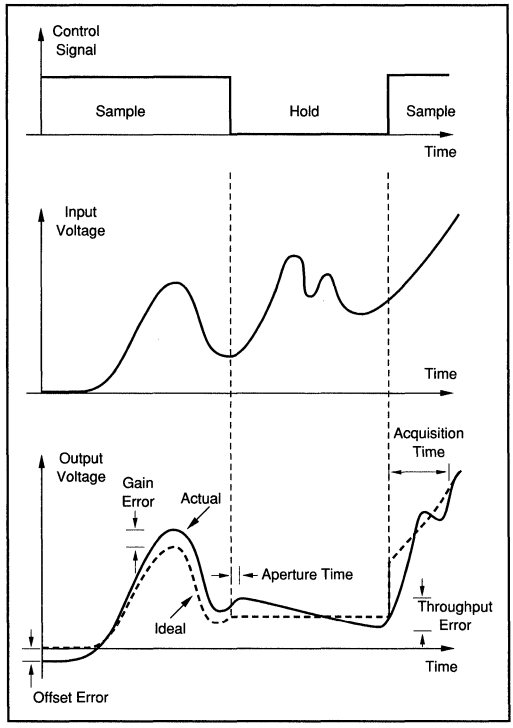


FIGURE 1. Sample/Hold Errors.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as Teflon®, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001µF capacitor. With a capacitor of 0.01µF, the droop will reduce to approximately 2.5µV/ms and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in the Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001µF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298 may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

DATA DISTRIBUTION

The SHC298 may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

TEST SYSTEMS

The SHC298 is also well suited for use in test systems to acquire and hold data transients for human operators or for the other parts of the test system such as comparators, digital voltmeters, etc.

With a 0.1µF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1µF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high-speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5). For low-level systems, and instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

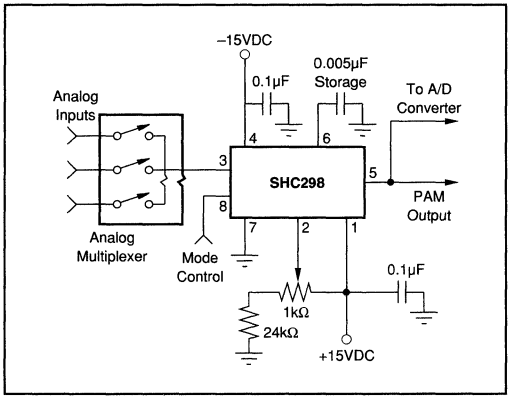


FIGURE 2. Data Acquisition.

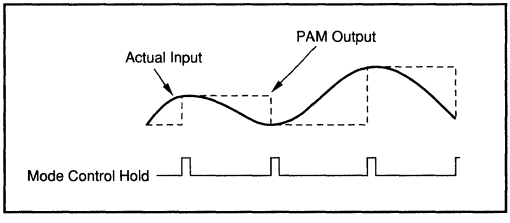


FIGURE 3. PAM Output.

®Teflon, DuPont de Nemours

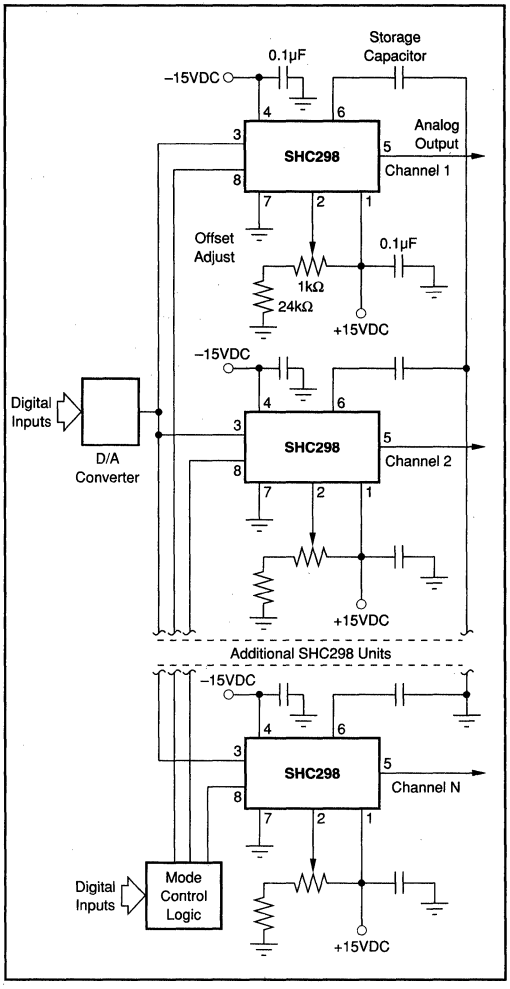


FIGURE 4. Data Distribution.

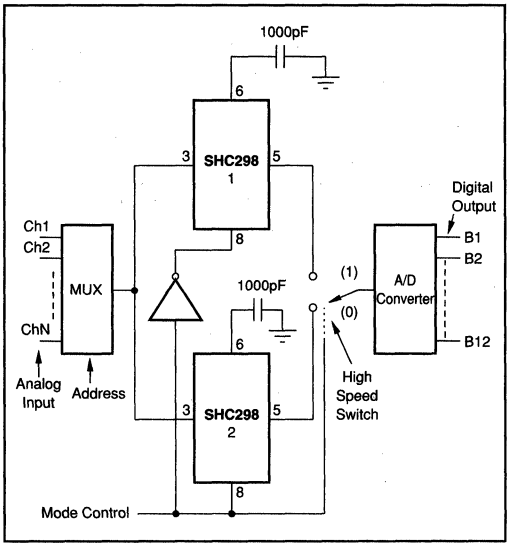


FIGURE 5. "Ping-Pong" Sample Holds.

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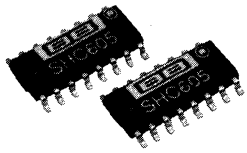


SHC605

DEMO BOARD AVAILABLE
See Appendix A

High-Speed Operational TRACK-AND-HOLD AMPLIFIER

FEATURES

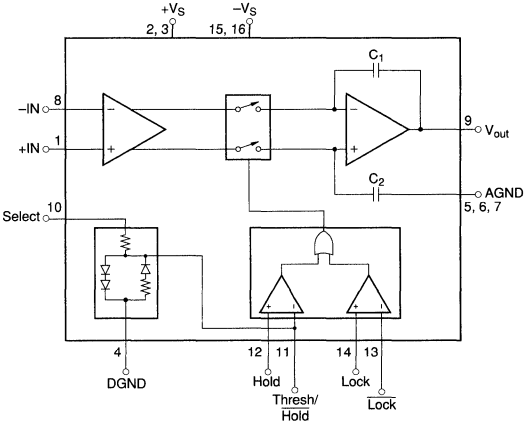
- **VERY GOOD SPURIOUS FREE DYNAMIC RANGE:**
  90dB at 1MHz F_{IN} and 20MSPS
  86dB at 2MHz F_{IN} and 20MSPS
  77dB at 5MHz F_{IN} and 20MSPS
- **LOW ACQUISITION TIME: 30ns to 0.01%**
- **LOW DROOP RATE: 8mV/µs max T_{MIN} to T_{MAX}**
- **LOW POWER CONSUMPTION: 335mW**
- **EXTREMELY VERSATILE ARCHITECTURE: Noninverting, Inverting, and Differential Gains**
- **LOGIC FLEXIBILITY: TTL and ECL Compatible**
- **SMALL PACKAGE: 16-Lead SOIC**
- **EXTENDED TEMPERATURE SPECS: –40°C to +85°C**

APPLICATIONS

- **A/D CONVERTER FRONT ENDS**
- **MULTIPLE CHANNEL SIMULTANEOUS SAMPLING**
- **IMPROVING FLASH ADC PERFORMANCE**
- **PEAK DETECTORS**
- **DAC DEGLITCHING**

DESCRIPTION

The SHC605 is a monolithic high-speed, high accuracy track-and-hold amplifier. It combines fast acquisition and low distortion to provide a complete solution for a wide range of sampling applications. Its new proprietary closed-loop architecture provides a single-chip solution to many data acquisition problems formerly requiring more than one device. Noninverting, inverting, and differential gain configurations are easy to apply with the SHC605. An on-board logic reference circuit makes the SHC605 compatible with both single-ended and differential ECL or TTL clock inputs. An internal track-mode lockout circuit allows edge-triggered operation in data acquisition systems. The SHC605 is available in a 16-lead SOIC package specified for the –40C to +85C industrial temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

PARAMETER	CONDITION	TEMP RANGE	SHC605AU MIN	SHC605AU TYP	SHC605AU MAX	UNITS
DC INPUT PARAMETERS						
Offset Voltage		Full		±1	±7.5	mV
Power Supply Rejection	V_S = ±4.5 to ±5.5V	+25°C	60	85		dB
Input Bias Current	V_{CM} = 0V	Full		15	50	µA
Input Offset Current	V_{CM} = 0V	Full		±0.2	±5	µA
Common-Mode Input Range		Full	±2.0	±2.5		V
Common-Mode Rejection	V_{CM} = ±2VDC	Full		80		dB
Differential Input Impedance		Full		13||1		kΩ||pF
Common-Mode Input Impedance		Full		2||1		MΩ||pF
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	+25°C		100		dB
OUTPUT						
Voltage Output	R_L = 50Ω	Full	±2.0	±2.5		V
Current Output		+25°C	±40	±80		mA
		Full	±40	±60		mA
Short Circuit Current		Full		±140		mA
Output Resistance,						
Closed-Loop: Track-Mode	DC	Full		0.0001		Ω
Hold-Mode	DC	Full		0.01		Ω
DIGITAL INPUTS/OUTPUTS						
TTL Input Levels [1]	Hold Input Only					
V_{IL}	Logic "LO"	Full	0		+1.0	V
V_{IH}	Logic "HI"	Full	+2.0		+5.0	V
Single-Ended ECL Input Levels [2]	Hold/$\overline{\text{Hold}}$ and Lock/$\overline{\text{Lock}}$ Inputs					
V_{IL}	Logic "LO"	Full	–1.80		–1.45	V
V_{IH}	Logic "HI"	Full	–1.05		–0.80	V
Common-Mode Input Voltages	Hold/$\overline{\text{Hold}}$	Full	–3		+5	V
	Lock/$\overline{\text{Lock}}$	Full	$-V_S$		+3	V
Differential Input Voltages	Hold/$\overline{\text{Hold}}$ and Lock/$\overline{\text{Lock}}$ Inputs	Full	0.2		5.0	V
Digital Input Currents						
I_{IL}, Lock/$\overline{\text{Lock}}$ Inputs Only	ECL Logic "LO", V_{IL} = –1.60V	Full			5	µA
I_{IL}, Hold/$\overline{\text{Hold}}$ Inputs Only	ECL or TTL Logic "LO"	Full			–100	µA
I_{IH}, Lock/$\overline{\text{Lock}}$ Inputs Only	Logic "HI", V_{IH} = –1.0V	Full			50	µA
I_{IH}, Hold/$\overline{\text{Hold}}$ Inputs Only		Full			–10	µA
Threshold Voltage Output[3]						
TTL[4]		Full	1.1	1.5	1.9	V
ECL[5]	$-V_S$ = –5.2V	Full	–1.40		–1.10	V
TRACK-MODE RESPONSE						
Closed-Loop Bandwidth	Gain = +1V/V	+25°C	100	200		MHz
	Gain = +2V/V	+25°C		75		MHz
	Gain = +5V/V	+25°C		20		MHz
	Gain = +10V/V	+25°C		10		MHz
Full Power Response	±1V Input, –3dB Output	Full		32		MHz
Slew Rate [6]	G = +1, 2V Step	+25°C	140	200		V/µs
		Full	120	200		V/µs
Acquisition Time to 1%[7]	2V Step	Full		15	25	ns
0.1%	2V Step	Full		23	35	ns
0.012%	2V Step	Full		30	45	ns
0.012%	4V Step	Full		40	60	ns
Input Voltage Noise	1MHz to 100MHz			2.5		nV/√Hz
Input Bias Current Noise	1MHz to 100MHz			2.5		pA/√Hz
Differential Gain	3.58MHz, V_O = 0 to 0.7Vp–p			0.005		%
Differential Phase	3.58MHz, V_O = 0 to 0.7Vp–p			0.005		degrees
Spurious Free Dynamic Range						
(5MHz)	V_O = ±1V			83		dBc
(10MHz)	V_O = ±1V			73		dBc

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is 10µVrms. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

PARAMETER	CONDITION	TEMP RANGE	SHC605AU MIN	SHC605AU TYP	SHC605AU MAX	UNITS
TRACK-TO-HOLD SWITCHING	V_{IN} = 0V					
Aperture Delay		Full		1.7		ns
Aperture Jitter		Full		2.4		ps rms
Pedestal Offset		+25°C		±5	±20	mV
over Temperature		Full		±5	±25	mV
Transient Amplitude		Full		±5		mV
Settling Time to 1mV		Full		8	15	ns
100µV		Full		15		ns
HOLD-MODE RESPONSE						
Spurious Free Dynamic Range						
(1MHz, 20MSPS)	V_O = ±1V	Full	78	90		dBc
(2MHz, 20MSPS)	V_O = ±1V	Full	74	86		dBc
(5MHz, 20MSPS)	V_O = ±1V	Full	65	77		dBc
(10MHz, 20MSPS)	V_O = ±1V	+25°C		60		dBc
(10MHz, 20MSPS)	V_O = ±0.5	+25°C		72		dBc
Hold Noise[8]				400xt_H		V/s rms
Droop Rate		Full		±1	±8	mV/µs
Hold Time[9]		Full			2	µs
Feedthrough Rejection (20MHz)		+25°C		85		dB
POWER SUPPLY						
Specified Operating Voltage		Full	±4.50	±5	±5.50	V
Positive Supply Current[10]		Full		34	39	mA
Negative Supply Current[10]		Full		33	39	mA
Total Power Dissipation		Full		335	390	mW
TEMPERATURE RANGE						
Specification	Ambient	Full	–40		+85	°C
Storage			–55		+150	°C
Thermal Resistance, θ_{JA}		Full		100		°C/W

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is 10µVrms. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Input Voltage Range	±5V
Differential Input Voltage	±5.5V (between +In and –In inputs)
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC605AU	16-Pin SOIC	265

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

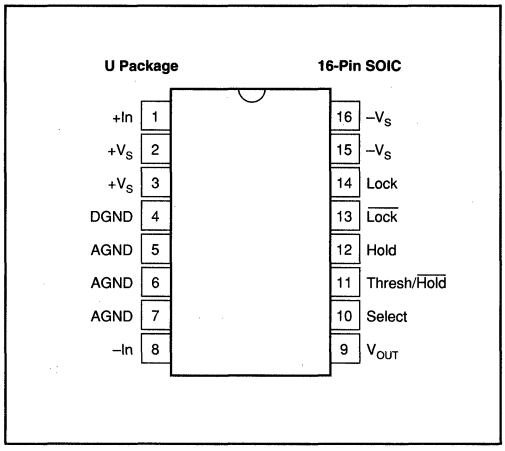
MODEL	PACKAGE	TEMPERATURE
SHC605AU	16-Pin SOIC	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

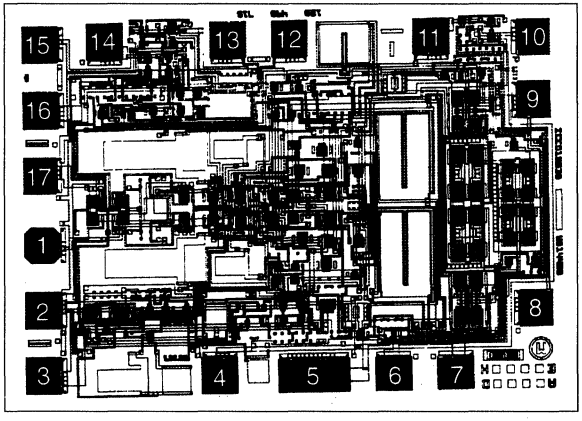
PIN CONFIGURATION



PIN DESCRIPTION

PIN #	SYMBOL	DESCRIPTION
1	+In	Non-Inverting Input
2	$+V_S$	+5V Supply
3	$+V_S$	+5V Supply
4	DGND	Digital Ground
5	AGND	Analog Ground
6	AGND	Analog Ground
7	AGND	Analog Ground
8	–In	Inverting Input
9	V_{OUT}	Output Voltage
10	Select	+5V Selects TTL; –5V Selects ECL
11	Thresh/$\overline{\text{Hold}}$	Logic threshold for single-ended operation or complement Hold input for differential operation
12	Hold	True Hold input
13	$\overline{\text{Lock}}$	Complement Lock Input
14	Lock	True Lock input; Locks SHC605 in Hold-mode regardless of Hold/$\overline{\text{Hold}}$ Inputs
15	$-V_S$	–5V Supply
16	$-V_S$	–5V Supply

DICE INFORMATION



SHC605 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	+In	10	Select
2	$+V_S$	11	Comp
3	$+V_S$	12	Thresh/$\overline{\text{Hold}}$
4	DGND	13	Hold
5	AGND	14	$\overline{\text{Lock}}$
6	C_2	15	Lock
7	C_1	16	$-V_S$
8	–In	17	$-V_S$
9	V_{OUT}		

Substrate Bias: Negative supply ($-V_S$).

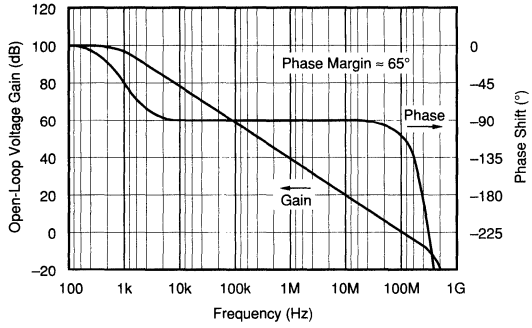
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	58 x 80	
Die Thickness	14 ±1	
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	
Metallization	Gold	

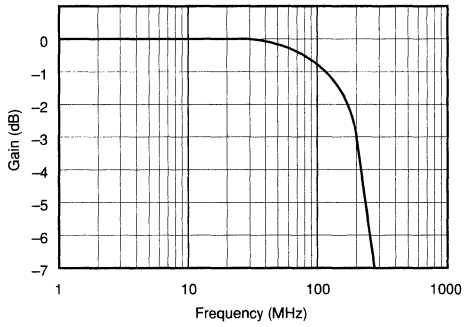
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

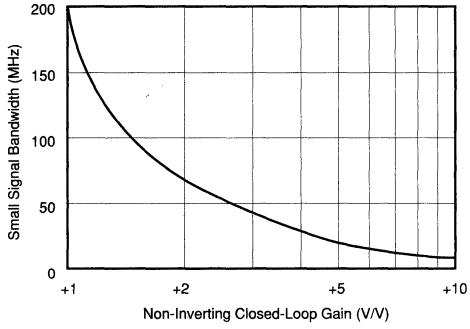
OPEN-LOOP FREQUENCY RESPONSE (Track Mode)



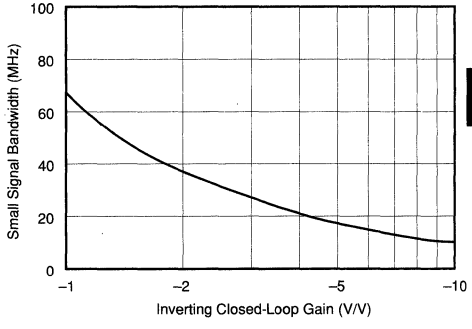
CLOSED-LOOP GAIN = +1V/V
vs FREQUENCY (Track Mode)



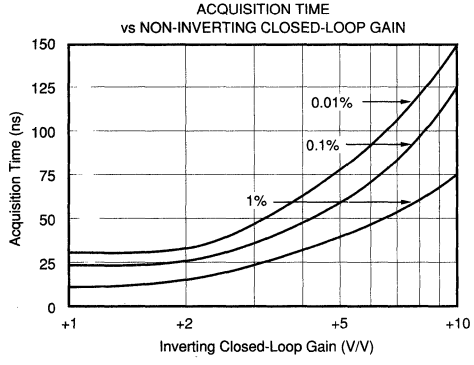
NON-INVERTING CLOSED-LOOP GAIN
vs SMALL SIGNAL BANDWIDTH



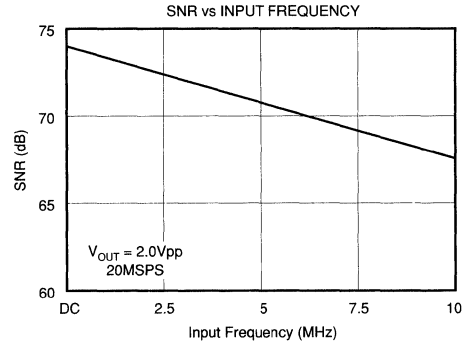
INVERTING CLOSED-LOOP GAIN
vs SMALL SIGNAL BANDWIDTH



ACQUISITION TIME
vs NON-INVERTING CLOSED-LOOP GAIN



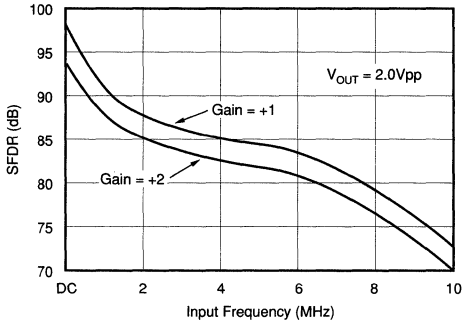
SNR vs INPUT FREQUENCY



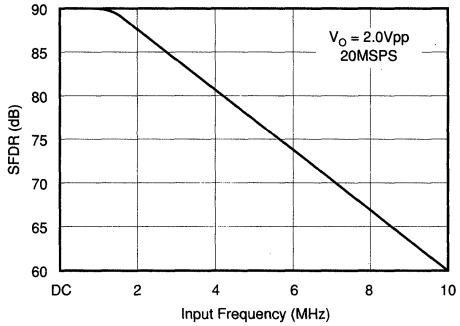
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

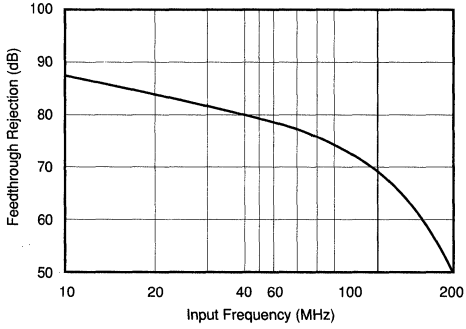
LARGEST HARMONIC
vs INPUT FREQUENCY (Track Mode)



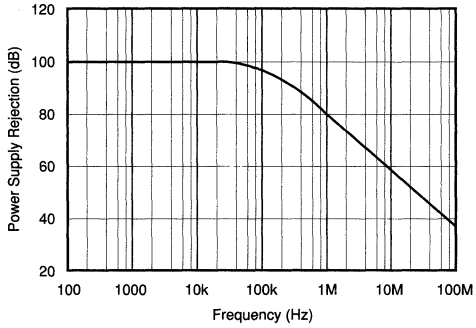
LARGEST HARMONIC
vs INPUT FREQUENCY (Hold Mode)



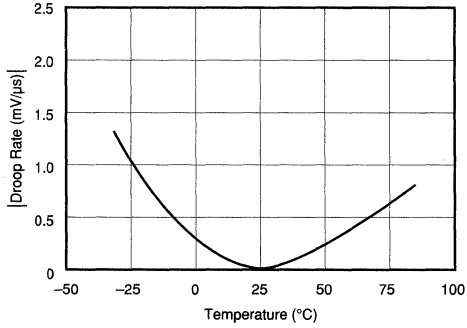
FEEDTHROUGH REJECTION
vs INPUT FREQUENCY



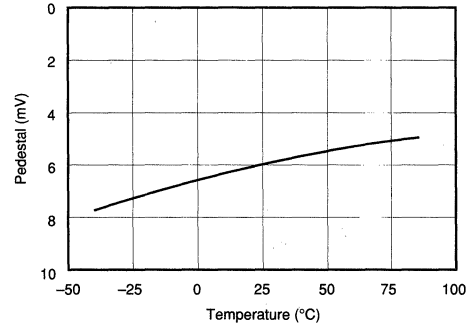
POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY (Track Mode)



DROOP RATE vs TEMPERATURE



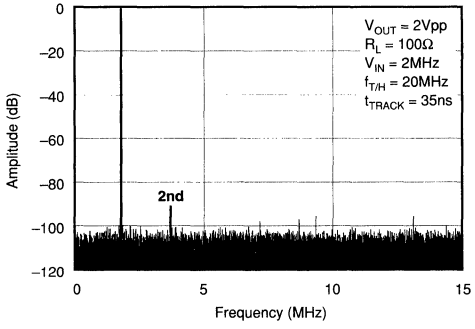
PEDESTAL vs TEMPERATURE



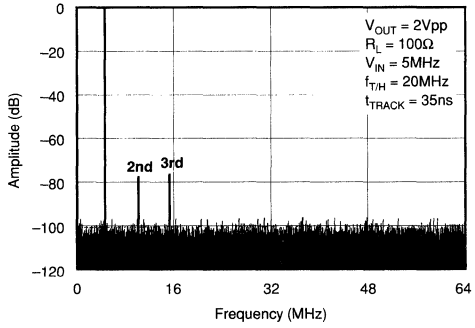
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

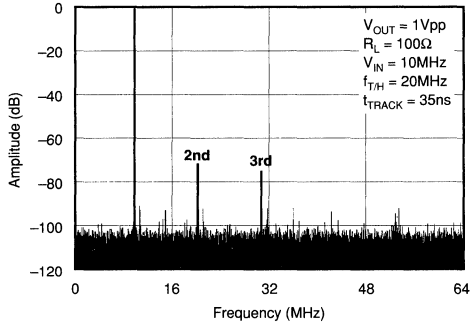
HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 2MHz



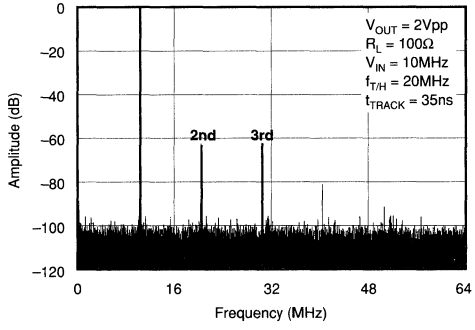
HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 5MHz



HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 10MHz



HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 10MHz



TIMING DEFINITIONS

Acquisition Time is the time it takes to reacquire the input signal when switching from the hold to track mode. This time interval starts at 50% of the clock transition and ends when the input signal is reacquired to within a specified accuracy at the output. This specification does not include the track-to-hold settling time.

Aperture Delay is a measure of the track-to-hold switch delay time. It is the difference between the analog input amplifier's signal path delay and the digital track-to-hold switch delay. A positive delay indicates the digital switch delay is larger than the analog amplifier delay.

Aperture Jitter is random variation in the aperture delay. This specification is measured in ps-rms and results in phase noise on the held signal. A large aperture jitter value can manifest itself by degrading the SNR of a sampling ADC.

Droop Rate is the change of the held output voltage as a function of time. The measurement starts immediately after the device switches from the track to hold mode.

Feedthrough Rejection is a measure of the amount of the input signal that "feeds through" to the output while the device is in the hold mode. This specification is usually a function of frequency, with degradation at higher frequencies.

Hold-to-Track Delay is the time from the track command to the point when the output begins changing to acquire a new signal. This delay is included in the SHC605's specified acquisition time.

Pedestal Offset is the error voltage step incurred at the output when the device is switched from the track to hold mode.

Track-to-Hold Settling Time is the time for the track to hold transient to settle to within a specified accuracy.

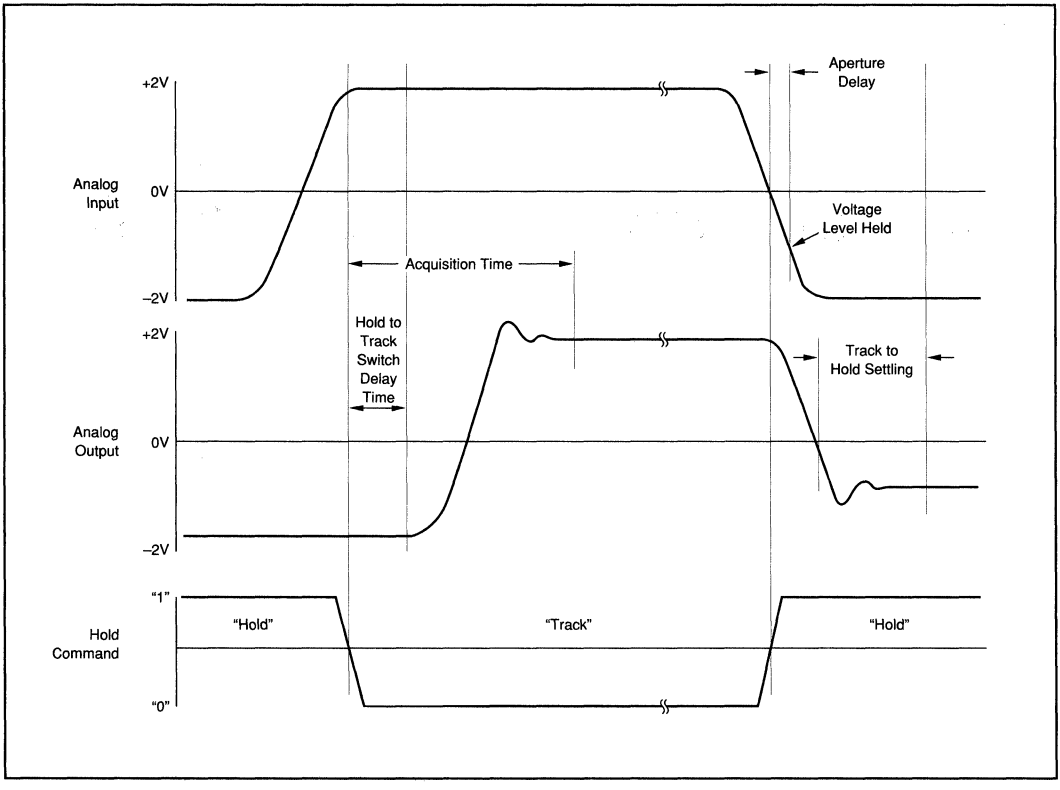


FIGURE 1. SHC605 Timing Diagram.

THEORY OF OPERATION

The SHC605 is a monolithic track-and-hold circuit fabricated on an extremely fast complementary bipolar process. Figure 2 provides a simplified circuit diagram of the SHC605. A conventional two-stage operational amplifier is shown with a standard differential phase compensation scheme sometimes referred to as "doublet compensation." Capacitors C_1 and C_2 compensate the amplifier in the track-mode and hold the analog output signal in the hold-mode. Switching from track to hold is achieved by turning off the amplifier's input stage and isolating C_1 and C_2 from the input signal.

The differential two-stage amplifier architecture of the SHC605 provides many performance advantages over traditional open-loop designs. The use of differential hold capacitors provides a first-order correction for many errors including distortion, pedestal, and droop. A dominant cause of distortion in high-speed amplifiers is the nonlinear transistor junction capacitance connected to the hold capacitor(s). This parasitic capacitance varies as the voltage across it changes. Most open-loop track-and-hold circuits have a fixed gain of +1V/V, which means the hold capacitor(s) and parasitic junction capacitance sees the full output signal swing. In the SHC605 the second gain stage attenuates the signal across the capacitors and greatly reduces the nonlinear capacitance. The SHC605's second stage has a unity-gain bandwidth of approximately 250MHz and its open-loop gain rolls off at –20dB/decade. With a 2.5MHz signal, the voltage across the hold capacitors is 100 times less than the output signal, and therefore, the nonlinear capacitance is greatly reduced.

The SHC605's patented architecture provides users with an extremely accurate high-speed *operational* track-and-hold amplifier. All common operational amplifier transfer functions can be realized with the SHC605; i.e. unity-gain, noninverting gain, inverting gain, and differential gain. These configurations are shown in Figures 3 through 6. In many instances, the SHC605 provides a superior single-chip solution to applications previously requiring two or more devices. As with any conventional voltage feedback op amp, it is important to consider tradeoffs between noise, bandwidth, and settling time for these applications. Refer to Discussion of Performance and Typical Performance Curves for more details.

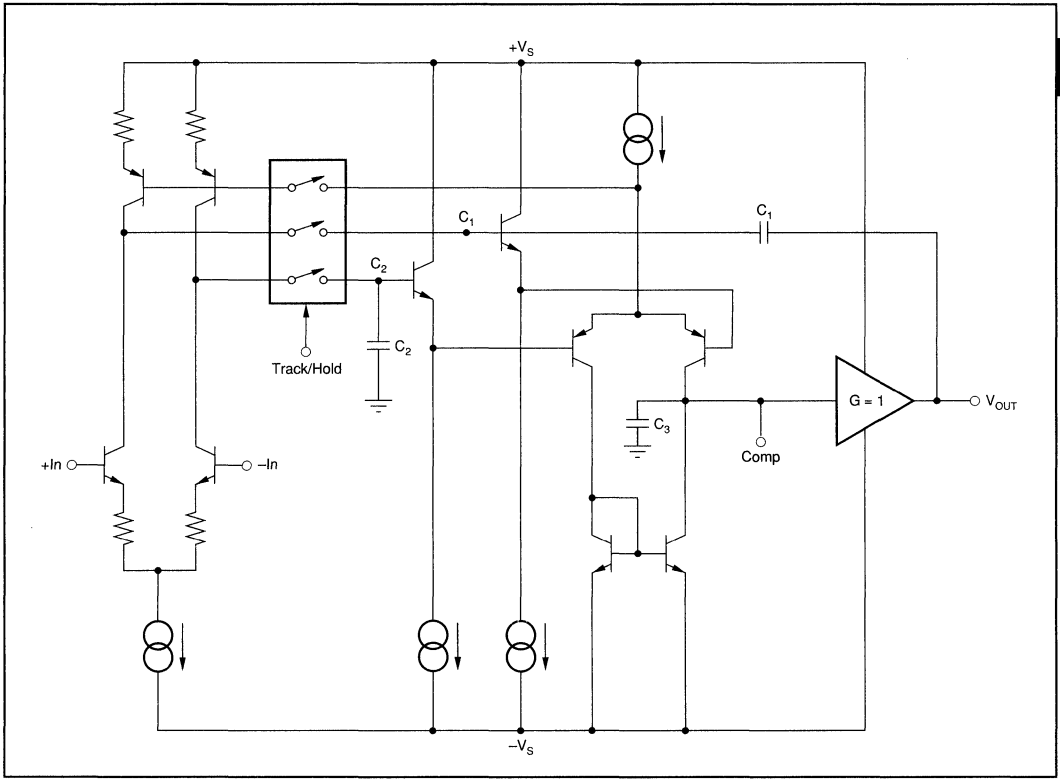


FIGURE 2. SHC605 Simplified Circuit Diagram.

DISCUSSION OF PERFORMANCE

DISTORTION

Hold-mode distortion is an important specification for a track-and-hold amplifier. This is a measure of the accuracy of the amplifier's held output while sampling a sinusoidal input signal. It includes errors from both the switching network and the amplifier's signal path. Hold-mode distortion depends on the input signal's amplitude and frequency as well as the sampling rate. The biggest cause of distortion in the SHC605 is slew-induced nonlinearity; the higher the amplitude of a high frequency input, the higher the distortion. Hold-mode distortion can also result from sampling too fast or not allowing enough acquisition time or track-to-hold settling time. The SHC605 has a typical 0.01% acquisition time of 30ns for a 2V step, and a typical 100µV track-to-hold settling time of 15ns. Thus, for 12-bit accuracy the clock rate should not exceed 22MHz (refer to Typical Performance Curves for details).

NOISE

The SHC605's noise performance is almost completely determined by track-mode noise. This is the noise sampled by the differential hold capacitors during track-mode, which is greater than the noise measured directly at the output. The input referred noise of the SHC605 is 2.5nV/$\sqrt{\text{Hz}}$. For unity-gain this corresponds to an output noise of approximately 35µVrms; which is much lower than the typical 150µVrms noise sampled by the hold capacitors. The track-mode noise sampled by the hold capacitors is independent of closed-loop gain, and therefore, the SHC605 can be used with higher closed-loop gain without degrading the overall noise performance.

The SHC605's noise performance is also affected by hold-mode noise and aperture jitter. Hold-mode noise is the result of current noise reacting with the hold capacitors. This noise accumulates on the capacitors at a rate which is proportional to the square root of the hold time. For sample rates above 1MHz this noise is usually insignificant. Aperture jitter describes the random variation in track-to-hold aperture delay, and causes increased hold-mode noise when high slew rate signals are sampled. A differential ECL clock input will provide lower aperture jitter than a single-ended ECL or TTL clock.

CHOOSING THE BEST ARCHITECTURE

The SHC605 is basically a high-speed operational amplifier which can hold its output on command. Unlike traditional high-speed track-and-hold amplifiers, which have fixed gains of +1V/V, the SHC605 can be used with non-inverting, inverting, or differential gains. In many applications, a single SHC605 can be used to solve a problem that previously required two or more devices.

Figures 3 through 6 show the SHC605 connected for non-inverting, inverting, and differential gains. As with any op amp, it is important to consider performance tradeoffs for all of these configurations. For gains less than ±10, the SHC605's track-to-hold settling, pedestal offset, droop, and total hold-mode noise remains constant. However, small-signal bandwidth and acquisition time will be compromised as the closed-loop gain is increased (refer to the Typical Performance Curves for details).

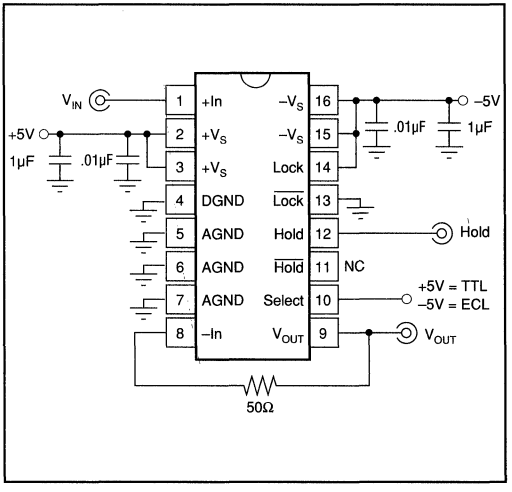


FIGURE 3. Gain of +1 Track-and-Hold Amplifier.

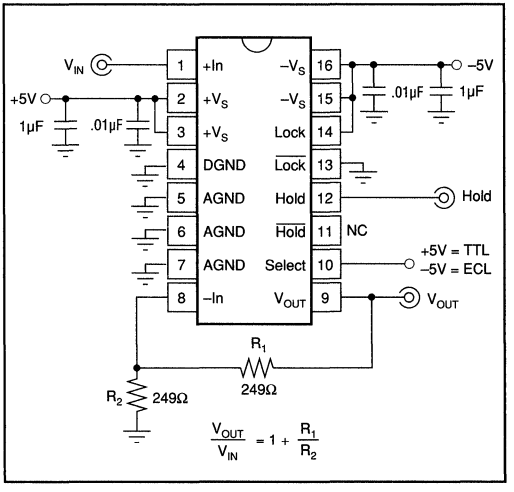


FIGURE 4. Gain of +2 Track-and-Hold Amplifier.

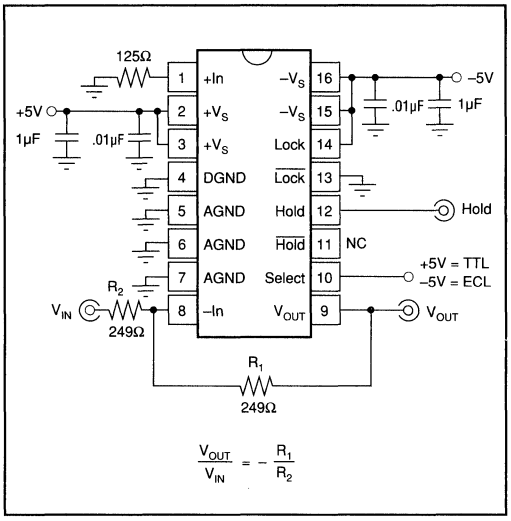


FIGURE 5. Gain of –1 Track-and-Hold Amplifier.

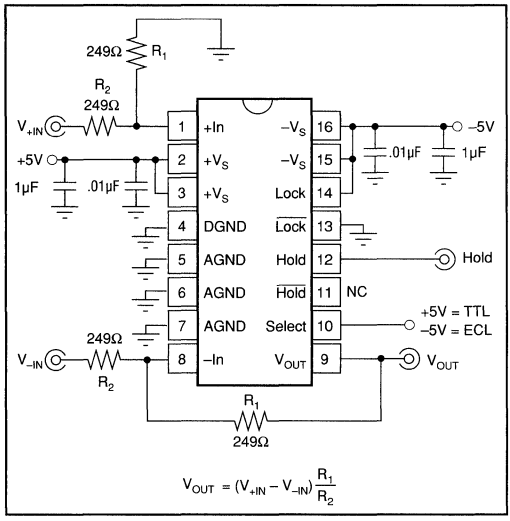


FIGURE 6. Differential Gain of 1 Track-and-Hold Amplifier.

APPLICATIONS INFORMATION

LOGIC COMPATIBILITY/TRACK-TO-HOLD SWITCHING

The SHC605 contains an internal reference circuit which produces either an ECL or TTL logic threshold voltage for single-ended track-to-hold switching. Differential ECL switching is also possible with the SHC605. Table I provides the proper pin connections for all of the possible switching options and the Performance Specifications Table gives the logic levels and input bias currents.

LOGIC TYPE	DGND (Pin 4)	SELECT (Pin 10)	THRESH/$\overline{\text{HOLD}}$ (Pin 11)	HOLD (Pin 12)
Single-ended TTL	GND	+5V	NC	Clock
Single-ended ECL	GND	–5V	NC	Clock
Differential ECL	NC	NC	$\overline{\text{Clock}}$	Clock

TABLE I. Track-to-Hold Switching Options.

LOCKOUT CIRCUITRY

The SHC605 includes additional logic circuitry which allows edge-triggered operation for sampling ADCs. The lockout comparator and Track/Hold comparator form a wired-or mode control circuit as shown in the block diagram on page one. When the Lock input, pin 14, is high with respect to the $\overline{\text{Lock}}$ input, pin 13, the SHC605 is in the Hold-mode regardless of the Hold/$\overline{\text{Hold}}$ inputs. This feature provides more flexibility in the convert command duty cycle and reduces noise resulting from aperture jitter.

Figure 7 shows how the SHC605 lockout circuit can be used with an ECL one-shot to provide an edge-triggered sampling ADC. An ECL threshold voltage is generated on Thresh/$\overline{\text{Hold}}$ (Pin 11), which is connected to $\overline{\text{Lock}}$ (Pin 13), to allow a single-ended lockout input on Lock (Pin 14). The ECL convert command is applied directly to the SHC605. The 10ns delay on the ADCs convert signal is to allow for SHC605 track-to-hold settling. The one-shot's duty cycle

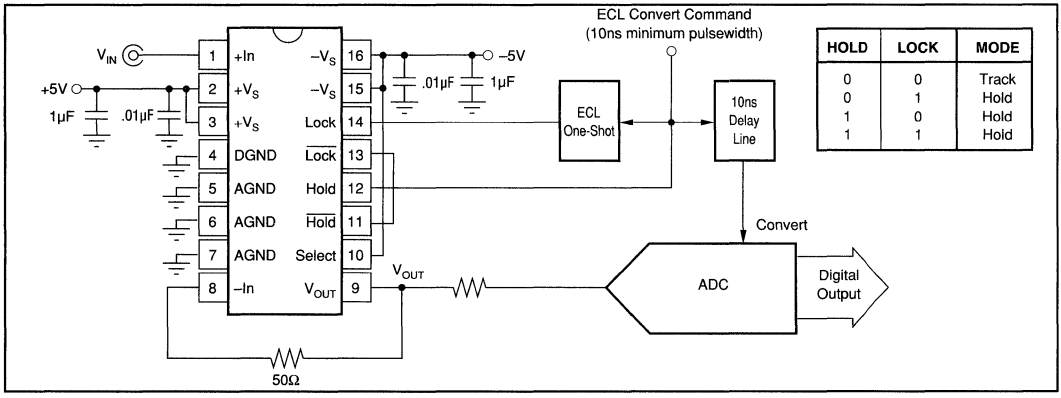


FIGURE 7. Edge-Triggered ADC.

will depend on the ADC conversion time. In this application the one-shot is used to set the critical ADC timing which means the user has more freedom in selecting the convert command duty cycle. Since the convert command is applied directly to the SHC605—instead of after additional logic and clock conditioning—aperture jitter noise is minimized.

OFFSET VOLTAGE ADJUSTMENT

The SHC605's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 8 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input offset voltage errors due to the amplifier's input offset current, which is typically only 0.2µA.

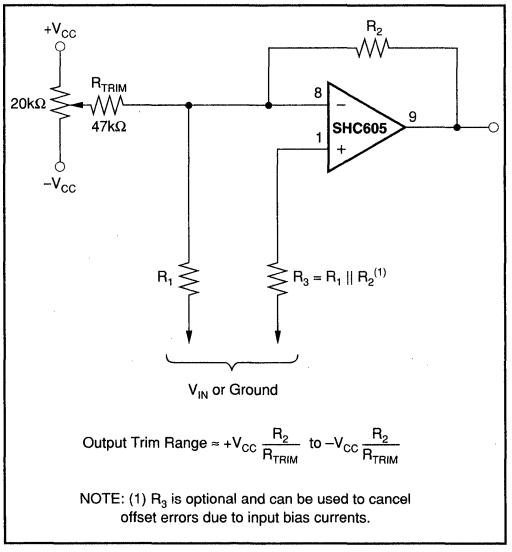


FIGURE 8. Offset Voltage Trim.

INPUT PROTECTION

The SHC605 incorporates on-chip ESD protection diodes as shown in Figure 9. All pins on the SHC605 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability diode current should be externally limited to 10mA or so whenever possible. Static damage can cause subtle changes in SHC605 input characteristics without necessarily destroying the device. In precision track-and-hold amplifiers, this may cause a noticeable degradation in performance. Therefore, static protection is recommended when handling the SHC605.

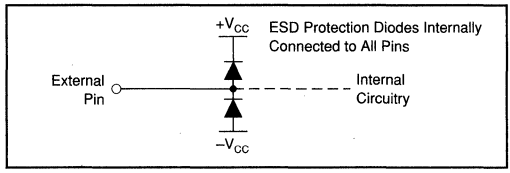


FIGURE 9. Internal ESD Protection.

LAYOUT AND BYPASSING

For best performance, good high speed design techniques must be applied. The component (top) side ground plane should be as large as possible and continuous (not fragmented). Two ounce copper cladding is recommended.

All traces should be as short as possible, especially the output. As much of the ground plane as possible should be removed from around the +In, –In, and V_{OUT} pins to reduce parasitic capacitance and minimize coupling onto the analog signal path.

Power supply decoupling capacitors must be used as shown in Figures 3 through 6. The 0.01µF capacitors should be low inductance surface mount devices and should be connected as close to the SHC605 ±Vs leads as possible (within 30 mils). The 1µF low frequency bypass capacitors should be tantalum capacitors (preferably surface mount) and should be located within one inch of the SHC605. Surface mount resistors are also recommended and should be placed as close to the SHC605 as possible to minimize inductance.

CAPACITIVE LOADS

The SHC605's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 20Ω to 50Ω, in series with the output as shown in

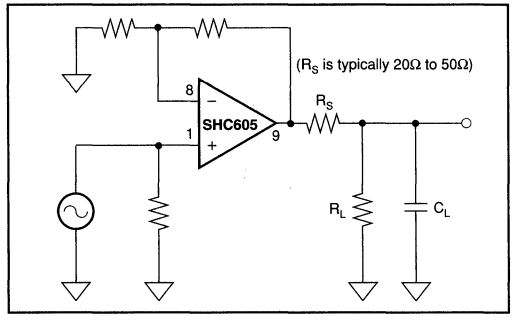


FIGURE 10. Driving Capacitance Load.

Figure 10. This is particularly important when driving high capacitance loads such as flash A/D converters.

The series resistor, R_S, should be connected as close to the SHC605 as possible. If R_S causes excessive output attenuation, add closed-loop gain to the SHC605 as shown in Figures 4 through 6.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coaxial cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

APPLICATIONS

The SHC605's combination of high speed and accuracy, small size, and low price makes it ideally suited for many data acquisition applications. Its versatile operational amplifier architecture and switching flexibility provides users with an extremely reliable single-chip solution to problems that previously required several components. Figures 11 through 16 show many application circuits using the SHC605. These include high-speed flash and sub-ranging ADC driving, multi-channel simultaneous sampling, DAC deglitching, and peak detecting.

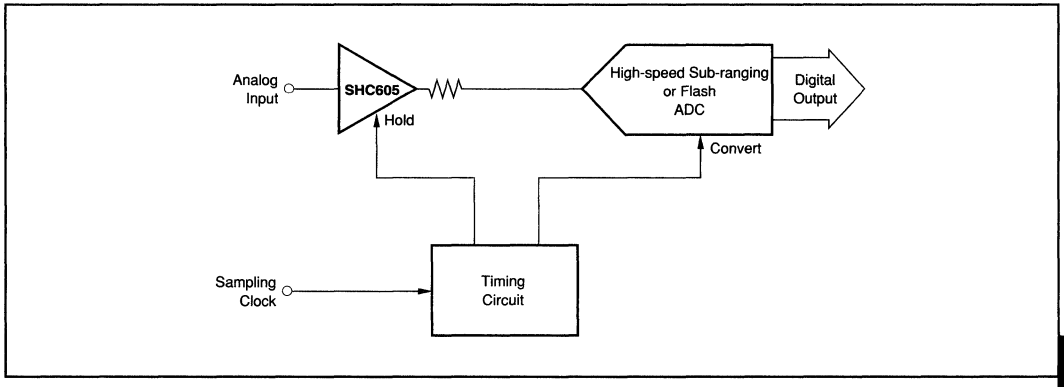


FIGURE 11. Sampling ADC.

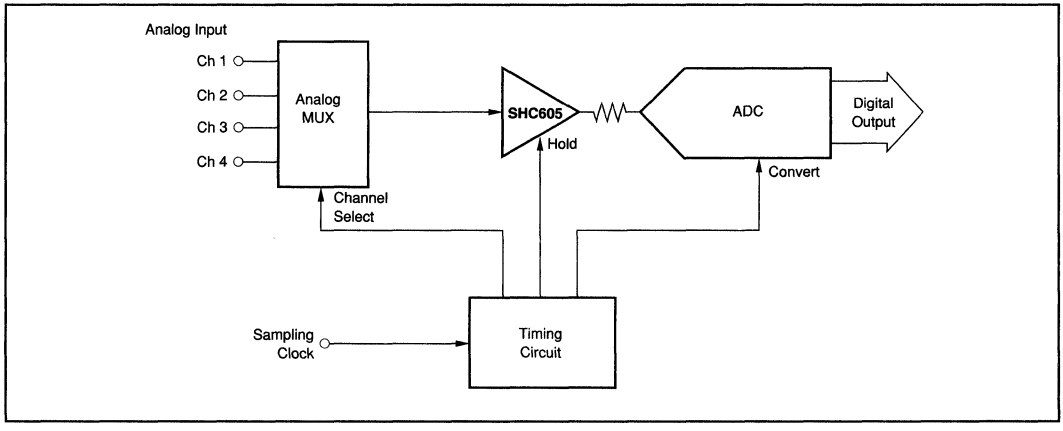


FIGURE 12. Traditional Data Acquisition System.

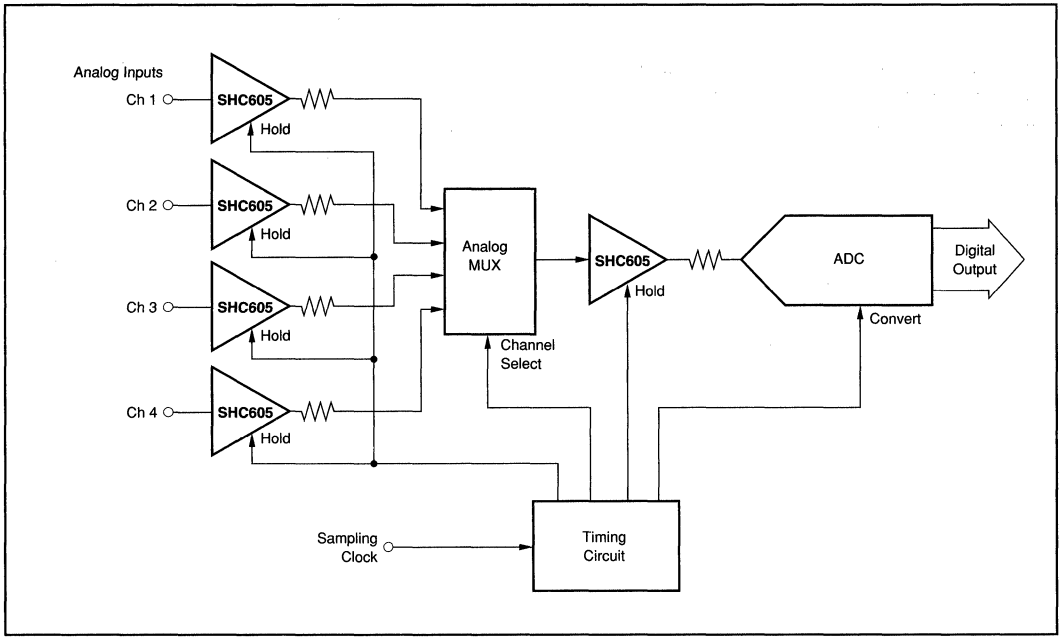


FIGURE 13. Multi-Channel Simultaneous Sampling System.

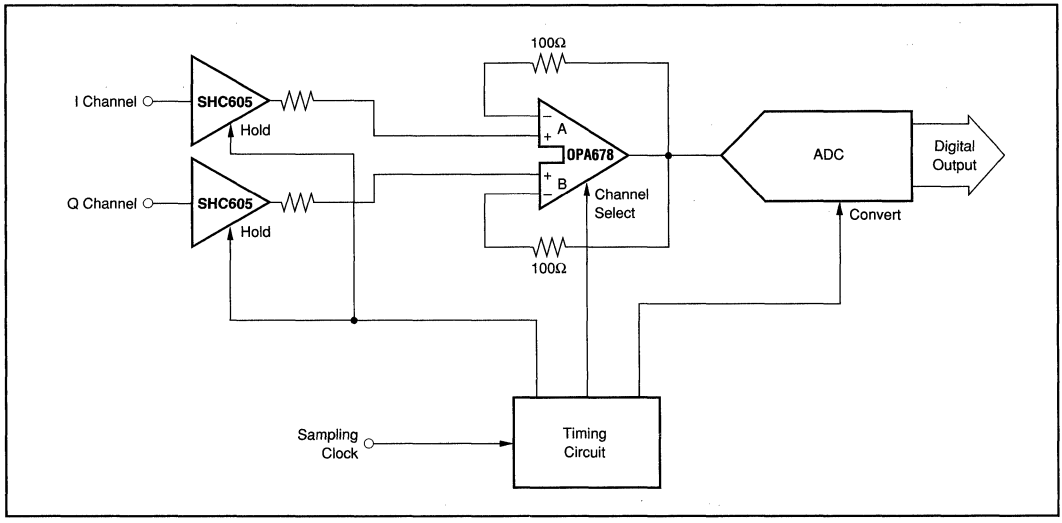


FIGURE 14. I/Q Channel Simultaneous Sampling.

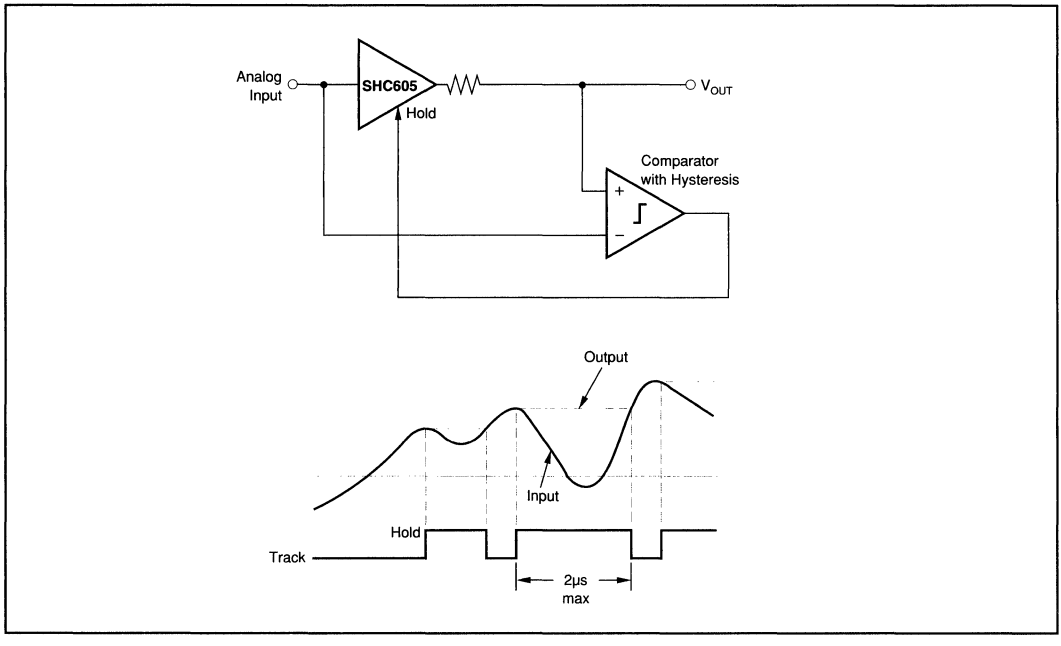


FIGURE 15. High-Speed Peak Detector.

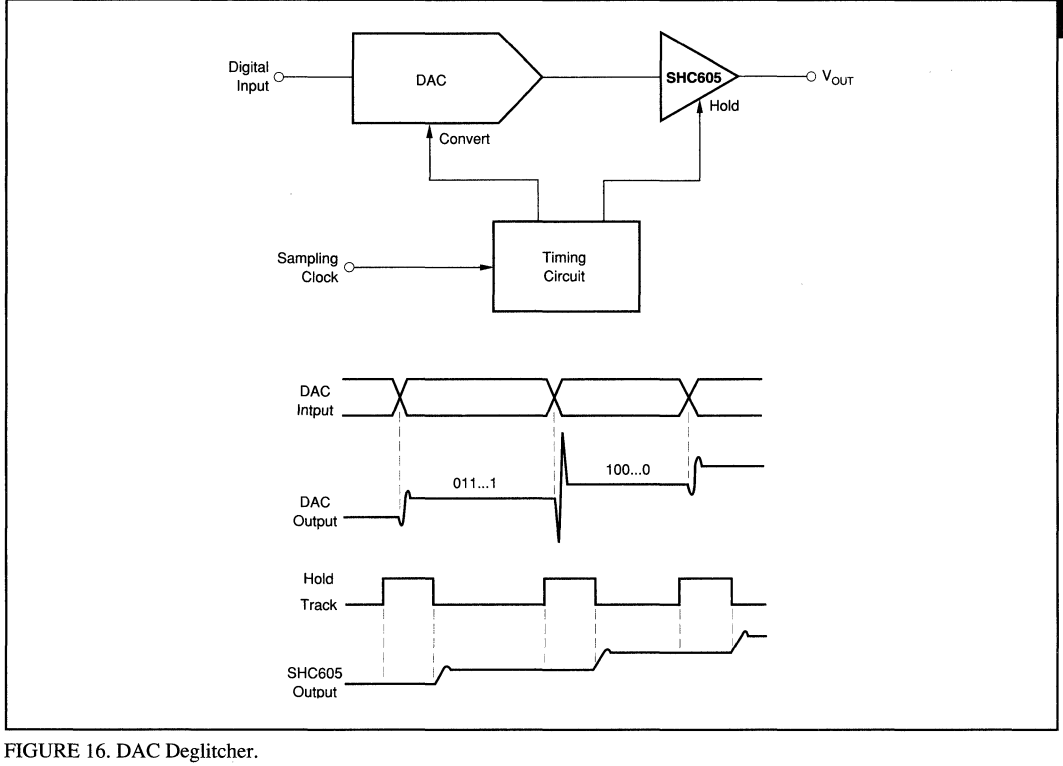


FIGURE 16. DAC Deglitcher.

BURR-BROWN®

SHC615

Wide-Bandwidth, DC RESTORATION CIRCUIT

FEATURES

- PROPAGATION DELAY: 2.2ns
- BANDWIDTH: OTA: 750MHz
  Comparator: 280MHz
- LOW INPUT BIAS CURRENT: –0.3µA
- SAMPLE/HOLD SWITCHING TRANSIENTS: +1/–7mV
- SAMPLE/HOLD FEEDTHROUGH REJECTION: 100dB
- CHARGE INJECTION: 40fC
- HOLD COMMAND DELAY TIME: 3.8ns
- TTL/CMOS HOLD CONTROL

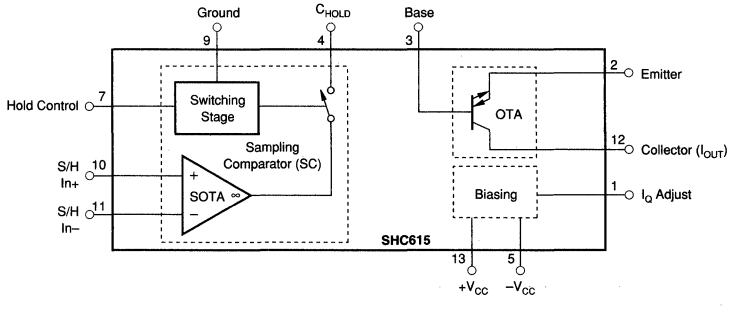
APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- TELECOMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- CAD MONITORS/CCD IMAGE PROCESSING
- NANO SECOND PULSE INTEGRATOR/ PEAK DETECTORS
- PULSE CODE MODULATOR/ DEMODULATOR
- COMPLETE VIDEO DC LEVEL RESTORATION
- SAMPLE/HOLD AMPLIFIER

DESCRIPTION

The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low frequency hum suppression of wideband amplifiers or buffers. Designed to stabilize the performance of video signals, it can also be used as a sample/hold amplifier, high-speed integrator, or peak detector for nanosecond pulses. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nanoseconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is available in SO-14 surface mount and 14-pin plastic DIPs, and is specified over the extended temperature range of –40°C to +85°C.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

DC SPECIFICATIONS

At V_{CC} = ±5V, R_{LOAD} = 100Ω, R_O = 300Ω, R_{IN} = 150Ω and T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU MIN	SHC615AP, AU TYP	SHC615AP, AU MAX	UNITS
OFFSET VOLTAGE, V_E at V_B = 0					
Initial			8	±40	mV
vs Temperature			40		µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	50	55		dB
B-INPUT BIAS CURRENT					
Initial			–0.3	±0.9	µA
vs Temperature			1		nA/°C
C-OUTPUT BIAS CURRENT, I_C at V_B = 0					
Initial		–200	–77	+100	µA
B-INPUT IMPEDANCE			4.4		MΩ
INPUT NOISE					
Voltage Noise Density, B-to-E	f_{OUT} = 100kHz to 100MHz		2.2		nV/√Hz
Voltage Noise Density, B-to-C	f_{OUT} = 100kHz to 100MHz		4.5		nV/√Hz
INPUT VOLTAGE RANGE			±3.4		V
OUTPUT					
Output Voltage Compliance			±3.2		V
C-Current Output		±18	±20		mA
E-Current Output		±18	±20		mA
C-Output Impedance			0.5		MΩ
E-Output Impedance			12		Ω
Open-Loop Gain			96		dB
TRANSCONDUCTANCE	Small Signal, <200mV		70		mA/V

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DC SPECIFICATIONS (CONT)

At V_{CC} = ±5V, R_{LOAD} = 1kΩ, R_Q = 300Ω, and T_A = +25°C, unless otherwise specified.

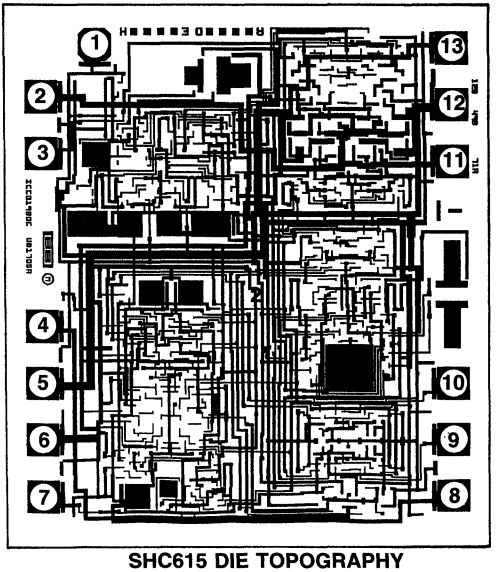
PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
COMPARATOR					
INPUT BIAS CURRENT					
Initial			1.0	±5	µA
vs Temperature			–2.3		nA/°C
C-OUTPUT BIAS CURRENT					
Initial			±10	±50	µA
vs Temperature			±13		nA/°C
INPUT IMPEDANCE					
Input Impedance			0.2		MΩ
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 100kHz to 100MHz		5		nV/√Hz
INPUT VOLTAGE RANGE					
Input Voltage Range			±3.0		V
Common-Mode Input Range			±3.2		V
OUTPUT					
Output Voltage Compliance			±3.5		V
C-Current Output		±2.5	±3.2		mA
C-Output Impedance			620 || 2		kΩ || pF
Open-Loop Gain			83		dB
TRANSCONDUCTANCE					
Transconductance			22		mA/V
HOLD CONTROL					
Logic 1 Voltage		+2		$+V_{CC}$ +0.6	V
Logic 0 Voltage		0		0.8	V
Logic 1 Current	V Hold Control = 5.0V		1		µA
Logic 0 Current	V Hold Control = 0.8V		0.05		µA
TRANSFER CHARACTERISTICS					
Charge Injection	Track-To-Hold		40		fC
Feedthrough Rejection	Hold Mode		–100		dB
COMPLETE SHC615					
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	R_Q = 300Ω	±12	±15	±18	mA
Quiescent Current Range	Programmable (Useful Range)		±3 to ±36		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C

AC SPECIFICATIONS

At V_{CC} = ±5V, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, R_Q = 300Ω, and T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU MIN	SHC615AP, AU TYP	SHC615AP, AU MAX	UNITS
FREQUENCY DOMAIN					
OTA					
LARGE-SIGNAL BANDWIDTH (–3dB), (B-to-E)	V_{OUT} = 5.0Vp-p V_{OUT} = 2.8Vp-p V_{OUT} = 1.4Vp-p		430 540 620		MHz MHz MHz
SMALL-SIGNAL BANDWIDTH B-TO-E	V_{OUT} = 0.2Vp-p		520		MHz
DIFFERENTIAL GAIN (B-TO-E)	f = 4.43MHz, V_{OUT} = 0.7Vp-p, R_L = 150Ω R_L = 500Ω		 1.8 0.1		 % %
DIFFERENTIAL PHASE (B-TO-E)	f = 4.43MHz, V_{OUT} = 0.7Vp-p, R_L = 150Ω R_L = 500Ω		 0.07 0.01		 Degrees Degrees
HARMONIC DISTORTION (B-TO-E) Second Harmonic Third Harmonic	f = 30MHz, V_{OUT} = 1.4Vp-p		 –50 –46		 dBc dBc
LARGE SIGNAL BANDWIDTH (–3dB), (B-to-C)	V_{OUT} = 5.0Vp-p V_{OUT} = 2.8Vp-p V_{OUT} = 1.4Vp-p		250 580 750		MHz MHz MHz
SMALL SIGNAL BANDWIDTH B-to-C	V_{OUT} = 0.2Vp-p		680		MHz
COMPARATOR	Sample Mode				
BANDWIDTH (–3dB)	I_{OUT} = 4mAp-p I_{OUT} = 2mAp-p I_{OUT} = 1mAp-p		240 270 280		MHz MHz MHz
TIME DOMAIN					
OTA					
RISE TIME	2Vp-p Step, 10% to 90% B-to-E B-to-C		 1.1 1.2		 ns ns
SLEW RATE	2Vp-p, B-to-E B-to-C 5Vp-p, B-to-E B-to-C		1800 1700 3300 3000		V/µs V/µs V/µs V/µs
COMPARATOR					
RISE TIME (Sample Mode)	10% to 90%, R_L = 50Ω, I_{OUT} = ±2mA C_{LOAD} = 1pF		2.5		ns
SLEW RATE (Sample Mode)	10% to 90%, R_L = 50Ω, I_{OUT} = ±2mA C_{LOAD} = 1pF		0.95		mA/ns
DYNAMIC CHARACTERISTICS Propagation Delay Time Propagation Delay Time Delay Time	 t_{PDH}, V_{OD} = 200mV t_{PDL}, V_{OD} = 200mV Sample-to-Hold Hold-to-Sample		 2.2 2.15 3.8 3.0		 ns ns ns ns

DICE INFORMATION



SHC615 DIE TOPOGRAPHY

DIE PAD	FUNCTION
1	I_Q Adjust
2	OTA-Emitter
3	OTA-Base
4	C_{HOLD}
5	–5V Supply, Analog
6	–5V Supply, Digital
7	Hold Control
8	Ground
9	S/H In+
10	S/H In–
11	I_{OUT}, OTA-Collector
12	+5V Supply, Analog
13	+5V Supply, Digital

Substrate Bias: Negative Supply.
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	73 x 81, ±5	1.86 x 2.06, ±0.13
Die Thickness	14, ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6V
Input Voltage[1]	$\pm V_{CC}$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Hold Control	–0.5V to $+V_{CC}$ +0.7V

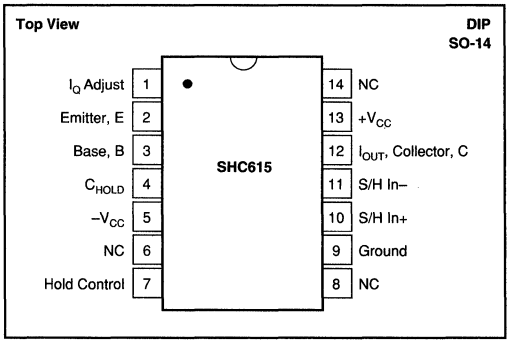
NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC615AP	Plastic 14-Pin DIP	010
SHC615AU	SO 14-Pin Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

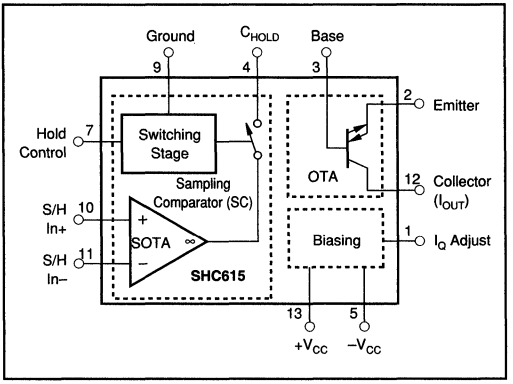
PIN CONFIGURATION



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
SHC615AP	Plastic 14-Pin DIP	–40°C to +85°C
SHC615AU	SO 14-Pin Surface Mount	–40°C to +85°C

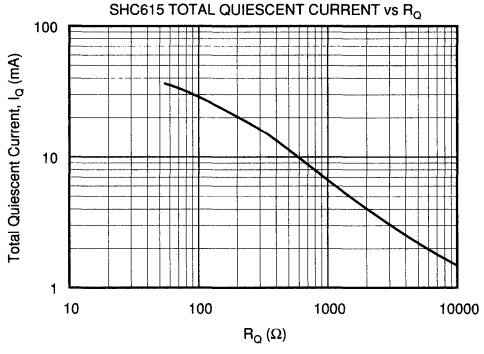
BLOCK DIAGRAM



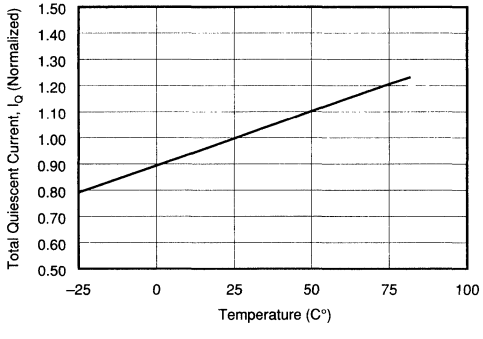
TYPICAL PERFORMANCE CURVES

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

SHC615 TOTAL QUIESCENT CURRENT vs R_Q

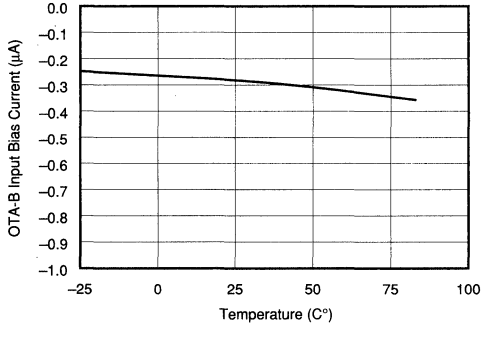


TOTAL QUIESCENT CURRENT vs TEMPERATURE

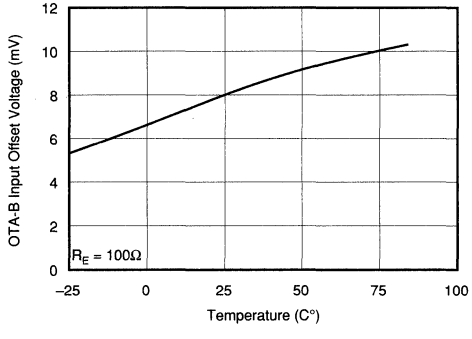


OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

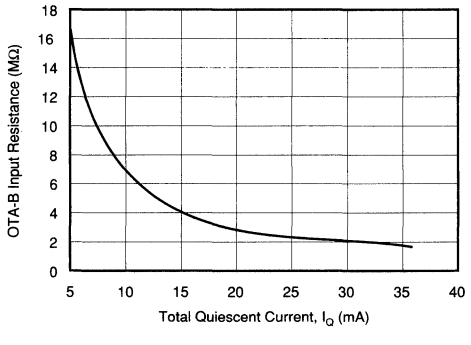
OTA B-INPUT BIAS CURRENT vs TEMPERATURE



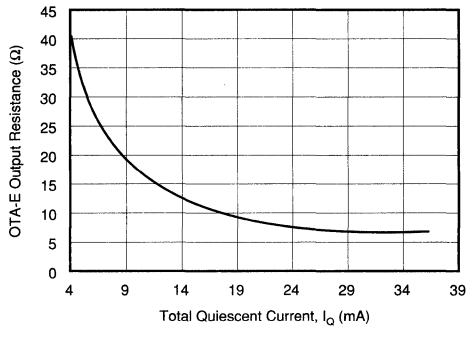
OTA-B INPUT OFFSET VOLTAGE vs TEMPERATURE



OTA-B INPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



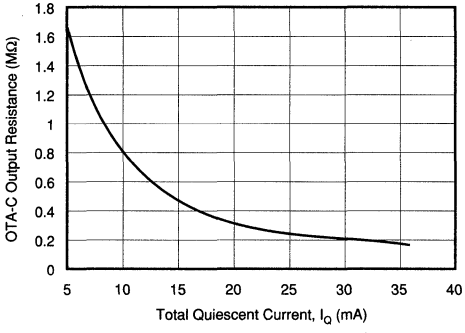
OTA-E OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



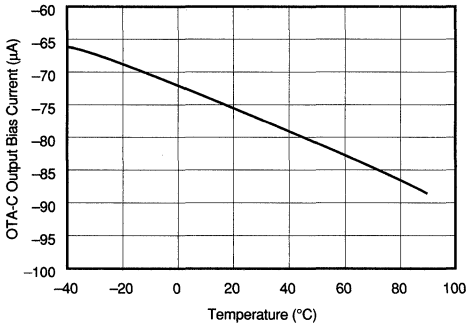
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

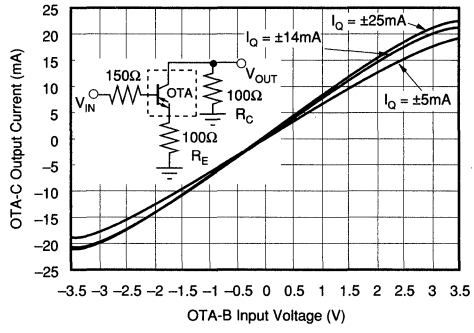
OTA-C OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



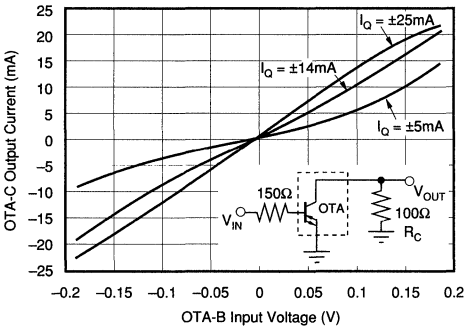
OTA-C OUTPUT BIAS CURRENT vs TEMPERATURE



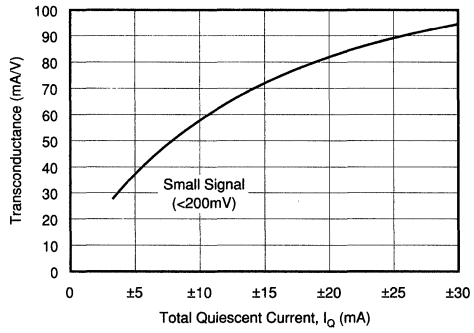
OTA TRANSFER CHARACTERISTICS vs INPUT VOLTAGE



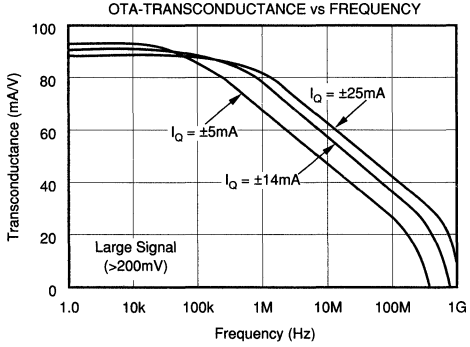
OTA TRANSFER CHARACTERISTIC vs INPUT VOLTAGE



OTA TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT



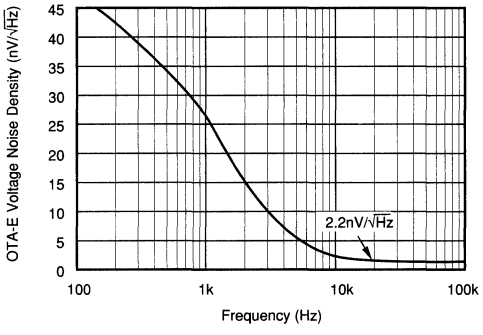
OTA-TRANSCONDUCTANCE vs FREQUENCY



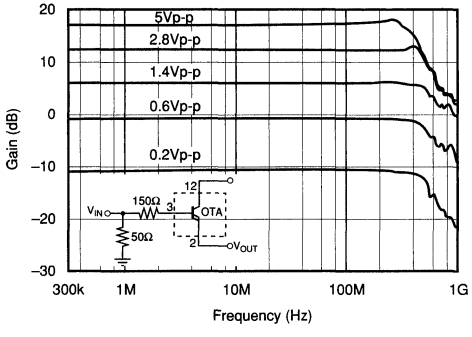
TYPICAL PERFORMANCE CURVES (CONT)

R_O = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

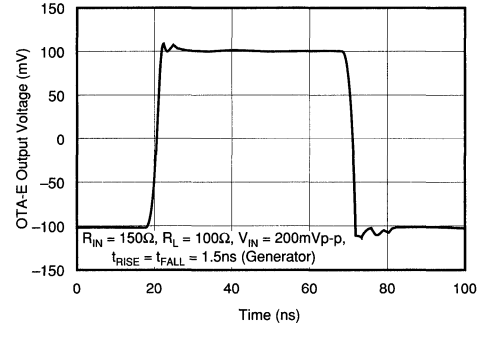
OTA-E VOLTAGE NOISE SPECTRAL DENSITY



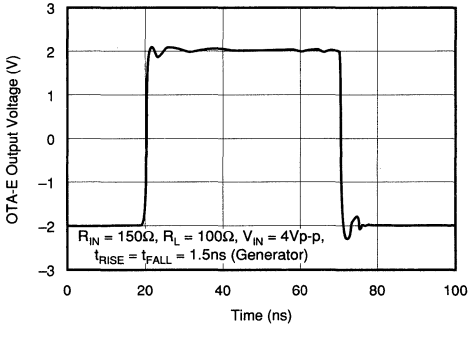
OTA-E FREQUENCY RESPONSE



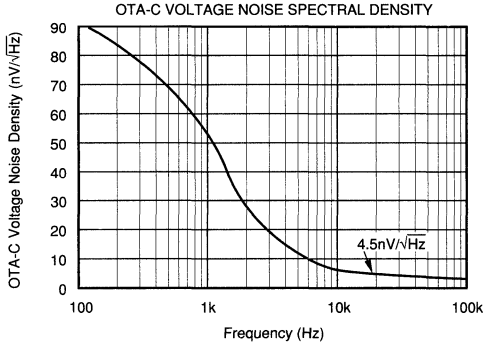
OTA-E SMALL SIGNAL PULSE RESPONSE



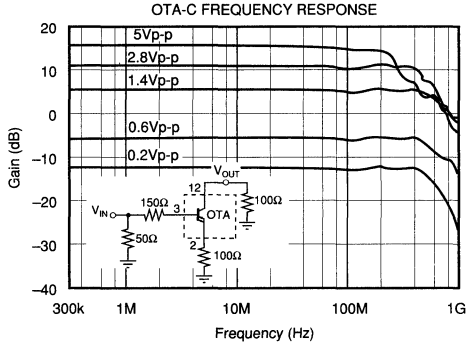
OTA-E LARGE SIGNAL PULSE RESPONSE



OTA-C VOLTAGE NOISE SPECTRAL DENSITY



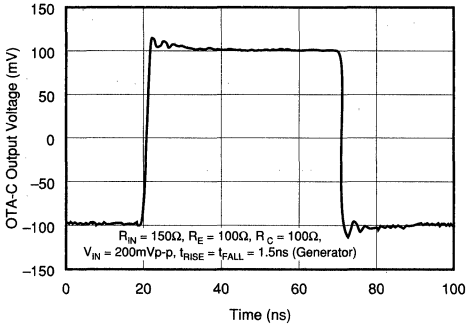
OTA-C FREQUENCY RESPONSE



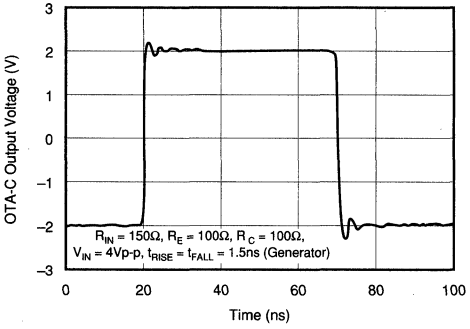
TYPICAL PERFORMANCE CURVES (CONT)

R_G = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

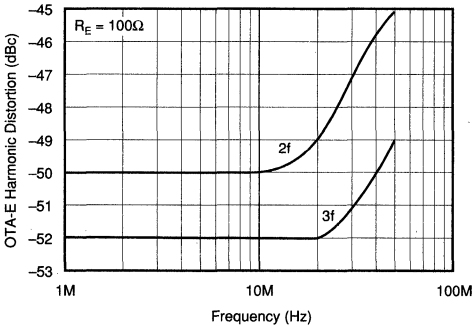
OTA-C SMALL SIGNAL PULSE RESPONSE



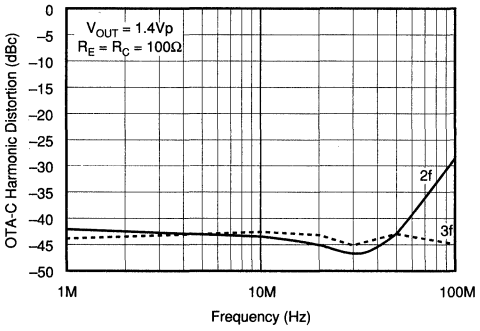
OTA-C LARGE SIGNAL PULSE RESPONSE



OTA-E HARMONIC DISTORTION vs FREQUENCY

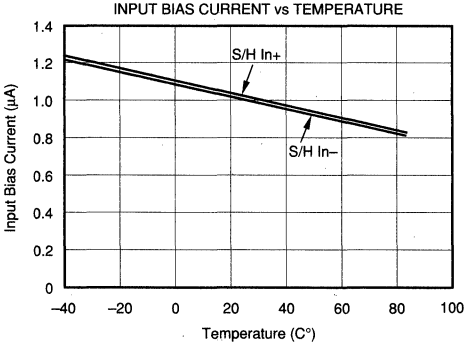


OTA-C HARMONIC DISTORTION vs FREQUENCY

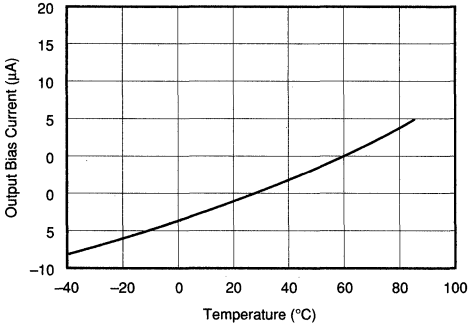


SAMPLING COMPARATOR

INPUT BIAS CURRENT vs TEMPERATURE



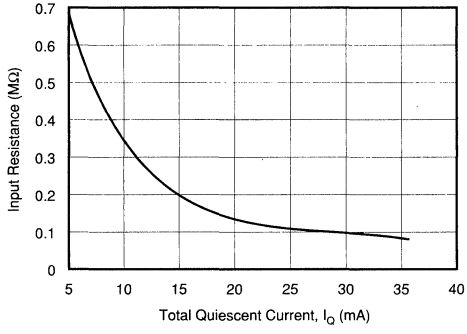
OUTPUT BIAS CURRENT vs TEMPERATURE



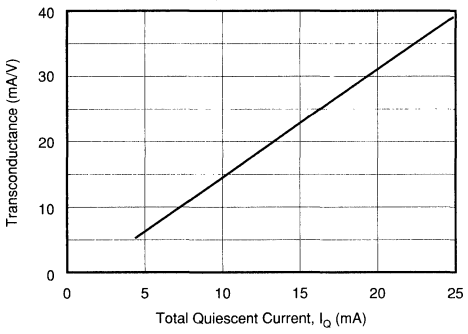
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

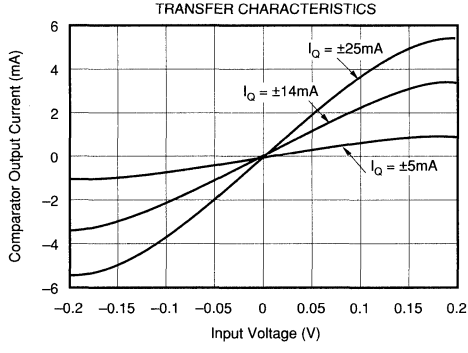
INPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



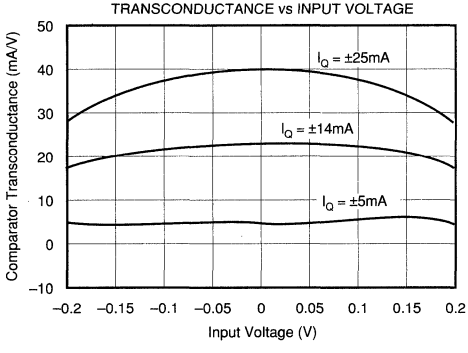
TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT



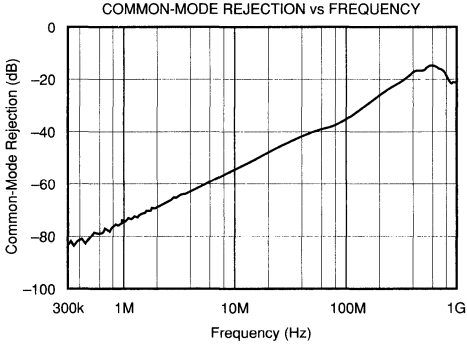
TRANSFER CHARACTERISTICS



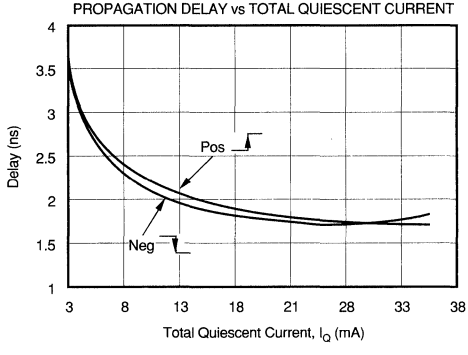
TRANSCONDUCTANCE vs INPUT VOLTAGE



COMMON-MODE REJECTION vs FREQUENCY



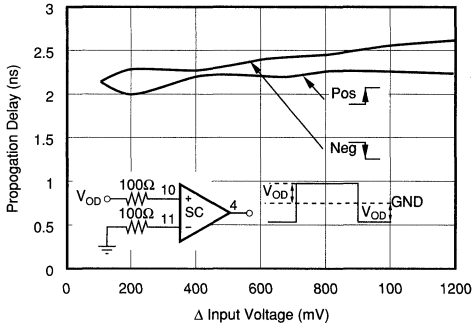
PROPAGATION DELAY vs TOTAL QUIESCENT CURRENT



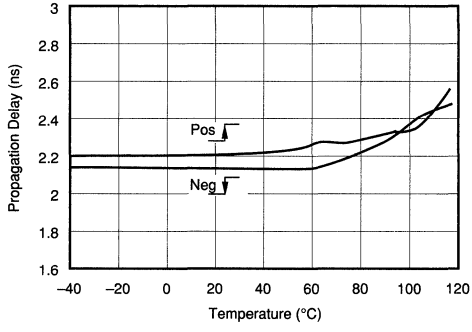
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

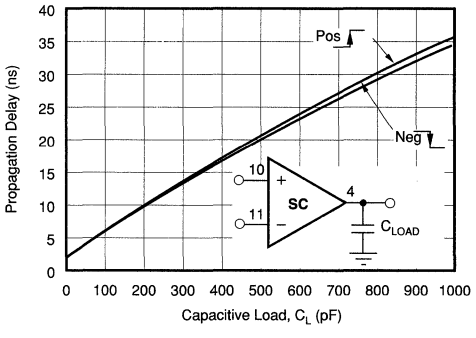
PROPAGATION DELAY vs OVERDRIVE



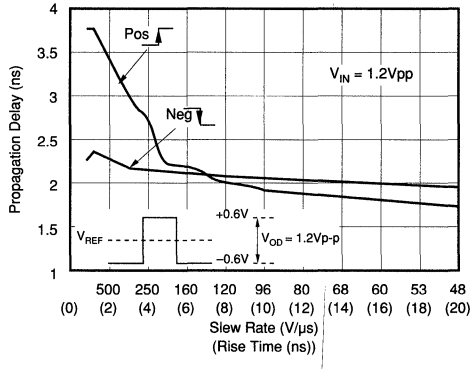
PROPAGATION DELAY TIME vs TEMPERATURE



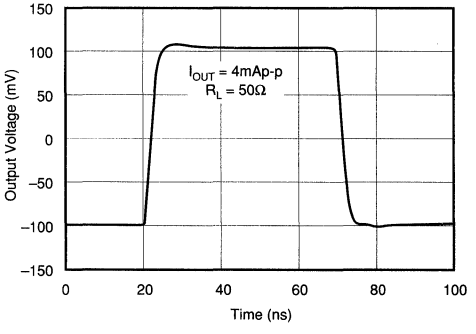
PROPAGATION DELAY vs LOAD CAPACITANCE



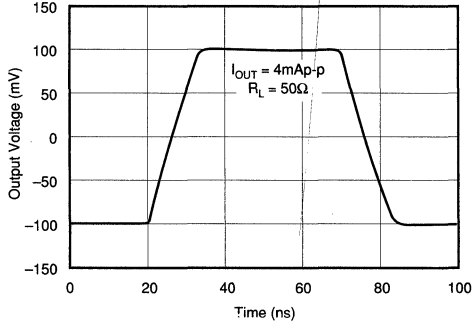
PROPAGATION DELAY vs SLEW RATE



COMPARATOR RESPONSE TO A 2ns ANALOG INPUT PULSE



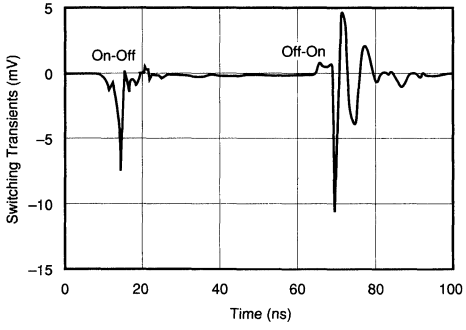
COMPARATOR RESPONSE TO A 10ns ANALOG INPUT PULSE



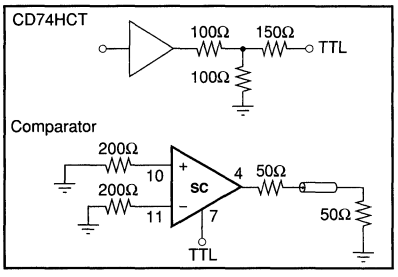
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

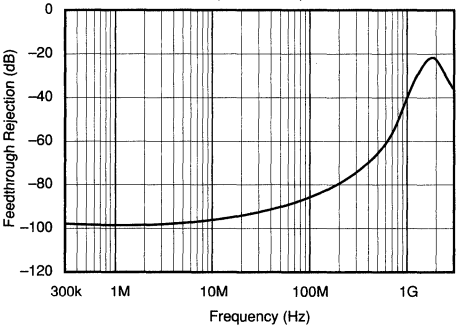
SWITCHING TRANSIENTS



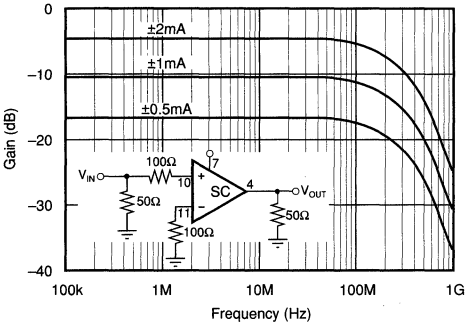
SWITCHING TRANSIENTS TEST CIRCUITS



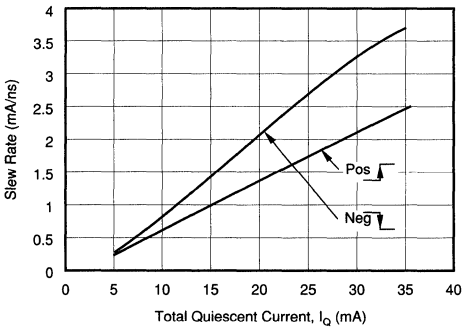
FEEDTHROUGH REJECTION vs FREQUENCY
(Off-Isolation)



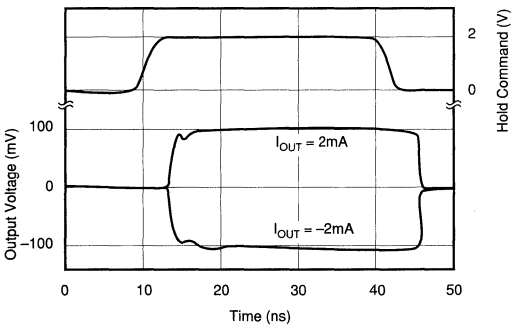
BANDWIDTH vs OUTPUT CURRENT SWING



SLEW RATE vs TOTAL QUIESCENT CURRENT



HOLD COMMAND DELAY TIME



DISCUSSION OF PERFORMANCE

The SHC615, which contains a wideband Operational Transconductance Amplifier and a fast sampling comparator, represents a complete subsystem for very fast and precise DC restoration, offset clamping and correction to GND or to an adjustable reference voltage, and low frequency hum suppression of wideband operational or buffer amplifiers.

Although the IC was designed to improve or stabilize the performance of complex, wideband video signals, it can also be used as a sample and hold amplifier, high-speed integrator, peak detector for nanosecond pulses, or demodulator or modulator for pulse code transmission systems. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and a fast and precise sampling comparator set a new standard for high-speed sampling applications.

Both can be used as stand-alone circuits or combined to create more complex signal processing stages like sample and hold amplifiers. The SHC615 simplifies the design of input amplifiers with high hum suppression, clamping or DC-restoration stages in professional broadcast equipment, high-resolution CAD monitors and information terminals, signal processing stages for the energy and peak value of small and fast nanoseconds pulses, and eases the design of high-speed data acquisition systems behind a CCD sensor or in front of an analog-to-digital converter.

An external resistor, R_Q, allows the user to set the quiescent current. R_Q is connected from Pin 1 (I_Q adjust) to $-V_{CC}$. It determines the operating currents of both the OTA and comparator sections and controls the bandwidth and AC behavior as well as the transconductance of both sections. Besides the quiescent current setting feature, the Proportional-to-Absolute-Temperature (PTAT) supply increases the quiescent current vs temperature and keeps it constant over a wide range of input voltages. This variation holds the transconductance g_m of the OTA and comparator relatively constant vs temperature. The circuit parameters listed in the specification table are measured with R_Q set to 300Ω, giving a nominal quiescent current at ±15mA. The circuit can be totally switched-off with a current flowing into Pin 1.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

SECTION AND OVERVIEW

The symbol for the OTA section is similar to that of a bipolar transistor, and the self-based OTA can be viewed as a quasi-ideal transistor or as a voltage-controlled current source. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor, also, is a voltage-controlled current source. Like a transistor, it has three terminals: a high-impedance input (base) optimized for a low input bias current of 0.3µA, a low-impedance input/output (emitter), and the high-impedance current output (collector).

The OTA consists of a complementary buffer amplifier and a subsequent complementary current mirror. The buffer amplifier features a Darlington output stage and the current mirror has a cascoded output. The addition of this cascode circuitry increases the current source output resistance to 1MΩ and the open-loop gain to typically 96dB. Both features improve the OTAs linearity and drive capabilities. Any bipolar input voltage at the high impedance base has the same polarity and signal level at the low impedance buffer or emitter output. For the open-loop diagrams the emitter is connected to GND and then the collector current is determined by the product voltage between base and emitter times the transconductance. In application circuits (Figure 2b.), a resistor R_E between emitter and GND is used to set the OTA transfer characteristics. The following formulas describe the most important relationships. r_E is the output impedance of the buffer amplifier (emitter) or the reciprocal of the OTA transconductance. Above ±5mA, collector current, I_C, will be slightly less than indicated by the formula.

$$I_C = \frac{V_{IN}}{r_E + R_E} \qquad R_E = \frac{V_{IN}}{I_C} - r_E$$

The R_E resistor may be bypassed by a relatively large capacitor to maintain high AC gain. The parallel combination of R_E and this large capacitor form a high pass filter enhancing the high frequency gain. Other cases may require a RC compensation network parallel to R_E to optimize the high-frequency response. The full power bandwidth measured at the emitter achieves 620MHz. The frequency response of the collector is directly related to the resistor's value between collector and GND; it decreases with increasing resistor values, because it forms a low-pass network with the OTA C-output capacitance.

Figure 1 shows a simplified block and circuit diagram of the SHC615 OTA. Both the emitter and the collector outputs offer a drive capability of ±20mA for driving low impedance lines or inputs. Connecting the collector to the emitter in a direct-feedback buffer configuration increases the drive capability to ±40mA. The emitter output is not current-limited or protected. Momentary shorts to GND should be avoided, but are unlikely to cause permanent damage.

While the OTA's function and labeling looks similar to that of transistors, it offers essential distinctive differences and improvements: 1) The collector current flows out of the C terminal for a positive B-to-E input voltage and into it for negative voltages; 2) A common emitter amplifier operates in non-inverting mode while the common base operates in inverting mode; 3) The OTA is far more linear than a bipolar transistor; 4) The transconductance can be adjusted with an external resistor; 5) Due to the PTAT biasing characteristic the quiescent current increases as shown in the typical performance curve vs temperature and keeps the AC performance constant; 6) The OTA is self-biased and bipolar; and, 7) The output current is zero for zero differential input voltages. AC inputs centered at zero produce an output current centered at zero.

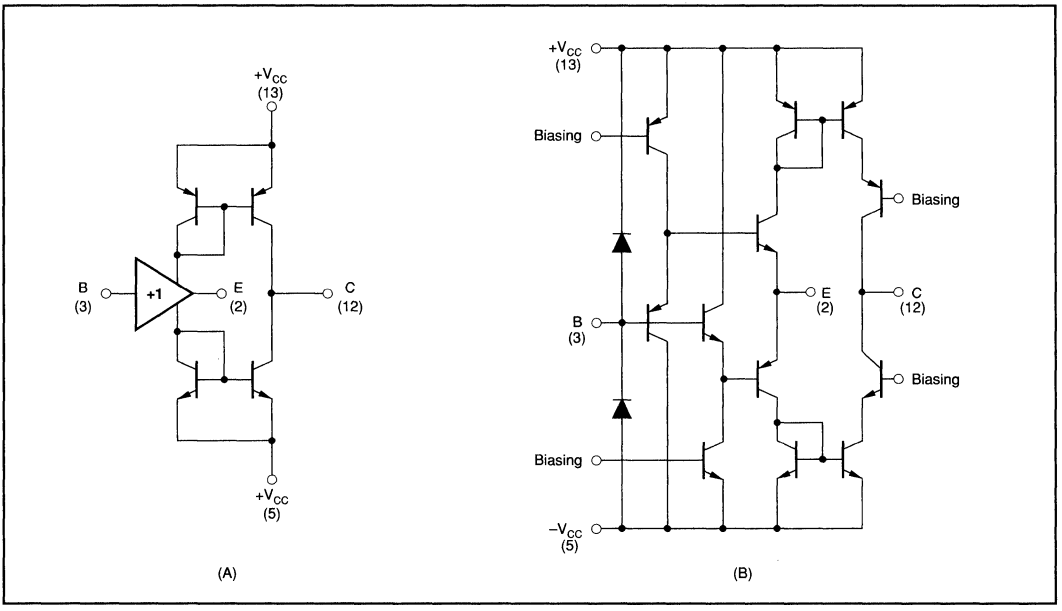


FIGURE 1. a) Simplified Block; and, b) Circuit Diagram of the OTA Section.

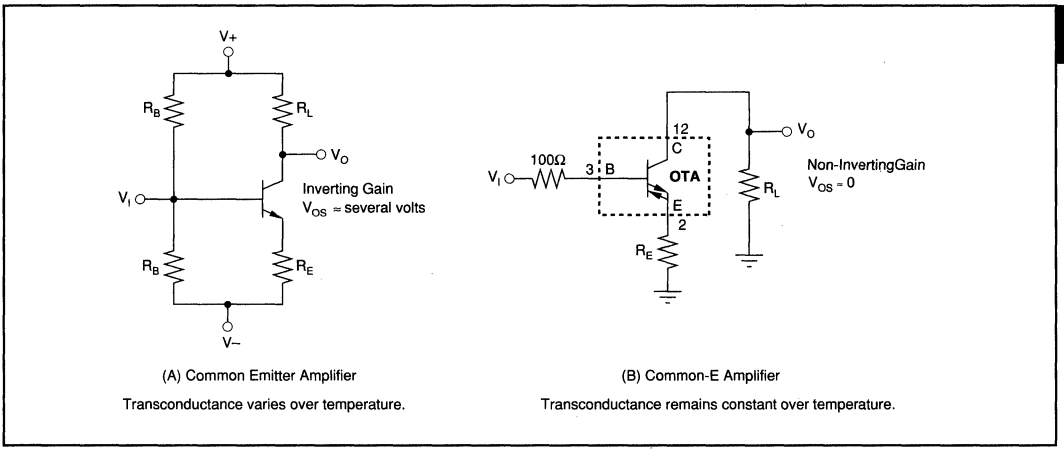


FIGURE 2. a) Common Emitter Amplifier Using a Discrete Transistor; b) Common-E Amplifier Using the OTA Portion of the SHC615.

BASIC APPLICATIONS CIRCUITS

Most application circuits for the OTA section consist of a few basic types which are best understood by analogy to discrete transistor circuits. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C (See Figures 2, 3 and 4). Figure 2 shows the OTA connected as a Common-E amplifier which is equivalent to a common emitter transistor amplifier. Input and output can be ground referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting.

Figure 4 shows the common-B amplifier. This configuration produces an inverting gain, and the input is low-impedance. When a high impedance input is needed, it can be created by inserting a buffer amplifier like BUF600 in series.

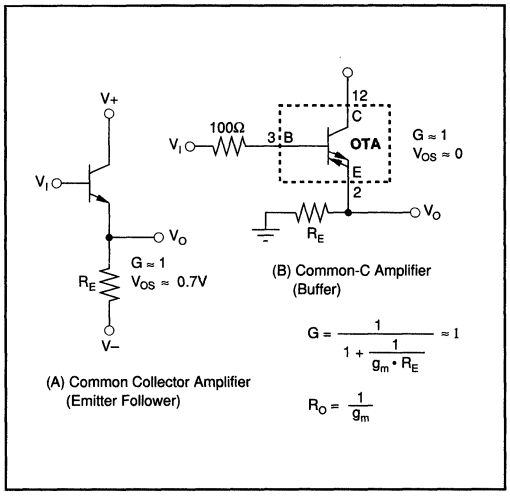


FIGURE 3. a) Common Collector Amplifier Using a Discrete Transistor; b) Common-C Amplifier Using the OTA Portion of the SHC615.

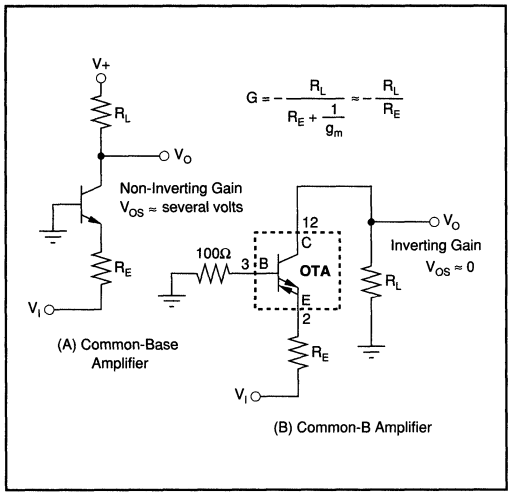


FIGURE 4. a) Common Base Amplifier Using a Discrete Transistor; b) Common-B Amplifier Using the OTA Portion of the SHC615.

SAMPLING COMPARATOR

The SHC615 sampling comparator features a very short 2.2ns propagation delay and utilizes a new switching circuit architecture to achieve excellent speed and precision.

It provides high impedance inverting and non-inverting inputs, a high-impedance current source output and a TTL-CMOS-compatible Hold Control Input.

The sampling comparator consists of an operational transconductance amplifier (OTA), a buffer amplifier, and a subsequent switching circuit. The OTA and buffer amplifier are directly tied together at the buffer outputs to provide the two identical high-impedance inputs and high open-loop transconductance. Even a small differential input voltage multiplied with the high transconductance results in an output current—positive or negative—depending upon the input polarity. This is similar to the low or high status of a conventional comparator. The current source output features high output impedance, output bias compensation, and is optimized for charging a capacitor in DC restoration, nanosecond integrators, peak detectors and S/H circuits. The typical comparator output current is ±3.2mA and the output bias current is minimized to typically ±10µA in the sampling mode.

This innovative circuit achieves the slew rate representatives of an open-loop design. In addition, the acquisition slew current for a hold or storage capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

The switching circuits in the SHC615 use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, reduced power supply and analog switching noise. Sample-to-hold peak switching is 40fC.

The additional offset voltage or switching transient induced on a capacitor at the current source output by the switching charge can be determined by the following formula:

$$\text{Offset(V)} = \frac{\text{Charge(pC)}}{C_H\ \text{Total(pF)}}$$

The switching stage input is insensitive to the low slew rate performance of the hold control command and compatible with TTL/CMOS logic levels. With a TTL logic high, the comparator is active, comparing the two input voltages and varying the output current accordingly. With a TTL logic low, the comparator output is switched off.

APPLICATION INFORMATION

The SHC615 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the SHC615 are protected with internal diode clamps as shown in Figure 1. These protection diodes can safely conduct 10mA continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V, the input signal current must be limited.

BASIC CONNECTIONS

Figure 6 shows the basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See "Circuit Layout" at the end of the applications discussion for further suggestions on layout.

If the high speed TTL-hold command signal goes negative due to reflections for AC-coupling, the hold control input must be protected by an external reverse bias diode to ground as shown in Figure 6.

CIRCUIT LAYOUT

The high-frequency performance of the SHC615 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute requirements. Oscillations, ringing, poor bandwidth, poor settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF); parallel 470pF and/or 10nF ceramic chip capacitors may be added if desired. Surface mount types are recommended because of their low lead inductance. Supply bypassing is extremely critical at high frequencies and when driving high current loads.
- PC board traces for power lines should be wide to reduce impedance.

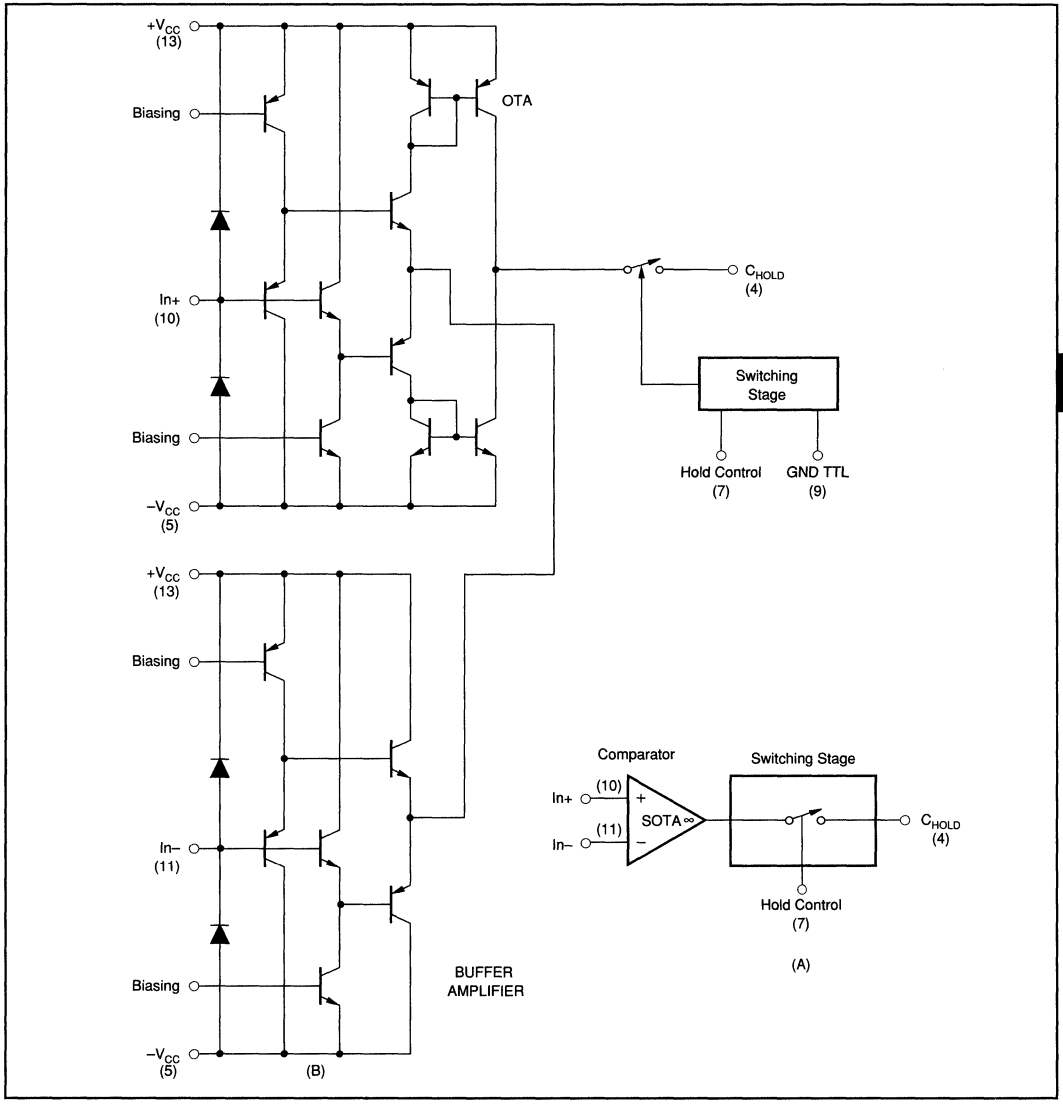


FIGURE 5. a) Simplified Block Diagram; and, b) Circuit Diagram of the Sampling Comparator which Includes the Sampling Operational Transconductance Amplifier (SOTA) and the Switching Stage.

- Make short, low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that a low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input terminals.
- Sockets are not recommended since they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile sockets.
- Use low-inductance, surface-mount components. Surface-mount components offer the best AC performance.
- A resistor of 100 to 250Ω in series with the high-impedance inputs is recommended to reduce peaking.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Terminate transmission line loads. Unterminated lines, such as box cables, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.
- Protect the hold control input with an external diode if necessary.

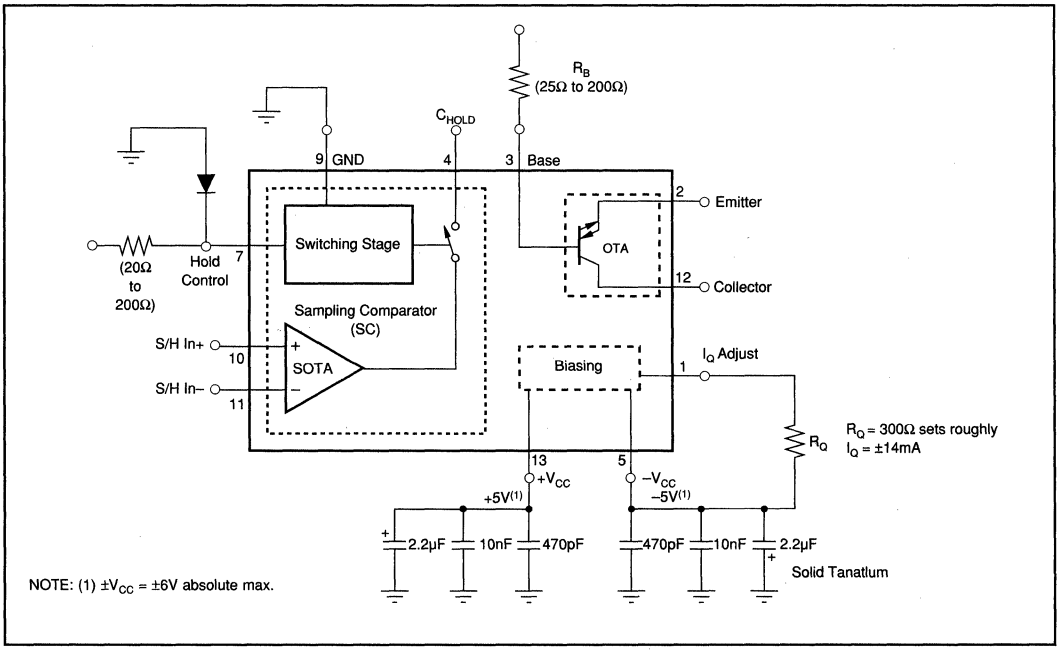


FIGURE 6. Basic Connections.

TYPICAL APPLICATIONS

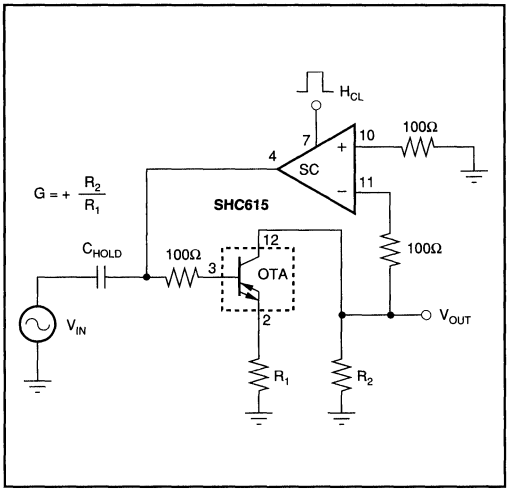


FIGURE 7. Complete DC Restoration System.

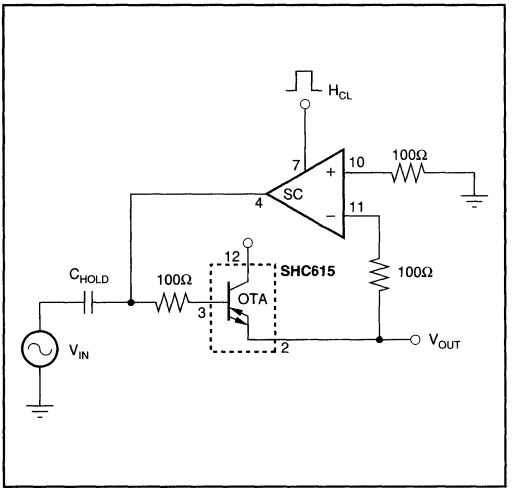


FIGURE 8. DC Restoration of a Buffer Amplifier.

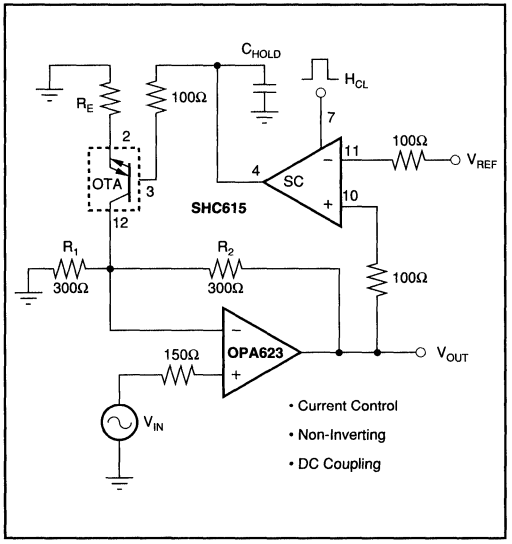


FIGURE 9. Clamped Video/RF Amplifier.

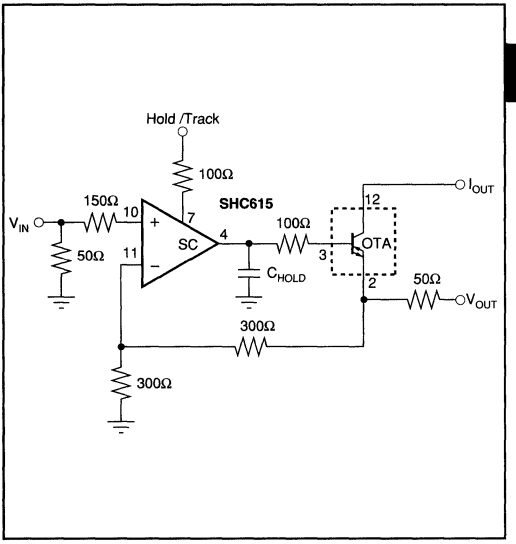


FIGURE 10. Sample/Hold Amplifier.

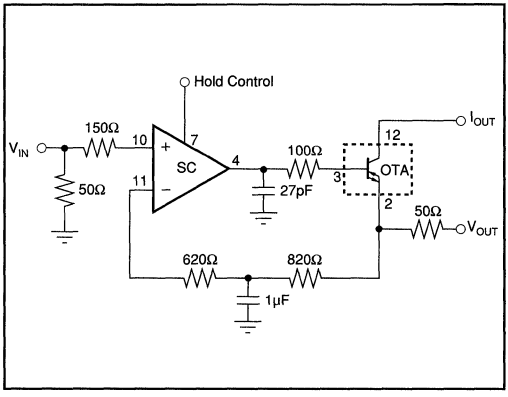


FIGURE 11. Integrator for ns-Pulses.

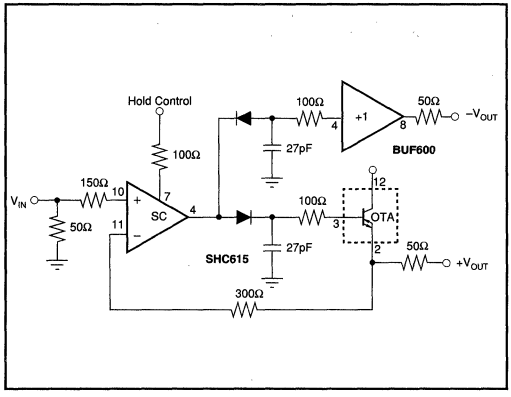


FIGURE 12. Fast Pulse Peak Detector.

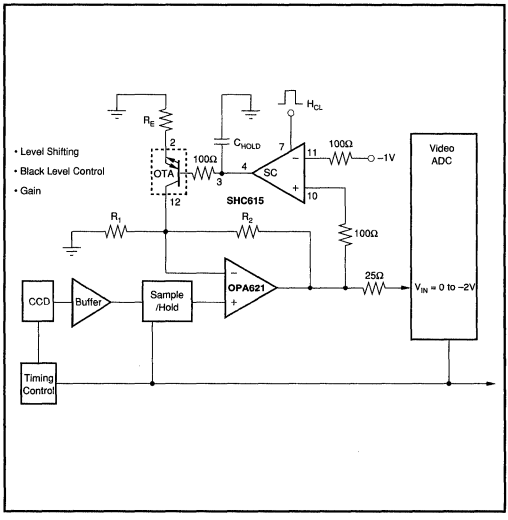


FIGURE 13. CCD Analog Front-End.

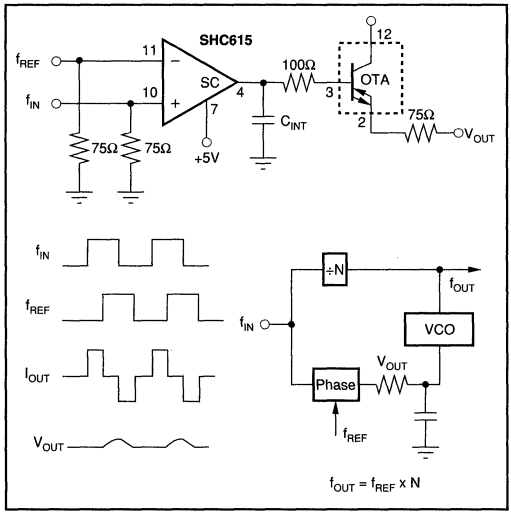
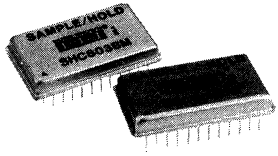


FIGURE 14. Phase Detector For Fast PLL-Systems.

BURR - BROWN®



SHC803BM, CM
SHC804BM, CM

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10512

High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- **350ns max ACQUISITION TIME**
- **±0.01% THROUGHPUT NONLINEARITY**
- **150ns max SAMPLE-TO-HOLD SETTLING TIME**
- **INPUT BUFFER (SHC803)**
- **24-PIN HERMETICALLY-SEALED METAL PACKAGE**

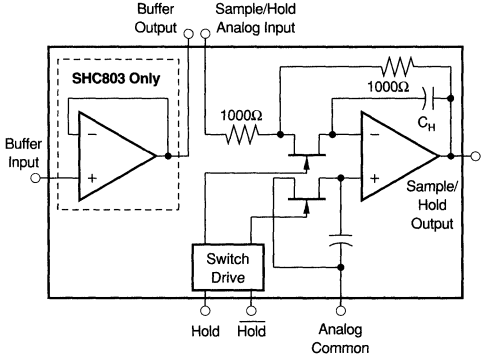
DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350ns to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the –25 to +85°C temperature range.

The ±25ps maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/µs. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is –25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.



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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM MIN	SHC803/SHC804BM TYP	SHC803/SHC804BM MAX	SHC803/SHC804CM MIN	SHC803/SHC804CM TYP	SHC803/SHC804CM MAX	UNITS
SAMPLE/HOLD INPUTS (without Input Buffer)							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL (HOLD, $\overline{HOLD}$)							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	µA
I_{IL}, V_{IN} = +0.4V			–1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS (without Input Buffer)							
ACCURACY							
Sample Mode							
Gain		–1			*		V/V
Gain Error			±0.1			*	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		*	*	% of FSR[1]
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		*	*	µV/µs
+85°C			±0.5			±0.1	mV/µs
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity[2]: ±V_{CC}			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V Step)							
to within: ±0.1% (±10mV)		220			*		ns
±0.01% (±1mV)		250	350		*	*	ns
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		*	*	ns
Sample-to-Hold Transient Amplitude		60	150		*	*	mV_{PEAK}
Aperture Delay TIme[3]		15	25		*	*	ns
Aperture Uncertainty		±10	±25		*	*	ps
Sample Mode: Output Slew Rate		160			*		V/µs
Full Power Bandwidth		1			*		MHz
Small Signal Bandwidth		16			*		MHz
Hold Mode Feedthrough Rejection							
(10V Square Wave Input)	±0.03	±0.005			*		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common			*		
Output Impedance (at DC)		0.01	0.1		*	*	Ω
INPUT BUFFER CHARACTERISTICS (SHC803 only)							
INPUT							
Offset Voltage		±1/2	±5		*	*	mV
vs Temperature		±1.5	±2.5		*	*	ppm of FSR/°C
Bias Current			±25			*	nA
Impedance		10^8 || 5			*		Ω || pF
V_{IN} Range	±10.25	±11		*	*		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320			*		kHz
Slew Rate[4]		10			*		V/µs
Settling Time[4] to ±2mV for 10V Step		2.5			*		µs
OUTPUT							
V_{OUT} Range	±10.25			*			V
Output Current	±10.25			*			mA

SPECIFICATIONS (CONT)

ELECTRICAL

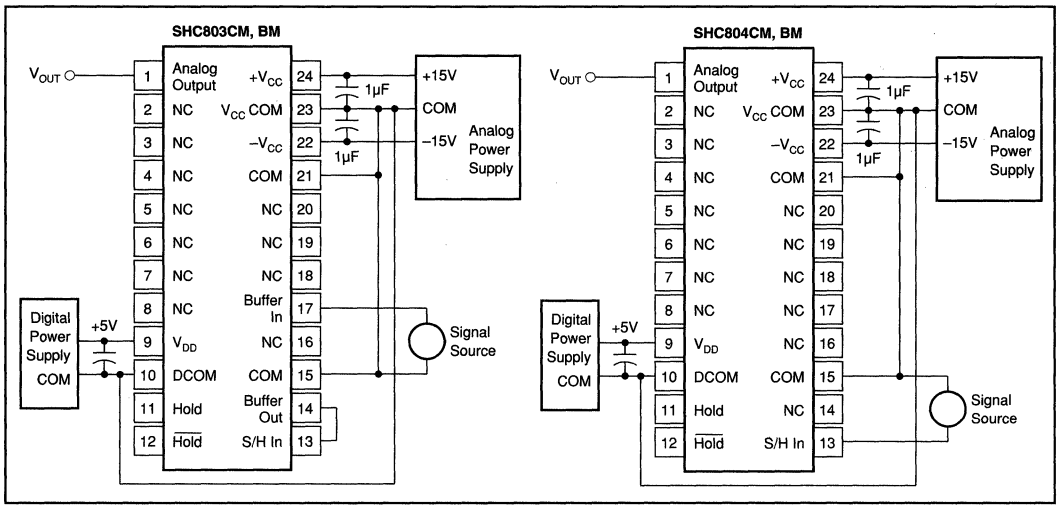
At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM			SHC803/SHC804CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Rated Voltage: $\pm V_{CC}$	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (No Load)							
SHC804: $+V_{CC}$		30	35		*	*	mA
$-V_{CC}$		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: $+V_{CC}$		33	40		*	*	mA
$-V_{CC}$		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	–25		+85	*		*	°C
Storage	–55		+125	*		*	°C

* Specification same as SHC803/SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804. (2) Sensitivity of offset plus charge offset. (3) With respect to HOLD. For $\overline{\text{HOLD}}$ add 5ns typical. (4) With buffer connected to the sample/hold amplifier.

CONNECTION DIAGRAMS



PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{HOLD}$	Logic "0" = HOLD
13	S/H In	SHC804 input; for SHC803 connect pin 13 to pin 14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal common
22	$-V_{CC}$	–15V supply
23	V_{CC} COM	Analog to power common, connected to case
24	$+V_{CC}$	+15V supply

ABSOLUTE MAXIMUM RATINGS

Input Overvoltage	±15V
$+V_{CC}$ to V_{CC} COMMON	0 to +18V
$-V_{CC}$ to V_{CC} COMMON	0 to –18V
Voltage on Digital Inputs (pins 11 and 12)	–0.5V to +7V
Power Dissipation	1500mW
V_{DD} to DCOM	–0.5V
Analog Output	Indefinite Short to V_{CC} COM

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC803BM	24-Pin	113
SHC803CM	24-Pin	113
SHC804BM	24-Pin	113
SHC804CM	24-Pin	113

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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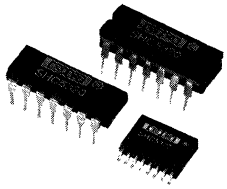


SHC5320

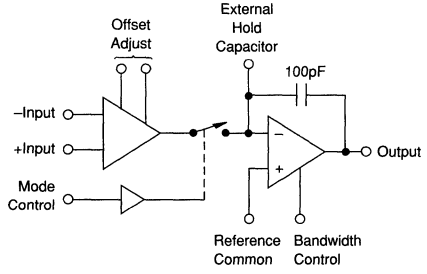
High-Speed Bipolar Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- ACQUISITION TIME TO 0.01%: 1.5µs max
- HOLD MODE SETTLING TIME: 350ns max
- DROOP RATE AT +25°C: 0.5µV/µs max
- TTL COMPATIBLE
- FULL DIFFERENTIAL INPUTS
- INTERNAL HOLDING CAPACITOR
- TWO TEMPERATURE RANGES:
  –40°C to +85°C (KH, KP, KU)
  –55°C to +125°C (SH)
- PACKAGE OPTIONS: 14-pin Ceramic, Plastic DIP, and 16-pin SOIC

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- DIGITAL-TO-ANALOG CONVERTER DEGLITCHER
- AUTO ZERO CIRCUITS
- PEAK DETECTORS



DESCRIPTION

The SHC5320 is a bipolar monolithic sample/hold circuit designed for use in precision high-speed data acquisition applications.

The circuit employs an input transconductance amplifier capable of providing large amounts of charging current to the holding capacitor, thus enabling fast acquisition times. It also incorporates a low leakage analog switch and an output integrating amplifier with input bias current optimized to assure low droop rates. Since the analog switch always drives into a load at virtual ground, charge injection into the holding capacitor is constant over the entire input voltage range. As a result, the charge offset (pedestal voltage) resulting from this charge injection can be adjusted to zero by use of the offset adjustment capability. The device includes an internal holding capacitor to simplify ease of application; however, provision is also made to add additional external capacitance to improve the output voltage droop rate.

The SHC5320 is manufactured using a dielectric isolation process which minimizes stray capacitance (enabling higher-speed operation), and eliminates latch-up associated with substrate SCRs. The SHC5320KH, KP, and KU feature fully specified operation over the extended industrial temperature range of –40°C to +85°C, while the SHC5320SH operates over the temperature range of –55°C to +125°C. The device requires ±15V supplies for operation, and is packaged in a reliable 14-pin ceramic or plastic dual-in-line package, as well as a 16-pin surface-mount plastic package.

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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

PARAMETERS	SHC5320KH, KP, KU MIN	SHC5320KH, KP, KU TYP	SHC5320KH, KP, KU MAX	SHC5320SH MIN	SHC5320SH TYP	SHC5320SH MAX	UNITS
INPUT CHARACTERISTICS							
ANALOG							
Voltage Range	±10			*			V
Common-Mode Range	±10			*			V
Input Resistance	1	5		*	*		MΩ
Input Capacitance			3			*	pF
Bias Current		±100	±300		±70	±200	nA
Bias Current Over Temperature Range			±300			±200	nA
Offset Current		±30	±300		*	±100	nA
Offset Current Over Temperature Range			±300			±100	nA
DIGITAL (Over Temperature Range)							
V_{IH} (Logic "1")	2.0			*			V
V_{IL} (Logic "0")			0.8			*	V
I_{IH} (V_I = +5V)			0.1			*	µA
I_{IL} (V_I = 0V)			4			*	µA
Logic "0" = SAMPLE							
Logic "1" = HOLD							
OUTPUT CHARACTERISTICS							
Voltage Range	±10			*			V
Current	±10			*			mA
Output Impedance (Hold Mode)		1			*		Ω
Noise, DC to 10MHz: Sample Hold		125	200		*	*	µVrms
Hold Mode		125	200		*	*	µVrms
DC ACCURACY/STABILITY							
Gain, Open Loop, DC	3 x 10^5	2 x 10^6		10^6	*		V/V
Input Offset Voltage		±0.5			±0.2		mV
Input Offset Voltage Over Temperature Range			±1.5			±2	mV
Input Offset Voltage Drift		±5	±20		*	±15	µV/°C
CMRR[1]	72	90		80	*		dB
Power Supply Rejection[2]: $+V_{CC}$	80			*			dB
$-V_{CC}$	65			*			dB
HOLD-TO-SAMPLE MODE DYNAMIC CHARACTERISTICS							
Acquisition Time, A = –1, 10V Step[3]:							
to ±0.01%		1	1.5		*	*	µs
to ±0.1%		0.8	1.2		*	*	µs
SAMPLE MODE							
Gain-Bandwidth Product (Gain = +1)[4]:							
C_H = 100pF		2			*		MHz
C_H = 1000pF		180			*		kHz
Full Power Bandwidth[5]		600			*		kHz
Slew Rate[6]		45			*		V/µs
Rise Time[4]		100			*		ns
Overshoot[4]		15			*		%
SAMPLE-TO-HOLD MODE DYNAMIC CHARACTERISTICS							
Aperture Time[7]		25			*		ns
Effective Aperture Time	–50	–25	0	*	*	*	ns
Aperture Uncertainty (Aperture Jitter)		0.3			*		ns
Charge Offset (Pedestal)[8] (Adjustable to Zero)		1	5		*	*	mV
Charge Transfer[8]		0.1	0.5		*	*	pC
Sample-to-Hold Transient Settling Time to ±0.01% of FSR		165	350		*	*	ns
HOLD MODE							
Droop[9]		0.08	0.5		*	*	µV/µs
Droop at Maximum Temperature[9]		1.2	100		17	*	µV/µs
Drift Current[9]		8	50		*	*	pA
Drift Current at Maximum Temperature[9]		0.12	10		1.7	*	nA
Feedthrough, 10Vp-p, 100kHz Sinewave		2			*		mV

SPECIFICATIONS (CONT)

ELECTRICAL

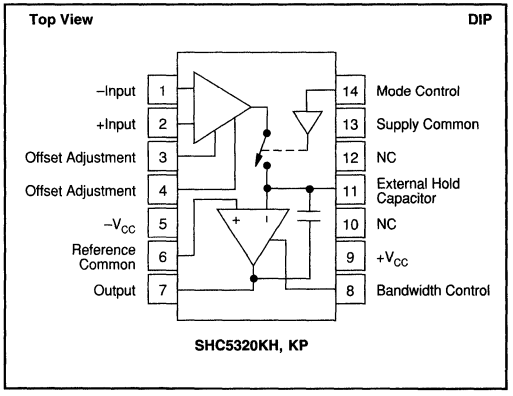
At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted.

PARAMETERS	SHC5320KH, KP, KU			SHC5320SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES							
$+V_{CC}$	+12	+15	+18	*	*	*	V
$-V_{CC}$	–12	–15	–18	*	*	*	V
$+I_{CC}$ ($+V_{CC}$ = 15V)[9]		11	13		*	*	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)[9]		–11	–13		*	*	mA
TEMPERATURE							
Specification	–40		+85	–55		+125	°C
Storage	–65		+150	*		*	°C
PACKAGE	Hermetic Ceramic, Plastic DIP, SOIC			Hermetic Ceramic			

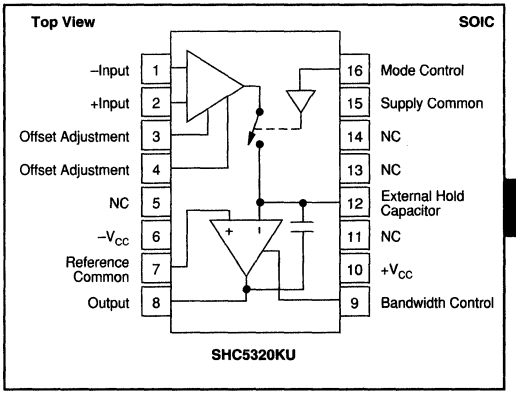
*Specification same as grade to the left.

NOTES: (1) V_{CM} = ±5VDC. (2) Based on a ±0.5V swing for each supply with all other supplies held constant. (3) V_O = 10V step, R_L = 2kΩ, C_L = 50pF. (4) V_O = 200mVp-p, R_L = 2kΩ, C_L = 50pF. (5) V_{IN} = 20Vp-p, R_L = 2kΩ, C_L = 50pF, unattenuated output. (6) V_O = 20V step, R_L = 2kΩ, C_L = 50pF. (7) Simulated only, not tested. (8) V_{IN} = 0V, V_{IH} = +3.5V, t_R <20ns (V_{IL} to V_{IH}). (9) Specified for zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA average at 20V differential.

PIN CONNECTIONS



SHC5320KH, KP



SHC5320KU

ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals	40V
Input Voltage	Actual Supply Voltage
Differential Input Voltage	±24V
Digital Input Voltage	+15V, –1V
Output Current, continuous[2]	±20mA
Internal Power Dissipation	450mW
Storage Temperature Range	$-65°C < T_A < +150°C$
Output Short-Circuit Duration[3]	None
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Absolute maximum ratings apply to both dice and package parts, unless otherwise noted. (2) Internal power dissipation may limit output current to less than +20mA. (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE
SHC5320KP	–40°C to +85°C	14-pin Plastic DIP
SHC5320KU	–40°C to +85°C	16-pin SOIC
SHC5320KH	–40°C to +85°C	14-pin Cerdip
SHC5320SH	–55°C to +125°C	14-pin Cerdip

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC5320KP	14-Pin Plastic DIP	010
SCH5320KU	16-Pin SOIC	211
SHC5320KH	14-Pin Cerdip	163
SHC5320SH	14-Pin Cerdip	163

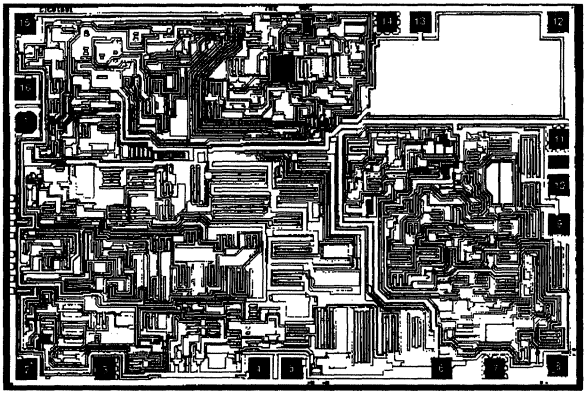
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DICE INFORMATION



SHC5320 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	–Input	9	Output
2	+Input	10	Bandwidth Control
3	NC	11	NC
4	Offset Adjustment	12	$+V_{CC}$
5	Offset Adjustment	13	External Hold Cap.
6	$-V_{CC}$	14	NC
7	NC	15	Supply Common
8	Reference Common	16	Mode Control

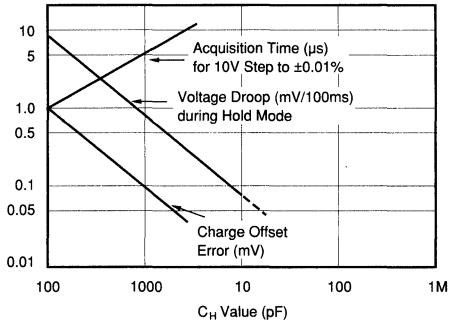
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	140 x 95	3.56 x 2.41
Die Thickness	18 ±0.8	0.45 ±0.02
Min. Pad Size	5 x 5	0.127 x 0.127

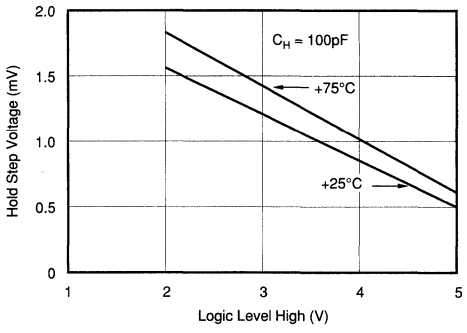
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = 15V.

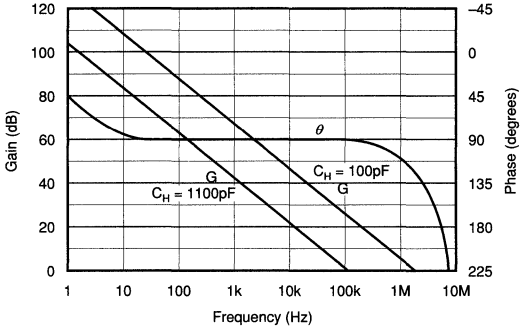
TYPICAL SAMPLE/HOLD PERFORMANCE
AS FUNCTION OF HOLDING CAPACITOR



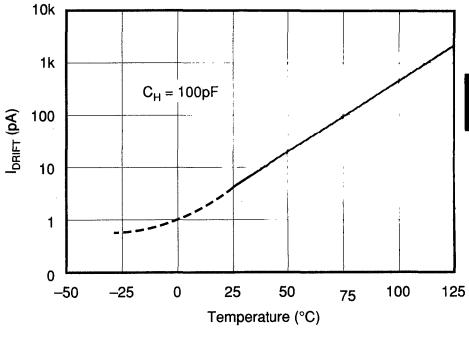
CHARGE OFFSET
vs MODE CONTROL (V_{IH}) VOLTAGE



OPEN-LOOP GAIN AND PHASE RESPONSE



DRIFT CURRENT vs TEMPERATURE



DISCUSSION OF SPECIFICATIONS

WHAT IS A SAMPLE/HOLD AMPLIFIER?

A sample/hold amplifier (also sometimes called a track-and-hold amplifier) is a circuit that captures and holds an analog voltage at a specific point in time under control of an external circuit, such as a microprocessor. This type of circuit has many applications; however, its primary use is in data acquisition systems which require that the voltage be captured and held during the analog-to-digital conversion process. Use of a sample/hold effectively increases the bandwidth of a data acquisition system by a significant amount. For further discussion of this capability, refer to "Signal Digitization" in the Applications section of this data sheet.

The ideal sample/hold amplifier in its simplest form contains four primary components as illustrated in Figure 1, although in actual practice they may not be internally connected exactly as shown. Amplifier A_1, the input buffer, provides a high impedance load to the source circuit and supplies charging current to the holding capacitor C_H. Switch S_1 opens and closes under external control to gate the buffered input signal to the holding circuit or to remove it so that the most recently sampled signal will be held. Amplifier A_2 serves to present a high impedance load to the holding capacitor and to provide a low impedance voltage source for external loads. A minimum of three terminals are provided for the user: input, output, and mode control (or sample/hold control). When S_1, is closed, the output signal follows the input signal, subject to errors imposed by amplifier bandwidth and other errors as discussed below. When S_1, is opened, the voltage stored on the holding capacitor will be held indefinitely (in the ideal case), and will appear at the output of the circuit until S_1, is again closed under command of the mode control signal.

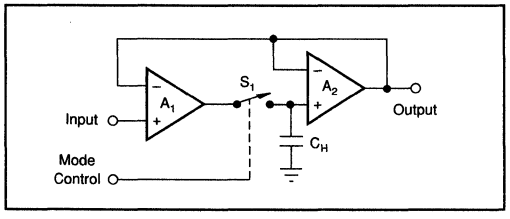


FIGURE 1. Ideal Sample/Hold Amplifier.

The following discussion of specifications covers the critical types of errors which may be experienced in applications of a sample/hold amplifier. These errors are depicted graphically in Figure 2, and in the Typical Performance Curves.

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value after the sample mode is initiated. Included in this time are effects of switch delay time, slew rate of the buffer amplifier, and settling time for a specified change in held voltage value. Slew rate limitations of the buffer amplifier will cause

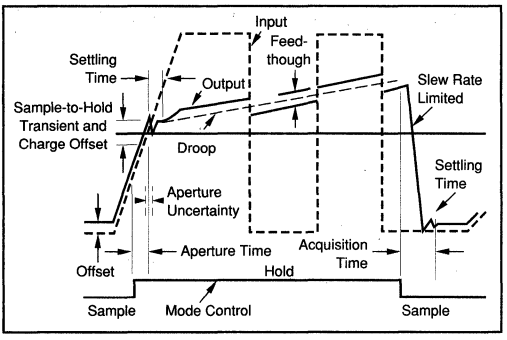


FIGURE 2. Illustration of Sample/Hold Specifications.

actual acquisition time to be highly dependent on the amplitude of the voltage to be acquired, relative to the value already held by the capacitor. Therefore, proper specification of sample/hold amplifier performance includes definition of both output value step size and required error band accuracy.

Aperture Time (or aperture delay time) is the time required for switch S_1, to open and remove the charging signal from the capacitor after the mode control signal has changed from "sample" to "hold." This time is measured from the 50% point of the Hold mode transition to the time at which the output stops tracking the input. This parameter is very important in applications for which the input signal is changing very rapidly when the Hold mode is initiated.

Effective Aperture Time is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to switch S_1. This time may be negative, zero, or positive. A negative value indicates that the mode control propagation delay is shorter than the analog propagation delay, with the result that the analog value present on the capacitor at the time the switch opens occurred earlier than the application of the mode control signal by the amount of the effective aperture delay time.

Aperture Uncertainty (or aperture jitter) is the variation observed in the aperture time over a large number of observations. This parameter is important when the analog input is a rapidly changing signal, as aperture uncertainty contributes to lack of knowledge (at the output) about the true value of the input at the precise time the Hold mode is initiated. The maximum input frequency for a given acceptable error contribution due to aperture uncertainty is

$$f_{MAX} = \text{Maximum Fractional Error}/2\pi t_U$$

where Maximum Fractional Error (MFE) is the ratio of the maximum allowable error voltage to peak voltage, and t_U is the aperture uncertainty time. For a bipolar ±10V signal and a maximum uncertainty error of 1/2LSB in a 12-bit system, the MFE is equal to 1/2LSB ÷ V_{PEAK} = 2.44mV ÷ 10V = 0.000244V/V, since 1/2LSB = 2.44mV for a 20V full-scale range.

For the same system operating with a unipolar 0V to 10V signal, MFE would be 0.000122V/V.

Charge Offset (pedestal) is the output voltage change that results from charge transfer into the hold capacitor through stray capacitance when the Hold mode command is given. This charge appears as an offset voltage at the output, and in some sample/hold amplifiers may be a function of the input voltage.

Charge offset is specified for the SHC5320 using only the internal holding capacitor. When an external capacitor is added, charge offset is calculated as Charge Transfer (pC) divided by total hold capacitance. Charge Transfer is also specified for the SHC5320, and total hold capacitance is the sum of the internal hold capacitor value (100pF) and the external hold capacitor. Since charge transfer is not a function of analog input voltage for the SHC5320, this error may be removed by means of the offset adjustment capability of the amplifier.

Droop Rate is the change in output voltage over time during the Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier. Droop rate varies with temperature and the quality of the external holding capacitor, if used. Careful circuit layout is also required to minimize droop.

Drift Current is the net leakage current affecting the hold capacitor during the Hold mode. With knowledge of the drift current, droop can be calculated as:

$$\text{Droop (V/s)} = I_D(\text{pA})/C_H(\text{pF})$$

Hold Mode Feedthrough is the fraction of the input signal which appears at the output while in the Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.

Hold Mode Settling Time is the time required for the sample-to-hold transient to settle within a specified error band.

OPERATING INSTRUCTIONS

(Developed Around 14-Pin Package)

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold modes. The offset should then be adjusted to zero output for the periods when the amplifier is in the Hold mode. In this way, the effects of both amplifier offset and charge offset will be accounted for.

SAMPLE/HOLD CONTROL

A TTL logic "0" applied to pin 14 switches the SHC5320 into the Sample (track) mode. In this mode, the device acts as an amplifier which exhibits normal operational amplifier behavior, with the relationship of output to input signal depending upon the circuit configuration selected (see the Installation section below). Application of a logic "1" to pin 14 switches the SHC5320 into the Hold mode, with the output voltage held constant at the value present when the hold command is given. Pin 14 presents less than one LSTTL load to the driving circuit throughout the full operating temperature range.

ADDITION OF AN EXTERNAL CAPACITOR

The SHC5320 contains an internal 100pF MOS holding capacitor, sufficient for most high-speed applications. If improved droop performance is desired (with increased acquisition time), additional capacitance may be added between pins 7 and 11. If an external holding capacitor C_H is used, then a noise-bandwidth capacitor with a value $0.1C_H$ should be connected from pin 8 to ground. The exact value and type of this bandwidth capacitor are not critical.

Capacitors with high insulation resistance and low dielectric absorption, *such as Teflon® or polystyrene units*, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with total hold capacitance from the values given in the specification table for the internal 100pF capacitor. The behavior of acquisition time versus total hold capacitance is shown in the Typical Performance Curves.

OUTPUT PROTECTION

In order to optimize high-frequency performance of this device, output protection is not included. This high frequency performance is mandatory for a good sample/hold, which must absorb high-frequency changes in load current when driving a successive-approximation A/D converter. Due to the lack of output protection, the output circuit will not tolerate an indefinite short to common, but a momentary short is permissible. The output should never be shorted to a supply.

INSTALLATION

(Developed Around 14-Pin Package)

LAYOUT PRECAUTIONS

Since the holding capacitor is connected to virtual ground at one end (pin 11) and to a low-impedance voltage source at the other (pin 7), the SHC5320 does not require the use of guard rings and other careful layout techniques which are required by many sample/hold circuits. However, normal good layout practice should be observed, minimizing the possibility of leakage paths across the holding capacitor. As in all digital-analog circuits, analog signal lines on the circuit board should cross digital signal paths at right angles whenever possible.

GROUNDING AND BYPASSING

Pin 6 (Reference Common) should be connected to the system analog signal common as close to the unit as possible. Likewise, pin 13 (Supply Common) should be connected to the system supply common. If the system design prevents running these two common lines separately, they should be connected together close to the unit, preferably to

Teflon® Du Pont Corporation

a large ground plane surrounding the sample/hold. Bypass capacitors (0.01µF to 0.1µF ceramic in parallel with 1µF to 10µF tantalum) should be connected from each power supply terminal of the device to pin 13 (Supply Common).

OFFSET ADJUSTMENT

Offset adjustment capability may be achieved by connecting a 10kΩ, 10-turn potentiometer as illustrated in Figure 3.

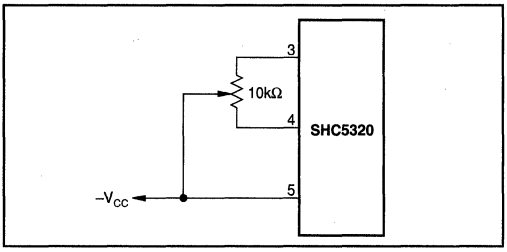


FIGURE 3. Connection of Offset Adjustment Potentiometer.

NONINVERTING MODE

The most common application of the SHC5320 will utilize the connection illustrated in Figure 4. In this mode of operation, the sample/hold will operate as a unity-gain noninverting amplifier when in the Sample mode, and the output signal will track the input. The high bandwidth of the SHC5320 and the large open-loop gain assure that gain error will be minimized.

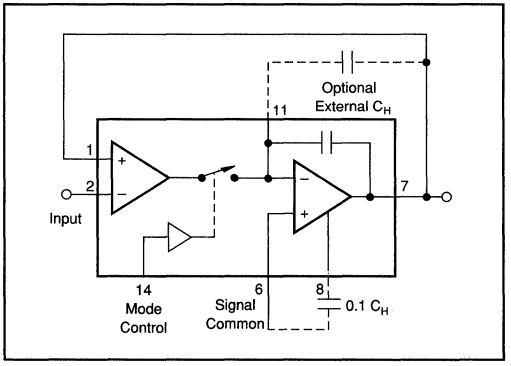


FIGURE 4. Noninverting Unity-Gain Connections.

When sampling lower-amplitude signals, the SHC5320 may also be connected as a noninverting amplifier with gain, as illustrated in Figure 5. In this circuit the gain of the amplifier is equal to $-R_2/R_1$ when sampling.

The Burr-Brown SHC5320 uses current sources to bias the internal amplifiers. This means that the bias of the amplifiers is not dependent on the common-mode voltage of the input signal. This makes the spurious free dynamic range in the non-inverting mode equal that of the inverting mode.

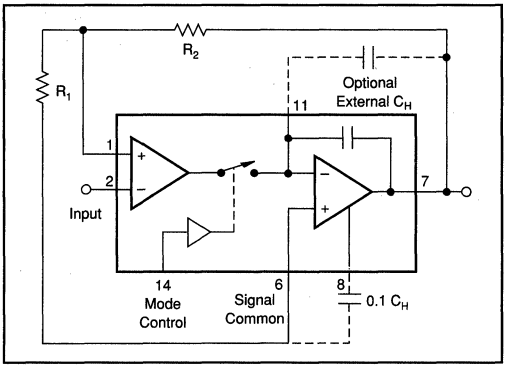


FIGURE 5. Noninverting Configuration with Gain = 1 + R_2/R_1.

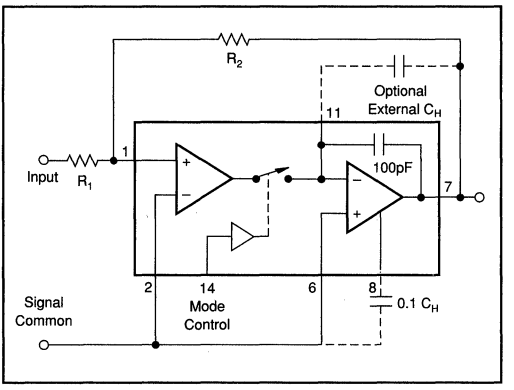


FIGURE 6. Inverting Configuration with Gain = $-(R_2/R_1)$.

INVERTING MODE

Unlike most sample/holds, the SHC5320 may also be connected to act as an inverting amplifier, as shown in Figure 6. For this configuration, the gain is equal to $-R_2/R_1$.

INPUT OVERLOAD PROTECTION

It is possible that the input transconductance amplifier of the SHC5320 will saturate when the unit is in the Hold mode, due to a non-zero differential signal appearing between pins 1 and 2. This differential signal may be the result of a rapidly changing input signal or application of a new channel from an input multiplexer. When the input buffer is saturated in this fashion, acquisition time may be degraded because of the time required for the buffer to recover from saturation. In addition, the input buffer, which is designed to provide large amounts of charging current to the output integrator, may draw large amounts of supply current which may exceed 40mA peak in some applications. For these reasons, it is desirable to limit the differential voltage which may appear at the summing junction of the input buffer. Figures 7 and 8 illustrate possible methods of providing this voltage limitation for the inverting and noninverting configurations. The

diodes may be Schottky diodes, which will provide the fastest clamping action and lowest clamping voltage, but fast signal diodes such as IN914 will also work in most applications. In each configuration the value of R_1 should be large enough to avoid excessive loading of the input signal source. Similarly, R_2 should have a value of 2kΩ or greater to insure sufficient load current capability from the sample/hold. If the value of R_2 becomes too large, however, the added capacitance of the diodes may change the sample/hold phase response enough to cause oscillation.

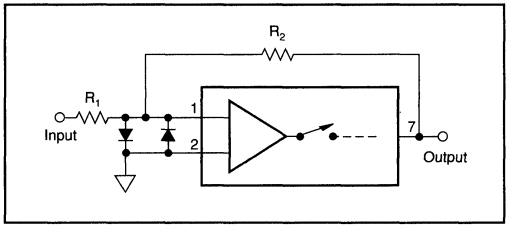


FIGURE 7. Input Overload Protection—Inverting Configuration.

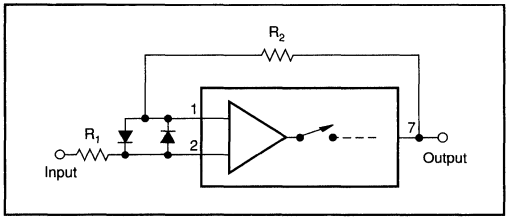


FIGURE 8. Input Overload Protection—Noninverting Configuration.

APPLICATIONS

(Developed Around 14-Pin Package)

SIGNAL DIGITIZATION

Sample/hold amplifiers are normally used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC80MAH-12 is a 12-bit successive-approximation converter with a 25µs conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during conversion.

The maximum rate of change of a sine wave of frequency, f, is dv/dt (max) = $2\pi Af(V/s)$. If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/25µs = 0.0976mV/µs. Thus the sampled sinusoidal signal frequency limit is

$$f = (0.0976 \times 10^3)/2\pi A = 15.5/A \text{ (Hz)},$$

where A is the peak amplitude of the sine wave. For a ±10V sine wave, this corresponds to a frequency of 1.6Hz, hardly acceptable for the majority of sampled data systems.

However, a sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold it at any instant in time. There is a short delay (aperture delay) between the time the hold command is asserted and the time the circuit actually holds. The hold command signal can usually be advanced in time (or delayed, in the case of negative effective aperture delay) to cause the amplifier to hold the signal actually desired.

Aperture uncertainty (also called aperture jitter) is also a key consideration. For the SHC5320 there is a 300ps period during which the signal should not change more than the amount allowed for aperture uncertainty in the system error budget, perhaps 1/2LSB for a 12-bit system. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/0.3ns = 8.13mV/ns. The equivalent input sine wave frequency is

$$f = 8.13 \times 10^6/2\pi A = 1.29/A \text{ (MHz)},$$

a factor of almost 84,000 higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC80/SHC5320 combination is 26.5µs (25µs A/D) conversion time plus 1.5µs S/H acquisition time). Sampling a sine wave at the Nyquist rate, this permits a maximum input signal frequency of 37.7kHz. The above analysis assumes that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion. Both of these assumptions are valid for the SHC5320 in this application.

DATA ACQUISITION

The SHC5320 may be used to hold data for analog-to-digital conversion or may be used to provide pulse-amplitude modulation (PAM) data output (see Figures 9 and 10).

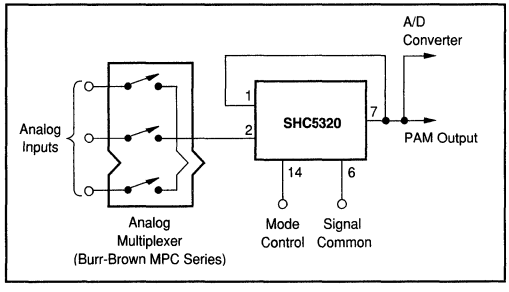


FIGURE 9. Typical Data Acquisition Configuration.

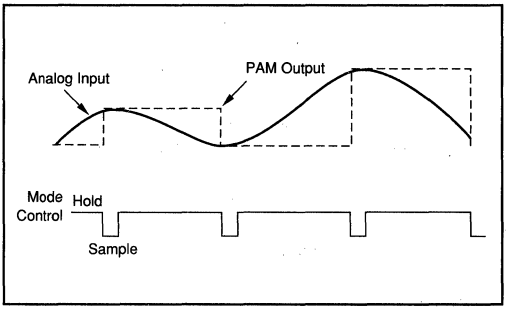


FIGURE 10. PAM Output.

DATA DISTRIBUTION

The SHC5320 may be used to hold the output of a digital-to-analog converter and distribute several different analog voltages to different loads (see Figure 11).

HIGH-SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the A/D converter. If two or more sample/holds are used with a multiplexer (such as the Burr-Brown MPC800 or MPC801) as shown in Figure 12, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched into the A/D converter, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this signal by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed. In low level systems an instrumentation amplifier (such as the Burr-Brown INA101) and a differential multiplexer (such as the Burr-Brown MPC509A or MPC507A) may be required in front of the sample/hold. The settling and acquisition times of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the total conversion time as before by operating in this overlapped mode with the sample/holds.

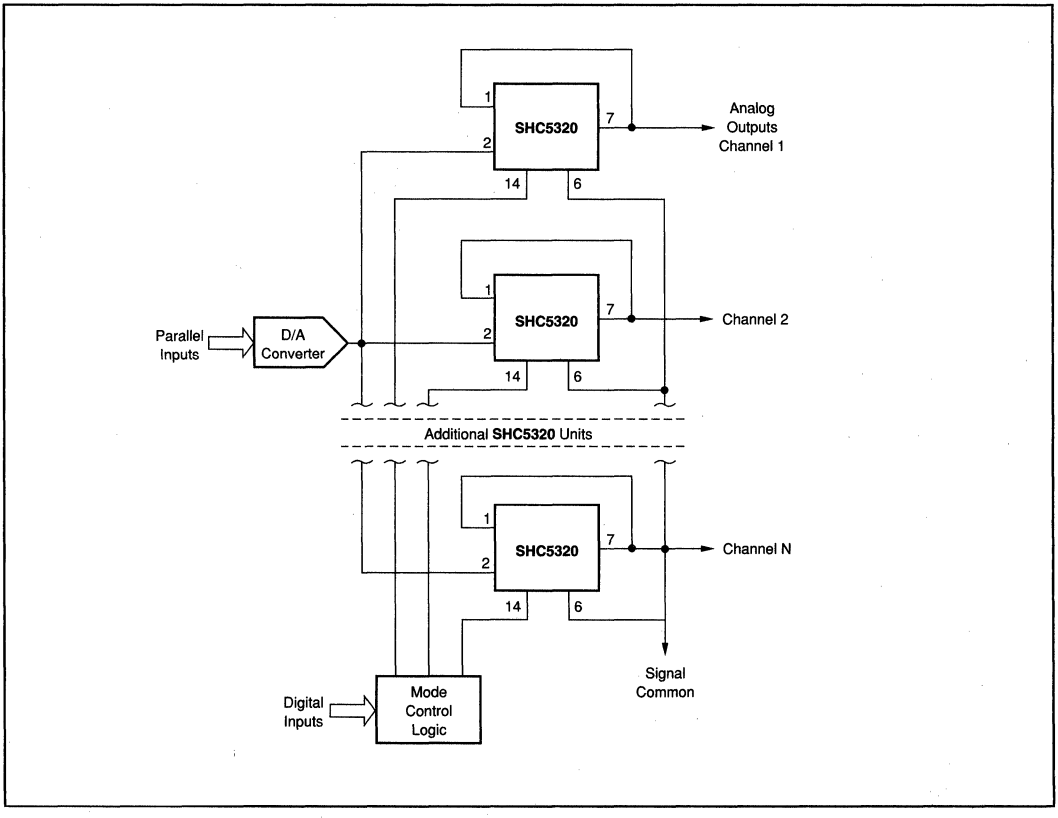


FIGURE 11. Typical Data Distribution Configuration.

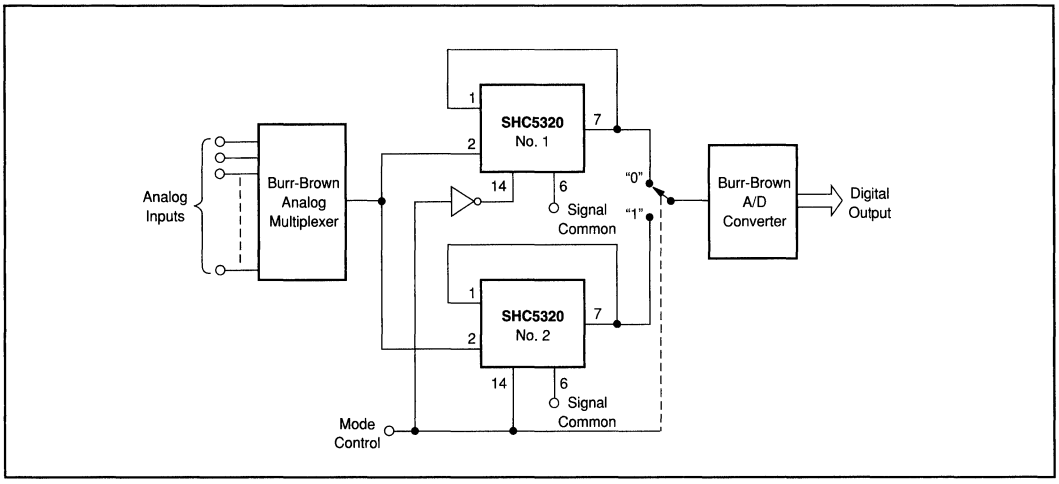


FIGURE 12. Typical Overlapped Sample/Hold Configuration.

7 Voltage-to-Frequency Converters

Voltage-to-frequency converters provide a simple, low-cost alternative to A/D converters. The frequency output is easily isolated, transmitted or recorded. It can be interfaced to many commonly used micro-controllers and processors through counter input ports or counter/timer peripheral ICs.

The voltage-to-frequency converters' integrating input properties make them ideal for high noise industrial environments. Connected in frequency-to-voltage mode, they are useful for tachometer and rate control circuitry, motor control and telemetry.

Choose from a variety of popular devices, including:

VFC32—Low cost V/F converter operates up to 500kHz.

VFC320—Operates up to 1MHz full-scale with improved accuracy for high performance A/D conversion.

VFC100, VFC101—Synchronized V/F converter up to 2MHz full-scale frequency is precisely determined by your system clock frequency. Excellent for A/D conversion.

VFC121—Operates from a single 4.5V to 36V power supply. Full-scale output frequency up to 1.5MHz.

VFC110—High performance V/F converter operates to 4MHz with low frequency jitter.

Other products provide special features and performance. Use our selection guide below to locate the V/F converter for your application.

VOLTAGE-TO-FREQUENCY CONVERTERS

ASYNCHRONOUS
VFC32 (Low Cost)
VFC320 (0.005% Linearity)
VFC110 (4MHz)
VFC121 (Single Supply)

SYNCHRONIZED
VFC100 (4MHz Clock)

* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

Product	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Temp Range[1]	Pkg	Description
VFC32	User-selected 500kHz, max	User-selected	±0.01 at 10kHz ±0.05 at 100kHz	Com Ind, Mil	DIP, SOIC TO-100	Low-Cost Monolithic
VFC100	Clock-Programmed 2MHz max	0 to +10	0.1 at 1MHz	Ind, Mil	DIP	Synchronized Monolithic
VFC110	User-selected 4MHz max	0 to +10	±0.05 at 1MHz	Ind	DIP	High-Performance
VFC121	User-selected 1.5MHz max	User-selected	±0.03 at 100kHz	Ind	DIP	Single Supply, Low Power
VFC320	User-selected 1MHz max	User-selected	±0.002 at 10kHz	Ind, Mil	DIP, TO-100	Precision Monolithic

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

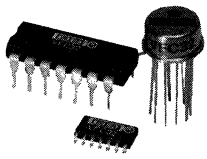
* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

BURR-BROWN®



VFC32

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10372

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- **OPERATION UP TO 500kHz**
- **EXCELLENT LINEARITY**
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- **V/F OR F/V CONVERSION**
- **MONOTONIC**
- **VOLTAGE OR CURRENT INPUT**

APPLICATIONS

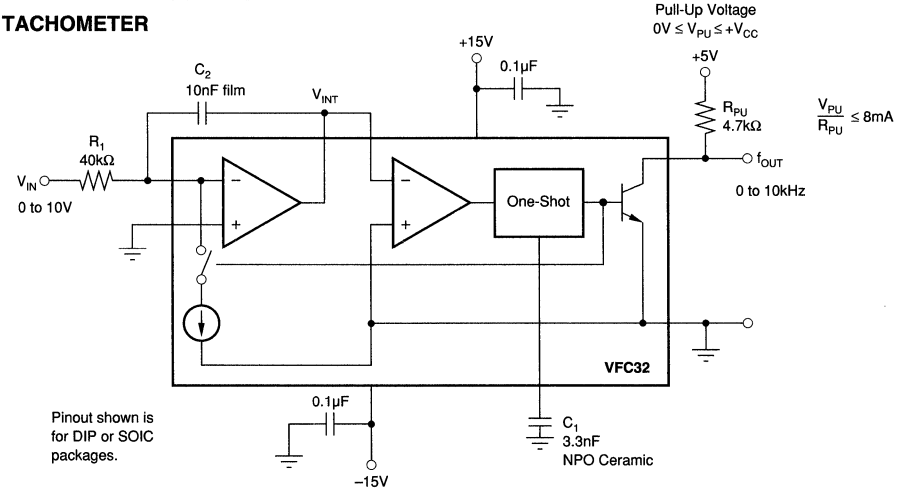
- **INTEGRATING A/D CONVERTER**
- **SERIAL FREQUENCY OUTPUT**
- **ISOLATED DATA TRANSMISSION**
- **FM ANALOG SIGNAL MOD/DEMOD**
- **MOTOR SPEED CONTROL**
- **TACHOMETER**

DESCRIPTION

The VFC32 voltage-to-frequency converter provides an output frequency accurately proportional to its input voltage. The digital open-collector frequency output is compatible with all common logic families. Its integrating input characteristics give the VFC32 excellent noise immunity and low nonlinearity.

Full-scale output frequency is determined by an external capacitor and resistor and can be scaled over a wide range. The VFC32 can also be configured as a frequency-to-voltage converter.

The VFC32 is available in 14-pin plastic DIP, SO-14 surface-mount, and metal TO-100 packages. Commercial, industrial, and military temperature range models are available.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	VFC32KP, KU MIN	VFC32KP, KU TYP	VFC32KP, KU MAX	VFC32BM MIN	VFC32BM TYP	VFC32BM MAX	VFC32SM MIN	VFC32SM TYP	VFC32SM MAX	UNITS
INPUT (V/F CONVERTER)	$F_{OUT} = V_{IN}/7.5\ R_1\ C_1$										
Voltage Range[1]											
Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		–10	*		*	*		*	V
Current Range[1]		>0		+0.25	*		*	*		*	mA
Bias Current											
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage[2]			1	4		*	*		*	*	mV
Differential Impedance		300 || 10	650 || 10		*	*		*	*	kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		*	*	MΩ || pF
INPUT (F/V CONVERTER)	$V_{OUT} = 7.5\ R_1\ C_1\ F_{IN}$										
Impedance		50 || 10	150 || 10		*	*		*	*		kΩ || pF
Logic "1"			+1.0		*		*	*		*	V
Logic "0"			–0.05		*		*	*		*	V
Pulse-width Range		0.1		150k/F_{MAX}	*		*	*		*	µs
ACCURACY											
Linearity Error[3]	0.01Hz ≤ Oper Freq ≤ 10kHz		±0.005	±0.010[4]		*	*		*	*	% of FSR[5]
	0.1Hz ≤ Oper Freq ≤ 100kHz		±0.025	±0.05		*	*		*	*	% of FSR
	0.5Hz ≤ Oper Freq ≤ 500kHz		±0.05			*			*		% of FSR
Offset Error Input Offset Votlage[2]			1	4		*	*		*	*	mV
Offset Drift[6]			±3			*			*		ppm of FSR/°C
Gain Error[2]			5			*			*		% of FSR
Gain Drift[6]	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift and gain drift)[6, 7]	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*		*	*	µA
Voltage, Logic "1"	External Pull-up Resistor Required (see Figure 4)			V_{PU}			*			*	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			*			*		s
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			*			*	ns
OUTPUT (F/V CONVERTER)	V_{OUT}										
Voltage	I_O ≤ 7mA	0 to +10			*			*			V
Current	V_O ≤ 7VDC	+10			*			*			mA
Impedance	Closed Loop			1			*			*	Ω
Capacitive Load	Without Oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500[8]	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	(V/F) to Specified Linearity for a Full Scale Input Step		[9]			*			*		
Overload Recovery	< 50% Overload		[9]			*			*		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					*		V
Quiescent Current			±5.5	±6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	–25		+85	–55		+125	°C
Operating		–25		+85	–55		+125	–55		+125	°C
Storage		–25		+85	–65		+150	–65		+150	°C

* Specification the same as VFC32KP.

NOTES: (1) A 25% duty cycle (0.25mA input current) is recommended for best linearity. (2) Adjustable to zero. See Offset and Gain Adjustment section. (3) Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C. (4) ±0.015% of FSR for negative inputs shown in Figure 5. Positive inputs are shown in Figure 1. (5) FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage). (6) Exclusive of external components' drift. (7) Positive drift is defined to be increasing frequency with increasing temperature. (8) For operations above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections. (9) One pulse of new frequency plus 1µs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, –Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range:	
VFC32BM, SM	–65°C to +150°C
VFC32KP, KU	–25°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
VFC32KP	14-Pin Plastic DIP	010
VFC32BM	TO-100 Metal	007
VFC32SM	TO-100 Metal	007
VFC32KU	SO-14 SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

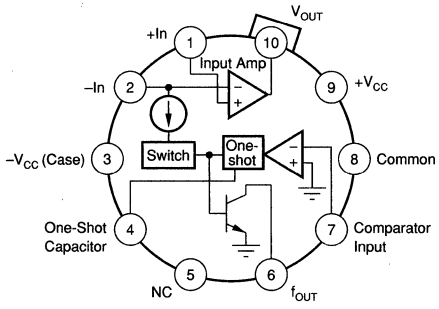
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC32KP	14-Pin Plastic DIP	0°C to 70°C
VFC32BM	TO-100 Metal	–25°C to +85°C
VFC32SM	TO-100 Metal	–55°C to +125°C
VFC32KU	SO-14 SOIC	0°C to +70°C

PIN CONFIGURATIONS

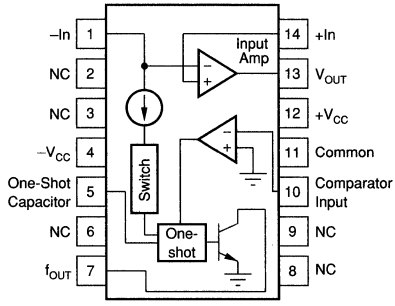
Top View

M Package
(TO-100)



NC = no internal connection
External connection permitted.

P Package
U Package
(Epoxy Dual-in-line)



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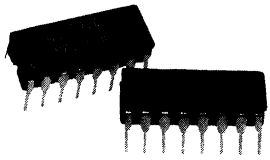


VFC100

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10547

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK; NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% max GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY:
  0.02% max at 100kHz FS
  0.1% max at 1MHz FS
- VERY LOW GAIN DRIFT: 50ppm/°C

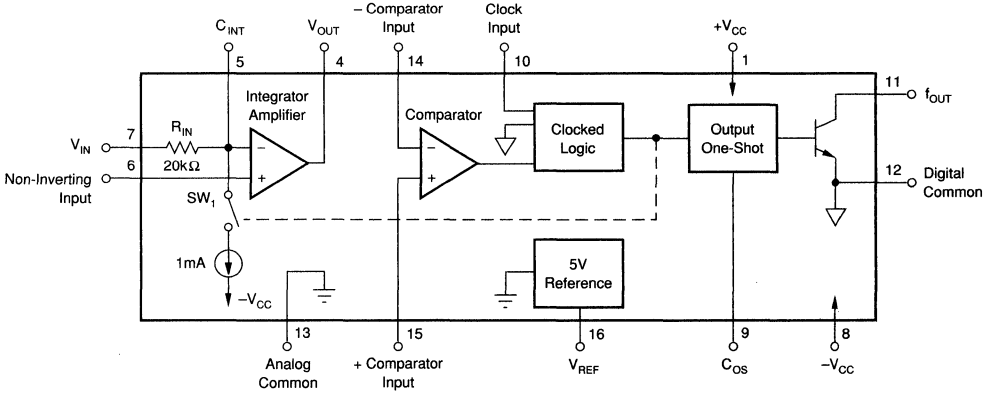
APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used; however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly useful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.



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SPECIFICATIONS

At T_A = +25°C and ±15VDC supplies, unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG MIN	VFC100AG TYP	VFC100AG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$							
Gain Error[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	% of FSR[4]
Linearity Error	FSR = 100kHz, Over Temperature		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.015			*	±0.05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.025			*	±0.1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			±70	±100		±30	±50	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6.5	±25	µV/°C
Power Supply Rejection	Full Supply Range			0.01			*	%/V
Response Time	To Step Input Change	One Period of New Output Frequency Plus One Clock Period						
Current-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$							
Gain Error			±0.5	±1		±0.2	±0.5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	$V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.5	±1		±0.2	±0.5	%
Linearity	FSR = 100kHz		±0.01	±0.025		*	±0.02	%
Input Resistor (R_{IN})								
Resistance		19.8	20	20.2	*	*	*	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	µV
V_{OS} Drift			±5			*		µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dBV
CM Range		–7.5		+0.1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	–0.2		+12		*	*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Current (Operating)	$-11V < V_{COMPARATOR} < +V_{CC} - 2V$			5			*	µA
CLOCK INPUT								
(Referred to Digital Common)								
Frequency (Maximum Operating)			4			*		MHz
Threshold Voltage			1.4			*		V
	Over Temperature	0.8		2	*		*	V
Voltage Range (Operating)		$-V_{CC}$ + 2V		$+V_{CC}$	*		*	V
Input Current	$-V_{CC} < V_{CLOCK} < +V_{CC}$		0.5	5		*	*	µA
Rise Time				2			*	µs
OPEN COLLECTOR OUTPUT								
(Referred to Digital Common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (Off Leakage)	V_{OH} = 30V		0.01	10		*	*	µA
Delay Time, Positive Clock								
Edge to Output Pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT								
Active[6]								
Pulse Width Out	C_{OS} = 300pF	1	1.4	2	*	*	*	µs
Deactivated[5]								
Pulse Width Out	100kHz ≤ FSR < 1MHz		$\frac{1}{4\ f_{CLOCK}}$			*		sec
Pulse Width Out	FSR = 1MHz	250	450	500	*	*	*	ns
REFERENCE VOLTAGE								
Accuracy	No Load	4.9	5	5.1	4.95	*	5.05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	Sourcing Capability	10				*		mA
Power Supply Rejection				0.015			0.015	%/V
Output Impedance			0.5	2		*	*	Ω

SPECIFICATIONS (CONT)

At T_A = +25°C and ±15VDC supplies, unless otherwise noted.

PARAMETER	CONDITIONS	VFC100AG MIN	VFC100AG TYP	VFC100AG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range								
(See Figure 9)	$+V_{CC}$	+7.5		+28.5	*		*	V
	$-V_{CC}$	–7.5		–28.5	*		*	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	*		*	V
Digital Common		$-V_{CC}$ + 2		$+V_{CC}$ – 4	*		*	V
Quiescent Current: $+I_{CC}$	Over Temperature		10.6	15		*	*	mA
$-I_{CC}$			9.6	15		*	*	mA
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Storage		–65		+150	*		*	°C
θ_{JA}			150			*		°C/W
θ_{JC}			100			*		°C/W

* Specification same as AG grade.

NOTES: (1) Offset and gain error can be trimmed to zero. See text. (2) Specified by the box method: (max. – min.) ÷ (FSR x ΔT). (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements. (4) FSR = Full Scale Range. (5) Pin 9 connected to $+V_{CC}$. (6) Nominal PW_{OUT} = (5ns/pF) x C_{OS} – 90ns.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
VFC100AG	16-Pin Ceramic DIP	129
VFC100BG	16-Pin Ceramic DIP	129

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S_1 is closed for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to half the clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V)\ f_{CLOCK}.$$

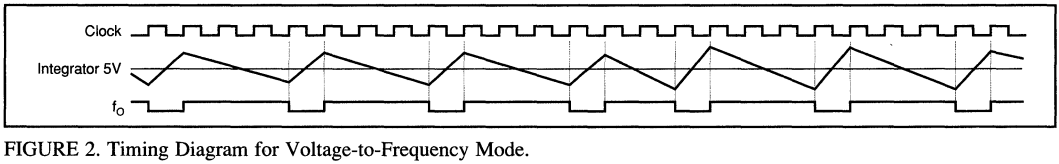

FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

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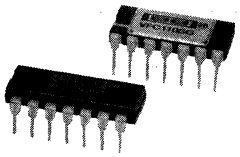


VFC110

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10861

High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- **HIGH-FREQUENCY OPERATION: 4MHz FS max**
- **EXCELLENT LINEARITY: ±0.02% typ at 2MHz**
- **PRECISION 5V REFERENCE**
- **DISABLE PIN**
- **LOW JITTER**

APPLICATIONS

- **INTEGRATING A/D CONVERSION**
- **PROCESS CONTROL**
- **VOLTAGE ISOLATION**
- **VOLTAGE-CONTROLLED OSCILLATOR**
- **FM TELEMETRY**

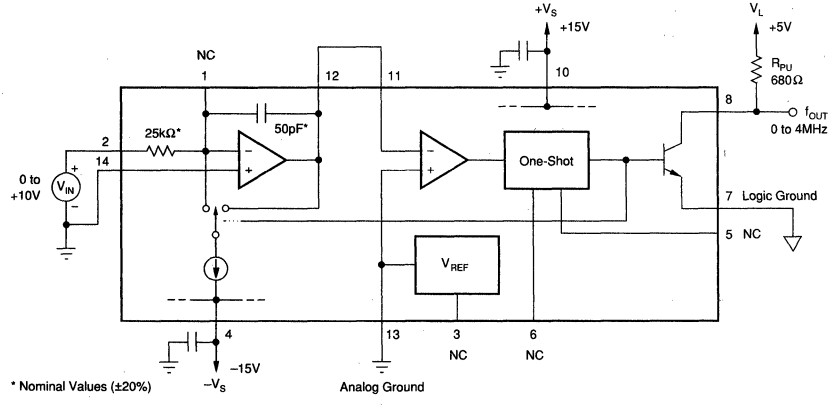
DESCRIPTION

The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range gradeouts are available.



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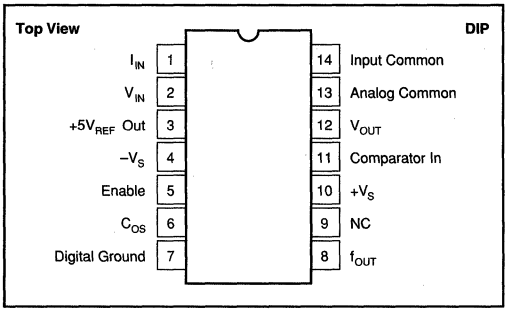
SPECIFICATIONS

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	VFC110BG MIN	VFC110BG TYP	VFC110BG MAX	VFC110AG/SG/AP MIN	VFC110AG/SG/AP TYP	VFC110AG/SG/AP MAX	UNITS
VOLTAGE-TO-FREQUENCY OPERATION								
Nonlinearity[1]: f_{FS} = 100kHz	C_{OS} = 2.2nF, R_{IN} = 44kΩ		0.005	0.01		0.01	0.05	%FS
f_{FS} = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ		0.01	0.05			0.1	%FS
f_{FS} = 2MHz	C_{OS} = 56pF, R_{IN} = 34kΩ		0.02			*		%FS
f_{FS} = 4MHz	C_{OS} = (Int), R_{IN} = (Int)		1			*		%FS
Gain Error, f = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ			5			*	%
Gain Drift, f = 1MHz	Specified Temp Range			50			100	ppm/°C
Relative to V_{REF}	Specified Temp Range		50			100		ppm/°C
PSRR	V_S = ±8V to ±18V			0.05			0.1	%/V
INPUT								
Full Scale Input Current			250	500		*	*	µA
I_B– (Inverting Input)			15	60		20	100	nA
I_B+ (Non-Inverting Input)			250			*		nA
V_{OS}				3			3	mV
V_{OS} Drift	Specified Temp Range		35			*		µV/°C
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 2kΩ	–0.2		$+V_S$ – 4	*		*	V
Output Current Drive		5	20		*	*		mA
Capacitive Load	No Oscillations		10			10		nF
COMPARATOR INPUT								
I_B (Input Bias Current)			–5			*		µA
Trigger Voltage			±50			*		mV
Input Voltage Range		–5		$+V_S$	*		*	V
OPEN COLLECTOR OUTPUT								
V_O Low				0.4			*	V
$I_{LEAKAGE}$			0.1	1		*	*	µA
Fall Time			25			*		ns
Delay to Rise			25			*		ns
Settling Time	To Specified Linearity for a Full-Scale Input Step		One Pulse of New Frequency Plus 1µs					
REFERENCE VOLTAGE								
Voltage		4.97	5	5.03	*	*	*	V
Voltage Drift				20			50	ppm/°C
Load Regulation	I_O = 0 to 10mA		2	10		*	*	mV
PSRR	V_S = ±8V to ±18V		5			*		mV/V
Current Limit	Short Circuit	15	20			*		mA
ENABLE INPUT								
V_{HIGH} (f_{OUT} Enabled)	Specified Temp Range	2			*			V
V_{LOW} (f_{OUT} Disabled)	Specified Temp Range			0.4			*	V
I_{HIGH}			0.1			*		µA
I_{LOW}			1			*		µA
POWER SUPPLY								
Voltage, ±V_S		±8	±15	±18	*	*	*	V
Current			13	16		*	*	mA
TEMPERATURE RANGE								
Specified								
AG, BG, AP		–25		+85	*		*	°C
SG		–55		+125				°C
Storage								
AG, BG, SG		–65		+150	*		*	°C
AP		–40		+125	*		*	°C

* Same specifications as VFC110BG.
NOTE: (1) Nonlinearity measured from 1V to 10V input.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages ($+V_S$ to $-V_S$)	40V
f_{OUT} Sink Current	50mA
Comparator In Voltage	–5V to $+V_S$
Enable Input	$+V_S$ to $-V_S$
Integrator Common-Mode Voltage	–1.5V to +1.5V
Integrator Differential Input Voltage	+0.5V to –0.5V
Integrator Out (short-circuit)	Indefinite
V_{REF} Out (short-circuit)	Indefinite
Operating Temperature Range	
G Package	–55°C to +125°C
P Package	–40°C to +85°C
Storage Temperature	
G Package	–60°C to +150°C
P Package	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
VFC110AG	14-Pin Ceramic DIP	169
VFC110BG	14-Pin Ceramic DIP	169
VFC110SG	14-Pin Ceramic DIP	169
VFC110AP	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC110AG	Ceramic DIP	–25°C to +85°C
VFC110BG	Ceramic DIP	–25°C to +85°C
VFC110SG	Ceramic DIP	–55°C to +125°C
VFC110AP	Plastic DIP	–25°C to +85°C

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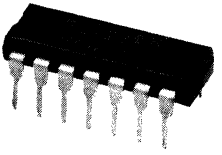


VFC121

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10971

Precision Single Power Supply VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- **SINGLE SUPPLY OPERATION: +4.5V to +36V**
- **f_o = 1.5MHz max**
- **LOW NONLINEARITY: 0.03% max at 100kHz, 0.1% max at 1MHz**
- **HIGH INPUT IMPEDANCE**
- **VOLTAGE REFERENCE OUTPUT**
- **THERMOMETER OUTPUT: 1mV/°K**

APPLICATIONS

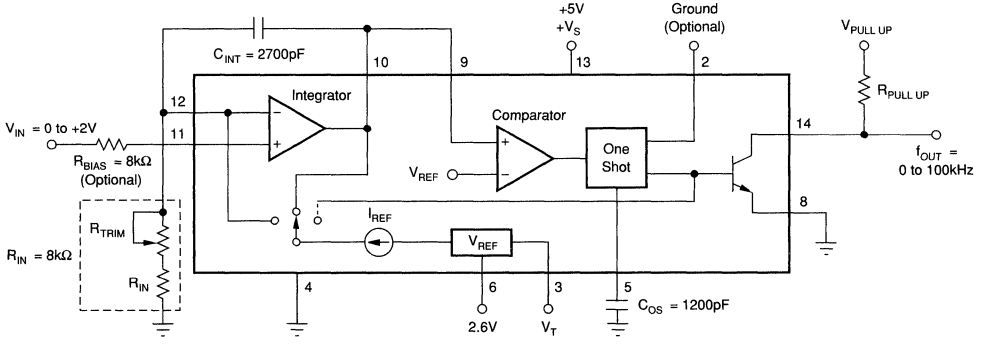
- **INTEGRATING A/D CONVERSION**
- **ANALOG SIGNAL TRANSMISSION**
- **PHASE-LOCKED LOOP VCO**
- **GALVANICALLY ISOLATED SYSTEMS**

DESCRIPTION

The VFC121 is a monolithic voltage-to-frequency converter consisting of an integrating amplifier, voltage reference, and one-shot charge pump circuitry. High-frequency complementary NPN/PNP circuitry is used to implement the charge-balance technique, achieving speed and accuracy far superior to previous single power supply VFCs.

The high-impedance input accepts signals from ground potential to V_S – 2.5V. Power supplies from 4.5V to 36V may be used. A 2.6V reference voltage output may be used to excite sensors or bias external circuitry. A thermometer output voltage proportional to absolute temperature (°K) may be used as a temperature sensor or for temperature compensation of applications circuits.

Frequency output is an open-collector transistor. A disable pin forces the output to the high impedance state, allowing multiple VFCs to share a common transmission path.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	VFC121AP MIN	VFC121AP TYP	VFC121AP MAX	VFC121BP MIN	VFC121BP TYP	VFC121BP MAX	UNITS
ACCURACY								
Nonlinearity: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			0.05			0.03	%FS
f_{FS} = 1MHz	C_{OS} 68pF, C_{INT} = 270pF		0.1				0.1	%FS
Gain Error: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			10			*	%FS
Gain Drift: f_{FS} = 100kHz	T_{MIN} to T_{MAX}			80			40	ppm/°C
Relative to V_{REF}	+V_S = +5V to +36V			100			40	ppm/°C
PSRR				0.025			*	%/V
INPUT								
Minimum Input Voltage				0			*	V
Maximum Input Voltage		V_S–2.5	V_S–2		*	*		V
Impedance		10	100		*	*		MΩ
I_{BIAS}			150	300		*	*	nA
V_{OS}			300	800		100	400	µV
V_{OS} Drift	T_{MIN} to T_{MAX}		10			*		µV/°C
OPEN COLLECTOR OUTPUT								
V_{SAT}	$I_{PULL\ UP}$ = 10mA			0.4			*	V
$I_{LEAKAGE}$	$V_{PULL\ UP}$ = 5V			1			*	µA
	$V_{PULL\ UP}$ = 36V			10			*	µA
Fall Time				100			*	ns
Delay to Rise	$R_{PULL\ UP}$ = 470Ω			100			*	ns
Settling Time	To Specified Linearity for Full Scale Input Step	(1)						
REFERENCE VOLTAGE								
Voltage		2.59	2.6	2.61	*	*	*	V
Voltage Drift				100			50	ppm/°C
Load Regulation	I_O = 0 to 10mA			10			*	mV
PSRR	V_S = +5V to +36V			10			*	mV
Current Limit		Short Circuit Protected						
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 100kΩ	0.8		2.9	*		*	V
COMPARATOR INPUT								
I_{BIAS}			+1			*		µA
Trigger Voltage			2.6			*		V
Input Voltage Range		0		2.9	*		*	V
THERMOMETER								
V_T	T_A = +25°C		298			*		mV
V_T Slope	T_{MIN} to T_{MAX}		1			*		mV/°K
DISABLE INPUT								
V_{HIGH} (Disabled)		2			*			V
V_{LOW}				0.8			*	V
I_{HIGH} (Disabled)	V_{HIGH} = 2V		10			*		µA
I_{LOW}	V_{LOW} = 0.8V		10			*		µA
POWER SUPPLY								
Voltage		4.5	5	36	*	*	*	V
Current			7.5	10		*	*	mA
TEMPERATURE RANGE								
Specified		–25		+85	*		*	°C
Storage		–40		+125	*		*	°C

* Same specification as VFC121AP.
NOTE: (1) One pulse of new frequency plus 1µs.

ORDERING INFORMATION

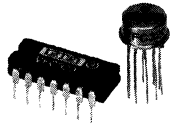
MODEL	PACKAGE	LINEARITY ERROR, MAX (f_S = 100kHz)	TEMPERATURE RANGE
VFC121AP	Plastic DIP	0.05%	–25°C to +85°C
VFC121BP	Plastic DIP	0.03%	–25°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
VFC121AP	14-Pin Plastic DIP	010
VFC121BP	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®



VFC320

ABRIDGED DATA SHEET
For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10483

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- **HIGH LINEARITY, 12 to 14 bits**
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
- **V/F OR F/V CONVERSION**
- **6-DECADE DYNAMIC RANGE**
- **20ppm/°C max GAIN DRIFT**
- **OUTPUT TTL/CMOS COMPATIBLE**

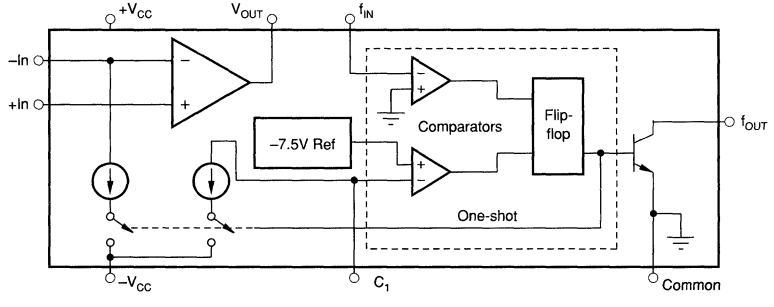
APPLICATIONS

- **INEXPENSIVE A/D AND D/A CONVERTER**
- **DIGITAL PANEL METERS**
- **TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY**
- **FM MOD/DEMOD OF TRANSDUCER SIGNALS**
- **PRECISION LONG TERM INTEGRATOR**
- **HIGH RESOLUTION OPTICAL LINK FOR ISOLATION**
- **AC LINE FREQUENCY MONITOR**
- **MOTOR SPEED MONITOR AND CONTROL**

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with –In and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the –25°C to +85°C and –55°C to +125°C ranges, and the dual-in-line units are specified from –25°C to +85°C.



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SPECIFICATIONS

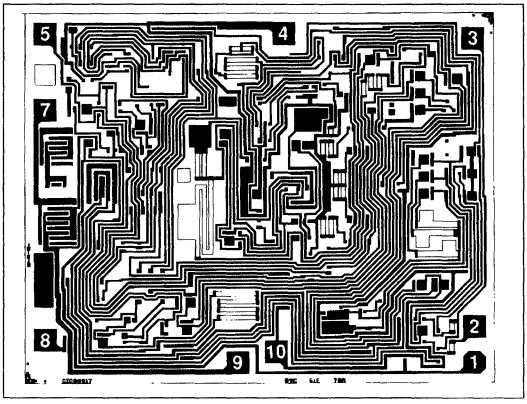
At T_A = +25°C and ±15VDC power supply, unless otherwise noted.

PARAMETER	CONDITIONS	VFC320BG/BM/SM MIN	VFC320BG/BM/SM TYP	VFC320BG/BM/SM MAX	VFC320CG/CM MIN	VFC320CG/CM TYP	VFC320CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	>0		Note 2				V
	Fig. 4 with $e_1 = 0$	<0		–10				V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-Mode								
Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1) (4) (5)	Fig. 4 with $e_2 = 0$(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% FSR
Offset Error Input								
Offset Voltage(3)				±15			*	ppm FSR
Offset Drift(7)			±0.5			*		ppm FSR/°C
Gain Error(3)			±5	±10		*	*	% FSR
Gain Drift(7)	f = 10kHz			50			20	ppm FSR/°C
Full Scale Drift	f = 10kHz			50			20	ppm FSR/°C
(Offset Drift and Gain Drift)(7)(8)(9)								
Power Supply Sensitivity	$\pm V_{CC}$ = 14VDC to 18VDC			±0.015			*	% FSR%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			Decades
Settling Time	(V/F) to Specified Linearity							
	For a Full Scale Input Step		Note 10			*		
Overload Recovery	<50% Overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	µA
Voltage, Logic "1"	External Pull-up Resistor							
	Required (See Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		ns
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ f_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		$+V_{CC}$	*		*	V
Logic "0"		$-V_{CC}$		–0.05	*		*	V
Pulse-width Range		0.25			*			µs
OUTPUT FROM OP AMP								
Voltage	I_O = 6mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-Loop			0.1			*	Ω
Capacitive Load	Without Oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6.5	±7.5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		–25		+85	*		*	°C
S Grade		–55		+125				°C
Operating								
B and C Grades		–40		+85	*		*	°C
S Grade		–55		+125				°C
Storage		–65		+150	*		*	°C

* Specification the same as for VFC320BG/BM/SM.

NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by R_{IN} and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For e_1 = 0 typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components' drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.

DICE INFORMATION



VFC320 DIE TOPOGRAPHY

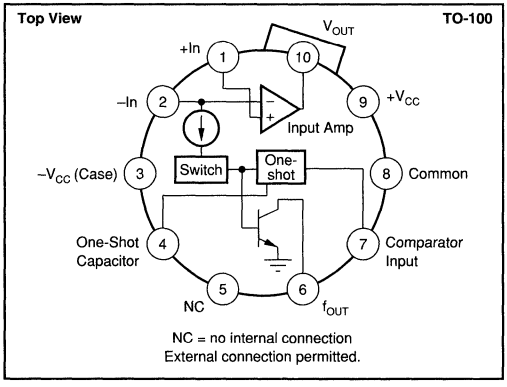
PAD	FUNCTION	PAD	FUNCTION
1	V_{OUT} (Int. Out)	6	NC
2	+In	7	f_{OUT}
3	–In	8	Comp. Input
4	$-V_{CC}$	9	Common
5	One-Shot Cap.	10	$+V_{CC}$

NC: No Connection.
Substrate Bias: Electrically connected to $-V_S$ supply.

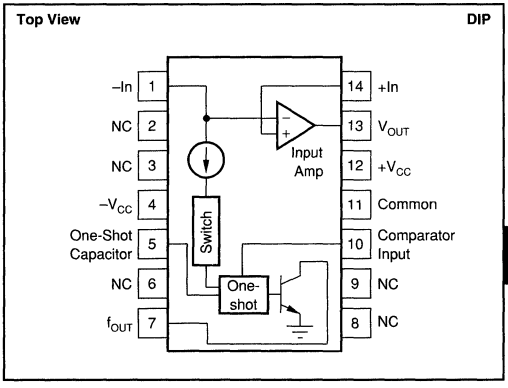
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	109 x 87 ±5	2.77 x 2.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

CONNECTION DIAGRAM



NC = no internal connection
External connection permitted.



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC320BG	14-Pin Ceramic DIP	–25°C to +85°C
VFC320BM	TO-100	–25°C to +85°C
VFC320SM	TO-100	–55°C to +125°C
VFC320CG	14-Pin Ceramic DIP	–25°C to +85°C
VFC320CM	TO-100	–25°C to +85°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
VFC320BG	14-Pin Ceramic DIP	163
VFC320BM	TO-100	007
VFC320SM	TO-100	007
VFC320CG	14-Pin Ceramic DIP	163
VFC320CM	TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, –Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

8 Digital Audio Products

Burr-Brown pioneered the digital audio industry a decade ago with the introduction of the world's first IC digital-to-analog converter specifically designed for audio applications. Burr-Brown continues to be a leader in this field with a complete line of D/As, A/Ds and Digital filters for all ranges of digital audio—from consumer to professional.

The selection guide on the following pages will assist in the selection of the proper component for each application—some of the newer products are:

PCM1710—This dual D/A offers the maximum performance (–88dB THD+N) in an economy converter for consumer applications. It is a complete converter and contains a digital filter, output low pass filters and op amps.

PCM1712/14/15—These derivations of the popular PCM1710 are tailored for specific applications. The PCM1712 is optimized for economy consumer applications. The PCM1714 is configured for music instruments. The PCM1715 has the output flexability required for communications, multi-media and DSP.

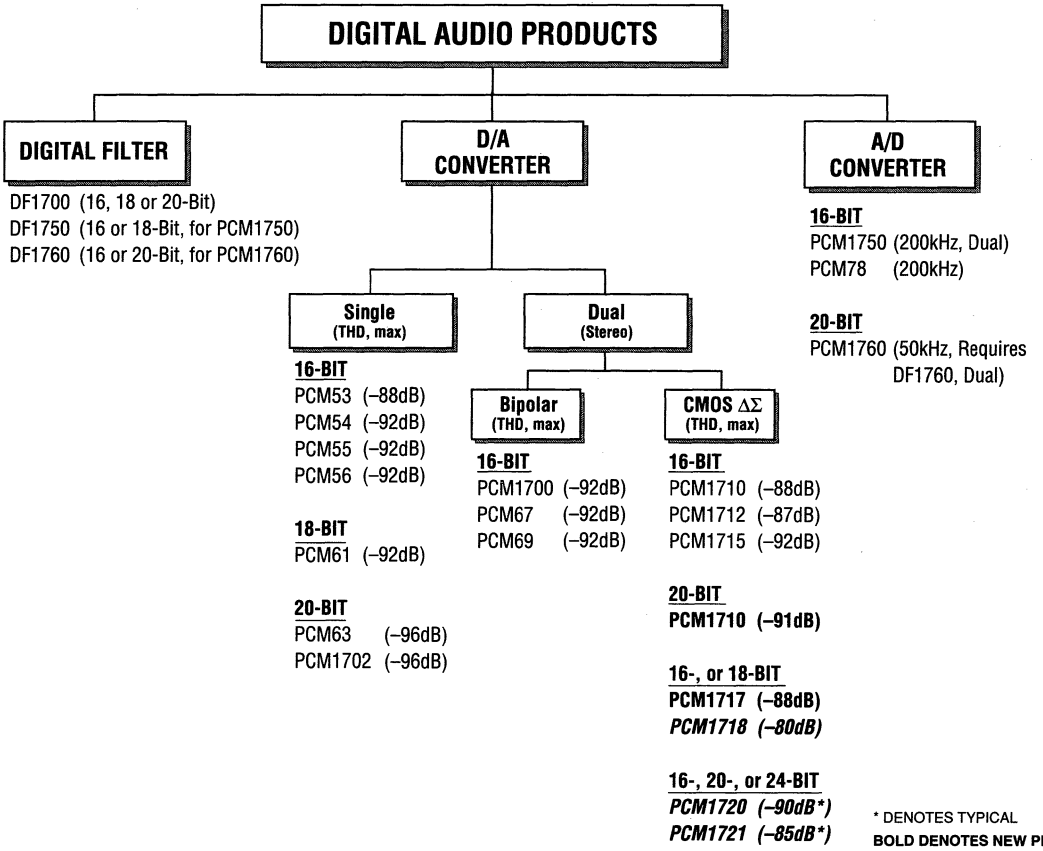
PCM1717—A new *SoundPlus* complete 16- or 18-bit stereo, audio D/A converter, including digital interpolation filter, 3rd-order delta-sigma D/A, and analog output amplifiers—fabricated using a highly advanced 0.6µ CMOS process.

PCM1718—Another in the *SoundPlus* line, this converter accepts 18-bit normal input data format, or 16- or 18-bit I^2S data format.

PCM1720—A complete, stereo audio converter, the PCM1720 can accept 16-, 20-, or 24-bit input data in either normal or I^2S formats. It can also accept standard digital audio sampling frequencies as well as one-half and double sampling frequencies.

PCM1721—Basically the same as the PCM1720, the PCM1721 has a programmable phase-locked loop (PLL) circuit included. The PLL derives either 256fs or 384fs system clock from an external 27MHz reference frequency.

PCM/DF1760—This combination provides 20-bit stereo A/D conversion with performance levels required by high-end consumer and pro audio applications.



* DENOTES TYPICAL
BOLD DENOTES NEW PRODUCT
BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

AUDIO QUALITY DIGITAL-TO-ANALOG

Product	Resolution[1] (Bits)	Sampling[2] Rate	Dynamic Range (typ in dB)	Configuration	Audio Data Format	Power Supply	Package	Comments
PCM54	16	500kHz	94	Mono	Parallel	±5 to ±15	DDIP-28	Bipolar, R-2R, Parallel Input
PCM56	16	800kHz	94	Mono	Serial Latched	±5 to ±12	DIP-16, SO-16	Bipolar, R-2R
PCM61	18	800kHz	94	Mono	Serial Latched	±5 to ±12	DIP-16	Bipolar, R-2R
PCM63	20	1MHz	104	Mono	Serial Latched	±5	DIP-28	Bipolar, Signed Magnitude
PCM69A	18	1MHz	100	Stereo	Serial Latched	±5	DIP-16, SO-20	BiCMOS, Advanced 1-Bit
PCM1700	18	800kHz	94	Stereo	Serial Latched	±5	DIP-28, SO-28	Bipolar, R-2R
PCM1702	20	1MHz	104	Mono	Serial Latched	±5	DIP-16, SO-20	BiCMOS, Signed Magnitude
PCM1710U	20	48kHz	98	Stereo	Normal, Continuous I²S	+5	SO-28	CMOS, Multi-Level ΔΣ
PCM1712U	16	48kHz	94	Stereo	Normal	+5	SO-28	CMOS, Multi-Level ΔΣ
PCM1715U	16	48kHz	98	Stereo	Normal	+5	SO-28	CMOS, Multi-Level ΔΣ
PCM1717E	**18**	**48kHz**	**96**	**Stereo**	**Normal, I²S**	**+3 to +5**	**SSOP-20**	**CMOS, Multi-Level ΔΣ**
PCM1718E	***18***	***48kHz***	***96***	***Stereo***	***Normal, I²S***	***+3 to +5***	***SSOP-20***	***CMOS, Multi-Level ΔΣ***
PCM1720E	***24***	***96kHz***	***96***	***Stereo***	***Normal, I²S***	***+5***	***SSOP-20***	***CMOS, Multi-Level ΔΣ***
PCM1721E	***24***	***96kHz***	***94***	***Stereo***	***Normal, I²S***	***+5***	***SSOP-24***	***CMOS, Multi-Level ΔΣ, Internal PLL***

NOTE: (1) Resolution is the maximum number of bits per word. (2) Sampling rate for the R-2R type products (with *) are based on settling time. The ΔΣ products inherently oversample at standard audio sampling frequencies.

DIGITAL FILTERS

Product	Input Resolution (Bits)	Typical Resolution (Bits)	Passband Ripple (dB)	Stopband Attenuation (dB)	Power Supply (V)	Pkg[1]	Page Description
DF1700	16	16/18/20	±0.00005dB	>100dB	+5V	DIP/SO	Dual Interpolation
DF1750	16/18	18	< ±0.0005dB	>95dB	+5V	DIP/SO	Dual 1/4 or 1/2 Decimating
DF1760	16/20	16/20	±0.0001dB	>94dB	+5V	DIP/SO	Dual Decimating

NOTE: (1) DIP = 0.3" wide DIP, SO = Small Outline Surface Mount.

AUDIO QUALITY

Product	Resolution (Bits)	Typical DC Linearity Accuracy	Input Range (V)	Conversion Time (μs)	THD+N dB, Max (V_{IN} = ±FS)	Output Format	Pkg[1]	Description
PCM78	16	14-Bit	±3	5	–88	Serial	DDIP	Low Cost
PCM1750	18	14-Bit	±2.75	5	–90	Serial	DDIP, SOIC	Dual
PCM1760	20	16-Bit	±2.5	20	–90, 88	Serial	DDIP, SOIC	Dual Channel, ΔΣ

NOTE: (1) DDIP = 0.6" wide DIP, SO = Small Outline Surface Mount.

* DENOTES TYPICAL

BOLD DENOTES NEW PRODUCT

BOLD, ITALIC DENOTES PRODUCT IN DEVELOPMENT

Some specifications have been estimated for comparison purposes. Refer to data sheets for guaranteed specifications.

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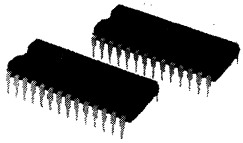


PCM78P

DEMO BOARD AVAILABLE
See Appendix A

16-Bit Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW COST/HIGH PERFORMANCE 16-BIT AUDIO A/D CONVERTER
- FAST 5µs MAX CONVERSION TIME (4µs typ)
- VERY LOW THD+N (typ –88dB at FS; max –82dB)
- ±3V INPUT RANGE
- TWO SERIAL OUTPUT MODES PROVIDE VERSATILE INTERFACING
- COMPLETE WITH INTERNAL REFERENCE AND CLOCK IN 28-PIN PLASTIC DIP
- ±5V TO ±15V SUPPLY RANGE (600mW Power Dissipation)

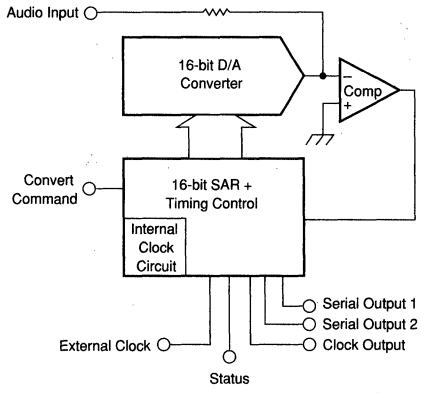
APPLICATIONS

- DSP DATA ACQUISITION
- TEST INSTRUMENTATION
- SAMPLING KEYBOARD SYNTHESIZERS
- DIGITAL AUDIO TAPE
- BROADCAST AUDIO PROCESSING
- TELECOMMUNICATIONS

DESCRIPTION

The PCM78P is a low-cost 16-bit analog-to-digital converter which is specifically designed and tested for dynamic applications. It features very fast, low distortion performance (4µs/–88dB THD+N typical) and is complete with internal clock and reference circuitry. The PCM78P is packaged in a reliable, low-cost 28-pin plastic DIP and data output is available in user-selectable serial output formats. The PCM78P is ideal for digital audio tape (DAT) recorders. Many similar applications such as digital signal processing and telecom applications are equally well served by the PCM78P.

The PCM78P uses a SAR technique. Analog and digital portions are efficiently partitioned into a high-speed, bipolar section and a low-power CMOS section. The PCM78P has been optimized for excellent dynamic performance and low cost.



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SPECIFICATIONS

ELECTRICAL

At T_C = +25°C, $+V_{DD}$ = +5V, and $\pm V_{CC}$ = ±12V, and one minute warm-up in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	PCM78P MIN	PCM78P TYP	PCM78P MAX	UNITS
RESOLUTION				16	Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		–3		+3	V
Input Impedance			1.5		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +40µA	+2		+5.5	V
V_{IL}	I_{IL} = –100µA	0		+0.8	V
V_{OH}	I_{OH} = 2TTL Loads	+2.4			V
V_{OL}	I_{OL} = 2TTL Loads			+0.4	V
Data Format			Serial BOB or BTC		
Convert Command			Negative Edge (1)		
Pulse Width		25	50		ns
CONVERSION TIME			4	5	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO-NOISE RATIO (SNR)(2)	f_S = 200kHz/T_{CONV} = 4µs(3)				
f = 1kHz (0dB)	BW = 20kHz		90		dB(4)
f = 10kHz (0dB)	BW = 100kHz		80		dB
TOTAL HARMONIC DISTORTION(5)	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–91		dB
f = 19kHz (0dB)	BW = 20kHz		–90		dB
f = 10kHz (0dB)	BW = 100kHz		–90		dB
f = 90kHz (0dB)	BW = 100kHz		–89		dB
TOTAL HARMONIC DISTORTION + NOISE(6)	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–88	–82	dB
f = 1kHz (–20dB)	BW = 20kHz		–74	–68	dB
f = 1kHz (–60dB)	BW = 20kHz		–34		dB
f = 19kHz (0dB)	BW = 20kHz		–87		dB
f = 10kHz (0dB)	BW = 100kHz		–82		dB
f = 90kHz (0dB)	BW = 100kHz		–81		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±20		mV
Differential Linearity Error			±0.002		% of FSR(7)
Integral Linearity Error			±0.003		% of FSR
Missing Codes			None		14 Bits(8)
DRIFT					
Gain	0°C to +70°C		±25		ppm/°C
Bipolar Zero	0°C to +70°C		±4		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.008		%FSR/%V_{CC}
$-V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.003		%FSR/%V_{DD}
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.75		+15.6	V
$-V_{CC}$		–4.75		–15.6	V
$+V_{DD}$		+4.75		+5.25	V
Current: $+V_{CC}$	$+V_{CC}$ = +12V		+15		mA
$-V_{CC}$	$-V_{CC}$ = –12V		–21		mA
$+V_{DD}$	$+V_{DD}$ = +5V		+7		mA
Power Dissipation	$\pm V_{CC}$ = ±12V		575		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		–50		+100	°C
Operating		–25		+85	°C

NOTES: (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. See detailed text on timing for convert command description when using external clock. (2) Ratio of Noise rms/Signal rms. (3) f = input frequency; f_S = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms. (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR: Full-Scale Range = 6Vp-p. (8) Typically no missing Codes at 14-bit resolution.

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	Analog In	I	Analog Signal Input (1.5kΩ impedance).
2	$-V_{CC}$	I	Analog power supply (–5V to –15V).
3	MSB Adjust	I	Internal adjustment point to allow adjustment of MSB major carry.
4	$+V_{DD}$	I	Power connection for comparator (+5V).
5	No Connection	—	No internal connection.
6	Comparator Common	I	Comparator common connection. Connect to ground.
7	$\overline{MSB}$	O	Parallel output of bit 1 (MSB) inverted.
8	BTC/BOB Select	I	Two's complement (open) or straight binary (grounded) data output format selection.
9	Status	O	Output signal held high until conversion is complete.
10	Clock Out	O	Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ~24ns and same duty cycle).
11	R_1C_1	I	RC connection point used to generate internal clock. Sets clock high time. See text for details.
12	R_2C_2	I	RC connection point used to generate internal clock. Sets clock low time. See text for details.
13	S_{OUT2}	O	Internal shift register containing the previous conversion result. (Alternate latched data output mode).
14	$+V_{DD}$	I	Power connection for +5V logic supply.
15	S_{OUT1}	O	Primary real-time data output synchronized to clock out.
16	External Clock	I	External clock input point (internal clock must be disabled).
17	Int/Ext Clock Select	I	Selects either internal or external clock mode (low = internal; open = external).
18	Short Cycle	I	Terminates conversion at less than 16 bits (open for 16-bit mode). See text for details.
19	Convert Command	I	Starts conversion process (can optionally be generated internally).
20	S_{OUT2} Latch	I	Latches previous conversion result for readout (must be issued with the S_{OUT2} clock to initiate latch and an internal convert command).
21	S_{OUT2} Clock	I	Used to read out internally latched data from previous conversion.
22	Digital Common	I	Digital grounding pin.
23	$+V_{CC}$	I	Analog supply connection (+5V to +15V).
24	V_{POT}	O	Voltage output (~2.5V) for optional adjustment of MSB transition.
25	Reference Decouple	I	Reference decoupling point.
26	Analog Common	I	Analog grounding pin.
27	Reference Out	O	2V reference out. Should not be used except as shown in connection diagram.
28	Speed Up	I	Connection point for a capacitor to speed reference settling. See text for details.

NOTE: Analog and digital commons are connected internally.

INPUT/OUTPUT RELATIONSHIPS

ANALOG INPUT	CONDITION	DIGITAL OUTPUT	
		BTC	BOB
+2.999908V	+ Full Scale	7FFF Hex	FFFF Hex
–3.000000V	–Full Scale	8000 Hex	0000 Hex
0.000000V	Bipolar Zero	0000 Hex	8000 Hex
–0.000092V	Zero-1 LSB	FFFF Hex	7FFF Hex

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to –16.5V
$-V_{DD}$ to Analog Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Digital Common	–0.3V to V_{DD} + 0.5V
Analog Inputs to Analog Common	±16.5V
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM78P	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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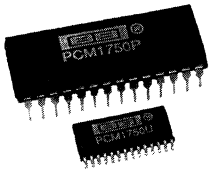


PCM1750P
PCM1750U

DEMO BOARD AVAILABLE
See Appendix A

Dual CMOS 18-Bit Monolithic Audio ANALOG-TO-DIGITAL CONVERTER

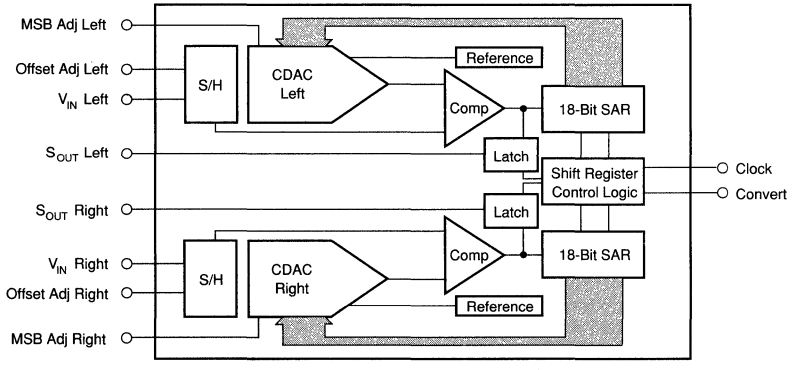
FEATURES

- **DUAL 18-BIT LOW-POWER CMOS AUDIO A/D CONVERTER**
- **FAST 4.5μs MIN CONVERSION TIME INCLUDING S/H**
- **VERY LOW MAX THD+N: –88dB Without External Adjust**
- **COMPLETE WITH INTERNAL REFERENCE AND DUAL S/H FUNCTION**
- **TWO CO-PHASE SAMPLED, ±2.75V AUDIO INPUTS**
- **CAPABLE OF 4X PER CHANNEL OVERSAMPLING RATE**
- **RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX**
- **COMPACT 28-PIN PLASTIC DIP OR SOIC**

DESCRIPTION

The PCM1750 is a low cost, dual 18-bit CMOS analog-to-digital converter optimized for dynamic signal applications. The PCM1750 features true co-phased inputs with an internal sample/hold function for each channel. The PCM1750 also comes complete with an internal reference. Total power dissipation is less than 300mW max using ±5V voltage supplies. Low maximum Total Harmonic Distortion + Noise (–88dB max) is 100% tested. The very fast PCM1750 is capable of 4 times oversampling of the audio bandwidth on both input channels simultaneously, providing greater freedom to designers in selecting input anti-aliasing filters.

PCM1750 outputs serial data in a format that is compatible with many digital filter chips and comes packaged in a space saving 28-pin plastic DIP or SOIC.



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SPECIFICATIONS

ELECTRICAL

At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5.0V$, unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1750P, U MIN	PCM1750P, U TYP	PCM1750P, U MAX	UNITS
RESOLUTION		18			Bits
DYNAMIC RANGE	THD + N at –60dB Referred to Full Scale	+88	+90		dB
ANALOG INPUT					
Input Range			±2.75		V
Input Capacitance			20		pF
Aperture Delay			10		ns
Aperture Uncertainty (Jitter)			50		ps_{rms}
Full Power Input Bandwidth			500		kHz
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS Compatible		
Logic Level: V_{IH}	$I_{IH} = \pm 5\mu A$	+3.5		$+V_D + 0.3$	V
V_{IL}	$I_{IL} = \pm 5\mu A$	–0.3		+1.5	V
V_{OH}	$I_{SOURCE} = 1.0mA$	+2.7	+4.7		V
V_{OL}	$I_{SINK} = 3.2mA$		+0.2	+0.4	V
Output Data Format			Serial, MSB First, BTC[1]		
Convert Command			Positive Edge		
Convert Command Pulse Width			81		ns
Conversion Time	Throughput Including Sample/Hold[2]	4.5	5.2	20.8	µs
DYNAMIC CHARACTERISTICS (20Hz to 24kHz; 4X data decimated to 1X)					
Signal-to-Noise Ratio[3]	fs = 192kHz[4]; f_{IN} = 1kHz (0dB)[5]	+88	+90		dB[6]
Total Harmonic Distortion + N[7]	Without External Adjustments				
f_{IN} = 1kHz (0dB)	fs = 192kHz		–90	–88	dB
f_{IN} = 1kHz (–20dB)	fs = 192kHz		–70	–68	dB
f_{IN} = 1kHz (–60dB)	fs = 192kHz		–30	–28	dB
Channel Separation	fs = 192kHz; f_{IN} = 1kHz (0dB) and 0V	+96	+108		dB
ACCURACY					
Gain Error			±2	±5	%
Gain Mismatch	Channel to Channel		±0.5	±2.0	%
BPZ (Bipolar Zero) Error[8]			±2		mV
BPZ Error Mismatch	Channel to Channel		±3		mV
BPZ Differential Linearity Error[9]			±0.002		% of FSR[10]
Linearity Error			±0.003		% of FSR
Warm-up Time			1		ms
DRIFT (With Internal Reference)					
Gain	0°C to 70°C		±50		ppm/°C
Bipolar Zero	0°C to 70°C		±10		ppm of FSR/°C
DRIFT (Exclusive of Internal Reference)					
Gain	0°C to 70°C		±10		ppm/°C
Bipolar Zero	0°C to 70°C		±3		ppm of FSR/°C
REFERENCE					
V_{REF} Output (Pins 19, 24):					
Voltage			+2.75		V
Current			±100		µA
Impedance			0.2		Ω
Accuracy			±25		mV
Drift	0°C to 70°C		±50		ppm/°C
V_{REF} Input (Pins 18, P25):					
Impedance[11]			363 || 120		Ω || pF
POWER SUPPLY REJECTION	% of V_{IN} / % of V_{SUPPLY} [12]		0.03		% / %
POWER SUPPLY REQUIREMENTS					
$\pm V_A$ Supply Voltage Range		±4.75	±5.00	±5.25	V
$+V_D$ Supply Voltage Range		+4.75	+5.00	+5.25	V
$+I_A$; $+I_D$ Combined Supply Current	$+V_A$; $+V_D$ = +5.0V		+28		mA
$-I_A$ Supply Current	$-V_A$ = –5.0V		–13		mA
Power Dissipation	$\pm V_A = \pm 5.0V$; $+V_D$ = +5.0V		210	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) The PCM1750 is tested and guaranteed at 5.2µs, however it will operate at 4.5µs. The dynamic performance is not guaranteed or tested at this conversion rate. (3) Ratio of $Signal_{RMS}$ / ($Distortion_{RMS}$ + $Noise_{RMS}$). (4) A/D converter sample frequency (4 x 48kHz; 4X oversampling per channel). (5) A/D converter input frequency (signal level). (6) Referred to input signal level. (7) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (8) Externally adjustable to zero error. (9) Differential non-linearity error at bipolar major carry input code. Externally adjustable to zero error. (10) Full scale range (5.50V). (11) Refer to equivalent circuit in Figure 1. (12) Worst case operating condition. Refer to typical performance curves.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply Voltage	$-V_A$
2	+5V Analog Supply Voltage	$+V_A$
3	Serial Output (Left Channel)	SOUTL
4	External Clock Input	CLK
5	+5V Analog Supply Voltage	$+V_A$
6	+5V Digital Voltage Supply	$+V_D$
7	+5V Digital Voltage Supply	$+V_D$
8	Digital Common Connection	DCOM
9	Analog Common Connection	ACOM
10	Digital Common Connection	DCOM
11	Convert Command Input	CONVERT
12	Serial Output (Right Channel)	SOUTR
13	+5V Analog Supply Voltage	$+V_A$
14	–5V Analog Supply Voltage	$-V_A$
15	Offset Adjust (Right Channel)	OFF_{ADJR}
16	MSB Adjust (Right Channel)	MSB_{ADJR}
17	Analog Voltage Input (Right Channel; ±2.75V)	V_{INR}
18	Reference Voltage Input (Right Channel)	$VREF_{INR}$
19	Reference Voltage Output (Right Channel)	$VREF_{OUTR}$
20	Analog Common Connection	ACOM
21	Reference Voltage Decouple	$VREF_{CAP}$
22	Reference Common Connection	RCOM
23	Analog Common Connection	ACOM
24	Reference Voltage Output (Left Channel)	$VREF_{OUTL}$
25	Reference Voltage Input (Left Channel)	$VREF_{INL}$
26	Analog Voltage Input (Left Channel; ±2.75V)	V_{INL}
27	MSB Adjust (Left Channel)	MSB_{ADJL}
28	Offset Adjust (Left Channel)	OFF_{ADJL}

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage (V_{IN})	$-V_A$ –0.3V to $+V_A$ + 0.3V
$+V_A$; $+V_D$ to ACOM/DCOM	0 to +7V
$-V_A$ to ACOM/DCOM	0 to –7V
$-V_A$ to $+V_A$; $+V_D$	0 to +14V
ACOM to DCOM	±1V
Digital Inputs (pins 4, 11) to DCOM	–0.3V to $+V_D$ + 0.3V
Power Dissipation	400mW
Lead Temperature, (soldering 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	80°C/W
Thermal Resistance, θ_{JA}: Plastic SOIC	100°C/W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

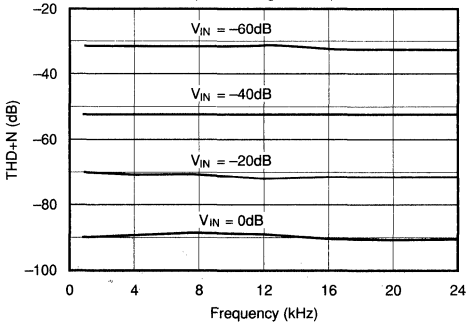
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PCM1750P	28-Pin Plastic DIP	215
PCM1750U	28-Pin Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

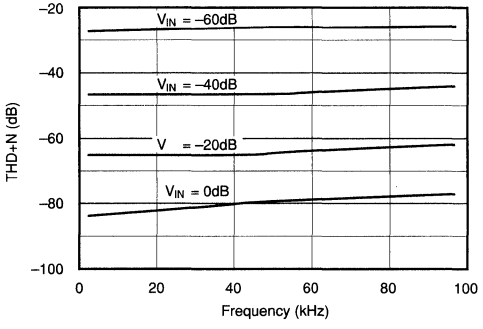
TYPICAL PERFORMANCE CURVES

At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5V$, unless otherwise noted. Where relevant, specifications apply to both left and right input output channels.

THD+N vs FREQUENCY
(With 4X Digital Filter)



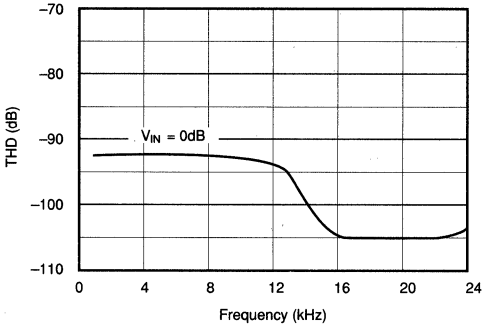
THD+N vs FREQUENCY
(Without 4X Digital Filter)



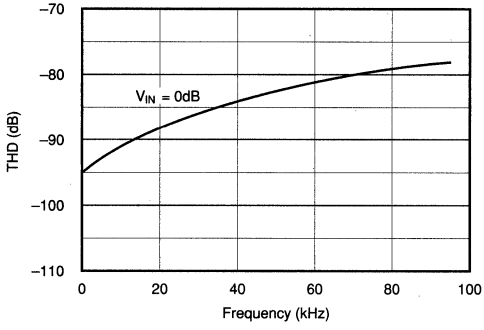
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5.0V$, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

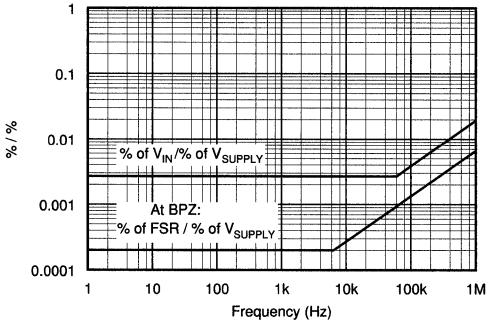
THD vs FREQUENCY
(With 4X Digital Filter)



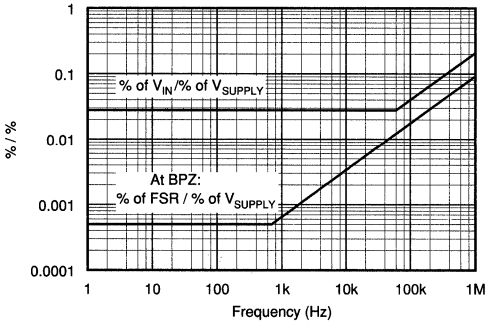
THD vs FREQUENCY
(Without 4X Digital Filter)



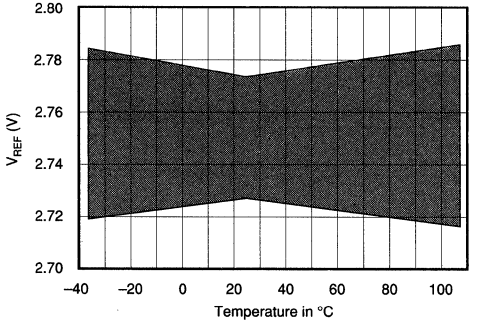
PSR vs FREQUENCY
(–5V SUPPLY)



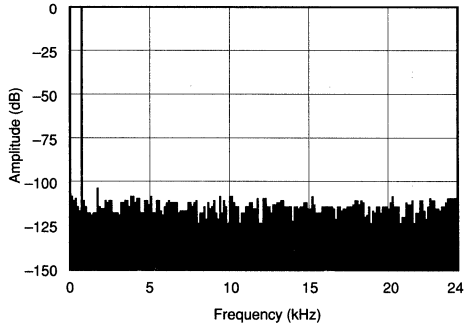
PSR vs FREQUENCY
(+5V SUPPLIES)



V_{REF} vs TEMPERATURE
(V_{REF} Outputs)



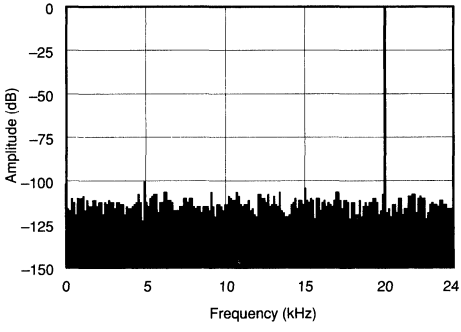
FFT 850Hz (24kHz BW; 2048 POINTS)



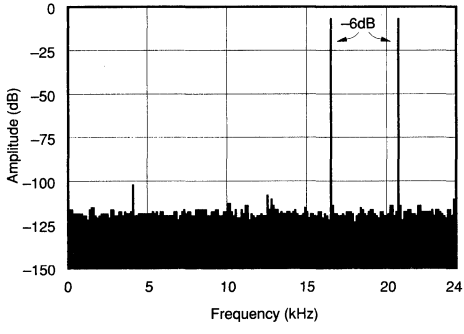
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, and $\pm V_A$; $+V_D = \pm 5V$, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

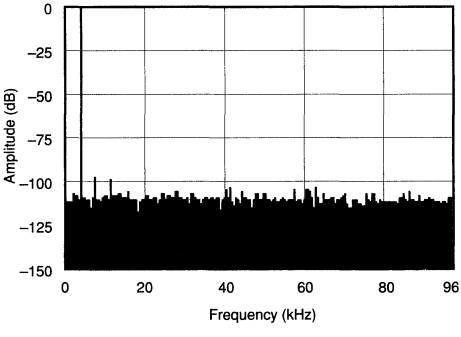
FFT 20kHz (24kHz BW; 2048 POINTS)



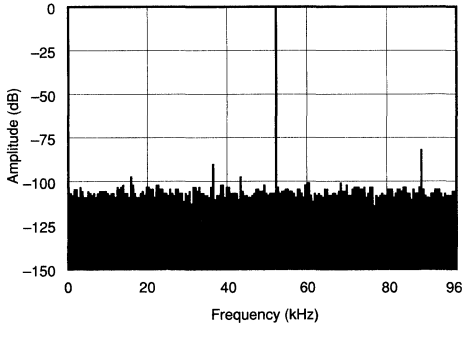
FFT 17kHz and 21kHz (24kHz BW; 16384 POINTS)



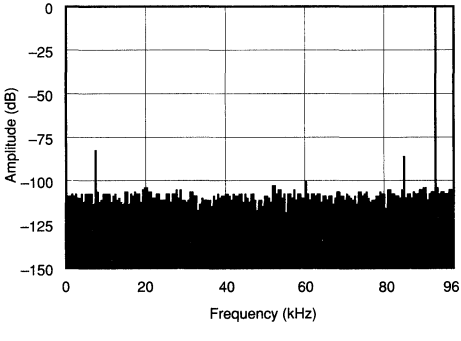
FFT 3.7kHz (96kHz BW; 2048 POINTS)



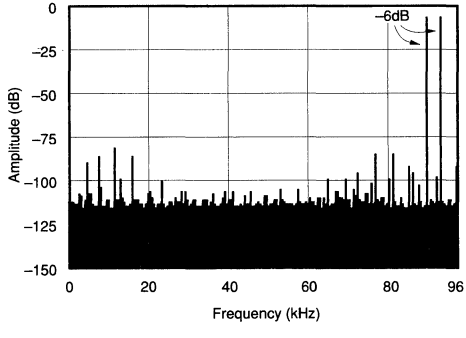
FFT 52kHz (96kHz BW; 2048 POINTS)



FFT 92kHz (96kHz BW; 2048 POINTS)



FFT 88kHz and 92kHz (96kHz BW; 16384 POINTS)



THEORY OF OPERATION

OVERVIEW

The PCM1750 is a dual 18-bit successive approximation CMOS analog-to-digital converter with serial data outputs designed especially for digital audio and similar applications. The single-chip converter is fabricated on a 3µ P-well CMOS process which includes poly-poly capacitors, laser-trimmable nichrome resistors, and two layers of interconnect metal. The dual converter employs a switched capacitor architecture which provides separate, simultaneous S/H (sample/hold) functions for each input channel. The separate S/H for each channel results in a desired feature called co-phase sampling which means that both S/H circuits are switched at the same time into the HOLD mode to capture their respective input signals simultaneously. This eliminates phasing errors produced by alternative architecture ADCs which do not sample the two input channels at the same time.

Switched binary-weighted poly-poly capacitors are used in CDAC (capacitive digital-to-analog converter) configurations to form the successive approximation converter sec-

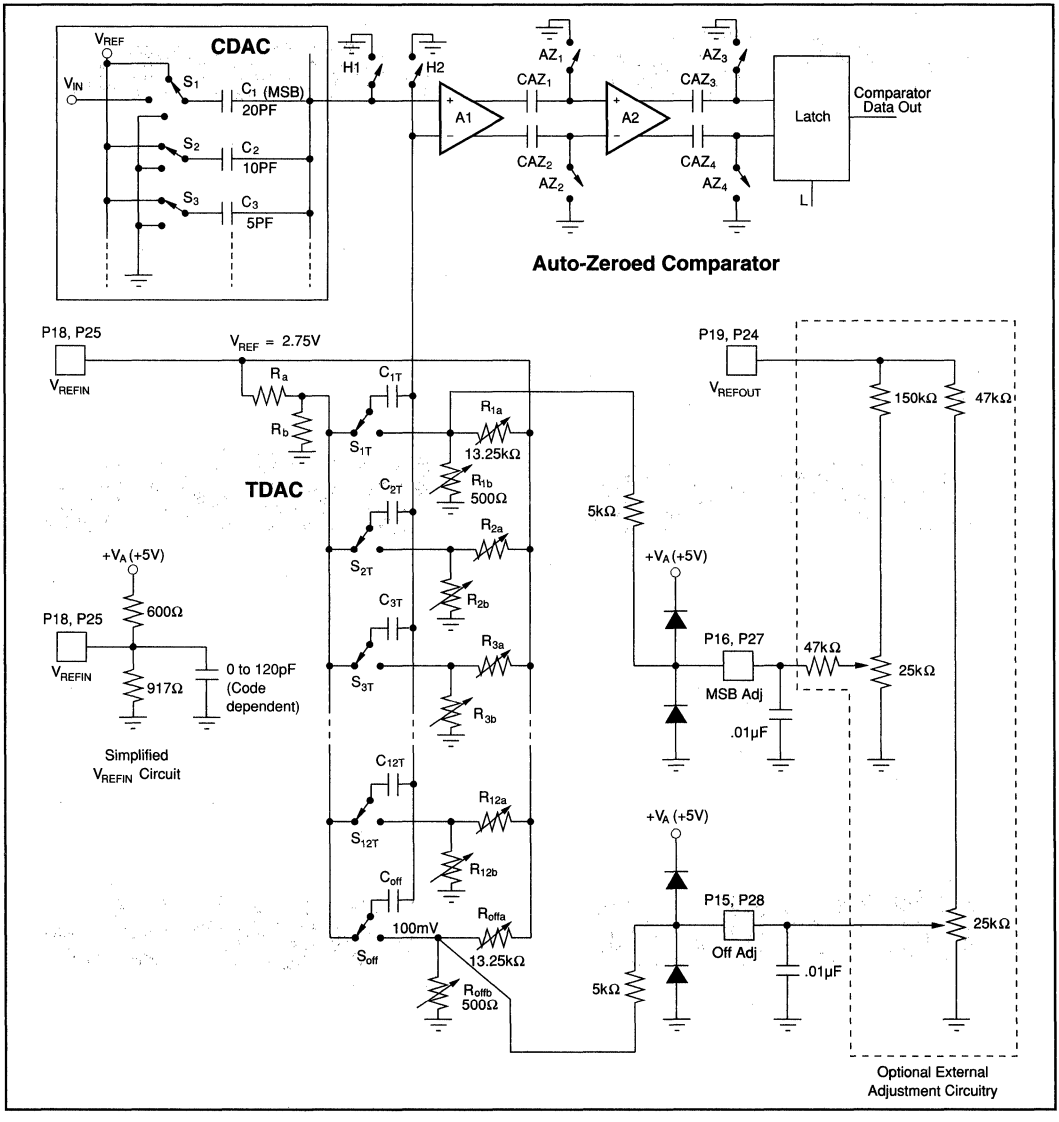


FIGURE 1. PCM1750 Simplified Circuit Diagram.

tions of the PCM1750. Two other switched-capacitor TDACs (trim-DACs, which employ laser-trimmed nichrome resistors) are also used to provide small correction voltages to the latching comparators. These small correction voltages compensate for ratio matching errors of the binary-weighted capacitors in the CDAC. The comparators contain autozeroed preamplifier stages ahead of the latching amplifier stage to produce a one bit, serial data stream that controls the successive approximation algorithm for each channel of the PCM1750.

To simplify user application, the PCM1750 includes an internal band-gap reference with fast settling buffer amplifiers to drive the CDACs. The dual converters operate synchronously (to minimize digital noise conversion errors) using an external system clock (normally at 1X, 2X or 4X the standard 48kHz audio sampling rate). By operating at a 2X or 4X oversampling rate the roll-off requirement for the input anti-aliasing filters is relaxed. For example, 1X systems typically use a 9 to 11 pole LPF (low pass filter) whereas a 4X system can use a 6th (or smaller) order filter when an appropriate digital filter such as the DF1750 is used in conjunction with the sampling system. Oversampling also has the added benefit of improved signal to noise ratio and total harmonic distortion. Two serial outputs, one for each input channel, provide binary-two's-complement coded output to an optional external digital decimation filter when over sampling operation is desired. The use of the optional companion digital filter, the DF1750, is described later in the installation and application sections of this product data sheet. A separate product data sheet is also available for the Burr-Brown DF1750 giving all the specifications and performance diagrams associated with this digital filter.

SAMPLE (TRACKING) MODE

After each conversion, the dual ADC returns to the SAMPLE mode in order to track the input signals. The switches shown in the simplified circuit diagram of Figure 1 will then be in the following states: S1 connects V_{IN} to C1 ; S2 to S18 connect C2 to C18 to V_{REF}; H1 and H2 connect the top plates of the capacitor arrays to analog common; and the latching comparator is switched into its auto-zero mode by closing AZ1 to AZ4. Notice that C1 serves two purposes: it samples and stores the input signal V_{IN} and it is the MSB of the CDAC. Storing V_{REF} on C2 to C18 creates a bipolar offset, enabling V_{IN} to cover a span from $-V_{REF}$ to $+V_{REF}$.

The 1/f noise as well as the DC input offset voltage of the comparator are removed by an autozeroing cycle which

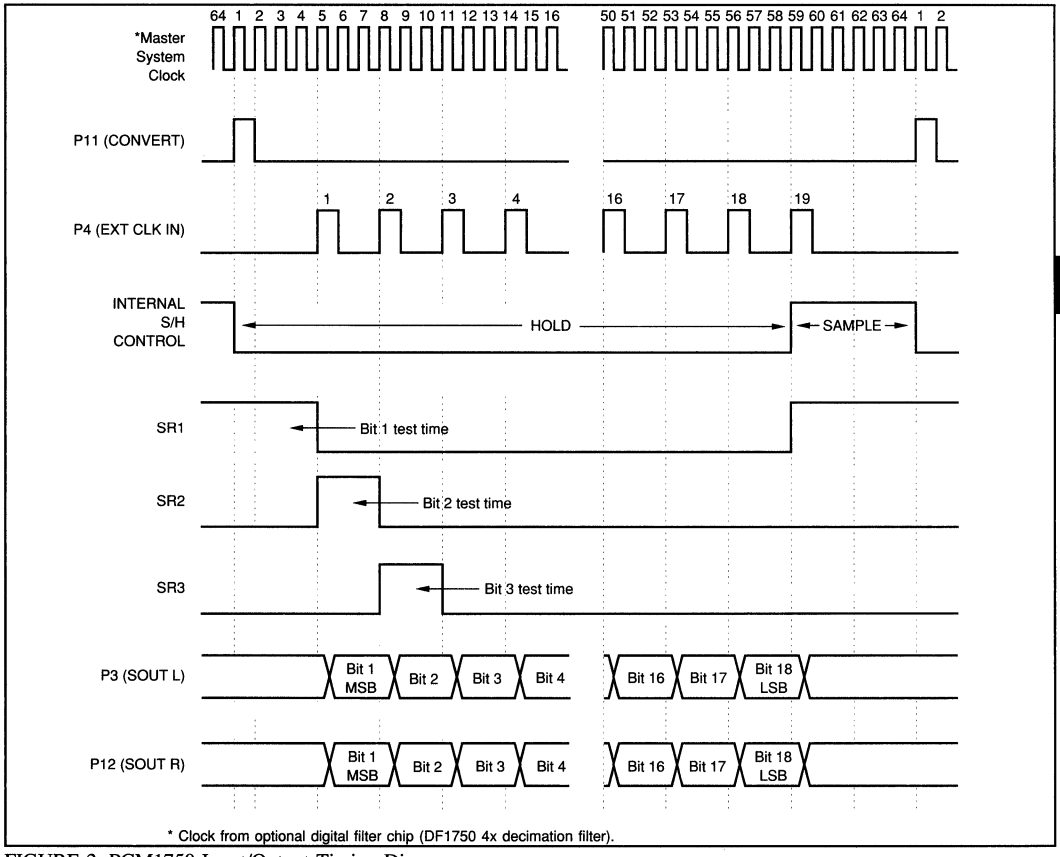


FIGURE 2. PCM1750 Input/Output Timing Diagram.

occurs during the SAMPLE period (see the timing diagram shown in Figure 2). These errors are stored on the AC coupling capacitors (CAZ1 to CAZ4, shown in Figure 1) between the gain stages. During the SAMPLE period the inputs to gain stages A1 and A2 and the latch are grounded by switches H1, H2, and AZ1 to AZ4. Capacitors CAZ1 and CAZ2 track the amplified offset voltage of gain stage A1 and capacitors CAZ3 and CAZ4 do the same for A2. At the beginning of a conversion cycle, the autozeroing switches open and the instantaneous amplified value of both the DC offset voltage and the low-frequency flicker noise is stored on the coupling capacitors to produce zero comparator offset during a conversion cycle.

SUCCESSIVE APPROXIMATION CONVERSION PROCESS

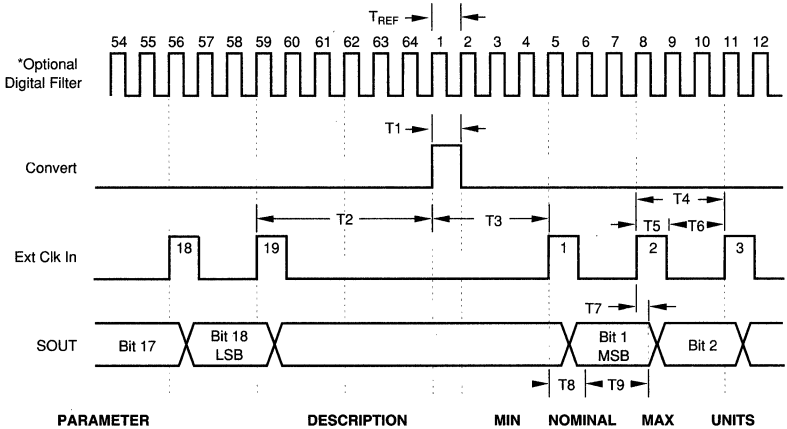
The timing diagram in Figure 2 illustrates the successive approximation routine of the PCM1750. Control signals CONVERT and CLK are derived from a master system clock which comes from a $256f_S$ (256 X the base sampling frequency of 48kHz) clock used by the optional digital filter. There are 64 clocks shown in the timing diagram because the PCM1750 is shown operating at 4 times the standard 48kHz sample rate (192kHz).

Several events occur on the rising edge of the CONVERT command. Switches AZ1 to AZ4, H1 and H2 open and switch S1 reconnects the MSB capacitor, C1, from V_{IN} to analog common (see Figure 1). This terminates the comparator auto-zero cycle and simultaneously switches (co-phase sampling) both converters from tracking their respective input signals into the HOLD mode, thus capturing the instantaneous value of V_{IN} (with a small delay specified as the aperture time).

At the start of a conversion cycle when S1 is switched to analog common, the sampled input signal V_{IN} will appear at the comparator input as $-V_{IN}/2$ due to the 2-to-1 capacitive divider action of C1 = C2 + C3 + ... C18. In a somewhat similar manner, V_{REF} is transferred to the comparator input as $-V_{REF}/2$ to create a bipolar offset.

The 19-bit shift register, shown in Figure 4, controls testing of the bits of the dual ADCs beginning with bit-1 (MSB) and proceeding one bit at a time to bit-18 (LSB), leaving ON those bits that don't cause the cumulative value of the CDAC to exceed the original input value and leaving OFF those bits that do. Since the bits of both channels are tested together, only one shift register is required to control both ranks of 18 data latches.

For example, the testing of bit-2 proceeds in the following manner. The positive pulse from the second shift register element SR2, (see Figure 2 and 4) is applied to the bit-2 data latch and NOR gate. The NOR gate in turn drives S2 and switches bit-2 at the beginning of the bit-2 test interval. Note that the bit interval must be long enough to allow both the comparator input to settle and the comparator to respond. On



PARAMETER		DESCRIPTION	MIN	NOMINAL	MAX	UNITS
T1	(1 x TREF)	Convert Command High	24	33	55	% of T4
T2	(6 x TREF)	S/H Acquisition Time	420	486		ns
T3	(4 x TREF)	Convert to Clock time	281	326	1302	ns
T4	(3 x TREF)	Master Clock Input	211	244	977	ns
T5	(1 x TREF)	Clock High	24	33	55	% of T4
T6	(2 x TREF)	Clock Low	45	67	76	% of T4
T7		Data Hold Time	10			ns
T8		Data Setup Time			100	ns
T9		Data Valid Time	120	154	1212	ns
TCONV	(64 x TREF)	Conversion Throughput Time	4.5	5.2	20.8	µs
TREF	(Sample Rate /64)	Ext Digital Filter Clock	70	81	326	ns

Note: The nominal timing shown in this diagram is all done automatically by the DF1750 digital filter. Only the optional digital filter clock is required when the DF1750 is used.

FIGURE 3. PCM1750 Setup and Hold Timing Diagram.

the next rising edge of CLKIN, at the end of the test interval, the comparator latch is strobed, providing a feedback logic level which tells the second data latch if bit-2 should be kept or rejected. This logic level is stored in the data latch and is passed on to switch S2 via the NOR gate on the falling edge of the pulse from SR2. This decision to keep or reject bit-2 moves the comparator input closer to a null condition, namely, zero potential. This sequential process continues for bit-3 through bit-18 and nulls the comparator inputs to within a value limited by the total system noise and the resolution/speed of the comparator.

Notice from the timing diagram in Figure 2 that the successive approximation algorithm operates synchronously with an external clock to minimize digitally-coupled switching noise from corrupting either the sample-to-hold operation or the critical comparator bit decisions. The two serial output data streams are derived synchronously from the respective latched comparator outputs and are available after a delay of one CLKIN cycle as illustrated in Figure 2. The serial output driver cells are TTL and CMOS compatible.

DIFFERENTIAL LINEARITY CALIBRATION

To understand the calibration of the PCM1750 it is necessary to discuss some of the characteristics of poly-poly capacitors. Poly capacitors are known to have equal or better stability and matching properties when compared to other precision components such as thin film resistors. On a well controlled process, ratio matching is typically 0.1%—a very respectable number for an untrimmed component. Even more impressive is their ratio tracking versus temperature of approximately 0.1ppm/°C.

Achieving DLE (differential linearity error) of less than 1/2 LSB at the 16-bit level requires ratio matching of the more significant bits to about 0.001%. Since the untrimmed ratio matching of poly capacitors is about two orders of magnitude larger than this requirement, a one-time factory calibration of the upper bits is required as described in the next section. Next, consider the effect of temperature due to the ratio tracking of 0.lppm/°C. Over a 50°C span, DLE will change less than 1LSB at 18-bits; therefore, recalibration at temperature extremes is not necessary. Because of this excellent stability versus temperature (and versus time, also), the one-time factory calibration to correct initial DLE is more than satisfactory in meeting the accuracy requirements of the PCM1750.

TDAC OPERATION

Operation of the TDAC (trim DAC), which is laser trimmed at the wafer level, is described using bit-1 as an example. Switch S1T (see Figure 1) operates between two voltage levels—a reference level set by voltage divider Ra, Rb and a laser trimmable level set by R1a, R1b. The differences of these two levels is coupled by capacitor C1T to the minus input of the comparator to generate a correction voltage for

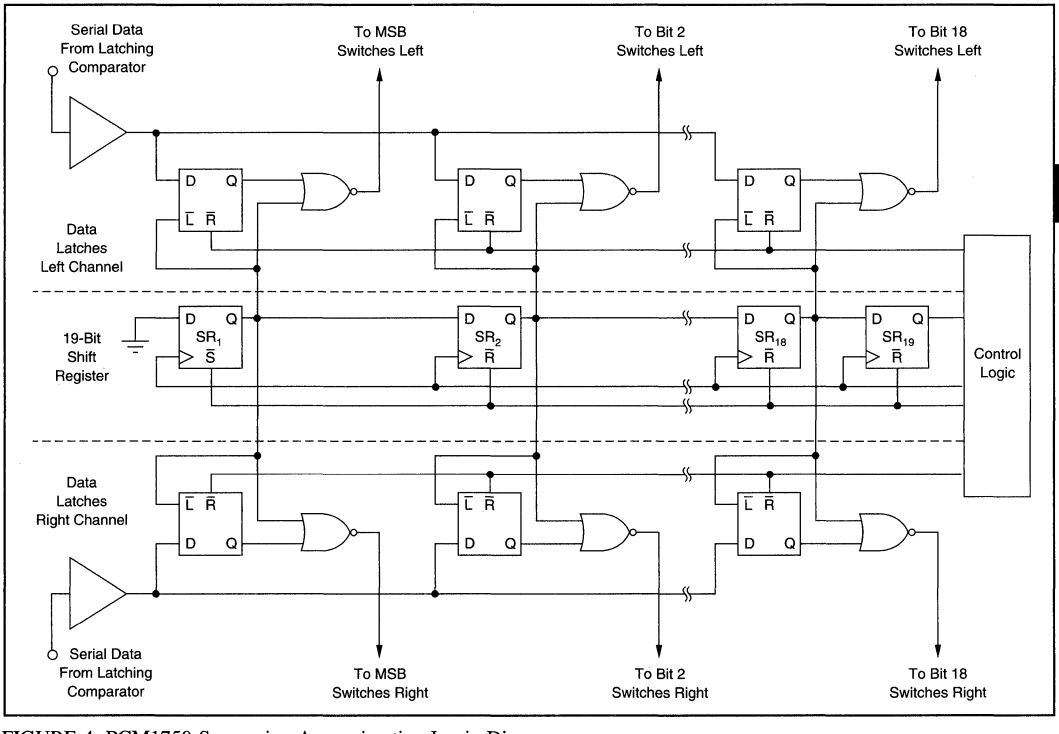


FIGURE 4. PCM1750 Successive Approximation Logic Diagram.

bit-1. The switches of the CDAC and the switches of the TDAC operate concurrently with each other, that is, when a decision is made to keep or reject bit-1, the same decision is made for the correction voltage for bit-1. Even though the ratio stability of the nichrome resistors used in the TDAC may not be as good as the poly capacitors, it is inconsequential because the correction voltage of each bit has a limited range of adjustment.

The DLE at the major carry (a code change from 111...111 to 000...000; in binary two's complement coding) is typically ±1/2 LSB at the 16-bit level, which is sufficient to provide 90dB SNR and –30dB low level distortion (–60dB input). For applications requiring less DLE at the major carry, a pin is provided for each channel to make an external MSB adjustment.

DISCUSSION OF SPECIFICATIONS

RESOLUTION AND DYNAMIC RANGE

The theoretical resolution of the PCM1750 is 18-bits. The maximum possible number of output codes or counts at 18-bits is 262,144 or 108dB (calculated by raising 2 to the 18th power). The relative accuracy of any A/D converter, however, is more a function of it's absolute linearity and signal-to-noise ratio than how many bits of resolution it has. These more pertinent specifications are described later in this section.

Dynamic range, as it is usually defined for digital audio converters, is the measure of THD+N at an effective input signal level of –60dB referred to 0dB. For the PCM1750 this value is typically 90dB and a minimum of 88dB (for audio bandwidth = 20Hz to 24kHz, THD+N at –60db = –30 db typ, –28dB max; f_{IN} = 1kHz and f_S = 192kHz). Resolution is also commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels.

ANALOG INPUT RANGE

The analog input range for the PCM1750 is a bipolar ±2.75V (nominal). Table I gives the precise input/output and voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format. It should be noted that the computed voltage input levels represent center values (the midpoint between code transitions). Output coding is in binary two's complement.

DIGITAL OUTPUT	ANALOG INPUT	VOLTAGE INPUT
262144 LSBs	Full Scale Range	5.50000000V
1 LSB	Minimum Step Size	20.98083496µV
$1FFFF_{HEX}$	+Full Scale	+2.74997902V
00000_{HEX}	Bipolar Zero	0.00000000V
$3FFFF_{HEX}$	Bipolar Zero –1LSB	–0.00002098V
20000_{HEX}	–Full Scale	–2.75000000V

TABLE I. Analog Input to Digital Output Relationships.

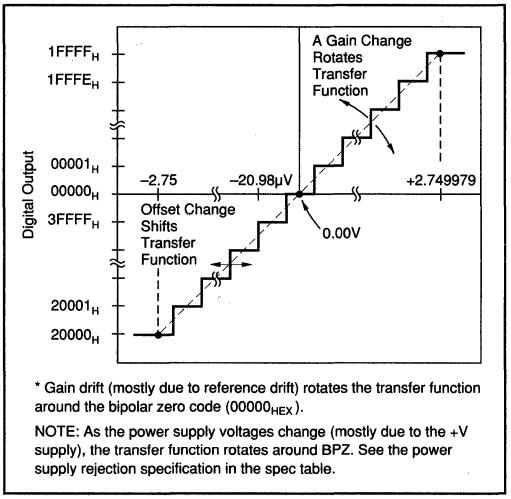


FIGURE 5. Analog Input to Digital Output Diagram.

From Figure 5, the effects of offset and gain errors can be visualized. These errors can change value in response to changes in temperature and/or supply voltage. In addition, gain error (or the full scale range, FSR) changes in direct proportion to the $VREF_{IN}$ voltage value.

SAMPLE AND HOLD PARAMETERS

Aperture Delay and Uncertainty

Aperture delay is the time required to switch from the SAMPLE to HOLD mode. This time is typically 10ns for the PCM1750 and it is constant. Aperture uncertainty (jitter) is the amount of uncertainty associated with the aperture delay. Aperture uncertainty affects the overall accuracy of the converter and is greatest at the maximum input frequency of the converter. The formula for determining the maximum input frequency (f_{MAX}) for a given error contribution due to aperture uncertainty is: $f_{MAX} = (2 \times \pi \times t_{jitter} \times 2^N)^{-1}$ where t_{jitter} is the RMS aperture uncertainty and 2^N is the desired SNR (signal-to-noise ratio) expressed in total number of quantization levels. A 15-bit SNR, therefore, would be expressed as 2^{15} or 32768. Using the typical PCM1750 aperture jitter of $50ps_{rms}$ and an SNR at the 15-bit level, $f_{MAX} = (2 \times \pi \times 50ps \times 32768)^{-1}$ or 97.1kHz. This matches very closely with the rated dynamic accuracy of the PCM1750 where THD+N = –88dB max. This means the typical aperture jitter of PCM1750 only becomes a factor when input signals to it exceed 97kHz and/or an SNR greater than 15 bits is desired.

Input Bandwidth

The full power bandwidth of the PCM1750 is that input frequency above which significant distortion is observed (THD+N > 10-bits or –60dB for a full scale input signal). In the data sheet, this number is specified as typically being 500kHz. In wideband operation (when no digital filter is used) the additional full power bandwidth of the PCM1750

can be used to purposely alias a band-limited signal down into the baseband of the converter. This technique is called undersampling and can be used to directly down-convert an intermediate frequency riding on a much higher carrier frequency.

DIGITAL I/O AND TIMING

Input/Output Logic Compatibility

Digital logic on the PCM1750 is CMOS compatible. Digital outputs on the PCM1750 are capable of driving a minimum of two standard TTL input loads.

Digital output coding is in binary two's complement. Table I gives the precise input/output voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format.

Convert Command and External Clock Input

A conversion is initiated on its positive going edge of the convert command. Although the convert command can return low at any time (prior to 50ns before the rising edge of the 19th clock), a typical convert command pulse width of 81ns (as called out in Figure 3) is specified for a 192kHz sample rate (f_S). The reason for a pulse width spec is to reduce problems associated with digital logic feedthrough noise. The return of convert command to a logic low level in the specified time interferes least with the successive approximation process. Also, it should be noted that putting fast logic edges (<5ns) on convert command (P11) and the external clock input (P4) may cause logic feedthrough to the analog stages in the converter and will result in added distortion during the sampling and conversion process. Using the optional DF1750 digital filter provides adequately slow transitions to maintain full specification performance. If necessary, an external RC, on the convert command line may be used to slow fast logic edges.

As with the convert command, the external clock input is positive edge triggered and is not duty-cycle dependent other than to improve digital feedthrough noise immunity. A 50% duty cycle clock can be used instead of 33% if desired. Refer to Figure 3 for recommended timing relationships. Regardless of what clock duty cycle is used, all operations relating to valid data clocking should be synchronized to the rising edge of the clock input.

Although there is a maximum conversion time called out in the specification table, the PCM1750 can have a considerably longer conversion cycle. Droop of the internal capacitors will ultimately determine what the true maximum conversion time can be. The min/typ/max times shown in Figure 3 are based on minimum sample rate of 48kHz, a typical of 192kHz, and a maximum of 222kHz. All specifications are tested at 192kHz. The minimum sample rate assumption is based on clock periods that increase as time between convert commands increases. Any sample rate down to near DC can be utilized by observing maximum clock cycle requirements and spacing convert commands to achieve lower sample rates. This means that the time interval T2 shown in Figure 3 does not have a maximum value.

Clock Lockout

Any number of clocks can be given to the PCM1750 beyond the 19 required for normal operation. If a continuous clock is used, all clocks beyond the 19th are gated off by the PCM1750's internal logic until the next positive going edge of the convert command. The converter also goes into the sample (track) mode starting on the positive edge of the 19th clock until the next positive edge of the convert command, regardless of how many additional clocks are offered. The ideal operation of the converter stops the clock input after the 19th during this critical signal acquisition time. This is the timing shown in Figure 3 . The critical timing aspect that must be observed if a clock input other than the recommended is used, is that ample time following the positive edge of convert command proceed the next rising clock edge. If this time is shortened, the most important bit-1 (MSB) decision, which is finalized on the first clock edge after convert command, will be adversely affected. In other words, the clock input cannot have a rising edge during the time interval T3 shown in Figure 3.

SIGNAL-TO-NOISE RATIO

Another specification for A/D converters is signal-to-noise ratio (SNR). For this measurement, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz. An FFT is performed on the digital output and the noise power in the non-harmonic audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

One advantage of using the PCM1750 in this oversampled mode with the optional DF1750 digital decimation filter is that the converter noise is spread over the full 0Hz to 96kHz passband and then suppressed by the digital filter stopband attenuation (from 24kHz to 96kHz). This effectively increases the SNR of the PCM1750 by 6dB when it is used as an audio bandwidth converter. The other advantage is that the need for a higher-order anti-aliasing input filtering is greatly reduced.

THD + N

The key specification for the PCM1750 is total harmonic distortion plus noise (THD+N). In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS}$ + $Noise_{RMS}$ / $Signal_{RMS}$ expressed in dB. For the PCM1750, THD+N is 100% tested at all three specified input levels using the production test setup shown in Figure 6. For this measurement, as with the SNR test, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz (which is 4X the standard digital audio sample rate of 48kHz). An FFT is performed on the digital output and the total power in all audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

For the audio band, the THD+N of the PCM1750 is essentially flat for all frequencies and input signal levels. In the *Typical Performance Curves* THD+N versus Frequency

plots are shown at four different input signal levels (with and without a 4X decimation filter): 0dB, –20dB, –40dB, and –60dB.

CHANNEL SEPARATION

To test channel separation a 1kHz signal sampled at 192kHz is placed on one input of the PCM1750 while the other input is held at 0V. An FFT is performed on the idle (0V) channel and the result checked to insure that the 1kHz tone is suppressed by a minimum of 96dB.

GAIN AND OFFSET ERRORS

Initial gain and bipolar offset errors are laser trimmed at the wafer level and 100% final tested to insure compliance with the electrical specifications. Bipolar offset errors can be further reduced to zero by using the optional offset adjustment circuitry shown in the connection diagram (Figure 7). Gain errors can be adjusted by varying V_{REF} to either channel of the converter. This is accomplished by either using an adjustable external reference or by placing buffer amplifiers with adjustable gain between $VREF_{OUT}$ and $VREF_{IN}$ as shown in Figure 8a.

INTEGRAL AND DIFFERENTIAL LINEARITY

DC Linearity Testing

The absolute linearity of the PCM1750 is on the order of 15 bits or more as can be seen from the THD versus Frequency plots in the *Typical Performance Curves*. Not every code in the converter must be 15-bit linear to achieve the specified THD+N performance, but a very high percentage will be that linear. The same observation also applies to differential linearity errors in the PCM1750. Because the PCM1750 is not 100% tested for DC linearity specifications, no minimum or maximum specifications are given for integral or differential linearity errors.

No Missing Codes Operation

A no missing codes specification is not given for the PCM1750 for the same reasons as given above. The PCM1750, however, typically has fewer than 16 codes (less than 0.01%) missing at a 14-bit resolution level. A 100% no missing codes specification cannot be maintained above the 12-bit level, although this has very little impact on overall dynamic performance (THD+N). The few missing codes that do occur at higher resolution levels are at the bit-2 and lower major carry transitions of the converter. There are typically no missing codes (at 14 bits) around the critical bipolar zero operation zone (±1/8 of full scale range around bipolar zero or 0V). The critical bipolar differential linearity error can be reduced from its initial value to zero using the optional MSB adjustment circuitry shown in the connection diagram (Figure 7).

REFERENCE

The gain drift of the PCM1750 is primarily due to the drift associated with the reference. Better drift performance can be achieved using an external reference like the ones explained in the applications section (Figures 8b, 8c). The *Typical Performance Curves* plot of V_{REF} Output versus Temperature shows the full range of operation including initial error and typical gain drift. Pertinent performance data are found in the electrical specification table.

Reference Bypass

Both P18 and P25 ($VREF_{IN}$) should be bypassed with a 10µF to 47µF tantalum capacitor. If there are important system reasons for using the PCM1750 reference externally, the outputs of P19 and P24 must be appropriately buffered, and bypassed (see Figure 8).

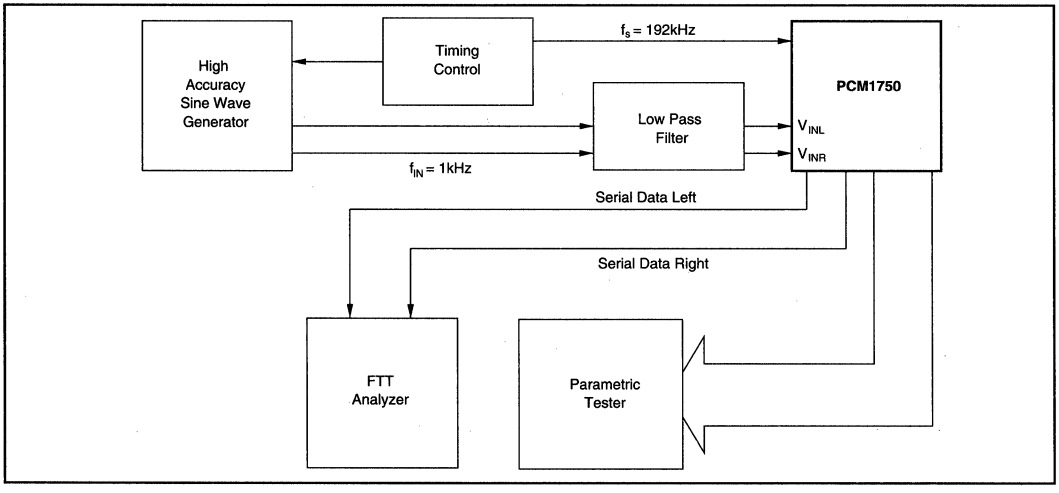


FIGURE 6. PCM1750 Production Test Setup.

POWER SUPPLY REJECTION

Because of the architecture of the PCM1750, power supply rejection varies with input signal size. The spec table value is expressed in the relative terms of percent of V_{IN} per percent change of the supply voltage. The PSR versus Frequency plot in the *Typical Performance Curves* show PSR expressed versus an increase in power supply ripple frequency.

PERFORMANCE OVER TEMPERATURE

Specification Temperatures

All critical specifications are tested at 25°C. The drift specification temperature range is from 0°C to +70°C. The PCM1750 will operate over the wider temperature range of –40°C to +85°C.

Gain and Offset Drift

Although the PCM1750 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC drift parameters such as temperature gain and offset drift. The primary cause of drift in the PCM1750 is the bandgap reference. Much lower gain drift can be realized if necessary by using any circuit similar to the external reference circuits shown in Figure 8. Also, refer to the *Typical Performance Curves* of V_{REF} Output versus Temperature.

Dynamic Performance

Dynamic performance is predominated by the absolute linearity of the PCM1750. Because of the excellent ratio tracking versus temperature of poly-poly capacitors, there is virtually no change in dynamic performance of the converter over temperature (primarily THD+N). The dynamic specifications over temperature cannot be guaranteed, however, as they are not 100% tested.

INSTALLATION

ANTI-ALIASING FILTER

To prevent unwanted input signals from being aliased into the passband of the converter, it is necessary to suppress all out of band signals above 1/2 the sampling frequency of the ADC by using a low-pass filter. The requirement for an anti-aliasing filter, however, can be reduced by using oversampling techniques. By raising the sample rate of the converter by a factor of 2 or even 4, the roll off of the anti-aliasing filter can be reduced. In Figure 9, a 6th order, linear-phase, anti-aliasing filter is implemented using low-cost dual audio op amps. This filter will suppress frequencies above 96kHz by 80dB. For many applications a 4th or 2nd order anti-aliasing filter will be adequate when using the PCM1750 in the 4x oversampling mode.

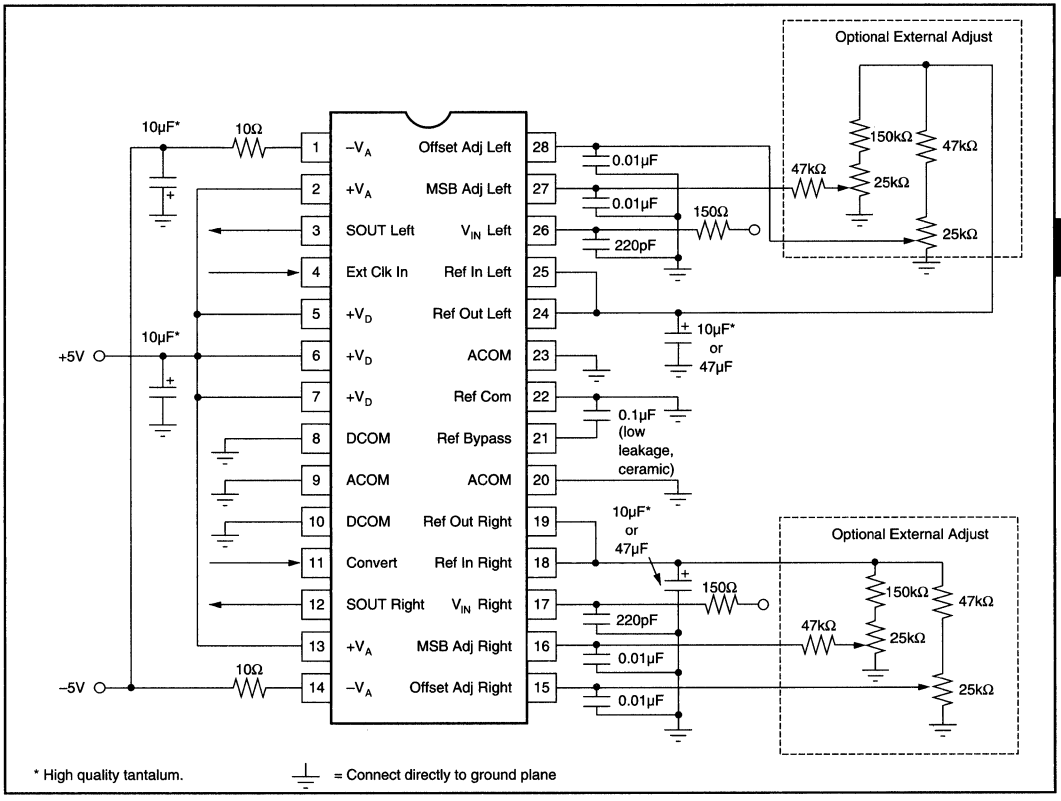


FIGURE 7. PCM1750 Connection Diagram.

INPUT SIGNAL CONDITIONING

RC Input Circuit

Note the 150Ω resistors and 220pF capacitors on each analog input as shown in the connection diagram (Figure 7). This input circuit configuration is required to achieve optimum SNR performance of the PCM1750. Various other component values will yield satisfactory results, but the resistor should never exceed 200Ω.

Buffer Amplifier

To avoid introducing distortion, the PCM1750 input must be driven by a low active impedance source (op amps such as the NE5532, Burr-Brown OPA2604, or equivalent are ideal).

EXTERNAL ADJUSTMENTS

The simplified circuit diagram (see Figure 1) shows one of two complete channels on the PCM1750. The input switched capacitors, trim DAC and comparator are detailed. The trim DAC switches are activated whenever the corresponding bit is chosen during the successive approximation routine. The first 12 bits of the ADC have corresponding trim DAC circuits. The R1a to R12a and R1b to R12b resistors can be laser trimmed at the wafer level if necessary to correct for any nonlinearities. The nominal voltage for the internally generated V_{REF} is 2.75V and it is a relatively low impedance, buffered voltage output. It should be noted that just the act of connecting the optional adjustment circuits will affect the MSB DLEs and bipolar offsets since it is unlikely that the initial potentiometer settings (even if centered) would match the factory trimmed null potentials. If connected, the potentiometers must be properly adjusted.

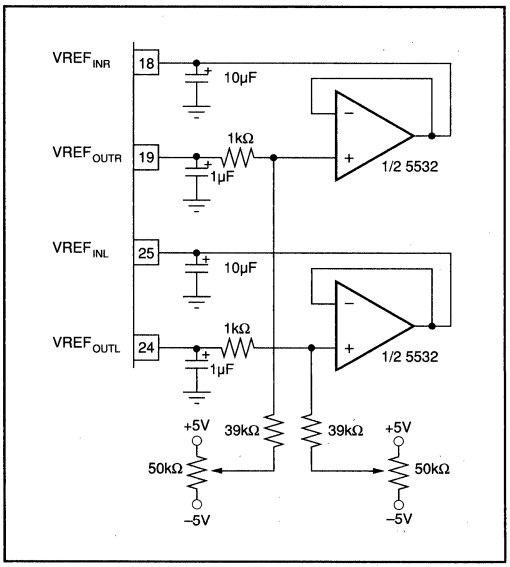


FIGURE 8a. Circuit for External Gain Adjustment Using the Internal Reference.

MSB Adjust

The MSB adjust pin connects to the center of the R1a/R1b resistive divider for bit-1. After laser trimming this point is nominally 100mV. All the MSB and offset adjust pins should be connected to ground using a 0.01µF capacitor, especially if traces to the potentiometers are long. If the adjust pins are not used, they should still be bypassed to ground.

Since there are internal 5kΩ resistors and clamp diodes to both ground and +5V on the MSB and offset adjust pins, there are obvious limits to their range of adjustment. With a nominal internal voltage on these points of +100mV, there will be a greater limitation in making negative adjustments than positive. A negative voltage at either adjustment pin, however, is acceptable up to one diode drop (–0.6V) below ground.

The preferred method of MSB DLE adjustment is to input a small level signal and adjust for minimum THD+N.

Offset Adjust

The offset adjust switch (S_{OFF}) position is controlled by whether the ADC is in the sample or hold mode. Switching from sample to hold effectively allows any charge offsets associated with the sampling process to be eliminated. Grounding the input to the converter as far ahead of the A/D as possible (in front of the anti-aliasing filter for example) and then adjusting the bipolar zero error will remove the offsets associated with the entire sampling system.

LAYOUT CONSIDERATIONS

Power Requirements

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used. Although the PCM1750 positive supplies have separate digital and analog +5V, for most applications the +5V digital supply pins should be connected to the +5V analog supply. If they aren't connected together, a potential latchup condition can occur when the power supplies are not turned on at the same time. If one supply pin is powered and the other is not, the PCM1750 may latch up and draw excessive current. In normal operation, this is not a problem because both $+V_A$ and $+V_D$ should be connected together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "hot" socket exists, care should be taken to power the PCM1750 only after it has been socketed.

All supplies should be bypassed as shown in Figure 7. The bypass capacitors should placed as close to their respective supply pins as possible. Additional .01µF capacitors may be placed in parallel with the larger value capacitors to increase high-frequency rejection, but generally they are not required when high quality tantalums are used. The 0.1µF capacitor between P21 and P22 should be a low leakage type (such as ceramic) and must be put as close to these pins as possible to reduce noise pickup.

The PCM1750 is sensitive to supply voltages outside the absolute maximum ratings shown in the specification tables. Do not exceed –8V on the negative supplies at any time or irreversible damage may occur. Note the 10Ω resistors in series with each –5V supply line (shown in Figure–7) to help protect the part from severe damage if the supplies are over-ranged momentarily.

Grounding Requirements

Because of the high resolution and linearity of the PCM1750, system design problems such as ground path resistance and contact resistance become very important.

The ACOM and DCOM pins are separated internally on the PCM1750. To eliminate unwanted ground loops, all commons (both analog and digital) should be connected to the same low-impedance ground plane. This should be an analog ground plane separate from other high-frequency digital ground planes on the same board. If the analog and digital commons of the PCM1750 are connected to different ground planes, care should be taken to keep them within 0.6V of each other to insure proper operation of the converter.

A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signals should be referenced to the ACOM pins. This will prevent voltage drops in the power supply returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external MSB and offset adjust potentiometers are used, the potentiometers and related resistors should be located as close to the PCM1750 as possible.

Minimizing "Glitches"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. Care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the PCM1750 has an internal sample/hold function, the signal that switches it into the HOLD state (CONVERT going HIGH) is critical, as it would be on any sample/hold amplifier. The CONVERT rising edge should have minimal ringing, especially during the 20ns after it rises.

APPLICATIONS

USING A DIGITAL FILTER

A 4x decimation filter is available for the PCM1750 called the DF1750. It is available in a 28-pin DIP or a 40-pin SOIC package. The use of this filter greatly eases the implementation of the PCM1750 in audio band applications.

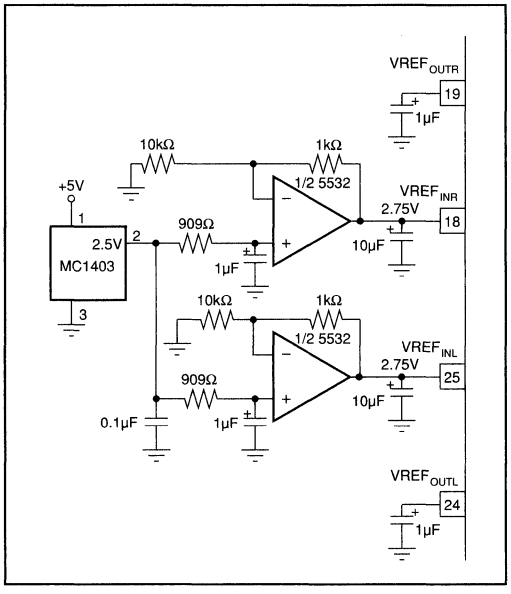


FIGURE 8b. External Reference Circuit Using Standard 2.5V Reference.

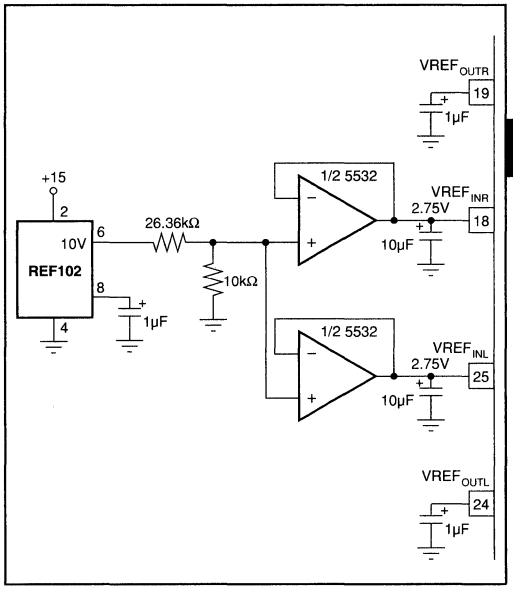


FIGURE 8c. Low Noise, Low Drift External Reference Circuit.

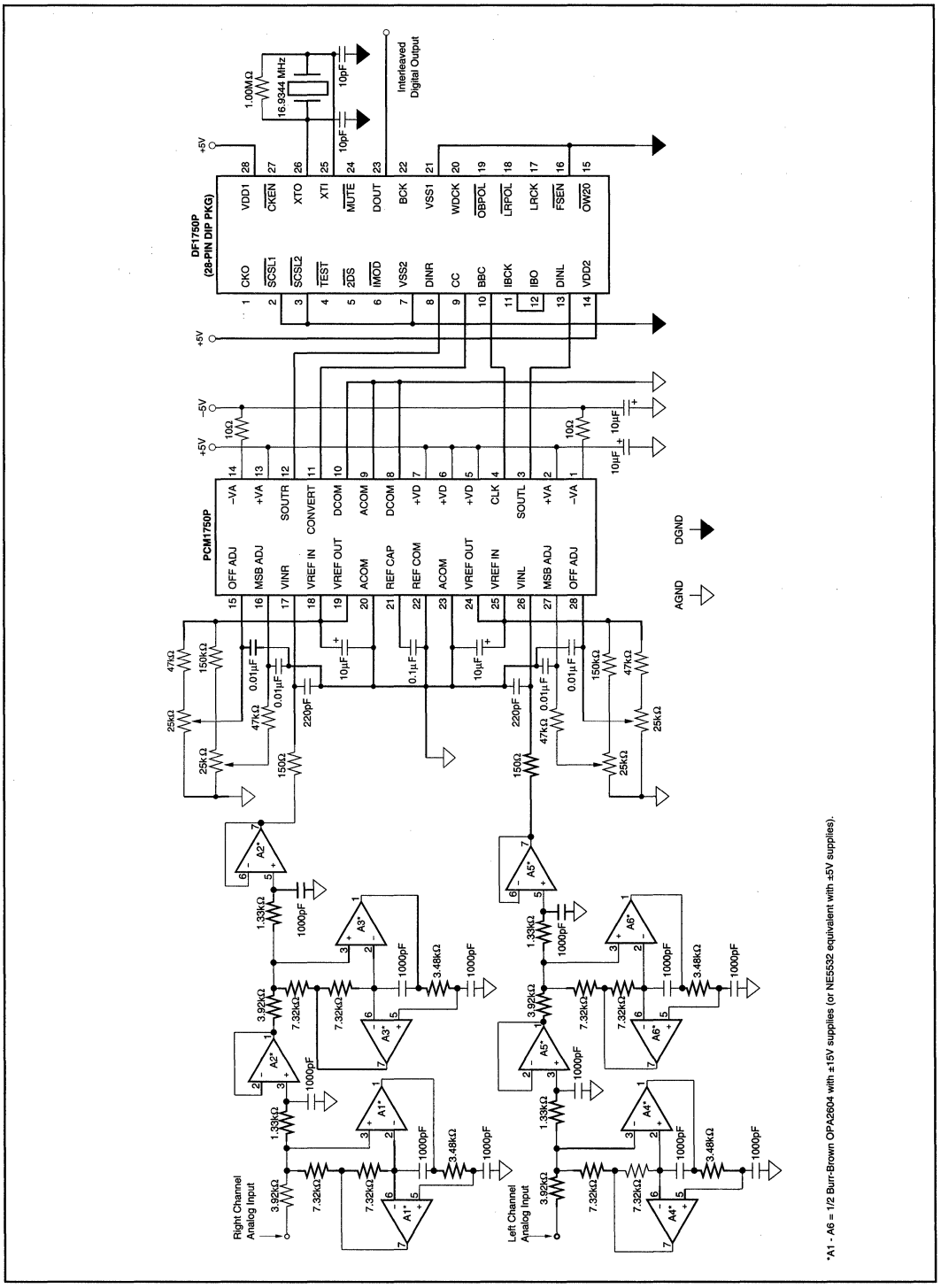


FIGURE 9. Complete Sampling A/D Circuit with Anti-aliasing and Digital Filter (44.1kHz output data rate).

USING AN EXTERNAL REFERENCE

Normally $VREF_{OUT}$ is connected directly to $VREF_{IN}$. The typical value for V_{REF} versus Temperature is shown in the *Typical Performance Curves*. If better drift or power supply rejection performance is desired, one of the external reference circuits shown in Figures 8b and 8c can be used. Note that the decoupling capacitors are still connected to $VREF_{IN}$. External gain adjustment is now possible by using the variable output options available on some precision voltage references or by varying the gain on external buffer amplifiers. The range of acceptable external references is from +2.0V to $+V_A$ – 2.0V, with 2.5V types being the most commonly available. Full scale input voltage range will be $\pm VREF_{IN}$ (a +2.5V $VREF_{IN}$ results in a ±2.5V input range).

If an external reference is used, P19 and P24 must be bypassed with at least 1µF capacitors.

SAMPLING A/D SYSTEM

Figure 9 is a partial schematic of the demonstration fixture for the PCM1750 (orderable by model number DEM1133). It shows the implementation of (1) a 6th order, linear-phase, anti-aliasing filter (22kHz low-pass); (2) the PCM1750P A/D converter; and (3) a 4x digital decimation filter called the DF1750P. Not shown on this schematic, but included on the demo fixture, are latched parallel data outputs with strobe and a serial digital interface format (SPDIF) data transmitter. Also included on the DEM1133 are user breadboard areas for application specific circuit implementation.

CONNECTION TO DSP WITH DIGITAL FILTER

The PCM1750 and DF1750 combination can be connected to the serial ports of most popular DSP processor ICs (such as those made by AT&T, Motorola, TI, and AD) by adding a small amount of external glue logic. Figures 10 and 11 show the timing diagram and schematic for this interface.

To use this interface, the DSP processor IC must be configured for 32-bit word inputs. The glue logic generates a flag bit, as the first bit of the 32-bit word, that signifies either left or right channel data. The flag bit will be low for left channel data and high for right channel data.

The DF1750 can be configured for either 16- or 20-bit data, although only 16-bit data is shown in Figure 10. After the data is transferred into the DSP processor IC, it must be shifted toward the LSB by one bit in order to compensate for a clock delay in the glue logic.

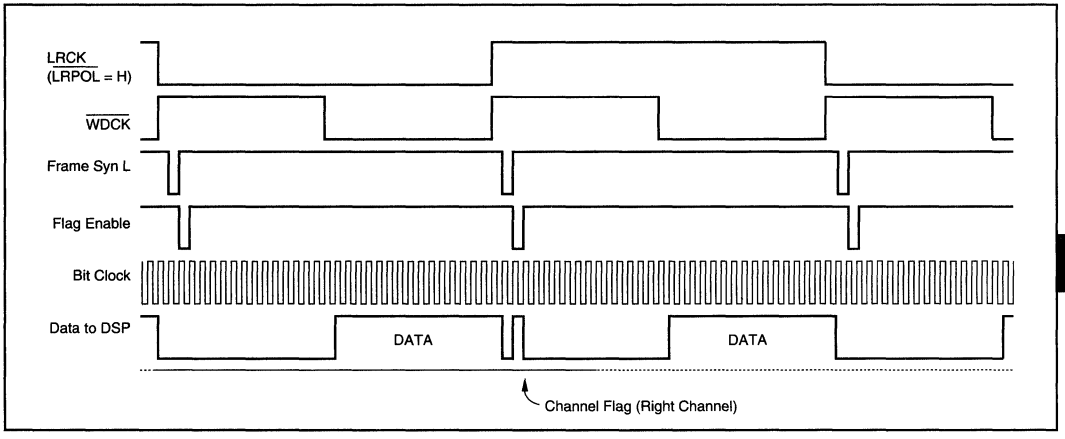


FIGURE 10. PCM1750/DF1750 To DSP IC Timing Diagram.

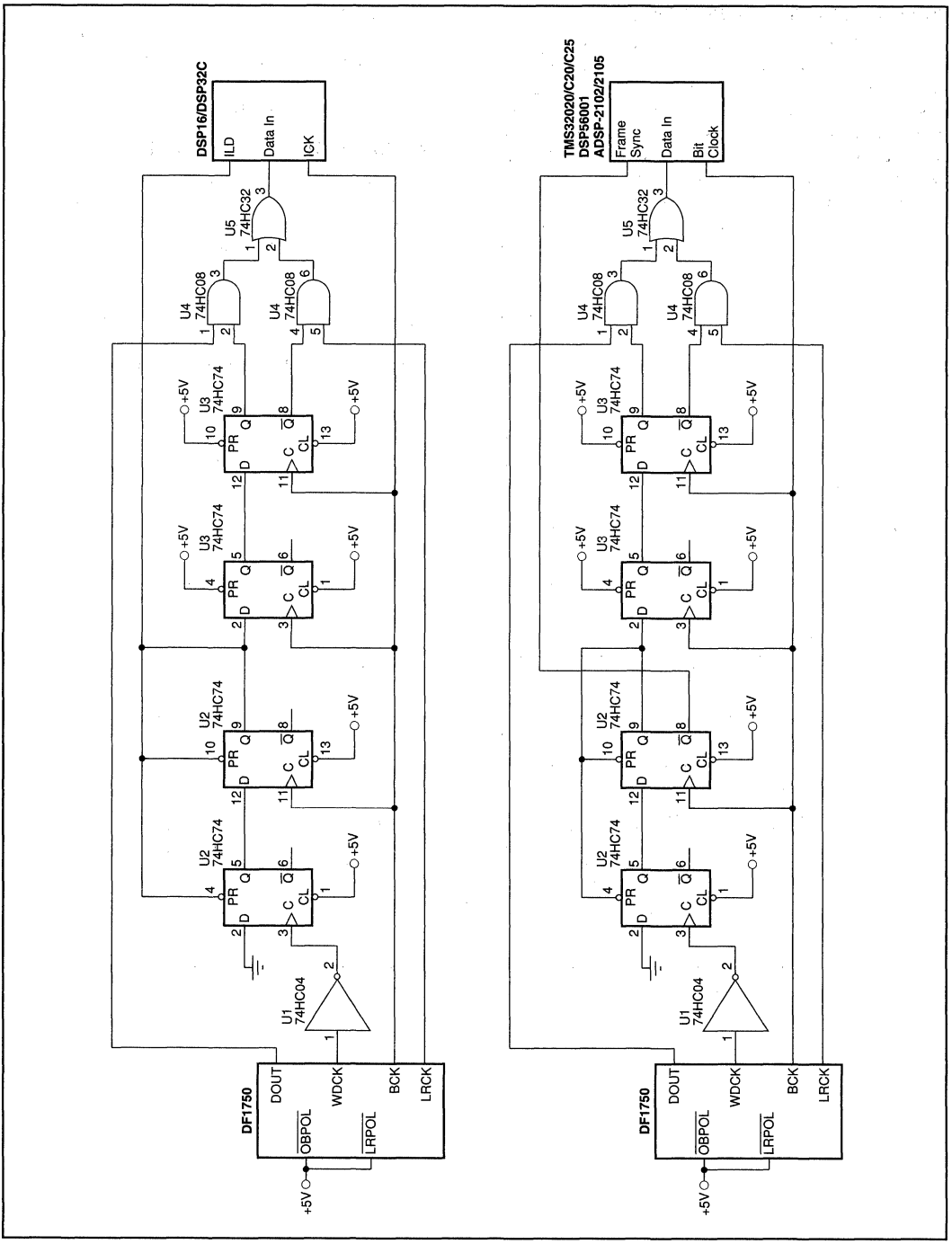


FIGURE 11. PCM1750/DF1750 to DSP IC Schematic.

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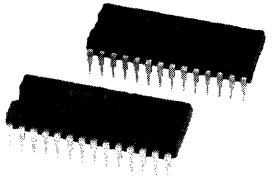


PCM1760P/U
DF1760P/U

DEMO BOARD AVAILABLE
See Appendix A

Multi-Bit Enhanced Noise Shaping 20-Bit ANALOG-TO-DIGITAL CONVERSION SYSTEM

FEATURES

- **DUAL 20-BIT MONOLITHIC MODULATOR (PCM1760) AND MONOLITHIC DECIMATING DIGITAL FILTER (DF1760)**
- **HIGH PERFORMANCE:**
  THD+N: –92dB typ, –90dB max
  Dynamic Range: 108dB typ
  SNR: 108dB min, 110dB typ
  Channel Separation: 98dB typ, 94dB min
- **64X OVERSAMPLING**
- **CO-PHASE CONVERSION**
- **RUNS ON 256fs OR 384fs SYSTEM CLOCK**
- **VERSATILE INTERFACE CAPABILITY:**
  16-, 20-Bit Output
  MSB First or LSB First Format
- **OPTIONAL FUNCTIONS:**
  Offset Error Calibration
  Overflow Detection
  Power Down Mode (DF1760)
- **RUNS ON ±5V SUPPLIES (PCM1760) AND 5V SUPPLY (DF1760)**
- **COMPACT 28-PIN PACKAGES:**
  28-Pin DIP and SOIC

DESCRIPTION

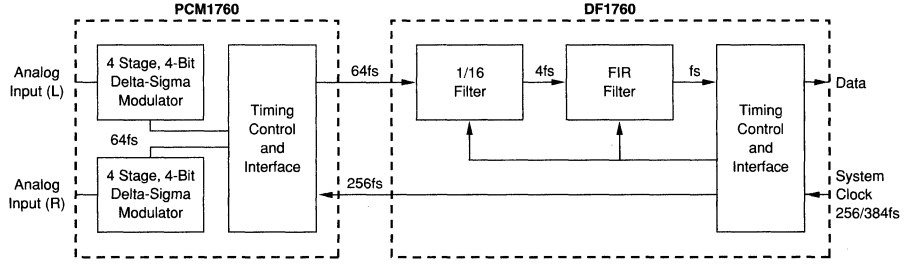
The PCM1760 and DF1760 combine for a low-cost, high-performance dual 20-bit, 48kHz sampling analog-to-digital conversion system which is specifically designed for dynamic applications.

The PCM1760/DF1760 pair form a 4-bit, 4th order, 64X oversampling analog-to-digital converter.

The PCM1760 is a delta-sigma modulator that uses a 4-bit quantizer within the modulation loop to achieve very high dynamic range.

The DF1760 is a high-performance decimating digital filter. The DF1760 accepts 4-bit 64fs data from the PCM1760 and decimates to 20-bit 1fs data.

The FIR filter of the DF1760 has pass-band ripple of less than ±0.001dB and greater than 100dB of the reject band attenuation.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$, $\pm V_{dd}$ = +5V, $+V_{DD}$ = +5V, f_S = 48kHz and ext. components = ±2% unless otherwise noted.

PARAMETER	CONDITIONS	PCM1760/DF1760 MIN	PCM1760/DF1760 TYP	PCM1760/DF1760 MAX	UNITS
RESOLUTION		20			Bits
ANALOG INPUT					
Input Range	$R_{IN}1$ = 2.2kΩ		±2.5		Vp-p
Input Impedance	$R_{IN}1$ = 2.2kΩ		$R_{IN}1$		Ω
SAMPLING FREQUENCY					
Cover Range of fs	Integrator Constants: Application(1)	30	48	50	kHz
ACCURACY					
Gain Error			±0.5	±1.0	dB
Gain Mismatch				±0.5	dB
Bipolar Zero Error	V_{IN} = 0 at 20s After Power-On			±0.4	% FSR(2)
Gain Drift	0°C to +70°C		±100		ppmfs/°C
Bipolar Zero Drift	0°C to +70°C		±20		ppmfs/°C
DYNAMIC CHARACTERISTICS(4)					
THD+N/(0dBFS) P, U	f_{IN} = 1kHz		–92	–90	dB
P-L, U-L			–90	–88	dB
THD+N/(–20dBFS) P, U	f_{IN} = 1kHz		–76	–70	dB
P-L, U-L			–76	–70	dB
THD+N/(–60dBFS) P, U	f_{IN} = 1kHz		–44	–42	dB
P-L, U-L			–44	–42	dB
Dynamic Range P, U	f_{IN} = 1kHz, V_{IN} = –60dBFS, A Filter	104	108		dB
P-L, U-L		104	108		dB
SNR P, U	V_{IN} = 0, A Filter	108	110		dB
P-L, U-L		106	110		dB
Frequency Response	f_{IN} = 20kHz		±0.1		dB
Channel Separation	f_{IN} = 1kHz, A Filter	94	98		dB
DIGITAL FILTER					
Over Sample Rate			64		fs
Ripple in Band	0 - 0.04535fs			±0.0001	dB
Stopband Attenuation –1	0.5465fs - 63.4535fs	–94			dB
Stopband Attenuation –2	0.5465fs - 3.4535fs	–100			dB
LOGIC INPUTS AND OUTPUTS					
Logic Family Input			TTL Level Compatible CMOS		
Frequency (System Clock 1)	256fs		12.288		MHz
Frequency (System Clock 2)	384fs		18.432		MHz
Duty Cycle (System Clock 1)	256fs	40	50	60	%
Duty Cycle (System Clock 2)	384fs	45	50	55	%
Data Clock Input		32	48	64	fs
Logic Family Output			CMOS		
Data Clock Output			64		fs
Data Coding			Two's Complement		
Data Bit Length		16	20		Bits
Data Format			Selectable		
Output Data Delay	fs = 48kHz		1.5		ms
POWER SUPPLY REQUIREMENTS					
Supply Voltage					
$\pm V_{CC}$	PCM1760	±4.75	±5.0	±5.25	V
$\pm V_{dd}$	PCM1760	±4.75	±5.0	±5.25	V
$+V_{DD}$	DF1760	4.75	5.0	5.25	V
Supply Current					
$+I_{CC}$	PCM1760		24	36	mA
$-I_{CC}$	PCM1760		–30	–45	mA
$+I_{dd}$	PCM1760		12	18	mA
$-I_{DD}$	PCM1760		–8	–12	mA
$+I_{DD}$ –1	DF1760, Normal Mode		40	55	mA
$+I_{DD}$ –2	DF1760, Power-Down Mode		4	6.6	mA
Power Consumption	PCM1760		370	500	mW
	DF1760, Normal Mode		200	275	mW
	DF1760, Power-Down Mode		20	33	mW
TEMPERATURE RANGE					
Operating	PCM1760/DF1760	0	+25	+70	°C
Storage	PCM1760/DF1760	–50		+125	°C

NOTES: (1) Integrator Constants are determined by the external components shown in the block diagram. (2) FSR means Full Scale Range, digital output code is from 90000H to 70000H, FSR = 5.0V. (3) Use 20-bit DAC, 20kHz LPF, 400Hz HPF, average response. (4) Average response using a 20-bit reconstruction DAC with 20kHz low-pass filter and 400Hz high-pass filter.

ABSOLUTE MAXIMUM RATINGS—PCM1760

Supply Voltage	±6V
Voltage Mismatch	0.1V
Analog Input	$\pm V_{CC}$
Digital Input	$+V_{DD}$ +0.3V
	GND –0.3V
Power Dissipation/P	580mW
Power Dissipation/U	550mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s)	235°C
Operating Temperature	0°C to +70°C
Storage Temperature	–50°C to +125°C

ABSOLUTE MAXIMUM RATINGS—DF1760

Supply Voltage	7.0V
Voltage Mismatch	0.1V
Digital Input	$+V_{DD}$ +0.5V
	V_{SS} –0.5V
Input Current	±20mA
Power Dissipation/P	460mW
Power Dissipation/U	440mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s, reflow)	235°C
Operating Temperature	0°C to +70°c
Storage Temperature	–50°C to +125°C

ORDERING INFORMATION

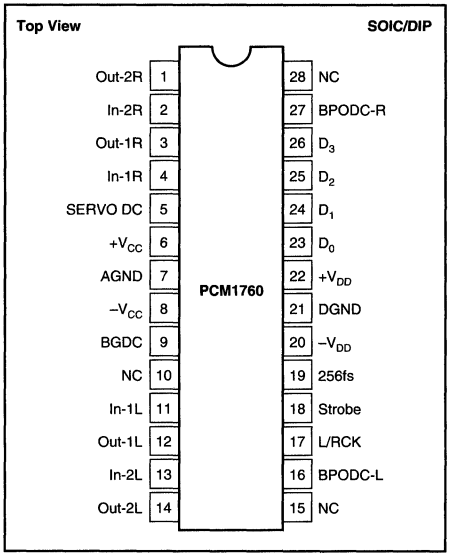
MODEL	PACKAGE	THD +N (fs)	SNR
PCM1760P	PDIP	–90dB	108dB
PCM1760U	SOIC	–90dB	108dB
PCM1760P-L	PDIP	–88dB	106dB
PCM1760U-L	SOIC	–88dB	106dB
DF1760P	PDIP	NA	NA
DF1760U	SOIC	NA	NA

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PCM1760P	28-Pin PDIP	800
PCM1760U	28-Pin SOIC	804
PCM1760P-L	28-Pin PDIP	800
PCM1760U-L	28-Pin SOIC	804
DF1760P	28-Pin PDIP	801
DF1760U	28-Pin SOIC	805

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

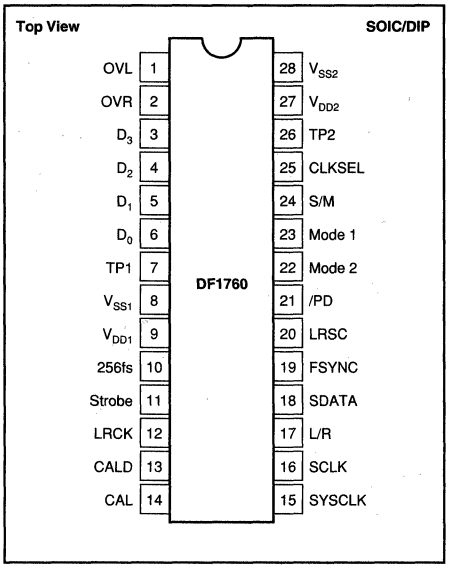
PIN ASSIGNMENTS PCM1760



PIN	I/O[1]	NAME	DESCRIPTION
1	O	Out-2R	Right Channel Second Integrator Output
2	I	In-2R	Right Channel Second Integrator Input
3	O	Out-1R	Right Channel First Integrator Output
4	I	In-1R	Right Channel First Integrator Input
5	–	SERVO DC	Servo Amp Decoupling Capacitor
6	–	$+V_{CC}$	+5V Analog Supply Voltage
7	–	AGND	Analog Common
8	–	$-V_{CC}$	–5V Analog Supply Voltage
9	–	BGDC	Band Gap Reference Decoupling Capacitor
10	–	NC	No Connection
11	I	In-1L	Left Channel First Integrator Input
12	O	Out-1L	Left Channel First Integrator Output
13	I	In-2L	Left Channel Second Integrator Input
14	O	Out-2L	Left Channel Second Integrator Output
15	–	NC	No Connection
16	–	BPODC-L	Left Channel Bipolar Offset Decoupling Capacitor
17	O	L/RCK	LR Clock Output (64fs)
18	O	Strobe	Data Strobe Output (128fs)
19	I	256fs	256fs Clock Input
20	–	$-V_{DD}$	–5V Digital Supply Voltage
21	–	DGND	Digital Common
22	–	$+V_{DD}$	+5V Digital Supply Voltage
23	O	D_0	D_0 Data Output (LSB)
24	O	D_1	D_1 Data Output
25	O	D_2	D_2 Data Output
26	O	D_3	D_3 Data Output (MSB)
27	–	BPODC-R	Right Channel Bipolar Offset Decoupling Capacitor
28	–	NC	No Connection

NOTE: (1) O = Output terminal; I = Input terminal.

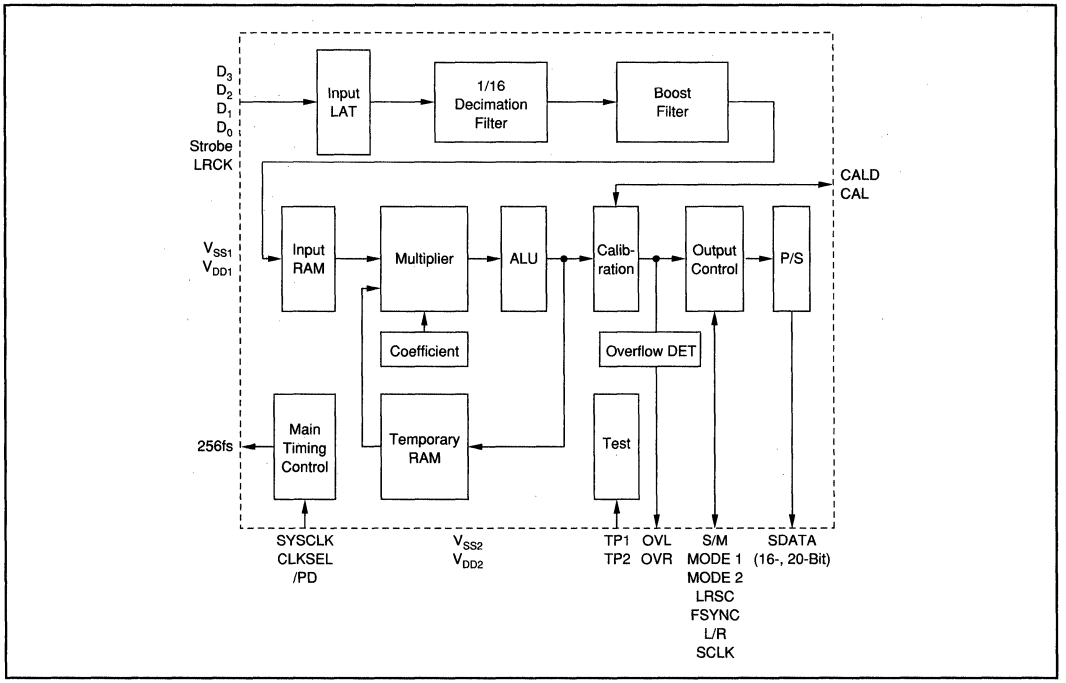
PIN ASSIGNMENTS DF1760



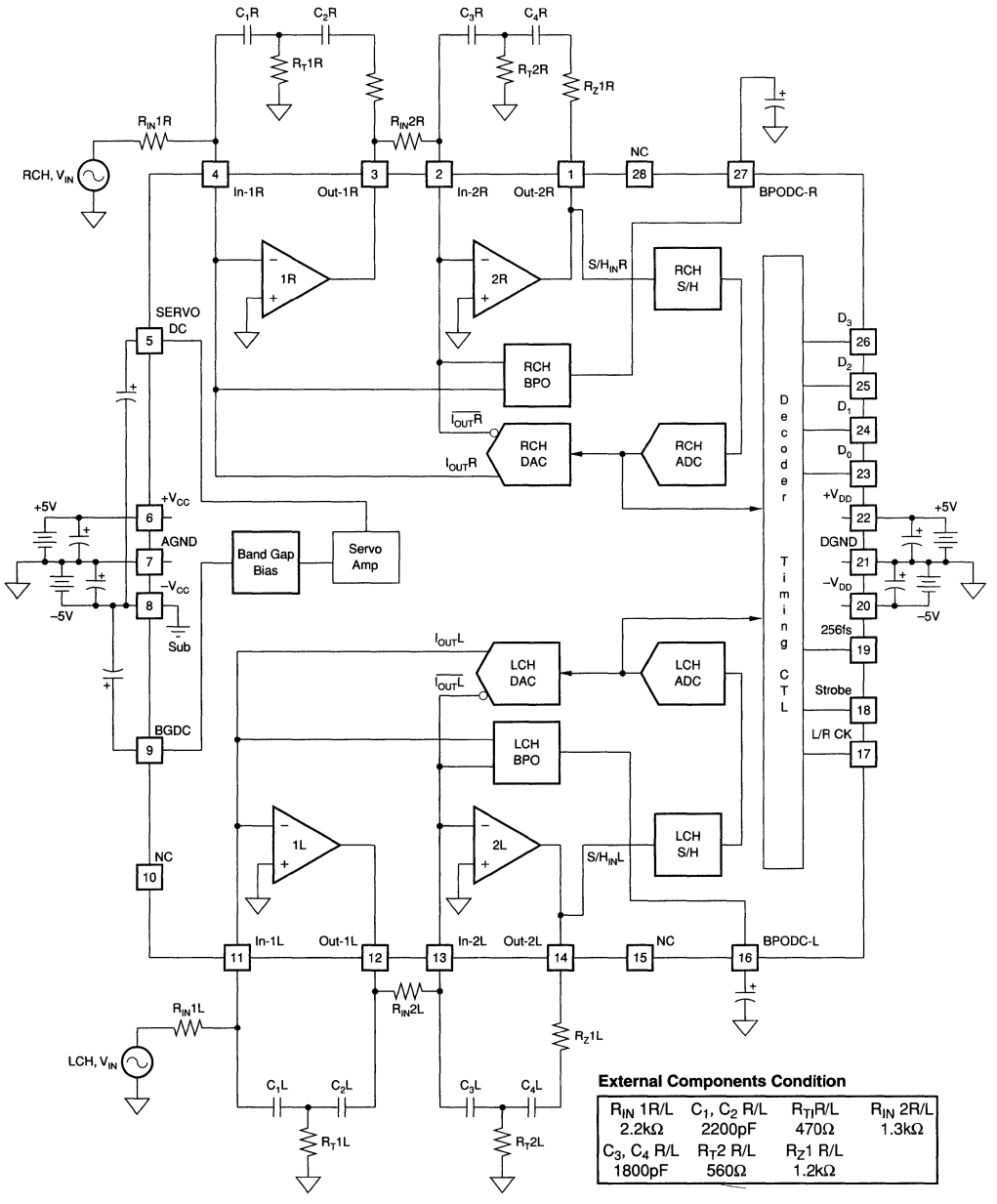
PIN	I/O(1)	NAME	DESCRIPTION
1	O	OVL	Left Channel Overflow Output (Active High)
2	O	OVR	Right Channel Overflow Output (Active High)
3	I	D_3	D3 Data Input (MSB)
4	I	D_2	D2 Data Input
5	I	D_1	D1 Data Input
6	I	D_0	D0 Data Input (LSB)
7	–	TP1	Test Pin (No Connection)
8	–	V_{SS1}	Common Channel 1
9	–	V_{DD1}	+5V Channel 1
10	O	256fs	256fs Clock Output
11	I	Strobe	Data Strobe Clock Input (128fs)
12	I	LRCK	LR Clock Input
13	I↑	CALD	Calibration Function Enable (Active Low)
14	O	CAL	Calibration Output (High During Calibration)
15	I	SYSCLK	System Clock Input (256fs or 384fs)
16	I↑/O	SCLK	Data Clock
17	I↑/O	L/R	LR Channel Phase Clock
18	O	SDATA	Serial Data Output (1fs)
19	I↑/O	FSYNC	Frame Clock (2fs)
20	I↑	LRSC	Phase Control of LR Channel Phase Clock
21	I↑	/PD	Power Down Mode Enable Input (Active Low)
22	I↑	Mode2	Output Format Selection Input 2
23	I↑	Mode1	Output Format Selection Input 1
24	I↑	S/M	Slave/Master Mode Selection Input (High Makes Slave Mode
25	I↑	CLKSEL	System Clock Selection Input (High Makes 256fs)
26	–	TP2	Test Pin (No Connection)
27	–	V_{DD2}	+5V Channel 2
28	–	V_{SS2}	Common Channel 2

NOTE: (1) O = Output terminal; I = Input terminal.

BLOCK DIAGRAM OF DF1760



BLOCK DIAGRAM OF PCM1760

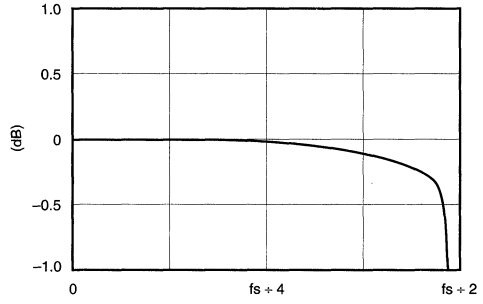


External Components Condition

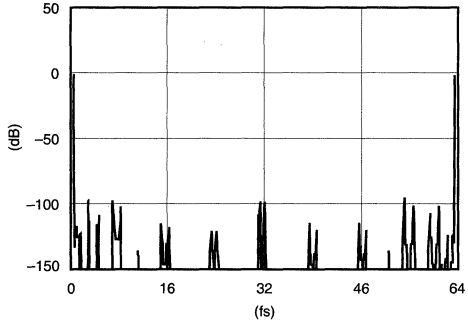
R_{IN} 1R/L	C_1, C_2 R/L	R_{TI}R/L	R_{IN} 2R/L
2.2kΩ	2200pF	470Ω	1.3kΩ
C_3, C_4 R/L	R_T2 R/L	R_Z1 R/L	
1800pF	560Ω	1.2kΩ	

TYPICAL PERFORMANCE CURVES

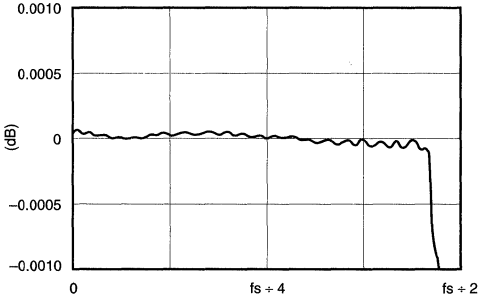
OVERALL PASS-BAND CHARACTERISTICS OF THE DF1760



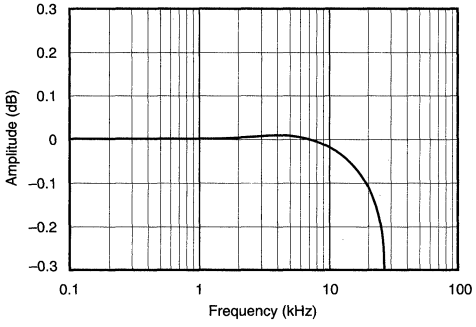
OVERALL CHARACTERISTICS OF THE DF1760



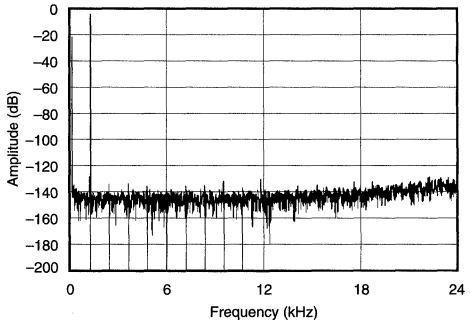
PASS-BAND CHARACTERISTICS OF THE FIR PORTION OF THE DF1760



TOTAL PASS-BAND FREQUENCY RESPONSE, COMBINATION OF PCM1760 AND DF1760

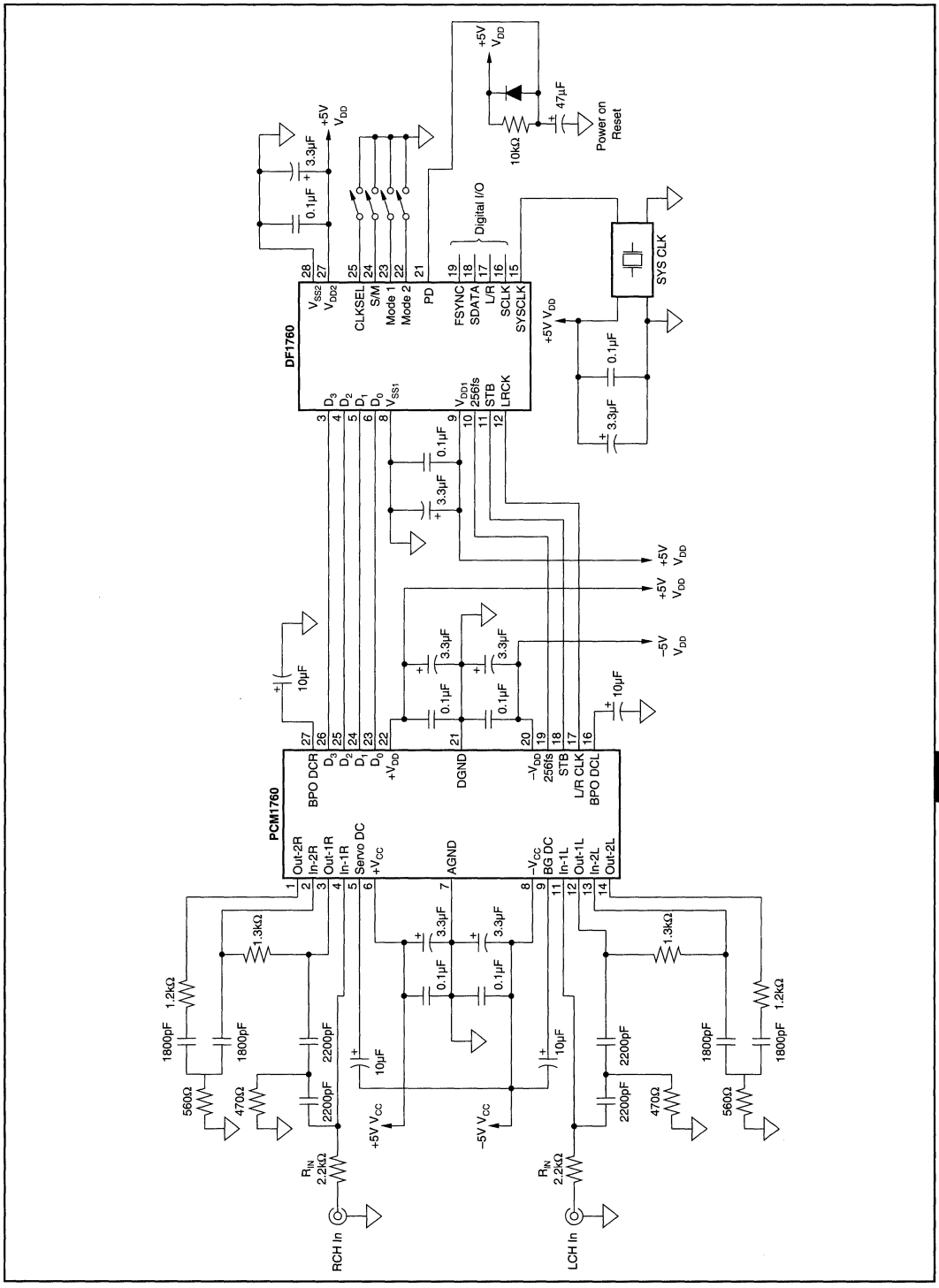


TYPICAL FFT ANALYSIS OF THE 1kHz fs INPUT SIGNAL



fs = 48.000000kHz F_{C1} = 1.171876kHz

BASIC CONNECTION DIAGRAM OF PCM1760 AND DF1760



FUNCTIONS OF THE DIGITAL FILTER

SYSTEM CLOCK

The DF1760 can accept a system clock of either 256fs or 384fs. If a 384fs system clock is used, the DF1760 divides by 2/3 to create the 256fs system clock required for the PCM1760. The system clock is applied to pin 15 (SYSCLK input). The actual clock selection is done by setting pin 25 (CLKSEL input) "high" for 256fs clock and "LOW" for 384fs clock.

The detailed timing requirements for the system clock are shown in Figure 3c.

CLKSEL	SYSCLK
H	256fs
L	384fs

MASTER/SLAVE MODE

The DF1760 can be used in both the master mode and slave mode. In the master mode, the DF1760 outputs L/R (left/right channel phase clock), SCLK (data clock) and FSYNC (frame clock 2fs) signals. In the slave mode, the DF1760 accepts L/R, SCLK and FSYNC signals. The mode selection is done by taking pin 24 (S/M INPUT) "HIGH" for slave mode and "LOW" for master mode.

S/M	MODE
H	Slave
L	Master

OUTPUT DATA FORMAT

The serial output data has four possible formats. The selection of the formats can be done by the Mode 1 and Mode 2 inputs.

MODE 1	MODE 2	FORMATS
H	H	MSB First, 16 Bits, Falling Edge
L	H	MSB First, 20 Bits, Falling Edge
H	L	MSB First, 20 Bits, Rising Edge
L	L	LSB First, 20 Bits, Falling Edge

LR CHANNEL PHASE CLOCK

The status of the LR channel phase clock can be set by the LRSC input.

LRSC	L/R CLOCK AND CHANNEL
H	H = LCH, L = RCH
L	L = LCH, H = RCH

OVERFLOW DETECTION

When a near-to-clipping input condition is detected, OVL output (Pin 1), or OVR output (Pin 2), becomes "HIGH" for a duration of 4096/fs (about 85ms) depending upon on the channel detected.

The OVL and OVR output return to "LOW" after 4096/fs duration automatically.

OFFSET CALIBRATION MODE

The offset error is calibrated by storing the digital data when the input is zero in registers and subtracting it from the future data with actual signal input.

CALD	CALIBRATION
H	Disable
L	Enable

To enable the calibration mode, set the CALD input (Pin 13) "LOW". The calibration mode is disabled by setting the CALD input (Pin 13) "HIGH". The calibration cycle is initiated by setting the /PD input (Pin 21) "LOW" for more than 2 system clock periods and then setting it "HIGH". During the calibration cycle, the CAL output (Pin 14) becomes "HIGH", all the serial data is forced to "LOW", and the L/R (Pin 17), SCLK (Pin 16) and FSYNC (Pin 19) pins become input terminals after the completion of the calibration cycle. The CAL output is "LOW".

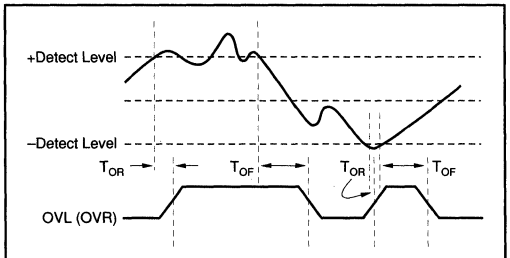
POWER DOWN MODE/RESET

The /PD input (Pin 21) has two functions. First, it should be set at "HIGH" after application or restoration of power (V_{SS} and/or V_{DD}) to accomplish the power-on/mode reset function. The detail timing requirements for this function are shown in Figure 3f. Second, the DF1760 is placed in the power down mode by setting the /PD input (Pin 21) "LOW". Set the /PD input (Pin 21) "HIGH" for normal operation mode.

/PD	OPERATION
H	Normal
L	Power Down

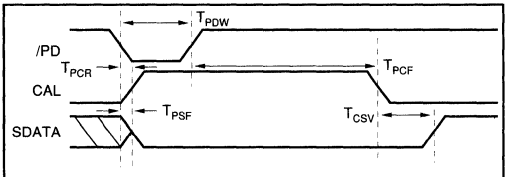
The power dissipation of the DF1760 in the power down mode is about 1/10 of the normal operation mode. During the power down mode, the L/R, SCLK, and FSYNC pins become input pins and all the serial data is forced "LOW". The 256fs output is enabled even in the power down mode.

The detailed timing of the power down mode operation and the offset calibration is shown in Figure 3b.



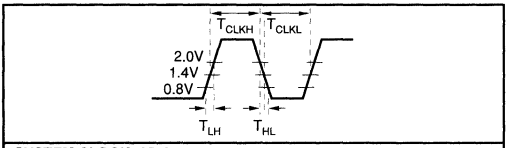
DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Delay from Overflow Detection to OVL (OVR) Output	T_{OR}	–	–	0	ns
OVL (OVR) Output Pulse Width	T_{OF}	–	4096	–	1/fs

FIGURE 3a. DF1760 Overflow Detection.



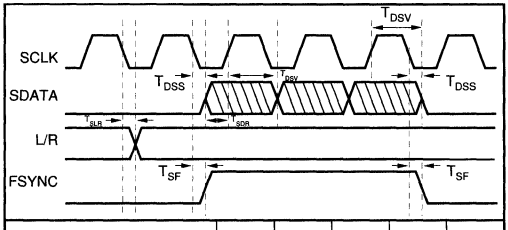
DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Pulse Width of /PD Input	T_{PDW}	2	–	–	1/Fclk
Delay from /PD Input to CAL Output	T_{PCR}	–	–	6	1/Fclk
Calibration Cycle Duration	T_{PCF}	–	4096	–	1/fs
Delay from /PD Input to S_{DATA} L	T_{PSF}	–	–	6	1/Fclk
Delay from Completion of Calibration to SDATA Valid	T_{CSV}	–	1	–	1/fs

FIGURE 3b. DF1760 Power Down and Offset Calibration.



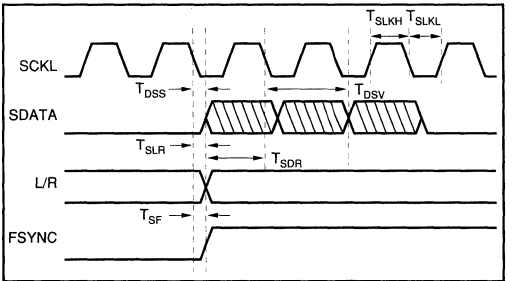
SYSTEM CLOCK: 256fs					
DESCRIPTION	**NAME**	**MIN**	**TYP**	**MAX**	**UNITS**
Low Level Duration	T_{CLKL}	31	–	–	ns
High Level Duration	T_{CLKH}	31	–	–	ns
SYSTEM CLOCK: 384fs					
DESCRIPTION	**NAME**	**MIN**	**TYP**	**MAX**	**UNITS**
Low Level Duration	T_{CLKL}	24	–	–	ns
High Level Duration	T_{CLKH}	24	–	–	ns
Rise Time	T_{LH}	–	–	6	ns
Fall Time	T_{HL}	–	–	6	ns

FIGURE 3c. System Clock Timing Requirements of DF1760.



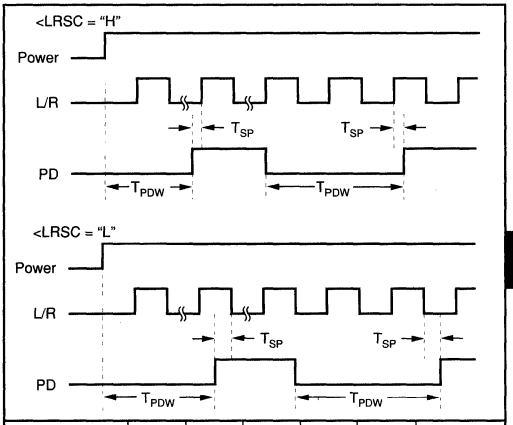
DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
SCLK Frequency	F_{SLK}	–	64fs	–	
SCLK Frequency Duty Cycle		–	50	–	%
FSYNC Frequency	F_{SYNC}	–	2fs	–	
FSYNC Frequency Duty Cycle		–	50	–	%
Delay from SCLK to L/R Edge	T_{SLR}	–20	–	50	ns
Delay from Falling Edge of SCLK to SDATA Valid	T_{DSS}	–	–	50	ns
Delay from SCLK to FSYNC Edge	T_{SF}	–20	–	50	ns
Delay from Rising Edge of SCLK to SDATA Valid	T_{SDR}	100	–	–	ns
Delay from SDATA Valid to Rising Edge of SCLK	T_{DSV}	100	–	–	ns

FIGURE 3d. Output Timing of Master Mode, DF1760.



DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
SCLK Frequency	F_{SLK}	32fs	48fs	64fs	–
Low Duration of FSCLK	T_{SLKL}	100	–	–	ns
High Duration of FSCLK	T_{SLKH}	100	–	–	ns
Delay from SCLK to L/R Edge	T_{SLR}	–70	–	70	ns
Delay from Falling Edge of SCLK to SDATA Valid	T_{DSS}	–	–	50	ns
Delay from SCLK to FSYNC Edge	T_{SF}	–70	–	0	ns
Delay from Rising Edge of SCLK to SDATA Valid	T_{DSV}	100	–	–	ns
Delay from SDATA Valid to Rising Edge of SCLK	T_{SDR}	100	–	–	ns

FIGURE 3e. Timing of Slave Mode, DF1760.



DESCRIPTION	NAME	MIN	TYP	MAX	UNITS[1]	APPLIES TO MODE
Power on to PD ↑	T_{PDW}	2			1/fs	Master/Slave
PD ↑ to L/R ↑ (LRSC = "H")	T_{SP}	–1		+1	1/Fclk	Slave
PD ↑ to L/R ↓ (LRSC = "L")	T_{SP}	–1		+1	1/Fclk	Slave

NOTE: (1) fs: sampling rate. Fclk: system clock frequency.

FIGURE 3f. Power On and Mode Reset Timing.

THEORY OF OPERATION

MULTI-BIT ENHANCED NOISE SHAPING

A block diagram of a typical 1-bit delta-sigma modulator is shown in Figure 4.

In Figure 4, the quantizer consists of a single bit which has two possible states, either "0" or "1". The input signal is sampled at a much higher sample rate than the nyquist sampling frequency. The quantizer output data stream is digitally filtered for higher resolution nyquist data. The theoretical SNR is determined by the number of the order of the integrator and the oversampling rate.

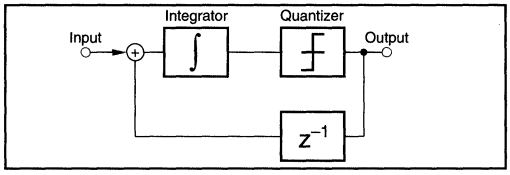


FIGURE 4. Single Stage 1-Bit Delta-Sigma.

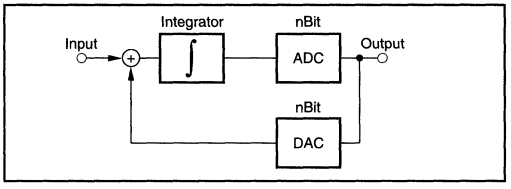


FIGURE 5. Single Stage Multi-bit Delta-Sigma.

There is a practical limit to increasing the numbers of order of the integrator due to an inherent oscillation in the modulator. There is also a limit to increasing the sample rate due to the increase in jitter sensitivity associated with high clock frequencies.

The PCM1760 utilizes a four-bit quantizer instead of the conventional one-bit method. The quantizing noise of a four-bit quantizer is 1/16 of the one-bit version. Using the four-bit quantizer allows for a lesser order number of the integrator and a lower oversampling rate to achieve similar performance to that of a more complex one-bit system.

A block diagram of the PCM1760 modulator is shown in Figure 6. The PCM1760 is a fourth-order integrator that samples at 64x oversampling, and samples left and right channel input signal simultaneously.

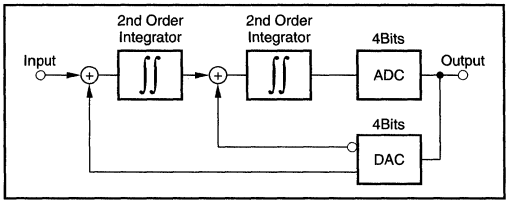


FIGURE 6. Multi-bit Enhanced Noise Shaping.

The DF1760 accepts the four-bit 64fs noise shaped data stream from the PCM1760 and decimates to 1/16 with an initial filter, and then decimates to 1fs 20-bit data using a 4x oversampling filter.

The PCM1760 and DF1760 combination achieves a dynamic range of 108dB and SNR of 110dB even with a single-ended input.

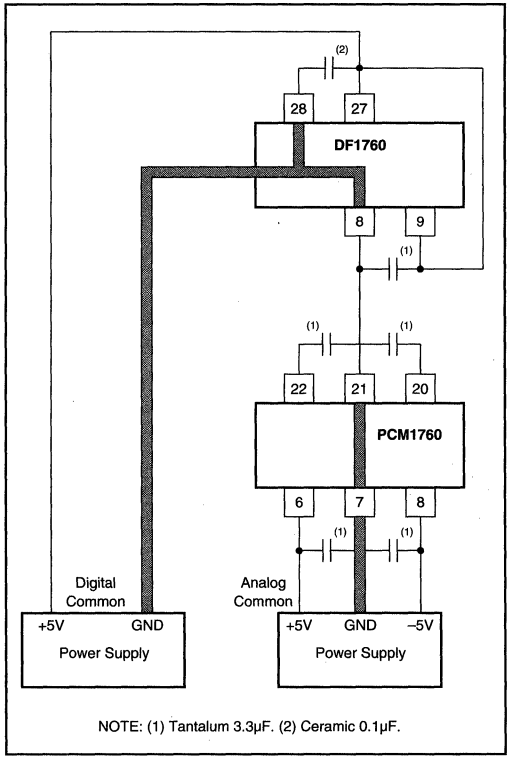


FIGURE 7. Recommended Power Supply Connection and Decoupling.

LAYOUT PRECAUTIONS

Analog common and digital common of the PCM1760 are not connected internally. These should be connected together with the common of the DF1760 as close to the unit as possible, preferably to a large ground plane under the PCM1760.

The use of a separate +5V supply is recommended for the PCM1760 and DF1760, and to connect the common at one point as described above. Low impedance analog and digital commons returns are essential for better performance.

The power supplies should be bypassed with tantalum capacitors as close as possible to the units. See Figure 7 for recommended common connections and power supplies bypassing.

OUTPUT TONE ELIMINATION

When the sampling frequency (fs) is between 40kHz and 50 kHz and the L/R relative offset voltage (ΔVs) is less than or equal to 0.05% of full scale range, the PCM1760 may output a tone similar to an idle tone. This tone is very low and its frequency depends on the input L/R relative offset voltage, ΔVs. This tone never occurs when the sampling frequency (fs) is 32kHz.

To avoid this tone, the offset voltage should be summed using an amplifier, buffer, active low pass filter, etc., to cause the input L/R relative offset voltage (ΔVs) to be greater than 0.05% of full scale range.

It is recommended that:

(A) Sum offset at both L/R channels
Lch: V_{IL} = –20mV ±10%
Rch: V_{IR} = +10mV ±10%

(B) Sum offset at L channel
Lch: V_{IL} = –30mV ±10%
Rch: V_{IR} = ±1mV (by a precircuit)

When FSR = 5V (±2.5V).

Figure 8 shows an application circuit for summing the offset at both L/R channels.

Alternately, Figure 9 shows an application circuit for use when fs = 48kHz which changes the external integrator circuit of the PCM1760.

MODULATOR COMPONENTS AND SAMPLING FREQUENCY

The PCM1760/DF1760 are capable to 30kHz to 50kHz fs sampling frequency by condition with external components value which are shown in Basic Connection Diagram.

The characteristics of the modulator's integrator can be set by external components. The values in the block diagram on page five are recommended for optimized performance. Low leakage, low voltage coefficient capacitors are recommended for integration capacitors.

The tolerance of external components should be better than ±2%.

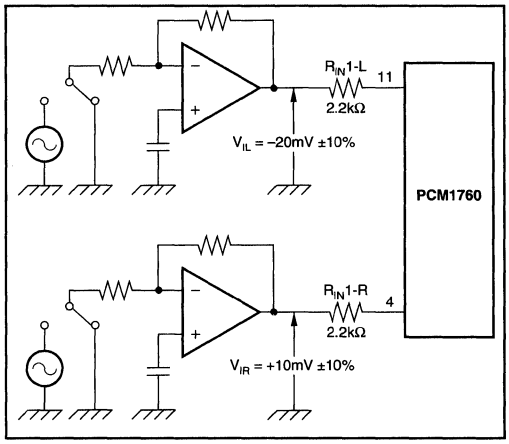


FIGURE 8. Application Example to Eliminate the Tone (offset voltage implementation for both channels).

OFFSET ERROR CALIBRATION

The offset voltage of the PCM1760 and the input stage of the system can be compensated by using the calibration mode of the DF1760. Offset calibration is shown in Figure 10. An optional analog switch is driven by a CAL output of the DF1760. The PD input of the DF1760 is used to initiate the calibration cycle.

ANALOG INPUT AND DIGITAL OUTPUT

Ideal output digital code range for 20-bit resolution is from 8000H (–Full Scale) to 7FFFFH (+Full Scale).

The DF1760, combined with 70000H (±FSR) of the PCM1760, produces a digital output code range at ±FSR input of 90000H (–FSR).

The relationship between analog input and digital output is shown in Table I.

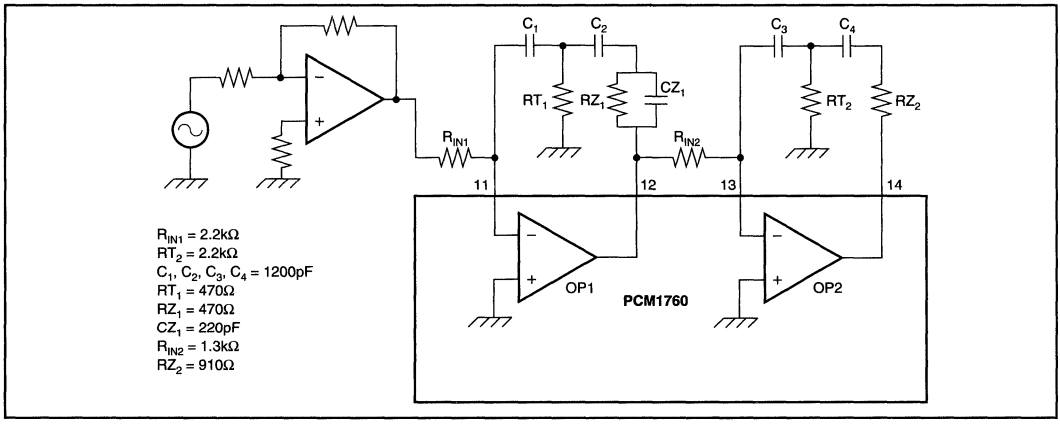


FIGURE 9. Application Example to Eliminate the Tone (alternative modulator's integrator circuit. Only for fs = 48kHz).

ANALOG INPUT	CONDITION	DIGITAL OUTPUT
+2.55V	+Max Input	72000H
+2.50V to +2.55V	Overflow	70000H to 72000H[2]
+2.50V	+FSR	70000H
0V	BPZ (Ideal)	00000H[1]
–2.50V	–FSR	90000H
–2.83V to –2.85V	Overflow	82FFFH to 82000H[2]
–2.85V	–Max Input	82000H

NOTES: (1) Incase of BPZ Error = 0. (2) Overflow detection level is over 70000H or under 82FFFH of digital output code.

TABLE I. Output Codes.

POWER SUPPLY SEQUENCING

The PCM1760 requires $\pm V_{CC}$ and $\pm V_{DD}$ power supplies. To avoid any possibility of latch-up, the $\pm V_{CC}$ and $\pm V_{DD}$ power should all be applied simultaneously or the $+V_{CC}$ and $+V_{DD}$ applied first followed by $-V_{CC}$ and $-V_{DD}$.

POWER-ON RESET AND MODE RESET

The timing requirements for POWER-ON RESET and MODE RESET are shown in Figure 3f. The DF1760 requires POWER-ON RESET when power is applied or restored. MODE RESET is required when any of the following has been changed: system clock, master/slave mode, output data format, L/R clock, calibration after POWER-ON in slave mode.

This reset should be done by holding the /PD input (pin 21) low for more than 2/fs. Suggested reset circuits are given in Figures 11, 12 and 13.

CLOCK INPUT

After power is applied to the DF1760, the system clock should be provided continuously. The DF1760 employs a dynamic logic architecture.

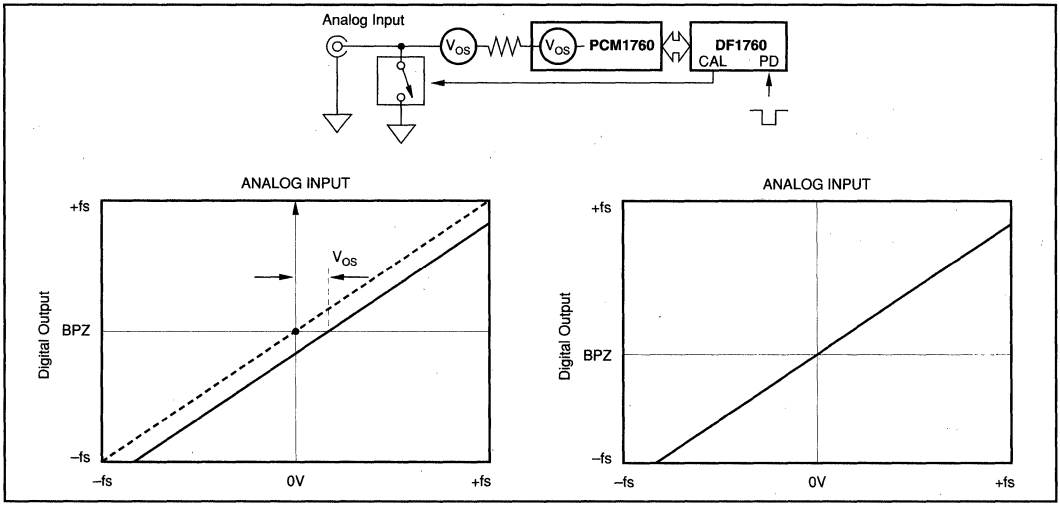


FIGURE 10. Illustration of Offset Calibration.

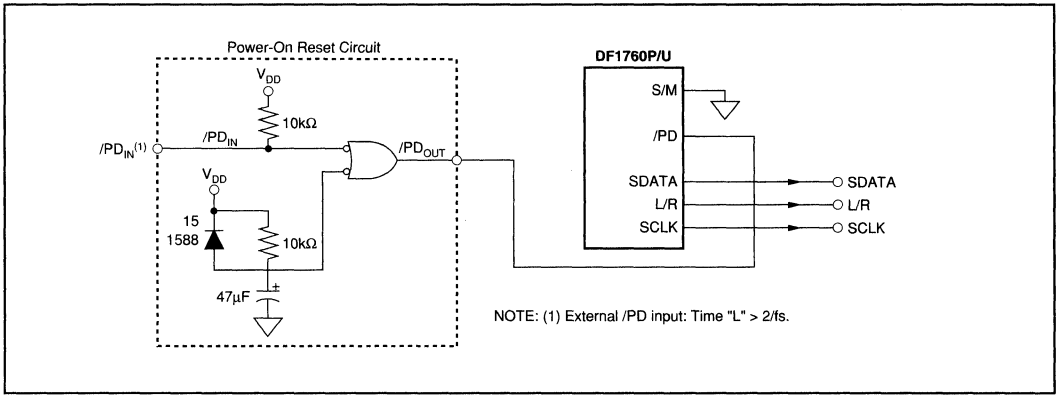


FIGURE 11. Master Mode Reset Circuit.

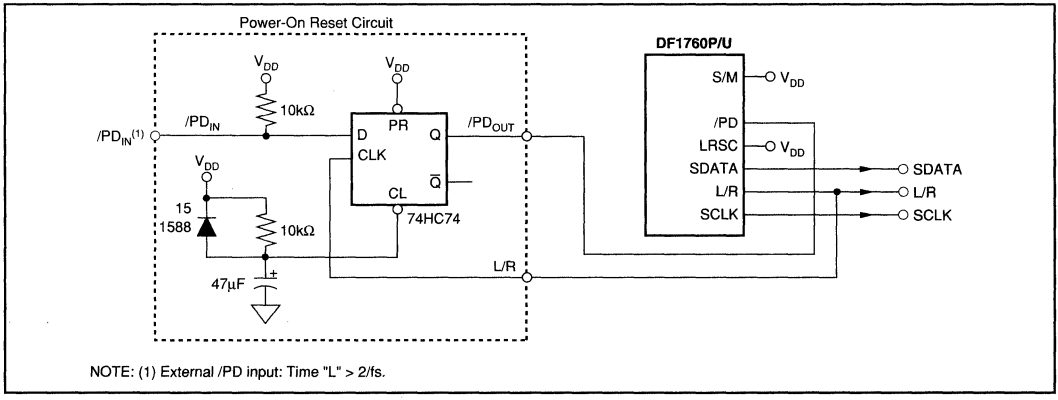


FIGURE 12. Slave Mode Reset Circuit, (LRSC = H).

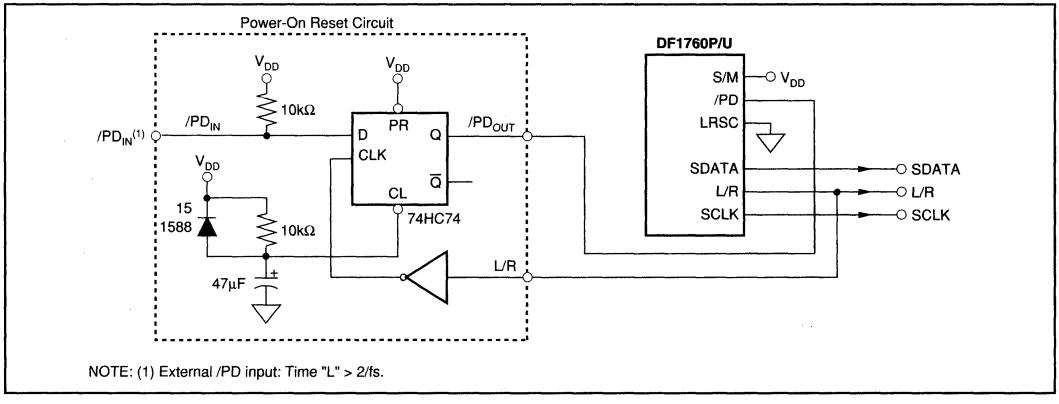


FIGURE 13. Slave Mode Reset Circuit, (LRSC = L).

TIMING CHARACTERISTICS

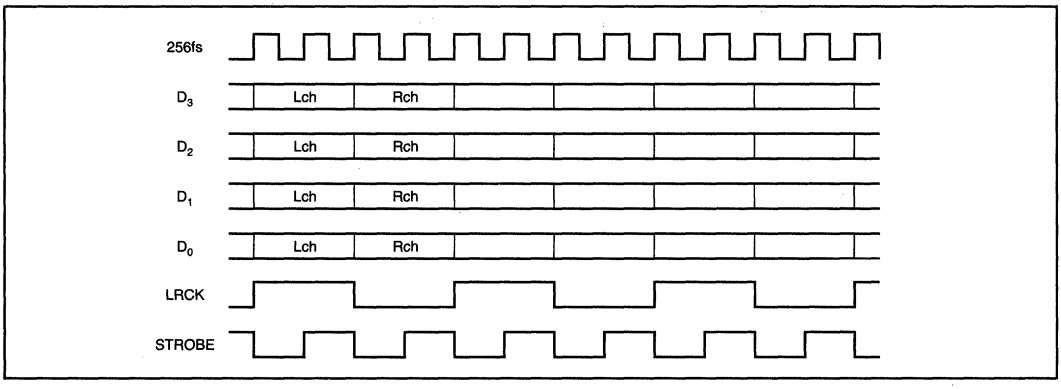


FIGURE 14. Input and Output Format of the DF1760 and PCM1760.

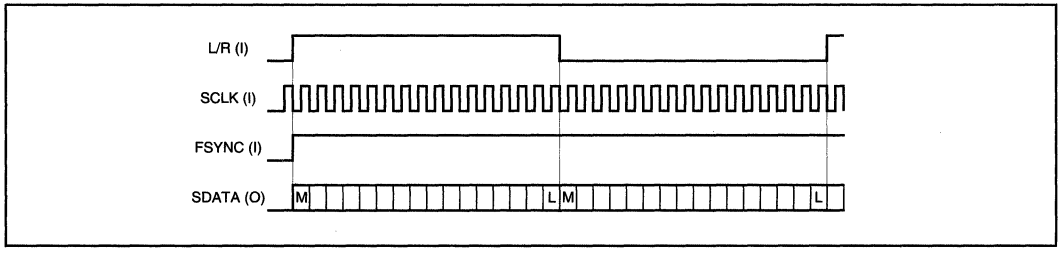


FIGURE 15a. Slave Mode and SCLK = 32fs (Output format of the DF1760).

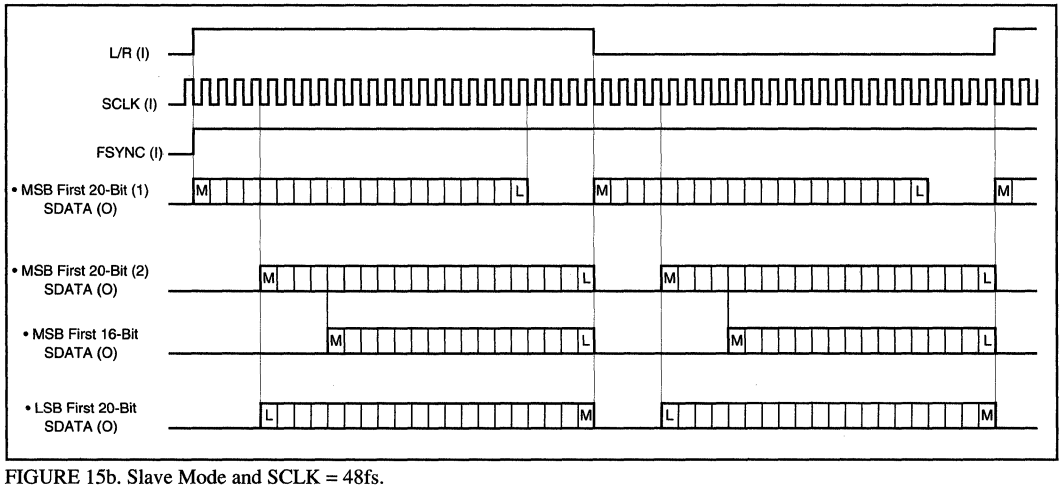


FIGURE 15b. Slave Mode and SCLK = 48fs.

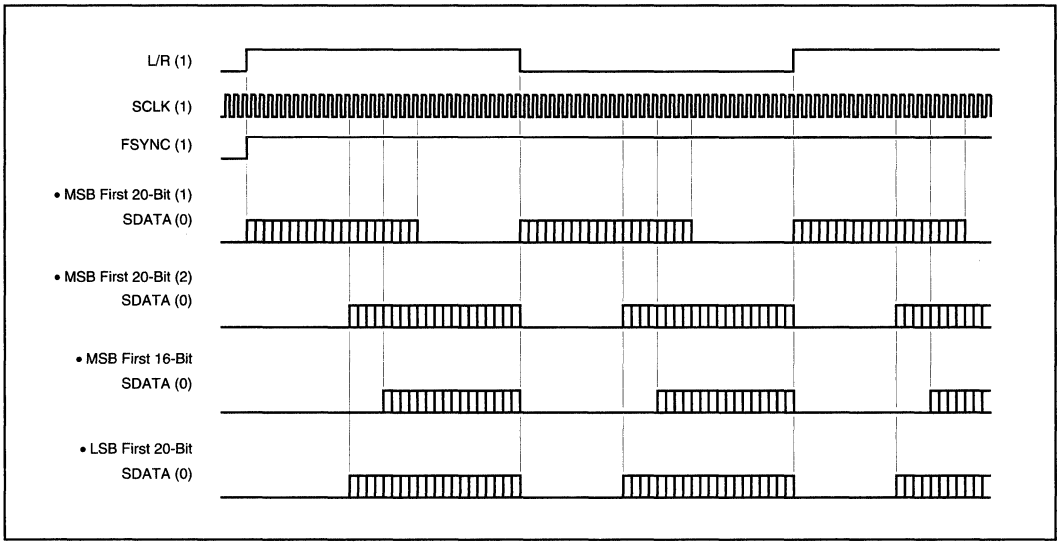


FIGURE 15c. Slave Mode and SCLK = 64fs.

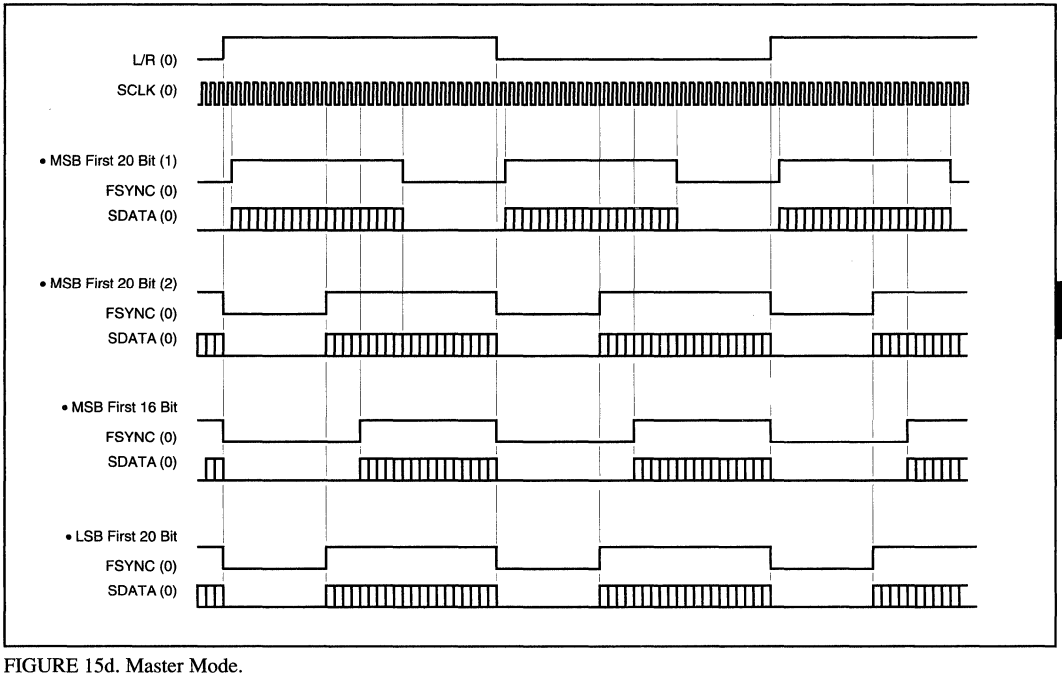


FIGURE 15d. Master Mode.

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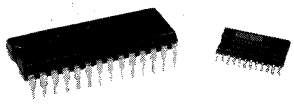


PCM54
PCM55

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10619

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **PARALLEL INPUT FORMAT**
- **16-BIT RESOLUTION**
- **15-BIT MONOTONICITY (typ)**
- **–92dB TOTAL HARMONIC DISTORTION (K Grade)**
- **3µs SETTLING TIME (Voltage Out)**
- **96dB DYNAMIC RANGE**
- **±3V or ±1mA AUDIO OUTPUT**
- **OPERATES ON ±5V (PCM55) to ±12V (PCM54) SUPPLIES**
- **28-PIN DIP (PCM54)**
- **24-LEAD SOIC (PCM55)**

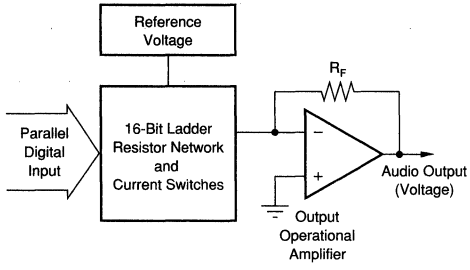
DESCRIPTION

The PCM54 and PCM55 family of converters are parallel input, fully monotonic, 16-bit digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve THD specifications if desired.

A current output (I_{OUT}) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-pin plastic miniflatpak.



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SPECIFICATIONS

ELECTRICAL

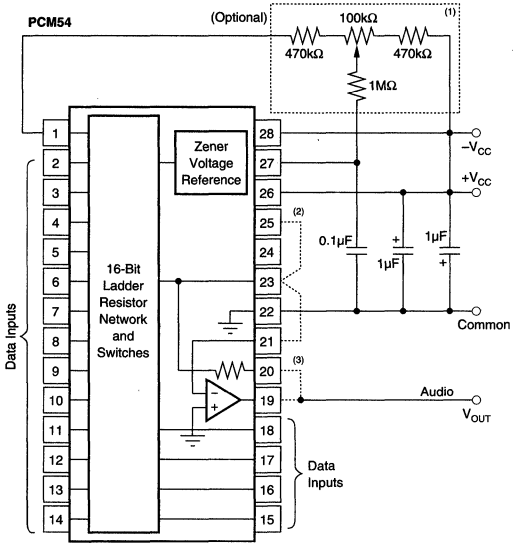
At +25°C, $\pm V_{CC}$ = 12V, unless otherwise noted.

PARAMETER	PCM54HP, PCM55HP MIN	PCM54HP, PCM55HP TYP	PCM54HP, PCM55HP MAX	PCM54JP, PCM55JP MIN	PCM54JP, PCM55JP TYP	PCM54JP, PCM55JP MAX	PCM54KP MIN	PCM54KP TYP	PCM54KP MAX	UNITS
DIGITAL INPUTS										
Resolution		16			*			*		Bits
Dynamic Range		96			*			*		dB
Logic Levels (TTL/CMOS Compatible):										
V_{IH}	+2.4		+5.25	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH}, V_{IN} = +2.7V			+40			*			*	µA
I_{IL}, V_{IN} = +0.4V			–0.5			*			*	mA
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error		±2			*			*		%
Bipolar Zero Error		±30			*			*		mV
Differential Linearity Error at Biploar Zero[1]		±0.001			*			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*			*		µV
TOTAL HARMONIC DISTORTION[3]										
(16-Bit Resolution)										
V_O = ±FS at f = 991Hz		–94	–82		*	–88	*	*	–92	dB
V_O = –20dB at f = 991Hz		–74	–68		*	*	*	–80	–74	dB
V_O = –60dB at f = 991Hz		–34	–28		*	*	*	–40	–34	dB
MONOTONICITY		15			*			*		Bits
SETTLING TIME (to ±0.006% of FSR)										
Voltage Output: 6V Step		3			*			*		µs
1LSB Step		1			*			*		µs
Current Output (1mA Step): 10Ω to 100Ω Load		350			*			*		ns
1kΩ Load[4]		350			*			*		ns
Deglitcher Delay (THD Test)[5]		2.5	4		*	*		*	*	µs
Slew Rate		10			*			*		V/µs
WARM-UP TIME	1			*			*			Min
ANALOG OUTPUT										
Voltage Output: Bipolar Range		±3			*			*		V
Output Current	±2			*			*			mA
Output Impedance		0.1			*			*		Ω
Short-Circuit Duration		Indefinite to Common			*			*		
Current Output:[6]										
Bipolar Range (±30%)		±1			*			*		mA
Bipolar Output Impedance (±30%)		1.2			*			*		kΩ
POWER SUPPLY REQUIREMENTS										
Voltage: $+V_{CC}$ (PCM54)	+4.75	+12	+15.75	*	*	*	*	*	*	V
$-V_{CC}$ (PCM54)	–4.75	–12	–15.75	*	*	*	*	*	*	V
$+V_{CC}$ (PCM55)	+4.75	+5	+7.5	*	*	*	*	*	*	V
$-V_{CC}$ (PCM55)	–4.75	–5	–7.5	*	*	*	*	*	*	V
Supply Drain: $+V_{CC}$		+13	+20		*	*		*	*	mA
$-V_{CC}$		–16	–25		*	*		*	*	mA
TEMPERATURE RANGE										
Operating	0		+70	*		*	*		*	°C
Storage	–55		+100	*		*	*		*	°C

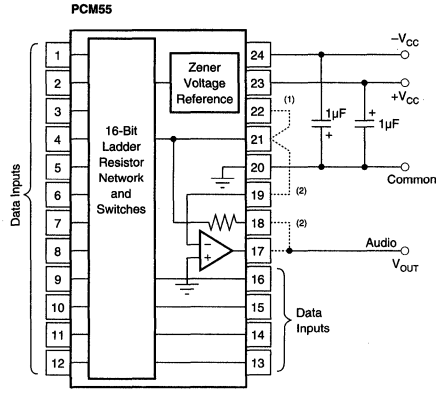
* Specifications same as for PCM54HP.

NOTES: (1) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected.

CONNECTION DIAGRAMS



NOTES: (1) MSB error (BPZ differential linearity error) can be adjusted to zero using this external circuit. (2) Connect to bipolar operation (+V_{CC} ≥ 8.5V for unipolar operation). (3) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21, and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.



NOTES: (1) Connect for bipolar operation. (+V_{CC} ≥ 8.5V for unipolar operation). (2) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19, and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.

PIN ASSIGNMENTS

PIN	PCM54-DIP	PIN	PCM54-DIP
1	Trim	15	Bit 13
2	Bit 1 (MSB)	16	Bit 14
3	Bit 2	17	Bit 15
4	NC	18	Bit 16 (LSB)
5	Bit 3	19	V_{OUT}
6	Bit 4	20	R_{FB}
7	Bit 5	21	SJ
8	Bit 6	22	Common
9	Bit 7	23	I_{OUT}
10	Bit 8	24	NC
11	Bit 9	25	I_{BPO}
12	Bit 10	26	+V_{CC}
13	Bit 11	27	MSB Adjust
14	Bit 12	28	−V_{CC}

PIN ASSIGNMENTS

PIN	PCM55-SOIC	PIN	PCM55-SOIC
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16
5	Bit 5	17	V_{OUT}
6	Bit 6	18	Feedback Resistor
7	Bit 7	19	Summing Junction
8	Bit 8	20	Common
9	Bit 9	21	Current Output
10	Bit 10	22	Bipolar Offset
11	Bit 11	23	+V_{CC}
12	Bit 12	24	−V_{CC}

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM54HP	28-Pin DIP	215
PCM54JP	28-Pin DIP	215
PCM54KP	28-Pin DIP	215
PCM55HP	24-Pin SOIC	178
PCM55JP	24-Pin SOIC	178

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±18VDC
Input Logic Voltage	−1V to +5.5V
Power Dissipation	PCM54 800mW, PCM55 400mW
Storage Temperature	−55°C to +100°C
Lead Temperature, (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	THD at FS	PACKAGE
PCM54HP	0.008	28-pin DIP
PCM54JP	0.004	28-pin DIP
PCM54KP	0.0025	28-pin DIP
PCM55HP	0.008	24-lead SOIC
PCM55JP	0.004	24-lead SOIC

BURR-BROWN®

PCM56P
PCM56U

DESIGNED FOR AUDIO

Serial Input 16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

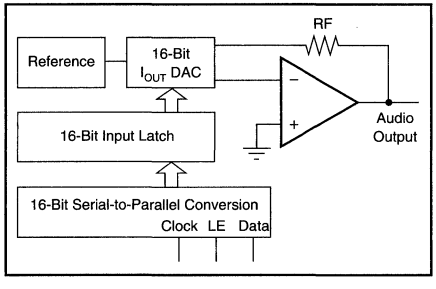
- SERIAL INPUT
- –92dB MAX THD: FS Input, K Grade
- –74dB MAX THD: –20dB Input, K Grade
- 96dB DYNAMIC RANGE
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 1.5µs SETTLING TIME, TYP: Voltage Out
- ±3V OR ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V TO ±12V SUPPLIES
- PINOUT ALLOWS I_{OUT} OPTION
- PLASTIC DIP OR SOIC PACKAGE

DESCRIPTION

The PCM56 is a state-of-the-art, fully monotonic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

This converter is completely self-contained with a stable, low noise, internal zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V to ±12V. Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero) to further improve total harmonic distortion (THD) specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

The PCM56 is packaged in a high-quality 16-pin molded plastic DIP package or SOIC and has passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C, and nominal power supply voltages ±5V, unless otherwise noted.

PARAMETER	PCM56U, PCM56P-J, -K MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution		16		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	V
V_{IL}	0		+0.8	V
I_{IH}, V_{IN} = +2.7V			+1.0	µA
I_{IL}, V_{IN} = +0.4V			–50	µA
Input Clock Frequency	10.0			MHz
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±2.0		%
Bipolar Zero Error		±30		mV
Differential Linearity Error		±0.001		% of FSR[2]
Noise (rms, 20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		6		µV
TOTAL HARMONIC DISTORTION				
V_O = ±FS at f = 991Hz: PCM56P-K		–94	–92	dB
PCM56P-J		–94	–88	dB
PCM56P, PCM56U		–94	–82	dB
PCM56P-L		–94	–80	dB
V_O = –20dB at f = 991Hz: PCM56P-K		–75	–74	dB
PCM56P-J		–75	–68	dB
PCM56P, PCM56U		–75	–68	dB
PCM56P-L		–75	–60	dB
V_O = –60dB at f = 991Hz: PCM56P-K		–35	–34	dB
PCM56P-J		–35	–28	dB
PCM56P, PCM56U		–35	–28	dB
PCM56P-L		–35	–20	dB
MONOTONICITY		15		Bits
DRIFT (0°C to +70°C)				
Total Drift[3]		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Output: 6V Step		1.5		µs
1LSB		1.0		µs
Slew Rate		10		V/µs
Current Output, 1mA Step: 10Ω to 100Ω Load		350		ns
1kΩ Load[4]		350		ns
WARM-UP TIME	1			Min
OUTPUT				
Voltage Output Configuration: Bipolar Range		±3.0		V
Output Current	±2.0			mA
Output Impedance		0.10		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration:				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.2		kΩ
POWER SUPPLY REQUIREMENTS[5]				
Voltage: $+V_S$ and $+V_L$	+4.75	+5.00	+13.2	V
$–V_S$ and $–V_L$	–4.75	–5.00	–13.2	V
Supply Drain (No Load): +V ($+V_S$ and $+V_L$ = +5V)		+10.00	+17.0	mA
–V ($–V_S$ and $–V_L$ = –5V)		–25.0	–35.0	mA
+V ($+V_S$ and $+V_L$ = +12V)		+12.0		mA
–V ($–V_S$ and $–V_L$ = –12V)		–27.0		mA
Power Dissipation: V_S and V_L = ±5V		175	260	mW
V_S and V_L = ±12V		468		mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	–25		+70	°C
Storage	–60		+100	°C

NOTES: (1) Logic input levels are TTL/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the V_{OUT} mode. (3) This is the combined drift error due to gain, offset, and linearity over temperature. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) All specifications assume $+V_S$ connected to $+V_L$ and $–V_S$ connected to $–V_L$. If supplies are connected separately, $–V_L$ must not be more negative than $–V_S$ supply voltage to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	−1V to $+V_S$/$+V_L$
Power Dissipation	850mW
Operating Temperature	−25°C to +70°C
Storage Temperature	−60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION

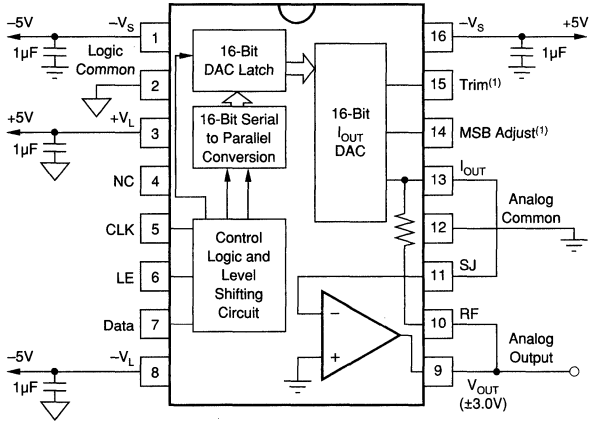
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM56U	16-Pin SOIC	211
PCM56P	16-Pin Plastic DIP	180
PCM56P-J	16-Pin Plastic DIP	180
PCM56P-K	16-Pin Plastic DIP	180
PCM56P-L	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Analog Negative Supply	$-V_S$
P2	Logic Common	LOG COM
P3	Logic Positive Supply	$+V_L$
P4	No Connection	NC
P5	Clock Input	CLK
P6	Latch Enable Input	LE
P7	Serial Data Input	DATA
P8	Logic Negative Supply	$-V_L$
P9	Voltage Output	V_{OUT}
P10	Feedback Resistor	RF
P11	Summing Junction	SJ
P12	Analog Common	ANA COM
P13	Current Output	I_{OUT}
P14	MSB Adjustment Terminal	MSB ADJ
P15	MSB Trim-pot Terminal	TRIM
P16	Analog Positive Supply	$+V_S$

CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 6.

DISCUSSION OF SPECIFICATIONS

The PCM56 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM56 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

DIGITAL INPUT CODES

The PCM56 accepts serial input data (MSB first) in the Binary Two's Complement (BTC) form. Refer to Table I for input/output relationships.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
7FFF Hex	+ Full Scale	+2.999908	–0.999970
8000 Hex	– Full Scale	–3.000000	+1.000000
0000 Hex	Bipolar Zero	0.000000	0.000000
FFFF Hex	Zero –1LSB	–0.000092	+0.030500µA

TABLE I. Digital Input to Analog Output Relationship.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "on" and all other bits "off") is the deviation from 0V out and is factory-trimmed to typically ±30mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM56 is factory trimmed to typically ±0.001% of FSR. The MSB DLE is adjustable to zero using the circuit shown in Figure 6.

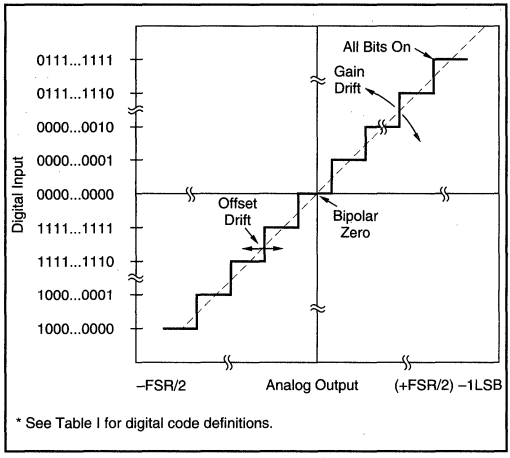


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM56 power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR: one for a large output voltage change of 6V and one for a 1LSB change. The 1LSB change is measured at the major carry (0000 hex to ffff hex), the point at which the worst-case settling time occurs.

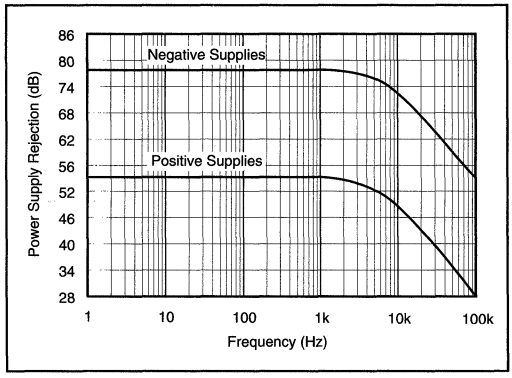


FIGURE 2. Power Supply Sensitivity.

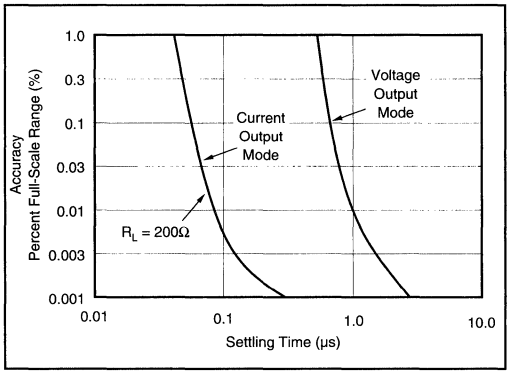


FIGURE 3. Full Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM56 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM56 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, or about 96dB of a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion.

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM56 error referred to the input can be shown to be:

$$\epsilon_{rms} = \sqrt{1/n \sum_{i=1}^{n} \left[E_L(i) + E_Q(i)\right]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM56 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as:

$$THD = \epsilon_{rms} / E_{rms} = \frac{\sqrt{1/n \sum_{i=1}^{n} \left[E_L(i) + E_Q(i)\right]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM56 the test period was chosen to be 22.7µs (44.1kHz), which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 991Hz and the amplitude of the input signal is 0dB, –20dB, and –60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

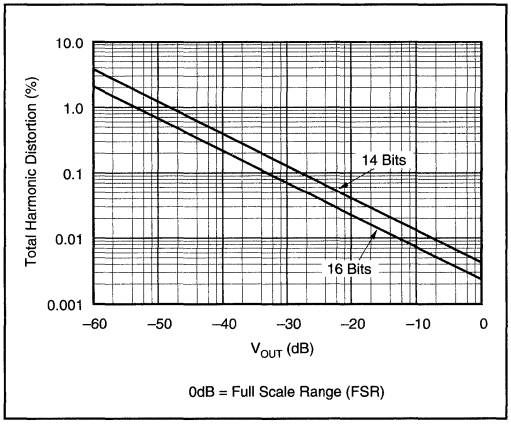


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

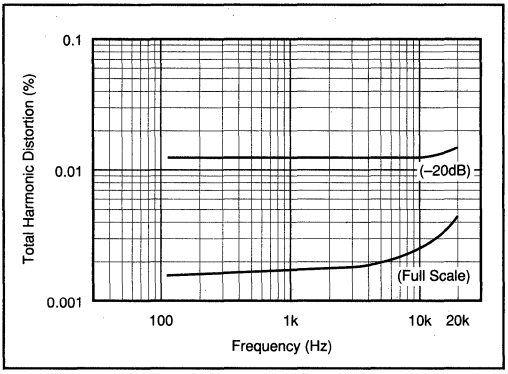


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1µF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM56 can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6, or the PCM56 connection diagram.

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM56, select input code FFFF hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 0000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92µV more than the voltage reading of the previous code (a 1LSB step = 92µV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –80dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

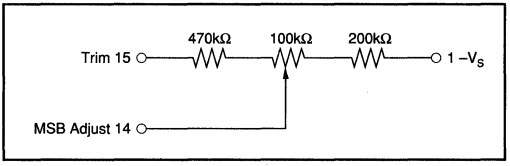


FIGURE 6. MSB Adjustment Circuit.

INPUT TIMING CONSIDERATIONS

Figure 7 and 8 refer to the input timing required to interface the inputs of PCM56 to a serial input data stream. Serial data is accepted in Binary Two's Complement (BTC) with the MSB being loaded first. Data is clocked in on positive going clock (CLK) edges and is latched into the DAC input register on negative going latch enable (LE) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are the ones that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

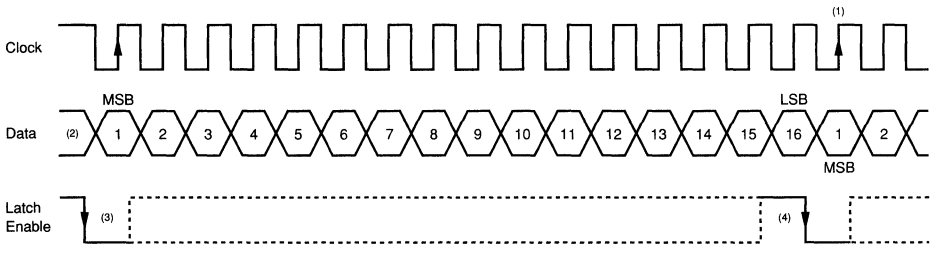
One requirement for clocking in all 16 bits is the necessity for a "17th" clock pulse. This automatically occurs when the clock is continuous (last bit shifts in on the first bit of the next data word). If the clock is stopped between input of 16-bit data words, the latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. This ensures that the latch is properly set up.

Figure 7 refers to the general input format required for the PCM56. Figure 8 shows the specific relationships between the various signals and their timing constraints.

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used, a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 14. If the circuit is not used, pins 14 and 15 should be left open.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination



NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 7. Input Timing Diagram.

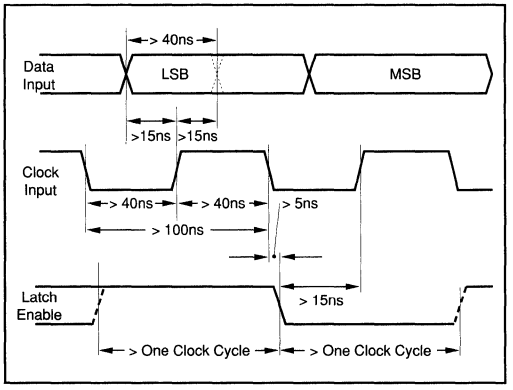


FIGURE 8. Input Timing Relationships.

of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

Figures 9 and 10 show a circuit and timing diagram for a single PCM56 used to obtain both left- and right-channel output in a typical digital audio system. The audio output of the PCM56 is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM56 is a complete D/A converter requiring no external reference or output op amp.

A sample/hold (S/H) amplifier, or "deglitcher" is required at the output of the D/A for both the left and right channel, as shown in Figure 9. The S/H amplifier for the left channel is composed of A_1, SW_1, and associated circuitry. A_1 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operate at a virtual ground when "C" and "B" are connected in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

Figure 10 shows the deglitcher controls for both left and right channels which are produced by timing control logic. A delay of 1.5µs ($t\omega$) is provided to allow the output of the PCM56 to settle within a small error band around its final value before connecting it to the channel output. Due to the fast settling time of the PCM56 it is possible to minimize the delay between the left- and right-channel outputs when using a single D/A converter for both channels. This is important because the right- and left-channel data are recorded in-phase and the use of the slower D/A converter would result in significant phase error at higher frequencies.

The obvious solution to the phase shift problem in a two-channel system would be to use two D/A converters (one per channel) and time the outputs to change simultaneously. Figure 11 shows a block diagram of the final test circuitry used for PCM56. It should be noted that no deglitching circuitry is required on the DAC output to meet specified THD performance. This means that when one PCM56 is used per channel, the need for all the sample/hold and controls circuitry associated with a single DAC (two-channel) design is effectively eliminated. The PCM56 is tested to meet its THD specifications without the need for output deglitching.

A low-pass filter is required after the PCM56 to remove all unwanted frequency components caused by the sampling frequency as well as those resulting from the discrete nature of the D/A output. This filter must have a flat frequency response over the entire audio band (0-20kHz) and a very high attenuation above 20kHz.

Most previous digital audio circuits used a higher order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristic transients contained in music.

SECOND GENERATION SYSTEMS

One method of avoiding the problems associated with a higher order analog filter would be to use digital filter oversampling techniques. Oversampling by a factor of two would move the sampling frequency (88.2kHz) out to a point where only a simple low-order phase-linear analog filter is required after the deglitcher output to remove unwanted intermodulation products. In a digital compact disc application, various VLSI chips perform the functions of error detection/correction, digital filtering, and formatting of the digital information to provide the clock, latch enable, and serial input to the PCM56. These VLSI chips are available from several sources (Sony, Yamaha, Signetics, etc.) and are specifically optimized for digital audio applications.

Oversampled circuitry requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more (for each output channel). A single PCM56 can provide two-channel oversampling at a 4X rate (176.4kHz/channel) and still remain well within the settling time requirements for maintaining specified THD performance. This would reduce the complexities of the analog filter even further from that used in 2X oversampling circuitry.

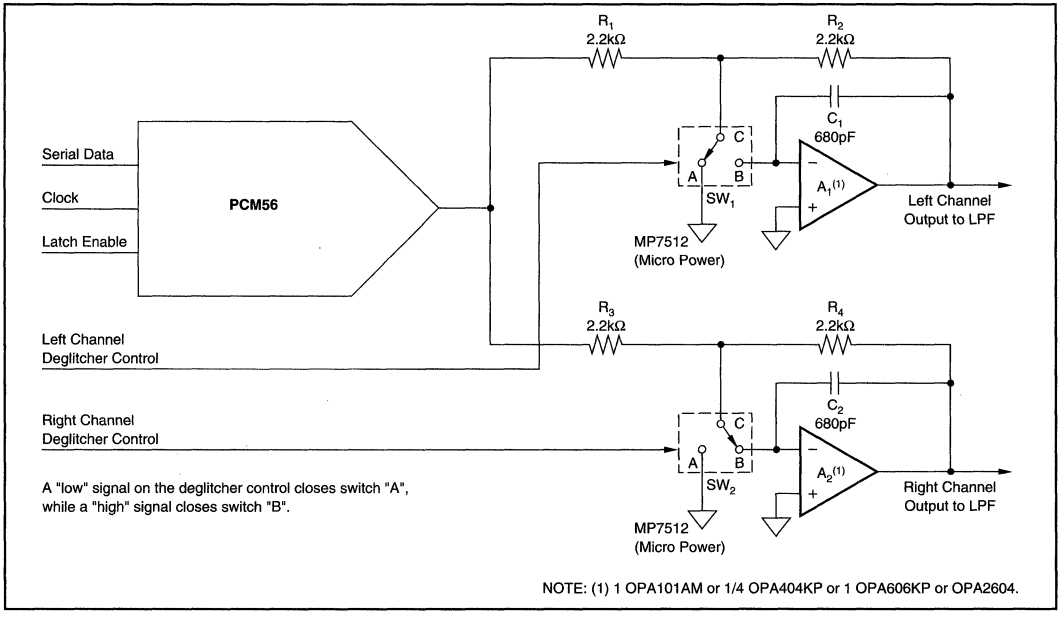


FIGURE 9. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

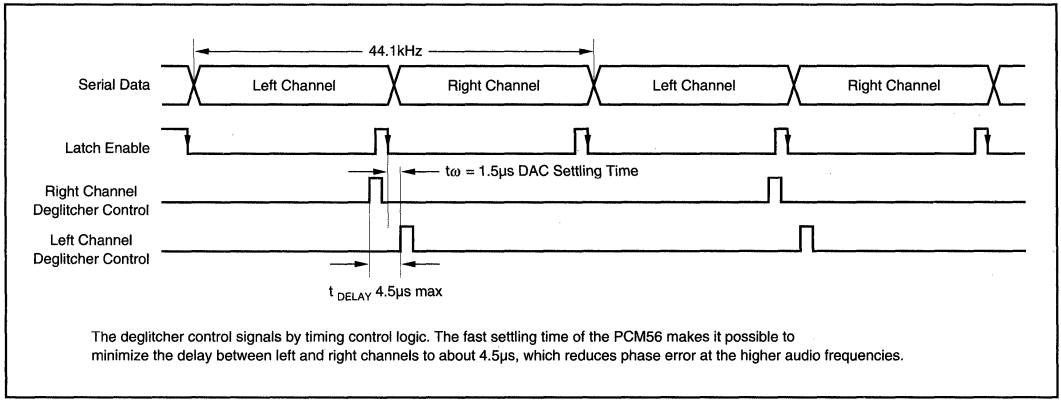


FIGURE 10. Timing Diagram for the Deglitcher Control Signals.

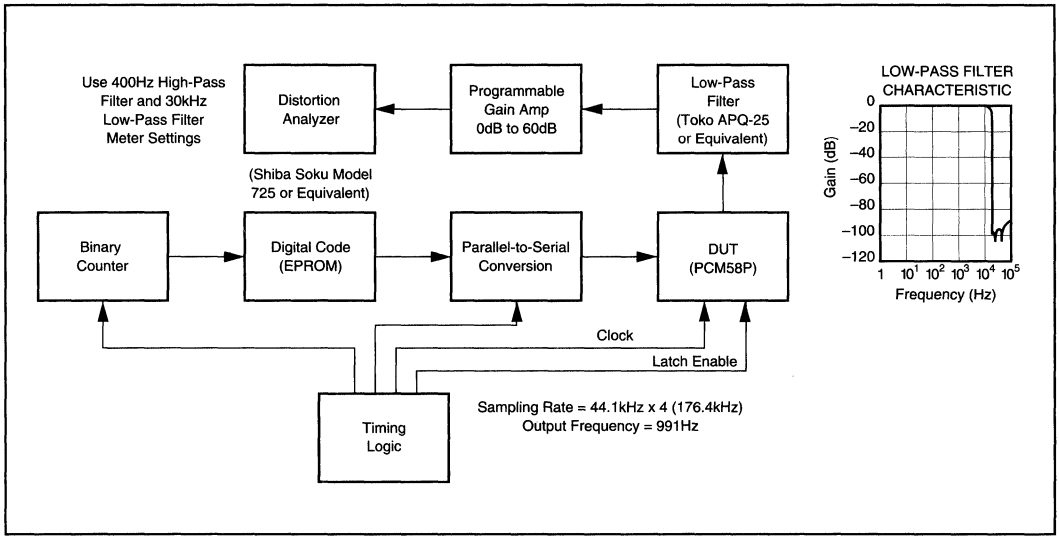


FIGURE 11. Block Diagram of Distortion Test Circuit.

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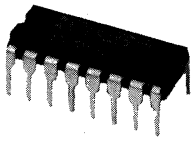


PCM61P

Serial Input 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

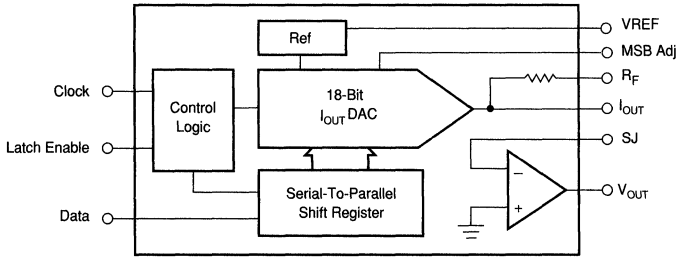
FEATURES

- **18-BIT MONOLITHIC AUDIO D/A CONVERTER**
- **LOW MAX THD + N: –92dB Without External Adjust**
- **100% PIN COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P**
- **LOW GLITCH OUTPUT OF ±3V OR ±1mA**
- **CAPABLE OF 8X OVERSAMPLING RATE IN V_{OUT} MODE**
- **COMPLETE WITH INTERNAL REFERENCE AND OUTPUT OP AMP**
- **RELIABLE PLASTIC 16-PIN DIP PACKAGE**

DESCRIPTION

The PCM61P is an 18-bit totally pin compatible performance replacement for the popular 16-bit PCM56P. With the addition of two extra bits, lower max THD+N (–92dB; PCM61P-K) can be achieved in audio applications already using the PCM56P. The PCM61P is complete with internal reference and output op amp and requires no external parts to function as an 18-bit DAC. The PCM61P is capable of an 8-times oversampling rate (single channel) and meets all of its specifications without an external output deglitcher.

The PCM61P comes in a small, reliable 16-pin plastic DIP package that has passed operating life tests under simultaneous high temperature, high humidity and high pressure testing.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, and $+V_{CC}$ = +5V, unless otherwise noted.

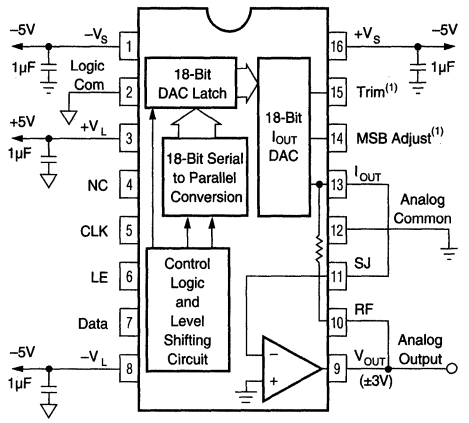
PARAMETER	CONDITIONS	PCM61P-P, J-P, K MIN	TYP	MAX	UNITS
RESOLUTION				18	Bits
DYNAMIC RANGE			108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_L$	V
V_{IL}		0		+0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format		Serial BTC[1]			
Input Clock Frequency				16.9	MHz
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion + N[2]	Without MSB Adjustments				
PCM61P					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–74	–68	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–34	–28	dB
PCM61P-J					
f = 991Hz (0dB)	f_S = 176.4kHz		–94	–88	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–76	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–36	–34	dB
PCM61P-K					
f = 991Hz (0dB)	f_S = 176.4kHz		–98	–92	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
IDLE CHANNEL SNR	20Hz to 20kHz at BPZ[5]		112		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%FSR
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		%FSR
Total Drift[6]	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±4		ppm of FSR/°C
Warm-up Time		1			Minute
MONOTONICITY			16		Bits
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Current		±2			mA
Output Impedance			0.1		Ω
Current: Output Range	±30%		±1		mA
Output Impedance	±30%		1.2		kΩ
SETTLING TIME	To ±0.006% of FSR				
Voltage: 6V Step			1.5		µs
1 LSB			1.0		µs
Slew Rate			12		V/µs
Current: 1mA Step	10Ω to 100Ω Load		250		ns
1mA Step	1kΩ Load		350		ns
Glitch Energy	Meets all THD+N specs without external deglitching				
POWER SUPPLY REQUIREMENTS[7]					
$\pm V_{CC}$ Supply Voltage		±4.75	±5	±13.2	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5V		+10	+17	mA
$+I_{CC}$	$+V_{CC}$ = +12V		+12		mA
$-I_{CC}$	$-V_{CC}$ = –5V		–25	–35	mA
$-I_{CC}$	$-V_{CC}$ = –12V		–27		mA
Power Dissipation	$\pm V_{CC}$ = ±5V		175	260	mW
	$\pm V_{CC}$ = ±12V		475		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Bipolar zero, using A-weighted filter. (6) This is the combined drift error due to gain, offset, and linearity over temperature. (7) All positive and all negative supply pins must be tied together respectively.

PIN ASSIGNMENTS

PIN	FUNCTION	DESCRIPTION
1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistance
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 4.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	–1V to V_S/$+V_L$
Power Dissipation	850mW
Operating Temperature Range	–25°C to +70°C
Storage Temperature Range	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

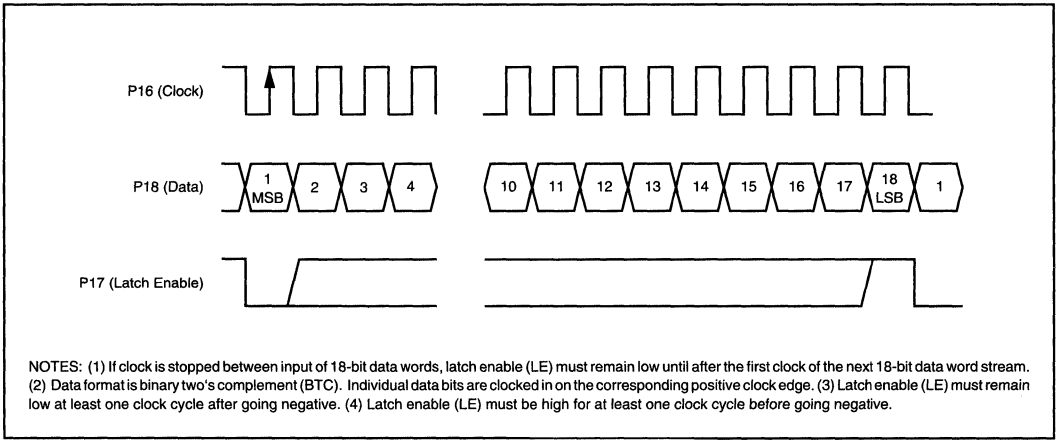
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM61P-P	16-Pin Plastic DIP	180
PCM61P-J	16-Pin Plastic DIP	180
PCM61P-K	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+FS	–0.99999237	+2.99997711
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	+0.00000763	–0.00002289
20000 Hex	–FS	+1.00000000	–3.00000000

TABLE I. PCM61P Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 1. PCM61P Timing Diagram.

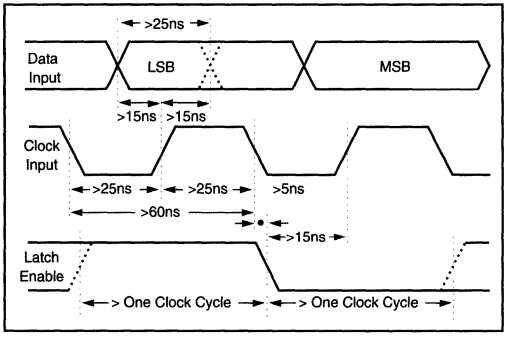


FIGURE 2. PCM61P Setup and Hold Timing Diagram.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9MHz for the PCM61P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16 x oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

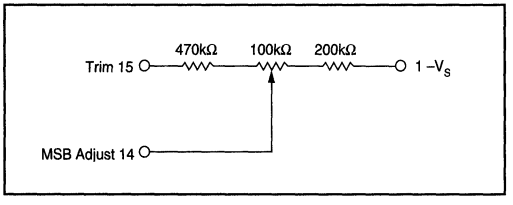


FIGURE 3. MSB Adjust Circuit.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM61P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 3 or the PCM61P connection diagram.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point, which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

After allowing ample warm-up time (5-10 minutes) to assure stable operation of the PCM61P, select input code 3FFFF hexadecimal (all bits on except the MSB). Measure the output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 00000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the output read 22.9μV more than the voltage reading of the previous code (a 1LSB step = 22.9μV). A much simpler method is to dynamically adjust the DLE at BPZ. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –60dB level sinusoidal output, then adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

BURR-BROWN®

PCM63P

DEMO BOARD AVAILABLE
See Appendix A

Colinear™ 20-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

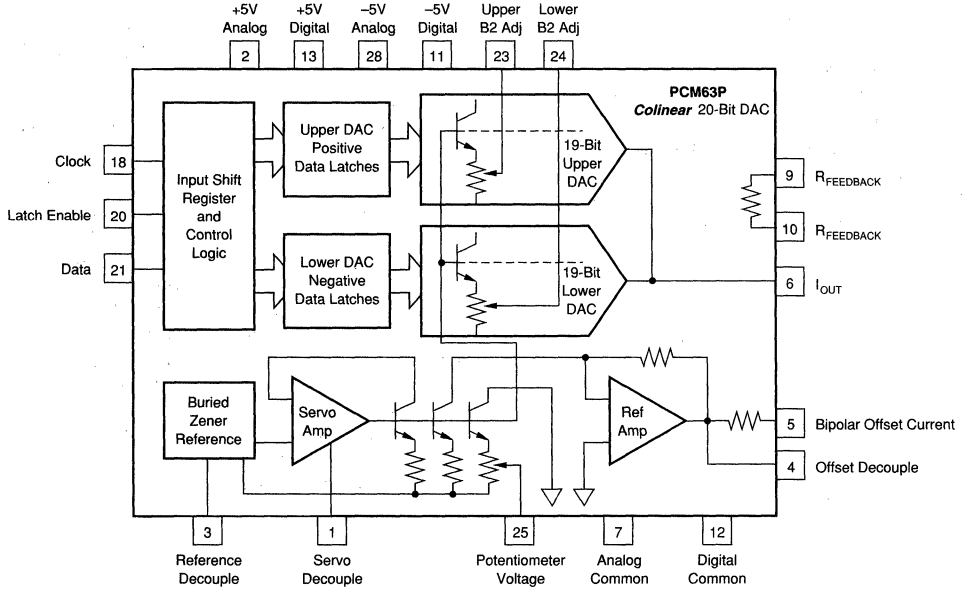
FEATURES

- ***COLINEAR* 20-BIT AUDIO DAC**
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **ULTRA LOW –96dB max THD+N (Without External Adjustment)**
- **116dB SNR min (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT (±2mA; ±2% max)**
- **CAPABLE OF 16x OVERSAMPLING**
- **COMPLETE WITH REFERENCE**

DESCRIPTION

The PCM63P is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB max with a full scale output; PCM63P-K). Incorporated into the PCM63P is a unique ***Colinear*** dual-DAC per channel architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM63P also features a very low noise (116dB max SNR; A-weighted method) and fast settling current output (200ns typ, 2mA step) which is capable of 16-times oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



Colinear™, Burr-Brown Corp.

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM63P, PCM63P-J, PCM63P-K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD+N at –60dB Referred to Full Scale					
PCM63P		96	100		dB
PCM63P-J		100	104		dB
PCM63P-K		104	108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_D$	V
V_{IL}		0		0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			12.5	25	MHz
TOTAL HARMONIC DISTORTION + N[2], Without Adjustments					
PCM63P					
f = 991Hz (0dB)[3]	f_S = 352.8kHz[4]		–92	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–36	dB
PCM63P-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–96	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–82	–76	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–44	–40	dB
PCM63P-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–100	–96	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–88	–82	dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–48	–44	dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±0.3	±1	dB
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20kHz at BPZ[7]	+116	+120		dB
POWER SUPPLY REJECTION			+86		dB
ANALOG OUTPUT					
Output Range			±2.00		mA
Output Impedance			670		Ω
Internal $R_{FEEDBACK}$			1.5		kΩ
Settling Time	2mA Step		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
$\pm V_A$, $\pm V_D$ Supply Voltage Range		±4.50	±5	±5.50	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		10	15	mA
$-I_A$, $-I_D$ Combined Supply Current	$-V_A$, $-V_D$ = –5V		–35	–45	mA
Power Dissipation	$\pm V_A$, $\pm V_D$ = ±5V		225	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter output frequency (signal level). (4) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 1.5kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Servo Amp Decoupling Capacitor	CAP
P2	+5V Analog Supply Voltage	$+V_A$
P3	Reference Decoupling Capacitor	CAP
P4	Offset Decoupling Capacitor	CAP
P5	Bipolar Offset Current Output (+2mA)	BPO
P6	DAC Current Output (0 to –4mA)	I_{OUT}
P7	Analog Common Connection	ACOM
P8	No Connection	NC
P9	Feedback Resistor Connection (1.5kΩ)	RF_1
P10	Feedback Resistor Connection (1.5kΩ)	RF_2
P11	–5V Digital Supply Voltage	$-V_D$
P12	Digital Common Connection	DCOM
P13	+5V Digital Voltage Supply	$+V_D$
P14	No Connection	NC
P15	No Connection	NC
P16	No Connection	NC
P17	No Connection	NC
P18	DAC Data Clock Input	CLK
P19	No Connection	NC
P20	DAC Data Latch Enable	LE
P21	DAC Data Input	DATA
P22	No Connection	NC
P23	Optional Upper DAC Bit-2 Adjust (–4.29V)*	UB2 Adj
P24	Optional Lower DAC Bit-2 Adjust (–4.29V)*	LB2 Adj
P25	Bit Adjust Reference Voltage Tap (–3.52V)*	V_{POT}
P26	No Connection	NC
P27	No Connection	NC
P28	–5V Analog Supply Voltage	$-V_A$

*Nominal voltages at these nodes assuming $\pm V_A$; $\pm V_D = \pm 5V$.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX THD+N, AT 0dB
PCM63P	28-Pin Plastic DIP	0°C to +70°C	–88dB
PCM63P-J	28-Pin Plastic DIP	0°C to +70°C	–92dB
PCM63P-K	28-Pin Plastic DIP	0°C to +70°C	–96dB

ABSOLUTE MAXIMUM RATINGS

$+V_A$, $+V_D$ to ACOM/DCOM	0V to +8V
$-V_A$, $-V_D$ to ACOM/DCOM	0V to –8V
$-V_A$, $-V_D$ to $+V_A$, $+V_D$	0V to +16V
ACOM to DCOM	±0.5V
Digital Inputs (pins 18, 20, 21) to DCOM	–1V to $+V_D$
Power Dissipation	500mW
Lead Temperature, (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}	70°C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

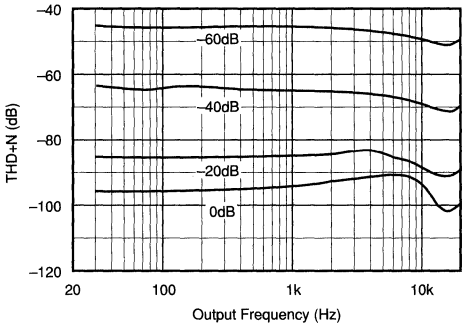
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM63P	28-Pin Plastic DIP	215
PCM63P-J	28-Pin Plastic DIP	215
PCM63P-K	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

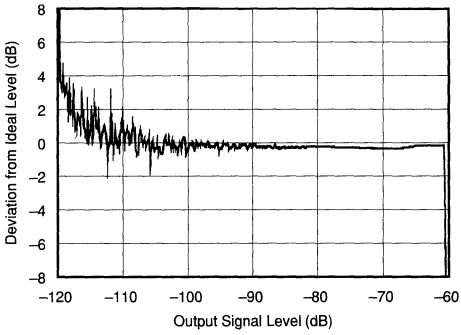
TYPICAL PERFORMANCE CURVES

All specifications at 25°C and $\pm V_A$ and $\pm V_D$ = ±5.0V, unless otherwise noted.

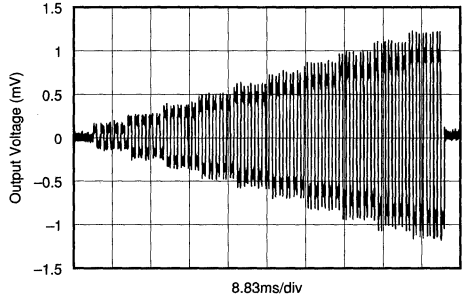
THD+N vs FREQUENCY



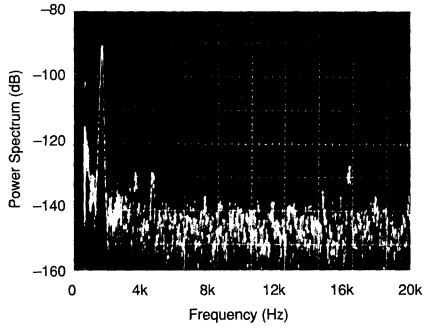
16-BIT LEVEL LINEARITY
(Dithered Fade to Noise)



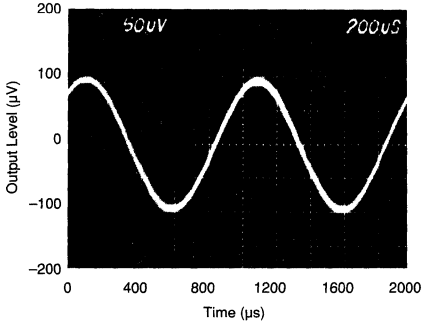
16-BIT MONOTONICITY



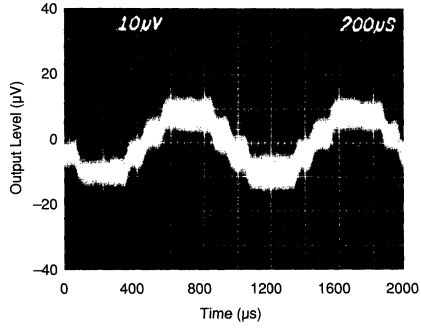
–90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



–90dB SIGNAL
(10Hz to 20kHz Bandwidth)



–110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

DUAL-DAC *COLINEAR* ARCHITECTURE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high oversampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DACs). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM63 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference and a common R-2R ladder to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or dual-DAC ***Colinear*** approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM63P is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table I shows the conversion made by the internal logic of the PCM63P from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM63P in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specification for the PCM63P is total harmonic distortion plus noise (THD+N). Digital data words are read into the PCM63P at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to an I to V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

For the audio bandwidth, THD+N of the PCM63P is essentially flat for all frequencies. The typical performance curve, "THD+N vs Frequency," shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low-level signal performance of the dual-DAC ***Colinear*** architecture of the PCM63P.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS} + Noise_{RMS} / Signal_{RMS}$ expressed in dB. For the PCM63P, THD+N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD+N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111 + 1LSB*	111...111
+Full Scale – 1LSB	011...110	111...111 + 1LSB*	111...110
Bipolar Zero + 2LSB	000...010	111...111 + 1LSB*	000...010
Bipolar Zero + 1LSB	000...001	111...111 + 1LSB*	000...001
Bipolar Zero	000...000	111...111 + 1LSB*	000...000
Bipolar Zero – 1LSB	111...111	111...111	000...000
Bipolar Zero – 2LSB	111...110	111...110	000...000
–Full Scale + 1LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

*The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to ***Colinear*** Conversion Chart.

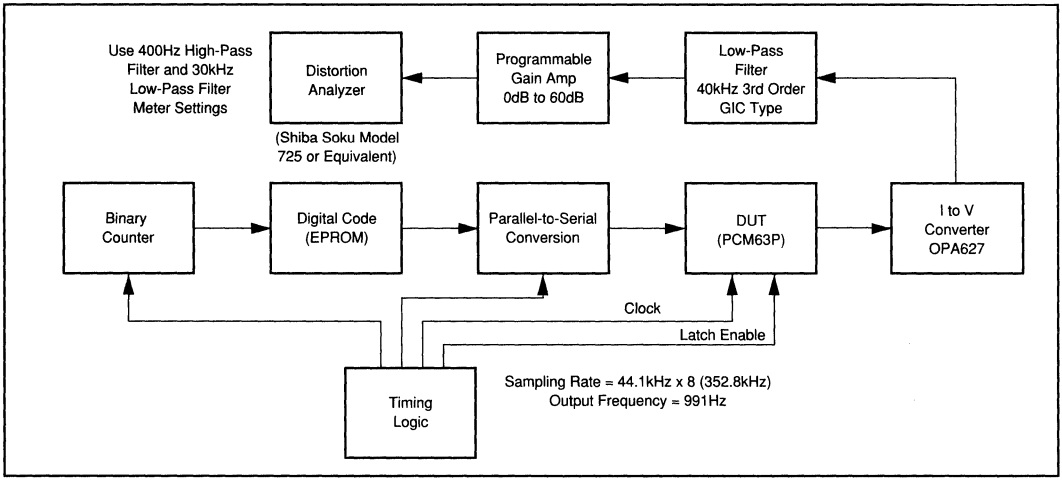


FIGURE 1. Production THD+N Test Setup.

Colinear architecture of the PCM63P, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM63P at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM63P at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal. This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM63P's ***Colinear*** DAC circuitry.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased from –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-Bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM63P tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATIONS

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM63P is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique dual-DAC ***Colinear*** architecture of the PCM63P, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-Bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM63P, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bitstream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM63P, the extremely low THD+N performance is typically indicative of 16-bit to 17-bit integral linearity in the DAC, depending on the grade specified. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, And Temperature Drift

Although the PCM63P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM63P accepts TTL compatible logic input levels. Noise immunity is enhanced by the use of differential current mode logic input architectures on all input signal lines. The data format of the PCM63P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after LE (P20, Latch Enable) has gone low.

All DAC serial input data (P21, DATA) bit transfers are triggered on positive clock (P18, CLK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable (P20, LE). The change in the output of the DAC coincides with the falling edge of Latch Enable (P20, LE). Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM63P is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16x oversampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The maximum clock rate of 25MHz is guaranteed, but is not 100% final tested. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM63P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable (LE, P20) goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

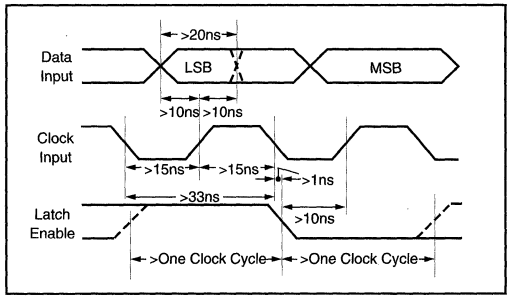
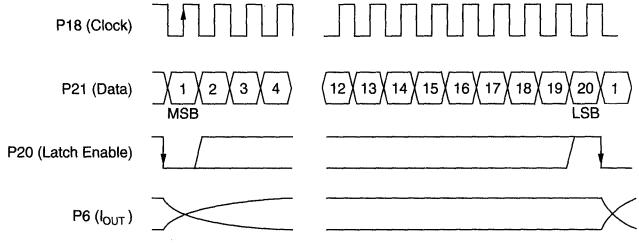


FIGURE 3. Setup and Hold Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT	VOLTAGE OUTPUT (With External Op Amp)
1,048,576LSBs	Full Scale Range	4.00000000mA	6.00000000V
1LSB	NA	3.81469727nA	5.72204590μV
$7FFFF_{HEX}$	+Full Scale	–1.99999619mA	+2.99999428V
00000_{HEX}	Bipolar Zero	0.00000000mA	0.00000000V
$FFFFF_{HEX}$	Bipolar Zero – 1LSB	+0.00000381mA	–0.00000572V
80000_{HEX}	–Full Scale	+2.00000000mA	–3.00000000V

TABLE II. Digital Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 20-bit data words, Latch Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

INSTALLATION

POWER SUPPLIES

Refer to Figure 4 for proper connection of the PCM63P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P9 and P10) should be left open if not used. The PCM63P only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in Figure 4, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM63P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM63P as possible to reduce noise pickup from surrounding circuitry.

MSB ADJUSTMENT CIRCUITRY

Near optimum performance can be maintained at all signal levels without using the optional MSB adjust circuitry of the PCM63P shown in Figure 5. Adjustability is provided for those cases where slightly better full-scale THD+N is desired. Use of the MSB adjustments will only affect larger dynamic signals (between 0dB and –6dB). This improvement comes from bettering the gain match between the upper and lower DACs at these signal levels. The change is realized by small adjustments in the bit-2 weights of each DAC. Great care should be taken, however, as improper adjustment will easily result in degraded performance.

In theory, the adjustments would seem very simple to perform, but in practice they are actually quite complex. The first step in the theoretical procedure would involve making each bit-2 weight ideal in relation to its code minus one value (adjusting each potentiometer for zero differential nonlinearity error at the bit-2 major carries). This would be the starting point of each 100kΩ potentiometer for the next adjustment. Then, each potentiometer would be adjusted equally, in opposite directions, to achieve the lowest full-scale THD+N possible (reversing the direction of rotation

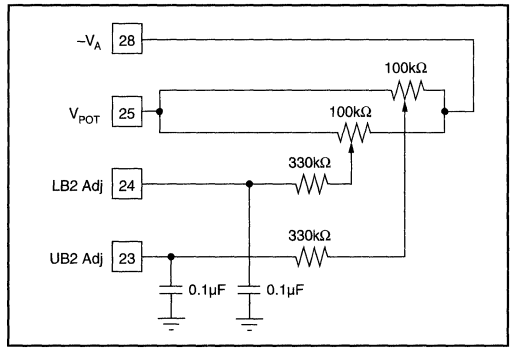


FIGURE 5. Optional Bit-2 Adjustment Circuitry.

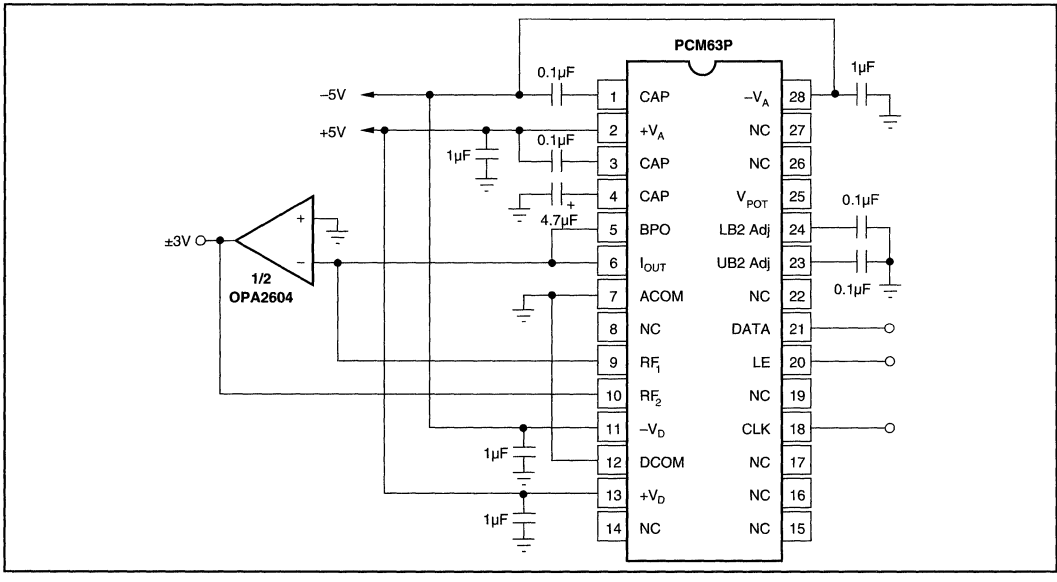


FIGURE 4. Connection Diagram.

for both if no immediate improvement were noted). This procedure would require the generation of the digital bit-2 major carry code to the input of the PCM63P and a DVM or oscilloscope capable of reading the output voltage for a one LSB step (5.72μV) in addition to a distortion analyzer.

A more practical approach would be to forego the minor correction for the bit-2 major carry adjustment and only adjust for upper and lower DAC gain matching. The problem is that just by connecting the MSB circuitry to the PCM63P, the odds are that the upper and lower bit-2 weights would be greatly changed from their unadjusted states and thereby adversely affect the desired gain adjustment. Just centering the 100kΩ potentiometers would not necessarily provide the correct starting point. To guarantee that each 100kΩ potentiometer would be set to the correct starting or null point (no current into or out of the MSB adjust pins), the voltage drop across each corresponding 330kΩ resistor would have to measure 0V. A voltage drop of ±1.25mV across either 330kΩ resistor would correspond to a ±1LSB change in the null point from its unadjusted state (1LSB in current or 3.81nA x 330kΩ = 1.26mV). Once these starting points for each potentiometer had been set, each potentiometer would then be adjusted equally, in opposite directions, to achieve the lowest full-scale THD+N possible. If no immediate improvement were noted, the direction of rotation for both potentiometers would be reversed. One direction of potentiometer counter-rotations would only make the gain mismatch and resulting THD+N worse, while the opposite would gradually improve and then worsen the THD+N after passing through a no mismatch point. The determination of the correct starting direction would be arbitrary. This procedure still requires a good DVM in addition to a distortion analyzer.

Each user will have to determine if a small improvement in full-scale THD+N for their application is worth the expense of performing a proper MSB adjustment.

APPLICATIONS

The most common application for the PCM63P is in high-performance and professional digital audio playback, such as in CD and DAT players. The circuit in Figure 6 shows the PCM63P in a typical combination with a digital interface format receiver chip (Yamaha YM3623), an 8x interpolating digital filter (Burr-Brown DF1700P), and two third-order low-pass anti-imaging filters (implemented using Burr-Brown OPA2604APs).

Using an 8x digital filter increases the number of samples to the DAC by a factor of 8, thereby reducing the need for a higher order reconstruction or anti-imaging analog filter on the DAC output. An analog filter can now be constructed using a simple phase-linear GIC (generalized immittance converter) architecture. Excellent sonic performance is achieved using a digital filter in the design, while reducing overall circuit complexity at the same time.

Because of its superior low-level performance, the PCM63P is also ideally suited for other high-performance applications such as direct digital synthesis (DDS).

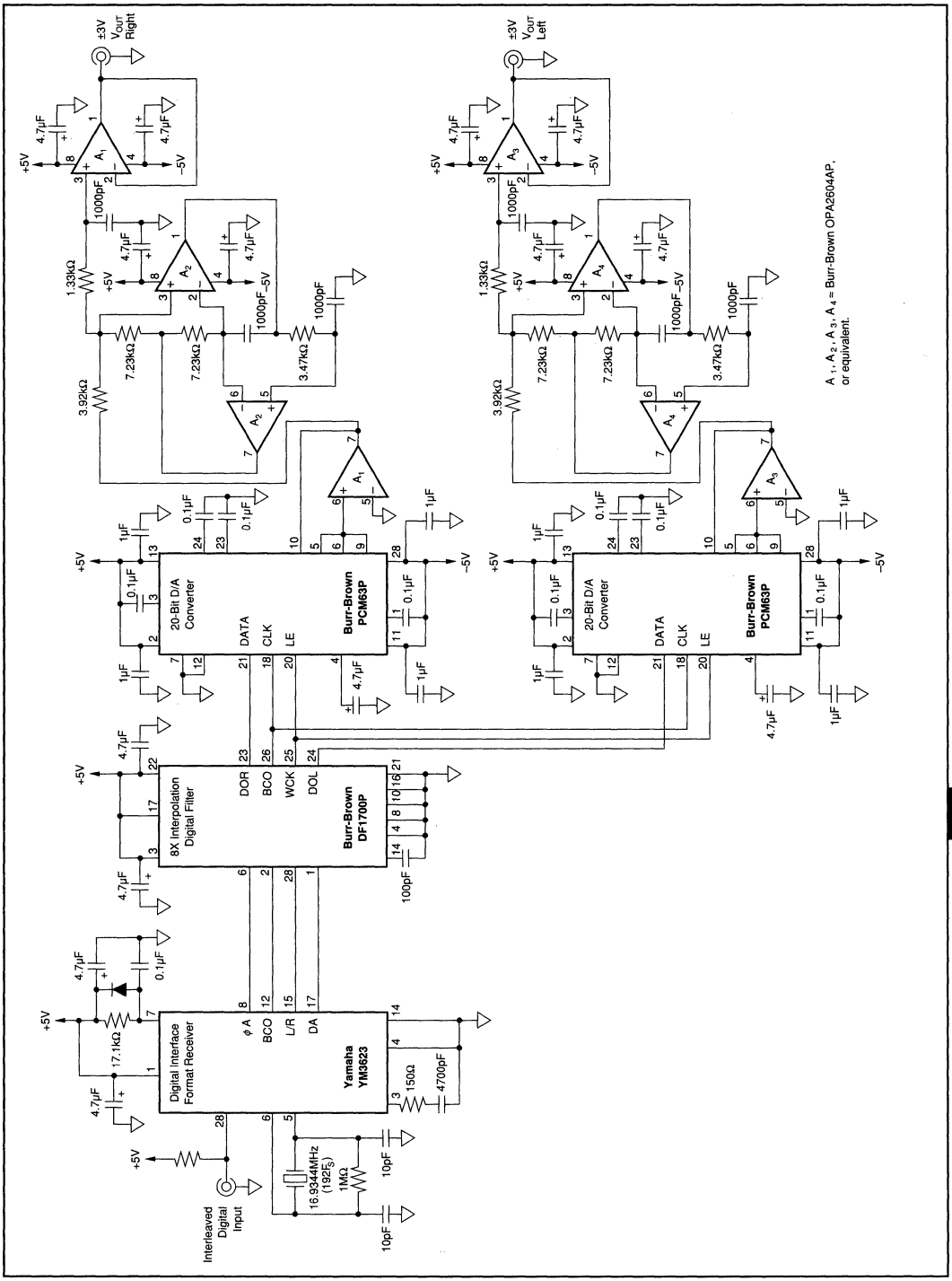


FIGURE 6. Stereo Audio Application.

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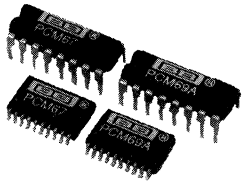


PCM67P/U
PCM69AP/AU

DEMO BOARD AVAILABLE
See Appendix A

Advanced 1-Bit BiCMOS Dual 18-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **18-BIT RESOLUTION DUAL AUDIO DAC**
- **EXCELLENT THD PERFORMANCE: 0.0025% (–92dB) at F/S, K Grade 1.0% (–40dB) at –60dB, K Grade**
- **HIGH S/N RATIO: 110dB typ (IHF-A)**
- **DUAL, CO-PHASE**
- **SINGLE SUPPLY +5V OPERATION**
- **LOW POWER: 75mW typical**
- **CAPABLE OF 16X OVERSAMPLING**
- **AVAILABLE IN SPACE SAVING 16-PIN DIP OR 20-PIN SOIC**
- **OPERATING TEMP RANGE: –25°C to +85°C**
- **EXTREMELY LOW GLITCH ENERGY**

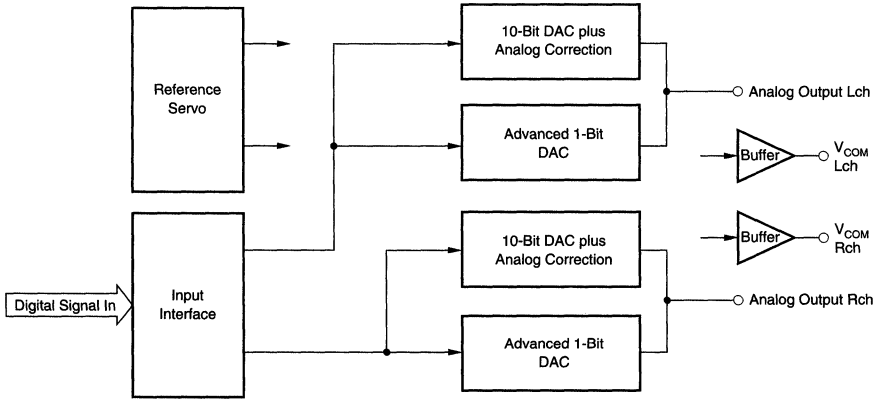
DESCRIPTION

The PCM67 and PCM69A dual 18-bit DAC are low cost, dual output 18-bit BiCMOS digital-to-analog converters utilizing a novel architecture to achieve excellent low level performance.

By combining a conventional thin-film R-2R ladder DAC, a digital offset technique with analog correction and an advanced one-bit DAC using first order noise shaping technique, the PCM67 and PCM69A achieve high resolution, minimal glitch, and low zero-crossing distortion.

PCM67 digital offset occurs at bit 9, making it ideal for high-performance CD players. PCM69A digital offset occurs at bit 4, making it an excellent choice for digital musical instruments and audio DSP.

Both PCM67 and PCM69A operate from a single +5V supply. The low power consumption and small size (16-pin PDIP or 20-pin SOIC) make these converters ideal for a variety of digital audio applications.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

All specifications at +25°C and $+V_A$, $+V_D$ = +5V unless otherwise noted

PARAMETER	CONDITIONS	PCM67/69A MIN	PCM67/69A TYP	PCM67/69A MAX	UNITS
RESOLUTION			18		Bits
DYNAMIC RANGE, THD+N at –60dB Referred to Full Scale			106		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}	I_{IH} = ±5µA	+2		$+V_D$	V
V_{IL}	I_{IL} = ±5µA	0		0.8	V
Data Format			Serial, MSB First, BTC[1]		
Input System Clock Frequency			16.9344		MHz
TOTAL HARMONIC DISTORTION + N[2,3,4]					
PCM67P/69AP, PCM67U/69AU					
f = 991Hz (0dB)	f_S = 352.8kHz		–86	–82	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–68		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–40	–34	dB
PCM67P-J/69AP-J, PCM67U-J/69AU-J					
f = 991Hz (0dB)	f_S = 352.8kHz		–91	–88	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–72		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
PCM67P-K/69AP-K, PCM67U-K/69AU-K					
f = 991Hz (0dB)	f_S = 352.8kHz		–95	–92	dB
f = 991Hz (–20dB)	f_S = 352.8kHz		–74		dB
f = 991Hz (–60dB)	f_S = 352.8kHz		–46	–40	dB
CHANNEL SEPARATION	(f = 1kHz)		106		dB
ACCURACY					
Level Linearity	at –90dB Signal Level		±1		dB
Gain Error			±3	±10	%
Gain Mismatch, Channel-to-Channel			±1	±5	%
Gain Drift	0°C to +70°C		95		ppm/°C
Warm-up Time			1		Minute
IDLE CHANNEL SNR[5]	20Hz to 40kHz at BPZ[6]		110		dB
ANALOG OUTPUT					
Output Range (±3%)			1.2		mA
Output Impedance (±30%)			1.8		kΩ
V_{COM}		3.35	3.50	3.65	V
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS, System Clock = 16.9344MHz					
$+V_A$, $+V_D$ Supply Voltage Range	$+V_A$ = $+V_D$	+4.75	+5.00	+5.25	V
$+I_A$, $+I_D$ Combined Supply Current	$+V_A$, $+V_D$ = +5V		15	20	mA
Power Dissipation	$+V_A$, $+V_D$ = +5V		75	105	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter output frequency/signal level (both left and right channels are "on"). (4) D/A converter sample frequency (8 x 44.1kHz; 8X oversampling per channel). (5) Ratio of $Noise_{RMS}$/$Signal_{RMS}$. Measured using a 40kHz 3rd-order GIC (Generalized Immittance Converter) filter and an A-weighted filter. (6) Bipolar Zero.

PIN ASSIGNMENTS

PCM67P PCM69AP	PCM67U PCM69AU	DESCRIPTION	MNEMONIC
1	1	+5V Analog Supply Voltage	$+V_A$
2	2	Left Voltage Common	LV_{COM}
	3	No Connection	NC
3	4	Left Current Output (0 to 1.2mA)	LI_{OUT}
4	5	Servo Decoupling Capacitor	SRVCAP
5	6	Reference Decoupling Capacitor	REFCAP
6	7	Right Current Output (0 to 1.2mA)	RI_{OUT}
	8	No Connection	NC
7	9	Right Voltage Common	RV_{COM}
8	10	Analog Common	ACOM
9	11	Digital Common	DCOM
	12	Mode Control 2	MC2
10	13	Right Data Input	RDATA
11	14	Bit Clock	BTCK
12	15	System Clock	SYSCK
13	16	Word Clock	WDCK
14	17	Left Data Input	LDATA
	18	Mode Control 3	MC3
15	19	Mode Control 1	MC1
16	20	+5V Digital Supply Voltage	$+V_D$

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM67P/69AP	16-Pin Plastic DIP	180
PCM67U/69AU	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

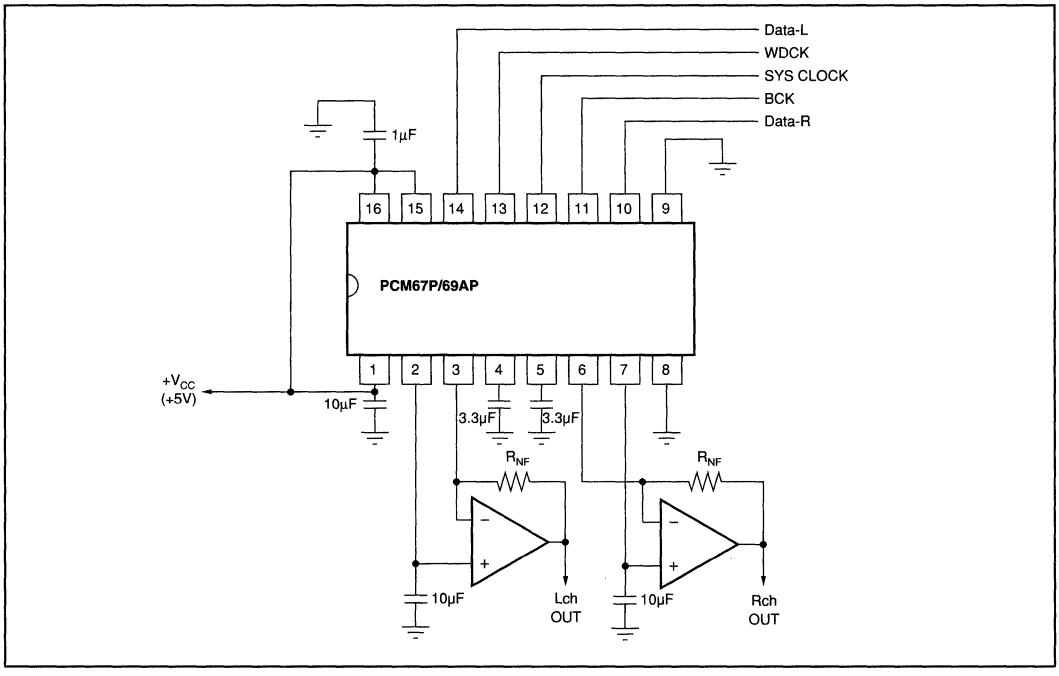
$+V_A$, $+V_D$ to ACOM, DCOM	0V to +6.5V
ACOM to DCOM	±0.5V
Digital Inputs to DCOM	–0.3V to $+V_D$ + 0.3V
Power Dissipation	300mW (U Package), 500mW (P Package)
Lead Temperature, (soldering, 10s)	+260°C
Max Junction Temperature	+165°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

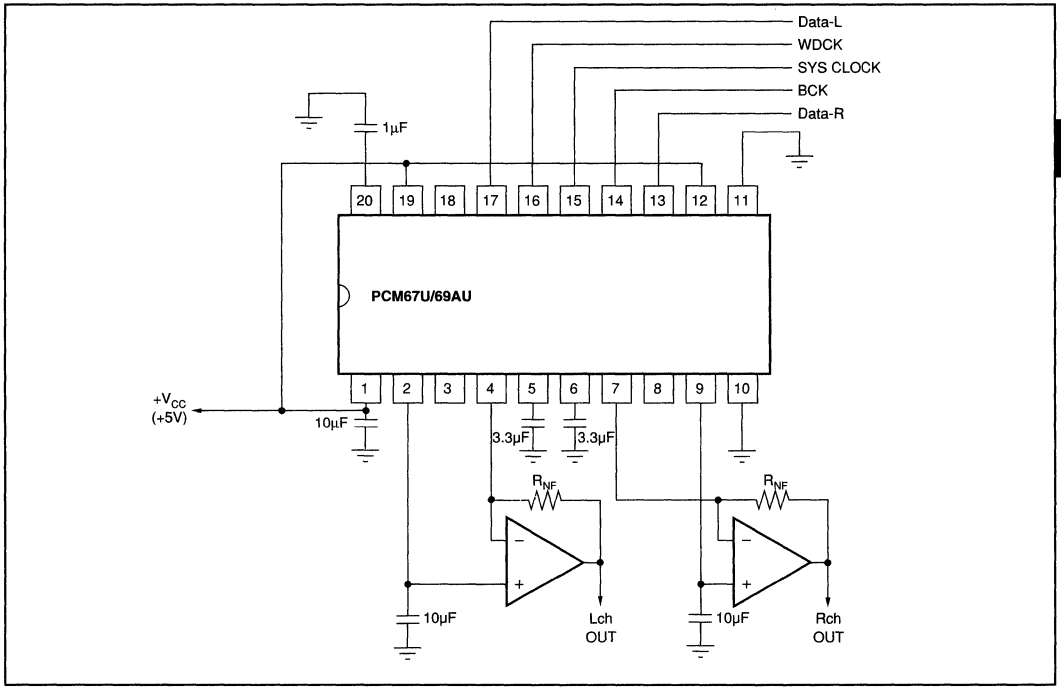
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN CONFIGURATION — PCM67P/69AP (16-Pin DIP)



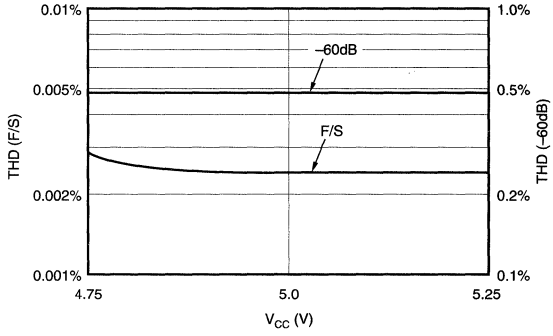
PIN CONFIGURATION — PCM67U/69AU (20-Pin SOIC)



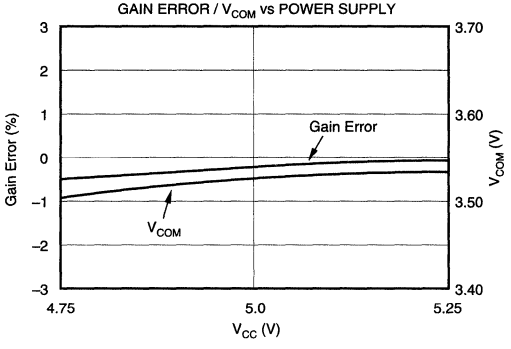
TYPICAL PERFORMANCE CURVES

All specifications at +25°C and V_{CC} = +5.0V unless otherwise noted.

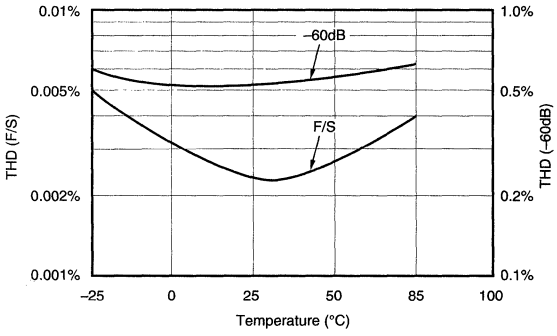
THD vs POWER SUPPLY VOLTAGE



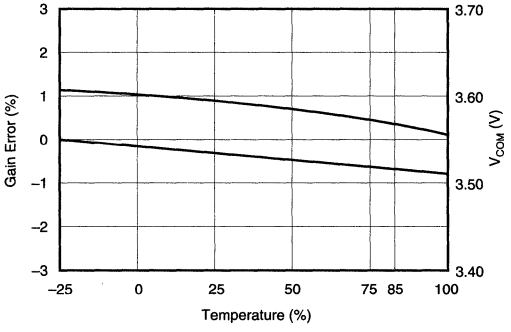
GAIN ERROR / V_{COM} vs POWER SUPPLY



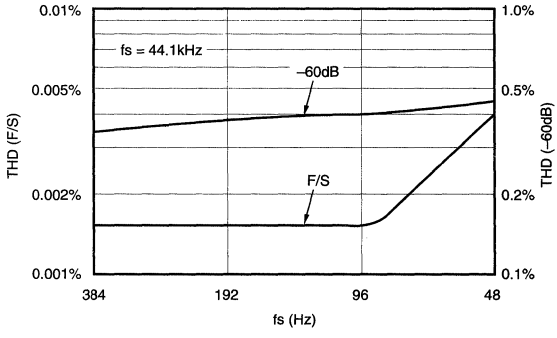
THD vs TEMPERATURE



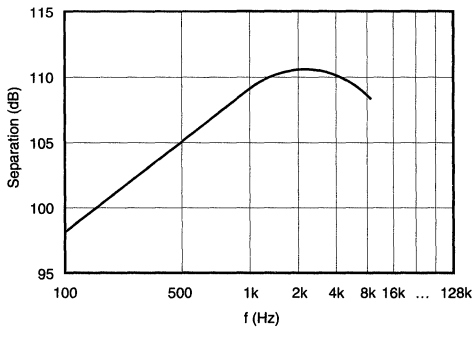
GAIN ERROR / V_{COM} vs TEMPERATURE



THD vs SYSTEM CLOCK FREQUENCY



CHANNEL SEPARATION vs SIGNAL FREQUENCY



DISCUSSION OF SPECIFICATIONS

The PCM67 and PCM69A are specified to provide critical performance criteria for a variety of applications. The accuracy of a D/A converter is described by the transfer function shown in Figure 1.

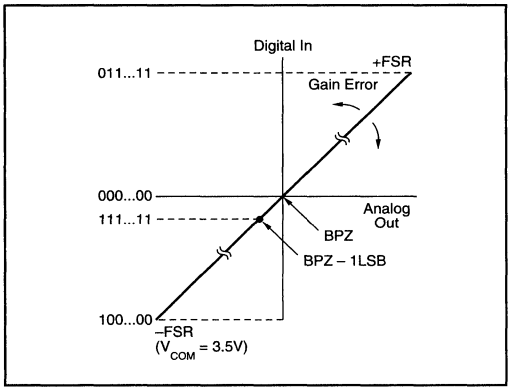


FIGURE 1. Transfer Performance.

DIGITAL INPUT CODE

The PCM67/69A accepts Binary Two's Complement (BTC) digital input code (MSB FIRST).The relationship of digital input to analog output is shown in Table 1.

DIGITAL INPUT	ANALOG OUTPUT (VOLTAGE)	ANALOG OUTPUT (CURRENT)
7FFFFF (HEX)	+FSR	–1.2mA
00003F (HEX)	BPZ	–0.6mA
FFFFFF (HEX)	BPZ – 1LSB	–0.59995mA
80003F (HEX)	–FSR	0mA

TABLE I. Digital Code and Analog Out.

GAIN ERROR AND GAIN MISMATCH, CHANNEL-TO-CHANNEL

Gain error is defined as deviation of the output current span from the ideal span of 1.2mA (FSR) on each channel. Gain error of PCM67/69A is typically ±3% of FSR.

Gain mismatch, channel-to-channel is defined as the difference in gain error between the left channel and right channel.

THE RELATIONSHIP OF V_{COM} AND I/V OUT

The output current range of PCM67 and PCM69A is 0mA to 1.2mA as shown in Table 1.

In the typical application, the non-inverting input of the external I/V op amp is connected to the V_{COM} pin of PCM67 and PCM69A. Accordingly, the output voltage level at FSR after I/V conversion is V_{COM} voltage (+3.5V) as shown in Figure 2.

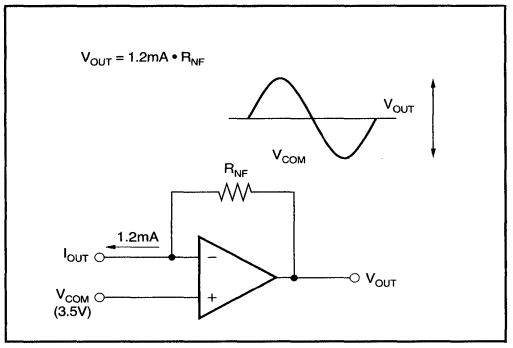


FIGURE 2. I/V Amplifier Circuit.

S/N RATIO

S/N ratio is defined as the ratio of full scale output and no input noise level at BPZ point. The PCM67/69A is specified at 110dB typical with "IHF-A" filter.

LEVEL LINEARITY ERROR

Level linearity error is defined as the deviation of actual analog output level from digital input level. PCM67/69A is specified at 1dB typical at –90dB output level. The 0.5LSB quantization error at –90dB of 16-bit conversion is equal to +1.94dB, –2.5dB.

TOTAL HARMONIC DISTORTION

THD is a key parameter in audio applications, THD is a measure of the magnitude and distribution of the linearity error, differential linearity error, and noise, as well as quantization error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM67/69A error referred to the input can be shown to be

$$\varepsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[E_L(i) + E_Q(i)\right]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM67 or PCM69A at each sampling point. THD can then be expressed as

$$THD = \frac{\varepsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}\left[E_L(i) + E_Q(i)\right]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to THD.

For PCM67 and PCM69A the test period is set at an 8X oversampling rate (352.8kHz = 44.1kHz • 8), which is the typical sample rate for CD player applications.

The test signal frequency is 991Hz and the amplitude of the signal level is F/S (0dB), and –60dB down from F/S.

All THD tests are performed without a deglitcher circuit and without a 20kHz low pass filter.

SYSTEM CLOCK REQUIREMENTS

The PCM67 and PCM69A need a system clock for the one-bit noise shaping DAC operation.

The PCM67 is capable of only a 384Fs corollary system clock frequency such as 192Fs, 96Fs (24 times word rate or integer multiple of 24).

The PCM69A is capable of any system clock up from 48Fs to 384Fs such as 384Fs, 256Fs, 100Fs with condition for timing as described in "Timing of PCM69A" in Figure 5.

The user can choose either model for their application. Table II shows the different SYSCLK options.

MODEL	BASIC SYSCLK	OTHER CAPABLE SYSCLK
PCM67	384Fs	192Fs, 96Fs
PCM69A	Any Clock (with timing condition) Examples: 384Fs, 300Fs, 256Fs, 200Fs, 90Fs	

TABLE II. System Clock Requirements.

LOGIC TIMING

The serial data bit transfers are triggered on positive bit clock (BCK) edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Word Clock (WDCK). The change in the output of the DAC coincides with the falling edge of WDCK.

Refer to Figure 3 for graphical relationships of these signals. The setup and hold timing relationships for these signals are shown in Figure 4.

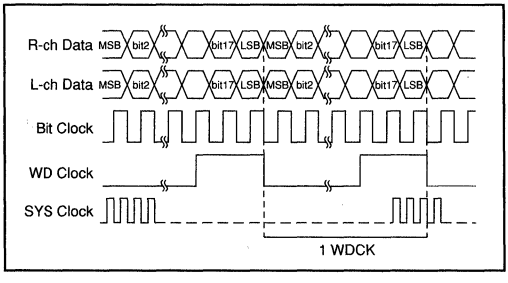


FIGURE 3. Timing Diagram.

The PCM67/69A accepts TTL compatible logic input levels. The data format of the PCM67/69A is BTC with the most significant bit (MSB) being first in the serial input bit stream.

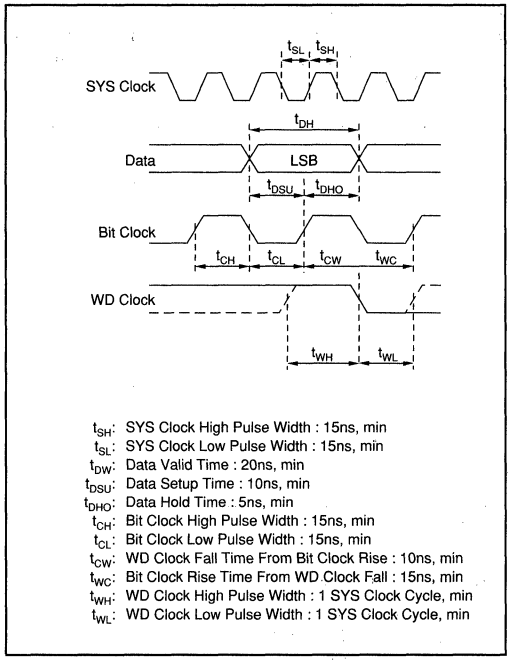


FIGURE 4. Timing Specification.

TIMING OF PCM69A

PCM69A timing is similar to PCM67 except that PCM69A is capable of operating from any system clock up to 384Fs. For synchronized operation, PCM69A system clock and WDCK timing must be as shown in Figure 5.

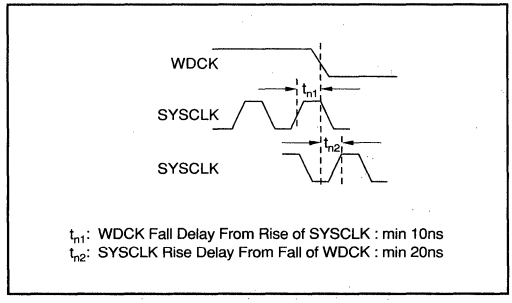


FIGURE 5. Timing of PCM69A for SYSCLK and WDCK.

INSTALLATION

POWER SUPPLIES

Refer to "Pin Configuration" diagram for proper connection of the PCM67/69A. The PCM67/69A requires only a +5V supply. Both analog and digital supplies should be tied together at a single point, as no real advantage is gained by using separate supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output.

FILTER CAPACITOR REQUIREMENTS

As shown in the "Pin Configuration" diagram, various sizes of decoupling capacitors can be used with no special tolerances required. All capacitors should be as close to the appropriate pins of the PCM67/69A as possible to reduce noise pickup from surrounding circuitry.

A power supply decoupling capacitor should be used near the analog supply pin to maximize power supply rejection, as shown in Figure 6, regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM67/69A as possible.

The value of these capacitors is influenced by actual board layout design and noise from power supplies and other digital input lines.

The best suitable value for the capacitors should be determined by the user's actual application board.

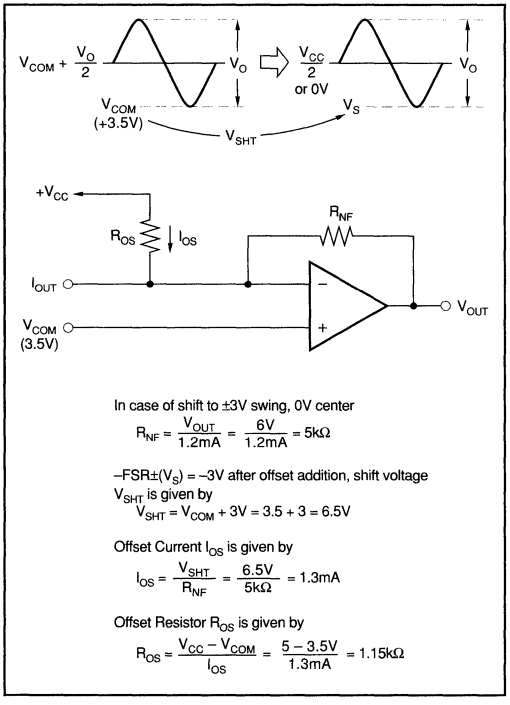


FIGURE 6. Shift of I/V Out Voltage.

SHIFT OF I/V OUT VOLTAGE

If the user requires a bipolar voltage output centered around 0V or one-half of V_{CC}, the output can be shifted by adding an offset current on the inverting point of the I/V op amp as shown in Figure 6.

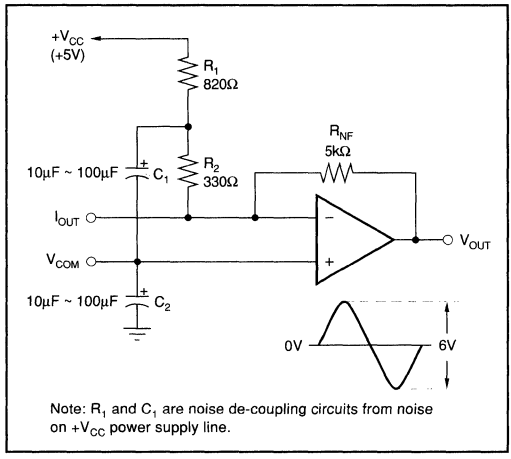


FIGURE 7. Useful Application Circuit for Shift of I/V Out Voltage.

INTERFACE CONTROL FUNCTION

Both the PCM67 and PCM69A (SOIC package type) are capable of 16-bit L/R serial input and 20-bit L/R parallel input as shown in Table 3.

MC1	MC2	MC3	DATA-R	INPUT FORMAT
0	0	1	0	16-Bit L/R Serial(1) $\overline{L}R\overline{L}R$ WDCK
0	0	1	1	16-Bit L/R Serial(1) $\overline{L}R\overline{L}R$ WDCK
0	1	1	0	18-Bit L/R Serial(1) $\overline{L}R\overline{L}R$ WDCK
0	1	1	1	18-Bit L/R Serial(1) $\overline{L}R\overline{L}R$ WDCK
1	0	1	X	20-Bit L/R Parallel
1	0	0	X	20-Bit L/R Parallel [WDCK Invert]
1	1	1	X	18-Bit L/R Parallel
1	1	0	X	18-Bit L/R Parallel [WDCK Invert]

NOTE: (1) Data input to Data-Lch (Pin 17) for L/R serial format.

TABLE III. Interface Control Function of SOIC.

PCM67P and PCM69AP (DIP package) have only 18-bit L/R serial input function as shown in Table 4.

MC1	DATA-R	INPUT FORMAT
0	0	18-Bit L/R Serial $\overline{L}R\overline{L}R$ WDCK
0	1	18-Bit L/R Serial $\overline{L}R\overline{L}R$ WDCK
1	X	18-Bit L/R Parallel

TABLE IV. Interface Control Function of DIP.

DIGITAL FILTER INTERFACE

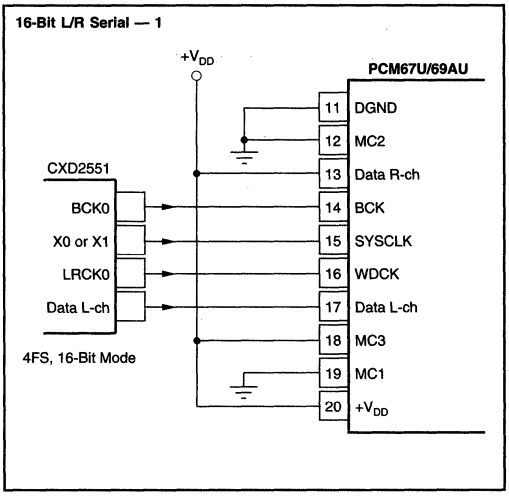


FIGURE 8. Using Sony CXD2551.

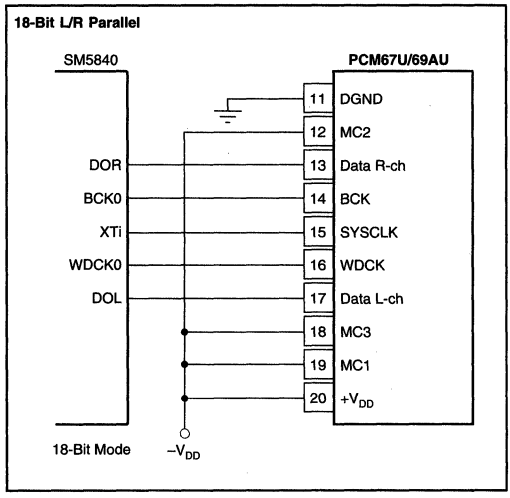


FIGURE 10. Using NPC SM5840.

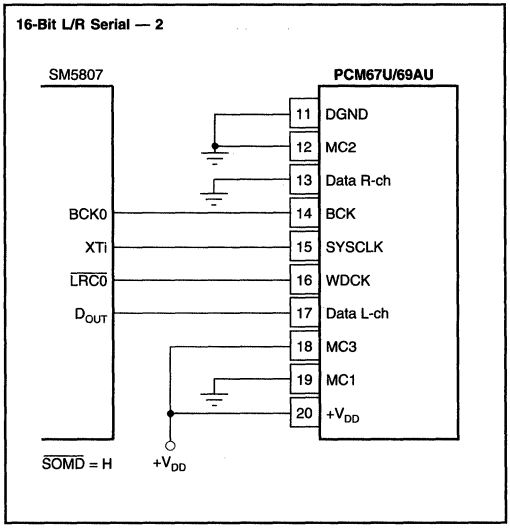


FIGURE 9. Using NPC SM5807.

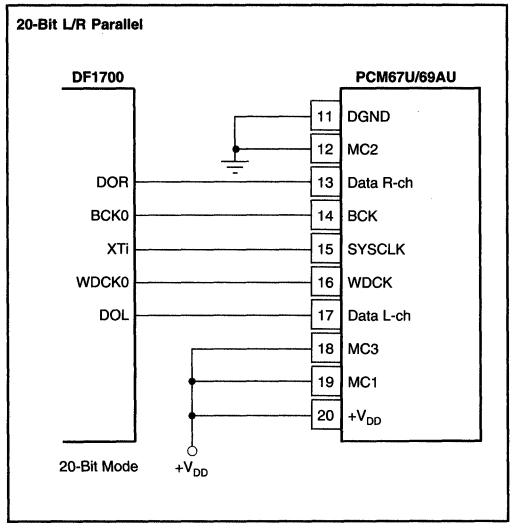


FIGURE 11. Using Burr-Brown DF1700.

THEORY OF OPERATION

Digital converters in audio systems have traditionally utilized a laser-trimmed, current-source DAC architecture. Unfortunately, this type of technology suffers from the problems inherent in switching widely varying current levels. Design improvements have helped, but DACs of this type still exhibit low-level nonlinearity due to errors at the major carry.

Recently, DACs employing a different architecture have been introduced. Most of these DACs utilize a one-bit DAC with "noise shaping" techniques and very high oversampling rate to achieve the digital-to-analog conversion. Basically, the trade-off is from very accurate but slow current sources to one rapidly sampled current source whose average output in the audio frequency range is equal to the current desired. Noise shaping insures that the "undesirable" frequencies associated with one-bit DAC output lie outside the audio range.

These "Bitstream", "MASH", or one-bit DACs overcome the low level linearity problems of conventional DACs, since there can be no major carry error. However, this architecture exhibits problems of its own: signal-to-noise performance is usually worse than a similar conventional DAC, "dither noise" may be needed in order to get rid of unwanted tones, a separate high-speed clock may be required, the part may show sensitivity to clock jitter, and a high-order low-pass filter is necessary to filter the DAC output.

The PCM67/69A is a cross between these two architectures. It includes both a conventional laser-trimmed, current-source DAC and an advanced one-bit DAC. The conventional DAC is a 10-bit DAC where each bit weight has been trimmed to 18-bit linearity. The one-bit DAC has a weight equal to bit 10 and employs a first-order noise shaper to generate the "bitstream."

This approach does not eliminate all the problems associated with the two architectures but rather minimizes them as much as possible. The conventional DAC still exhibits some major carry error which would normally reduce low-level linearity. However, to reduce this error even further, the PCM67/69A utilizes an offset technique whereby bit n is subtracted from the digital input code whenever it is positive (see Figure 1 and Table I). When this is done, an offset current equal to the weight of bit n is switched in to compensate. This offset comes from a one-bit DAC which has also been trimmed to 18-bit linearity. While this technique doesn't remove the major carry error completely, the "glitch" is only present in higher amplitude signals where it is much less audible.

As for the one-bit DAC, a number of problems with this architecture are also reduced: the DAC is designed to operate from the system clock, thus eliminating the need for a separate clock; the lower quantizing level of the DAC make it less sensitive to clock jitter; and output filtering requirements are reduced because "out-of-band noise" has smaller amplitude, is "farther-out," and increases much more slowly due to the first-order noise shaper. Still, it is important to keep in mind that the one-bit DAC imposes some design considerations. Figure 2 shows the THD + N of the converter versus "System Clock" frequency. This is the clock used to operate the one-bit DAC and noise shaper. Generally, the higher the oversampling the better. However, near full-scale, the converter is limited by other constraints and higher clock frequencies (past $96f_s$) tend to slightly worsen its performance. At low levels, performance improves almost linearly with increasing clock frequency. The one-bit DAC was designed to operate between $96f_s$ (4X oversampling) and $384f_s$ (16X oversampling). But, it can be operated at $48f_s$ (2X oversampling) with slightly reduced performance.

TOTAL HARMONIC DISTORTION + NOISE

A key specification for audio DACs is usually total harmonic distortion plus noise (THD + N). For the PCM67/69A, THD + N is tested in production as shown in Figure 12. Digital data words are read into the PCM67/69A at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 991Hz is realized. The output of the DAC goes to an I-to-V converter, then to a programmable gain amplifier to provide gain at lower signal output test levels, and then through a 40kHz low pass filter before being fed into an analog type distortion analyzer.

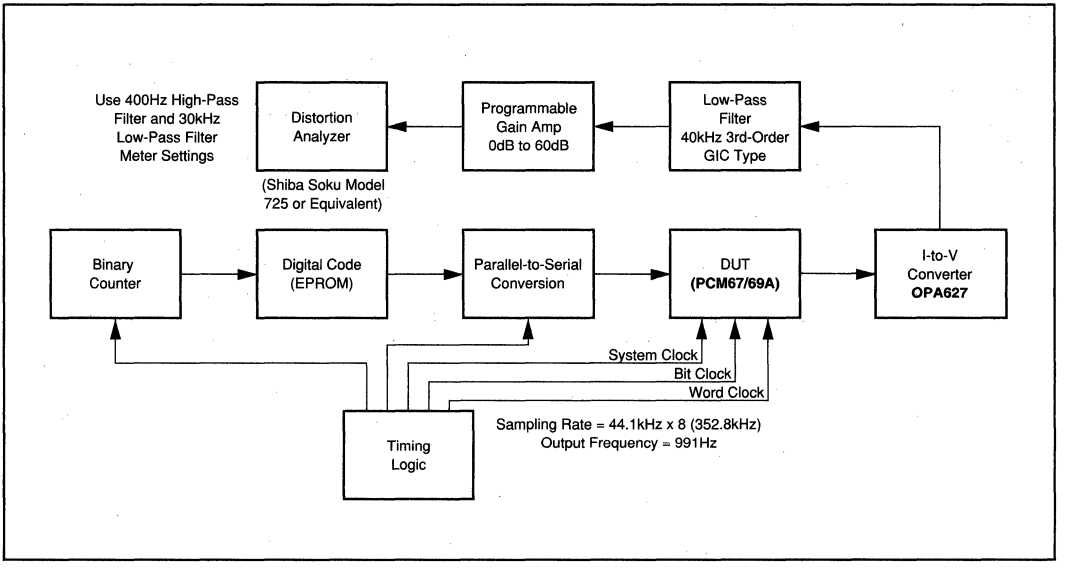


FIGURE 12. PCM67/69A THD+N Production Test.

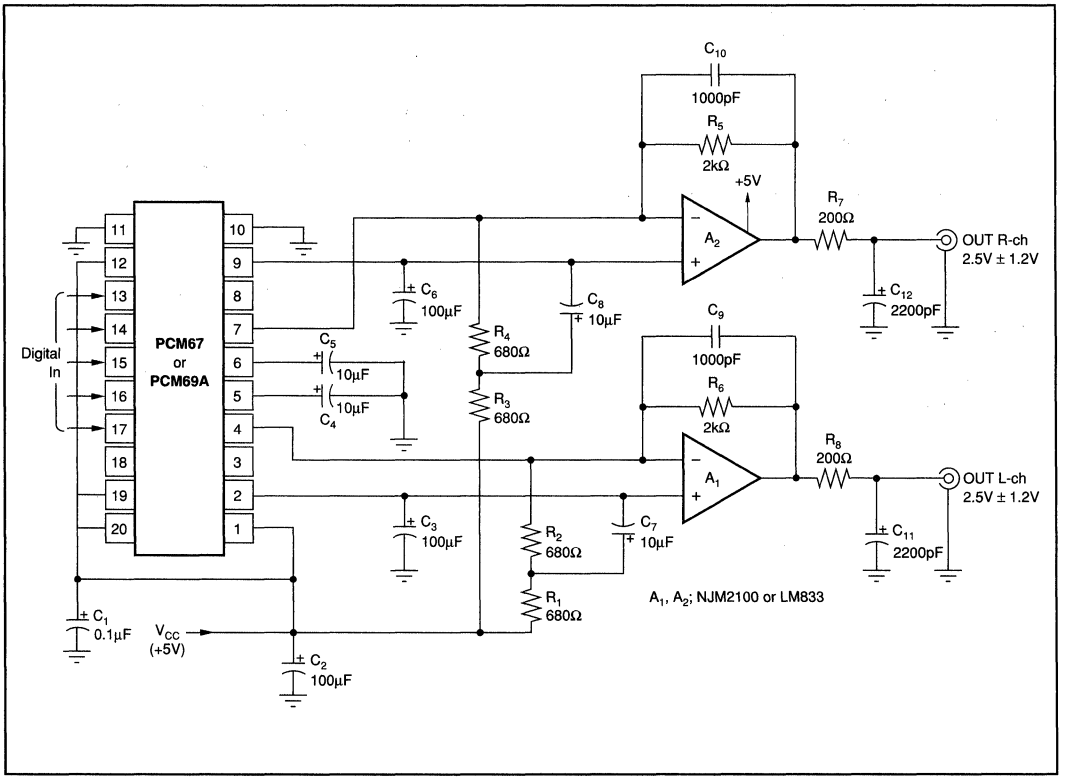


FIGURE 13. Single +5V Power Supply, with LPF, I/V Amp Application Circuit for Portable Digital Audio.

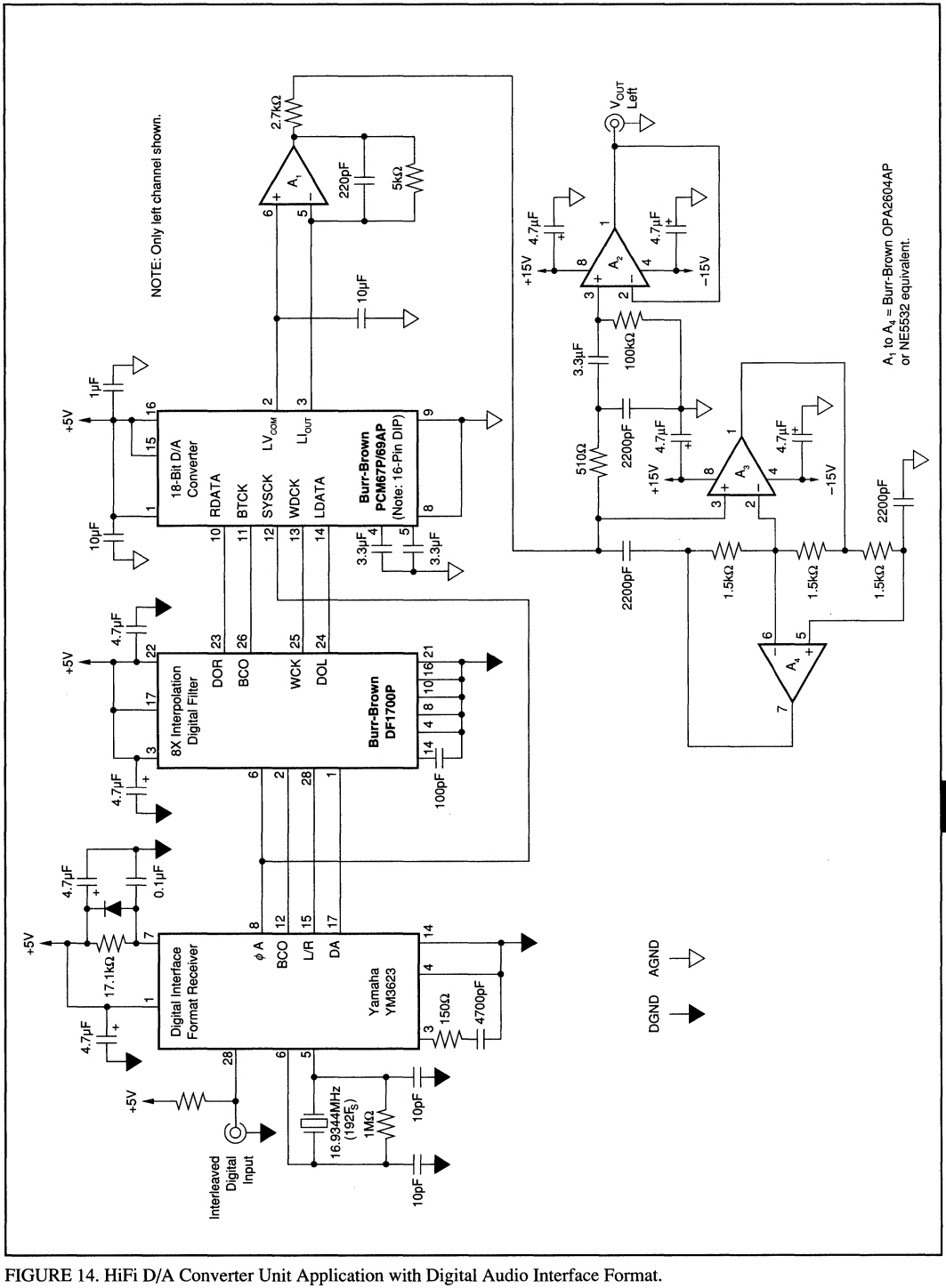


FIGURE 14. HiFi D/A Converter Unit Application with Digital Audio Interface Format.

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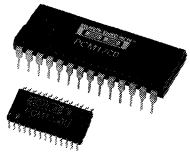


PCM1700U
PCM1700P

DEMO BOARD AVAILABLE
See Appendix A

Dual 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

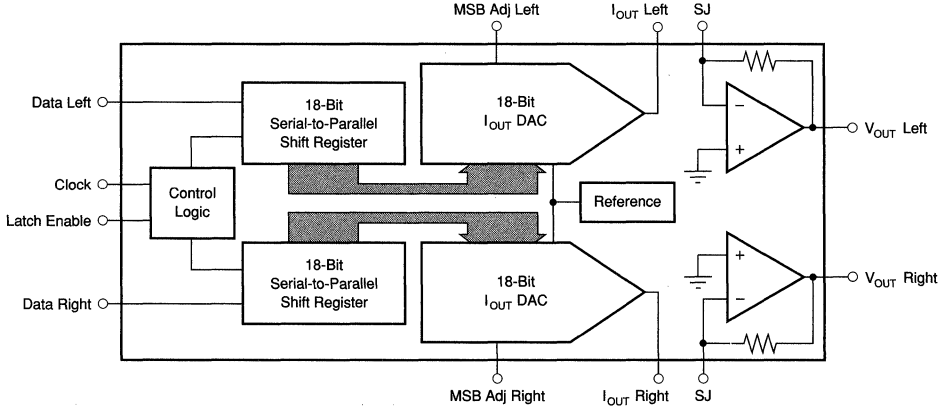
FEATURES

- **DUAL 18-BIT LOW-POWER MONOLITHIC AUDIO D/A CONVERTER**
- **VERY LOW MAX THD+N: –92dB Without External Adjust**
- **CO-PHASE, LOW-GLITCH ±3V OR ±670µA AUDIO OUTPUTS**
- **CAPABLE OF 16X PER CHANNEL OVERSAMPLING RATE**
- **COMPLETE WITH INTERNAL REFERENCE**
- **SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD PCM56P**
- **RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX**
- **COMPACT 28-PIN PLASTIC DIP OR SOIC**

DESCRIPTION

The PCM1700 is a low cost, high-performance, dual 18-bit digital-to-analog converter. The PCM1700 features low glitch, co-phase current and voltage outputs and only requires ±5V supplies. The PCM1700 comes complete with an internal reference and optional MSB adjustability for even greater THD performance. Total power dissipation is less than 400mW max. Low maximum Total Harmonic Distortion + Noise (–92dB max; PCM1700P-K) is 100% tested. The very fast PCM1700 is also capable of 16X oversampling rates on both channels simultaneously, providing freedom in output filter selection.

The PCM1700 comes in space-saving 28-pin plastic DIP and SOIC packages. PCM1700 accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



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SPECIFICATIONS

ELECTRICAL

At 25°C, and $\pm V_{CC}$ = ±5.00V unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1700U/U-J/U-K, PCM1700P/P-J/P-K MIN	TYP	MAX	UNITS
RESOLUTION		18			Bits
DYNAMIC RANGE			+108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL Compatible		
Logic Level: V_{IH}		+2		$+V_{DD}$	V
V_{IL}		0		+0.8	V
I_{IH}	V_{IH} = +2.7V			+1	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial BTC[1]		
Input Clock Frequency		11.288	20		MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[6]					
PCM1700_:					
f = 991kHz (0dB)	f_S = 352.8kHz[4]		–88	–82	dB
f = 991kHz (–20dB)	f_S = 352.8kHz		–74	–68	dB
f_{IN} = 991kHz (–60dB)	f_S = 352.8kHz		–34	–28	dB
PCM1700_-J:					
f = 991kHz (0dB)	f_S = 352.8kHz		–94	–88	dB
f = 991kHz (–20dB)	f_S = 352.8kHz		–76	–74	dB
f = 991kHz (–60dB)	f_S = 352.8kHz		–36	–34	dB
PCM1700_-K:					
f = 991kHz (0dB)	f_S = 352.8kHz		–98	–92	dB
f = 991kHz (–20dB)	f_S = 352.8kHz		–80	–74	dB
f = 991kHz (–60dB)	f_S = 352.8kHz		–40	–34	dB
CHANNEL SEPARATION		+96	+108		dB
SIGNAL-TO-NOISE RATIO[5]	20Hz to 20kHz at BPZ[6]		+108		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±3	%
Gain Mismatch	Channel to Channel		±1	±3	%
Bipolar Zero Error			10		mV
BPZ Error Mismatch	Channel to Channel		5		mV
BPZ Differential Linearity Error[7]			±1		LSB
Gain Drift			100		ppm/°C
Bipolar Zero Drift			20		ppm of FSR/°C
Warm-up Time		1			minute
POWER SUPPLY REJECTION	$\pm V_{CC}$ to V_{OUT}		+86		dB
ANALOG OUTPUT					
Voltage: Output Range			±3		V
Output Impedance			0.1		Ω
Current Output			±2		mA
Capacitive Load Drive	R_{LOAD} = 1.5kΩ		TBD		pF
Short Circuit Duration			Indefinite		
Settling Time			Sufficient to Meet THD+N Specs		
Glitch Energ			Meets All THD+N Specs Without External Output Deglitching		
Current: Output Range	(±2%)		±670		µA
Output Impedance	(±2%)		1.67		kΩ
POWER SUPPLY REQUIREMENTS					
$\pm V_{CC}$ Supply Voltage		+4.75	+5.00	+5.25	V
Supply Current: $+I_{CC}$	$+V_{CC}$ = +5.0V		+18	+30	mA
$-I_{CC}$	$-V_{CC}$ = –5.0V		–42	–65	mA
Power Dissipation	$\pm V_{CC}$ = ±5.0V		280	475	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (6) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter input frequency/signal level on both left and right channels. (4) D/A converter sample frequency (8 X 44.1kHz; 8X oversampling per channel). (5) Ratio of Noise$_{RMS}$ / Signal$_{RMS}$. Measured using an A-weighted filter. (6) Bipolar zero. (7) Differential non-linearity at bipolar major carry input code. Measured in 16-bit LSBs. Adjustable to zero error.

PIN ASSIGNMENTS (Plastic PKG)

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply	$-V_{CC}$
2	Left Channel Servo-Amp Decoupling Point	CAP
3	Left Channel MSB Adjustment	MSB ADJ (L)
4	No Connect	NC
5	Left Channel Bipolar Offset Decoupling Point	CAP
6	Left Channel Current Output	IOUT (L)
7	Left Channel Analog Common	ACOM
8	Left Channel Summing Junction	SJ (L)
9	Left Channel Voltage Output	VOUT (L)
10	No Connect	NC
11	+5V Digital Supply	$+V_{DD}$
12	Left Channel Data Input	DATA
13	Clock Input	CLOCK
14	–5V Logic Supply	$-V_{DD}$
15	Latch Enable Input	LE
16	Right Channel Data Input	DATA (R)
17	Digital Common	DCOM
18	No Connect	NC
19	Right Channel Voltage Output	VOUT (R)
20	Right Channel Summing Junction	SJ (R)
21	Right Channel Analog Common	ACOM
22	Right Channel Current Output	IOUT (R)
23	Right Channel Bipolar Offset Decoupling Point	CAP
24	Right Channel MSB Adjustment	MSB ADJ (R)
25	Right Channel Servo-Amp Decoupling Point	CAP
26	MSB Adjustment Potentiometer Voltage Output	VPOT
27	+5V Analog Supply	$+V_{CC}$
28	Digital Common	DCOM

ORDERING INFORMATION

PCM1700 ( ) ( )

Basic Model Number

P: Plastic U: SOIC

Performance Grade Code

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±7.5VDC
Input Logic Voltage	–1V to $+V_{CC}$
Power Dissipation	500mW
Operating Temperature	–25°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

PIN ASSIGNMENTS (SOIC PKG)

PIN	DESCRIPTION	MNEMONIC
9	–5V Analog Supply	$-V_{CC}$
10	Left Channel Servo-Amp Decoupling Point	CAP
11	Left Channel MSB Adjustment	MSB ADJ (L)
19	No Connect	NC
12	Left Channel Bipolar Offset Decoupling Point	CAP
13	Left Channel Current Output	I_{OUT} (L)
14	Left Channel Analog Common	ACOM
15	Left Channel Summing Junction	SJ (L)
16	Left Channel Voltage Output	V_{OUT} (L)
17	No Connect	NC
18	+5V Digital Supply	$+V_{DD}$
20	Left Channel Data Input	DATA
21	Clock Input	CLOCK
22	–5V Logic Supply	$-V_{DD}$
23	Latch Enable Input	LE
24	Right Channel Data Input	DATA (R)
25	Digital Common	DCOM
26	No Connect	NC
27	Right Channel Voltage Output	V_{OUT} (R)
28	Right Channel Summing Junction	SJ (R)
1	Right Channel Analog Common	ACOM
2	Right Channel Current Output	I_{OUT} (R)
3	Right Channel Bipolar Offset Decoupling Point	CAP
4	Right Channel MSB Adjustment	MSB ADJ (R)
5	Right Channel Servo-Amp Decoupling Point	CAP
6	MSB Adjustment Potentiometer Voltage Output	V_{POT}
7	+5V Analog Supply	$+V_{DD}$
8	Digital Common	DCOM

NOTE: In the SOIC (PCM1700U) package, the die is rotated 90°. Therefore, the pin assignments are different from the DIP. See pin assignments on page 4 for details.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1700U	28-Pin SOIC	217
PCM1700U-J	28-Pin SOIC	217
PCM1700U-K	28-Pin SOIC	217
PCM1700P	28-Pin Plastic DIP	126
PCM1700P-J	28-Pin Plastic DIP	126
PCM1700P-K	28-Pin Plastic DIP	126

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

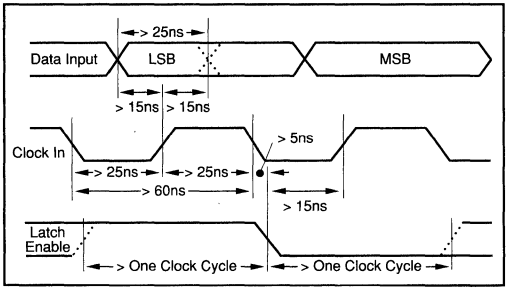

FIGURE 1. PCM1700P Setup and Hold Timing Diagram.

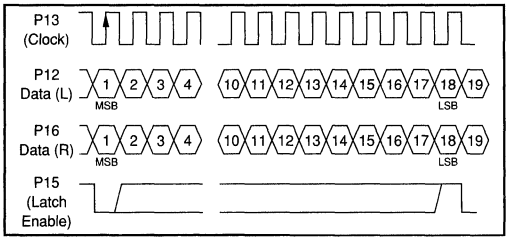

FIGURE 2. Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
1FFFF Hex	+ FS	+2.99997711	–0.66999489
00000 Hex	BPZ	0.00000000	0.00000000
3FFFF Hex	BPZ – 1LSB	–0.00002289	+0.00000511
20000 Hex	– FS	–3.00000000	+0.67000000

TABLE I. PCM1700 Input/Output Relationships.

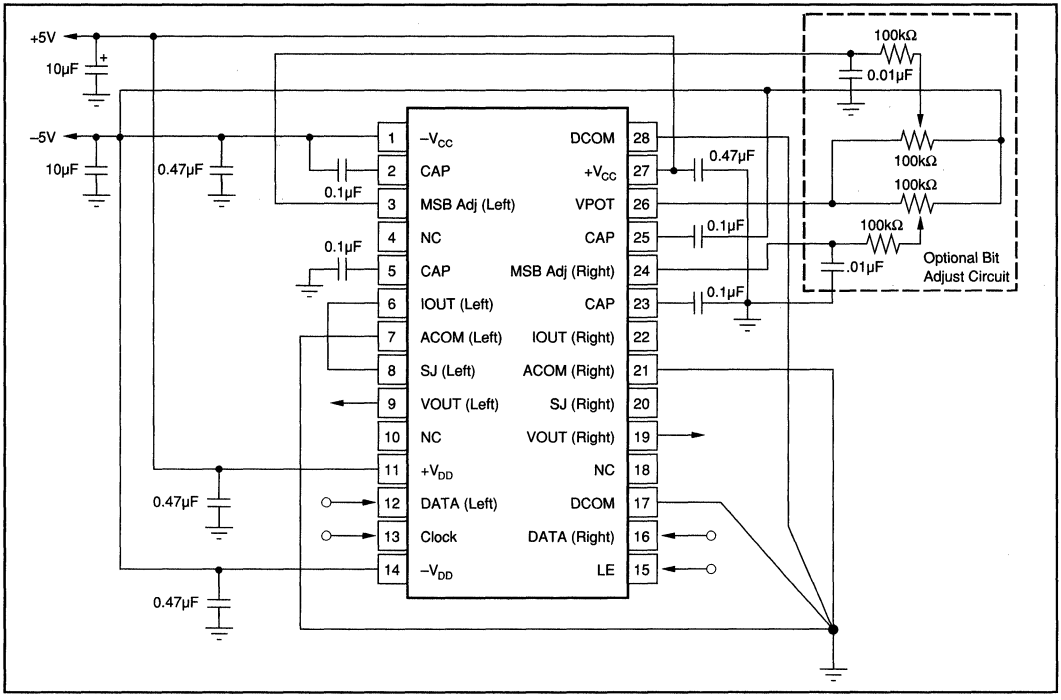

FIGURE 3. Voltage Output Connection Diagram (DIP Package Diagram.)

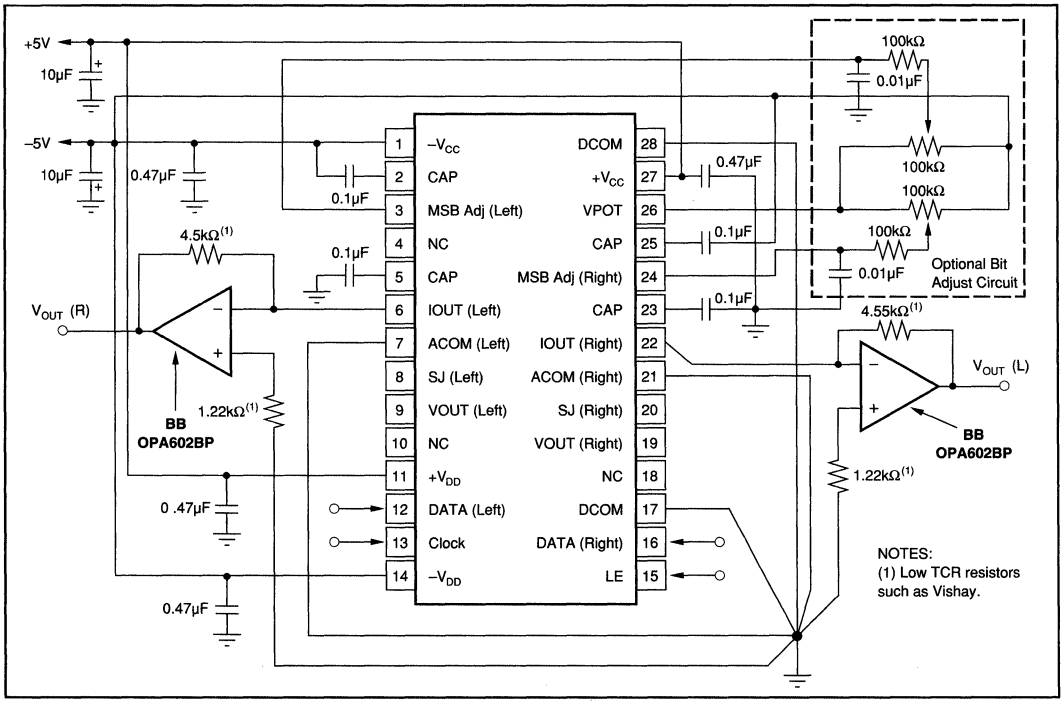

FIGURE 4. Current Output Connection Diagram (DIP Package Diagram.)

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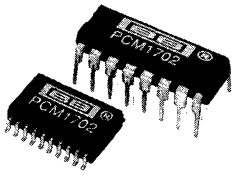


PCM1702P
PCM1702U

BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

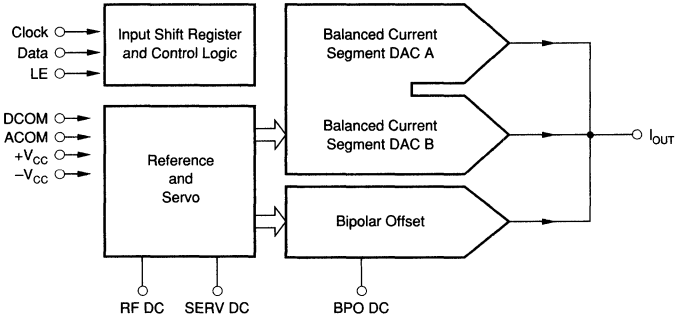
FEATURES

- ULTRA LOW –96dB max THD+N (No External Adjustment Required)
- NEAR-IDEAL LOW LEVEL OPERATION
- GLITCH-FREE OUTPUT
- 120dB SNR TYP (A-Weight Method)
- INDUSTRY STD SERIAL INPUT FORMAT
- FAST (200ns) CURRENT OUTPUT (±1.2mA)
- CAPABLE OF 16X OVERSAMPLING
- COMPLETE WITH REFERENCE
- LOW POWER (150mW typ)

DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

All specifications at 25°C, $\pm V_{CC}$ and $+V_{DD} = \pm 5V$ unless otherwise noted.

PARAMETER	CONDITIONS	PCM1702P/U, -J, -K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale, with A-weight			110		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_{DD}$	V
V_{IL}		0		0.8	V
I_{IH}	$V_{IH} = +V_{DD}$			±10	µA
I_{IL}	$V_{IL} = 0V$			±10	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			12.5	20.0	MHz
TOTAL HARMONIC DISTORTION + N[2]					
P/U V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–92	–88	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–82	–74	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–46	–40	dB
P/U, -J V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–96	–92	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–83	–76	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–48	–42	dB
P/U, -K V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–100	–96	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–84	–80	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–50	–44	dB
ACCURACY					
Level Linearity	At –90dB Signal Level		±0.5		dB
Gain Error			±0.5	±3	%
Bipolar Zero Error[5]			±0.25		%
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±5		ppm of FSR/°C
Warm-up Time			1		minute
IDLE CHANNEL SNR[6]	Bipolar Zero, A-weighted Filter	110	120		dB
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	(±0.003% of FSR, 1.2mA Step)		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
Supply Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.00	+5.25	V
$-V_{CC} = -V_{DD}$		–4.75	–5.00	–5.25	V
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5V$		+5.00	+9.0	mA
Combined Supply Current: $-I_{CC}$	$-V_{CC} = -V_{DD} = -5V$		–25.00	–41.0	mA
Power Dissipation	$\pm V_{CC} = \pm V_{DD} = \pm 5V$		150	250	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$)/$Signal_{RMS}$. (3) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (4) D/A converter output frequency (signal level). (5) Offset error at bipolar zero. (6) Measured using an OPA627 and 5kΩ feedback and an A-weighted filter.

ABSOLUTE MAXIMUM RATINGS (DIP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	500mW
Lead Temperature (soldering, 10s)	260°C

ABSOLUTE MAXIMUM RATINGS (SOP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	300mW
Lead Temperature (soldering, 5s)	260°C

PIN ASSIGNMENTS (DIP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	9	+V_{CC}
2	CLOCK	10	BPO DC
3	+V_{DD}	11	I_{OUT}
4	DCOM	12	ACOM
5	–V_{DD}	13	ACOM
6	LE	14	SERV DC
7	NC	15	REF DC
8	NC	16	–V_{CC}

PIN ASSIGNMENTS (SOP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	11	+V_{CC}
2	CLOCK	12	BPO DC
3	NC	13	NC
4	+V_{DD}	14	I_{OUT}
5	DCOM	15	ACOM
6	–V_{DD}	16	ACOM
7	LE	17	SERV DC
8	NC	18	NC
9	NC	19	RFE DC
10	NC	20	–V_{CC}

PACKAGE INFORMATION

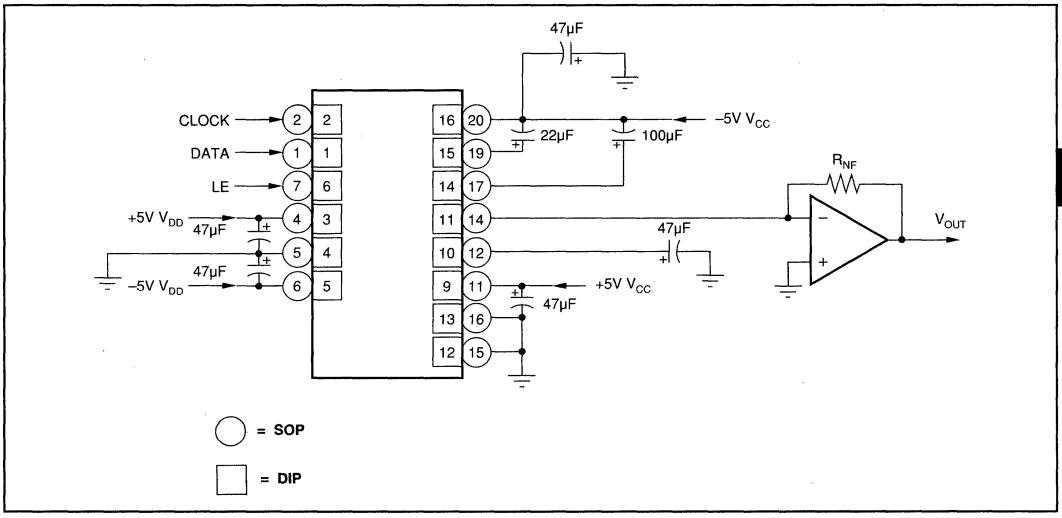
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1702P	16-Pin Plastic DIP	180
PCM1702U	20-Pin Plastic SOP	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

GRADE MARKING (SOP Package)

MODEL	PACKAGE
PCM1702U	Marked PCM1702.
PCM1702U-J	Marked with white dot by pin 10.
PCM1702U-K	Marked with red dot by pin 10.

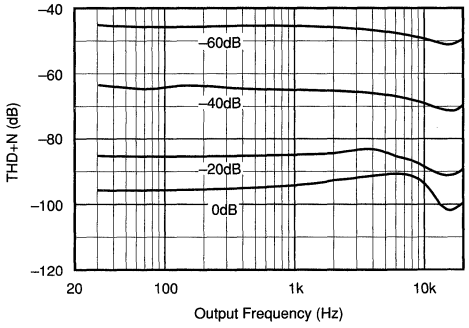
CONNECTION DIAGRAM



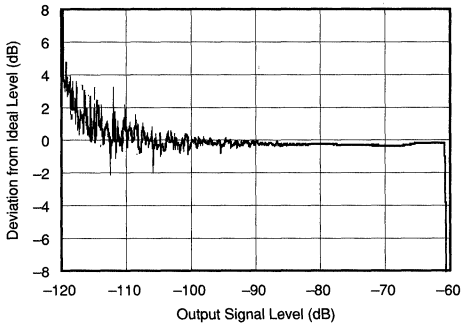
TYPICAL PERFORMANCE CURVES

All specifications at 25°C, $\pm V_A$ and $\pm V_D$ = ±5.0V unless otherwise noted.

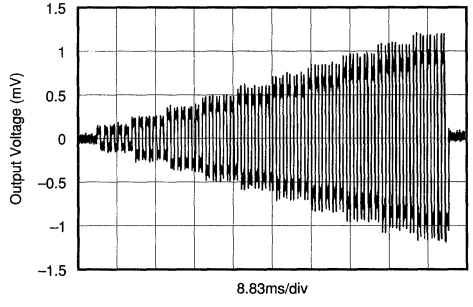
THD+N vs FREQUENCY



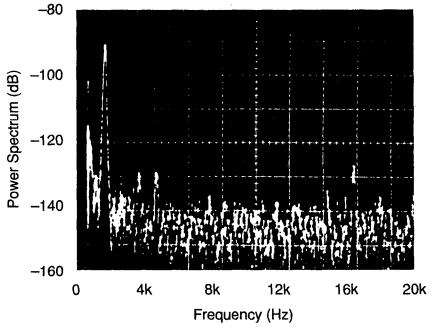
16-BIT LEVEL LINEARITY
(Dithered Fade-to-Noise)



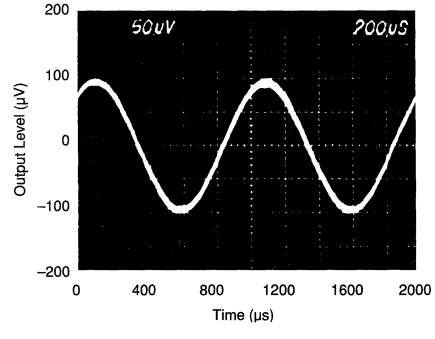
16-BIT MONOTONICITY



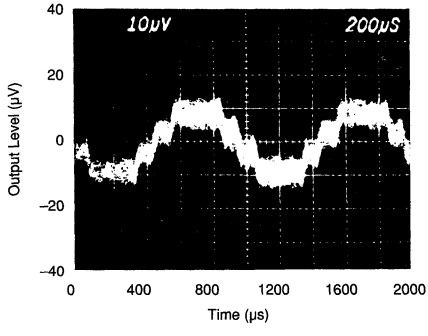
–90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



–90dB SIGNAL
(10Hz to 20kHz Bandwidth)



–110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

ADVANCED SIGN MAGNITUDE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However, even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high over-sampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DAC). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM1702 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference, and a common R-2R ladder for bit current sources by dual balanced current segments to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or advanced sign magnitude approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM1702 is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table 1 shows the conversion made by the internal logic of the PCM1702 from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM1702 in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specifications for the PCM1702 is total harmonic distortion plus noise (THD+N).

Digital data words are read into the PCM1702 at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 1002Hz is realized.

For production testing, the output of the DAC goes to an I to V converter, then through a 40kHz low pass filter, and then to a programmable gain amplifier to provide gain at lower signal output test levels before being fed into an analog-type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

For the audio bandwidth, THD+N of the PCM1702 is essentially flat for all frequencies. The typical performance curve, "THD+N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low level signal performance of the advanced sign magnitude architecture of the PCM1702.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS} + Noise_{RMS}$/ $Signal_{RMS}$ expressed in dB. For the PCM1702, THD+N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD+N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The advanced sign magnitude architecture of the PCM1702, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111+1LSB(1)	111...111
+Full Scale –1LSB	011...110	111...111+1LSB(1)	111...110
Bipolar Zero +2LSB	000...010	111...111+1LSB(1)	000...010
Bipolar Zero +1LSB	000...001	111...111+1LSB(1)	000...001
Bipolar Zero	000...000	111...111+1LSB(1)	000...000
Bipolar Zero –1LSB	111...111	111...111	000...000
Bipolar Zero –2LSB	111...110	111...110	000...000
–Full Scale +LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

NOTE: (1) The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to Sign Magnitude Conversion Chart.

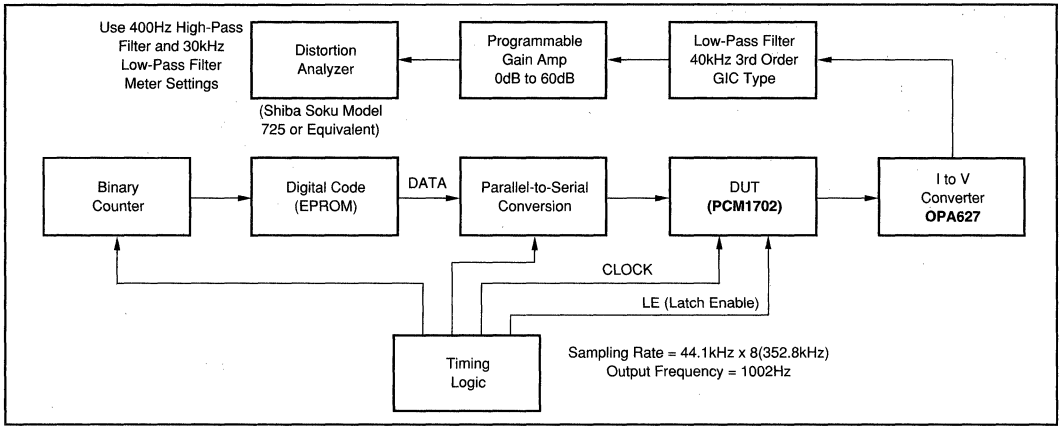


FIGURE 1. Production THD+N Test Setup.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM1702 at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM1702 at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal.

This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM1702 advanced sign magnitude.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased form –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM1702 tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATION

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero, while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM1702 is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique advanced sign magnitude architecture of the PCM1702, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM1702, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bit-stream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM1702, the extremely low THD+N performance is typically indicative of 17-bit integral linearity in the DAC. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, and Temperature Drift

Although the PCM1702 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM1702 accepts TTL compatible logic input levels. The data format of the PCM1702 is binary two's complement (BTC) with the most significant bit (MSB) being first

in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after Latch Enable (Pin6 <PCM1702P>, Pin7 <PCM1702U>, LE) has gone low.

All DAC serial input data (Pin1, DATA) bit transfers are triggered on positive clock (Pin2, CLOCK), edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable. The change in the output of the DAC occurs at a rising edge of the 4th clock of the CLOCK after the falling edge of Latch Enable. Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM1702 is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X over-sampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM1702 is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT
1,048,576LSBs	Full Scale Range	2.40000000mA
1LSB	NA	2.28882054nA
$7FFFF_{HEX}$	+Full Scale	–1.19999771mA
00000_{HEX}	Bipolar Zero –1LSB	0.00000000mA
80000_{HEX}	–Full Scale	+1.20000000mA

TABLE II. Digital Input/Output Relationships.

INSTALLATION

POWER SUPPLIES

Refer to CONNECTION DIAGRAM for proper connection of the PCM1702. The PCM1702 only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in CONNECTION DIAGRAM regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM1702 as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in CONNECTION DIAGRAM, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM1702 as possible to reduce noise pickup from surrounding circuitry.

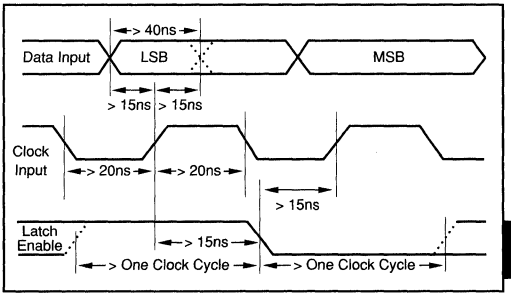
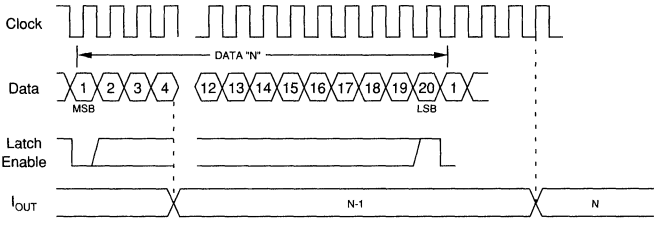


FIGURE 3. Setup and Hold Timing Diagram.



NOTES : (1) If clock is stopped between input of 20-bit data words, "Latch" Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on positive going edge of the 4th clock after negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

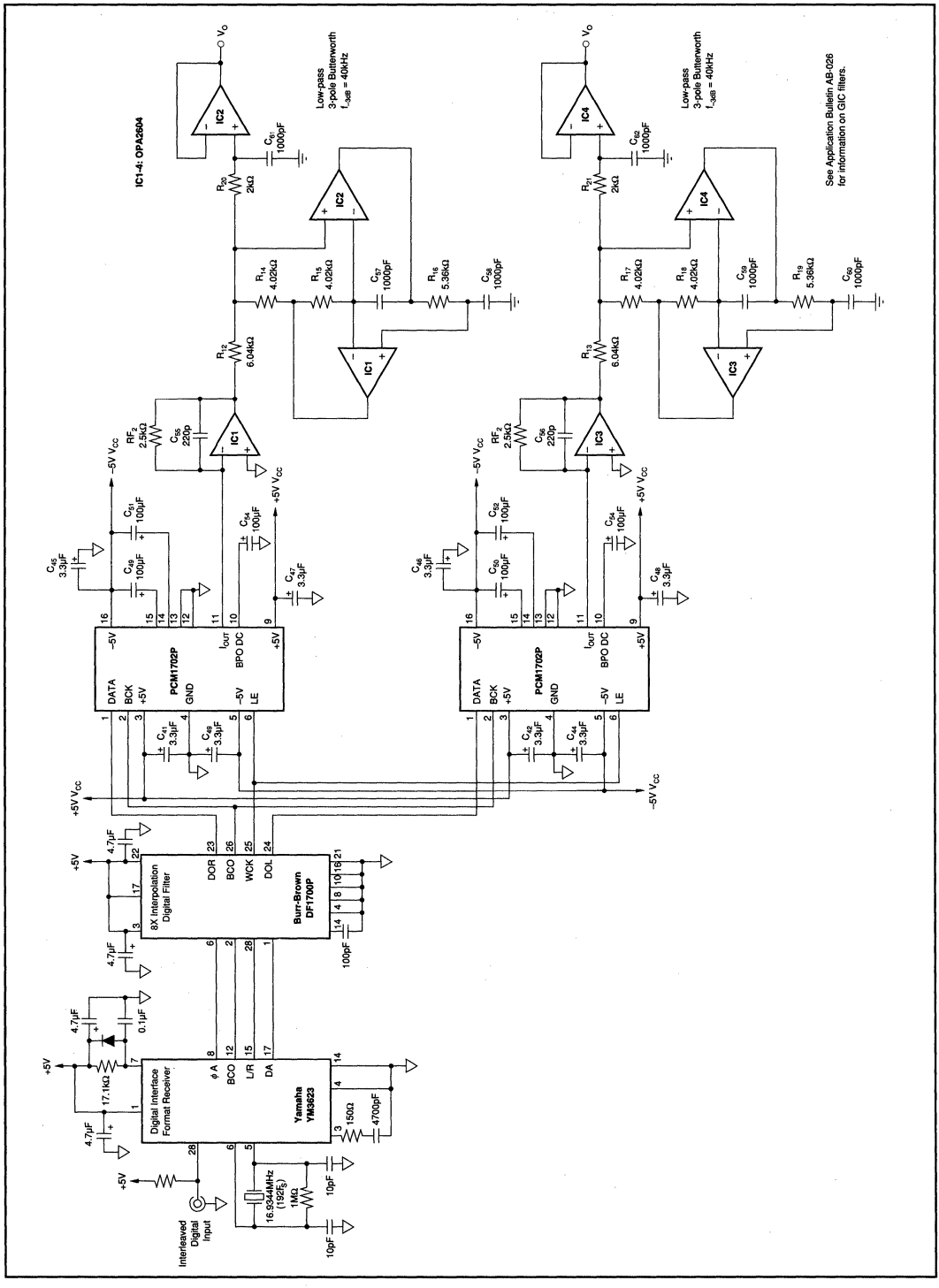


FIGURE 4. Typical Application for Stereo Audio 8X Oversampling System.

BURR-BROWN®

PCM1710U

SpeedPlus™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

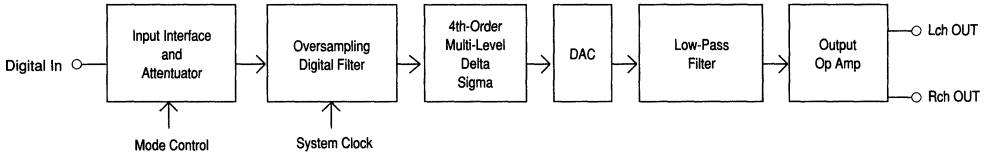
- **COMPLETE STEREO DAC:**
  8X Oversampling Digital Filter
  Multi-Level Delta-Sigma DAC
  Analog Low Pass Filter
  Output Amplifier
- **HIGH PERFORMANCE:**
  –92dB THD+N
  98dB Dynamic Range
  110dB SNR
- **ACCEPTS 16 OR 20 BITS INPUT DATA**
- **SYSTEM CLOCK: 256fs or 384fs**
- **SINGLE +5V POWER SUPPLY**
- **ON-CHIP DIGITAL FILTER:**
  Soft Mute and Attenuator
  Digital De-emphasis
  Double-Speed Dubbing Mode
- **SMALL 28-PIN SOIC PACKAGE**

DESCRIPTION

The PCM1710 is a complete stereo audio digital-to-analog converter, including digital interpolation filter, delta-sigma DAC, and analog voltage output. PCM1710 can accept either 16-bit normal or 20-Bit normal input data (MSB first, right justified), or 16-bit IIS data (32-bits per word, continuous clock).

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, de-emphasis and double-speed dubbing. Performance of the digital feature is excellent, featuring –62dB stop band attenuation and ±0.008dB ripple in the pass band.

PCM1710 is suitable for a wide variety of consumer applications where good performance is required. Its low cost, small size and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive and CD-Karaoke systems.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384/256fs, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1710U MIN	PCM1710U TYP	PCM1710U MAX	UNITS
RESOLUTION		16		20	Bits
DIGITAL INPUT					
Logic Family					
Input Logic Level (except XTI)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (except XTI)				–200	µA
Input Logic Level (XTI)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTI)				±50	µA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current (CLKO)		±10			mA
Data Format	Normal (16/20-bit)/IIS (16-bit) selectable				
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	$384f_S$	12.288	16.934	18.432	MHz
System Clock Frequency	$256f_S$	8.192	11.2894	12.288	MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20.0		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE[1]					
THD+N at F/S (0dB)[2]	f_{IN} = 991kHz		–92	–88	dB
THD+N at –60fdB[2]	f_{IN} = 991kHz		–36	–32	dB
Dynamic Range	EIAJ A-weighted		98		dB
S/N Ratio	EIAJ A-weighted	104	110		dB
Channel Separation		90	94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple	Normal Mode			±0.008	dB
Pass Band Ripple	Double Speed Mode			±0.018	dB
Stop Band Attenuation	Normal Mode	–62			dB
Stop Band Attenuation	Double Speed Mode	–58			dB
Pass Band	Normal Mode			0.4535	fs
Pass Band	Double Speed Mode			0.4535	fs
Stop Band	Normal Mode			0.5465	fs
Stop Band	Double Speed Mode			0.5465	fs
De-emphasis Error	(f_S 32kHz ~ 48kHz)	–0.05		+0.03	dB
ANALOG OUTPUT					
Voltage Range			3.2		Vp-p
Load Impedance		5			kΩ
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current ($+I_{CC}$) + ($+I_{DD}$)			45	70	mA
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) Dynamic performance specs are tested with external 20kHz low pass filter. (2) 30kHz LPF, 400Hz HPF, Average Mode. Shibusoku #725 THD Meter.

PIN ASSIGNMENTS

PIN NAME	NUMBER	FUNCTION
Input Interface Pins		
LRCIN	1	Sample Rate Clock Input. Controls the update rate (fs).
DIN	2	Serial Data Input. MSB first, right justified format contains a frame of 16-bit or 20-bit data.
BCKIN	3	Bit Clock Input. Clocks in the data present on DIN input.
Mode Controls and Clock Signals		
CLKO	4	Buffered Output of Oscillator. Equivalent to fs.
XTI	5	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
XTO	6	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 5) of the crystal oscillator. When using an external clock, leave XTO open.
CKSL	23	System Clock Select. For 384fs, tie CKSL "High". For 256fs, tie CKSL "Low".
MODE	24	Operation Mode Select. For serial mode, tie MODE "High". For parallel mode, tie MODE "Low".
MUTE	25	Mute Control. To disable soft mute, tie MUTE "High". To enable soft mute, tie MUTE "Low".
MD/DM1	26	Mode Control for Data/De-emphasis. See "Mode Control Functions" on page 11.
MC/DM2	27	Mode Control for BCKIN/De-emphasis. See "Mode Control Functions" on page 11.
ML/DSD	28	Mode Control for WDCK/Double speed dubbing. See "Mode Control Functions" on page 11.
Analog Functions		
$V_{OUT}R$	13	Right Channel Analog Output.
$V_{OUT}L$	16	Left Channel Analog Output.
Power Supply Connections		
DGND	7, 22	Digital Ground.
V_{DD}	8, 21	Digital Power Supply (+5V).
$V_{CC}2R$	9	Analog Power Supply (+5V), Right Channel DAC.
AGND2R	10	Analog Ground (DAC), Right Channel.
EXT1R	11	Output Amplifier Common, Right Channel. Bypass to ground with a 10µF capacitor.
EXT2R	12	Output Amplifier Bias, Right Channel. Connect to EXT1R.
AGND	14	Analog Ground.
V_{CC}	15	Analog Power Supply (+5V).
EXT2L	17	Output Amplifier Bias, Left Channel. Connect to EXT1L.
EXT1L	18	Output Amplifier Common, Left Channel. Bypass to ground with a 10µF capacitor.
AGND2L	19	Analog Ground (DAC), Left Channel.
$V_{CC}2L$	20	Analog Power Supply (+5V), Left Channel DAC.

ABSOLUTE MAXIMUM RATINGS

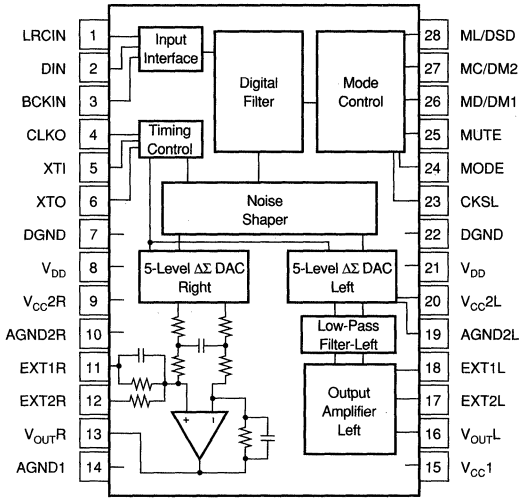
Power Supply Voltages	±6.5VDC
$+V_{CC}$ to V_{DD} Voltage	±0.1V
Input Logic Voltage	–0.3V to V_{DD} +0.3V
Power Dissipation	400mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PACKAGE INFORMATION

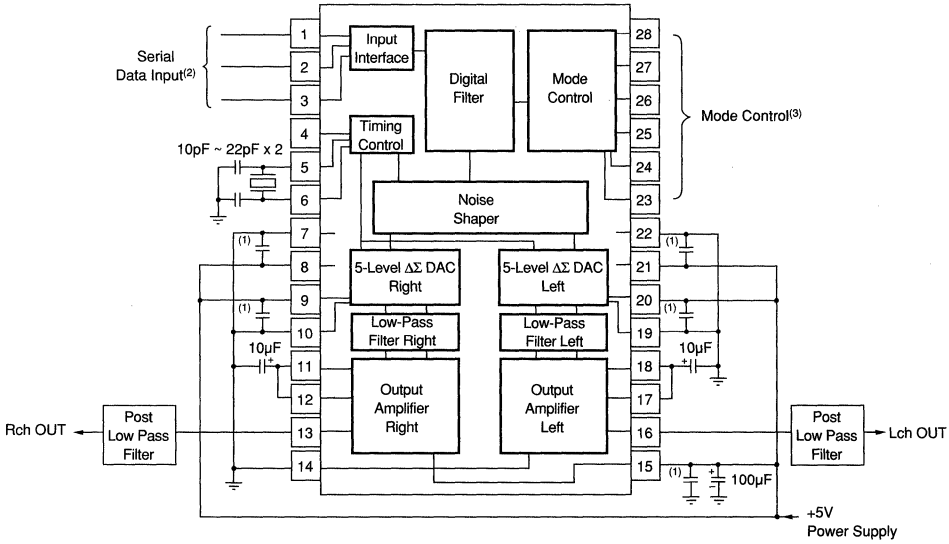
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1710U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION



CONNECTION DIAGRAM



NOTES: (1) Bypass Capacitor :1μF ~ 10μF.
(2) Input pins require pull-up resistors. (3) Mode control pins require pull-up resistors.

DATA INPUT TIMING

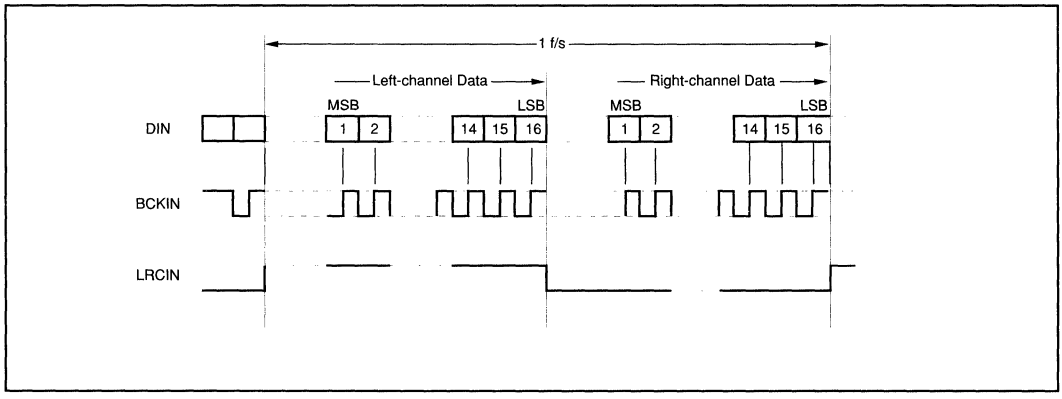


FIGURE 1. Normal Format, 16-Bit (LRCIN H: Lch).

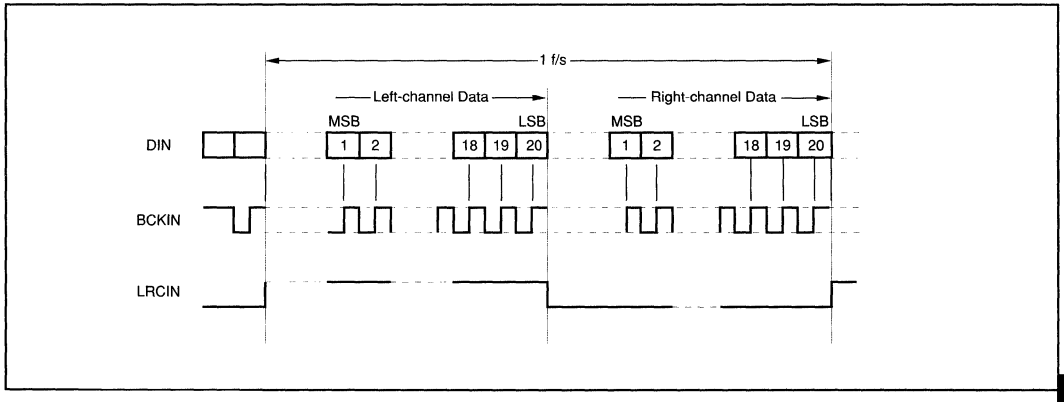


FIGURE 2. Normal Format, 20-Bit (LRCIN H: Lch).

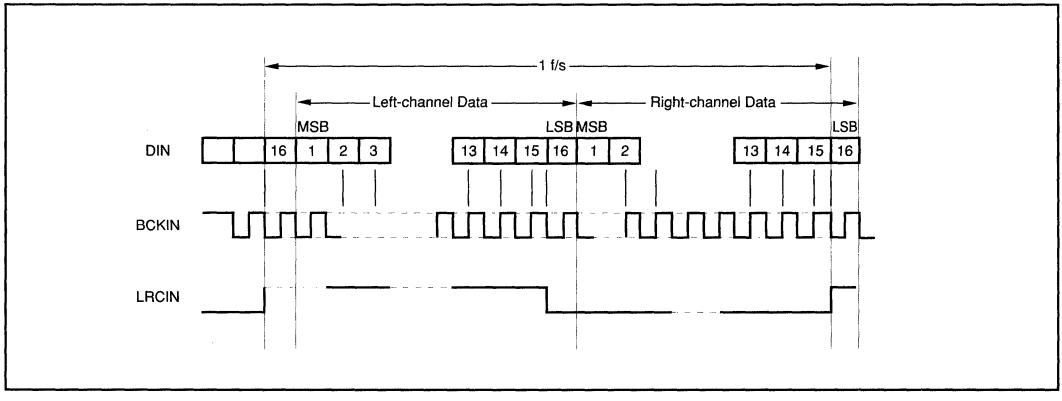


FIGURE 3. IIS Format, (16-Bit, 32 BCKIN Clock Cycles Per fs Interval).

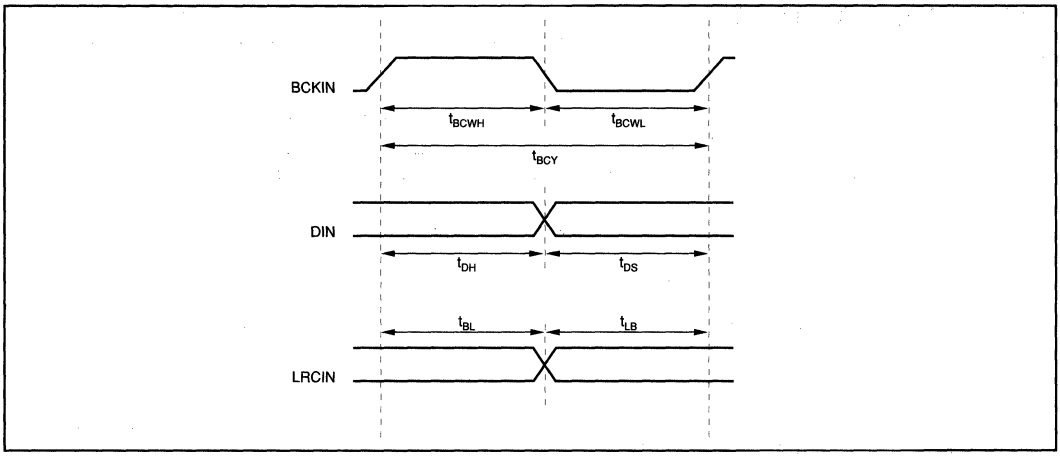


FIGURE 4. Data Input Timing.

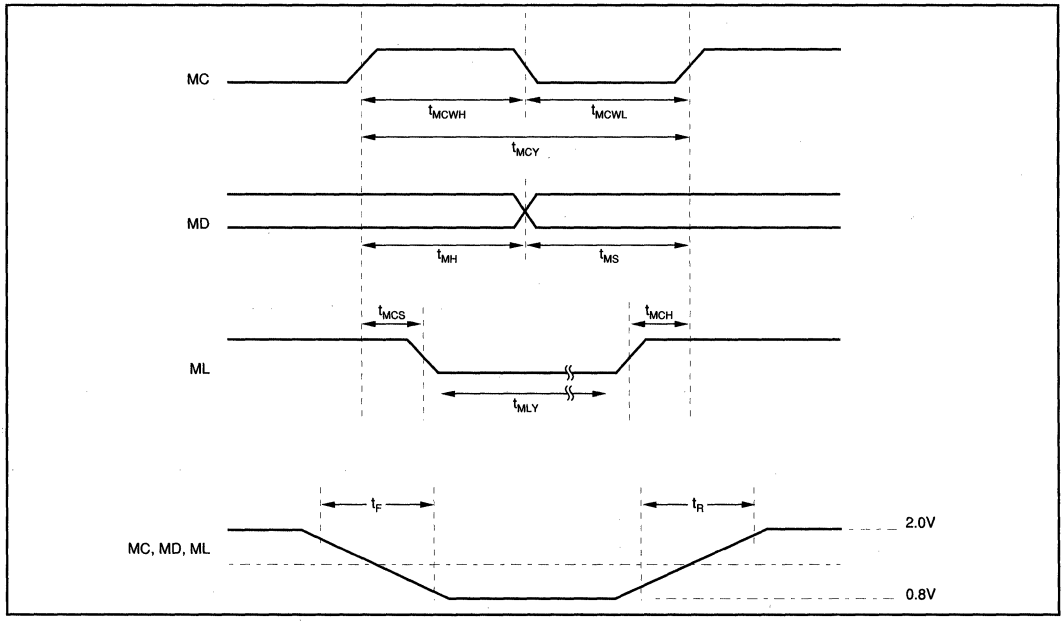


FIGURE 5. Serial Mode Control Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level)	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRC I Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE I. Data Input Timing Specifications (Refer to Figure 4).

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)
MC, MD, ML Rise Time	t_R	15ns (max)
MC, MD, ML Fall Time	t_F	15ns (max)

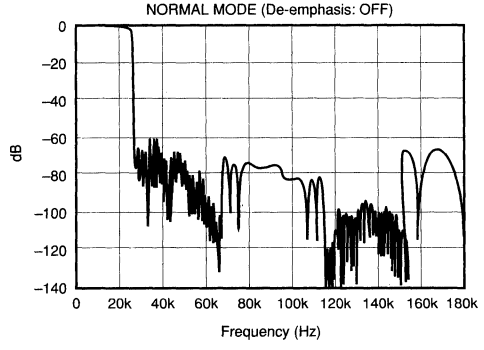
TABLE II. Serial Mode Control Timing Specifications (Refer to Figure 5).

TYPICAL PERFORMANCE CURVES

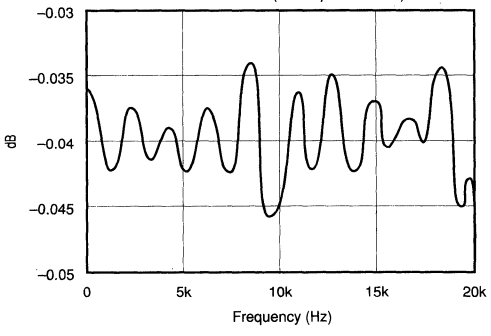
All specifications at +25°C, $+V_{CC}$ = + V_{DD} + 5V, f_S = 44.1kHz, f_{SYS} = 384/256fs, and 16-bit data, unless otherwise noted.

DIGITAL FILTER

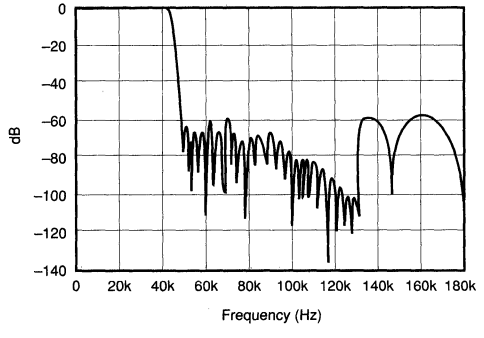
OVERALL FREQUENCY CHARACTERISTIC
NORMAL MODE (De-emphasis: OFF)



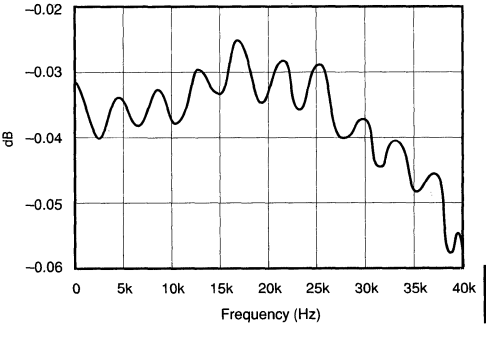
PASSBAND RIPPLE CHARACTERISTIC
NORMAL MODE (De-emphasis: OFF)



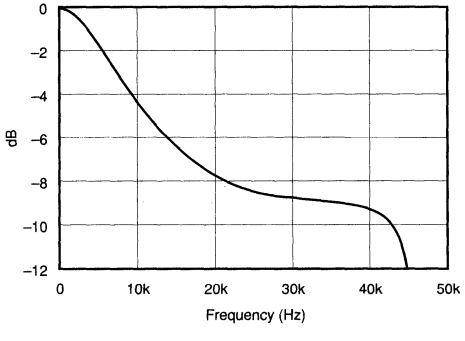
OVERALL FREQUENCY CHARACTERISTIC
DOUBLE-SPEED MODE (De-emphasis: OFF)



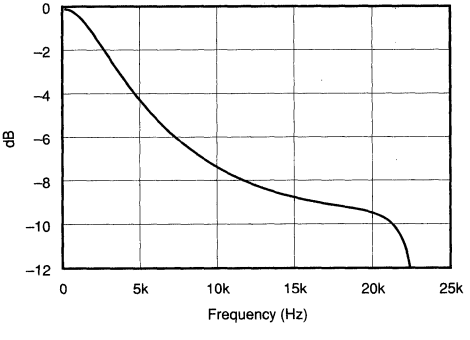
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
DOUBLE-SPEED MODE (De-emphasis: OFF)



DE-EMPHASIS CHARACTERISTIC
DOUBLE-SPEED MODE



DE-EMPHASIS CHARACTERISTIC, NORMAL MODE

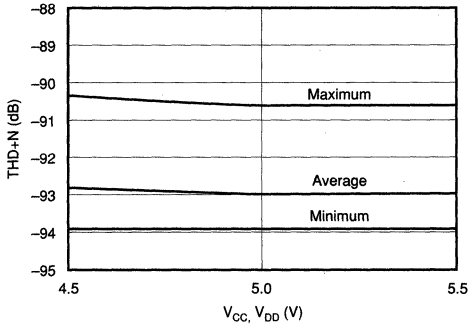


TYPICAL PERFORMANCE CURVES (CONT)

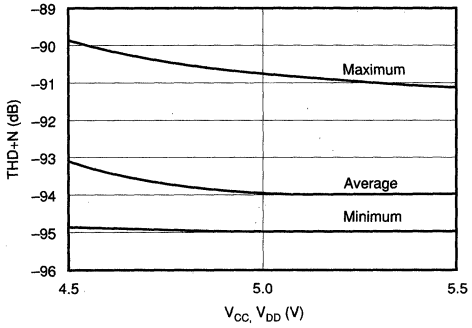
At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 402Ω, unless otherwise noted. Based on 200 piece sample from 3 diffusion runs.

DYNAMIC PERFORMANCE

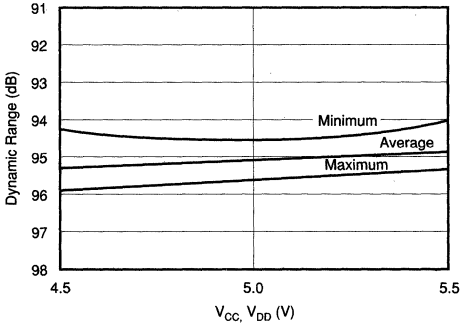
256fs
THD+N vs V_{CC}, V_{DD}
FULL-SCALE INPUT



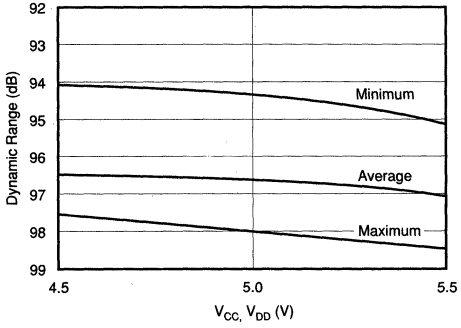
384fs
THD+N vs V_{CC}, V_{DD}
FULL SCALE INPUT



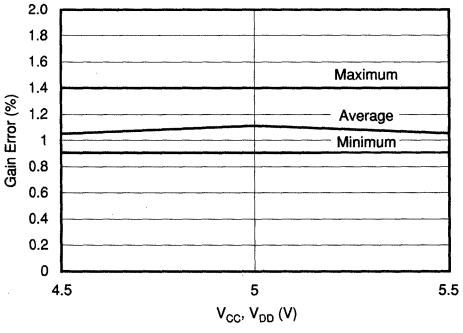
256fs
DYNAMIC RANGE vs V_{CC}, V_{DD}



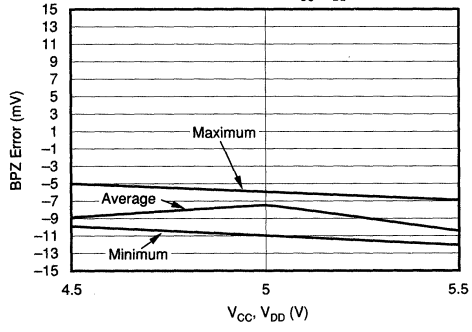
384fs
DYNAMIC RANGE vs V_{CC}, V_{DD}



384fs
GAIN ERROR vs V_{CC}, V_{DD}



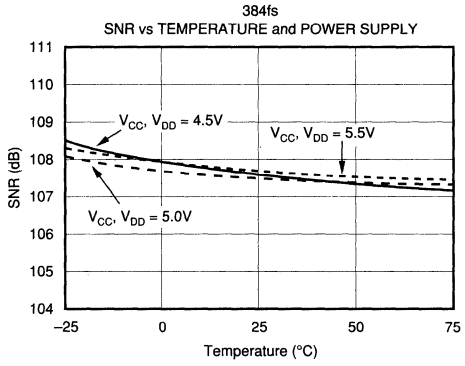
384fs
BPZ ERROR vs V_{CC}, V_{DD}

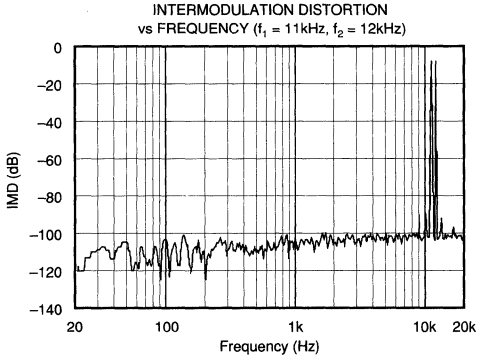


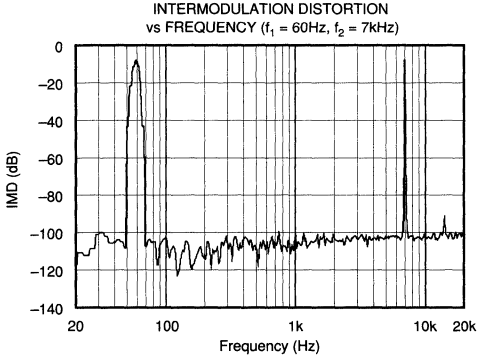
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 402Ω, unless otherwise noted. Based on 200 piece sample from 3 diffusion runs.

DYNAMIC PERFORMANCE







CAUTION: Minimum and maximum values on typical performance curves are not meant to imply a guarantee. Curves should be used for reference only. Refer to specification for guaranteed performances.

FUNCTIONAL DESCRIPTION

PCM1710 has several built-in functions including digital attenuation, digital de-emphasis and soft mute. These functions are software controlled. PCM1710 can be operated in two different modes, **Serial** or **Parallel**. Serial Mode is a three-wire interface using pin 26 (MD), pin 27 (MC), and pin 28 (ML). Data on these pins are used to control de-emphasis mode, mute, double-speed dubbing, input resolution and input format. PCM1710 can also be operated in parallel mode, where static control signals are used on pin 26 (DM1), pin 27 (DM2), and pin 28 (DSD). Operation of both of these modes are covered in detail in the next sections.

CAUTION: Mode control signals operate on level triggered logic. The minimum timing conditions detailed in Figures 5 and 6 MUST be observed.

MODE CONTROL: SERIAL/PARALLEL SELECTION

MODE = H	Serial Mode
MODE = L	Parallel Mode

TABLE III. Serial and Parallel Mode are Selectable by MODE Pin (Pin 24).

MODE CONTROL: SELECTABLE FUNCTIONS

FUNCTION	SERIAL MODE (MODE = H)	PARALLEL MODE (MODE = L)
Input Data Format Selection	0	X(Normal Mode Fixed)
Input Data Bit Selection	0	X(16-bit Fixed)
Input LRCI Polarity Selection	0	X
De-emphasis Control	0	0
Mute	0	0
Attenuation	0	X
Double Speed Dubbing	0	0
NOTE: 0: Selectable, X: Not Selectable.		

TABLE IV. Selectable Functions in Serial Mode and Parallel Mode.

Table IV indicates which functions are selectable within the user's chosen mode. All of the functions shown are selectable within the serial mode, but only de-emphasis control, mute and double-speed dubbing may be selected when using PCM1710 in the parallel mode.

PARALLEL-MODE: DE-EMPHASIS CONTROL (PIN 24 [MODE] = L)

DM1 (Pin 26)	DM2 (Pin 27)	De-emphasis
L	L	OFF
H	L	32kHz
L	H	48kHz
H	H	44.1kHz

TABLE V. De-emphasis (Pins 26 and 27).

In the parallel mode, de-emphasis conditions are controlled by the logic levels on pin 26 (DM1) and pin 27 (DM2). For PCM1710, de-emphasis can operate at 32kHz, 44.1kHz, 48kHz, or disabled.

PARALLEL-MODE: DOUBLE-SPEED DUBBING CONTROL (PIN 24 [MODE] = L)

DSD = H	Normal Mode
DSD = L	Double-Speed Dubbing Mode
NOTE: When the Double-Speed Dubbing Mode is selected, the System Clock must be 384fs (CKSL: Pin 23 = H).	

TABLE VI. DSD (Pin 28).

In the parallel mode, double-speed dubbing can be enabled by holding pin 28 (DSD) at a logic "low".

CAUTION: Double-speed dubbing cannot operate if the system clock is set at 256fs.

SERIAL MODE CONTROL

In order to use all of PCM1710's functionality, the **serial mode control** should be used. PCM1710 must be addressed three separate times to set all of the various registers and flags that control these functions.

Table VII together with Figure 6 details the control of the PCM1710 in the serial mode. Internal latches are used to hold this serial data until the PCM1710 is enabled to use the data. The serial mode is used by applying clocked data to the following pins:

NAME	PIN	FUNCTION
MC	27	Clock for Strobing in Data
ML	28	Latches Data into the Registers
MD	26	8-bit Data Word Defining Operation

	B0	B1	B2	BIT NO.	MODE FLAG	FUNCTION MODE SELECTION MODE	BIT VALUE	SELECTED FUNCTION	MODE BY DEFAULT
Mode 1	H	L	L	B3	DEEM2	Sampling Frequency for De-emphasis		DEEM2: 0 / 1; DEEM1: 0 → 48kHz; 1 → 32kHz / 44.1kHz	
				B4	DEEM1				
				B5	IIR	De-emphasis	0	De-emphasis OFF	OFF
							1	De-emphasis ON	
				B6	MUTE	Mute	0	Mute OFF	OFF
							1	Mute ON	
				B7	DSD	Double-Speed	0	Double-speed OFF	OFF
							1	Double-speed ON	
Mode 2	H	L	H	B3		Not Assigned			
				B4	TST	Test Mode	0	Infinite Zero Detection OFF	ON
							1	Infinite Zero Detection ON	
				B5	IW	Input Resolution	0	16-Bit	16-Bit
							1	20-Bit	
				B6	LRPL	Polarity for LRCI	0	Lch:high/Rch:low	Lch:high Rch:low
							1	Lch:low/Rch:high	
				B7	IIS	Input Format	0	Normal	Normal
							1	IIS	

TABLE VII. Serial-Mode Control Input Format (Pin 24 [MODE] = H)—Refer to Figure 6 for Timing Diagram.

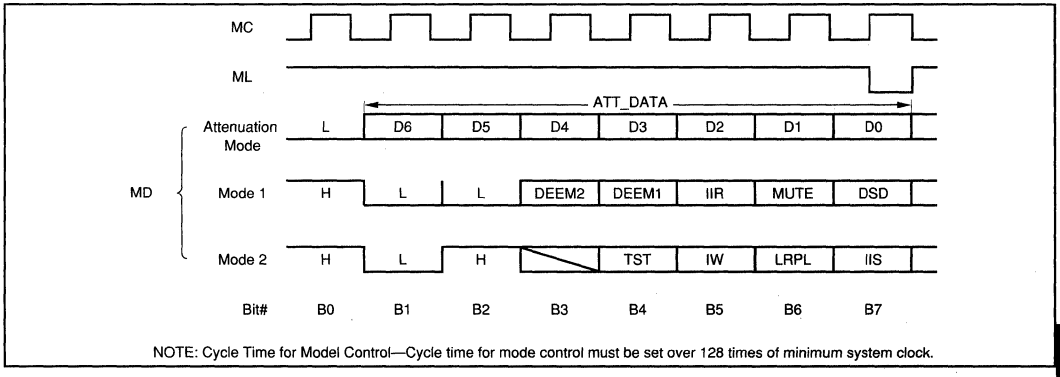


FIGURE 6. Mode Control Input Format, Serial Mode.

DIGITAL ATTENUATION

One of the functions which can be implemented through use of the serial mode control is attenuation. This function allows the user to control the level of the output, independent of the of the input level set by the actual input data supplied to the DAC.

Referring to Figure 6, when the first data bit (B0) on MD (pin 26) is low, the attenuation function is enabled. The next seven bits (B1 - B6) define a binary value, ATT_DATA, that indicates the desired level of attenuation. The attenuation level is given by:

$$\text{Level} = 20\log_{10}(1 - \text{ATT\_DATA}/127)\ \text{dB}$$

When all 7 bits of the ATT_DATA word are high (ATT_DATA = 127), attenuation is infinite and the output of PCM1710 will be zero.

MODE 1 CONTROLS

This mode can be enabled with the sequence of 1, 0, 0 as the first three bits on MD (pin 26). This mode allows for the following functions:

De-emphasis	On/Off
De-emphasis Frequency	32kHz, 44.1kHz, 48kHz
Soft Mute	On/Off
Double-Speed Dubbing	On/Off

DIGITAL DE-EMPHASIS

PCM1710 allows three different sampling rates for digital de-emphasis. B3 and B4 are used for binary control of the de-emphasis frequency:

B3	B4	Frequency
0	0	OFF
0	1	48kHz
1	0	32kHz
1	1	44.1kHz

Once the reset has been established on pin 27 (MC), the de-emphasis frequency defaults to 44.1kHz. B5 is a master control for de-emphasis. A high level on B5 enables de-emphasis (frequency controlled by B3 and B4), and a low level on B5 disables de-emphasis.

SOFT MUTE

Soft mute is enabled when B6 is high. The soft mute occurs gradually, unlike the forced infinite zero detection. When the mute data bit is high, complete muting will occur in 127/fs seconds. For f_S = 44.1kHz, complete mute will occur in 2.88ms.

DOUBLE-SPEED DUBBING

Double-speed dubbing is used when the application allows for the CD to be copied at twice the normal playback rate. Double-speed dubbing is enabled when B7 is high. This mode can only operate when the system clock is set at 384fs. Double-speed dubbing can only occur when the sample rate is 44.1kHz. Since f_S is set at 44.1kHz, the system clock in double-speed mode is at 192fs.

MODE 2 CONTROLS

Mode 2 is enabled when B0 is high, B1 is low, and B2 is high. This mode controls infinite zero detection, input resolution, LRCI polarity and input format.

INFINITE ZERO DETECTION

B4 is used to enable or disable infinite zero detection. PCM1710 monitors both data input (DIN) and bit clock (BCKIN). When the data input is continuously zero for 65,536 cycles of the bit clock, infinite zero detection occurs, which forces the output of the PCM1710 to one-half of V_{CC} (typically 2.5V). Once this happens, only the output amplifier is connected. This is done to avoid having the noise shaped output spectrum of the DAC appear at the output of the PCM1710. This function is especially useful for CD applications when the player is between tracks. An inherent attribute of all delta-sigma architectures is the presence of quantization noise when the input is constant (all 1s or 0s). When the zero detect circuit disconnects the DAC from the output amplifier, a very low level "click" noise may be audible. The click noise occurs at approximately –76dB, and in many cases is inaudible.

INPUT RESOLUTION

PCM1710 is capable of accepting either 16-bit or 20-bit input data. Specifications for PCM1710 are tested and guaranteed using 16-bit data. When 20 bits are used, dynamic performance is improved by approximately 2dB. Refer to "Typical Performance Curves" for a comparison of 16-bit and 20-bit data. A low on B5 places PCM1710 in 16-bit mode, and a high on B5 sets PCM1710 to 20-bit mode.

SAMPLE RATE CLOCK POLARITY

B6 controls the polarity of the sample rate clock (LRCIN) polarity. When B6 is low, data will be accepted on the left channel when LRCIN is high, and on the right channel when LRCIN is low. When B6 is high, data will be accepted on the right channel when LRCIN is high, and on the left channel when LRCIN is low.

INPUT FORMAT

Normal input mode for PCM1710 is MSB first, right justified. PCM1710 may also be operated with IIS (32 continuous clock cycles per word) input format. When B7 is low, the input format is "normal". When B7 is high, the input format is "IIS". However, PCM1710 can only accept IIS input format when it is in 16-bit mode. 20-bit data must be entered in normal mode.

DEFAULT MODE

At initial power-on, default settings for PCM1710 are 44.1kHz f_S, de-emphasis off, mute off, double-speed off, infinite zero detect on, 16-bit input LRCIN left channel high, and normal input mode.

SYSTEM CLOCK

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY	
32kHz	256fs	8.1920MHz
32kHz	384fs	12.2880MHz
44.1kHz	256fs	11.2896MHz
44.1kHz	384fs	16.9344MHz
48kHz	256fs	12.2880MHz
48kHz	384fs	18.4320MHz

TABLE VIII. Relationship of fs and System Clock.

NORMAL/DOUBLE-SPEED DUBBING

For most CD playback applications operating at 384fs, the system clock frequency must be 16.9344MHz, in both the normal mode and double-speed dubbing mode. Table VIII illustrates the relationship between fs and output clock frequency in both modes.

PARAMETER	ML/DSD (PIN 28)	
	H (Normal)	L (Double Speed)
XTI Input Clock Frequency	384fs	192fs
XTI Frequency	16.9344MHz (f_S = 44.1kHz)	16.9344MHz (f_S = 88.2kHz)
CLKO Output Clock Frequency	384fs	192fs

TABLE IX. Relationship Between Normal/Double Speed and fs.

EXTERNAL SYSTEM CLOCK

Figure 7 is a diagram showing the internal clock in conjunction with an external crystal oscillator.

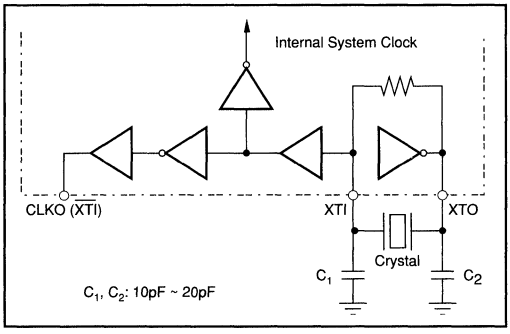


FIGURE 7. External Crystal Oscillator.

Figure 8 is a diagram showing the internal clock with an external clock source, instead of an oscillator. An external system clock (input to XTI) must meet the following conditions:

HIGH LEVEL	V_{IH} > 0.64V_{DD}	T_H > 10ns
LOW LEVEL	V_{IH} > 0.28V_{DD}	T_L > 10ns

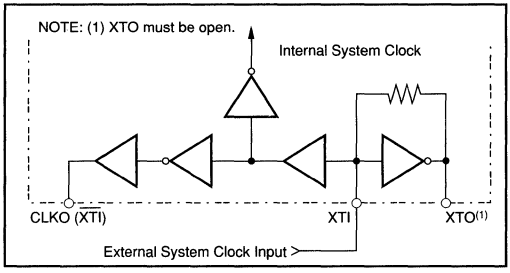


FIGURE 8. External System Clock.

POWER SUPPLY CONNECTIONS

PCM1710 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 9.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 19 for optimal values of bypass capacitors. For applications which require very high performance at low levels (such as keyboards, synthesizers, etc.) it may be beneficial to provide additional bypassing on pin 15 (V_{CC1}) with a low ESR 100µF capacitor. This will eliminate stray tones which may be above the noise floor.

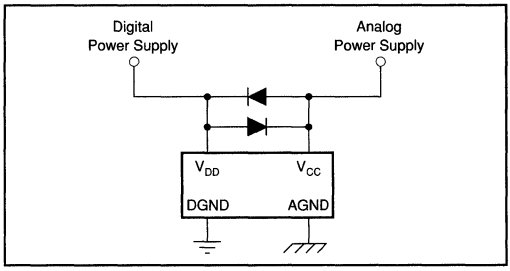


FIGURE 9. Latch-up Prevention Circuit.

THEORY OF OPERATION

PCM1710 is an oversampling delta-sigma D/A converter, consisting of an input interface/attenuator, a 4th-order multi-level delta-sigma modulator, a low pass filter and an output amplifier (see Figure 10).

MODULATOR

The delta-sigma section of the PCM1710 is based on a 5-level amplitude quantizer and a 4th-order filter. This converts oversampled 16-or 20-bit input data to 5-level delta-sigma format. A block diagram of the 5-level modulator is shown in Figure 11.

This 5-level delta-sigma modulator has the advantage of improved stability and jitter sensitivity over the typical one bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X oversampling digital filter is 48fs at a system clock of 384fs and 32fs at a system clock of 256fs.

A block diagram of the 4th-order filter section Hf (z) in the delta-sigma modulator is shown in Figure 12.

In general, high order one-bit delta-sigma modulators have disadvantages due to loop instability (multiple integration stages). The five level delta-sigma modulator of the PCM1710 uses phase compensation techniques to obtain stable operation. In Figure 12, the coefficients B1 to B4 give the basic form of the filter, and A2 to A4 are used for phase compensation of the feedback loop.

The theoretical quantization noise performance of five level delta-sigma modulator is shown in Figure 13 and 14. In the audio band, the quantization noise floor level of the PCM1710 is less than 130dB (at a system clock of 384fs).

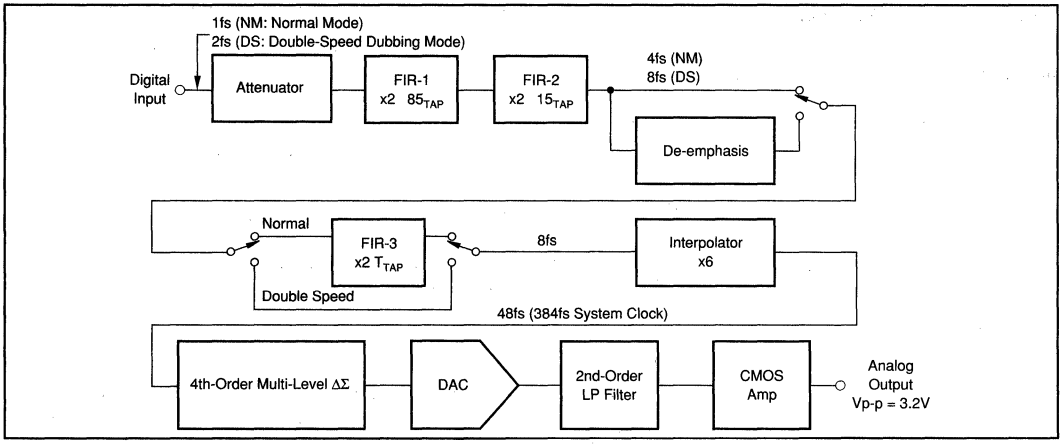


FIGURE 10. PCM1710 Block Diagram.

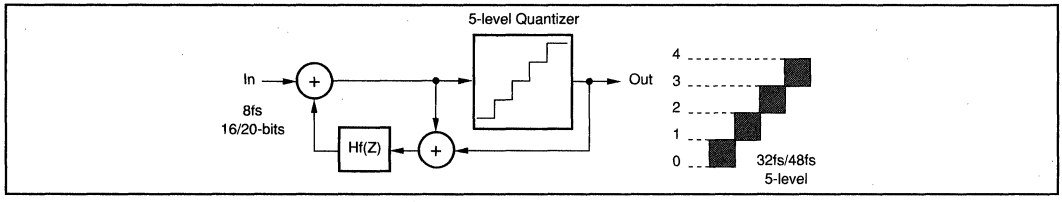


FIGURE 11. Block Diagram of Multi-level ΔΣ Modulator.

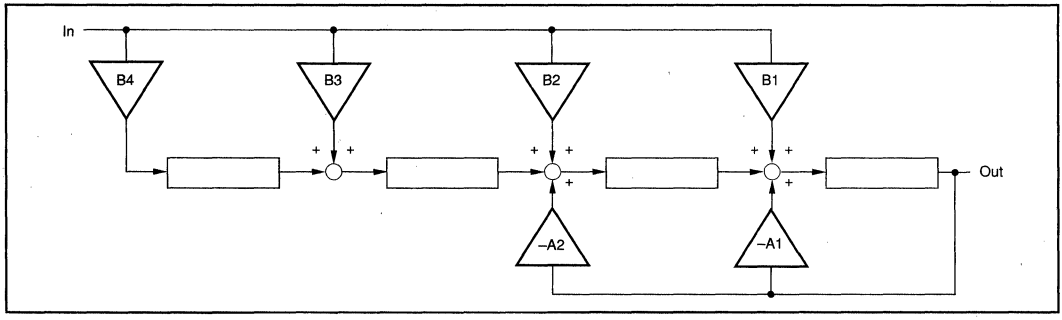


FIGURE 12. Block Diagram of 4th-order Filter Section (H_f (z)).

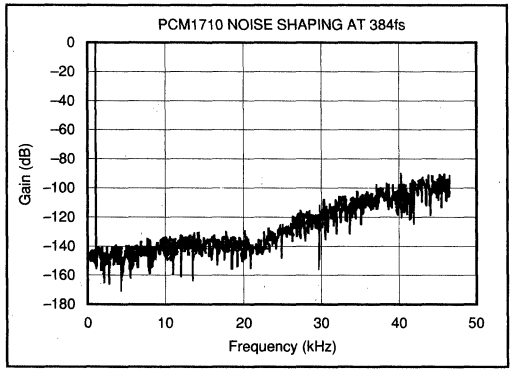


FIGURE 13. Theoretical Modulator Performance at 384fs.

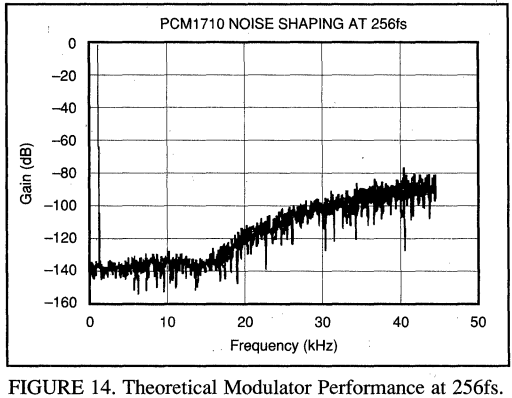


FIGURE 14. Theoretical Modulator Performance at 256fs.

APPLICATION CONSIDERATIONS

16-BIT vs 20-BIT OPERATION

In the serial mode, PCM1710 can be configured to accept either 16-bit or 20-bit data. The specifications listed in this data sheet are the 16-bit data. Some improvements in dynamic performance can be realized by using 20-bit data.

Internally, the PCM1710's digital filter uses only 20-bit data. If the input data is 16-bit, the filter adds four zeros to complete the 20-bit input word. Typical performance differences between 16-bit and 20-bit data are shown in Tables X and XI.

DATA	256fs	384fs
16-bit	–91dB	–93dB
20-bit	–94dB	–96dB

TABLE X. THD+N Performance at Full Scale.

DATA	256fs	384fs
16-bit	94dB	96dB
20-bit	96dB	98dB

TABLE XI. Dynamic Range.

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1710:

$$T_D = 22.625 \times 1/fs$$

For f_S = 44.1kHz, T_D = 22.625/44.1kHz = 513.04µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

INTERNAL RESET

If the sample rate clock (LRCIN) is stopped during operation, the infinite zero detect circuit will cause the output to go to $V_{CC}/2$ after 65,536 cycles of the bit clock (BCKIN). Once a new system clock has been applied, there will be a delay until output data is correlated to the input. This is due to the digital delay of the filter.

When power is first applied to PCM1710, an automatic reset function occurs after 64 cycles of LRCIN.

CHANGING SAMPLING RATE

For normal operation, LRCIN and XTI should be synchronized at either 256fs or 384fs. When the sampling rate is changed during operation, output data is invalid during the delay period (T_D) and for two subsequent cycles of LRCIN. After two cycles of LRCIN, the output is a valid representation of the input data.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1710 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 15. The higher frequency rolloff of the filter is shown in Figure 16. If the user's application has the PCM1710 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 17. For some applications, a passive RC filter or 2nd-order filter may be adequate.

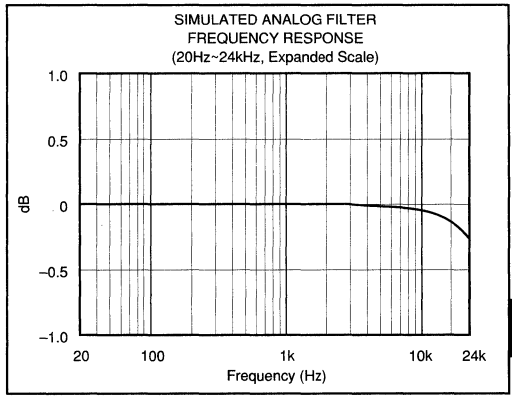


FIGURE 15. Low Pass Filter Frequency Response.

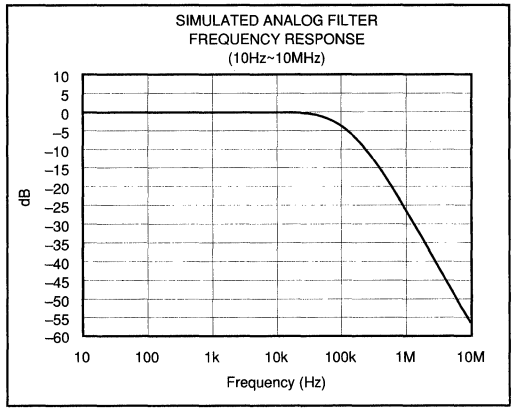


FIGURE 16. Low Pass Filter Frequency Response.

TEST CONDITIONS

Figure 18 illustrates the actual test conditions applied to PCM1710 in production. The 11th-order filter is necessary in the production environment for the removal of noise, resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the third-order filter shown in Figure 17 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –92dB when the external 20kHz second-order filter is used.

EVALUATION FIXTURES

Two different evaluation fixtures are available for PCM1710.

DEM-PCM1710

This evaluation fixture is primarily intended for quick evaluation of the PCM1710's performance. DEM-PCM1710 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1710 does not contain a receiver chip or an external low pass filter. DEM-PCM1710 requires a single +5V power supply.

DEM-DAI1710

This fixture is more complete than DEM-PCM1710; it includes a Digital Audio Interface (DAI) receiver chip for easy use and to provide a low-jitter 256fs system clock to the PCM1710. Also included are dual second-order low pass filters using Burr-Brown's OPA2604 dual FET-input op amp. The output of the DEM-DAI1710 is 2Vrms, using standard BNC-type connectors.

All of the functions of PCM1710 can be evaluated by using the DEM-DAI1710 jumper selections. DEM-DAI1710 requires +5V and ±5V to ±15V power supplies. The schematic diagram for DEM-DAI1710 is shown in Figure 19. For more detailed information on the evaluation fixtures, contact your local Burr-Brown representative.

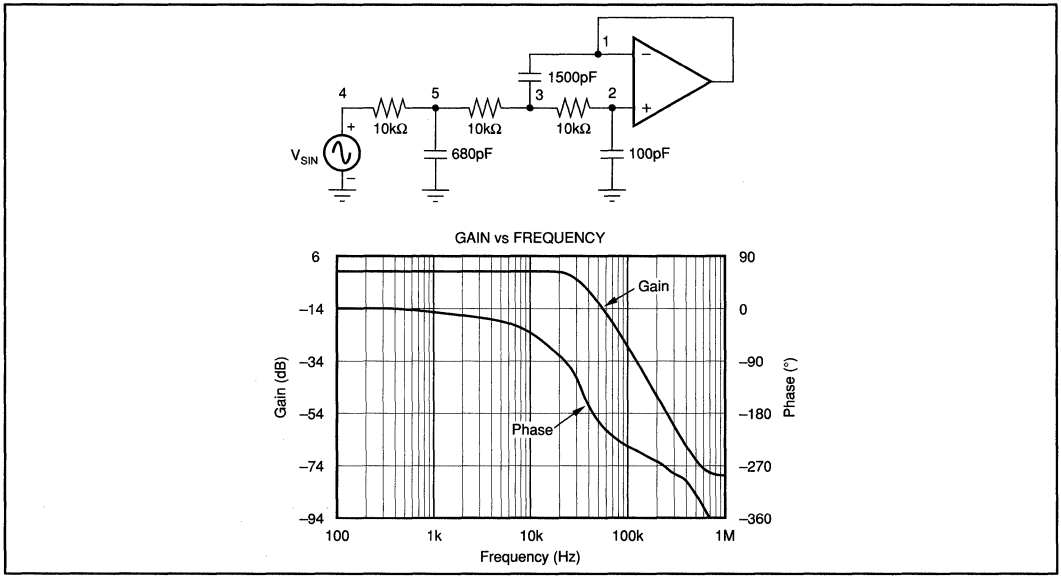


FIGURE 17. 3rd-Order LPF.

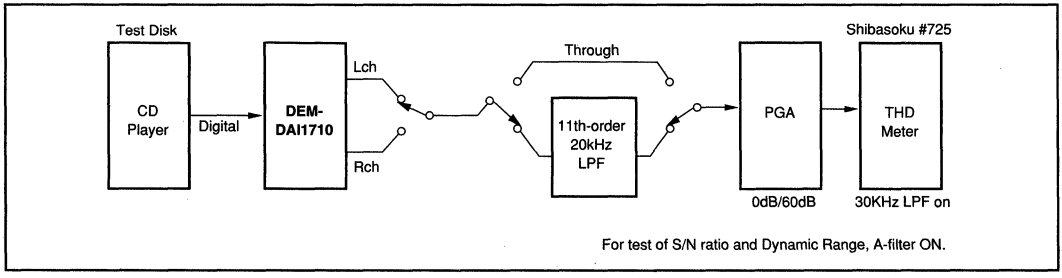


FIGURE 18. Test Block Diagram.

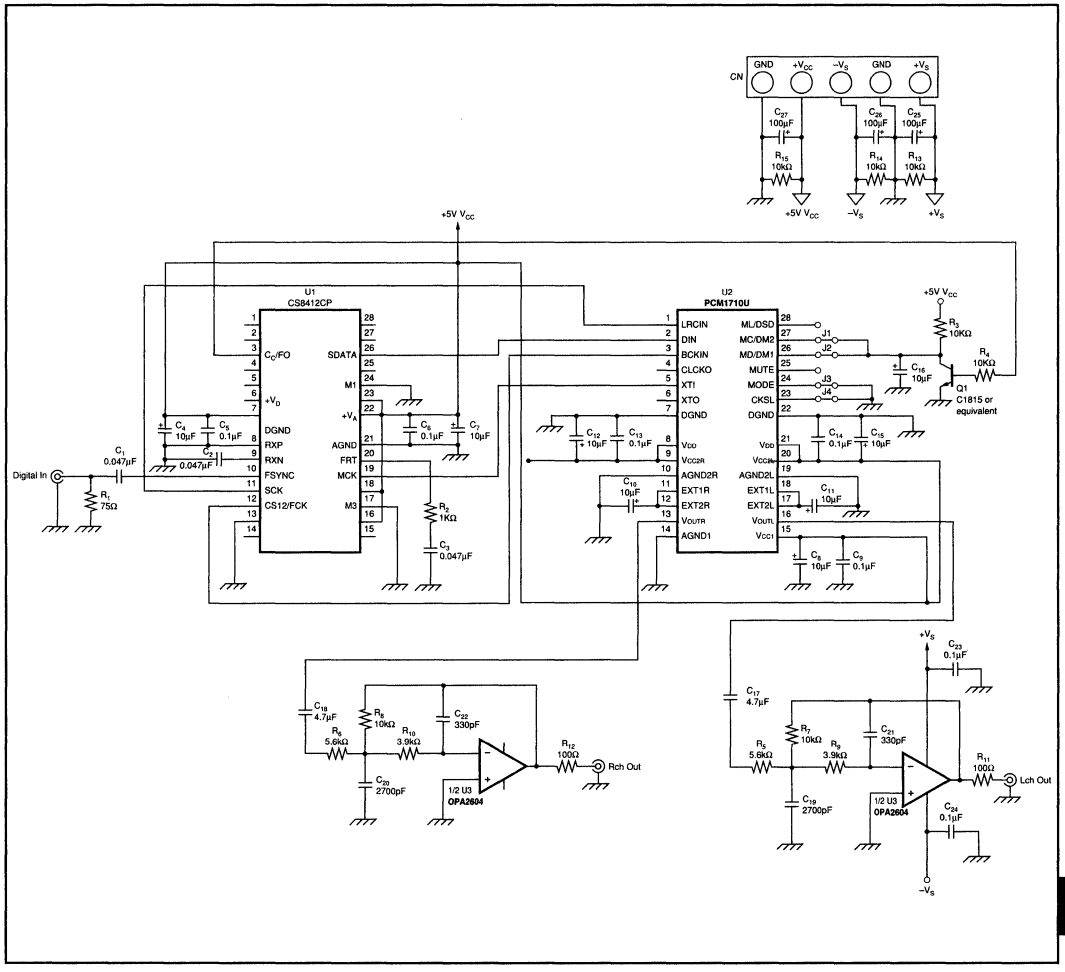


FIGURE 19. DEM-DAI1710 Schematic Circuit Diagram.

BURR-BROWN®

PCM1712U

SpeedPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

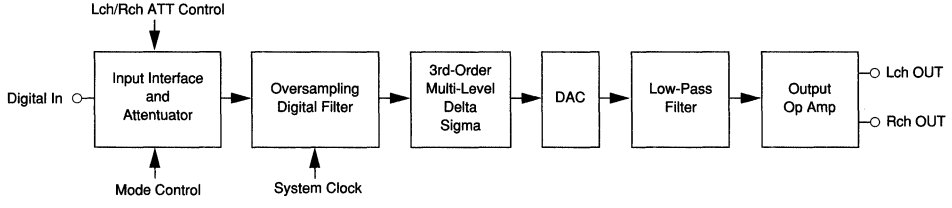
- **16-BIT RESOLUTION**
- **COMPLETE STEREO DAC:**
  8X Oversampling Digital Filter
  Multi-Level Delta-Sigma DAC
  Analog Low Pass Filter
  Output Amplifier
- **HIGH PERFORMANCE:**
  –87dB THD + N
  94dB Dynamic Range
  98dB SNR
- **SYSTEM CLOCK: 384fs**
- **SINGLE +5V POWER SUPPLY**
- **ON-CHIP DIGITAL FILTER:**
  Soft Mute and Attenuation
  Digital De-emphasis
  Double Speed Dubbing Mode
- **SMALL 28-PIN SOIC PACKAGE**

DESCRIPTION

The PCM1712 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1712 accepts 16-bit normal input data (MSB first, right justified), or 16-bit IIS data (32-bits per word, continuous clock).

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, de-emphasis and double-speed dubbing.

PCM1712 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive and CD-Karaoke systems. PCM1712 has the same pinout functions as PCM1710.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 16-bit data, SYSCLK = 384fs, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1712U MIN	PCM1712U TYP	PCM1712U MAX	UNITS
RESOLUTION			16		Bits
DIGITAL INPUT/OUTPUT					
Logic Family					
Input Logic Level (pins 1 to 3)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (pins 1 to 3)					
I_I				–200	µA
Input Logic Level (pins 24 to 28)					
V_{IH}		3.5			VDC
V_{IL}				1.5	VDC
Input Logic Level (pins 24 to 28)					
I_I				–200	µA
Input Logic Level (XTI)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTI)					
I_I				–120	µA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current					
I_O		±10			mA
Data Format		Normal/IIS (see Timing) SELECTABLE			
Data Bit		16-Bit/MSB First, Two's Complement			
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	384fs	12.288	16.934	18.432	MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE[1]					
THD+N at F/S (0dB)	f_{IN} = 991Hz	–82	–87		dB
THD+N at –60fdB	f_{IN} = 991kHz		–34		dB
Dynamic Range	EIAJ A-weighted		94		dB
S/N Ratio	EIAJ A-weighted	92	98		dB
Channel Separation	f_{IN} = 991Hz	90	96		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple	Normal Mode			±0.17	dB
Pass Band Ripple	Double Speed Mode			±0.22	dB
Stop Band Attenuation	Normal Mode	–35			dB
Stop Band Attenuation	Double Speed Mode	–34			dB
Pass Band	Normal Mode		0.4535		fs
Pass Band	Double Speed Mode		0.4535		fs
Stop Band	Normal Mode		0.5465		fs
Stop Band	Double Speed Mode		0.5465		fs
De-emphasis Error	(f_S 32kHz ~ 48kHz)	–0.2		+0.55	dB
ANALOG OUTPUT					
Voltage Range			3.1		Vp-p
Load Impedance		5k			Ω
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current $+I_{CC}$ $+I_{DD}$	$+V_{CC}$ = $+V_{DD}$ = +5.0V		28	40	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5.0V		140	200	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting.

PIN ASSIGNMENTS

PIN NAME	NUMBER	FUNCTION
Input Interface Pins		
LRCIN	1	Sample Rate Clock Input. Controls the update rate (fs).
DIN	2	Serial Data Input. MSB first, right justified format contains a frame of 16-bit or 20-bit data.
BCKIN	3	Bit Clock Input. Clocks in the data present on DIN input.
Mode Controls and Clock Signals		
CLKO	4	Buffered Output of Oscillator. Equivalent to fs.
XTI	5	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
XTO	6	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 5) of the crystal oscillator. When using an external clock, leave XTO open.
MODE	24	Operation Mode Select. For serial mode, tie MODE "High". For parallel mode, tie MODE "Low".
MUTE	25	Mute Control. To disable soft mute, tie MUTE "High". To enable soft mute, tie MUTE "Low".
MD/DM1	26	Mode Control for Data/De-emphasis. See "Mode Control Functions" on page 10.
MC/DM2	27	Mode Control for BCKIN/De-emphasis. See "Mode Control Functions" on page 10.
ML/DSD	28	Mode Control for WDCK/Double speed dubbing. See "Mode Control Functions" on page 10.
Analog Functions		
$V_{OUT}R$	13	Right Channel Analog Output.
$V_{OUT}L$	16	Left Channel Analog Output.
Power Supply Connections		
DGND	7, 22	Digital Ground.
V_{DD}	8, 21	Digital Power Supply (+5V).
$V_{CC}2R$	9	Analog Power Supply (+5V), Right Channel DAC.
AGND2R	10	Analog Ground (DAC), Right Channel.
EXT1R	11	Output Amplifier Common, Right Channel. Bypass to ground with a 10µF capacitor.
EXT2R	12	Output Amplifier Bias, Right Channel. Connect to EXT1R.
AGND	14	Analog Ground.
V_{CC}	15	Analog Power Supply (+5V).
EXT2L	17	Output Amplifier Bias, Left Channel. Connect to EXT1L.
EXT1L	18	Output Amplifier Common, Left Channel. Bypass to ground with a 10µF capacitor.
AGND2L	19	Analog Ground (DAC), Left Channel.
$V_{CC}2L$	20	Analog Power Supply (+5V), Left Channel DAC.
NC	23	No Connection.

ABSOLUTE MAXIMUM RATINGS

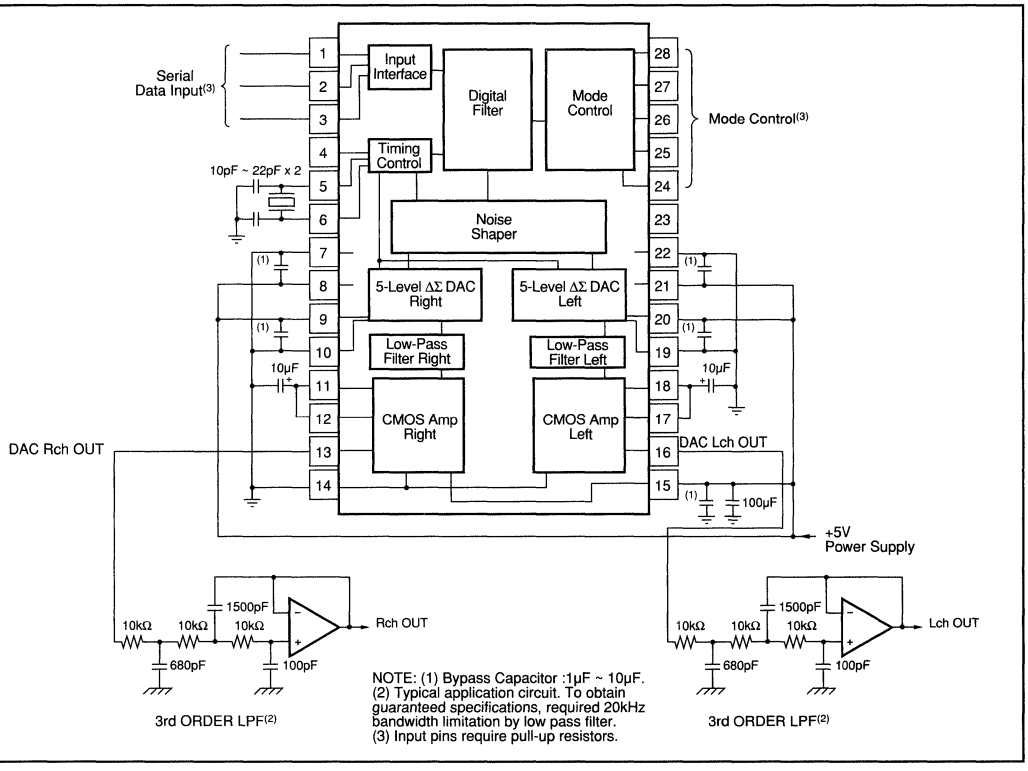
Power Supply Voltage	+6.5V
$+V_{CC}$ to V_{DD} Voltage	±0.1V
Input Logic Voltage	$-0.3V \sim V_{DD}+0.3V$
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PACKAGE INFORMATION

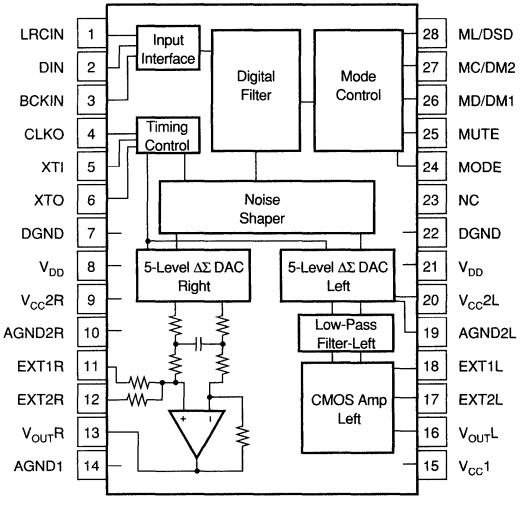
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1712U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

CONNECTION DIAGRAM



PIN CONFIGURATION



DATA INPUT TIMING

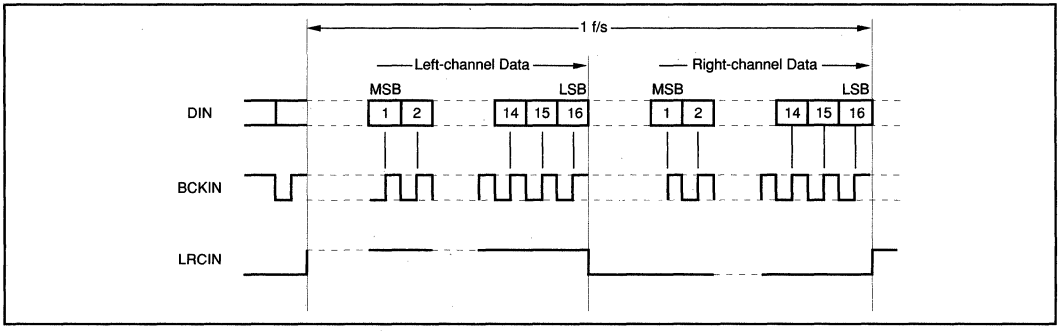


FIGURE 1. Normal Format, 16-Bit (LRCIN H: Lch).

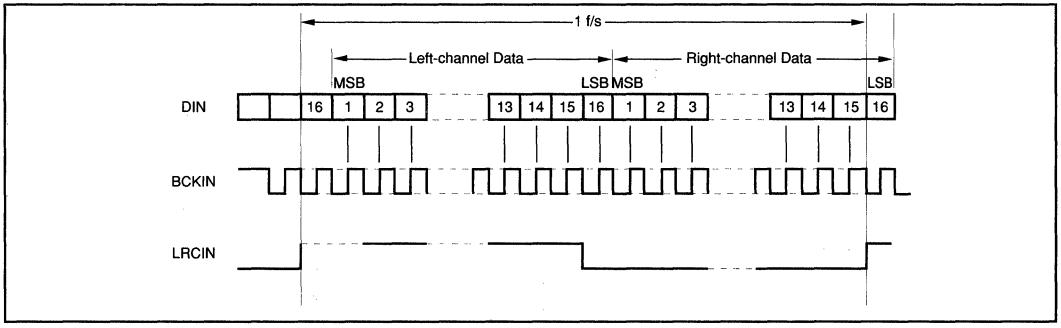


FIGURE 2. IIS Format, 16-Bit (32 BCKIN/fs, continuous data).

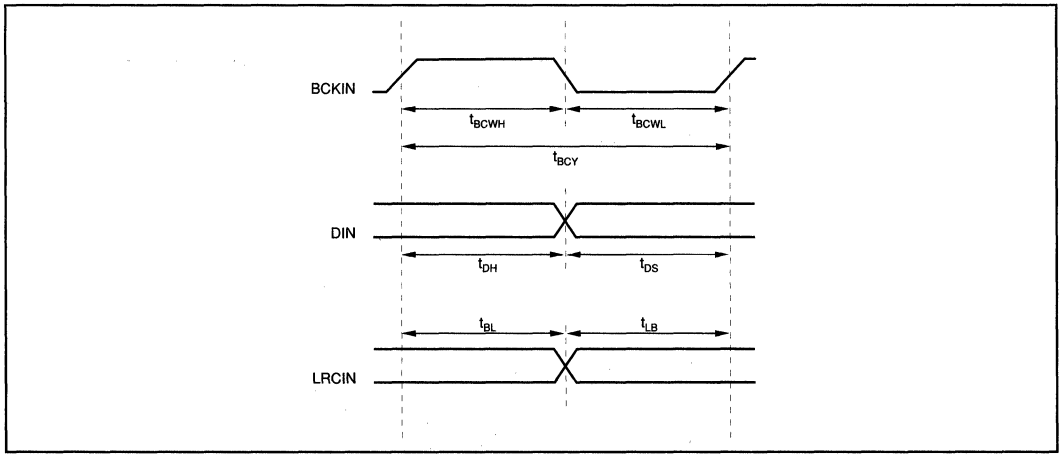


FIGURE 3. Data Input Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRC I Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE I. Data Input Timing Specifications.

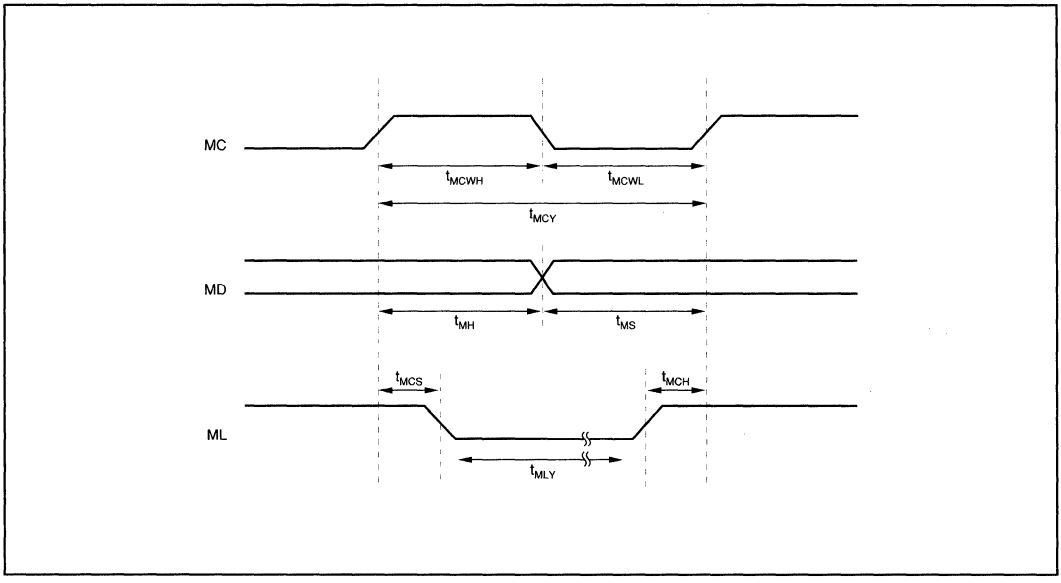


FIGURE 4. Serial Mode Control Timing.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

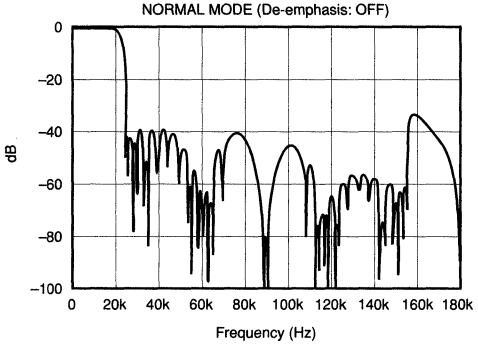
TABLE II. Serial Mode Control Timing Specifications (Refer to Figure 5).

TYPICAL PERFORMANCE CURVES

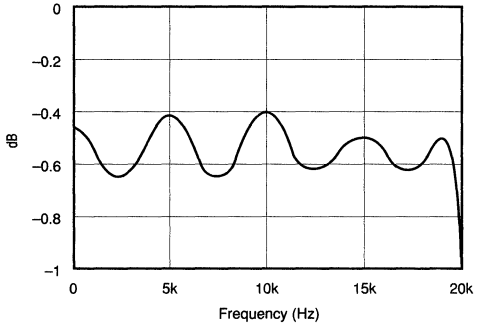
All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384fs, and 16-bit data, unless otherwise noted.

DIGITAL FILTER

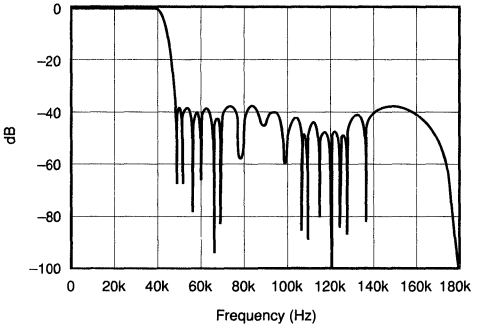
OVERALL FREQUENCY CHARACTERISTICS
NORMAL MODE (De-emphasis: OFF)



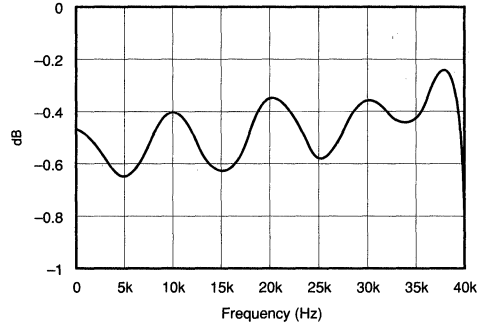
PASSBAND RIPPLE CHARACTERISTIC
NORMAL MODE (De-emphasis: OFF)



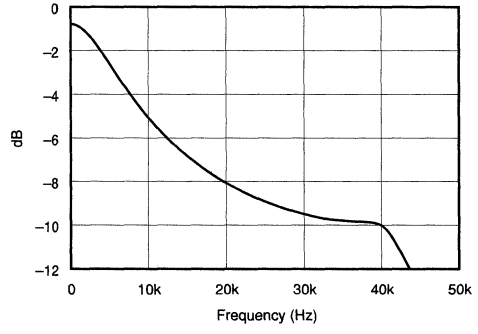
OVERALL FREQUENCY CHARACTERISTICS
DOUBLE-SPEED MODE (De-emphasis: OFF)



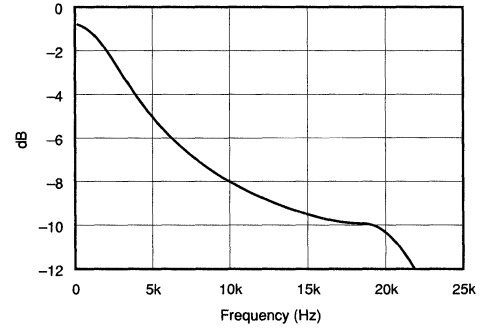
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
DOUBLE-SPEED MODE (De-emphasis: OFF)



DE-EMPHASIS CHARACTERISTIC
DOUBLE-SPEED MODE



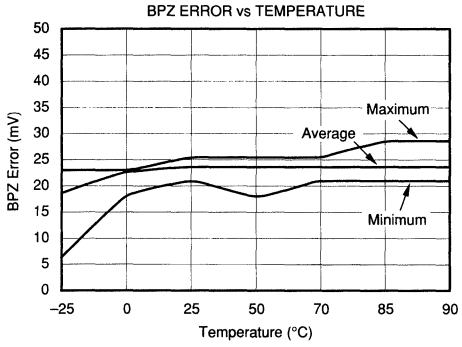
DE-EMPHASIS CHARACTERISTIC
NORMAL MODE

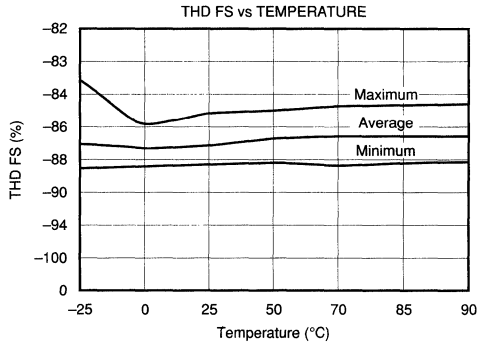


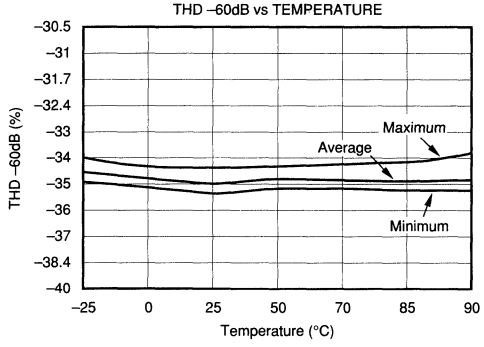
TYPICAL PERFORMANCE CURVES (CONT)

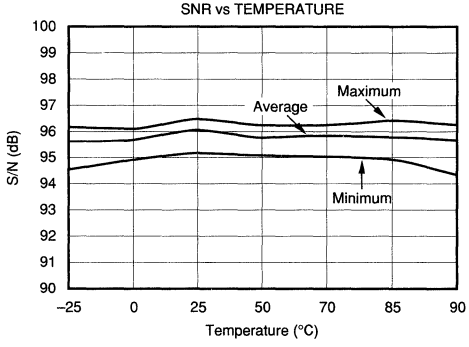
All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384fs, and 16-bit data, unless otherwise noted.

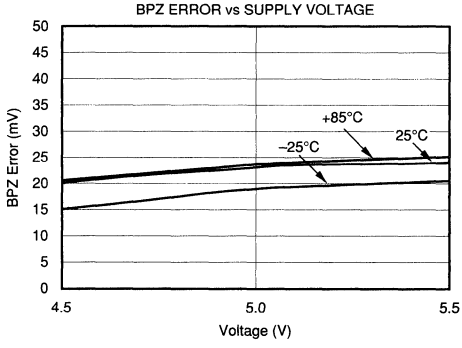
DYNAMIC PERFORMANCE (Based on 200 piece sample from 3 diffusion runs)

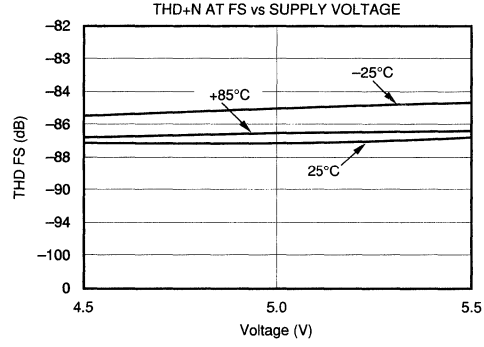








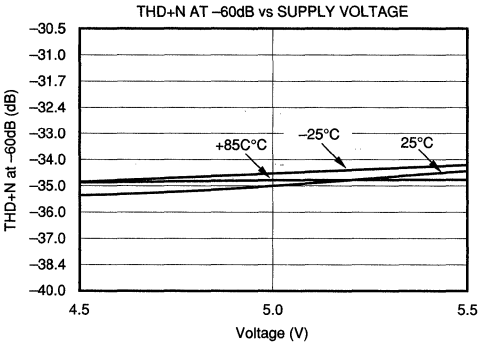


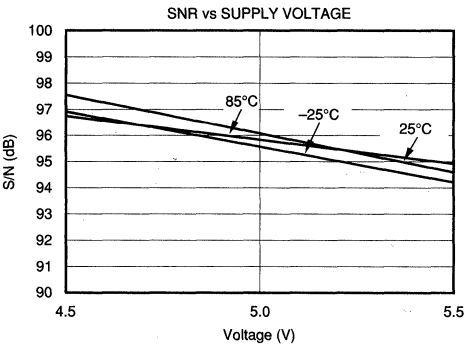


TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384fs, and 16-bit data, unless otherwise noted.

DYNAMIC PERFORMANCE (Based on 200 piece sample from 3 diffusion runs)





CAUTION: Minimum and maximum values on typical performance curves are not meant to imply a guarantee. Curves should be used for reference only. Refer to specifications for guaranteed performance.

FUNCTIONAL DESCRIPTION

PCM1712 has several built-in functions including digital attenuation, digital de-emphasis and soft mute. These functions are software controlled. PCM1712 can be operated in two different modes, **Serial** or **Parallel**. Serial Mode is a three-wire interface using pin 26 (MD), pin 27 (MC), and pin 28 (ML). Data on these pins are used to control de-emphasis modes, mute, double-speed dubbing, input resolution and input formats. PCM1712 can also be operated in parallel mode, where static control signals are used on pins 26 (DM1), pin 27 (DM2), and pin 28 (DSD). Operation of both of these modes are covered in detail in the next sections.

CAUTION: Mode control signals operate on level triggered logic. The minimum timing conditions detailed in Figures 4 and 5 MUST be observed.

MODE CONTROL: SERIAL/PARALLEL SELECTION

MODE = H	Serial Mode
MODE = L	Parallel Mode

TABLE III. Serial and Parallel Mode are Selectable by MODE Pin (Pin 24).

MODE CONTROL: SELECTABLE FUNCTIONS

FUNCTION	SERIAL MODE (MODE = H)	PARALLEL MODE (MODE = L)
Input Data Format Selection	0	X (Normal Mode Fixed)
Input LRCI Polarity Selection	0	X
De-emphasis Control	0	0
Mute	0	0
Attenuation	0	X
Double-Speed Dubbing	0	0
NOTE: 0: Selectable, X: Not Selectable.		

TABLE IV. Selectable Functions in Serial Mode and Parallel Mode.

Table IV indicates which functions are selectable within the user's chosen mode. All of the functions shown are selectable within the serial mode, but only de-emphasis control, mute and double-speed dubbing may be selected when using PCM1712 in the parallel mode.

PARALLEL-MODE: DE-EMPHASIS CONTROL (PIN 24 [MODE] = L)

DM1 (Pin 26)	DM2 (Pin 27)	De-emphasis
L	L	OFF
H	L	32kHz
L	H	48kHz
H	H	44.1kHz

TABLE V. De-Emphasis (Pins 26 and 27).

In the parallel mode, de-emphasis conditions are controlled by the logic levels on pin 26 (DM1) and pin 27 (DM2). For PCM1712, de-emphasis can operate at 32kHz, 44.1kHz, 48kHz, or disabled.

PARALLEL-MODE: DOUBLE-SPEED DUBBING CONTROL (PIN 24 [MODE] = L)

DSD = H	Normal Mode
DSD = L	Double Speed Dubbing Mode

TABLE VI. DSD (Pin 28).

In the parallel mode, double-speed dubbing can be enabled by holding pin 28 (DSD) at logic "low".

SERIAL MODE CONTROL

In order to use all of PCM1712's functionality, the **serial mode control** should be used. PCM1712 must be addressed three separate times to set all of the various registers and flags that control these functions.

Table VII together with Figure 6 details the control of the PCM1712 in the serial mode. Internal latches are used to hold this serial data until the PCM1712 is enabled to use the data. The serial mode is used by applying clocked data to the following pins:

NAME	PIN	FUNCTION
MC	27	Clock for Strobing in Data
ML	28	Latches Data into the Registers
MD	26	8-bit Data Word Defining Operation

DIGITAL ATTENUATION

One of the functions which can be implemented through use of the serial mode control is attenuation. This function allows the user to control the level of the output, independent of the input level set by the actual input data supplied to the DAC.

Referring to Figure 5, when the first data bit (B0) on MD (pin 26) is low, the attenuation function is enabled. The next seven bits (B1 - B6) define a binary value, ATT_DATA, that indicates the desired level of attenuation. The attenuation level is given by:

$$\text{Level} = 20\log_{10}(1 - \text{ATT\_DATA}/127)\ \text{dB}$$

When all 7 bits of the ATT_DATA word are high (ATT_DATA = 127), attenuation is infinite and the output of PCM1712 will be zero.

	B0	B1	B2	BIT NO.	MODE FLAG	FUNCTION MODE SELECTION MODE	BIT VALUE	SELECTED FUNCTION	MODE BY DEFAULT
Mode 1	1	0	0	B3	DEEM2	Sampling Frequency for De-emphasis		DEEM2 0 1 / DEEM1 0 48kHz / 1 32kHz 44.1kHz	44.1kHz
				B4	DEEM1				
				B5	IIR	De-emphasis	0	De-emphasis OFF	OFF
							1	De-emphasis ON	
				B6	MUTE	Mute	0	Mute OFF	OFF
							1	Mute ON	
				B7	DSD	Double-Speed	0	Double-speed OFF	OFF
							1	Double-speed ON	
Mode 2	1	0	1	B3		Not Assigned			
				B4		Not Assigned			
				B5		Not Assigned			
				B6	LRPL	Polarity for LRCI	0	Lch:high/Rch:low	Lch:HIGH Rch:LOW
							1	Lch:low/Rch:high	
				B7	IIS	Input Format	0	Normal	Normal
							1	IIS	

TABLE VII. Serial-Mode Control Input Format (MODE: H, Pin 24).

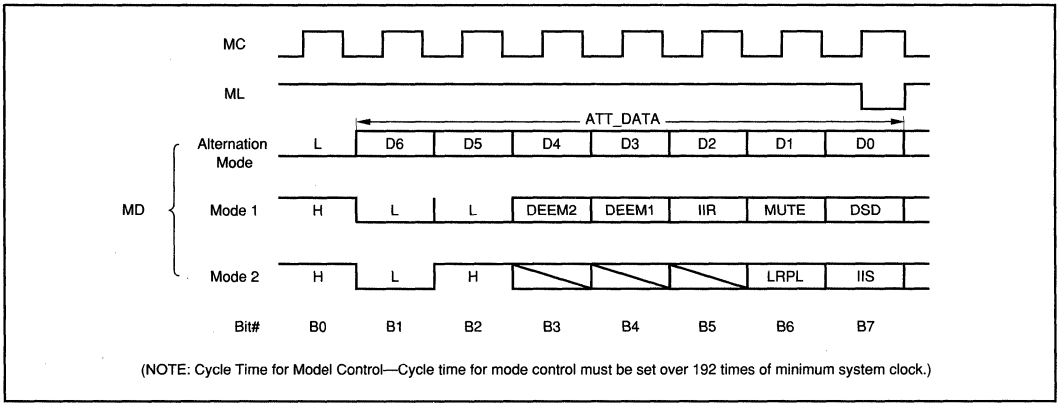


FIGURE 5. Mode Control Input Format, Serial Mode.

MODE 1 CONTROLS

This mode can be enabled with the sequence of 1, 0, 0 as the first three bits on MD (pin 26). This mode allows for the following functions:

De-emphasis	On/Off
De-emphasis Frequency	32kHz, 44.1kHz, 48kHz
Soft Mute	On/Off
Double-Speed Dubbing	On/Off

DIGITAL DE-EMPHASIS

PCM1712 allows three different sampling rates for digital de-emphasis. B3 and B4 are used for binary control of the de-emphasis frequency:

B3	B4	FREQUENCY
0	0	OFF
0	1	48kHz
1	0	32kHz
1	1	44.1kHz

Once the reset has been established on pin 27 (MC), the de-emphasis frequency defaults to 44.1kHz. B5 can be used to override B3 and B4; a logic low on B5 disables de-emphasis, and a logic high on B5 forces de-emphasis at 44.1kHz.

SOFT MUTE

Soft mute is enabled when B6 is high. The soft mute occurs gradually, unlike the forced infinite zero detection. When the mute data bit is high, complete muting will occur in 127/fs seconds.

DOUBLE-SPEED DUBBING

Double-speed dubbing is enabled when B7 is high. Since f_S is set at 44.1kHz, the system clock in double-speed mode is at 192fs.

MODE 2 CONTROLS

This mode is enabled when the first three bits on MD are 1, 0, 1. Mode 2 allows for the following functions:

LR Polarity	Controls Left/Right Channel Select
Input Format	Normal/IIS (Philips format)

SAMPLE RATE CLOCK POLARITY

B6 controls the polarity of the sample rate clock (LRCIN) polarity. When B6 is low, data will be accepted on the left channel when LRCIN is high, and on the right channel when LRCIN is low. When B6 is high, data will be accepted on the right channel when LRCIN is high, and on the left channel when LRCIN is low.

INPUT FORMAT

Normal input mode for PCM1712 is MSB first, right justified. PCM1712 may also be operated with IIS input format. When B7 is low, the input format is "normal". When B7 is high, the input format is "IIS".

DEFAULT MODE

At initial power-on, default settings for PCM1712 are 44.1kHz f_S, de-emphasis off, mute off, double speed off, infinite zero detect on, 16-bit input LRCIN left channel high, and normal input mode.

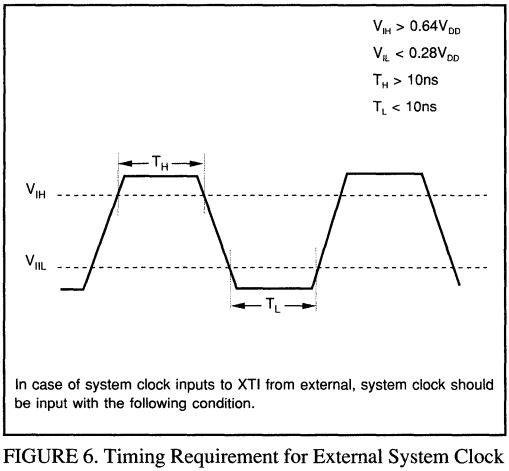


FIGURE 6. Timing Requirement for External System Clock (XTi).

SYSTEM CLOCK

SAMPLING FREQUENCY	SYSTEM CLOCK	FREQUENCY
32kHz	384fs	12.2880MHz
44.1kHz	384fs	16.9344MHz
48kHz	384fs	18.4320MHz

NORMAL/DOUBLE-SPEED DUBBING

For most CD playback applications operating at 384fs, the system clock frequency must be 16.9344MHz, in both the normal mode and double-speed dubbing mode. Table VIII illustrates the relationship between fs and output clock frequency in both modes.

PARAMETER	DSD	
	H (Normal)	L (Double Speed)
XTI Input Clock Frequency	384fs	192fs
XTI Frequency	16.9344MHz (f_S = 44.1kHz)	16.9344MHz (f_S = 88.2kHz)
CLKO Output Clock Frequency	384fs	192fs

TABLE VIII. Relationship Between Normal/Double Speed and fs.

EXTERNAL SYSTEM CLOCK

Figure 7 is a diagram showing the internal clock in conjunction with an external crystal oscillator.

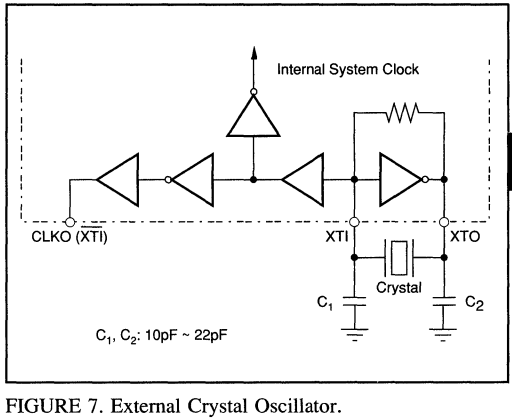


FIGURE 7. External Crystal Oscillator.

Figure 8 is a diagram showing the internal clock with an external clock source, instead of an oscillator. An external system clock (input to XTI) must meet timing requirement which is shown in Figure 6.

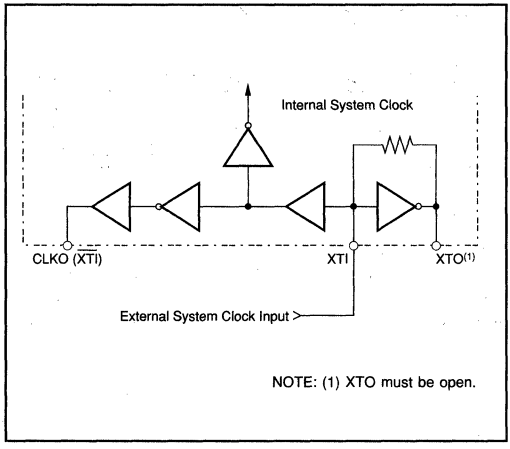


FIGURE 8. Latch-up Prevention Circuit.

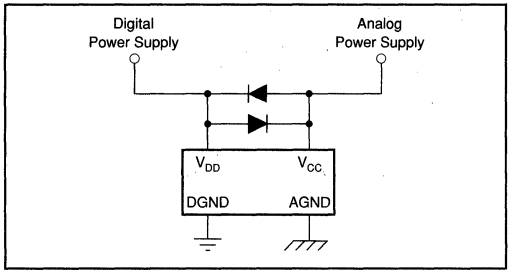


FIGURE 9. Latch-up Prevention Circuit.

POWER SUPPLY CONNECTIONS

PCM1712 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 9.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 16 for optimal values of bypass capacitors. For applications which require very high performance at low levels (such as keyboards, synthesizers, etc.), it may be beneficial to provide additional bypassing on pin 15 (V_{CC1}) with a low ESR 100µF capacitor. This will eliminate stray tones which may be above the noise floor.

THEORY OF OPERATION

The delta-sigma section of PCM1712 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled 16-bit input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 10. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

Multi Level Delta Sigma

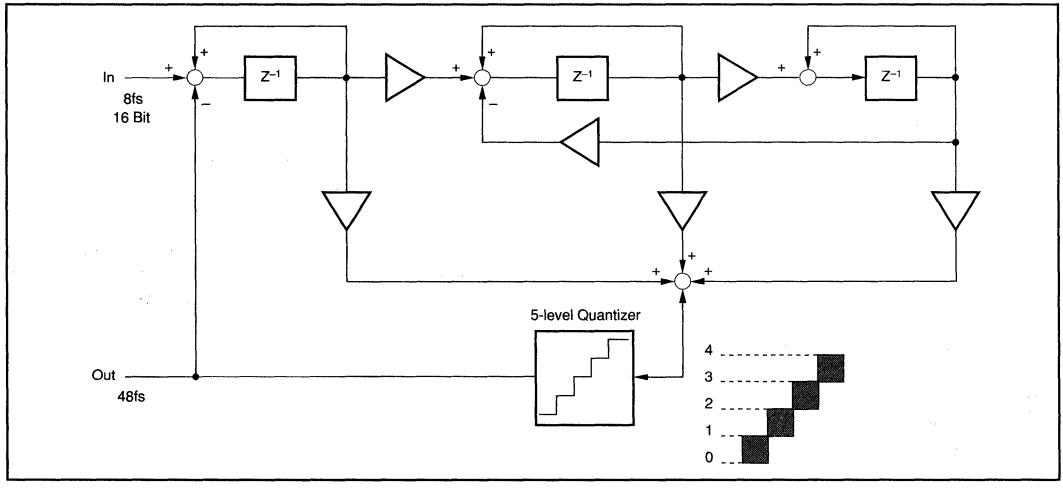


FIGURE 10. 5 Level ΔΣ Modulator Block Diagram.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is 48fs. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 11.

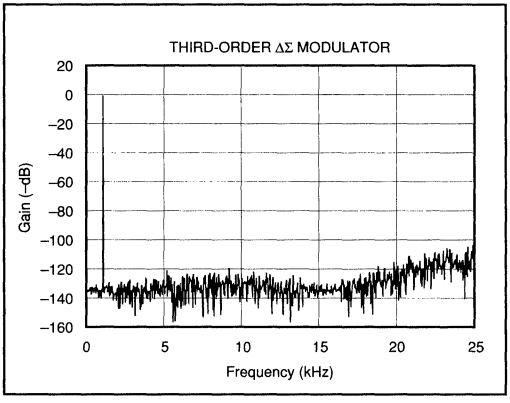


FIGURE 11. Quantization Noise Spectrum.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1712:

$$T_D = 12.625 \times 1/fs$$

For f_S = 44.1kHz, T_D = 12.625/44.1kHz = 286.28μs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

INTERNAL RESET

When power is first applied to PCM1712, an automatic reset function occurs after 64 cycles of LRCIN.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1712 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD + N, etc. to 20kHz. Failure to use such a filter will result in higher THD + N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 12. The higher frequency rolloff of the filter is shown in Figure 13. If the user's application has the PCM1712 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 14. For some applications, a passive RC filter or 2nd-order filter may be adequate.

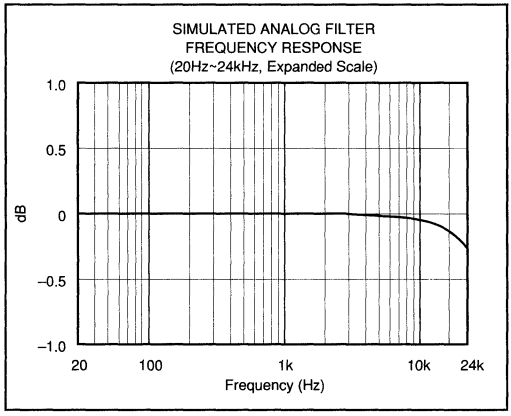


FIGURE 12. Low Pass Filter Frequency Response.

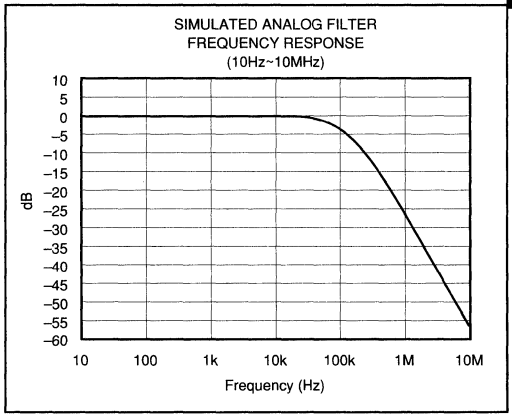


FIGURE 13. Low Pass Filter Frequency Response.

TEST CONDITIONS

Figure 15 illustrates the actual test conditions applied to PCM1712 in production. The 11th-order filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the third-order filter shown in Figure 14 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –92dB when the external 20kHz second-order filter is used.

EVALUATION FIXTURES

An evaluation fixture is available for PCM1712.

DEM-PCM1712

This evaluation fixture is primarily intended for quick evaluation of the PCM1712's performance. DEM-PCM1712 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1712 does not contain a receiver chip or an external low pass filter. DEM-PCM1712 requires a single +5V power supply.

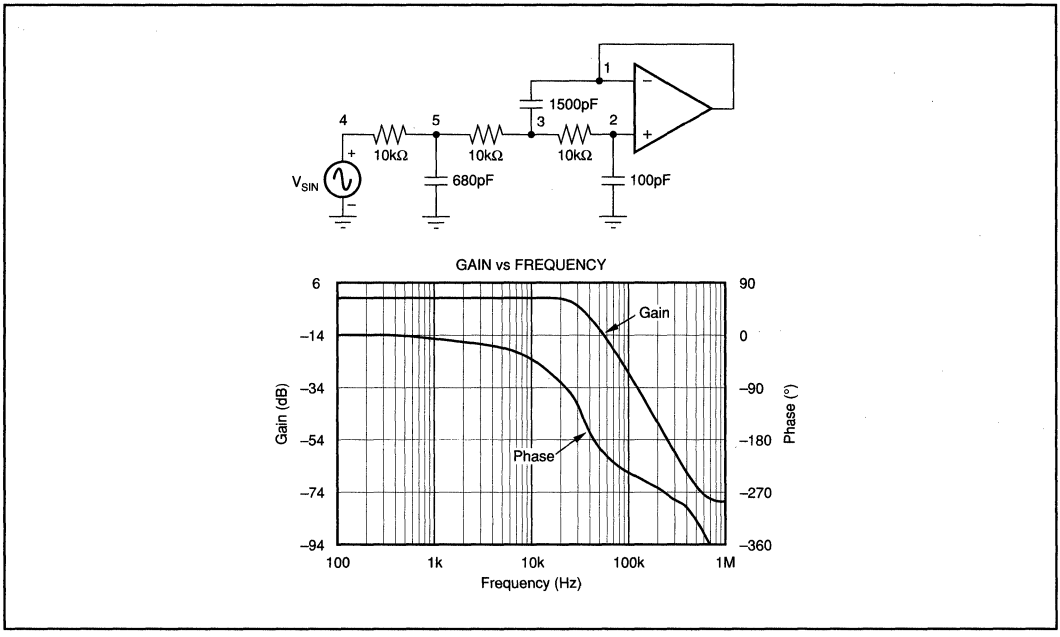


FIGURE 14. 3rd-Order LPF.

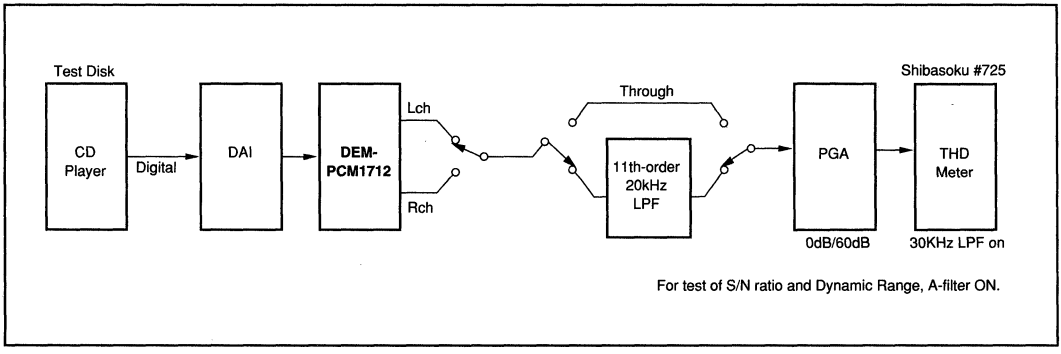


FIGURE 15. Test Block Diagram.

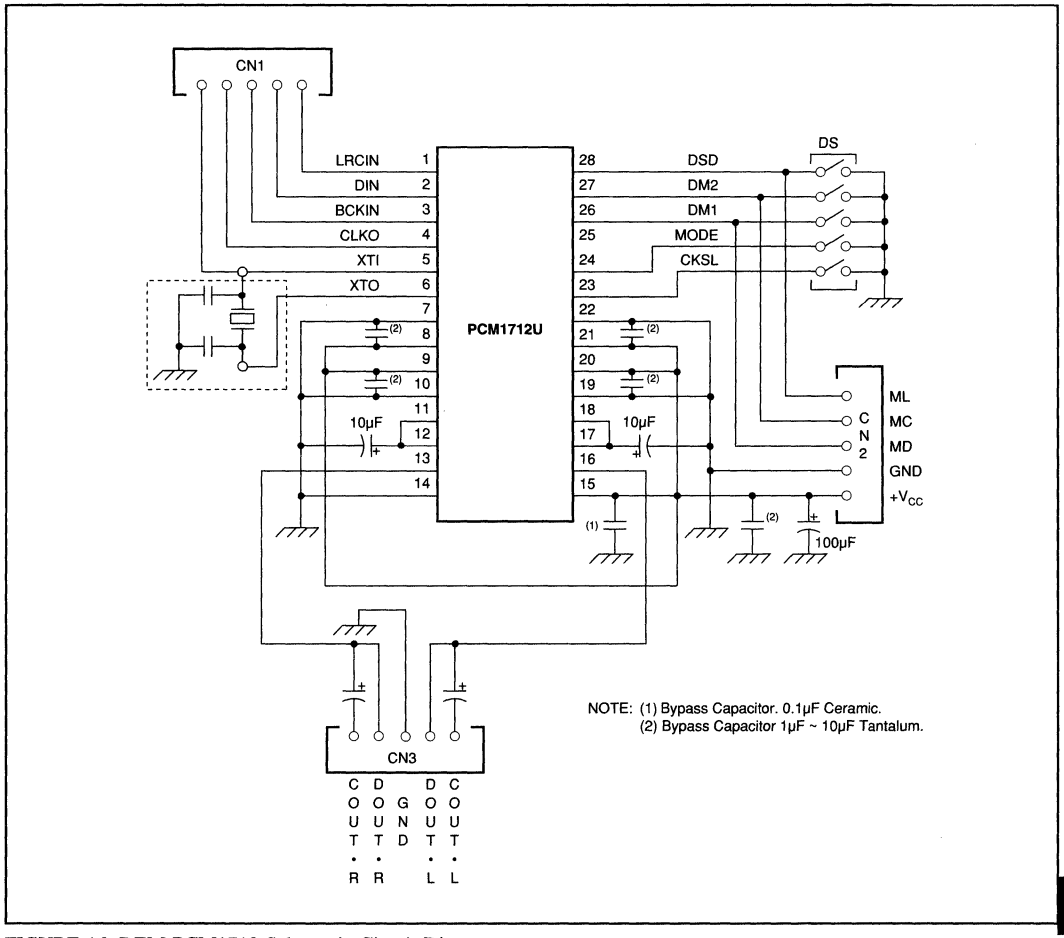


FIGURE 16. DEM-PCM1712 Schematic Circuit Diagram.

BURR-BROWN®

PCM1715U

Dual Voltage Output CMOS Delta-Sigma DIGITAL-TO-ANALOG CONVERTER With On-Chip Digital Filter

FEATURES

- **DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER**
- **HIGH PERFORMANCE:**
  THD+N: 0.0025% (–92dB) typ
  Dynamic Range: 98dB typ
  S/N RATIO: 110dB typ
- **ANALOG VOLTAGE OUTPUT:**
  V_O = 3.2Vp-p
- **ON-CHIP ANALOG LOW PASS FILTER**
- **JITTER TOUGH AND LOW RADIO FREQUENCY INTERFERENCE ENERGY ARCHITECTURE**
- **SYSTEM CLOCK 256fs or 384fs**
- **ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH:**
  Lch/Rch Individual Attentuator Control
  Digital De-Emphasis (44.1kHz)
  Analog Output Mode Select
- **SINGLE +5V POWER SUPPLY OPERATION**
- **SMALL 28-PIN SOIC PACKAGE**

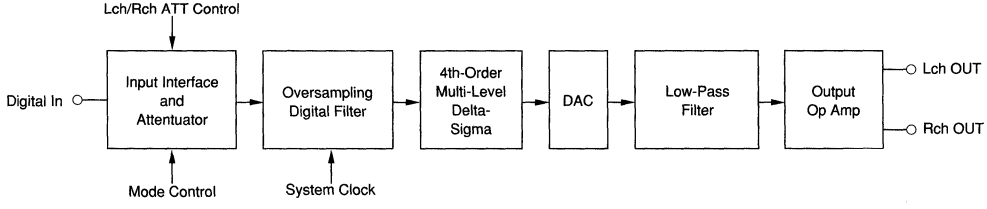
DESCRIPTION

The PCM1715 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1715 is a unique multi-level 4th-order delta-sigma architecture that eliminates influence from input clock jitter and RF interferance resulting in truly superior performance.

The PCM1715 has individual channel attenuator and analog output mode select function which is suitable for CD-ROM application.

The on-chip digital filter of the PCM1715 has –62dB stop band attenuation and ±0.008dB ripple in the pass band.

The PCM1715 can be used in a wide variety of consumer audio applications. Its low cost, small size, and single +5V operation make it ideal for portable, automotive, CD players, CD-I, CD-ROM, VIDEO-CD, tuners, music instruments, and other digital audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

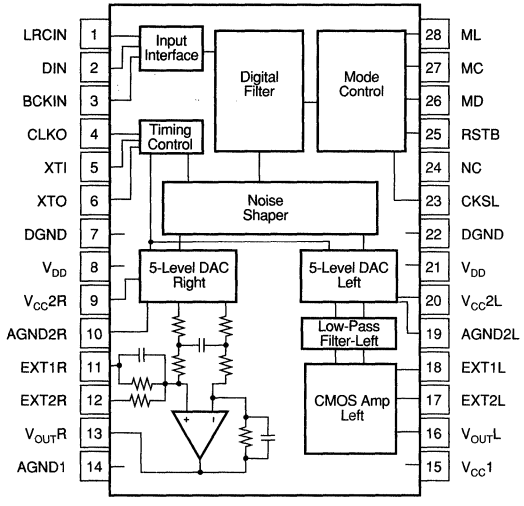
ELECTRICAL

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1715U MIN	PCM1715U TYP	PCM1715U MAX	UNITS
RESOLUTION			16		Bits
DIGITAL INPUT					
Logic Family					
Input Logic Level (except XTi)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (except XTi)				–200	µA
Input Logic Level (XTi)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTi)				±50	µA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current (CLKO)		±10			mA
Data Format			MSB First, Two's Complement		
Sampling Frequency			44.1		kHz
System Clock Frequency	384fs		16.934		MHz
System Clock Frequency	256fs		11.2894		MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20.0		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE					
THD+N at F/S (0dB)[1]	f_{IN} = 991Hz		–92	–88	dB
THD+N at –60dB[1]	f_{IN} = 991Hz		–36	–32	dB
Dynamic Range	EIAJ A-weighted		98		dB
S/N Ratio	EIAJ A-weighted	104	110		dB
Channel Separation	f_{IN} = 991Hz	90	94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple				±0.008	dB
Stop Band Attenuation		–62			dB
Pass Band			0.4535		fs
Stop Band			0.5465		fs
De-emphasis Error	(fs = 44.1kHz)			+0.03	dB
ANALOG OUTPUT					
Voltage Range	fs (0dB) OUT		3.2		Vp-p
Load Impedance		5			kΩ
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current: $+I_{CC}$ $+I_{DD}$	$+V_{CC}$ = $+V_{DD}$ = +5.0V		45	70	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5.0V		225	350	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) 30kHz LPF, 400Hz HPF, Average Mode.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	LRCIN	Sample Rate Clock Input (fs)
2	DIN	Data Input
3	BCKIN	Bit Clock Input
4	CLKO	Buffered Output of Oscillator
5	XTI	Oscillator Input (External Clock Input)
6	XTO	Oscillator Output
7	DGND	Digital Ground
8	V_{DD}	Digital Power Supply (+5V)
9	$V_{CC}2R$	Analog (DAC) $+V_{CC}$, Rch
10	AGND2R	Analog (DAC) Ground, Rch
11	EXT1R	Output Amp Common, Rch
12	EXT2R	Output Amp Bias, Rch
13	$V_{OUT}R$	Rch Analog Output
14	AGND	Analog Ground

PIN	NAME	FUNCTION
15	$V_{CC}1$	Analog Power Supply (+5V)
16	$V_{OUT}L$	Lch Analog Output
17	EXT2L	Output Amp Bias, Lch
18	EXT1L	Output Amp Common, Lch
19	AGND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) $+V_{CC}$, Lch
21	V_{DD}	Digital Power Supply, (+5V)
22	DGND	Digital Ground
23	CKSL	System Clock Select (H:384fs, L:256fs)
24	NC	No Connection
25	RSTB	Reset
26	MD	Mode Control
27	MC	Mode Control, BCK
28	ML	Mode Control, WDCK

NOTE: All input pins require pull up resistors.

ABSOLUTE MAXIMUM RATINGS

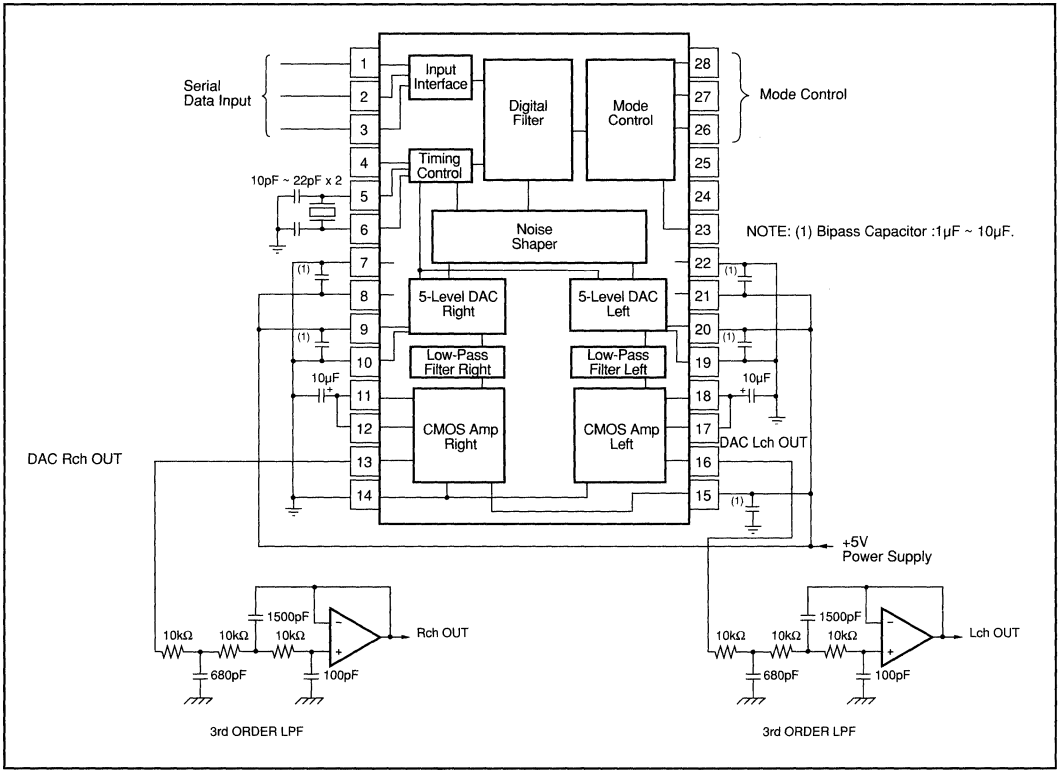
Power Supply Voltage	±6.5VDC
$+V_{CC}$ to V_{DD} Voltage	±0.1V
Input Logic Voltage	–0.3V ~ V_{DD} +0.3V
Power Dissipation	400mW
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PCM1715U	28-Pin SOIC	217

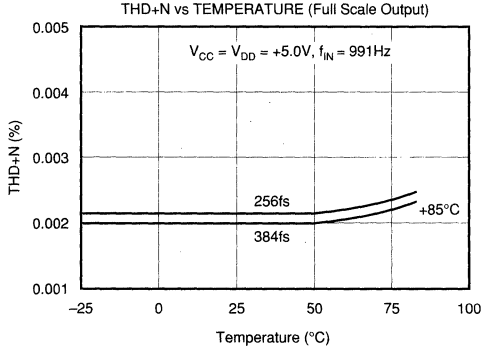
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

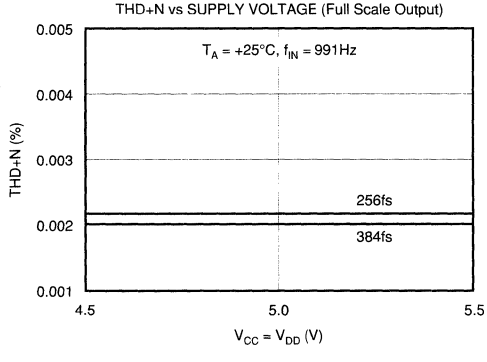
CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

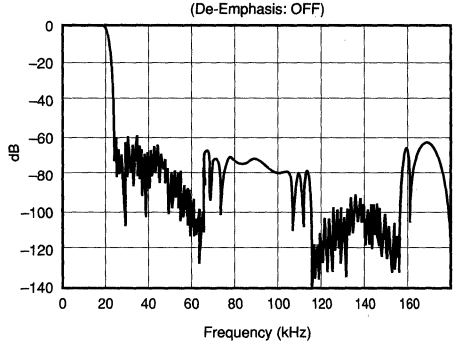




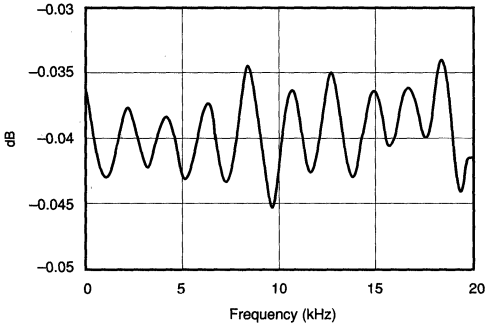
TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, SYSCLK = 384fs/256fs, and 16-bit data, unless otherwise noted.

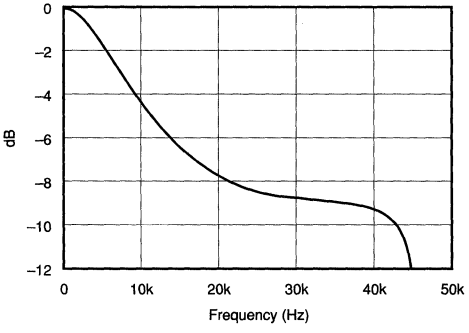
OVERALL FREQUENCY CHARACTERISTIC
(De-Emphasis: OFF)



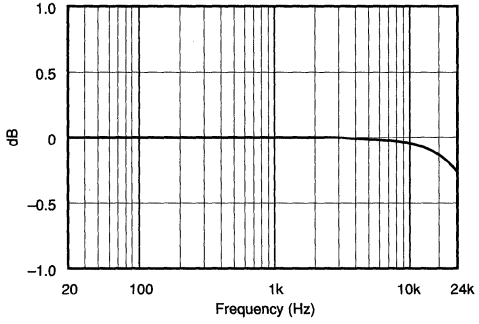
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
(De-Emphasis: OFF)



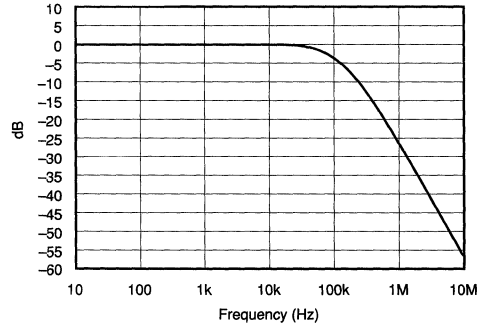
DE-EMPHASIS CHARACTERISTIC



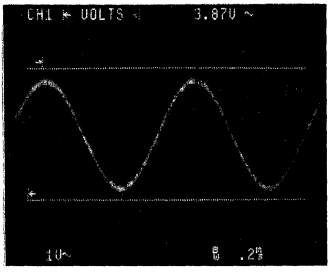
SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(20Hz~24kHz, Expanded Scale)



SIMULATED ANALOG FILTER
FREQUENCY RESPONSE
(10Hz~10MHz)



OUTPUT WAVE FORM FULL SCALE SIGNAL
(Without External Filter)



NOTES: (1) Measured at V_{OUT} Pin (Pin 13 or 16). (2) The PCM1715 has internal analog low pass filter to reduce high frequency noise-shaped spectrum. Application of the PCM1715 requires external post analog low pass filter which has 2nd-Order or 3rd-Order attenuation performance to get low noise analog output.

THEORY OF DELTA-SIGMA OPERATION

The delta-sigma section of the PCM1715 is based on a 5-level amplitude quantizer and a 4th-order filter. This converts the oversampled 16-bit input data to 5-level delta-sigma form. A block diagram of the 5-level modulator is shown in Figure 1.

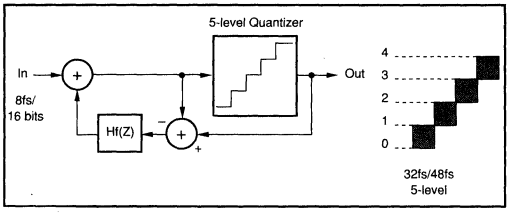


FIGURE 1. Block Diagram of 5-Level Delta-Sigma Quantizer.

This 5-level delta-sigma modulator has the advantage of stability of delta-sigma loop and jitter sensitivity over the typical 1-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8x oversampling digital filter is 48fs at a system clock speed of 384fs, 32fs at a system clock speed of 256fs.

A block diagram of the 4th-order filter section Hf(z) in the delta-sigma modulator is shown in Figure 2.

In general, high order 1-bit delta-sigma modulators have disadvantages due to loop instability. The 5 level delta-sigma modulator of the PCM1715 uses phase compensation techniques to obtain stable operation. In Figure 2, the coefficients, b1 to b4, give the basic form of the filter and –a1 and –a2 are used for phase compensation of the feedback loop.

The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figures 3 and 4. In the audio band, the quantization noise floor level of the PCM1715 is less than –130dB (384fs).

MODE OF OPERATION

Serial inputs to MD, MC, and ML (Pins 26, 27 and 28) control the following functions:

(1) Digital Attenuator [AL0 ~ AL7, AR0 ~ AR7]
Attenuation data is constructed by 8-bit/Lch, 8-bit/Rch (total 16-bit), can be controlled as 255 step attenuation by individual channel. AL0 and AR0 are LSB, and AL7 and AR7 are MSB. Attenuation Level ATT is given by:

$$ATT = 20LOG_{10} (ATT\ DATA/255)\ [dB]$$

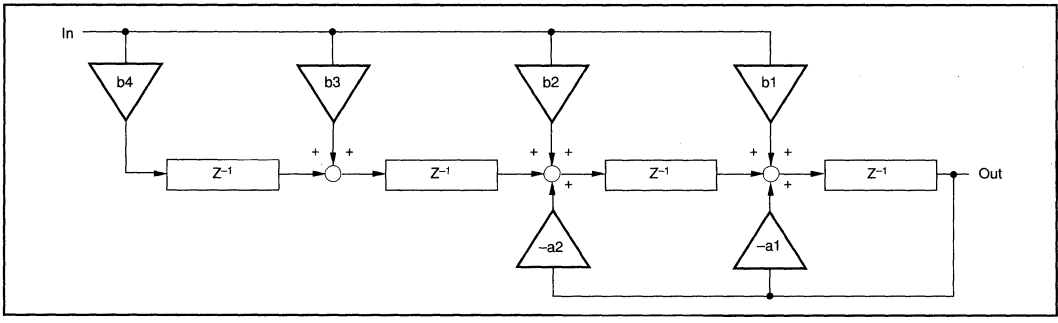


FIGURE 2. Block Diagram of the Hf(z).

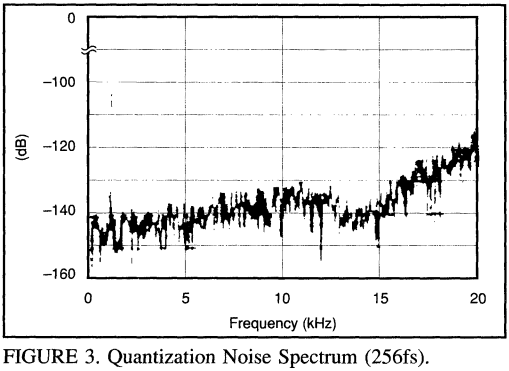


FIGURE 3. Quantization Noise Spectrum (256fs).

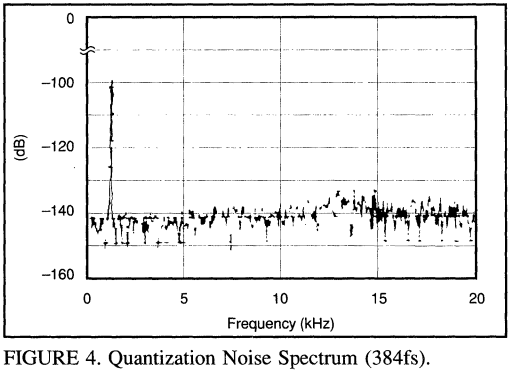


FIGURE 4. Quantization Noise Spectrum (384fs).

At ATT DATA: 0XFF, output is 0dB. At ATT DATA 0X00, output is $-\infty$.

When "Muting" is chosen by output mode control, output goes to $-\infty$ from the present ATT level.

Moving speed from 0dB to $-\infty$ is 1024/f.

Initialized (RESET) ATT level is 0dB.

(2) Versatile Output Mode [PL0 ~ PL3]
By using PL0 ~ PL3 data, up to 16 different output modes (Lch/Rch/L+R/MUTE) can be selected to the output of Lch and Rch, as shown in Table I.

Initialized mode is STEREO mode.

(3) De-emphasis Control (DEM)
De-emphasis function is controlled by DEM flag (H: ON, L: OFF)

De-emphasis is enabled only at 44.1kHzfs. At other fs frequencies, de-emphasis error is not guaranteed. Initialized mode is De-emphasis OFF.

(4) Attenuator Control (ATC)
If common attenuator control of Lch and Rch is needed, use the ATC flag (ATC = "H"). Common attenuation can be controlled by Lch (AL0 ~ AL7) data. Initialized mode is individual.

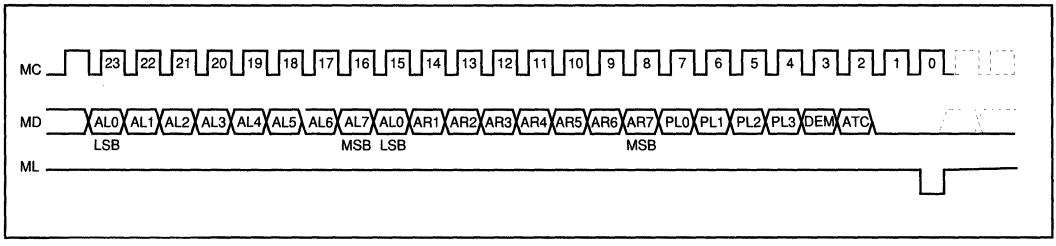
(5) Infinity-Zero Detection
The PCM1715 has an infinity-zero detect function which monitors the input data and bit clock. When the input data is continuously "zero" for 8192 cycles of the bit clock, the infinity zero detect occurs and the DAC outputs are set to bipolar zero ($1/2V_{CC}$).

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE I. PCM1715 Output Mode Control.

(6) Reset
Normally, internal initialize (reset) is done automatically at power on (V_{DD} > 3.5V). The RSTB-pin (Pin 25) accepts external forced reset by RSTB=L. During RSTB=L, the output of the DAC is invalid, set to $1/2V_{CC}$ after internal initialize (1024XTI clock count after RSTB=H).

MODE CONTROL FORMAT



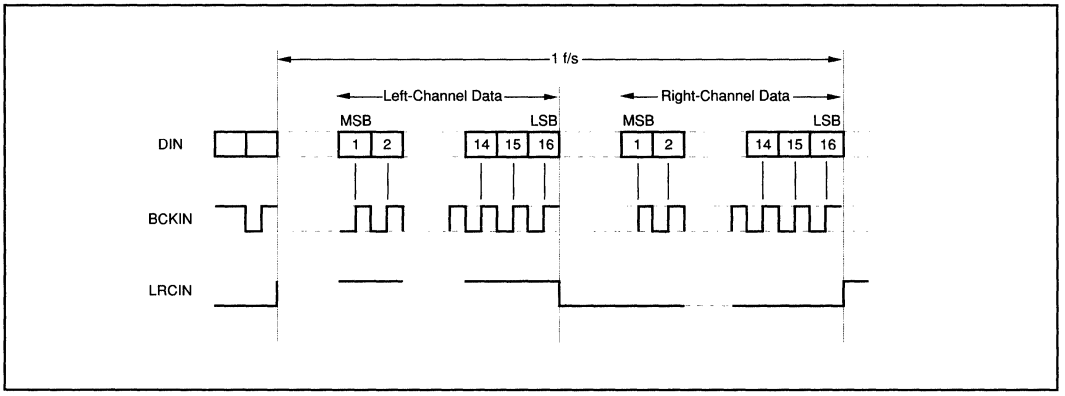


FIGURE 5. Data Input Timing, 16-Bit.

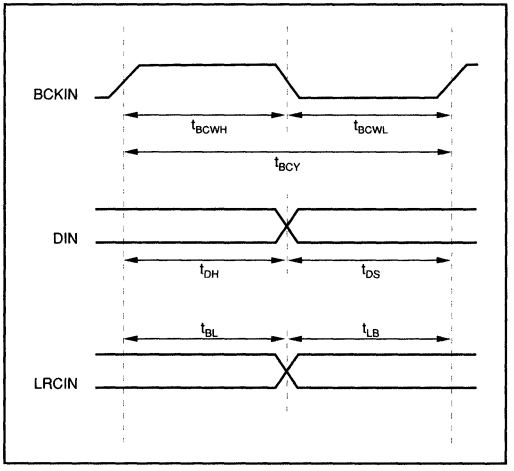


FIGURE 6. Data Input Timing.

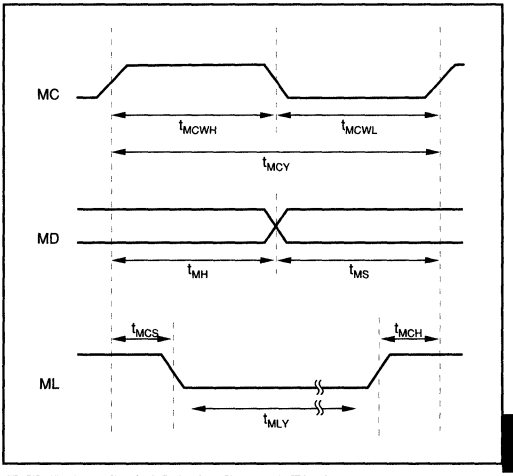


FIGURE 7. Serial Mode Control Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRCI Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE II. Data Input Timing Specifications.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

TABLE III. Serial Mode Control Timing Specifications.

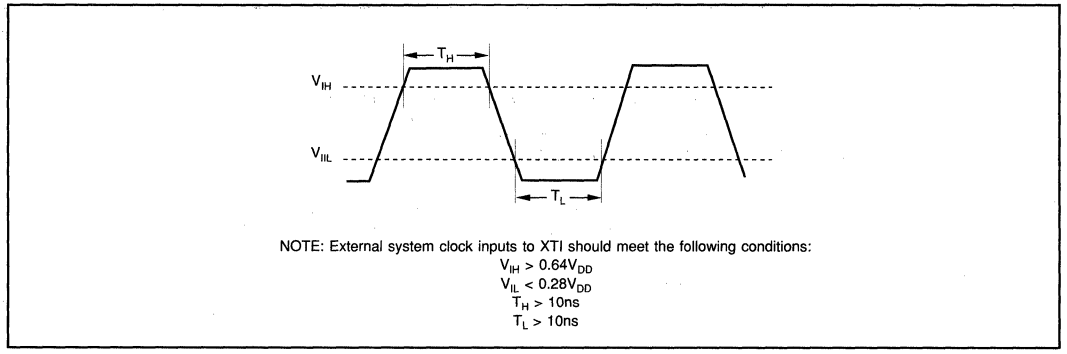


FIGURE 8. Operation Instruction For System Clock.

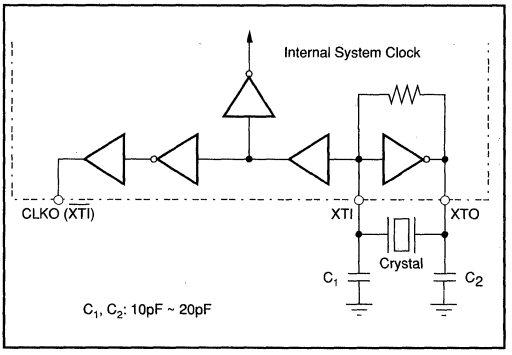


FIGURE 9. Oscillator Circuit Connection Diagram. Optional external crystal oscillator.

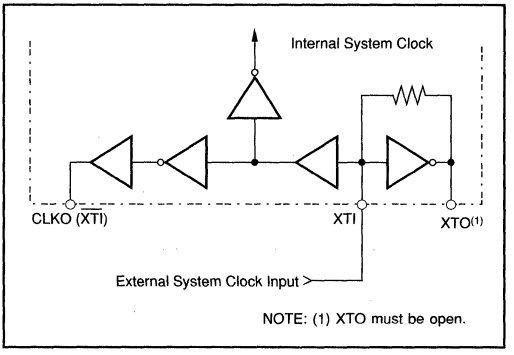


FIGURE 10. Oscillator Circuit Connection Diagram. External system clock.

EVALUATION BOARD

Burr-Brown's DEM-PCM1710 evaluation board for the PCM1710 is capable of evalution of the PCM1715 and PCM1710. Digital input signals for the evaluation board are LRCK, BCK, DATA, and system clock (256fs or 384fs). Power supply requirement is only +5V.

The DEM-PCM1710 has a pattern layout for an optional crystal oscillator. However, the crystal is not installed.

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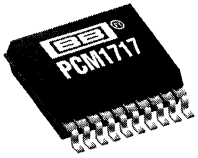


PCM1717E

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

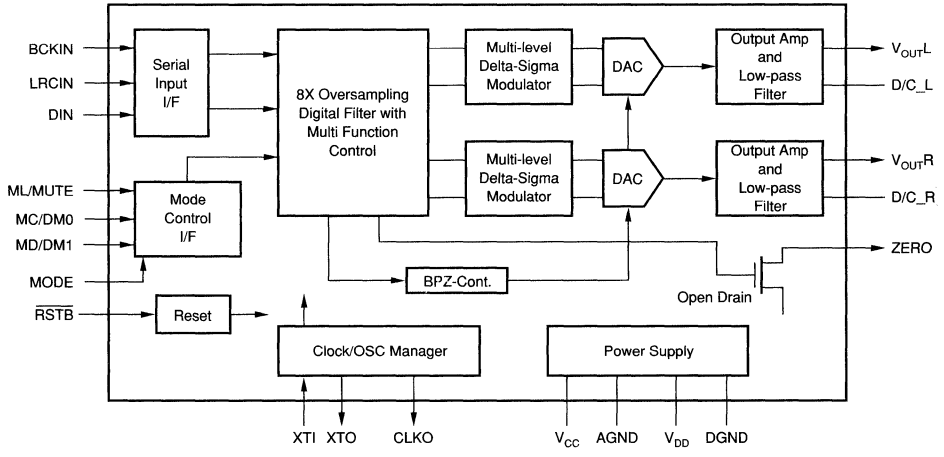
- ACCEPTS 16- OR 18-BIT INPUT DATA
- COMPLETE STEREO DAC:
  8X Oversampling Digital Filter
  Multi-Level Delta-Sigma DAC
  Analog Low Pass Filter
  Output Amplifier
- HIGH PERFORMANCE:
  –90dB THD+N
  96dB Dynamic Range
  100dB SNR
- SYSTEM CLOCK: 256fs or 384fs
- SINGLE +5V POWER SUPPLY
- SELECTABLE FUNCTIONS:
  Soft Mute
  Digital Attenuation (256 Steps)
  Digital De-emphasis
  Output Mode: L, R, Mono, Mute
- SMALL 20-PIN SSOP PACKAGE

DESCRIPTION

The PCM1717 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1717 is fabricated on a highly advanced 0.6µ CMOS process. PCM1717 accepts 16- or 18-bit normal input data format, or 16- or 18-bit IIS data format.

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, and digital de-emphasis. The digital filter features –35dB stop band attenuation and ±0.17dB ripple in the pass band.

PCM1717 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size, and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive, and CD-Karaoke systems.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

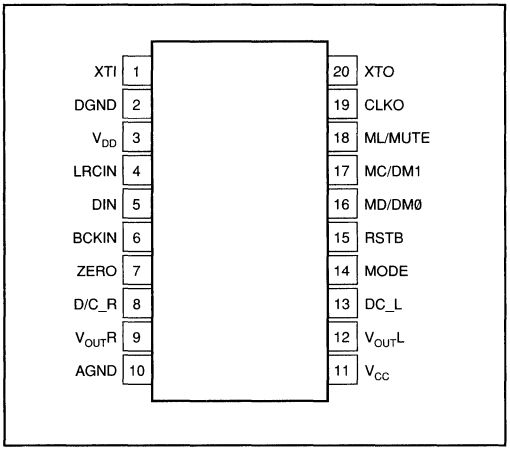
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 16-bit input data, SYSCLK = 384f_S, unless otherwise noted. Measurement bandwidth is 20kHz.

PARAMETER	CONDITIONS	PCM1717E MIN	PCM1717E TYP	PCM1717E MAX	UNITS
RESOLUTION		16		18	Bits
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Input Logic Level:					
V_{IH}(2)		70% of V_{DD}			V
V_{IL}(2)				30% of V_{DD}	V
V_{IH}(3)		70% of V_{DD}			V
V_{IL}(3)				30% of V_{DD}	V
V_{IH}(4)		64% of V_{DD}			V
V_{IL}(4)				28% of V_{DD}	V
Input Logic Current:					
I_{IH}(5)				–1	µA
I_{IL}(5)				120	µA
I_{IH}(6)				–1	µA
I_{IL}(6)				0.02	µA
I_{IH}(4)	V_{IN} = 3.2V			40	µA
I_{IL}(4)	V_{IN} = 1.4V			–40	µA
Output Logic Level:					
V_{OH}(7)	I_{OH} = –5mA	3.8			V
V_{OL}(7)	I_{OL} = +5mA			1.0	V
V_{OL}(8)	I_{OL} = +5mA			1.0	V
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mismatch Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2 V_{CC} at Bipolar Zero		±30		mV
DYNAMIC PERFORMANCE(1)	V_{CC} = +5V, f_{IN} = 991Hz				
THD+N at FS (0dB)			–90	–80	dB
THD+N at –60dB			–34		dB
Dynamic Range	EIAJ, A-weighted	90	96		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	92	100		dB
Channel Separation		90	97		dB
Level Linearity Error (–90dB)			±0.5		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple	Normal Mode			±0.17	dB
Stop Band Attenuation	Normal Mode	–35			dB
Pass Band	Normal Mode			0.445	fs
Stop Band	Normal Mode	0.555			fs
De-emphasis Error	(f_S = 32kHz ~ 48kHz)	–0.2		+0.55	dB
Delay Time (Latency)			22.25 ÷ fs		sec
ANALOG OUTPUT					
Voltage Range	FS (0dB) OUT, V_{CC} = +5V		62% of V_{CC}		Vp-p
Load Impedance		5			kΩ
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: +V_{CC}		+4.5		+5.5	VDC
+V_{DD}		+4.5		+5.5	VDC
Supply Current: +I_{CC} +I_{DD}(9)	+V_{CC} = +V_{DD} = +5V		18.0	25.0	mA
Power Dissipation	+V_{CC} = +V_{DD} = +5V		90	125	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting. (2) Pins 4, 5, 6, 14: LRCIN, DIN, BCKIN, MODE. (3) Pins 15, 16, 17, 18: RSTB, MD/DM0, MC/DM1, ML/MUTE (Schmitt trigger input). (4) Pin 1: XTI. (5) Pins 15, 16, 17, 18: RSTB, MD/DM0, MC/DM1, ML/MUTE (if pull-up resistor is used). (6) Pins 4, 5, 6: LRCIN, DIN, BCKIN (if pull-up resistor is not used). (7) Pin 19: CLKO. (8) Pin 7: ZERO. (9) No load on pins 19 (CLKO) and 20 (XTO).

PIN CONFIGURATION



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1717E	20-Pin SSOP	334-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	200mW
Operating Temperature Range	–25°C to +85°C
Storge Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

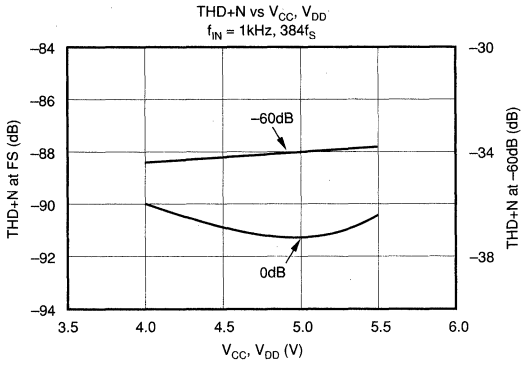
PIN ASSIGNMENTS

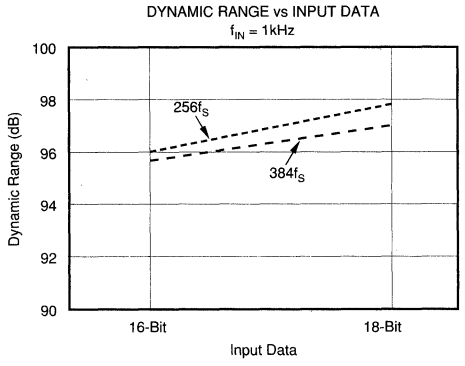
PIN	NAME	FUNCTION
Data Input Interface Pins		
4	LRCIN	Sample Rate Clock Input. Controls the update rate (fs).
5	DIN	Serial Data Input. MSB first, right jus•ified (Sony format) or I²S (Philips). Contains a frame of 16- or 18-bit data.
6	BCKIN	Bit Clock Input. Clocks in the data present on DIN input.
Mode Control and Clock Signals		
1	XTI	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
14	MODE	Operation Mode Select. For Software Mode, tie Mode "HIGH". For Hardware Mode, tie Mode "LOW".
16	MD/DM0	Mode Control for Data Input or De-emphasis. When "HIGH" MD is selected, and a "LOW" selects DM0.
17	MC/DM1	Mode Control for BCKIN or De-emphasis. When "HIGH", MC is selected, and a "LOW" selects DM1.
18	ML/MUTE	Mode Control for Strobe Clock or Mute. When "HIGH", ML is selected, and a "LOW" selects mute.
19	CLKO	Buffered Output of Oscillator. Equivalent to XTI.
20	XTO	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 1) of the crystal oscillator. When using an external clock, leave XTO open.
Operational Controls and Flags		
7	ZERO	Infinite Zero Detection Flag, open drain output. When the zero detection feature is muting the output, ZERO is "LOW". When non-zero input data is present, ZERO is in a high impedance state. When the input data is continuously zero for 65.536 BCKIN cycles, zero will be low.
15	RSTB	Resets DAC operation with an active "LOW" pulse.
Analog Output Functions		
8	D/C_R	Right Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
9	$V_{OUT}R$	Right Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
12	$V_{OUT}L$	Left Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
13	D/C_L	Left Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
Power Supply Connections		
2	DGND	Digital Ground.
3	V_{DD}	Digital Power Supply (+5V).
10	AGND	Analog Ground.
11	V_{CC}	Analog Power Supply (+3V).

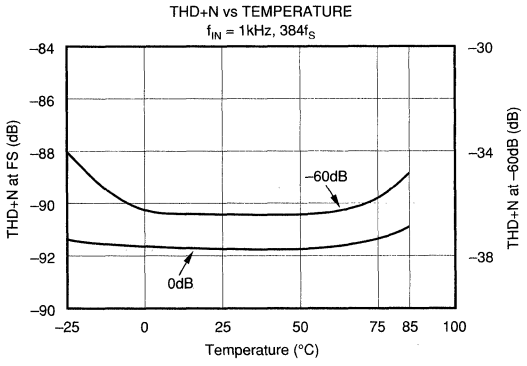
TYPICAL PERFORMANCE CURVES

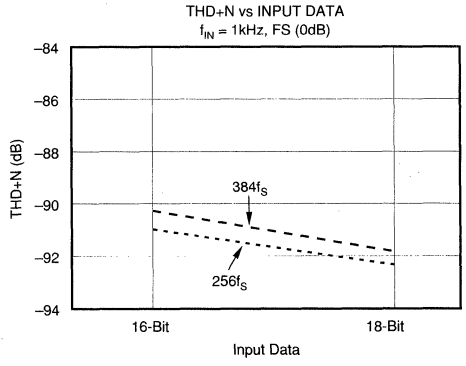
At T_A = +25°C, V_S = +5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 402Ω, unless otherwise noted.

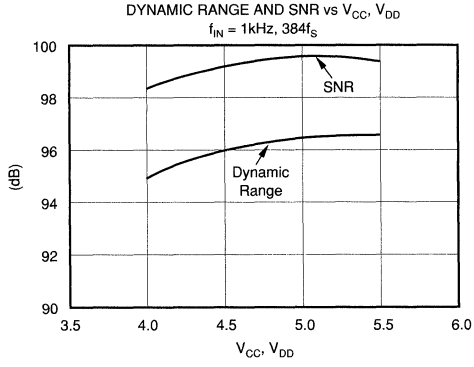
DYNAMIC PERFORMANCE









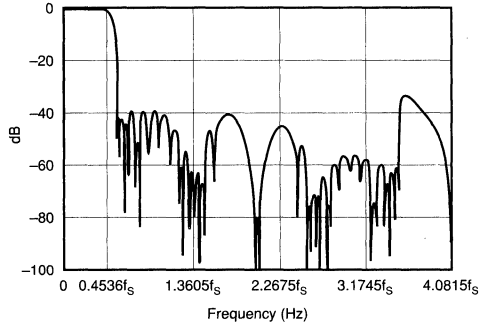


TYPICAL PERFORMANCE CURVES

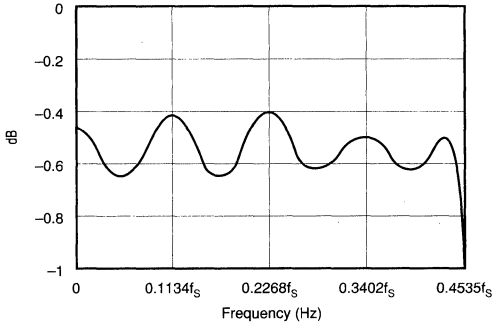
At T_A = +25°C, V_S = +5V, R_L = 44.1kHz, f_{SYS} = 384f_S, and 16-bit input data, unless otherwise noted.

DIGITAL FILTER

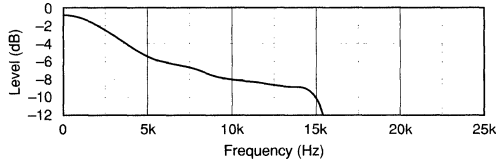
OVERALL FREQUENCY CHARACTERISTIC



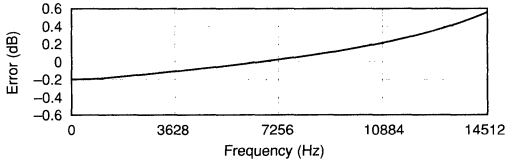
PASSBAND RIPPLE CHARACTERISTIC



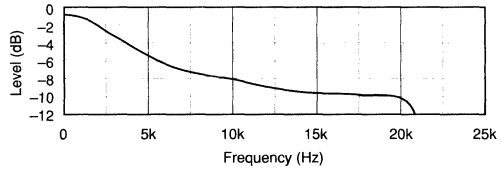
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



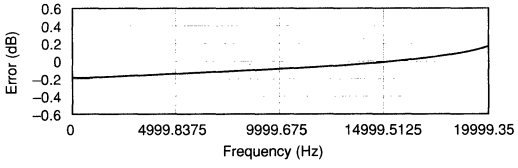
DE-EMPHASIS ERROR (32kHz)



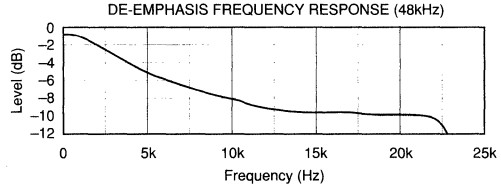
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



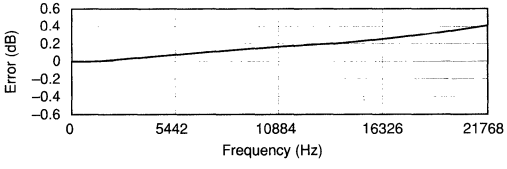
DE-EMPHASIS ERROR (44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



DE-EMPHASIS ERROR (48kHz)



SYSTEM CLOCK

The system clock for PCM1717 must be either 256fs or 384fs, where fs is the audio sampling frequency (typically 32kHz, 44.1kHz, or 48kHz). The system clock is used to operate the digital filter and the modulator.

The system clock can be either a crystal oscillator placed between XTI (pin 1) and XTO (pin 20), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1717 has a system clock detection circuit which automatically senses if the system clock is operating at 256fs or 384fs. The system clock should be synchronized with LRCIN (pin 4) clock. LRCIN (left-right clock) operates at the sampling frequency fs. In the event these clocks are not synchronized, PCM1717 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6 bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1717 on pins 4, 5, and 6—LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1717 can accept both normal and I²S data formats. Normal data format is MSB first, two's complement, right-justified. I²S data is compatible with Philips serial data protocol. In the I²S format, the data is 16- or 18-bit, selectable by bit 0 on Register 3 (Software Control Mode). In the Hardware Mode, PCM1717 can only function with 16-bit normal data. Figures 3 through 7 illustrate timing and input formats.

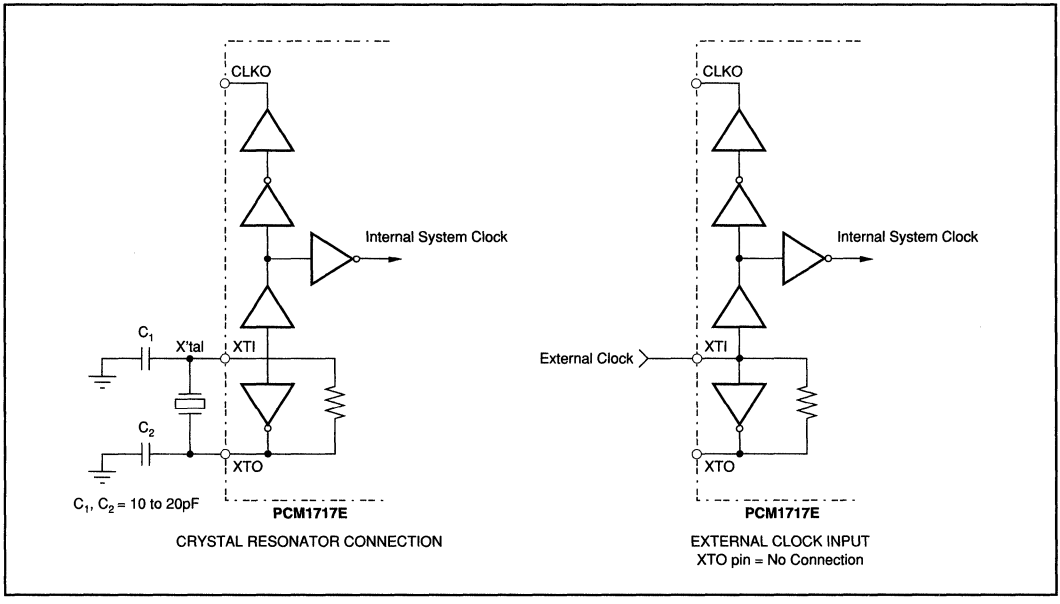
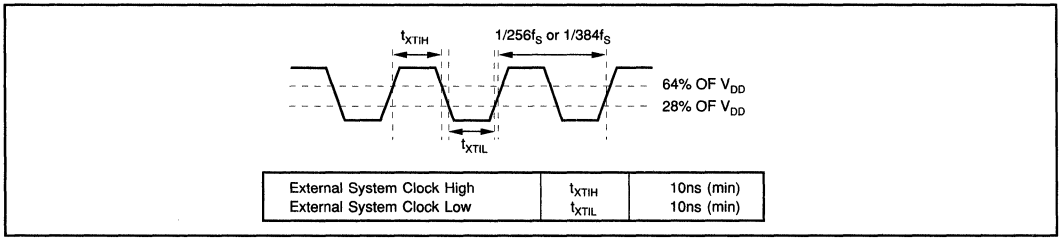


FIGURE 1. Internal Clock Circuit Diagram and Oscillator Connection.



External System Clock High	t_{XTIH}	10ns (min)
External System Clock Low	t_{XTIL}	10ns (min)

FIGURE 2. External Clock Timing Requirements.

OPERATIONAL CONTROL

PCM1717 can be controlled in two modes. Software Mode allows the user to control operation with a 16-bit serial register. Hardware Mode allows the user to hard-wire operation of PCM1717 using four parallel wires. The MODE pin determines which mode PCM1717 is in; a LOW level on pin 14 places PCM1717 in Hardware Mode, and a HIGH on pin 14 places PCM1717 in Software Mode.

MODE (Pin 14)	Selected Mode	Pin 16	Pin 17	Pin 18
"HIGH"	Software Mode	MD	MC	ML
"LOW"	Hardware Mode	DM0	DM1	MUTE

Table I indicates which functions are selectable within the user's chosen mode. All of the functions shown are selectable in the Software Mode, but only soft mute and de-emphasis control may be selected in the Hardware Mode.

FUNCTION	SOFTWARE MODE SELECTABLE	DEFAULT	HARDWARE MODE SELECTABLE	DEFAULT
Input Data Format	Yes		No	
Normal Format		Normal	Normal Only	Normal
I^2S Format				
Input Resolution	Yes		No	
16 Bits		16 Bits	16 Bits Only	16 Bits
18 Bits				
LRCIN Polarity	Yes		No	
L/R = High/Low		L/R = H/L	L/R = H/L	L/R = H/L
L/R = Low/High			Only	
De-emphasis Control	Yes		Yes	
32kHz				
44.1kHz		OFF		OFF
48kHz				
OFF				
Soft Mute	Yes	OFF	Yes	OFF
Digital Attenuation	Yes	0dB	No	0dB
Analog Output Mode	Yes	Stereo	No	Stereo
Infinite Zero Detection	Yes	Disabled	No	Disabled
DAC Operation Control	Yes	ON	No	ON

TABLE I. Feature Selections by Mode.

HARDWARE MODE

(Pin 14 = "0")

This mode is controlled by logic levels present on pins 15, 16, 17 and 18. Hardware Mode allows for control of soft mute, digital de-emphasis and disable ONLY. Other functions such as attenuation, I/O format and infinite zero detect can only be controlled in the Software Mode.

SOFT MUTE (Pin 18)

A LOW level on pin 18 will force both channels to be muted; a HIGH level on pin 18 will allow for normal operation.

DIGITAL DE-EMPHASIS (Pins 16 and 17)

Pins 16 and 17 are used as a two-bit parallel register to control de-emphasis modes:

PIN 16	PIN 17	MODE
0	0	De-emphasis disabled
1	0	De-emphasis enabled at 48kHz
0	1	De-emphasis enabled at 44.1kHz
1	1	De-emphasis enabled at 32kHz

RESET MODE (Pin 15)

A LOW level on pin 15 will force the digital filters, modulators and mode controls into a reset (disable) mode. While this pin is held low, the output of PCM1717 will be forced to $V_{CC}/2$ (Bipolar Zero). Bringing pin 15 HIGH will initialize all DAC functions, and allow for normal operation.

SOFTWARE MODE

(Pin 14 = "1")

The Software Mode uses a three-wire interface on pins 16, 17 and 18. Pin 17 (MC) is used to clock in the serial control data, pin 18 (ML) is used to synchronize the serial control data, and pin 16 (MD) is used to latch in the serial control register. There are four distinct registers, with bits 9 and 10 (of 16) determining which register is in use.

REGISTER CONTROL (Bits 9, 10)

REGISTER	B9 (A0)	B10 (A1)
0	0	0
1	1	0
2	0	1
3	1	1

Control data timing is shown in Figure 6. ML is used to latch the data from the control registers. After each register's contents are checked in, ML should be taken low to latch in the data. A "res" in the register indicates that location is reserved for factory use. When loading the registers, the "res" bits should be set LOW.

REGISTER 0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0-7 (AL0-AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20\log_{10} (ATT\_DATA/255)]\ dB$$

ATTENUATION DATA LOAD CONTROL, LCH

Bit 8 (LDL) is used to simultaneously set analog outputs of Lch and Rch. An output level is controlled by AL[0:7] attenuation data when this bit is set to 1. When set to 0, an output level is not controlled and remained at the previous attenuation level. A LDR bit in Register 1 has an equivalent function as the LDL. When one of LDL or LDR is set to 1, the output level of the left and right channel is simultaneously controlled. The attenuation level is given by:

ATT = 20log (y/256) (dB), where y = x, when $0 \le x \le 254$

y = x + 1, when x = 255

X is the user-determined step number, an integer value between 0 and 255.

Example:

let x = 255

$$ATT = 20\log\left(\frac{255+1}{256}\right) = 0dB$$

let x = 254

$$ATT = 20\log\left(\frac{254}{256}\right) = -0.068dB$$

let x = 1

$$ATT = 20\log\left(\frac{1}{256}\right) = -48.16dB$$

let x = 0

$$ATT = 20\log\left(\frac{0}{256}\right) = -\infty$$

REGISTER 1

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0-7 (AR0-AR7) control the level of attenuation.

REGISTER 2

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	res	res	res	res	IZD	OPE	DM1	DM0	MUTE

Register 2 is used to control soft mute, digital de-emphasis, disable, and infinite zero detect. Bit 0 is used for soft mute; a HIGH level on bit 0 will cause the output to be muted. Bits 1 and 2 are used to control digital de-emphasis as shown below:

BIT 1 (DM0)	BIT 2 (DM1)	DE-EMPHASIS
0	0	De-emphasis disabled
1	0	De-emphasis enabled at 48kHz
0	1	De-emphasis enabled at 44.1kHz
1	1	De-emphasis enabled at 32kHz

Bits 3 (OPE) and 4 (IZD) are used to control the infinite zero detection features. Tables II through IV illustrate the relationship between IZD, OPE, and RSTB (reset control):

	DATA INPUT	DAC OUTPUT
IZD = 1	Zero	Forced to BPZ(1)
	Other	Normal
IZD = 0	Zero	Zero(2)
	Other	Normal

TABLE II. Infinite Zero Detection (IZD) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
OPE = 1	Zero	Forced to BPZ(1)	Enabled
	Other	Forced to BPZ(1)	Enabled
OPE = 0	Zero	Controlled by IZD	Enabled
	Other	Normal	Enabled

TABLE III. Output Enable (OPE) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
RSTB = "HIGH"	Zero	Controlled by OPE and IZD	Enabled
	Other	Controlled by OPE and IZD	Enabled
RSTB = "LOW"	Zero	Forced to BPZ(1)	Disabled
	Other	Forced to BPZ(1)	Disabled

TABLE IV. Reset (RSTB) Function.

NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier. (2) $\Delta\Sigma$ is connected to output amplifier.

OPE controls the operation of the DAC: when OPE is "LOW", the DAC will convert all non-zero input data. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will only be forced to zero only if IZD is "HIGH". When OPE is "HIGH", the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IZD controls the operation of the zero detect feature: when IZD is "LOW", the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is "HIGH", the zero detect feature is enabled. If the input data is continuously zero for 65,536 cycle of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1717 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

REGISTER 3

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	res	PL3	PL2	PL1	PL0	ATC	IW	LRP	IIS

Register 3 is used to select the I/O data formats. Bit 0 (IIS) is used to control the input data format. If the input data source is normal (16- or 18-bit, MSB first, right-justified), set bit 0 "LOW". If the input format is IIS, set bit 0 "HIGH".

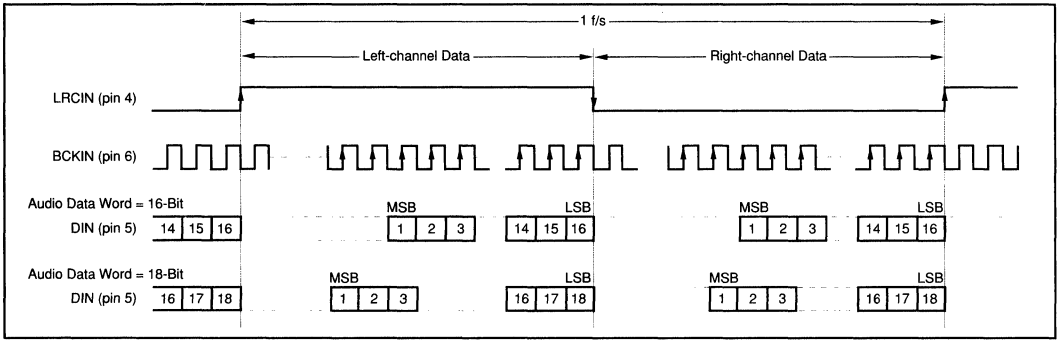


FIGURE 3. "Normal" Data Input Timing.

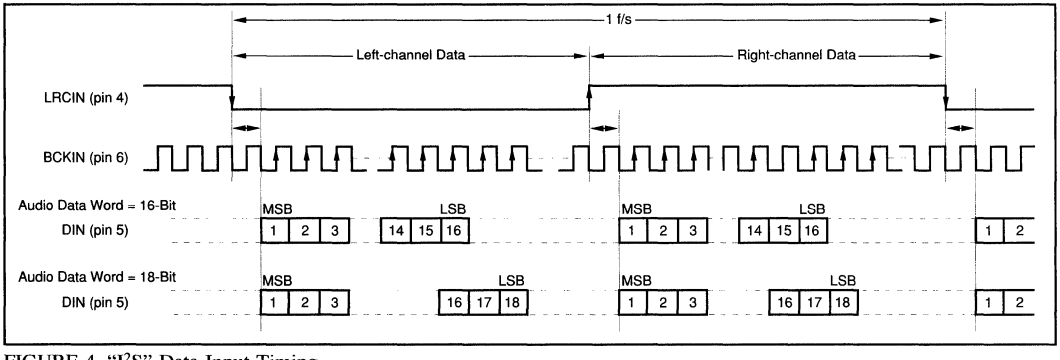
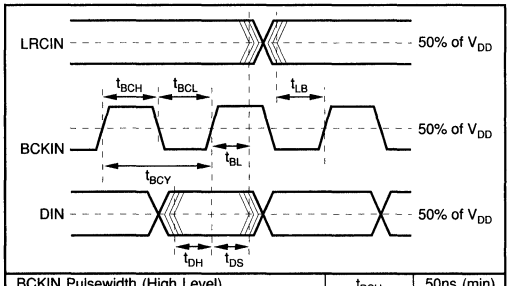


FIGURE 4. "I²S" Data Input Timing.



BCKIN Pulsewidth (High Level)	t_{BCH}	50ns (min)
BCKIN Pulsewidth (Low Level)	t_{BCL}	50ns (min)
BCKIN Pulse Cycle Time	t_{BCY}	100ns (min)
BCKIN Rising Edge → LRCIN Edge	t_{BL}	30ns (min)
LRCIN Edge → BCKIN Rising Edge	t_{LB}	30ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)

FIGURE 5. Data Input Timing.

Bit 1 is used to select the polarity of LRCIN (sample rate clock). When bit 1 is LOW, a HIGH state on LRCIN is used for the left channel, and a LOW state on LRCIN is used for the right channel. When bit 1 is HIGH the polarity of LRCIN is reversed.

Bit 2 is used to select the input word length. When bit 2 is LOW, the input word length is set for 16 bits; when bit 2 is HIGH, the input word length is set for 18 bits.

Bit 3 is used as an attenuation control. When bit 3 is set HIGH, the attenuation data on Register 0 is used for both channels, and the data in Register 1 is ignored. When bit 3 is LOW, each channel has separate attenuation data.

Bits 4 through 7 are used to determine the output format, as shown in Table V:

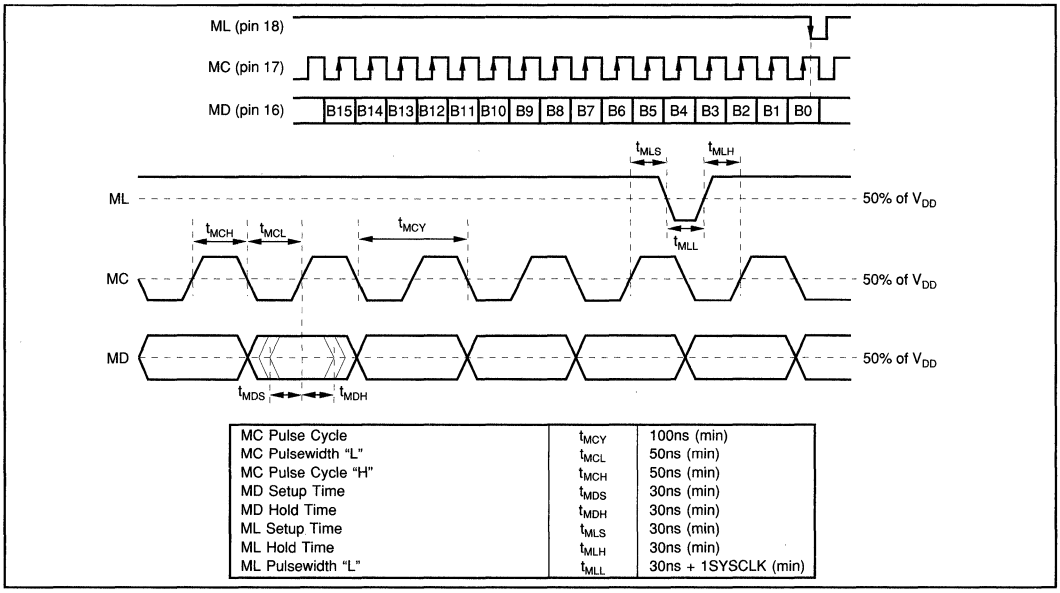
PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE V. PCM1717 Output Mode Control.

REGISTER RESET STATES

After reset, each register is set to a predetermined state:

Register 0	0000 0000 1111 1111
Register 1	0000 0001 1111 1111
Register 2	0000 0010 0000 0110
Register 3	0000 0011 1001 0000



MC Pulse Cycle	t_{MCY}	100ns (min)
MC Pulsewidth "L"	t_{MCL}	50ns (min)
MC Pulse Cycle "H"	t_{MCH}	50ns (min)
MD Setup Time	t_{MDS}	30ns (min)
MD Hold Time	t_{MDH}	30ns (min)
ML Setup Time	t_{MLS}	30ns (min)
ML Hold Time	t_{MLH}	30ns (min)
ML Pulsewidth "L"	t_{MLL}	30ns + 1SYSCLK (min)

FIGURE 6. Control Data Timing in Software Mode Control.

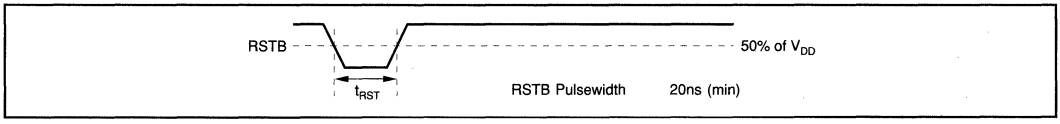


FIGURE 7. External Reset Timing.

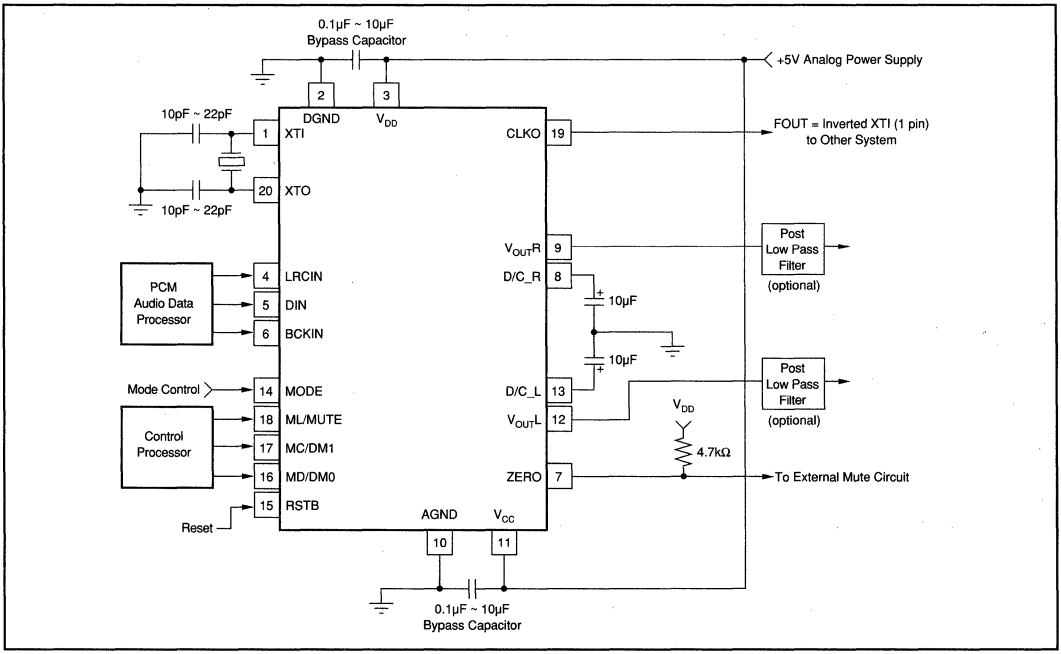


FIGURE 8. Typical Connection Diagram of PCM1717.

POWER SUPPLY CONNECTIONS

PCM1717 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 9.

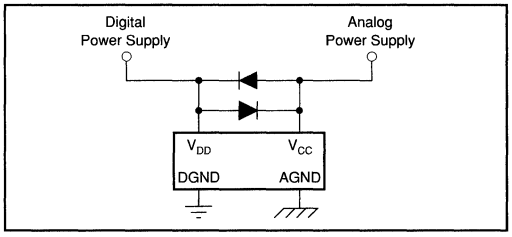


FIGURE 9. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 8 for optimal values of bypass capacitors.

THEORY OF OPERATION

The delta-sigma section of PCM1717 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 10. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $48f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 11.

Multi Level Delta Sigma

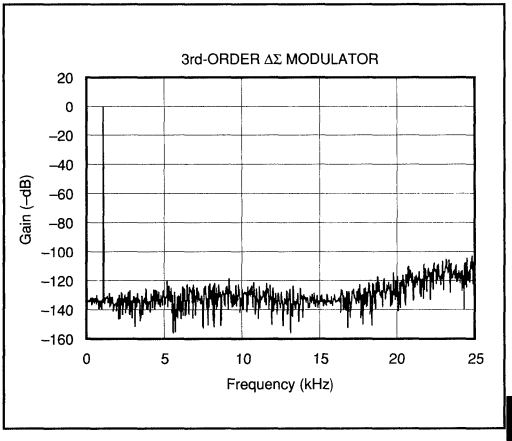


FIGURE 11. Quantization Noise Spectrum.

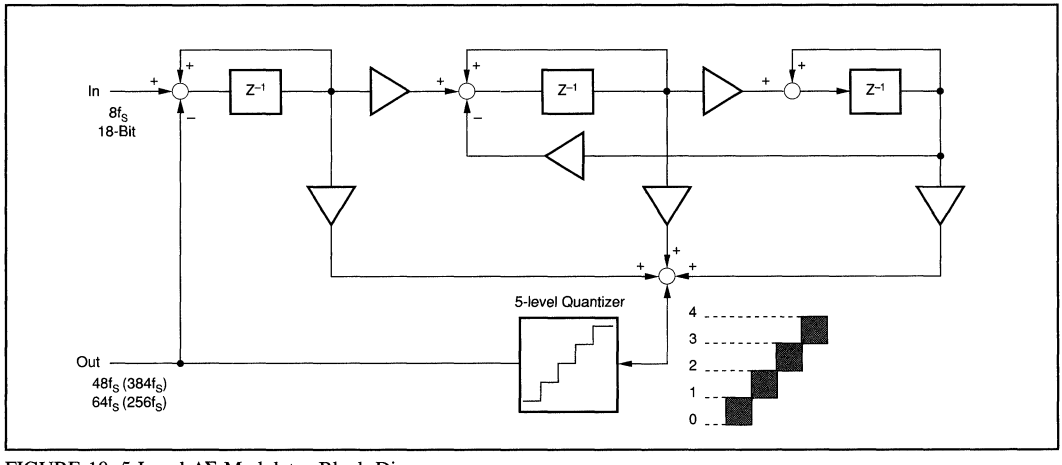


FIGURE 10. 5-Level ΔΣ Modulator Block Diagram.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1717:

$$T_D = 22.25 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 22.25/44.1kHz = 502.8μs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

INTERNAL RESET

When power is first applied to PCM1717, an automatic reset function occurs after 1,024 cycles of XTI clock. Refer to Table I for default conditions. During the first 1,024 cycles of XTI clock, PCM1717 cannot be programmed (Software Control). Data can be loaded into the control registers during this time, and after 1,204 cycles of XTI clock, a "LOW" on ML (pin 18) will initiate programming.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1717 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 12. The higher frequency rolloff of the filter is shown in Figure 13. If the user's application has the PCM1717 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 14. For some applications, a passive RC filter or 2nd-order filter may be adequate.

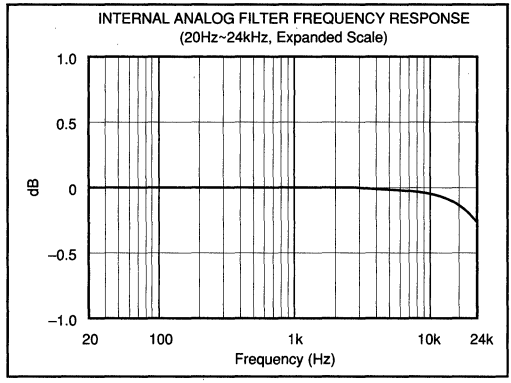


FIGURE 12. Low Pass Filter Frequency Response.

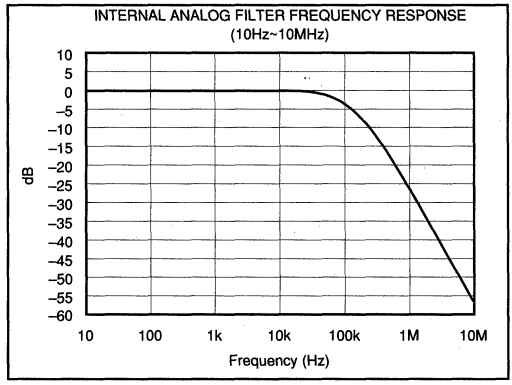


FIGURE 13. Low Pass Filter Frequency Response.

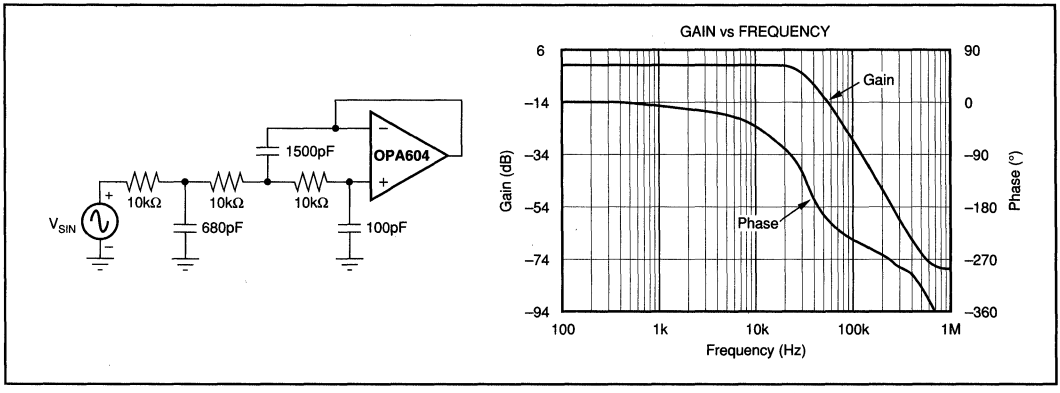


FIGURE 14. 3rd-Order LPF.

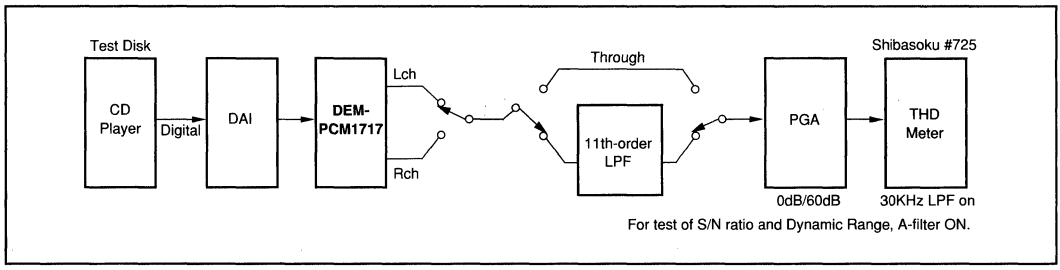


FIGURE 15. Test Block Diagram.

TEST CONDITIONS

Figure 15 illustrates the actual test conditions applied to PCM1717 in production. The 11th-order filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the 3rd-order filter shown in Figure 14 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –89dB when the external 20kHz 11th-order filter is used.

EVALUATION FIXTURES

Three evaluation fixtures are available for PCM1717.

DEM-PCM1717

This evaluation fixture is primarily intended for quick evaluation of the PCM1717's performance. DEM-PCM1717 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1717 does not contain a receiver chip or an external low pass filter. DEM-PCM1717 requires a single +5V power supply.

OUT-OF-BAND NOISE CONSIDERATIONS

Delta-sigma DACs are by nature very sensitive to jitter on the master clock. Phase noise on the clock will result in an increase in noise, ultimately degrading dynamic range. It is difficult to quantify the effect of jitter due to problems in synthesizing low levels of jitter. One of the reasons delta-sigma DACs are prone to jitter sensitivity is the large quantization noise when the modulator can only achieve two discrete output levels (0 or 1). The multi-level delta-sigma DAC has improved theoretical SNR because of multiple output states. This reduces sensitivity to jitter. Figure 16 contrasts jitter sensitivity between a one-bit PWM type DAC and multi-level delta-sigma DAC. The data was derived using a simulator, where clock jitter could be completely synthesized.

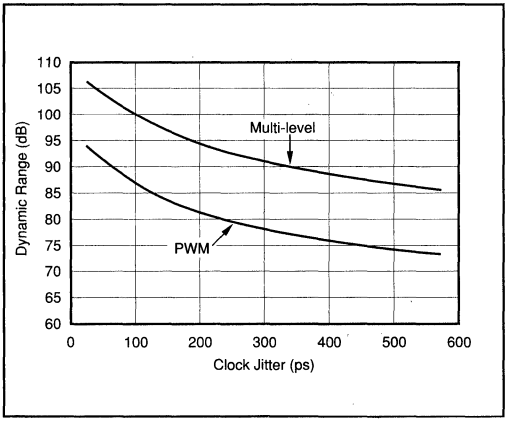


FIGURE 16. Simulation Results of Clock Jitter Sensitivity.

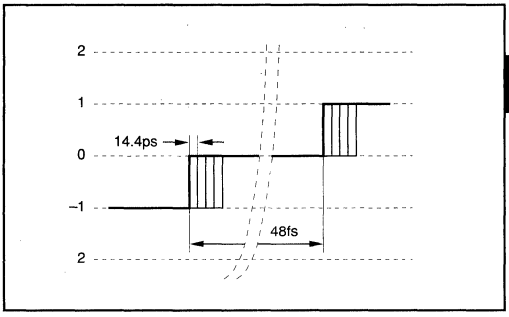


FIGURE 17. Simulation Method for Clock Jitter.

BURR-BROWN®

PCM1718E

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

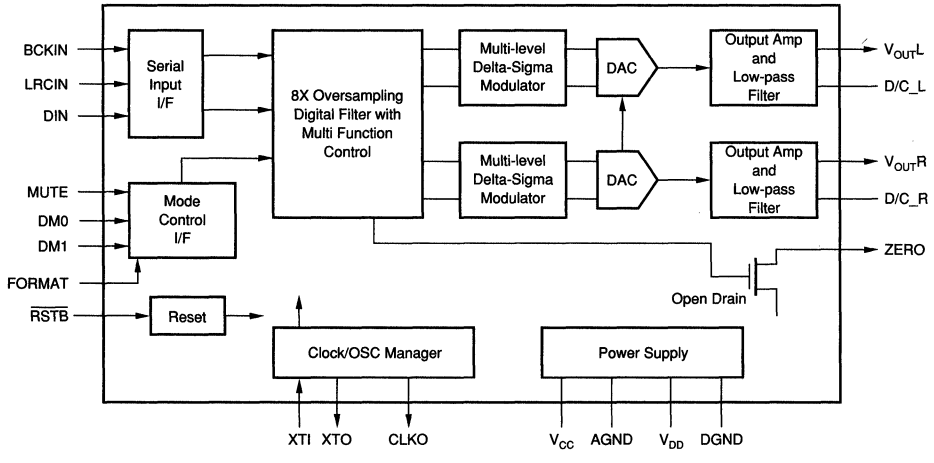
- **ACCEPTS 16- or 18-BIT I²S, OR 18-BIT NORMAL INPUT DATA**
- **COMPLETE STEREO DAC:**
  8X Oversampling Digital Filter
  Multi-Level Delta-Sigma DAC
  Analog Low Pass Filter
  Output Amplifier
- **HIGH PERFORMANCE:**
  –90dB THD+N
  96dB Dynamic Range
  100dB SNR
- **SYSTEM CLOCK: 256fs or 384fs**
- **WIDE POWER SUPPLY: +2.7V to +5.5V**
- **SELECTABLE FUNCTIONS:**
  Soft Mute
  Digital De-emphasis
- **SMALL 20-PIN SSOP PACKAGE**

DESCRIPTION

The PCM1718 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1718 is fabricated on a highly advanced 0.6µ CMOS process. PCM1718 accepts 18-bit normal input data format, or 16- or 18-bit I²S data format.

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute and digital de-emphasis.

PCM1718 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size, and single power supply make it ideal for BS tuners, keyboards, MPEG audio, PCMCIA audio cards, MIDI applications, and set-top boxes.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

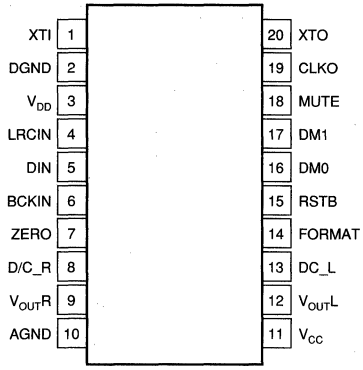
All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, and 18-bit input data, SYSCLK = 384fs, unless otherwise noted. Measurement bandwidth is 20kHz.

PARAMETER	CONDITIONS	PCM1718E MIN	PCM1718E TYP	PCM1718E MAX	UNITS
RESOLUTION		16		18	Bits
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Input Logic Level:					
V_{IH}(2)		70% of V_{DD}			V
V_{IL}(2)				30% of V_{DD}	V
V_{IH}(3)		70% of V_{DD}			V
V_{IL}(3)				30% of V_{DD}	V
V_{IH}(4)		64% of V_{DD}			V
V_{IL}(4)				28% of V_{DD}	V
Input Logic Current:					
I_{IH}(5)				–1	µA
I_{IL}(5)				120	µA
I_{IH}(6)				–1	µA
I_{IL}(6)				0.02	µA
I_{IH}(4)	V_{IN} = 3.2V			40	µA
I_{IL}(4)	V_{IN} = 1.4V			–40	µA
Output Logic Level:					
V_{OH}(7)	I_{OH} = –5mA	3.8			V
V_{OL}(7)	I_{OL} = +5mA			1.0	V
V_{OL}(8)	I_{OL} = +5mA			1.0	V
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mismatch Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2 V_{CC} at Bipolar Zero		±30		mV
DYNAMIC PERFORMANCE(1)	V_{CC} = +5V, f_{IN} = 991Hz				
THD+N at FS (0dB)			–90	–80	dB
THD+N at –60dB			–34		dB
Dynamic Range	EIAJ, A-weighted	90	96		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	92	100		dB
Channel Separation		90	97		dB
Level Linearity Error (–90dB)			±0.5		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple	Normal Mode			±0.17	dB
Stop Band Attenuation	Normal Mode	–35			dB
Pass Band	Normal Mode			0.445	fs
Stop Band	Normal Mode	0.555			fs
De-emphasis Error	(fs = 32kHz ~ 48kHz)	–0.2		+0.55	dB
Delay Time (Latency)			22.25 ÷ fs		sec
ANALOG OUTPUT					
Voltage Range	FS (0dB) OUT, V_{CC} = +5V		62% of V_{CC}		Vp-p
Load Impedance		5			kΩ
Center Voltage			50% of V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+2.7		+5.5	VDC
$+V_{DD}$		+2.7		+5.5	VDC
Supply Current: $+I_{CC}$ $+I_{DD}$(9)	$+V_{CC}$ = $+V_{DD}$ = +5V		18.0	25.0	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5V		90	125	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting. (2) Pins 4, 5, 6, 14: LRCIN, DIN, BCKIN, FORMAT. (3) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (Schmitt trigger input). (4) Pin 1: XTI. (5) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (if pull-up resistor is used). (6) Pins 4, 5, 6: LRCIN, DIN, BCKIN (if pull-up resistor is not used). (7) Pin 19: CLKO. (8) Pin 7: ZERO. (9) No load on pins 19 (CLKO) and 20 (XTO).

PIN CONFIGURATION

TOP VIEW — SSOP



PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1718E	20-Pin SSOP	334-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	200mW
Operating Temperature Range	–25°C to +85°C
Storge Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

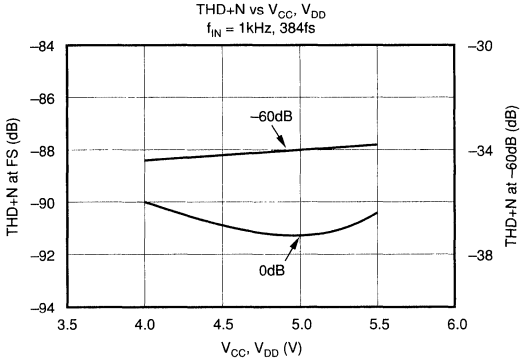
PIN ASSIGNMENTS

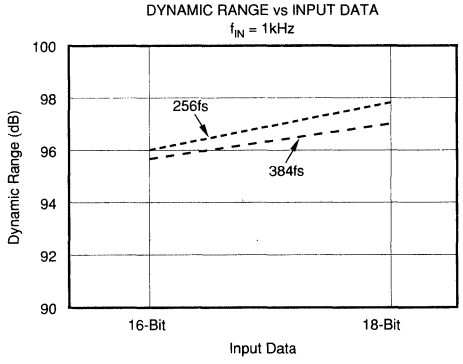
PIN	NAME	FUNCTION
Data Input Interface Pins		
4	LRCIN	Sample Rate Clock Input. Controls the update rate (fs).
5	DIN	Serial Data Input. MSB first, right justified (Sony format, 18 bits) or I²S (Philips format, 16 or 18 bits).
6	BCKIN	Bit Clock Input. Clocks in the data present on DIN input.
Mode Control and Clock Signals		
1	XTI	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
14	FORMAT	A "HIGH" selects I²S input data format, and a "LOW" selects Normal (Sony) input data format.
16	DM0	De-emphasis selection.
17	DM1	De-emphasis selection.
18	MUTE	Soft Mute Control. When set "LOW", the outputs are muted.
19	CLKO	Buffered Output of Oscillator. Equivalent to XTI.
20	XTO	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 1) of the crystal oscillator. When using an external clock, leave XTO open.
Operational Controls and Flags		
7	ZERO	Infinite Zero Detection Flag, open drain output. When the input is continuously zero for 65,536 cycles of BCKIN, ZERO is "LOW".
15	RSTB	Resets DAC operation with an active "LOW" pulse.
Analog Output Functions		
8	D/C_R	Right Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
9	$V_{OUT}R$	Right Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
12	$V_{OUT}L$	Left Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
13	D/C_L	Left Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
Power Supply Connections		
2	DGND	Digital Ground.
3	V_{DD}	Digital Power Supply (+5V or +3V).
10	AGND	Analog Ground.
11	V_{CC}	Analog Power Supply (+5V or +3V).

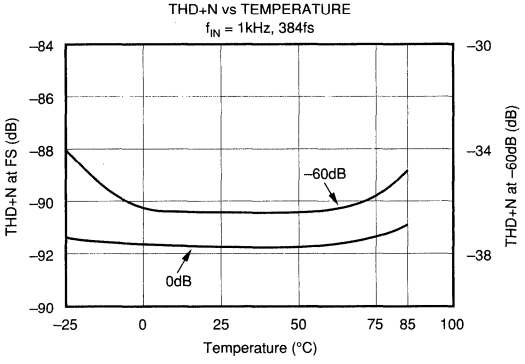
TYPICAL PERFORMANCE CURVES

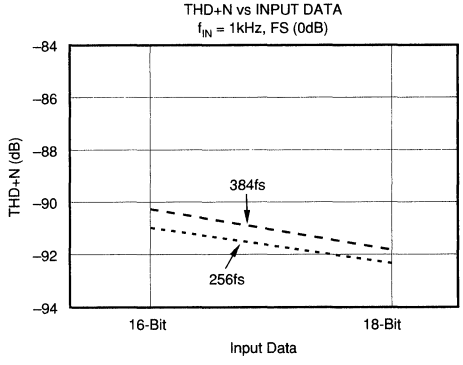
At T_A = +25°C, V_S = +5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 402Ω, unless otherwise noted.

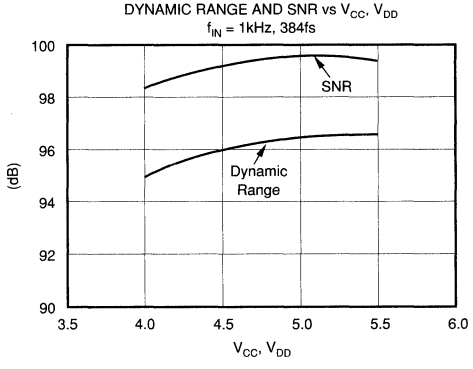
DYNAMIC PERFORMANCE







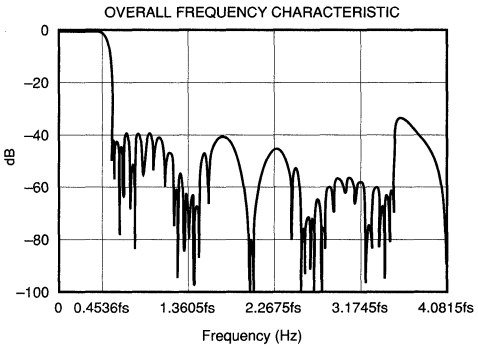


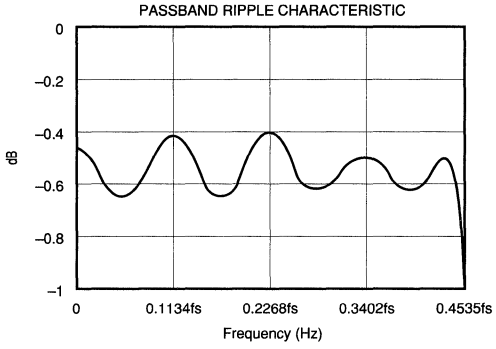


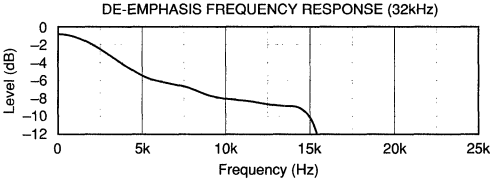
TYPICAL PERFORMANCE CURVES

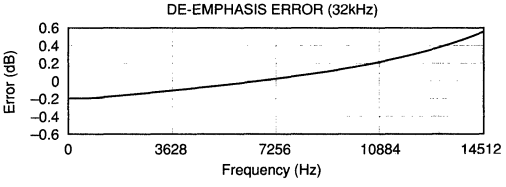
At T_A = +25°C, V_S = +5V, R_L = 44.1kHz, f_{SYS} = 384fs, and 18-bit input data, unless otherwise noted.

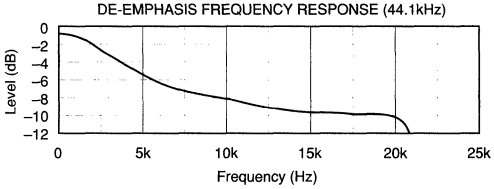
DIGITAL FILTER

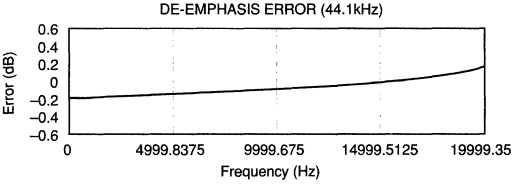


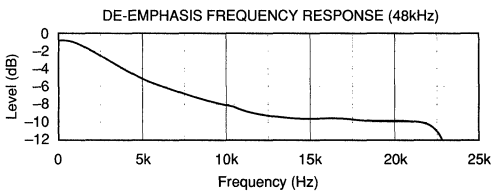


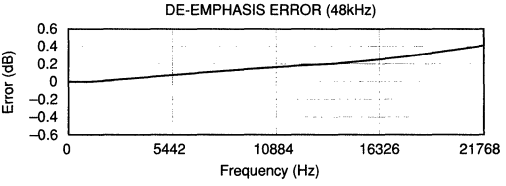












SYSTEM CLOCK

The system clock for PCM1718 must be either 256fs or 384fs, where fs is the audio sampling frequency (typically 32kHz, 44.1kHz, or 48kHz). The system clock is used to operate the digital filter and the modulator.

The system clock can be either a crystal oscillator placed between XTI (pin 1) and XTO (pin 20), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1718 has a system clock detection circuit which automatically senses if the system clock is operating at 256fs or 384fs. The system clock should be synchronized with LRCIN (pin 4) clock. LRCIN (left-right clock) operates at the sampling frequency fs. In the event these clocks are not synchronized, PCM1718 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6 bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1718 on pins 4, 5, and 6—LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1718 can accept both normal and I²S data formats. Normal data format is MSB first, two's complement, right-justified. I²S data is compatible with Philips serial data protocol. Figures 3 and 4 illustrate the input data formats.

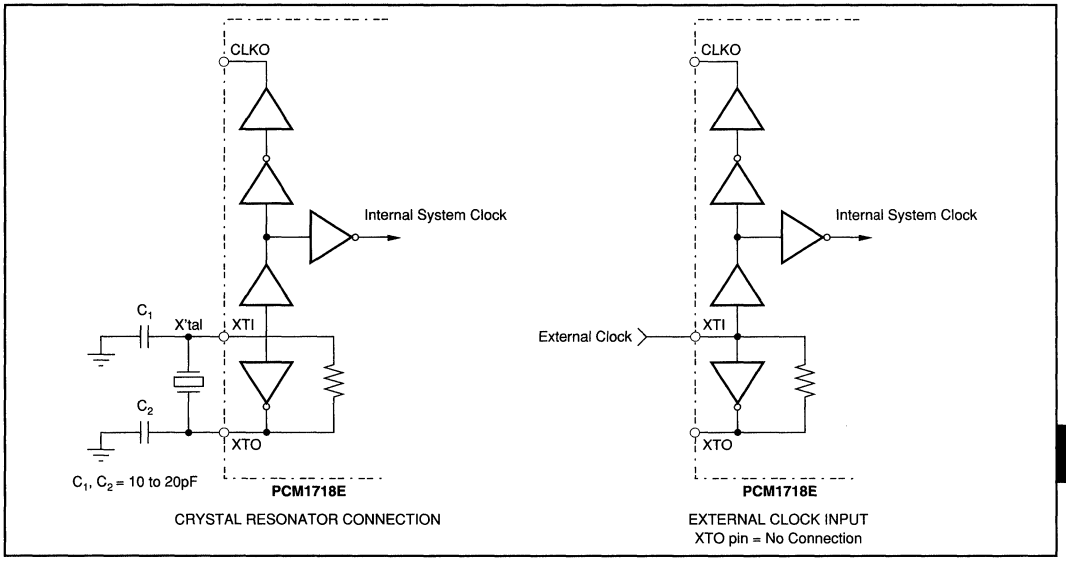
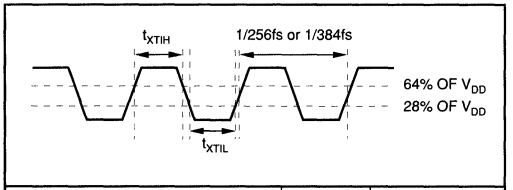


FIGURE 1. Internal Clock Circuit Diagram and Oscillator Connection.



External System Clock High	t_{XTIH}	10ns (min)
External System Clock Low	t_{XTIL}	10ns (min)

FIGURE 2. External Clock Timing Requirements.

FUNCTIONAL CONTROLS

PCM1718 allows the user to control the input data format, soft mute, and digital de-emphasis frequency. Table I illustrates the selectable functions:

FUNCTION	CONTROL PIN
Data Input Format Normal I²S	FORMAT (Pin 14)
De-emphasis 32kHz 44.1kHz 48kHz	DM0, DM1 (Pins 16, 17)
Soft Mute	MUTE (Pin 18)
Reset	RSTB (Pin 15)

TABLE I. Selectable Functions.

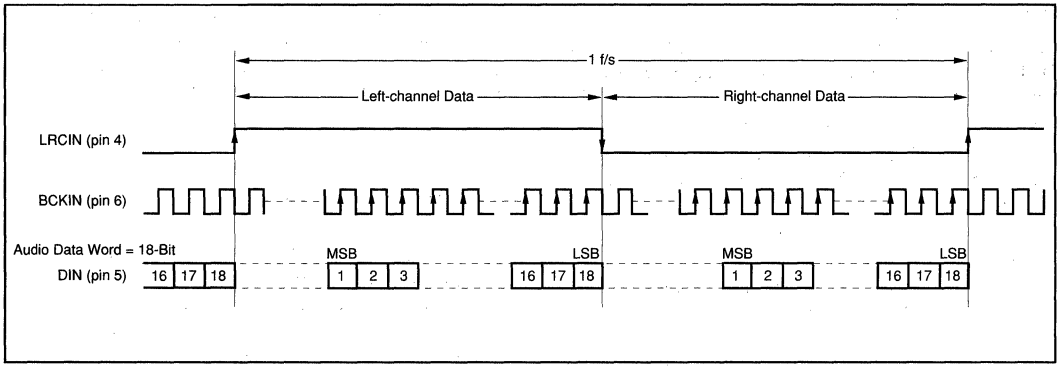


FIGURE 3. "Normal" Data Input Timing.

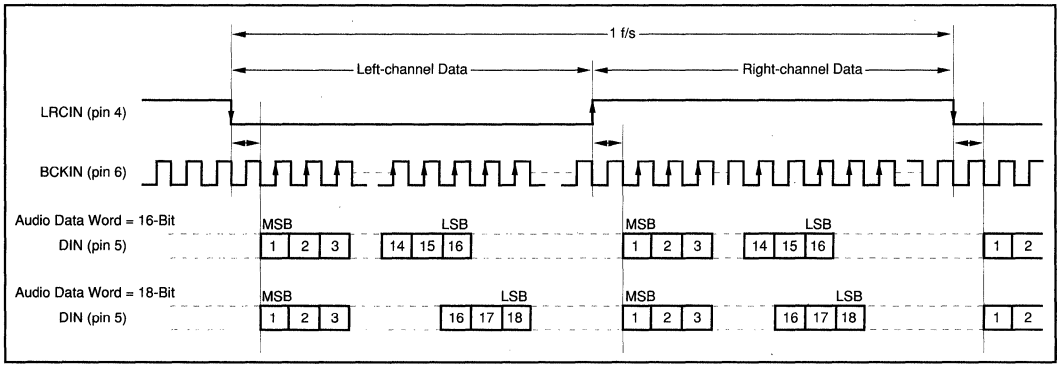
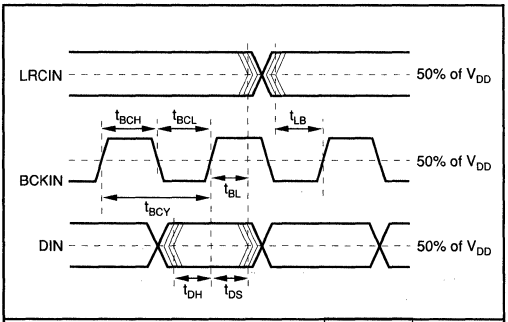


FIGURE 4. "I²S" Data Input Timing.



BCKIN Pulsewidth (High Level)	t_{BCH}	50ns (min)
BCKIN Pulsewidth (Low Level)	t_{BCL}	50ns (min)
BCKIN Pulse Cycle Time	t_{BCY}	100ns (min)
BCKIN Rising Edge → LRCIN Edge	t_{BL}	30ns (min)
LRCIN Edge → BCKIN Rising Edge	t_{LB}	30ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)

FIGURE 5. Data Input Timing.

Data Format

A "HIGH" on pin 14 (FORMAT) sets the input format to I²S, and a "LOW" sets the format to Normal (MSB-first, right-justified Sony format).

Soft Mute

A "LOW" on pin 18 (MUTE) causes both outputs to be muted. This muting is done in the digital domain so there is no audible "click" when the soft mute is enacted.

De-Emphasis

PCM1718 allows for digital de-emphasis for all three standard sampling frequencies:

DM1 (Pin 17)	DM0 (Pin 16)	De-Emphasis Mode
0	0	OFF
0	1	48kHz
1	0	44.1kHz
1	1	32kHz

Reset

PCM1718 has both internal power on reset circuit and the RSTB-pin (pin 15) which accepts external forced reset by RSTB = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 6 illustrates the timing of internal power on reset.

For the RSTB-pin, PSTB-pin accepts external forced reset by RSTB = L. During RSTB = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialize (1024 system clocks count after RSTB = H.) Figure 7 illustrates the timing of RSTB-pin reset.

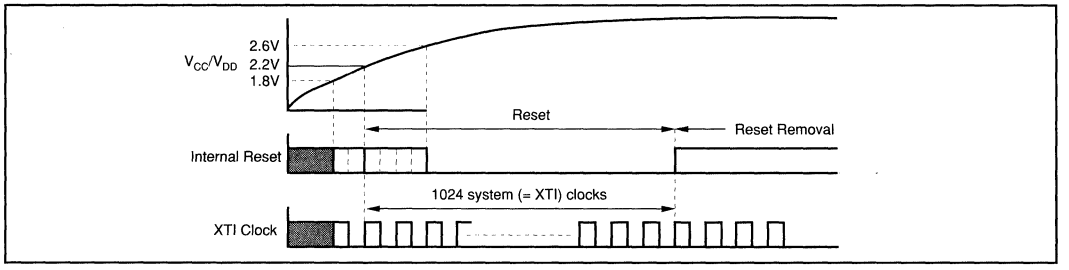


FIGURE 6. Internal Power-On Reset Timing.

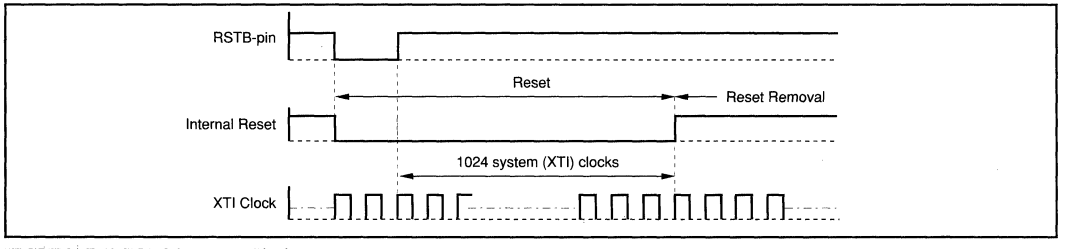


FIGURE 7. RSTB-Pin Reset Timing.

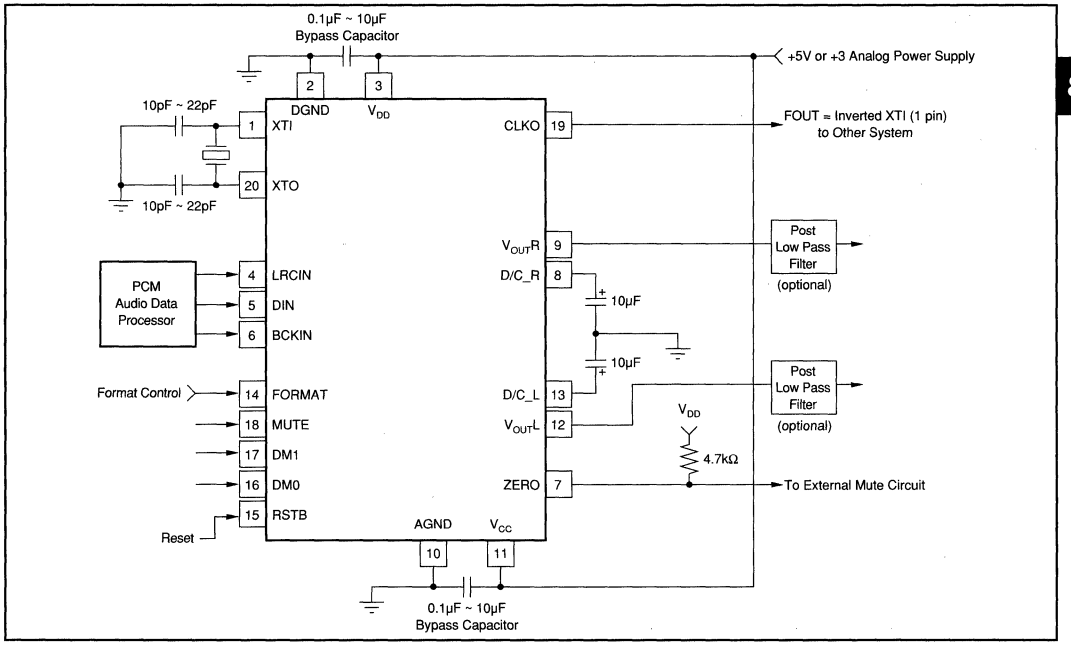


FIGURE 8. Typical Connection Diagram of PCM1718.

POWER SUPPLY CONNECTIONS

PCM1718 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 9.

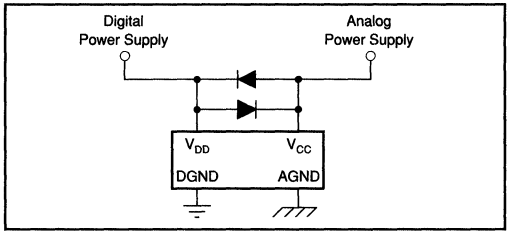


FIGURE 9. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 8 for optimal values of bypass capacitors.

THEORY OF OPERATION

The delta-sigma section of PCM1718 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 10. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is 48fs for a 384fs system clock, and 64fs for a 256fs system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 11.

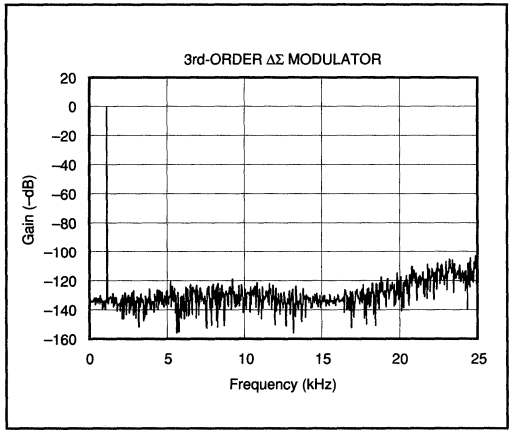


FIGURE 11. Quantization Noise Spectrum.

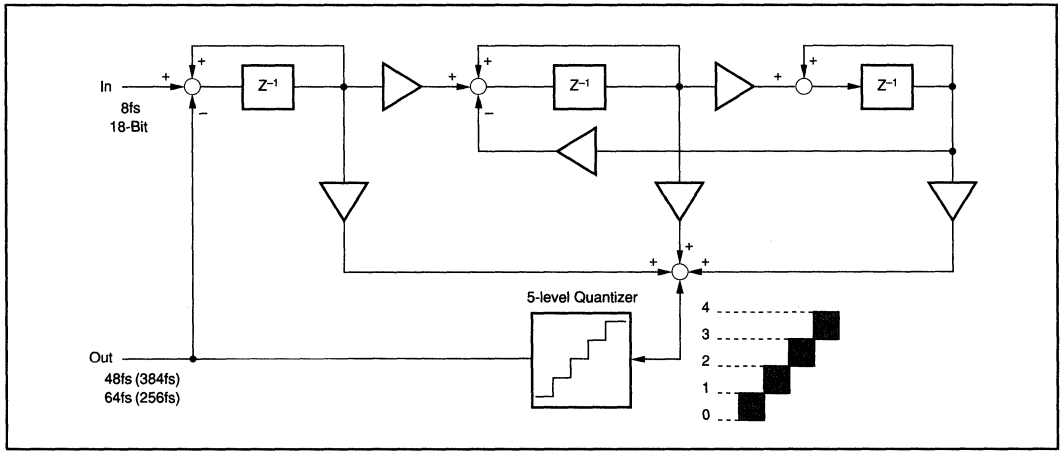


FIGURE 10. 5-Level ΔΣ Modulator Block Diagram.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1718:

$$T_D = 22.25 \times 1/fs$$

For fs = 44.1kHz, T_D = 22.25/44.1kHz = 502.8μs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1718 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 12. The higher frequency rolloff of the filter is shown in Figure 13. If the user's application has the PCM1718 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 14. For some applications, a passive RC filter or 2nd-order filter may be adequate.

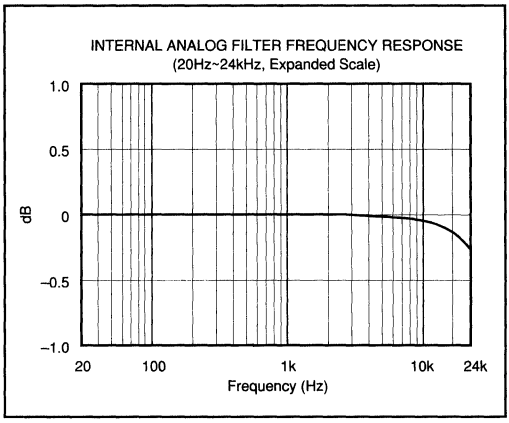


FIGURE 12. Low Pass Filter Frequency Response.

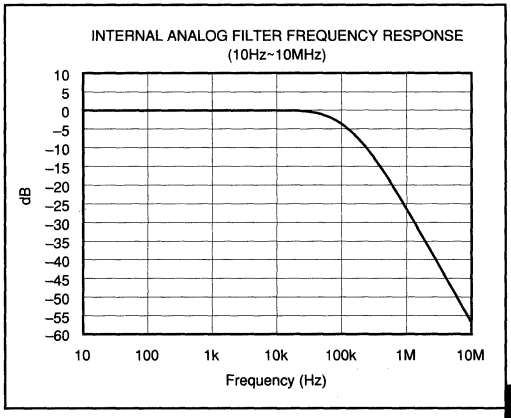


FIGURE 13. Low Pass Filter Frequency Response.

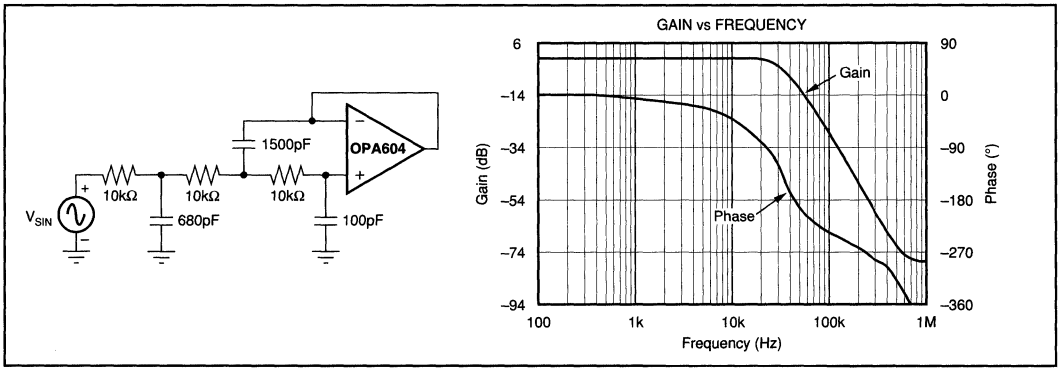


FIGURE 14. 3rd-Order LPF.

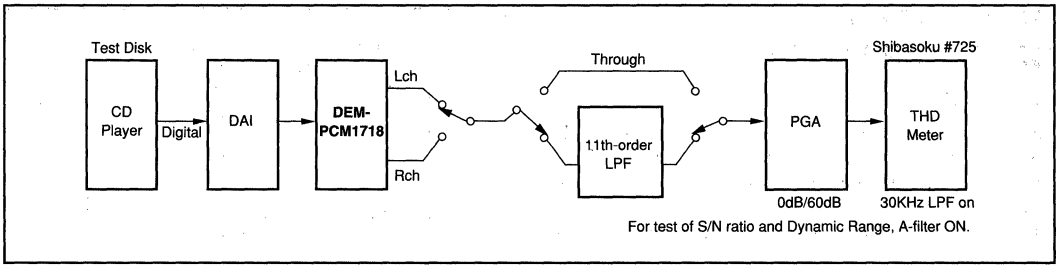


FIGURE 15. Test Block Diagram.

TEST CONDITIONS

Figure 15 illustrates the actual test conditions applied to PCM1718 in production. The 11th-order filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the 3rd-order filter shown in Figure 14 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –89dB when the external 20kHz 11th-order filter is used. For cost-sensitive applications, a single RC filter, as shown in Figure 18, may be adequate.

EVALUATION FIXTURES

DEM-PCM1718

This evaluation fixture is primarily intended for quick evaluation of the PCM1718's performance. DEM-PCM1718 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1718 does not contain a receiver chip or an external low pass filter. DEM-PCM1718 requires a single +2.7V to +5V power supply.

OUT-OF-BAND NOISE CONSIDERATIONS

Delta-sigma DACs are by nature very sensitive to jitter on the master clock. Phase noise on the clock will result in an increase in noise, ultimately degrading dynamic range. It is difficult to quantify the effect of jitter due to problems in synthesizing low levels of jitter. One of the reasons delta-sigma DACs are prone to jitter sensitivity is the large quantization noise when the modulator can only achieve two discrete output levels (0 or 1). The multi-level delta-sigma DAC has improved theoretical SNR because of multiple output states. This reduces sensitivity to jitter. Figure 16 contrasts jitter sensitivity between a one-bit PWM type DAC and multi-level delta-sigma DAC. The data was derived using a simulator, where clock jitter could be completely synthesized.

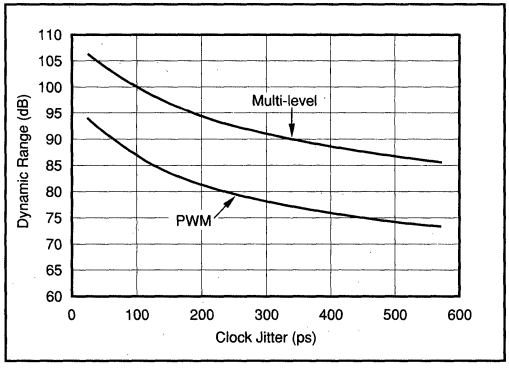


FIGURE 16. Simulation Results of Clock Jitter Sensitivity.

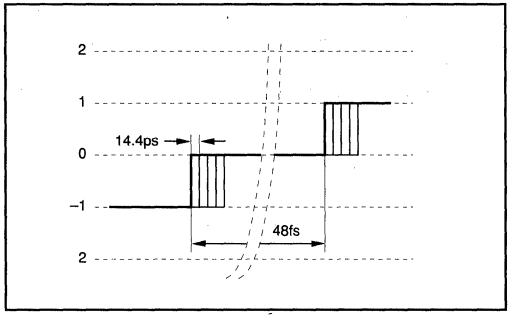


FIGURE 17. Simulation Method for Clock Jitter.

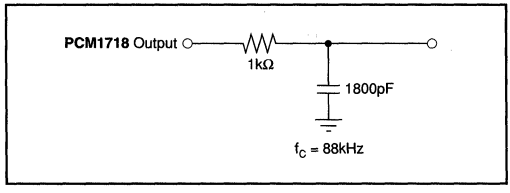


FIGURE 18. RC Output Filter.

BURR-BROWN®

PCM1721

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER WITH PROGRAMMABLE PLL

FEATURES

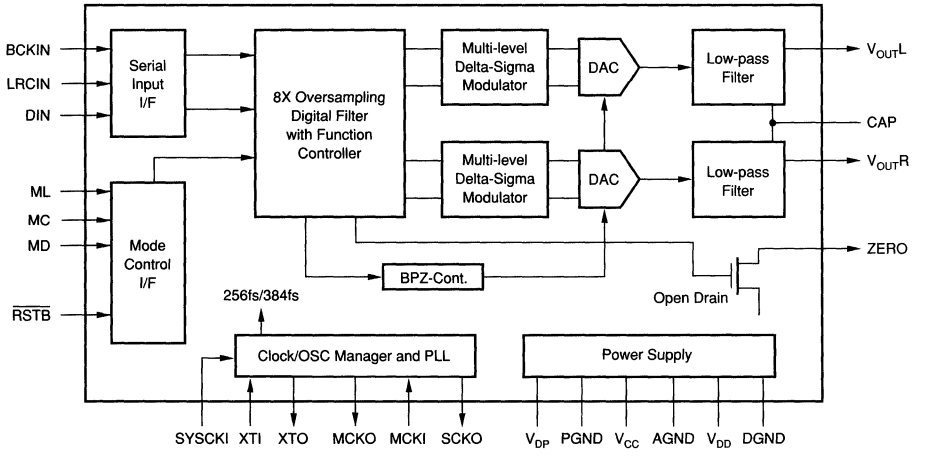
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 94dB
- MULTIPLE SAMPLING FREQUENCIES:
  16kHz, 22.05kHz, 24kHz
  32kHz, 44.1kHz, 48kHz
  64kHz, 88.2kHz, 96kHz
- PROGRAMMABLE PLL CIRCUIT:
  256fs/384fs from 27MHz Master Clock
- NORMAL OR I²S DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
  Soft Mute
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- OUTPUT MODE: Left, Right, Mono, Mute

DESCRIPTION

The PCM1721 is a complete low cost stereo audio digital-to-analog converter (DAC) with a phase-locked loop (PLL) circuit included. The PLL derives either 256fs or 384fs system clock from an external 27MHz reference frequency. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1721 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PLL can be programmed for sampling at standard digital audio frequencies as well as one-half and double sampling frequencies.

The PCM1721 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

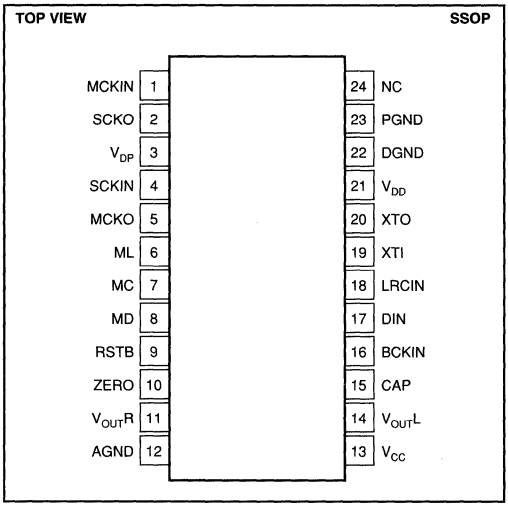
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 16-bit input data, SYSCLK = 384fs, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1721 MIN	PCM1721 TYP	PCM1721 MAX	UNITS
RESOLUTION		16		24	Bits
DATA FORMAT					
Audio Data Format			Standard/I²S		
Data Bit Length			16/20/24 Selectable		
Sampling Frequency (fs)	Standard fs	32	44.1	48	kHz
	One-half fs	16	22.05	24	kHz
	Double	64	88.2	96	kHz
Master Clock Input Frequency			27		MHz
Internal System Clock Frequency			256fs/384fs		
DIGITAL INPUT/OUTPUT LOGIC LEVEL			TTL		
DYNAMIC PERFORMANCE(1)					
THD+N at fs (0dB)	fs = 44.1kHz		–85		dB
	fs = 96kHz		TBD		dB
THD+N at –60dB	fs = 44.1kHz		–34		dB
	fs = 96kHz		TBD		dB
Dynamic Range	fs = 44.1kHz		94		dB
	fs = 96kHz		TBD		dB
Signal-to-Noise Ratio(2)	fs = 44.1kHz		98		dB
	fs = 96kHz		TBD		dB
Channel Separation	fs = 44.1kHz		94		dB
	fs = 96kHz		TBD		dB
DC ACCURACY					
Gain Error			±1.0		% of FSR
Gain Miss-Match, Channel-to-Channel			±1.0		% OF FSR
Gain Drift			±50		ppm of FSR/°C
Bipolar Zero Error			±20		mV
Bipolar Zero Drift			±20		ppm of FSR/°C
ANALOG OUTPUT					
Voltage Range			3.1		Vp-p
DIGITAL FILTER PERFORMANCE					
Passband			0.445fs		
Stopband			0.555fs		
Passband Ripple			±0.17		dB
Stopband Attenuation			–35		dB
Delay Time			22.25		1/fs
De-emphasis Error			+0.55/–0.2		dB
ANALOG FILTER PERFORMANCE					
Frequency Response	20 to 20kHz		TBD		dB
	20 to 40kHz		TBD		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	4.5	5	5.5	VDC
Supply Current: I_{CC}	V_{CC} = 5V		TBD		
I_{DD}	V_{DD} = 5V		TBD		
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (2) SNR is tested at Internal Infinity Zero Detection off.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	TYPE	FUNCTION
1	MCKIN	IN	Master Clock Input. Under normal conditions, this pin is connected to MCKO (pin 21).
2	SCKO	OUT	System Clock Out. This output is 256fs or 384fs system clock generated by the internal PLL.
3	V_{DP}	PWR	PLL Power Supply (+5V)
4	SCKIN	IN	System Clock (256fs or 384fs) Input. Under normal conditions, this pin is connected to SCKO (pin 24).
5	MCKO	OUT	Master Clock Output (27MHz)
6	ML	IN	Latch for serial control data
7	MC	IN	Clock for serial control data
8	MD	IN	Data for serial control
9	RSTB	IN	Reset Input. When this pin is low, the digital filters and modulators are held in reset.
10	ZERO	OUT	Zero Data Flag. This pin is low when the input data is continuously zero for more than 65, 535 cycles of BCKIN.
11	$V_{OUT}R$	OUT	Right Channel Analog Output
12	AGND	GND	Analog Ground
13	V_{CC}	PWR	Analog Power Supply (+5V)
14	$V_{OUT}L$	OUT	Left Channel Analog Output
15	CAP		Common pin for analog output amplifiers.
16	BCKIN	IN	Bit clock for clocking in the audio data.
17	DIN	IN	Serial audio data input
18	LRCIN	IN	Left/Right Word Clock. Frequency is equal to fs.
19	XTI	IN	Crystal or Master Clock Input
20	XTO	OUT	System Clock Out. This output is either 256fs or 384fs and is generated by the internal PLL.
21	V_{DD}	PWR	Analog Power Supply (+5V)
22	DGND	GND	Digital Ground
23	PGND	GND	PLL Ground
24	NC		No Connection

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1721	24-Pin SSOP	338

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	200mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

TYPICAL CONNECTION DIAGRAM

Figure 1 illustrates the typical connection diagram and shows the master clock from an external source (such as an MPEG decoder) used as an external clock driving XTI, leaving XTO open.

MASTER CLOCK AND SYSTEM CLOCK

PCM1721 has a programmable internal PLL circuit. The PLL is designed to accept a 27MHz master clock at the XTI input and generate all internal system clocks required to operate the digital filter and ΔΣ modulator, either at 256fs or 384fs. The master clock can be an external 27MHz frequency source directly connected to XTI, as shown in Figure 1.

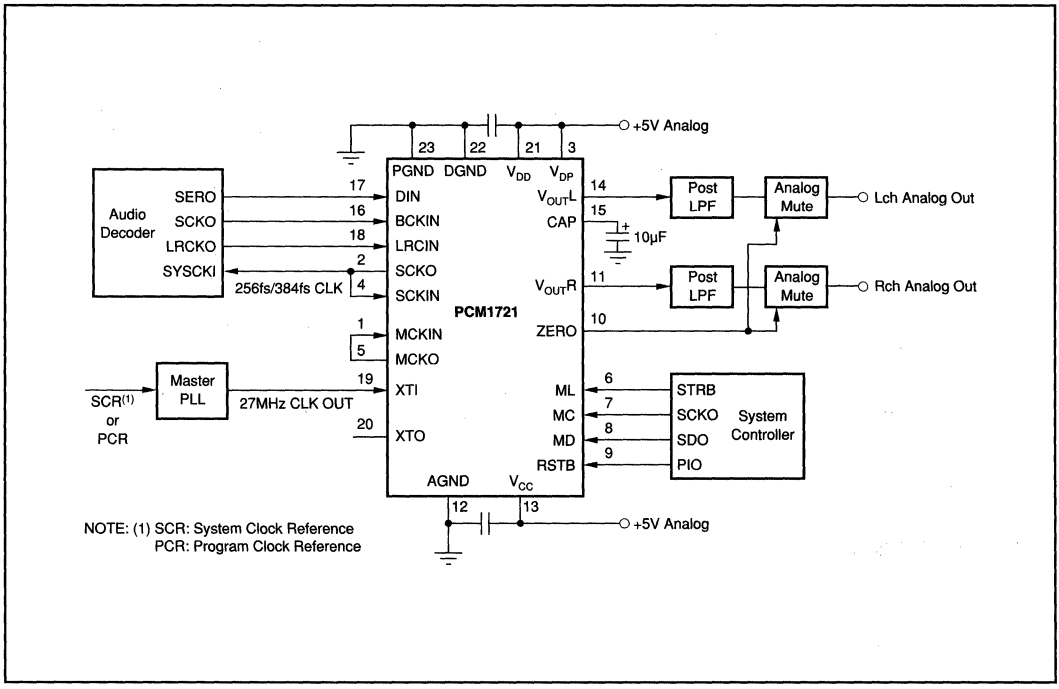


FIGURE 1. External Master Clock Input.

	Sampling Frequencies-LRCIN (kHz)		
Half of Standard Sampling Freq	16	22.05	24
Standard Sampling Freq	32	44.1	48
Double of Standard Sampling Freq	64	88.2	96

TABLE I. Sampling Frequencies.

PCM1721's internal PLL can be programmed for nine different sampling frequencies (LRCIN), as shown in Table I. The internal sampling clocks generated by the various programmed frequencies are shown in Table II.

	HALF OF STANDARD SAMPLING FREQUENCY						STANDARD SAMPLING FREQUENCY						DOUBLE OF STANDARD SAMPLING FREQUENCY					
	256fs (kHz)			384fs (kHz)			256fs (kHz)			384fs (kHz)			256fs (kHz)			384fs (kHz)		
INTERNAL SYSTEM CLOCK (MHz)	16	22.05	24	16	22.05	24	32	44.1	48	32	44.1	48	64	88.2	96	64	88.2	96
4.096	○																	
5.6448		○																
6.144			○															
6.144				○														
8.4672					○													
9.216						○												
8.192							○											
11.2896								○										
12.288									○									
12.288										○								
16.934											○							
18.432												○						
16.384													○					
22.5792														○				
24.576															○			
24.576																○		
33.8688																	○	
36.864																		○

TABLE II. Sampling Frequencies vs Internal System Clock.

FUNCTION	DEFAULT MODE
Input Audio Data Format Selection Normal Format I²S Format	Normal Format
Input Audio Data Bit Selection 16/20/24 Bits	16 Bits
Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High	Lch/Rch = High/Low
De-emphasis Control	OFF
Soft Mute Control	OFF
Attenuation Control Lch, Rch Individually Lch, Rch Common	0dB Lch, Rch Individually Fixed
Infinite Zero Detection Circuit Control	OFF
DAC Operation Control	Enabled
Sample Rate Selection Internal System Clock Selection 256fs 384fs	384fs
Double Sampling Rate Selection Standard Sampling Rate—44.1/48/32kHz Double Sampling Rate—88.2/96/32kHz Half Sampling Rate—22.05/24/16kHz	Standard Sampling Rate
Sampling Frequency 44.1kHz Group 48kHz Group 32kHz Group	44.1kHz
Analog Output Mode L, R, Mono, Mute	Stereo

TABLE III. Selectable Functions.

SPECIAL FUNCTIONS

PCM1721 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 8) is used for the program data, MC (pin 7) is used to clock in the program data, and ML (pin 6) is used to latch in the program data. Table III lists the selectable special functions.

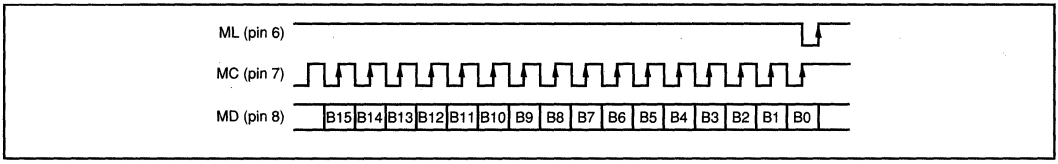


FIGURE 2. Serial Interface Timing.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	I²S

PROGRAM REGISTER BIT MAPPING

PCM1721's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table IV shows the complete mapping of the four registers and Figure 2 illustrates the data input timing.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0)	DAC Attenuation Data for Lch
	LDL	Attenuation Data Load Control for Lch
	A (1:0)	Register Address
	res	Reserved
Register 1	AR (7:0)	DAC Attentuation Data for Rch
	LDL	Attenuation Data Load Control for Rch
	A (1:0)	Register Address
	res	Reserved
Register 2	MUT	Left and Right DACs Soft Mute Control
	DEM	De-emphasis Control
	OPE	Left and Right DACs Operation Control
	IW (1:0)	Input Audio Data Bit Select
	PL (3:0)	Output Mode Select
	A (1:0)	Register Address
	res	Reserved
Register 3	I²S	Audio Data Format Select
	LRP	Polarity of LRCIN (pin 7) Select
	ATC	Attenuator Control
	SYS	System Clock Select
	DSR (1:0)	Double Sampling Rate Select
	SF (1:0)	Sampling Rate Select
	IZD	Infinite Zero Detection Circuit Control
	A (1:0)	Register Address
	res	Reserved

TABLE IV. Internal Register Mapping.

REGISTER 0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20\log10\ (ATT\_DATA/255)]\ dB$$

ATTENUATION DATA LOAD CONTROL, LCH

Bit 8 (LDL) is used to simultaneously set analog outputs of Lch and Rch. An output level is controlled by AL[0:7] attenuation data when this bit is set to 1. When set to 0, an output level is not controlled and remains at the previous attenuation level. A LDR bit in Register 1 has an equivalent function as the LDL. When one of LDL or LDR is set to 1, the output level of the left and right channel is simultaneously controlled. The attenuation level is given by:

$$ATT = 20\log\ (y/256)\ (dB),\ \text{where } y = x,\ \text{when } 0 \le x \le 254$$
$$y = x + 1,\ \text{when } x = 255$$

X is the user-determined step number, an integer value between 0 and 255.

Example:

let x = 255

$$ATT = 20\log\left(\frac{255+1}{256}\right) = 0dB$$

let x = 254

$$ATT = 20\log\left(\frac{254}{256}\right) = -0.068dB$$

let x = 1

$$ATT = 20\log\left(\frac{1}{256}\right) = -48.16dB$$

let x = 0

$$ATT = 20\log\left(\frac{0}{256}\right) = -\infty$$

REGISTER 1

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a "HIGH" level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no "click" is audible). Bit 1 is used to control de-emphasis. A "LOW" level on bit 1 disables de-emphasis, while a "HIGH" level enables de-emphasis.

Bit 2, (OPE) is used for operational control. Table V illustrates the features controlled by OPE.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
OPE = 1	Zero	Forced to BPZ(1)	Enabled
	Other	Forced to BPZ(1)	Enabled
OPE = 0	Zero	Controlled by IZD	Enabled
	Other	Normal	Enabled

TABLE V. Output Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is "LOW", the DAC will convert all non-zero input data. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be forced to zero only if IZD is "HIGH". When OPE is "HIGH", the output of the DAC will be forced to bipolar zero, irrespective of any input data.

	DATA INPUT	DAC OUTPUT
IZD = 1	Zero	Forced to BPZ(1)
	Other	Normal
IZD = 0	Zero	Zero(2)
	Other	Normal

TABLE VI. Infinite Zero Detection (IZD) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
RSTB = "HIGH"	Zero	Controlled by OPE and IZD	Enabled
	Other	Controlled by OPE and IZD	Enabled
RSTB = "LOW"	Zero	Forced to BPZ(1)	Disabled
	Other	Forced to BPZ(1)	Disabled

TABLE VII. Reset (RSTB) Function.

NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier. (2) $\Delta\Sigma$ is connected to output amplifier.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1721 can be set up for input word resolutions of 16, 20, or 24 bits:

Bit 4 (IW1)	Bit 3 (IW0)	Input Resolution
0	0	16-bit Data Word
0	1	20-bit Data Word
1	0	24-bit Data Word
0	0	Reserved

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1721 can be programmed for 16 different states, as shown in Table VIII.

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE VIII. Programmable Output Format.

REGISTER 3

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	I²S

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency and infinite zero detection.

Bits 0 (I^2S) and 1 (LRP) are used to control the input data format. A "LOW" on bit 0 sets the format to "Normal" (MSB-first, right-justified Japanese format) and a "HIGH" sets the format to I^2S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is "LOW", left channel data is assumed when LRCIN is in a "HIGH" phase and right channel data is assumed when LRCIN is in a "LOW" phase. When bit 1 is "HIGH", the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is "HIGH", the attenuation data loaded in program Register 0 is used for both left and right channels. When bit 2 is "LOW", the attenuation data for each register is applied separately to left and right channels.

Bit 3 (SYS) is the system clock selection. When bit 3 is "LOW", the system clock frequency is set to 384fs. When bit 3 is "HIGH", the system clock frequency is set to 256fs.

Bits 4 (DSR0) and 5 (DSR1) are used to control multiples of the sampling rate:

DSR1	DSR0	Multiple	
0	0	Normal	32/44.1/48kHz
0	1	Double	64/88.2/96kHz
1	0	One-half	16/22.05/24kHz
1	1	Reserved	Not Defined

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency:

SF1	SF0	Sampling Frequency	
0	0	44.1kHz group	22.05/44.1/88.2kHz
0	1	48kHz group	24/48/96kHz
1	0	32kHz group	16/32/64kHz
1	1	Reserved	Not Defined

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is "LOW", the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is "HIGH", the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1721 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

Appendix A

Demonstration Boards

Burr-Brown offers a wide variety of demonstration boards for both its Linear and Mixed Signal Products. New boards for new products are continually being added to the selection—contact the factory your local salesperson for availability.

NOTE: All evaluation fixtures whose model number ends with a 'C' include the product or products mentioned. All others do not include the product, except where specifically noted.

MODEL	PRODUCT	DESCRIPTION
DEM-ACF2101BP-C	ACF2101BP	Evaluation Fixture with Programmable Timing Generator
DEM-ADS1210P-C	ADS1210P	Evaluation Fixture—24-bit single channel A/D converter; includes FFT Software and IBM PC Interface.
DEM-ADS1211P-C	ADS1211P	Evaluation Fixture—24-bit four channel A/D converter; includes FFT Software and IBM PC Interface.
DEM-ADS7804/05C	ADS7804/05	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7806/07C	ADS7806/07	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7808/09C	ADS7808/09	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7810/19C	ADS7810/19	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7833	ADS7833	Evaluation Fixture—12-bit data acquisition system; board includes LCD display, microcontroller and reconstruction DAC.
DEM-ADS800U	ADS800U	Evaluation Fixture—12-bit, 40MHz ADC, AC-and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS801U	ADS801U	Evaluation Fixture—12-bit, 25MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS802U	ADS802U	Evaluation Fixture—12-bit, 10MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS820U	ADS820U	Evaluation Fixture—10-bit, 20MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-ADS821U	ADS821U	Evaluation Fixture—10-bit, 40MHz ADC, AC- and DC-coupled inputs, on-board clock, bus driver, SMA connectors.
DEM-BUF600-1GC	BUF600AP	Evaluation Fixture—900MHz Buffer Amplifier
DEM-BUF601-1GC	BUF601AP	Evaluation Fixture—650MHz Buffer Amplifier
DEM-DAC650J-E	DAC650JL	Evaluation Fixture—Digital Input and Analog Output (all SMA connectors). The part is included and soldered to the board.
DEM-DDC101P-C	DDC101P	Evaluation Fixture,— includes the DDC101 board, interface board to connect to parallel PC-port and software. Supports all DDC101 options plus FFT.
DEM-MPC100-1GC	MPC100AU	Evaluation Fixture—4 to 1 High Speed Multiplexer and Output Buffer BUF601AU.

MODEL	PRODUCT	DESCRIPTION
DEM-MPC102-1GC	MPC102AU	Evaluation Fixture—Dual 2 to 1 High Speed Multiplexer and optional output buffer, BUF601AU.
DEM-OPA465xP	OPA465xP	Evaluation Fixture—Unpopulated board for quad High Speed op amp OPA465x in DIP package.
DEM-OPA465xU	OPA465xU	Evaluation Fixture—Unpopulated board for quad High Speed op amp OPA465x in SOIC package.
DEM-OPA622-1GC	OPA622AP	Evaluation Fixture—For voltage and current feedback configuration.
DEM-OPA623-1GC	OPA623AP	Evaluation Fixture—High Speed current feedback Op Amp.
DEM-OPA628AP-C	OPA628AP	Evaluation Fixture—User selectable configuration for the DIP package.
DEM-OPA628AU-C	OPA628AU	Evaluation Fixture-User selectable configuration for the SOIC package.
DEM-OPA64XP-Y	OPA64XP	Evaluation Fixture—Three boards are offered for the DIP package of the OPA64X series of operational amplifiers. DEM-OPA64XP-F: follower configuration; DEM-OPA64XP-N: noninverting configuration; DEM-OPA64XP-I: inverting configuration. (Note: each board will operate with any OPA64XP series op amp. No component is included—it must be ordered separately.)
DEM-OPA64XU-Y	OPA64XU	Evaluation Fixture—Three boards are offered for the SOIC package of the OPA64X series of operational amplifiers. DEM-OPA64XU-F: follower configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-I: inverting configuration. (Note: each board will operate with any OPA64XU series op amp. No component is included—it must be ordered separately.)
DEM-OPA65XP	OPA65XP	Evaluation Fixture—One board for OPA65X single op amps for the DIP package.
DEM-OPA65XU	OPA65XU	Evaluation Fixture—One board for OPA65X single op amps for the SOIC package.
DEM-OPA265XP	OPA265XP	Evaluation Fixture—One board for OPA265X dual op amps for the DIP package.
DEM-OPA265XU	OPA265XU	Evaluation Fixture—One board for OPA265X dual op amps for the SOIC package.
DEM-OPA660-XXX	OPA660	Evaluation Fixture—Five boards are offered for five different configurations. DEM-OPA660-1GC: Diamond transistor and buffer; DEM-OPA660-2GC: Current-feedback operational amplifier; DEM-OPA660-3GC: Direct-feedback amplifier; DEM-OPA660-4G: Layouts for all applications using SOIC (unassembled); DEM-OPA660-5G: Layouts for all applications using DIP packages (unassembled)
DEM-OPA2662-1GC	OPA2662	Evaluation Fixture—High speed voltage controlled current source.

MODEL	PRODUCT	DESCRIPTION
DEM-PCM1700P-C	PCM1700	Evaluation Fixture—Serial/SPDIF Inputs (formerly DEM-1143). Includes product.
DEM-PCM1702	PCM1702	Evaluation Fixture—Serial digital input, 8X digital interpolator (NPC5842), and analog output. A PCM1702P is included. The board will interface directly to the DEM-1760. The fixture does not accept SPDIF input.
DEM-PCM1710	PCM1710U	Evaluation Fixture—Serial Digital Audio In. Left and Right channel analog out.
DEM-DAI1710	PCM1710U	Evaluation Fixture—Includes Digital Audio Interface (DAI) receiver chip and dual 2nd-order lowpass output filters.
DEM-PCM1712	PCM1712U	Evaluation Fixture—Low cost version of PCM1710.
DEM-PCM1715	PCM1715U	Evaluation Fixture—Serial digital audio in. Left and right channel analog out,
DEM-PCM1717	PCM1717	Evaluation Fixture—For the 16-/18-bit PCM1717
DEM-PCM1717-1	PCM1717	Evaluation Fixture—For the 16-/18-bit PMC1717; includes PC interface and control software.
DEM-DAI1717	PCM1717	Evaluation Fixture—For the 16-/18-bit PCM1717; includes Digital Audio Interface, PC interface and control software.
DEM-PCM1750P-C	PCM1750	Evaluation Fixture—Serial/Parallel Output, SPDF Out (Formerly DEM 1133). Includes product.
DEM-PCM1760	PCM1760/DF1760	Evaluation Fixture—Analog input and serial digital output. A PCM1760P and DF1760P are included. The board will interface directly to the DEM-1702. The fixture does not provide SPDIF output.
DEM-PCM63P-C	PCM63P	Evaluation Fixture—Includes Dual PCM63s, SPDIF Input
DEM-PCM67P-C	PCM67P	Evaluation Fixture—Includes Dual PCM67s (single/dual supply operation), SPDIF Input.
DEMPCM78P-C	PCM78P	Evaluation Fixture—Analog Input, Parallel Data Output. Includes SHC5320 sample hold and PCM56 as a reconstruction ADC (formerly DEM-1122).
DEM-SHC605AU	SHC605AU	Evaluation Fixture—Analog input, digital control input, and sample/hold output (all SMA connectors). A SHC605AU is included and is soldered to the board.
DEM-VCA610AP-C	VCA610AP	Evaluation Fixture—Voltage Controlled Amplifier.

Appendix B

Tape and Reel Information

The listed surface mount packages are available spooled on embossed carrier tape and reel, meeting EIA481-A requirements. Package numbers can be found in individual product data sheet. Package drawings can be found in Appendix C.

PACKAGE NUMBER(1)	DESCRIPTION	TAPE WIDTH, W (mm)	PITCH, P (mm)	DEVICES PER REEL	REEL DIAMETER (mm)
178	SO-24	24	16	1000	360
182	SO-8	12	8	2500	360
211	SOL-16	16	12	1000	360
217	SO-28	24	12	1000	360
219	SOL-18	24	16	1000	360
221	SO-20	24	12	1000	360
235	SO-14	16	8	2500	360
239	SO-24	24	12	1000	360
248	SO-20	24	12	1000	360
311	SOT-223	12	8	2500	360
322	SSOP-16	12	8	2500 250	360 178
324	SSOP-28	24	12	1000	360
325	5-Lead DD Pak	24	16	1000	360
328	7-Lead DD Pak	24	16	1000	360
331	SOT23-5	8	4	 3000 250	360 178 178
332	SOT23-6	8	4	3000 250	178 178
333	SSOP-48	32	16	1000	360
334	SSOP-20	32	16	1000	360
337	MSOP-8	12	8	2500 250	360 178

NOTE: (1) Package numbers can be found in individual product data sheet in the "Package Information" table. Package drawings are in Appendix C.

TABLE I.

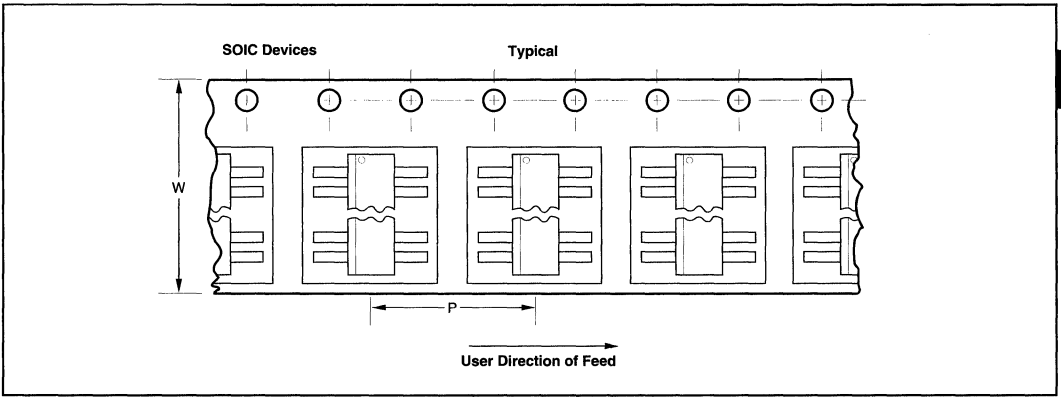


FIGURE 1.

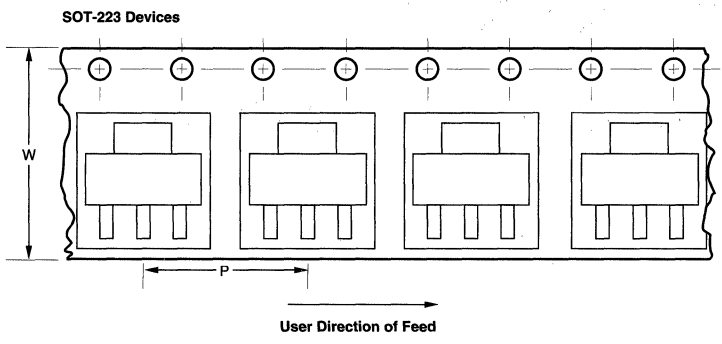
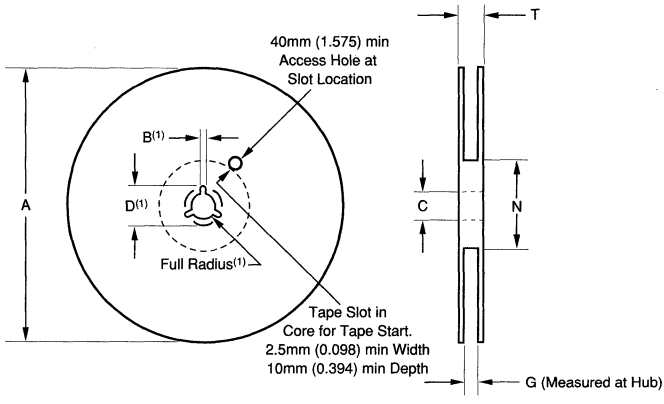


FIGURE 2.



NOTE: (1) Drive spokes optional. Noted dimensions apply if used.

FIGURE 3.

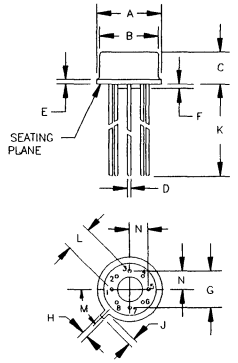
TAPE SIZE	A MAX	B MAX	C	D MIN	N MIN	G	T MAX
12mm	330mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	12.4 + 1.0 (–0.0mm)	18.4mm
16mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	16.4 + 1.0 (–0.08mm)	22.4mm
24mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	24.4 + 1.0 (–0.00mm)	30.4mm

TABLE II.

Appendix C

Package Drawings (Mechanicals)

Package Number 001 - Metal TO-99



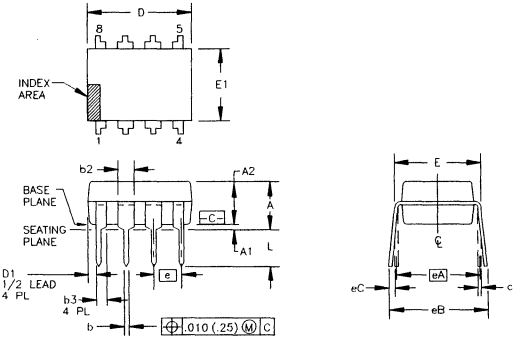
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.335	.380	8.51	9.65	
B	.305	.335	7.75	8.51	
C	.165	.185	4.19	4.70	
D	.016	.021	0.41	0.53	
E	.010	.040	0.25	1.02	
F	.010	.040	0.25	1.02	
G	.200	BASIC	5.08	BASIC	
H	.028	.034	0.71	0.86	
J	.029	.045	0.74	1.14	
K	.500	--	12.7	--	
L	.110	.160	2.79	4.06	
M	45°	BASIC	45°	BASIC	
N	.095	.105	2.41	2.67	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ001 | REV.: B
JEDEC NUMBER: UNKNOWN

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



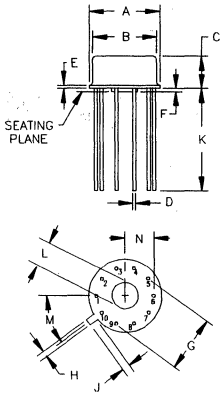
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 | REV.: E
JEDEC NUMBER: MS-001-BA

Package Number 007 - TO-100 Package



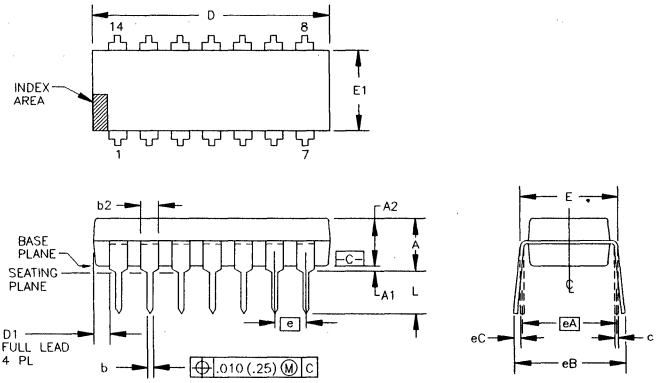
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.335	.370	8.51	9.40	
B	.305	.335	7.75	8.51	
C	.165	.185	4.19	4.70	
D	.016	.021	0.41	0.53	
E	.010	.040	0.25	1.02	
F	.010	.040	0.25	1.02	
G	.230	BASIC	5.84	BASIC	
H	.028	.034	0.71	0.86	
J	.029	.045	0.74	1.14	
K	.500	--	12.70	--	
L	.120	.160	3.05	4.06	
M	36°	BASIC	36°	BASIC	
N	.110	.120	2.79	3.05	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ007	REV.: A
JEDEC NUMBER: UNKNOWN	

Package Number 010 - 14-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	.735	.775	18.67	19.69	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6

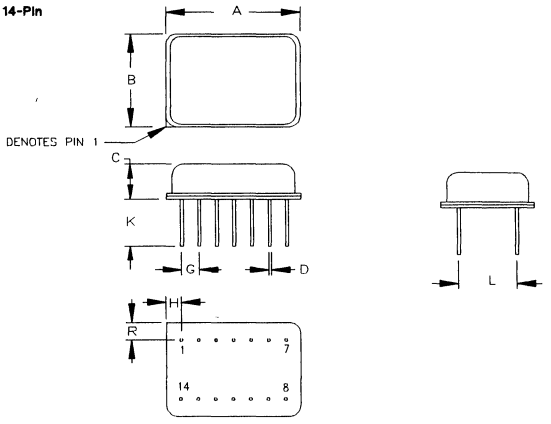
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
L	.115	.150	2.92	3.81	3
N	14		14		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010	REV.: G
JEDEC NUMBER: MS-001-AA	

Package Number 107 - 14-Pin



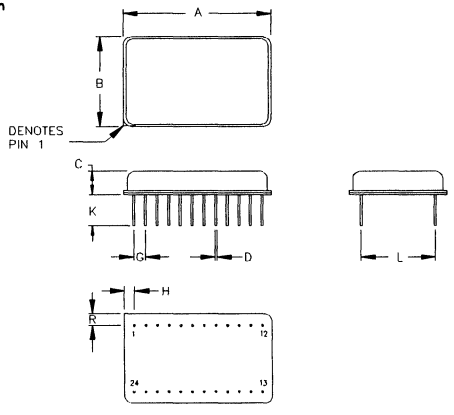
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.860	.880	21.84	22.35	
B	.490	.510	12.45	12.95	
C	.170	.250	4.32	6.35	
D	.016	.021	0.41	0.53	
G	.100	BASIC	2.54	BASIC	
H	.115	.155	2.92	3.94	
K	.150	.300	3.81	7.62	
L	.300	BASIC	7.62	BASIC	
R	.080	.120	2.03	3.05	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.

PACKAGE NUMBER: ZZ107 | REV.: A
JEDEC NUMBER: UNKNOWN

Package Number 113 - 24-Pin



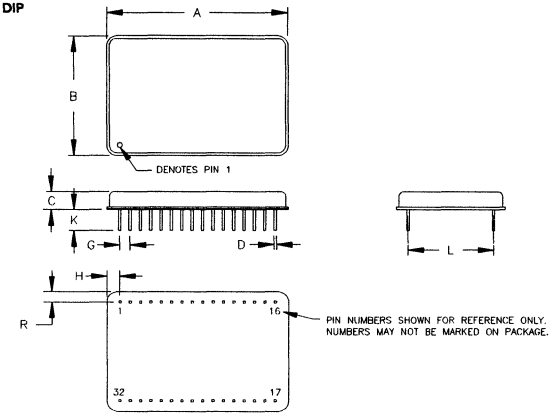
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	1.365	1.385	34.67	35.18	
B	.790	.810	20.07	20.57	
C	.170	.250	4.32	6.35	
D	.016	.021	0.41	0.53	
G	.100	BASIC	2.54	BASIC	
H	.125	.150	3.18	3.81	
K	.150	.300	3.81	7.62	
L	.600	BASIC	15.24	BASIC	
R	.080	.110	2.03	2.79	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.

PACKAGE NUMBER: ZZ113 | REV.: A
JEDEC NUMBER: UNKNOWN

Package Number 116 - 32-Pin DIP



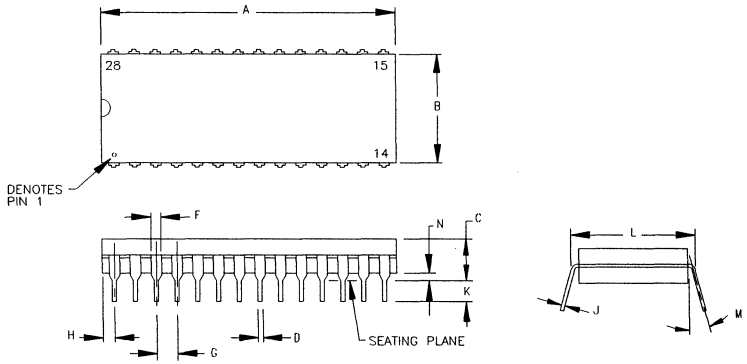
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	1.720	1.760	43.69	44.70	
B	1.120	1.160	28.45	29.46	
C	.170	.250	4.32	6.35	
D	.016	.021	0.41	0.53	
G	.100	BASIC	2.54	BASIC	
H	.100	.140	2.54	3.56	
K	.150	.300	3.81	7.62	
L	.900	BASIC	22.86	BASIC	
R	.100	.140	2.54	3.56	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

PACKAGE NUMBER: ZZ116 | REV.: A
JEDEC NUMBER: UNKNOWN

Package Number 126 - 28-Pin CERDIP



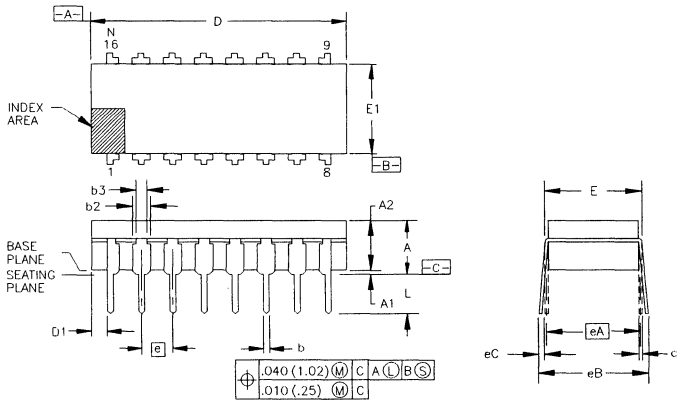
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	1.360	1.470	34.54	37.34	
B	.500	.550	12.70	13.97	
C	--	.200	--	5.08	
D	.015	.021	0.38	0.53	
F	.030	.070	0.76	1.78	
G	.100	BASIC	2.54	BASIC	
H	.030	.095	0.76	2.41	
J	.007	.013	0.18	0.33	
K	.100	--	2.54	--	
L	.600	BASIC	15.24	BASIC	
M	--	15°	--	15°	
N	.020	.090	0.51	2.29	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ126 | REV.: B
JEDEC NUMBER: UNKNOWN

Package Number 129 - 16-Lead CERDIP, .300 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.230	--	5.84	
A1	.015	--	0.38	--	
A2	.140	.180	3.56	4.57	
b	.015	.023	0.38	0.58	9
b2	.045	.070	1.14	1.78	
b3	.035	TYP	0.89	TYP	
c	.008	.015	0.20	0.38	9
D	.753	.885	19.13	22.48	3
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.25	4
E1	.280	.295	7.11	7.50	3
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.62	BASIC	4
eB	--	.450	--	11.43	5

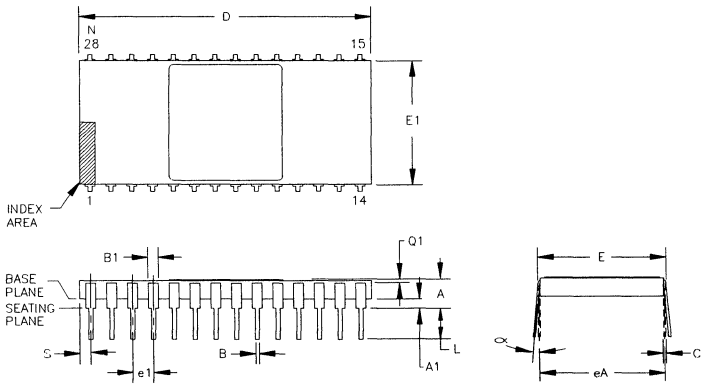
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	--	0.00	--	5
L	.100	--	2.54	--	
N	16		16		6

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ129	REV.: D
JEDEC NUMBER: NONE	

Package Number 149 - 28-Lead Side Braze DIP, .600 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.085	.190	2.16	4.83	
A1	.020	.070	0.51	1.78	
B	.015	.023	0.38	0.58	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	1.380	1.430	35.05	36.32	
E	.595	.625	15.11	15.88	
E1	.580	.610	14.73	15.49	6
e1	.100	TYP.	2.54	TYP.	2
eA	.600	TYP.	15.24	TYP.	2
L	.125	.175	3.18	4.45	
N	28		28		4
Q1	.010	--	0.25	--	
S	.030	.065	0.76	1.65	

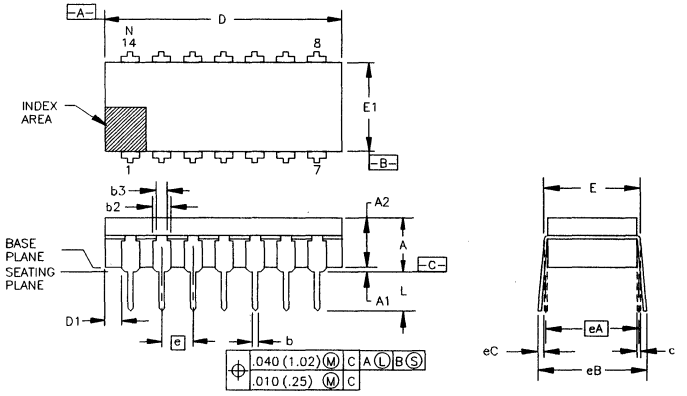
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
α	0°	15°	0°	15°	3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ149	REV.: C
JEDEC NUMBER: MO-038-AB	

Package Number 163 - 14-Lead CERDIP, .300 Wide



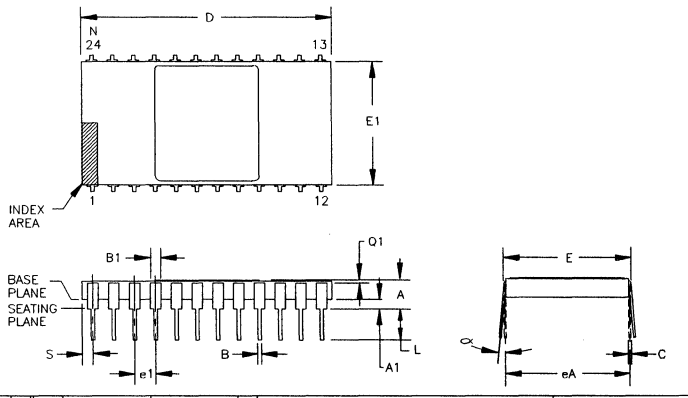
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.230	--	5.84	
A1	.015	--	0.38	--	
A2	.140	.180	3.56	4.57	
b	.015	.023	0.38	0.58	9
b2	.045	.070	1.14	1.78	
b3	.035	TYP	0.89	TYP	
c	.008	.015	0.20	0.38	9
D	.753	.767	19.13	19.48	3
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	4
E1	.280	.295	7.11	7.50	3
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.62	BASIC	4
eB	--	.450	--	11.43	5

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	--	0.00	--	5
L	.100	--	2.54	--	
N	14		14		6

NOTES:
1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE C.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
8. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
9. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
10. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ163	REV.: C
JEDEC NUMBER: NONE	

Package Number 165 - 24-Lead Side Braze DIP, .600 Wide



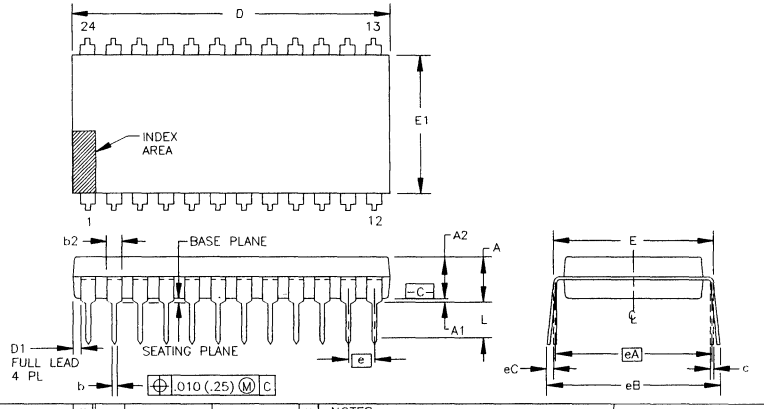
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.085	.190	2.16	4.83	
A1	.020	.070	0.51	1.78	
B	.015	.023	0.38	0.58	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	1.180	1.220	29.97	30.99	
E	.595	.625	15.11	15.88	
E1	.580	.610	14.73	15.49	6
e1	.100	TYP.	2.54	TYP.	2
eA	.600	TYP.	15.24	TYP.	2
L	.125	.175	3.18	4.45	
N	24		24		4
Q1	.010	--	0.25	--	
S	.030	.065	0.76	1.65	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ165	REV.: C
JEDEC NUMBER: MO-038-AA	

Package Number 167 - 24-Pin Plastic Double-Wide DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.250	--	6.35	3
A1	.015	--	0.38	--	3
A2	.125	.195	3.18	4.95	
b	.014	.022	0.36	0.56	
b2	.030	.070	0.76	1.78	9
c	.008	.015	0.20	0.38	
D	1.150	1.290	29.21	32.77	4
D1	.005	--	0.13	--	4
E	.600	.625	15.24	15.88	5
E1	.485	.580	12.32	14.73	4
e	.100 BASIC		2.54 BASIC		
eA	.600 BASIC		15.26 BASIC		5
eB	--	.700	--	17.78	6
eC	.000	.060	0.00	1.52	6

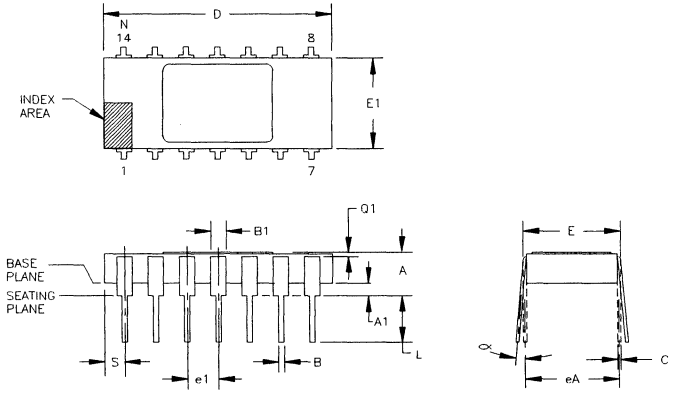
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
L	.115	.200	2.92	5.08	3
N	24		24		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ167 | REV.: H
JEDEC NUMBER: MS-011-AA

Package Number 169 - 14-Lead, Ceramic Side Braze DIP, .300 Wide



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	.690	.770	17.53	19.56	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	14		14		4
Q1	.010	--	0.25	--	
S	.030	.095	0.76	2.41	

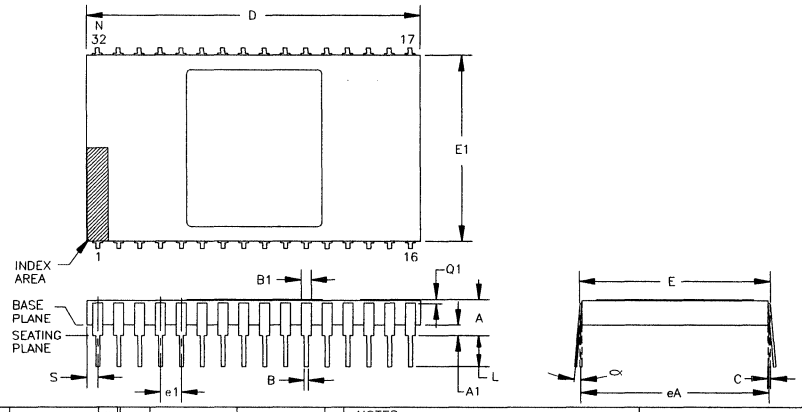
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
∝	0°	15°	0°	15°	3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ169 | REV.: F
JEDEC NUMBER: MO-36-AB

Package Number 172-5 - 32-Lead Side Braze DIP, .900 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.145	.195	3.68	4.95	
A1	.040	.060	1.02	1.52	
B	.016	.020	0.41	0.51	5
B1	.050 TYP.		1.27 TYP.		5
C	.009	.012	0.23	0.30	
D	1.580	1.620	40.13	41.15	
E	.900	.920	22.86	23.37	
E1	.885	.905	22.48	22.99	6
e1	.100 TYP.		2.54 TYP.		2
eA	.900 TYP.		22.86 TYP.		2
L	.125	.175	3.18	4.45	
N	32		32		4
Q1	.010	--	0.25	--	
S	.030	.065	0.76	1.65	

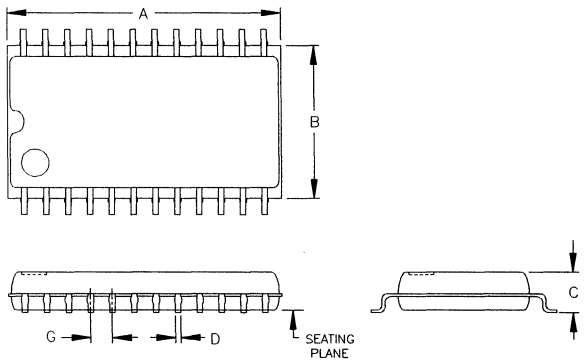
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
∝	0°	15°	0°	15°	3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ172-5	REV.: B
JEDEC NUMBER: NONE	

Package Number 178 - 24-Pin SOIC

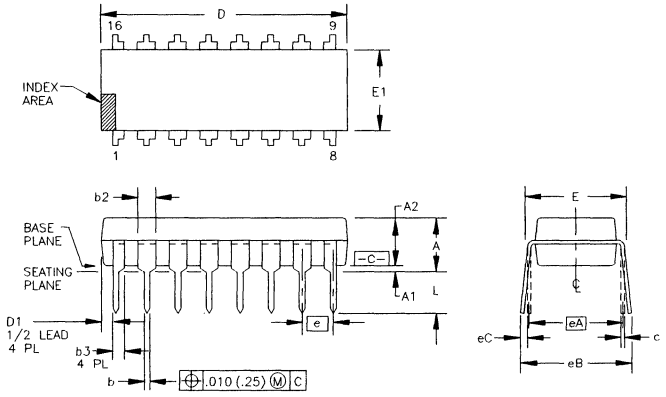


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.614	.630	15.60	16.00	
B	.346	.362	8.80	9.20	
C	--	.098	--	2.50	
D	.012	.020	0.30	0.50	
G	.046	.054	1.17	1.37	

NOTES:

PACKAGE NUMBER: ZZ178	REV.: A
JEDEC NUMBER: NONE	

Package Number 180 - 16-Pin Plastic, Single-Wide DIP



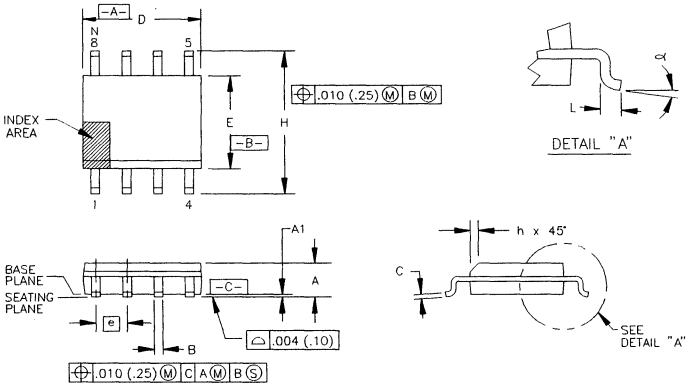
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.735	.775	18.67	21.34	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	16		16		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ180 | REV.: F
JEDEC NUMBER: MS-001-BB

Package Number 182 - 8-Lead SOIC

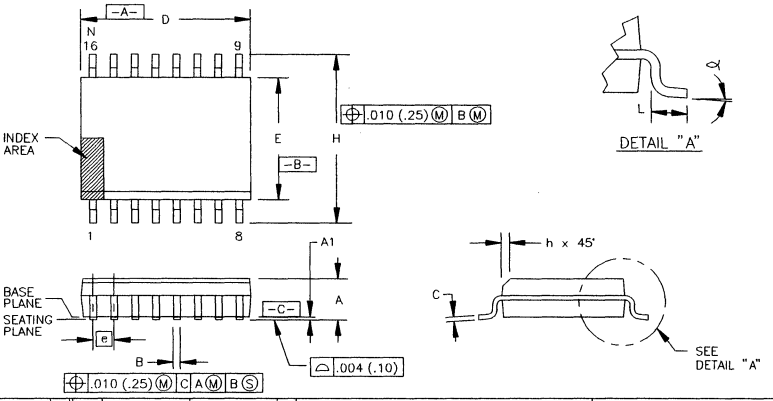


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.41	1.27	5
N	8		8		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 | REV.: H
JEDEC NUMBER: MS-012-AA

Package Number 211 - 16-Lead SOIC, .300 Wide

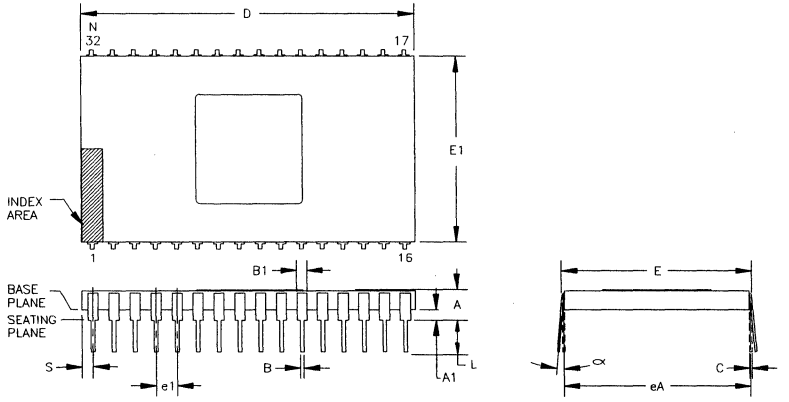


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.3977	.4133	10.10	10.50	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	16		16		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ211	REV.: F
JEDEC NUMBER: MS-013-AA	

Package Number 212 - 32-Lead Side Braze DIP, .900 Wide

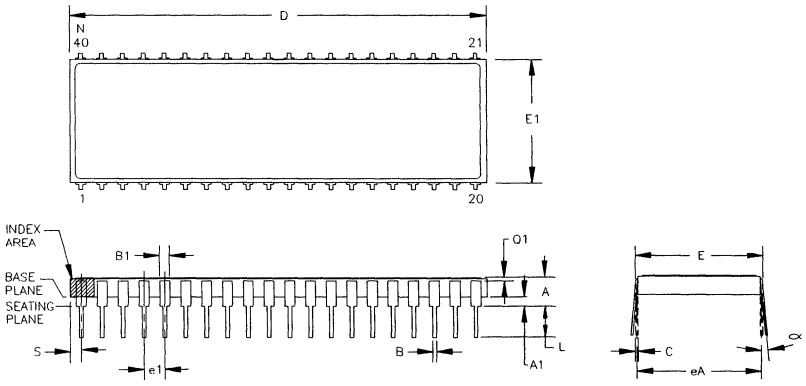


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.124	.166	3.15	4.22	
A1	.040	.060	1.02	1.52	
B	.016	.020	0.41	0.51	5
B1	.045	.055	1.14	1.40	5
C	.009	.012	0.23	0.30	
D	1.584	1.616	40.23	41.05	
E	.900	.920	22.86	23.37	
E1	.885	.905	22.48	22.99	6
e1	.100 TYP.		2.54 TYP.		2
eA	.900 TYP.		22.86 TYP.		2
L	.125	.180	3.18	4.57	
N	32		32		4
S	.030	.065	0.76	1.65	
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ212	REV.: C
JEDEC NUMBER: NONE	

Package Number 214 - 40-Lead Side Braze DIP, .600 Wide



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.085	.190	2.16	4.83	
A1	.020	.070	0.51	1.78	
B	.015	.023	0.38	0.58	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	1.980	2.030	50.29	51.56	
E	.595	.625	15.11	15.88	
E1	.580	.610	14.73	15.49	6
e1	.100 TYP.		2.54 TYP.		2
eA	.600 TYP.		15.24 TYP.		2
L	.125	.175	3.18	4.45	
N	40		40		4
Q1	.010	--	0.25	--	
S	.030	.065	0.76	1.65	

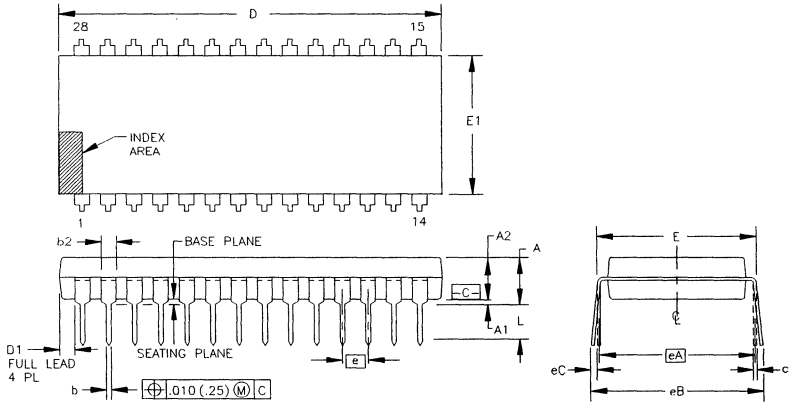
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
∝	0°	15°	0°	15°	3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ214	REV.: C
JEDEC NUMBER: MO-038-AC	

Package Number 215 - 28-Pin Plastic, Double-Wide DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.250	--	6.35	3
A1	.015	--	0.38	--	3
A2	.125	.195	3.18	4.95	
b	.014	.022	0.36	0.56	
b2	.030	.070	0.76	1.78	9
c	.008	.015	0.20	0.38	
D	1.380	1.565	35.05	39.75	4
D1	.005	--	0.13	--	4
E	.600	.625	15.24	15.88	5
E1	.485	.580	12.32	14.73	4
e	.100 BASIC		2.54 BASIC		
eA	.600 BASIC		15.26 BASIC		5
eB	--	.700	--	17.78	6
eC	.000	.060	0.00	1.52	6

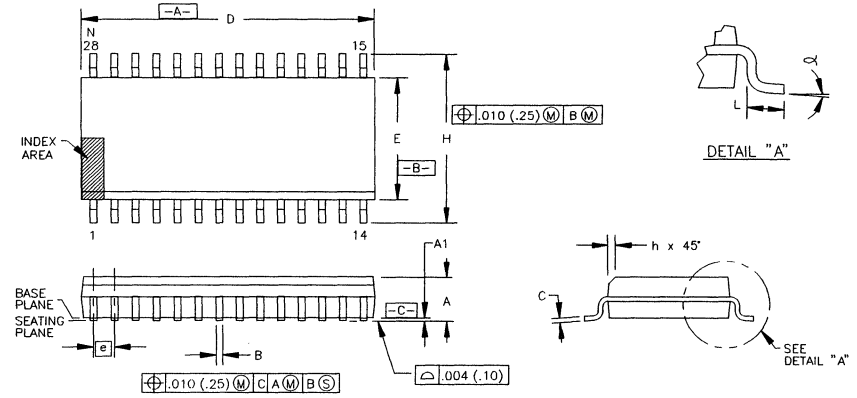
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
L	.115	.200	2.92	5.08	3
N	28		28		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ215	REV.: J
JEDEC NUMBER: MS-011-AB	

Package Number 217 - 28-Lead SOIC



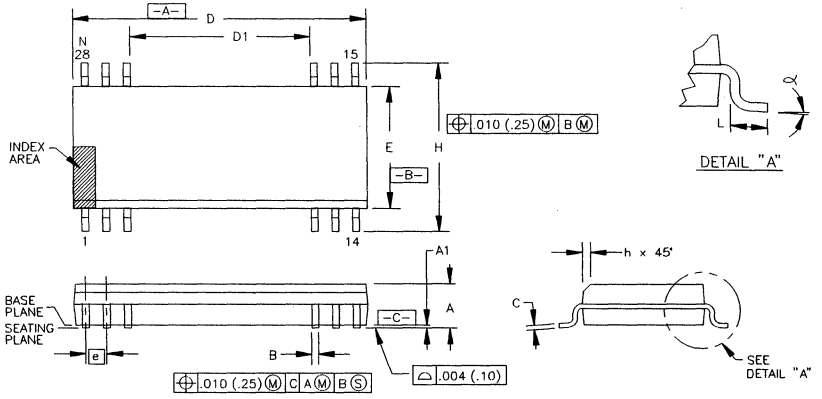
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.6969	.7125	17.70	18.10	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.398	.419	10.11	10.65	
h	.010	.0295	0.25	0.75	4
L	.020	.040	.508	1.02	5
N	28		28		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ217 | REV.: G

JEDEC NUMBER: MS–013–AE WITH THE EXCEPTION OF DIM. H, L.

Package Number 217-2 - 28-Lead SOIC, ISO Package



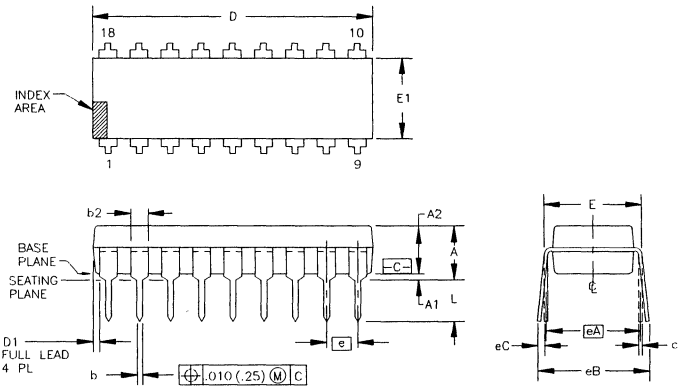
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.6969	.7125	17.70	18.10	2
D1	.426	.441	10.82	11.20	
E	.2914	.2992	7.42	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.01	10.65	
h	.010	.0295	0.25	0.75	4
L	.016	.050	0.41	1.27	5
N	12		12		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ217-2 | REV.: D

JEDEC NUMBER: MS–013–AE WITH THE EXCEPTION OF "N"

Package Number 218 - 18-Pin Plastic, Single-Wide DIP



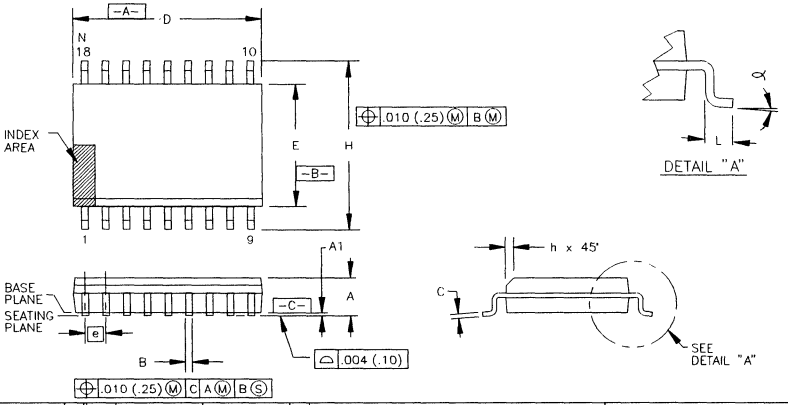
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	.880	.920	22.35	23.37	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
L	.115	.150	2.92	3.81	3
N	18		18		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM C.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ218 | REV.: D
JEDEC NUMBER: MS-001-AC

Package Number 219 - 18-LEAD SOIC

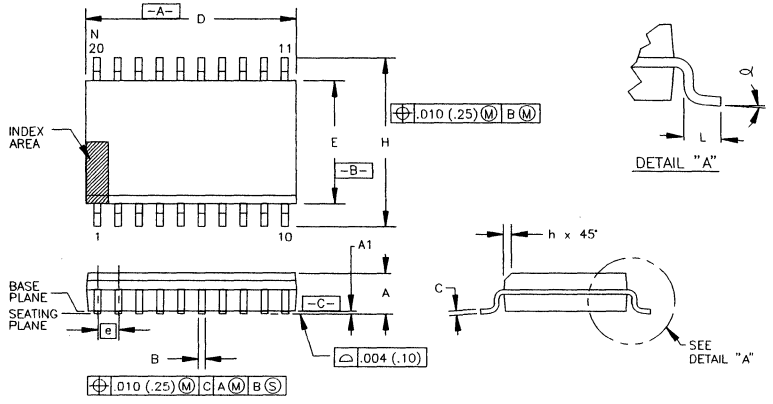


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.4469	.4625	11.35	11.75	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	18		18		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ219 | REV.: E
JEDEC NUMBER: MS-013-AB

Package Number 221 - 20-LEAD SOIC

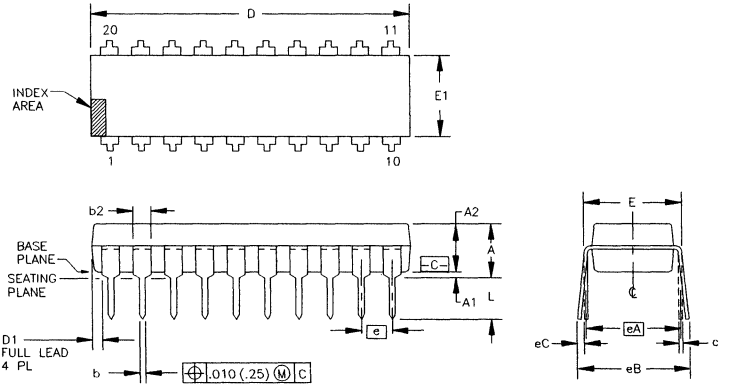


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.4961	.5118	12.60	13.00	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	20		20		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ221	REV.: D
JEDEC NUMBER: MS–013–AC	

Package Number 222 - 20-Pin Plastic, Single-Wide DIP

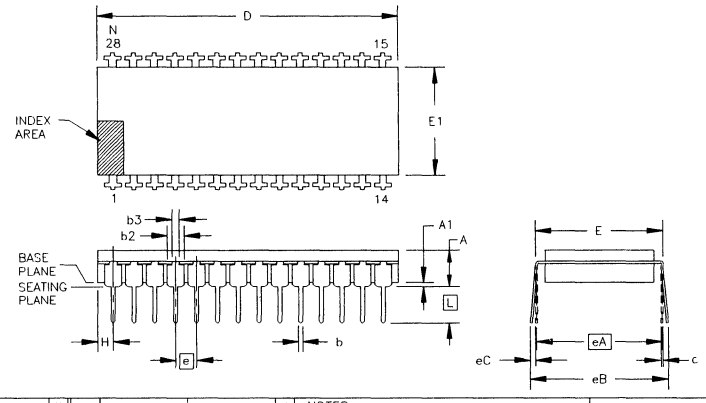


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	.980	1.060	24.89	26.92	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	20		20		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ222	REV.: C
JEDEC NUMBER: MS–001–AD	

Package Number 228 - 28-Lead CERDIP, .600 Wide



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.155	.193	3.94	4.90	
A1	.018	.022	0.46	0.56	
b	.018	TYP.	0.46	TYP.	8
b2	.080	TYP.	2.03	TYP.	
b3	.035	TYP.	0.89	TYP.	
c	.0098	.0102	0.249	0.259	8
D	1.440	1.460	36.57	37.08	3
E	.608	.614	15.44	15.60	
E1	.514	.526	13.06	13.36	3
e	.100	BASIC	2.54	BASIC	
eA	.600	BASIC	15.24	BASIC	
eB	.645	.675	16.38	17.15	4
eC	.000	--	0.00	--	4
H	.070	.080	1.78	2.03	

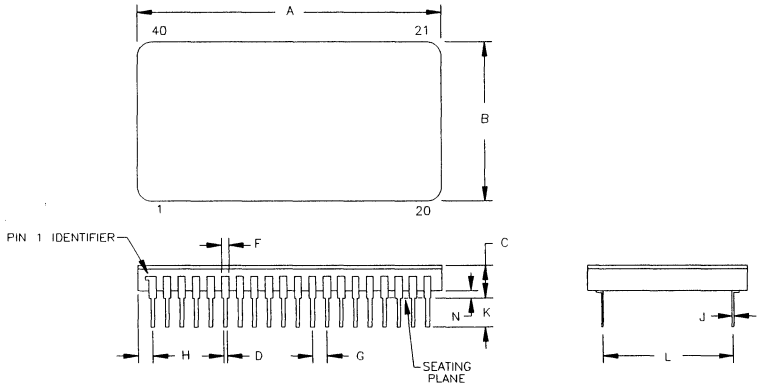
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
L	.175	BASIC	4.45	BASIC	
N	28		28		5

NOTES:

1. CONTROLLING DIMENSIONS: INCH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. D AND E1 DIMENSIONS INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS, AND LID TO BASE MISMATCH.
4. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
5. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
6. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
7. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.
8. b AND c DIMENSIONS INCLUDE BOTH THE BASE MATERIAL AND THE COATING OR PLATING ON THE LEADS.
9. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ228	REV.: B
JEDEC NUMBER: NONE	

Package Number 230 - 40-Pin Ceramic DIP



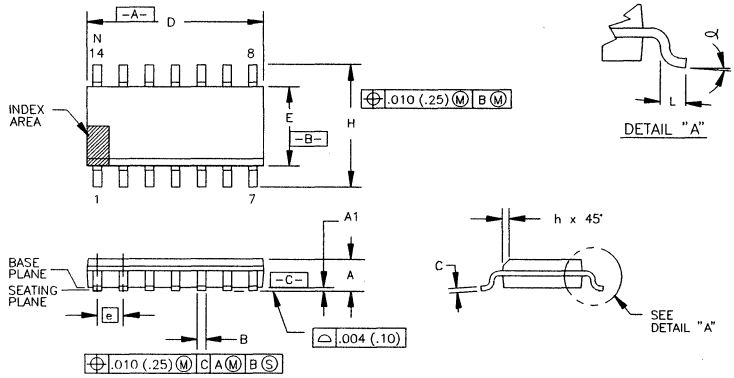
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	2.075	2.115	52.71	53.72	
B	1.080	1.100	27.43	27.94	
C	.145	.175	3.68	4.45	
D	.018	TYP.	0.46	TYP.	
F	.040	TYP.	1.02	TYP.	
G	.100	TYP.	2.54	TYP.	
H	.093	.103	2.36	2.62	
J	.020	BASIC	0.51	BASIC	
K	.205	BASIC	5.21	BASIC	
L	.900	BASIC	22.86	BASIC	
N	.015	.035	0.38	0.89	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25MM) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON THE PACKAGE.

PACKAGE NUMBER: ZZ230	REV.: A
JEDEC NUMBER: NONE	

Package Number 235 - 14-Lead SOIC

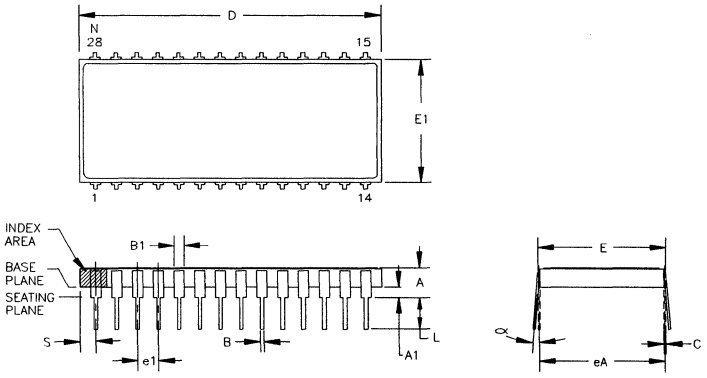


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.25	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.19	0.25	
D	.3367	.3444	8.55	8.75	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.40	1.27	5
N	14		14		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ235	REV.: E
JEDEC NUMBER: MS–012–AB	

Package Number 237 - 28-Lead Side Braze DIP, .600 Wide

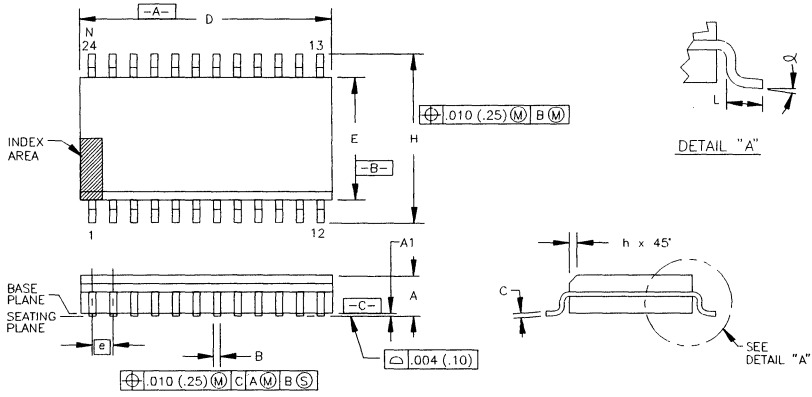


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.085	.190	2.16	4.83	
A1	.040	.060	1.02	1.52	
B	.016	.020	0.41	0.51	5
B1	.045	.055	1.14	1.40	5
C	.009	.012	0.23	0.30	
D	1.425	1.475	36.20	37.47	
E	.600	.620	15.24	15.75	
E1	.585	.605	14.86	15.37	6
e1	.100 TYP.		2.54 TYP.		2
eA	.590	.610	14.99	15.49	2
L	.125	.180	3.18	4.57	
N	28		28		4
S	.060	.090	1.52	2.29	
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.

PACKAGE NUMBER: ZZ237	REV.: C
JEDEC NUMBER: NONE	

Package Number 239 - 24-Lead SOIC

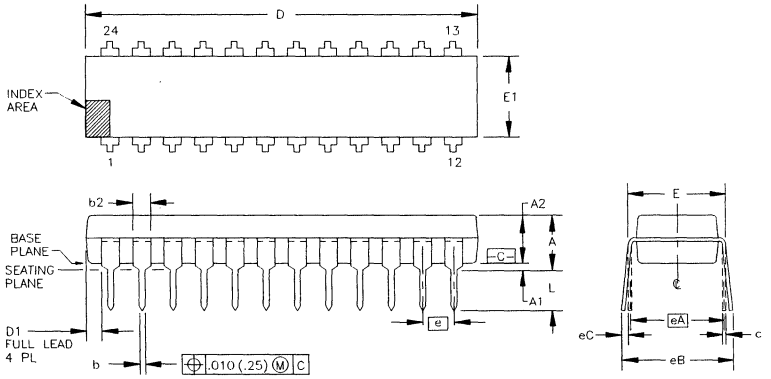


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.5985	.6141	15.20	15.60	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.0295	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	24		24		6
∝	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM THE SEATING PLANE.

PACKAGE NUMBER: ZZ239	REV.: E
JEDEC NUMBER: MS-013-AD	

Package Number 243 - 24-Pin Plastic, Single-Wide DIP

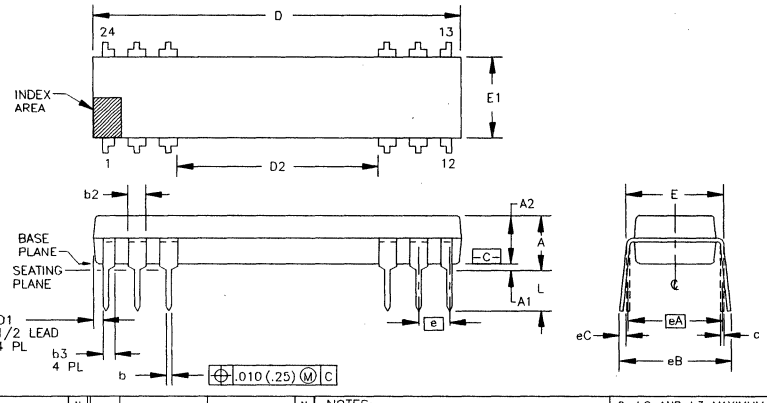


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	1.230	1.280	31.24	32.51	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.62 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	24		24		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243	REV.: D
JEDEC NUMBER: MS-001-AF	

Package Number 243-1 - 24-Pin Plastic, Single-Wide DIP, ISO Package



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	1.160	1.195	29.46	30.35	4
D1	.005	--	0.13	--	4
D2	.630	.655	16.00	16.64	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.62 BASIC		5

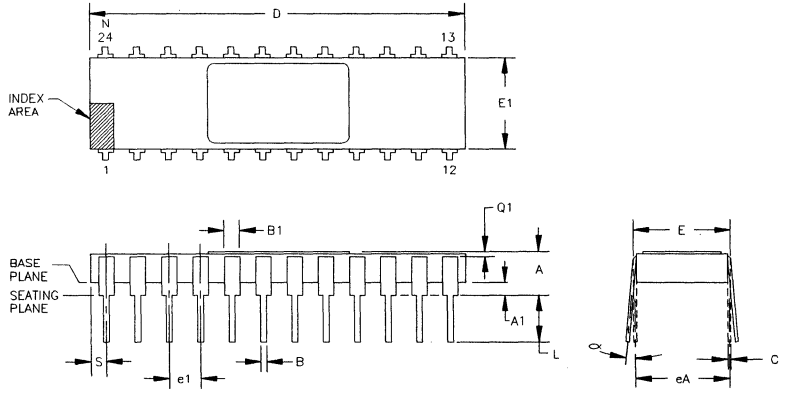
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	12		12		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ243-1 | REV.: J

JEDEC NUMBER: MS-001-BE WITH THE EXCEPTION OF "N"

Package Number 245 - 24-Lead, Ceramic Side Braze DIP, .300 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	1.188	1.212	30.18	30.78	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	24		24		4
Q1	.010	--	0.25	--	
S	.030	.065	0.76	1.65	

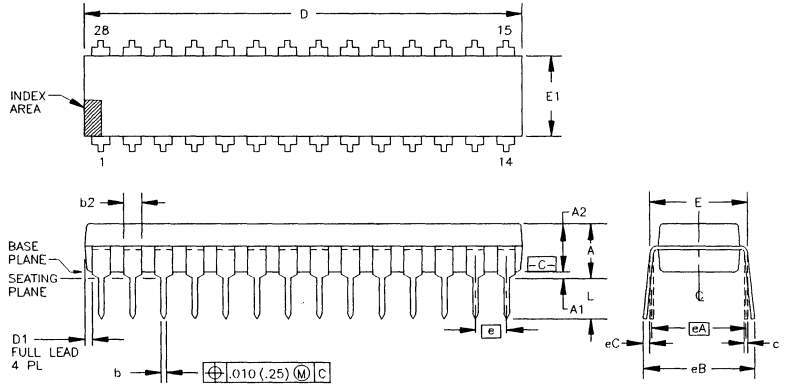
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ245 | REV.: C

JEDEC NUMBER: MO-36-AE WITH THE EXCEPTION OF DIM. D, N

Package Number 246 - 28-Pin Plastic, Single-Wide DIP



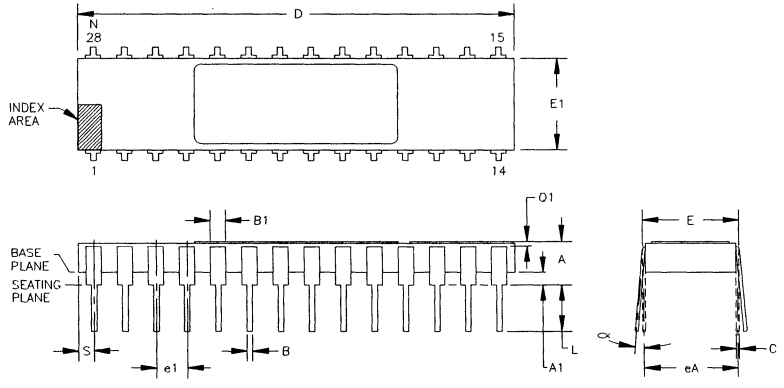
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	1.385	1.425	35.18	36.20	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.62 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
L	.115	.150	2.92	3.81	3
N	28		28		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ246	REV.: D
JEDEC NUMBER: MS-001-AG WITH THE EXCEPTION OF "N"	

Package Number 247 - 28-Lead, Ceramic Side Braze DIP, .300 Wide



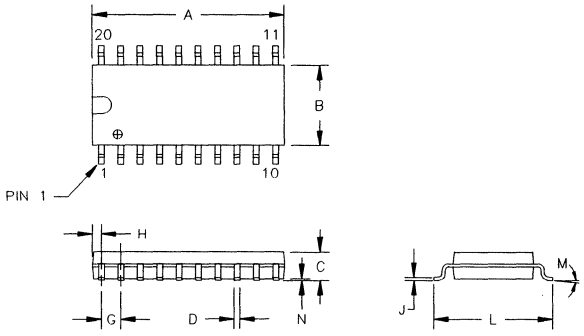
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	1.388	1.412	35.25	35.86	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	28		28		4
Q1	.010	--	0.25	--	
S	.030	.065	0.76	1.65	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ247	REV.: D
JEDEC NUMBER: MO-036-AE WITH THE EXCEPTION OF DIM. D, N	

Package Number 248 - 20-Pin Plastic SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.494	.498	12.55	12.65	
B	.206	.210	5.23	5.33	
C	.071	.077	1.80	1.96	
D	.013	.017	0.33	0.43	
G	.050	BASIC	1.27	BASIC	
H	.021	.025	0.53	0.64	
J	.0076	.0082	0.19	0.21	
L	.303	.311	7.70	7.90	
M	3°	5°	3°	5°	
N	.002	.006	0.05	0.15	

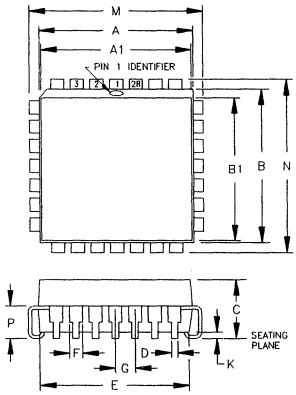
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25MM) @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER:	ZZ248	REV.: A
JEDEC NUMBER:	NONE	

Package Number 251 - 28-Pin LCC



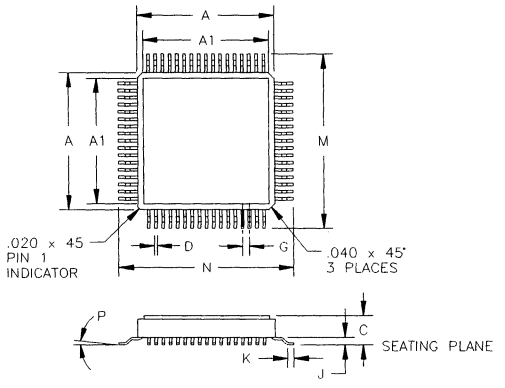
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.450	.460	11.43	11.68	
A1	.450	.460	11.43	11.68	
B	.450	.460	11.43	11.68	
B1	.450	.460	11.43	11.68	
C	.165	.180	4.19	4.57	
D	.013	.023	0.33	0.58	
E	.390	.430	9.91	10.92	
F	.026	.032	0.66	0.81	
G	.050	BASIC	1.27	BASIC	
K	.015	.025	0.38	0.64	
M	.485	.495	12.32	12.57	
N	.485	.495	12.32	12.57	
P	.100	.110	2.54	2.79	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

PACKAGE NUMBER:	ZZ251	REV.: A
JEDEC NUMBER:	UNKNOWN	

Package Number 256 - 68-Lead with Gull Wing



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.940	.960	23.88	24.38	
A1	.865	.875	21.97	22.23	
C	.200	REF.	4.81	REF.	
D	.013	.025	0.33	0.64	
G	.050	BASIC	1.27	BASIC	
J	.045	.055	1.14	1.40	
K	.045	REF.	1.14	REF.	
M	1.200	1.220	30.48	30.99	
N	1.200	1.220	30.48	30.99	
P	0°	6°	0°	6°	

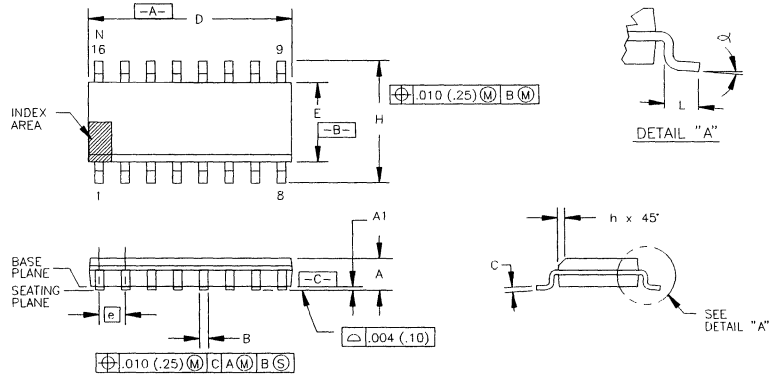
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 MAX AT SEATING PLANE.

PACKAGE NUMBER:	ZZ256	REV.:	A
JEDEC NUMBER:	UNKNOWN		

Package Number 265 - 16-Lead SOIC, .150 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.25	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.19	0.25	
D	.3859	.3937	9.80	10.00	2
E	.1497	.1574	3.80	4.00	3
e	.050	BASIC	1.27	BASIC	
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.40	1.27	5
N	16		16		6
∝	0°	8°	0°	8°	

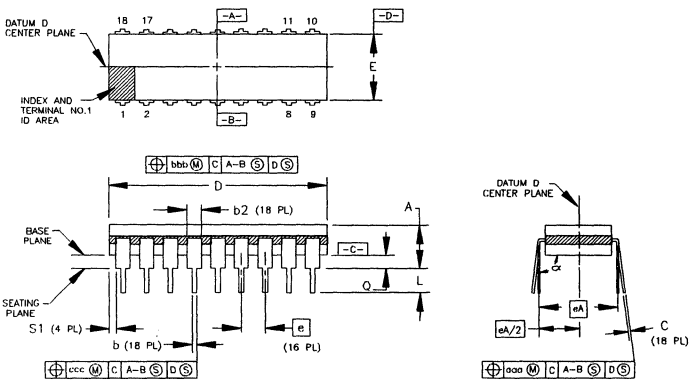
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER:	ZZ265	REV.:	D
JEDEC NUMBER:	MS-012-AC		

Package Number 266 - 18-Pin Side-Braze Ceramic



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.200	--	5.08	
b	.014	.026	0.36	0.66	
b2	.045	.065	1.14	1.65	
C	.008	.018	0.20	0.46	
D	--	.960	--	24.38	
E	.220	.310	5.59	7.87	
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.62 BASIC		
eA/2	.150 BASIC		3.81 BASIC		
L	.125	.200	3.18	5.08	
N	18		18		
Q	.015	.070	0.38	1.78	
S1	.005	--	0.13	--	
α	90°	105°	90°	105°	

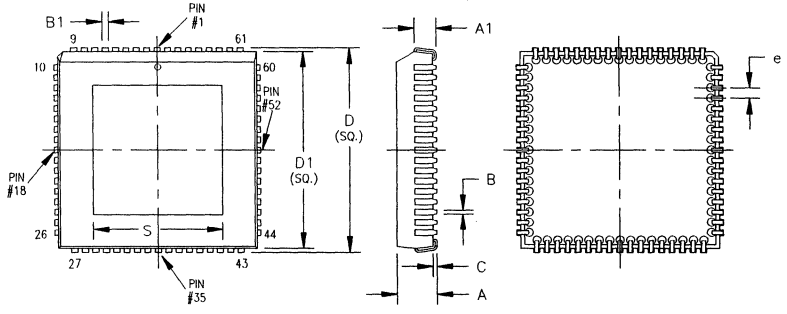
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONS ARE MIL-STD-1835 COMPLIANT (REF GDIP-P188, D-6).

PACKAGE NUMBER: ZZ266	REV.: A
JEDEC NUMBER: NONE	

Package Number 312-1 - 68-Pin Plastic Quad



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.167	.177	4.24	4.50	
A1	.100	.110	2.54	2.79	
B	.016	.020	0.41	0.51	
B1	.026	.032	0.66	0.81	
C	.020	.025	0.51	0.64	
D	.985	.995	25.02	25.27	
D1	.950	.958	24.13	24.33	2
e	.050 BASIC		1.27 BASIC		
N	68		68		
S	.618	.628	15.70	15.95	

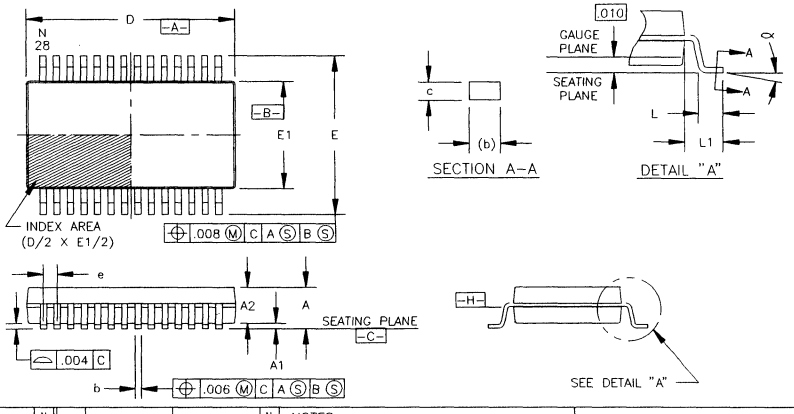
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .254mm/ .010 INCH.
3. CONTROLLING DIMENSION: INCH

PACKAGE NUMBER: ZZ312-1	REV.: B
JEDEC NUMBER: NONE	

Package Number 324 - 28-Lead Plastic SSOP

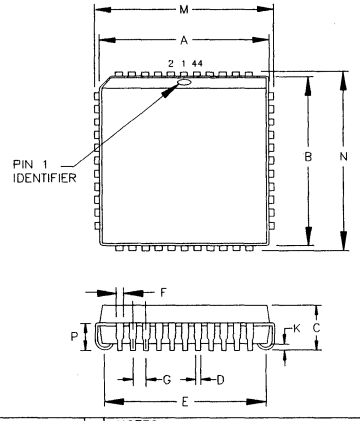


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.079	--	2.00	
A1	.002	--	0.05	--	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	3,7
c	.004	.010	0.09	0.25	7
D	.390	.413	9.90	10.50	2
E	.291	.323	7.40	8.20	
E1	.196	.220	5.00	5.60	2
e	.0256 BASIC		0.65 BASIC		
L	.022	.037	0.55	0.95	4
L1	.049	REF	1.25	REF	
N	28		28		5
θ	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM C.
5. N IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ324 | REV.: C
JEDEC NUMBER: MO-150

Package Number 329 - 44-Pin PLCC

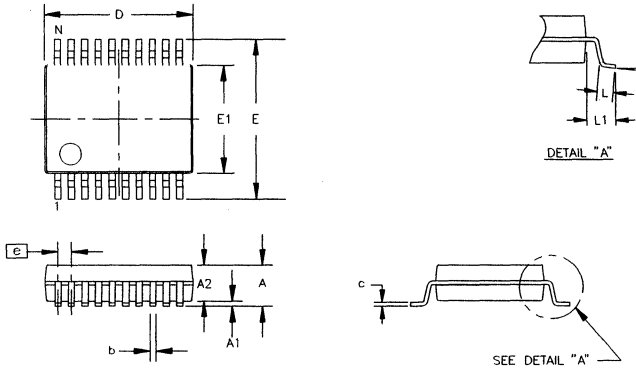


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.650	.656	16.51	16.66	
B	.650	.656	16.51	16.66	
C	--	.180	--	4.57	
D	.014	.022	0.36	0.56	
E	.600	.620	15.24	15.75	
F	.024	.032	0.61	0.81	
G	.050 BASIC		1.27 BASIC		
K	.020	--	0.51	--	
M	.685	.695	17.40	17.65	
N	.685	.695	17.40	17.65	
P	.100	.110	2.54	2.79	

NOTES:
1. LEADS IN TRUE POSITION WITHIN 0.01" (0.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ329 | REV.: A
JEDEC NUMBER: NONE

Package Number 334-1 - 20-Lead SSOP

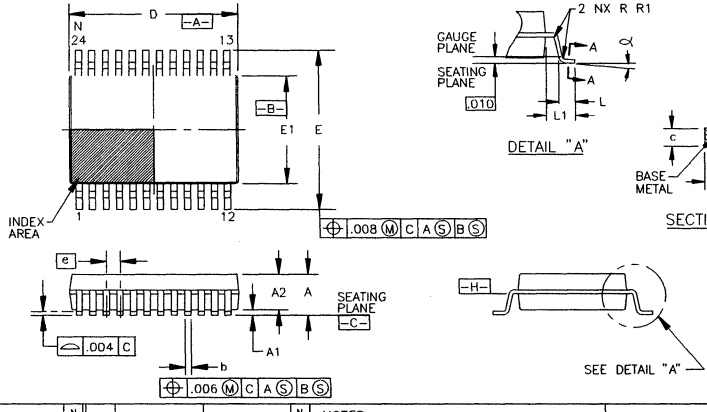


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.079	--	2.00	
A1	.002	--	0.05	--	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	
c	.004	.010	0.09	0.25	
D	.272	.295	6.90	7.50	
E	.291	.323	7.40	8.20	
E1	.196	.220	5.00	5.60	
e	.0256	BASIC	0.65	BASIC	
L	.018	.037	0.45	0.95	
L1	.047	.055	1.20	1.40	
N	20		20		
θ	0°	8°	0°	8°	

NOTES:

PACKAGE NUMBER: ZZ334-1 | REV.: A
JEDEC NUMBER: NONE

Package Number 338 - 24-Lead SSOP, .209 Wide



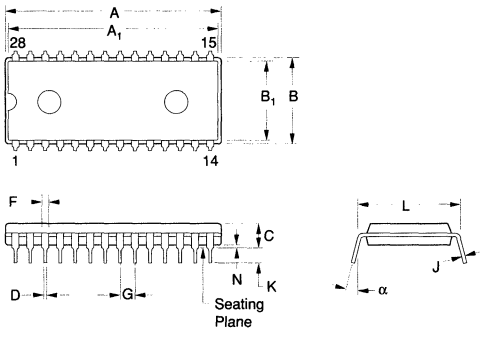
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.079	--	2.00	
A1	.002	--	0.05	--	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	3,7
c	.004	.010	0.09	0.25	7
D	.311	.335	7.90	8.50	2
E	.291	.323	7.40	8.20	
E1	.197	.220	5.00	5.60	2
e	.0256	BASIC	0.65	BASIC	
L	.022	.037	0.55	0.95	4
L1	.049	REF	1.25	REF	
N	24		24		5
α	0°	8°	0°	8°	
R1	.004	--	0.09	--	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH (0.20mm) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13mm) TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH (0.07mm) AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM "C".
5. N IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSSHATCHED AREA.
7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

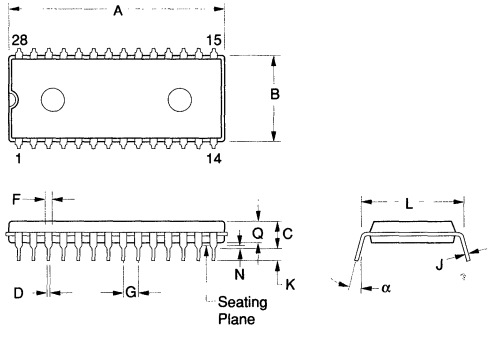
PACKAGE NUMBER: ZZ338 | REV.: A
JEDEC NUMBER: MO-150-AG

Package Number 800 — 28-Pin Plastic, DIP



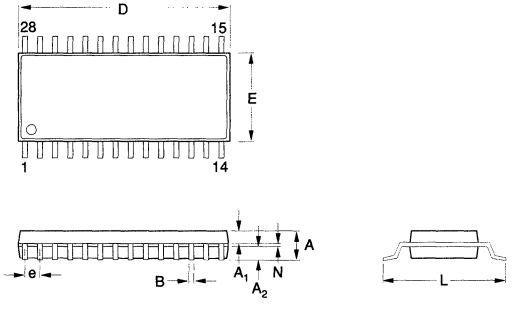
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	1.441	—	36.60
A_1	1.402 TYPICAL		35.6 TYPICAL	
B	—	.236	—	14.6
B_1	.528 TYPICAL		13.4 TYPICAL	
C	—	.224	—	5.70
D	.016	.017	0.42	0.44
F	.047 BASIC		1.20 TYPICAL	
G	.090	.110	2.29	2.79
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.600 BASIC		15.24 BASIC	
α	0°	15°	0°	15°
N	.020	—	0.51	—

Package Number 801 — 28-Pin Plastic DIP



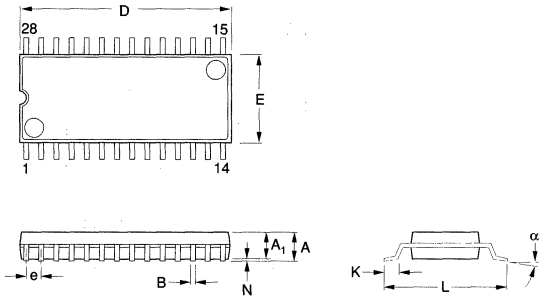
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.417	1.449	36.00	36.80
B	.516	.539	13.10	13.70
C	—	.224	—	5.70
D	.015	.023	0.38	0.58
G	.100 TYPICAL		2.54 TYPICAL	
J	.006	.014	0.15	0.35
K	.098	—	2.50	—
L	.600 TYPICAL		15.24 TYPICAL	
N	.020	—	0.50	—
Q	—	.224	—	5.70
α	0°	15°	0°	15°

Package Number 804 — 28-Pin Plastic SOIC



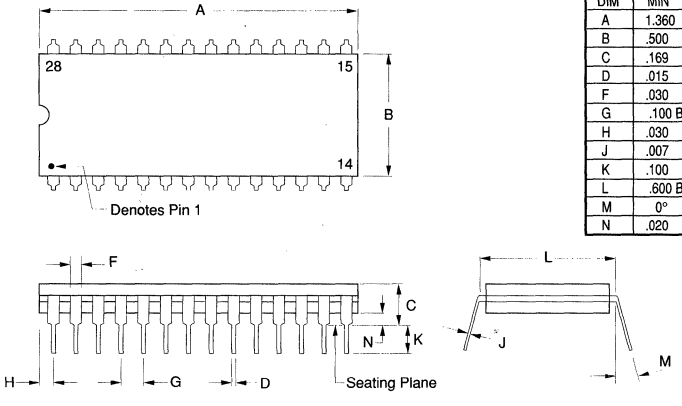
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.093	.104	2.31	2.39
A_1	.050 BASIC		1.045 BASIC	
A_2	.050 BASIC		1.045 BASIC	
B	.0095	.012	0.35	0.48
D	.697	.712	17.81	18.06
E	.292	.299	7.42	7.62
e	.050 BASIC		1.27 BASIC	
N	.016	.050	0.23	0.32
L	.398	.414	10.11	10.51

Package Drawing 805 — 28-Pin Plastic SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	.118	—	3.00
A_1	.096	.108	2.45	2.75
B	.012	.020	0.30	0.50
D	.709	.732	18.00	18.60
E	.323	.339	8.20	8.60
e	.050 TYPICAL		1.27 TYPICAL	
K	.039 BASIC		1.00 BASIC	
L	.449	.480	11.40	12.20
N	.000	.008	0.00	0.20
α	0°	10°	0°	10°

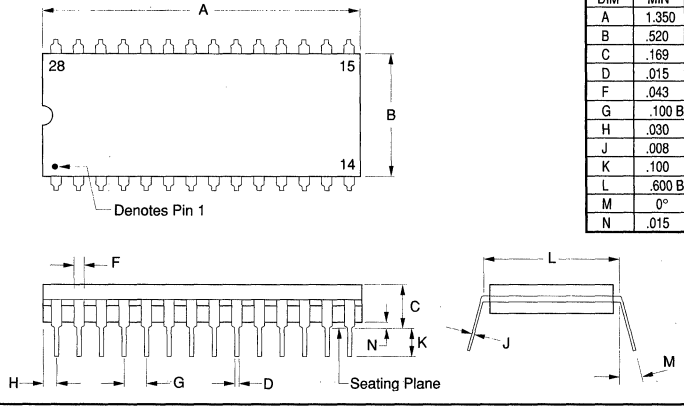
Package Number 904 — 28-Pin Ceramic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.360	1.470	34.54	37.34
B	.500	.590	12.70	14.99
C	.169	.200	4.29	5.08
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.015	0.18	0.38
K	.100	.150	2.54	3.81
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.020	.090	0.51	2.29

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.

Package Number 905 — 28-Pin Plastic, Dual-Wide DIP

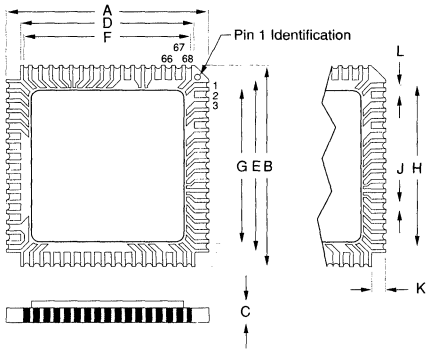


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.350	1.470	34.29	37.34
B	.520	.575	13.21	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.065	1.09	1.65
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.150	2.54	3.81
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.015	.040	0.38	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package.

Package Number 906

TOP VIEW

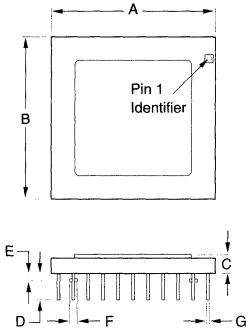


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.945	.965	24.003	24.511
B	.945	.965	24.003	24.511
C	.076	.094	1.934	2.388
D	.841	.859	21.361	21.819
E	.841	.859	21.361	21.819
F	.755	.785	19.177	19.939
G	.755	.785	19.177	19.939
H	.800 BASIC		20.320 BASIC	
J	.027	.033	.686	.838
K	.045 BASIC		1.143 BASIC	
L	.050 BASIC		1.270 BASIC	

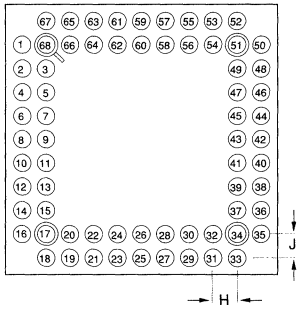
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.
TERMINATION: Gold plated nickel on refractory metallization.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 4.37 grms (0.124 oz)

Package Number 907

TOP VIEW



Bottom VIEW



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.095	.120	2.413	3.048
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100 BASIC		2.540 BASIC	
J	.100 BASIC		2.540 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.
TERMINATION: Gold plated KOVAR.
CASE: Ceramic with gold plated nickel lid.
HERMETICITY: Gross leak test.
WEIGHT: 9 grms (0.32 oz)

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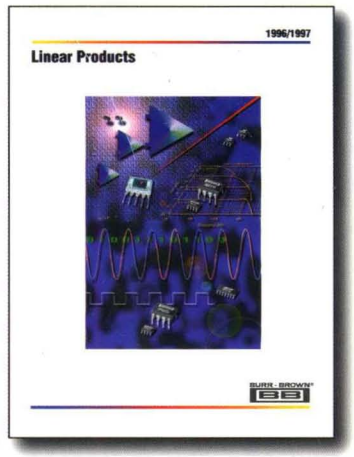

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