

CHIPS

**SHORT
FORM
CATALOG**

1990

Chips and Technologies, Inc. is the world's leading supplier of proprietary VLSI hardware and integrated software solutions for high performance microcomputer systems based on evolving industry standard architectures.

This catalog contains an overview of Chips' product offering, spanning entry level, midrange, and high-performance applications in notebook, laptop and desktop computers.

For more detailed information on Chips' products, please complete the order form found in the back of this catalog or contact the Chips' representative in your area.

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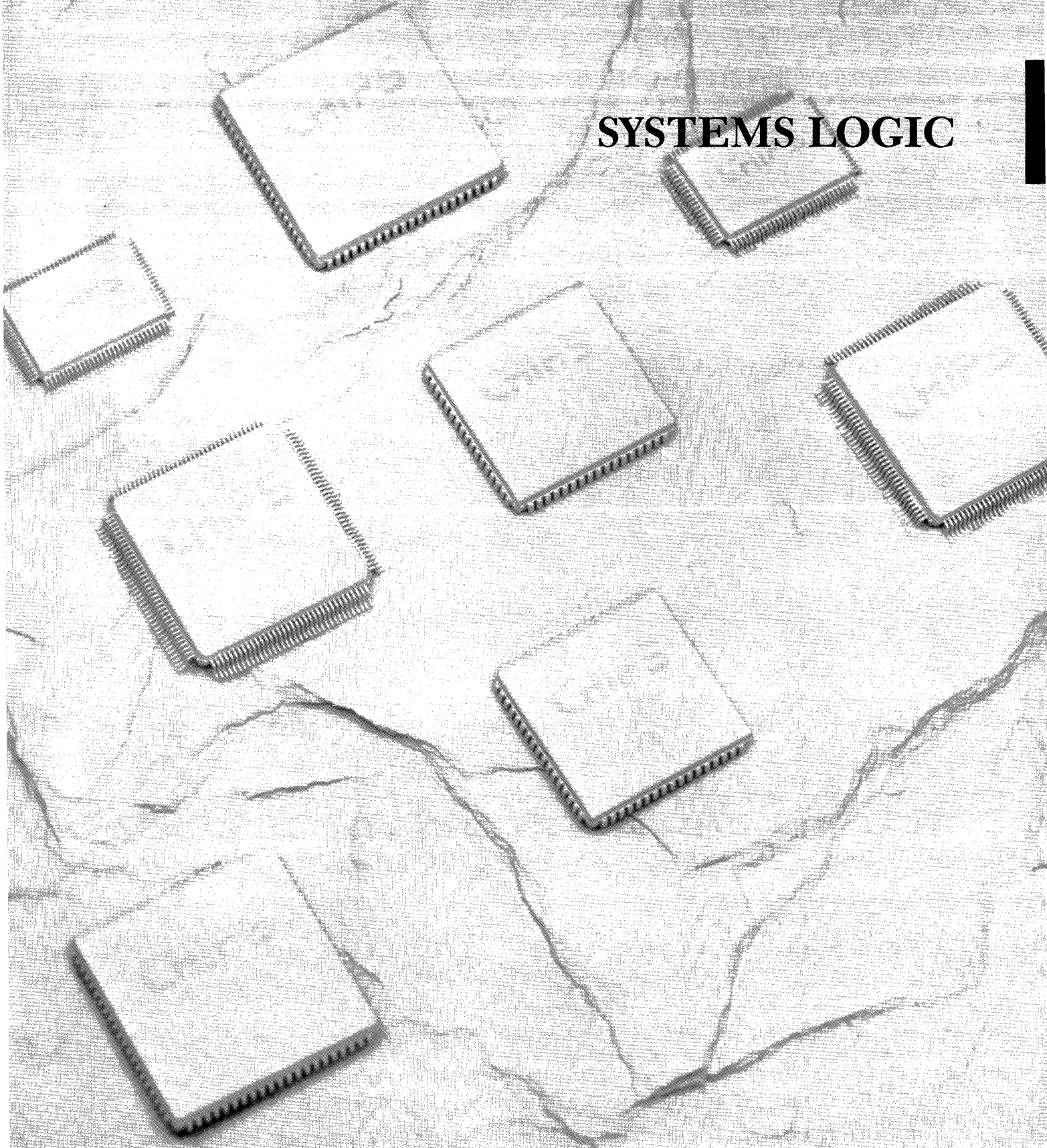
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CHIPS

SYSTEMS LOGIC



**CS8220: PC/AT COMPATIBLE CHIPSet
82C201, 82C201-10/82C202/82A203/82A204/82A205**

- Fully IBM®PC/AT Compatible
- Flexible Architecture allows usage in any iAPX 286 Design
- Early ALE Generation
- Early RAS Generation
- Low Power CMOS Process Technology for 82C201 and 82C202, and Advance Low Power Schottky Process Technology for 82A203, 82A204 and 82A205
- 10 or 8 MHz with One Wait State or 6 MHz with Zero Wait State Capability
- Complete System Board Memory Decode
- Configurable RAM Selects
- 16 Bit to 8 Bit Conversion Logic
- Variable Wait State Selection
- 24 mA Sink and -3.3 mA Source Current for System Bus outputs
- Single 5 Volt Supply

The CS8220 PC/AT compatible CHIPSet is a 5 chip LSI implementation of most of the MSI/SSI logic used to control the IBM Personal Computer AT. The flexible architecture of the CHIPSet allows it to be used in any iAPX 286 based system design. The 82C201 and 82C202 perform the functions of the Intel 82284 Clock Generator and Ready Interface, 82288 Bus Controller for iAPX286 processors, 8284A Clock Generator and Driver, and replace 30 other MSI/SSI devices in the IBM PC/AT design. Significant new features have been added to enhance system performance while still maintaining PC/AT compatibility

The 82C201 is the standard 8 MHz device. The 82C201-10 will operate with a system clock frequency of 10 MHz.

Two signals, ALE and RAS can be altered with the activation of the Early Mode select line

(EMODE). When EMODE is low, both signals become valid before the normal ALE and RAS signals. This allows the use of 120nsec DRAMS in a 6MHz zero wait state system or 150nsec DRAMS in a 8 MHz one wait state system. The 10 MHz one wait state system using 82C201-10 will require 120nsec DRAMS. Variable wait state selection is also provided to accommodate slower memories and peripherals where necessary.

The 82A203, 82A204, and 82A205 include most of the buffers and drivers required in an IBM PC/AT compatible design. Advanced Schottky Bipolar process technology is used to implement these devices, allowing high speed and high source (-3.3mA) and sink (24mA) current capability.

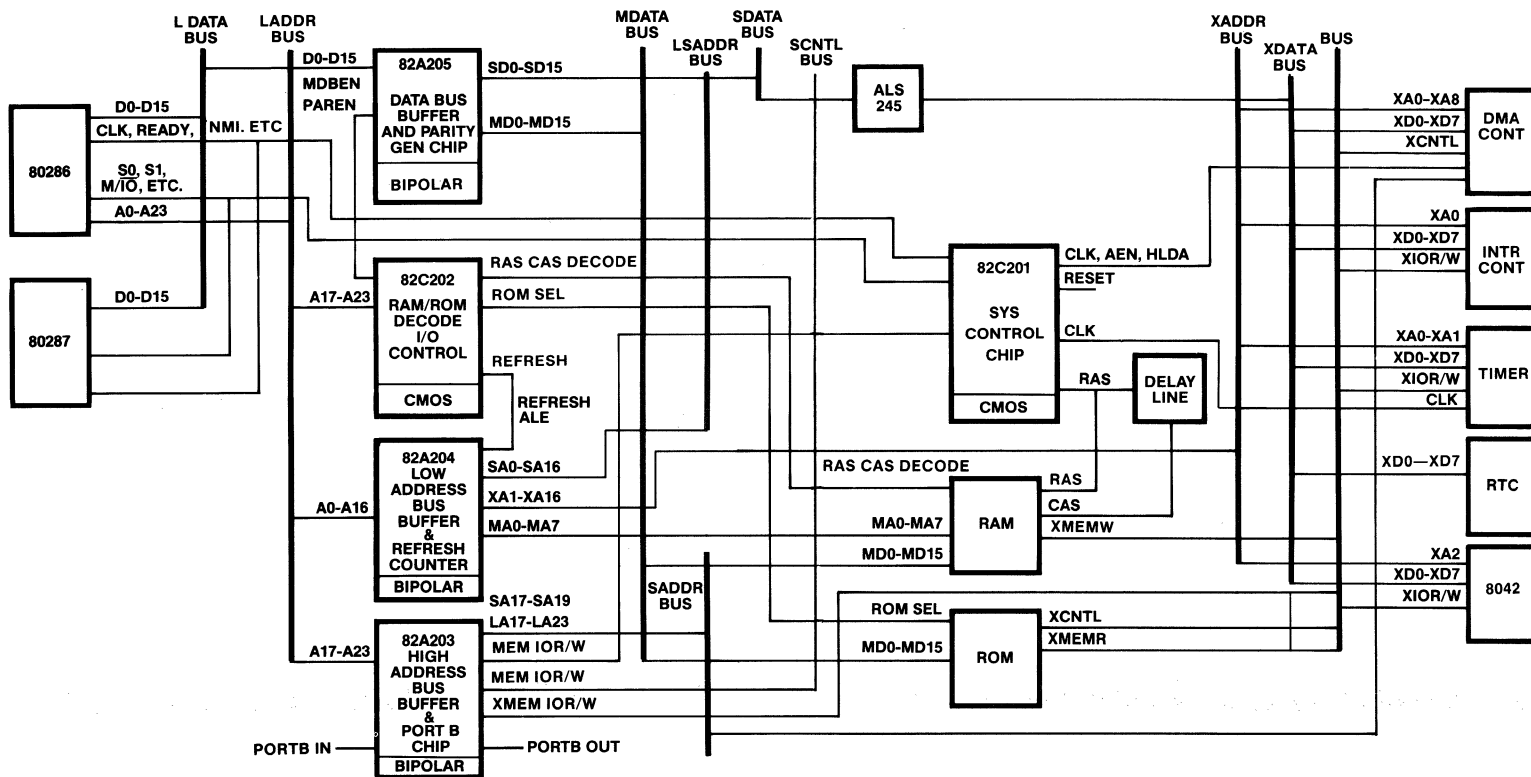


Figure 1. CS8220 PC/AT Block Diagram

CS8221 NEW ENHANCED AT (NEAT) CHIPSet 82C211/82C212/82C215/82C206 (IPC)

- 100% IBM PC/AT Compatible New Enhanced CHIPSet for 12 MHz to 16 MHz systems
- Supports 16 MHz 80286 operation with only 0.5-0.7 wait states for 100ns DRAMs and 12 MHz operation with 150ns DRAMs, 0 wait state 12 MHz operation with 80ns DRAMs
- Separate CPU and AT Bus clocks
- Page Interleaved Memory supports single bank page mode, 2 way and 4 way page interleaved mode
- Integrated Lotus®-Intel®-Microsoft® Expanded Memory Specification (LIM EMS™) Memory Controller Supports EMS 4.0
- Software Configurable Command Delays, Wait states and Memory Organization
- Optimized for OS/2 operation
- Shadow RAM for BIOS and video ROM to improve system performance
- Complete AT/286 system board requires only 28 logic components plus memory and processor
- Targeted at Desktop PC/ATs, Laptops and CMOS Industrial Control Applications
- Available as four CMOS 84-pin PLCC or 100-pin PFP components.

The CS8221 PC/AT compatible NEAT CHIPSet is an enhanced, high performance 4 chip VLSI implementation (including the 82C206 IPC) of the control logic used on the

IBM PC/AT. The flexible architecture of the NEAT CHIPSet allows it to be used in any 80286 based system.

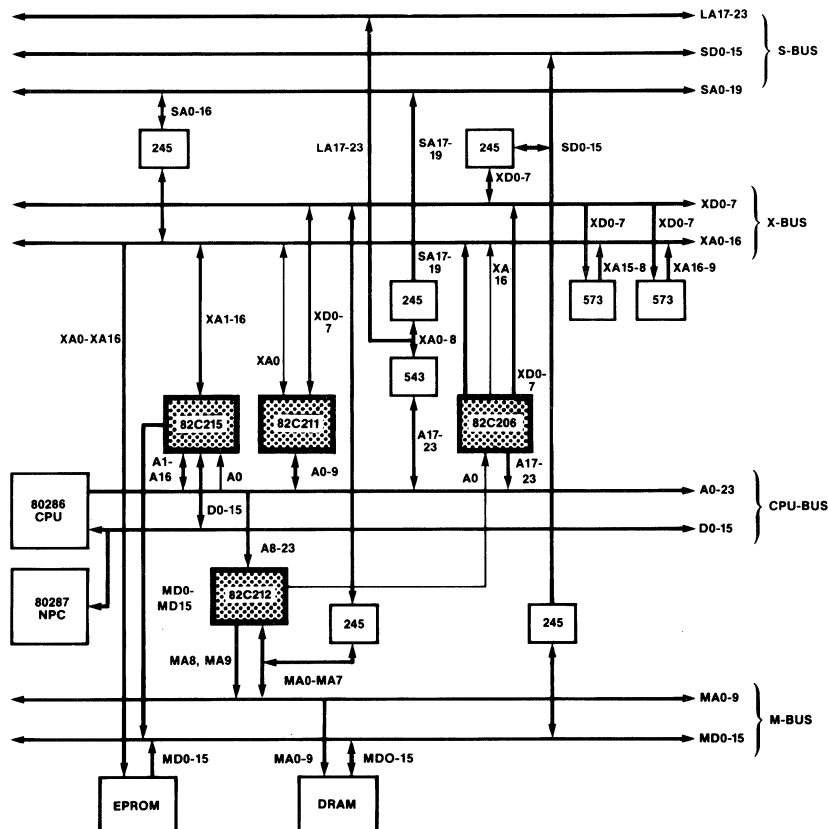


Figure 1. CS8221 NEAT Block Diagram

The CS8221 NEAT CHIPSet provides a complete 286 PC/AT compatible system, requiring only 24 logic components plus memory devices.

The CS8221 NEAT CHIPSet consists of the 82C211 CPU/Bus controller, the 82C212 Page/Interleave and EMS Memory controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEAT CHIPSet supports the local CPU bus, a 16 bit system memory bus, and the AT buses as shown in the NEAT System Block Diagram. The 82C211 provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and the user selectable AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

The 82C212 Page/Interleave and EMS Memory controller provides an interleaved memory sub-system design with page mode operation. It supports up to 8 MB of on-board DRAM with combinations of 64Kbit, 256Kbit and 1Mbit DRAMs. The processor can operate at 16MHz with 0.5-0.7 wait state memory accesses, using 100 nsec DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM, by downloading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution. In a DOS environment, memory above 1Mb can be treated as LIM EMS memory.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU

address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

The 82C206 Integrated Peripherals Controller is an integral part of the NEAT CHIPSet. It is described in the 82C206 Integrated Peripherals Controller data book.

System Overview

The CS8221 NEAT CHIPSet is designed for use in 12 to 16 MHz 80286 based systems and provides complete support for the IBM PC/AT bus. There are four buses supported by the CS8221 NEAT CHIPSet as shown in Figure 1: CPU local bus (A and D), system memory bus (MA and MD), I/O channel bus (SA and SD), and X bus (XA and XD). The system memory bus is used to interface the CPU to the DRAMs and EPROMs controlled by the 82C212. The I/O channel bus refers to the bus supporting the AT bus adapters which could be either 8 bit or 16 bit devices. The X bus refers to the peripheral bus to which the 82C206 IPC and other peripherals are attached in an IBM PC/AT.

Notation and Glossary

The following notations are used to refer to the configuration and diagnostics registers internal to the 82C211 and 82C212:

REGnH denotes the internal register of index n in hexadecimal notation.

REGnH<x:y> denotes the bit field from bits x to y of the internal register with index n in hexadecimal notation.

**CS8223/CS8283 LeAPset/LeAPset-sx CHIPSet
LAPTOP SUPPORT CIRCUITS**

- Part of a complete laptop solution from Chips and Technologies
- Optimized power conservation
 - Sleep mode for short intervals of power reduction
 - Stand-by mode for maximum power savings
 - Support for slow refresh DRAMs
 - Software selectable operating frequency
 - Auto-power off for display backlight
 - Power-on at user request, after a programmable interval or in response to a modem ring
- 100% PC/AT compatible
- Supports both the '286/'C286 and the '386SX
- Multiple speeds: 12, 16 and 20 MHz
- Optimizations for OS/2™
- Full support for EMS 4.0
- High-performance, low-power memory controller
 - Page interleaving increases performance
 - Slow access DRAMs reduce costs
 - Slow refresh DRAMs reduce power consumption
- Backward-compatible with NEAT CHIPSet
- Compatible with other members of CHIPS' laptop solutions
 - 82C455 Flat Panel/CRT VGA Controller
 - 82C456 Advanced Flat Panel/CRT Controller
 - 83C601 Multifunction Controller
- Convenience features
 - Security password support
 - ROM/RAM card

The LeAPset package of integrated circuits is the first complete solution for full-function battery-powered portable computers. All of the CPU and AT bus control functions, memory control logic, VGA graphics, peripheral support and special laptop features are integrated into 6 CMOS flat-pack devices.

LeAPset CS8223 supports the 80286 and the 802C286 while LeAPset-sx CS8283 supports the 80386SX. Both work together with the 82C601 Multifunction Controller, the 82C455 Flat Panel/CRT VGA Controller and the 82C456 Advanced Flat Panel/CRT Controller. Using the LeAPset solution, a complete laptop motherboard requires a total of only 29 ICs plus memory.

Four chips are included in the LeAPset system controller circuits: the 82C242 data/address buffers and bus conversion logic, the 82C636 Power Control Unit (PCU) and the 82C206 Integrated Peripheral Controller (IPC) and the appropriate CPU/bus/memory controller. The

82C241 is the CPU controller used with the '286 and contained in the CS8223. The 82C841 is the CPU controller used with the '386SX and contained in the CS8283.

Power Saving Features

Both CHIPSets support features tailored for laptops, such as power conservation features to increase battery life. Such features include sleep mode, stand-by mode and automatic shut-off for power-hungry devices.

In sleep mode, clocks to static devices (such as the 'C286) are shut off. Clock to dynamic devices (such as the '386SX) are reduced to the 1/2, 1/4 or 1/8 of normal operating frequency.

In stand-by mode, all devices except DRAM and memory controller chips are powered off; DRAM chips are refreshed. The state of the machine, including the display buffer, can be saved in battery-backed slow refresh DRAMs. After the user strikes the power switch, a

programmed interval or the telephone lines to the modem ring, power is turned back on, state is restored and the application can be resumed where it was left off.

Power-hungry subsystems such as the display backlight can be automatically shut off. For example, if the user does not strike a key within a programmed interval, the LeAPset PCU will automatically turn off power to the backlight. If the power has been shut off, power is restored as soon as the user strikes any key.

Board Space

When using the LeAPset system, the designer can take advantage of several features to help reduce space on the main system board. For example, both system and VGA BIOS can be squeezed into a single 128 kilobyte EPROM. In addition there are several programmable decoders that can be used to replace external SSI for decoding addresses to subsystems on the motherboard. All LeAPset circuits are packaged in space-saving surface mount flat packs.

Performance Features

The LeAPset circuits are backward-compatible with the NEAT CHIPSet CS8221; all

LeAPset internal registers are a superset of NEAT registers. As a result, all of the performance features that have been designed into the NEAT CHIPSet are available for laptops. These features include optimization for OS/2, 2-way and 4-way page interleaving, shadow RAM and software-selectable command delays, wait states and memory organizations, and 4 on-chip EMS page registers.

Complete Solutions

Because optimum designs must take into account system-wide issues, CHIPS offers complementary integrated circuits and services. The 82C455 VGA Flat Panel/CRT Controller and the 82C456 Advanced VGA Flat Panel/CRT Controller drive LCD, gas plasma, electroluminescent displays as well as CRTs. Both provide 100% compatibility with IBM VGA along with intelligent color to gray scale conversion and power save modes. The 82C601 Single Chip Peripheral Controller is also 100% IBM compatible and contains 2 UARTs, one bi-directional parallel port and an IDE hard disk interface. In addition, CHIPS offers ready-made BIOS as well as software and hardware design services.

CS8230 386/AT CHIPSet
82C301 BUS CONTROLLER
82C302 PAGE/INTERLEAVE MEMORY CONTROLLER
82A303 HIGH ADDRESS BUFFER
82A304 LOW ADDRESS BUFFER
82B305 DATA BUFFER
82A306 CONTROL BUFFER

The CS8330-16,20,25 AT/386 CHIPSet is a seven chip VLSI implementation of most of the system logic to control an iAPX 386™ based system. The CHIPSet is designed to offer a 100% PC/AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

CS8230 CHIPSet combined with CHIPS 82C206, Integrated Peripherals Controller, provides a complete PC/AT compatible system using only 40 components plus memory devices.

The CS8230 CHIPSet consists of one 82C301 Bus Controller, one 82C302 Page/Interleave Memory Controller, one each of 82A303 and two 82A304 Address Bus Interfaces, two 82A305 or 82B305 Data Bus Interfaces, and a 82A306 Control Signal Buffer. An all CMOS CS8232-16 and CS8232-20 CHIPSet allow OEM's to reduce the form factor, size and weight of their portable and laptop machines due to the CHIPSets' reduced power cooling and buffering requirements. In particular, the all CMOS CS8232-16 and CS8232-20 CHIPSet will reduce a system's power consumption requirement by at least half that of an NMOS/BIPOLAR/CMOS based system.

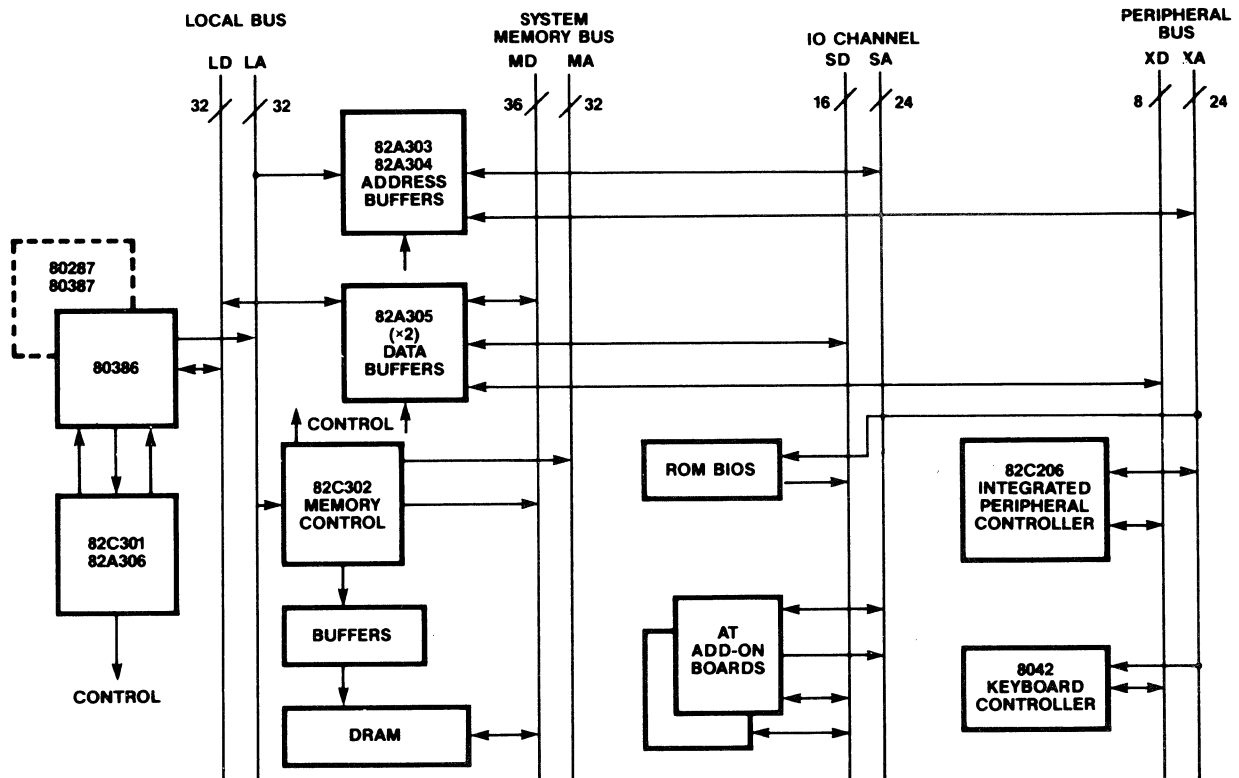


Figure 1. CS8230 AT/386 Block Diagram

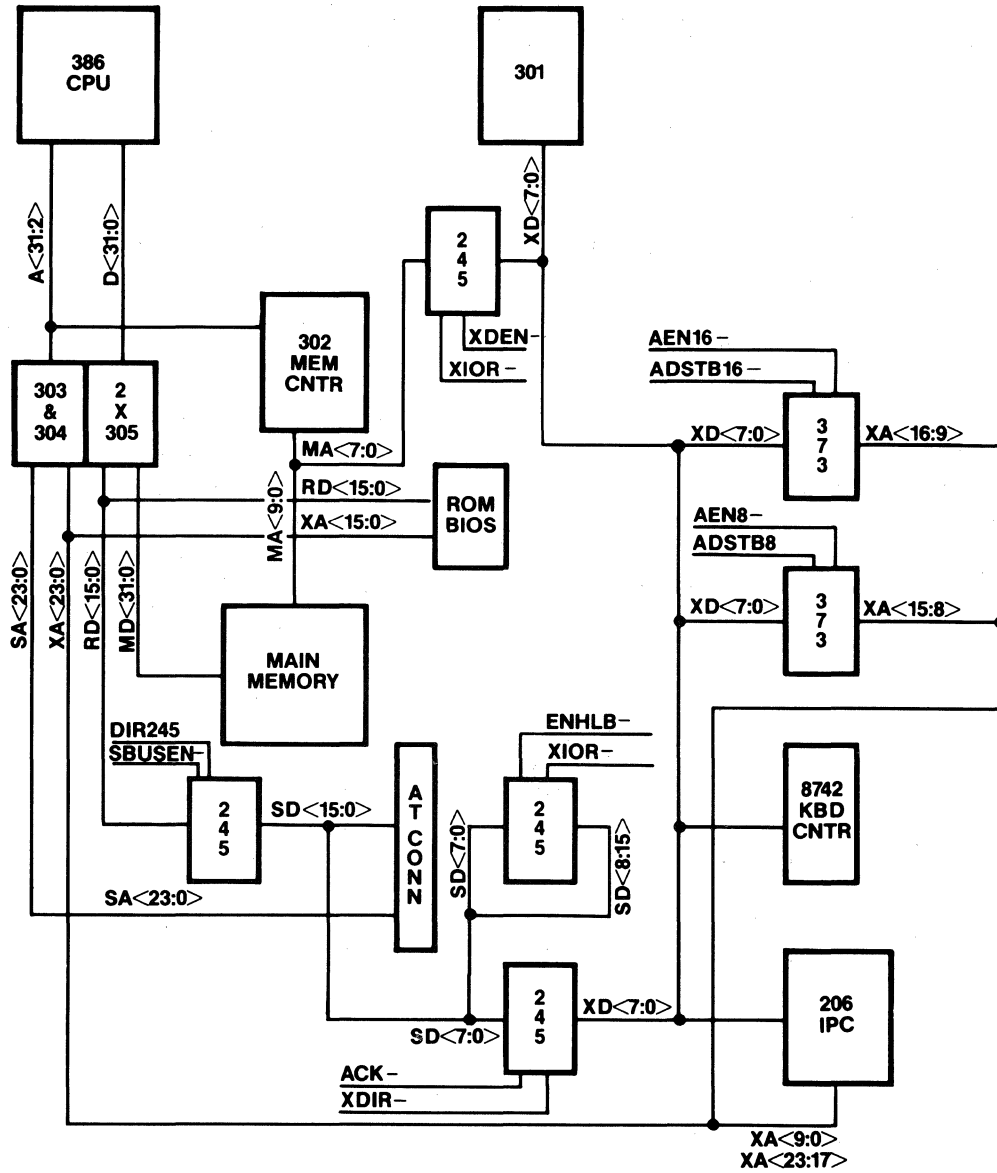


Figure 2. CS8230 AT/386 Detailed Block Diagram

CS8231: TURBO CACHE-BASED 386/AT CHIPSet
82C301 BUS CONTROLER
82A303 HIGH ORDER ADDRESS BUFFER
82A304 LOW ORDER ADDRESS BUFFER
82B305 DATA BUFFER
82A306 CONTROL BUFFER
82C307 INTEGRATED CACHE/DRAM CONTROLLER

The CS8231 **TURBO CACHE BASED** 386/AT CHIPSet is a seven chip VLSI implementation of most of the system logic to implement a **CACHE BASED** iAPX 386 based system. The CHIPSet is designed to offer a 100% AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX 386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

The CS8231 CHIPSet combined with CHIPS' 82C206, Integrated Peripherals Controller, provides a complete PC/AT compatible system using only 40 components plus memory devices.

The CS8231 CHIPSet consists of one 82C301

Bus Controller, one 82C307 Integrated CACHE/DRAM controller, one each of 82A303 and 82A304 Address Bus Interfaces, two 82B305 Data Bus Interfaces, and one 82A306 Control Signal Buffer.

The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the system diagram below. The 82C301 and 82A306 provide the generation and synchronization of control signals for all buses. The 82C301 also supports an independent AT bus clock and allows for dynamic selection of the processor clock between the 16 MHz, 20 MHz, or 25 MHz clocks and the AT bus clock. The 82A306 provides buffers for bus control signals in addition to other miscellaneous logic functions.

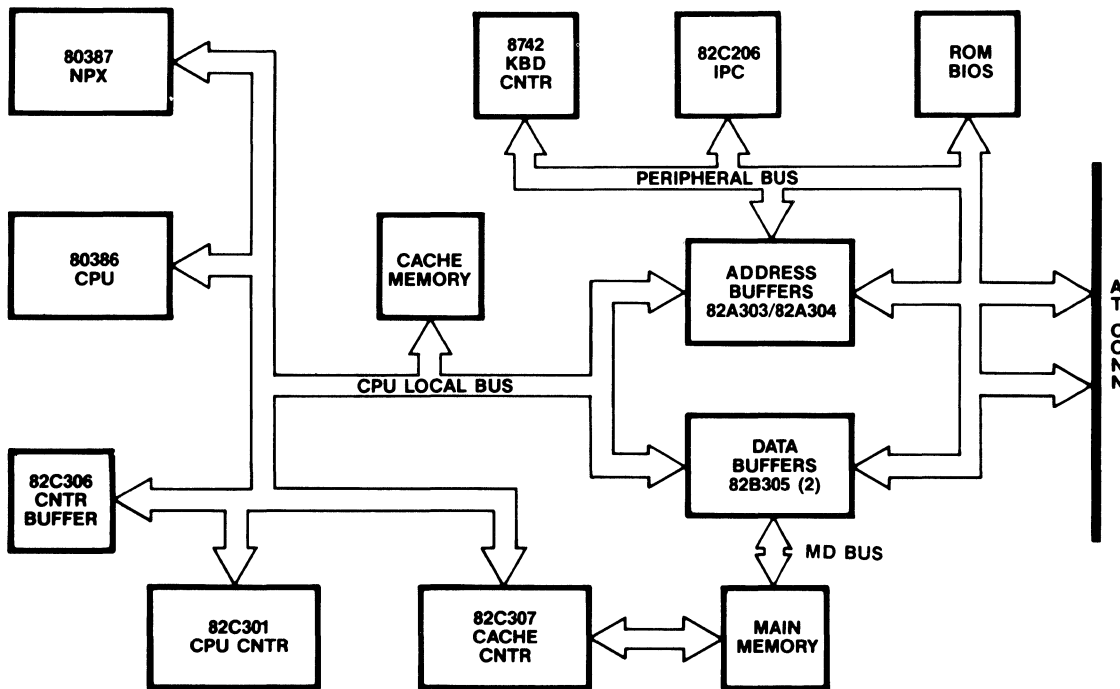


Figure 1. CS8231 Turbo Cache Based 386/AT Block Diagram

The 82C307 is a high performance and high integration CACHE/DRAM controller designed to interface directly to the 80386 microprocessor. It maintains frequently accessed code and data in high speed memory, allowing the 80386 to operate at its maximum rated frequency with near zero waitstates. By integrating DRAM control functions on-chip, it supports simultaneous activation of cache and DRAM access, thereby minimizing the cache miss cycle penalty. It has hardware support to allow the user to designate up to four blocks (of variable size from 2KB to 128KB) of main memory as non-cacheable address space. This feature is important for compatibility issues when operating in a multiprocessing or LAN environment, or where dual-port memory is used, and to designate certain regions of video RAM as non-cacheable. This feature eliminates the need to use very fast PALs externally to decode non-cacheable regions and gives the user much more flexibility. Optional EDC support logic is integrated on to the 82C307 which allows it to interface to any of the generically available 32-bit Error Detection

and Correction Circuits to realize a highly reliable memory subsystem.

Cache coherency is maintained during DMA cycles by channeling all accesses through the cache controller logic. During DMA read operations, the cache RAM is not accessed and data is retrieved from the main memory. During DMA write operations, if a cache hit is detected, the cache RAM is updated and the corresponding tag validated. Cache coherency is maintained at all times, with no performance penalty. The 82C307 is available in a 100 pin PFP package.

The 82A303 and 32A304 interface between all address buses, and the addresses needed for proper data path conversion. Two 82B305 are used to interface between the local, system memory, and at data buses. In addition to having high current drive, they also perform the conversion necessary between the different sized data paths.

CS8233: PEAKset/386 CHIPSet
82C311 CPU/CACHE/DRAM CONTROLLER
82C315 BUS CONTROLLER
82C316 PERIPHERAL CONTROLLER

- **100% IBM PC/AT Compatible CACHE BASED 386/AT Compatible CHIPSet**
- **Supports 16, 20, 25, 33 and 40 MHz 80386 based Systems**
- **Independent clock to support correct AT bus timing (SYSNC/ASYNC AT bus clock option)**
- **Flexible architecture allows usage in any iAPX 386 design**
- **A Complete 386/AT CACHE BASED PC/AT Compatible now requires only 19 IC's plus memory**
- **Integrates Cache Directory and CPU/CACHE/DRAM CONTROLLER on a single chip to provide PEAK Integration and PEAK performance**
- **Integrated CPU/CACHE/DRAM Controller enhances 80386 CPU and memory system performance**
 - **Averages to nearly zero wait state memory access**
 - **Zero wait state non-pipelined/pipelines read hit access**
 - **Zero wait state non-pipelined/pipelined write access**
 - **Buffered-write through DRAM update scheme to minimize write cycle penalty**
- **Supports 32KB, 64KB, and 128KB two-way set associative cache organization**
 - **64 byte line size**
 - **4 byte sub-line size with associative valid bit**
 - **Supports 4 blocks (of variable size**
- **4KB to 4M) of main memory as non-cacheable address space**
- **Supports caching of data and code**
- **Supports control mechanism for preventing unnecessary disturbance of cache contents during I/O operation**
- **Tightly coupled 80386 interface**
 - **Designed to interface directly with the 80386**
 - **Supports 16, 20, 25, 33, and 40 MHz operation**
 - **Integrated support for 80387 and Weitek 3167 co-processor**
- **DRAM Controller supports page mode operation**
- **Flexible memory architecture**
 - **Supports memory configurations up to 128 MB**
 - **Programmable wait states**
 - **Supports 256K, 1MB, and 4MB DRAMs in configurations of up to 4 blocks and 8 banks**
 - **Supports static column mode DRAMs**
 - **Supports staggared RAS during refresh**
 - **Supports hidden refresh and burst refresh**
 - **Supports 256K/512K/1M PROMs**
- **Supports shadowing of BIOS EPROMs**
- **Cache hit rate up to 99%**
- **Includes interface logic to support the 82C636 Power Control Unit (PCU) for very high-performance 386/AT based laptops and portables**

The CS8233 PEAKset/386 is a three chip VLSI implementation of most of the system logic required to implement a CACHE BASED iAPX 386 based system. The CHIPSet is designed to offer a 100% PC/AT compatible

integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX 386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

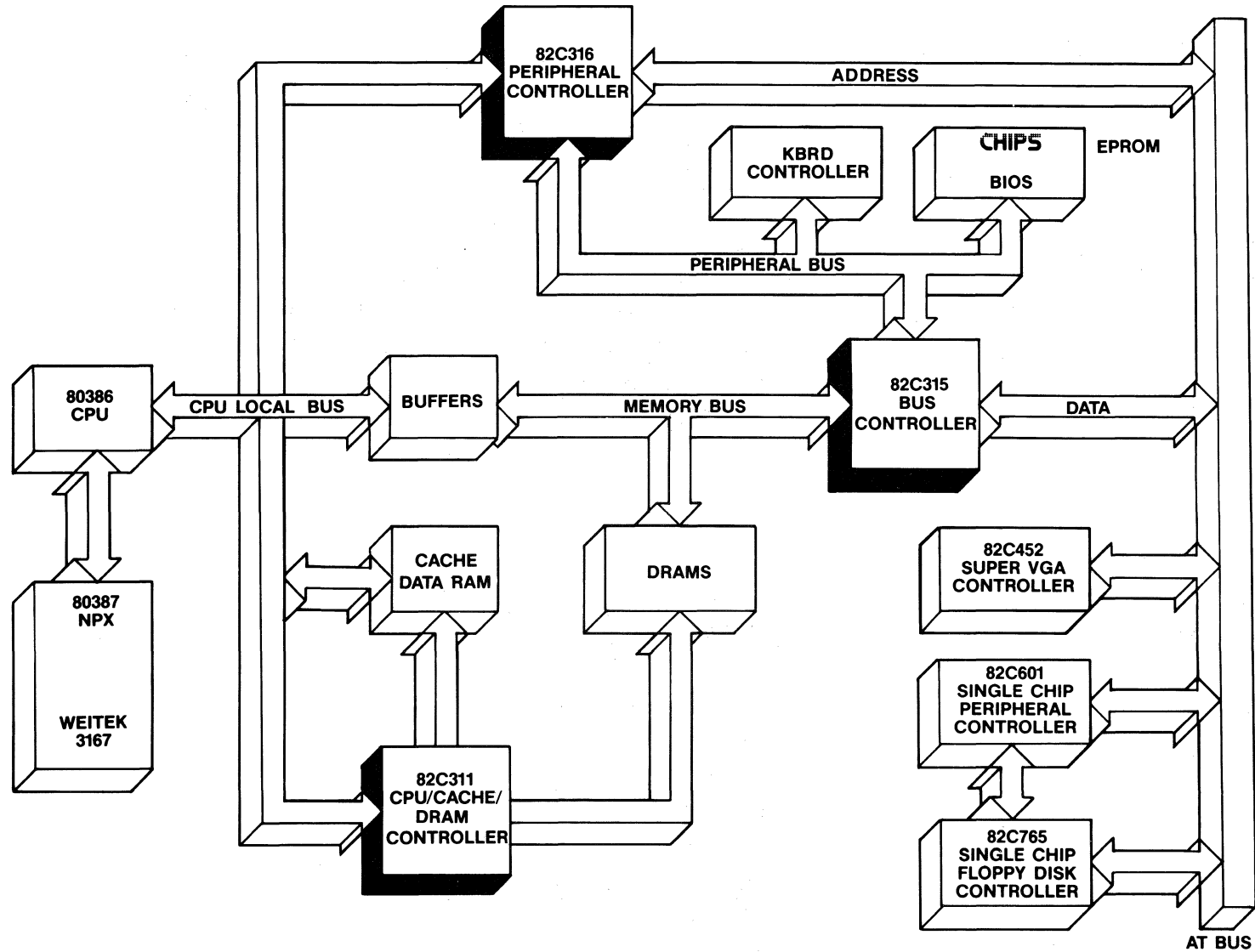


Figure 1. CS8233 PEAKset/386 Block Diagram

CS8281: NEATsx CHIPSet NEW ENHANCED AT CHIPSet FOR THE 386SX

- 100% IBM PC/AT Compatible New Enhanced CHIPSet for the 386SX micro-processor
- Supports 387SX coprocessor
- Supports 16 MHz, 20 MHz and beyond with only 0.5 – 0.7 wait states
- Single bank, 2-way and 4-way interleaved paging with 100 ns DRAMs for 16 MHz
- Supports the full EMS 4.0 with on-chip or off-chip EMS page registers
- Optimized for OS/2 operations
- Shadow RAM for AT BIOS and graphics BIOS for improved performance
- Complete AT/386SX system board requires 24 logic components
- Four CMOS components available in 84-pin PLCC or 100-pin QFP packages

The CS8281 NEATsx CHIPSet is an enhanced, high performance 4 chip VLSI implementation of the control logic to build PC/AT compatibles based on the 386SX micro-processor.

Based on the proven NEAT CHIPSet architecture, NEATsx provides a complete 386SX AT system board with 24 components plus memory devices.

The CS8281 CHIPSet is optimized for OS/2™ and will run OS/2 applications as fast as equivalent PS/2 systems. The CHIPSet also supports fast task switching under DOS™ environment. Besides the on-chip 4 EMS page registers, NEATsx supports up to 512 page registers in hardware. There is a hook to external EMS Mapper chips which can be nested together. Each one of these mapper chips carry 128 page registers.

The CS8281 NEATsx CHIPSet consists of the 82C811 CPU/Bus controller, the 82C812 the Page interleave/EMS memory controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripheral Controller.

Since NEATsx supports asynchronous CPU and AT bus architecture as well as synchronous, the AT bus can be run independent of the CPU bus.

The 82C811 also provides dynamic clock selection between the processor clock and the user selectable AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow and fast peripheral boards.

The advanced memory controller, 82C812 provides an interleaved memory subsystem design with page mode operation. Two banks, four banks can be interleave-paged. Single bank paging using slow memories is also available for cost sensitive memory designs.

The 82C215 Data/Address buffer provides the latching and buffering between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

82C206 is an integral part of the NEATsx CHIPSet. It is explained in detail in the 82C206 data book.

NEATsx CHIPSet will support the 386SX at higher speeds as the processor becomes available at those speeds.

Now, a cost competitive 386SX based AT compatible can be designed with the most advanced NEATsx CHIPSet.

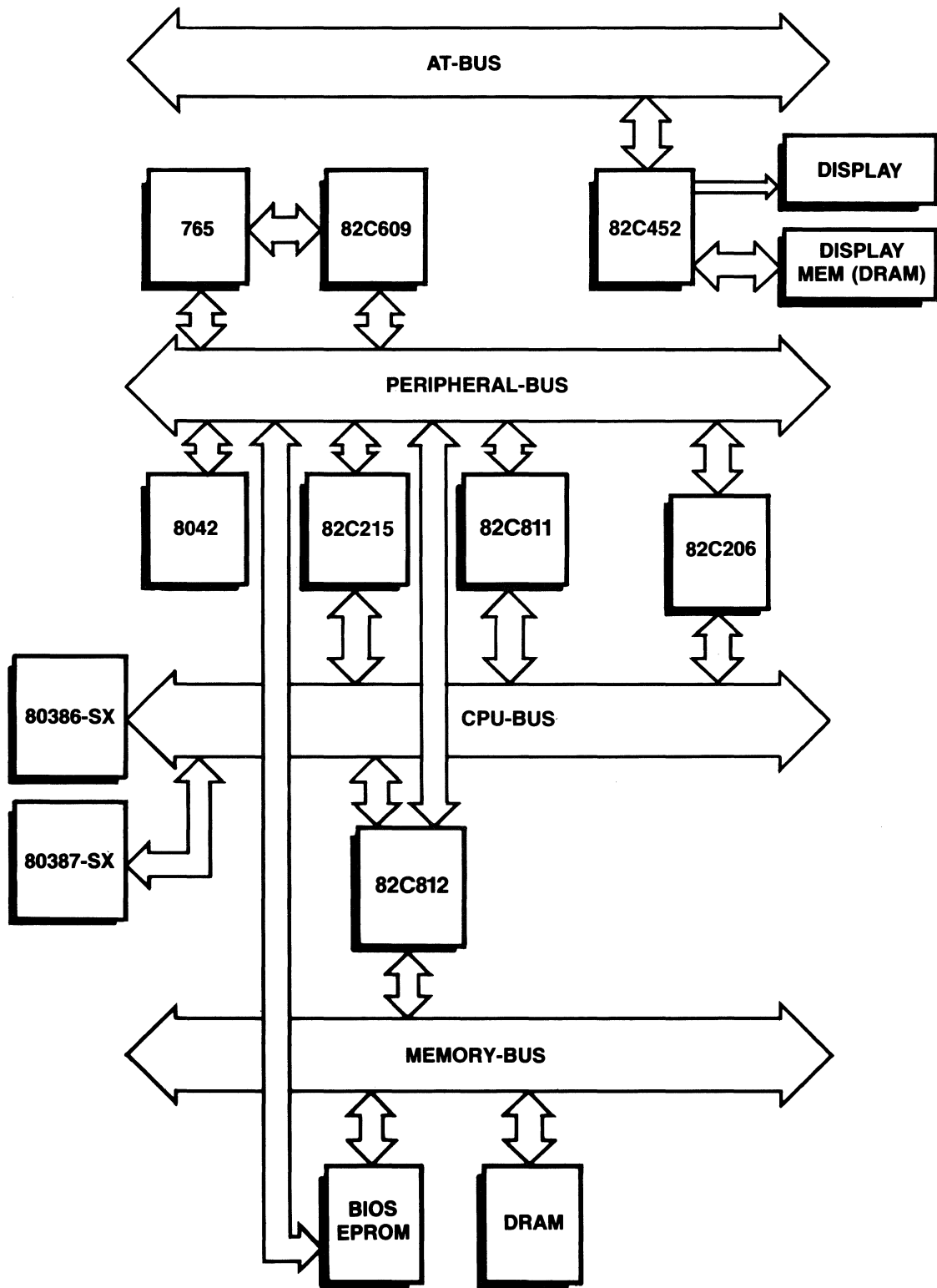


Figure 1. CS8281 NEATsx Based Block Diagram

**CHIPS/250: COMPLETE IBM PS/2
MODEL 50/60 COMPATIBLE CHIPSet
82C221, 82C222, 82C223, 82C225, 82C226, 82C607, 82C451**

- 100% IBM PS/2 Model 50/60 Compatible CHIPSet
- Supports 10, 12, 16 and 20 MHz 80286 based Systems
- Complete IBM PS/2 Model 50 Compatible Mother Board requires 68 components plus memory
- Available as CMOS PLCC and PFP Components
- Integrated Lotus®-Intel®-Microsoft® Expanded Memory Specification (LIM EMS 4.0) Memory Controller expandable to full LIM EMS 4.0 specification with 8 register sets of 64 mapping registers
- High performance, proprietary Matched Memory interface for Micro Channel Memory Adapters

SYSTEM LOGIC CS8225 CHIPSet

- Asynchronous CPU, DMA and Micro Channel Operation
- Advanced Page/Interleave Memory Controller with Integrated Bad Block Remapping Capability, Shadow RAM and LIM EMS 4.0 Support
- Slow DRAMs at high CPU clock speeds, without Wait State penalty - 0.5 to 0.7 wait states with:
 - 150ns DRAMs @ 12.5 MHz
 - 120ns DRAMs @ 16 MHz
 - 80ns DRAMs @ 20 MHz

CHIPS/250 is a 7-chip, Enhanced CMOS implementation of most of the system logic necessary to implement IBM PS/2 Model 50/60 compatible personal computers. CHIPS/250 will enable OEMs to offer PCs that are more functional, more integrated and clearly higher in performance than IBM's Model 50 and Model 60.

CHIPS/250 includes the CS8225 System Logic CHIPSet, the 82C607 Multi-Function Controller with an Analog FDC Data Separator and 16550 compatible serial port, and the Enhanced Gate-Level Compatible 82C451 VGA chip. With these 7 VLSI devices, it requires only 61 additional components plus memory to implement superior PCs to IBM's models.

System Logic CS8225 CHIPSet

The CS8225 System Logic CHIPSet consists of the 82C221 CPU and Micro Channel Controller, the 82C222 Page/Interleave and EMS Memory Controller, the 82C223 DMA Controller, the 82C225 Data/Address Bus Buffer

GRAPHICS

- Enhanced Gate-level Compatible VGA
- High performance, proprietary FAST VGA interface to CPU controller

PERIPHERAL SUPPORT

- Integrated Analog Data Separator and 16550 compatible serial port

and the 82C226 System Peripherals Controller. Each of these 5 components is available in 84-pin PLCC and 100-pin PFP.

The 82C221 CPU and Micro Channel Controller manages the system timing for the asynchronous CPU, DMA and Micro Channel cycles. It supports CPU clock speeds from 10, 12, 16 to 20 MHz. It supports all Micro Channel cycles, along with Matched Memory and Fast VGA cycles. It includes state machines for command and control logic signal generation, DMA and refresh logic control.

The 82C222 Page/Interleave and EMS Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 4 memory banks, with memory configurations from 640KB to 8MB. While operating under DOS, memory above 1MB can be treated as EMS memory, improving significantly the value of the large memory organizations of the OS/2 era. The on-chip EMS logic provides 4 mapping registers, however, with external EMS mappers, the full

LIM EMS 4.0 specification with 8 sets of 64 mapping registers can be implemented.

The 82C223 DMA Controller provides 8 DMA channels for slave devices and the Central Arbitration Control Point (CACP) for the entire system. Each DMA Channel has 24-bit address capability and can perform 8-bit or 16-bit transfers. It also supports Virtual DMA so that DMA Channels 0 and 4 can be used to service multiple DMA slaves by multiplexing the DMA Channels between the arbitration levels assigned to those slaves. It supports Multiple Bus Masters via the CACP arbitrator and control signals which enable Bus Masters to monitor the readiness and data size of other adapters and system board components. The Bus Arbitration logic includes protection mechanisms against error conditions, like burst-mode devices not relinquishing the bus within the specified time.

The 82C225 Data Bus Buffer provides high speed bus switching support to enable the use of low speed DRAMs at high clock speeds.

The 82C226 System Peripherals Controller integrates PS/2 compatible peripherals in one compact package, with an optimized bus interface to the Peripheral Bus. It includes two 8259 compatible interrupt controllers, one 8254 compatible timer, one 146818 compatible real-time clock, 114 bytes of CMOS battery back-up RAM and one PS/2 compatible Bi-directional Parallel Port.

Graphics

The 82C451 Gate Level compatible VGA provides 100% VGA compatible graphics with backwards compatibility to EGA, CGA, MDA and Hercules. In VGA Graphics modes, it provides resolutions from 320 × 200 with 256 colors to 640 × 480 with 16 colors. In VGA text mode, it supports fonts up to 9 × 32. It supports all standard monitors—IBM PS/2 analog, Multi-frequency, EGA, CGA and Monochrome. The 82C451 boosts graphics performance with a tightly coupled high performance interface to the CPU and a 16-bit memory interface. The 82C451 is packaged in a 144 pin PFP package.

Peripheral Support

The 82C607 Multi-Function Controller integrates additional PS/2 compatible peripherals in one compact package. It includes one 16550 Compatible UART, an Analog Data Separator, POS registers and Glue Logic for a NEC 765A Floppy Disk Controller. The 82C607 is available in a 68 pin PLCC package.

Additional components that complement CHIPS/250 are the MicroCHIPS for Micro Channel Adapters and EMS Mapper Chips. The 82C610 and 82C611 MicroCHIPS can be used for I/O intensive Micro Channel Adapters, while the 82C612 is applicable to Adapters that require Slave DMA support.

CHIPS/280: COMPLETE IBM PS/2 MODEL 80 COMPATIBLE CHIPSet 82C321, 82C322, 82C223, 82C325, 82C226, 82C607, 82C452

- 100% IBM PS/2 Model 80 Compatible Chip-set
- Supports 20, 25 and 33 MHz 80386-based Systems
- Complete IBM PS/2 Model 80 Compatible Motherboard requires only 66 components plus memory
- Available as CMOS PFP Components

SYSTEM LOGIC CS8238 CHIPSet

- Asynchronous CPU, DMA and Micro Channel Operation
- Advanced Page/Interleave Memory Controller with Integrated Bad Block Remapping Capability, Shadow RAM and LIM EMS 4.0 Support
- Supports 4Mb DRAMs

GRAPHICS

- Enhanced Gate-level Compatible VGA
- High-performance FAST VGA interface to CPU controller

CHIPS/280 is a 7-chip, enhanced CMOS implementation of most of the system logic necessary to implement IBM PS/2 Model 80 compatible personal computers. CHIPS/280 enables OEMs to offer PCs that are more functional, more integrated and higher in performance than IBM's Model 80.

CHIPS/280 includes the CS8238 System Logic CHIPSet, the 82C607 Multi-Function Controller with an Analog FDC Data Separator and a NS16550-compatible serial port, and the Enhanced Gate-Level Compatible 82C451 VGA chip. With these 7 VLSI devices, it requires only 66 additional components plus memory to implement superior PCs to IBM's models.

- Slow DRAMs at high CPU clock speeds, without wait state penalty: 0.5 to 0.7 wait states with:

- 80ns DRAMs @ 20 MHz
- 80ns DRAMs @ 25 MHz
- 60ns DRAMs @ 33 MHz

- Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS 4.0) Memory Controller expandable to full LIM EMS 4.0 specification with 8 register sets of 64 mapping registers
- High-performance Matched Memory interface for Micro Channel Memory Adapters at 20 MHz, 25 MHz and 33 MHz
- PS/2 Model 80 Compatible Address Recovery Logic
- User-Programmable I/O Decodes

PERIPHERAL SUPPORT

- Integrated Analog Data Separator and a NS 16550-compatible serial port

System Logic CS8238 CHIPSet

The CS8238 System Logic CHIPSet consists of the 82C321 CPU and Micro Channel Controller, the 82C322 Page/Interleave and EMS Memory Controller, the 82C223 DMA Controller, the 82C325 Data/Buffer Controller and the 82C226 System Peripherals Controller. The 82C321 is available in a 100 pin PFP, the 82C322 and the 82C225 are available in a 144 pin PFP, and the 82C223 and 82C226 are available in both a 84-pin PLCC and 100-pin PFP packages.

The 82C321 CPU and Micro Channel Controller manages the system timing for the asynchronous 80386 CPU, DMA and Micro

Channel cycles. It supports CPU clock speeds of 20, 25 and 33 MHz. It supports all Micro Channel cycles, along with Matched Memory and Fast VGA cycles at 16,20,25 and 33 MHz. It includes state machines for command and control logic signal generation, DMA and refresh logic control.

The 82C322 Page/Interleave and EMS Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 4 memory banks, with memory configurations from 1MB to 16MB. While operating under DOS, memory above 1MB can be treated as EMS memory, improving significantly the value of the large memory organizations of the OS/2 era. The on-chip EMS logic provides 4 mapping registers, however, with external EMS mappers, the full LIM EMS 4.0 specification with 8 sets of 64 mapping registers can be implemented. It supports static column DRAMS and shadow RAM BIOS. It contains on-board I/O decode logic and IBM PS/2 Model 80-compatible Address Recovery Logic.

The 82C223 DMA Controller provides 8 DMA channels for slave devices and the Central Arbitration Control Point (CACP) for the entire system. Each DMA Channel has 24-bit address capability and can perform 8-bit or 16-bit transfers. It also supports Virtual DMA so that DMA Channels 0 and 4 can be used to service multiple DMA slaves by multiplexing the DMA Channels between the arbitration levels assigned to those slaves. It supports Multiple Bus Masters via the CACP arbitrator and control signals which enable Bus Masters to monitor the readiness and data size of other adapters and system board components. The Bus Arbitration logic includes protection mechanisms against error conditions, like burst-mode devices not relinquishing the bus within the specified time.

The 82C325 Data Buffer/Controller provides high speed bus sizing and conversion to enable the use of low speed DRAMs at high clock speeds. It contains system POS registers, and NMI as well as DRAM parity generation and detection logic. User-programmable I/O ports, 82C607 Decode Sig-

nals, and 82C451 VGA Setup and Enable Signals are also contained in the 82C325.

The 82C226 System Peripherals Controller integrates PS/2-compatible peripherals in one compact package, with an optimized bus interface to the Peripheral Bus. It includes two 8259-compatible interrupt controllers, one 8254-compatible timer, one 146818-compatible real-time clock, 114 bytes of CMOS battery back-up SRAM and one PS/2-compatible Bi-directional Parallel Port.

Graphics

The 82C452 Gate Level-compatible VGA provides 100% VGA-compatible graphics with backwards compatibility to EGA, CGA, MDA and Hercules. In VGA Graphics modes, it provides resolutions from 320 x 200 with 256 colors to 640 x 480 with 16 colors. In VGA text mode, it supports fonts up to 9x 32. It supports all standard monitors — IBM PS/2 analog, Multi-frequency, EGA, CGA and Monochrome. The 82C452 boosts graphics performance with a tightly-coupled high performance interface to the CPU and a 16-bit memory interface. The 82C452 is packaged in a 144-pin PFP package.

Peripheral Support

The 82C607 Multi-Function Controller integrates additional PS/2-compatible peripherals in one compact package. It includes one NS16550 Compatible UART, an Analog Data Separator, POS registers and Glue Logic for a NEC® 765A Floppy Disk Controller. The 82C607 is available in a 68-pin PLCC package.

Additional components that complement CHIPS/280 are the MicroCHIPS for Micro Channel Adapters and EMS Mapper Chips. The 82C610 and 82C611 MicroCHIPS can be used for I/O intensive Micro Channel Adapters, while the 82C612 is applicable to Adapters that require Slave DMA support.

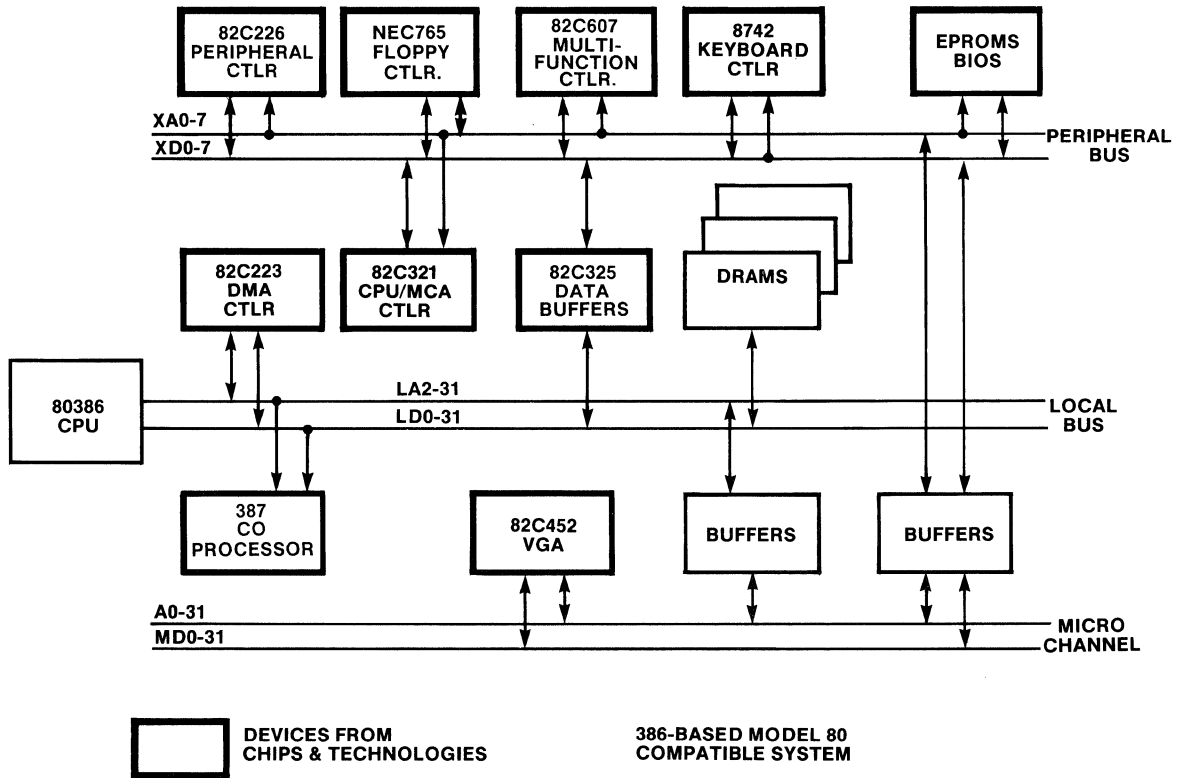


Figure 1. CHIPS/280 Block Diagram

**82C100
SUPER XT COMPATIBLE CONTROLLER**

- 100% PC/XT compatible
- Build IBM PS/2 Model 30 with XT software compatibility
- Bus Interface compatible with 8086, 80C86, V30, 8088, 80C88, V20
- Includes all PC/XT functional units compatible with:
 - 8284, 8288, 8237, 8259, 8254, 8255, DRAM control, SRAM control, Keyboard control, Parity Generation and Configuration registers
- Key superset features: EMS control, dual clock, and power management
- Complete system requires 12 ICs plus memory
- 10 MHz Zero wait state operation
- Applicable for high performance Desktop PCs, Laptop PCs and CMOS Industrial Control Applications
- Single chip implementation available in 100-pin flat pack

The 82C100 is a single chip implementation of most of the system logic necessary to implement a super XT compatible system with PS/2 Model 30 functionality using either an 8086 or 8088 microprocessor. The 82C100 can be used with either 8 or 16-bit microprocessors. The 82C100 includes features which will enable the PC manufacturer to design a super PS/2 Model 30/XT compatible system with the *highest performance* at 10 MHz zero wait state system with an 8086, the *highest functionality* with dual clock and 2.5 MB

DRAM (with integrated Extended Memory System control logic), the *lowest power* implementation by utilizing the on-chip power management features and the *highest integration* with the lowest component count SMT design.

The 82C100 can be combined with CHIPS' 82C601 Multifunction Controller and 82C451 VGA Graphics Controller to provide a high performance, high integration PS/2 Model 30 type system.

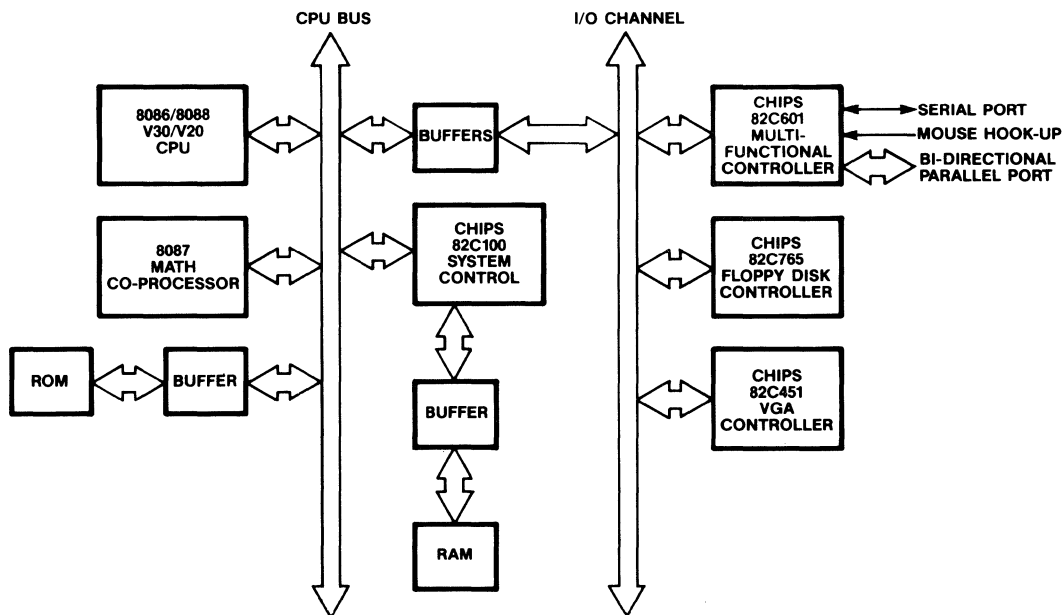


Figure 1. 82C100 Super XT Model 30 Compatible Block Diagram

The 82C100 supports most of the peripheral functions on the PS/2 Model 30 planar board: 8284 compatible clock generator with the option of 2 independent oscillators, 8288 compatible bus controller, 8237 compatible DMA controller, 8259 compatible interrupt controller, 8254 compatible timer/counter, 8255 compatible peripheral I/O port, XT Keyboard interface, Parity Generation and Checking for DRAM memory and memory controller for DRAM and SRAM memory sub-systems.

The 82C100 enables the user to add PS/2 Model 30 superset functionality on the planar board: dual clock with synchronized switching between the two clocks, built-in Lotus-Intel-Microsoft (LIM) EMS support for up to 2.5 Megabytes of DRAM and power management features for SLEEP mode, as well as SUSPEND/RESUME operations. The SLEEP and SUSPEND/RESUME features help in

preserving the battery life in laptop portable applications.

The 82C100 supports a very flexible memory architecture. For systems with DRAMs, the DRAM controller supports 64K, 256K and 1M DRAMs. These DRAMs can be organized in four banks of up to a maximum of 2.5 MB on the planar board. The 2.5 MB memory can be implemented with 2 banks of 1M × 1 DRAMs, partitioned locally as 640KB of real memory and 1.875MB of EMS memory. For systems which require low operating power and minimum standby power dissipation, the chips provide the decode logic which in conjunction with external decoders allows selection of up to 640KB of static RAM. This option is useful in laptop portable applications.

The 82C100 is packaged in a 100-pin plastic flatpack.

82C206 INTEGRATED PERIPHERAL CONTROLLER

- **100% Compatible to IBM PC/AT**
- **Fully compatible to Intel's 8237 DMA controller, 8259 Interrupt controller, 8254 Timer/Counter, and Motorola™'s 146818 Real Time Clock**
- **Offers 7 DMA channels, 13 Interrupt request channels, 2 Timer/Counter channels, and a Real Time Clock**
- **Reduced recovery time (120 ns) between control**
- **114 bytes of CMOS RAM memory**
- **8 MHz DMA clock with programmable internal divider for 4 MHz operation**
- **Programmable wait states for the DMA cycle**
- **16 Mbytes DMA address space**
- **Single chip 84-pin CMOS implementation**

The 82C206 Integrated Peripheral Controller incorporates two 8237 DMA controllers, two 8259 Interrupt controllers, one 8254 Timer/Counter, one MC146818 Real Time Clock, 74LS612 memory mapper, in addition to several other TTL/SSI interface logic chips to offer a single chip integration of all the peripherals attached to the peripheral bus (X-Bus) in the IBM PC/AT. While offering a complete compatibility to the IBM PC/AT architecture, the chip offers enhanced features and improved speed performance. These include an additional 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 8259 and 8254.

Variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip. The chip also provides an option to select 8 or 4 MHz system clock.

The 82C206, along with the CS8220 PC/AT Compatible CHIPSet, provides a highly integrated high performance solution for a PC/AT compatible implementation.

The 82C206 is implemented using advanced CMOS technology and is packaged in an 84-pin PLCC.

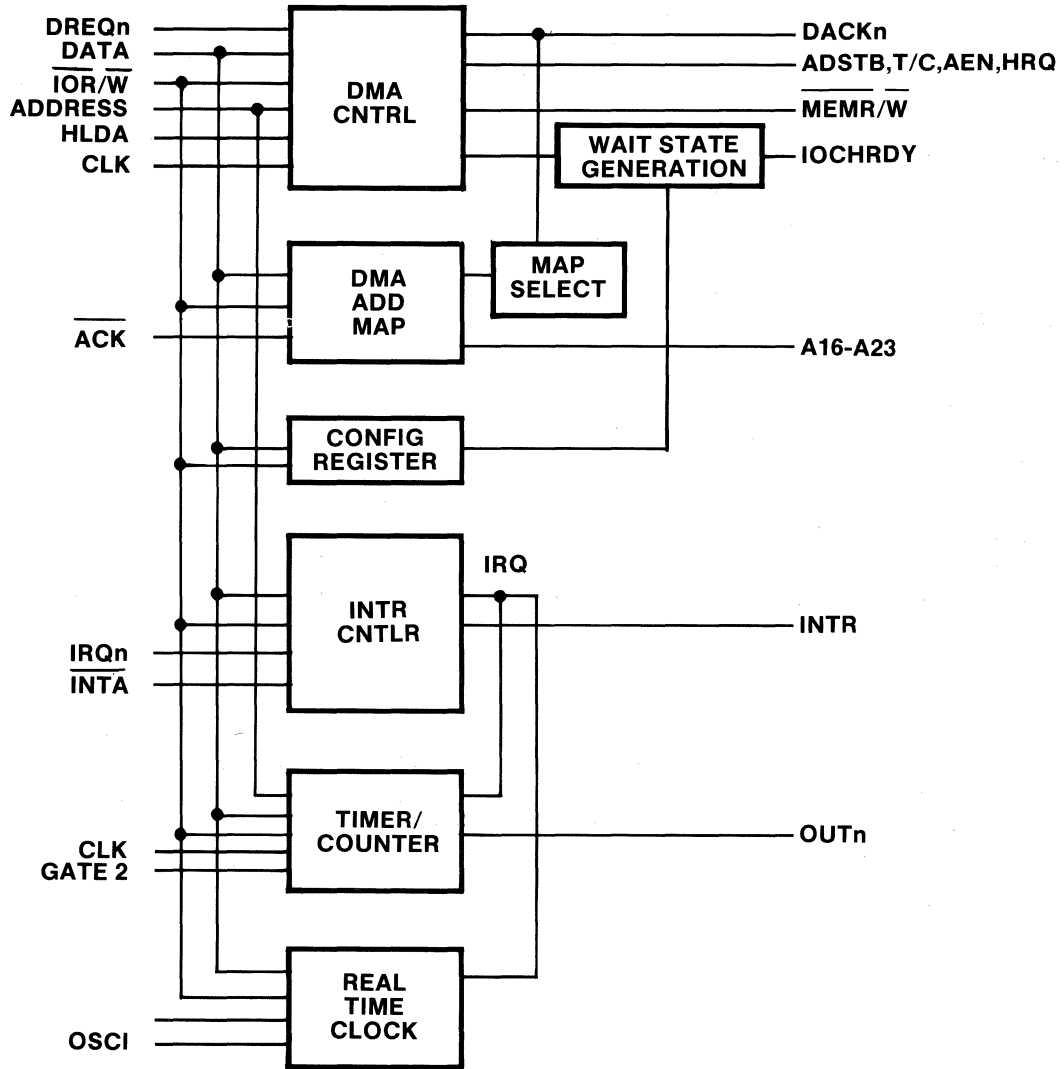


Figure 1. 82C206 Integrated Peripheral Controller Block Diagram

**82C230
HIGH PERFORMANCE IBM PS/2
MODEL 30 COMPATIBLE CHIPSet**

- 100% IBM Model 30 (8086) Compatible, but uses the 80286 CPU for increased performance
- Single chip includes:
 - CPU Support Logic
 - Memory Controller w/ EMS
 - Keyboard and Mouse Ports
 - Bus Interface/Conversion Logic
 - 8237, 8254, 8255, 8259 Equivalents
 - Numeric Processor Interface
 - Peripheral Chip Selects
- Supports up to 8 Megabytes of Memory with EMS and Shadow RAM capabilities.
- Supports CPU speeds of 8, 10, 12.5, 16 and 20 MHz
- Supports 8 or 16 bit 82C451 VGA interfaces
- Supports 82C601 Multi-Function Peripheral Chip
- Has flexible bus timing to solve adapter compatibility problems
- Supports either 8 or 16 bit ROMs for space and cost savings
- High level of integration allows a Model 30 footprint without the need to surface mount all components
- Single chip implementation in 144 Pin Flat Pack

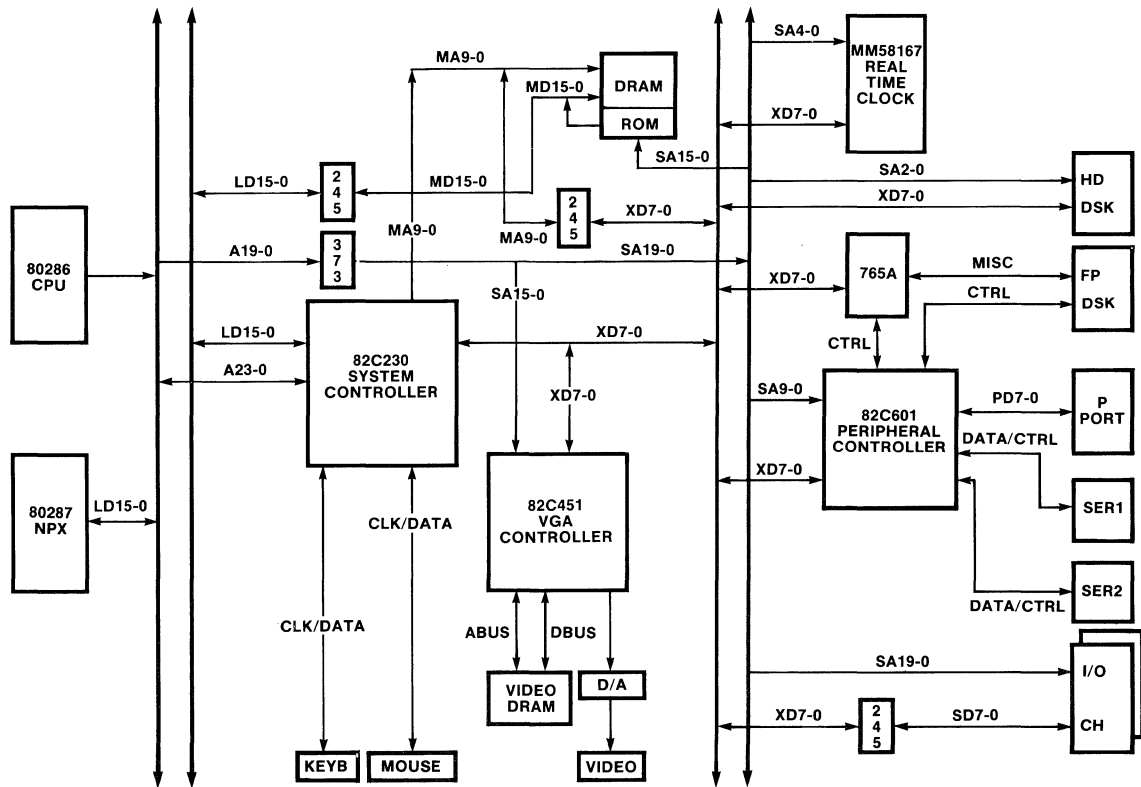


Figure 1. 82C230 Model 30 Compatible Block Diagram

The 82C230 is a single chip that contains most of the core logic required to support the system logic functions required to build a 100% IBM Model 30 (8086) Compatible computer, but based on the higher performance 80286 processor. This allows the OEM to offer a compatible solution for the low end of the marketplace that out-performs the offerings from IBM or compatibles based on the 8086 CPU.

The 82C230 contains CPU control logic including clocks, a DRAM controller that supports up to 8 megabytes of memory with EMS and Shadow RAM capabilities, 8259, 8237, 8254 and 8255 equivalents, refresh controller, expansion bus interface, keyboard and mouse interfaces, numeric processor interface, and peripheral chip selects for floppy and hard disks, real-time-clock, video, serial and parallel ports.

The 82C230 can be combined with the 82C601 multi-function peripheral chip and the 82C451 VGA chip to build a complete Model 30 compatible motherboard that offers superior performance with much higher integration. The

82C230 can support the 82C451 on the 8 bit system bus, or on the 16 bit local bus for higher performance.

The 82C230 DRAM controller can support zero wait state designs at CPU speeds of 12.5 MHz using 80 ns DRAM, or 16 MHz with 60 ns DRAM. Wait states can be inserted so that lower speed DRAMs may be used with high speed processors.

The 82C230 memory controller supports up to 8 megabytes of DRAM. The CPU can access this memory directly or through an EMS 4.0 compatible register set. BIOS ROM support is provided for both 8 and 16 bit wide data paths. Since Shadow RAM is also supported, an OEM can choose to save board space and costs by using a single 8 bit ROM and copying it to shadow RAM for fast execution.

For today's low-end machines, which must have performance levels greater than yesterday's high-end machines, the 82C230 is the clear choice.

**82C235 SINGLE CHIP AT (SCAT)
SYSTEM CONTROLLER**

- 80286 control logic and clocks which support CPU speeds of up to 12.5 MHz with 0 or 1 wait states
- 32 EMS Page Registers (supporting LIM EMS 4.0)
- Two 8237 compatible DMA controllers
- Two 8259 compatible interrupt controllers
- An 8254 compatible programmable interval timer
- An 8255 compatible peripheral interface
- An 82284 compatible clock generation and READY interface
- An 82288 compatible bus controller
- A DRAM controller which supports up to 16MB of DRAM
- A memory controller which provides shadow RAM and support for either 8-bit or 16-bit BIOS ROM configurations
- A 146818 compatible real time clock with 114 bytes of CMOS RAM
- A DRAM refresh controller
- Interface logic for 80287 numeric coprocessor
- Interface logic for 8042 keyboard controller
- Fast Gate A20 and Fast CPU Reset logic
- Power management features
- Packaged in a single 160-pin plastic flat pack

82C235—SCAT

The 82C235 is a VLSI device that incorporates most of the motherboard logic required to build a low-cost, highly-integrated IBM PC/AT compatible computer. It is designed to be used in conjunction with other Chips and Technologies controllers such as the 82C451 VGA Controller, the 82C601 Periph-

eral Controller, and the 82C765 Floppy Disk Controller. When used with these devices, the 82C235 serves as the heart of a highly-integrated system, significantly reducing the system's motherboard size and component count, and the need for many I/O Channel (AT Bus) slots.

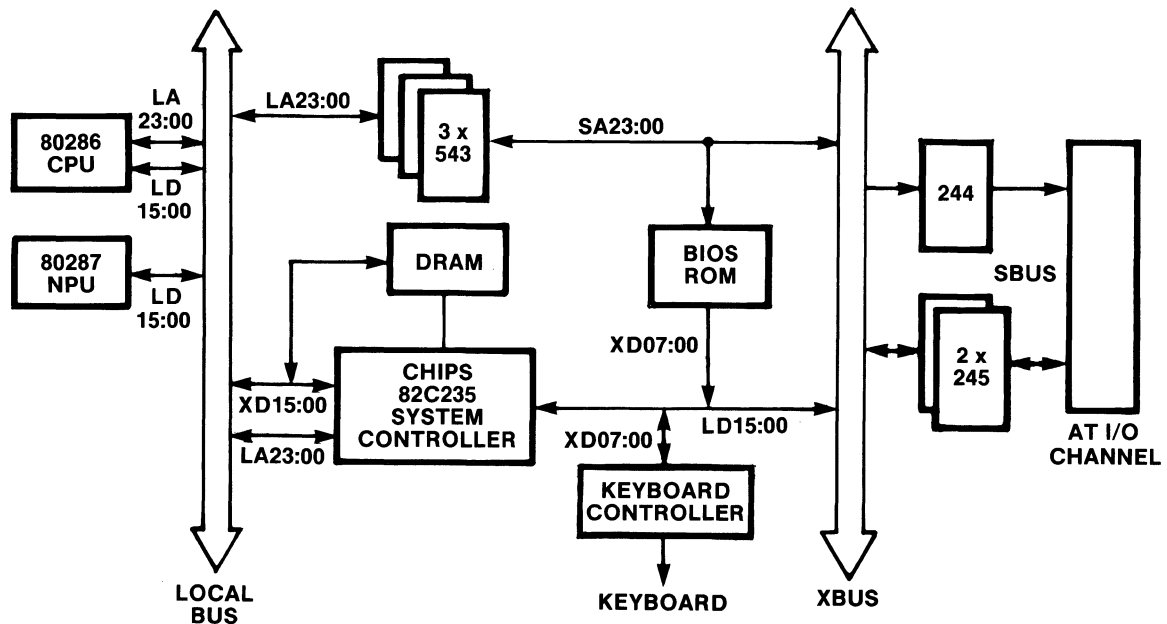


Figure 1. 82C235 Single Chip AT Block Diagram

**82C611, 82C612
MicroCHIPS: MICRO CHANNEL INTERFACE**

- Implements 100% IBM PS/2 Compatible Micro Channel Adapters
- 82C611 Supports Multi-function, I/O and Memory Adapters
- 82C612 Supports Controller-type Adapters, including all DMA Slave Arbitration Functions
- Programmable Option Select (POS) Support including:
 - Adapter ID Support
 - Flexible I/O and Memory Relocation Support
 - POS Port Decode Logic and Handshaking
- Full Micro Channel Interface including:
 - Command and Status Decoding
 - Response Signal Generation
 - Full DMA Slave Arbitration and Handshake (82C612 only)
- Meets all IBM specified Timing and Drive Specifications
- Simplifies migration of XT/AT adapter designs to the Micro Channel
- Available as 68-pin PLCC or 80-pin PFP components

Description

The MicroCHIPS (Micro Channel Interface Parts) family of components integrates most of the interface logic required on an adapter card for the Micro Channel—IBM's new high speed bus for its latest generation of PCs. MicroCHIPS provide many benefits to de-

signers of add-in adapters for the Micro Channel: space savings because of the single-chip VLSI approach; cost savings because of the integration of many components into one; and time savings because of the ease of design.

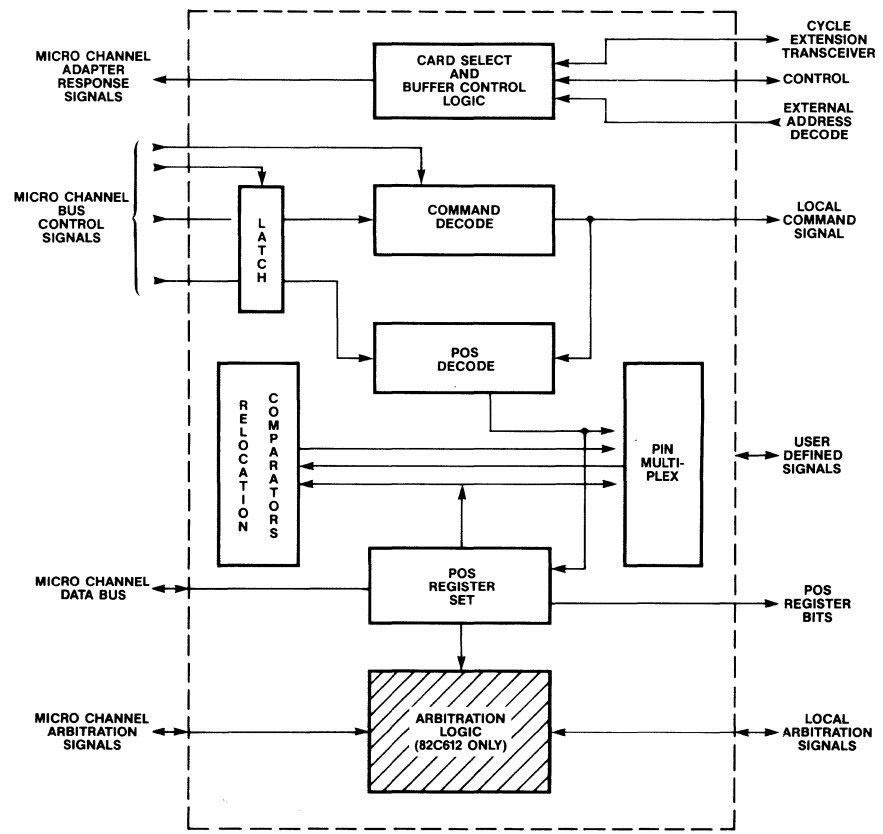


Figure 1. 82C611/612 Simplified System Block Diagram

There are currently two members of the MicroCHIPS family: The 82C611 is optimized for memory and I/O interfaces such as those on multi-function cards. It does not support the DMA arbitration and handshaking signals. The 82C612 adds full support for DMA arbitration and handshaking including single cycle and burst modes. It also supports both "preempt" and "fairness" modes as defined by IBM. Both chips are available in either a 68-pin PLCC (plastic leadless chip carrier) or 80-pin PFP (plastic flat pack) packages.

In addition to the standard functions supplied by the 82C611 and 82C612, CHIPS has the capability to customize these standard devices for dedicated high-volume applications. The macrocells for these parts can be integrated into custom controller designs.

Note: IBM uses a leading minus sign (-) to indicate an active low signal. The convention used in this data sheet is the overbar. Therefore a signal such as $\overline{\text{ADL}}$ in the IBM documentation would be represented as ADL herein.

82C614 MicroCHIP BUS MASTER

- Single Chip Bus Master Interface for the Micro Channel
- Transfer Rates up to 20 Megabytes per Second
- High Speed, Cost Effective Alternative to DMA Slaves
- Contains 4 DMA Channels with Integral FIFO Buffer
- Complete Micro Channel Interface Requires just 1 Component
- Adapter Side has AT-like Structure for Ease of Interfacing
- 32 bit Address and 16 bit Data Support
- Compatible with Subsystem Control Block Architecture
- Supports New Micro Channel Features including:
 - Streaming Data Transfers
 - Data Parity Checking and Generation
 - Extended POS
 - Synchronous CHCK
- Four Programmable Decode Outputs Provided
- Eight Multi-Function Pins Provide Maximum Flexibility
- Jointly Developed by Chips and Technologies and IBM
- Applications include SCSI Host Adapters, Hard Disk Controllers, LAN Adapters, High Speed Communication Adapters, Modem/FAX Adapters and many more
- 144 Pin Plastic Flat Pack

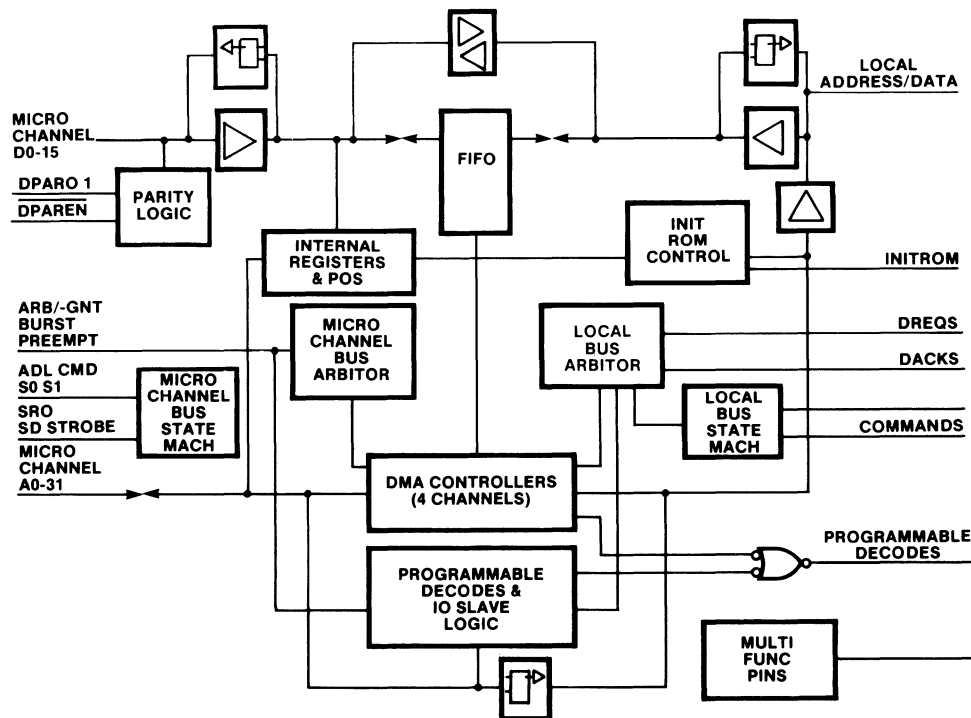


Figure 1. 82C614 Block Diagram

The 82C614 Bus Master MicroCHIP (**Micro Channel Interface Part**) is a single chip that contains all of the logic required on an adapter card to implement a Bus Master interface to the Micro Channel. It is intended to give bus mastering capabilities to adapter cards that would normally use the system DMA controller. The advantages of bus mastering vs. standard DMA include faster transfer rates (up to 4 times) and the ability to easily implement "full duplex" DMA. One of the goals of the 82C614 is to allow adapter card designers to take advantage of the performance improvements offered by bus mastering while remaining cost competitive with standard DMA slave designs.

The 82C614 has four complete DMA Channels. Each channel has DREQ and DACK signals on the local or adapter side to interface to standard peripherals. The local side also supports a full 16 bit data bus and up to 24 address lines. An integral 80 byte FIFO Buffer is provided to "speed match" peripherals to the Micro Channel and allow simultaneous transfers to occur on the Micro Channel and local sides for increased throughput. The DMA Channels are compatible with the newly defined Subsystem Control Block Architecture, including linked list chaining ability.

The 82C614 requires just one external '245 type transceiver to form the complete interface to the Micro Channel. It supports a full 32 bit address path and a 16 bit data path with parity generation and checking. It supports the new Streaming Data Procedure to achieve transfer rates up to 20 megabytes per second, which is four times the bandwidth available using the DMA controllers in existing systems.

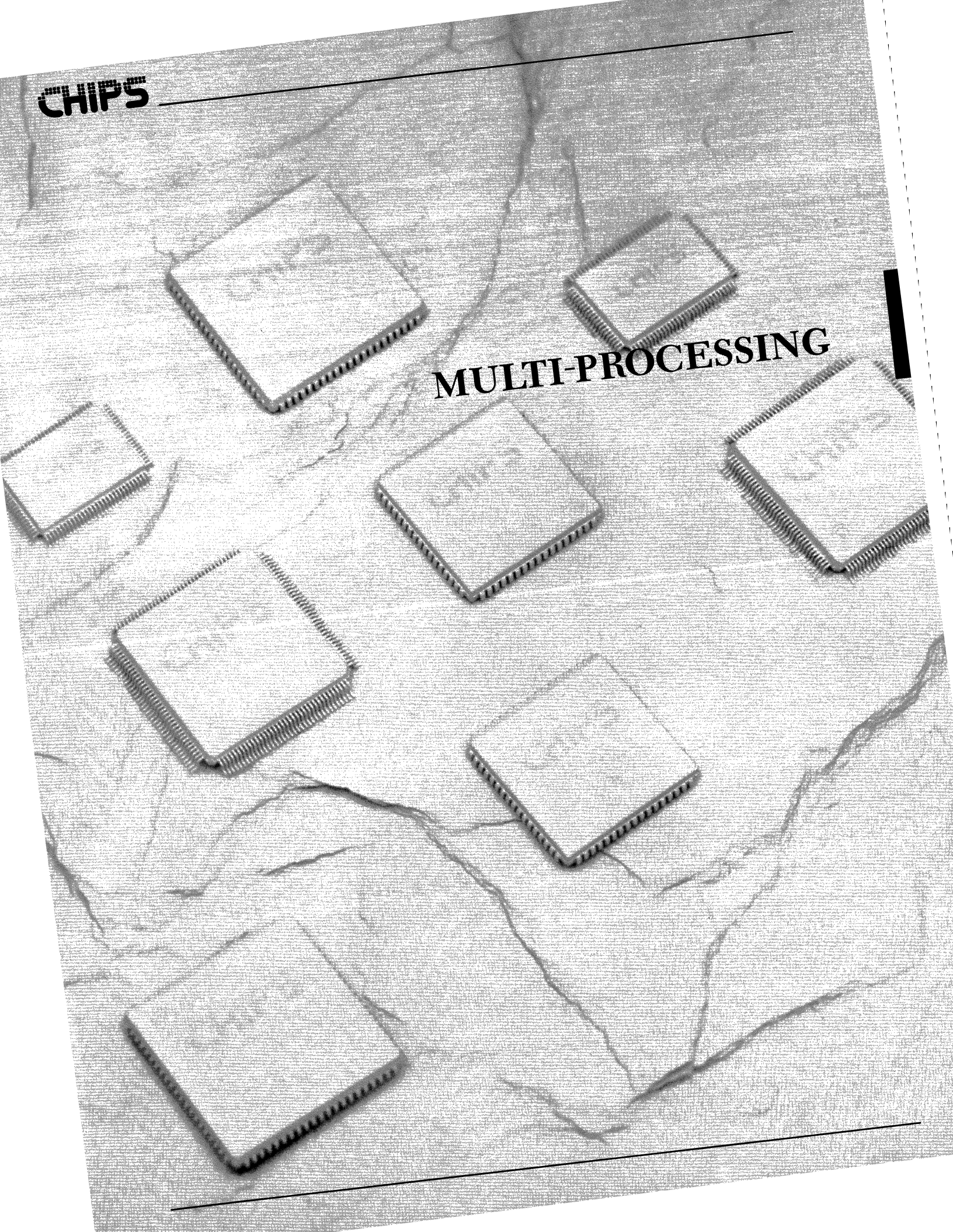
The local side features an AT-like set of signals that ease in the interfacing of standard peripheral components, as well as providing a familiar environment for the designer to work with. Eight Multi-Function Pins are provided which may be programmed to provide a variety of useful functions. This allows the adapter side interface to be optimized for individual applications while eliminating external components.

The 82C614 provides four Programmable Decode outputs that allow an adapter card to also function as a slave. One of these outputs is optimized for large memory spaces, one for BIOS ROMs and the remaining two for I/O spaces. In addition, five more decode outputs are available on the multi-function pins.

In summary, the 82C614 Bus Master MicroCHIP is intended to make it easy for the designer to implement a high speed peripheral adapter using bus mastering instead of standard DMA, with no cost penalties. Because of the high level of integration provided by the 82C614, the design may require no external components to interface to standard peripheral chips, and only one component for the Micro Channel side. It supports the new features of the Micro Channel so that new designs will be in step with both today's and tomorrow's systems. New designs may never be DMA slaves again.

CHIPS

MULTI-PROCESSING





CS9239 M/PAX MULTI-PROCESSOR PLATFORM

- **Supports 486™ Processors:**
 - Clock rates of 25-33 MHz with 40-50 MHz in the future
 - Second level (L2) cache, 64K-1MB
 - Zero wait-state hits, read and write 16B line sizes
 - Direct-mapped allows use of a single bank of SRAM
 - Copy-back (store-in) write policy reduces bandwidth requirements in an MP configuration
 - Castout performed from external cache
 - Invalidate performed on internal and external caches
 - Processors can run asynchronous to Multi-Processor Interface clock
- **High Bandwidth message-based Multi-Processor Interface (MPI):**
 - Distributed arbitration, central control
 - 32 bit address bus
 - 128 bit data bus
 - 16 to 25 MHz bus clock rate
- **High Bandwidth main memory system:**
 - 51 MB per second sustained (3 cycle access, 2 cycles recovery) @ 16 MHz
 - Lower MPI clock frequency reduces noise generation due to bus switching
 - 128 bit wide memory data array
 - Large memory configurations — 4 MB, 16 MB or 64 MB increments using 256K, 1 MB or 4 MB devices, respectively
 - 16B data move-in/out in one memory access
 - ECC (single bit correction, double bit detection)
- **Central Data Coherency Unit handles:**
 - Cache invalidation
 - Castouts
- **High resolution timing facilities**
- **High throughput DMA byte-serial I/O channel**
- **PC Compatibility, if required, can be achieved by connection to existing PC CHIPSets**

The M/PAX (Multi-Processor Architecture Extension) architecture provides a platform for symmetrical multi-processing. The CS9239 CHIPSet is a specific implementation of the M/PAX architecture that supports up to six 80486 or other CISC or RISC processors connected to memory and I/O resources via a wide, non-multiplexed, multi-master Multi-Processor Interface (MPI) bus.

OBJECTIVES:

- Provide high-performance CHIPSet for tightly-coupled multi-processor systems composed of multiple *processor modules* and shared system functions such as memory and I/O.
- Implement copy-back caches to reduce memory/bus bandwidth requirements
- Ensure data coherency among caches
- Provide high memory bandwidth to support the instruction/data bandwidth of multiple processors

An implementation of a Modular System Architecture that allows:

- Symmetrical attachment of other RISC and CISC processors
- Easier interface to different Compatible I/O PC busses such as ISA, EISA, MCA, NuBus or industrial busses such as Multibus, VME
- Orderly upgrade strategy to support more and faster processors, higher bandwidth memory and I/O

Enhance I/O capability provides inexpensive connection for on-board block-mode byte-serial devices such as

- SCSI host adapters
- Network controllers
- Laser Printer, Scanner, video capture display interfaces

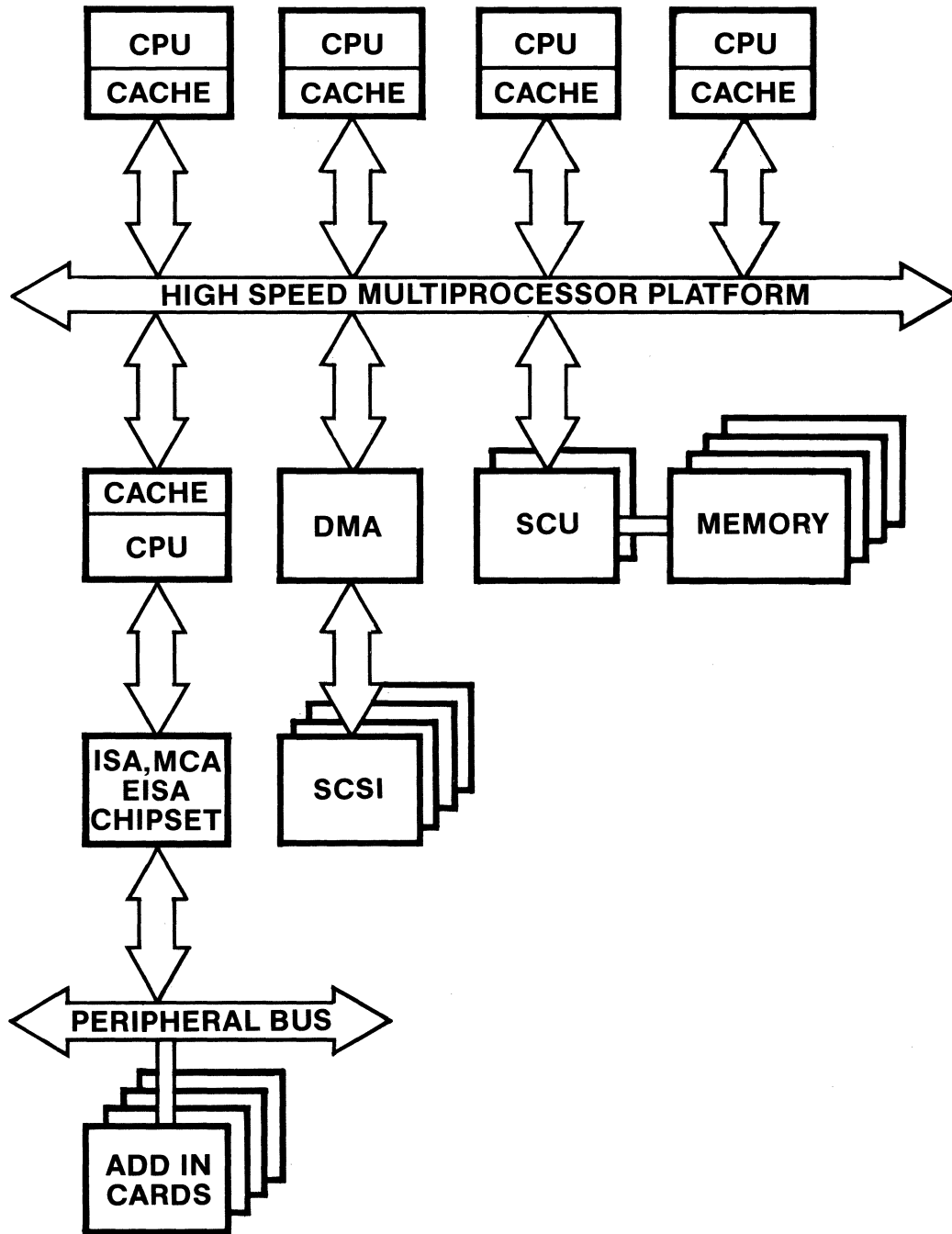
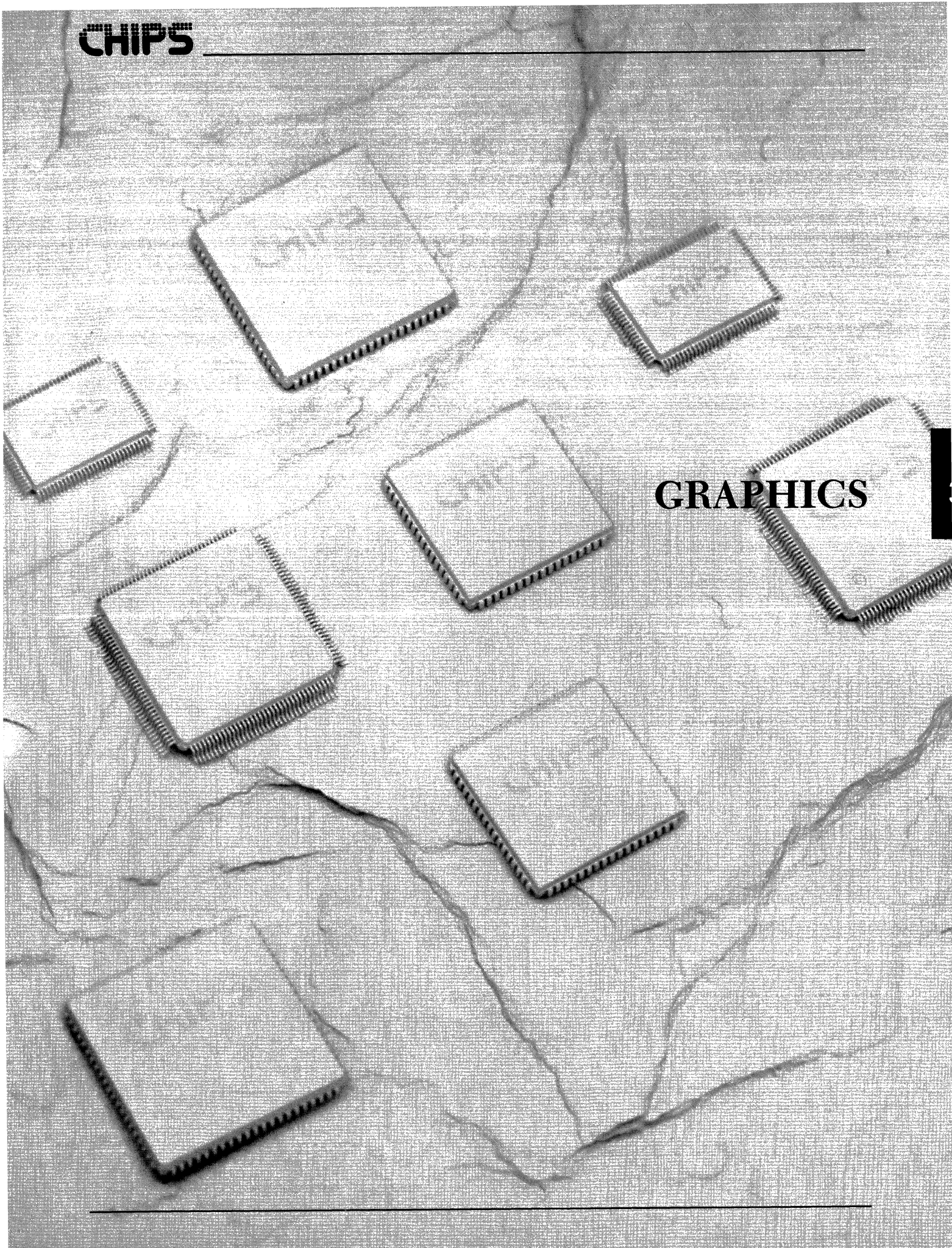


Figure 1. CS9239 M/PAX Platform

CHIPS

GRAPHICS





**CS8245 VGA CHIPSet
82C441 VGA CONTROLLER, 82A442 BUS INTERFACE**

- **Compatible to:**
 - IBM PS/2 Video Graphics Array (VGA)
 - IBM Enhanced Graphics Adapter™
 - IBM Color Graphics™ Adapter
 - IBM Monochrome™ Adapter
 - Hercules™ Adapters
- **Supports the following monitors:**
 - IBM PS/2 Analog displays
 - IBM EGA, CGA and Monochrome monitors
 - Multifrequency Monitors (NEC Multi-sync™, Sony Multiscan™ and compatibles)
- **VGA solution for PC add-in cards can be implemented using 14 standard components, including 256 Kbytes of display memory and Color Palette/DACs**
- **Hardware support for context switching in windowing and multi-tasking environments**
- **Smart Auto-Emulation™ adjusts automatically to display mode required by application software**

The 82C441 Graphics Controller and 82A442 Bus Interface offer a complete, highly integrated solution for implementing an IBM Video Graphics Array compatible controller, with backward compatibility to EGA, CGA, IBM Monochrome, and Hercules modes. A complete VGA, with backward compatibility can be implemented using a total of 14 off-the-shelf components, including 256K bytes of display memory and color palette and D/A converters for analog displays.

82C441 Graphics Controller

The 82C441 is a single-chip graphics controller which supports all the display modes of the IBM's VGA. The 82C441 includes support logic and registers for supporting the IBM's new VGA modes.

The 82C441 is packaged in an 84-pin PLCC or optional 100-pin PFP.

82A442 Bus Interface

The 82A442 Bus Interface provides bus interface, memory select and I/O select logic functions. This includes all the logic to interface to the Inmos G171 (and compatible palette) color palette/DAC. The 82A442 is a bipolar device and is packaged in a 68 pin PLCC.

Backward Compatibility/Smart Auto-Emulation

The 82C441 supports backward compatibility on-chip to EGA, CGA, IBM Monochrome and Hercules modes. It also supports Smart Auto-Emulation which automatically adjusts to the graphics mode required by the application software. The 82C441 provides enhanced performance to CGA modes by allowing CGA text to be displayed in EGA/VGA resolution.

Hardware Support for Context Switching

For support of multitasking and windowing environments, the entire state of the 82C441/82A442 (registers and latches in the 82C441/82A442) is readable and writable. This feature is compatible to IBM's VGA.

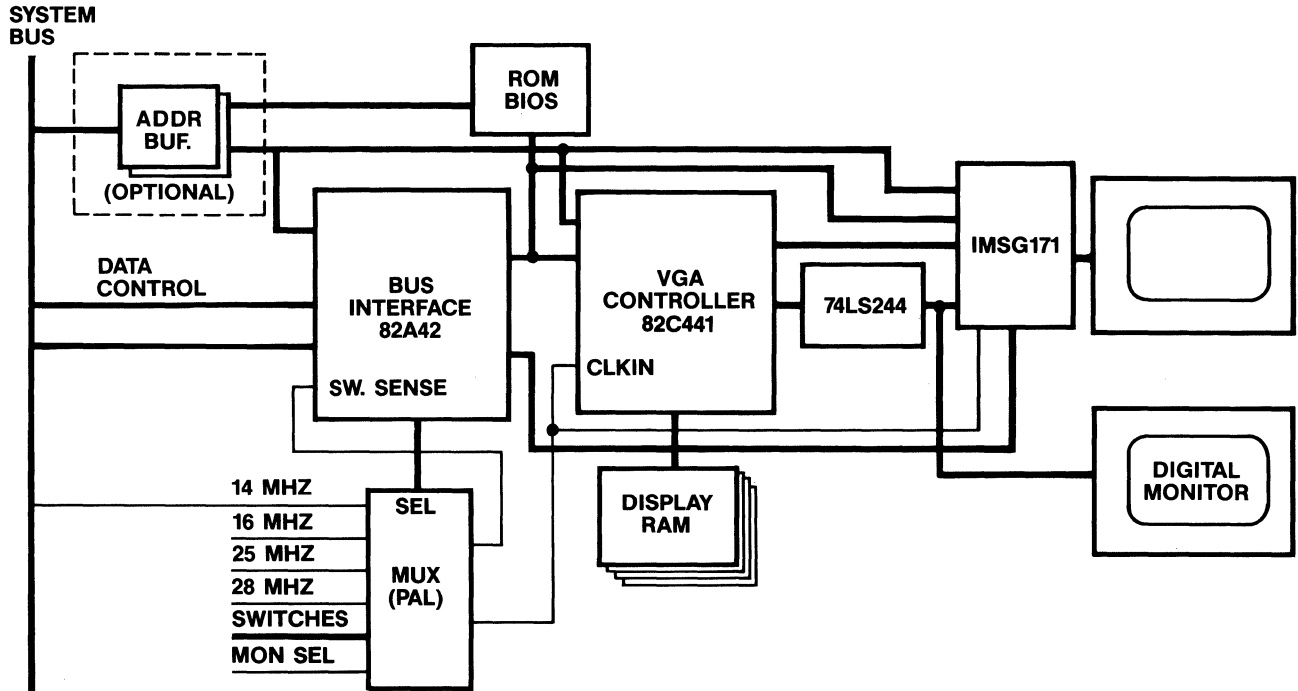


Figure 1. 82C441/82A442 VGA Implementation Block Diagram

82C425 LCD/CRT CONTROLLER

- Single chip 100% IBM CGA-compatible LCD/CRT controller
- Very-low power 100-pin CMOS device
- Supports all CGA modes
- Supports up to eight gray scales
- Intelligent memory arbitration
- Support for two fonts
- Built-in CPU interface
- Interfaces directly to SRAMs used for display and font memory
- Ideal for laptop computers

The 82C425 is a display controller for Liquid Crystal Displays (LCDs) and CRTs. It is ideal for portable and "laptop" IBM-compatible computers. The device is designed to drive a single-panel, single-drive LCD with 4 bits of parallel data. LCDs having 200 dot vertical resolution and panel duty cycles of 1/200 are supported. The 82C425 also supports CGA-compatible CRTs and is fully compatible with applications designed for the IBM Color Graphics Adapter.

CPU/82C425 INTERFACE

The 82C425 interfaces directly to the PC I/O bus with no "glue" logic, using separate data and address buses. Two external clock inputs are supported; either can be selected under software control. Direct connection to display and font SRAMs is supported; a buffer is used for driving each display. Figure 1 depicts a graphics subsystem using the 82C425.

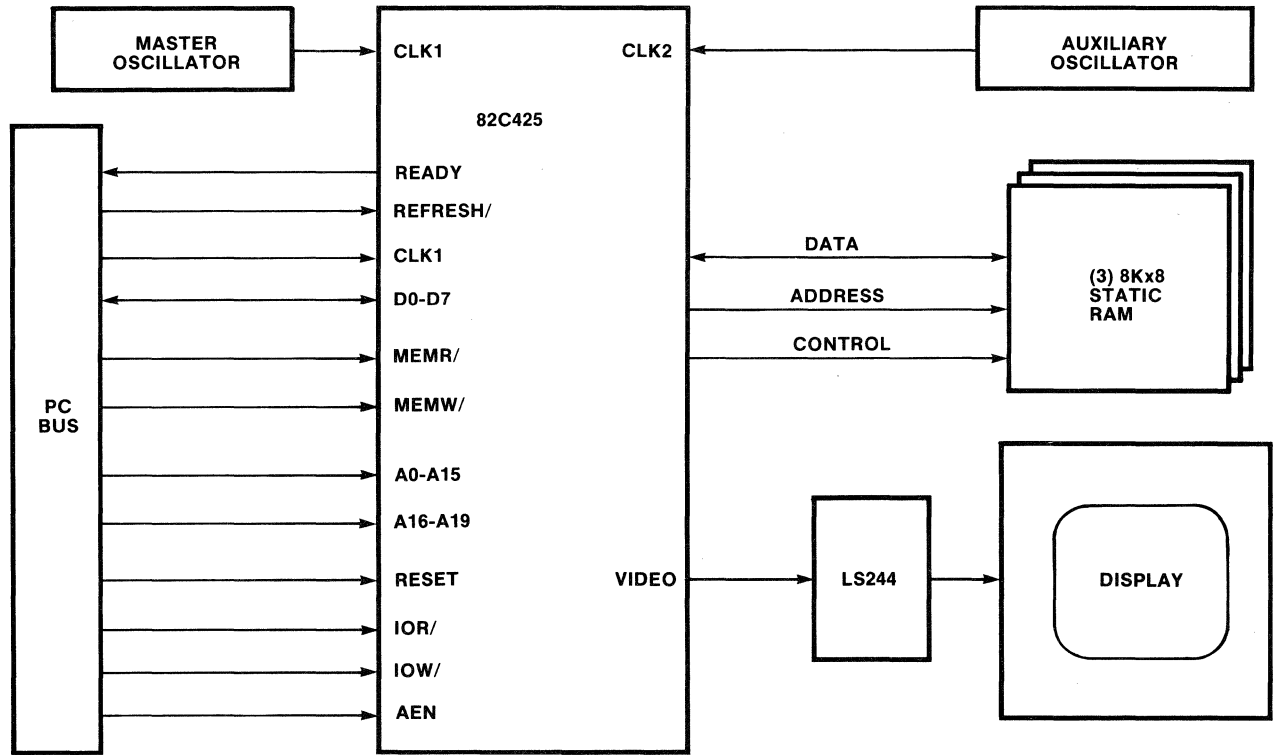


Figure 1. 82C425 LCD/CRT Controller Block Diagram

82C435 ENHANCED GRAPHICS CONTROLLER 82A436 BUS INTERFACE

- **100% hardware and software compatible to IBM Enhanced Graphics Adapter card**
- **Backward compatible to IBM Color Graphics, IBM Monochrome and Hercules adapters**
- **Reduces the chip-count for an EGA implementation to 13 standard components, including 256 Kbytes of display memory**
- **Hardware support for context switching in windowing and multi-tasking environments**
- **Smart Auto-Emulation adjusts automatically to display mode required by application software**
- **Improved CPU access to display memory, allowing up to two times faster performance over IBM EGA without software changes**
- **Supports 640 × 480 resolution**
- **38 MHz option supports 800 × 600 resolution**
- **BIOS and software drivers for 640 × 480 resolution and 800 × 600 resolution available**

The 82C435 Graphics Controller and 82A436 Bus Interface offer a complete, highly integrated solution for implementing an IBM Enhanced Graphics Adapter compatible controller, with backward compatibility to CGA, IBM Monochrome, and Hercules modes. A complete EGA, with backward compatibility can be implemented using a total of 13 off-the-shelf components, including 256K bytes of display memory.

82C435 Graphics Controller

The 82C435 single-chip graphics controller integrates the functions of the four-chip CS8240 CHIPSet (82C431 Graphics Controller, 82C432A Sequencer, 82C433 Attributes Controller, and 82C434A CRT Controller) with additional support logic and registers for backward compatibility to CGA, Hercules and IBM Monochrome modes.

The 82C435 is packaged in an 84-pin PLCC.

82A436 Bus Interface

The 82A436 Bus Interface provides bus interface, memory select and I/O select logic functions. The 82A436 is a bipolar device and is packaged in a 68 pin PLCC.

Backward Compatibility/Smart Auto-Emulation

The 82C435 supports backward compatibility on-chip to CGA, IBM Monochrome and Hercules modes. It also supports Smart Auto-Emulation which automatically adjusts to the graphics mode required by the application software. The 82C435 provides enhanced performance to CGA modes by displaying CGA text in EGA resolution.

Hardware Support for Context Switching

For support of multitasking and windowing environments, the entire state of the 82C435/82A436 (most registers and latches in the 82C435/82A436) is readable and writable.

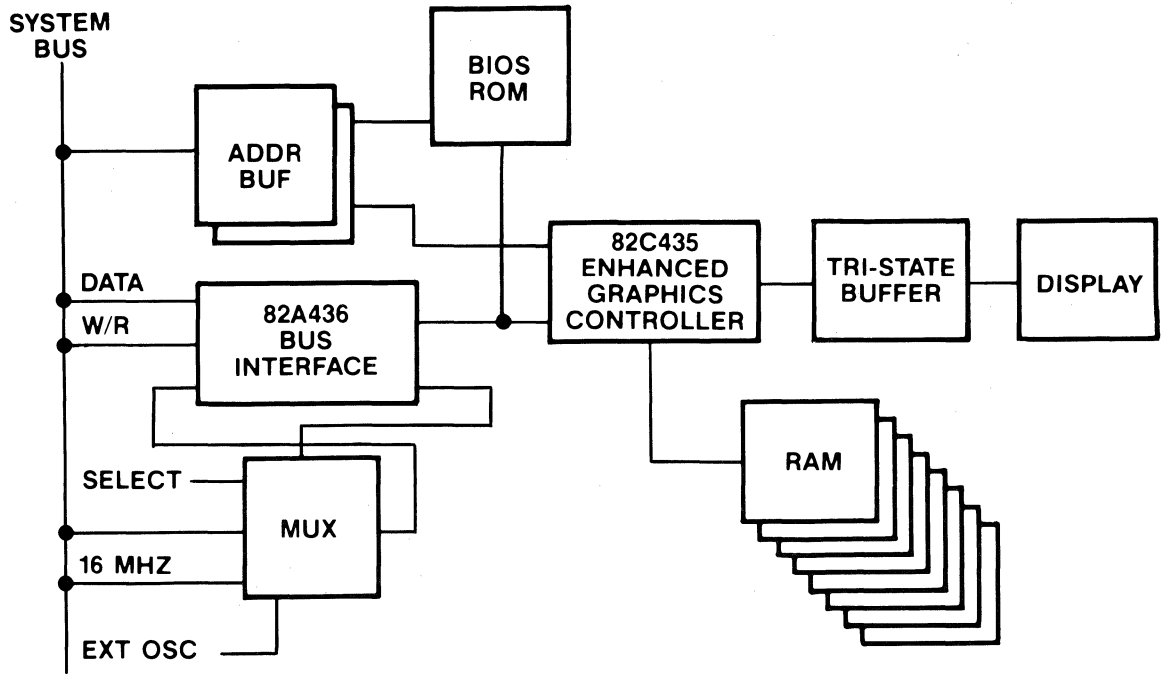


Figure 1. 82C435/82A436 EGA Block Diagram

82C451 INTEGRATED VGA CONTROLLER

- Fully IBM VGA Compatible at hardware, register and BIOS level
- Dual Bus Architecture
- Integrated interface to PC-Bus and Micro Channel (CHIPS/250 and CHIPS/280)
- Single Chip Solution
- Proprietary High Speed Interface to CHIPS/250 and CHIPS/280 Systems
- Supports 8 and 16 bit CPU interface for memory and I/O cycles
- Supports external palette DAC of up to 16 million colors
- Resolutions up to 640 x 480 in 16 colors, 960 x 720 in 4 colors and 1280 x 960 monochrome
- Enhanced backward compatibility with EGA,CGA,Hercules, MDA without using NMI
- Processor Latches and Attribute Flip Flop are readable
- Pinout Compatible with 82C452
- Same board design can use both parts

CPU Interface

82C451 has a strap option to select a PC-Bus Interface or a Micro Channel Interface. All control signals for both the interfaces are integrated into the single chip.

82C451 supports both a 8 bit and 16 bit CPU interface. The 16 bit interface can be independently enabled/disabled for memory and I/O cycles. On reset, the chip is configured for 8 bit accesses for memory and I/O cycles. 16 bit interface for I/O cycles is restricted to index/data pair of registers. This includes the Sequencer (3C4h), Graphics Controller (3CEh), CRT Controller (3B4h/3D4h) and the Attribute Controller (3C0h). All other I/O addresses (color palette, Misc Output and Status) are always treated as 8 bit ports.

If the 16 bit interface is chosen, then depending on the state of A0 and BHE, either a 8 bit or 16 bit cycle will actually be executed. This ensures compatibility with old software.

All I/O cycles are completed without wait states. For memory cycles, the cycles are extended with wait states.

BIOS ROM Interface

In the PC-BUS Interface, the 82C451 supports an external BIOS ROM. The ROM address is decoded and the ROMCS pin is asserted to enable ROM data on the CPU bus. In the Microchannel Interface, the system BIOS includes the video BIOS.

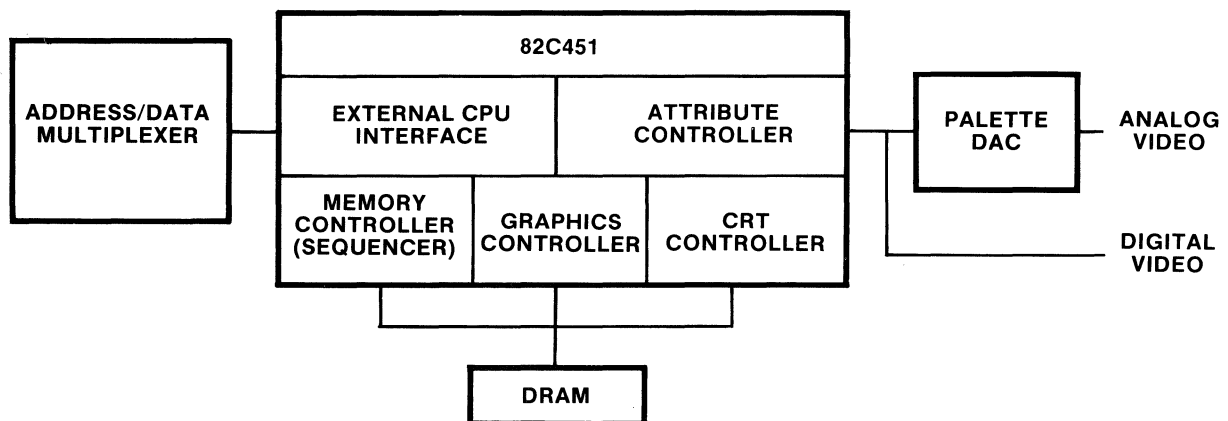


Figure 1. 82C451 Integrated VGA Controller Block Diagram

Display Modes and Resolution

82C451 supports a superset of all VGA display modes. It supports resolutions upto 640 x 480 in 16 colors, 960 x 720 in 4 colors and 1280 x 960 in monochrome.

Memory Interface

The entire display memory (256 Kbytes) is always available to the CPU in regular 4 plane mode, chained 2 plane mode and in super chained 1 plane mode.

The display memory control signals are derived from the dot clock. The MCLK is used for internal sequencing of 16 bit memory cycles. MCLK should be 25-40 MHz.

Extended Registers

All functionality of the extended registers in 82C451 are disabled on reset. Before the extended registers can be written into, they must be enabled by two sets of control bits (disabled on reset). The Processor Latches in

the Graphics Controller and the Attribute Flipflop are readable in the extended register space. **No new bits are defined or any of the unused bits used in the regular VGA registers.**

External Palette Interface

82C451 supports programming of an external palette DAC by decoding the CPU addresses and generating the \overline{RD} and \overline{WR} signals to the external palette. 82C451 decodes I/O addresses 3C6-3C9h as valid external palette addresses.

High Speed CPU Interface

82C451 supports a high speed interface to CHIPS/250 and CHIPS/280 systems. There are special interface pins on the CHIPS/250, CHIPS/280 and 82C451. Using these special interface pins, CPU accesses to the 82C451 can be executed faster than CPU accesses to other peripheral devices.

The 82C451 is packaged in a 144 pin plastic flat pack (PFP).

82C452 SUPER VGA CONTROLLER

- Fully IBM VGA Compatible at hardware, register and BIOS level
- Dual Bus Architecture
- Integrated interface to PC-Bus and Micro Channel (CHIPS/250 and CHIPS/280)
- Single Chip Solution
- Proprietary High Speed Interface to CHIPS/250 and CHIPS/280 Systems
- Supports 8 and 16 bit CPU interface
- Graphics Cursor with transparency
- Resolutions up to 640 x 480 in 256 colors, 960 x 720 in 16 colors and 1280 x 960 in 4 colors
- Enhanced backward compatibility with EGA,CGA,Hercules, MDA without using NMI
- Intelligent memory cycle arbitration to maximize CPU bandwidth
- Pinout compatible with 82C451
- Same board design can use both parts
- New Patented Write Mode to speed up graphics text

CPU Interface

82C452 has a strap option to select the PC-Bus Interface or the Micro Channel Interface. All control signals for both of the interfaces are integrated on the single chip.

82C452 supports both 8 and 16 bit CPU interface. The 16 bit interface can be independently enabled/disabled for memory and I/O cycles. On reset, the chip is configured for 8 bit cycles. The 16 bit interface for I/O cycles is restricted to the index/data pair of registers. This includes the Sequencer, Graphics Controller, CRT Controller and the Attribute Controller. All other registers are always treated as 8 bit ports.

If the 16 bit interface is selected, then software can still execute 8 bit cycles. This ensures compatibility with old software.

All I/O cycles are completed without wait states. Memory cycles are arbitrated using an intelligent algorithm and is completed in the fastest possible time.

BIOS ROM Interface

In the PC-BUS Interface, the 82C452 supports an external BIOS ROM. The ROM address is decoded and the $\overline{\text{ROMCS}}$ pin is asserted to enable ROM data to the CPU.

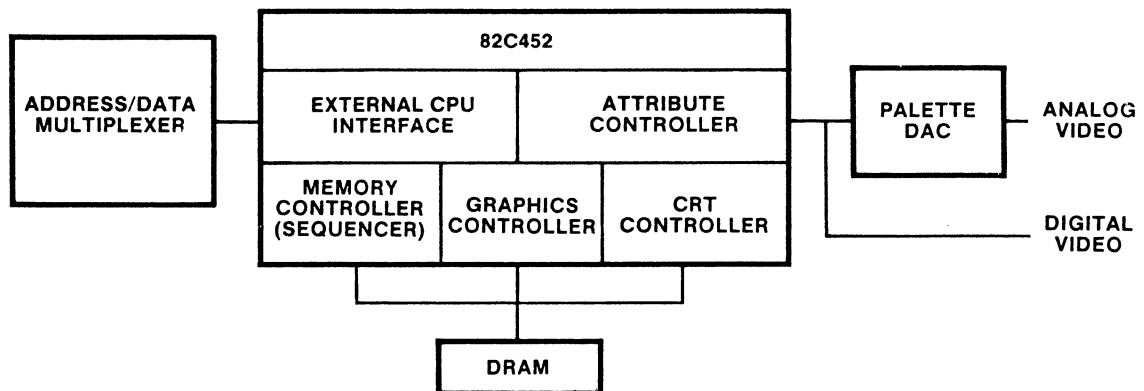


Figure 1. 82C452 Super VGA Controller Block Diagram

Display Memory Interface

The 82C452 supports a high speed page mode DRAM interface. This along with the 16 bit data path and intelligent CPU arbitration, can improve CPU performance by upto 8 times.

The 82C452 supports 256 KB, 512 KB and 1 MB of display memory as follows:

8 devices 64k x 4	256KB
16 devices 64k x 4	512KB
8 devices 256k x 4	1MB

The entire display memory (256 Kbytes, 512 Kbytes or 1 Mbyte) is always available to the CPU in regular 4 plane mode, chained 2 plane mode and in super chained 1 plane mode.

The display memory control signals are derived from an independent clock (MCLK). For 120ns DRAMs, the MCLK frequency should be in the range of 30-33 MHz. This can support a 50 MHz (4 bits/pixel) video data stream. With 100ns DRAMs, the MCLK frequency can be up to 35-36 MHz. At this frequency, the average number of wait states for the CPU is reduced resulting in higher performance.

Display Modes and Resolution

82C452 supports a superset of all VGA display modes. The maximum display bandwidth is 200 Mbits/s — 25 MHz at 8 bit/pixel or 50 MHz at 4 bit/pixel. This translates to resolutions up to 640 x 480 in 256 colors (packed pixel mode), up to 960 x 720 in 16 colors (both planar and packed pixel mode) and up to 1280 x 960 in 4

colors (both planar and packed pixel mode).

Extended Registers

All functionality of the extended registers in 82C452 are disabled on reset. Before the extended registers can be written into, they must be enabled by two sets of control bits (disabled on reset). The Processor Latches in the Graphics Controller and the Attribute Flipflop are readable in the extended register space. **No new bits are defined or any of the unused bits in the regular VGA registers are used.**

Graphics Cursor

82C452 supports a 32 pixel wide and 512 pixel high hardware graphics cursor. The graphics cursor supports transparency and can be any arbitrary shape within the outline box. The hardware cursor is based on the definition of the graphics pointer in Microsoft Windows™. Use of the hardware cursor frees the CPU of the responsibility of managing the pointer in any graphics environment like Windows or Presentation Manager,™ leading to improved performance of the application programs.

External Palette Interface

The 82C452 supports programming an external palette DAC by decoding the CPU addresses and generating the READ and WRITE signals for the external palette.

The 82C452 is packaged in a 144 pin plastic flat pack (PFP).

82C455 VGA FLAT PANEL CONTROLLER

- **VGA Compatible flat panel controller optimized for laptop computer applications**
 - **Supports CRT, LCD, Plasma and Electro-Luminescent displays of varying resolutions.**
 - **Single chip implementation tightly couples to the CHIPS/250 and CHIPS/280 and interfaces with 8 and 16 bit PC bus and MCA (an interface compatible with the Micro Channel™)**
- **Up to 40 MHz dot clock speed for graphics and text modes**
 - **Can utilize an external palette DAC with up to 16 million colors**
 - **Provides intelligent backward compatibility to the EGA, CGA, Hercules, and MDA on Flat Panel displays**

The 82C455 Graphics Controller provides a complete solution for implementing a Video Graphics Array compatible controller. The 82C455 is supplied in a 144-pin PFP package. It can be used in 8 and 16-bit PC bus and in 16-bit MCA bus environments.

Display Types Supported

CGA, EGA, MDA, Multifrequency, IBM PS/2 and other monitors can be used. The choice of flat panel displays includes EL, plasma, as well as single panel/single drive, dual panel/single drive and dual panel/double drive LCDs. Both gray scale and monochrome panels are supported; a proprietary frame rate control algorithm provides gray scale capability on monochrome panels.

Chips/250 and Chips 280 Interface

The 82C455 interfaces directly to the CHIPS/250 and CHIPS/280, providing a simple, cost-effective

solution for PS/2 compatible systems. When used with one of these CHIPSets, the 82C455 can execute FAST memory cycles at a speed greater than that normally available on the MCA bus.

Backward Compatibility

The 82C455 is compatible with IBM's EGA, CGA and MDA, in addition to offering a Hercules monochrome-graphics compatible mode. On-chip compensation registers permit software designed for low resolution displays to utilize the entire screen area on a flat panel with higher resolution.

Hardware Support for Context Switching

Multitasking and windowing environments can be implemented easily since all internal registers of the 82C455 can be read and written.

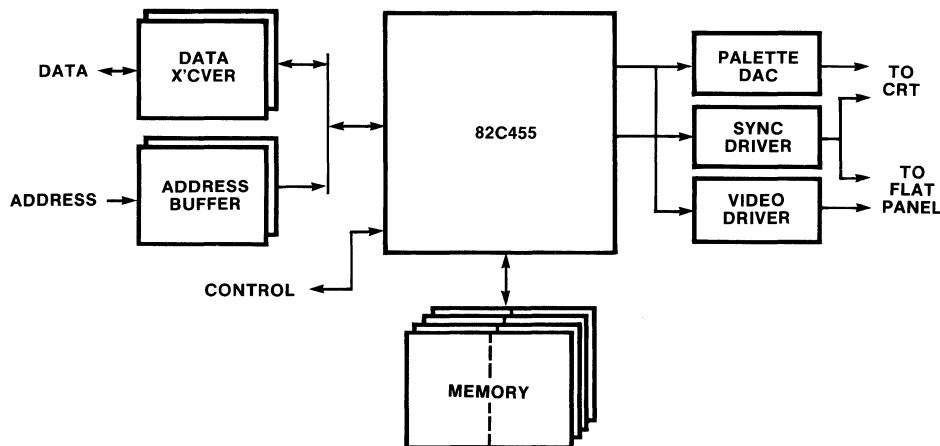


Figure 1. 82C455 VGA Flat Panel Controller Block Diagram

82C455 Functional Description

The 82C455 offers a complete solution for implementing a VGA/MCGA/EGA/CGA/MDA/Hercules compatible display system. By integrating all necessary logic the device ensures that total chip count for a VGA compatible solution can be as low as 14 chips (includes 82C455, display memory, buffers and drivers).

Any one of a variety of CRT monitors or flat panel displays can be driven. Internal compensation registers ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software. The 256 Kbytes of display memory size is comprised of 8 64k x 4 DRAMs. Display memory refresh is controlled by the 82C455; it is transparent to the CPU.

For support of multitasking environments and context switching, the entire state of the 82C455 (internal registers and latches) is readable and writeable. This feature is 100% compatible to IBM's VGA.

The 82C455 directly interfaces to 8-bit PC and PC/XT, 16-bit PC/AT and 8 or 16-bit MCA buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations and generation of the necessary control signals.

The 82C455 contains 16 color palette registers. It also interfaces directly to an external Inmos G171 (or compatible) color palette and D/A converter. Like the VGA, it is capable of display resolutions of 640 x 480 with 16 on-screen colors (internal palette) and 320 x 200 with 256 on-screen colors from an external palette of 256 thousand (or 16 million) colors. The 82C455 can also be programmed for higher resolutions up to 800 x 600 in 16 colors.

The 82C455 integrates four different modules as follows:

Graphics Controller

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies to the Attribute Controller display memory data for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and an attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Sequencer

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access and contains mask registers which can prevent writes of individual display memory planes.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and graphic modes the 4-bit pixel data acts as an index into a set of internal palette registers which generate a 6-bit stream. Two additional bits of color data are added if 256-color mode is enabled. Text blink, underline and cursor are also the responsibility of the Attribute Controller.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

82C456/460 ENHANCED VGA FLAT PANEL CONTROLLER

- **100% IBM VGA Compatible (Register, Gate & BIOS levels)**
- **Up to 64 gray scales**
- **Drives color panels**
- **IBM VGA monochrome CRT compatibility on monochrome panels**
- **SMARTMAP™ intelligent color to gray scale conversion**
- **Flexible display formats**
- **Advanced SLEEP modes**
- **Proven DOS & OS/2 Compatible**
- **Full backwards Compatibility with IBM, EGA, CGA, MDA and Hercules standards**
- **Drives 640 x 480 LCD, PLASMA, Electro-luminescent and CRT displays**

The 82C456 is Chips and Technologies' second generation VGA flat panel/CRT controller, optimized for high-end laptops. The 82C456 provides complete Video Graphics Array (VGA) compatibility at the register, gate and BIOS levels. The 82C456 produces up to 64 gray scales or colors for photographic image quality on monochrome panels and enhanced color displays. Additionally, the 82C456 provides IBM VGA Monochrome CRT compatibility on monochrome flat panels. The 82C456 provides proven DOS and OS/2 compatibility across all modes.

The 82C456 drives a variety of monochrome and color flat panel displays, including electro-luminescent (EL), plasma and all configuration of LCD's. Complete CRT support is included for a wide variety of monitors.

The 82C456 provides full backwards compatibility in hardware with EGA, CGA, MDA and Hercules graphics standards to ensure that older software can be run with no modification.

Screen format compensation automatically adjusts the flat panel display area. This feature is required, for example, to allow software written for a 350-line application to fill an entire 480-line display. Compensation is accomplished by line replication (stretching), line insertion, pixel doubling and programmable border and margin sizes to center the display.

Chips' proprietary SMARTMAP™ intelligently maps colors to gray scales. This technique works by first comparing and then suitably adjusting the foreground and background values to produce adequate display contrast on LCD screens.

The 82C456 offers two advanced SLEEP modes to extend battery based operation. In the first mode when the backlight is normally shut off, the display is blanked and the CPU retains complete access to all internal registers and display memory. System operation is suspended in the second mode while the 82C456 continues to refresh the display memory DRAMs at a programmable reduced rate to prevent data loss.

The 82C456 integrates the graphics controller, sequencer, attribute controller and CRT controller on one chip. The 82C456 is packaged in a 144-pin CMOS QFP.

The 82C460 is connected in parallel with the existing CRT color palette DAC. Its inclusion in the normal video path ensures the integrity of all application software RAMDAC data. Thus, switching between the CRT and flat panel is accomplished without compromise in all modes. The 82C460 performs the 256 color to 64 gray scale or color reduction using the following techniques: 1) NTSC color weighting, 2) equal weighting, 3) green data output only, or 4) 64 colors on color panels. The 82C460 is packaged in a 64-pin CMOS QFP.

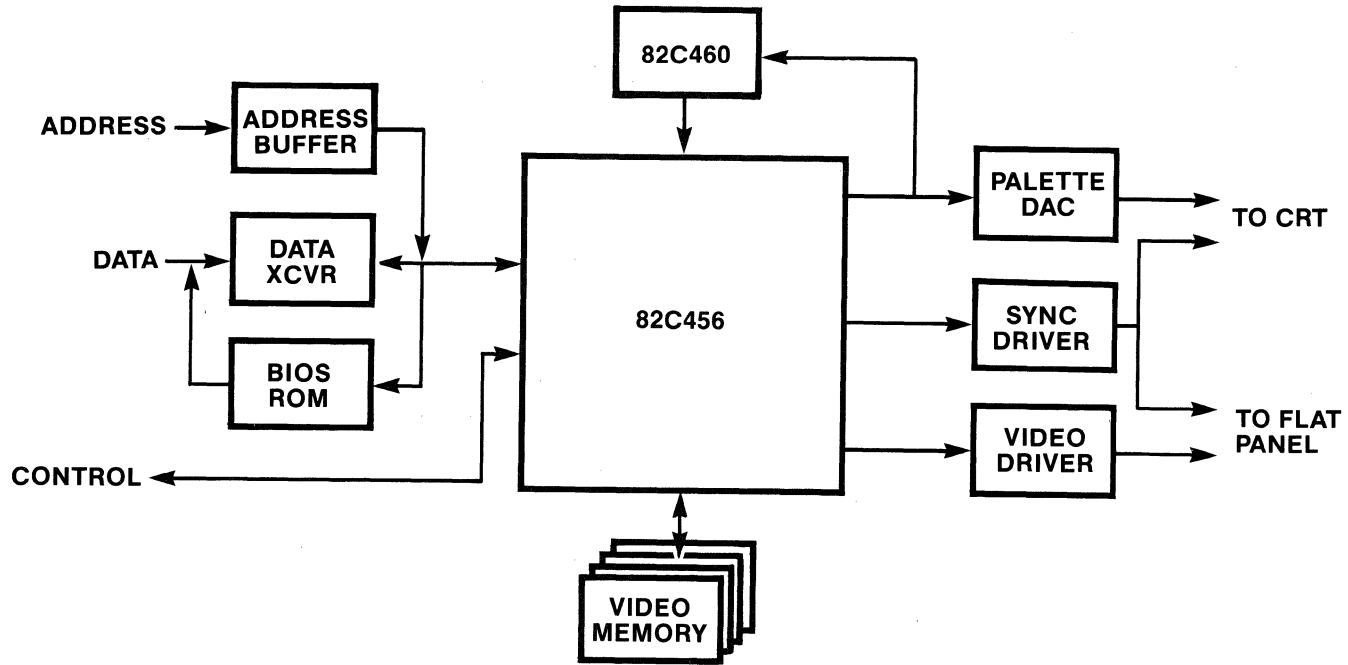


Figure 1. 82C456/460 Enhanced VGA Flat Panel Controller

82C480 8514/A COMPATIBLE GRAPHICS CONTROLLER

- Fully Compatible with IBM 8514/A at both register and software ('Adapter Interface' or AI) level
- Runs Windows and Presentation Manager for the 8514/A without special drivers
- Single Chip Solution: 160-Pin Plastic Flatpack
- Integrated Micro Channel and Industry Standard Architecture (PC Bus) Interfaces
- Autoconfigurable for 8-bit or 16-bit System Interface
- Demultiplexed bus interface resulting in lower chip count. Total of 9 chips required for a complete 8514/A implementation including memory:
 - 1 82C480 Graphics Controller
 - 1 74LS245 Bus Tranceiver
 - 1 RAMDAC
 - 1 LM339 Comparator
 - 4 256Kx4 VRAMs (+4 for 256 colors)
 - 1 82B484 Support Chip
 - +1 EPROM (optional)

- Supports both 256K and 1M VRAMs

	16	32	4	8
	256K	256K	1M	1M
640x480x16-color	x	x	x	x
640x480x256-color	x	x	x	x
1024x768x16-color	x	x	x	x
1024x768x256-color		x		x

- Hardware Graphics Functions:
 - Bit Blt
 - Polygon Fill
 - Line Draw
 - Pattern Fill
 - Color Mixing
 - Scissoring
- External palette DAC support for up to 16 million colors (Autoconfigurable for 6-bit or 8-bit RAMDACs)
- Resolutions supported up to 2540x2048 (either interlaced or non-interlaced)
- Video rates supported up to 300 MHz (with ECL external logic)
- Low-Power CMOS process

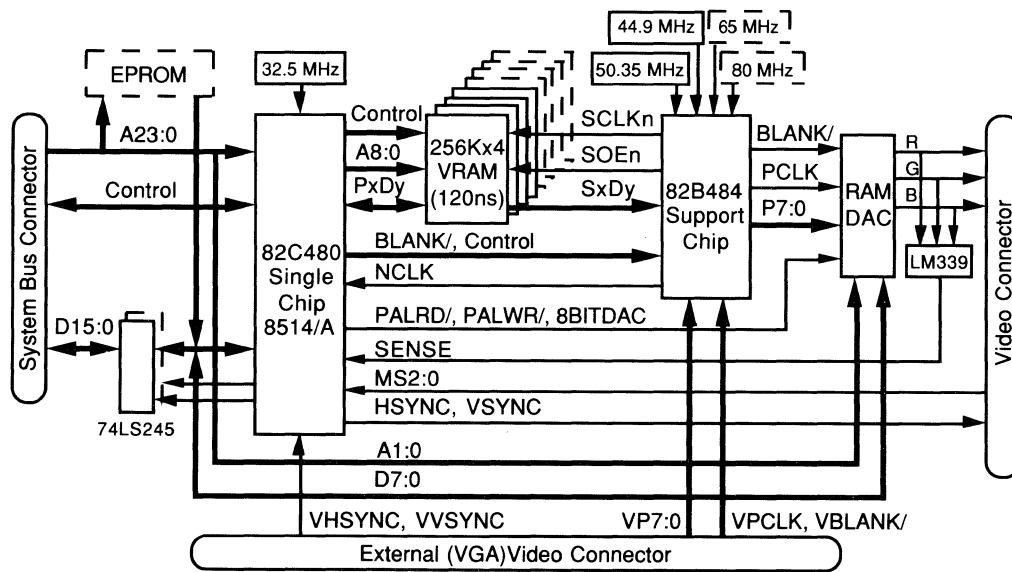


Figure 1. 82C480 Block Diagram

The 82C480 is a 100% register-level IBM 8514/A compatible controller. The 82C480 provides memory interface logic, video control logic, and interface logic to both the ISA (PC/AT) Bus and Micro Channel (MCA).

With 512 KBytes of display memory, the 82C480 supports 16 and 256 displayable colors in 640x480 resolution and 16 with 1024x768 resolution. With 1Mbyte VRAM, it supports 256 displayable colors with 1024x768. An external RAMDAC supports 256K (6-bit DAC) or 16 million (8-bit DAC) total colors.

The 82C480 supports the following modes selectable via software:

- VGA mode (pass through video from VGA subsystem)
- Advanced Function mode (8514/A 1Kx768 or 640x480)

The 82C480 powers up in VGA mode. In the Advanced Function mode, the 82C480 supports 640x480 or 1024x768 resolution as well as providing more complex hardware functions such as BitBit, line drawing, polygon fill, patterns, raster operations, and scissoring (post-clipping).

Software support for the 82C480 is provided via the Chips and Technologies' Adapter Interface (AI), Windows drivers, OS/2 Presentation Manager (PM) drivers, and drivers for other major software applications.

The 82C480 is supplied in a 160-pin PFP package.

CPU Interface

The 82C480 allows selection of either ISA or MCA Bus Interface by detecting a strapping option during reset. All control signals for both interface types are integrated onto the single 8514/A compatible chip.

The 82C480 supports both 8-bit and 16-bit CPU interfaces.

ROM Interface

The 82C480 supports an optional 8-bit ROM for Power-On-Self-Test (POST) code which may be implemented in AT-bus systems using no additional external components except the ROM chip. The ROM address is decoded and the ROMCS/ pin is asserted to enable ROM data onto the data bus. A 16-bit ROM may be implemented with two ROM chips and one additional external PAL.

Video initialization code and support functions may be included in the POST ROM, incorporated into the system BIOS, loaded from disk at system initialization as a TSR, or incorporated directly into drivers.

VRAM Interface

Like the IBM 8514/A, the 82C480 supports 256K (64Kx4) VRAMs. In addition, the 82C480 also supports 1M (256Kx4) VRAMs, allowing a lower cost, lower chip-count 8514/A implementation. The 82C480 provides a faster sequencer and supports a faster memory clock (40 MHz) to maximize use of VRAM bandwidth.

The 82C480 supports five memory cycle types:

1. Read (page mode)
2. Write (page mode)
3. Read-Modify-Write (page mode)
4. RAS-only refresh
5. Data Transfer Cycle

Extensions and Extended Registers

The 82C480 chip provides enhanced modes of operation which are not available on the IBM 8514/A. These extended features are controlled via bits in extension registers.

The 82C480 has extended the 8514/A architecture to make the registers readable to improve the testability of the chip and to allow state save and restore to be accomplished. ***This capability is not implemented in revision 0 silicon.***

82B484 VIDEO SUPPORT CHIP

- Allows an IBM 8514/A compatible display adaptor to be implemented with 9 chips (including memory);
 - 1 82C480 Graphics Controller
 - 1 82B484 Video Support Chip
 - 1 74LS245 Bus Transceiver
 - 1 RAMDAC
 - 1 LM339 Comparator
 - 4 256Kx4 VRAMs (minimum)
 - +1 EPROM (optional)
- 80-pin Plastic Flat Package
- Reduces chip count for 82C480 based 8514/A compatible display adaptors
- Select up to 4 clock sources
- Contains VGA Video pass-through circuitry
- Implements VESA compatible video pass through logic
- Supports video rates to 80 MHz
- High-speed Bi-CMOS process
- Pinouts optimized for PCB layout

Designed to work with the 82C480, the 82B484 Video Support Chip integrates all TTL components required for 8514/A compatible display adaptors. With the 82B484, a minimum system 1024x768 non-interlaced 8514/A compatible display adaptor can be implemented in 9 chips including VRAM

memory. Included in the 82B484 is all clock selection circuitry, video shift registers, and VGA video pass through logic. The 82B484 CMOS circuitry allows 80 MHz clock frequencies supporting non-interlaced monitor resolutions up to 1024x768 and interlaced monitor resolutions up to 1280x1024.

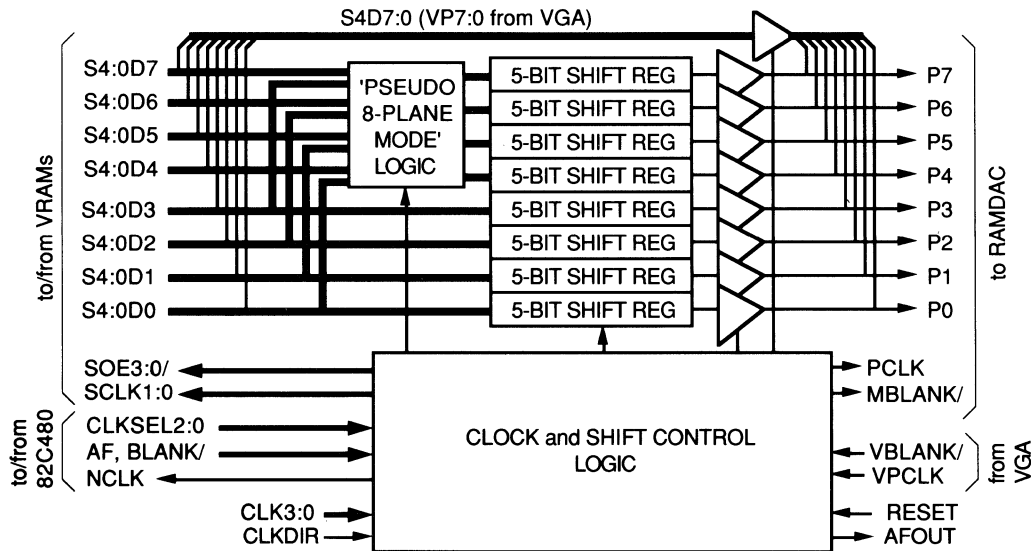


Figure 1. 82B484 Block Diagram

Video Subsystem Total Chip Count

Using the 82C480 and 82B484, a complete 8514/A compatible 8-bit video subsystem can be built with just 9 ICs (10 ICs for a 16-bit system), including display memory, as shown in the table below:

Qty Chip Type

1	82C480 Graphics Controller Chip
1	74LS245 Tranceiver (2 for 16-bit interface)
1	IMSG176-65 or IMSG178-65 RAMDAC
1	LM339 Comparator
4	256Kx4 VRAM (120 ns) (+4 for 8 planes)
1	82B484 Video Support Chip
9	Total
+1	27256 POST ROM (optional)

Additional components required are 44.900, 50.350, and 65.000 MHz oscillators, 15-pin video connector, LM334 Current reference, 1N4148 diode, and various resistors and capacitors. The indicated configuration supports 640x480 non-interlaced 16-color and 256-color modes and 1024x768 interlaced and non-interlaced 16-color mode.

Adding 256-color support for 1024x768 would require four additional 256Kx4 VRAM chips.

Adding support for 1280x1024 interlaced would require an additional oscillator (80 MHz), a '-80' RAMDAC, and a total of 5 VRAMs (16-color) or 10 VRAMs (256-color).

The same video subsystem configured for the MCA bus with a 'Power-On-Self-Test' (POST) ROM would require two additional 8-bit address latches (74LS373 or equivalent).

Package

The 82B484 is available in a 80-pin plastic flat pack (PFP).

CHIPS

COMMUNICATIONS

The background of the page is a high-contrast, black and white image of several square microchips scattered on a piece of crumpled paper. The chips are arranged in a non-uniform pattern, with some showing their pin edges. The overall aesthetic is technical and textured.

**82C570 CHIPSlink
SINGLE CHIP "3270" PROTOCOL CONTROLLER**

- Implements IBM 3270 Communication Protocol
- Provides IBM 3278/79 and IRMA™ emulation adapter cards interface
- Supports both CUT and DFT modes
- Type A coaxial transmitter and receiver
- 8X Digital Phase Locked Loop (DPLL)
- On chip 4.7 MIPS microcontroller
- Dual port RAM control function
- 2.4K bytes internal microcode
- Provisions for external microcode
- Low power CMOS technology
- 18.8696 MHz crystal oscillator
- 84 pins PLCC package

The 82C570 is a highly integrated IBM 3270 coaxial type A protocol controller chip. It serves as an I/O processor to emulate most of the IBM terminals and printers. It works with IBM 3276/3274/3174 control units either locally or remotely attached.

The 82C570 internal microcode supports most display terminals and printers in both CUT and DFT modes except 3279-S3G due to the large memory requirement. The programmed symbol and APA graphics for 3179/G and 3270 PC/G can only be supported in DFT mode. There are provisions for adding an additional 8K × 8 SRAM and using external microcode.

The 82C570 provides both IRMA and IBM emulation adapter compatible interface. All the IRMA and IBM emulation, file transfer and application software can run on the adapter using 82C570.

The 82C570 along with an external 120ns 8K × 8 SRAM , line driver, line receiver and pulse transformer, a complete 3270 protocol emulation adapter can be built easily.

The 82C570 is fabricated using advanced CMOS technology and is packaged in an 84 pin PLCC.

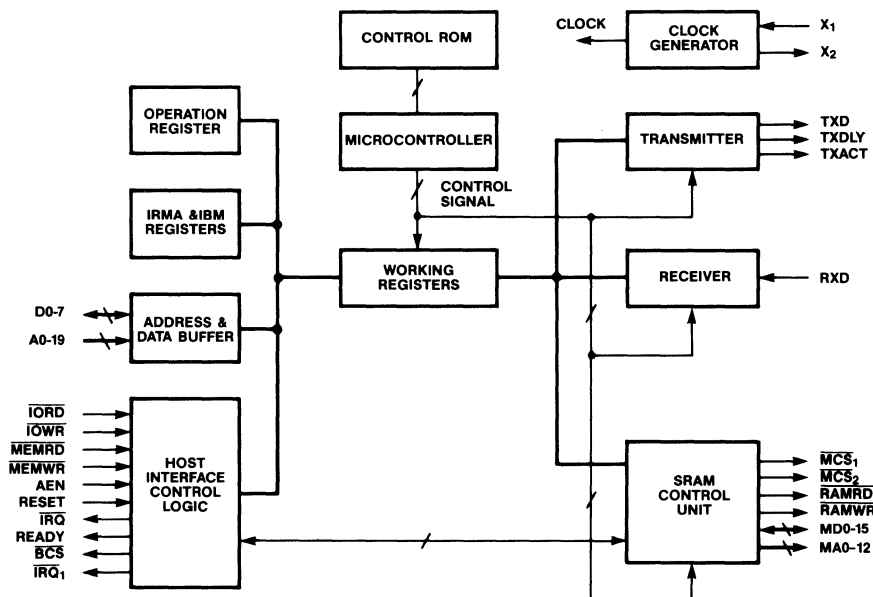


Figure 1. 82C570 Block Diagram

CHIPS 82C574 MICRO CHANNEL INTERFACE CHIP

- Compatible with IBM Micro Channel specifications
- Provides highly integrated Micro Channel interface solution
- Flexible Card ID assignment
- Supports POS registers
- Resource relocation capability to avoid address conflict
- Flexible Interrupt level selection
- Sophisticated Card Channel Ready signal generator
- Two modes of operation:
 - Mode 1 for general purpose 8 bit slave I/O peripherals
 - Mode 0 for 82C570 CHIPSlink application
- Low power CMOS technology
- 68 pins PLCC package

The 82C574 is a highly integrated Micro Channel interface chip for IBM PS/2 personal computer application. It can be configured to operate in either of two modes; "mode 0" for 82C570 CHIPSlink 3270 coaxial protocol controller or "mode 1" for the 8 bit general purpose IO slave peripherals.

When **mode 0** is selected, the chip decodes the IO address of 02DXH and 022XH for IBM & IRMA registers and generates the IORD, IOWR signals for 82C570. It also decodes the memory space of 0CE000 to 0CFFFF for the display buffer and external micro code access by activating the MEMRD, MEMWR signals.

In **mode 1** operation, the 82C574 supports the microchannel bus interface to most 8 bit IO slave devices. The adapter IO address can be programmable during the setup procedure. This resource relocation capability avoids conflicts with the adapter's address. The interrupt level can also be selected via software. The 82C574 greatly simplifies the circuitry to interface to the microchannel bus.

The 82C574 is fabricated using advanced CMOS technology and is packaged in a 68 pin PLCC.

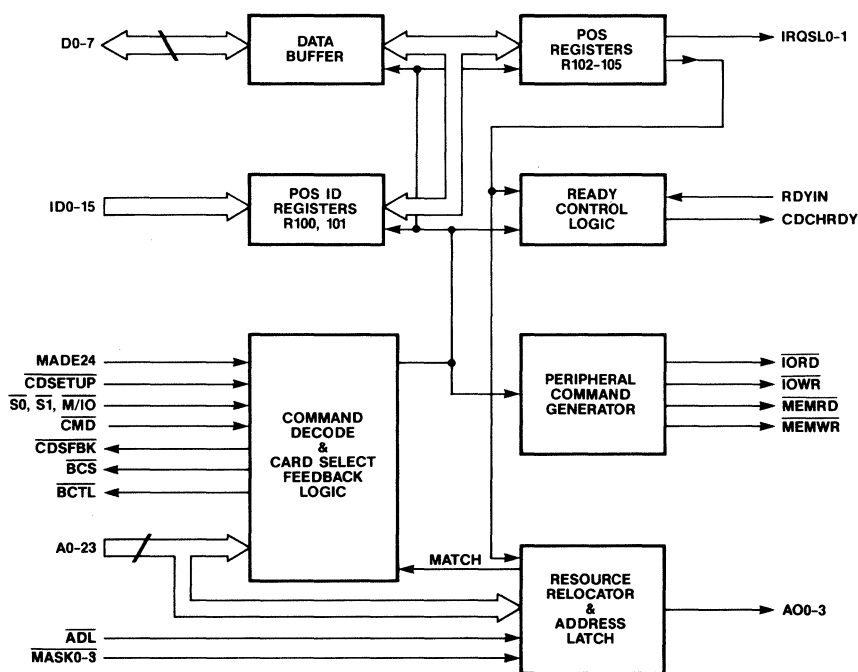


Figure 1. 82C574 Block Diagram

82C575 COMMUNICATION MICRO CHANNEL INTERFACE CHIP

- **Compatible with IBM Micro Channel specifications**
- **Provides highly integrated Micro Channel compatible interface solution for most communication adapter applications**
- **Suitable for most 8 bit slave IO peripheral applications**
- **Unique and flexible Card ID assignment**
- **Supports POS registers**
- **Four POS register bit outputs for system configuration**
- **Resource relocation capability to avoid address conflict**
- **Dual resource relocators to support multiple peripherals per card**
- **Sophisticated Card Channel Ready signal generator**
- **On chip system wait state generator**
- **Low power CMOS technology**
- **68 pins PLCC package**

The 82C575 is a highly integrated Micro Channel compatible interface chip for use in personal computer applications compatible with the IBM PS/2 standard. It supports the Micro Channel compatible interface to most of the 8 bit IO slave devices. The adapter IO address can be programmed during the setup procedure; this resource relocation capability avoids adapter address conflicts. The interrupt level can also be selected via software. The on-chip wait state generator allows the user to optimize the system bus timing to his/her specific needs. A unique Card ID generator does not require any external components.

All these features greatly simplify the design of a circuit to interface to the Microchannel™ compatible bus.

The 82C575 supports application markets such as intelligent Modems, SDLC/BISYNC/UART adapter card applications, instrumentation, etc. The dual resource relocater provides the capability to support multiple peripheral system with a maximum of 32 IO address space. The 82C575 is fabricated using advanced CMOS technology and is packaged in a 68 pin PLCC.

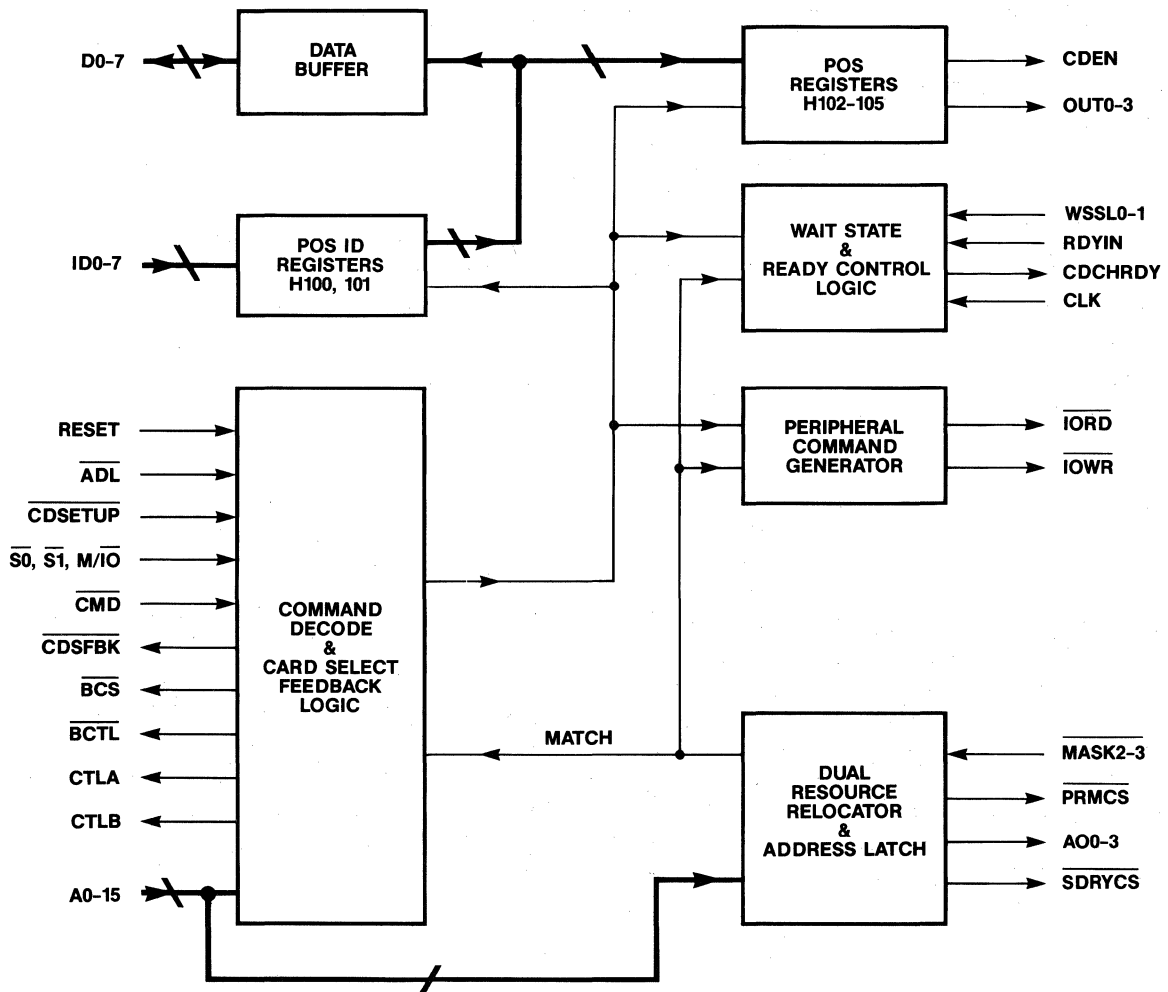


Figure 1. 82C575 Block Diagram

82C578 CHIPSterm SINGLE CHIP 3270 TERMINAL CONTROLLER

- Complete 3270 Terminal Controller on a single chip
- High speed microengine (10 MIPS) with 64K Bytes of Memory, 32K of I/O, and 128K of Font
- Unique 3-way arbiter to evenly balanced memory cycles
- Flexible display list processor for soft screen formats, multiple windows, multiple interlaced and non-interlaced displays
- Supports both color and monochrome monitor up to 60 MHz dot clock
- 16mA Centronics™ parallel interface
- Supports individual scan line display and random scan line
- Light-pen interface
- Supports all 3270 modes and receives 3299 packets
- User-definable screen formats:
 - Color remapping and background color
 - Variety of Rules: cross-hair, vertical and horizontal
 - Overscan
- User definable Character size: 5-16 wide by 1-32 pixels high
- Download feature for more economical solution
- Programmable wait-states for slow peripherals
- Supports both AT and PS/2 Compatible style keyboards
- EEPROM support
- CMOS technology in 144-pin PFP package

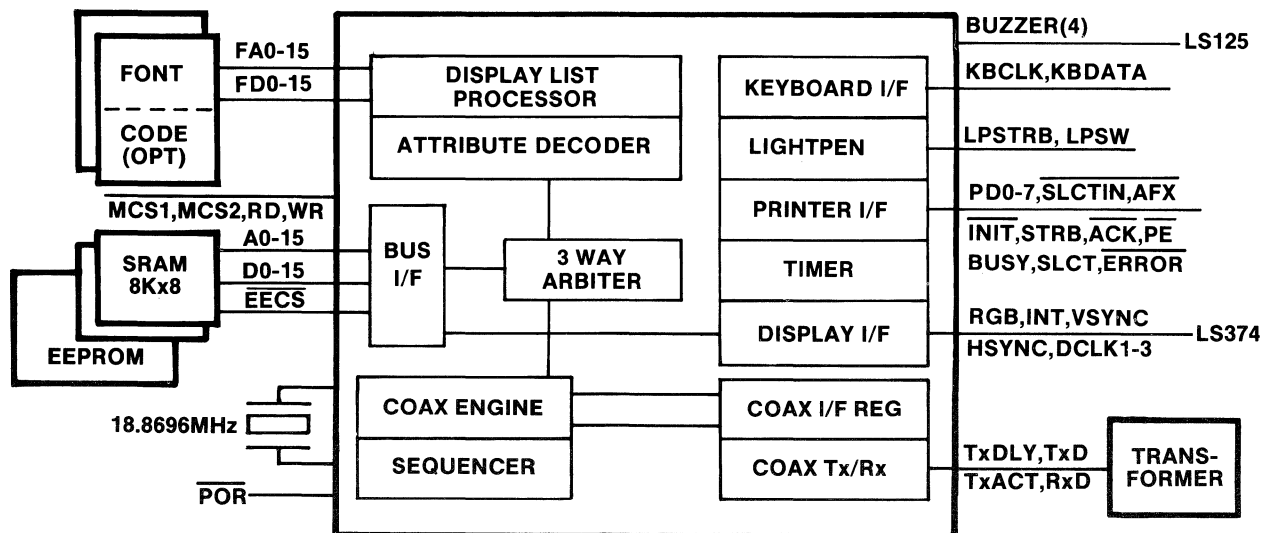


Figure 1. 82C578 Block Diagram

The 82C578 is a highly-integrated single chip processor to be used to design 3270 Display Stations such as 3191 and 3192-compatible display terminals. It has all necessary logic to handle 3270 coax protocol, coax transmitter/receiver, video sync generation, 3270 attribute, light-pen, keyboard, Centronics compatible parallel interface, security keylock, buzzer control, and many more. A complete

3270 compatible terminal consists of 2 buffer SRAM, 1 font EPROM, 1 configuration EEPROM, a transformer, an LS374 to drive the RGBI signals, and an LS125 for the buzzer.

82C601 SINGLE CHIP PERIPHERAL CONTROLLER

- **100% Compatible with IBM PC/XT, AT**
- **Two 16450 Compatible UARTs**
- **One IBM PC/XT, AT Compatible Enhanced Parallel**
- **ADAPTER mode functions:**
 - **Game Port Decodes**
 - **Select Pins for Serial & Parallel ports**
- **MOTHERBOARD mode functions:**
 - **IDE Interface**
 - **Real-Time Clock Chip Select**
 - **General Purpose Chip Select**
- **Power Saving & Power Down Modes**
- **16mA and 24mA Output Drivers**
- **Schmitt Trigger RESET Input**
- **Internal Address Decoders**
- **EISA Ready (MOTHERBOARD mode)**
 - **Relocatable Ports**
 - **Relocatable IRQ**
 - **Interrupt Sharing Capability**
- **Low Power CMOS**
- **80-pin PFP or 84-pin PLCC packages**

The 82C601 features two 16450 compatible UARTs, an enhanced parallel port, an IDE hard disk interface and chip selects (MOTHERBOARD mode) or select pins and Game port decodes (ADAPTER mode).

ADAPTER mode where the base addresses are determined by the select pins.

MOTHERBOARD mode where all the ports are relocatable, and power management that in-

cludes power down for each port, oscillator disable, and chip power down using the PWRGND pin.

The host interface is PC-compatible, i.e. D0-D7, A0-A9, \overline{IOR} , \overline{IOW} , AEN, INTR1, INTR2, INTR3, INTR4, and RESET, and can be connected directly to the bus. The system bus interface buffers (D0-D7, INTR₁₋₄) are capable of sinking 24mA, the parallel port interface signals are capable of sinking 16mA.

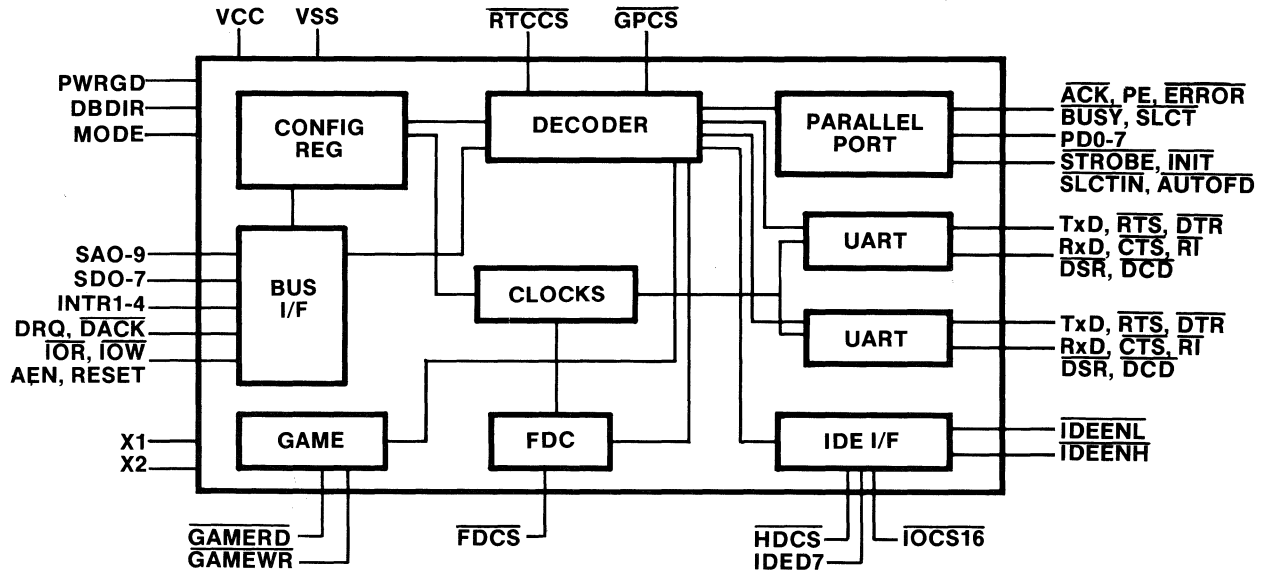


Figure 1. 82C601 Block Diagram

82C605/82C606 CHIPSpak/CHIPSport MULTIFUNCTION CONTROLLERS

- **100% Compatible to IBM PC/XT, AT**
- **Fully compatible to the NS16450 Asynchronous Communications Element, and the Motorola™ 146818A Real Time Clock (82C606 only)**
- **Provides a parallel interface which can be configured for use with either a printer or a scanner**
- **Provides two UART channels which can be powered from external sources**
- **Support for a game port**
- **Provides a Real Time Clock with 100 year calendar (82C606 only)**
- **CMOS Configuration RAM with Battery Backup support permits software selection of internal register base addresses (82C606 only)**
- **114 bytes of CMOS RAM**
- **Single chip 68-pin CMOS implementation**

The 82C606 CHIPSpak Multifunction Controller incorporates two UARTs, one parallel port, one game port decoder and one Real Time Clock. The UARTs are fully compatible to the NS16450 and the Real Time Clock is fully compatible with the Motorola 146818A. The 82C606 thus offers a single chip implementation of the most commonly used IBM PC/XT or AT peripherals. While offering complete compatibility with the IBM architecture, the chip offers enhanced features. These include support for power derived from three sources (main, auxiliary and standby), an additional 64 bytes of user RAM for the Real Time Clock and a software configuration scheme which permits development of a system configuration program.

The CHIPSpak Multifunction Controller can be used on the system board to provide serial and parallel ports or on a multifunction card to create a low cost, high density peripheral for use with general purpose microcomputer systems.

The 82C605 CHIPSport is a functional subset of 82C606 CHIPSpak. The two products are identical, with the exception of the Real Time Clock. The 82C605 does not integrate the Real Time Clock.

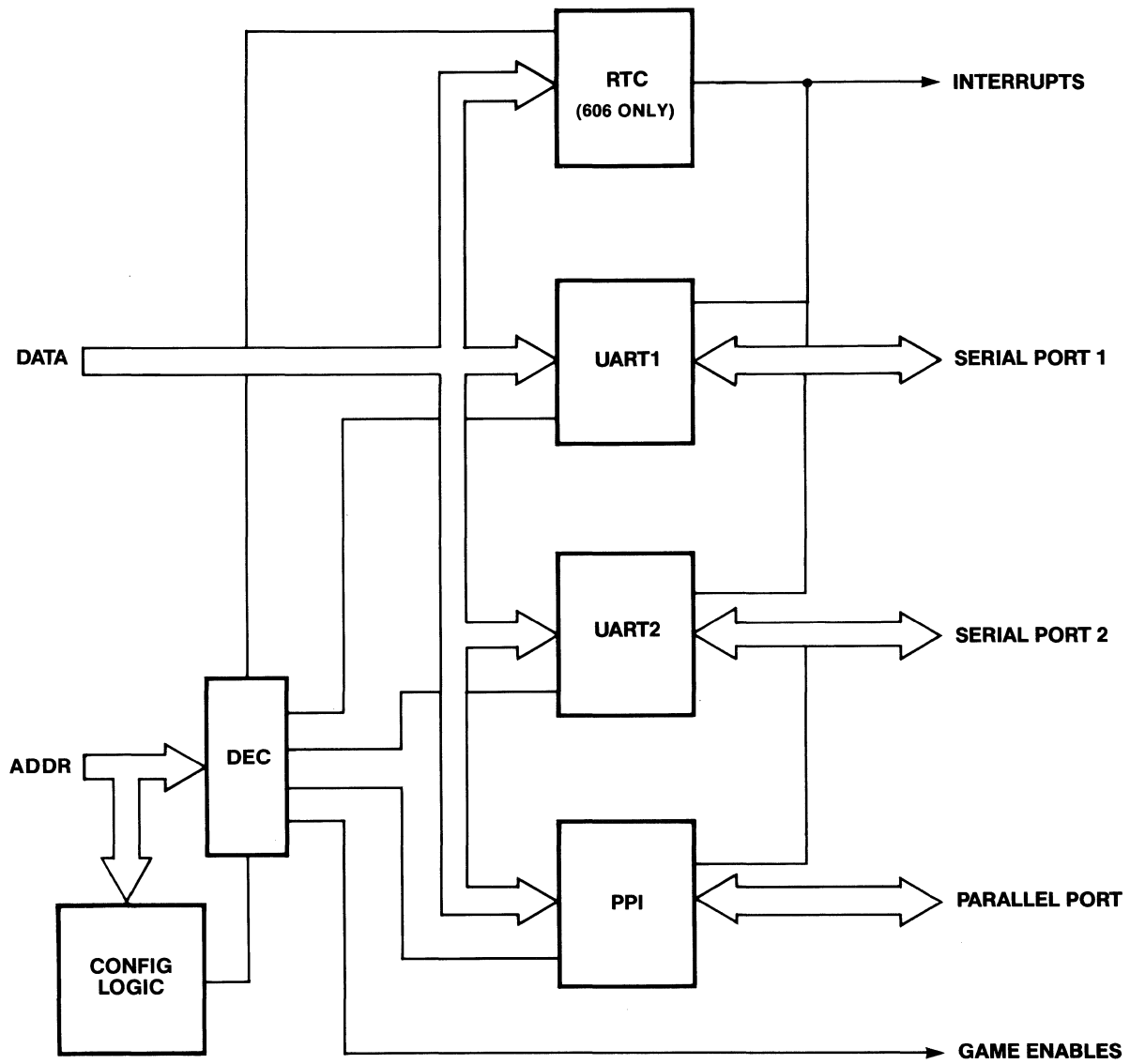


Figure 1. 82C605/606 CHIPSpak/CHIPSport Multifunction Controller Block Diagram

82C607 CHIPS/250/280 MULTIFUNCTION CONTROLLER

- Single Chip UART and Analog Data Separator
- 100% functionally compatible to the IBM PS/2 model 50, 60, and 80
- Fully compatible NS16550 Asynchronous Communications Element
- 16 bytes FIFO for transmitter and receiver buffers
- Easy interface to the industry standard floppy disk controllers (765A/765B/8272A)
- Supports multiple data rates (250K, 300K, and 500Kbps)
- High drive, 48 mA output buffer
- Schmitt trigger inputs
- Low power advanced CMOS technology
- 68 pin PLCC or 80 pin Flat Pack

The 82C607 Multifunction Controller incorporates a single channel UART, an analog floppy disk data separator and the host interface logic compatible with IBM PS/2 model 50, 60, and 80 personal computers.

The UART is functionally compatible to NS16550 Asynchronous Communications Element. The data separator contains a self-calibrated analog phase locked loop (PLL), write precompensation circuit, and the logic interface to the industry standard 765A/765B/8272A floppy disk controller. It supports three

standard data rates: 250K, 300K, and 500K bits per second, each selectable by software.

Together with 765A/765B/8272A, the 82C607 provides a very cost effective and high performance implementation for the serial port and the floppy disk sub-system for systems compatible to the PS/2 environment.

The 82C607 is implemented using advanced CMOS technology; available in 68 pin PLCC or 80 pin Flat Pack packages.

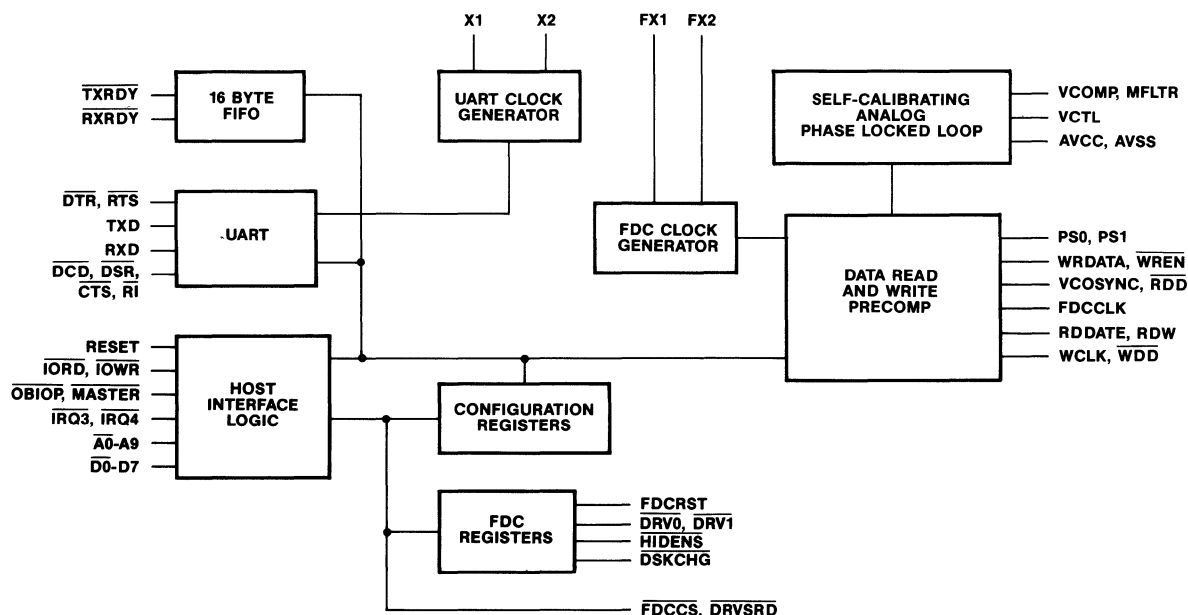


Figure 1. 82C607 Block Diagram



MASS STORAGE



**82C710
PC/AT COMPATIBLE MULTIFUNCTION FLOPPY CONTROLLER**

- Low Power Advanced 1.5 μ CMOS Technology, 100 QFP Package
- 16450 Compatible Serial Port
- Enhanced Bi-Directional Parallel Port with 16 mA Output Drive
- General Purpose Programmable Chip Select
- PS/2 Compatible Type Mouse Port Logic With Driver Support
- IDE Interface for Embedded PC/AT and PC/XT Hard Disk Drives
- Integrated Floppy Subsystem
 - μ PD72065B Compatible Floppy Controller
 - Analog PLL with Transfer Rates Up To 1 Mbits
 - 48 mA Floppy Drive Interface Buffers
 - Programmable Precompensation Modes
- 100% IBM PC/XT, AT Compatible Register Set
- 16mA PC/XT, AT Compatible Host Interface Drive Capability
- Complete On-Board Power Management Features

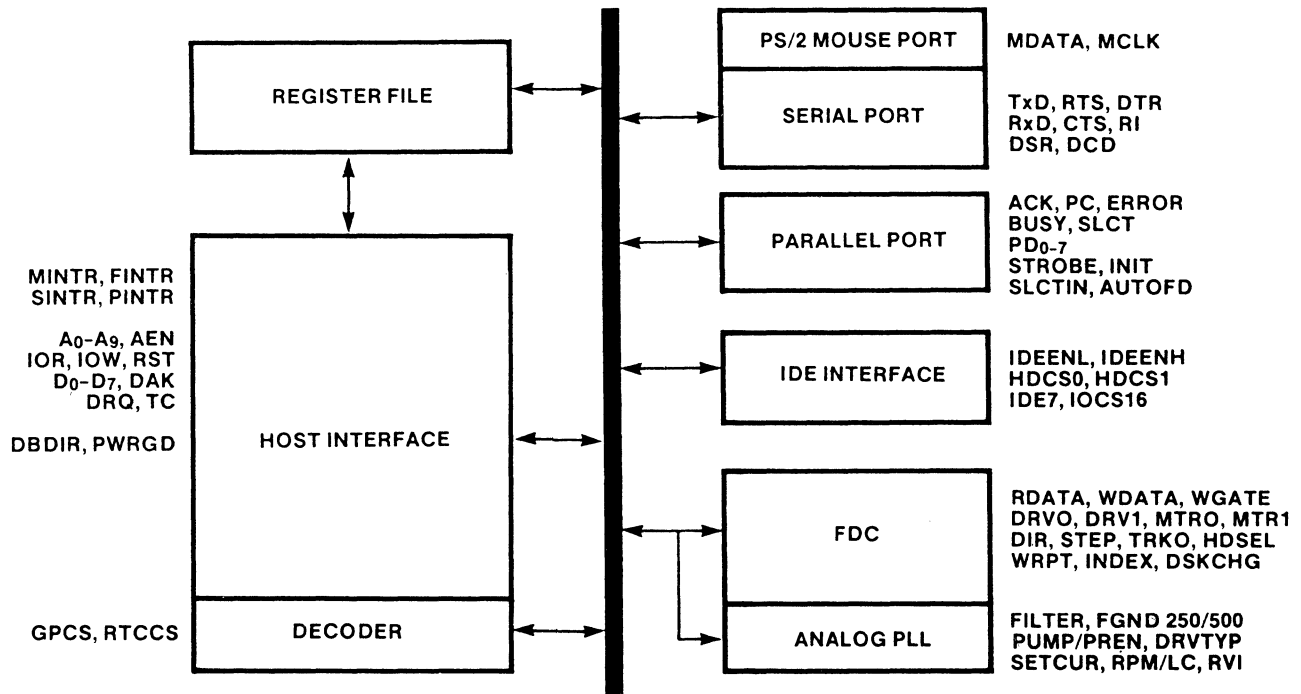


Figure 1. 82C710 Block Diagram

The 82C710 is a single chip offering the complete I/O solution for the PC/XT, AT compatible motherboard environments today. The 82C710 provides the functionality of a 16450 compatible UART, which when coupled with a 145406 and a 1488 results in the implementation of a complete PC/XT, AT compatible serial port. The parallel port is just like the one on the PC/XT, AT compatible and supports the PS/2 compatible bi-directional mode of operation. In addition it supports a drive capability of 16mA, which alleviates the need for external buffers. A PS/2 compatible mouse

port is provided, along with the drivers necessary to support it in a PC/XT, AT compatible environment. The IDE interface logic needed on the host end to support embedded PC/XT, AT compatible hard disk drives is provided by the 82C710, thereby contributing to lower chip count on the motherboard. A complete floppy subsystem consisting of a μ PD72065B floppy core, an analog data separator, capable of transfer rates up to 1 Mbits/s and the host interface registers is on-board in the 82C710. The 82C710 provides complete power management and software configurability, thus providing the most optimum solution of its kind in the market today.

**82C781
HARD DISK MICRO CHANNEL INTERFACE CHIP**

- Low power advanced 1.5 μ CMOS technology
- On-board Micro Channel Compatible Arbitration Logic
- On-board Bus Acquisition Logic
- On-board POS 102 and 103 register
- Provides CARD ID read controls
- Provides programmable address select capability through the POS 104 and 105 registers
- Provides optional, register-definable CARD ID in conjunction with the 82C782
- Provides synchronous and asynchronous bus transfer cycle extension
- Programmable burst length capability
- Provides external read decodes for diagnostic registers
- 68-pin PLCC or 80-pin Flat Pack

Functional Description:

The 82C781 Hard Disk Micro Channel Compatible Interface Chip provides the interface between the Micro Channel bus and the hard disk controller or other DMA/I/O slave-oriented peripherals.

When used in a hard disk mode, it works in conjunction with the 82C782 Hard Disk Data Manager Chip to facilitate bus acquisition and DMA transfers. It also decodes the bus addresses and status ($\overline{M/\overline{IO}}$, $\overline{S0}$, $\overline{S1}$) for I/O slave reads. When used in the general purpose mode, it will work in conjunction with other

DMA or I/O slave peripherals (as long as the handshake requirements are met) to provide the Micro Channel interface functions.

Together with the 82C782, a disk formatter and a data separator/encoder, the 82C781 provides a very cost-effective and high-performance implementation of the Fixed Disk Adapter for systems compatible to the PS/2 environment. On the other hand, the 82C781 provides the Micro Channel interface for other DMA/I/O slave oriented peripheral adapters, thus allowing the designer to concentrate on the main task of adapter design.

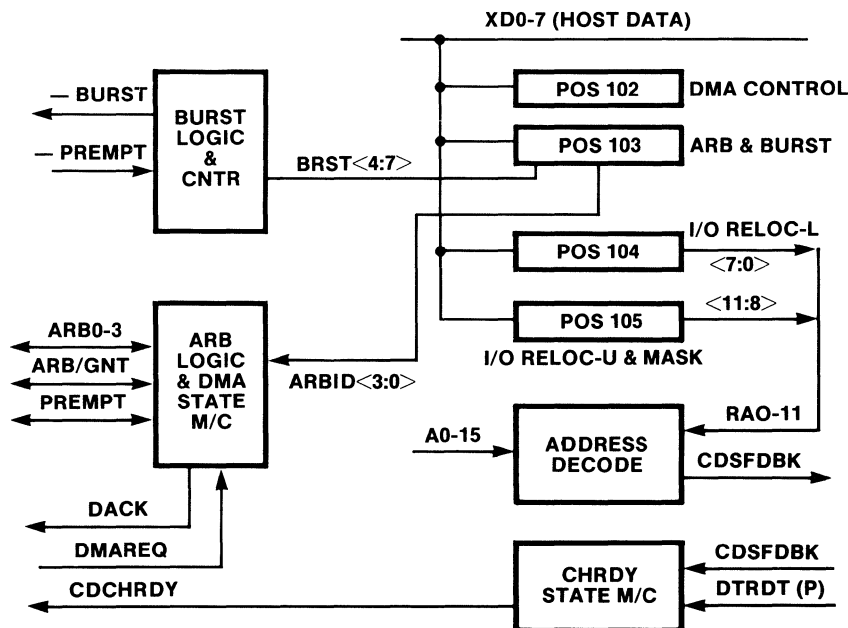


Figure 1. 82C781 Block Diagram

82C782 HARD DISK DATA MANAGER

- Low power advanced 1.5 μ CMOS technology
- PS/2 Model 50/60 compatible
- On-board register file for command and status
- Slave DMA controller, max 2.5 MBytes/s to the host
- 8-/16-bit data pipeline to sustain high bus transfer rates
- On-board address generation for local buffer
- Provides address generation during local CPU buffer accesses, with optional auto-increment capabilities
- Addresses up to 64K of static RAM
- Supports both 8751 and 68HC11 microcontroller families
- Provides interrupt to the local CPU
- Supports Adaptec AIC-011 and compatible formatters
- Supports 1:1 interleave
- Supports ST506 type drives
- 84-pin PLCC package

Functional Description:

The 82C782 Hard Disk Data Manager Chip provides the DMA, buffer management and register file functions for the Fixed Disk Adapter in the PS/2 Micro Channel environment. The slave DMA controller is responsible for

transfer of data between the disk and local buffer and also between the local buffer and the host. It ensures an interleaved data transfer between disk and host, and hence facilitates a 1:1 interleave capability. It operates at 10 MHz and supports up to 64K of direct static RAM

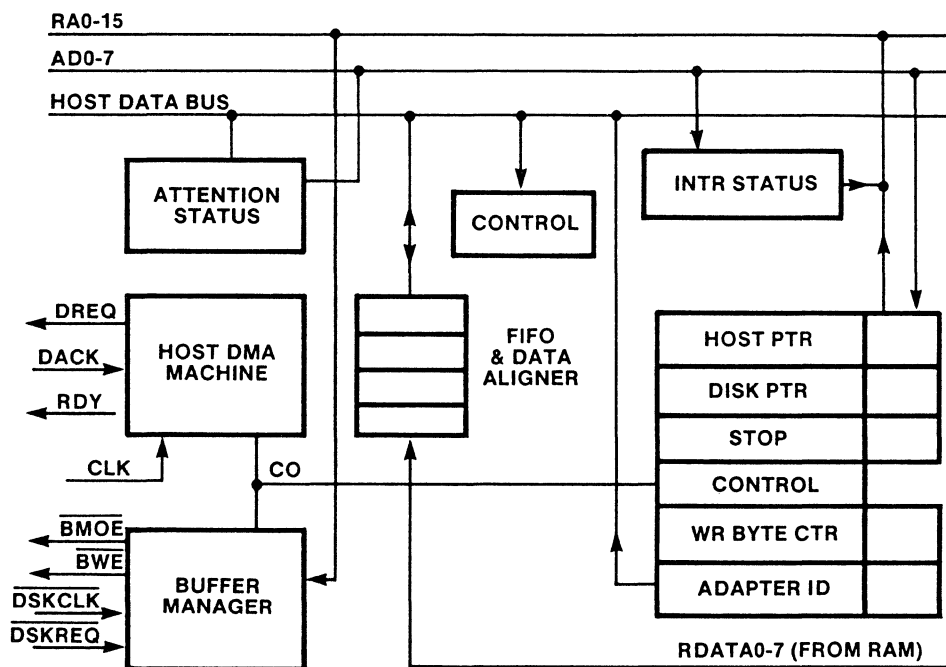


Figure 1. 82C782 Block Diagram

addressing capability. It also provides the PS/2 Compatible register file of Control, Status, Attention and Interrupt Status registers.

The 82C782 works in conjunction with the 82C781 and a local microcontroller to provide

the data path functions between the disk and the host. This, combined with a disk formatter and a data separator/endec, results in a low-cost Fixed Disk Adapter implementation for systems compatible with the PS/2 environment.

**82C784
MFM/RLL DATA SEPARATOR & ENDEC**

- Low Power advanced 1.5 μ CMOS technology
- Onboard 5 Mbits/s MFM(1,3) encoder/decoder
- Onboard 7.5 Mbits/s RLL(2,7) encoder/decoder
- Synchronous start-up Phase-Locked Oscillator (PLO)
- MFM Write Precompensation with built in delay line
- De-glitched Read/Reference Clock output
- Onboard Address Mark Detection circuitry
- Provides NRZ interface to the disk controller chip
- Dedicated Analog Vcc/Gnd for better noise immunity
- Onboard 48 mA drivers/receivers for disk data lines
- Single +5V operation (Digital & Analog)
- 44 pin PLCC package

The 82C784 provides the Data Separation function and a user selectable MFM or 2,7RLL encode/decode function, for the Disk Data Path. When used in conjunction with the

82C780, it results in the implementation of a low cost Fixed Disk Adapter for the PS/2 Micro Channel Compatible environment and greatly reduces board space, while enhancing the performance.

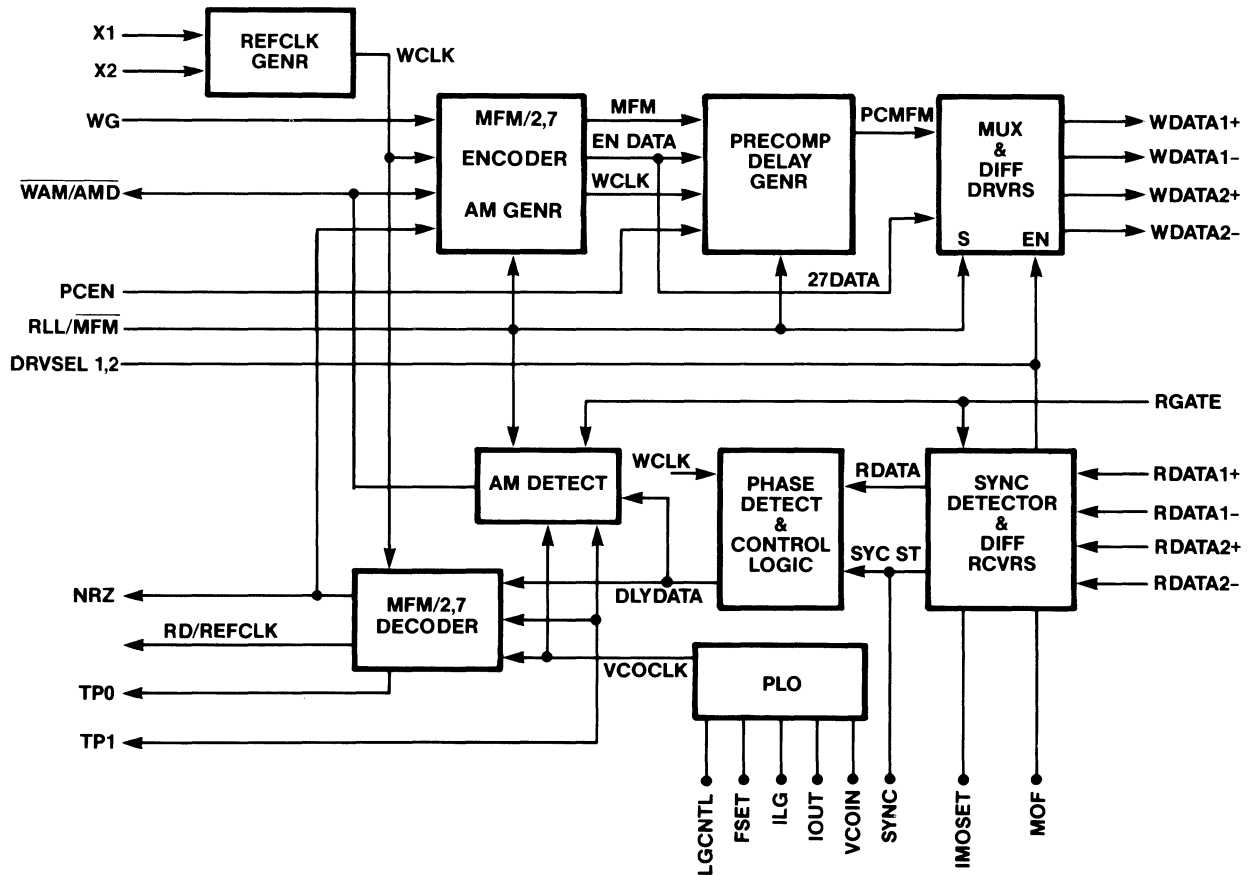


Figure 1. 82C784 Block Diagram

The 82C784 boasts of a high level of integration by supporting both the MFM & RLL encode/decode schemes, along with the synchronous start-up Phase Locked Oscillator and the dif-

ferential driver/receiver pairs for the disk data path signals. The advanced architecture also results in the use of a minimum number of passive components.

**82C785
SINGLE CHIP PC/AT HARD DISK CONTROLLER**

- Low Power Advanced 1.5 μ CMOS Technology, 100 QFP/84PLCC
- 100% IBM PC/AT Compatible Task File Support
- 24 mA Drivers for Direct Interface to the PC/AT Bus
- Auto-Generated Wait States For Interfacing to Fast Hosts
- PIO and DMA Modes for Buffer Data Transfers Up To 8 MBytes/s
- Auto-Command Mode to Speed Up Disk Command Response
- Support for Daisy Chaining of Two Embedded Drives
- Control for Implementation of a 64K Dual Port Static RAM Buffer
- Optional Auto-Increment of Address Pointer for Local CPU to Buffer Access
- Higher Buffer Memory Throughput, Up To 10 MBytes/s
- Supports Disk Data Rates Up To 24 Mbits/s
- Programmable Disk Sequencer RAM of 30 x 4 Bytes
- Optional Dual Brand Registers
- Support for 16-Bit CRC and 32/56-Bit Programmable ECC
- Provides Complete On-Board Power Management Features

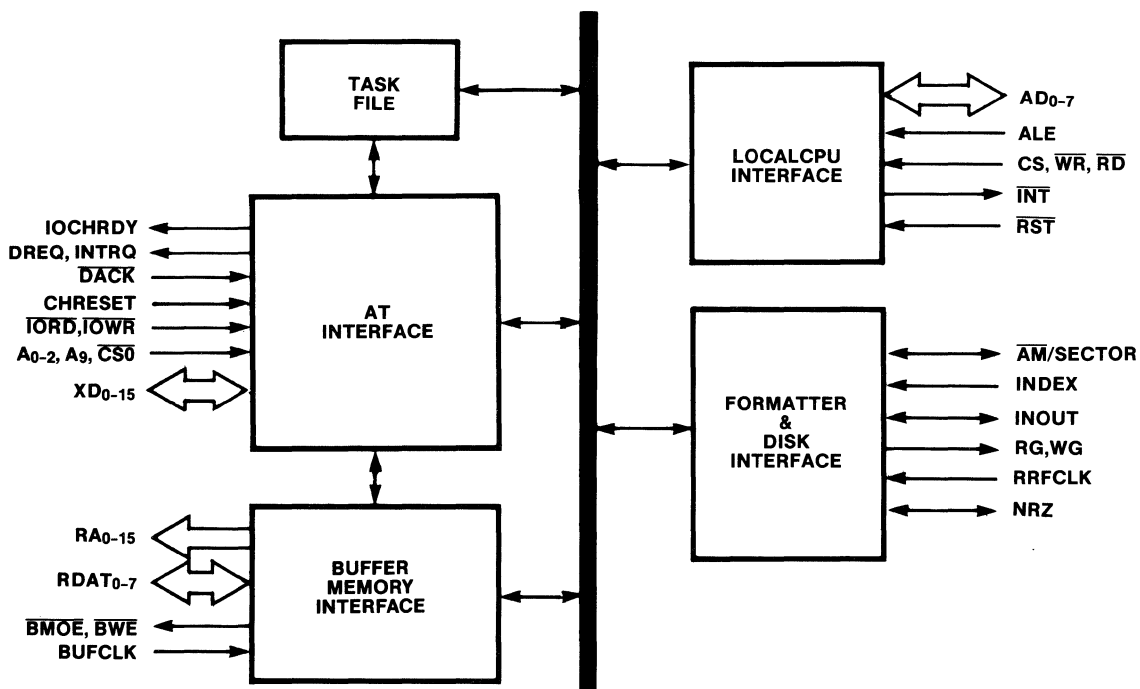


Figure 1. 82C785 Block Diagram

The 82C785 is an enhanced, high-performance VLSI circuit that provides an optimum implementation of a Winchester disk controller for the PC/AT compatible interface. It incorporates the function of a disk formatter, buffer memory controller and AT bus interface controller. It is capable of accomplishing 1:1 interleave format with concurrent transfers of up to 24 Mbit/s on the disk and 8 MBytes/s on the host. The built-in AT interface logic, with

24 mA drive capability, allows the chip to support the 40-pin Connors interface, popular with the embedded disk drive designs. In addition the 82C785 provides support for complete power management, thereby lending itself to drive implementations oriented towards the laptop market. Also because of its high integration levels, it provides an opportunity for the OEM to develop low-cost solutions for the add-on board market.

10C5055B

MEMORY CONTROLLER AND PROGRAMMABLE DATA SEQUENCER

Memory Controller Features

- Low Power 2 μ CMOS Technology
- High Performance Dual Bus Architecture
- Two Independent DMA Channels
- 8 Megabyte Device Bandwidth at 32 MHz Clock
- 16-bit Address and Count Registers for Each Channel for the 5055B
- Independent Mask for Channel-End Interrupt
- Bus Access Resolved on Channel Priority Basis
- Logic to De-Multiplex the Microprocessor Address/Data and Drive the Low Order Microprocessor Address Lines
- Programmable Request/Acknowledge and Interrupt Polarity
- Programmable Auto Count Re-Initialization
- Programmable Memory Access Cycle Timing (2 to 5 Clock Cycles)
- Buffer Memory Address for 64K (2 Memory Chip Enables for 32K x 8 SRAM)
- DRAM Support for up to 1 Megabyte
- Data Memory Parity, Check and Generate Option (In 8 Bit Mode)
- 16 Bit Host Transfer Support (With 16 Bit Memory)
- Channel 1 Optional Level Request

Device Control Features

- High Level Instruction Set Including:
 - Read/Write
 - Individual Sector Formatting
 - Track Formatting
 - Read ID
 - Read/Write Long

- Read Syndrome
- Verify (With Data In Buffer)
- Check Data ECC
- Check Track Format
- Supports Up To 15 MHz Serial NRZ Bit Rate
- Programmable Disk Format:
 - Programmable Sector Size Up to 65,536 Bytes Per Sector
 - Programmable ID Data and Length
 - Programmable Gap Sizes and Fill Characters
 - User-Definable Header Flag Byte or Nibble
 - Selectable 32, 48 or 56-Bit ECC Polynomial and ID CRC
 - Disk-Compatible ID and Data Field CRC
- Hard or Soft Sector Modes
- NRZ Serial Disk Interface
- Direct Interface to ESDI Type Drives, Both Hard and Soft Sectored
- Multi-Sector Transfer Capability With Automatic Sector Increment
- Programmable Automatic ID Retries
- Store Logic to Access External Registers on the Microbus
- Logic to Transfer Data Between the Microbus and Buffer Memory
- ESDI ID Sync Timeout Programmable Option
- ESDI Write Gate to AM ENABLE Programmable
- Format Track With Data From Buffer
- Programmable Write Gate Disable for Embedded Servo

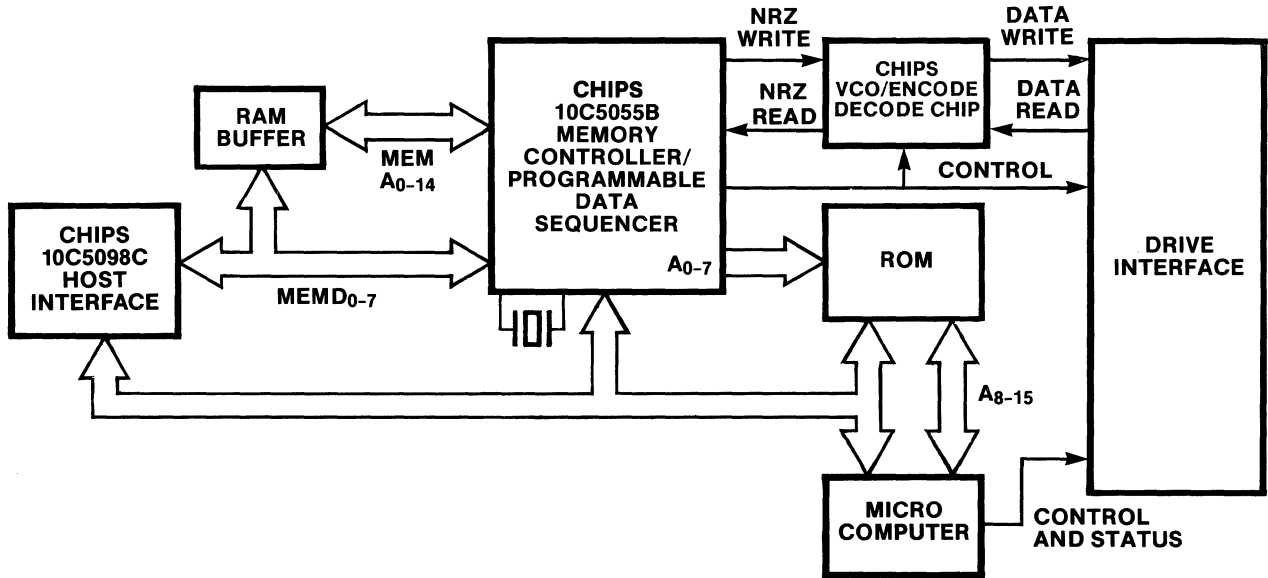


Figure 1. 10C5055B Block Diagram

82C5059 SINGLE CHIP PC/AT DISK CONTROLLER

Memory Controller Features

- Two Independent DMA Channels
- 13 Megabyte Device Bandwidth at 40 MHz Clock
- 20-Bit Address and 16-Bit Transfer Count Registers For Each Channel
- Holding Registers for Addresses Counts for Non-Contiguous Memory Transfers
- Bus Access Resolved on Channel Priority Basis
- Programmable:
 - Interrupt Polarity
 - Auto-Count Re-Initialization
 - Memory Access Cycle Timing (2 To 5 Clock Cycles)
- Buffer Memory Address for 64K SRAM (2 Memory Chip Enables for 32K x 8 SRAM)
- DRAM Support For Up To 1 Megabyte

Programmable Data Sequencer Features

- High Level Instruction Set
- Supports up to 20 MHz Serial Bit Rate (NRZ)
- Programmable Disk Format
- NRZ Serial Disk Interface
- Direct Interface to ESDI Type Drives

- Multi-Sector Transfer Capability with Automatic Sector Increment
- Programmable Automatic ID Retries
- ESDI ID Sync Timeout Programmable
- ESDI Write Gate to AM ENABLE Programmable
- Format Track With Data From Buffer
- Programmable Write Gate Disable for Embedded Servo
- 32, 48, 56 Bit ECC Polynomial

AT Interface Features

- Direct Interface to AT Compatible Systems, Including 40-Pin Bus Interface
- High Current Drivers for Host Interface
- Schmidt Trigger Inputs Form Host Interface
- Configurable Primary or Secondary Address
- 2 Word FIFO
- Automatic BUSY, INTRQ and ECC Mode
- Flexible Interrupt Capability
- Advanced 1.5 μ CMOS, Low Power Technology
- 100-Pin Quad Flat Pack Packaging

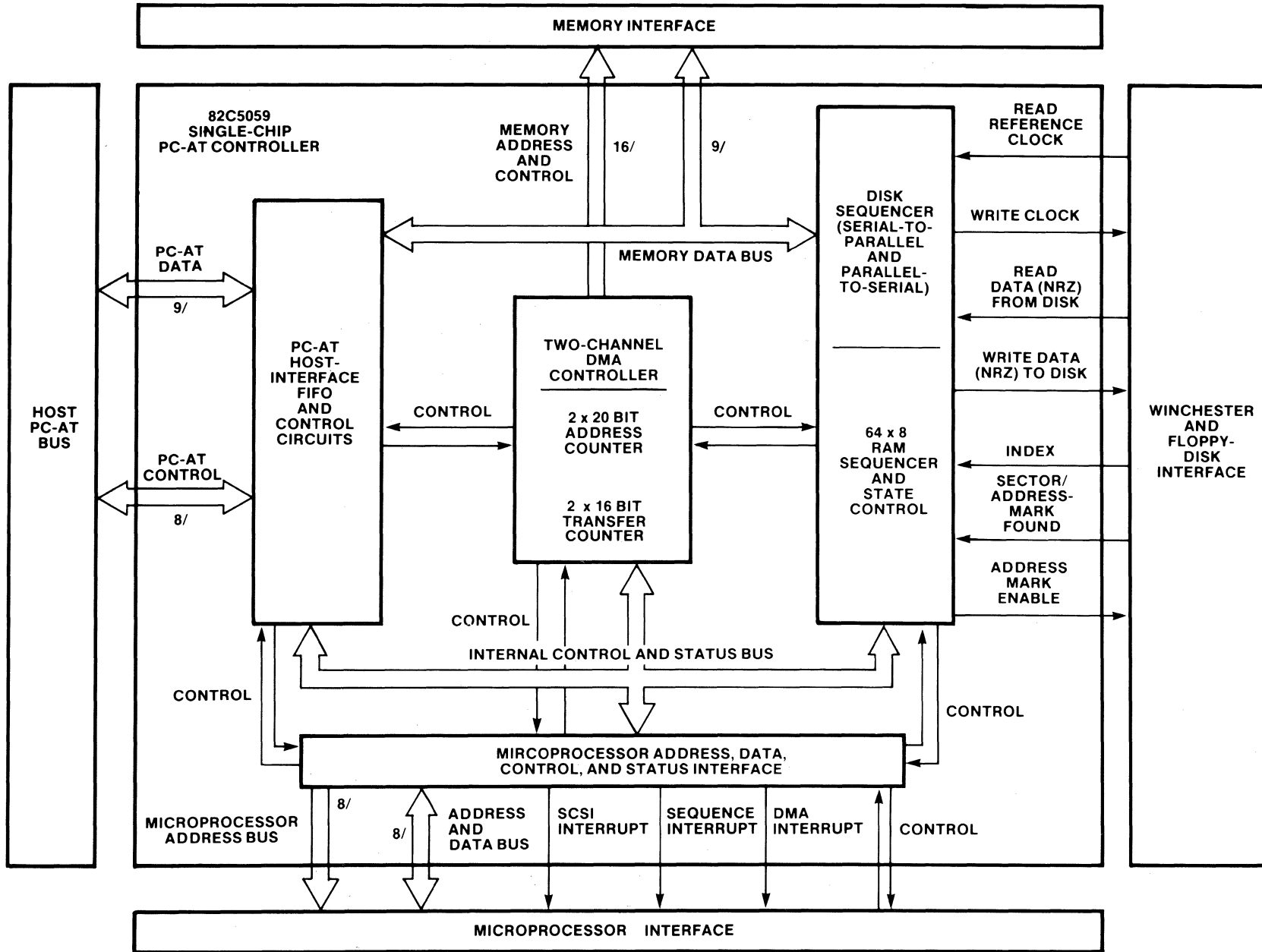


Figure 1. 82C5059 Block Diagram

10C5080C SCSI MULTIFUNCTION DEVICE

- Includes Single-Ended Drivers/Receivers
- Supports the Following Types of Interfaces:
 - SCSI Bus
 - Winchester Disk drives ST506/412, ESDI
 - QIC-02 Streaming Tape
- Up to 2 Megabytes Per Second Asynchronous SCSI Data Transfer Rate
- Programmable I/O or DMA Transfer Mode
- Programmable Microprocessor Interrupt Mode
- Microprocessor Direct Control of Bus Signals
- Programmable SCSI Initiator or Target Role
- Supports SCSI Disconnect/Reconnect Functions
- Programmable SCSI Arbitration Delay and SCSI Timings From Clock Input
- Programmable SCSI Initiator and Target IDs
- Support Hard and Soft Reset
- Programmable Bus Parity Check/Nocheck
- Separate DMA and I/O Data Paths Allowing Overlap DMA Transfers
- Includes Six Bus Drive Ground Pins.
- 68 Pin Plastic Package and 80 Pin Quad Flat Pack
- Low Power 2 μ CMOS Technology

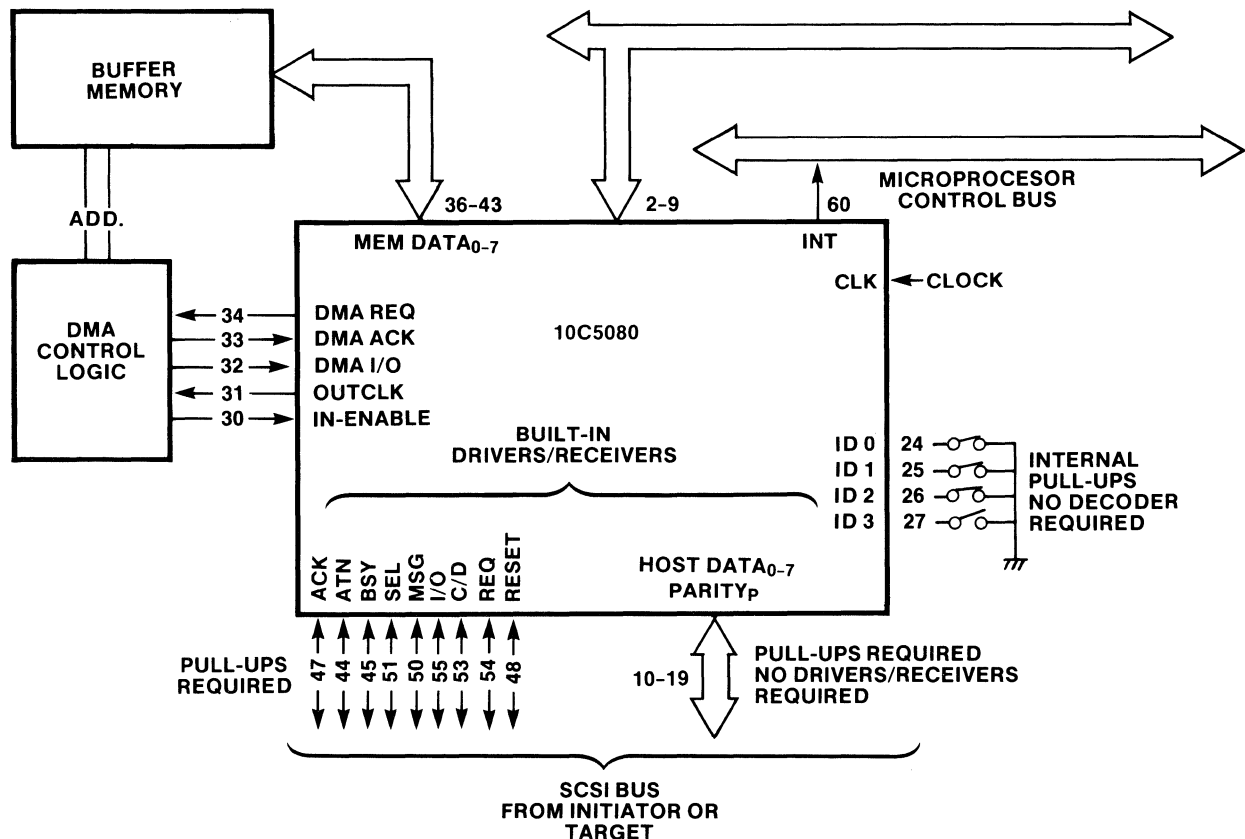


Figure 1. 10C5080C Block Diagram

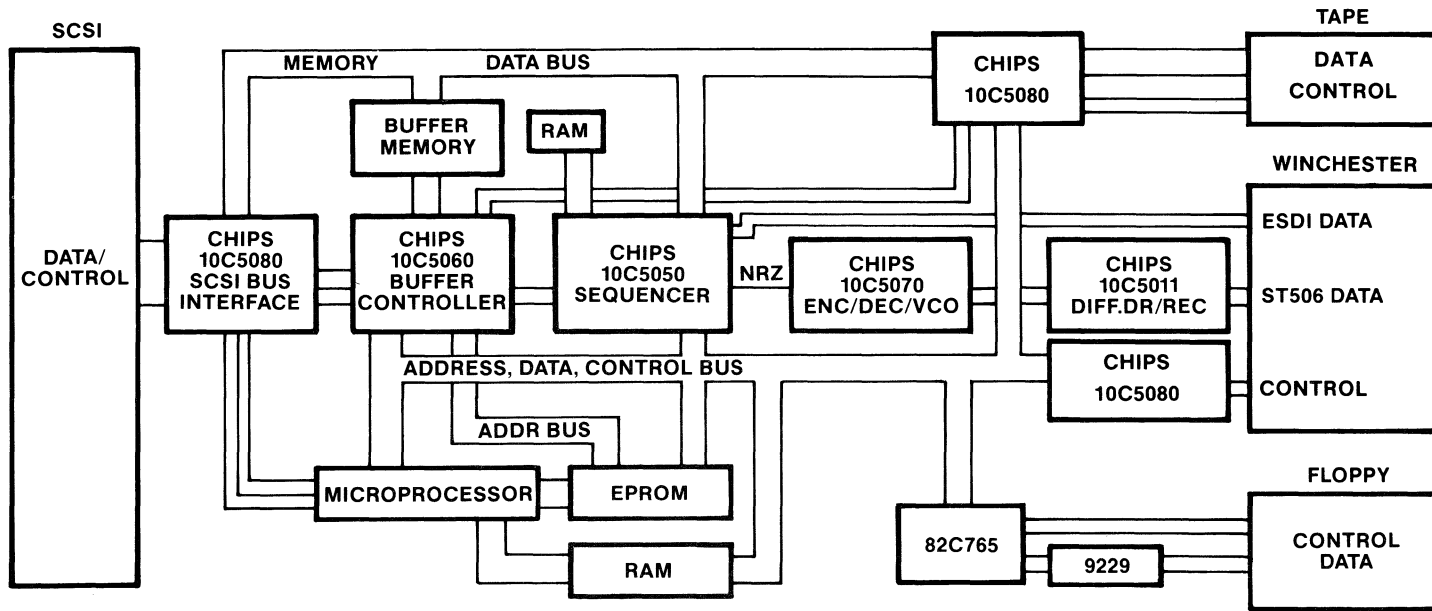


Figure 2. 10C5080C Typical System Configuration

82C5086B
SYNCHRONOUS/ASYNCHRONOUS SCSI PROTOCOL CONTROLLER

- 5.3 Megabyte Data Transfer Rate
- Support for Wide SCSI Bus
- Internal State Machine
- 64-Byte FIFO—Offset of 63
- 16-Bit Host Interface
- Queue for Four SCSI Command Sequences
- Pipelined Commands Plus Control Queuing
- Powerful Command Set: One Command Performs Any One of a Variety of Initiator or Target Sequences
- Multiported Bus Structure
- Pipelining for Up to Four Commands
- 6 Separate On-Chip 32-Byte Scripts for SCSI Command and/or Message Queuing
- Synchronous Transfer Mode Provides:
 - Sustained Data Transfer Rates of 5.3 Megabytes/Second
 - Programmable Offset to 63 (64-Byte FIFO)
- Asynchronous Data Transfer Rates up to 4 Megabytes/Second
- Single-Ended Drivers and Receivers
- Support for Differential Drivers and Receivers
- Support for Wide SCSI Bus (Multiples of 8 Bit)
- Connects to Non-Multiplexed and Multiplex Address/Data Microprocessor Bus
- Clock Rate Up to 32 MHz
- Pin-Compatible with 10C5080 Asynchronous SCSI Controller
- 68-Pin and 84-Pin Plastic Leadless Chip Carrier, 80-Pin Flat Pack
- Low Power, Advanced 1.5 μ CMOS Technology

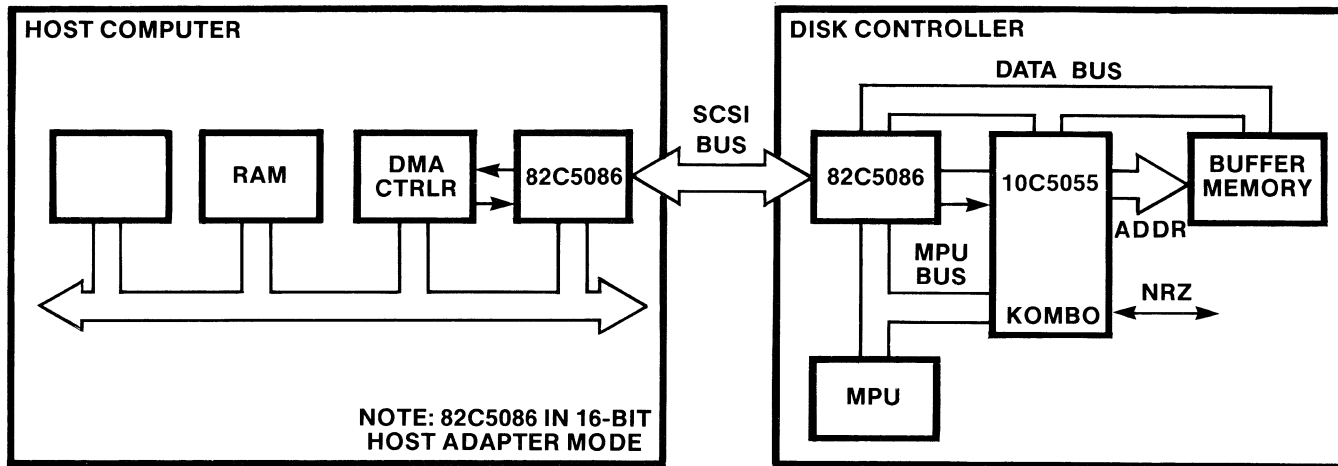


Figure 1. 82C5086 Block Diagram

**10C5098C
PC/AT COMPATIBLE INTERFACE**

- High-Performance Dual-Bus Architecture
- Direct Interface to PC/AT Compatible Systems
- No External Logic Required with Chips 10C5055B Device
- Support for External Floppy Controller
- High Current Drivers For Host Interface
- Schmitt Trigger Inputs From Host Interface
- Configurable Primary or Secondary Address
- 2-Word FIFO
- Automatic BUSY, INTRQ and ECC Mode
- Compatible with AT Drive 40-Pin Bus Interface
- Low Power 2 μ CMOS Technology
- Available in 84-Pin PLCC Package or 80-Pin QFP Package

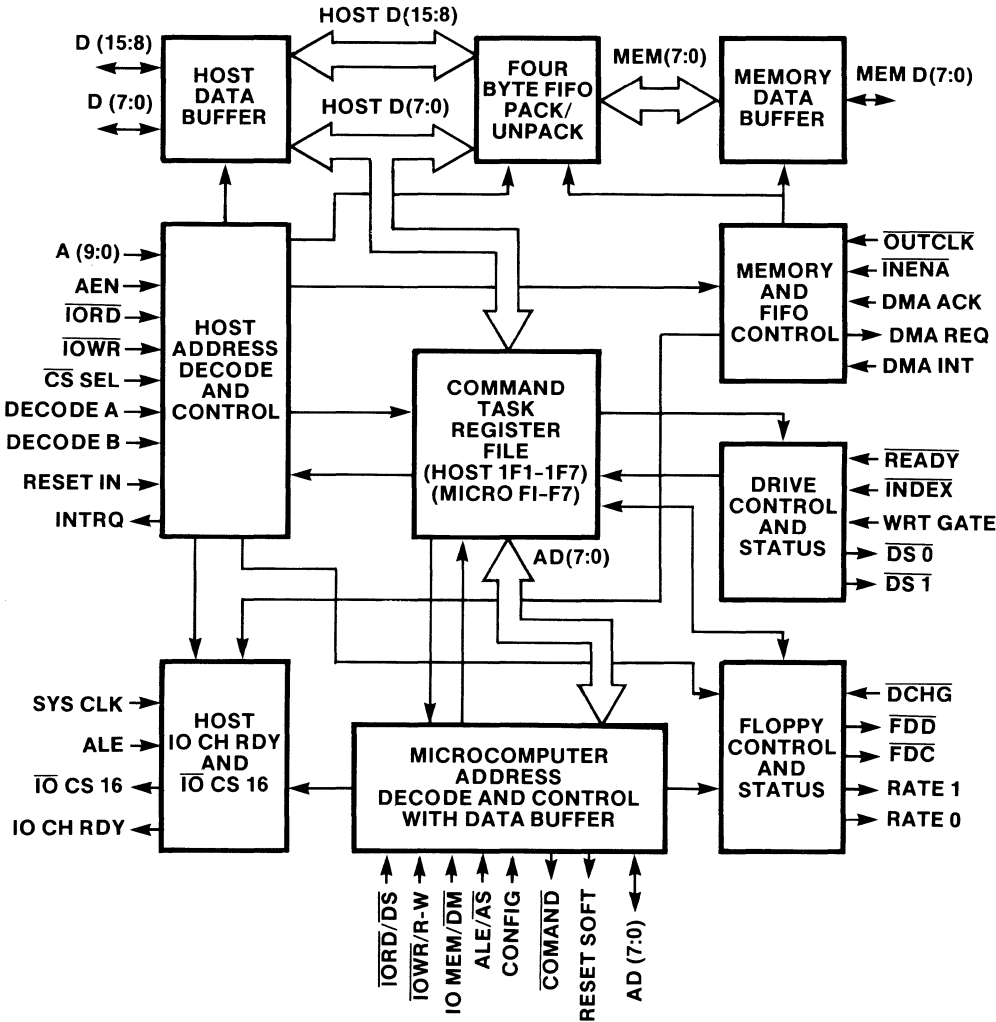


Figure 1. 10C5098C Block Diagram

CHIPS

BIOS & DRIVERS

OC82C100 SXT XT COMPATIBLE BIOS

- Fully compatible with the IBM XT BIOS
- Supports CPU speeds up to 10 MHz
- Optimized for performance with the CS82C100 SXT CHIPSet
- Developed using Clean-Room Methodology
- Support for 82C425 LCD CGA Controller Chip
- Easy customization of key BIOS parameters
- Supports 8086 or 8088 processors
- Total Hardware/Software Support

Overview

The OC82C100 Super XT (SXT) Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CS82C100 SXT CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM XT BIOS. It provides all of the standard features, including support for:

- 8086 and 8088 processor and 8087 math coprocessor operating at clock speeds from 4..77 MHz to 10 MHz
- Low capacity 5.25-inch diskette drive
- 84, 101, or 102 key keyboard
- Monochrome and CGA video adapters
- Power-on self test diagnostics

Complete BIOS Solution

The OC82C100 BIOS is available in two forms to best meet the needs of the OEM. The SK82C100 BIOS Software Kit provides a production-ready master copy of the system BIOS and utility programs to customize the BIOS. The SC82C100 BIOS Source Kit provides the source code and documentation for the system BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows

many common modifications of BIOS and CHIPSet configuration parameters. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS82C100 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC82C100	SXT BIOS (Label)
CB82C100	CS82C100 SXT CHIPSet with OC82C100 BIOS (Label)
SK82C100	SXT BIOS Software Kit
SC82C100	SXT BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object

Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

**DR82C100
SXT EMS DRIVER KIT**

■ **Optimized for the CS82C100 SXT CHIPSet**

■ **Supports LIM 4.0 EMS Specification**

Overview

The DR82C100 SXT EMS Driver Kit provides driver software to support EMS based on the CS82C100 SXT CHIPSet. The DR82C100 software is designed to utilize the capability of the CHIPSet to operate according to the LIM (Lotus, Intel, & Microsoft) 4.0 EMS Specification.

The Driver's main job is to initialize the CHIPSet EMS registers to function according to the specified setup. Once the driver is installed, it acts as an interface between the system and the EMS hardware. It provides service function calls that allow an application to access the EMS memory.

The EMS Driver is capable of handling up to 8 megabytes of memory (limit of the CHIPSet). The EMS memory size must be setup either by the BIOS or a CHIPSet configuration program. The driver has options to select the base EMS I/O address, the page frame address, the maximum number of open processes, and enable an extensive memory diagnostic test during initialization.

Included on the diskette with the driver is documentation describing installation and usage of the EMS driver.

■ **Total Hardware/Software Support**

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS82C100 CHIPSet with the DR82C100 drivers and utilities. The CHIPSet together with the drivers and utilities have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

DR82C100	SXT EMS Driver/Utility Kit
DS82C100	SXT EMS Driver/Utility Source Kit

CHIPS' software products are obtained by an OEM through license agreement. An OEM Software License Agreement must be signed and returned before ordering a CHIPS' Driver/Utility product. This agreement entitles the OEM to reproduce and distribute one copy of the driver/utility software with each product containing the appropriate CHIPSet.

OC82C100+ ENHANCED SXT XT COMPATIBLE BIOS

- A Superset of the IBM XT BIOS
- Optimized for performance with the CS82C100 SXT CHIPSet
- Support for 82C425 LCD CGA Controller Chip
- Supports 8086 or 8088 processors
- Supports CPU speeds up to 10 MHz
- SETUP embedded in BIOS using CMOS RAM
- Supports 5.25-inch and 3.5-inch diskette drives
- Built-in support for CHIPS Multifunction Controller
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC82C100+ Enhanced Super XT (SXT) Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CS82C100 SXT CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM XT BIOS. It provides all of the standard features, including support for:

- 8086 and 8088 processor and 8087 math coprocessor operating at clock speeds from 4.77 MHz to 10 MHz
- 84, 101, or 102 key keyboards
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS82C100 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- Additional AT-type BIOS interrupt functions
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- 82C606 Multifunction Controller

- Embedded SETUP program for machine configuration using CMOS RAM
- Dynamic memory sizing
- Setup of CHIPSet EMS registers

Complete BIOS Solution

The OC82C100+ BIOS is available in two forms to best meet the needs of the OEM. The SK82C100+ BIOS Software Kit provides a production-ready master copy of the system BIOS and utility programs to customize the BIOS. The SC82C100+ BIOS Source Kit provides the source code and documentation for the system BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications.

Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS82C100 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC82C100+	Enhanced SXT BIOS (Label)
CB82C100+	CS82C100 SXT CHIPSet with OC82C100+ BIOS (Label)
SK82C100+	Enhanced SXT BIOS Software Kit
SC82C100+	Enhanced SXT BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC8220 AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the CS8220 AT CHIPSet
- Includes Keyboard Controller BIOS
- Supports CPU speeds up to 12 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC8220 AT Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CS8220 AT CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80286 processor and 80287 math coprocessor operating at clock speeds from 6 MHz to 12 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS8220 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- 82C601, 82C604, and 82C605 Multifunction Controllers
- Embedded SETUP program for machine configuration
- Dynamic memory sizing

Complete BIOS Solution

The OC8220 BIOS is available in two forms to best meet the needs of the OEM. The SK8220 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS. The SC8220 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8220 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware products. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

Ordering Information

OC8220	AT BIOS (Label)
CB8220	CS8220 AT CHIPSet with OC8220 BIOS (Label)
CB8226	CS8226 AT CHIPSet with OC8220 BIOS (Label)
SK8220	AT BIOS Software Kit
SC8220	AT BIOS Source Kit

OC8221 NEAT™ AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the CS8221 NEAT CHIPSet
- Includes Keyboard Controller BIOS
- Supports 80286 or 80386SX processors
- Supports CPU speeds up to 25 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS' Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC8221 New Enhanced AT (NEAT) Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CS8221 NEAT CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80286 processor and 80287 math coprocessor operating at clock speeds from 6 MHz to 25 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS8221 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- Embedded SETUP program for machine configuration
- Moving BIOS to shadow RAM to improve performance
- Dynamic memory sizing

- Setup of CHIPSet EMS registers
- 80386SX processor and 80387SX math coprocessor
- 82C206 Integrated Peripheral Controller
- 82C601, 82C604, and 82C605 Multifunction Controllers

Complete BIOS Solution

The OC8221 BIOS is available in two forms to best meet the needs of the OEM. The SK8221 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS. The SC8221 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications.

CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8221 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8221	NEAT BIOS (Label)
CB8221	CS8221 NEAT CHIPSet with OC8221 BIOS (Label)
SK8221	NEAT BIOS Software Kit
SC8221	NEAT BIOS Source Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

DR8221 NEAT EMS DRIVER KIT

- **Optimized for the CS8221 NEAT CHIPSet**
- **Supports LIM 4.0 EMS Specification**

Overview

The DR8221 NEAT EMS Driver Kit provides driver software to support EMS based on the CS8221 NEAT and CS8281 NEATsx CHIPSets. The DR8221 software is designed to utilize the capability of the CHIPSet to operate according to the LIM (Lotus-Intel-Microsoft) 4.0 EMS Specification

The Driver's main job is to initialize the CHIPSet EMS registers to function according to the specified setup. Once the driver is installed, it acts as an interface between the system and the EMS hardware. It provides service function calls that allow an application to access the EMS memory.

The EMS Driver is capable of handling up to 8 megabytes of memory (limit of the CHIPSet). The EMS memory size must be setup either by the BIOS or a CHIPSet configuration program. The driver has options to select the base EMS I/O address, the page frame address, the maximum number of open processes, and enable an extensive memory diagnostic test during initialization.

Included on the diskette with the driver is documentation describing installation and usage of the EMS driver.

- **Total Hardware/Software Support**

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8221 CHIPSet with the DR8221 drivers and utilities. The CHIPSet together with the drivers and utilities have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

DR8221	NEAT EMS Driver/Utility Kit
DS8221	NEAT EMS Driver/Utility Source Kit

CHIPS' software products are obtained by an OEM through license agreement. A CHIPS' OEM Software License Agreement must be signed and returned before ordering a CHIPS' Driver/Utility product. This agreement entitles the OEM to reproduce and distribute one copy of the driver/utility software with each product containing the appropriate CHIPSet.

OC8223 LeAPset/LeAPset-sx AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for the CS8223 LeAPset and CS8283 LeAPset-sx
- Suspend/Resume Mode
- Sleep Mode and Smart Sleep Mode
- Clock Speed Selection
- Automatic Screen Blanking
- Pop-Up Laptop Set-Up Window and Embedded System Set-Up
- Includes AT Keyboard Controller BIOS
- Built-in Support for CHIPS' Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Built-In Development/Debug Support
- Total Hardware/Software Support

Overview

The OC8223 LeAPset/LeAPset-sx BIOS is an enhanced, high performance BIOS that is used with the CS8223 LeAPset or CS8283 LeAPset-sx to provide an integrated hardware and software solution for Laptop computers. The BIOS is fully compatible with the IBM AT BIOS, is optimized to utilize the extended capabilities of LeAPset and LeAPset-sx and provides several extended features, including Smart Sleep Mode. The BIOS is also designed to be easily customized by the OEM and to be easily used in the development/debug process.

BIOS Extensions

The Laptop features of LeAPset and LeAPset-sx supported by the BIOS include Suspend/Resume Mode, Sleep Mode, clock speed selection and automatic screen blanking. A pop-up window and hot-keys are provided for the user to set-up, enter and exit these modes.

Suspend/Resume Mode places the system in an ultra low power mode of operation that appears as if the system is turned off. Suspend is entered by turning power off, pressing a hot-key or by calling a BIOS function from an application. Resume to normal operation is performed by turning the power switch on.

Sleep Mode puts the system in a low power mode of operation that appears as if the sys-

tem is operating normally. Sleep Mode is entered automatically whenever the BIOS is idle, such as waiting for a key to be pressed, or when selected by the user. The system will wake up when the BIOS is no longer idle or when the user presses a key.

The screen is automatically blanked and shut off to conserve power after a user-specified time of keyboard inactivity. The time is specified by the user in the pop-up window.

The BIOS supports Smart Sleep Mode to allow a Laptop computer to operate with an even longer battery life. Smart Sleep Mode automatically detects when an application is idle and puts the system to sleep until the application is no longer idle.

The extended AT compatible features contained in the OC8223 BIOS include an embedded set-up, dynamic memory sizing, shadow RAM support, EMS register initialization and support for other CHIPS' multifunction controllers. The set-up capability allows the system configuration to be set up without the need for an external set-up program. Dynamic memory sizing automatically initializes the system for the type and amount of memory used. The Shadow RAM support feature moves the BIOS into RAM at the same location as the BIOS ROM to improve BIOS operation speed. The CHIPS' multifunction controllers supported by the BIOS include the 82C601, 82C605 and 82C710.

Complete BIOS Solution

The SK8223 BIOS Software Kit provides a production-ready master copy of the OC8223 BIOS, a production-ready master copy of the AT keyboard controller BIOS, and utility programs to customize the BIOS and to support the development/debug process. The SC8223 BIOS Source Kit provides the source code for the BIOS and keyboard controller BIOS and all of the contents of the SK8223.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program allows modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default Laptop and system set-up values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules by a source code OEM to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

CHIPS' system BIOS products are designed with built-in support to aid the development/debug process. The BIOS is designed to allow the CHIPSet registers to be loaded from battery backed-up memory on power-up. A utility program is provided to edit which registers are to be loaded and the values that are to be loaded.

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8223 LeAPset or CS8283 LeAPset-sx with OC8223 BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8223	LeAPset/LeAPset-sx BIOS (Label)
CB8223	CS8223 LeAPset with OC8223 BIOS (Label)
CB8283	CS8283 LeAPset-sx with OC8223 BIOS (Label)
SK8223	LeAPset/LeAPset-sx BIOS Software Kit
SC8223	LeAPset/LeAPset-sx BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

DR8223 LeAPset EMS DRIVER KIT

- **Optimized for the CS8223 LeAPset CHIPSet**

- **Supports LIM 4.0 EMS Specification**

Overview

The DR8223 LeAPSet EMS Driver Kit provides driver software to support EMS based on the CS8223, LeAPset and CS8283 LeAPset-sx CHIPSets. The DR8223 software is designed to utilize the capability of the CHIPSet to operate according to the LIM (Lotus-Intel-Microsoft) 4.0 EMS Specification.

The Driver's main job is to initialize the CHIPSet EMS registers to function according to the specified setup. Once the driver is installed, it acts as an interface between the system and the EMS hardware. It provides service function calls that allow an application to access the EMS memory.

The EMS Driver is capable of handling up to 8 megabytes of memory (limit of the CHIPSet). The EMS memory size must be setup either by the BIOS or a CHIPSet configuration program. The driver has options to select the base EMS I/O address, the page frame address, the maximum number of open processes, and enable an extensive memory diagnostic test during initialization.

Included on the diskette with the driver is documentation describing installation and usage of the EMS driver.

- **Total Hardware/Software Support**

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8223 CHIPSet with the DR8223 drivers and utilities. The CHIPSet together with the drivers and utilities have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

DR8223	LeAPset EMS Driver/Utility Kit
DS8223	LeAPset EMS Driver/Utility Source Kit

CHIPS' software products are obtained by an OEM through license agreement. An OEM Software License Agreement must be signed and returned before ordering a CHIPS' Driver/Utility product. This agreement entitles the OEM to reproduce and distribute one copy of the driver/utility software with each product containing the appropriate CHIPSet.

OC8230 AT/386 AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the CS8230 AT/386 CHIPSet
- Includes Keyboard Controller BIOS
- Supports CPU speeds up to 25 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC8230 AT/386 Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CS8230 AT/386 CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80386 processor and 80387 math coprocessor operating at clock speeds from 16 MHz to 25 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS8230 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- 32 bit memory operations
- 82C206 Integrated Peripheral Controller
- 82C601, 82C604, and 82C605 Multifunction Controllers
- Embedded SETUP program for machine configuration

- Moving BIOS to shadow RAM to improve performance
- Dynamic memory sizing

Complete BIOS Solution

The OC8230 BIOS is available in two forms to best meet the needs of the OEM. The SK8230 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS. The SC8230 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8230 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8230	AT/386 BIOS (Label)
CB8230	CS8230 AT/386 CHIPSet with OC8230 BIOS (Label)
SK8230	AT/386 BIOS Software Kit
SC8230	AT/386 BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC8231 AT/386-CACHE AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the CS8231 AT/386 CHIPSet
- Includes Keyboard Controller BIOS
- Supports CPU speeds up to 25 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC8231 AT/386-Cache Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CS8231 AT/386 CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80386 processor and 80387 math coprocessor operating at clock speeds from 16 MHz to 25 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS8231 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- 32 bit memory operations
- 82C206 Integrated Peripheral Controller
- 82C601, 82C604, and 82C605 Multifunction Controllers
- 82C307 Cache Controller Chip

- Embedded SETUP program for machine configuration
- Moving BIOS to shadow RAM to improve performance
- Dynamic memory sizing

Complete BIOS Solution

The OC8231 BIOS is available in two forms to best meet the needs of the OEM. The SK8231 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS. The SC8231 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort.

CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8231 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8231	AT/386-Cache BIOS (Label)
CB8231	CS8231 AT/386 CHIPSet with OC8231 BIOS (Label)
SK8231	AT/386-Cache BIOS Software Kit
SC8231	AT/386-Cache BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC8233 PEAKset/386 AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the CS8233 PEAKset/386 CHIPSet
- Includes Keyboard Controller BIOS
- Supports CPU speeds up to 40 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Built-In Development/Debug Support
- Total Hardware/Software Support

Overview

The OC8233 PEAKset/386 Basic Input/Output System (BIOS) is an enhanced, high performance product that is used with the CS8233 PEAKset/386 CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80386 processor and 80387 math coprocessor operating at clock speeds from 20 MHz to 40 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS8233 CHIPSet to provide the user with enhanced functionality and better performance. The BIOS is also designed to be customized by the OEM and to be easily used in the development/debug process. The additional functions include support for:

- 32 bit memory operations
- 82C206 Integrated Peripheral Controller
- 82C601, 82C604, and 82C605 Multifunction Controllers

- Setup and usage of cache options
- Embedded SETUP program for machine configuration
- Moving BIOS to shadow RAM to improve performance
- Dynamic memory sizing

Complete BIOS Solution

The OC8233 BIOS is available in two forms to best meet the needs of the OEM. The SK8233 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS and support the development/debug process.

The SC8233 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be in-

tegrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

CHIPS' system BIOS products are designed with built-in support to aid in the development/debug process. The BIOS is designed to allow the CHIPSet registers to be loaded from saved information during power-up. The registers and their values that will be loaded can be controlled by a program that is included in the software kit.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review upon request.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8233 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test

department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8233 PEAKset/386 BIOS (Label)

CB8233 CS8233 PEAKset/386 CHIPSet
with OC8233 BIOS (Label)

SK8233 PEAKset/386 BIOS Software Kit

SC8233 PEAKset/386 BIOS Source
Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC82C235 SCAT AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the 82C235 SCAT CHIPSet
- Includes Keyboard Controller BIOS
- Supports 80286 processor at speeds up to 16 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS Multifunction Controller
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Built-In Development/Debug Support
- Total Hardware/Software Support

Overview

The OC82C235 Single Chip AT (SCAT) Basic Input/Output System (BIOS) is an enhanced, high performance product that is used with the 82C235 SCAT CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80286 processor and 80287 math coprocessor operating at clock speeds from 8 MHz to 16 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the 82C235 CHIPSet to provide the user with enhanced functionality and better performance. The BIOS is also designed to be customized by the OEM and to be easily used in the development/debug process. The additional functions include support for:

- 82C601 Multifunction Controller with two serial ports, one parallel port, 16-Bit IDE hard disk interface, and floppy controller chip select

- Embedded SETUP program for machine configuration
- Moving BIOS to Shadow RAM to improve performance
- Dynamic memory sizing
- Setup of 82C235 EMS registers

Complete BIOS Solution

The OC82C235 BIOS is available in two forms to best meet the needs of the OEM. The SK82C235 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS and support the development/debug process. The SC82C235 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

CHIPS' system BIOS products are designed with built-in support to aid in the development/debug process. The BIOS is designed to allow the CHIPSet registers to be loaded from saved information during power-up. The registers and their values that will be loaded can be controlled by a program that is included in the software kit.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review upon request.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the

82C235 Single Chip AT with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC82C235	SCAT BIOS (Label)
CB82C235	82C235 SCAT CHIPSet with OC82C235 BIOS (Label)
SK82C235	SCAT BIOS Software Kit
SC82C235	SCAT BIOS Source Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

**DR82C235
SCAT EMS DRIVER KIT**

- **Optimized for the 82C235 SCAT CHIPSet**
- **Total Hardware/Software Support**
- **Supports LIM 4.0 EMS Specification**

Overview

The DR82C235 Single Chip AT (SCAT) EMS Driver Kit provides driver software to support EMS based on the 82C235 SCAT CHIPSet. The DR82C235 software is designed to utilize the capability of the Single Chip AT to operate according to the LIM (Lotus-Intel-Microsoft) 4.0 EMS Specification.

The Driver's main job is to initialize the 82C235 EMS registers to function according to the specified setup. Once the driver is installed, it acts as an interface between the system and the EMS hardware. It provides service function calls that allow an application to access the EMS memory.

The EMS Driver is capable of handling up to 16 megabytes of memory. The EMS memory size must be setup either by the BIOS or a CHIPSet configuration program. The driver has options to select the base EMS I/O address, the page frame address, the maximum number of open processes, and enable an extensive memory diagnostic test during initialization.

Included on the diskette with the driver is documentation describing installation and usage of the EMS driver.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the 82C235 Single Chip AT compatible CHIPSet with the DR82C235 drivers and utilities. The Single Chip AT compatible CHIPSet, together with the drivers and utilities, have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

DR82C235	SCAT EMS Driver/Utility Kit
DS82C235	SCAT EMS Driver/Utility Source Kit

CHIPS' software products are obtained by an OEM through license agreement. An OEM Software License Agreement must be signed and returned before ordering a CHIPS' Driver/Utility product. This agreement entitles the OEM to reproduce and distribute one copy of the driver/utility software with each product containing the appropriate CHIPSet.

OC82C451 82C451 VGA COMPATIBLE BIOS

- Fully Compatible with the IBM VGA BIOS
- Optimized for the 82C451 VGA Controller
- Extended Graphics and Text Modes
- High Performance 16-Bit CPU Interface Support
- Support for Backwards Compatible Emulation of EGA, CGA, MDA and Hercules Display Adapters
- Digital Monitor Support for Standard EGA, CGA and Monochrome Displays
- Complete BIOS Solution:
 - SK82C451 VGA BIOS Software Kit
 - SC82C451 VGA BIOS Source Code Kit
- Available in Display Adapter and Motherboard Versions
- Clean-Room Development Methodology
- Total Hardware/Software Support

Overview

The OC82C451 VGA BIOS is an enhanced, high performance BIOS that is used with the 82C451 VGA Controller to provide an integrated hardware and software VGA solution. The OC82C451 is fully compatible with the IBM VGA BIOS and is optimized to utilize the extended capability of the 82C451.

The OC82C451 provides all of the standard VGA features, including support for:

- 640 × 480 16 color graphics
- 80 × 25 text using a 9 × 16 character font
- VGA analog color and analog monochrome displays
- Up to 256 simultaneous colors from a palette of 256K
- 64 gray scale levels
- Automatic double scan of 200 line modes

BIOS Extensions

The OC82C451 utilizes the extended capability of the 82C451 to provide enhanced VGA functionality and performance. The BIOS supports three extended, higher resolution video modes that are implemented as extensions to the standard Set Video Mode function call. The extended video modes are:

- 800 × 600 16 color graphics
- 132 × 25 16 color text
- 132 × 50 16 color text

The inclusion of these video modes in the BIOS greatly simplifies creation of specialized

drivers required for software packages to operate in extended video resolutions.

The 82C451 supports the standard 8-bit CPU interface and an extended 16-bit CPU interface. The OC82C451 uses 16-bit I/O and memory operations wherever appropriate to increase performance in a 16-bit VGA implementation.

The 82C451 contains the capability to emulate EGA, CGA, MDA and Hercules display adapters. An extended function call is provided in the OC82C451 to select the desired display adapter emulation mode. All emulation modes are supported on VGA analog color and VGA analog monochrome displays.

The OC82C451 provides digital monitor support for EGA, CGA and monochrome displays. This allows emulation of EGA, CGA, MDA and Hercules display adapters on these standard displays (see Table).

OC82C451 Emulation Support

Video Mode	Displays			
	VGA	EGA	CGA	Monochrome
VGA	X			
EGA	X	X		
CGA	X	X	X	
MDA	X			X
Hercules	X			X

Complete BIOS Solution

The OC82C451 is part of the complete CHIPS' BIOS solution for the 82C451. CHIPS' BIOS products are designed to be customized to best meet OEM requirements. The SK82C451 VGA BIOS Software Kit provides a binary master copy of the BIOS and utility programs to customize the BIOS. A BIOS modification utility program, contained in the SK82C451, allows certain BIOS and chip parameters and the sign-on message to be configured by the OEM. The SK82C451 supports a VGA display adapter or motherboard with integrated VGA version of the BIOS.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. BIOS source code is available to an OEM to create their own modules or CHIPS can provide in-house customization services. The BIOS source code and documentation is available as part of the SC82C451 VGA BIOS Source Code Kit.

The OC82C451 was developed using a clean-room methodology that helps ensure that CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the 82C451 with the OC82C451 BIOS. The chip together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC82C451	VGA BIOS (Label)
CB82C451	82C451 with VGA BIOS (Label)
SK82C451	VGA BIOS Software Kit
SC82C451	VGA BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source code kit can then be ordered to obtain a master copy of the BIOS. For each order of the BIOS, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC82C452 82C452 SUPER VGA COMPATIBLE BIOS

- Fully Compatible with the IBM VGA BIOS
- Optimized for the 82C452 Super VGA Controller
- Extended Graphics and Text Modes
- High Performance 16-Bit CPU Interface Support
- Support for Backwards Compatible Emulation of EGA, CGA, MDA and Hercules Display Adapters

Overview

The OC82C452 VGA BIOS is an enhanced, high performance BIOS that is used with the 82C452 Super VGA Controller to provide an integrated hardware and software Super VGA solution. The OC82C452 is fully compatible with the IBM VGA BIOS and is optimized to utilize the extended capability of the 82C452.

The OC82C452 provides all of the standard VGA features, including support for:

- 640 × 480 16 color graphics
- 80 × 25 text using a 9 × 16 character font
- VGA analog color and analog monochrome displays
- Up to 256 simultaneous colors from a palette of 256K
- 64 gray scale levels
- Automatic double scan of 200 line modes

BIOS Extensions

The OC82C452 utilizes the extended capability of the 82C452 to provide enhanced VGA functionality and performance. The BIOS supports six extended, higher resolution video modes that are implemented as extensions to the standard Set Video Mode function call. The extended video modes are:

- 640 × 400 256 color graphics
- 640 × 480 256 color graphics
- 800 × 600 16 color graphics
- 1024 × 768 16 color graphics
- 132 × 25 16 color text
- 132 × 50 16 color text

- Digital Monitor Support for Standard EGA, CGA and Monochrome Displays
- Complete BIOS Solution:
 - SK82C452 VGA BIOS Software Kit
 - SC82C452 VGA BIOS Source Code Kit
- Available in Display Adapter and Motherboard Versions
- Clean-Room Development Methodology
- Total Hardware/Software Support

The inclusion of these video modes in the BIOS greatly simplifies creation of specialized drivers required for software packages to operate in extended video resolutions.

The 82C452 supports the standard 8-bit CPU interface and an extended 16-bit CPU interface. The OC82C452 uses 16-bit I/O and memory operations wherever appropriate to increase performance in a 16-bit VGA implementation.

The 82C452 contains the capability to emulate EGA, CGA, MDA and Hercules display adapters. An extended function call is provided in the OC82C452 to select the desired display adapter emulation mode. All emulation modes are supported on VGA analog color and VGA analog monochrome displays.

The OC82C452 provides digital monitor support for EGA, CGA and monochrome displays. This allows emulation of EGA, CGA, MDA and Hercules display adapters on these standard displays (see Table).

OC82C452 Emulation Support

Video Mode	Displays			
	VGA	EGA	CGA	Monochrome
VGA	X			
EGA	X	X		
CGA	X	X	X	
MDA	X			X
Hercules	X			X

Complete BIOS Solution

The OC82C452 is part of the complete CHIPS' BIOS solution for the 82C452. CHIPS' BIOS products are designed to be customized to best meet OEM requirements. The SK82C452 VGA BIOS Software Kit provides a binary master copy of the BIOS and utility programs to customize the BIOS. A BIOS modification utility program, contained in the SK82C452, allows certain BIOS and chip parameters and the sign-on message to be configured by the OEM. The SK82C452 supports a VGA display adapter or motherboard with integrated VGA version of the BIOS.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. BIOS source code is available to an OEM to create their own modules or CHIPS can provide in-house customization services. The BIOS source code and documentation is available as part of the SC82C452 VGA BIOS Source Code Kit.

The OC82C452 was developed using a clean-room methodology that helps ensure that CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the 82C452 with the OC82C452 BIOS. The chip together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC82C452	VGA BIOS (Label)
CB82C452	82C452 with VGA BIOS (Label)
SK82C452	VGA BIOS Software Kit
SC82C452	VGA BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source code kit can then be ordered to obtain a master copy of the BIOS. For each order of the BIOS, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC82C455 82C455 FLAT-PANEL VGA COMPATIBLE BIOS

- Fully Compatible with the IBM VGA BIOS
- Optimized for the 82C455 Flat-Panel VGA Controller
- Support for LCD, Plasma, EL and CRT Displays
- Support for Smartmap Automatic Contrast Enhancement
- Support for Automatic Vertical Compensation
- Digital Monitor Support for Standard EGA, CGA and Monochrome Displays
- Support for Backwards Compatible Emulation of EGA, CGA, MDA and Hercules Display Adapters
- High Performance 16-Bit CPU Interface Support
- Easy Customization of Key Flat-Panel Parameters
- Clean-Room Development Methodology
- Total Hardware/Software Support

Overview

The OC82C455 VGA BIOS is an enhanced, high performance BIOS that is used with the 82C455 Flat-Panel VGA Controller to provide an integrated hardware and software VGA solution intended for Laptop computers. The OC82C455 is fully compatible with the IBM VGA BIOS and is optimized to utilize the extended capability of the 82C455.

The OC82C455 provides the support necessary to allow VGA on flat-panel displays. VGA features supported include:

- 640 × 480 graphics resolution
- 80 × 25 text using a 9 × 16 character font
- Up to 64 colors
- Up to 16 gray scale levels
- Automatic double scan of 200 line modes
- In addition, the OC82C455 supports all of the standard VGA features on CRT displays.

BIOS Extensions

The OC82C455 utilizes the extended capability of the 82C455 to provide enhanced VGA functionality and performance. The OC82C455 supports use of LCD, Plasma, EL and CRT displays. The flat-panels supported can have resolutions of up to 720 × 480 and can be single or dual drive. The BIOS provides an extended function call to allow dynamic switching between a flat-panel display and a CRT.

The 82C455 provides the SMARTMAP intelligent color to gray scale mapping for text mode operations and automatic vertical compensation of lower resolution images to fill a larger flat-panel display. The OC82C455 supports these features with extended function calls.

The 82C455 contains the capability to emulate EGA, CGA, MDA and Hercules display adapters on flat-panel and CRT displays. An extended function call is used to select the desired display adapter emulation mode. A partial image will be displayed on flat-panels of lower resolution than used by the video mode selected. The OC82C455 provides an extended function call to support windowing within the image so that access to the entire image is possible.

OC82C455 Emulation Support

Video Mode	Flat-Panels*	CRTs	VGA	EGACGA	Mono-chrome
VGA	X	X			
EGA	X	X	X		
CGA	X	X	X	X	
MDA	X	X			X
Hercules	X	X			X

*Flat-Panels of lower resolution display a partial image.

The OC82C455 provides digital monitor support for EGA, CGA and monochrome displays. This allows emulation of EGA, CGA, MDA and Hercules display adapters on these standard displays (see Table).

The 82C455 supports the standard 8-bit CPU interface and an extended 16-bit CPU interface. The OC82C455 uses 16-bit I/O and memory operations wherever appropriate to increase performance in a 16-bit VGA implementation.

Complete BIOS Solution

The OC82C455 is part of the complete CHIPS' BIOS solution for the 82C455. CHIPS' BIOS products are designed to be customized to best meet OEM requirements. The SK82C455 VGA BIOS Software Kit provides a binary master copy of the BIOS and utility programs to customize the BIOS.

A BIOS modification utility program, contained in the SK82C455, allows certain BIOS and device parameters and the sign-on message to be configured by the OEM. This program is used to configure the BIOS to support the flat-panel display being used by the OEM. Flat-panel parameters easily customized include the display resolution and number of gray scales or colors supported. The program also supports integration of the OC82C455 into a system BIOS.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. BIOS source code is available to an OEM to create their own modules or CHIPS can provide in-house customization services. The

BIOS source code and documentation is available as part of the SC82C455 VGA BIOS Source Code Kit.

The OC82C455 was developed using a clean-room methodology that helps ensure that CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the 82C455 with the OC82C455 BIOS. The chip together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC82C455	VGA BIOS (Label)
CB82C455	82C455 with VGA BIOS (Label)
SK82C455	VGA BIOS Software Kit
SC82C455	VGA BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source code kit can then be ordered to obtain a master copy of the BIOS. For each order of the BIOS, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC8247 82C441 EGA COMPATIBLE BIOS

- Fully Compatible with the IBM EGA BIOS
- Optimized for the CS8245 EGA/VGA Controller CHIPSetm
- Extended VGA Compatible Graphics Modes
- Support for Backwards Compatible Emulation of CGA, MDA and Hercules Display Adapters
- Auto-Switching Between Emulation Modes
- Hercules Emulation on an EGA Display
- Double Scan of 200 Line Modes
- Complete BIOS Solution:
 - SK8247 EGA BIOS Software Kit
 - SC8247 EGA BIOS Source Code Kit
- Clean-Room Development Methodology
- Total Hardware/Software Support

Overview

The OC8247 EGA BIOS is an enhanced, high performance BIOS that is used with the CS8245 (82C441/82A442) EGA/VGA Controller CHIPSet to provide an integrated hardware and software EGA solution. The OC8247 is fully compatible with the IBM EGA BIOS and is optimized to utilize the extended capability of the CS8245 CHIPSet.

The OC8247 provides all of the standard EGA features, including support for:

- 640 × 350 16 color graphics
- 720 × 350 monochrome graphics
- 80 × 25 text using a 9 × 14 character font

BIOS Extensions

The OC8247 BIOS utilizes the extended capability of the CS8245 CHIPSet to provide enhanced EGA functionality and performance. The BIOS supports two of the standard VGA 640 × 480 graphics modes (11 and 12). This allows VGA software to run on an EGA display adapter based on the CS8245 and OC8247. The BIOS supports double scanning of all 200 line display modes.

The BIOS supports backwards compatible emulation of CGA, MDA and Hercules display adapters. In addition, the BIOS supports emulation of a Hercules monochrome display

adapter on an EGA color monitor. An emulation mode can be entered manually or automatically when an application begins running if auto-switching is enabled (see Table).

Auto-Switching supports automatic switching between EGA color modes and emulation of a CGA display adapter and switching between EGA monochrome modes and emulation of a MDA or Hercules display adapter. Auto-Switching doesn't support switching between color and monochrome display adapter emulation.

OC8247 Emulation Support

Video Mode	Displays		
	EGA	CGA	Monochrome
EGA	X		
CGA	X	X	
MDA			X
Hercules	X		X

Complete BIOS Solution

The OC8247 is part of the complete CHIPS' BIOS solution for the CS8245 CHIPSet. CHIPS' BIOS products are designed to be customized to best meet OEM requirements. The SK8247 EGA BIOS Software Kit provides a binary master copy of the BIOS and utility programs to customize the BIOS. A BIOS modification

utility program, contained in the SK8247, allows certain BIOS and CHIPSset parameters and the sign-on message to be configured by the OEM.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. BIOS source code is available to an OEM to create their own modules or CHIPS can provide in-house customization services. The BIOS source code and documentation is available as part of the SC8247 EGA BIOS Source Code Kit.

The OC8247 was developed using a clean-room methodology that helps ensure that CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CS8245 CHIPSset with the OC8247 BIOS. The CHIPSset together with the BIOS have been extensively

tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8247	EGA BIOS (Label)
CB8247	CS8245 CHIPSset with EGA BIOS (Label)
SK8247	EGA BIOS Software Kit
SC8247	EGA BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source code kit can then be ordered to obtain a master copy of the BIOS. For each order of the BIOS, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

OC8281 NEATsx AT COMPATIBLE BIOS

- Fully compatible with the IBM AT BIOS
- Optimized for performance with the CS8281 NEATsx CHIPSet
- Includes Keyboard Controller BIOS
- Supports 80386SX processor
- Supports CPU speeds up to 20 MHz
- SETUP embedded in BIOS
- Built-in support for CHIPS Multifunction Controllers
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Built-In Development/Debug Support
- Total Hardware/Software Support

The OC8281 New Enhanced AT Compatible (NEATsx) Basic Input/Output System (BIOS) is an enhanced, high performance product that is used with the CS8281 NEATsx CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM AT BIOS. It provides all of the standard features, including support for:

- 80386sx processor and 80387sx math coprocessor operating at clock speeds from 6 MHz to 20 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Monochrome and CGA video adapters
- Power-on self test diagnostics

BIOS Extensions

The BIOS utilizes the extended capabilities of the CS8281 CHIPSet to provide the user with enhanced functionality and better performance. The BIOS is also designed to be customized by the OEM and to be easily used in the development/debug process. The additional functions include support for:

- 82C206 Integrated Peripheral Controller
- 82C601, 82C604, and 82C605 Multifunction Controllers

- Embedded SETUP program for machine configuration
- Moving BIOS to shadow RAM to improve performance
- Dynamic memory sizing
- Setup of CHIPSet EMS registers

Complete BIOS Solution

The OC8281 BIOS is available in two forms to best meet the needs of the OEM. The SK8281 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS and support the development/debug process. The SC8281 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications.

Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

CHIPS' system BIOS products are designed with built-in support to aid in the development/debug process. The BIOS is designed to allow the CHIPSet registers to be loaded from saved information during power-up. The registers and their values that will be loaded can be controlled by a program that is included in the software kit.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS' offers complete hardware and software support for customers using the CS8281 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS

products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC8281 NEATsx BIOS (Label)

CB8281 CS8281 NEATsx CHIPSet with
OC8221 BIOS (Label)

SK8281 NEATsx BIOS Software Kit

SC8281 NEATsx BIOS Source Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

**OC/250
CHIPS/250 MODEL 50/60 COMPATIBLE BIOS**

- Fully compatible with the IBM PS/2 Model 50 and Model 60 BIOS including both CBIOS and A BIOS functionality
- Optimized for performance with the CHIPS/250 CHIPSet
- Includes Keyboard Controller BIOS
- Supports 80286 or 80386SX processors
- Supports CPU speeds up to 25 MHz
- Includes external setup and diagnostic utilities
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC/250 Basic Input/Output System (BIOS) is an optimized, high performance product that is used with CHIPS/250 CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM PS/2 Model 50 and Model 60 BIOS. It provides all of the standard features, including support for:

- 80286 processor and 80287 math coprocessor operating at clock speeds from 10 MHz to 25 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Built-in 82C451 or 82C452 VGA graphics
- Power-on self test diagnostics and Micro Channel™ setup
- External reference disk which contains CHIPS/250 configuration and system diagnostics utilities

BIOS Extensions

The BIOS utilizes the extended capabilities of the CHIPS/250 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- 80386SX processor and 80387SX math coprocessor

- Moving BIOS to shadow RAM to improve performance
- Dynamic memory sizing
- Setup of CHIPSet EMS registers

Complete BIOS Solution

The OC/250 BIOS is available in two forms to best meet the needs of the OEM. The SK/250 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS. The SC/250 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort.

CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the PS/250 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC/250	BIOS (Label)
CB/250	CHIPS/250 CHIPSet with OC/250 BIOS (Label)
SK/250	BIOS Software Kit
SC/250	BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

DR/250 CHIPS/250 EMS DRIVER KIT

- Optimized for the CHIPS/250 CHIPSet
- Supports LIM 4.0 EMS Specification

Overview

The DR/250 EMS Driver Kit provides driver software to support EMS based on the CHIPS/250 CHIPSet. The DR/250 software is designed to utilize the capability of the CHIPSet to operate according to the LIM (Lotus-Intel-Microsoft) 4.0 EMS Specification.

The Driver's main job is to initialize the CHIPSet EMS registers to function according to the specified setup. Once the driver is installed, it acts as an interface between the system and the EMS hardware. It provides service function calls that allow an application to access the EMS memory.

The EMS Driver is capable of handling up to 8 megabytes of memory (limit of the CHIPSet). The EMS memory size must be setup either by the BIOS or a CHIPSet configuration program. The driver has options to select the base EMS I/O address, the page frame address, the maximum number of open processes, and enable an extensive memory diagnostic test during initialization.

Included on the diskette with the driver is documentation describing installation and usage of the EMS driver.

- Total Hardware/Software Support

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CHIPS/250 CHIPSet with the DR/250 drivers and utilities. The CHIPSet together with the drivers and utilities have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

DR/250	CHIPS/250 EMS Driver/Utility Kit
DS/250	CHIPS/250 EMS Driver/Utility Source Kit

CHIPS' software products are obtained by an OEM through license agreement. An OEM Software License Agreement must be signed and returned before ordering a CHIPS' Driver/Utility product. This agreement entitles the OEM to reproduce and distribute one copy of the driver/utility software with each product containing the appropriate CHIPSet.

OC/280 CHIPS/280 MODEL 80 COMPATIBLE BIOS

- Fully compatible with the IBM PS/2 Model 80 BIOS including both CBIOS and A BIOS functionality
- Optimized for performance with the CHIPS/280 CHIPSet
- Includes Keyboard Controller BIOS
- Supports CPU speeds up to 25 MHz
- Includes external setup and diagnostic utilities
- Developed using Clean-Room Methodology
- Easy customization of key BIOS parameters
- Total Hardware/Software Support

Overview

The OC/280 Basic Input/Output System (BIOS) is an optimized, high performance product that is used with the CHIPS/280 CHIPSet to provide an integrated hardware and software solution. The BIOS is fully compatible with the IBM PS/2 Model 80 BIOS. It provides all of the standard features, including support for:

- 80386 processor and 80387 math coprocessor operating at clock speeds from 16 MHz to 25 MHz
- 84, 101, or 102 key keyboards
- High and low capacity 5.25-inch or 3.5-inch diskette drives
- Built-in 82C451 or 82C452 VGA graphics
- Power-on self test diagnostics and Micro Channel setup
- External reference disk which contains CHIPS/280 configuration and system diagnostics utilities

BIOS Extensions

The BIOS utilizes the extended capabilities of the CHIPS/280 CHIPSet to provide the user with enhanced functionality and better performance. The additional functions include support for:

- 32 bit memory operations

- Moving BIOS to shadow RAM to improve performance
- Setup of CHIPSet EMS registers

Complete BIOS Solution

The OC/280 BIOS is available in two forms to best meet the needs of the OEM. The SK/280 BIOS Software Kit provides a production-ready master copy of the system BIOS, a keyboard controller BIOS, and utility programs to customize the BIOS. The SC/280 BIOS Source Kit provides the source code and documentation for the system and Keyboard Controller BIOS, as well as all support utilities.

All CHIPS' BIOS products are designed to be customized to meet OEM requirements. A BIOS modification utility program is provided in both the software and source kit. It allows many common modifications of BIOS and CHIPSet configuration parameters, including the fixed disk table, the default CMOS values, and the sign-on message. This provides a method for an OEM to customize the BIOS without requiring access to the source code.

The consistent, modular structure of CHIPS' BIOS products allows creation of additional modules to support custom applications. Once a module is developed, it can be integrated into the BIOS with minimal effort. CHIPS also provides in-house customization services.

Clean Room Methodology

The BIOS was developed using a clean-room methodology that helps ensure CHIPS' BIOS products do not infringe on any applicable copyrights. The methodology used is well documented and is available for review.

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CHIPS/280 CHIPSet with the BIOS. The CHIPSet together with the BIOS have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests all CHIPS' BIOS products using industry standard software and hardware. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

OC/280	BIOS (Label)
CB/280	CHIPS/280 CHIPSet with OC/280 BIOS (Label)
SK/280	BIOS Software Kit
SC/280	BIOS Source Code Kit

CHIPS' BIOS products are licensed on a per copy royalty basis. A CHIPS' BIOS Object Code or Source Code license must be signed and returned before ordering a CHIPS' BIOS product. A software kit or source kit can then be ordered to obtain a master copy of the BIOS. For each BIOS ordered, the OEM receives an EPROM label and is entitled to make one copy of the BIOS from the master.

**DR/280
CHIPS/280 EMS DRIVER KIT**

- Optimized for the CHIPS/280 CHIPSet
- Supports LIM 4.0 EMS Specification

Overview

The DR/280 EMS Driver Kit provides driver software to support EMS based on the CHIPS/280 CHIPSet. The DR/280 software is designed to utilize the capability of the CHIPSet to operate according to the LIM (Lotus-Intel-Microsoft) 4.0 EMS Specification.

The Driver's main job is to initialize the CHIPSet EMS registers to function according to the specified setup. Once the driver is installed, it acts as an interface between the system and the EMS hardware. It provides service function calls that allow an application to access the EMS memory.

The EMS Driver is capable of handling up to 16 megabytes of memory (limit of the CHIPSet). The EMS memory size must be setup either by the BIOS or a CHIPSet configuration program. The driver has options to select the base EMS I/O address, the page frame address, the maximum number of open processes, and enable an extensive memory diagnostic test during initialization.

Included on the diskette with the driver is documentation describing installation and usage of the EMS driver.

- Total Hardware/Software Support

Total Hardware/Software Support

CHIPS offers complete hardware and software support for customers using the CHIPS/280 CHIPSet with the DR/280 drivers and utilities. The CHIPSet together with the drivers and utilities have been extensively tested for quality, reliability and compatibility. CHIPS has an in-house compatibility test department that tests CHIPS' products with industry standard hardware and software. CHIPS has a technical support staff available to assist in resolving any hardware or software problems that may arise.

Ordering Information

DR/280	CHIPS/280 EMS Driver/Utility Kit
DS/280	CHIPS/280 EMS Driver/Utility Source Kit

CHIPS' software products are obtained by an OEM through license agreement. An OEM Software License Agreement must be signed and returned before ordering a CHIPS' Driver/Utility product. This agreement entitles the OEM to reproduce and distribute one copy of the driver/utility software with each product containing the appropriate CHIPSet.

CHIPS

The background of the entire page is a textured, crumpled paper effect. Scattered across this background are several square microchips with pins along their edges, shown from a top-down perspective. The chips are arranged in a non-uniform pattern, with some appearing more prominent than others.

QUICK REFERENCE GUIDE
A GUIDE TO COMPLETE SYSTEM SOLUTIONS

This Product Quick Reference Guide provides a convenient look at Chips and Technologies' wide range of complete system solutions for entry level, mid-range, and high-performance applications. Chips also offers skilled technical, BIOS and customer support service for every complete system solution application.

For more detailed information on Chips' complete system solutions, mail in the attached order form or call the Chips and Technologies' representative in your area.

AT/XT CHIPSet SOLUTIONS

ENTRY-LEVEL SOLUTIONS

PROCESS SPEED

Systems Logic

82C100	Super XT System Controller	CMOS	10MHz
82C230	High Performance Model 30 Controller	CMOS	10,12,16MHz
82C235	Single Chip AT System Controller (SCAT)	CMOS	10,12,16MHz

CS8220

PC/AT-Compatible CHIPSet

10,12MHz

82C201	System Controller	CMOS	10,12MHz
82C202A	Memory Decoder & I/O Controller	CMOS	10,12MHz
82A203	High Address Buffer & Port B	Bipolar	10,12MHz
82A204	Low Address Buffer & Refresh Control	Bipolar	10,12MHz
82A205	Data Bus Buffer & Parity Generator	Bipolar	10,12MHz
82C206	Integrated Peripheral Controller	CMOS	12,16MHz

Graphics

82C435	Enhanced Graphics Controller	CMOS	30,38MHz
82C436	EGA Bus Interface	Bipolar	38MHz
CS8245	Super EGA/VGA CHIPSet		30,38MHz
82C451	Integrated VGA Controller	CMOS	40,50MHz

Communications

82C570	Single Chip "3270" Protocol Controller	CMOS	
82C578	Single Chip "3270" Terminal Controller	CMOS	
82C601	Single Chip Peripheral Controller	CMOS	
82C604A	CHIPSport II Multifunction Controller	CMOS	
82C605	CHIPSport Multifunction Controller	CMOS	
82C606	CHIPSpak Multifunction Controller	CMOS	

Mass Storage

82C710	Multifunction Floppy Controller	CMOS	
82C784	Data Separator & MFM/RLL Endec	CMOS	
82C785	Single Chip AT Hard Disk Controller	CMOS	
82C5055B	Hard Disk Formatter & Memory Controller	CMOS	
82C5059	Single Chip AT Hard Disk Controller	CMOS	
82C5080C	Asynch SCSI Interface Chip	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	
82C5090B	XT Interface Chip	CMOS	
82C5098	AT Interface Chip	CMOS	

AT/XT CHIPSet SOLUTIONS (Continued)

ENTRY-LEVEL SOLUTIONSPROCESS SPEED

BIOS & Drivers

OC8220	AT-Compatible BIOS
OC82C100	SXT XT-Compatible BIOS
OC82C100+	SXT Enhanced XT-Compatible BIOS
OC82C235	Single Chip AT System Controller (SCAT) BIOS
OC8241	82C435 EGA-Compatible BIOS
OC8247	82C441 EGA-Compatible ROM BIOS
OC82C451	82C451 VGA-Compatible ROM BIOS
DR82C100	Super XT EMS Driver
DR82C235	Single Chip-AT System Controller (SCAT) Driver

AT/XT CHIPSet SOLUTIONS (Continued)

MID-RANGE SOLUTIONS

		PROCESS	SPEED
Systems Logic			
82C206	Integrated Peripheral Controller	CMOS	12,16,20,25MHz
CS8221	NEAT New Enhanced PC/AT CHIPSet		12,16,20,25MHz
82C211	Bus Controller	CMOS	12,16,20,25MHz
82C212	Memory Interleave Controller	CMOS	12,16,20,25MHz
82C215	Data Bus Buffer & Transceiver	CMOS	12,16,20,25MHz
82C206	Integrated Peripheral Controller	CMOS	12,16,20,25MHz
82C631	EMS Mapper Chip (Optional)	CMOS	10,12,16,20,25MHz
CS8221A	NEAT New Enhanced PC/AT CHIPSet		12,16,20,25MHz
82C211	Bus Controller	CMOS	12,16,20,25MHz
82C212B	Memory Page/Interleave Controller	CMOS	12,16,20,25MHz
82C215	Data Bus Buffer & Transceiver	CMOS	12,16,20,25MHz
82C206	Integrated Peripheral Controller	CMOS	12,16,20,25MHz
82C631	EMS Mapper Chip (Optional)	CMOS	10,12,16,20,25MHz
CS8281	NEATsx CHIPSet	CMOS	16,20MHz
82C811	SX CPU Controller	CMOS	16,20MHz
82C812	SX Memory Controller	CMOS	16,20MHz
82C215	Address/Data Buffer	CMOS	16,20MHz
82C206	Integrated Peripheral Controller	CMOS	12,16,20,25MHz
82C631	EMS Mapper Chip	CMOS	10,12,16,20,25MHz
Graphics			
82C451	Integrated VGA Controller	CMOS	40,50MHz
82C452	Super VGA Controller	CMOS	50,65MHz
Communications			
82C570	Single Chip "3270" Protocol Controller	CMOS	
82C604	CHIPSport II Multifunction Controller	CMOS	
82C605	CHIPSport Multifunction Controller	CMOS	
82C606	CHIPSpak Multifunction Controller	CMOS	
Mass Storage			
82C710	Multifunction Floppy Controller	CMOS	
82C784	Data Separator & MFM/RLL Endec	CMOS	
82C785	Single Chip AT Hard Disk Controller	CMOS	
82C5055B	Hard Disk Formatter & Memory Controller	CMOS	
82C5059	Single Chip AT Hard Disk Controller	CMOS	
82C5080C	Asynch SCSI Interface Chip	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	
82C5090B	XT Interface Chip	CMOS	
82C5098	AT Interface Chip	CMOS	

AT/XT CHIPSet SOLUTIONS (Continued)**MID-RANGE SOLUTIONS**PROCESS SPEED

BIOS & Drivers

OC8221	NEAT AT-Compatible BIOS
OC8281	NEATsx AT-Compatible BIOS
OC82C451	82C451 VGA-Compatible BIOS
OC82C452	82C452 VGA-Compatible BIOS
DR8221	NEAT New Enhanced AT EMS Driver

AT/XT CHIPSet SOLUTIONS (Continued)

HIGH-END SOLUTIONS

PROCESS SPEED

Systems Logic

82C206	Integrated Peripheral Controller	CMOS	12,16,20,25MHz
CS8230/1/2	AT/386 CHIPSet		16,20,25MHz
82C301	Bus Controller	CMOS	16,20,25MHz
82C302	Memory Controller	CMOS	16,20,25MHz
82A303	Bipolar High Address Buffer	Bipolar	16,20,25MHz
82C303	CMOS High Address Buffer	CMOS	16,20,25MHz
82A304	Bipolar Low Address Buffer	Bipolar	16,20,25MHz
82C304	CMOS Low Address Buffer	CMOS	16,20,25MHz
82A305	Bipolar Data Buffer	Bipolar	16,20,25MHz
82B305	BiCMOS Data Buffer	BiCMOS	16,20,25MHz
82C305	CMOS Data Buffer	CMOS	16,20,25MHz
82C306	CMOS Control Signal Buffer	CMOS	16,20,25MHz
82C307	Cache Controller (Incl. w/CS8231)	CMOS	16,20,25MHz
CS8233	PEAKset/386 CHIPSet		16,20,25,33,40MHz
82C311	CPU/CACHE/DRAM Controller	CMOS	16,20,25,33,40MHz
82C315	Bus Controller	CMOS	16,20,25,33,40MHz
82C316	Peripheral Controller	CMOS	16,20,25,33,40MHz
CS8281	NEATsx CHIPSet	CMOS	16,20MHz
82C811	SX CPU Controller	CMOS	16,20MHz
82C812	SX Memory Controller	CMOS	16,20MHz
82C215	Address/Data Buffer	CMOS	16,20MHz
82C206	Integrated Peripheral Controller	CMOS	12,16,20,25MHz
82C631	EMS Mapper Chip (Optional)	CMOS	10,12,16,25MHz

Graphics

82C452	Super VGA Controller	CMOS	50,65MHz
82C480	8514/A-Compatible Controller	CMOS	
82B484	Video Support Chip	BiCMOS	

Communications

82C604	CHIPSport II Multifunction Controller	CMOS	
82C605	CHIPSport Multifunction Controller	CMOS	
82C606	CHIPSpak Multifunction Controller	CMOS	
82C570	Single Chip "3270" Protocol Controller	CMOS	

Mass Storage

82C785	Single Chip AT Hard Disk Controller	CMOS	
82C5055B	Hard Disk Formatter & Memory Controller	CMOS	
82C5059	Single Chip AT Hard Disk Controller	CMOS	
82C5080C	Asynch SCSI Interface Chip	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	
82C5090B	XT Interface Chip	CMOS	
82C5098	AT Interface Chip	CMOS	

AT/XT CHIPSet SOLUTIONS (Continued)**HIGH-END SOLUTIONS**PROCESS SPEED

BIOS & Drivers

OC8230	AT/386 AT-Compatible BIOS
OC8231	386 Cache AT-Compatible BIOS
OC8233	PEAKset/386 AT-Compatible BIOS
OC8281	NEATsx AT-Compatible BIOS
OC82C452	82C452 VGA-Compatible BIOS
DR8221	NEAT New Enhanced AT EMS Driver

PS/2 CHIPSet SOLUTIONS**ENTRY-LEVEL SOLUTIONS**PROCESS SPEED

Systems Logic

82C230	High Performance Model 30 Controller	CMOS	10,12,16MHz
82C235	Single Chip AT System Controller (SCAT)	CMOS	10,12,16MHz
CHIPS/250	IBM PS/2 Model 50/60-Compatible CHIPSet		
82C221	CPU Controller	CMOS	10,12,16,20MHz
82C222	Advanced Memory Controller	CMOS	10,12,16,20MHz
82C223	DMA Controller	CMOS	10,12,16,20MHz
82C225	Address/Data Buffer	CMOS	10,12,16,20MHz
82C226	System Peripheral Chip	CMOS	10,12,16,20MHz
82C631	EMS Mapper Chip	CMOS	10,12,16,20MHz
82C611	MicroCHIPS Micro Channel Interface	CMOS	
82C612	MicroCHIPS Micro Channel w/DMA	CMOS	
82C614	MicroCHIPS Bus Master	CMOS	

Graphics

82C451	Integrated VGA Controller	CMOS	40,50MHz
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Communications

82C570	Single Chip "3270" Protocol Controller	CMOS	
82C607	Multifunction Controller	CMOS	

Mass Storage

82C5055B	Hard Disk Formatter & Memory Controller	CMOS	
82C5080C	Async SCSI Interface Chip	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	

BIOS & Drivers

OC/250	CHIPS/250 Model 50/60 BIOS		
OC82C451	82C451 VGA-Compatible BIOS		
DR/250	CHIPS/250 EMS Driver		

PS/2 CHIPSet SOLUTIONS (Continued)**MID-RANGE SOLUTIONS**

PROCESS SPEED

Systems Logic**CHIPS/250****IBM PS/2 Model 50/60-Compatible CHIPSet**

82C221	CPU Controller	CMOS	10,12,16,20MHz
82C222	Advanced Memory Controller	CMOS	10,12,16,20MHz
82C223	DMA Controller	CMOS	10,12,16,20MHz
82C225	Address/Data Buffer	CMOS	10,12,16,20MHz
82C226	System Peripheral Chip	CMOS	10,12,16,20MHz
82C611	MicroCHIPS Micro Channel Interface	CMOS	
82C612	MicroCHIPS Micro Channel w/DMA	CMOS	
82C614	MicroCHIPS Bus Master	CMOS	
82C631	EMS Mapper Chip (Optional)	CMOS	10,12,16,20,25MHz

Graphics

82C451	Integrated VGA Controller	CMOS	40,50MHz
82C452	Super VGA Controller	CMOS	50,65MHz
82C480	8514/A-Compatible Controller	CMOS	
82B484	Video Support Chip	BiCMOS	

Communications

82C607	CHIPS/250/280 Multifunction Controller	CMOS	
82C570	Single Chip "3270" Protocol Controller	CMOS	
82C574	Micro Channel Interface Chip	CMOS	
82C575	Communication Micro Channel Interface	CMOS	

Mass Storage

82C780	Single Chip MCA Hard Disk Controller	CMOS	
82C781	Micro Channel Interface Chip	CMOS	
82C782	Fixed Disk Data Manager Chip	CMOS	
82C784	Data Separator & MFM/RLL Endec	CMOS	
82C5055B	Hard Disk Formatter & Memory Controller	CMOS	
82C5080C	Async SCSI Interface Chip	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	

BIOS & Drivers

OC/250	CHIPS/250 Model 50/60-Compatible BIOS		
OC82C451	82C451 VGA-Compatible BIOS		
OC82C452	82C452 VGA-Compatible BIOS		
DR/250	CHIPS/250 EMS Driver		

PS/2 CHIPSet SOLUTIONS (Continued)

HIGH-END SOLUTIONS

PROCESS SPEED

Systems Logic

CHIPS/280		IBM PS/2 Model 70/80-Compatible CHIPSet	
82C321	Micro Channel/80386 CPU Controller	CMOS	16,20,25MHz
82C322	Advanced Page/Interleave Memory Cont	CMOS	16,20,25MHz
82C325	Data/Buffer Controller	CMOS	16,20,25MHz
82C223	Advanced DMA Controller	CMOS	16,20,25MHz
82C226	System Peripheral Chip	CMOS	16,20,25MHz
82C327	32-Bit Integrated Cache/DRAM Controller	CMOS	16,20,25MHz
82C611	MicroCHIPS Micro Channel Interface	CMOS	
82C612	MicroCHIPS Micro Channel w/DMA	CMOS	
82C614	MicroCHIPS Bus Master	CMOS	

Graphics

82C452	Super VGA Controller	CMOS	50,65MHz
82C480	8514/A-Compatible Controller	CMOS	
82B484	Video Support Chip	BiCMOS	

Communications

82C607	CHIPS/250/280 Multifunction Controller	CMOS	
82C570	Single Chip "3270" Protocol Controller	CMOS	
82C574	Micro Channel Interface Chip	CMOS	
82C575	Communication Micro Channel Interface	CMOS	

Mass Storage

82C780	Single Chip MCA Hard Disk Controller	CMOS	
82C781	Micro Channel Interface Chip	CMOS	
82C782	Fixed Disk Data Manager Chip	CMOS	
82C784	Data Separator & MFM/RLL Endec	CMOS	
82C5055B	Hard Disk Formatter & Memory Controller	CMOS	
82C5080C	Async SCSI Interface Chip	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	

BIOS & Drivers

OC/280	CHIPS/280 Model 70/80-Compatible BIOS		
OC82C452	82C452 VGA-Compatible BIOS		
DR/280	CHIPS/280 EMS Driver		

LAPTOP CHIPSet SOLUTIONS

NOTEBOOK COMPUTER SOLUTIONSPROCESS SPEED

Systems Logic

82C100	Super XT-Compatible Controller	CMOS	10MHz
82C230	High Performance Model 30-Compatible Controller	CMOS	10,12,16MHz
82C631	EMS Mapper Chip (Optional)	CMOS	10,12,16,20,25MHz

Graphics

82C425	LCD/CRT Controller	CMOS	20MHz
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Communications

82C605	Multifunction Controller	CMOS	
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Mass Storage

82C5059	Single Chip AT Hard Disk Controller	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	

BIOS & Drivers

OC82C100	SXT XT-Compatible BIOS		
OC82C100+	SXT Enhanced XT-Compatible BIOS		
DR82C100	Super XT EMS Driver		
DR82C230	82C230 EMS Driver		

LAPTOP CHIPSet SOLUTIONS (Continued)

MID-RANGE SOLUTIONS

PROCESS SPEED

Systems Logic

<p>CS8223 82C241 82C242 82C206 82C636</p>	<p>LeAPset Low Power Enhanced AT Portable 286 CPU and Memory Controller Address/Data Buffer Integrated Peripheral Controller Power Control Unit</p>	<p>CMOS CMOS CMOS CMOS</p>	<p>12,16,20MHz 16,20MHz 16,20MHz 16,20MHz</p>
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Graphics

<p>82C425 82C455</p>	<p>LCD/CRT Controller VGA Flat Panel Controller</p>	<p>CMOS CMOS</p>	<p>20MHz 40MHz</p>
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Communications

<p>82C605</p>	<p>Multifunction Controller</p>	<p>CMOS</p>	
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Mass Storage

<p>82C710 82C784 82C785 82C5059 82C5086B</p>	<p>Multifunction Floppy Controller Data Separator & MFM/RLL Endec Single Chip AT Hard Disk Controller Single Chip AT Hard Disk Controller SCSI Protocol Controller (Async/Sync)</p>	<p>CMOS CMOS CMOS CMOS CMOS</p>	
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BIOS & Drivers

<p>OC8223 OC82C455 DR8223</p>	<p>LeAPset-sx AT-Compatible BIOS 82C455 Flat Panel VGA-Controller BIOS LeAPset-sx EMS Driver</p>		
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LAPTOP CHIPSet SOLUTIONS (Continued)**HIGH-END SOLUTIONS**PROCESS SPEED

Systems Logic

LeAPset-sx Low Power Enhanced SX AT Portable		PROCESS	SPEED
CS8283	SX CPU and Memory Controller	CMOS	16MHz
82C841	Address/Data Buffer	CMOS	16,20MHz
82C242	Integrated Peripheral Controller	CMOS	16,20MHz
82C206	Power Control Unit	CMOS	16,20MHz
82C636			

Graphics

82C455 VGA Flat Panel Controller

Communications

82C605 Multifunctional Controller CMOS

Mass Storage

82C710	Multifunction Floppy Controller	CMOS	
82C784	Data Separator & MFM/RLL Endec	CMOS	
82C785	Single Chip AT Hard Disk Controller	CMOS	
82C5059	Single Chip AT Hard Disk Controller	CMOS	
82C5086B	SCSI Protocol Controller (Async/Sync)	CMOS	

BIOS & Drivers

OC8223	LeAPset/LeAPset-sx AT-Compatible BIOS		
OC82C455	VGA Flat Panel Controller BIOS		
DR8223	LeAPset/LeAPset-sx Driver		



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CS8231	Turbo Cache-Based 386/AT CHIPSet	010231-002	<input type="checkbox"/>
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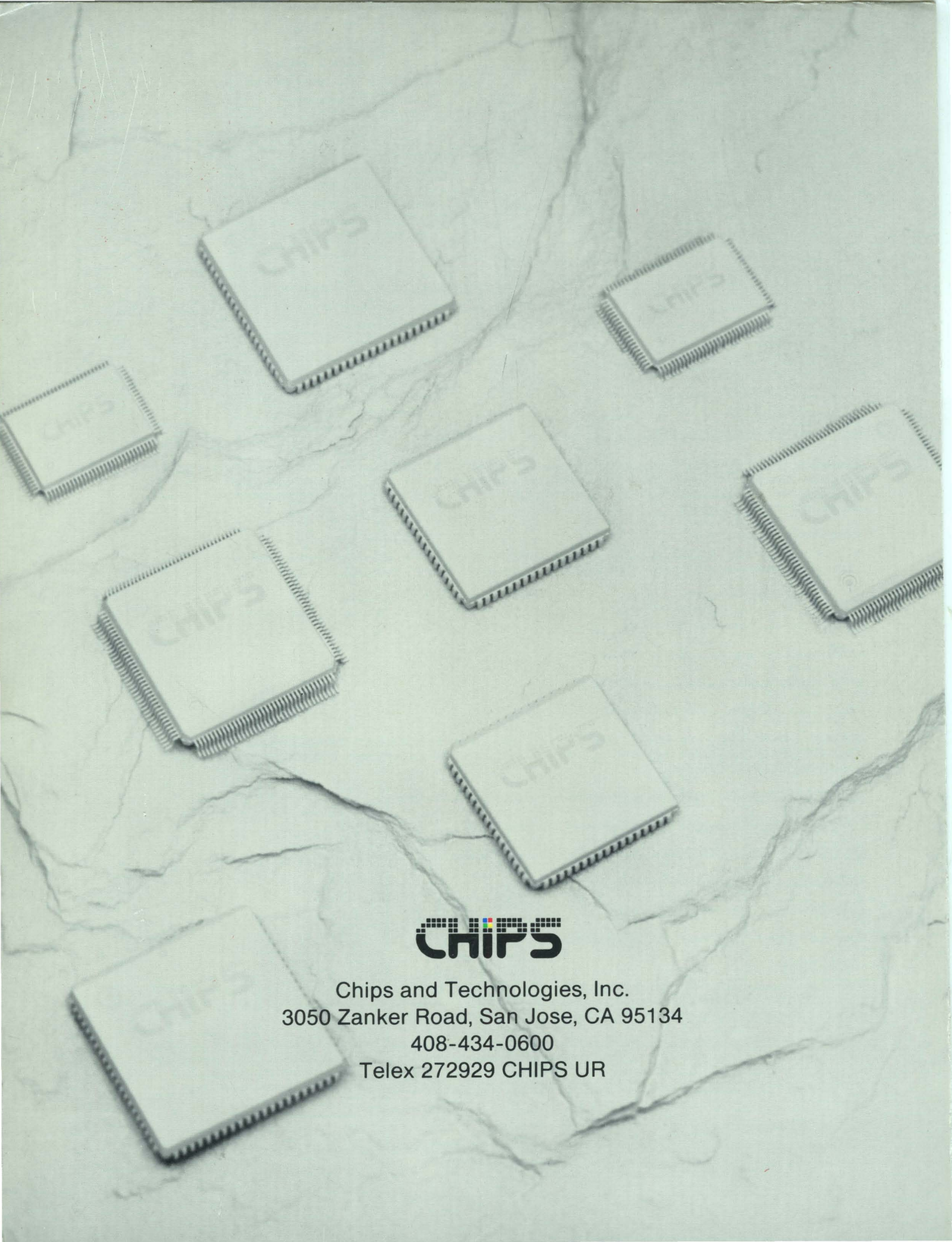
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