

82C451 CHIPS Integrated VGA

- Fully IBM™ VGA Compatible at hardware, register and BIOS level.
- Dual Bus Architecture. Integrated interface to PC-Bus and Microchannel (CHIPS/250 and CHIPS/280).
- Single Chip Solution.
- Proprietary High Speed Interface to CHIPS/250 and CHIPS/280 Systems.
- Supports 8 and 16 bit CPU interface for memory and I/O cycles.
- Supports external palette DAC of up to 16 million colors.
- Resolutions up to 640*480 in 16 colors, 960*720 in 4 colors and 1280*960 monochrome.
- Enhanced backward compatibility with EGA, CGA, Hercules™, MDA without using NMI.
- Processor Latches and Attribute Flip Flop are readable.
- Pinout Compatible with 82C452. Same design can use both parts.

CPU Interface

82C451 has a strap option to select a PC-Bus Interface or a Microchannel Interface. All control signals for both the interfaces are integrated into the single chip.

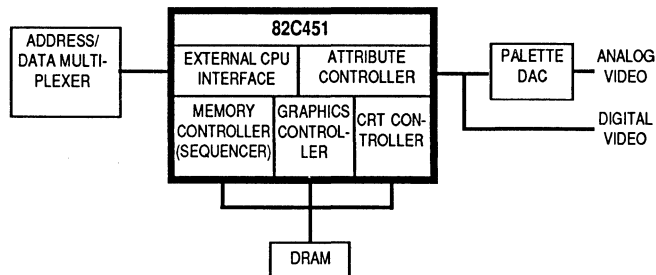
82C451 supports both a 8 bit and 16 bit CPU interface. The 16 bit interface can be independently enabled/disabled for memory and I/O cycles. On reset, the chip is configured for 8 bit accesses for memory and I/O cycles. 16 bit interface for I/O cycles is restricted to index/data pair of registers. This includes the Sequencer (3C4h), Graphics Controller (3CEh), CRT Controller (3B4h/3D4h) and the Attribute Controller (3C0h). All other I/O addresses (color palette, Misc Output and Status) are always treated as 8 bit ports.

If the 16 bit interface is chosen, then depending on the state of A0 and BHE, either a 8 bit or 16 bit cycle will actually be executed. This ensures compatibility with old software.

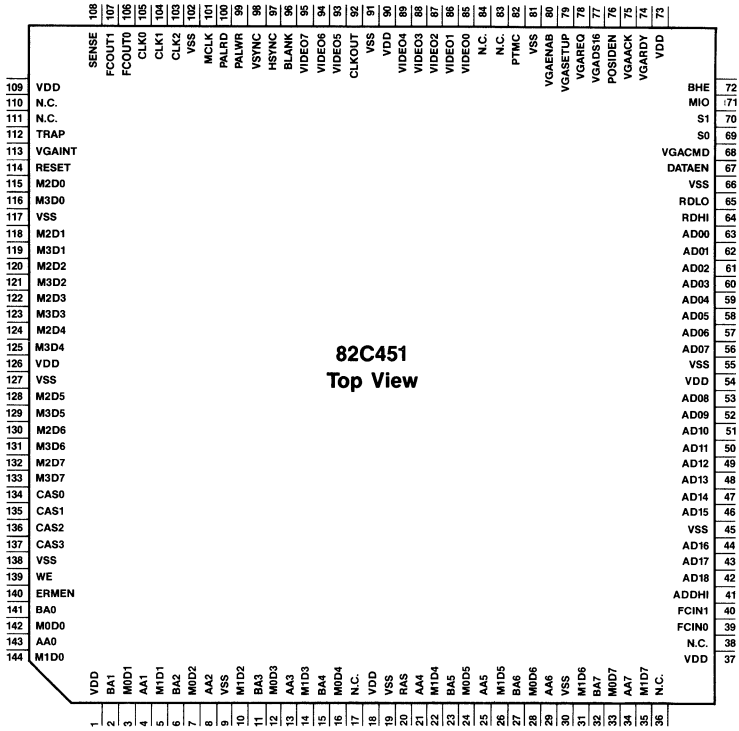
All I/O cycles are completed without wait states. For memory cycles, the cycles are extended with wait states.

BIOS ROM Interface

In the PC-BUS Interface, the 82C451 supports an external BIOS ROM. The ROM address is decoded and the ROMCS pin is asserted to enable ROM data on the CPU bus. In the Microchannel Interface, the system BIOS includes the video BIOS.



82C451 System Diagram



Display Modes and Resolution

82C451 supports a superset of all VGA display modes. It supports resolutions upto 640*480 in 16 colors, 960*720 in 4 colors and 1280*960 in monochrome.

Memory Interface

The entire display memory (256 Kbytes) is always available to the CPU in regular 4 plane mode, chained 2 plane mode and in super chained 1 plane mode.

The display memory control signals are derived from the dot clock. The MCLK is used for internal sequencing of 16 bit memory cycles. MCLK should be 25-40 MHz.

Extended Registers

All functionality of the extended registers in 82C451 are disabled on reset. Before the extended registers can be written into, they must be enabled by two sets of control bits (disabled on reset). The Processor Latches in the Graphics Controller and the Attribute Flipflop are readable in the extended register space. **No new bits are defined or any of the unused bits used in the regular VGA registers.**

External Palette Interface

82C451 supports programming of an external palette DAC by decoding the CPU addresses and generating the \overline{RD} and \overline{WR} signals to the external palette. 82C451 decodes I/O addresses 3C6-3C9h as valid external palette addresses.

High Speed CPU Interface

82C451 supports a high speed interface to CHIPS/250 and CHIPS/280 systems. There are special interface pins on the CHIPS/250, CHIPS/280 and 82C451. Using these special interface pins, CPU accesses to the 82C451 can be executed faster than CPU accesses to other peripheral devices.

The 82C451 is packaged in a 144 pin plastic flat pack (PFP).

Pin Description

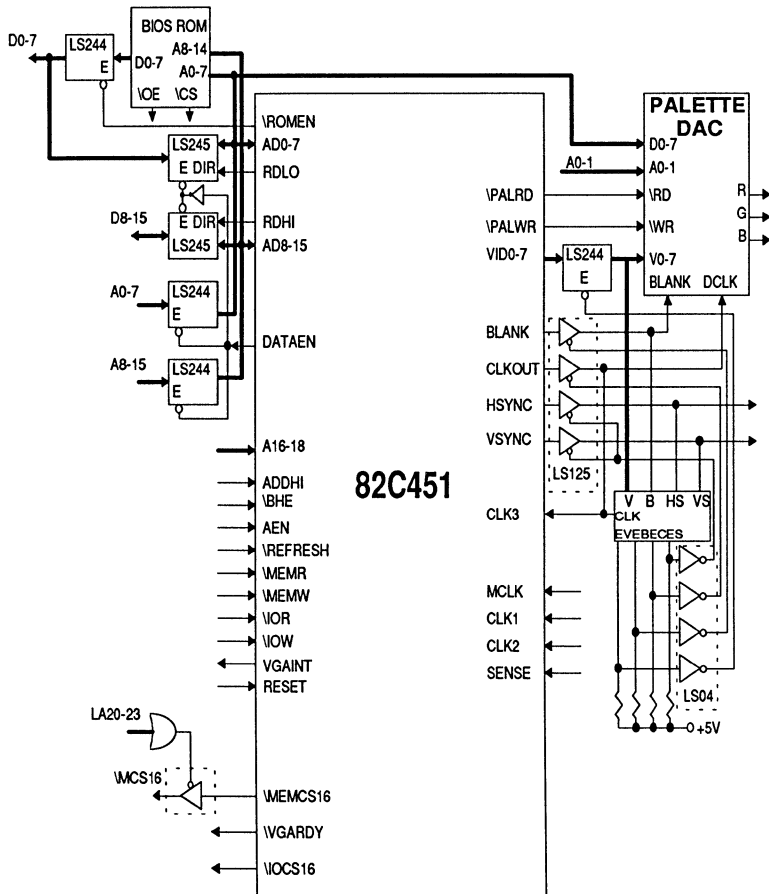
Pin Name	Type	Active	Description
AD0-15	I/O	High	Multiplexed address and Data bus. Addresses latched internally.
A16-18	I	High	High order address bus. Address latched internally.
BHE	I	Low	Byte High Enable bit. BHE low indicates that the high order byte at the current word address is being accessed. Latched internally.
ADDHI	O	High	Memory address enable. Defines that the current memory address is a valid address for 82C451. Ignored for I/O cycles.
RDLO, RDHI	O	Low	Controls direction of external Data Transceivers for the AD bus. 0: read from 82C451, 1: write into 82C451. Enable for the transceiver is externally generated off DATAEN.
DATAEN	O	Low	Controls multiplexing of external address/data multiplexers. 0: Enable address; 1: Enable Data.
M/IO	I	Both	Defined in Microchannel Interface only. Memory or IO cycle indicator signal.
AEN	I	High	Defined in PC-Bus Interface only. Indicates that the current IO cycle is a valid IO cycle.
S0	I	Low	Defined in Microchannel Interface only. Memory and IO Write signal.
MEMW	I	Low	Defined in PC-Bus Interface only. Memory Write signal.
S1	I	Low	Defined in Microchannel Interface only. Memory and IO Read signal.
MEMR	I	Low	Defined in PC-Bus Interface only. Memory Read signal.
VGACMD	I	Low	Defined in Microchannel Interface only. Indicates that the address should be latched and data bus enabled.
IOR	I	Low	Defined in PC-Bus Interface only. IO Read signal.
VGASETUP	I	Low	Defined in Microchannel Interface only. Puts 82C451 in setup mode.
IOW	I	Low	Defined in PC-Bus Interface only. IO Write signal.
VGAENAB	I	High	Defined in Microchannel Interface only. Enables memory and IO cycles.
REFRESH	I	Low	Defined in PC-Bus Interface only. Indicates that the current memory read cycle is actually a refresh cycle. 82C451 does not respond to a memory cycle when this pin is low.
VGADS16	O	Low	Defined in Microchannel Interface only. Signal indicating valid 16 bit memory or I/O cycle. Can be disabled through a register.

Pin Description (Continued)

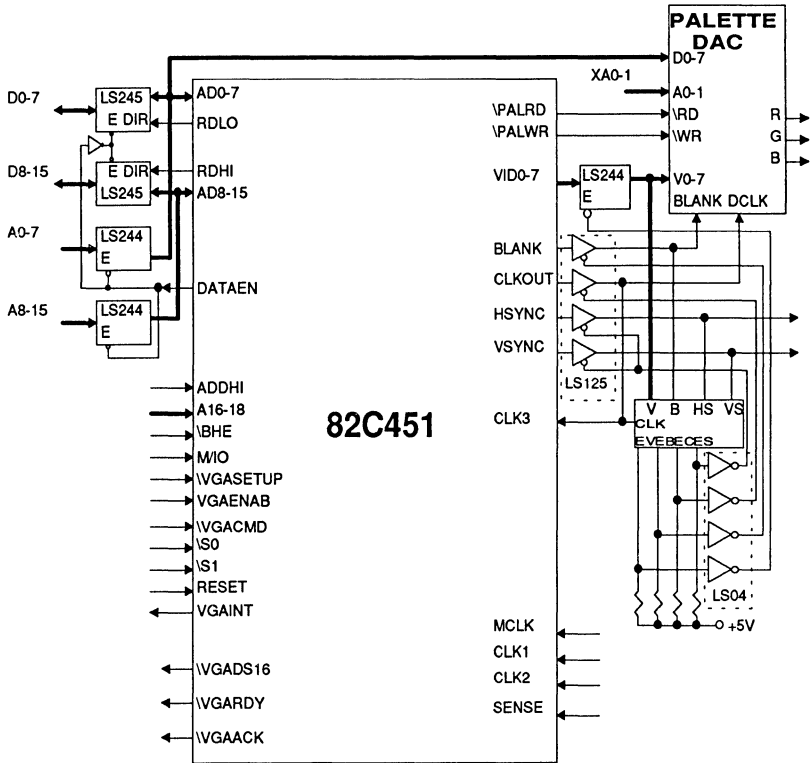
Pin Name	Type	Active	Description
MEMCS16	O	Low	Defined in PC-Bus Interface only. Signal indicating valid 16 bit memory cycle. Can be disabled through a register.
VGAREQ	O	Low	Defined in Microchannel Interface only. Indicates to CHIPS/250 and CHIPS/280 that the current CPU cycle to 82C451 can be completed faster than normal CPU cycles directed to peripheral devices.
IOCS16	O	Low	Defined in PC-Bus Interface only. Signal indicating valid 16 bit IO cycle. Can be disabled through a register.
VGAACK	O	Low	Defined in Microchannel Interface only. Indicates CPU access to display memory or registers.
RESET	I	High	Reset signal.
ROMCS	O	Low	Defined in PC-Bus Interface only. Low when ROM address is valid. Can be disabled through a register.
VGARDY	O	Low	Indicates that current cycle should be extended with wait states.
VGAINT	O	High	Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller.
CLK0-2	I	High	3 dot clocks. Selected through Misc Output Register (3C2h).
MCLK	I	High	Memory Clock. Used to generate display memory control signals. Can be used as display dot clock.
SENSE	I	High	Input pin read back to the CPU through Input Status Register 0 (3C2h). Can be used to detect type of monitor.
PALRD	O	Low	Connected to Read input of Palette DAC. Asserted when I/O Read at address 3C6-3C9h.
PALWR	O	Low	Connected to Write input of Palette DAC. Asserted when I/O Write at address 3C6-3C9h.
M0D0-7, M1D0-7 M2D0-7, M3D0-7	O	High	DRAM Data Bus A, B, C and D respectively.
AA0-7, BA0-7	O	High	DRAM address bus for planes 0, 1 and 2, 3 respectively.
RAS	O	Low	Row Address strobe for memory bank.
CAS0, CAS1 CAS2, CAS3	O	Low	Column Address strobes for memory planes 0, 1, 2 and 3 respectively.
WE	O	Low	Active Low. Write Enable for all memory banks/planes.
HSYNC, VSYNC	O	Both	Horizontal and Vertical sync signals for the monitor. Polarity is programmable.

Pin Description (Continued)

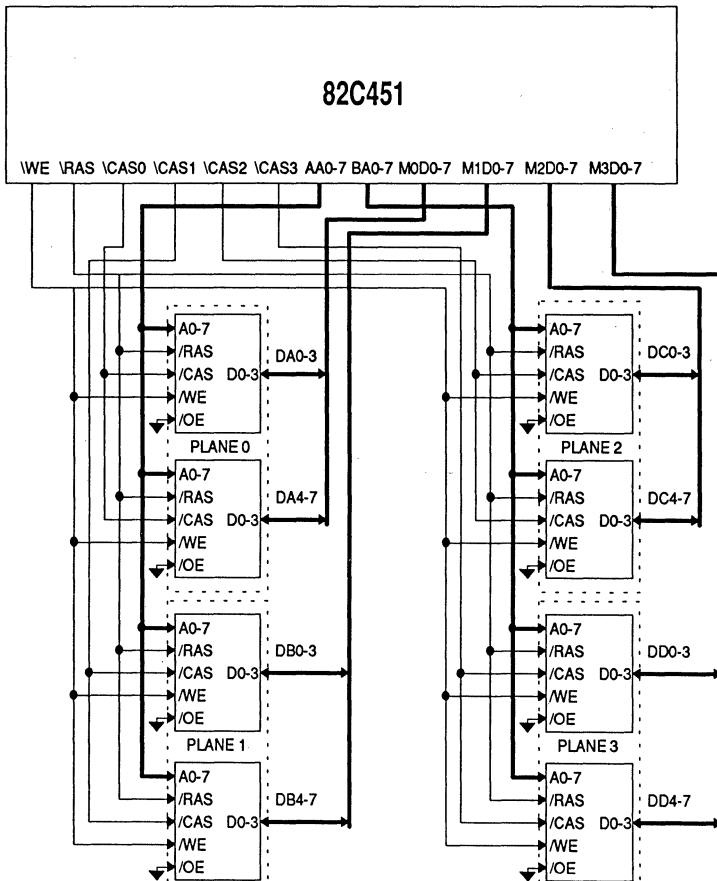
Pin Name	Type	Active	Description
BLANK	O	Both	Blanking signal for external palette DAC. Polarity is programmable. Can be redefined as the Display Enable signal.
VIDEO0-7	O	High	8 bit Video output.
CLKOUT	O	High	Output pixel clock. Video data synchronized to this clock.
PTMC	I	Both	Select Interface type. 0: Microchannel Interface selected. 1: PC-Bus Interface selected.



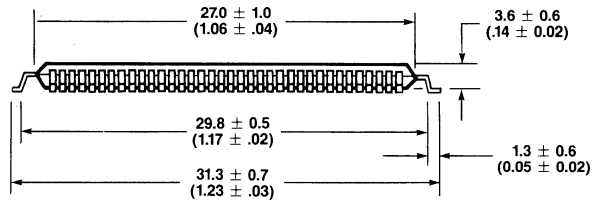
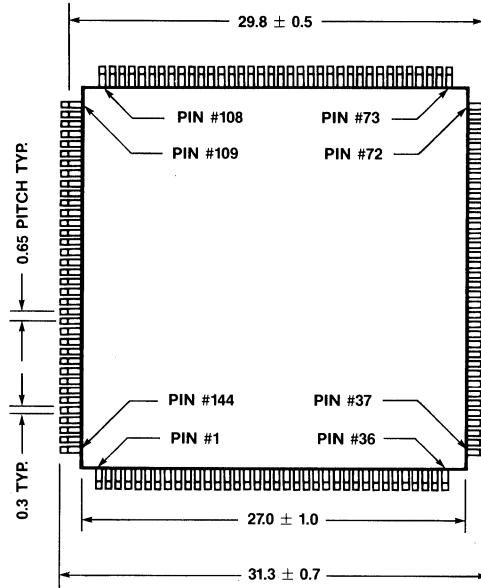
82C451 System Diagram—16 Bit PC-AT Bus Interface



82C451 System Diagram—16 Bit Microchannel Interface



Interfacing 82C451 to 256 Kbytes DRAM



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Phone: 313-478-8106

MINNESOTA

**High Technology Sales
Assoc.**
11415 Valley View Road
Eden Prairie, MN 55344
Phone: 612-944-7274

NEW JERSEY

T.A.I.
12 South Blackhorse Pike
Bellmawr, NJ 08031
Phone: NJ: 609-933-2600
PA: 215-627-6615

NEW MEXICO

Reptronix
237-C Eubank Blvd. NE
Albuquerque, NM 87123
Phone: 505-292-1718

NEW YORK

ERA, Incorporated
351 Veterans Memorial Hwy.
Commack, NY 11725
Phone: 516-543-0510

L-Mar Associates

349 W. Commercial St.
Suite 2285
Rochester, NY 14445
Phone: 716-381-9100

NORTH CAROLINA

The Novus Group, Inc.
5337 Trestlewood Lane
Raleigh, NC 27610
Phone: 919-833-7771

OHIO

Giesting & Associates
2854 Blue Rock Road
P. O. Box 39398
Cincinnati, OH 45239
Phone: 513-385-1105

Giesting & Associates
26250 Euclid Avenue
Suite 525
Cleveland, OH 44132
Phone: 216-261-9705

Giesting & Associates
8843 Washington Colony
Drive
Dayton, OH 45459
Phone: 513-433-5832

OREGON

L-Squared Limited
15234 NW Greenbrier Pkwy.
Beaverton, OR 97006
Phone: 503-629-8555

PENNSYLVANIA

Giesting & Associates
471 Walnut Street
Pittsburgh, PA 15238
Phone: 412-963-5832

TEXAS

OM Sales
13915 Burnet Road
Suite 301
Austin, TX 78728
Phone: 512-388-1151

Chips & Technologies, Inc.
15415 Katy Freeway
Suite 209
Houston, TX 77095
Phone: 713-579-9633

OM Sales

10500 Richmond Avenue
Suite 115
Houston, TX 77042
Phone: 713-789-4426

OM Sales

2323 N. Central Expwy.
Suite 150
Richardson, TX 76080
Phone: 214-690-6746

UTAH

Wescor Marketing, Inc.
3499 S. Main
Salt Lake City, UT 84114
Phone: 801-269-0419

WASHINGTON

L-Squared Limited
105 Central Way
Suite 203
Kirkland, WA 98033
Phone: 206-827-8555

WISCONSIN

Micro-Tex, Inc.
22660 Broadway
Suite 3B
Waukesha, WI 53186
Phone: 414-542-5352

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Chips and Technologies, Incorporated

3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR

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