# 82C5058 SINGLE CHIP SCSI DISK CONTROLLER

## Memory Controller Features

- Two Independent DMA Channels
- Up to 13 Megabyte Memory Bandwidth
- Addressing for 64K SRAM and up to 1 Megabyte DRAM
- Address Holding Registers for Non-Contiguous Sector Buffers

## Programmable Data Sequencer Features

- Programmable Disk Format Via Internal Register File
- Up to 20 Megabit Per Second NRZ Data Rate
- Direct Interface to ESDI Type Drives
- 32, 48, 56 Bit ECC Polynomial
- High Level Instruction Set
- No Real-Time Firmware Requirements

## SCSI Interface Features

- Internal Single-Ended Driver and Receiver
- Support for External Differential Driver/Receiver (Target Mode Only)
- Microprocessor Direct Control of Bus Signals
- Asynchronous DMA Data Transfer to Greater Than 3 Megabytes Per Second
- Synchronous DMA Data Transfer Up to 10 Megabytes Per Second (Target Mode Only)

## Total System Performance Features

- Latch Microprocessor Memory Address Bus
- Internal Oscillator Circuit to 40 Megahertz
- Flexible Interrupt Capability Throughout
- Advanced 1.5$\mu$ CMOS Low Power Technology
- 100-Pin Quad Flat Pack Packaging

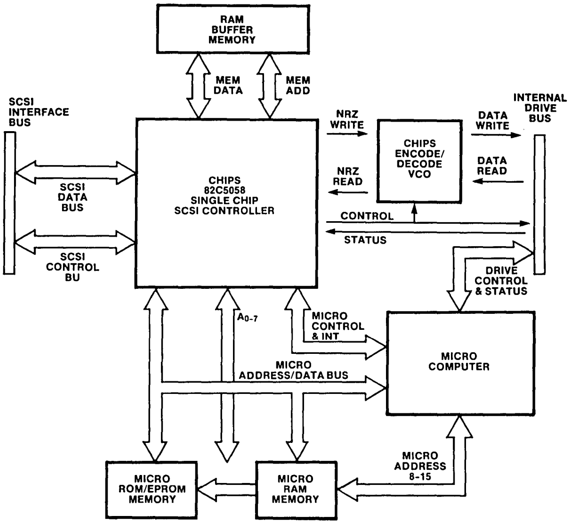
## Introduction

The 82C5058 Single Chip SCSI Controller is a highly integrated, CMOS, VLSI, Application Specific Integrated Circuit (ASIC) designed to be the primary component in a high-performance, intelligent, Winchester or floppy disk drive controller. It is designed to be an ideal solution for embedded intelligent disk controller applications. To design a complete embedded SCSI controller using the 82C5058, designers simply add a microcontroller with either a Z8 or 8051-type bus structure and the associated memory, 64 Kbytes of SRAM or up to 1 Megabyte of DRAM and a 10C5027 or 10C5070 data separator device or other ESDI devices.

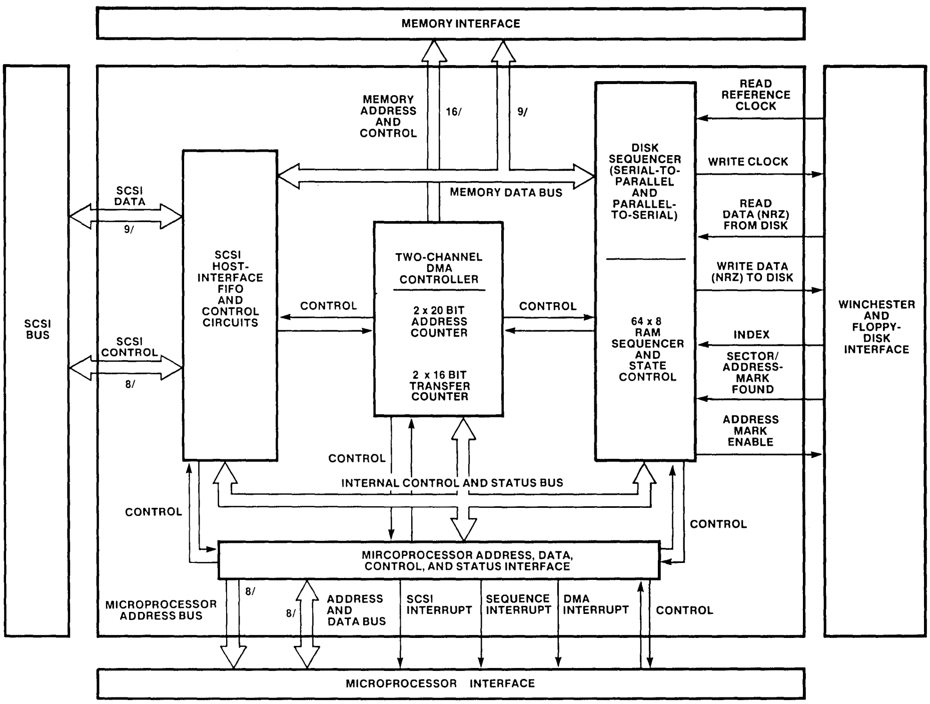
The total SCSI controller solution requires less board space than previous controller configurations with more performance added. The CHIPS solution has the advantage of backward compatibility with previous SCSI hardware and firmware for an easy-to-implement upgrade with reduced cost of previous controller configurations. CHIPS offers years of experience in controller firmware with our own disk drive controller design group to help you take full advantage of the highly programmable features of our SCSI chip set.

## Architectural Overview

The 82C5058 is an integrated memory controller, programmable data sequencer and synchronous/asynchronous SCSI interface controller device.The 82C5058 manages the flow of data for a serial peripheral, controls access to the external RAM buffer memory that is required for such transfers and allows a microprocessor to have full control of the SCSI bus. The 82C5058 is designed to be used with a microprocessor having either a Z8 or 8051-type bus structure.




## 82C5058 Functional Block Diagram




## 82C5058 Typical System Configuration

1. A DMA controller.
2. A data sequencer.
3. A SCSI interface controller.

The 82C5058 incorporates a dual-bus architecture, providing separate ports for microprocessor and memory buffer operations. With the goal of achieving the highest possible performance, this dual-bus structure is used so that disk data transfers can occur simultaneously with microprocessor operations.

In the DMA controller, Channel 0 is used for moving blocks of data between the data sequencer and the external buffer, while Channel 1 is used for moving blocks of data between the SCSI host interface and the buffer. (When the data sequencer is not using Channel 0, this channel can also be used to allow the microprocessor to access the RAM buffer). DMA controller operation is programmed by writing the DMA controller registers; while operation may be monitored by reading the DMA controller registers.

The programmable data sequencer provides format control, error detection, and serial/parallel (SERDES) conversion functions normally associated with disk controllers. It is designed to be used with NRZ (Non-Return to Zero) interfaces such as those used in the ESDI (Enhanced Small Device Interface) or any of the CHIPS family of encode/ decode VCO devices. Flexible operation of the sequencer is made possible by write registers that program its operation, while read registers allow the firmware to monitor operation. Additionally, complete flexibility in disk formatting is permitted by a 64-byte on-device format RAM, which is accessed through three of the data sequencer write registers.

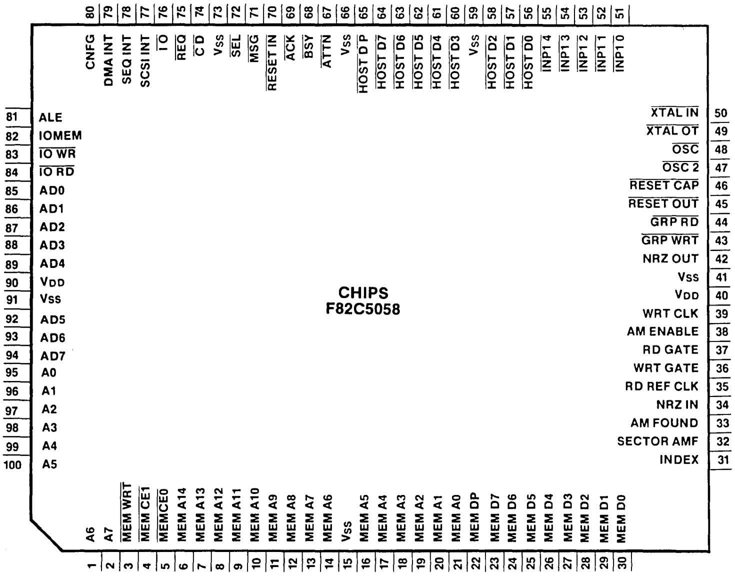
In addition to an external RAM buffer, a byte-oriented microprocessor such as the Z8 or 8051, with its associated memory, the 82C5058 may be connected with the 10C5070 Encode/ Decode/PLL for MFM encoding/ decoding up to 5 Mbits/sec or the 10C5027 Encode/ Decode/PLL for RLL 2,7 encoding/ decoding up to 10 Mbits/sec thus providing a total solution for an embedded SCSI interfacing disk drive.

## Ordering Information

The 82C5058 can be ordered using the following part number:

F82C5058 (100-pin QFP)

Evaluation samples available now. Production orders being accepted with standard lead-times.

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