DATA BOOK

VOL 2

CRYSTAL

Communications IC's

1990

CRYSTAL
Semiconductor Corporation

DATA BOOK VOL 2
COMMUNICATIONS IC's

MODEL INDEX

Crystal Semiconductor Corporation

Communications Data Book

LIFE SUPPORT AND NUCLEAR POLICY

CRYSTAL SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF CRYSTAL SEMICONDUCTOR.

Life Support Systems are equipment intended to support or sustain life and whose failure to perform when properly used in accordance with instructions provide can be reasonably expected to result in personal injury or death. Users contemplating applications of Crystal Semiconductor products in Life Support Systems are requested to contact Crystal Semiconductor factory headquarters to establish suitable terms and conditions for these applications. Crystal Semiconductor's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequiential damages.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (whether used for anasthesia, pain relief, or other purposes), autotransfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, pertoneal dialysis systems, neonatal ventilator incubators, ventilators for both adults and infants, aneshesia ventilators, and infusion pumps, as well as other devices designated as "critical" by the FDA. The above are examples only and are not intended to be conclusive or exclusive of any other life support device.

Examples of nuclear facility applications are applications in (a) a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabricating, alloying, storing, or disposal of fissionable material or waste products thereof.

Crystal Semiconductor brings the benefits of leadership, high quality, analog VLSI solutions to our customers.

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COMPANY INFORMATION

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

CSLXXXX - TPNNH/R

DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.
REVISION IS COVERED IN DATE CODE STAMP.
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING ,ALPHA ONLY A-COMMERCIAL HIGH-REL
B-MILITARY 883B REV. C PROCESSING

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2
NUMERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED ,ALPHA CHARACTER ONLY,NO NUMERICS

P = PLASTIC DIP	S = 0.3" SOIC
C = CERAMIC SIDEBRAZE	E= CERAMIC LCC
D = CERDIP	J= J-LEAD CERAMIC CHIP CARRIER
L = PLASTIC LEADED CHIP CARRIER,J LEAD	G= GULLWING CERAMIC CHIP CARRIER
U= UNPACKAGED DIE	

TEMPERATURE SPECIFICATION - REQUIRED,ALPHA CHARACTER ONLY
SIGNAL CONDITIONING/COMMUNICATION:
BLANK or C = 0 °C to 70 °C
I = -40 °C to 85 °C
M = -55 °C to 125 °C

TEMPERATURE/ACCURACY - REQUIRED,ALPHA CHARACTER ONLY
DATA ACQUISITION:

TEMPERATURE	ACCURACY		
	GOOD	BETTER	BEST
0 °C to 70 °C	J	K	L
-40 °C to 85 °C	A	B	C
-55 °C to 125 °C	S	T	U

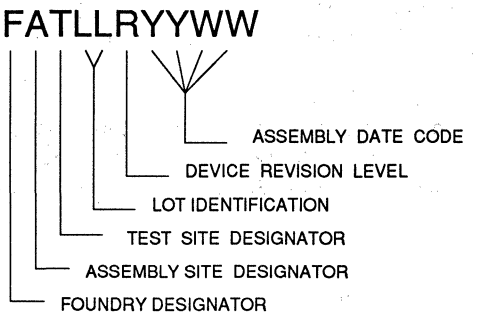
UP TO FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):
3 = DATA ACQ. SUPPORT CIRCUITS
4 = D/A CONVERTERS
5 = A/D CONVERTERS
6 = TELECOMMUNICATIONS
7 = SIGNAL CONDITIONING
8 = DATACOMMUNICATIONS

CRYSTAL SEMICONDUCTOR
"CS" = ALL CRYSTAL PRODUCTS;EXCEPT FOR
"CXT" = QUARTZ CRYSTALS
"CDB" = EVALUATION BOARD
"CX" = CUSTOM PRODUCTS

REV3

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



LOT CODE IDENTIFIER - TWO DIGIT ALPHA CHARACTER. IDENTIFIER SEQUENCE WILL BEGIN WITH AA,AB,AC, ETC. EACH LOT WILL RECEIVE A UNIQUE IDENTIFIER REGARDLESS OF DEVICE OR START DATE. SEQUENCE BEGINS AGAIN WITH AA WHEN ZZ HAS BEEN UTILIZED.

COMPANY BACKGROUND

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, a universal filter, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

QUALITY AND RELIABILITY INFORMATION

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This committment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability is an active concern of each Crystal employee.

In Product Definition

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

In Design

Conservative 3-micron CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART Analog product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883C, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch current.

Crystal SMART Analog design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. On-chip digital error correction provides stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer error sources to consider. The result is a less complicated, more reliable system.

In Fabrication and Assembly

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations (Japan and California today). Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and offshore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883C, Method 2010. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection to 3.0 percent LTPD is one of the standard production tests.)

In Test

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.

In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Table 1.)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited every six months and periodically monitored. Any major design or process changes restart the qualification procedure.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

TABLE 1 - QUALIFICATION TESTS

TEST	MIL STD 883C METHOD	CONDITION	INFANT MORTALITY TESTS		LONG-TERM RELIABILITY TESTS		
			DURATION	PASS/FAIL CRITERION	DURATION	PASS/FAIL CRITERION	CRYSTAL GOAL
OPERATING LIFE	1015 COND D	+125°C, Dynamic Bias +/-5.5V Supplies	168 hrs	0.25%	1000 HRS	75 FITS†† (25°C/60%UCL 1.0 eV Act. Energy)	10 FITS† (25° C/ 60% UCL)
TEMPERATURE HUMIDITY STRESS (Plastic Parts)		+85° C/85% RH Static Bias	168 hrs	1.0 LTPD	1000 HRS	3.0 LTPD	1.0 LTPD
TEMPERATURE CYCLING Hermetic Packages	1010.5 COND C	-65° C to + 150°C Then Gross Leak Test	100 CYCLES	1.0 LTPD	1000 CYCLES	3.0 LTPD	1.0 LTPD
TEMPERATURE CYCLING Molded Packages	1010.5 COND B or *	-55°C to + 125°C or -40°C to + 125°C	100 CYCLES	1.0 LTPD	500 CYCLES	3.0 LTPD	1.0 LTPD
THERMAL SHOCK	1011.4 COND B or **	-55°C to + 125°C or -40°C to + 125°C *** Then Gross Leak Test	100 CYCLES	1.0 LTPD	500 CYCLES	3.0 LTPD	1.0 LTPD
AUTOCLAVE (Plastic Parts)		+121°C/100% RH 2 Atmosphere, No Bias	48 HRS	1.0 LTPD	144 HRS	3.0 LTPD	1.0 LTPD
CENTRIFUGE	2001	30 Kg/Y1 Axis				5.0 LTPD	1.0 LTPD
ELECTROSTATIC DISCHARGE	3015			1500V-0 Fail	5 UNITS, ALL PINS	1500V-0 FAIL	4000V
LATCH UP		dc Current		100 mA-0Fail	5 UNITS, ALL PINS	100mA-0 FAIL	200mA

* JEDEC STD 22-B, A104 COND B
** JEDEC STD 22-B, A106 COND C
*** For hermetic Packages Only
† Equivalent to 50 FITS, 70°C/60% UCL, 0.7 eV
†† Equivalent to 300 FITS, 70°C/60% UCL, 0.7 eV

In Customer Service

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass"(Crystal On-line Marketing Production and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semiannual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow, training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883C, METHOD 2010. Test die are electrically tested to verify compliance to key process parameters based upon design rules specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until corrective action is agreed upon. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

• Notes •

INTRODUCTION

Using SMART *Analog*™ technology, Crystal Semiconductor has created a wide range of IC's for data aquisition applications. All feature on-chip self-calibration and are manufactured in low-power CMOS. This chapter contains cover pages for the data sheets describing these products. Complete data sheets are provided in the Crystal A/D Conversion Data Book (DADB3.0). Given below are brief, introductory descriptions of these data acquistion products. They have been grouped into the following categories: **Analog to Digital Converters, Digital to Analog Converters, Track and Hold Amplifiers, Voltage References, Switched Capacitor Filter and AES/EBU Transmitters & Receivers.**

ANALOG TO DIGITAL CONVERTERS

CS5012A, CS5014, CS5016 SAR Family

The CS5012A, CS5014 and CS5016 converters have 12, 14 & 16 bits of resolution, with conversion times of 7 µs to 16 µs. The converters are tested both for static and dynamic performance, at full rated conversion speed. On-chip self-calibration ensures that linearity, offset and full-scale errors remain within spec., with no missing codes.

CS5101 16-bit 100 kHz ADC

Derived from the CS5016, the CS5101 is a 16-bit ADC capable of converting in 8 µs, yielding sample rates of 100 kHz. A 2-channel analog input mux. is included. Output data is available serially, with 4 interface modes. An on-chip crystal oscillator is provided, along with a power-down control.

CS5102 16-bit, 20 kHz Low Power ADC

The CS5102 is a low power version of the CS5101. Requiring only 44 mW from ±5V supplies, along with a 1 mW power down mode, the CS5102 is ideal for battery powered applications. The part also features the same high speed serial interface as the CS5101.

CS5412 12-bit, 1 MHz ADC

Using a 2-step flash approach, the CS5412 achieves 12-bit performance at 1MHz sample rate. Self calibration insures accuracy over time and the military temperature range. Available in both DIP and J-lead LCC packages, with on-chip S/H, the IC offers a very compact ADC solution.

CS5317 16-bit Voice Band ADC

The CS5317 is well suited for a wide range of voiceband applications, from speech recognition to passive sonar. An on-chip PLL/Clock generator makes the part perfect for high-performance modems. The device features a 20 kHz word rate, a 10 kHz bandwidth, 84 dB dynamic range and 80 dB THD. CMOS design keeps power consumption to 280 mW.

CS5126 Audio A/D Converter

The CS5126 2-channel ADC is ideal for digital audio applications. An on-chip sample and hold is included, and sampling rates can be up to 100 kHz for 2X oversampling, yielding a dynamic range of 95 dB. Signal to noise plus distortion is 92 dB and self-calibration insures excellent low-level distortion characteristics.

CS5326,7,8,9 and CS5336,7,8,9 Delta Sigma Audio A/D Converters

This new class of device features 64X oversampling using a delta sigma architecture, with resolutions of 16 or 18-bits. Output word rates can be from 1kHz to 50kHz. These stereo parts have 2 sample and holds, dual delta sigma modulators, two anti-aliasing and decimation filters, and a voltage reference, all in a 28-pin package. Performance measures include 95 dB dynamic range in stereo mode, up to 100 dB in mono mode, along with 0.0015% THD.

CS5501/3 16/20-bit DC Measurement ADC

The CS5501/3 feature an on-chip 6-pole low pass filter with adjustable corner frequencies from 0.1 Hz to 10 Hz. The parts achieve linearity errors of 0.0007%, with no missing codes. A highly flexible serial interface, along with 25 mW power consumption, all in a 20 pin package, make the parts ideal for weigh scale and process control applications. The CS5503 is the 20-bit version of the CS5501, offering increased dynamic range, often removing the need for external gain scaling.

CS5505 4-Channel, 16-bit, DC Measurement ADC

Very low power consumption of 2 mW, along with the 4 channel input mux, make this part ideal for process control applications.

CS5322, CS5323, CS5324 24-bit Variable Bandwidth ADC

The CS5323 modulator, combined with the CS5322 digital filter, offers >120 dB dynamic range in the DC to 500 Hz frequency band. Eight different filter corner frequencies and output update rates are offered, allowing the ADC to be optimized for different types of seismic measurements. The CS5324 includes a modulator and the first stage of digital filtering, allowing the user to implement their own final filter stage.

CS7820 8-bit 1.4 µs ADC

The CS7820 8-bit sampling A/D has an inherent track-and-hold input, along with a 1.4 µs conversion time and easy interfacing to microprocessors.

Specifications	CS5012A/14/16	CS5101/2	CS5126	CS5317	CS5322/3 CS5324	CS5326/7 CS5328/9 CS5336/7 CS5338/9	CS5412	CS5501/3	CS5505	CS7820
Application	GP	GP	Audio	Modem	Seismic	Audio	GP Fast	DC Measurement		GP
Resolution (bits)	12/14/16	16	16	16	24	16/18	12	16/20	16	8
Conversion Time (us)	7/14/16	8/40	8	-	-	-	1.25	-	-	1.4
Throughput (kHz)	100/56/50	100/20	100	20	-	50	1 MHz	4	20Hz	-
Number of Inputs	1	2	2	1	1	2	1	1	4	1
Input Bandwidth	-	-	24 kHz	10 kHz	500 Hz	22/20 kHz	4 MHz	10Hz	10 Hz	-
Integral Non-Linearity	.006/.002/.001 %	.0015%	-	-	-	-	.01 %	.0007/.003 %	.001 %	.2%
Differential (± LSB) Non-Linearity	0.25/0.25/NMC	NMC	NMC	NMC	NMC	NMC	0.9	0.125/NMC	0.125	NMC
No Missing Codes	12/14/16	16	16	16	20	16/18	12	16/20	16	8
Total Harmonic Distortion (%)	.008/.003/.001	.001	.001	.007	.0003	.0015	.02	-	-	-
Signal-to-Noise plus Distortion (dB)	73/83/92	92	92	80	-	92	70	-	-	-
Dynamic Range (dB)	73/83/92	92	92	84	120	95/100*	70	-	-	-
Power Needed (mW)	120	280/44	280	220	150	450/400	750	25	2	40
Conversion Method	Succ. Approx.	Succ. Approx.	Succ. Approx.	Delta Sigma	Delta Sigma	Delta Sigma	2-Step Flash	Delta Sigma	Delta Sigma	2-Step Flash
Power Down Mode		√	√		√	√		√	√	
On-Chip Sample and Hold	√	√	√	√	√	√	√	√	√	√
On-Chip V. Ref				√		√			√	
On-Chip Filtering				√	√	√		√	√	
Statically Tested	√	√					√	√	√	√
Dynamically Tested	√	√	√	√	√	√	√			
Temperature Range	Com Ind Mil	Com Ind Mil	Com	Com Ind Mil	Com Ind	Com	Com Ind Mil	Com Ind Mil	Com Ind	Com Ind Mil
Number of Pins (DIP)	40	28	28	18	28	28	40	20	20	20
Packages	DIP PLCC LCC	DIP PLCC LCC	DIP PLCC	DIP SOIC	DIP PLCC	DIP SOIC	DIP CLCC	DIP SOIC	DIP SOIC	DIP

NMC=No Missing Codes * CS5328 In Mono Mode GP=General Purpose

DIGITAL TO ANALOG CONVERTERS

Crystal offers the digital audio industry a quantum improvement in digital-to-analog system integration, along with cost-effective performance enhancement. The CS4328 is industry's first complete stereo digital-to-analog output system. This 18-bit stereo D/A converter uses Crystal's well established oversampling A/D converter techniques.

The CS4328 includes the major system elements of 8X interpolation filter, 64X oversampling 18-bit D/A converter and a 95 dB dynamic range analog anti-imaging filter, all in one packaged, tested, solution. As with our A/D converters, the device features patented delta sigma architectures to maintain excellent distortion performance, even at low signal levels. The output anti-imaging filters are the first to be based on a mixed linear/switched capacitor architecture. This allows the benefit of bandwidth scaling proportionally to the system master clock, while retaining the low noise performance of linear filters. The CS4328 is therefore adjustable for both audio and voice band applications. The flexible digital interface mates with CD player circuitry, DAT recorders, DSP's or winchester disk drives.

TRACK & HOLD

As the industry's first monlithic 4-channel track-and-hold amplifier, the CS31412 frees-up board space and reduces system costs normally associated with sampling and multiplexing analog signals for conversion. The CS31412 takes a snapshot of four single-ended or two differential signals and stores the analog values in on-chip hold capacitors. An on-chip digital correction scheme calibrates all dc and dynamic errors, including hold pedestals, to less than 4 mV. Channel selection and calibration can be placed under software control using the microprocessor interface. Since the CS31412 can calibrate at any time or temperature, it ensures accuracy throughout its operating life.

The CS31412's fast 800 ns acquisition time and 12-bit accuracy make it ideal for processing high-frequency signals. In applications where fast sampling is not critical, the CS31412's 0.007 mV/ ms droop in the hold mode allows slower conversion of the channels without loss of accuracy. The CS31412 dissipates only 250 mW of power.

A complete single-channel track-and-hold, the CS3112, is also available. On-chip hold capacitors and calibration logic simplify use, and keep all dc and dynamic errors, including pedestal error, below 3.0 mV. This accuracy is ensured over time and temperature by easy user control of the calibration circuitry.

VOLTAGE REFERENCES

Crystal offers two voltage references which complement our A/D converters. Designed to operate with the CS5412 12-bit 1MHz ADC, the CS3901 produces a stable, buffered ±1.5V and +3.0V. Particularly suitable for Crystal's successive approximation A/D converters, the CS3902 produces a very stable and accurate +4.5V.

SWITCHED CAPACITOR FILTER

Ideal for adaptive filtering applications, the CS7008 digitally programmable switched capacitor filter provides the user with complete software control over the filter response.

Virtually any audioband filter response of eighth order or below is obtained by writing digital configuration coefficients to on-chip registers through a standard microprocessor interface. The chip can also load itself by reading coefficients directly from memory. Accuracy of a filter response is typically within 1 percent of the calculated value (for corner frequencies) and dynamic range is a minimum of 72 dB.

Bandwidth varies depending upon the transfer function implemented, but can extend from 0 to 50 kHz. Anti-aliasing, smoothing and input gain

control are supported with on-chip uncommited operational amplifiers.

The user is provided instant feedback on filter performance in his system by the Crystal-ICE filter development system. The PC-based design tool includes filter synthesis software and an in-circuit hardware emulator.

AES/EBU TRANSMITTERS & RECEIVERS

The CS8401/2 AES/EBU transmitters, along with the CS8411/2 AES/EBU receivers, allow digital communication between audio equipment. Requiring minimum external circuitry, these IC's support both professional and consumer formats.

CONTENTS

See Crystal A/D Conversion Data Book (DADB3.0) for complete data sheets on the above.

• Notes •

High Speed Precision Track and Hold

Features

- Completely Self-Contained On-Chip Hold Capacitor Microprocessor Interface
- Fast Acquisition: 800ns to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset, Including Hold Pedestal: 1.8 mV
- Low Droop Rate: 0.001uV/us
- Self-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 130 mW

General Description

The CS3112 is a high speed track and hold with 12-bit linearity. It is completely self-contained, including hold capacitor, output buffer, and calibration circuitry.

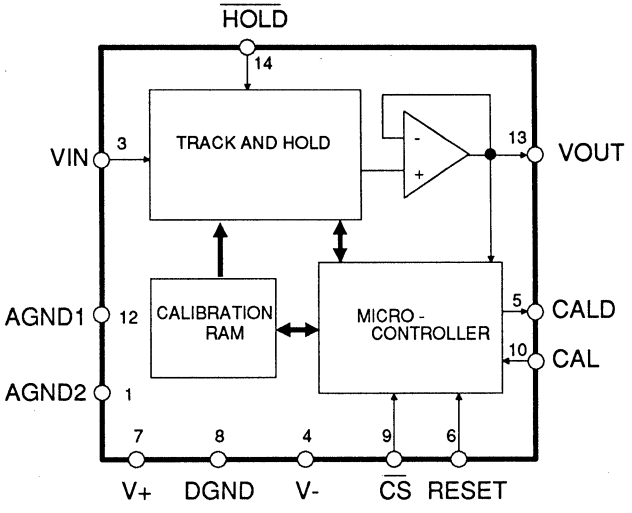
Aperture jitter of 100ps and acquisition time of 800ns to 0.01% provide excellent dynamic performance. An on-chip hold capacitor limits droop to 0.001 uV/us, and first order leakage compensation minimizes droop over the full operating temperature range.

Advanced CMOS fabrication insures low power consumption and increased reliability.

The CS3112 can be controlled and monitored through its microprocessor interface, or can operate independently.

ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS3112-KD2	2.0 µs	0 to 70 °C	14-pin CerDIP
CS3112-KD1	1.0 µs	0 to 70 °C	14-pin CerDIP
CS3112-BD1	1.0 µs	-40 to +85 °C	14-pin CerDIP
CS3112-TD1	1.0 µs	-55 to +125 °C	14-pin CerDIP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS31412

4 Channel Simultaneous Track and Hold

Features

- Completely Self-Contained
  - Four Track-and-Hold Amplifiers
  - On-Chip Hold Capacitors
  - Two Output Buffer Amplifiers
  - Microprocessor Interface
- 800ns Acquisition Time to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset Including Hold Pedestal: 2.8mV
- Low Droop Rate: 0.001uV/us
- Auto-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 250mW

General Description

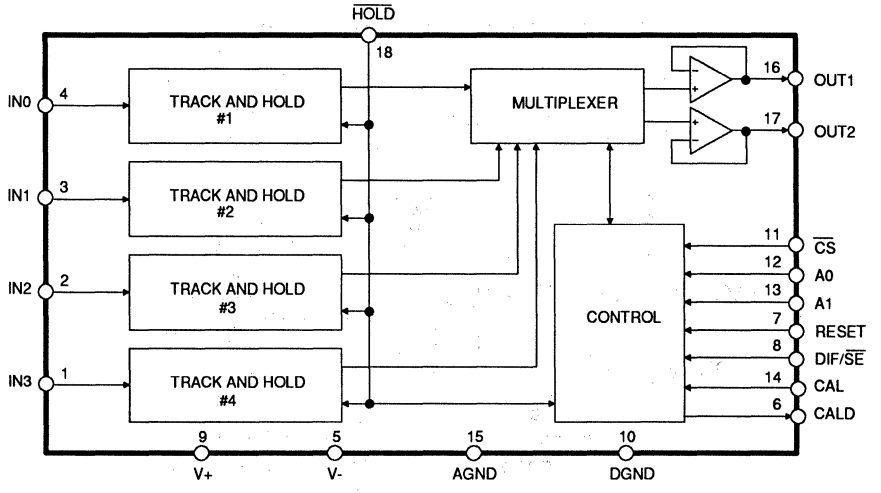
The CS31412 is a four-channel track and hold capable of processing four single-ended or two differential inputs with 12-bit linearity. It consists of four track-and-hold amplifiers, an analog multiplexer, two output buffers, and a microprocessor interface.

Controlled by a single $\overline{\text{HOLD}}$ input, the four track-and-hold amplifiers can simultaneously hold their outputs with only 100ps of aperture jitter and later acquire their inputs within 800ns to 0.01%. On-chip hold capacitors limit droop to 0.001uV/us, and first order leakage compensation minimizes droop over temperature.

The CS31412 can be configured, controlled, and monitored through its microprocessor interface, or can be operated independently of intelligent control.

ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS31412-KC2	2.0 µs	0 to 70°C	18-pin Ceramic SB DIP
CS31412-KC1	1.0 µs	0 to 70°C	18-pin Ceramic SB DIP
CS31412-BC1	1.0 µs	-40 to +85°C	18-pin Ceramic SB DIP
CS31412-TC1	1.0 µs	-55 to +125°C	18-pin Ceramic SB DIP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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Semiconductor Corporation

CS3901

± 1.5 V and 3.0 V Voltage Reference

Features

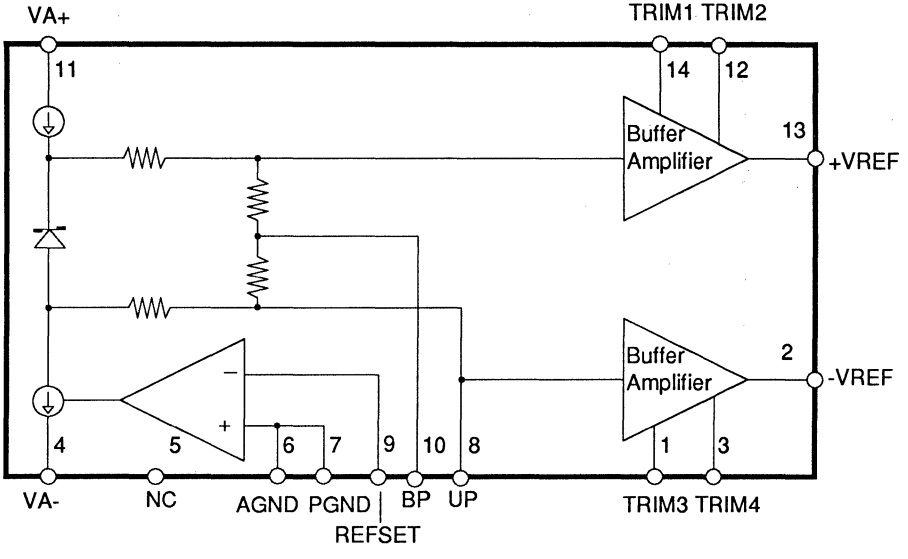
- High Accuracy
- Low Drift
- Excellent Stability
- Operates from ±5V
- + 3.0V or ± 1.5V outputs, jumper selectable
- Small package size - 14 Pin DIP

General Description

The CS3901 is a precision hybrid voltage reference for the CS5412 A/D Converter. The device offers jumper-selection options to provide either +3.0V or ± 1.5V outputs from ± 5V inputs. The voltage outputs do not require trimming, but trim pins are available if fine adjustments are desired. The outputs of the CS3901 provide low impedance, low noise and excellent temperature stability to insure optimum performance from the A/D converter. The unit is also compatible with other A/D converters where +3.0V or ±1.5V reference voltages are required.

ORDERING INFORMATION:

CS3901 - KC	0 °C to 70 °C
CS3901 - TC	- 55 °C to +125 °C



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS3902

+ 4.5V Precision Voltage Reference

Features

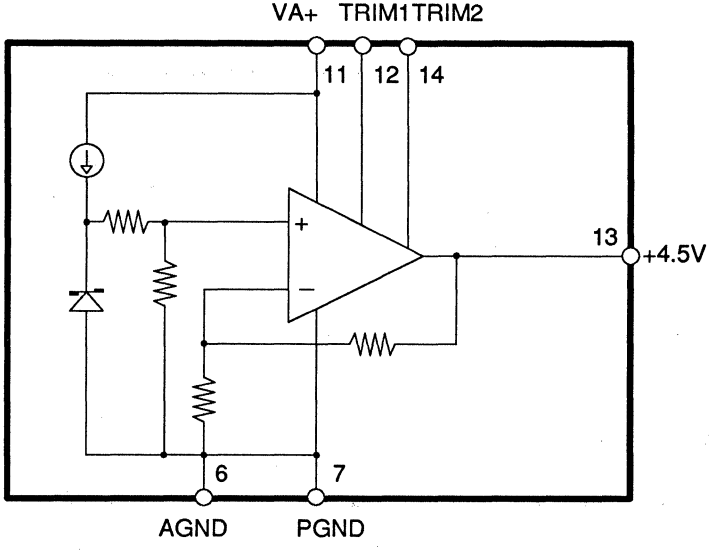
- Very High Accuracy: + 4.500V ± 0.4 mV
- Very Low Temperature Drift: ± 0.6 ppm / °C -55 °C to+125 °C
- Excellent Long-Term Stability: 25 ppm/1000 hours
- Excellent Line Regulation: 6 ppm/V Typ.
- Designed for use with CS5012, CS5014, CS5016, CS5101, and CS5102 A/D Converters
- 14 Pin DIP Package

General Description

The CS3902 is a precision voltage reference providing +4.500V from an input voltage of 11V to 22V. It offers very high accuracy without trimming and exhibits very low temperature drift: 1/50 LSB / °C at 16 bits. Long term stability of the CS3902 is excellent. The device is suitable for all Crystal Semiconductor Successive Approximation A/D Converters.

ORDERING INFORMATION:

Model	Initial Error	Thermal Drift	Temperature
CS3902-AC	800 µV	400 µV	-25 °C to +85 °C
CS3902-BC	400 µV	200 µV	-25 °C to +85 °C
CS3902-SC	800 µV	600 µV	-55 °C to +125 °C
CS3902-TC	400 µV	300 µV	-55 °C to +125 °C



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CS4328

18-Bit, Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System
  - 8x Interpolation Filter
  - Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 95 dB Dynamic Range over the Audio Band
- 0.001 dB Passband Ripple
- Completely Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
  - No External Components Needed
- 16 or 18 bit Input Words
- Supports Multiple Input Formats

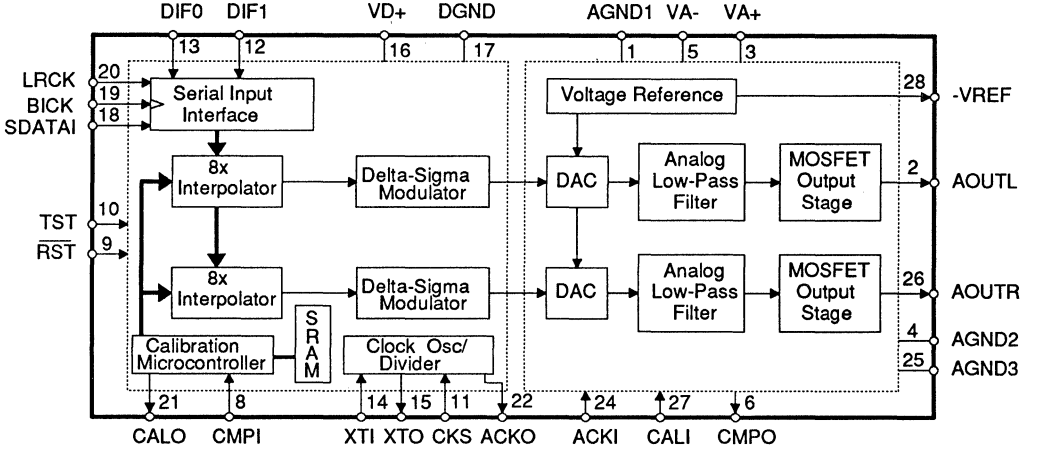
General Description

The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8× digital interpolation filter followed by a 64× oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultralinear analog low-pass filter. The total D/A system provides a linear phase response.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

To support various audio environments a clock select pin chooses between 256- and 384-times the input word rate for the master clock.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



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CRYSTAL
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CS5012A

12-Bit, 7 us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12-Bit Precision
  - Linearity Error: ±1/4 LSB
  - Total Unadjusted Error: ±1/4 LSB
  - DNL: ±1/16 LSB
- Low Distortion
  - Total Harmonic Distortion: 0.008%
  - Peak Harmonic or Noise: -92 dB
- 7.2 Microsecond Conversion Time
  - Throughout Rates up to 100 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 150 mW
- Pin Compatible with CS5014/CS5016

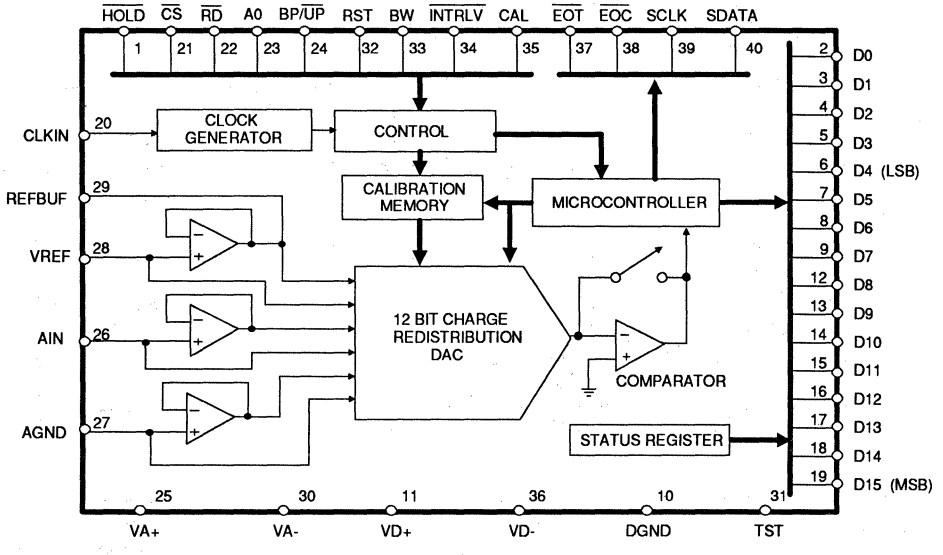
General Description

The CS5012A is a 12-bit monolithic analog to digital converter with a conversion time as fast as 7.2 µs. Unique self-calibration circuitry insures maximum nonlinearity of 1/2 LSB and no missing codes. Offset and full scale errors are kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5012A consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 2.8 µs to 0.01%, allowing throughput rates up to 100 kHz.

An evaluation board (CDB5012) is available for the CS5012A which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing. The CS5012A is pin compatible with the CS5014 and CS5016 A/D converters allowing system upgrading and downgrading without hardware alterations.

ORDERING INFORMATION: See ADC Data Book



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Semiconductor Corporation

CS5014

14-Bit, 14 us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 14-Bit Precision
  - Linearity Error: ±1/4 LSB
  - Total Adjusted Error: ±1 LSB
  - No Missing Codes
- Low Distortion
  - Total Harmonic Distortion: 0.003%
  - Peak Harmonic or Noise: -98 dB
- 14.25 Microsecond Conversion Time
  - Throughout Rates up to 56 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120 mW
- Pin Compatible with CS5012/CS5016

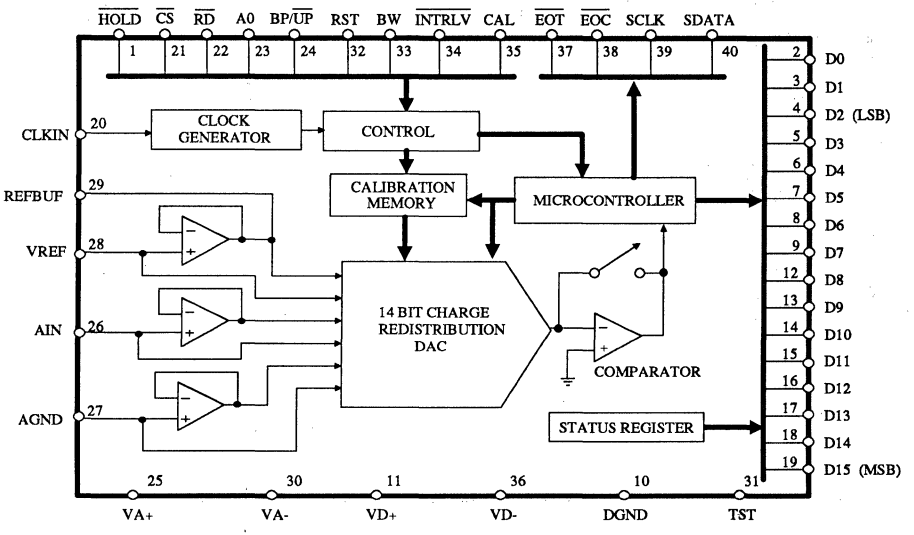
General Description

The CS5014 is a 14-bit monolithic analog to digital converter with a 14.25 µs conversion time. Unique self-calibration circuitry, which can be under intelligent control, insures maximum nonlinearity of 1/2 LSB and no missing codes. Offset and full scale errors are kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5014 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 µs to 0.003%, allowing throughput rates up to 56 kHz.

An evaluation board (CDB5014) is available for the CS5014 which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing. The CS5014 is pin compatible with the CS5012 and CS5016 A/D converters allowing system upgrading and downgrading without hardware alterations

ORDERING INFORMATION: See ADC Data Book



Semiconductor Corporation

CS5016

16-Bit, 16 us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 16-Bit Precision
  - Linearity Error: 0.001% FS
  - No Missing Codes
- Ultra-Low Distortion
  - Total Harmonic Distortion: 0.001%
  - Peak Harmonic or Noise: -104 dB
- 16.25 µs Conversion Time
  - Sample Rates up to 50 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120 mW
- Pin Compatible with CS5012/CS5014

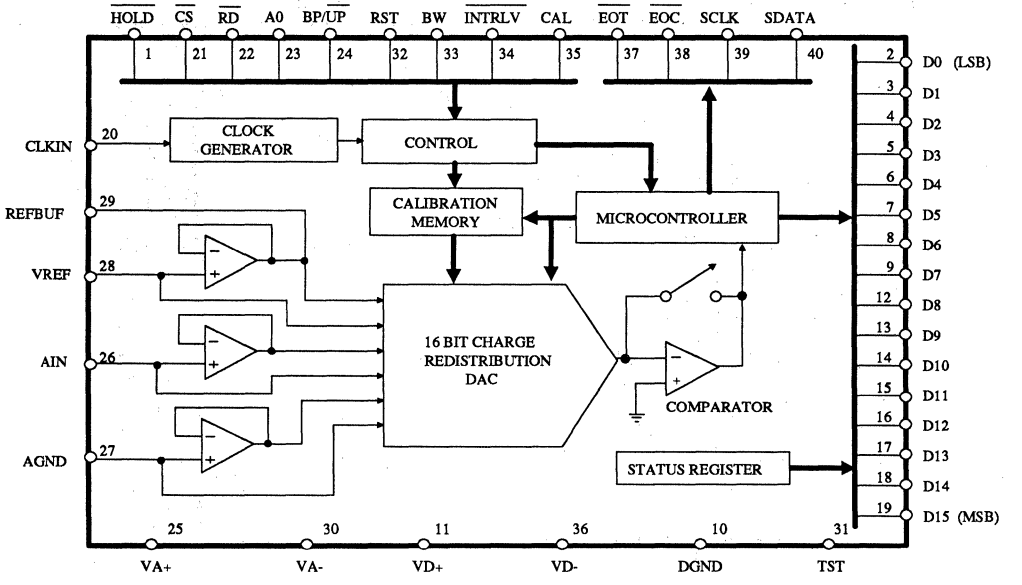
General Description

The CS5016 is a 16-bit monolithic analog to digital converter with a 16.25 µs conversion time. Unique self-calibration circuitry insures maximum nonlinearity of 0.001% FS and no missing codes. This insures low distortion and maintains good signal to noise performance with low-level signals. Offset and full scale errors are kept within 1 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5016 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 µs to 0.01%, allowing throughput rates up to 50 kHz.

An evaluation board (CDB5016) is available for the CS5016 which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing.

ORDERING INFORMATION: See ADC Data Book



Crystal Semiconductor Corporation
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Semiconductor Corporation

CS5101

16-Bit, 100 kHz Serial-Output A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 92 dB; THD: 0.001%
- Linearity Error: ± 0.001% FS
- 8.1 µs Conversion Time with Guaranteed 16-bit No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption: 320 mW
  - Power-down Mode: 1 mW
- Evaluation Board Available

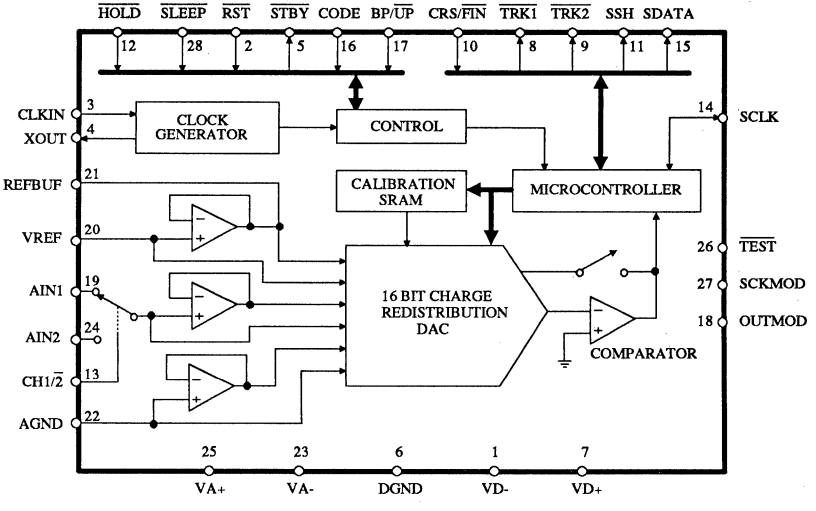
General Description

The CS5101 is a 16-bit monolithic CMOS analog-to-digital converter capable of 100 kHz throughput. On-chip self-calibration circuitry achieves nonlinearity of ±0.001% of FS and guarantees 16-bit no missing codes. Superior linearity also leads to 92 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are similarly kept within 2 LSB, eliminating the need for manual calibration of any kind.

The CS5101 consists of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, crystal oscillator, comparator, and serial communications port. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input after each conversion within 1.9 µs, allowing throughput rates up to 100 kHz.

The converter's 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION: See ADC Data Book



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Semiconductor Corporation

CS5102

16-Bit, 20 kHz Serial-Output A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 91 dB; THD: 0.001%
- 40 µs Conversion Time
  - Linearity Error: ± 0.001% FS
  - Guaranteed No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption: 44 mW
  - Power-down Mode: 1 mW
- Evaluation Board Available
- Pin compatible with CS5101, 100 kHz 16-bit ADC

General Description

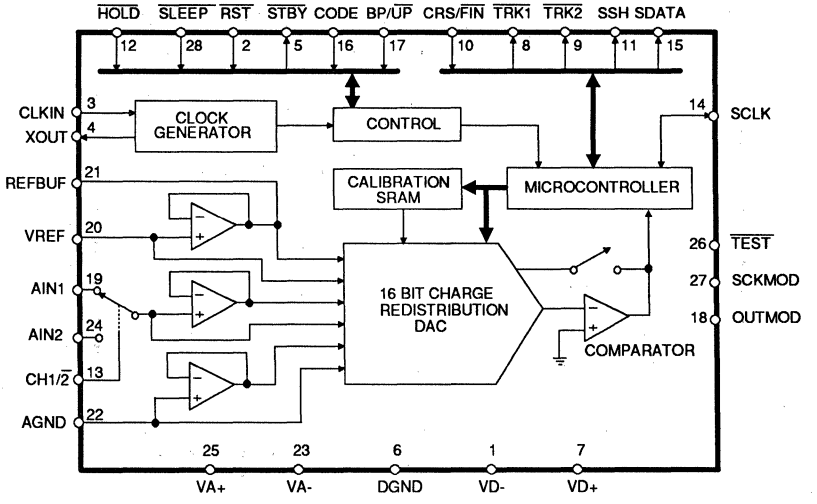
The CS5102 is a 16-bit monolithic CMOS analog-to-digital converter capable of 20 kHz throughput. The CS5102's low power consumption of 44 mW, coupled with a power down mode, makes it particularly suitable for battery powered operation.

On-chip self-calibration circuitry achieves nonlinearity of ±0.0015% of FS and guarantees 16-bit no missing codes up to 20 kHz throughput. Superior linearity also leads to 91 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are similarly kept within 2 LSB, eliminating the need for manual calibration of any kind.

The CS5102 consists of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input after each conversion, allowing throughput rates up to 20 kHz.

The converter's 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION: See ADC Data Book



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

16-Bit, Stereo A/D Converter for Digital Audio

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Stereo or Monaural Capability
  - Serial Output
- Monaural Sampling Rates up to 100 kHz
  - 50 kHz/Channel Stereo Sampling
- Signal-to-(Noise+Distortion): 92 dB
- Dynamic Range: 92 dB
  - 95dB in 2X Oversampling Schemes
- Interchannel Isolation: 90 dB
- 2's Complement or Binary Coding
- Low Power Dissipation: 260 mW
  - Power Down Mode for Portable Applications
- Evaluation Board Available

General Description

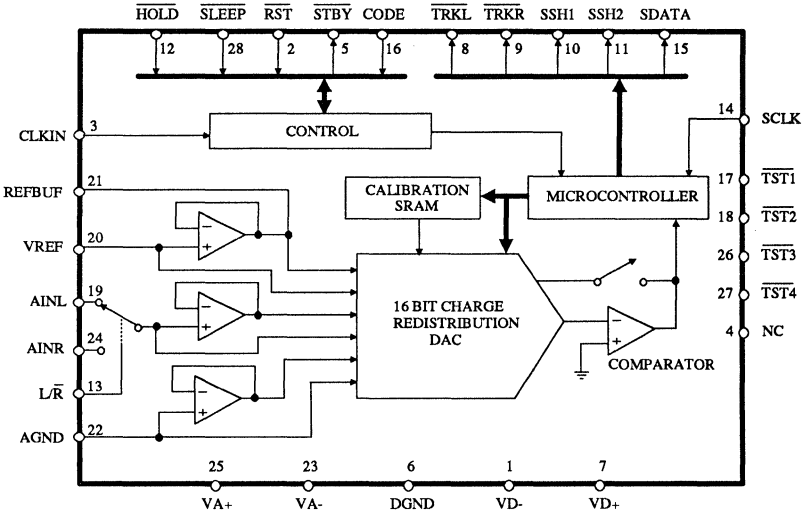
The CS5126 CMOS analog-to-digital converter is an ideal front-end for stereo or monaural digital audio systems. The CS5126 can be configured to handle two channels at up to 50kHz sampling per channel, or it can be configured to sample one channel at rates up to 100kHz.

The CS5126 executes a successive approximation algorithm using a charge redistribution architecture. On-chip self-calibration circuitry has 18-bit resolution thus avoiding any degradation in performance with low-level signals. The charge redistribution technique also provides an inherent sampling function which avoids the need for external sample/hold amplifiers.

Signal-to-(noise+distortion) in stereo operation is 92dB, and is dominated by internal broadband noise (1/2 LSB rms). When the CS5126 is configured for 2X oversampling, digital post-filtering bandlimits this white noise to 20kHz, increasing dynamic range to 95dB.

ORDERING INFORMATION:

CS5126-KP	0 °C to 70 °C	(was CSZ5126-KP) 28-Pin Plastic DIP
CS5126-KL	0 °C to 70 °C	28-Pin PLCC



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CRYSTAL
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CS5317

16-Bit, 20 kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

General Description

The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

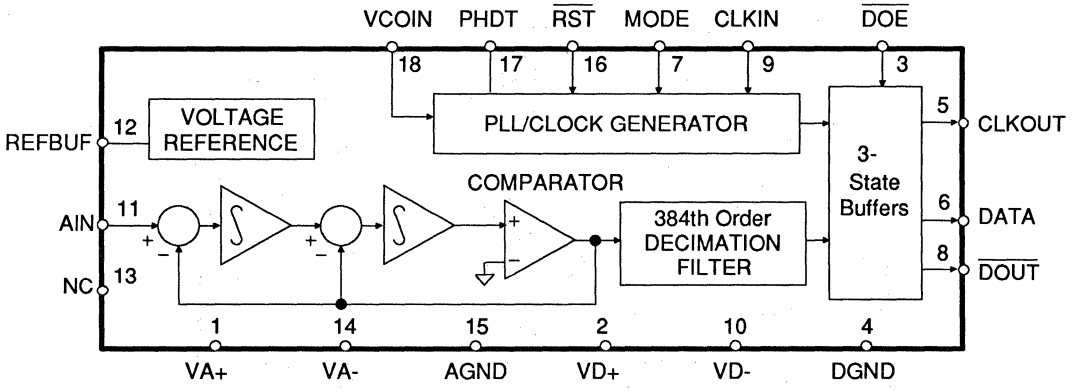
An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: See ADC Data Book

Block Diagram



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(512) 445-7222 FAX 512 445- 7581

Semiconductor Corporation

CS5322/CS5323

24-Bit Variable Bandwidth A/D Converter

Features

- Monolithic CMOS A/D Converter
- 100 dB Harmonic Distortion
- Delta-Sigma Architecture
  -Variable Oversampling: X32 to X4096
  -Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  -Hardware or Software Selectable Options
  -Eight Selectable Filter Corner Frequencies: 23, 47, 94, 187, 375, 750, 1500 and 3000 Hz
- Low Power Dissipation

General Description

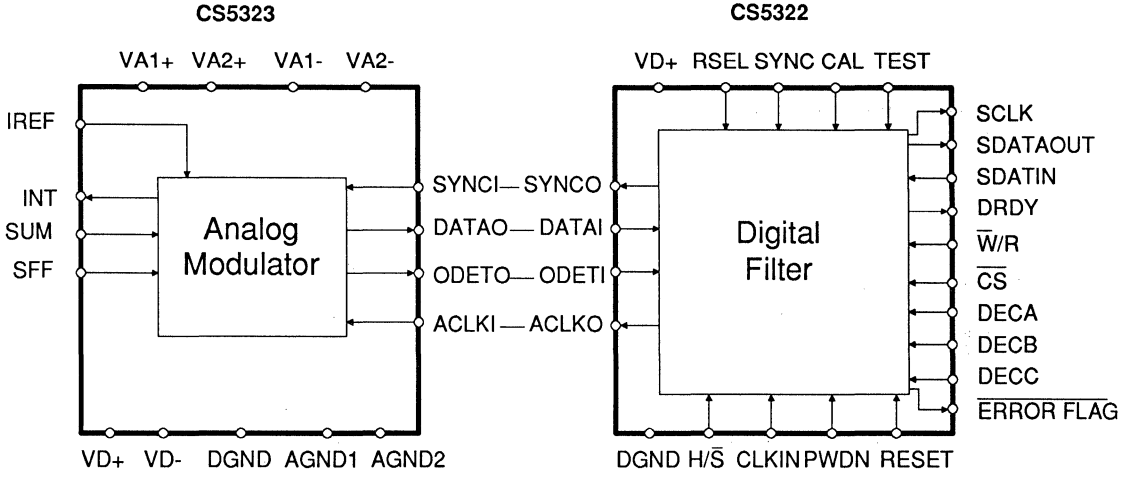
The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of eight selectable update periods: 16, 8, 4, 2, 1, 0.5, 0.25 and 0.125 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation. Power dissipation for the pair is less than 250 mW.

ORDERING INFORMATION

CS5322-BL	-40 to +85 °C	28-pin PLCC
CS5323-BL	-40 to +85 °C	28-pin PLCC



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Semiconductor Corporation

CS5324

120 dB, 500 Hz Oversampling A/D Converter

Features

- Monolithic CMOS A/D converter
- 120dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - —256X Oversampling
  - —Linear Phase Digital Filter
  - —Output Word Rate 32 kHz
- Low Power Dissipation: 180 mW max.
- Evaluation Board Available

General Description

The CS5324 analog to digital converter is a unique, very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

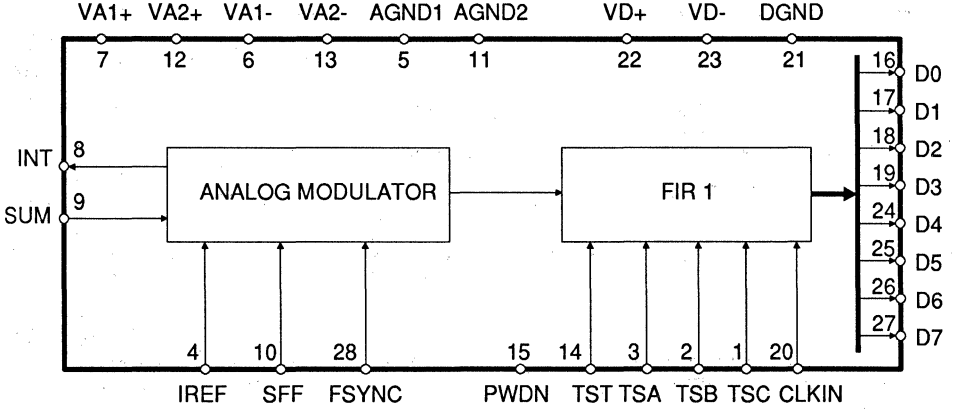
The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

ORDERING GUIDE:

CS5324-KL	0° to 70°C	28-pin PLCC
CS5324-BL	-40° to +85°C	28-pin PLCC
CDB5324	Evaluation Board	

Block Diagram



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CRYSTAL
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CS5326 CS5327
CS5328 CS5329

16 & 18-Bit, Stereo A/D Converters for Digital Audio

2

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  - 30 kHz to 50 kHz
- Low Noise and Distortion
  - 95 dB dynamic range, 16-Bit
  - 97 dB dynamic range, 18-Bit
  - 100 dB dynamic range, 19-Bit Mono
  - 0.0015% THD
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.001dB Passband Ripple
  - 86dB Stopband Rejection
- Low Power Dissipation: 450 mW
  - Power-Down Mode for Portable Applications

General Description

The CS5326, CS5327, CS5328 & CS5329 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16 or 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

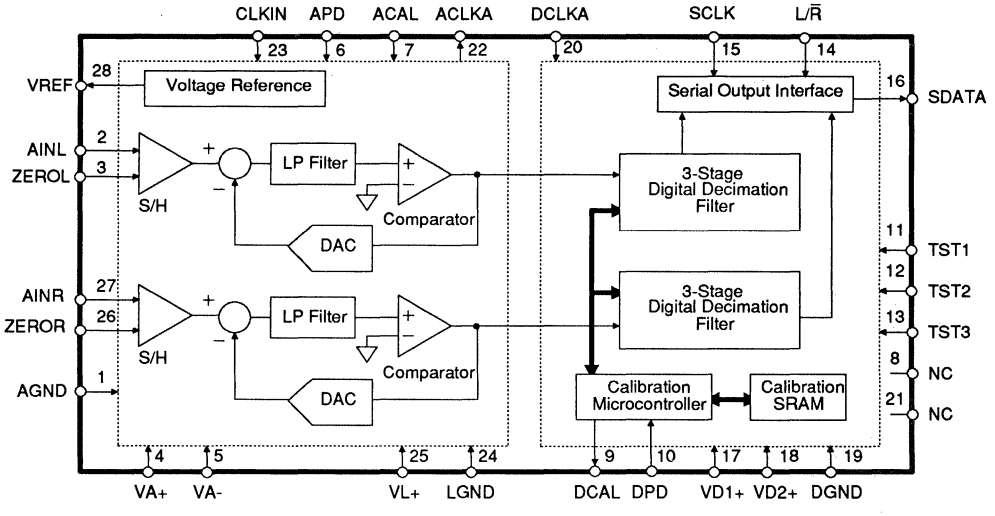
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5326 & CS5327 are 16-bit ADCs, achieving 95 dB dynamic range. The CS5328 & CS5329 are 18-bit ADCs with 97 dB dynamic range in stereo mode and 100 dB dynamic range in mono mode.

The CS5326 & CS5328 have digital filters which are compatible with CD requirements. The CS5327 & CS5329 have filters which guarantee no aliasing. The filters have linear phase, 0.001 dB passband ripple, and >86 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP.

ORDERING INFORMATION: See ADC Data Book



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CRYSTAL
Semiconductor Corporation

CS5336 CS5337
CS5338 CS5339

16-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion
  - >90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 400 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5336, CS5337, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

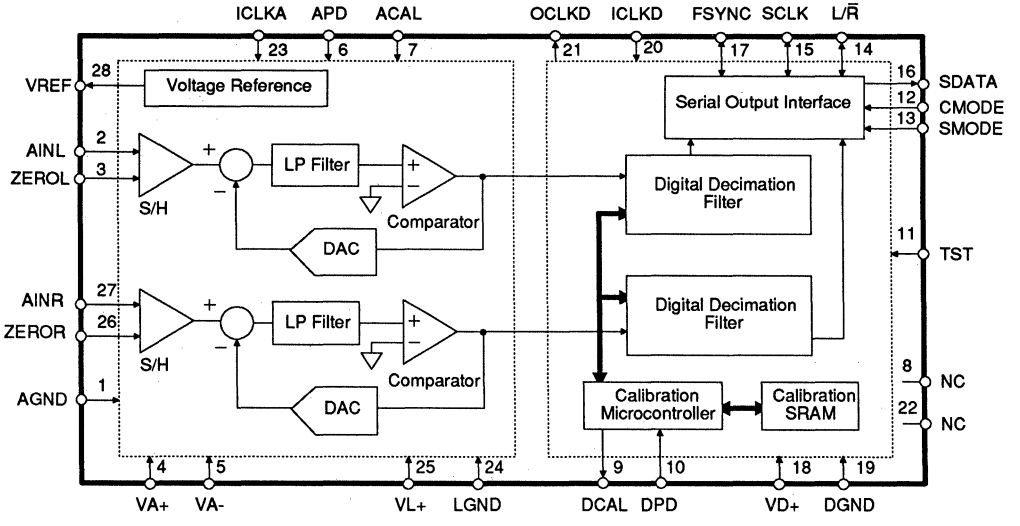
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5337 & CS5339 have an SCLK which clocks out data on falling edges.

The CS5336 & CS5337 have a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package.

ORDERING INFORMATION: See ADC Data Book



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS5412

12-Bit, 1MHz Self-Calibrating A/D Converter

2

Features

- Monolithic CMOS Sampling ADC
  On-Chip Track and Hold Amplifier
  Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  Typical Nonlinearity: 3/4 LSB
  No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

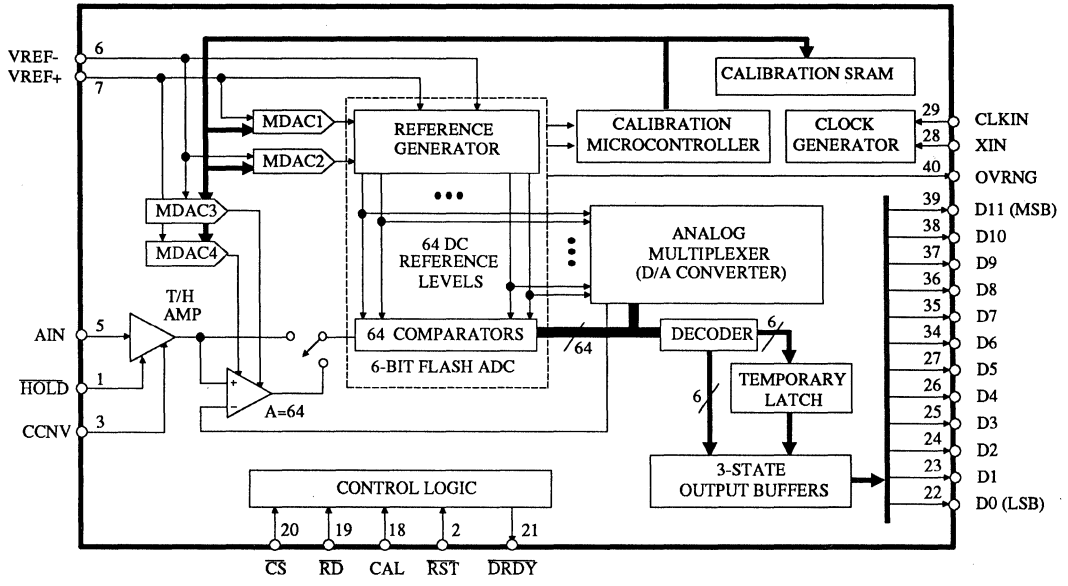
The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acqusition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

ORDERING INFORMATION: See ADC Data Book



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS5501

Low-Cost, 16-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering
  6-Pole, Low-Pass Gaussian Filter
  Corner Frequencies from 0.1 to 10Hz
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.0015% FS Max
  Offset and Full-Scale Errors: ±1/2 LSB
  16-Bit No Missing Codes (DNL ±1/8 LSB)
- System Calibration Capability
- Flexible Serial Communications Port
  UART- and µC-Compatible Formats
  3-State Data and Clock Outputs
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  10µW Sleep Mode for Portable Applications
- Evaluation Board Available

General Description

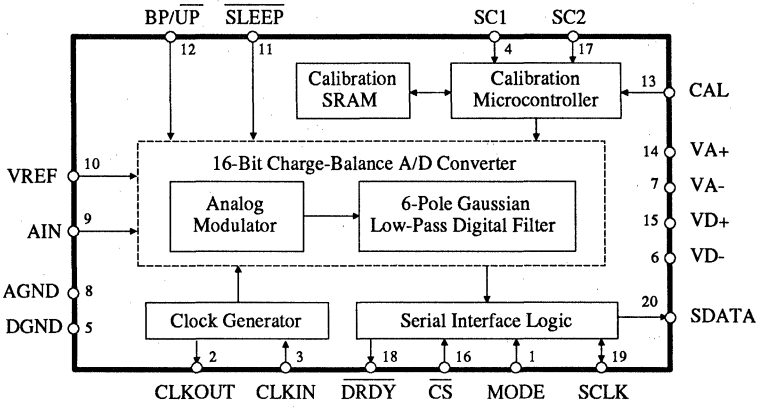
The CS5501 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5501 utilizes charge-balance techniques to achieve true 16-bit accuracy with up to 4kHz word rates at very low cost.

The CS5501 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The filter has a low-pass, 6-pole Gaussian response with no overshoot in response to step functions. Corner frequencies can be set from 0.1Hz to 10Hz, thus rejecting 50Hz and 60Hz line frequencies and any noise at spurious frequencies.

The CS5501 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB. The device can also be applied in system calibration schemes to null offset and gain errors in the input channel.

The CS5501's serial port offers three modes of operation. In addition to a UART-compatible mode of asynchronous communication, there are two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

ORDERING INFORMATION: See ADC Data Book



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Crystal Semiconductor Corporation
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(512) 445-7222 FAX: 512 445-7581

Semiconductor Corporation

CS5503

Low-Cost, 20-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering:
  6-Pole, Low-Pass Gaussian Filter with Corner Frequencies from 0.5 to 10Hz
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.0003% FS
  Offset and Full-Scale Errors: ±4 LSB
  20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  µC-Compatible Formats
  3-State Data and Clock Outputs
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  Sleep Mode for Portable Applications
- Evaluation Board Available

General Description

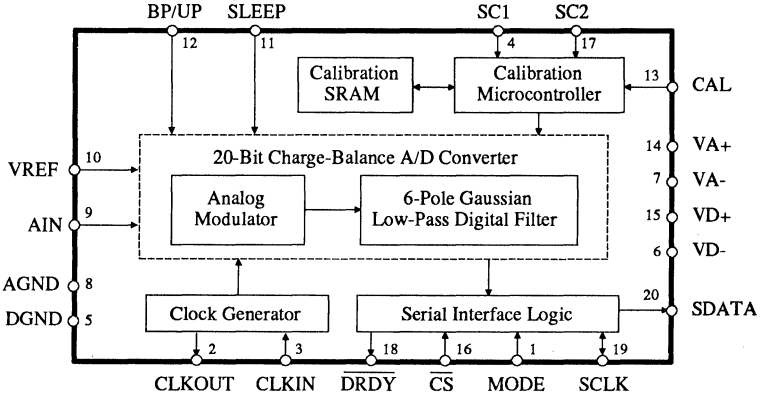
The CS5503 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5503 utilizes charge-balance techniques to achieve true 18-bit accuracy with up to 4kHz word rates at low cost, in a 20-pin DIP package.

The CS5503 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at a 4kHz rate. The filtering assumes a low-pass, 6-pole Gaussian response. Corner frequencies can be set from 0.5Hz to 10Hz, thus rejecting 50Hz and 60Hz frequencies and any noise at spurious frequencies.

The CS5503 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of less than 4 LSB. The device can also be applied in system calibration schemes to null offset and gain errors in the input channel.

The CS5503's serial port offers two modes of operation, for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. The CS5503 is pin compatible with the 16-bit CS5501.

ORDERING INFORMATION: See ADC Data Book



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: 512 445 7581

Semiconductor Corporation

CS5505

Low-Cost, Four channel, 16 - bit A/D Converter

Features

- Offers superior performance to integrating A/D converters.
- Four channel pseudo- differential inputs
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.0015% FS Max
  16-Bit No Missing Codes (DNL ±1/8 LSB)
- Output data rates up to 60/second
- Flexible Serial Communications Port
  µC-Compatible Formats
  3-State Data and Clock Outputs
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 2mW
  10µW Sleep Mode for Portable Applications
- Available in 24 pin 0.3 in molded and hermetic DIP, and SOIC packages

General Description

The CS5505 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5505 utilizes charge-balance techniques to achieve true 16-bit accuracy with 20Hz word rates at very low cost.

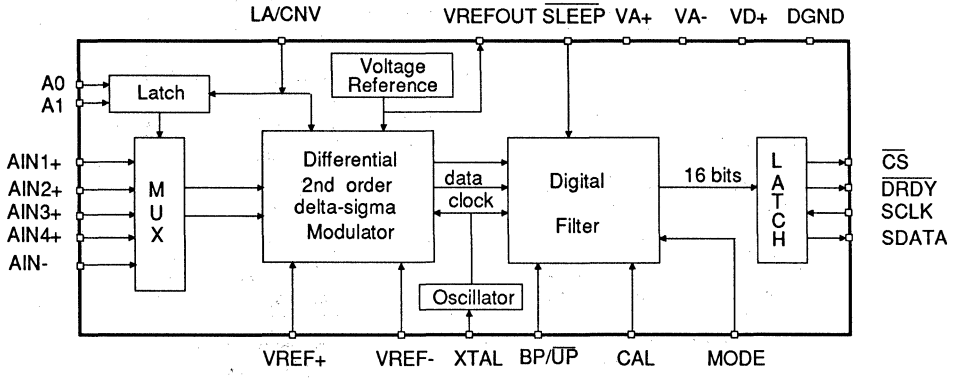
The CS5505 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at a 20Hz rate. The user can randomly address any of the four pseudo-differential input channels and perform conversions on demand.

The on chip digital filter offers superior line rejection at 50 and 60Hz with the added advantage of spurious noise rejection at higher frequencies.

The CS5505 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB.

The CS5505's serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

ORDERING INFORMATION:
Contact Crystal Semiconductor



Preliminary Specification

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Crystal Semiconductor Corporation
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(512) 445-7222 FAX: 512 445-7581

Semiconductor Corporation

CS7008

Digitally Configurable Universal Filter

Features

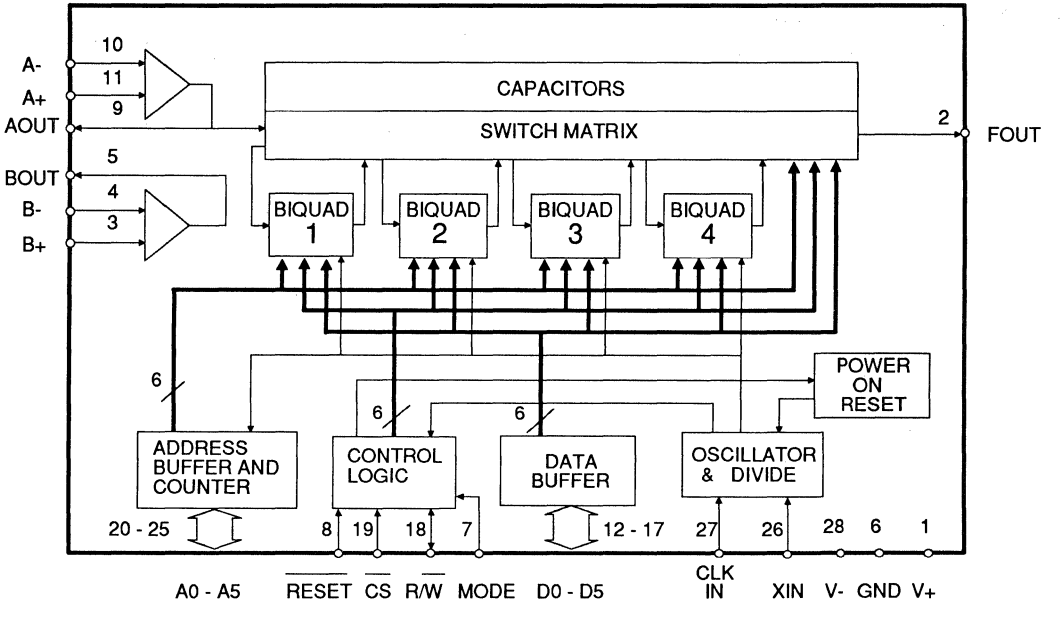
- Implements Even-Order Filters:
  - To 50 kHz
  - To 8th Order
- Same output pin for all filter types
- Digitally Programmable:
  - Self Loading Mode
  - µP bus Mode
- Filter can be changed in 30 µs for adaptive applications
- Two Uncommitted Op Amps for Input Antialiasing and Output Smoothing
- Supported by CRYSTAL-ICE Filter Development System CDS7000
- Readback capability

General Description

The CS7008 is fabricated in standard 3 micron digital CMOS. It achieves high levels of performance through Crystal's SMART *Analog*™ design techniques. The CS7008 is a digitally configurable switched capacitor filter capable of implementing virtually any even-order filter response of eighth order or below to 50 kHz. A microprocessor interface permits in-system reconfiguration of the filter resonse. Access to two op amps is also provided for use as input antialialsing and output smoothing filters if desired.

System design is greatly simplified by using the Crystal-ICE Filter Development System, CDS7000. The development system provides menu-driven software that aids in the design and optimization of filters and provides hardware to download the filter parameter to a CS7008 (for in-circuit verification of performance) or to an EPROM programmer or DOS Files. The development system consists of hardware and software for use with an IBM PC and provides in-circuit emulation of the CS7008.

ORDERING INFORMATION: See ADC Data Book



Semiconductor Corporation

CS7820

High Speed 8-Bit A-to-D with Track and Hold

Features

- Completely Self-Contained
  - On-Chip Track and Hold
  - Microprocessor Interface
  - Internal Clock
  - Overrange Flag
- Fast Conversion: 1.36µs Max
- True 8-bit Accuracy over Temperature
  - No Trims Required
  - No Missing Codes
- Low Power Dissipation: 100mW Max
- Replaces ADC0820 and AD7820
- Single +5V Supply
- Improved Latch-up Resistance

General Description

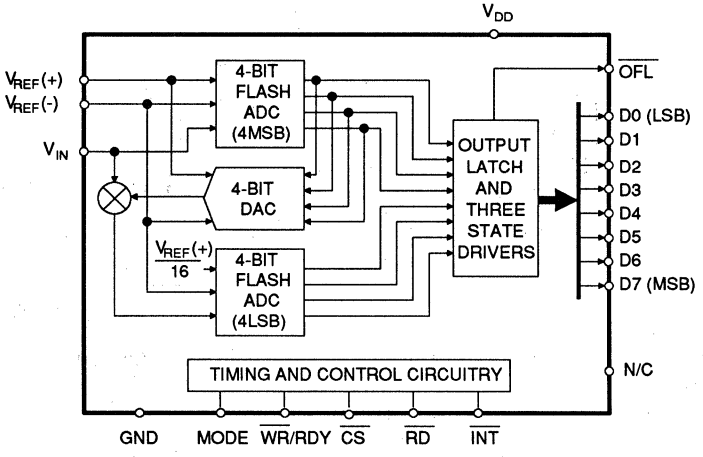
The CS7820 is a low-cost, easy to use, microprocessor compatible 8-bit analog-to-digital converter with on-chip track-and-hold function. Use of CMOS and half-flash techniques allow both high throughput rates (1.36µs max conversion time) and low power requirements (100mW max over the full Mil temperature range).

The input to the CS7820 is tracked and held by on-chip sampling circuitry, eliminating the need for an external track-and-hold amplifier for input signals slewing at less than 100mV/µs.

The CS7820 is designed to appear as a memory location or I/O port to a microprocessor without additional external interfacing logic. All of the data outputs use latched, three-state output buffers, allowing direct connection to a data bus or input port on a microprocessor system.

The CS7820 is pin compatible with the ADC0820 and AD7820.

ORDERING INFORMATION: See ADC Data Book



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Crystal Semiconductor Corporation
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AES/ EBU Interface Line Driver

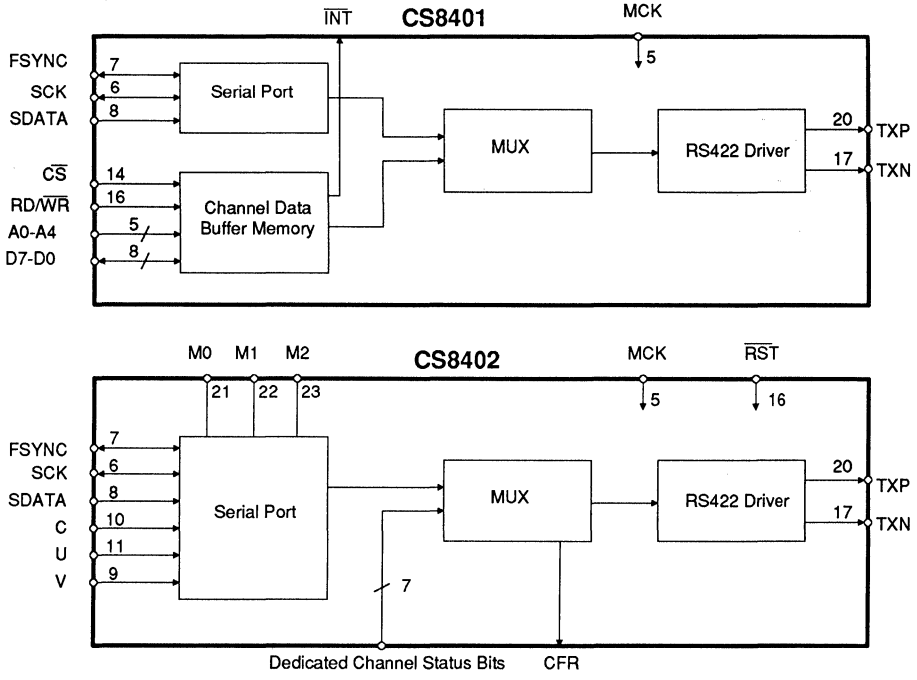
Features

- Monolithic AES/EBU Interface Transmitter
- Supports S/PDIF and EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver

General Description

The CS8401/2 is a monolithic CMOS device which encodes and transmits audio data according to the AES/EBU interface standards. The CS8401/2 accept audio and digital data, which is then multiplexed, encoded and driven directly, or through a transformer, onto a cable. The CS8401 has an internal buffer memory for 1 block of channel data, which is loaded via an 8-bit parallel interface. The CS8402 multiplexes in the channel data directly from external input pins.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



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Semiconductor Corporation

CS8411 CS8412

AES/ EBU Interface Line Receiver

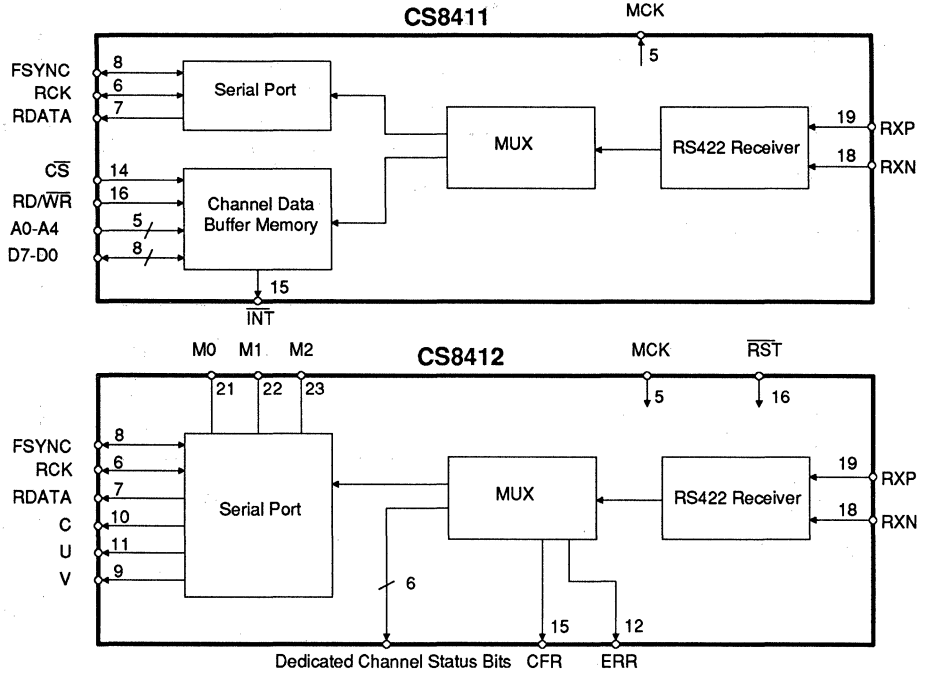
Features

- Monolithic AES/EBU Interface Receiver
- Supports S/PDIF and EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Checks CRC Codes and Parity Bits
- On-Chip RS422 Line Receiver
- Low Jitter Clock Recovery

General Description

The CS8411/12 is a monolithic CMOS device which receives and decodes audio data encoded according to the AES/EBU interface standard. The CS8411/12 receives data from the transmission line, recovers the clock and synchronization signals, and de-multiplexes the audio and digital data. Differential or single ended inputs can be decoded to the professional and consumer interface standards. The CS8411 has an internal buffer memory for 1 block of channel data, which is read via an 8-bit parallel interface. The CS8412 de-multiplexes channel data directly to external pins.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



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INTRODUCTION

Low Power T1, PCM-30 and ISDN Primary Rate Line Interface Circuits

Crystal Semiconductor offers a broad family of low power CMOS PCM line interface circuits, with each device optimized for a unique system application. The CS6152, CS6159, CS61535A, CS61574A, and CS61575 are recommended for use in new designs.

CS6152: Basic DSX-1 driver and receive buffer. For low power cards using digital-ASIC clock recovery. Ideal for trunk card bays where T1 density is limited by heat dissipation.

CS6159: Ideal for large synchronous systems such as central offices and DCS 0/1, which need the lowest cost per line, small package and low power consumption.

CS61535A: Enhanced transmit-side jitter attenuator supports SONET VT1.5 and VT2, and other high speed transmission systems such as digital microwave radio and M13 multiplexers.

CS61574A and CS61575: Receive-side jitter attenuation supports loop-timing in customer-premises equipment (which needs to meet AT&T 62411) and in channel banks.

Since introducing the industry's first T1 and PCM-30 line interface circuits (the CS61534 and CS61544), we have shipped more CMOS PCM line interface ICs than any other vendor worldwide. Crystal Semiconductor's leadership continues with the best in pulse shapes, jitter attenuation, jitter tolerance and low power consumption.

Product	CS6152	CS6159	CS61535A	CS61574A	CS61575
Application	T1	T1 & PCM-30	T1 & PCM-30	T1 & PCM-30	T1 & PCM-30
Receiver Functions	Data Slicer	Clock & Data Recovery	Clock & Data Recovery	Clock & Data Recovery & Jitter Atten.	Clock & Data Recovery & Jitter Atten.
Transmitter Functions	Driver	Driver	Jitter Atten. & Driver	Driver	Driver
Serial Control Port	-	-	yes	yes	yes
DIP Package	24-pin, 300 mil	24-pin, 300 mil	28-pin, 600 mil	28-pin, 600 mil	28-pin, 600 mil
AMI/B8ZS/ HDB3 Coder	-	-	yes	yes	yes
Jitter Tolerance of Receiver	> 300 UI	> 300 UI	> 300 UI	28 UI	138 UI

Early generation line interface products have been superceded for new designs by enhanced performance devices:

- CS61535A supercedes the CS61534 and CS61544 for high-speed transmission systems.
- CS6159 supercedes the CS6158/CS6158A for large synchronous systems.

However, all Crystal line interface ICs remain in volume production.

T1 Transceiver

Crystal Semiconductor's CS2180B T1 Transceiver is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (D4, SLC-96 and T1DM and ESF). Serial interface and control registers make it simple to configure from a microprocessor, including per-channel control options. Packages available include 40-pin DIP or 44-lead PLCC.

While maintaining 100% compatibility, Crystal has improved on industry-standard 2180 designs:

- Support of SLC-96 and T1DM formats
- Compliance with TR-TSY-000191 AIS detection criteria
- Compliance with Bellcore Loss-of-carrier detection criteria
- Buffered serial data interface, eliminating need for SDI to be valid for both rising/falling edges of SCLK
- Enhanced serial data interface addressing, allowing one microprocessor serial port to be shared with a Crystal Line Interface
- Universal AMI/B8ZS receiver
- Industrial temperature operating range

Quartz Crystals

To complement our family of T1 Line Interface circuits, Crystal Semiconductor now supplies pullable quartz crystals. The CXT6176 (for T1 applications at 1.544 Mbps) and CXT8192 (for PCM-30 applications at 2.048 Mbps) are designed for 100% compatibility with our PCM line interface and jitter attenuator circuits.

CONTENTS

T1 Transceivers

Features

- Monolithic T1 Framing Device
- Both Transceivers support D4 and ESF framing formats
- CS2180B also supports SLC-96 and T1DM framing formats
- CS2180B has updated AIS and Carrier Loss detection criteria
- CS2180B is Plug Compatible with CS2180A, DS2180A and DS2180

General Description

The CS2180A and CS2180B are monolithic CMOS devices which encode and decode T1 framing formats. The devices support bit-seven and B8ZS zero suppression, and bit-robbed signaling. Clear channel mode can be selected on a per channel basis.

The serial interface has been enhanced to allow the CS2180A and CS2180B to share a chip select signal and register address space with the CS61534/35/74 PCM Line Interface device.

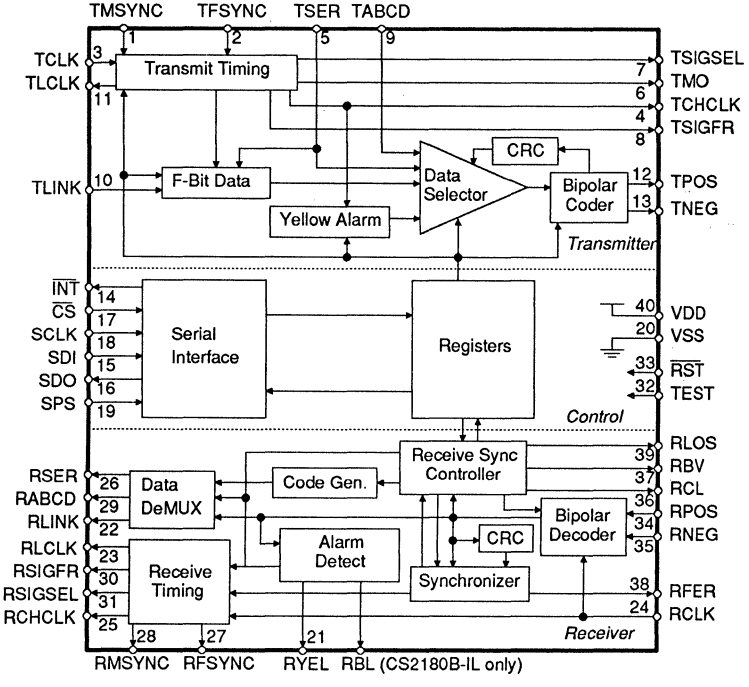
Applications

- T1 Line Cards
- ISDN Primary Rate Line Cards

Ordering Information:

CS2180B-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180B-IL	44 Pin PLCC	-40 to 85 °C
CS2180A-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180A-IL	44 Pin PLCC	-40 to 85 °C

3



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Referenced to GND)	V_{DD}	-	-	6.0	V
Input Voltage, any pin(Referenced to GND)	V_{IN}	-1.0	-	+7	V
Input Current, any pin (Note 1)	I_{IN}	-10	-	+10	mA
Ambient Operating Temperature	T_A	-40	-	85	°C
Storage Temperature	T_{STG}	-65	-	150	°C
Soldering Temperature for 10 s.	-	-	-	260	°C

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Voltage	V_{DD}	4.5	5.0	5.5	V
Supply Current (Notes 2, 3)	I_{DD}	-	3	10	mA
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Consumption (Notes 2, 3)	P_C	-	15	55	mW

Notes: 2. TCLK = RCLK = 1.544 MHz. If RCLK is static and $\overline{RST}$ is high, P_C will typically be 400 mW. Long term operation in this condition may degrade reliability.
3. Outputs open.

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; V_{DD} = 5.0 V ±10%; GND = 0 V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}	-0.3	-	+0.8	V
High-Level Output Voltage (Note 4)	V_{OH}	V_{DD} - 1.0	-	-	V
Low-Level Output Voltage (I_{OUT} = 1.6 mA)	V_{OL}	-	-	0.4	V
Output Current @ 2.4 V (Note 5)	I_{OH}	-	-	-1	mA
Output Current @ 0.4 V (Note 6)	I_{OL}	+4	-	-	mA
Input Leakage Current	I_{IL}	-	-	1	uA
Output Leakage Current (Note 7)	I_{LO}	-	-	1	uA
Input Capacitance	C_{IN}	-	-	5	pF
Output Capacitance	C_{OUT}	-	-	7	pF

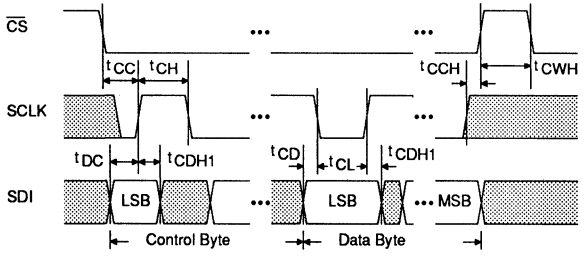
Notes: 4. I_{OUT} = -100 µA. This guarantees the ability to drive one TTL load (V_{OH} = 2.4 V @ I_{OUT} = -40 µA).
5. All outputs except $\overline{INT}$, which is open drain.
6. All outputs.
7. Applies to SDO when tristated.

SWITCHING CHARACTERISTICS - SERIAL PORT

(T_A = -40 to 85 °C; V_{DD} = 5V ± 10%; V_{IH} = 2.0V; V_{IL} = 0.8V; Maximum input rise & fall times of 10 ns)

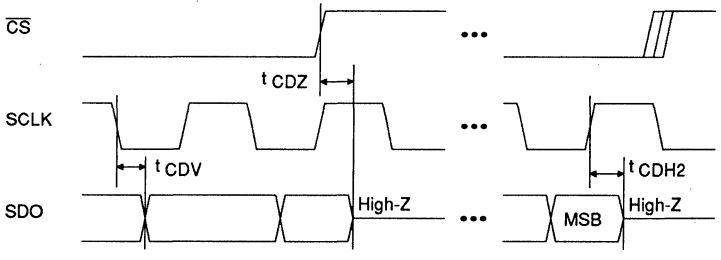
Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup	t_{DC}	50	-	-	ns
SCLK to SDI Hold	t_{CDH1}	50	-	-	ns
SDI to SCLK Falling Edge (Applies to CS2180A)	t_{CD}	50	-	-	ns
SCLK Low Time	t_{CL}	250	-	-	ns
SCLK High Time	t_{CH}	250	-	-	ns
SCLK Rise & Fall Times	t_R, t_F	-	-	500	ns
$\overline{CS}$ to SCLK Set up	t_{CC}	50	-	-	ns
SCLK to CS Hold	t_{CCH}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{CWH}	250	-	-	ns
SCLK to SDO Valid (Note 8)	t_{CDV}	-	-	200	ns
SCLK Rising to MSB of SDO Hold (Note 9)	t_{CDH2}	25	-	-	ns
$\overline{CS}$ to SDO High-Z	t_{CDZ}	-	-	75	ns

Note: 8. Output load capacitance = 100 pF.
9. SDO goes High-Z after rising edge of SCLK for MSB, regardless of the state of $\overline{CS}$.



Serial Port Write Timing

Notes: 10. For the CS2180A only, data bytes must be valid across low clock periods to prevent transients in operating modes. t_{CD} is not a requirement for the CS2180B. In the CS2180B data is latched on the rising edge of SCLK.
11. Shaded regions indicate *don't care* states.



Serial Port Read Timing

Note: 12. Serial port write must precede a port read to provide address information.
13. SDO will go High-Z: 1) if $\overline{CS}$ returns high at anytime; 2) after outputing MSB.

SWITCHING CHARACTERISTICS - TRANSMITTER

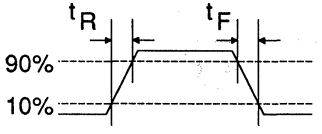
(T_A = -40 to 85 °C; V_{DD} = 5V ± 10%; V_{IH} = 2.0V; V_{IL} = 0.8V; Maximum input rise & fall times of 10 ns)

Parameter	Symbol	Min	Typ	Max	Units
TCLK Period	t_P	250	648	-	ns
TCLK Pulse Width	t_{WL}, t_{WH}	125	324	-	ns
TCLK Rise & Fall Times	t_F, t_R	-	20	-	ns
TSER, TABCD, TLINK Setup to TCLK Falling	t_{STD}	50	-	-	ns
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	50	-	-	ns
TFSYNC, TMSYNC Setup to TCLK Rising	t_{STS}	-125	-	125	ns
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100	-	-	ns
Propagation Delays					
TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}	-	-	75	ns
TCLK Rising to TCHCLK	t_{PTCH}	-	-	75	ns

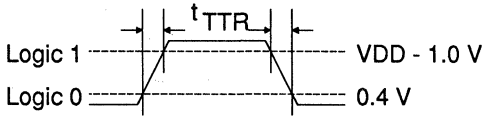
SWITCHING CHARACTERISTICS - RECEIVER

(T_A = -40 to 85 °C; V_{DD} = 5V ± 10%; V_{IH} = 2.0V; V_{IL} = 0.8V; Maximum input rise & fall times of 10 ns)

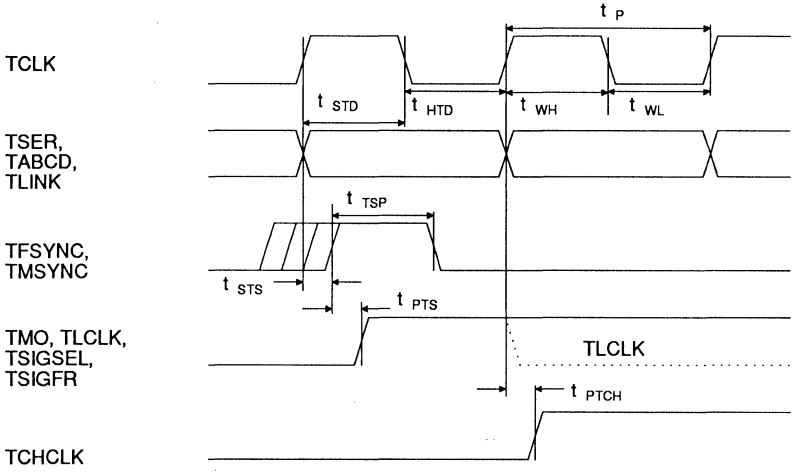
Parameter	Symbol	Min	Typ	Max	Units
Transition Time, All Outputs	t_{TTR}	-	-	20	ns
RCLK Period	t_P	250	648	-	ns
RCLK Pulse Width	t_{WL}, t_{WH}	100	324	-	ns
RCLK Rise & Fall Times	t_R, t_F	-	20	-	ns
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50	-	-	ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50	-	-	ns
Minimum $\overline{RST}$ Pulse Width on System Power Up or Restart	t_{RST}	1	-	-	us
Propagation Delays					
RCLK to RMSYNC, RFSYNC, RSIGSEL RSIGFR, RLCLK, RCHCLK	t_{PRS}	-	-	75	ns
RCLK to RSER, RABCD, RLINK	t_{PRD}	-	-	75	ns
RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}	-	-	75	ns



Rise and Fall Times for RCLK & TCLK.

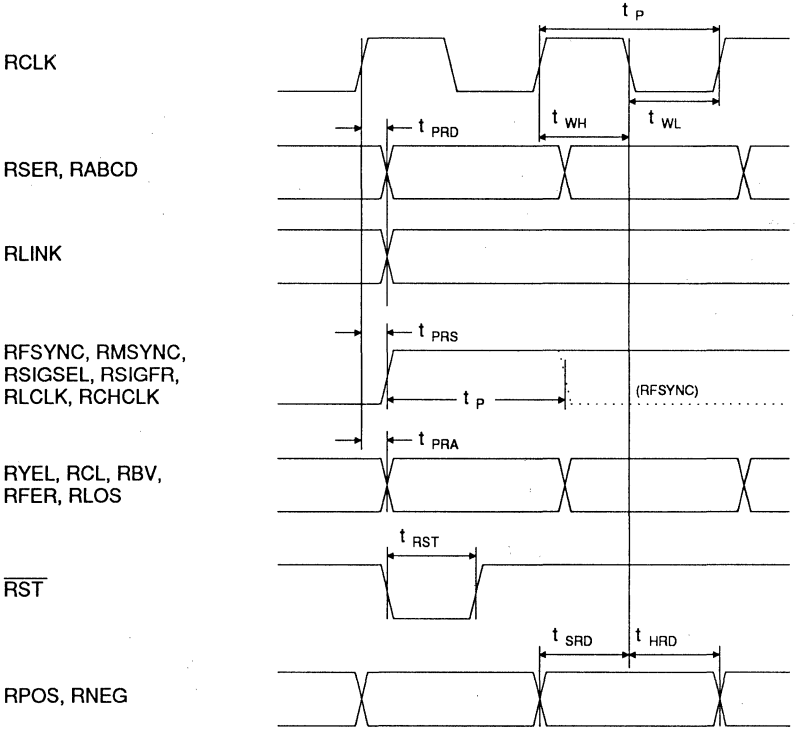


Transition Times for All Receiver Outputs.



Note: TMO, TLCLK, TSIGSEL and TSIGFR are generally coincident with the rising edge of TCLK.

Transmitter Timing



Receiver Timing

GENERAL DESCRIPTION

The CS2180A is a monolithic CMOS circuit that encodes and decodes T1 (1.544 MHz) digital transmission formats for D4 (193S: 12 frames per superframe), and ESF (193E: 24 frames per superframe) framing formats. The CS2180B also encodes and decodes the SLC-96 (SLC: 72 frames per superframe) and DDS T1DM (T1DM: 12 frames per superframe plus unique channel number 24) formats.

Both the CS2180A and the CS2180B provide full support for individual clear channels, bit-robbed signaling, alarm detection and generation, zero suppression, and idle channels. An overview of the 193S, 193E, SLC and T1DM framing formats is provided in the Application section at the end of this data sheet. The device provides independent transmission and reception sides, with a shared serial controller interface for use with a host processor. A hardware mode is also available for operation independent of a host controller. The SLC and T1DM formats can be selected only via the CS2180B serial controller interface.

The serial interface provides access to 16 on-chip control and status registers. The control registers are used to configure global parameters such as the framing format and zero suppression mode, as well as transmitter or receiver specific parameters. A hardware interrupt is provided, which can be configured via interrupt mask and status registers to signal any combination of alarm conditions.

Transmitter commands include enabling external framing bit, CRC, or S-bit insertion, declaring individual DS0 channels clear and/or idle, and enabling yellow and blue alarm modes in different formats. The receiver can be configured to replace individual incoming channels with idle or digital milliwatt (μ-LAW) codes, and a large variety of resync options are provided. Bipolar violations, CRC and framing errors are automatically counted in another set of registers which can be arbitrarily reset via the serial interface to provide variable saturation points. The Receive Status Register (RSR) provides data on all error and alarm conditions, and in conjunction with the Receive Interrupt Mask Register (RIMR), can be configured to signal an interrupt on $\overline{INT}$ in response to any alarm condition.

Note: there are two different naming conventions in practice concerning the numbering of bits within a word. The most common convention in EE and Computer Science is to number the bits as 0 - 7, starting from the LSB. This is the convention used throughout this data sheet when referring to register bits. A different convention is used in the telecom literature when referring to the bits in a digital transmission stream. In this case, they are numbered 1 - 8, *starting from the MSB*. This convention is maintained in this data sheet whenever referring to the bits of a DS0 channel word.

CS2180B ENHANCEMENTS

Enhancements made in the CS2180B include the following. The SLC-96 and DDS T1DM framing formats are supported in host mode. The AIS (Blue Code) detection is made compatible with TR-TSY-000191 requirements (unframed all ones), and a received-blue-alarm output pin is added to the PLCC package. The Receive Carrier Loss detection criteria is made compatible with industry standard requirement of 175 ±75 zeros. The receiver line code decoder is made universal. The decoder will automatically decode either AMI or B8ZS. The CS2180B B8ZS control option controls only the transmitter's encoder. The universal decoder simplifies the provisioning of B8ZS in the network. Lastly, the serial control interface was simplified. When writing data bytes on SDI, it is no longer necessary to have SDI valid for both the rising and falling edges of SCLK. Rather, SDI need be stable only on the rising edge of SCLK.

HOST MODE

Serial Interface

For applications in which the device is to interface with a host processor, the CS2180A and CS2180B can be configured to run in host mode by tying the Serial Port Select pin (SPS) to the +5 V supply (VDD). This allows access to the serial port, providing a large number of configuration options via the 16 on-chip control and status registers.

Serial read/write timing, controlled by SCLK, is entirely independent of the transmit and receive timing. This allows the host microcontroller to monitor the status register and counters, modify configuration options, and issue commands asynchronously with the T1 system. A serial timing overview is provided in Figure 1.

All data transfers are initiated by setting Chip Select ($\overline{CS}$) low. Any read or write to the serial port is initiated by writing an 8-bit command word. The command word consists of 4 separate fields (see Figure 2). When reading from the port, data is output on the falling edge of SCLK, and held until the next falling edge.

CS2180A Only: All data is written to and read from the port LSB first. When writing to the port, input data is not latched, and the device registers are open to the bus during SCLK low. *To avoid transient corruption of the device registers, data must be valid for the entire low period of SCLK.*

CS2180B Only: All data is written to and read from the port LSB first. When writing to the port, SDI input data is sampled on the rising edge of SCLK.

D0 (LSB) is the R/$\overline{W}$ field, and specifies whether the current operation is to be a read or a write: 1 = read, 0 = write. The second 4 bits (D1 - D4) contain the address field. Written LSB first, they specify which of the sixteen registers to access. D5 (Device Select) should be set to zero when addressing the CS2180A or CS2180B. However, if the CS2180A or CS2180B shares the same serial interface lines with a CS61534/35 or CS61574 Line Interface (see Figure 3), D5 will be set to a "1" when addressing the Line Interface device. The CS2180A and CS2180B will ignore any read/write commands with a "1" in D5, allowing both parts to share $\overline{CS}$. D6 is reserved, and must be set to 0 for normal operation.

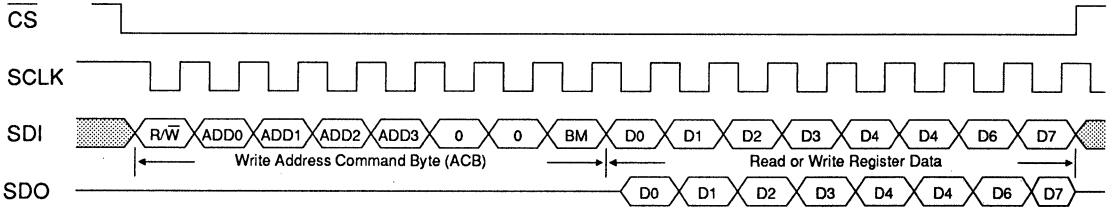


Figure 1. Serial Read/Write Timing

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BM	**0**	**DS**	**ADD3**	**ADD2**	**ADD1**	**ADD0**	**R/W**
0 Individual 1 Burst	Set to "0"	0 CS2180A/B 1 CS Line Dr.	(MSB)	Register Address Field		(LSB)	0 Write 1 Read

Figure 2. Address Command Byte (ACB)

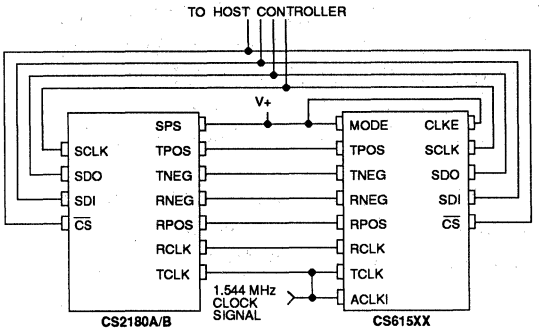


Figure 3. Interfacing with CS61534/35/74 Line Drivers

D7 (MSB) specifies burst mode if set to 1. When using burst mode, the address field of the command word must be "0000", any other value will invalidate the command, and the CS2180A and CS2180B will simply ignore it. This effectively means that the command for a burst write is 80 (hex) and a burst read is 81 (hex).

Burst mode allows the sixteen registers to be consecutively read or written. Writing all registers allows fast initialization at power-up or system reset. (Note that the Receiver Status Register, RSR, is read-only, so a write during burst mode will have no effect.) When using burst mode, registers are read or written in address order, 0000 (RSR) to 1111 (RMR3). Burst mode ends on the first rising edge of $\overline{CS}$. See Table 1 for a complete list of the CS2180A and CS2180B on-chip registers.

ADDR	REGISTER NAME AND DESCRIPTION		(T) TRANSMIT (R) RECEIVE
0000	RSR	**Receive Status Register**- A read only register which reports all active receiver alarm conditions.	R
0001	RIMR	**Receive Interrupt Mask Register** - A mask which allows selection of individual alarm conditions for generation of hardware interrupt	R
0010	BVCR	**Bipolar Violation Count Register** - A bipolar violation alarm is generated after this 8 bit counter surpasses it's user definable limit.	R
0011	ECR	**Error Count Register**- Two separate 4 bit counters, which record OOF errors, and frame bit or CRC errors. Like BVCR, each can be preset to a saturation point.	R
0100	CCR	**Common Control Register** - Selects global configuration options, such as: framing mode, zero suppression, or loopback.	T/R
0101	RCR	**Receive Control Register** - Selects receiver specific options, such as the resync algorithm or insertion of digital milliwatt codes.	R
0110	TCR	**Transmit Control Register** - Selects transmitter specific options, such as alarm generation, clear or idle channel enable, and external S-bit or CRC insertion.	T
0111 1000 1001	TIR1 TIR2 TIR3	**Transmit Idle Registers**- Each bit of the three TIR registers corresponds to an individual DS0 channel. When set, that channel is replaced with an idle code.	T
1010 1011 1100	TTR1 TTR2 TTR3	**Transmit Transparent Registers** - Each bit corresponds to a DS0 channel. When set, that signaling and B7 zero suppression is disabled for that channel.	T
1101 1110 1111	RMR1 RMR2 RMR3	**Receive Mark Registers** - Each bit correponds to a DS0 channel. When set, the channel data is replaced with an idle or digital milliwatt code.	R

Table 1. On-Chip Registers

7 (MSB)	6	5	4	3	2	1	0 (LSB)
FM1	FRSR2	EYELMD	FM	YELS	B8ZS	B7	LPBK
See Fig. 4b	0 B8ZS 1 COFA	0 FDL 1 Bit 2	See Fig. 4b	0 Bit 2 1 S-bit	0 Disable 1 Enable	0 Transparent 1 B7 Stuffing	0 Normal 1 Loopback

Figure 4a. Common Control Register (CCR)

Common Control Register

The Common Control Register (CCR) determines global operating characteristics common to both the transmitter and receiver. It currently provides for selection of the framing mode (193S, 193E, SLC or T1DM), the format of yellow alarms, the zero suppression format (B7 or B8ZS), loopback operation, and control of output to RSR.2. In the CS2180A, CCR.7 is reserved for future use, and should always be set 0 for proper operation. See Figure 4a for an overview of the CCR.

Loopback
CCR.0: LPBK

Setting LPBK (CCR.0) to "1" puts the CS2180A and CS2180B into loopback mode. While in loopback, the output of TPOS/TNEG is internally rerouted directly to the RPOS/RNEG inputs, and an unframed, all "1's" stream is output on TPOS/TNEG. All operating modes, except blue alarm transmission, remain functional during loopback. Note that enabling loopback will usually invoke an out-of-frame (OOF) error until the receiver can resync to the new framing alignment. See the section on the Receive Control Register (RCR) for a description of the resync options available.

Zero Suppression
CCR.1: B7
CCR.2: B8ZS

B7 and B8ZS select the zero suppression mode. Setting B7 (CCR.1) to "1" will enable bit 7 zero substitution. This causes any channel word with all zeros to be transmitted with bit 7 (2nd LSB) forced to a "1". B7 mode only affects the transmitter, the receiver does not decode B7. Note that bit 7 stuffing can be disabled on an individual channel basis for clear channel transmission via the Transmit Transparent Registers TTR1 - TTR3 (see description of transmitter which follows).

7	4	
FM1	FM	Format Selected
0	0	193S (D4)
0	1	193E (ESF)
1	0	SCL-96 (CS2180B only)
1	1	T1DM (CS2180B only)

Figure 4b. Framing Format Selection

B8ZS coding operates independent of channel boundaries, and is transparent to all other functions. When using B8ZS, the final transmission stream is examined before transmission, and any eight consecutive zeros will be replaced with a B8ZS code word before transmission.

CS2180A Only: If B8ZS (CCR.2) is set to a "1", B8ZS zero substitution will be enabled in both the transmitter and receiver. Incoming B8ZS codes will be intercepted by the receiver and replaced with 8 zeros before being processed by the rest of the receive side.

CS2180B Only: If B8ZS (CCR.2) is set to a "1", B8ZS zero substitution will be enabled in the transmitter. Independent of the setting of CCR.2, any incoming B8ZS codes will be intercepted by the receiver and replaced with 8 zeros before being processed by the rest of the receive side. The receiver is always capable of receving either AMI or B8ZS encoded data.

Note: For T1DM, CCR.1 and CCR.2 should be set to a "0" since DDS equipment assures a 1-in-8 one's density.

193S Yellow Alarm Format
CCR.3: YELS

The CS2180A and CS2180B supports two different yellow alarm formats for 193S framing. Whichever format is selected, it will be used by both the transmit side, for yellow alarm generation, and the receive side, for alarm detection.

When using 193S framing, a "0" in YELS (CCR.3) will encode/decode yellow alarms as a "0" in bit 2 (2^{nd} MSB) of all channels. Setting CCR.3 to "1" will cause yellow alarms to be encoded/decoded as a "1" is the S-bit position of frame 12. Either setting is only effective when using 193S framing.

Note: for T1DM, CCR.3 should be set to a "0".

Framing Format
CCR.4: FM
CCR.7: FM1

As shown in Figure 4b, CCR.4 and CCR.7 select the framing format. Note that in the CS2180A, CCR.7 must be set to "0", and the SLC-96 and T1DM formats are not available. See the text for the Transmit Control Register (TCR) and Receive Control Register (RCR) for further information on the particular options available for each framing format.

193E Yellow Alarm Format
CCR.5: EYELMD

The CS2180A and CS2180B supports two different yellow alarm formats for 193E framing. Whichever format is selected, it will be used by both the transmit side, for yellow alarm generation, and the receive side, for alarm detection.

When using 193E framing, a "0" in EYELMD (CCR.5) will encode/decode yellow alarms as a repeating sequence of 00FF (hex) on the 4 kHz facility data link (FDL). If CCR.5 is set, 193E yellow alarms will be handled as a "0" in bit 2 (2^{nd} MSB) of all channels.

Control of RSR.2
CCR.6: FRSR2

CCR.6 allows you to change the meaning of D2 in the Receive Status Register (RSR.2). If CCR.6 is clear, RSR.2 will report the detection of B8ZS codes in the received T1 input. If CCR.6 is set to a "1", RSR.2 will be used to signal a Change of Frame Alignment (COFA). A COFA is reported when the last receiver resync resulted in a change of framing or multiframing alignment. Refer to the description of the Receive Status Register for further information.

TRANSMITTER

The transmit sides of the CS2180A and CS2180B have three types of inputs, the clock, sync, and data inputs. Control is handled through the serial port in host mode, and through the mode control pins in hardware mode (see the last section for a description of hardware mode operation).

Input Data

None of the data inputs are buffered, so the data at each input must be available at the appropriate time for the CS2180A and CS2180B to multiplex into the output stream. All inputs are sampled on the falling edge of TCLK. The delay from input to output is 10 TCLK cycles.

NRZ data for DS0 channels is input on TSER. Framing bits (F_T or FPS bits) and CRC data may either be generated internally or supplied by the host system. If this data is to be externally supplied, it must be inserted into the DS0 input stream at the appropriate frames and input via TSER.

S-bits may be generated internally, or externally provided via TLINK. FDL bits are always provided externally on TLINK. Bit-robbed signaling, when enabled, is always sampled at TABCD. The CS2180A and CS2180B muxes in data from these 3 sources (TSER, TLINK, and TABCD) automatically depending on the transmitter configuration.

Output Data

The completed T1 data stream, ready for line transmission, is output on TPOS/TNEG. For operation with the CS6152, CS61534, CS61535, CS6158, CS6159 or CS61574 line interfaces, output can be set to dual-unipolar format by clearing bit 7 of the Transmit Control Register (TCR.7). TCR.7 should be set to a "1" for operation with the CS61544. In this configuration, the data will be output on TPOS in NRZ format, and TNEG will remain low. When operating in hardware mode, output defaults to the dual-unipolar format. TPOS and TNEG may not be tied together, so an external OR gate is recommended if NRZ output is required while in hardware mode.

Frame/Multiframe Synchronization

The CS2180A and CS2180B maintain timing for frame and multiframe alignment with internal counters driven by TCLK. The timing signals generated by those counters are output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK. These counters determine when the CS2180A and CS2180B will insert F-bits and sample external signaling data. The frame and multiframe counters can be reset independently via TMSYNC and TFSYNC. If left to run without a sync pulse, the CS2180A and CS2180B will arbitrarily choose a framing alignment.

A low to high transition of TMSYNC, occurring near the rising edge of TCLK, resets the CS2180A's and CS2180B's counters to mark the bit-period concurrent with the next falling edge of TCLK as the F-bit of the first frame of a new superframe. All other timing will be set to match the superframe alignment automatically. TMSYNC may be pulsed once at start-up and left low, or left running in sync with superframe timing.

A low to high transition of TFSYNC, occurring near the rising edge of TCLK, resets the CS2180A's and CS2180B's counters to mark the bit-period concurrent with the next falling edge of TCLK as the F-bit of a new frame. If TMSYNC is used to set superframe alignment, frame alignment will also be set, and TFSYNC may be tied low. There is, of course, no harm in using both TMSYNC and TFSYNC together, as TFSYNC has no effect on multiframe alignment if it is in sync. If, however, TFSYNC is used out of sync with TMSYNC, the superframe alignment will be moved forward by the least number of bits necessary to be in alignment with the new frame boundary.

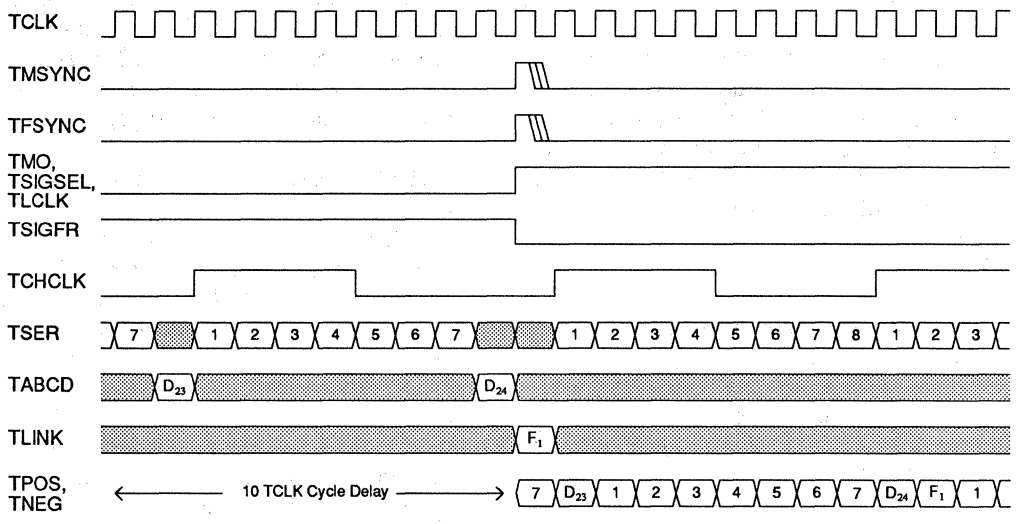


Figure 5. Bit Level Transmit Timing (193E, signaling enabled)

Figure 5 shows the bit-level timing (with signalling enabled). Note that the delay from input to output is 10 TCLK cycles. TCHCLK transitions high at the beginning of every DS0 channel (50% duty cycle).

193S Timing

Frame and multiframe timing is output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK. TMO transitions high at the beginning of every superframe (50% duty cycle). TSIGFR goes high during signaling frames (every 6 frames). TLCLK is a 4 kHz clock for the TLINK input. TLCLK goes high during odd frames (external S-bit insertion).

TSIGSEL runs at twice the frequency of TMO. Logical combination of TMO and TSIGSEL provides a way to distinguish the 6^{th} and 12^{th} frames for external multiplexing of signaling channels. TMO is high for channel A, and low for B. See Figure 6 for timing diagram.

193E Timing

Frame and multiframe timing is output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK. TMO transitions high at the beginning of every superframe (50% duty cycle). TSIGFR goes high during signaling frames (every 6 frames). TLCLK is a 4 kHz clock for the TLINK input. TLCLK goes high during odd frames (FDL insertion).

TSIGSEL runs at twice the frequency of TMO. Logical combination of TMO and TSIGSEL provides a way to distinguish the 6th, 12th, 18th, and 24th frames for external multiplexing of signaling channels. TMO is high for channels A and B, and TSIGSEL is high for channels A and C. See Figure 7 for timing diagram.

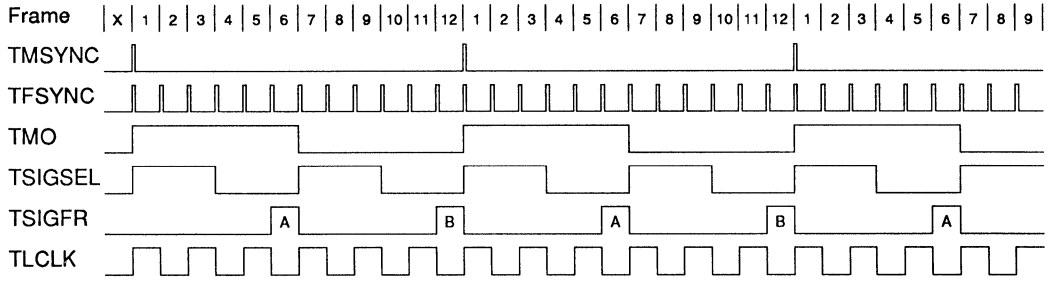


Figure 6. 193S Multiframe Transmit Timing

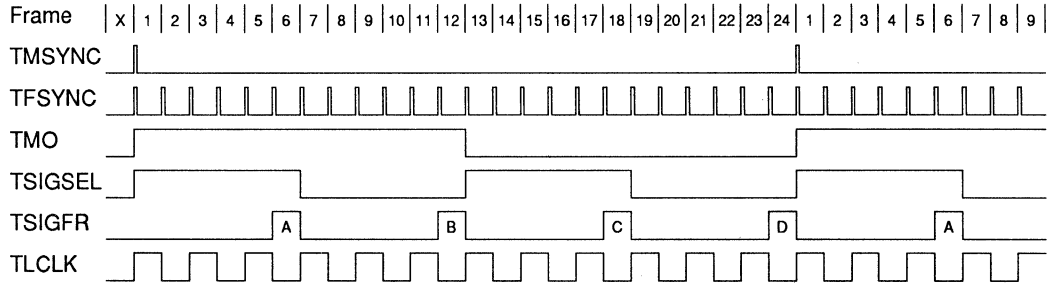


Figure 7. 193E Multiframe Transmit Timing

SLC-96 Timing

Figure A6 of the Application Section, shows the SLC-96 superframe structure. Note that in Figure A6, the first C bit (C1) resides in frame 12. A low to high transition of TMSYNC identifies Frame 1 of Figure A6.

Frame and multiframe timing is output on TCHCLK, TMO, TSIGSEL, TSIGFR and TLCLK. TSIGSEL can be used to identify the location of the DL bits. The TSIGSEL output is high during frames 58 to 11, and is low during frames 12 to 57. When TSIGSEL is low, the CS2180B accepts DL bits on TLINK at a 4 kHz rate, The DL bits which are input on TLINK are: C1-C11, DC, DC, DC, M1-M3, A1, A2, S1-S4. "DC" signifies "don't care" bits. The DC-bit positions correspond to the spoiler bits. The CS2180B internally generates the spoiler bits. The data input on TLINK in the DC position is ignored by the CS2180B. TLCLK is a 4 kHz clock for the TLINK input. TLCLK goes high during odd frames.

TMO transitions high at the beginning of every 12th frame. TSIGFR goes high during signaling frames (every 6 frames). The rising edge of TMO identifies the 6^{th} frame, and the falling edge of TMO identifies the 12^{th} frame for external multiplexing of signaling channels. See Figure 8 for timing diagram.

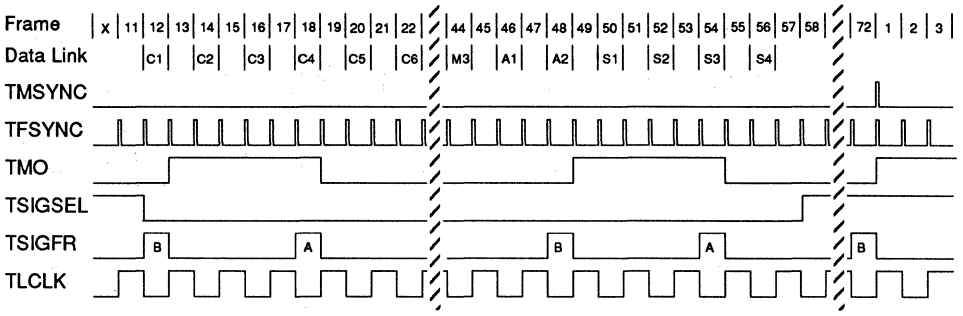


Figure 8. SLC-96 Multiframe Transmit Timing

T1DM Timing

Frame and multiframe timing is output on TCHCLK, TMO, and TLCLK. TMO transitions high at the beginning of every superframe (50% duty cycle). TSIGFR goes high during signaling frames (every 6 frames).

The channel 24 data link is input on TLINK using TLCLK. TLCLK is a 8 kHz clock with a duty cycle of 1 bit period high per frame. When TLCLK is high, TLINK will be sampled on the falling edge of TCLK. See Figure 9 and "Switching Characteristics - Transmitter" for timing diagrams.

TSIGSEL and TSIGFR serve no purpose in the T1DM mode and can be ignored. However, TSIGSEL and TSIGFR operate as in 193S mode.

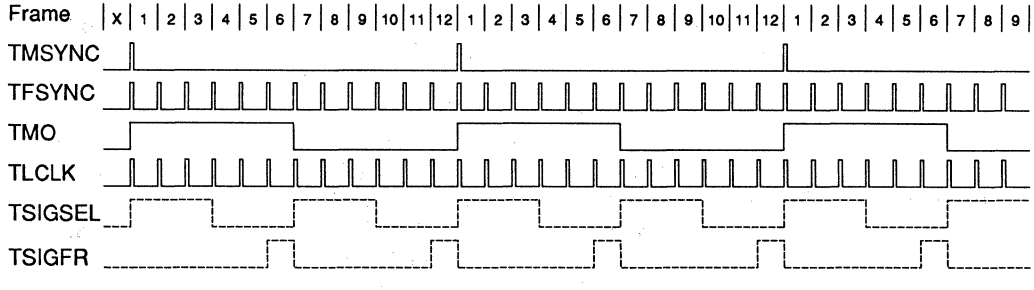


Figure 9. T1DM Multiframe Transmit Timing

7 (MSB)		6		5		4		3		2		1		0 (LSB)	
ODF		TFPT		TCP		RBSE		TIS		193SI		TBL		TYEL	
0	Bipolar	0	Internal	0	Internal	0	Disabled	0	7F (Hex)	0	Internal	0	Normal	0	Normal
1	NRZ	1	External	1	External	1	Enabled	1	FF (Hex)	1	External	1	Blue Alarm	1	Yel. Alarm

Figure10. Transmit Control Register (TCR)

Transmitter Control Register (TCR)

When in host mode, there are a number of options available for transmitter configuration which can be enabled via the Transmit Control Register (TCR), Transmit Transparent Registers (TTR1 - TTR3), and Transmit Idle Registers (TIR1 - TIR3). Serial read and write operations to access these registers are explained in the *Serial Interface* section above. When operating in hardware mode, all control bits in the TCR default to "0" (except TCR.4, which defaults to "1" to enable bit-robbed signaling), and dynamic control is limited to the mode control pins as described under hardware mode below.

The TCR provides control to enable bit-robbed signaling, external framing bit, CRC, or S-bit insertion, and yellow and blue alarm modes. It also provides for two different idle code formats, and selection of bipolar or NRZ output. Figure 10 shows an overview of the Transmit Control Register.

Transmit Yellow Alarm
TCR.0: TYEL

Setting TYEL (TCR.0) to a "1" causes the CS2180A and CS2180B to automatically generate and transmit a yellow alarm in the appropriate format. In 193S mode the yellow alarm format used will be determined by the setting of CCR.3. In 193E mode, the yellow alarm format will be determined by the setting of CCR.5. See Common Control Register, above, for description of the available yellow alarm formats for 193S and 193E modes. In SLC mode, the CS2180B does not generate the yellow alarm code. rather, the user transmits the SLC-96 yellow alarm via the data link. In T1DM mode, the yellow alarm is transmitted in bit 5 of channel 24 (and CCR.3 should be set to a "0"). Clearing TCR.0 disables yellow alarm transmission.

Transmit Blue Alarm
TCR.1: TBL

Setting TBL (TCR.1) to a "1" generates a blue alarm; an unframed sequence of all "1's". If a framed, all "1's" signal is required, an FF (hex) idle code may be output on all channels via appropriate settings of TCR.3 and the TIR registers (see Transmit Idle Code Select below). Blue alarm (Alarm Indication Signal, or AIS) overrides all other transmission data, and a blue alarm is automatically output during loopback. Clearing TCR.1 disables blue alarm transmission.

193S, SLC and T1DM S-bit Insertion
TCR.2: 193SI

TCR.2 is applicable to 193S, SLC and T1DM modes, but not to the 193E mode.

In the 193S and T1DM modes, setting 193SI (TCR.2) to a "1" allows the S-bit (all even F-bits) to be externally supplied via TLINK. When TCR.2 is clear, the S-bit will be internally generated.

In the SLC mode, setting 193SI (TCR.2) to a "1" allows the S-bit (selected even F-bits) to be externally supplied via TLINK, and the user must input all Fs, spoiler and DL bits. When TCR.2 is clear, the CS2180B generates the SLC-96 spoiler bits and Fs bits, and the user inputs all other DL bits on TLINK using TLCLK.

Note: when using internal S-bit generation (TCR.2 = 0) in conjunction with external FT bit insertion (TCR.6 = 1), the CS2180A and CS2180B will logically 'OR' the value at TSER with the internally generated value. This means that the data on TSER during S-bit periods should always be "0" to avoid corrupting the generated FS pattern.

Transmit Idle Code Select
TCR.3: TIS

Individual DS0 channels can be replaced with idle codes by setting the corresponding bits in the Transmit Idle Registers (TIR1 - TIR3) described below. TIS (TCR.3) selects which of two codes to use. A "0" in TCR.3 will cause a 7F (hex) to be inserted into the channels specified in the TIR. Setting TCR.3 to a "1" will select an FF (hex) code. By asserting all 24 channels idle in the TIR, this setting can be used to generate a "framed" blue alarm. Whichever mode is selected, bit-robbed signaling will still effect idle channels unless they are programmed clear (see *Transmit Transparent Registers*, below).

Robbed Bit Signaling Enable
TCR.4: RBSE

A "0" in RBSE (TCR.4) will disable bit-robbed signaling. Setting TCR.4 to a "1" will enable signaling in all channels. In this mode, data on TABCD is inserted into the LSB of all DS0 channels during signaling frames. For mixed voice and data transmission, individual DS0 channels can be programmed clear by setting the corresponding bits in the Transmit Transparent Registers (TTR1 - TTR3) described below.

CRC Pass-through
TCR.5: TCP

In 193E framing mode, the CRC bits (F-bit of frames 2, 6, 10, 14, 18, and 22) may be either generated internally, or supplied by the user. Clearing TCP (TCR.5) causes the CS2180A and CS2180B to generate and insert the CRC bits automatically. If TCR.5 is set to a "1", data for the CRC channel may be externally supplied. When using this mode, CRC bits are sampled from TSER, and must be externally multiplexed into the DS0 channel data at the F-bit times of CRC frames.

FT/FPS Pass Through
TCR.6: TFPT

When TFPT (TCR.6) is clear, the framing bits for 193S, T1DM and SLC (FT), or 193E (FPS) are generated internally and automatically inserted into the outgoing data stream. Setting TCR.6 to a "1" allows the framing bits to be externally provided. When using this mode, framing bits are sampled from TSER, and must be externally multiplexed into the DS0 channel data at the F-bit times of the appropriate frames. See note under TCR.2, above.

Output Data Format
TCR.7: ODF

ODF (TCR.7) allows the format of the output data at TPOS/TNEG to be set to either dual-unipolar or NRZ format. Clearing TCR.7 selects for dual-unipolar format on TPOS/TNEG. Setting TCR.7 to a "1" causes data to be output on TPOS in NRZ format, and TNEG is held low. When operating in hardware mode, output defaults to the dual-unipolar format. TPOS and TNEG may not be tied together, so an external OR gate is recommended if NRZ is required while in hardware mode.

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
TTR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
TTR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
TTR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

"0" = Normal "1" = Corrsponding DS0 Channel is Transparent. (No Signaling or B7 Insertion.)

Figure11. Transmit Transparent Registers (TTR1 - TTR3)

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
TIR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
TIR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
TIR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

"0" = Normal "1" = Corrsponding DS0 Channel is Replaced with Idle Code. (See TCR.3)

Figure 12. Transmit Idle Registers (TIR1 - TIR3)

3

Transmit Transparent Registers (TTR)

The Transmit Transparent Registers allow individual DS0 channels to be programmed clear, disabling robbed bit signaling and B7 zero suppression for that channel (if selected, B8ZS is unaffected by transparent channels). There are 3 TTR registers: TTR1, TTR2, and TTR3. Each bit in the TTR registers corresponds to a DS0 channel: TTR1.0 = channel 1, TTR1.7 = channel 8, TTR2.7 = channel 16, etc. A channel is programmed clear by setting the bit which corresponds to that channel in the appropriate TTR register. See Figure 11.

Transmit Idle Registers (TIR)

By setting the appropriate bits in the Transmit Idle Registers, individual DS0 channels can be replaced with the idle code selected via TCR.3 (see above). If the idle channel is not also programmed clear (via TTR1 - TTR3), the code may be corrupted during signaling frames if robbed bit signaling is enabled (TCR.4 = 1). There are 3 TIR registers: TIR1, TIR2, and TIR3. Each bit in the TIR registers corresponds to a DS0 channel: TIR1.0 = channel 1, TIR1.7 = channel 8, TIR2.7 = channel 16, etc. A channel is programmed idle by setting the bit which corresponds to that channel in the appropriate TIR register. See Figure 12.

Transmission Insertion Hierarchy

Figures 13a - 13c give an overview of the decision hierarchy which determines the final composition of the output stream. It shows the various control options as inputs into decision branches of the flow chart, and the order in which the various optional signals are muxed into the final data stream.

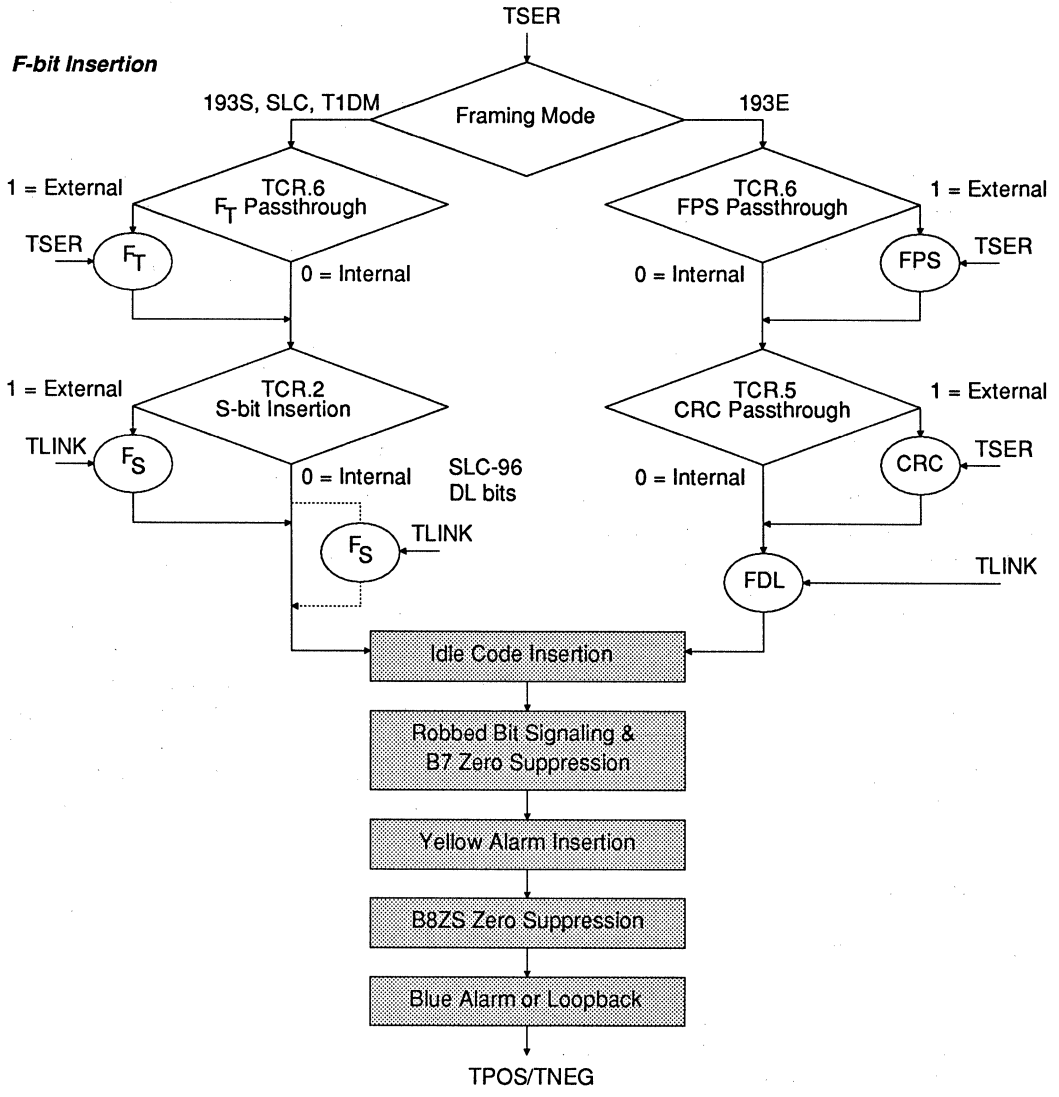


Figure 13a. Transmit Insertion Hierarchy: Framing Bits

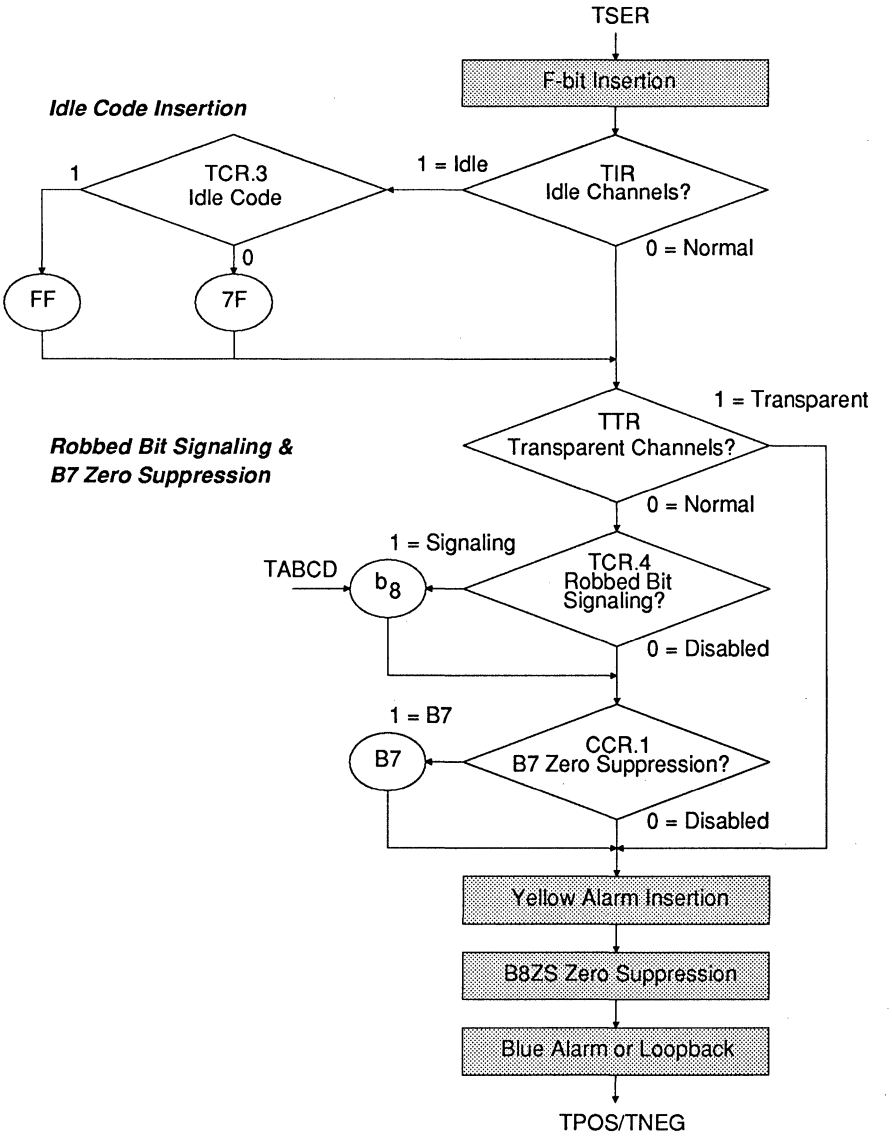


Figure 13b. Transmit Insertion Hierarchy: Idle Codes, Signaling, and B7

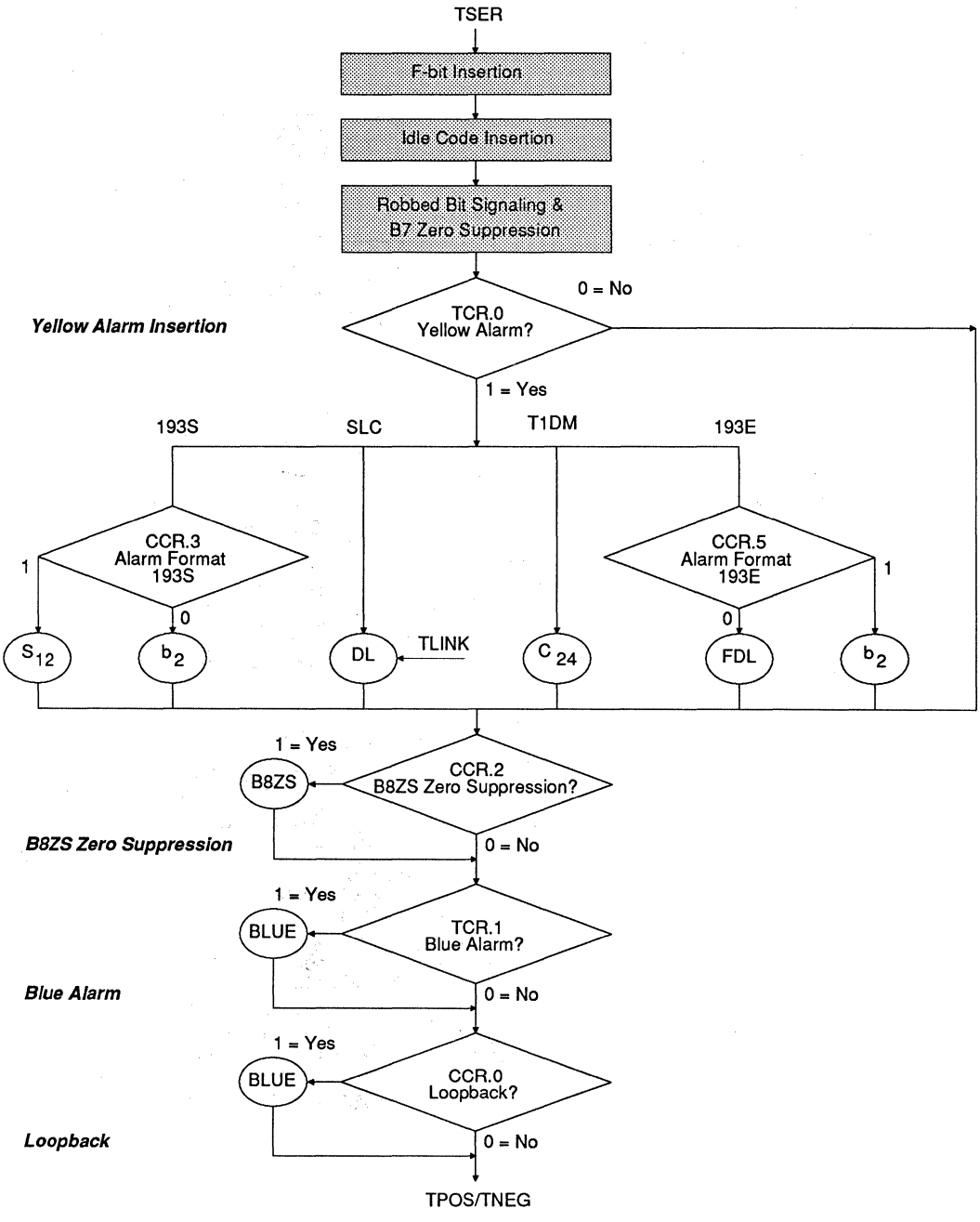


Figure 13c. Transmit Insertion Hierarchy: Alarms, B8ZS, and Loopback

RECEIVER

The receive sides of the CS2180A and CS2180B have only three inputs: the clock (RCLK), the incoming signal (RPOS/RNEG), and a reset pin ($\overline{RST}$). The receiver determines the framing synchronization of the incoming data, and outputs the timing information on the six timing clocks: RLCLK, RCHCLK, RFSYNC, RMSYNC, RSIGFR, and RSIGSEL. Alarms and error conditions are recorded in the Receive Status Register, and output in real time on the five status pins: RYEL, RCL, RBV, RFER, and RLOS. The decoded data is separated into it's component channel, link, and signaling components and output on RSER, RLINK, and RABCD respectively.

When in host mode, the Receive Control Register allows control of the sync algorithm, and insertion of idle or digital milliwatt (μ-LAW) codes into individual DS0 channels. The internal error counters can be accessed, and the Interrupt Mask Register can be programmed to specify the conditions under which a hardware interrupt is generated on $\overline{INT}$. When running in hardware mode, receiver status can still be monitored on the status pins; and access to the error counters, sync algorithm, interrupt mask, and the insertion of idle codes are disabled.

Input Data

The receiver accepts the incoming T1 stream via RPOS/RNEG in dual-unipolar format. Tying RPOS/RNEG together disables the bipolar violation alarm and allows reception of data in NRZ format. Input data is sampled on the falling edge of RCLK. Delay from input at RPOS/RNEG to output on RSER is 13 RCLK periods.

Output Data

The receiver will attempt to sync and decode the framing format selected via CCR.4 and CCR.7. The decoded T1 stream is output in NRZ format on RSER, and updated every RCLK period. Output data is latched on the rising edge of RCLK, and held until the next update. Delay from input at RPOS/RNEG to output on RSER is 13 RCLK periods.

Link and signaling data is always output on RLINK and RABCD respectively, independent of the transmitter configuration. RABCD outputs the LSB of every DS0 channel word, whether it is currently a signaling frame or not. The data is updated on the channel boundary, concurrent with the MSB, and held until the next update (8 or 9 bits). RLINK outputs either S-bit, SLC DL or FDL bits, depending on the framing format. Data is updated 1 bit period prior to the Fs or FDL frame and held until the next update (2 frames).

Output Clocks

Several timing clocks are provided for identifying this data. The timing clocks are RLCLK, RCHCLK, RFSYNC, RMSYNC, RSIGFR, and RSIGSEL. Logical combination of these six signals allows easy extraction of any part of the received data stream. RMSYNC runs on a 50% duty cycle, and transitions high at the start of each new superframe output on RSER. RFSYNC transitions high at the start of every new frame. Individual DS0 channels are identified by RCHCLK, which runs on a 50% duty cycle and transitions high at the MSB of every individual time slot. Bit level timing is shown in Figure 14.

193S Timing

Link data can be identified by RLCLK, which goes high for all odd numbered frames. RSIGFR is high for signaling frames, and low at all other times. RSIGSEL runs at twice the frequency of RMSYNC. Logical combination of RMSYNC and RSIGSEL provides a way to distinguish the 6^{th} and 12^{th} frames for external multiplexing of signaling channels. RMSYNC is high for those frames containing A signaling bits, and low for frames containing B bits. Refer to Figure 15 for a timing diagram.

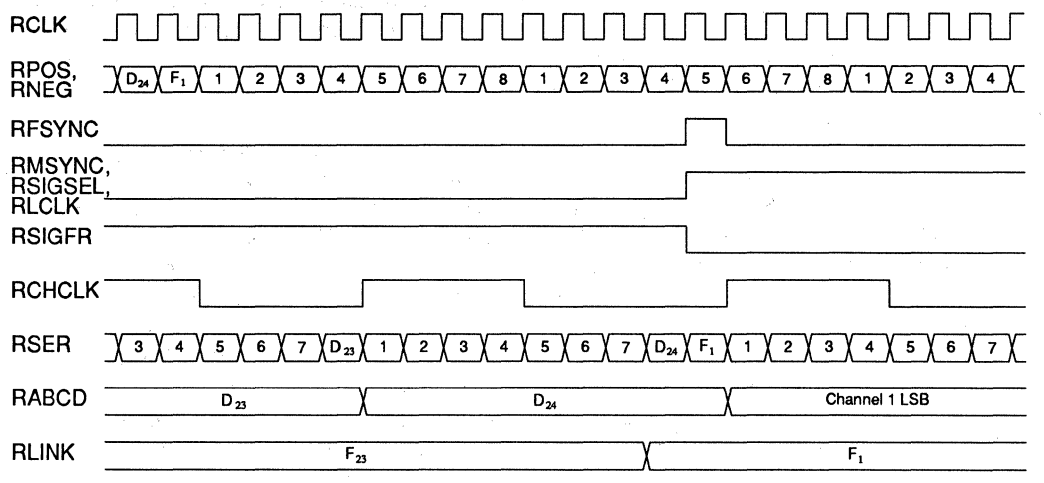


Figure 14. Bit Level Receive Timing (193E mode)

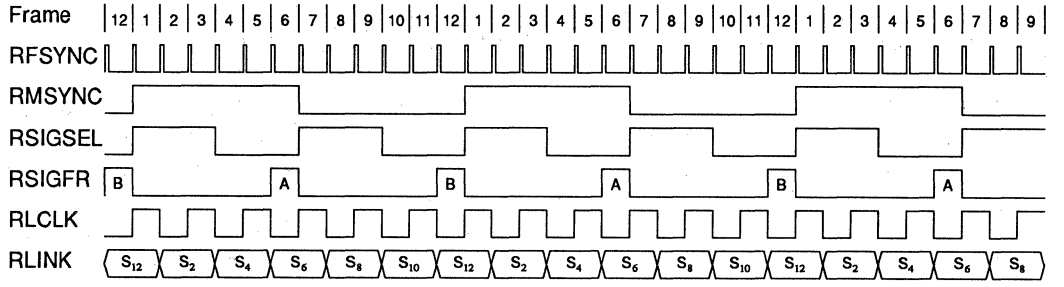


Figure 15. 193S Multiframe Receive Timing

193E Timing

Link data can be identified by RLCLK, which goes high for all odd numbered frames. RSIGFR is high for signaling frames, and low at all other times. RSIGSEL runs at twice the frequency of RMSYNC. Logical combination of RMSYNC and RSIGSEL provides a way to distinguish the 6^{th}, 12^{th}, 18^{th}, and 24^{th} frames for external multiplexing of signaling channels. RMSYNC is high for frames containing A and B signaling bits, and RSIGSEL is high for frames with A and C bits. Refer to Figure 16 for a timing diagram.

SLC-96 Timing

The CS2180B will output 36 bits of the DL on RLINK using RLCLK. RSIGSEL can be used to locate the DL bits. RSIGSEL will be held high in those frames where Fs bits and the last spoiler bit are present (frames 58 to 11). RSIGSEL is held low in all other frames (frames 12 to 57). RSIGFR is high for signaling frames, and low at all other times. RMSYNC is high for frames containing A signaling bits, and low for frames containg B bits. Refer to Figure 17 for a timing diagram.

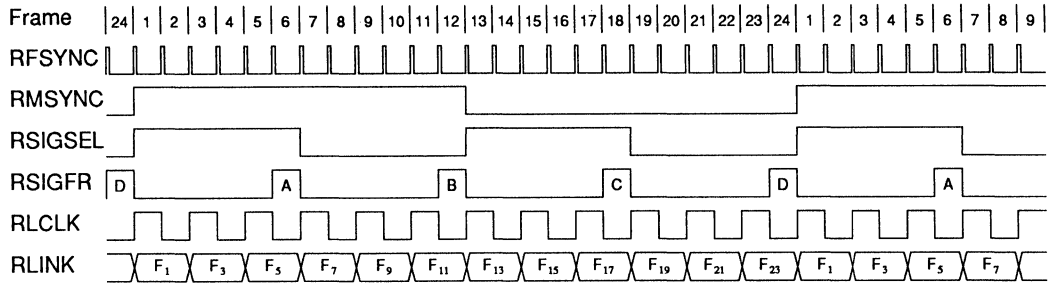


Figure 16. 193E Multiframe Receive Timing

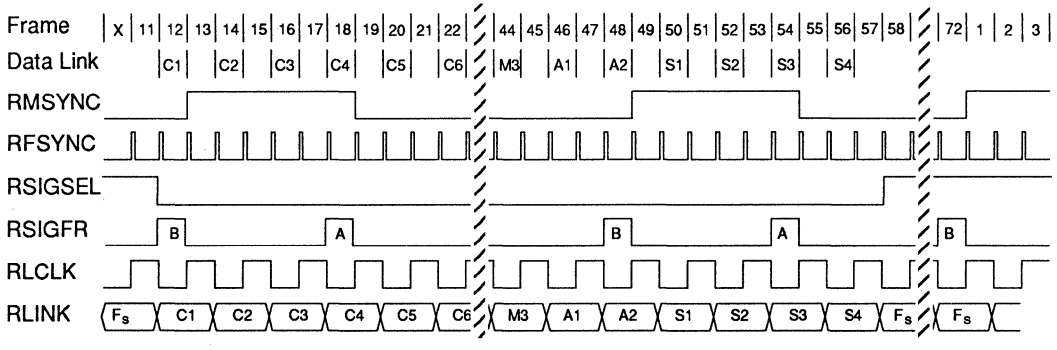


Figure 17. SLC-96 Multiframe Receive Timing

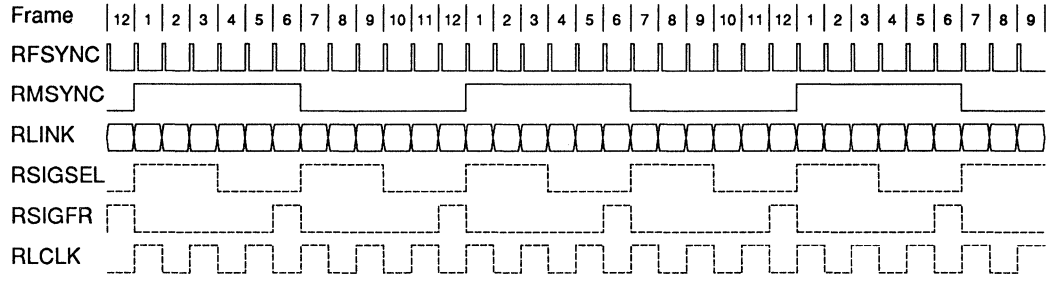


Figure 18. T1DM Multiframe Receive Timing

T1DM Timing

The 8 kHz link data can be sampled on RLINK using the falling edge of RFSYNC. Refer to Figure 18 and "Switching Characteristics–Receiver" for timing diagrams. RSIGFR, RSIGSEL and RLCLK serve no purpose in the T1DM mode and may be ignored.

7 (MSB)	6	5	4	3	2	1	0 (LSB)
ARC	OOF	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC
0 OOF/RCL	0 2 out of 4	0 Disabled	0 Idle (7F)	0 Ft/FPS only	0 10 bits	0 Autoresync	rising edge
1 OOF only	1 2 out of 5	1 Enabled	1 Milliwatt	1 Fs/CRC	1 24 bits	1 Disabled	triggered.

Figure 19. Receive Control Register (RCR)

Receive Control Register (RCR)

The RCR provides for insertion of either idle or digital milliwatt codes, and has six different control bits which enable a large number of options for tailoring the receiver resync behavior. Refer to Figure 19 for an overview of the RCR.

Receive Code Select/Insert
RCR.4: RCS
RCR.5: RCI

When enabled via RCI (RCR.5), the Receive Mark Registers are used to select individual DS0 channels for insertion of idle or digital milliwatt codes, as selected via RCS (RCR.4). There are three RMR registers: RMR1, RMR2, and RMR3 (Figure 20). Each bit in the RMR registers corresponds to a received DS0 channel: RMR1.0 = channel 1, RMR1.7 = channel 8, RMR2.7 = channel 16, etc. A channel is marked for code insertion by setting the bit which corresponds to that channel in the appropriate RMR register. When RCR.5 is clear, code insertion is disabled, and the contents of the RMR registers are ignored.

RCS (RCR.4) selects whether to insert an idle code, or a digital milliwatt code, into the individual DS0 channels marked in the three Receive Mark Registers (RMR1 - RMR3). Clearing RCR.4 will select for an idle code (7F hex) to be inserted into marked channels. Setting RCR.4 to a "1" will cause a digital milliwatt code (μ-LAW format) to be inserted into all marked channels.

Receiver Synchronization

The receiver monitors the incoming signal for loss of frame or multiframe alignment. Unless auto resync has been disabled via RCR.1 (see below), the receiver will automatically initiate a search for the correct framing alignment when loss of synchronization is detected, and RLOS (pin 39) will go high until a new framing alignment is declared.

When the receiver initiates an auto resync, RSIGFR is held low, but all other output timing will continue in the old alignment until the new framing is found. When the new framing alignment is qualified, the output timing will change to the new alignment at the beginning of the next superframe, and RLOS will return low one bit period before the F-bit of the second frame.

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
RMR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
RMR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
RMR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

"0" = Normal "1" = Corrsponding DS0 Channel is Replaced with Idle or Digital Milliwatt Code. (See RCR.4 and RCR.5)

Figure 20. Receive Mark Registers (RMR1 - RMR3)

A receiver resync has no effect on the transmit side timing or configuration, and behavior of the output timing and RLOS pin is the same as that for an auto resync described above. This is in contrast to a reset initiated via the $\overline{RST}$ pin, which clears all internal registers on the falling edge, including the transmit side registers, resets the output timing while $\overline{RST}$ is low, and then initiates a receiver resync on the rising edge.

The time it takes the receiver to resync depends on resync algorithm selected via RCR.2 and RCR.3. The remaining bits in the RCR (1, 6, and 7) determine under what conditions an automatic resync will be initiated.

Forced Resync
RCR.0: RESYNC

RESYNC (RCR.0) can be used to force a receiver resync. Toggling RCR.0 will initiate a resync immediately on the rising edge. It must then be cleared and set again to initiate another resync. Toggling RCR.0 when going into loopback mode will force the receiver to resync to the new frame alignment immediately. This is faster than waiting for the internal hardware to recognize an out-of-frame (OOF) condition and initiating an automatic resync.

Auto Resync Conditions
RCR.1: SYNCE
RCR.6: OOF
RCR.7: ARC

SYNCE (RCR.1) can be set to a "1" to completely disable automatic resync. If RCR.1 is clear, a resync will automatically be initiated when the conditions specified by RCR.6 and RCR.7 are detected.

OOF (RCR.6) specifies how many framing bits (F_T or FPS channels only) must be in error before the receiver declares an out-of-frame (OOF) condition. A resync is always initiated (unless disabled) when an OOF is detected. If RCR.6 is clear, an OOF is declared if 2 out of 4 F_T or FPS bits are in error. If RCR.6 is set to a one, an OOF is declared if 2 out of 5 framing bits are errored. Note that the setting of RCR.6 also effects the reporting of OOF events to the Receive Status Register (RSR) and Error Count Register (ECR). Refer to the appropriate sections below for details.

ARC (RCR.7) declares whether the receiver will initiate a resync on an OOF event only, or resync on both OOF and carrier loss (RCL). If RCR.7 is cleared, the receiver will commence resync upon detection of either an OOF event (as defined by RCR.6 above), or an RCL. If RCR.7 is set, the receiver will only resync in response to an OOF condition.

Resync Algorithm
RCR.2: SYNCT
RCR.3: SYNCC

SYNCT (RCR.2) allows you to declare how many bits must be qualified in the framing pattern before the receiver declares synchronization. When RCR.2 is clear, 10 consecutive F_T or FPS framing bits must be qualified. Setting RCR.2 to a "1" requires the CS2180A and CS2180B to qualify 24 consecutive F_T or FPS framing bits before declaring synchronization.

SYNCC (RCR.3) allows you to modify the algorithm employed to search for and qualify the framing alignment. There are two different qualifying conditions available for each framing mode (193S or 193E), and the meaning of RCR.3 depends on which framing mode has been selected via CCR.4.

193S Resync

When operating with the 193S framing format, RCR.3 selects whether or not the CS2180A and CS2180B will qualify the F_S bits during resync. If a non-standard S-bit pattern is being used, clearing RCR.3 will enable the device to first

search for the F_T framing pattern to find frame alignment, and then only reset multiframe alignment if the F_S pattern can be found. This means that if a valid F_S pattern is not found, synchronization will be declared anyway, and the multiframe alignment indicated by RMSYNC may be false. The S-bits output on RLINK can be used to decode framing externally in such applications.

When using standard F_S signaling, setting RCR.3 to a "1" will cause the device to cross check the F_T and F_S patterns to find sync, and both patterns must be valid before sync is declared. Note that in either setting, S-bit format yellow alarms are recognized by the synchronizer if they have been selected by setting CCR.3.

193E Resync

Clearing RCR.3 while in 193E mode will cause the CS2180A and CS2180B to use only the FPS framing pattern when looking for a valid framing alignment. If RCR.3 is set, the device will attempt to qualify the CRC bits after a candidate alignment has been found. If the CRC codes match, then the new alignment will be declared, if not, the device will try two more times. If the third CRC code does not qualify, then the device will start a new resync procedure and continue in this manner until a framing alignment can be verified with the CRC codes.

Note that after 24 ms, if there are still multiple candidates for framing alignment, the device will test the CRC codes to eliminate false candidates regardless of the setting of RCR.3. After the framing alignment has been found, it takes about 9 ms for the device to check the CRC codes for the first superframe. If that superframe fails, it takes about 3 ms to check each additional CRC code.

SLC-96 Resync

When operating with the SLC-96 framing format, the receiver should be programmed for F_S/F_T cross-coupling (RCR.3=1) and for minimum resync time (RCR.2=0). This causes the CS2180B to sync on 12 valid F_S/F_T bits in frames 60 through 10, and prevents false synchronization to data link and/or spoiler bits.

T1DM Resync

Resync is based upon the 6-bit sync word in channel 24. Once the sync word is recognized, 6 consecutive frames with the correct sync word and F_S/F_T bits are required before declaring synchronization. RCR.2 must be set to "0". RCR.3 is ignored. When frame synchronization is declared, RLOS goes low and RFSYNC is output concurrent with the f-bits. However, the superframe output clocks (RMSYNC, RSIGFR and RSIGSEL) are held low for an additional short period of time until superframe synchronization is found.

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
	BVCS	**ECS**	**RYEL**	**RCL**	**FERR**	**B8ZSD**	**RBL**	**RLOS**
1 =	BVCR Saturation	ECR Saturation	Yellow Alarm Detected	Carrier Loss Detected	Frame Error Detected	B8ZS/COFA Detected	Blue Alarm Detected	Resync in progress

Figure 21. Receive Status Register (RSR)

Receive Status Register (RSR)

The CS2180A and CS2180B monitors the incoming T1 data for a number of error conditions. These alarms are recorded in the Receive Status Register (RSR), and output in real time on the status pins: RYEL, RCL, RBV, RFER, and RLOS. Three presettable counters are provided which count the number of occurrences of Bipolar Violations, Framing and CRC errors. The Receive Interrupt Mask Register, RIMR (see below), can be set to specify which of the eight errors recorded in the RSR will generate a hardware interrupt on $\overline{INT}$. When operating in hardware mode, all these registers are cleared, and only the status pins provide real time alarm information.

Each of the eight bits of the RSR (Figure 21) corresponds to an alarm condition. A bit in the RSR is set when the corresponding alarm is detected. It will be cleared when the RSR is directly read, unless the alarm condition persists (see Alarm Servicing, below). TCLK is used to clock the internal circuitry which clears RSR after RSR is directly read; therefore, a 1.544 MHz signal must always be input to TCLK, even for a "receiver-only" application. The status pins which correspond to many of the RSR bits operate in real time. They go high when the error is detected, and return low either immediately, or as soon as the error condition is cleared. Alarms are reported synchronously with the emergence of the offending bits on RSER. See Figure 22, and the corresponding alarm description below for further description of status pin timing.

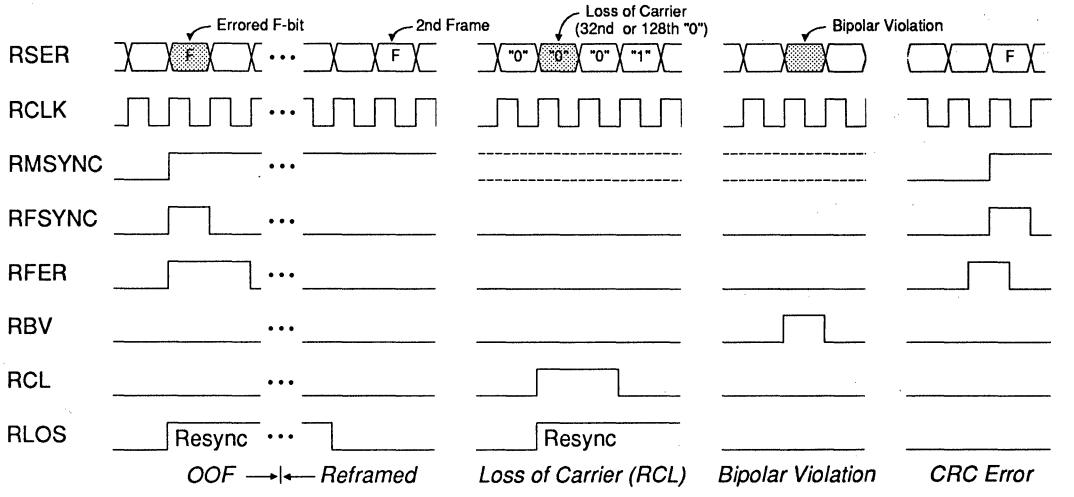


Figure 22. Receive Status Pin Timing

Receive Loss of Sync
RSR.0: RLOS

RLOS (RSR.0) goes high when a receiver resync is in progress. When the receiver is set to auto resync (RCR.1 = 0), the receiver will commence resync when an OOF event or loss of carrier is detected. If in response to an OOF, RLOS transitions high synchronously with the output of the offending F-bit on RSER (see RCR.6).

CS2180A only: If in response to an RCL, RLOS goes high with the 32nd consecutive zero bit.

CS2180B only: If in response to an RCL, RLOS goes high with the 128th ±1 consecutive zero bit.

The RLOS pin will return low one bit period prior to the F-bit of the second frame after the new alignment has been declared (timing signals will reset at the start of the new superframe). Refer to *Receiver Synchronization*, above, for more information.

Receive Blue Alarm
RSR.1: RBL

RBL (RSR.1) will transition high when a blue alarm is detected, and is updated at the beginning of odd-numbered frames.

CS2180A only: A blue alarm is reported whenever less than 3 zeros are detected in the channel data of 2 consecutive frames (F-bit positions are not tested). There is no status pin corresponding to RBL.

CS2180B only: A blue alarm is reported whenever unframed all ones occurs, as per Bellcore TR-TSY-000191. The algorithm used is to simultaneously check for an out-of-frame (OOF) condition, and check for 14 or less zeros out of 13,895 bits. All bits, including frame bits, are tested. RBL goes high on a frame boundary. RBL goes low immediately (indicating the termination of the AIS condition) if OOF goes low, or if 15 or more zeros are counted and the number of bit periods is less than or equal to 13,895. RBL is reported on pin 3 of the 44-pin PLCC package. There is no status pin corresponding to RBL on the 40-pin DIP package.

B8ZS/COFA Detect
RSR.2: B8ZSD

B8ZSD (RSR.2) is a multifunction bit. It can be configured either to report the detection of B8ZS codes, or to indicate a change of framing alignment. This selection is performed through the setting of CCR.6 (see Common Control Register, above). There is no status pin corresponding to RSR.2.

If CCR.6 is clear, RSR.2 will go high every time a B8ZS code is detected in the incoming T1 data. This detector remains operational, whether or not B8ZS substitution has been enabled via CCR.2.

If CCR.6 is set to a "1", RSR.2 will go high in response to a Change of Frame Alignment (COFA). A COFA is reported when the last receiver resync resulted in a change of frame or multiframe alignment. RSR.2 will go high at the same time the timing signals are reset after a resync. (See *Receiver Synchronization*, above.)

Frame Bit Error
RSR.3: FERR

FERR (RSR.3) is set whenever a framing bit is in error.

193S Frame Bit Errors: The framing bits for the 193S is the F_T channel (odd F-bits). The RFER status pin (pin 38) signals the same F_T errors, but in addition, signals F_S errors as well. When signaling a frame bit error, RFER will go high simultaneously with the output of the offending F-bit on RSER, and hold for 2 bit periods.

193E Frame Bit Errors: The framing bits for the 193E mode are the FPS channel (F-bits of frames

4, 8, 12, 16, 20, and 24). The RFER status pin (pin 38) signals the same FPS errors, but in addition, signals CRC errors as well. When signaling a frame bit error, RFER will go high simultaneously with the output of the offending F-bit on RSER, and hold for 2 bit periods. When signaling a CRC error, RFER will transition high 1/2 bit before the new superframe to indicate a CRC error in the previous superframe. It goes high on the falling edge of RCLK, and is held for only one period, returning low on the next falling edge of RCLK.

SLC Frame Bit Errors: The framing bits for the SLC mode is the F_T channel (odd F-bits). The RFER status pin (pin 38) signals the same F_T errors, but in addition, signals F_S errors as well. The presence of DL bits in F_S bit positions will not be reported as frame bit errors on pin RFER, or in registers RSR.3 and ECR.0-3, and will not contribute to determining that an OOF condition exists. When signaling a frame bit error, RFER will go high simultaneously with the output of the offending F-bit on RSER, and hold for 2 bit periods.

T1DM Frame Bit Errors: The framing bits for the T1DM mode are the F_T and F_S bits, plus the channel 24 sync word. The RFER status pin (pin 38) signals errors in the frame bits. RFER will go high simultaneously with the F-bit of the frame following the frame in which the error(s) occured, and will remain high for two bit periods.

Receive Carrier Loss
RSR.4: RCL

CS2180A only: Carrier loss is declared when 32 consecutive zero's are detected at RPOS/RNEG. RCL (RSR.2) and the RCL pin (pin 36) transition high with the output of the 32^{nd} zero bit on RSER. The RCL pin will return low as soon as the next "1" is received at RPOS/RNEG.

CS2180B only: Carrier loss is declared when 128±1 consecutive zero's are detected at RPOS/RNEG. RCL (RSR.2) and the RCL pin (pin 36) transition high with the output of the 128^{th}±1 zero bit on RSER. The RCL pin will return low as soon as the next "1" is received at RPOS/RNEG.

Receive Yellow Alarm
RSR.5: RYEL

RYEL (RSR.5) transitions high when a yellow alarm is detected. The format of the alarm detected is determined by the settings of either CCR.3 or CCR.5, depending on the framing format being used. The RYEL pin (pin 21) will return low as soon as the alarm clears, that is, when the next expected alarm bit no longer indicates an alarm.

When using a bit 2 yellow alarm, in either 193S or 193E mode, a yellow alarm is defined as a "0" in bit 2 (2nd MSB) of every DS0 channel. RYEL will signal a bit 2 yellow alarm when 256 or more consecutive channels are detected with a "0" in bit 2. The alarm will clear at the next "1" detected in a bit 2 position.

When using an FDL yellow alarm in 193E mode, RYEL will declare a yellow alarm after 16 repetitions of "00FF" on the FDL. The alarm will clear at the next bit which is out of sequence.

When using an S-bit yellow alarm in 193S mode, RYEL will transition high whenever a "1" is detected in the F-bit of frame 12. The alarm is not cleared until a zero is detected in the F-bit of frame 12.

In T1DM mode , a yellow alarm is detected by checking the channel 24 sync word. In SLC-96 mode, the CS2180B does not recognize yellow alarms, rather, they are recognized by the user via the DL.

7 (MSB)	6	5	4 (LSB)	3 (MSB)	2	1	0 (LSB)
OOFD3	OOFD2	OOFD1	OOFD0	ESFD3	ESFD2	ESFD1	ESFD0
OOF Count		Presetable. Saturates at 15 (1111).		ESF Error Count		Presetable. Saturates at 15 (1111).	

Figure 23. Error Count Register (ECR)

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0
Counts individual Bipolar Violations. Sets RSR.7 high when overflows past 255 (11111111). Presetable to any starting value to limit the number of Bipolar Violations needed to overflow.							

Figure 24. Bipolar Violation Count Register (BVCR)

Error Count Saturation
RSR.6: ECS

ECS (RSR.6) monitors the status of the Error Count Register (ECR), as shown in Figure 23. The ECR provides two, separate, 4 bit counters at one register address: the ESF Error Count (D0 - D3), and the OOF Count (D4 - D7). RSR.6 will go high after either of these 4 bit counters becomes saturated (at 15), and a new OOF or ESF event is detected (the 16^{th} or greater).

The OOF Counter (D4 - D7) records the number of out-of-frame events. An OOF event occurs when 2 out of either 4 or 5 consecutive framing bits are in error, as defined by RCR.6. In 193S mode, the F_T bits are monitored for OOF events, while in 193E mode, the FPS bits are used.

The ESF counter (D0 - D3) records the number of "Errored Superframes". An ESF event in 193E mode is defined as an OOF event, or a CRC error. The ESF counter will be advanced each time either event is detected. In 193S mode, the ESF counter records individual framing bit errors. If RCR.3 is set, requiring F_S bits to be qualified for synchronization, both F_T and F_S bit errors will advance the ESF counter. If RCR.3 is clear, only F_T bits will be monitored.

The OOF and ESF operate separately, each counting up from 0 (hex) and saturating at F (hex). The saturation threshold can be changed for each counter separately, by presetting the counter to some value higher than 0. Because they share the same register address, both counters must be read or written simultaneously. There is no status pin directly corresponding to the ECS bit, but FERR signals individual frame bit and CRC errors, and RLOS signals an OOF event.

Bipolar Violation Count Saturation
RSR.7: BVCS

Individual Bipolar Violations are recorded in an 8 bit counter, the Bipolar Violation Count Register (BVCR), as show in Figure 24. The BVCR counts up from 0 (all "0's") to 255 (all "1's"). After reaching saturation at 255, every Bipolar Violation received will cause BVCS (RSR.7) to be set to a "1". The BVCR can be preset, to a value greater than 0, to lower the threshold at which it saturates and signals an alarm in RSR.7. B8ZS codes will not be counted if B8ZS format is enabled via CCR.2. Note also that the Bipolar

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

0	Disables interrupts for the corresponding bit of the RSR.
1	Enables an interrupt whenever the corresponding bit of the RSR goes high.

Figure 25. Receive Interrupt Mask Register (RIMR)

Violation monitoring circuit is disabled entirely when using NRZ input at RPOS/RNEG (selected by tying RPOS/RNEG together).

Individual Bipolar Violations are also reported in real time on RBV (pin 37). RBV will go high simultaneously with the output of the accused bit at RSER. It will only be held for that bit period, falling at the next bit, unless another violation is detected.

Interrupts

When operating in host mode, an interrupt pin, $\overline{\text{INT}}$ (pin 14), is provided to signal the host processor of alarm conditions. $\overline{\text{INT}}$ is an open drain output, and should be tied to the positive supply through a resistor. The $\overline{\text{INT}}$ pin can be programmed to respond whenever any bit of the Receive Status Register (RSR) goes high by setting the corresponding bit of the Receive Interrupt Mask Register (RIMR). Each bit of the RIMR is 'AND'ed with the corresponding bit of the RSR to determine the interrupt. Clearing any bit in the RIMR will disable the interrupt for that alarm condition. When an interrupt has been signaled, the CS2180A and CS2180B must be serviced by the host processor to clear the alarm, as described below. Figure 25 shows an overview of the RIMR.

Alarm Servicing

The CS2180A and CS2180B must be serviced by the host processor to clear the interrupt. Clearing the appropriate bit (or bits, if more than 1 alarm condition exists) in the Receive Interrupt Mask Register (RIMR) will clear any interrupt unconditionally. The interrupt for that alarm will remain disabled until the bit in the RIMR is set again.

Depending on the type of alarm condition, an interrupt may also be cleared without changing the RIMR. If the alarm is in response to a counter saturation (see *Bipolar Violation Count Saturation* and *Error Count Saturation*, above), then the counter must be reset to a value other than all "1's" to clear the alarm. If the interrupt is in response to a real time event, then it may be cleared by a *direct* read (a burst read will have no effect) of the RSR. Note that reading the RSR will only clear the interrupt if the alarm condition no longer persists. For real time events of long duration, clearing the appropriate bits in the RIMR is the only way to clear the interrupt.

HARDWARE MODE

For stand alone applications or prototyping in which the device is to operate without a host processor, the CS2180A and CS2180B can be configured to run in hardware mode by tying the Serial Port Select pin (SPS) to ground (VSS). This disables the serial port and redefines pins 14 through 18 as mode control pins. All registers are cleared, with the exception of the control bits which are mapped to the mode control pins, and TCR.4, which is set to "1", enabling robbed bit signaling. This means that, with the exception of robbed bit signaling, the configuration of the CS2180A and CS2180B in hardware mode is the

same as if it were in host mode with all control bits cleared. Dynamic control of a few of the control bits is provided by mapping them directly to pins 14 - 18. Operation of these pins is described in *Hardware Mode Control Pins* and Table 2, below. Note that the SLC-96 and T1DM frame format are not supported in the hardware mode.

When operating in hardware mode, bit-robbed signaling is enabled for all channels. Signaling data sampled from TABCD is inserted into the 8th bit position (LSB) of every DS0 channel during signaling frames (every 6th frame). There is no facility for programming individual channels clear, however; all channels may be made transparent by tying TABCD to TSER.

When pulling 193SI (pin 14) high for external S-bit insertion in 193S mode, data is sampled from TLINK and inserted into the F-bits of even frames. Pin 14 has no effect when the device is in 193E mode. When using 193E format, TLINK is sampled for insertion into every odd F-bit (FDL). CRC data is internally generated and cannot be externally supplied.

The receiver will initiate a resync if 2 of the previous 4 framing bits were in error. It will declare synchronization after 10 consecutive F-bits are qualified. When in 193E mode, CRC errors will be reported on RFER, but not used to qualify synchronization. Receiver status can be monitored via the status outputs: RYEL, RCL, RBV, RFER, and RLOS (pins 21, 36, 37, 38, and 39). There is no support for generating blue alarms or idle code insertion when in hardware mode.

Hardware Mode Control Pins

Framing Format

FM (pin 15) allows selection of the framing mode for both transmit and receive sides. Holding pin 15 low selects 193S framing mode. 193E framing may be selected by pulling pin 15 high.

Yellow Alarm

A yellow alarm may be generated on the transmit side by pulling TYEL (pin 16) high. In 193S mode, bit 2 yellow alarms are supported internally. In 193E mode, FDL yellow alarms are supported. These formats are also detected by the receiver and reported on RYEL. Blue alarms are not supported in hardware mode, except for the transmission of all "1's" on TPOS/TNEG during loopback.

If S-bit yellow alarm is desired while in 193S mode, it may be externally provided via S-bit insertion, enabled by pulling pin 14 high. There is,

PIN NUMBER	REGISTER MAPPING	DESCRIPTION	FUNCTION
14	TCR.2	193S: S-bit Insertion	0= Internal 1= External
15	CCR.4	Framing Mode Select	0= 193S 1= 193E
16	TCR.0	Transmit Yellow Alarm	0= Disabled 1= Enabled
17	CCR.1	B7 Zero Suppression	0= Transparent 1= B7 Stuffing
18	CCR.2	B8ZS Zero Suppression	0= Disabled 1= Enabled

Table 2. Hardware Mode Control Pins

however, no way to generate a bit 2 yellow alarm while in 193E mode. Moreover, the device will not decode either of these formats, while in hardware mode. If they are required, external alarm detection must be provided.

Zero Suppression

CS2180A only: B7 and B8ZS, pins 17 and 18, select the zero suppression format for both transmitter and receiver (B8ZS only). Pulling pin 17 high enables bit 7 stuffing (B7), pulling pin 18 high enables B8ZS. Transparent mode may be selected by holding both 17 and 18 low.

CS2180B only: B7, pin 17, selects the B7 zero suppression format for the transmitter. Pulling pin 17 high enables bit 7 stuffing (B7). Pulling pin 18 high enables B8ZS on the transmitter. The receiver is always capable of decoding either B8ZS or AMI-encoded data. Transparent mode may be selected by holding both 17 and 18 low.

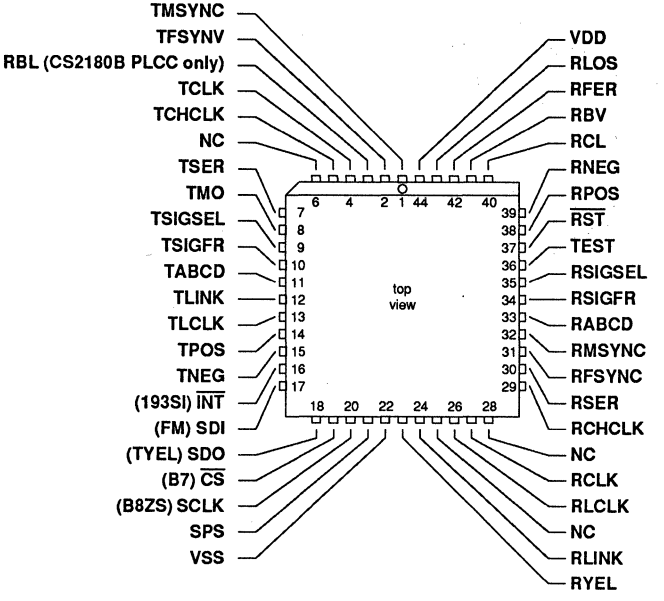
Loopback

Loopback is also provided in the hardware mode by simultaneously driving B7 and B8ZS (pins 17 and 18) high. The previous state of pins 17 and 18 are remembered, and the selected zero suppression mode remains effective during loopback. While in loopback, an unframed all "1's" signal (Blue alarm) is output on TPOS/TNEG.

PIN DESCRIPTION

TRANSMIT MULTIFRAME SYNC	TMSYNC	1	40	VDD	POSITIVE POWER SUPPLY
TRANSMIT FRAME SYNC	TFSYNC	2	39	RLOS	RECEIVE LOSS OF SYNC
TRANSMIT CLOCK	TCLK	3	38	RFER	RECEIVE FRAME ERROR
TRANSMIT CHANNEL CLOCK	TCHCLK	4	37	RBV	RECEIVE BIPOLAR VIOLATION
TRANSMIT SERIAL DATA	TSER	5	36	RCL	RECEIVE CARRIER LOSS
TRANSMIT MULTIFRAME OUT	TMO	6	35	RNEG	RECEIVE NEGATIVE BIPOLAR DATA
TRANSMIT SIGNALING SELECT	TSIGSEL	7	34	RPOS	RECEIVE POSITIVE BIPOLAR DATA
TRANSMIT SIGNALING FRAME	TSIGFR	8	33	$\overline{RST}$	RESET
TRANSMIT ABCD SIGNALING	TABCD	9	32	TEST	TEST MODE
TRANSMIT LINK DATA	TLINK	10	31	RSIGSEL	RECEIVE SIGNALING SELECT
TRANSMIT LINK CLOCK	TLCLK	11	30	RSIGFR	RECEIVE SIGNALING FRAME
TRANSMIT POSITIVE BIPOLAR DATA	TPOS	12	29	RABCD	RECEIVE ABCD SIGNALING
TRANSMIT NEGATIVE BIPOLAR DATA	TNEG	13	28	RMSYNC	RECEIVE MULTIFRAME SYNC
RECEIVE ALARM INTERRUPT	(193SI)$\overline{INT}$	14	27	RFSYNC	RECEIVE FRAME SYNC
SERIAL DATA IN	(FM)SDI	15	26	RSER	RECEIVE SERIAL DATA
SERIAL DATA OUT	(TYEL)SDO	16	25	RCKCLK	RECEIVE CHANNEL CLOCK
CHIP SELECT	(B7)$\overline{CS}$	17	24	RCLK	RECEIVE CLOCK
SERIAL DATA CLOCK	(B8ZS)SCLK	18	23	RLCLK	RECEIVE LINK CLOCK
SERIAL PORT SELECT	SPS	19	22	RLINK	RECEIVE LINK DATA
SIGNAL GROUND	VSS	20	21	RYEL	RECEIVE YELLOW ALARM

CS2180A and CS2180B



CS2180B 44-pin PLCC Pinout

Power Supply Connections

VDD - Positive Supply, Pin 40.

Positive digital power supply. Nominally +5.0 volts.VDD current requirements increase if RCLK is static, and if $\overline{RST}$ is held high.

VSS - Signal Ground, Pin 20.

Power supply ground. Nominally 0 volts.

Host Mode Serial Interface

Pins 14 - 18 are multifunctional. When in Host mode, they operate as serial interface pins. When in hardware mode, they are redefined as mode control pins. Their hardware mode operation is described separately under *Hardware Mode Control Pins*, below.

SPS - Serial Port Select, Pin 19.

Must be tied to VDD to select host mode, allowing operation of serial port. Tying SPS to VSS selects hardware mode. Selecting hardware mode clears all internal registers except the common control register (CCR) and transmitter control register (TCR), and redefines pins 14 through 18 as mode control pins.

Inputs

SDI - Serial Data In, Pin 15.

Serial data input for addressing and writing to on-board control registers. Data is input LSB first. Input data is latched on the rising edge of SCLK. On the CS2180A only, the data must be valid during the SCLK low period to prevent momentary corruption of control registers.

$\overline{CS}$ - Chip Select, Pin 17.

$\overline{CS}$ low enables serial port for read or write. When $\overline{CS}$ transitions high, all data transfers are terminated, port control logic is disabled, and SDO is tri-stated to allow for multiprocessor interface.

SCLK - Serial Data Clock, Pin 18.

Used to read or write the serial port. Data at SDO is output on the falling edge of SCLK and held to the next falling edge. Input data on SDI is latched on the rising edge of SCLK. On the CS2180A only, data must be valid during the SCLK low period to prevent momentary corruption of control registers.

Outputs

$\overline{INT}$ - Receive Alarm Interrupt, Pin 14.

Pulled low to flag host controller when an alarm interrupt condition occurs. The user may select which alarm conditions will trigger an interrupt by appropriately setting the Receive Interrupt Mask Register (RIMR). $\overline{INT}$ is an open drain output, and should be tied to the positive supply (VDD) through a resistor.

SDO - Serial Data Out, Pin 16.

When reading the serial port, data is output LSB first. Data is updated on the falling edge of SCLK and held to the next falling edge. SDO goes to a high impedance state when $\overline{CS}$ is high or after the rising edge of SCLK corresponding to the output of the MSB (last bit output).

Hardware Mode Control Pins

Pins 14 - 18 are multifunctional. When in Host mode, they operate as serial interface pins. When in hardware mode, they are redefined as mode control pins. Their host mode operation is described separately under *Host Mode Serial Interface*, above. SPS (pin 19) must be tied low to enable hardware mode.

193SI - 193S S-bit Insertion, Pin 14.

In hardware mode, pin 14 is redefined as a control pin and maps directly to TCR.2. Holding pin 14 low while in 193S framing format, configures the CS2180A and CS2180B to generate the F_S framing pattern internally for transmission. Pulling pin 14 high allows external insertion of transmitted S-bits via TLINK.

FM - Frame Mode Select, Pin 15.

In hardware mode, pin 15 is redefined as a control pin and maps directly to CCR.4. Holding pin 15 low configures the CS2180A and CS2180B for 193S framing format, pulling it high selects 193E format.

TYEL - Transmit Yellow Alarm, Pin 16.

In hardware mode, pin 16 is redefined as a control pin and maps directly to TCR.0. Pulling pin 16 high enables transmission of a yellow alarm in the default format. In 193S mode yellow alarms default to a "0" in bit 2 (D6) of all DS0 channels. In 193E mode, yellow alarms are encoded/decoded as a repeating pattern of 00FF (hex) on the FDL.

B7 - Bit 7 Zero Suppression, Pin 17.

In hardware mode, pin 17 is redefined as a control pin and maps directly to CCR.1. Holding pin 17 low disables bit 7 stuffing (B7) for transparent operation. Pulling pin 17 high enables B7 zero suppression. Pulling pins 17 and 18 high simultaneously puts the CS2180A and CS2180B into loopback operation.

B8ZS - Bipolar Eight Zero Suppression, Pin 18.

In hardware mode, pin 18 is redefined as a control pin and maps directly to CCR.2. On the CS2180A, pulling pin 18 high enables B8ZS zero suppression in both the transmitter and receiver. On the CS2180B, pulling pin 18 high enables B8ZS zero suppression in just the transmitter, since the CS2180B receiver is always capable of receiving either B8ZS or AMI-encoded data. Pulling pins 17 and 18 high simultaneously puts the CS2180A and CS2180B into loopback operation.

Transmitter

Inputs

TCLK - Transmit Clock, Pin 3.

1.544 MHz primary transmitter clock. Divided down internally to provide timing signals. TPOS and TNEG are updated on the rising edge of TCLK. Input transmission data (TSER, TABCD, and TLINK) is sampled on the falling edge of TCLK.

A 1.544 MHz signal must be input into TCLK even for those applications where the transmitter is not being used. TCLK is used by the circuitry which clears status registers after those registers have been directly read.

TMSYNC - Transmit Multiframe Sync, Pin 1.

A low to high transition of TMSYNC, occurring near the rising edge of TCLK, resets transmitter's frame and multiframe counters, identifying bit period (at TSER) concurrent with the next falling edge of TCLK as the F-bit of frame 1. If tied low, TFSYNC may be used to set frame alignment, and the CS2180A and CS2180B will arbitrarily choose multiframe alignment. Internal channel, frame, and multiframe counters are output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK.

TFSYNC - Transmit Frame Sync, Pin 2.

A low to high transition of TFSYNC, occurring near the rising edge of TCLK, resets transmitter's frame counters, identifying bit period (at TSER) concurrent with the next falling edge of TCLK as the F-bit of a new frame. If tied low, TMSYNC may be used to set both frame and multiframe alignment. Without any sync input, the CS2180A and CS2180B will arbitrarily choose both frame and multiframe alignment. Internal channel, frame, and multiframe counters are output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK.

TSER - Transmit Serial Data, Pin 5.

Input data (NRZ format), sampled on the falling edge of TCLK. TSER may also be used to provide externally supplied data for insertion into F_T, FPS, and CRC channels. Refer to *Transmit Control Register*, bits 5 and 6. Delay from TSER to TPOS/TNEG is 10 TCLK periods.

TABCD - Transmit ABCD Signaling, Pin 9.

When enabled, by setting bit 4 of the Transmit Control Register (TCR), data provided on TABCD is inserted into the 8th bit position (LSB) of every DS0 channel during signaling frames. Those are frames 6 and 12 in 193S format, and 6, 12, 18, and 24 in 193E. Signaling on individual DS0 channels may be suppressed by declaring those channels transparent in the Transmit Transparent Registers (TTR). Signaling in hardware mode is always enabled. Delay from TABCD to TPOS/TNEG is 10 TCLK periods.

TLINK - Transmit Link Data, Pin 10.

In 193S framing mode, setting bit 2 of the Transmission Control Register (TCR) enables data on TLINK to be inserted into the S-bit channel (F-bit of all even frames). In 193E mode, TLINK is sampled for data to be inserted into the F-bit of all odd frames for the 4 kHz facility data link (FDL). In the SLC-96 mode, TLINK is sampled for data to be inserted into the DL. In T1DM mode, TLINK is sampled for data to be inserted into the channel 24 "A" data link. Delay from TLINK to TPOS/TNEG is 10 TCLK periods. In hardware mode, external S-bit insertion on TLINK is enabled by setting pin 14 (193SI) high.

Outputs

TPOS, TNEG - Transmit Bipolar Data Outputs, Pins 12 and 13.

Coded data for transmission, updated on rising edge of TCLK. If TCR.7 is clear, or the CS2180A or CS2180B is in hardware mode, data is output in dual-unipolar format. If TCR.7 is set to a "1", data is output on TPOS in NRZ format, and TNEG is held low. Delay from input to TPOS/TNEG is 10 TCLK periods.

TCHCLK - Transmit Channel Clock, Pin 4.

192 kHz clock which identifies DS0 channel boundaries. TCHCLK rises to indicate that the next bit input on TSER is the first bit (MSB) of the DS0 channel. TCHCLK has a 50% duty cycle.

TMO - Transmit Multiframe Out, Pin 6.

Output of internal multiframe counter. Rising edge marks beginning of multiframe, with 50% duty cycle. Internal multiframe counter can be set on the rising edge of TMSYNC. In 193S mode, TMO is high for frames 1-6, and low for frames 7-12, allowing easy distinction of signaling channels A and B. In 193E mode, TMO is high for 1-12, and low for 13-24, and can be used together with TSIGSEL to distinguish channels A, B, C, and D.

TSIGSEL - Transmit Signaling Select, Pin 7.

In 193S, 193E and T1DM modes, TSIGSEL runs at 2x TMO with a 50% duty cycle. Together with TMO, TSIGSEL provides a way to distinguish signaling channels A, B, C, and D in 193E mode. TMO is high for channels A and B. TSIGSEL is high for channels A and C (frames 1-6 and 13-18). In SLC96 mode, TSIGSEL provides a way to distinquish when the DL bits are to input.

TSIGFR - Transmit Signaling Frame, Pin 8.

TSIGFR goes high during signaling frames only, remaining low at all other times. Signaling frames are frames 6 and 12 in 193S, SLC96 and T1DM modes, and 6, 12, 18, and 24 in 193E mode.

TLCLK - Transmit Line Clock, Pin 11.

In 193S, 193E and SLC96 modes, TLCLK runs at 4 kHz with a 50% duty cycle. It's high during odd numbered frames, and is useful for marking F_S or FDL channel timing (input on TLINK), and F_T, FPS, and CRC channels (input on TSER). In T1DM, TLCLK runs at 8 kHz, with a duty cycle of one bit period high per frame.

Receiver

Inputs

RCLK - Receive Clock, Pin 24.

1.544 MHz primary receiver clock. Receiver data is output on the rising edge, and input on the falling edge of RCLK. If no signal is present on RCLK, $\overline{RST}$ should be held low to minimize power consumption.

RPOS, RNEG - Receive Bipolar Data Inputs, Pin 34.

Recovered data, sampled on falling edge of RCLK. Tie pins together to receive NRZ data and disable bipolar violation monitoring circuitry. Delay from RPOS/RNEG to output at RSER is 13 RCLK periods.

$\overline{RST}$ - Reset, Pin 33.

Falling edge of $\overline{RST}$ clears all internal registers and resets receiver error counters. A receiver resync is forced when $\overline{RST}$ returns high. This resync effects only the receiver synchronization, and has no effect on transmit timing, but transmit control modes are cleared. The host processor should restore all control modes following a reset by writing the appropriate control registers. NOTE: *On system power-up, $\overline{RST}$ must be held low to insure initialization of all on-board registers.*

Outputs

RYEL - Receive Yellow Alarm, Pin 21.

Transitions high when a yellow alarm is detected, returns low when yellow alarm is cleared. When in Host mode, Yellow alarm formats for both 193S and 193E modes can be selected via bits 3 and 5 of the Common Control Register. When in hardware mode, the 193S mode defaults to bit 2 Yellow alarms, and the 193E mode defaults to FDL yellow alarms. Refer to bit 5 of the Receive Status Register (RYEL) for a description of alarm detection conditions.

RCL - Receive Carrier Loss, Pin 36.

On the CS2180A, RCL transitions high if 32 consecutive "0's" are detected on RPOS and RNEG and returns low on next "1". On the CS2180B, RCL transitions high if 128±1 consecutive "0's" are detected on RPOS and RNEG and returns low on the next "1".

RBL - Receive Blue Alarm, (CS2180B PLCC only, Pin 3).

Transitions high on a frame boundary if an unframed-all ones and an out-of-frame condition simultaneously occur. Returns low when either out-of-frame ends or zeros are detected.

RBV - Receive Bipolar Violation, Pin 37.

If a bipolar violation is detected, RBV goes high simultaneous with output of accused bit on RSER, low otherwise.

RFER - Receive Frame Error, Pin 38.

Transitions high with the output of an errored framing bit, and is held for 2 bit periods. F_T and F_S bits are tested in 193S and SLC modes, and FPS bits are tested in 193E. In T1DM mode, the F_S, F_T and channel 24 sync bits are tested. Also signals CRC errors in 193E mode, by going high 1/2 bit before the next extended superframe, and holding for 1 period (from falling edge of RCLK to next falling edge).

RLOS - Receive Loss of Sync, Pin 39.

Transitions high during receiver resync, low otherwise. Transitions high when receiver begins a resync, and falls low one frame after new timing is declared.

RSER - Receive Serial Data, Pin 26.

Received data, output in NRZ format. Data on RSER is valid and stable on the falling edges of RCLK. Delay from RPOS/RNEG to RSER is 13 RCLK periods.

RABCD - Receive ABCD Signaling, Pin 29.

Signaling data extracted from LSB of DS0 channels during signaling frames is valid on RABCD during corresponding channel output on RSER (LSB is available on RABCD seven bit periods before it appears at RSER). During non-signaling frames, RABCD continues to output LSB concurrently with word on RSER. After update, data on RABCD is valid and stable on the falling edge of RCLK.

RLINK - Receive Link Data, Pin 22.

In 193S mode, S-bit data is output on RLINK one RCLK prior to start of corresponding even frame, and held for 2 frames until next update. In 193E mode, FDL data is output on RLINK one RCLK prior to start of corresponding odd frame, and held for 2 frames until next update. After update, data on RLINK is valid and stable on the falling edge of RCLK.

In SLC mode, all Fs and DL bits are output on RLINK using RLCLK. In T1DM mode, channel 24 "A" link data is output on RLINK, and is valid and stable on the falling edge of RFSYNC.

RLCLK - Receive Link Clock, Pin 23.

RLCLK runs at 4 kHz with a 50% duty cycle. It's high during odd numbered frames. RCLK is useful for marking S-bit, DL or FDL channel timing, output on RLINK. RLCLK is present, but serves no useful purpose in the T1DM mode.

RCHCLK - Receive Channel Clock, Pin 25.

192 kHz clock which identifies DS0 channel boundaries output on RSER. RCHCLK is useful for parallel to serial conversion of DS0 channel data.

RFSYNC - Receive Frame Sync, Pin 27.

Goes high for one RCLK period concurrent with the F-bit of each new frame output on RSER, low otherwise. In the T1DM mode, the falling edge of RFSYNC can be used to sample the "A" link channel on RLINK.

RMSYNC - Receive Multiframe Sync, Pin 28.

Rising edge signals the F-bit of 1st frame of multiframe, except in SLC-96 mode. RMSYNC runs on 50% duty cycle, high for frames 1-6 in 193S mode, distinguishing signaling channels A and B. In 193E mode, it's high for frames 1-12, and can be used with RSIGSEL to distinguish channels A, B, C, and D. In SLC-96 mode, multiframe alignment can be determined by gating RMSYNC with RSIGSEL.

RSIGFR - Receive Signaling Frame, Pin 30.

High during signaling frames, low at all other times, including resync. Serves no purpose in T1DM mode.

RSIGSEL - Receive Signaling Select, Pin 31.

In 193E mode, RSIGSEL goes high for frames 1-6 and 13-18, identifying signaling channels A and C. Used together with RMSYNC, which is high for channels A and B, it allows identification of all 4 signaling channels. In 193S mode, RSIGSEL goes high for frames 1-3 and 7-9. Serves no purpose in T1DM mode. In SLC mode, RSIGSEL goes high in those frames where Fs bits (frames 59 to 11) and the last spolier bit (frame 58) are present; goes low in all other frames (frames 12 to 57).

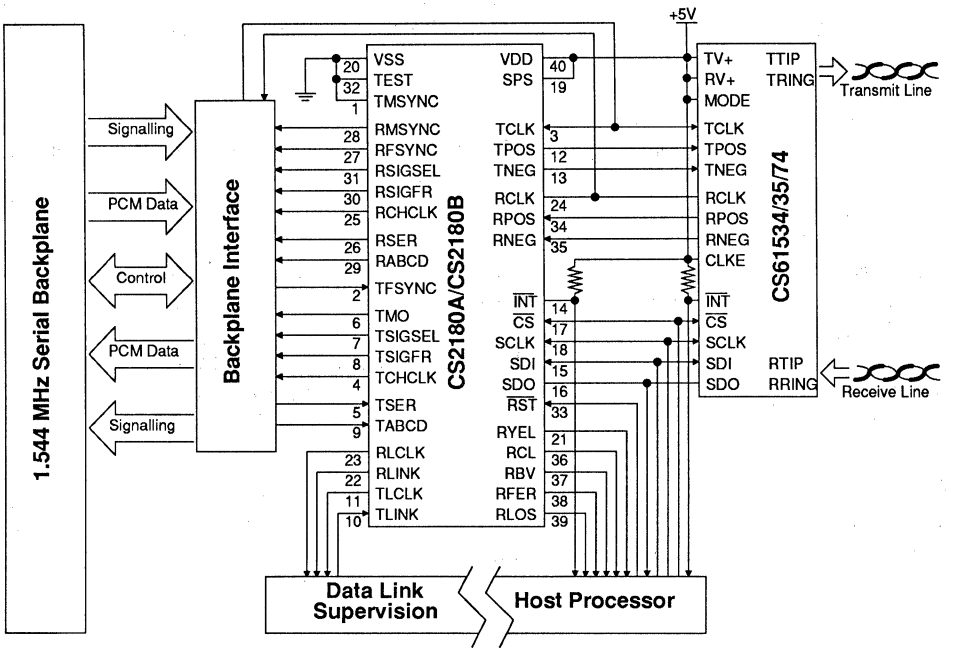
Miscellaneous

TEST - Test Mode, Pin 32.

Tie to VSS for normal operation. Factory use only.

APPLICATIONS

System Connection Diagram



Typical System Connection

T1 Frame Formats

T1 is the basic format in the T-carrier PCM transmission system used in the United States. Detailed technical specifications can be found in ANSI T1.107-1988.

The T1 format time-division multiplexes 24 digitized voice (telephone) or data channels into a single, 1.544 Mbps data stream. This format is used primarily for transmission over dual twisted-pair cable with digital repeaters at 6000 ft. intervals. The T-carrier system also defines higher level formats for long-haul transmission via satellite or microwave relay. These higher level formats are constructed by multiplexing several T1 lines into higher and higher data rates. Figure A1 gives an overview of the T-carrier hierarchy.

The T1 format provides a 64 kbps channel for each individual voice or data line. These PCM voice channels consist of 8-bit samples which are sampled at 8 kHz for a data rate of 64 kbps. A T1 frame is constructed by multiplexing 24 of these DS-0 channels and inserting a framing bit at the

Level	Number of voice channels	Bit Rate (Mbps)
T-1	24	1.544
T-1C	48	3.152
T-2	96	6.312
T-3	672	44.736
T-4	4032	274.176

Figure A1. T-carrier Hiearchy

beginning of the series. This results in 192 bits of channel data, plus an F-bit, for a total of 1.544 Mbps (193 bits/frame transmitted at 8 kHz). See Figure A2.

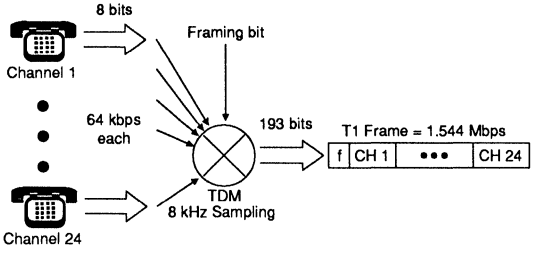


Figure A2. T1 Overveiw

Multiple T1 frames are then grouped into superframes of 12 or 24 frames to provide for framing and signaling synchronization. The older 193S or D4 format defines a superframe as 12 frames, with the F-bits carrying 2 channels of synchronization signals. The emerging 193E, or Extended Superframe Format (ESF) calls for 24 frames in a superframe. This allows the 24 F-bits to be divided into 3 separate channels for framing, CRC checks, and system messages.

Additional variations on T1 are used for Subscriber Loop Carrier (SLC-96) and Digital Data Service (DDS) T1DM.

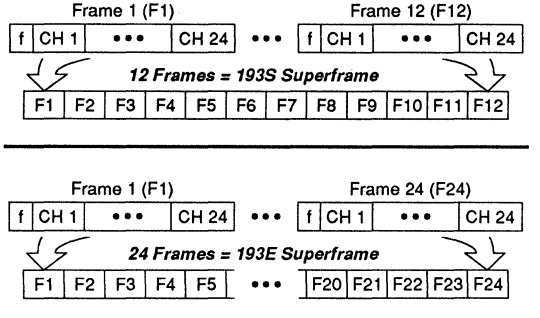


Figure A3. Framing Overveiw

193S Framing Format

Figure A4 shows the bit uses in the 193S framing format. The framing bits are divided into two channels. The odd F-bits are designated as the F_T (terminal framing) channel, which always carries a repeating pattern of "101010". This pattern allows synchronization to the frame boundaries, and distinguishes the even and odd frames. The even F-bits are designated as the F_S (signaling framing) channel. This channel carries a different synchronization code (001110) which identifies superframe alignment. The F_S channel can alternately be used as a message channel for system use, in which case there is no facility provided for multiframe synchronization.

Signaling information associated with each individual voice channel, such as on-hook/off-hook, call progress, dialing digits, etc., is transmitted within the voice channel itself. The signaling data is transmitted in the LSB of each channel during the 6th and 12th frames. The original LSB of the channel is actually replaced with the signaling data, hence this is known as "robbed-bit" signaling. The 6th and 12th frames can be treated as one, 2-state channel, allowing a 2-state signal to be updated twice every superframe. The two frames can also be treated as

193S	F-bits		Channel bits		Signalling Options		
Frame	F_T	F_S	Data	Signalling	T	2	4
1	1		1-8				
2		0					
3	0						
4		0					
5	1						
6		1	1-7	Bit 8	-	A	A
7	0		1-8				
8		1					
9	1						
10		1					
11	0						
12		0	1-7	Bit 8	-	A	B

Figure A4. 193S Framing Format

separate channels (A and B), yielding up to 4 separate codes for each channel every superframe. For voice grade applications, these signaling bits offer no noticeable degradation in the signal quality. When error-free data transmission is required however, robbed bit signaling can be disabled (transparent mode), and some other signaling facility must be provided by the host system.

193E Framing Format

The 193E or Extended Superframe Format allows much greater flexibility in both the use of the framing bits, and the number of signaling channels provided. As shown in Figure A5, the framing bits are divided into 3 channels. The FPS, or Framing Pattern Sequence, provides a synchronization signal for determining frame and superframe alignment. The FDL, or 4 kHz Facility Data Link, provides a dedicated channel for system messages. The CRC (Cyclic Redundancy Check) channel allows CRC check sums to be transmitted with each superframe to monitor line quality. As with the 193S format, every 6th frame is designated as a signaling frame. The 4 signaling frames (6, 12, 18, and 24) can be multiplexed in different configurations to provide 2, 4, or 16-state signaling codes.

193E	F-bits			Channel bits		Signaling Options			
Frame	FPS	FDL	CRC	Data	Signalling	T	2	4	16
1		m		1-8					
2			C1						
3		m							
4	0								
5		m							
6			C2	1-7	Bit 8	-	A	A	A
7		m		1-8					
8	0								
9		m							
10			C3						
11		m							
12	1			1-7	Bit 8	-	A	B	B
13		m		1-8					
14			C4						
15		m							
16	0								
17		m							
18			C5	1-7	Bit 8	-	A	A	C
19		m		1-8					
20	1								
21		m							
22			C6						
23		m							
24	1			1-7	Bit 8	-	A	B	D

Figure A5. 193E Framing Format

SLC-96 Framing Format

The SLC-96 T1 format is used between the Local Digital Switch (LDS) and a SLC-96 Remote Terminal (RT). The framing format is a D4 superframe format with specialized Data Link (DL) information bits. The DL bits consist of Concentrator (C), Spoiler (S), Maintenance (M), Alarm (A) and Protection Line Switch (PLS) bits as shown in Figure A6.

T1DM Framing Format

The T1DM T1 format is used for DDS service among hub and local intermediate DDS offices. As shown in Figure A7, the framing format is a D4 superframe format with a specialized channel 24 structure. The T1DM accepts up to 23 DS-0 signals and inserts one seven-bit byte from each signal into the first twenty-three 8-bit channel slots of the DS1 frame. The 24th channel slot contains a special synchronizing byte as shown in Figure A8. DDS equipment insures that every DS0 channel contains at least one "1". Therefore, neither B8ZS nor bit-7 zero substitution should be selcted in the CS2180B.

SLC	F-bits			Channel bits	
Frame	F_T	F_S	DL	Data	Signalling
1	1			1-8	
2		0			
3	0				
4		0			
5	1				
6		1		1-7	Bit 8 (A)
7	0			1-8	
8		1			
9	1				
10		1			
11	0				
12			C1	1-7	Bit 8 (B)
13	1			1-8	
14			C2		
15	0				
16			C3		
17	1				
18			C4	1-7	Bit 8 (A)
19	0			1-8	
20			C5		
21	1				
22			C6		
23	0				
24			C7	1-7	Bit 8 (B)
25	1			1-8	
26			C8		
27	0				
28			C9		
29	1				
30			C10	1-7	Bit 8 (A)
31	0			1-8	
32			C11		
33	1				
34			S=0		
35	0				
36			S=1	1-7	Bit 8 (B)

SLC	F-bits			Channel bits	
Frame	F_T	F_S	DL	Data	Signalling
37	1			1-8	
38			S=0		
39	0				
40			M1		
41	1				
42			M2	1-7	Bit 8 (A)
43	0			1-8	
44			M3		
45	1				
46			A1		
47	0				
48			A2	1-7	Bit 8 (B)
49	1			1-8	
50			S1		
51	0				
52			S2		
53	1				
54			S3	1-7	Bit 8 (A)
55	0			1-8	
56			S4		
57	1				
58			S=1		
59	0				
60		0		1-7	Bit 8 (B)
61	1			1-8	
62		0			
63	0				
64		0			
65	1				
66		1		1-7	Bit 8 (A)
67	0			1-8	
68		1			
69	1				
70		1			
71	0				
72		0		1-7	Bit 8 (B)

Figure A6. SLC-96 Framing Format

T1DM	F-bits		Channel Bits
Frame	F_T	F_S	
1	1		1-7 (Bit 8 of user channels is reserved for network use)
2		0	
3	0		
4		0	
5	1		
6		1	
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	

Figure A7. T1DM Framing Format

Bit	Assignment
0	Synchronization Pattern = 1
1	Synchronization Pattern = 0
2	Synchronization Pattern = 1
3	Synchronization Pattern = 1
4	Synchronization Pattern = 1
5	Yellow Alarm: 0=alarm; 1=no alarm
6	8 kHz Data Link ("A" channel)
7	Synchronization Pattern = 0

Figure A8. T1DM Channel 24 Format

Alarms

Figure A9 shows a useful overview of the alarm operation in a PCM link. When an intermediate monitoring system (or central office repeater) detects a loss of signal, it transmits an all "1's" signal (Blue alarm, or Alarm Indication Signal) on the line to maintain clock recovery operation in the subsequent digital repeaters and the destination's receiver. The same Blue alarm may be used by the source transmitter if, for some reason, it cannot maintain normal functionality (such as during loopback).

When the loss of signal is detected at the intermediate monitor, an internal Red alarm (also known as a Service Alarm Indication, or Prompt Maintenance Alarm) is generated. While in a Red alarm mode, the monitor transmits a Yellow alarm back to the source's receiver, indicating a remote loss of alignment. This Yellow alarm informs the source that there's a problem farther down the line and it's transmission is not being received at the destination.

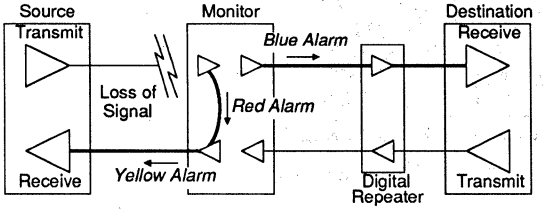


Figure A9. Alarm Operation

Zero Substitution

As was mentioned in the T1 overview, data is transmitted over dual twisted-pair cable with digital repeaters at 6000 ft. intervals. It is encoded in a bipolar AMI (Alternate Mark Inversion) format. Successive "1's" are encoded alternately as positive and negative voltage pulses. A zero is simply an absence of pulses. This means that a long stream of "0's" is indistinguishable from a dead line. Clock recovery circuits in the network maintain clock synchronization by syncing to the "1's" pulses in the transmission stream. Synchronization may be lost if there are too many consecutive zero's, hence there is a general requirement that there be at least 12.5 % "1's" density in the transmission stream. Furthermore, no more than 15 consecutive "0's" are allowable. Various zero substitution schemes have been developed to meet these requirements. The CS2180A and CS2180B supports B7 and B8ZS zero suppression formats.

B7 Zero Substitution

B7 zero substitution guarantees at least one "1" in all DS0 channels. This satasfies the 12.5 % ones density, and guarantees that more than 15 consecutive zeros will never occur. In B7 substitution systems, the 7^{th} bit (2^{nd} LSB) of an all zero channel is forced to a "1". This strategy maintains 1's density in voice grade transmission, with negligible audible interference. The drawback with the B7 format is that it's impossible for the receiving end to detect and remove the changed bits. This makes B7 zero suppression unacceptable for clear channel transmission, in which the integrity of the data must be maintained.

B8ZS Zero Substitution

B8ZS (Bipolar Eight Zero Substitution) satisfies the one's density requirement without corrupting transmission data. Instead of operating on individual channels, the B8ZS format looks at the entire transmission stream. Any eight consecutive zeros are replaced with an 8 bit code. This code uses specific bipolar violations of the AMI format to distinguish it from the ordinary data. If the last "1" transmitted before a string of zeros was encoded as a positive pulse, then the B8ZS code for the next eight bits will be 000+-0-+. Similarly, if the last "1" was a negative pulse, then the code will be 000-+0+-. In either case, bipolar violations occur in the fourth and seventh bits. These

violations are decoded as a string of zeros by the CS2180A and CS2180B if B8ZS is enabled. The received B8ZS code is replaced with eight zeros before any other processing is done on the incoming data. Note also that even if B8ZS is not enabled, the CS2180A and CS2180B monitors the incoming signal for B8ZS codes, and reports them on RSR.2 (if CCR.6 = 0).

A serious provisioning problem exists in the network regarding B8ZS. It is sometimes difficult to selectively turn-on B8ZS on all segments of an end-to-end path through the network, especially when some equipment types, such as M13s, sometimes require that all four lines on a line card be configured the same way. It is thereby highly desireable that all receivers in the network be able to receive B8ZS independent of the provisioning of B8ZS on the corresponding transmitter. Therefore, the CS2180B has its B8ZS receiver turned on all of the time, and bit CCR.2 controls only the B8ZS encoder in the transmitter. The CS2180B reports B8ZS occurrences on RSR.2. B8ZS substitutions will not increment the Bipolar Violation Count register.

Digital Milliwatt Code

The Digital Milliwatt code is the digital representation of a 0 dBm0, 1 kHz signal. It's used as a test reference for calibrating channel bank equipment as specified in AT&T Publication 43801.

• Notes •

Semiconductor Corporation

CS6152

Low Power T1 Analog Interface

Features

- Provides Analog T1 Line Interface
- Low Power Consumption (normally 180 mW)
- EXPERT *Pulse* ™ Programmable Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer Which Compliments Digital Gate Array Clock-Recovery Circuits
- Driver Performance Monitor
- Minimal External Components

General Description

The CS6152 combines the analog transmit and receive line interface functions for T1 system interface in one device. The T1 analog interface operates from a 5 Volt supply, and is transparent to the T1 framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. The device provides the ideal front-end to digital gate array based clock recovery circuits.

Applications

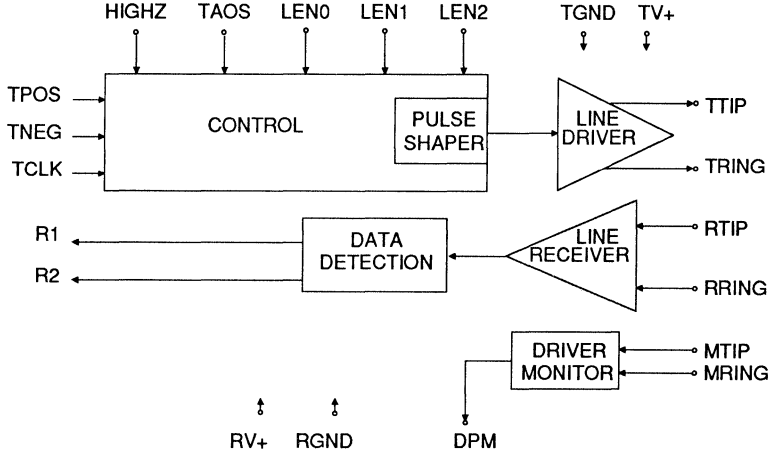
- Interfacing Network Equipment such as Multiplexors, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexors, Data PBX's and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS6152A-IP - 24 Pin Plastic, 300 mil DIP
CS6152-IL - 28 Pin J-lead PLCC

3

Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, MTIP, and MRING, which must stay within a range of -6V to RV+ + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Notes 4, 5) 100% ones density & max. line length @ 5.25V	P_D	-	-	350	mW
Normal Power Dissipation (Notes 4, 5) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	180	-	mW
Normal Power Dissipation (Notes 5, 6) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	145	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 54 Ω load over operating temperature range. Includes CS6152 and load.
5. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
6. Power dissipation internal to CS6152 while driving 54 Ω load over operating temperature range.

DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS: TCLK, TPOS, TNEG, HIGHZ, LEN0/1/2, TAOS	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS: TCLK, TPOS, TNEG, HIGHZ, LEN0/1/2, TAOS	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 7) I_{OUT}= ± 4 mA PINS: R1, R2, DPM	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 7) I_{OUT}= ± 4 mA PINS: R1, R2, DPM	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA
3-State Leakage Current PINS: DPM, R1, R2	I_{OZ}	-	-	±10	uA

Note: 7. Output drivers are high speed CMOS compatible.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Min	Typ	Max	Units
TRANSMITTER				
AMI Output Pulse Amplitudes **Line Length Selections LEN2/1/0 = 0/0/0** (Measured at transformer output) **All line length settings except, LEN2/1/0 = 0/0/0 ; 0/0/1 ; 0/1/0** (Measured at the DSX; Normalization factor for Figure 4)	2.7 2.4	3.0 3.0	3.3 3.6	V V
Load Presented To Transmitter Output	-	54	-	Ohms
Jitter Added by the Transmitter (Note 8) 10Hz - 8kHz 8kHz - 40kHz 10Hz - 40kHz Broad Band	- - - -	0.005 0.008 0.010 0.015	- - - -	UI UI UI UI
Power in 2kHz band at 772kHz (Note 9)	12.6	15	17.9	dBm
Difference in power in 2kHz band at 1.544MHz to power in 2kHz band at 772kHz (Note 9)	-29	-40	-	dB
Positive to Negative Pulse Imbalance (Note 9)	-	0.2	0.5	dB
RECEIVER				
Input Signal Squelch Level	-	0.5	-	V
Data Decision Threshold	-	70	-	% of peak

Notes: 8. Input signal to TCLK is jitter free.
9. Measured with a nonpolarized 0.47 µF capacitor in series with the primary of the transmit transformer. Not production tested. Parameters guaranteed by design and characterization.

T1 SWITCHING CHARACTERISTICS

(T_A = - 40 ° to 85 °C; V+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
TCLK Frequency	f_{in}	-	1.544	-	MHz
RTIP/RRING Rising to R1/R2 Rising (Note 10)	t_{dr}	20	45	150	ns
RTIP/RRING Falling to R1/R2 Falling (Note 10)	t_{df}	60	135	370	ns
Rise Time, All Digital Outputs (Note 11)	t_r	-	-	30	ns
Fall Time, All Digital Outputs (Note 11)	t_f	-	-	30	ns
TPOS/TNEG to TCLK Falling Setup Time	t_{su}	50	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time	t_h	25	-	-	ns

Notes: 10. Both rising and falling delays will exhibit similiar tendencies, that is, for fast process, times will tend towards minimum delay times; slower process results in longer delays.
11. At max load of 4.0 mA and 50 pF.

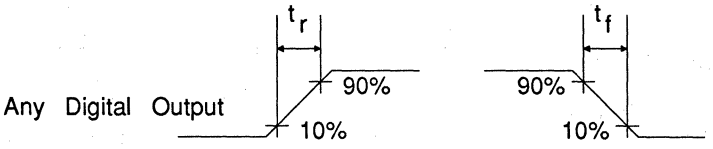


Figure 1. - Signal Rise and Fall Characteristics

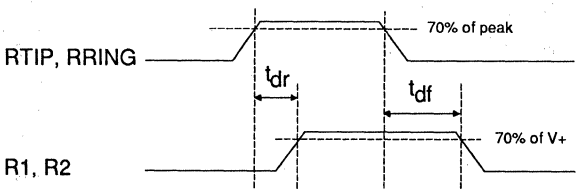


Figure 2. - Receiver Switching Characteristics

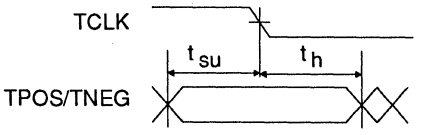


Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS6152 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a 1:1.36, step-up transformer is required. The line driver is designed to drive a 54 Ω equivalent load.

When any transmit control pin (TAOS or LEN0/1/2) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter options are: HIGHZ which places TTIP, TRING, R1, and R2 in a high impedance state, and TAOS which transmits an AMI-encoded all ones on TTIP/TRING.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. These phases are then used to trigger different portions of the output waveform. For T1 applications, the line length selection offers a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS6152 modifies the output pulse to meet the requirements of Compatibility Bulletin 119. The exact pulse shape achieved at the DSX-1 can be effected by details of the board layout, transformer selection, and other factors. For cable types other than ABAM, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	APPLICATION
0	1	1	0-133	DSX-1 ABAM (AT&T 600B Or 600C)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	1		Reserved
0	1	0		
0	0	0	Part 68, Option A	CSU
0	1	1	T1C1.2	

Table 1 - Line Length Selection

The T1 CSU pulse shapes meet FCC Part 68 for 0dB line build out and future ECSA T1C1.2 pulse shapes as shown in Table 1.

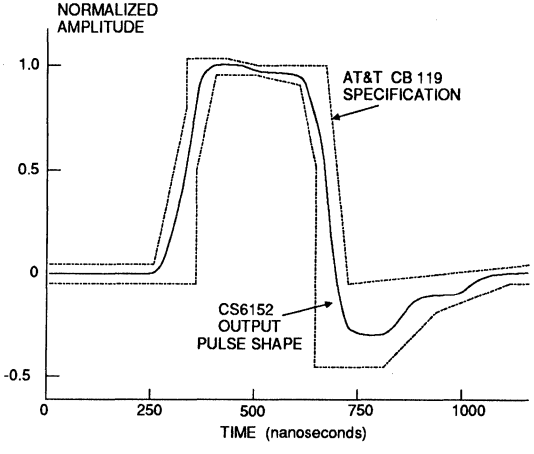


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6152 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for between 31 to 63 TCLK cycles, the DPM pin goes high. If TCLK stops, DPM can not change state.

To provide immunity from spurious DPM reports, the following application procedure is recommended: If the controller on the T1 line card detects that DPM has gone high, the controller should reconfirm that DPM is still high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can only occur when ones density is very low.

Whenever more than one CS6152 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS6152 monitor performance of a neighboring CS6152 device, rather than having it monitor its own performance.

Receiver

The receiver converts AMI (Alternate Mark Inversion) coded signals to binary (dual unipolar) data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators detect pulses on RTIP and RRING. Comparator thresholds are dynamically established by peak detectors to be 70% of the peak signal level. The comparator outputs are output on R1 and R2 respectively. A positive pulse on RTIP results in a positive pulse on R1. A positive pulse on RRING results in a positive pulse on R2. The pulses are typically stretched 90 ns before being output on R1 and R2.

Squelch control in the receiver will force R1 and R2 low if the inputs on RTIP and RRING are below the squelch level of 0.5 volts.

Power On Reset

Upon power-up, the CS6152 is held in a static state until the supply crosses a threshold of approximately 3 volts. When this happens, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay line used in the transmit section commences. The delay line can be calibrated only if the transmit clock is present. The initial calibration should take less than 20 ms after TCLK is applied.

In operation, the delay line is continuously calibrated, making the performance of the device independent of power supply or temperature variations, and eliminating the need to reset a CS6152 when in operation.

Power Supply

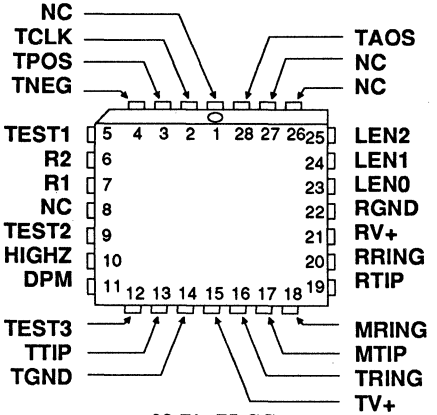
The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for proper operation of the analog circuits in the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1µF capacitor should be connected between TV+ and TGND, and a 0.1µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as close as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap bread-boarding of the CS6152 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

TRANSMIT CLOCK	TCLK	1	24	TAOS	TRANSMIT ALL ONES SELECT
TRANSMIT POSITIVE PULSE	TPOS	2	23	LEN2	BIT 2 OF LINE LENGTH SELECT
TRANSMIT NEGATIVE PULSE	TNEG	3	22	LEN1	BIT 1 OF LINE LENGTH SELECT
FACTORY TEST1	TEST1	4	21	LEN0	BIT 0 OF LINE LENGTH SELECT
RECEIVED SIGNAL 2	R2	5	20	RGND	RECEIVE GROUND
RECEIVED SIGNAL 1	R1	6	19	RV+	RECEIVE V+ (+5VDC)
FACTORY TEST2	TEST2	7	18	RRING	RECEIVE RING
HIGH IMPEDANCE	HIGHZ	8	17	RTIP	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	DPM	9	16	MRING	MONITORED RING
FACTORY TEST3	TEST3	10	15	MTIP	MONITORED TIP
TRANSMIT TIP	TTIP	11	14	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	12	13	TV+	TRANSMIT V+ (+5VDC)

24-Pin DIP



28-Pin PLCC

Power Supplies

TV+ - Positive Power Supply, Transmit Drivers.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Control

HIGHZ - High Impedance.
Setting HIGHZ to a logic 1 causes TTIP, TRING, DPM, R1, and R2 to enter a high impedance state. This pin is internally pulled down, so the device will be in normal operating mode if this pin is left floating.

TAOS - Transmit All Ones Select.
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

LEN0, LEN1, LEN2 - Line Length Selection.
Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TEST1, TEST2, TEST3 - Factory Test1, 2, 3.
Reserved for factory testing, TEST1 must be tied low for normal operation. TEST2 and TEST3 should be left floating.

Inputs

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data.
Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted. If the clock signal is removed from TCLK, then TPOS and TNEG should both be logic low during last falling edge of TCLK.

RTIP, RRING - Receive Tip, Receive Ring.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 1:2, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data is buffered and output on R1 and R2.

MTIP, MRING - Monitored Tip, Monitored Ring.

These pins are normally connected to TTIP and TRING and monitor the output of a CS6152. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status

DPM - Driver Performance Monitor.

If no signal is present on MTIP and MRING for between 31 to 63 clock cycles, DPM goes to a logic 1 until the first detected signal. If TCLK is static, DPM cannot change state.

Outputs

TTIP, TRING - Transmit Tip, Transmit Ring.

The AMI signal is driven to the line through these pins. This output is designed to drive a 54 Ω load. A 1.36:1 step-up transformer is required as shown in Figure A1.

R1, R2 - Received Signal 1, Received Signal 2.

RTIP and RRING inputs are buffered and stretched before being output digitally on R1 and R2 respectively.

Miscellaneous

NC - No Connection (PLCC package only) Pins, 1, 8, 26, 27.

APPLICATIONS

Line Interface

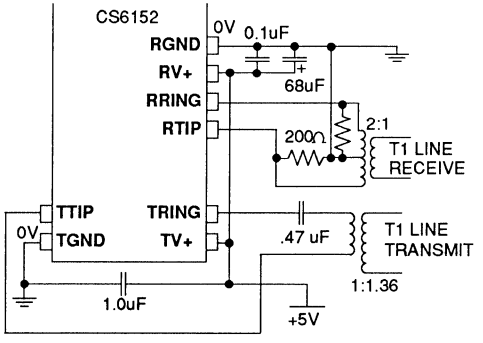


Figure A1. - Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS6152 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS6152 side. These resistors provide the 100 Ω termination for the T1 line.

To save on power consumption under normal operating conditions, the line driver outputs, TTIP and TRING, are forced into a high impedance state during the transmission of a space (zero) on to the line. Just prior to transmitting a mark (one), the driver outputs are enabled. The transformer interacting with the driver can cause a slight voltage difference (< 200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a 0.47 µF non-polarized capacitor in series with the primary of the transformer.

Transformers

Transformers listed below have been found to be suitable for use with the CS6152. Receive transformer specifications are not as critical.

Manufacturer	Part#
Transmit + Receive	
Pulse Engineering	PE-64952
Schott	68114920
Transmitter	
Schott	67112020
Midcom	671-5961
Pulse Engineering	PE-64937
Receiver	
Pulse Engineering	PE-64931
Schott	67115100
Midcom	671-5832
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001

A 1:1.36 turns ratio transformer is required for the transmit side. The receiver side transformer is normally 1:2 turns ratio. However, the receiver side transformer can be 1:1.36 if it is necessary to have only 1 type of transformer, at the expense of a few dB of receive sensitivity. The input squelch level of the CS6152 is set at 0.5 V, with a 1:2 transformer. Using a 1:1.36 transformer will lower the effective squelch level.

•Notes•

Semiconductor Corporation

CS61534

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Transparent to AMI Polarity
- Diagnostic and Performance Monitoring Features
- Selectable Hardware or Host Processor Modes
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61534 combines the analog transmit and receive line interface functions for a PCM system interface in one 28 pin device. The PCM line interface operates from a single 5 Volt supply, is transparent to the PCM framing format, and can work with ABAM and other cable types.

Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet in T1 applications. Maximum range is greater than 450 meters. The transmitter users an elastic store to remove jitter from the outgoing data prior to transmission.

3

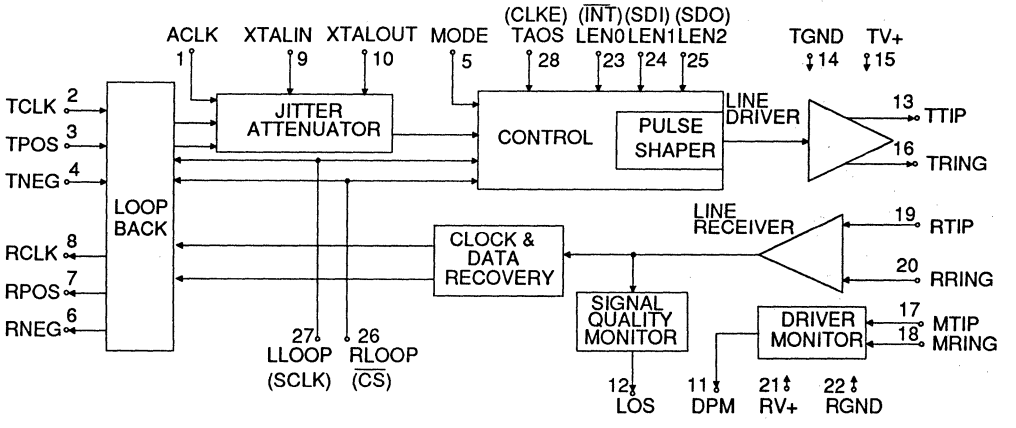
Applications

- Interfacing Network Equipment to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexers, Data PBX's and LAN Gateways to a channel Service Unit or T1 Modem.

ORDERING INFORMATION

CS61534-IP	28 Pin Plastic DIP	(T1 only)
CS61534-IP1	28 Pin Plastic DIP	(T1 & CEPT)
CS61534-IL	28 Pin J-lead PLCC	(T1 only)
CS61534-IL1	28 Pin J-lead PLCC	(T1 & CEPT)
CS61534-ID	28 Pin CERDIP	(T1 only)
CS61534-ID1	28 Pin CERDIP	(T1 & CEPT)

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 RV+ + 0.3	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature Industrial Temperature Range	T_A=	-40	25	85	°C
Total Power Dissipation (Note 4) 100% ones density & max. line length @ 5.25V	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25 Ω load over operating temperature range. Includes CS61534 and load.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 5, 6) Pins 1-5, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 5, 6) Pins 1-5, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 5, 6) I_{OUT}=-40 uA Pins 6-8, 11, 12, 23, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 5, 6) I_{OUT}= 1.6 mA Pins 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA
High Impedance Leakage Current Pin 25 (Note 5)		-	-	±10	uA

Notes: 5. Functionality of pins 23 and 25 depends on the mode. See Host/Hardware mode description.
6. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver Sensitivity Below DSX-1		-10	-	-	dB
Jitter Attenuation Curve Corner Frequency	(Note 7)	-	-	50	Hz
Receiver Jitter Tolerance	(Note 8)				
1.544 MHz:	8kHz - 40kHz	0.1	-	-	U.I.
	10Hz - 500Hz	5	-	-	U.I.
2.048 MHz:	18kHz - 100kHz	0.2	-	-	U.I.
	20Hz - 2.4kHz	1.5	-	-	U.I.
Input Jitter Tolerance -	Transmitter	7.0	-	-	U.I.
Loss of Signal Threshold		-	0.5	-	V
Transmitter Output Load	(Note 9)	-	25	-	ohms
AMI Output Pulse Amplitudes					
Line Length Selection LEN2/1/0 = 0/0/0 (Measured at xfmr output; 0/0/0 see Figure 7)		2.7	3.0	3.3	V
All Line Length settings except, LEN2/1/0 = 0/0/0 (Measured at the DSX; Normalization factor for Figure 6)		2.4	3.0	3.6	V
Power in 2kHz band about 772kHz	(Note 10)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544 MHz (referenced to power at 772kHz)	(Note 10)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 10)	-	0.2	0.5	dB

Notes:
7. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter.
8. For CERDIP ICs, assumes IC is operated within -70 ° to +70 °C of reset temperature. For plastic ICs, assumes IC is operated within -25 ° to +40 °C of reset temperature (meets Bellcore central office specification: TR-EOP-000063 NEBS). For all packages, assumes IC is operated within 0.1V of reset V+. Input data pattern is quasi-random. For 1.544 MHz: (2↑20)-1 with 1-in-15. For 2.048 MHz: (2↑15)-1 as defined in CCITT 0.151. For frequencies not specified above, the jitter tolerance will be better than the AT&T 43802 line or the CCITT G.823 line shown in Figure 10.
9. Transmitter is a low impedance voltage source. Transmitter performance is typical with a 25Ω load for T1 applications, which is determined by the 2:1 turns ratio of transformer and 100 Ω line impedance.
10. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.

3

T1 SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 11)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 12)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width		t_{pwh}	-	324	-	ns
	(Note 13)	t_{pwl}	-	324	-	ns
Duty Cycle	(Note 14)		-	50	-	%
Rise Time, All Digital Outputs	(Note 15)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 15)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	274	-	ns
Reset Pulse Duration			0.2	-	2000	us

Notes: 11. Crystal must meet specifications described in CXT6176 data sheet.
12. ACLK provided by an external source.
13. The sum of the pulse widths must always meet the frequency specifications.
14. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
15. At max load of 1.6 mA and 50 pF.

CCITT SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 16)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{in}	-	2.048	-	MHz
ACLK Frequency	(Note 17)	f_{out}	-	2.048	-	MHz
RCLK Pulse Width		t_{pwh}	-	244	-	ns
	(Note 18)	t_{pwl}	-	244	-	ns
Duty Cycle	(Note 19)		-	50	-	%
Rise Time, All Digital Outputs	(Note 20)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 20)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	194	-	ns
Reset Pulse Duration			0.2	-	2000	us

Notes: 16. Crystal must meet specifications described in CXT8192 data sheet.
17. ACLK provided by an external source.
18. The sum of the pulse widths must always meet the frequency specifications.
19. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
20. At max load of 1.6 mA and 50 pF.

SWITCHING CHARACTERISTICS - HOST MODE (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ.	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	250	-	-	ns
SCLK High Time	t_{ch}	250	-	-	ns
SCLK Rise and Fall Time	t_r , t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 21)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns

Note: 21. Output load capacitance = 50 pF.

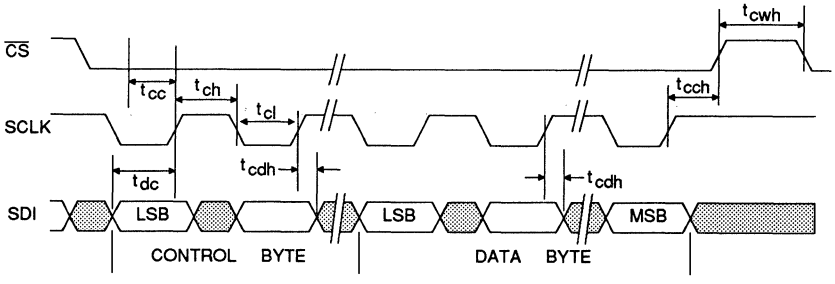


Figure 1. - Serial Port Write Timing Diagram

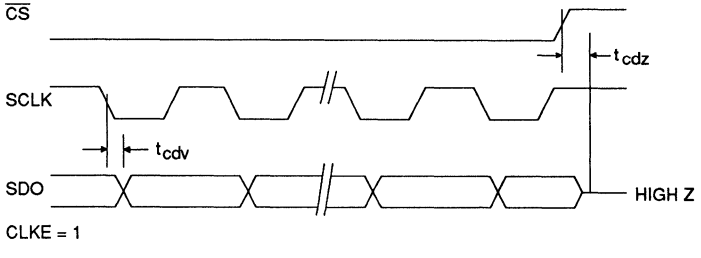


Figure 2. - Serial Port Read Timing Diagram

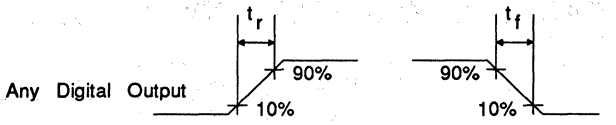


Figure 3. - Signal Rise and Fall Characteristics

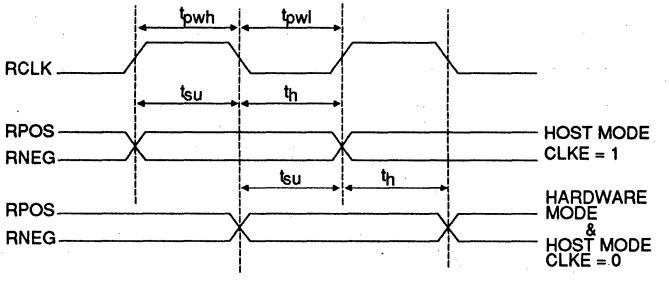


Figure 4. - Recovered Clock and Data Switching Characteristics

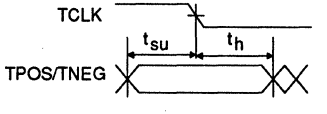


Figure 5. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a PCM transceiver and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

The CCITT pulse shape and T1 pulse shapes for line lengths from 0 to 655 feet (as measured from the CS61534 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver is a low-impedance voltage source designed to drive a 25 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	1	1	0-220	MAT and ICCT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM (AT&T 600B or 600C)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	0	G.703	2.048 MHz CCITT

Table 1. Line Length Selection

Transmit Line Length Selection

For T1 applications, the line length selection supports both a three partition arrangement for ICOT and MAT cable, and a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS61534 modifies the output pulse to meet the requirements of Compatibility Bulletin 119 and TR-TSY-000009. A typical output pulse is shown in Figure 6.

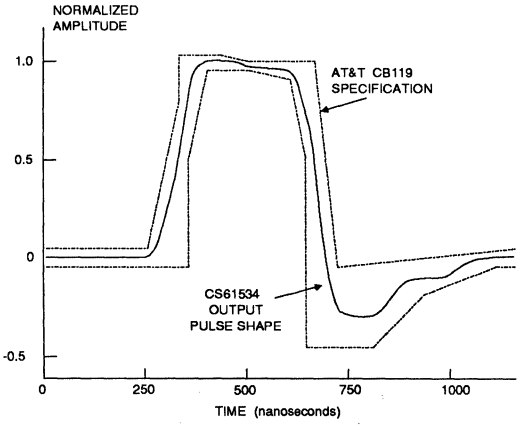


Figure 6. Typical Pulse Shape at DSX-1 Cross Connect

The remaining line length selection is for CCITT options. Transformer and resistor values depend on whether the coax or shielded cable is used, as shown in the *Applications* section at the back of this data sheet. The CCITT pulse shape meets the template shown in Figure 7, and the requirements of Table 2 for the given load conditions.

Transmit Jitter Attenuator

The CS61534 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a signal. Figure 8 shows a family of curves which show the jitter attenuation achieved by the CS61534 at T1 data rates. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The

	For coaxial cable, 75 ohm load and transformer specified in Table A2.	For shielded twisted pair, 120 ohm load and transformer specified in Table A2.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

Table 2. CCITT G.703 Pulse Specifications

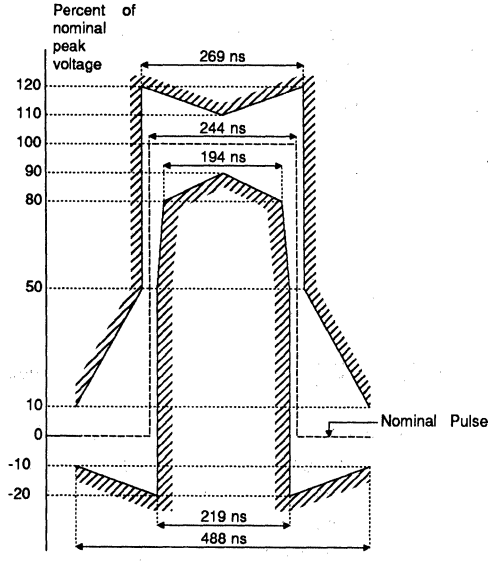


Figure 7. Mask of the Pulse at the 2048 kbps Interface

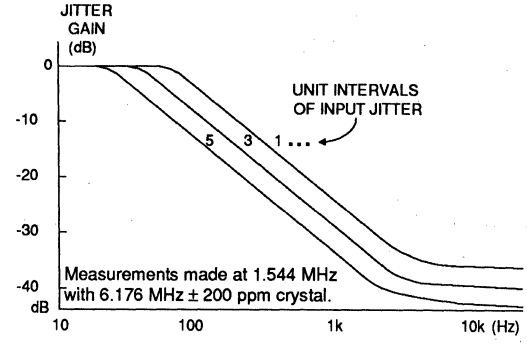


Figure 8. Jitter Attenuation Curves

more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 9 and 10.

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, (8.192 MHz for PCM-30 rates), and have a pull range, in the oscillator circuit, that is

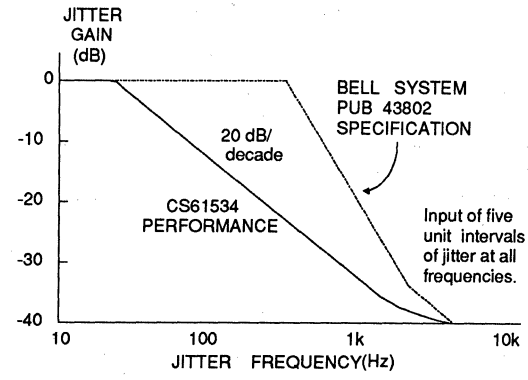


Figure 9. Jitter Attenuation Characteristics

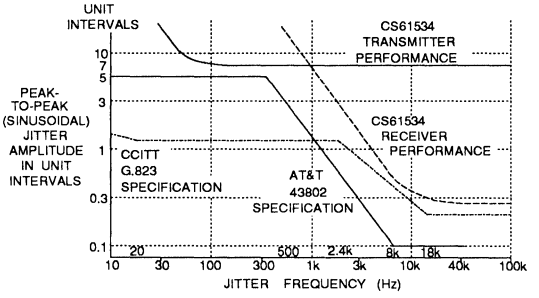


Figure 10. Typical Input Jitter Tolerance

sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is *exactly* four times the TCLK frequency. Remote loopback should not be used if the jitter attenuator is disabled.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock, ACLK. In this mode, the TPOS, TNEG and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of DSX-1/PCM-30 cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61534 side. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802 and CCITT G. 823, (see Figure 10).

The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61534, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until the ICO is near the reference frequency. This current is then held constant. The FPLL is controlled, small signal, by the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage as shown in the Analog Specifications table, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness. Resetting the CS61534 will optimize receiver performance for the operating power supply and temperature.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

X= Don't care

Table 3. Data Output / Clock Relationship

falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 31 bit periods. When a loss of signal is detected, RPOS and RNEG are not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output but may drift up to 6% from the nominal frequency. Note that in the host mode, LOS is simultaneously available from pin 12 and the register.

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. The transmit data and clock signals (TPOS, TNEG and TCLK) are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case AMI-coded continuous ones are transmitted on the line at the rate determined by ACLK.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 4). The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). Bipolar violations are passed unchanged through the CS61534 during remote loopback.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS61534 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TPOS & TNEG	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 4. Interaction of RLOOP and TAOS

CS61534. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, the DPM pin goes high.

To provide immunity from spurious DPM reports, the following application procedure is recommended: If the controller on the line card detects that DPM has gone high, the controller should reconfirm that DPM is still high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where

DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can occur only when ones density is very low.

Whenever more than one CS61534 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS61534 monitor performance of a neighboring CS61534 device, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

Reset

The CS61534 initiates internal reset procedures either on power up or in response to a reset request. After initial power up, the device will delay for approximately 10 ms before initiating the training procedure for the FPLL. It is advisable to issue a reset request after the power supply has stabilized and signals have been applied to the device to ensure that conditions on the chip are stable before the FPLL training takes place. Training the FPLL takes at most 43ms, but typically requires less than half that amount of time. These conditions should also be adhered to if temporary loss of power supply occurs.

In the Hardware Mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. The device will first clear its data registers then initiate the FPLL training procedure which will be complete within 53 ms.

During the reset procedure, the loss of signal indicator, LOS, is high. Once the reset procedures are completed, the loss of signal indicator goes low signifying that normal operation of the device has begun.

Mode of Operation

The CS61534 can be operated in two modes, the hardware mode and the host mode. In the hardware mode, discrete pins are used to interface the device's control functions and status information. In the host mode, the CS61534 is connected to a host processor and a serial data bus is used for input and output of control and status information. There are six dual function pins whose functionality is determined by the mode pin, MODE. Table 5 shows the pin definitions.

PIN #	MODE	
	HARDWARE	HOST
PIN 23	LEN0	$\overline{INT}$
PIN 24	LEN1	SDI
PIN 25	LEN2	SDO
PIN 26	RLOOP	$\overline{CS}$
PIN 27	LLOOP	SCLK
PIN 28	TAOS	CLKE

Table 5. Pin Definitions

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no

sooner than 50 ns after the falling edge of the 16th SCLK cycle, and must go high before the rising edge of the 24th SCLK cycle.

Figure 11 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. Data bit D7 is held until the rising edge of the 17th clock cycle.

An address/command byte, shown in Table 6, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61534 responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 6. Address / Command Byte

The data register, shown in Table 7, can be read/written by the serial port. Data is input/output on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are read only. During a write to the register, the CS61534 ignores the first two bits of the data byte. SDO goes to a high-impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

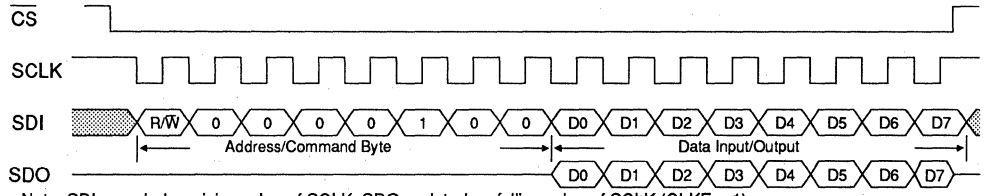
LSB: first bit in or out	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in or out	7	TAOS	Transmit All Ones Select

Table 7. Data Register

Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61534 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

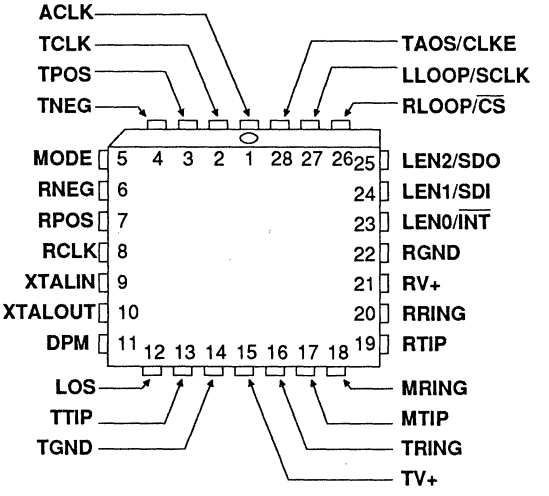


Note: SDI sampled on rising edge of SCLK; SDO updated on falling edge of SCLK (CLKE = 1).

Figure 11. Input / Output Timing

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLK	1	28	TAOS/CLKE — TRANSMIT ALL ONES / CLOCK EDGE
TRANSMIT CLOCK	TCLK	2	27	LLOOP/SCLK — LOCAL LOOPBACK / SERIAL CLOCK
TRANSMIT POSITIVE PULSE	TPOS	3	26	RLOOP/$\overline{CS}$ — REMOTE LOOPBACK / CHIP SELECT
TRANSMIT NEGATIVE PULSE	TNEG	4	25	LEN2/SDO — LINE / SERIAL DATA OUT
MODE SELECTION	MODE	5	24	LEN1/SDI — LENGTH / SERIAL DATA OUT
RECEIVED NEGATIVE PULSE	RNEG	6	23	LEN0/$\overline{INT}$ — SELECT / ALARM INTERUPT
RECEIVED POSITIVE PULSE	RPOS	7	22	RGND — RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+ — RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	XTALIN	9	20	RRING — RECEIVE RING
CRYSTAL CONNECTION	XTALOUT	10	19	RTIP — RECEIVE TIP
DRIVER PERFORMANCE MONITOR	DPM	11	18	MRING — MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP — MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING — TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+ — TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (8.192 MHz for CCITT applications) crystal should be connected across these pins. If desired, an externally generated 6.176 MHz (8.192 MHz for CCITT) clock signal may be input to XTALIN, pin 9; XTALOUT, pin 10, should be left floating. Overdriving the oscillator with an external source disables the jitter attenuator. This externally generated clock must be *exactly* four times the frequency of the TCLK signal.

Control

MODE - Mode Select, Pin 5.

Setting MODE to logic 1 puts the CS61534 in the host mode. In the host mode, a serial control port is used to control the CS61534 and determine its status. Setting MODE to logic 0 puts the CS61534 in the hardware mode, where configuration and status are controlled by discrete pins. MODE defines the status of pins 23 through 28.

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored. If the oscillator is being driven with a 4x clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.

Goes low when received signal is lost (LOS is high), or the transmitter driver has failed (DPM is high), to flag the host processor. $\overline{\text{INT}}$ will stay low until the fault condition goes away. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.

Data for the on-chip registers and is sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.

Status and control information from the on-chip registers. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or $\overline{\text{CS}}$ is high.

CLKE - Clock Edge, Pin 28.

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.

Clock used to read or write the serial port registers.

$\overline{\text{CS}}$ - Chip Select, Pin 26.

Pin must transition from high to low to read or write the serial ports.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 (or 2.048) MHz clock. The frequency of ACLK determines the rate at which TAOS is output.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1. Data and clock are recovered and output on RPOS/RNEG and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61534. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{INT}$ pin in the host mode is used, and the monitor is not used, input a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-voltage level. This clock frequency can range from 100 kHz to the TCLK frequency.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 31 clock cycles without a detected one. LOS returns to logic 0 when signal returns.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

Data and clock are recovered from the RTIP and RRING inputs are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, approximately 4.4 Ω of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

APPLICATIONS

Line Interface

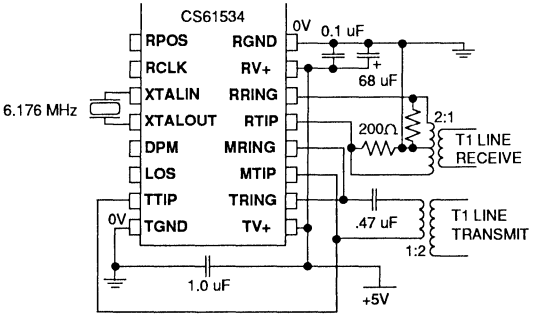


Figure A1. Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS61534 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS61534 side. These resistors provide the 100 Ω termination for the T1 line. When terminating twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

Figure A2 shows the configuration needed for transmitting data at 2.048 MHz onto a 75 Ω coax cable. The 2.2 Ω resistors serve two functions.

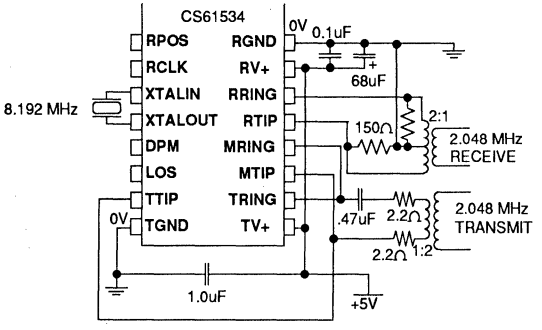


Figure A2. Configuration for Transmitting onto 75 Ω Coax

First, they provide the appropriate 25 Ω load to TTIP and TRING. Second, the resistors attenuate the signal slightly to meet the CCITT pulse amplitude requirements. Note that these 2.2 Ω resistors should not be used when interfacing to CCITT 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61534. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for PCM-30 applications.

Transformers

Transformers listed in Table A1 have been found to be suitable for use with the CS61534.

Figure A3 shows the connections for some of the recommended transformers for the transmitter. Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1) ± 5%,

Primary inductance: 600 µH min measured at 772 kHz

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted

Secondary leakage inductance: 0.4 µH max at 772 kHz

Interwinding capacitance: 23 pF max, primary to secondary

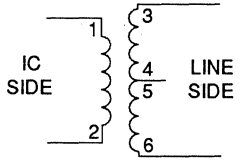
ET-Constant: 16 V-µs minimum for T1; 12 V-µs for CEPT

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this ef-

Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott Corp.	67115100 & 67124670
Schott Corp.	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the above Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A1. Suitable Transformers



Bell Fuse 0553-5006-IC
Schott Corp. 67115100
Pulse Engineering 5764 & PE-64931

Figure A3.Some Recommended Transmitter/Transformer Connections

fect be eliminated by inserting a 0.47uF non-polarized capacitor in series with the primary of the transmit transformer.

Receive Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A4. In the host mode, the inverter is not needed if CLKE is high.

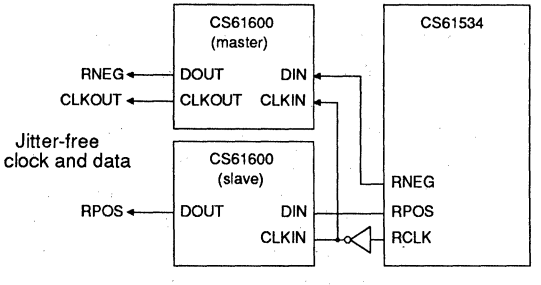


Figure A4. Receive Jitter Attenuation

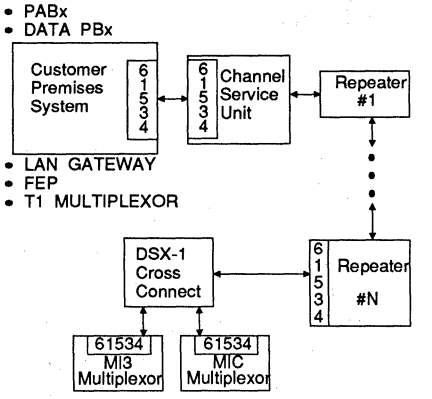


Figure A5. Application of CS61534

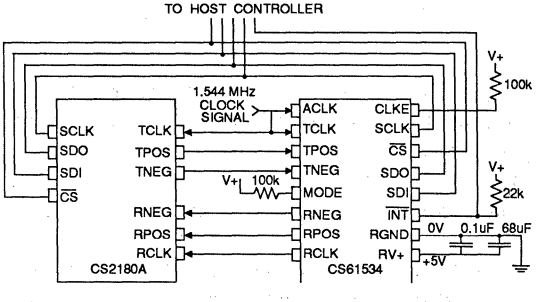


Figure A6. Interfacing the CS61534 with a CS2180A

Applicable Systems

Figure A5 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A5, the CS61534 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and in network equipment that connects to a DSX-1 cross connect.

Interfacing The CS61534 With T1 Digital Transceivers

To interface with the CS2180A, connect the devices as shown in Figure A6. In this case, the CS61534 and CS2180A are in host mode controlled by a microprocessor serial interface. If the CS61534 is used in hardware mode, then the CS61534 RCLK output must be inverted before being input to the CS2180A.

Semiconductor Corporation

CS61535A

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes

General Description

The CS61535 and CS61535A combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device. The line interface unit (LIU) operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. The transmitter uses a 32-bit elastic store to remove jitter from the transmit data.

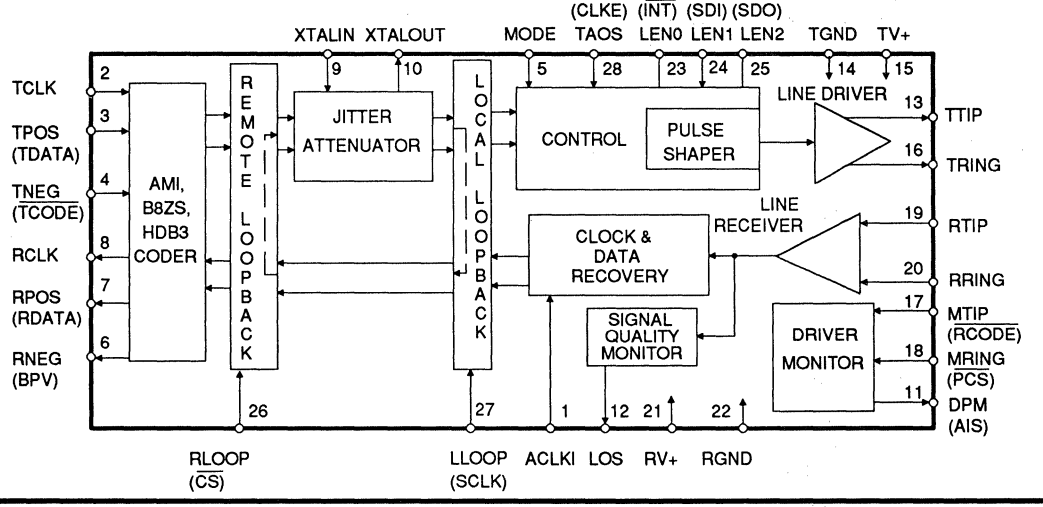
Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to PCM-30 links.

Ordering Information

CS61535A-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS61535A-IL1	28 Pin PLCC (j-leads)	T1 & PCM-30
CS61535-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS61535-IL1	28 Pin PLCC (j-leads)	T1 & PCM-30

Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 (RV+) + 0.3	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within the range of -6V to (RV+)+ 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
CS61535A Power Consumption (Note 4,5)	P_C	-	290	350	mW
CS61535A Power Consumption (Note 4,6)	P_C	-	175	-	mW
CS61535 Power Consumption (Note 4,5)	P_C	-	620	760	mW
CS61535 Power Consumption (Note 4,6)	P_C	-	400	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50pF capacitive load.
5. Assumes 100% ones density and maximumum line length at 5.25V.
6. Assumes 50% ones density and 300 ft. line length at 5.0V.

CS61535 DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ , RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-5, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-5, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 7) I_{OUT} =-40 uA PINS 6-8, 11,12, 23, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 7) I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	uA

Notes: 7. Output drivers will output CMOS logic levels into a CMOS load. Functionality of pins 23 and 25 depends on the mode. See Operating Mode description.

CS61535A DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ , RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 8,9) PINS 1-4, 17,18, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 8,9) PINS 1-4, 17, 18, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 8) I_{OUT}=-40 uA PINS 6-8, 11, 12, 23, 25	V_{OH}	4.0	-	-	V
Low-Level Output Voltage (Note 8) I_{OUT}= 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	uA
Low-Level Input Voltage, Pin 5	V_{IL}	-	-	0.2	V
High-Level Input Voltage, Pin 5	V_{IH}	(RV+)-0.2	-	-	V
Mid-Level Input Voltage, Pin 5 (Note 10)	V_{IM}	2.3	-	2.7	V

Notes: 8. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40 µA). Functionality of pins 23 and 25 depends on the mode. See Operating Mode description.
9. Pins 17 and 18 have digital characteristics in the Extended Hardware Mode.
10. As an alternative to supplying a 2.3-to-2.7 V input, this pin may be left floating.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+ , RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
DRIVER PERFORMANCE MONITOR					
CS61535A Sensitivity: Differential Voltage Required for Detection					
With one input at 1.5V		-	0.75	-	V
With one input at 0V		-	2.0	-	V
RECEIVER					
CS61535A RTIP/RRING Input Impedance		-	50k	-	Ohms
Sensitivity Below DSX (0dB = 2.4V)		-10	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold	T1 pulse settings	-	65	-	% of peak
	PCM-30 LEN2/1/0 = 000	-	50	-	
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	10kHz - 100kHz	0.4	-	-	UI
	2kHz	6.0	-	-	
(Note 11)	10Hz and below	300	-	-	

Notes: 11. Jitter tolerance increases at lower frequencies. See Figure 12.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C;TV+, RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes	(Note 12)				
PCM-30, 75 Ohm	(Note 13)	2.14	2.37	2.6	V
PCM-30, 120 Ohm	(Note 14)	2.7	3.0	3.3	V
T1	(Note 15)	2.4	3.0	3.6	V
Load Presented To Transmitter Output	(Note 12)				
	CS61535A	-	75	-	Ohms
	CS61535	-	25	-	Ohms
Jitter Added During Remote Loopback (Note 16)	10Hz - 8kHz	-	0.005	-	UI
	8kHz - 40kHz	-	0.008	-	UI
	10Hz - 40kHz	-	0.010	-	UI
	Broad Band	-	0.015	-	UI
Power in 2kHz band about 772kHz	(Note 17)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544 MHz (referenced to power in 2kHz band at 772kHz)	(Note 17)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 17)	-	0.2	0.5	dB
Transmitter Input Jitter Tolerance	(Note 18)	12	23	-	UI
Jitter Attenuation Curve Corner Frequency	(Note 18)	-	6	-	Hz
CS61535A PCM-30 Transmitter Return Loss	(Notes 12, 19)				
	51 kHz to 102 kHz	8	-	-	dB
	102 kHz to 2.048 MHz	14	-	-	dB
	2.048 MHz to 3.072 MHz	10	-	-	dB

Notes: 12. Using transformer as recommended in the Application Section.

13. These amplitudes, measured at the output of the transformer, are for line length settings LEN2/1/0=0/0/0 (see Figure 9).
14. These amplitudes, measured at the output of the transformer, are for line length settings LEN2/1/0 = 0/0/0 (see Figure 9) or LEN2/1/0 = 0/1/0.
15. These amplitudes, measured at the DSX-1 Cross-Connect, are for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1 (see Figure 8).
16. Input signal to RTIP/RRING is jitter free.
17. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
18. The jitter attenuator in the transmit path has circuitry to prevent FIFO overflow or underflow. Tolerance parameters shown reflect jitter levels at which overflow/underflow circuit will be inactive. The circuit attenuates jitter at 20dB/decade above the corner frequency. See Figure 10. When more than 12 UI's are input to the attenuator, output jitter can increase significantly. See discussion in Wander and Jitter Attenuator section.
19. Return loss = 20 log $_{10}$ ABS($(z_1+z_0)/(z_1-z_0)$) where z_1=impedance of the transmitter, and z_0 = impedance of line load, measured with a repeating 1010 data pattern.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+, RV+ = 5.0V ± 5%;

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
ACLKI Frequency	(Note 20)	f_{aclki}	-	1.544	-	MHz
CS61535A RCLK Cycle Width When Phase Locked	(Notes 21, 22, 24)	t_{pw1} t_{pwh1} t_{pwl1}	320 130 100	648 190 458	980 240 850	ns ns ns
CS61535 RCLK Cycle Width When Phase Locked	(Notes 21, 22, 24)	t_{pw1} t_{pwh1} t_{pwl1}	348 - 100	648 508 140	980 - -	ns ns ns
CS61535A RCLK Duty Cycle	(Notes 21, 22, 24)	t_{pwh1} / t_{pw1}	-	29	-	%
CS61535 RCLK Duty Cycle	(Notes 21, 22, 24)	t_{pwh1} / t_{pw1}	-	78	-	%
Rise Time, All Digital Outputs	(Note 23)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 23)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Setup Time	(Notes 22, 24)	t_{su1}	50	-	-	ns
RCLK to RPOS/RNEG Hold Time	(Notes 22, 24)	t_{h1}	50	-	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

Notes: 20. ACLKI provided by an external source or TCLK.
21. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
22. Max & Min RCLK duty cycles and cycle widths and RX setup and hold times are for worst case jitter conditions: i.e. 0.4 UI AMI data displacement for T1 or 0.2 UI AMI data displacement for CCITT 2.048 MHz. See text section on *Jitter and Recovered Clock.*
23. At max load of 1.6 mA and 50 pF.
24. Not production tested. Guaranteed by design and/or characterization.

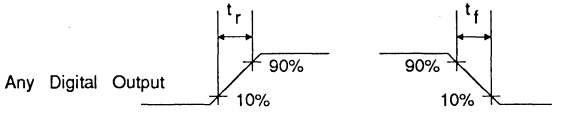


Figure 1. - Signal Rise and Fall Characteristics

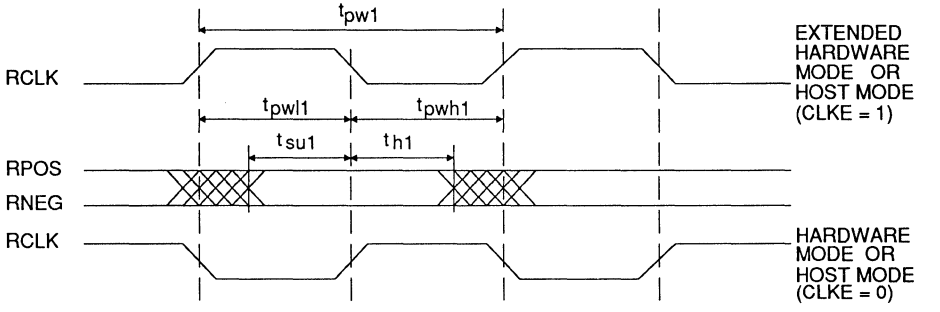


Figure 2. - Recovered Clock and Data Switching Characteristics

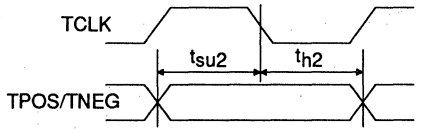


Figure 3. - Transmit Clock and Data Switching Characteristics

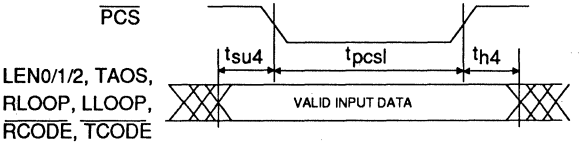


Figure 4. - Extended Hardware Mode Parallel Chip Select Timing Diagram

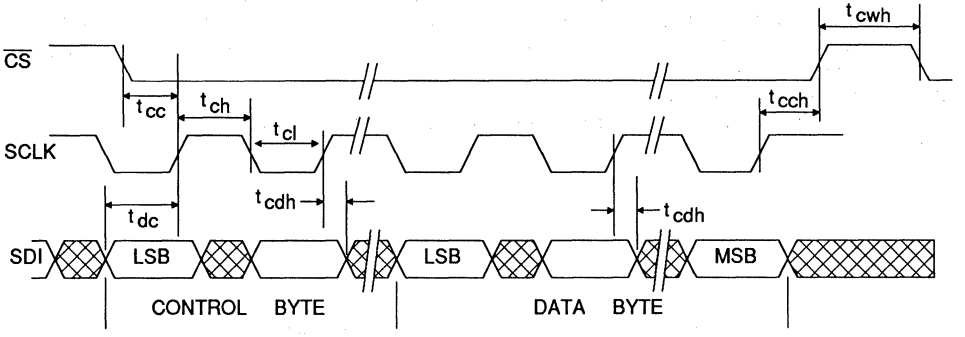


Figure 5. - Serial Port Write Timing Diagram

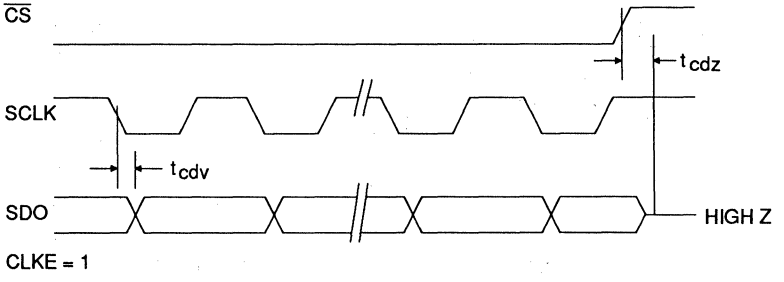


Figure 6. - Serial Port Read Timing Diagram

PCM-30 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+, RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
ACLKI Frequency	(Note 20)	f_{aclki}	-	2.048	-	MHz
CS61535A RCLK Cycle Width		t_{pw1}	310	488	670	ns
When Phase Locked		t_{pwh1}	90	140	190	ns
	(Notes 21, 22, 24)	t_{pwl1}	120	348	500	ns
CS61535 RCLK Cycle Width		t_{pw1}	310	488	670	ns
When Phase Locked		t_{pwh1}	-	348	-	ns
	(Notes 21, 22, 24)	t_{pwl1}	100	140	-	ns
CS61535A RCLK Duty Cycle	(Notes 21, 22, 24)	t_{pwh1}/t_{pw1}	-	29	-	%
CS61535 RCLK Duty Cycle	(Notes 21, 22, 24)	t_{pwh1}/t_{pw1}	-	71	-	%
Rise Time, All Digital Outputs	(Note 23)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 23)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Setup Time	(Notes 22, 24)	t_{su1}	50	-	-	ns
RCLK to RPOS/RNEG Hold Time	(Notes 22, 24)	t_{h1}	50	-	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ , RV+ = 5.0V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ.	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	tcl	240	-	-	ns
SCLK High Time	tch	240	-	-	ns
SCLK Rise and Fall Time	t_r , tf	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	tcc	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	tcch	50	-	-	ns
$\overline{CS}$ Inactive Time	tcwh	250	-	-	ns
SCLK to SDO Valid (Note 22)	tcdv	-	-	200	ns
$\overline{CS}$ to SDO High Z	tcdz	-	100	-	ns
Input Valid to $\overline{PCS}$ Falling Setup Time	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	t_{pcsl}	250	-	-	ns

3

THEORY OF OPERATION

Enhancements in CS61535A

The performance improvements made to the 'A' version of the CS61535 are the following:

- 50% reduction in power consumption
- Transmitter output impedance matches line (during transmission of both marks & spaces) achieving return loss of greater than 14dB
- Addition of optional AMI, B8ZS, HDB3 line code encoder/decoder
- AIS (all ones) detection
- Upon power up, RCLK immediately starts and LOS (loss of signal) is set high
- When the transmitter senses the absence of a signal on TCLK, TTIP and TRING are forced to zero.
- The Loss of Signal condition is exited upon recognition of 12.5% one's density (4-of-32 and no more than14 consecutive zeros).
- The Driver Performance Monitor operates over a wider range of input signal levels.
- Elimination of the requirement that a reference clock be input on the ACLKI pin.

The same PCB can be used for both the CS61535 and CS61535A. When converting an existing CS61535 PCB to use the CS61535A, the only change required is to update the parts list to specify the new IC (CS61535A) and to specifiy a transmitter transformer with a different turns ratio (The new transformer supports the reduced power consumption). The PCB art work remains the same. See Table A3 in the application section.

Introduction to Operating Modes

The CS61535A supports three operating modes (as selected by pin MODE) as shown in Tables 1 and 2, and Figure 7, and Figures A1-A3 of the application section.

The modes are the hardware mode, the extended hardware mode and host mode. In the hardware and extended hardware modes, discrete pins are used to interface the device's control functions and status information. In the host mode, the line interface is connected to a host processor and a serial data bus is used for input and output of control and status information. There are thirteen multi-function pins whose functionality is determined by the mode pin, MODE (Table 2).

	HARDWARE MODE	EXTENDED HARDWARE MODE	HOST MODE
SUPPORTED BY:	CS61535A CS61535	CS61535A	CS61535A CS61535
MODE-PIN INPUT LEVEL	< 0.2 v	FLOAT, or 2.5 v	> (RV+) - 0.2V
CONTROL METHOD	INDIVIDUAL CONTROL LINES	INDIVIDUAL CONTROL LINES & PARALLEL CHIP SELECT	SERIAL u-PROCESSOR PORT
LINE CODE ENCODER & DECODER	NONE	AMI, B8ZS, HDB3	NONE
AIS DETECTION	NO	YES	NO
DRIVER PERFORMANCE MONITOR	YES	NO	YES

Table 1. Differences in Operating Modes

		MODE		
FUNCTION	PIN	HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

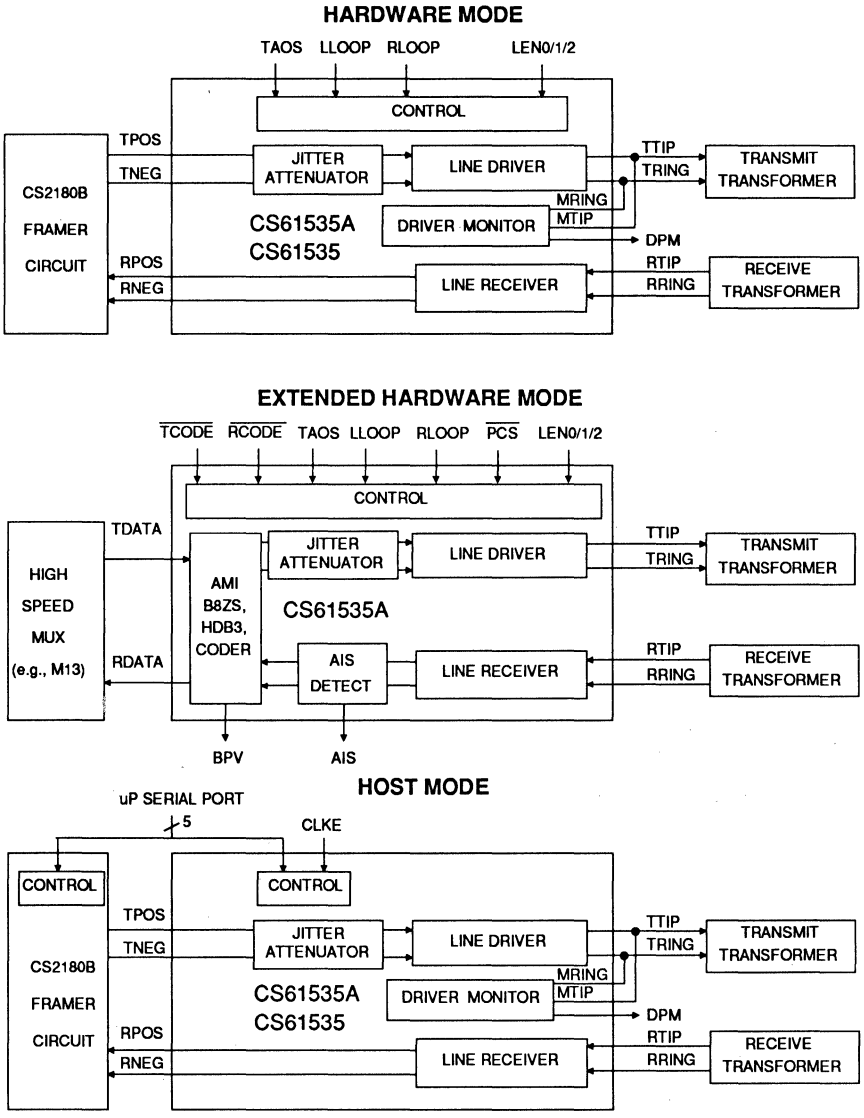


Figure 7. Overview of Operating Modes

Transmitter

The transmitter takes data from a T1 (or PCM-30) terminal, attenuates jitter, and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG or TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 (DSX-1 or Network Interface) or PCM-30 G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 3. The

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		Reserved
0	0	0	PCM-30 G.703	2.048 MHz CCITT
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 3. Line Length Selection

CS61535A line driver is designed to drive a 75 Ω equivalent load. The CS61535 drives a 25 Ω load.

For PCM-30 applications, the CS61535A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61535A automatically adjusts the pulse width based upon the "line length " selection made.

The PCM-30 G.703 pulse shape is supported with line length selection LEN2/1/0=000. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

The CS61535A transmitter will detect a failed TCLK, and will insure that neither TTIP nor TRING gets stuck high. If the clock signal is

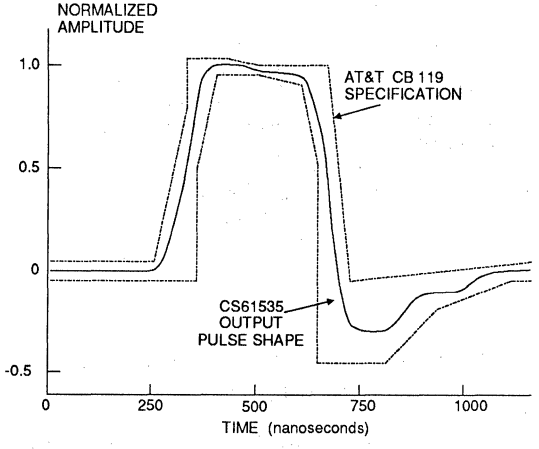


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

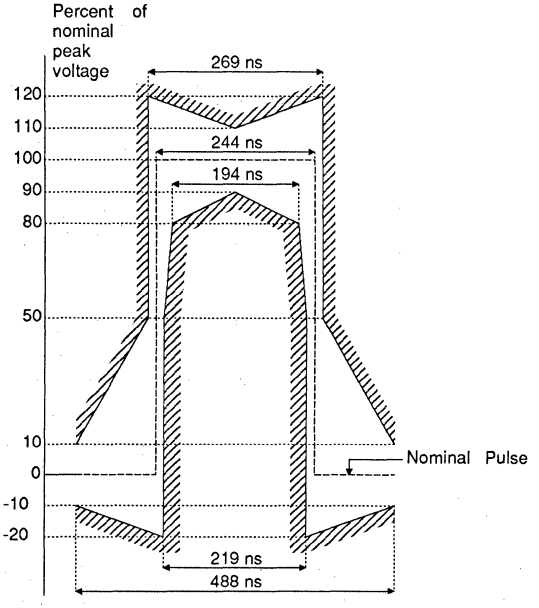


Figure 9 . Mask of the Pulse at the 2048 kbps Interface

removed from TCLK on the CS61535, TPOS and TNEG should both be low during the last falling edge of TCLK.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG (or TDATA) should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

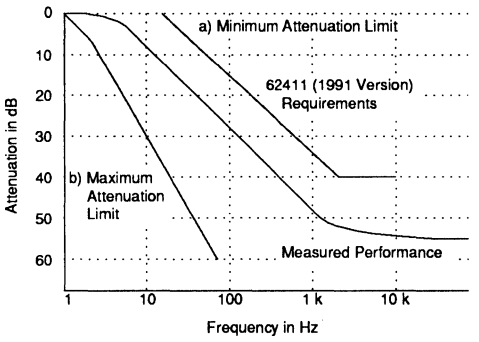


Figure 10. Typical Jitter Attenuation Curve

Wander and Jitter Attenuator

The jitter attenuator is designed to reduce wander and jitter in the transmit clock signal. It consists of a 32 bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 10.

The jitter attenuator works in the following manner. Data on TPOS and TNEG (or TDATA) are written into the jitter attenuator's FIFO by TCLK. The rate at which data is read out of the FIFO and transmitted is determined by the oscillator. Logic circuits adjust the capacitive loading on the crystal to set its oscillation frequency to the average of the TCLK frequency. Signal jitter is absorbed in the FIFO.

Jitter Tolerance of Jitter Attenuator

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter

	For coaxial cable, 75 ohm load and transformer specified in Application Section.	For shielded twisted pair, 120 ohm load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05 *	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

* When configured with a 0.47 uF nonpolarized capacitor in series with the Tx transformer primary as shown in Figures A1, A2 and A3.

Table 4 . CCITT Pulse Specifications

amplitude becomes very large, the read and write pointers may get very close together. Should the pointers attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. When a divide by 3 1/2 or 4 1/2 occurs, the data bit will be driven on to the line either an eighth bit period early or an eighth bit period late.

When the TCLK frequency is close to the center frequency of the crystal oscillator, the high frequency jitter tolerance is 23 UI before the divide by 3 1/2 or 4 1/2 circuitry is activated. [Note: If your application requires more than 23 UI of jitter tolerance before the onset of divide by 3 1/2 or 4 1/2, please contact Crystal Semiconductor.] As the center frequency of the oscillator and the TCLK frequency deviate from one another, the jitter tolerance is reduced. As this frequency deviation becomes large, the maximum jitter tolerance at high frequencies is reduced to 12 UI before the underflow/overflow circuitry is activated. In application, it is unlikely that the oscillator center frequency will be precisely aligned with the TCLK frequency due to allowable TCLK tolerance, part to part variations, crystal to crystal variations, and crystal temperature drift. The oscillator tends to track low frequency jitter so jitter tolerance increases as jitter frequency decreases.

The crystal frequency must be 4 times the nominal signal frequency: 6.176 MHz for 1.544 MHz operation; 8.192 MHz for 2.048 MHz applications. Internal capacitors load the crystal, controlling the oscillation frequency. The crystal must be designed so that over operating temperature, the oscillator frequency range exceeds the system frequency tolerance. Crystal Semiconductor offers the CXT6176 & CXT8192 crystals, which yield optimum CS61535A and CS61535 performance.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of ACLKI. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. A TAOS request will be ignored if Remote Loopback is in effect. ACLKI jitter will be attenuated.

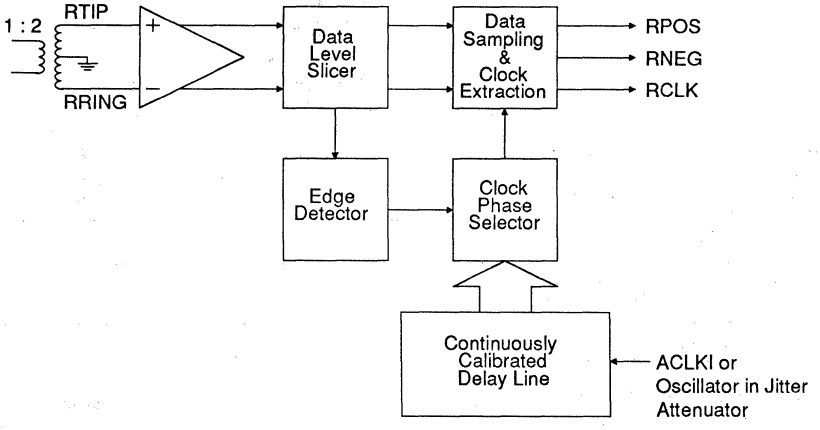


Figure 11. Receiver Block Diagram

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 11. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for PCM-30, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI or the jitter attenuator's oscillator, into 13 equal divisions or phases. Continuous calibration assures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that shown in Figure 12.

The CS61535 device outputs a clock at RCLK after the first signal is input to RTIP/RRING. The CS61535A outputs a clock immediately upon power-up. In either case, the clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the extended hardware mode, data at RDATA is stable and may be sampled on the fallings edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 5.

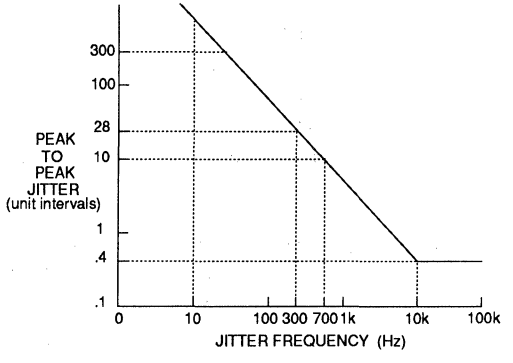


Figure 12. Input Jitter Tolerance of Receiver

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2v)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+)-0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+)-0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5v)	X	RDATA	RCLK	Falling

X= Don't care

Table 5. Data Output/Clock Relationship

Jitter and Recovered Clock

The CS61535A and CS61535 are designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until a data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UI. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS61535A or CS61535, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similiar calculations hold for PCM-30 rates.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS61535A and CS61535, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS61535A and CS61535 is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt issued on INT. LOS will go low (and flag the INT pin again if serial I/O is used) when a valid signal is detected. Note that in the host mode, LOS is simultaneously available from both the register and pin 12.

In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. In the CS61535, LOS returns to a logic zero upon receipt of the first bit at the

RTIP/RRING inputs. In the CS61535A, LOS returns to logic zero when the received signal returns to 12.5% ones density (based on 4 ones out of 32 bit periods, and no more than 14 zeros in a row). Also in the CS61535A, a power-up or manual reset will set LOS high.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA) and outputs it at RCLK, RPOS and RNEG (or RDATA). Receiver inputs are ignored when local loopback is in effect. The jitter attenuator is bypassed in th CS61535, but included in the loopback path of the CS61535A. Local loopback is selected by taking LLOOP, pin 27, high. Selection of local loopback overrides the chip's loss of signal response.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). A remote loopback bypasses the line code encoder/decoder, insuring that the transmitted signal matches the received signal, even in the presence of received bipolar violations.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the hardware and host modes of the CS61535A and CS61535 are able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors a transmitted AMI signal on input pins, MTIP and MRING. If no valid AMI signal is present on MTIP and MRING for 64±2 clock cycles, the DPM pin goes high.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring device, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

For the CS61535 only, the following application procedure is recommended to provide immunity from spurious DPM reports. If the controller on the line card detects that DPM has gone high, the controller should reconfirm that DPM is still high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can occur only when ones density is very low.

Line Code Encoder/Decoder

In the CS61535A Extended hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using pins LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ as shown in Table 6.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 6. Selection of Encoder/Decoder

Alarm Indication Signal

In the CS61535A Extended Hardware Mode, the receiver sets output pin AIS high when less than 3 zeros are detected out of 2048 bit periods. AIS returns low when 4 or more zeros, out of 2048 bits, are detected.

Parallel Chip Select

In the CS61535A Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low. Changes in inputs will immediately change the operating state of the CS61535A. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the CS61535A and CS61535 are held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI or by the crystal oscillator if ACLKI is not present. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware modes, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0.

In the CS61535A, a reset will set LOS high.

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One eight-bit register can be written to via the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The

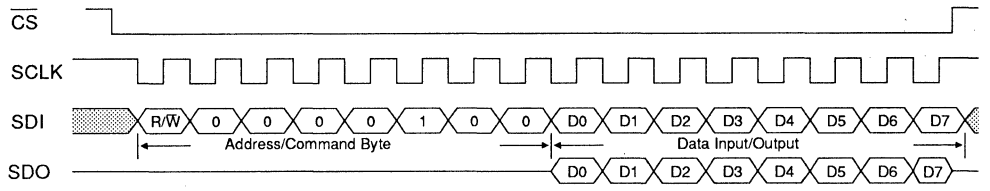


Figure 13. Input/Output Timimg

serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). SCLK may be either high or low when $\overline{CS}$ initially goes low. Address and input data bits are clocked in on the rising edge of SCLK. Data on SDO is valid and stable on the falling edge of SCLK when CLKE is low, and on the rising edge of SCLK when CLKE is high. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. For CLKE = 1, data bit D7 is held to the falling edge of the 16th clock cycle; for CLKE = 0, data bit D7 is held to the rising edge of the 17th clock cycle. SDO goes to a high impedance state either after bit D7 is output or at the end of the hold period of data bit D7.

An address/command byte, shown in Table 7, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61535A and CS61535 respond to address 16 (0010000). The last bit is ignored.

The data register, shown in Table 8, can be written to the serial port. Data is input on the eight

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 7. Address/Command Byte

clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver. If bits 0 of 1 are true, the corresponding interrupt is suppressed. So if a loss of signal interrupt is cleared by writing a 1 to bit 0, the interrupt will be reenabled by writing a 0 to bit 0. This holds for DPM as well.

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61535 into a factory test mode.

Table 8. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) the current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt)

2) output data bits 5, 6 and 7 will be reset as appropriate

3) future interrupts for the corresponding LOS or DPM will be suppressed (i.e., prevented from occuring)

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Output data from the serial interface is presented as shown in Tables 9 and 10. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermitent losses of signal and/or driver problems. Writing clear LOS and/or clear DPM to the register also resets status bits 5,6, and 7.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 9. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 10. Coding for Serial Output bits 5,6,7

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

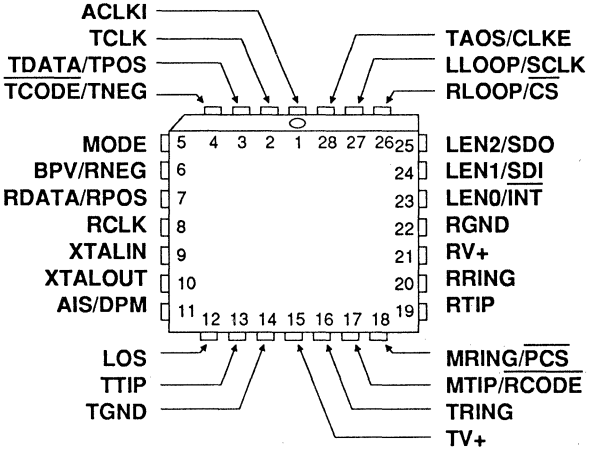
Power Supply

The device operates from a single 5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61535A or CS61535 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLKI	1	28	TAOS/CLKE	TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	TCLK	2	27	LLOOP/SCLK	LOCAL LOOP BACK
TRANSMIT POSITIVE PULSE	TDATA/TPOS	3	26	RLOOP/$\overline{CS}$	REMOTE LOOP BACK
TRANSMIT NEGATIVE PULSE	$\overline{TCODE}$ /TNEG	4	25	LEN2/SDO	BIT 2 OF LINE LENGTH SELECT
MODE SELECTION	MODE	5	24	LEN1/SDI	BIT 1 OF LINE LENGTH SELECT
RECEIVED NEGATIVE PULSE	BPV/RNEG	6	23	LEN0/$\overline{INT}$	BIT 0 OF LINE LENGTH SELECT
RECEIVED POSITIVE PULSE	RDATA/RPOS	7	22	RGND	RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+	RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	XTALIN	9	20	RRING	RECEIVE RING
CRYSTAL CONNECTION	XTALOUT	10	19	RTIP	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	AIS/DPM	11	18	MRING/$\overline{PCS}$	MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP/ $\overline{RCODE}$	MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (8.192 MHz for PCM-30 applications) crystal should be connected across these pins. Overdriving the oscillator with an external clock is not supported. See CXT6176/CXT8192 data sheet for crystal specifications.

Control

MODE - Mode Select, Pin 5.

Setting MODE to logic 1 puts the CS61535A or CS61535 in the host mode. In the host mode, a serial control port is used to control the CS61535A or CS61535 and determine its status. Setting MODE to logic 0 puts the CS61535A or CS61535 in the hardware mode, where configuration and status are controlled by discrete pins. Floating the MODE pin puts the CS61535A in the extended hardware mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no PCB trace attached to the pin. Alternatively, extended hardware mode can be entered by setting MODE to 2.5 V. MODE defines the status of 13 pins (see Table 2).

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLKI. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

LLOOP - Local Loopback, Pin 27.

In the CS61535, setting LLOOP to a logic 1 routes the transmit clock and data directly to the receive clock and data outputs. In the CS61535A, the transmit clock and data are routed to the receive clock and data pins through the jitter attenuator. TCLK and TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored in the hardware mode. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 2 for information on line length selection.

Extended Hardware Mode (CS61535A only)

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18.
Setting PCS high causes the CS61535A to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4.
Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder (see Table 6).

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17.
Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 6).

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.
Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing either "clear LOS" or "clear DPM" to the register. If "clear LOS" or "clear DPM" is true, the corresponding interrupt is disabled. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.
Data for the on-chip registers. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.
Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

CLKE - Clock Edge, Pin 28.
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.
Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

$\overline{\text{CS}}$ - Chip Select, Pin 26.
Pin must transition from high to low to read or write the serial ports.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.

For the CS61535, either a 1.544 MHz (or 2.048 MHz for PCM-30) clock must be input to ACLKI, which is used to calibrate the receiver clock recovery circuit. In a loss of signal state, the clock output, RCLK, will equal the ACLKI frequency. Transmit All Ones Mode frequency is set by ACLKI. ACLKI may not be provided by RCLK.

The CS61535A does not require a clock signal to be input on ACLKI. If a clock is not provided on ACLKI, this input must be grounded. If ACLKI is grounded, the oscillator in the jitter attenuator is used to calibrate the clock recovery circuit. A signal must be input on ACLKI if transmit all ones is selected.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

TDATA - Transmit Data, Pin 3.

Input data to be transmitted. TDATA inputs pass through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK. Used only in the extended hardware mode of the CS61535A.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG (or RDATA) and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61535A or CS61535. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "clear DPM" to the serial interface will inhibit any DPM interrupts.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. When in the loss of signal state, any received ones are output at RPOS/RNEG. In the CS61535, LOS returns to logic zero on the first bit received. In the CS61535A, LOS returns to logic 0 when a 12.5% ones density signal returns (determined by receipt of 4 ones within 32 bit periods).

DPM - Driver Performance Monitor, Pin 11.

If no AMI signal is present on MTIP and MRING , DPM goes to a logic 1 until the first detected AMI signal. DPM is available only in the CS61535A hardware and host modes.

BPV- Bipolar Violation Strobe, Pin 6.

BPV goes to a logic 1 for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled. Available only in the extended hardware mode.

AIS -Alarm Indication Signal, Pin 11.

AIS goes high when an all-ones condition (blue code) is detected, using the detection criteria of less than three zeros out of 2048 bit periods. Available only in the extended hardware mode.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

The receiver recovered clock and NRZ digital data is output on these pins. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the RCLK edge for which RPOS and RNEG are stable and valid; see Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RDATA - Receive Data - Pin 7.

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK. Used only in the extended hardware mode.

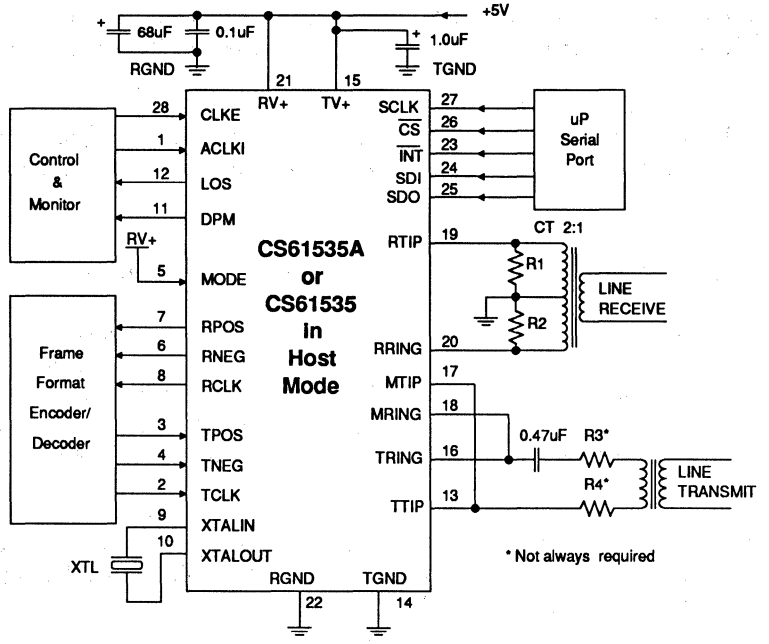
TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins.

In the CS61535A, this output is designed to drive a 75 Ω load. A transformer is required as shown in Table A2.

In the CS61535, this output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Table A4. When driving 75 Ω coax cable, a 4.4Ω resistor should be added in series with the transformer primary. The transmitter will drive twisted-pair cable, terminated with 100Ω or120 Ω, without additional components.

APPLICATIONS



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3&4 Ω	Transmit Transformer	Crystal XTL
CS61574	1.544	110	200	0	1:2	CXT6176
	2.048	120	240	0	1:2	CXT8192
	2.048	75	150	2.2	1:2	CXT8192
CS61574A OR CS61575	1.544	110	200	0	1:1.15	CXT6176
	2.048	120	240	0	1:1.26	CXT8192
	2.048	75	150	0	1:1	CXT8192

Figure A1. Host Mode Configuration

Line Interface

Figures A1-A3 show the typical configurations for interfacing the I.C. to a line through transmit and receive transformers. Note that the CS61535A transmitter transformer requirements have changed from those of the CS61535. This new transformer allows the CS61535A's lower power driver to be implemented.

The receiver transformer is center tapped and center grounded with resistors between the center tap and each leg on the I.C. side. These resistors provide the termination for the line.

Figures A1-A3 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the

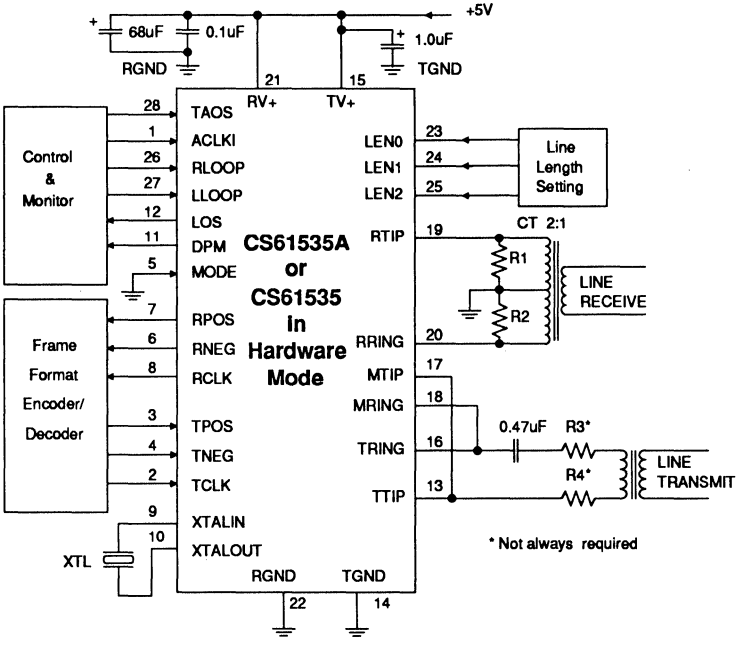


Figure A2. Hardware Mode Configuration

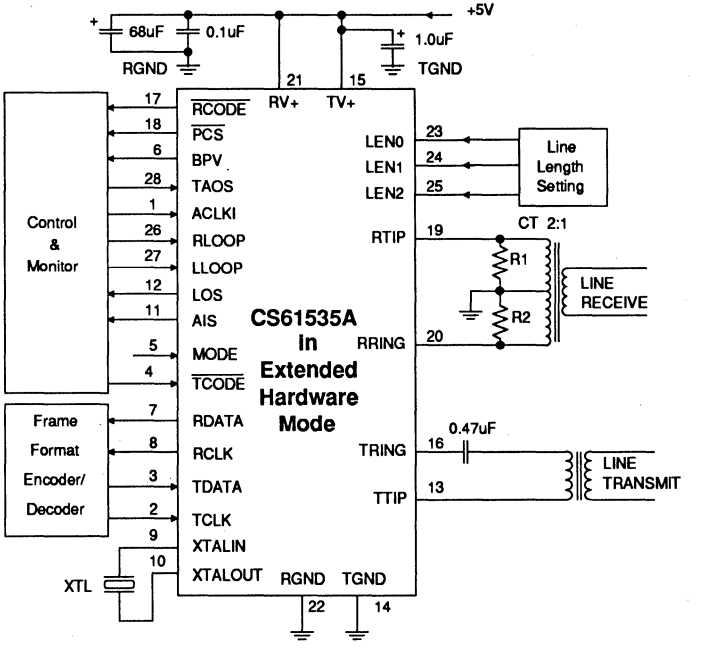


Figure A3. Extended Hardware Mode Configuration

transmission of a space (zero) as the transformer tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61535A and CS61535. It is recommended that the CXT6176 from Crystal Semiconductor be used for T1 applications, and that the CXT8192 be used for PCM-30 applications.

Interfacing The CS61535A With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A4. In this case, the CS61535A and CS2180B are in host mode controlled by a microprocessor serial interface. If the CS61535A is used in hardware mode, then the CS61535A RCLK output must be inverted before being input to the CS2180B. If the CS61535A is used in extended hardware mode, the CS61535A RCLK output does not need to be inverted before being input to the CS2180B.

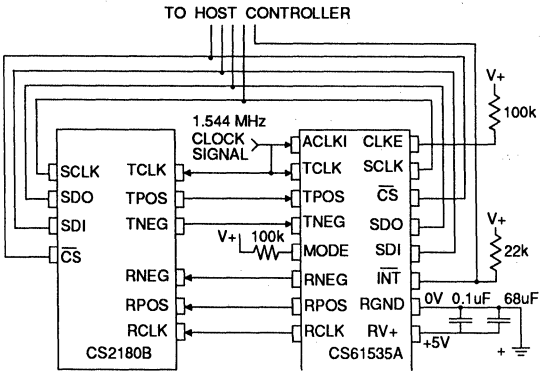


Figure A4. - Interfacing the CS61535A with the CS2180B (Host Mode)

CS61534 Compatibility

The CS61535A/61535 and CS61534 are pin compatible. Significant functional differences are the jitter tolerance of both transmit and receive sides, and more robust jitter attenuation. The greater jitter tolerance and attenuation in the transmit path makes the CS61535A/61535 more suitable for CCITT demultiplexing applications where eight bits can be dropped from the clock/data stream at once. Similarly, the CS61535A/61535 can be applied to SONET applications with the addition of some external circuitry.

The main differences between the CS61535A/61535 and CS61534 are as follows:

On the CS61535 and CS61535A, selection of LEN 2/1/0 = 0,0,0 changes the voltage at which the receiver accepts an input as a pulse (slicing level) from 65% to 50% of the peak pulse amplitude. Lowering the data slicing level will improve receiver sensitivity at long cable lengths when the data is jittered. A 50% slicing level will also improve crosstalk sensitivity for channels where received pulses do not have undershoot.

There are differences in the functionality of the ACLKI (ACLK) input on the CS61534, CS61535 and CS61535A. ACKLI (ACLK) is used as the transmit clock in the transmit all ones (TAOS) mode. On the CS61535 and CS61535A, ACLKI is used as a calibration reference for the receiver clock recovery circuit and therefore may not be supplied by RCLK. On the CS61534, ACLK may be supplied by RCLK . If an external clock is not provide on the ACLKI input of the CS61535A, the crystal oscillator is used to calibrate the receiver clock recovery circuit. ACLKI on the CS61535 must be connected to an external timing reference.

On the CS61535 and CS61535A, the host mode status register bits 5, 6 and 7 are en-

coded so that state changes on LOS and DPM may be reported.

RCLK on the CS61534 has a 50% duty cycle, while the CS61535 has a duty cycle which is typically over 70%, and the duty cycle and instantaneous frequency vary with received jitter. RCLK on the CS61535A/61535 may exhibit jitter even when the incoming signal is jitter free.

The CS61535 and CS61535A require 25 ns of setup time on TPOS and TNEG before the falling edge of TCLK and 25 ns of hold time on these inputs after the falling edge of TCLK. The CS61534 requires 50 ns of hold time on TPOS and TNEG after the falling edge of TCL, and 0 ns of setup time.

DPM and LOS occur after 31 consecutive zeros on the CS61534. For the CS61535A and CS61535, DPM occurs after 64±2 consecutive zeros and LOS after 175 zeros.

Since the internal timing circuits of the CS61535A and CS61535 are continuously calibrated, there is no need to issue a reset to initialize the receiver timing as with the CS61534.

Using the CS61535A for SONET

The CS61535A can be applied to SONET VT1.5 and VT2.0 interface circuits as shown in Figure A5. The SONET data rate is 51.84 MHz, and has 6480 bits per frame (125 us per frame). An individual T1 frame (193 bits per frame) or PCM-30 frame (256 bits per frame) has its data mapped into the 6480 bit SONET frame. The mapping does not result in a uniform spacing between sucessive T1 (or PCM-30) bits. Rather, for locked VT applications, gaps as large as 24 T1 bit periods or 32 PCM-30 bit periods can exist between successive bits. With floating VTs, the gaps can be even larger.

The circuit in Figure A5 eliminates the demultiplexing jitter in a two-step approach. The first step uses a FIFO which is filled at a 51.84 MHz rate (when T1 or PCM-30 bits are present), and which is emptied at a sub-multiple of the 51.84 rate. The FIFO is emptied only when it contains data. When the FIFO is empty the output clock is not pulsed.

The sub-multiple rate chosen should be slightly faster than the target rate (1.544 or 2.048 MHz), but as close to the target rate as possible. For locked VT operation, Table A1 shows potential

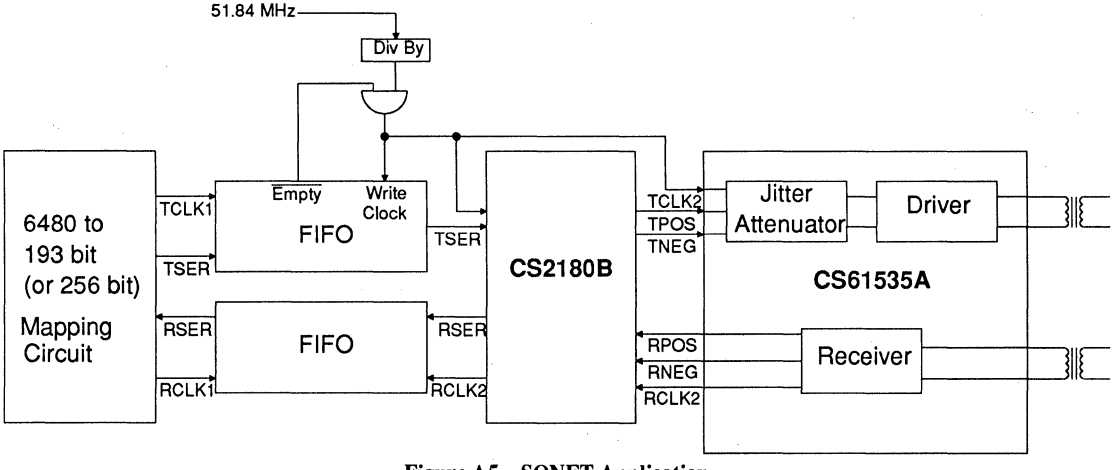


Figure A5. - SONET Application

sub-multiple data rates, and the impact on those rates on the maximum gap in the output clock of the FIFO, and depth of FIFO required. FIFO depth will have to be increased for floating VT operation, with 8 bits of FIFO depth being added for each pointer alignment change that can occur.

The objective that should be met in picking a FIFO depth and clock divider is keep the maximum gap on the output of the FIFO at 12 bits or less. Twelve bits is the maximum jitter which can be input to the CS61535A's jitter attenuator without causing the overflow/undeflow protection circuit to operate. The CS61535A then removes the remaining jitter from the signal.

The receive path also requires a bit mapping (from 193 or 256 bits to 6480 bits). This mapping requires an input buffer with the same depth as use on the transmit path. This buffer also absorbs the output jitter generated by the CS61535A's digital clock recovery.

CS61535A Transmitter Transformer

Target transformer specifications for the CS61535A transmitter are given in Table A2. The use of other transformer specifications can also result in acceptable performance. Table A3 lists transformers which have been qualified by Crystal Semiconductor for use when upgrading existing CS61535 boards to the CS61535A. Table A4 lists transformers recommended for new board designs. The Table A4 transformers provide higher isolation performance (as may be required for European applications).

Turns ratios:
1:1.26 ±1.5% for 120 ohm G.703 cable
1:1 ±1.5% for 75 ohm G.703 cable
1:1.15 ± 5% for 100 ohm T1 cable.

Primary inductance: 1.5 mH min measured at 772kHz.

Primary Leakage inductance: 0.3 µH max at 772 kHz with secondary shorted.

Secondary Leakage Inductance: 0.4 uH max at 772 kHz.

Interwinding capacitance: 18 pF max, primary to secondary

ET-constant: 16 V-us minimum for T1;
12 V-us minimum for PCM-30.

Table A2 CS61535A Transmitter Transformer Specifications

CS61535A and CS61535 Receiver Transformers

The receiver uses a 1:1:1 ± 5% transformer. Since pulse shapes are not measured at the receiver, the receive transformer specifications are not critical. Specifications similar to that for the CS61535 transmitter transformer (Table A5) provide excellent performance.

CS61535 Transmit Transformers

Key CS61535 transmit transformer specifications are given in Table A5. Transformers listed in Table A6 have been found to be suitable for use with the CS61535. Figure A6 shows the connections for some of the recommended transformers for the transmitter.

Target Rate (MHz)	Clock Divider	Resultant Rate (MHz)	Maximum Gap (us)	Maximum Gap bits	FIFO Depth Required
1.544	32	1.620	6.2	10	21
1.544	33	1.571	3.9	6	26
2.048	25	2.074	3.4	7	34

Table A1. - Locked VT FIFO Analysis

Transformer Used with CS61535		Application	Transformer for Use with CS61535A	
Vendor	Part Number		Vendor	Part Number
Pulse Eng. Schott Schott	PE-64931 67112060 67115100	T1	Pulse Eng. Schott	PE-65387 67124980
		PCM-30 75 Ω	Pulse Eng.	PE 65400
		PCM-30 120 Ω	Pulse Eng.	PE 65401

Table A3. CS61535A Transmitter Transformers for existing CS61535 boards

Application	Vendor	Transformer
T1	Pulse Eng. Schott	PE-65388 67124840
PCM-30	Pulse Eng. Schott	PE-65389 67124850

Table A4. CS61535A Transmit Transformers for New Designs

Turns ratio: 1:2 (or 1:1:1) ± 5%.

Primary inductance: 600 µH min measured at 772 kHz.

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted.

Secondary leakage inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 23 pF max, primary to secondary.

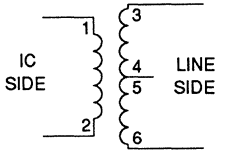
ET-constant: 16 V-us minimum for T1; 12 V-us minimum for PCM-30.

Table A5 - Transformer Specifications for CS61535A Receiver and CS61535

Manufacturer	Part#
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott Corp.	67115100 & 67124670
Schott Corp.	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the other Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A6. Suitable Transformers for CS61535A Receiver and CS61535



Pulse Engineering 5764 & PE-64931
Bell Fuse 0553-5006-16
Schott 67115100

Figure A6. Some Recommended CS61535 Transmitter Transformer Configurations

•Notes•

Semiconductor Corporation

CS61544

T1 Line Interface

Features

- Provides Analog T1 Line Interface
- Fully Compatible with CB119, Publication 43802, & TR-TSY-000009
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Implements ISDN Primary Rate and DMI Interface
- Diagnostic and Performance Monitoring Features
- Selectable B8ZS Encode/Decode
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61544 combines the analog transmit and receive line interface functions for a T1 system interface in one 28 pin device. The T1 line interface operates from a single 5V supply, is transparent to the T1 framing format, and can work with ABAM and other cable types.

Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for the line lengths ranging from 0 to 655 feet. Maximum range is greater than 1500 feet. The transmitter uses an elastic store to remove jitter from the outgoing data prior to transmission.

3

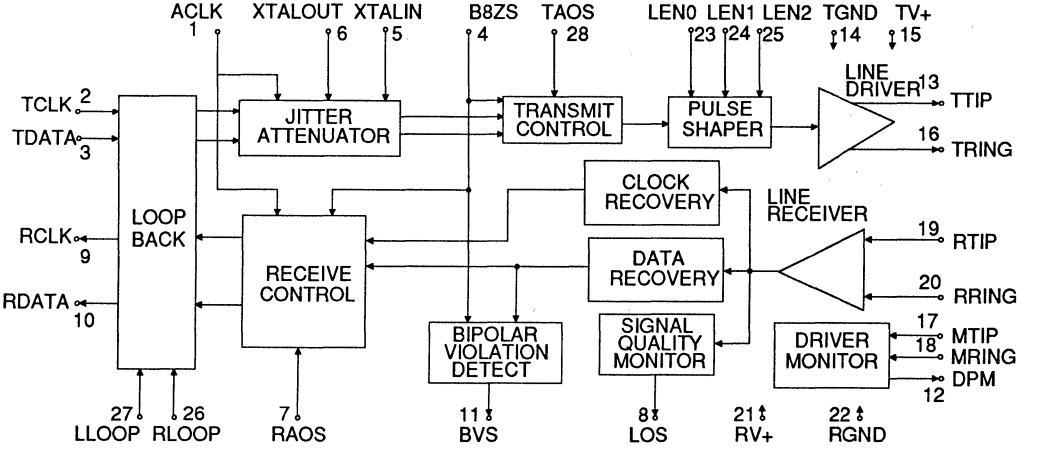
Applications

- Interfacing Networking Equipment such as M13 Multiplexers to a DSX-1 Cross Connect.
- Interfacing fiber optic transmission equipment to T1 lines.

ORDERING INFORMATION

CS61544-IP	-	28 Pin Plastic DIP
CS61544-ID	-	28 Pin Cerdip
CS61544-IL	-	28 Pin PLCC (j-leads)

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 1 & 2)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 1. Excluding RTIP and RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Note 4) 100% ones density & max. line length @ 5.25 V	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25Ω load, over operating temperature range. Includes CS61544 and load.

DIGITAL CHARACTERISTICS (T_A = -40 °C to 85 °C; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage Pins 1-5, 7, 23 - 28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage Pins 1-5, 7, 23 - 28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 5) I_{OUT}=-40 uA Pins 6, 8 - 12	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 5) I_{OUT}= 1.6 mA Pins 6, 8 - 12	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Note: 5. Output drivers will output CMOS logic levels into a CMOS load.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = -40°C to +85°C; V+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
AMI Output Pulse Amplitudes	Measured at the DSX	2.4	3.0	3.6	V_{0-p}
Load Presented to Transmitter Output	(Note 6)	-	25	-	ohms
Power in 2kHz band about 772kHz	(Note 7)	12.6	15	17.9	dBm
Power in 2kHz band about 1.554MHz (referenced to power at 772kHz)	(Note 7)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 7)	-	0.2	0.5	dB
Input Jitter Tolerance-Transmitter		7.0	-	-	U.I.
Jitter Attenuation Curve Corner Frequency	(Note 8)	-	-	50	Hz
Loss of Signal Threshold		-	0.5	-	V
Receiver Sensitivity Below DSX-1	(2.4V)	-10	-	-	dB
Receiver Jitter Tolerance	(Note 9)				
8kHz - 40kHz		0.1	-	-	U.I.
10Hz - 500Hz		5	-	-	U.I.

Notes:
6. On the CS61544 side of the 2:1 transformer, with a 100Ω impedance line attached to the secondary.
7. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
8. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter. Slope above corner frequency is -20dB/decade. See Figure 5.
9. For CERDIP ICs, assumes IC is operated within -70° to +70° C of reset temperature. For Plastic ICs, assumes IC is operated within -25° to +40° C of reset temperature (meets Bellcore central office specification: TR-EOP-000063 NEBS). For all packages, assumes IC is operated within 0.1 V of reset V+. Input data pattern is quasi-random: (2↑20) - 1 with 1-in-15. Between 500 Hz and 8 kHz the jitter tolerance will be better than the AT&T 43802 line shown in Figure 7.

SWITCHING CHARACTERISTICS (T_A = -40°C to +85°C; V+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 10)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 11)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width		t_{pwh}	-	324	-	ns
	(Note 12)	t_{pwl}	-	324	-	ns
Duty Cycle	(Note 13)		-	50	-	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	100	ns
TDATA to TCLK Falling Setup Time		t_{su}	25	-	-	ns
TCLK Falling to TDATA Hold Time		t_h	25	-	-	ns
RDATA to RCLK Rising Setup Time		t_{su}	-	274	-	ns
RCLK Rising to RDATA Hold Time		t_h	-	274	-	ns
Reset Pulse Duration			0.2	-	2000	us

Notes: 10. Crystal must meet specifications described in CXT6176 data sheet.
11. ACLK provided by an external source or TCLK.
12. The sum of the pulse widths must always meet the frequency specifications.
13. Duty cycle is $(t_{pwh} / (t_{pwh}+t_{pwl}))*100\%$.
14. At maximum load of 1.6mA and 50pF.

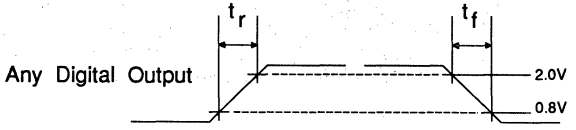


Figure 1 - Signal Rise and Fall Characteristics

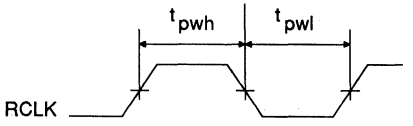


Figure 2 - Clock Signal Quality

Figure 3 - Switching Characteristics

Note that when externally looping RCLK back into TCLK, RCLK must be inverted.

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS61544 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew-rate-controlled fast digital-to-analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver drives a 25Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the B8ZS and TDATA should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0, LEN1, LEN2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

B8ZS coding can be inserted into the data stream using the B8ZS select feature. This feature replaces every string of eight consecutive zeros with a pulse train containing bipolar violations. The violations can then be decoded at the receive end and the original data recovered.

Transmit Line Length Selection

Line length selection can be controlled by an intelligent controller or hard-wired with a switch which is set at the time of installation. The line length selection supports both a three-partition arrangement for ICOT and MAT cable, and a five-partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS61544 modifies the output pulse to meet the requirements of Compatibility Bulletin 119 and TR-TSY-000009. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	0	0	0-220	MAT and ICOT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM (AT&T 600B & 600C series)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	

Table 1 - Line Length Selection

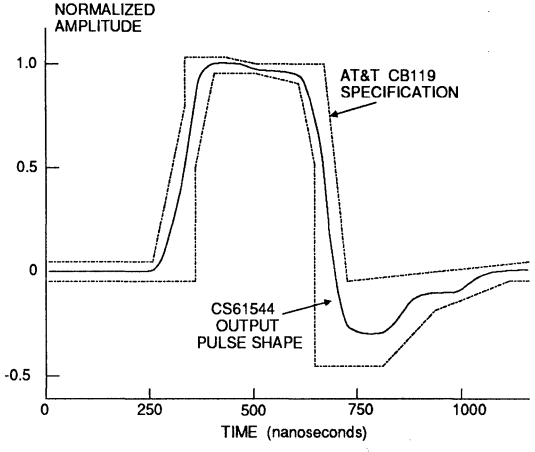


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

Transmit Jitter Attenuator

The 61544 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a T1 signal. Figure 5 shows a family of curves which show the jitter attenuation achieved by the 61544. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 6 and 7.

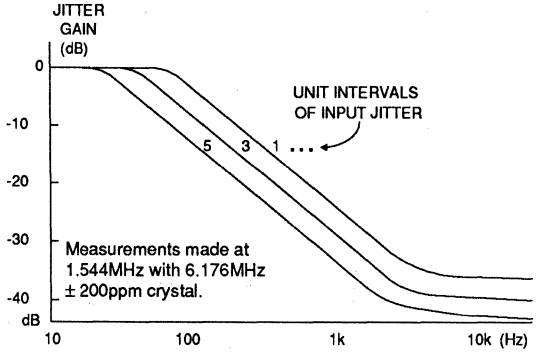


Figure 5 - CS61544 Jitter Attenuation Curves

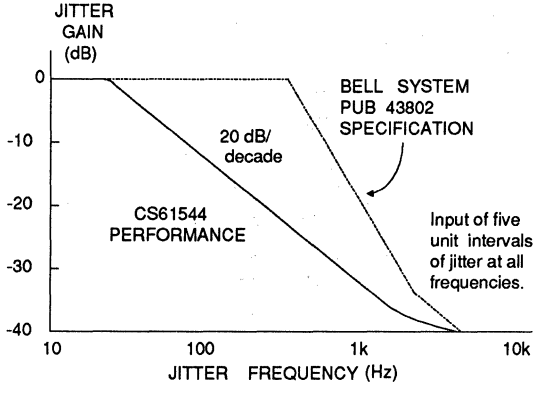


Figure 6 - Jitter Attenuation Characteristics

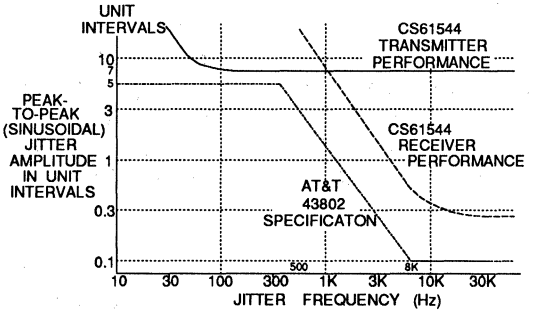


Figure 7 - Typical Input Jitter Tolerance of Transmitter and Receiver

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, and have a pull range, in the oscillator circuit, that is sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is exactly four times the TCLK frequency. Remote loopback should not be used if the jitter attenuator is disabled.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. (The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together). Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock. The TDATA and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61544 side. Data on RDATA is stable and may be sampled on the rising edge of the recovered clock, RCLK. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802.

The two leads of the receiver transformer have opposite polarity and drive the receiver inputs RTIP and RRING differentially. Comparators detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61544, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until the ICO frequency is near the reference frequency. This current is then held constant. The FPLL has small signal control from the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage as shown in the Analog Specifications table, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness. Resetting the CS61544 will optimize receiver performance for the operating power supply and temperature.

The received signal is monitored to detect bipolar violations. If a bipolar violation is detected, a positive strobe (BVS) is output with a width of one half the clock period.

The receiver has the capability to decode signals which have been transmitted with B8ZS bipolar violations. This feature is enabled when B8ZS (pin 4) goes high. Recovered data is processed by B8ZS decode (if enabled) and sent to the output. The bipolar violation detection algorithm is also modified to not detect the B8ZS encoded violation as an error.

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 31 bit periods. When a loss of signal is detected, RDATA is not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output, but may drift up to ± 6% from 1.544 MHz.

Receive All Ones Select

Receive all ones is selected when RAOS goes high. If receive all ones is selected when the local loopback is not in effect, continuous ones are sent to RDATA using the alternate clock, ACLK, for timing. The alternate clock, ACLK, is sent to RCLK. (The transmit clock, TCLK, can be used as the alternate clock by connecting pins 1 and 2 together.) If it is desirable to have all ones automatically replace recovered data (at RDATA) upon loss of signal, then RAOS and LOS should be tied together (pins 7 and 8).

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. Any RAOS request is overridden (see Table 2). The transmit clock and data signals, TCLK and TDATA are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case continuous ones are transmitted on the line at the rate determined by ACLK.

LLOOP Input Signal	RAOS Input Signal	Source of Data for RDATA	Source of Clock for RCLOCK
0	0	RTIP & RRING	RTIP & RRING
0	1	all 1s	ACLK
1	X	TDATA	TCLK

Table 2 - Interaction of LLOOP and RAOS

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 3). The recovered incoming signals are also sent to RCLK and RDATA unless receive all ones (RAOS) is selected, in which case continuous ones and an alternate clock are sent to RDATA and RCLK. Remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see *Reset*).

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X - Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicated that Loopback or All Ones option is selected.

Table 3 - Interaction of RLOOP and TAOS

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning T1 links, the CS61544 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring CS61544. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, the DPM pin goes high.

To provide immunity from spurious DPM reports, the following application procedure is recommended: If the controller on the T1 line card detects that DPM has hone high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can occur only when ones density is very low.

Whenever more than one CS61544 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS61544 monitor performance of a neighboring CS61544 device, rather than having it monitor its own performance.

Reset

The CS61544 initiates internal reset procedures either upon power up or in response to a reset request. After initial power up, the device will delay for approximately 10 ms before initiating the training proceedure for the FPLL. It is advisable to issue a reset request after the power supply has stabilized and signals have been applied to the device to insure that conditions on the chip are stable before FPLL training takes place. Training the FPLL takes at most 43 ms, but typically requires less than half that amount of time. These conditions should also be adhered to if temporary loss of power supply occurs.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

During the reset procedure, the loss of signal indicator is high. Once the reset procedures are completed, the loss of signal indicator goes low, signifying that normal operation of the device has begun.

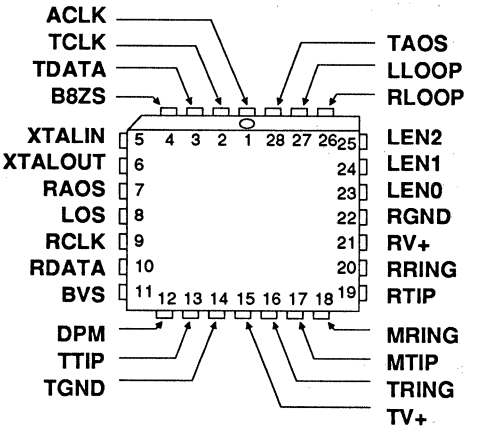
Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. These capacitors should be located physically close to the device. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61544 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLK	1	28	TAOS — TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	TCLK	2	27	LLOOP — LOCAL LOOPBACK
TRANSMIT DATA	TDATA	3	26	RLOOP — REMOTE LOOPBACK
B8ZS ENABLE	B8ZS	4	25	LEN2 — BIT 2 OF LINE LENGTH SELECT
CRYSTAL INPUT 2	XTALIN	5	24	LEN1 — BIT 1 OF LINE LENGTH SELECT
CRYSTAL INPUT 1	XTALOUT	6	23	LEN0 — BIT 0 OF LINE LENGTH SELECT
RECEIVE ALL ONES SELECT	RAOS	7	22	RGND — RECEIVE GROUND
LOSS OF SIGNAL	LOS	8	21	RV+ — RECEIVE V+ (+5V DC)
RECOVERED CLOCK	RCLK	9	20	RRING — RECEIVE RING
RECEIVE DATA	RDATA	10	19	RTIP — RECEIVE TIP
BIPOLAR VIOLATION STROBE	BVS	11	18	MRING — MONITORED RING
DRIVER PERFORMANCE MONITOR	DPM	12	17	MTIP — MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING — TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+ — TRANSMIT V+ (+5V DC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Inputs, Pins 5 and 6.

A 6.176 MHz crystal should be connected across these pins. An externally generated 6.176 MHz clock signal may be put into the XTALIN pin, disabling the jitter attenuator. This clock must be *exactly* four times the frequency at TCLK. See the CXT6176 data sheet for more information on crystals.

Control

B8ZS - B8ZS Encoding Enable, Pin 4.

Setting B8ZS to a logic 1 enables B8ZS encoding of the transmit data and B8ZS decoding of the receive data.

3

RAOS - Receive All Ones Select, Pin 7.

Setting RAOS to a logic 1 causes continuous ones to be sent to RDATA at the frequency determined by ACLK.

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. Any RAOS request is ignored. TCLK and TDATA are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RDATA unless overridden by a RAOS request. Any TAOS request is ignored. If the oscillator is being driven with a 4X clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accomodate several cable types and lengths. See Table 1 for information on line length selection.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 MHz clock. The frequency of ACLK determines the rate at which TAOS and RAOS are output.

TCLK, TDATA - Transmit Clock, Transmit Data, Pins 2 and 3.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The receive AMI signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A3. Data and clock are recovered and output on RDATA and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61544. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Outputs

RCLK, RDATA - Recovered Clock, Receive Data, Pins 9 and 10.

Data and clock are recovered from the RTIP and RRING inputs and output at these pins. RDATA is valid on the rising edge of RCLK.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI, T1 signal is driven to the line through these pins. This output is designed to drive a 25Ω load. A 2:1 step-up transformer is required to drive the line as shown in Figure A1.

Status

LOS - Loss of Signal, Pin 8.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 31 clock cycles with out a detected one. LOS returns to logic 0 when the signal returns.

BVS - Bipolar Violation Strobe, Pin 11.

BVS goes to a logic 1 when a bipolar violation is detected in the received signal. The strobe is approximatly 324 ns wide and aligned with the rising edge of RCLK. The strobe will occur concurrently with the RDATA output for which the violation was detected. The bipolar violation detection algorithm is modified when B8ZS is selected to accept B8ZS encoded data.

DPM - Driver Performance Monitor, Pin 12.

If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, DPM goes to a logic 1 until the first detected signal.

APPLICATIONS

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61544. It is recommended that the Crystal Semiconductor CXT6176 be used with the CS61544.

General Applications

Figure A1 shows the typical configuration for the CS61544, including transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200Ω resistors between the center tap and each leg on the CS61544 side. These resistors provide the 100Ω termination for the T1 line. Line Length Select pins are shown in a manual switching configuration. These inputs can be controlled by logic circuitry if desired.

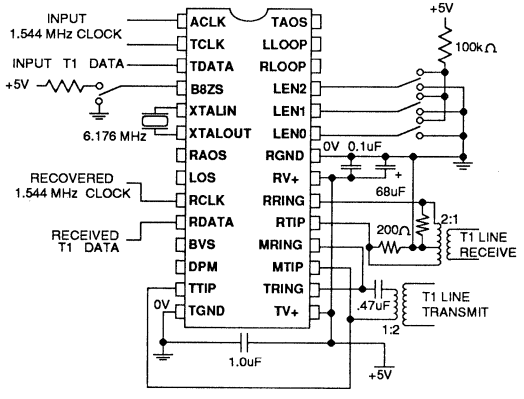


Figure A1. Typical Configuration Showing Line Interface

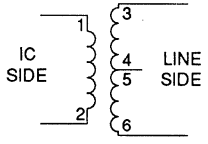
Transformers

Transformers listed in Table A1 have been found to be suitable for use with the CS61544. Figure A2 shows the connections for some of the transformers mentioned in the Table A1. The transformers should be placed physically close to the CS61544.

Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott Corp.	67115100 & 67124670
Schott Corp.	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the above Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A1. Suitable Transformers



Bell Fuse 0553-5006-IC
Schott Corp. 67115100
Pulse Engineering 5764 & PE-64931

Figure A2. Transmitter Transformer Configuration

Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1)±5%

Primary inductance: 600 µH min measured at 772 khz

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted

Secondary leakage inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 23 pF max, primary to secondary

ET-Constant: 16 V-µs min for T1;

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage dif-

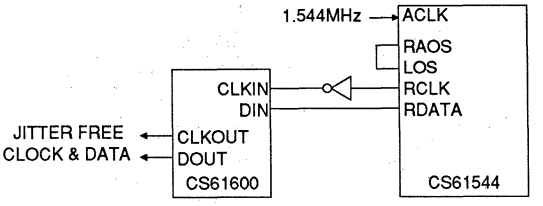


Figure A3. Receiver Jitter Attenuation

ference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a 0.47 µF non-polarized capacitor in series with the primary of the transformer.

Receive Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A3.

Maintaining Recovered Clock

Figure A3 also shows how the recovered clock, RCLK, can be maintained within desired specifications in the event that the received AMI signal is lost. This design requires a locally generated 1.544 MHz clock whose frequency is within the required system specifications. This clock is input to the ACLK input of the CS61544. The loss of signal output, LOS, is connected to the receive all ones select input, RAOS.

If the AMI signal is lost, the LOS signal goes high, taking RAOS high, directing the CS61544 to output all ones at RDATA at the frequency determined by ACLK (i.e. RCLK = ACLK). The CS61600 will buffer any instantaneous phase or frequency change at the RCLK and RDATA pins, retaining clock integrity. This type of circuit is necessary since the frequency/phase lock loop in the CS61544 may drift when the AMI signal is lost.

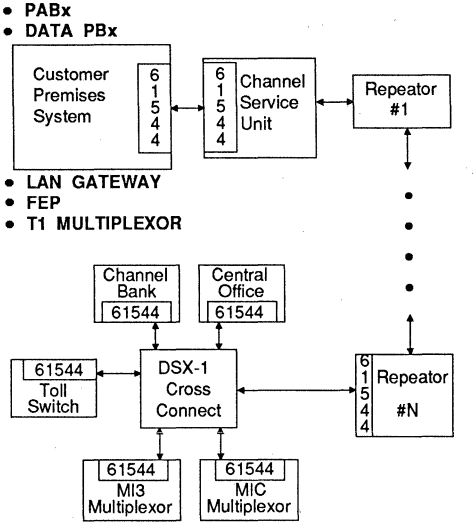


Figure A4. Applicable Types of Connection

If the receiver input returns, LOS goes low, deselecting RAOS, and returning the circuit to its normal operating status. It is important to note that LOS will go low as soon as a valid pulse is detected, which is before the receiver has locked onto the incoming signal. It is advisable to delay the transition from RAOS to the receiver output for a few milliseconds after LOS indicates receipt of signal.

Applicable Systems

Figure A4 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A4, the CS61544 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and is applicable in network equipment that connects to a DSX-1 cross connect.

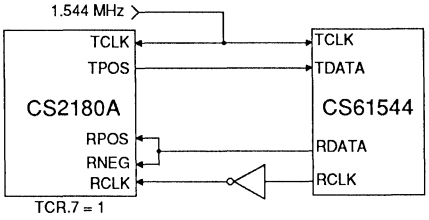


Figure A5. Interfacing CS61544 with CS2180A

Interfacing The CS61544 With T1 Digital Transceivers

To interface with the CS2180A, connect the devices as shown in Figure A5. When RPOS is tied to RNEG, B8ZS encoding/decoding and bipolar violation detection functions are performed by the CS61544.

Test and Evaluation of the CS61544

When connecting the receive clock and data, RCLK and RDATA, to the transmit clock and data, TCLK and TDATA, of the CS16544, be sure to invert the clock signal.

Transmitter or Receiver Function Only

If the CS61544 is used for transmit only, tie RTIP and RRING high through a resistor, ground RAOS, RLOOP, and LLOOP, and float the outputs. To configure the device for receive only, float TTIP, TRING, TV+ and TGND, ground TAOS, TCLK, TDATA, RLOOP, LLOOP and LEN0/1/2 .

• Notes •

Semiconductor Corporation

CS61575 CS61574A CS61574

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, Jitter Attenuation & Clock Recovery Functions
- Fully Compliant with AT&T 62411 (1990 Version) Jitter/Synchronizer (Stratum 4, Type II) Requirements
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss

General Description

The CS61575, CS61574A and CS61574 combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device.

The line interface unit (LIU) operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connnecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. The CS61575 receiver uses a 128-bit elastic store to remove jitter from the incoming data. The CS61574A and CS61574 employ a 32-bit elastic store.

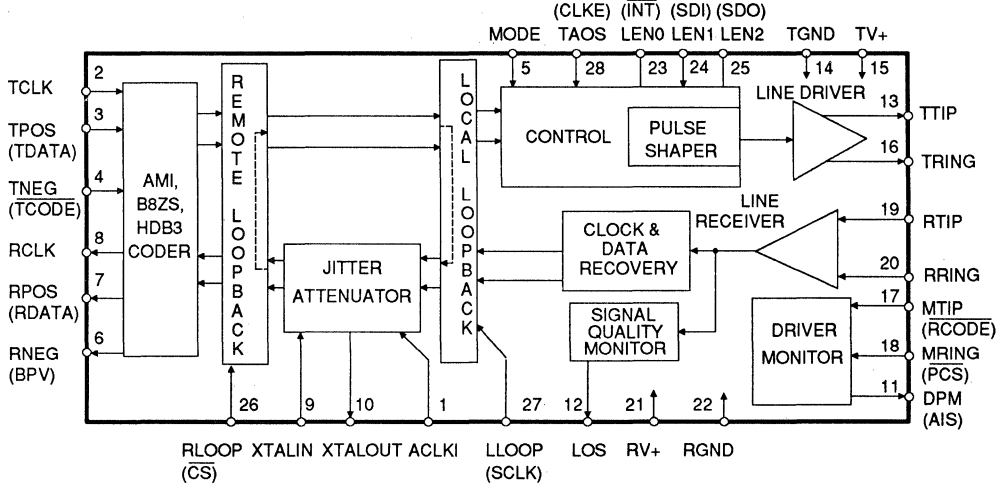
3

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION - See page 3-151.

Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply	(referenced to GND)	RV+	-	6.0	V
		TV+	-	(RV+) + 0.3	V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
CS61575/4A Power Consumption	(Note 4,5)	P_C	-	290	350	mW
CS61575/4A Power Consumption	(Note 4,6)	P_C	-	175	-	mW
CS61574 Power Consumption	(Note 4,5)	P_C	-	620	760	mW
CS61574 Power Consumption	(Note 4,6)	P_C	-	400	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

CS61574 DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-5, 23-28	(Note 7)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-5, 23-28	(Note 7)	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT}=-40 uA PINS 6-8, 11,12, 23, 25	(Note 8)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT}= 1.6 mA PINS 6-8, 11,12, 23, 25	(Note 8)	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)			-	-	±10	uA

Notes: 7. Functionality of pins 23 and 25 depends on the mode. See Operating Modes description.
8. Output drivers will output CMOS logic levels into a CMOS load.

CS61575 and CS61574A DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+, RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 7, 9, 10) PINS 1-4, 17,18, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 7, 9, 10) PINS 1-4, 17, 18, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 7, 9) I_{OUT} =-40 uA PINS 6-8, 11, 12, 23, 25	V_{OH}	4.0	-	-	V
Low-Level Output Voltage (Notes 7, 9) I_{OUT} =1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	± 10	uA
Low-Level Input Voltage, PIN 5	V_{IL}	-	-	0.2	V
High-Level Input Voltage, PIN 5	V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, PIN 5 (Note 11)	V_{IM}	2.3	-	2.7	V

Notes: 9. This specification guarantees TTL compatiblity (V_{OH} = 2.4 V @ I_{OUT} = -40µA).
10. Pins 17 and 18 have digital characteristics in Extended Hardware Mode.
11. As an alternative to supplying a 2.3-to-2.7 V input, this pin may be left floating.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes	(Note 12)				
PCM-30, 75 Ohm	(Note 13)	2.14	2.37	2.6	V
PCM-30, 120 Ohm	(Note 14)	2.7	3.0	3.3	V
T1	(Note 15)	2.4	3.0	3.6	V
Load Presented To Transmitter Output	(Note 12)				
CS61575 & CS61574A		-	75	-	Ohms
CS61574		-	25	-	Ohms
Jitter Added During Remote Loopback (Note 16)	10Hz - 8kHz	-	0.005	-	UI
	8kHz - 40kHz	-	0.008	-	UI
	10Hz - 40kHz	-	0.010	-	UI
	Broad Band	-	0.015	-	UI
Power in 2kHz band about 772kHz	(Note 17, 18)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544 MHz (referenced to power in 2kHz band at 772kHz)	(Note 17, 18)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 17, 18)	-	0.2	0.5	dB
CS61575/4A PCM-30 Transmitter Return Loss	(Notes 12, 18, 19)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Min	Typ	Max	Units
DRIVER PERFORMANCE MONITOR				
CS61575/4A MTIP/MRING Sensitivity: Differential Voltage Required for Detection				
With one input at 1.5 V	-	0.75	-	V
With one input at 0 V	-	2.0	-	V
RECEIVER				
CS61575/4A RTIP/RRING Input Impedance	-	50k	-	Ohms
Sensitivity Below DSX (0dB = 2.4V)	-10	-	-	dB
Loss of Signal Threshold	-	0.3	-	V
Data Decision Threshold T1 pulse settings	-	65	-	% of peak
PCM-30 LEN2/1/0 = 000	-	50	-	% of peak
Allowable Consecutive Zeros before LOS	160	175	190	bits
Receiver Input Jitter Tolerance 10kHz - 100kHz	0.4	-	-	UI
2kHz	6.0	-	-	UI
(Note 20) 10Hz and below	300	-	-	UI
JITTER ATTENUATOR				
Jitter Attenuation Curve Corner Frequency (Notes 18, 21)	-	6	-	Hz
Attenuation at 10 kHz Jitter Frequency (Notes 18, 21)	-	50	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection) (Notes 18, 21)				
CS61575	138	-	-	UI
CS61574A & CS61574	12	23	-	UI

Notes: 12. Using transformer recommended in the Application Section.
13. These amplitudes, measured at the output of the transformer, are for line length settings LEN2/1/0 = 0/0/0 (see Figure 9).
14. These amplitudes, measured at the output of the transformer, are for line length settings LEN2/1/0 = 0/0/0 (see Figure 9) or LEN2/1/0 = 0/1/0.
15. These amplitudes, measured at the DSX-1 Cross-Connect, are for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1 (see Figure 8).
16. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
17. Typical performance with a 0.47 µF capacitor in series with primary of transmitter output transformer.
18. Not production tested. Parameters guaranteed by design and characterization.
19. Return loss = 20 log $_{10}$ ABS$((z_1+z_0)/(z1-z_0))$ where z_1=impedance of the transmitter, and z_0=impedance of line load measured with a repeating 1010 data pattern.
20. Jitter tolerance increases at lower frequencies. See Figure 11.
21. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 12. On the CS61574A and CS61574, output jitter can increase significantly when more than 12 UI's are input to the attenuator. On the CS61575, output jitter can increase significantly when more than 138 UI's are input to the attenuator at > 1 Hz jitter frequency. See discussion in Wander and Jitter Attenuator section.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+) (See Figures 1, 2 & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 22)	f_C	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
ACLKI Frequency	(Note 24)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 25)	t_{pwh1}/t_{pw1}	-	50	-	%
Rise Time, All Digital Outputs	(Note 26)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 26)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_{h1}	-	274	-	ns

3

PCM-30 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+) (See Figures 1, 2 & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 22)	f_C	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 23)	t_{pwh2}/t_{pw2}	44	50	53	%
ACLKI Frequency	(Note 24)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 25)	t_{pwh1}/t_{pw1}	-	50	-	%
Rise Time, All Digital Outputs	(Note 26)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 26)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_{h1}	-	194	-	ns

Notes: 22. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
23. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK for the CS61574.
24. ACLKI provided by an external source or TCLK.
25. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
26. At max load of 1.6 mA and 50 pF.

SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ.	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r ,t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to S DO Valid (Note 27)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns
Input Valid To $\overline{PCS}$ Falling Setup Time	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	t_{pcsl}	250	-	-	ns

Note: 27. Output load capacitance = 50 pF.

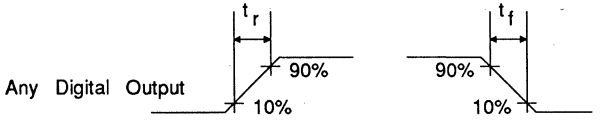


Figure 1. - Signal Rise and Fall Characteristics

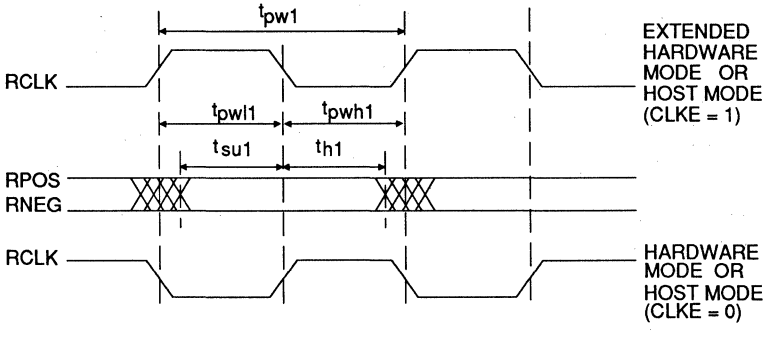


Figure 2. - Recovered Clock and Data Switching Characteristics

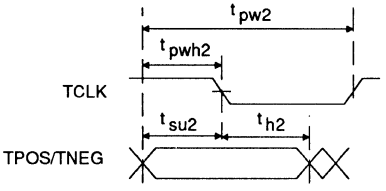


Figure 3. - Transmit Clock and Data Switching Characteristics

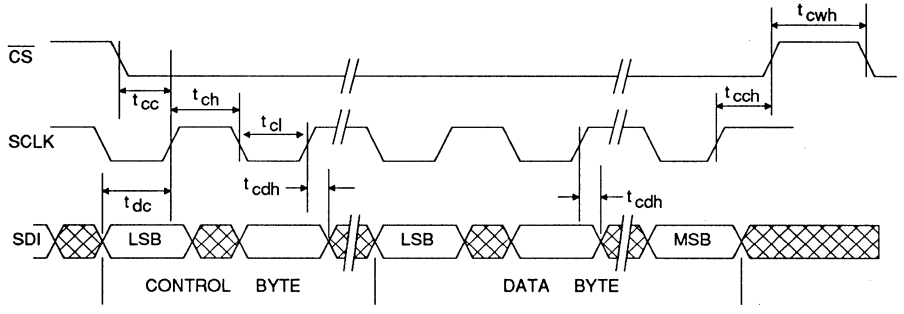


Figure 4. - Serial Port Write Timing Diagram

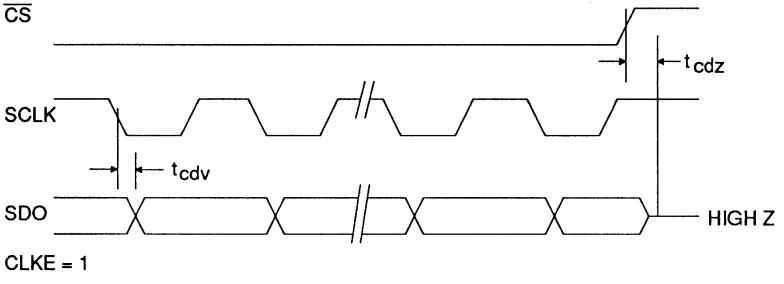


Figure 5. - Serial Port Read Timing Diagram

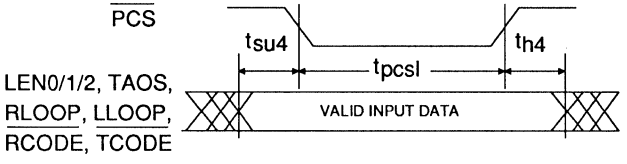


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Enhancements in CS61575 and CS61574A

The performance improvements available in the CS61575 and CS61574A are the following:

- The ***CS61575 fully meets AT&T 62411 (1991 version) requirements for jitter attenuation***, over the full range of operating signal frequencies. By using a 192-bit FIFO, the jitter attenuator will tolerate 138 UIs of jitter at 80 Hz.
- Power consumption has been reduced by 50%.
- 14 dB of transmitter return loss (during transmission of both marks and spaces) improves signal quality.
- AMI, B8ZS, HDB3 line code encoder/decoder options have been added.
- AIS (all ones) detection has been added.
- For PCM-30 applications, the CS61575 and CS61574A internally set the transmitted pulse width, eliminating the need for a TCLK input with precise duty cycle.
- Upon power up, LOS (loss of signal) is set high.
- When the transmitter senses the absence of a signal on TCLK, TTIP and TRING are forced to zero.
- The Loss of Signal condition is exited upon recognition of 12.5% one's density (4-of-32 and no more than 14 consecutive zeros).
- The Driver Performance Monitor operates over a wider range of input signal levels.

A PCB designed to use the CS61574 can be converted to the CS61575 or CS61574A with no change in art work. The only change required is to update the parts list to specify the new IC (CS61575 or CS61574A) and to specifiy a transmitter transformer with a different turns ratio. See Table A2 in the Applications Section. The new transformer supports the reduced power consumption.

Understanding the Difference Between the CS61575 and CS61574A

The only difference between the CS61575 and CS61574A is the depth of the FIFO in the jitter attenuator. The CS61575 has a 192-bit FIFO. The CS61574A has a 32-bit FIFO. What this means at the system level is that the CS61575 will attenuate jitter, even when the jitter amplitude is 138 UIs (the AT&T 62411, 1990 version, requirement). The CS61574A will typically stop attenuating jitter when the jitter amplitude exceeds 23 UIs. At that point the CS61574A will track very large amplitudes of jitter (for example, 300 UIs) through its 32-bit FIFO by using a different jitter transfer function. This alternative jitter transfer function will introduce some jitter peaking. The CS61574 operates just like the CS61574A in this regard, so that if the CS61574 works satisfactorily in your system, so will the CS61574A.

	HARDWARE MODE	EXTENDED HARDWARE MODE	HOST MODE
SUPPORTED BY:	CS61575 CS61574A CS61574	CS61575 CS61574A	CS61575 CS61574A CS61574
MODE-PIN INPUT LEVEL	< 0.2 v	FLOAT, or 2.5 v	> (RV+) - 0.2 V
CONTROL METHOD	INDIVIDUAL CONTROL LINES	INDIVIDUAL CONTROL LINES & PARALLEL CHIP SELECT	SERIAL u-PROCESSOR PORT
LINE CODE ENCODER & DECODER	NONE	AMI, B8ZS, HDB3	NONE
AIS DETECTION	NO	YES	NO
DRIVER PERFORMANCE MONITOR	YES	NO	YES

Table 1. Differences in Operating Modes

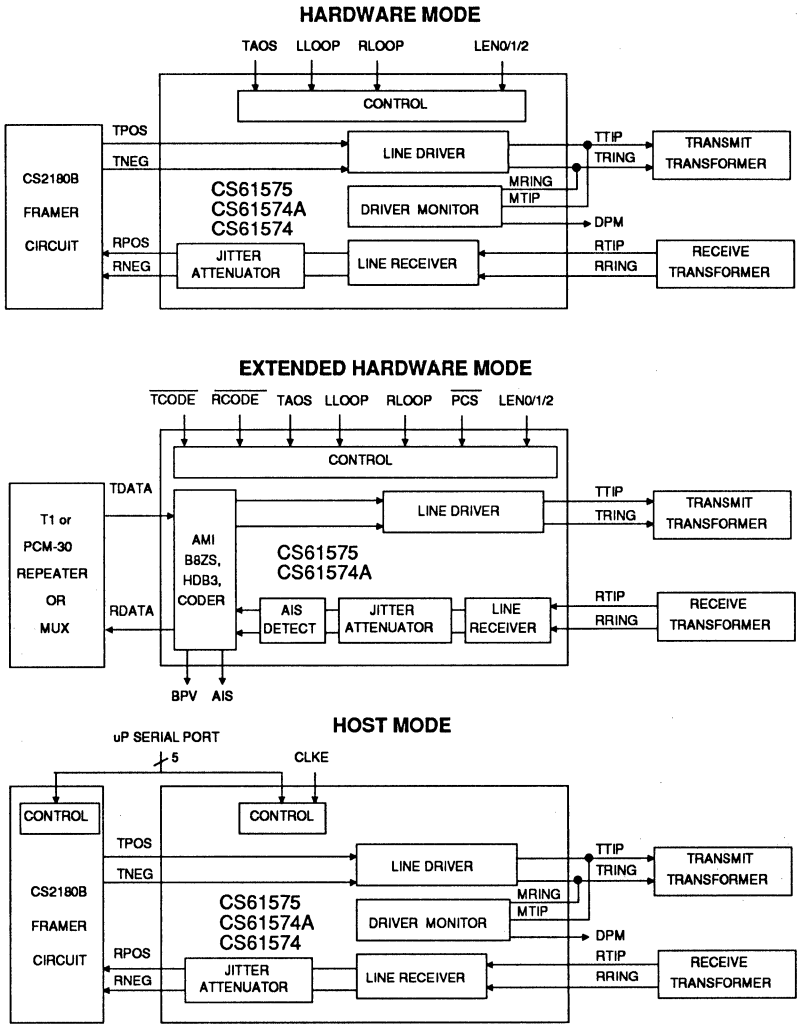


Figure 7. Overview of Operating Modes

Introduction to Operating Modes

The CS61575 and CS61574A support three operating modes (as selected by pin MODE) as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the applications section.

The modes are hardware mode, extended hardware mode, and host mode. In hardware and extended hardware modes, discrete pins are used to interface the device's control functions and status information. In the host mode, the line interface is connected to a host processor and a serial data bus is used for input and output of control and status information. There are thirteen multi-function pins whose functionality is determined by the mode pin, MODE (Table 2).

FUNCTION	PIN	MODE		
		HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

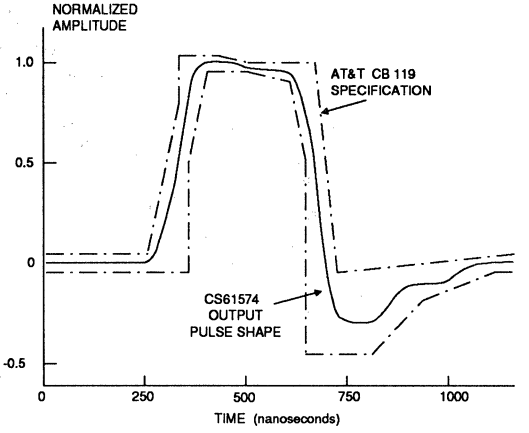


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

Transmitter

The transmitter takes data from a T1 (or PCM-30) terminal, and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG or TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 (DSX-1 or Network Interface) or PCM-30 G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 3. The CS61575 and CS61574A line drivers are designed to drive a 75 Ω equivalent load. The CS61574 drives a 25 Ω load.

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B and 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		Reserved
0	0	0	PCM-30 G.703	2.048 MHz CCITT
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 3. Line Length Selection

For PCM-30 applications, the CS61575 and CS61574A drivers provide 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61575 and CS61574A automatically adjusts the pulse width based upon the "line length" selection made.

The PCM-30 G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

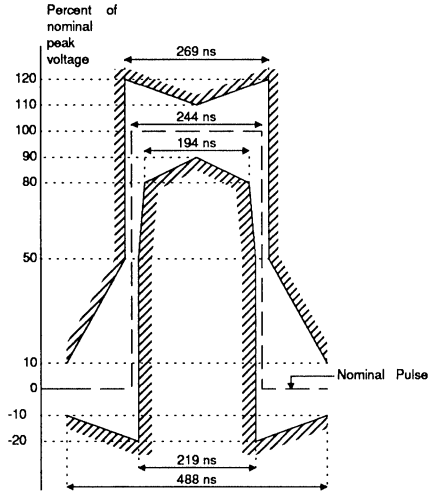


Figure 9. Mask of the Pulse at the 2048 kbps Interface

Note that in the case of the CS61574 (and not for CS61574A or CS61575) and only for LEN2/1/0=000, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 9, and specified in Table 4, assuming the TCLK duty cycle and frequency are appropriate.

The CS61575 and CS61574A transmitter will detect a failed TCLK, and will insure that neither TTIP nor TRING gets stuck high. If the clock signal is removed from TCLK on the CS61574, TPOS and TNEG should both be low during the last falling edge of TCLK.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG (or TDATA) should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs may not meet all data sheet specifications for 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

	For coaxial cable, 75 ohm load and transformer specified in Application Section	For shielded twisted pair, 120 ohm load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05 *	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

* When configured with a 0.47 uF nonpolarized capacitor in series with the Tx transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

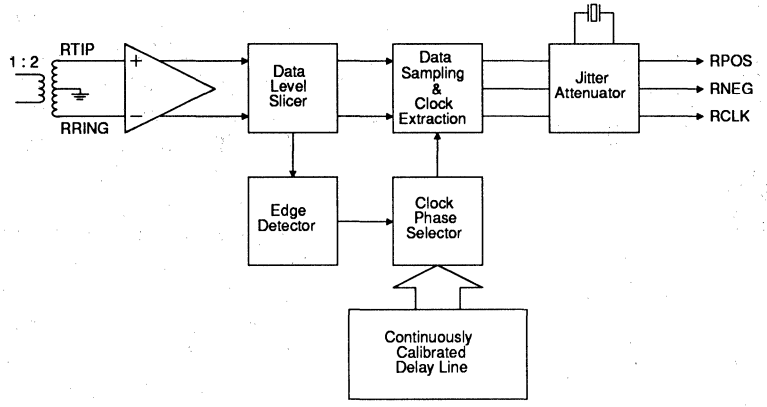


Figure 10. Receiver Block Diagram

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

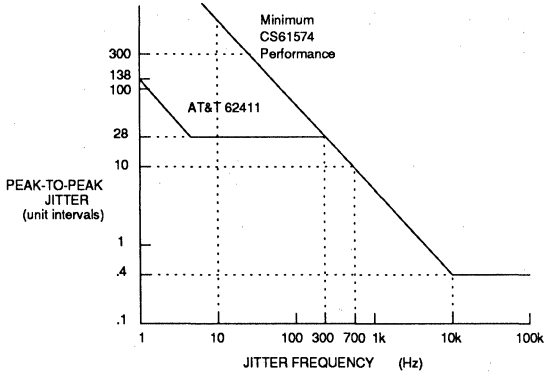


Figure 11. Minimum Input Jitter Tolerance of Receiver
(Clock Recovery Circuit and Jitter Attenuator)

A block diagram of the receiver is shown in Figure 10. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for PCM-30, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 11. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2v)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2 V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2 V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5v)	X	RDATA	RCLK	Falling

X= Don't care

Table 5. Data Output/Clock Relationship

sampler will continuously sample data based on its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated relative to a reference clock, which is provided by the crystal oscillator. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the extended hardware mode, data at RDATA is stable and may be sampled on the fallings edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 5.

Loss of Signal

The receiver will indicate loss of signal upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. The zero input level is determined either when zeros are received, or when the received signal amplitude degrades below a $0.3V_{peak}$ threshold.

Applicable Device	Crystal present?	ACLKI present?	Source of RCLK
All	No	Yes	ACLKI
All	Yes	No	Centered Crystal
CS61574	Yes	Yes	RTIP/RRING via Jitter Attenuator
CS61575 CS61574A	Yes	Yes	ACLKI via the Jitter Attenuator

Table 6. RCLK Status at LOS

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt will be issued on $\overline{INT}$. LOS will go low (and flag the $\overline{INT}$ pin again if the serial I/O is used) when a valid signal is detected. Note that in the host mode, LOS is simultaneously available from both the register and pin 12. Table 6 shows the status of RCLK upon LOS. Received data is output on RPOS/RNEG (RDATA) regardless of LOS status.

In the CS61575 and CS61574A, LOS typically returns to logic zero when the received signal returns to 12.5% ones density - based on 4 ones out of 32 bit periods with no more than 14 consecutive zeros. If ACLKI is present during the LOS state, ACLKI is switched into the input of the jitter attenuator, resulting in RCLK matching the frequency of ACLKI. The jitter attenuator buffers any instantaneous changes in phase between the last recovered clock and the ACLKI reference clock. This means that RCLK will smoothly transition to the new frequency. If ACLKI is not present, then the crystal oscillator of the jitter attenuator is forced to its center frequency. In the CS61575 or CS61574A, a power-up or manual reset will set LOS high.

In the CS61574, LOS returns to logic zero when the first one is received. In the CS61574, ACLKI

serves no significant purpose and should be grounded.

Wander and Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a 32 or 192-bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 12. The CS61575 fully meets AT&T 62411 jitter attenuation requirements. The CS61574A/74 will have a discontinuity in the jitter transfer function when the incoming jitter amplitude exceeds approximately 23 UIs.

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG (or RDATA). The update rate of the read pointer is analogous to RCLK. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Signal jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. During this activity, data will never be lost.

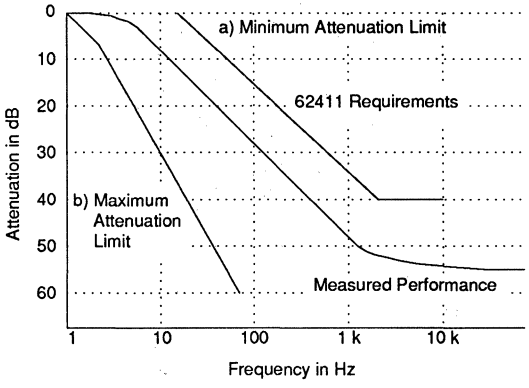


Figure 12. Typical Jitter Transfer Function

The jitter attenuator of the CS61575 contains a 192-bit FIFO, and will tolerate 138 UIs at 1 Hz and 28 UIs at 4.9 Hz as required by 62411, before the overflow or underflow mechanism takes effect. The jitter attenuators of the CS61574A and CS61574 contain a 32-bit FIFO, and will typically tolerate 23 UIs before the overflow or underflow mechanism takes effect.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG (or RDATA). If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on the line, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted to the line at the rate determined by TCLK. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high or LLOOP may be commanded via the serial interface.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 7. Interaction of RLOOP with TAOS

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 8. Encoder/Decoder Selection

3

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 6). The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). A remote loopback bypasses the line code encoder/decoder, insuring that the transmitted signal matches the received signal, even in the presence of received bipolar violations.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors a transmitted AMI signal on input pins, MTIP and MRING. If no valid AMI signal is present on MTIP and MRING for 64±2 clock cycles, the DPM pin goes high.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

In the CS61574 only, the following application procedure is recommended to provide immunity from spurious DPM reports. If the controller on the line card detects that DPM has gone high, the controller should reconfirm that DPM is still high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can only occur when one's density is very low.

Line Code Encoder/Decoder

In the CS61575 and CS61574A Extended hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDAT and BPV (Bipolar Violation Strobe). The

encoder and decoder are selected using pins LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ as shown in Table 8.

Alarm Indication Signal

In the CS61575 and CS61574A Extended Hardware Mode, the receiver sets output pin AIS high when less than 3 zeros are detected out of 2048 bit periods. AIS returns low when 4 or more zeros, out of 2048 bits, are detected.

Parallel Chip Select

In the CS61575 and CS61574A Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low. Changes in inputs will immediately change the operating state of the CS61575/74A. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware modes, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration.

In the CS61574, the RCLK output is forced low while reset is held high.

In the CS61575 and CS61574A, a reset will set LOS high.

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{\text{CS}}$, low ($\overline{\text{CS}}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{\text{CS}}$ high. $\overline{\text{CS}}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{\text{CS}}$ may go high any time to terminate the output.

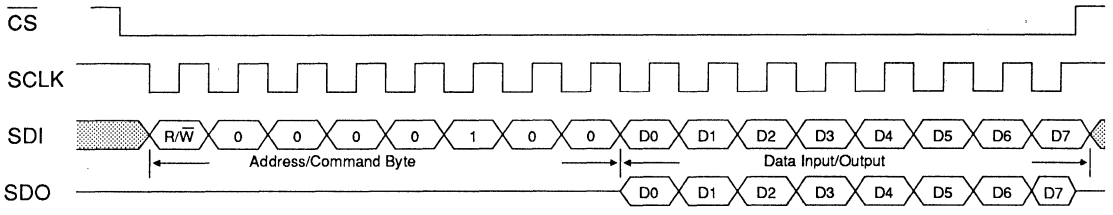


Figure 13. Input/Output Timing

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle.When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{CS}$ goes high *or* at the end of the hold period of data bit D7.

An address/command byte, shown in Table 9, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

The data register, shown in Table 10, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as ap propriate.
3) Future interrupts for the corresponding LOS or DPM will be suppressed (i.e., prevented from occurring).

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Input bits 5/6/7=111 and 5/6/7=101 are the same request, and cause the line interface to enter into the factory test mode. In other words, when RLOOP=1 (Bit 5) and TAOS=1 (Bit 7), LOOP (Bit 6) is a don't care. For normal operation, RLOOP and TAOS should not be simultaneously selected via the serial interface.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 9. Address/Command Byte

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61574 into a factory test mode.

Table 10. Input Data Register

Output data from the serial interface is presented as shown in Tables 11 and 12. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermitent losses of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

LSB: first bit in			
	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 11. Output Data Bits 0 - 4

Power Supply.

The device operates from a single 5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. However, these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

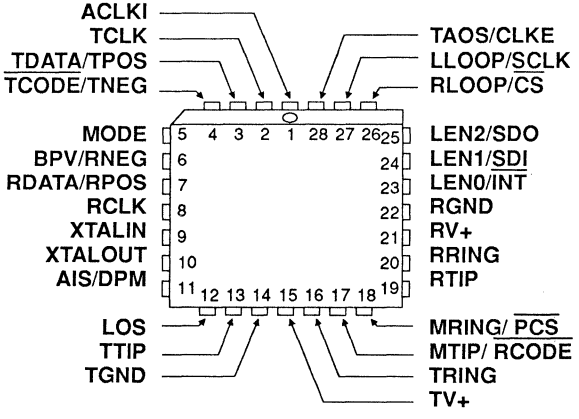
Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 12. Coding for Serial Output bits 5,6,7

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLKI	1	28	TAOS / CLKE	TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	TCLK	2	27	LLOOP / SCLK	LOCAL LOOP BACK
TRANSMIT POSITIVE PULSE	TDATA / TPOS	3	26	RLOOP / CS	REMOTE LOOP BACK
TRANSMIT NEGATIVE PULSE	TCODE / TNEG	4	25	LEN2 / SDO	BIT 2 OF LINE LENGTH SELECT
MODE SELECTION	MODE	5	24	LEN1 / SDI	BIT 1 OF LINE LENGTH SELECT
RECEIVED NEGATIVE PULSE	BPV / RNEG	6	23	LEN0 / INT	BIT 0 OF LINE LENGTH SELECT
RECEIVED POSITIVE PULSE	RDATA / RPOS	7	22	RGND	RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+	RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	XTALIN	9	20	RRING	RECEIVE RING
CRYSTAL CONNECTION	XTALOUT	10	19	RTIP	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	AIS/ DPM	11	18	MRING / PCS	MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP / RCODE	MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (8.192 MHz for PCM-30 applications) crystal should be connected across these pins. The jitter attenuator may be disabled by tying XTALIN, Pin 9 to the power supply through a resistor, and floating XTALOUT, Pin 10. Overdriving the oscillator with an external clock is not supported.

Control

MODE - Mode Select, Pin 5.

Setting MODE to logic 1 puts the line interface in the host mode. In the host mode, a serial control port is used to control the line interface and determine its status. Setting MODE to logic 0 puts the line interface in the hardware mode, where configuration and status are controlled by discrete pins. Floating the MODE pin puts the CS61575 or CS61574A in the extended hardware mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no PCB trace attached to the pin. Alternatively, extended hardware mode can be entered by setting MODE to 2.5 V. MODE defines the status of 13 pins (see Table 2).

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored in the hardware mode. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 2 for information on line length selection. Also controls the receiver slicing level.

Extended Hardware Mode (CS61575 and CS61574A only)

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18.

Setting $\overline{\text{PCS}}$ high causes the line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4.

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder (see Table 8).

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17.

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

3

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.

Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

CLKE - Clock Edge, Pin 28.

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

$\overline{\text{CS}}$ - Chip Select, Pin 26.

Pin must transition from high to low to read or write the serial ports.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.

Either a 1.544 MHz (or 2.048 MHz for PCM-30) clock may be input to ACLKI, or this pin must be tied to ground. In the CS61575 and CS61574A, the ACLKI input signal, if present, is driven upon loss of signal to the RCLK output through the jitter attenuator. In the CS61574, ACLKI serves no significant purpose and should be grounded.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4 (Host Mode and Hardware Mode).

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

TDATA - Transmit Data, Pin 3 (Extended Hardware Mode).

Input data to be transmitted. TDATA inputs pass through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK. Used only in the extended hardware mode (CS61574A and CS61575).

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18 (Host Mode and Hardware Mode).

These pins are normally connected to TTIP and TRING and monitor the output of a line interface IC. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{INT}$ pin in the host mode is used, and the monitor is not used, writing "clear DPM" to the serial interface will prevent any interrupt from the driver performance monitor.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. When in the loss of signal state, any received ones are output at RPOS/RNEG. In the CS61574, LOS returns to logic zero on the first bit received. In the CS61575 and CS61574A, LOS returns to logic 0 when a 12.5% ones density signal returns (determined by receipt of 4 ones within 32 bit periods with no more than 14 consecutive zeros). When in the loss of signal state on the CS61575 and CS61574A, ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present, RCLK is forced to the center frequency of the crystal oscillator upon LOS.

DPM - Driver Performance Monitor, Pin 11 (Host Mode and Hardware Mode).

If no AMI signal is present on MTIP and MRING, DPM goes to a logic 1 until the first detected AMI signal. Available only in Host and Hardware Mode.

AIS - Alarm Indication Signal, Pin 11 (Extended Hardware Mode).

AIS goes high when an all-ones condition (blue code) is detected, using the detection criteria of less than three zeros out of 2048 bit periods. Available only in the extended hardware mode.

BPV- Bipolar Violation Strobe, Pin 6 (Extended Hardware Mode).

BPV goes to a logic 1 for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled. Available only in the extended hardware mode (CS61574A and CS61575).

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6 (Extended Hardware Mode).

The receiver recovered clock and NRZ digital data is output on these pins. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RDATA - Receive Data - Pin 7 (Extended Hardware Mode).

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK. Used only in the extended hardware mode (CS61574A and CS61575).

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

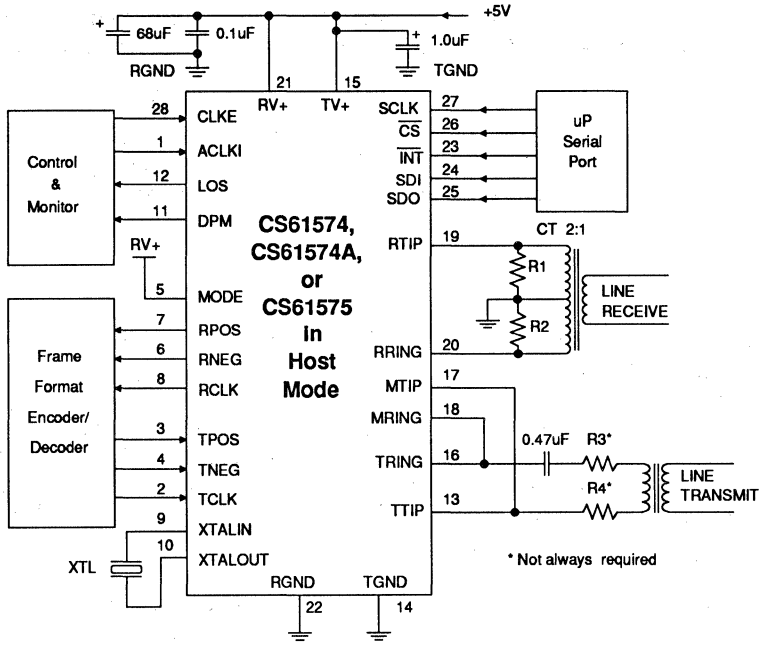
The AMI signal is driven to the line through these pins. In the CS61575 and CS61574A, this output is designed to drive a 75 Ω load. A transformer is required as shown in Table A2.

In the CS61574, this output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Table A4. When driving 75 Ω coax cable, two 2.2 Ω resistors should be added in series with the transformer primary. The transmitter will drive twisted-pair cable, terminated with 100 Ω or 120 Ω, without additional components.

Ordering Guide

Model	Frequency	FIFO Depth (Bits)	Package
CS61575-IP1	T1 & PCM-30	192	28-pin Plastic DIP
CS61575-IL1	T1 & PCM-30	192	28-pin PLCC
CS61574A-IP1	T1 & PCM-30	32	28-pin Plastic DIP
CS61574A-IL1	T1 & PCM-30	32	28-pin PLCC
CS61574-ID	T1 only	32	28-pin CERDIP
CS61574-ID1	T1 & PCM-30	32	28-pin CERDIP
CS61574-IP	T1 only	32	28-pin Plastic DIP
CS61574-IP1	T1 & PCM-30	32	28-pin Plastic DIP
CS61574-IL	T1 only	32	28-pin PLCC
CS61574-IL1	T1 & PCM-30	32	28-pin PLCC

APPLICATIONS



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3&4 Ω	Transmit Transformer	Crystal XTL
CS61574	1.544	110	200	0	1:2	CXT6176
	2.048	120	240	0	1:2	CXT8192
	2.048	75	150	2.2	1:2	CXT8192
CS61574A OR CS61575	1.544	110	200	0	1:1.15	CXT6176
	2.048	120	240	0	1:1.26	CXT8192
	2.048	75	150	0	1:1	CXT8192

Figure A1. Host Mode Configuration

Line Interface

Figures A1-A3 show the typical configurations used to connect the line interface to a line through transmit and receive transformers. Note that the CS61574A/CS61575 transmitter transformer requirements have changed from those of the CS61574. This new transformer allows the CS61574A/CS61575's lower power driver to be implemented.

The receiver transformer is center tapped and center grounded with resistors between the center tap and each leg on the IC side. These resistors provide the termination for the line.

Figures A1-A3 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the transmission of a space (zero) as the transformer tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

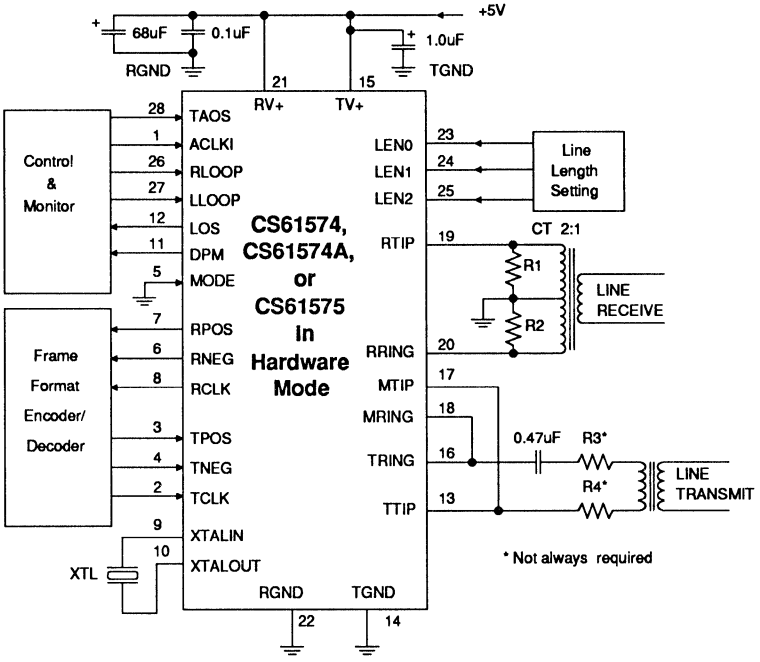


Figure A2. Hardware Mode Configuration

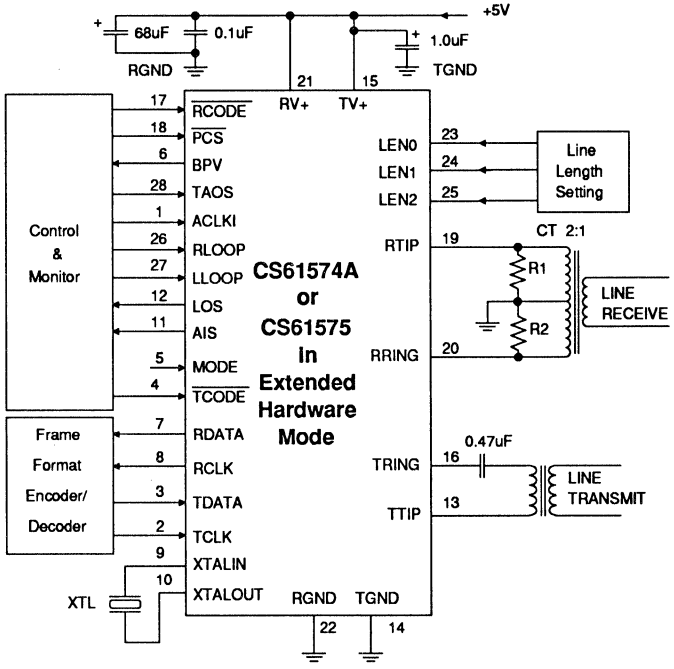


Figure A3. Extended Hardware Mode Configuration

CS61575 and CS61574A Transmitter Transformer

Target transformer specifications for the CS61574A and CS61575 transmitter are given in Table A1. The use of other transformer specifications can also result in acceptable performance.

Turns ratios:
1:1.26 ±1.5% for 120 ohm G.703 cable
1:1 ±1.5% for 75 ohm G.703 cable
1:1.15 ± 5% for 100 ohm T1 cable.

Primary inductance: 1.5 mH min measured at 772 kHz.

Primary Leakage inductance: 0.3 µH max at 772 kHz with secondary shorted.

Secondary Leakage Inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 18 pF max, primary to secondary

ET-constant: 16 V–µs minimum for T1; 12 V-us minimum for PCM-30.

Table A1. CS61574A and CS61575 Transmittter Transformer Specifications.

Table A2 lists transformers which have been qualified by Crystal Semiconductor for use when upgrading existing CS61574 boards to the CS61574A or CS61575. Table A3 lists transformers for new board designs. Table A3 transformers provide higher isolation performance (as may be required for European applications).

Application	Vendor	Transformer
T1	Pulse Eng. Schott	PE-65388 67124840
PCM-30	Pulse Eng. Schott	PE-65389 67124850

Table A3. Recommended CS61574A and CS61575 Transmit Transformers for New Designs

Receiver Transformers

The receivers of the CS61575, CS61574A and CS61574 use a 1:1:1 ± 5% transformer. Since pulse shapes are not measured at the receiver, the receive transformer specifications are not critical. Specifications similar to that for the CS61574 transmitter transformer (Table A4) provide excellent performance.

Transformer Used with CS61574		Application	Transformer for Use with CS61574A, CS61575	
Vendor	Part Number		Vendor	Part Number
Pulse Eng. Schott Schott	PE-64931 67112060 67115100	T1	Pulse Eng. Schott	PE-65387 67124980
		PCM-30 75 Ω	Pulse Eng.	PE 65400
		PCM-30 120 Ω	Pulse Eng.	PE 65401

Table A2. CS61574A and CS61575 Transmitter Transformers for existing CS61574 boards

CS61574 Transmit Transformers

Key CS61574 transmit transformer specifications are given in Table A4. Transformers listed in Table A5 have been found to be suitable for use with the CS61574. Figure A4 shows the connections for some of the recommended transformers for the transmitter.

Turns ratio: 1:2 (or 1:1:1) ±5%

Primary inductance: 600 µH min measured at 772 kHz.

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted.

Secondary leakage inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 23 pF max, primary to secondary.

ET-constant: 16V-us minimum for T1; 12 V-us minimum for PCM-30.

Table A4. Receiver and CS61574 Transmitter Transformer Specifications

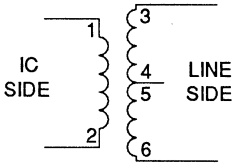
Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott	67115100 & 67124670
Schott	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the other Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A5. Recommended Receiver and CS61574 Transmitter Transformers

Interfacing The CS61575 and CS61574A With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A5. In this case, the line interface and CS2180B are in host mode controlled by a microprocessor serial interface. If the line interface is used in hardware mode, then the line interface RCLK output must be inverted before being input to the CS2180B. If the CS61575 or CS61574A is used in extended hardware mode, the RCLK output does not have to be inverted before being input to the CS2180B.



Bell Fuse 0553-5006-IC
Schott Corp. 67112060 & 67115100
Pulse Engineering 5764 & PE-64931

Figure A4. Some Recommended Transmitter Transformer Configurations

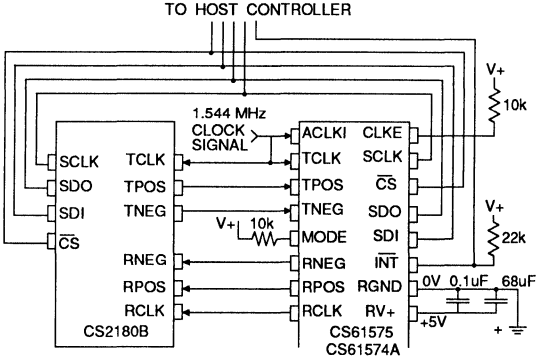


Figure A5. Interfacing the CS6157x with a CS2180B (Host Mode)

Transmit Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61575 in local loopback mode can be used as a jitter attenuator. The inputs to the jitter attenuator are TPOS, TNEG, TCLK. The outputs from the jitter attenuator are RPOS, RNEG and RCLK.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for PCM-30 applications.

Designing for AT&T 62411

For additional information on the requirements of AT&T 62411 and the design of an appropriate system synchronizer, please refer to the Crystal Semiconductor Application Notes: "AT&T 62411 Design Considerations – Jitter and Synchronization" and "Jitter Testing Procedures for Compliance with AT&T 62411".

Designing for T1 Long Haul Applications

Please refer to the Crystal Semiconductor Application Note: "T1 Long Haul Physical Layer Interface".

Semiconductor Corporation

CS6158A

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Low Power Consumption (typically 175 mW)
- Internal generation of transmitted pulse width and pulse shape.
- 14 dB of Transmitter Return Loss
- Fully Monolithic Clock Recovery
- Minimum External Components (no external crystal required)

General Description

The CS6158 and CS6158A combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device. The line interface unit (LIU) operates from a single 5 volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. These devices offer pin compatibility with the higher functionality CS61535, CS61535A, CS61574, and CS61574A.

Applications

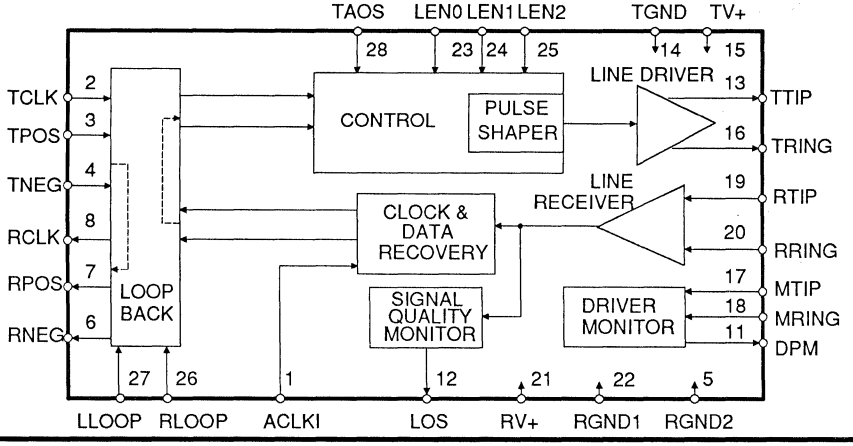
Synchronous communication systems which employ frame buffers, including:

- Central Office Exchanges
- Digital Access and Cross Connect Systems
- Large PABX's

ORDERING INFORMATION

CS6158A-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS6158A-IL1	28 Pin PLCC	T1 & PCM-30
CS6158-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS6158-IL1	28 Pin PLCC	T1 & PCM-30

Block Diagram



Preliminary Product Information | This document contains information on a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
CS6158A Power Consumption (Note 4) 100% ones density & max. line length @ 5.25V	P_C	-	290	350	mW
CS6158A Power Consumption (Note 4) 50% ones density & 300 ft. line length @ 5.0V	P_C	-	175	-	mW
CS6158 Power Consumption (Note 4) 100% ones density & max. line length @ 5.25V	P_C	-	620	760	mW
CS6158 Power Consumption (Note 4) 50% ones density & 300 ft. line length @ 5.0V	P_C	-	400	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving 25 Ω load over operating temperature range. Includes CS6158 and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

CS6158A DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5 %;

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 5) PINS 1-4, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 5) PINS 1-4, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 5) I_{OUT}=-40 uA PINS 6-8, 11, 12	V_{OH}	4.0	-	-	V
Low-Level Output Voltage (Note 5) I_{OUT}= 1.6 mA PINS 6-8, 11, 12	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Notes: 5. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40μA).

CS6158 DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 6) PINS 1-4, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 6) PINS 1-4, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 6) I_{OUT}=-40 uA PINS 6-8, 11, 12	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 6) I_{OUT}= 1.6 mA PINS 6-8, 11, 12	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Notes: 6. Output drivers will output CMOS logic levels into a CMOS load.

3

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Min	Typ	Max	Units
DRIVER PERFORMANCE MONITOR				
CS6158A MTIP/MRING Sensitivity: Differential Voltage Required for Detection				
With one input at 1.5 V	-	0.75	-	V
With one input at 0 V	-	2.0	-	V

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes (Note 7)					
Line Length Selections LEN2/1/0 = 0/0/0 & 0/1/0 (Measured at xfmr output; for 0/0/0 see Figure 5)		2.14 2.7	2.37 3.0	2.6 3.3	V V
All line length settings except, LEN2/1/0 = 0/0/0, 0/1/0 (Measured at the DSX; Normalization factor for Figure 4)		2.4	3.0	3.6	V
Load Presented To Transmitter Output (Note 7)					
	CS6158A	-	75	-	Ohms
	CS6158	-	25	-	Ohms
Jitter Added by the Transmitter (Note 8)	10Hz - 8kHz	-	0.005	-	UI
	8kHz - 40kHz	-	0.008	-	UI
	10Hz - 40kHz	-	0.010	-	UI
	Broad Band	-	0.015	-	UI
Power in 2kHz band about 772kHz (Note 9)		12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (Note 9) (referenced to power at 772kHz)		-29	-38	-	dB
Positive to Negative Pulse Imbalance (Note 9)		-	0.2	0.5	dB
CS6158A PCM-30 Transmitter Return Loss (Notes 7, 17)					
	51kHz - 102kHz	8	-	-	dB
	102kz - 2.048MHz	14	-	-	
	2.048MHz - 3.072MHz	10	-	-	
RECEIVER					
Sensitivity Below DSX (0dB = 2.4V)		-10	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold	T1 pulse settings	-	65	-	% of peak
	PCM-30 LEN2/1/0 = 000	-	50	-	
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance (Note 10)	10kHz - 100kHz	0.4	-	-	UI
	2 kHz	6.0	-	-	
	10Hz and below	300	-	-	
CS6158A RTIP/RRING Input Impedance		-	50k	-	Ohms

Notes: 7. Using transformers as recommended in Application Section.
8. Input signal to TCLK is jitter free.
9. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
10. See Figure 7.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
ACLKI Frequency	(Note 11)	f_{ackli}	-	1.544	-	MHz
CS6158A RCLK Cycle Width		t_{pw1}	320	-	980	ns
When Phase Locked		t_{pwh1}	130	190	240	ns
	(Notes 12, 13, 15)	t_{pwl1}	100	458	850	ns
CS6158 RCLK Cycle Width		t_{pw1}	320	648	980	ns
When Phase Locked		t_{pwh1}	-	508	-	ns
	(Notes 12, 13, 15)	t_{pwl1}	100	140	-	ns
CS6158A RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1} / t_{pw1}	-	29	-	%
CS6158 RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1} / t_{pw1}	-	78	-	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Setup Time	(Notes 13, 15)	t_{su1}	50	-	-	ns
RCLK to RPOS/RNEG Hold Time	(Notes 13, 15)	t_{h1}	50	-	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

Notes: 11. ACLKI provided by an external source or TCLK.
12. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
13. Max & Min RCLK duty cycles and pulse widths and RX setup and hold times are for worst case jitter conditions: i.e. 0.4 UI AMI data displacement for T1 or 0.2 UI AMI data displacement for CCITT 2.048 MHz. See text section on *Jitter and Recovered Clock.*
14. At max load of 1.6 mA and 50 pF.
15. Not production tested. Guaranteed by design and/or characterization.
16. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK for the CS6158.
17. Return loss = $20\log_{10}ABS((z_1+z_0)/(z_1-z_0))$ where z_1 = impedance of transmitter, and z_0 = impedance of line load. Measured with alternating 1010 pattern.

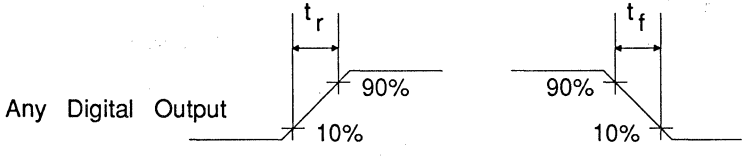


Figure 1. - Signal Rise and Fall Characteristics

PCM-30 SWITCHING CHARACTERISTICS

(T_A = - 40 ° to 85 ° C; TV+ ,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
ACLKI Frequency	(Note 11)	f_{ackli}	-	2.048	-	MHz
CS6158A RCLK Cycle Width		t_{pw1}	310	488	670	ns
When Phase Locked		t_{pwh1}	90	140	190	ns
	(Notes 12, 13, 15)	t_{pwl1}	120	348	580	ns
CS6158 RCLK Cycle Width		t_{pw1}	310	488	670	ns
When Phase Locked		t_{pwh1}	-	348	-	ns
	(Notes 12, 13, 15)	t_{pwl1}	100	140	-	ns
CS6158A RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1} /t_{pw1}	-	29	-	%
CS6158 RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1} /t_{pw1}	-	71	-	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Setup Time	(Notes 13, 15)	t_{su1}	50	-	-	ns
RCLK to RPOS/RNEG Hold Time	(Notes 13, 15)	t_{h1}	50	-	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 16)	t_{pwh2} / t_{pw2}	44	50	53	%

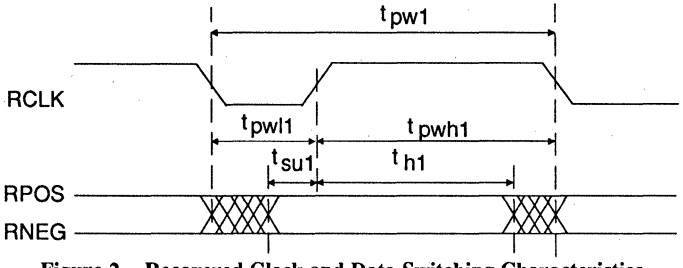


Figure 2. - Recovered Clock and Data Switching Characteristics

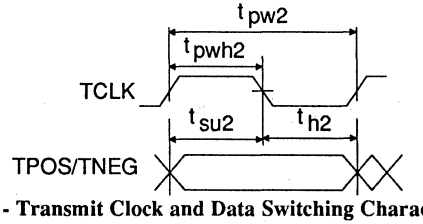


Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Enhancements in CS6158A

The performance impovements made to the 'A' version of the CS6158 are the following:

- 50% reduction in power consumption
- 14 dB of transmitter return loss (during transmission of both marks and spaces) improves signal quality
- The pulse width of PCM-30 transmitted pulses is set internally by the CS6158A (and not by the TCLK input duty cycle)
- Upon power up, RCLK immediately starts and LOS (loss of signal) is set high
- When the transmitter senses the absence of a signal on TCLK, TTIP and TRING are forced to zero.
- The loss of signal condition is exited upon recognition of 12.5% one's density (4-of-32 and no more than 14 consecutive zeros)
- The driver performance monitor operates over a wider range of input signal levels

The CS6158A is a pin compatible replacement for the CS6158 which maintains compatibility with existing printed circuit board designs. The upgrade of an existing design requires specification of the CS6158A instead of the CS6158 and specification of a new pin compatible transmitter transformer from table A2 in the applications section. The new transformer supports the lower power consumption.

Transmitter

The transmitter takes data from a T1 (or PCM-30) terminal and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		Reserved
0	0	0	PCM-30 G.703	2.048 MHz CCITT
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1 - Line Length Selection

Either T1 (DSX-1 or Network Interface) or PCM-30 G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 1. The CS6158A line driver is designed to drive a 75 Ω equivalent load. The CS6158 drives a 25 Ω load.

For PCM-30 applications, the CS6158A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

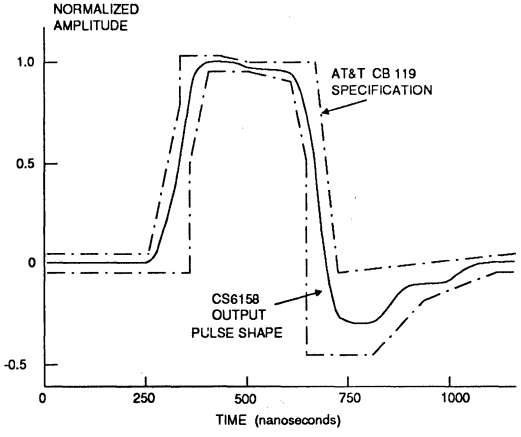


Figure 4 - Typical Pulse Shape at DSX-1 Cross

	For coaxial cable, 75 ohm load and transformer specified in Application. Section	For shielded twisted pair, 120 ohm load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05 *	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

* When configured with a 0.47 uF nonpolarized capacitor in series with the Tx transformer primary as shown in Figure A1.

Table 2 - CCITT G.703 Pulse Specifications

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the CS6158A or CS6158 to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 4.

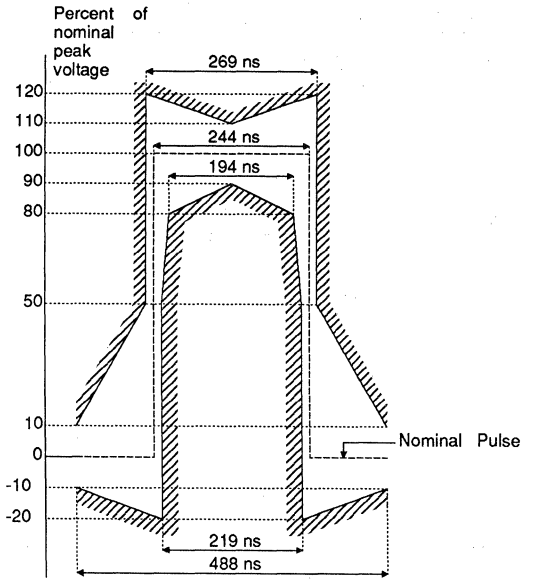


Figure 5 - Mask of the Pulse at the 2048 kbps Interface

These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narraower than the optimal pulse width for DSX-1 (350 ns). The CS6158A automatically adjusts the pulse width based upon the "line length " selection made.

The PCM-30 G.703 pulse shape is supported with line length selection LEN2/1/0=000. The pulse width will meet the G.703 pulse shape template shown in Figure 5, and specified in Table 2.

Only in the case of CS6158 and LEN2/1/0 = 000, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 5, and specified in Table 1, assuming the TCLK duty cycle and frequency are appropriate. The rising and falling edge of TCLK control the time at which the rising and falling edges of the output pulse occur.

The CS6158A transmitter will detect a failed TCLK, and will insure that neither TTIP nor

TRING gets stuck high. If the clock signal is removed from TCLK on the CS6158, TPOS and TNEG should both be low during the last falling edge of TCLK. This places the CS6158 in a low-power dissipation mode.

When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals down to approximately 300 mV in amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS6158A or CS6158 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for PCM-30, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI, into 13 equal divisions of phases. Continuous calibration ensures timing

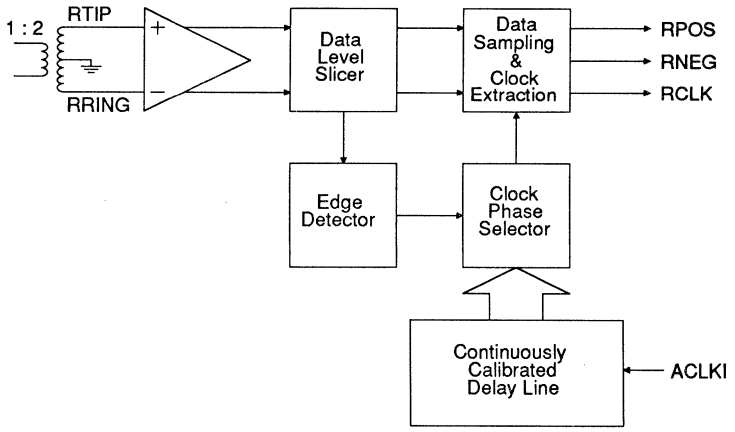


Figure 6. - Receiver Block Diagram

accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that plot shown in Figure 7.

The CS6158 device outputs a clock at RCLK after the first signal is input to RTIP/RRING. The CS6158A outputs a clock on RCLK immediately upon power-up. In either case, the clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

Data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock.

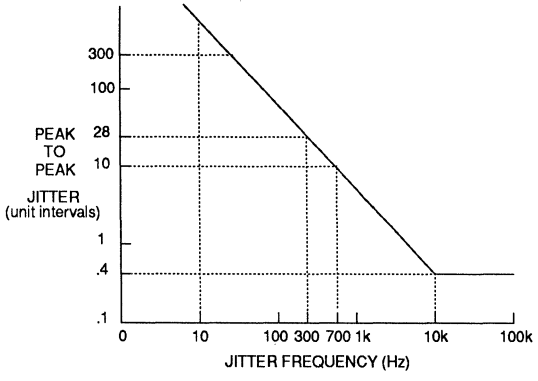


Figure 7. - Input Jitter Tolerance of Receiver

Jitter and Recovered Clock

The CS6158A and CS6158 are designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UI. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS6158A and CS6158, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similiar calculations hold for PCM-30 rates.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by

seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS6158A and CS6158, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS6158A and CS6158 is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. In the CS6158, LOS returns to a logic zero upon receipt of the first bit at the RTIP/RRING inputs. In the CS6158A, LOS returns to logic zero when the received signal returns to 12.5% ones density (based on 4 ones out of 32 bit periods, and no more than 14 zeros in a row).

Also in the CS6158A, a power-up or manual reset will set LOS high.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line. Because RCLK cycle times vary, selecting RLOOP will result in adding jitter to the transmitted data. *Therefore selection of the RLOOP function on a functioning link is not recommended.* Rather, it is recommended that remote loopbacks be implimented external to the CS6158A and CS6158, for example, by using a frame buffer in the data path between the CS6158A and CS6158 receiver and transmitter.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6158A and CS6158 are able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted AMI signal on input pins, MTIP and MRING. If no valid AMI signal is present on MTIP and MRING for 64±2 clock cycles, the DPM pin goes high.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring device, rather than having it monitor its own performance.

For the CS6158 only, the following application procedure is recommended to provide immunity from spurious DPM reports. If the controller on the line card detects that DPM has gone high, the controller should reconfirm that DPM is still high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can occur only when ones density is very low.

Power On Reset / Reset

Upon power-up, the CS6158A and CS6158 are held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear the internal logic.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP or LLOOP).

In the CS6158A, a reset will set LOS high.

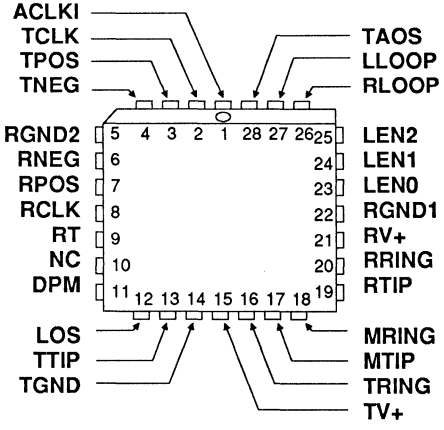
Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as close as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap bread-boarding of the CS6158A and CS6158 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

ALT. EXTERNAL CLOCK INPUT	ACLKI	1	28	TAOS	TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	TCLK	2	27	LLOOP	LOCAL LOOP BACK
TRANSMIT POSITIVE PULSE	TPOS	3	26	RLOOP	REMOTE LOOP BACK
TRANSMIT NEGATIVE PULSE	TNEG	4	25	LEN2	BIT 2 OF LINE LENGTH SELECT
RECEIVE GROUND2	RGND2	5	24	LEN1	BIT 1 OF LINE LENGTH SELECT
RECEIVED NEGATIVE PULSE	RNEG	6	23	LEN0	BIT 0 OF LINE LENGTH SELECT
RECEIVED POSITIVE PULSE	RPOS	7	22	RGND1	RECEIVE GROUND1
RECOVERED CLOCK	RCLK	8	21	RV+	RECEIVE V+ (+5VDC)
RESISTOR TERMINATION	RT	9	20	RRING	RECEIVE RING
NO CONNECT	NC	10	19	RTIP	RECEIVE TIP
DRIVER PERFOMANCE MONITOR	DPM	11	18	MRING	MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP	MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND1, RGND2 - Ground, Pins 22 and 5

Power supply grounds for the device, except transmit drivers; typically 0 volts.

Control

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TAOS - Transmit All Ones select, Pin 28.

Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency selected by TCLK.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.

Either a 1.544 MHz (or 2.048 MHz for PCM-30) clock must be input to ACLKI, which is used to calibrate the receiver delay line. Since ACLKI is used to calibrate the receiver, RCLK will equal ACLKI upon loss of signal.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

RT - Resistor Termination, Pin 9.

This pin should be connected to a supply rail. Power consumption will be minimized by connecting pin to RV+ through a 1kΩ resistor.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS6158. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. In the CS6158, LOS returns to logic 0 on the first bit received. When in loss of signal state, received ones are output at RPOS/RNEG. In the CS6158A, LOS returns to a logic 0 when a 12.5% ones density signal returns (determined by receipt of 4 ones within 32 bit periods).

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

The receiver recovered clock and NRZ digital data is output on these pins. RPOS and RNEG are stable and valid on the rising edge of RCLK. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins.

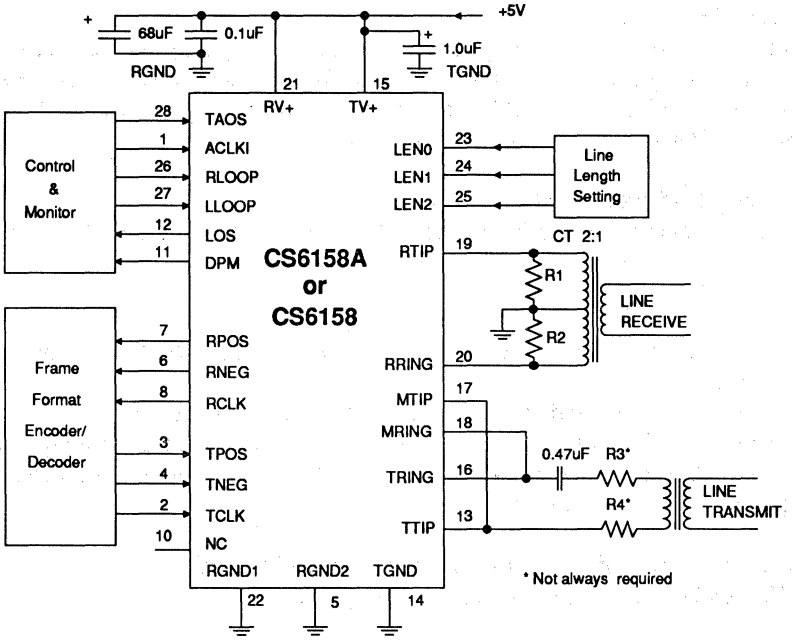
In the CS6158A, this output is designed to drive a 75 Ω ohm load. A transformer is required as shown in Table A1.

In the CS6158, this output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Table A4. When driving 75 Ω coax cable, approximately 4.4 ohms of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

Miscellaneous

NC - No Connect, Pin 10

Pin 10 may be left floating (recommended for new designs), or may be tied to ground.



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3&4 Ω	Transmit Transformer
CS6158	1.544	110	200	0	1:2
	2.048	120	240	0	1:2
	2.048	75	150	2.2	1:2
CS6158A	1.544	110	200	0	1:1.15
	2.048	120	240	0	1:1.26
	2.048	75	150	0	1:1

Figure A1. - Typical Connection Diagram

APPLICATIONS

Line Interface

Figure A1 shows the typical configuration for the CS6158A and CS6158. Note that CS6158A transmitter transformer requirements have changed from those of the CS6158. This new transformer allows the CS6158A's lower power driver to be implemented.

For T1 applications, the receiver transformer is center-tapped and center-grounded with 200 Ω resistors between the center tap and each leg on the IC side. These resistors provide the 100 Ω termination for the T1 line.

When terminating 2.048 MHz twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

For transmitting data at 2.048 MHz onto a 75 Ω coax cable, the terminating resistors should be

150 Ω to provide the necessary 75 Ω termination to the line.

Figure A1 shows a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the transmission of a space (zero) as the transformer tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

Interfacing the CS6158A with CS2180B T1 Transceiver

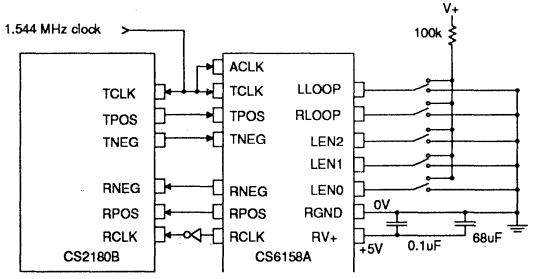


Figure A2. - Interfacing the CS6158A with a CS2180B

To interface with the CS2180B, connect the devices as shown in Figure A2.

CS6158A Transmitter Transformer

Target transformer specifications for the CS6158A transmitter are given in Table A1. The use of other transformer specifications can also result in acceptable performance.

Turns ratios:
1:1.26 ±1.5% for 120 Ω G.703 cable
1:1 ±1.5% for 75 Ω G.703 cable
1:1.15 ± 5% for 100 Ω T1 cable.

Primary inductance: 1.5 mH min measured at 772 kHz.

Primary Leakage inductance: 0.3 µH max at 772 kHz with secondary shorted.

Secondary Leakage Inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 18 pF max, primary to secondary.

ET-constant: 16 V-us minimum for T1; 12 V-us minimum for PCM-30.

Table A1. CS6158A Transmitter Transformer Specifications

Transformer Used with CS6158		Application	Transformer for Use with CS6158A	
Vendor	Part Number		Vendor	Part Number
Pulse Eng. Schott Schott	PE-64931 67112060 67115100	T1	Pulse Eng. Schott	PE-65387 67124980
		PCM-30 75 Ω	Pulse Eng.	PE 65400
		PCM-30 120 Ω	Pulse Eng.	PE 65401

Table A2.- CS6158A Transmitter Transformers for existing CS6158 boards

Application	Vendor	Transformer
T1	Pulse Eng. Schott	PE-65388 67124840
PCM-30	Pulse Eng. Schott	PE-65389 67124850

Note: Additional transformer options are available from Pulse Engineering and Schott

Table A3.- CS6158A Transmit Transformers for New Designs

with higher isolation performance (as may be required for European applications).

CS6158A and CS6158 Receiver Transformers

The receiver uses a 1:1:1 ± 5% transformer. Since pulse shapes are not measured at the receiver, the receive transformer specifications are not critical.

Turns ratio: 1:2 (or 1:1:1) ± 5%.

Primary inductance: 600 µH min measured at 772 kHz.

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted.

Secondary leakage inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 23 pF max, primary to secondary.

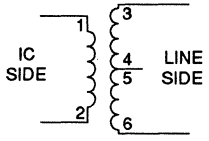
ET-constant: 16 V-us minimum for T1; 12 V-us minimum for PCM-30.

Table A4. - Transformer Specifications for CS6158A Receiver and for CS6158.

Specifications similar to that for the CS6158 transmitter transformer (Table A4) provide excellent performance.

CS6158 Transmit Transformers

Key CS6158 transmit transformer specifications are given in Table A4. Transformers listed in Table A5 have been found to be suitable for use with the CS6158. Figure A3 shows the connections for some of the recommended transformers for the transmitter.



Pulse Engineering 5764 & PE-64931
Bell Fuse 0553-5006-16
Schott 67112060 & 67115100

Figure A3.- Some Recommended CS6158 Transmitter Transformer Configurations

Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott	67115100 & 67124670
Schott	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the other Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the other Schott transformers are preferred.

Table A5. - Suitable Transformers for CS6158A Receiver and for CS6158

Semiconductor Corporation

CS6159

Low Power PCM Line Interface

Features

- Provides CMOS Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Internal generation of transmitted pulse width and pulse shape.
- Low power - typically 180 mW
- Small package - 300 mil DIP & SOIC
- Minimum External Components

General Description

The CS6159 combines the analog transmit and receive line interface functions for a T1 or PCM-30 interface in a 24-pin skinny-DIP or SOIC device. The line interface operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for line lengths ranging from 0 to 655 feet from a DSX-1 cross connect.

Applications

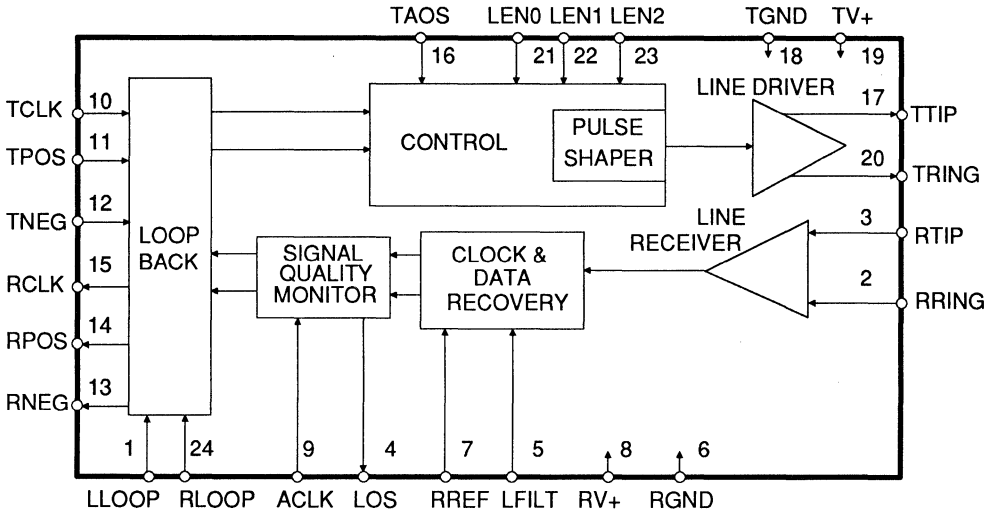
- Central Office Exchanges
- Digital Access and Cross Connect Systems
- Customer Premises Equipment
- PABX's

Ordering Information

CS6159-IP1	24 Pin Plastic DIP (300 mils)	T1 & PCM-30
CS6159-IS1	24 Pin Plastic SOIC	T1 & PCM-30

3

Block Diagram



Preliminary Product Information | This document contains information on a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+)+ 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Consumption (Note 4) 100% ones density & max. line length @ 5.25V	P_C	-	-	335	mW
Normal Power Consumption (Note 4) 50% ones density & 300 ft. line length @ 5.0V	P_C	-	180	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation at 1.544 Mbps while driving 54 Ω load over operating temperature range. Includes CS6159 and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load. Power dissipation at 2.048 Mbps will be 30% higher.

DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+, RV+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage Pins 1, 9-12, 16, 21-24	V_{IH}	2.0	-	-	V
Low-Level Input Voltage Pins 1, 9-12, 16, 21-24	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 5) I_{OUT}= - 40 uA Pins 4, 13-15	V_{OH}	4.0	-	-	V
Low-Level Output Voltage I_{OUT}= +1.6 mA Pins 4, 13-15	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Notes: 5. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40 µA).

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C; TV+,RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes					
Line Length Selections LEN2/1/0 = 0/0/0 & 0/1/0 (Measured at xfmr output)		2.7	3.0	3.3	V
All line length settings except, LEN2/1/0 = 0/0/0, 0/1/0 & 0/0/1 (Measured at the DSX; Normalization factor for Figure 4)		2.4	3.0	3.6	V
Load Presented To Transmitter Output		-	54	-	Ohms
Jitter Added by the Transmitter (Note 6)	10Hz - 8kHz	-	0.005	-	UI
	8kHz - 40kHz	-	0.008	-	UI
	10Hz - 40kHz	-	0.010	-	UI
	Broad Band	-	0.015	-	UI
Power in 2kHz band about 772kHz	(Note 7)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power at 772kHz)	(Note 7)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 7)	-	0.2	0.5	dB
RECEIVER					
Sensitivity Below DSX (0dB = 2.4V)		-10	-	-	dB
Loss of Signal Threshold		-	0.325	-	V
Data Decision Threshold	T1 pulse settings	-	65	-	% of
	CCITT LEN2/1/0 = 000	-	50	-	Peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance (Notes 8, 9)	10kHz - 100kHz	0.3	-	-	UI
	10Hz and below	300	-	-	
PLL 3 dB Bandwidth	(Note 9)	-	20	-	kHz
PLL Jitter Peaking	(Note 9)	-	1.4	-	dB

Notes:
6. Input signal to TCLK is jitter free.
7. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
8. See Figure 7.
9. Contact the factory for the recommended external component values. Assumes 1-in-8 input data pattern.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 10)	f_{out}	-	1.544	-	MHz
RCLK Cycle Width		t_{pw1}	646	648	650	ns
		t_{pwh1}	-	324	-	ns
	(Notes 12, 13, 15)	t_{pwl1}	-	324	-	ns
RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Falling Setup Time	(Note 15)	t_{su1}	240	324	-	ns
RCLK Falling to RPOS/RNEG Hold Time	(Note 15)	t_{h1}	240	324	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

PCM-30 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C; TV+,RV+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Frequency		f_{in}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 11)	t_{pwh2}/t_{pw2}	44	50	56	%
ACLK Frequency	(Note 10)	f_{out}	-	2.048	-	MHz
RCLK Cycle Width		t_{pw1}	484	488	492	ns
		t_{pwh1}	-	244	-	ns
	(Notes 12, 13, 15)	t_{pwl1}	-	244	-	ns
RCLK Duty Cycle	(Notes 12, 13, 15)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Falling Setup Time	(Note 15)	t_{su1}	160	244	-	ns
RCLK Falling to RPOS/RNEG Hold Time	(Note 15)	t_{h1}	160	244	-	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns

Notes: 10. ACLK provided by an external source or TCLK.
11. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK.
12. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
13. Max & Min RCLK duty cycles and cycle widths are for worst case jitter conditions.
14. At max load of 1.6 mA and 50 pF.
15. Not production tested. Guaranteed by design and/or characterization. Not applicable during loss of signal.

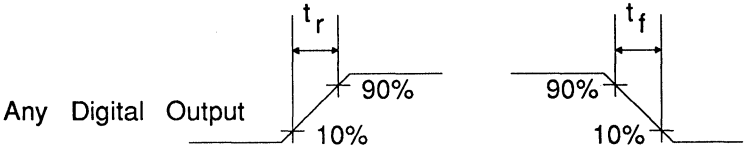


Figure 1. - Signal Rise and Fall Characteristics

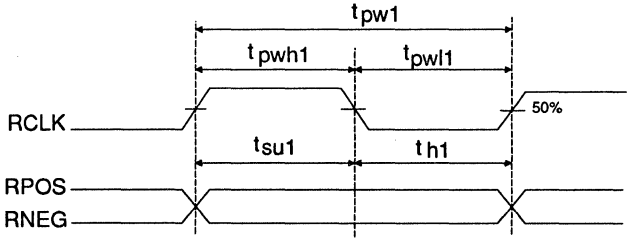


Figure 2. - Recovered Clock and Data Switching Characteristics

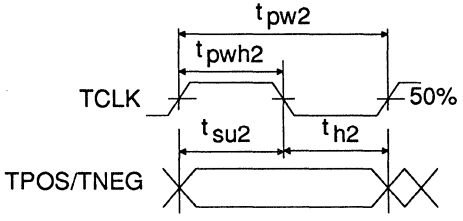


Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 or PCM-30 transceiver and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 or PCM-30 G.703 pulse shapes may be selected. For T1 applications, line lengths from 0 to 655 feet (as measured from the CS6159 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by digital "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 Volt supply, a 1.36:1, step-up transformer is required. The line driver is designed to drive a 54 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. For T1 applications, these phases are used to trigger different portions of the output waveform. For T1 DSX-1 applications, the line length selection offers a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS6159 modifies the output pulse to meet the requirements of ANSI T1.102, Bellcore TR-TSY-000499, AT&T Compatibility Bulletin 119 and the CCITT G.703 1.544 Mbps template. The exact pulse shape achieved at the DSX-1 can be affected by details of the board layout, transformer selection, and other factors. For cable types other than ABAM, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		Reserved
0	0	0	PCM-30 G.703	2.048 MHz CCITT
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1 - Line Length Selection

The T1 Network Interface pulse shapes meet FCC Part 68 for 0 dB line build out and ANSI T1.403 pulse shapes as shown in Table 1.

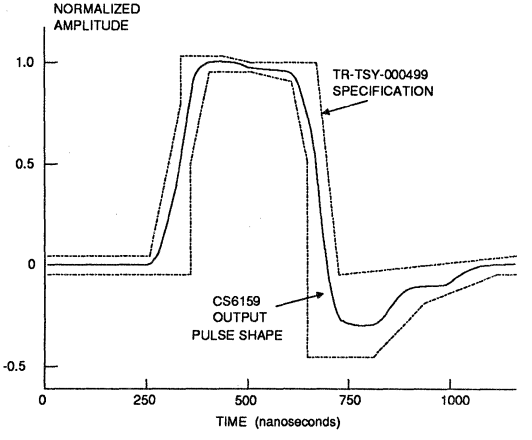


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75 ohm load and transformer specified in Table A1.	For shielded twisted pair, 120 ohm load and transformer specified in Table A1.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05 *	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

* When configured with a 0.47 uF nonpolarized capacitor in series with the Tx transformer primary as shown in Figure A1.

Table 2 - CCITT G.703 Pulse Specifications

3

The PCM-30 G.703 pulse shape is also supported with line length selection LEN2/1/0 = 000. In this case only, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 5, and specified in Table 2, assuming the transmitter is terminated correctly and the TCLK duty cycle and frequency are appropriate. The rising and falling edge of TCLK control the time at which the rising and falling edges of the output pulse occur. Transmitter termination information is provided in the applications section which appends this data sheet. Note that the pulse shape LEN2/1/0 = 010 generates the same amplitudes as the G.703 pulse (LEN2/1/0 = 000), but the pulse width is determined internally by the transmit delay line and will be approximately 263 ns when TCLK is 2.048 MHz.

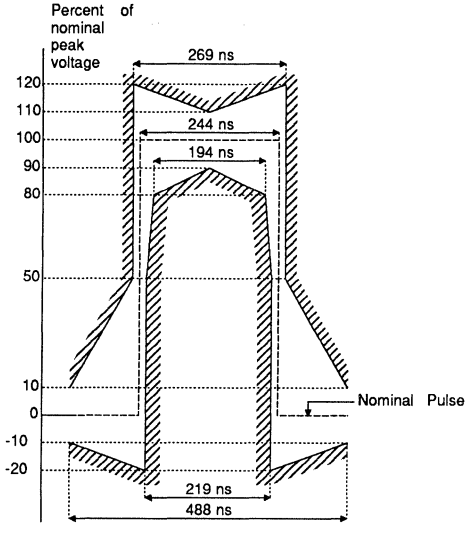


Figure 5 - Mask of the Pulse at the 2048 kbps Interface

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver typically is sensitive to signals down to approximately 325 mV in peak amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the CS6159 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43801, 43802, AT&T 62411

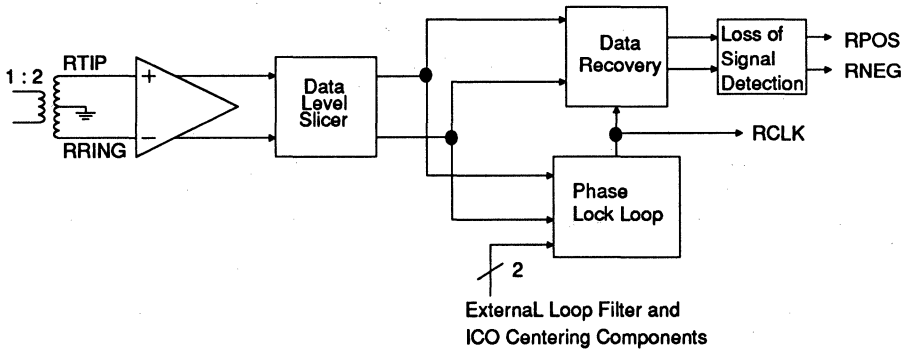


Figure 6. - Receiver Block Diagram

on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the CS6159 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43801, 43802, AT&T 62411 December 1988, Bellcore TR-TSY-000499 (Categories I & II), and CCITT REC. G.823. The center frequency of the PLL is controlled by the line length selection. Selection LEN2/1/0=000 sets the center frequency for PCM-30 operation. All other line length selections set the center frequency for T1 operation.

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. For all cases except where the PCM-30 pulse shape (LEN2/1/0 = 000) is selected, the comparator thresholds are dynamically established by peak detectors to be 65% of peak level. When the PCM-30 pulse shape is selected, the comparator threshold is 50% of

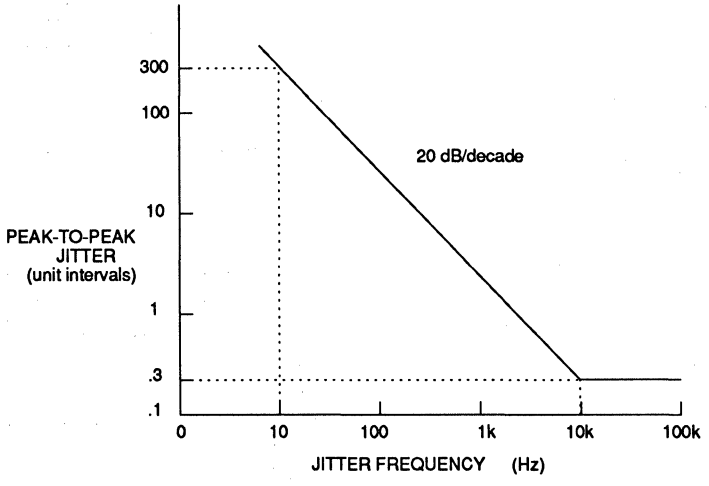


Figure 7. - Input Jitter Tolerance of Receiver

frequency set by an external resistor and by the line-length select inputs. This insures immunity to false lock over time and temperature variations.

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.325 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. Upon LOS the receiver substitutes ACLK for the incoming signal at RCLK (if ACLK is present) and forces RPOS and RNEG to zero. Therefore, RCLK will always be within required frequency limits (e.g.,± 50ppm). LOS returns to logic zero upon detection of 12.5% ones density. When LOS goes low, RCLK outputs the recovered clock, and RPOS and RNEG output the recovered data.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 1, high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

Remote Loopback

In remote loopback, the RCLK, RPOS and RNEG output signals are also sent back out on the line via TTIP and TRING. These signals are the recovered clock and data unless loss of signal has occurred and ACLK is present (see Loss of Signal section above). Transmitter inputs, TCLK, TPOS, TNEG, and TAOS, are ignored during remote loopback. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line.

Power On Reset/Reset

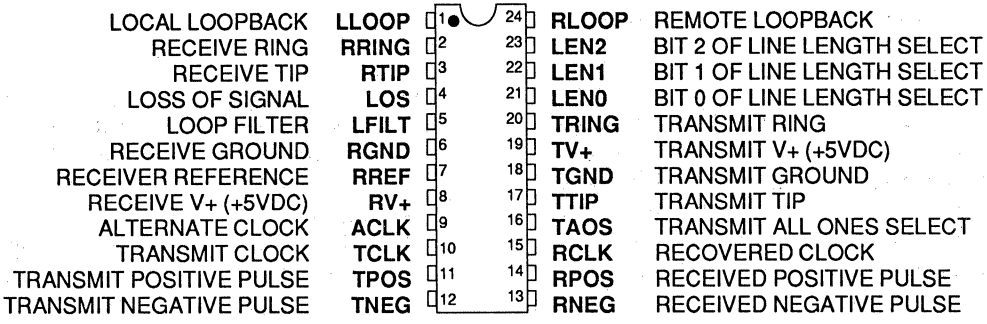
Upon power-up, the CS6159 is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the transmitter delay line commences. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the transmitter delay line is continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset a CS6159 when in operation. However, a manual reset is made by simultaneously setting both RLOOP and LLOOP high for least 200 ns. Reset will initiate on the falling edge of RLOOP and LLOOP.

Power Supply

The device operates from a single 5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. However, these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. If the same power bus is used, the receive power supply should be decoupled from ground with a 68 µF tantalum capacitor and a mylar or ceramic 0.1 µF capacitor. A 1.0 µF mylar or ceramic capacitor should be used on the transmit power supply. These capacitors should be located physically close to the device. If separate power busses are used for TV+/TGND and RV+/RGND, an additional 68 µF capacitor should be used on the transmit supply. TV+ must not exceed RV+ by more than 0.3V.

PIN DESCRIPTIONS



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 19.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 18.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 8.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 6.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Control

LLOOP - Local Loopback, Pin 1.
Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 24.
Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Inputs on TCLK, TPOS, TNEG, and TAOS are ignored

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 21, 22 and 23.
Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection. Also controls the receiver slicing levels and receive PLL center frequency.

TAOS - Transmit All Ones Select, Pin 16.

Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

Inputs

ACLK - Alternate External Clock Input, Pin 9.

Either a 1.544 MHz (or 2.048 MHz for CCITT) clock can be input to ACLK, which is substituted for RCLK upon loss of signal. If ACLK is grounded, no substitution takes place.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 10, 11 and 12.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 3 and 2.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK

RREF, LFILT - Receiver Reference, Loop Filter, Pins 7 and 5.

External components are connected to these pins to set the center-frequency of the PLL, and to provide a loop filter. Contact the factory for the recommended component values.

Status

LOS - Loss of Signal, Pin 4.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. LOS returns to a logic 0 when a 12.5% ones density signal returns.

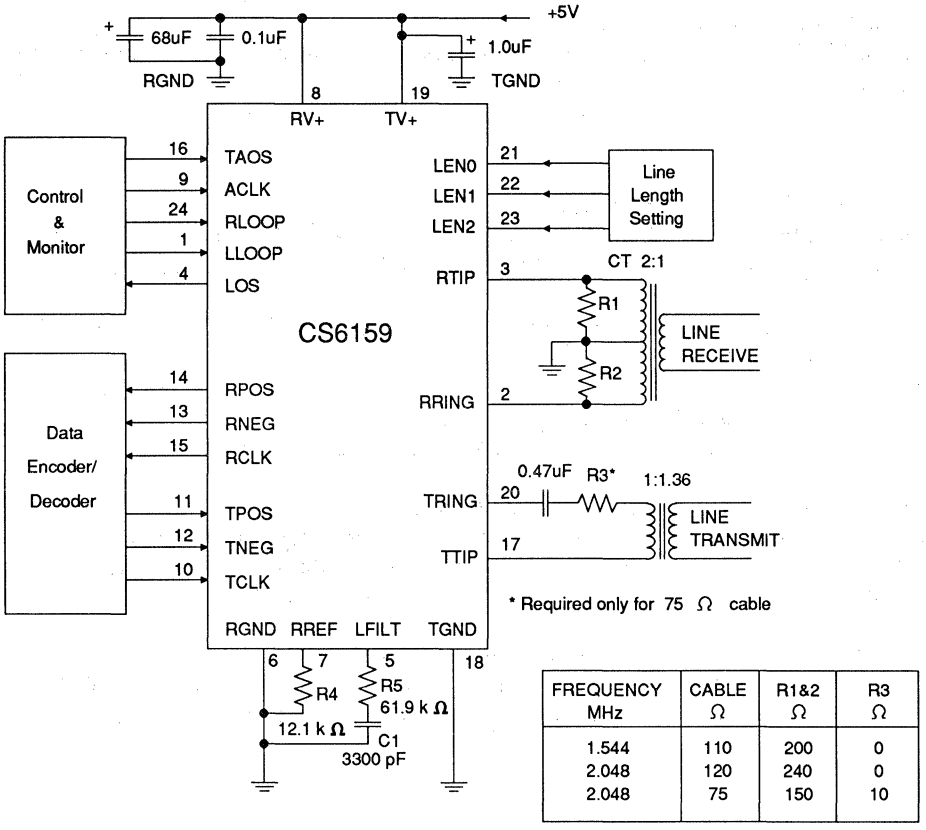
Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data, Pins 15, 14 and 13.

The recovered clock and NRZ data outputs of the receiver. RPOS and RNEG are stable and valid on the falling edge of RCLK. A positive pulse (with respect to ground) received on the RTIP pin is recovered by the receiver and causes a logic 1 to be output on RPOS. A positive pulse received on the RRING pin is recovered by the receiver and causes a logic 1 to be output on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 17 and 20.

The AMI signal is driven to the line through these pins. This output is designed to drive a 54 Ω load. A 1.36:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, a 10 Ω resistor should be added as shown in Figure A1. The transmitter will drive twisted-shielded pair cable, terminated with 100 Ω or 120 Ω, without additional components.



FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3 Ω
1.544	110	200	0
2.048	120	240	0
2.048	75	150	10

Figure A1: Typical Connection Diagram

APPLICATIONS

Line Interface

Figure A1 shows the typical application configuration for the CS6159. For T1 applications, the receiver transformer is center-tapped and center-grounded with 200 Ω resistors between the center tap and each leg on the CS6159 side. These resistors provide the 100 Ω termination for the T1 line.

When terminating 2.048 MHz twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

For transmitting data at 2.048 MHz onto a 75 Ω coax cable, a 10 Ω resistor is used between TTIP (or TRING) and the transformer. The resistor serves two functions. First, it provides the appropriate 54 Ω load to TTIP and TRING. Second, the resistor attenuates the signal slightly to meet the G.703 pulse amplitude requirements. Note that the 10 Ω resistor should not be used when interfacing to G.703 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Figure A1 shows a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the

core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the transmission of a space (zero) as the transformer tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

Transformers

The CS6159 requires two transformers. A 1:1.36 step-up transformer is used with the transmitter while a 1:2 center-tapped transformer is used with the receiver. The same transformers may be used with the CS6159 in both T1 and CEPT applications, although some CEPT applications may be subject to more stringent safety requirements in other countries imposing additional constraints upon the transformers. Contact the appropriate PTT or regulatory agency for more information on applicable performance and safety requirements. The recommended transmitter and receiver transformer specifications and approved vendor part numbers are summarized below.

Key receiver transformer specifications:

Turns ratio: 1:2 center-tapped (or 1:1:1).

Other specifications: not critical.

The transformers listed in Table A1 have been approved for use with the CS6159 receiver.

RECEIVER

Manufacturer	Part #
Pulse Engineering	PE-64931
Schott Corp.	67124670

Table A1. - Approved Receiver Transformers

Key transmitter transformer specifications:

Turns ratio: 1:1.36

Primary inductance: 600 µH min measured at 10kHz and 0.005 VRMS.

Leakage inductance: 1.3 µH max with secondary shorted.

Interwinding capacitance: 23 pF max, primary to secondary.

ET-Constant: 16 V-µs min. for T1,
12 V-µs for CEPT.

The transformers listed in Table A2 have been approved for use with the CS6159 transmitter.

TRANSMITTER

Manufacturer	Part #
Pulse Engineering	PE-64937
Schott	67112020

Table A2. - Approved Transmitter Transformers

Interfacing The CS6159 With The CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A2.

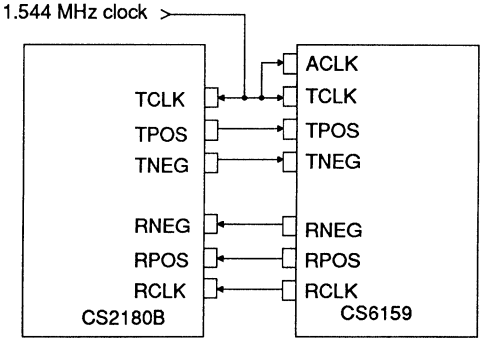


Figure A2. - Interfacing the CS6159 with CS2180B

• Notes •

Semiconductor Corporation

CXT6176
CXT8192

Pullable Quartz Crystals

Features

- Complements CS61534, CS61535, CS61535A, CS61544, CS61574, CS61574A, and CS61575 PCM Line Interface integrated circuits and CS61600 PCM Jitter Attenuator.

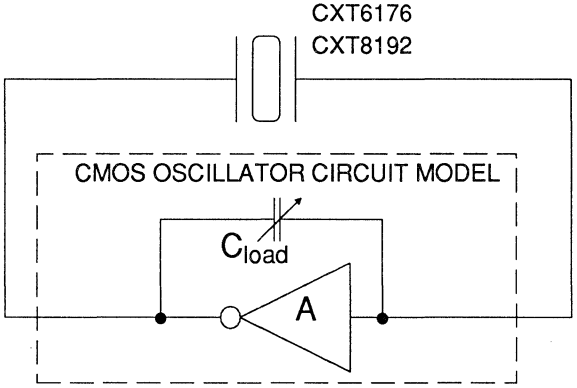
Description

Crystal Semiconductor's line interface and jitter attenuator IC's require unique performance specifications for the crystals. The CXT6176 and CXT8192 are built to meet Crystal's specifications for T1 and PCM-30 applications respectively.

Ordering Information

CXT6176	Crystal for T1 Applications
CXT8192	Crystal for PCM-30 Applications

3



Crystal Line Interface or Jitter Attenuator I.C.

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

CXT6176 Performance Specifications

Parameter			Min	Typ	Max	Units
Total Frequency Range		(Note 1)	-	370	390	ppm
Operating Frequency	C_{load} = 11.6 pF	(Note 2)	6.176803	-	-	MHz
	C_{load} = 19.0 pF	(Note 3)	6.175846	6.176	6.176154	MHz
	C_{load} = 37.0 pF	(Note 2)	-	-	6.175197	MHz

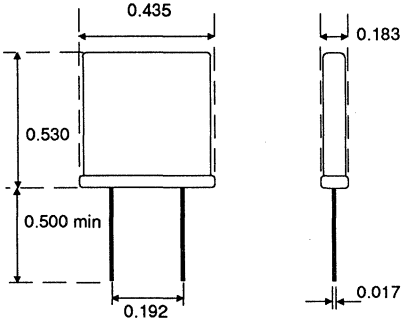
CXT8192 Performance Specifications

Parameter			Min	Typ	Max	Units
Total Frequency Range		(Note 4)	-	210	230	ppm
Operating Frequency	C_{load} = 11.7 pF	(Note 2)	8.192410	-	-	MHz
	C_{load} = 34.0 pF	(Note 2)	-	-	8.191590	MHz

Notes:
1. With C_{load} varying from 11.6 to 37.0 pF at a given temperature.
2. Measured at -40 to 85 °C.
3. Measured with Saunders 150D meter at 25 °C
4. With C_{load} varying from 11.7 to 34.0 pF at a given temperature.

General Specifications & Package Dimensions

Mode	Fundamental
Drive Level	2 mW (max)
Aging	5 ppm/yr. (max)
Shock	10 G's, 6 ms, 6 planes
Vibration	5 G's, 10 Hz to 500 Hz
Seal Leaks	10^{-8} cc/sec in Helium
Solderability	per Mil. std. 202, method 208
Thermal Shock	5 cycles, -55 to 125 C°, 1/2 cycle/hr. in air
Series Resistance	40 Ω (max) at 50 uW power



All measurements are in inches
Package identifier: HC-49

INTRODUCTION

Crystal's CS6300 and CS6301 are high-performance analog receivers for T3(44 MHz), E3 (34 MHz) and SONET STS-1/OC-1 (51 MHz) applications. These devices provide line equalization, plus clock and data recovery. For optical applications, the line equalizer can be bypassed, allowing the output of an optical receiver to be input to the clock recovery section. The Phase Lock Loop used for clock recovery has continuous frequency calibration, and matches the frequency of an external reference clock upon loss of signal.

USER'S GUIDE

Device	CS6300	CS6301
Applications Supported	T3, 44.736 MHz STS-1, 51.84 MHz OC-1, 51.84 MHz	E3 (34.368 MHz)

CONTENTS

Semiconductor Corporation

CS6300
CS6301

E3/T3/STS-1 Analog Line Receiver

Features

- CS6300 Provides Complete Analog Line Receiver for T3 and STS-1 Applications
- CS6301 Provides Complete Analog Line Receiver for E3 G.703/G.823 Applications
- Provides Line Equalization, and Clock and Data Recovery Functions
- T3/STS-1 performance is compatible with TR-TSY-000499 and TA-T54-000253, Issue 5
- Line equalizer can be bypassed for optical applications

General Description

The CS6300 provides the analog receive line interface functions for a 44.736 MHz T3 or 51.84 MHz STS-1 interface in a single 24 pin device. The CS6301 supports 34.368 MHz E3 operation. The line interface operates from a single +5 Volt supply and is transparent to the framing format.

Applications

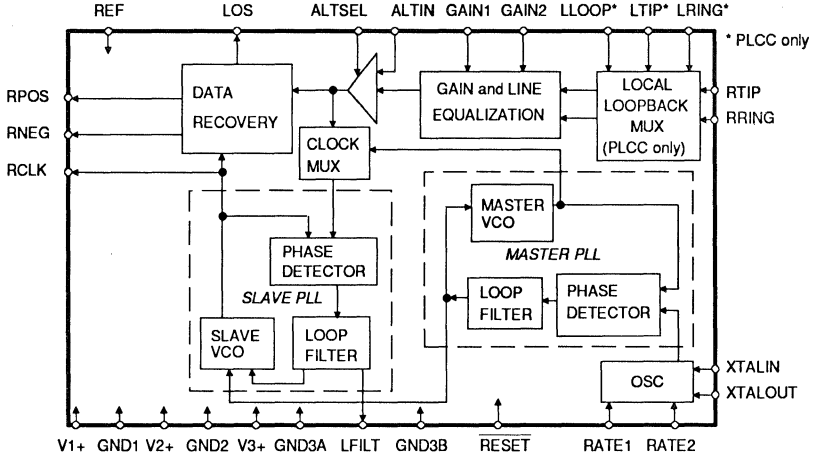
- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-3 cross connect.
- Interfacing customer premises equipment to a line.

Ordering Information

Contact Crystal Semiconductor

4

Contact Crystal Semiconductor for updated data sheet.



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512)445-7222

ANALOG SPECIFICATIONS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Slave PLL Jitter Transfer:	3 dB Bandwidth Peaking (Note 1)	- -	100 0.05	- -	kHz dB
Jitter Tolerance	(Notes 1,2)				
CS6301 @ 34.386 MHz:	10kHz - 800 kHz 100Hz - 1kHz	0.15 1.5	- -	- -	U.I. U.I.
CS6300 @ 44.736 MHz:	24kHz - 300kHz 2.3kHz	0.3 5	- -	- -	U.I. U.I.
CS6300 @ 51.84 MHz:	26kHz - 300kHz 2.3kHz	0.3 5	- -	- -	U.I. U.I.
Signal Noise Immunity	(Note 3)	-	11	-	dB
Output Jitter with Jitter-Free Input	(Note 1)	-	0.01	-	UIrms
Output Clock Duty Cycle	(Note 1)	45	-	55	%
Slave PLL Lock Aquisition Time	(Notes 1, 4)	-	1.0	-	ms
RTIP/RRING Input Impedance		4	6	-	kΩ
CS6300 Receiver Input Range	GAIN1=0, GAIN2=0 GAIN1=1, GAIN2=0 GAIN1=0, GAIN2=1	170 34 54	- - -	950 95 300	mV mV mV
CS6301 Receiver Input Range	GAIN1=0, GAIN2=0 GAIN1=1, GAIN2=0 GAIN1=0, GAIN2=1	200 40 62	- - -	1200 120 377	mV mV mV
ALTIN Signal Amplitude	(Note 5)	0.6	-	2.0	V_{p-p}

Notes:
1. Assumes external loop parameter components as defined in the application section. Measured with 2^{20}-1 pseudo-random, B3ZS or HDB3-encoded data.
2. Typical performance is shown in Figures 1, 2 and 3.
3. Measured with sinusoidal noise. Peak amplitude of noise is 11 dB down from peak amplitude of signal. The noise frequency is 22MHz ±22 kHz.
4. With device powered up. Measurement starts at the time when signal is reapplied to RTIP/RRING.
5. An ECL signal can be directly AC-coupled into ALTIN. CMOS and TTL signals should be attenuated before being AC-coupled.

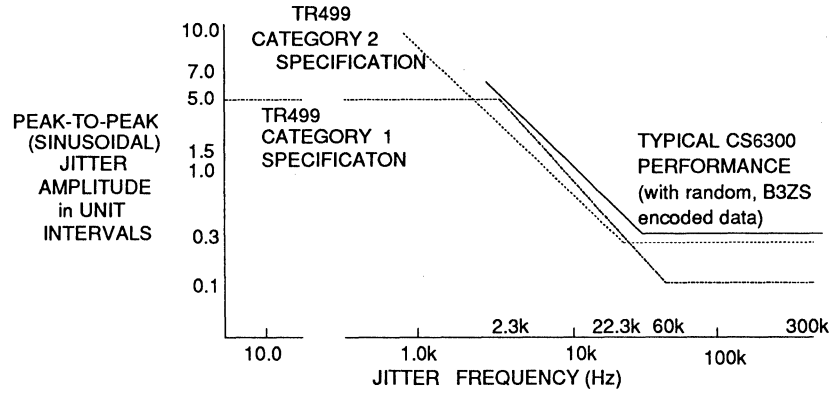


Figure 1. Typical CS6300 Jitter Tolerance at 44.736 MHz

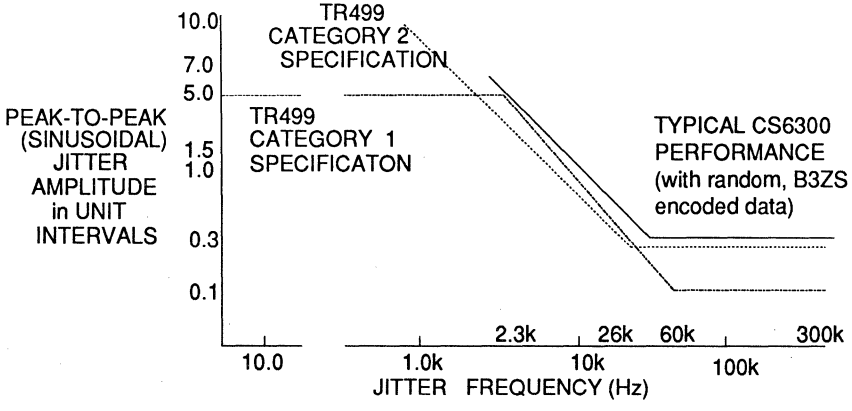


Figure 2. Typical CS6300 Jitter Tolerance at 51.84 MHz

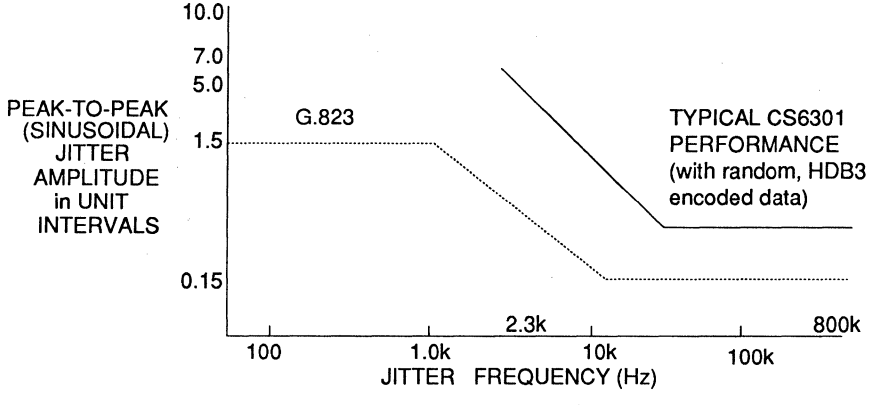


Figure 3. Typical CS6301 Jitter Tolerance at 34.386 MHz

CS6300 T3 SWITCHING CHARACTERISTICS

(T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
RCLK Pulse Width	(Notes 6, 7)	t_{pwh} t_{pwl}	10.1 10.1	11.177 11.177	12.2 12.2	ns ns
XTALIN Duty Cycle	(Note 8)	t_{pwh1}	40	-	60	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	-	5	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	-	5	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	5	11	15	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	5	11	15	ns
Reset Pulse Duration			200	-	-	ns

Notes: 6. Assumes Slave PLL is locked to 44.736 MHz signal.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Prescribed duty cycle is required only when XTALIN is driven by line-rate clock.
9. At max load of 1.6 mA and 25 pF. Guaranteed by design and characterization.

CS6300 STS-1 SWITCHING CHARACTERISTICS

(T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
RCLK Pulse Width	(Notes 7, 10)	t_{pwh} t_{pwl}	8.7 8.7	9.645 9.645	10.6 10.6	ns ns
XTALIN Duty Cycle	(Note 8)	t_{pwh1}/t_{pw}	40	-	60	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	-	5	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	-	5	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	5	9.5	14	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	5	9.5	14	ns
Reset Pulse Duration			200	-	-	ns

Notes: 10. Assumes Slave PLL is locked to 51.84 MHz signal.

CS6301 E3 SWITCHING CHARACTERISTICS

(T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
RCLK Pulse Width	(Notes 7, 11)	t_{pwh} t_{pwl}	13.1 13.1	14.548 14.548	16.0 16.0	ns ns
XTALIN Duty Cycle	(Note 8)	t_{pwh1}/t_{pw}	40	-	60	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	-	5	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	-	5	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	5	14.5	22	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	5	14.5	22	ns
Reset Pulse Duration			200	-	-	ns

Notes: 11. Assumes Slave PLL is locked to 34.368 MHz signal.

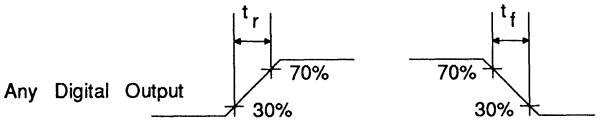


Figure 4. Signal Rise and Fall Characteristics

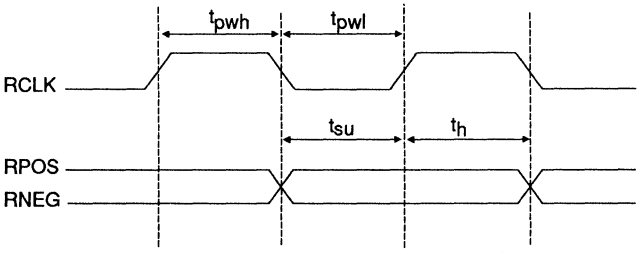


Figure 5. Recovered Clock and Data Switching Characteristics

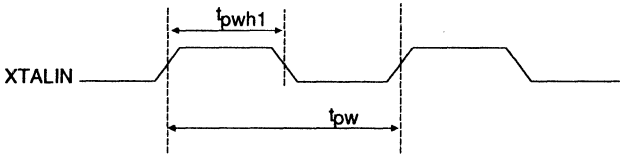


Figure 6. XTALIN Duty Cycle Requirements

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	V+	-0.3	6.0	V
Input Voltage, Any Pin	V_{in}	GND-0.3	(V+) + 0.3	V
Input Current, Any Pin (Note 12)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 12. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (referenced to GND)	V+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Crystal Frequency	F_C	3.43	3.5795	3.5831	MHz
Crystal Shunt Capacitance	C_O	-	3.5	-	pF
Crystal Load Capacitance	C_L	-	18.5	-	pF
Crystal Series Resistance	R_S	-	-	100	Ohms
External Resistor value (REF)	R_R	-	10	-	k Ohms
Supply Current	I_S	-	50	70	mA

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 13)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 13)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 14) I_{OUT}=-40 uA	V_{OH}	(V+) x 0.8	-	-	V
Low-Level Output Voltage (Note 14) I_{OUT}= 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Notes: 13. Pins XTALIN (when driven by logic signal), ALTSEL, GAIN1, GAIN2, LOOP, RATE1, RATE2, RESET
14. Pins LOS, RPOS, RNEG, RCLK

THEORY OF OPERATION

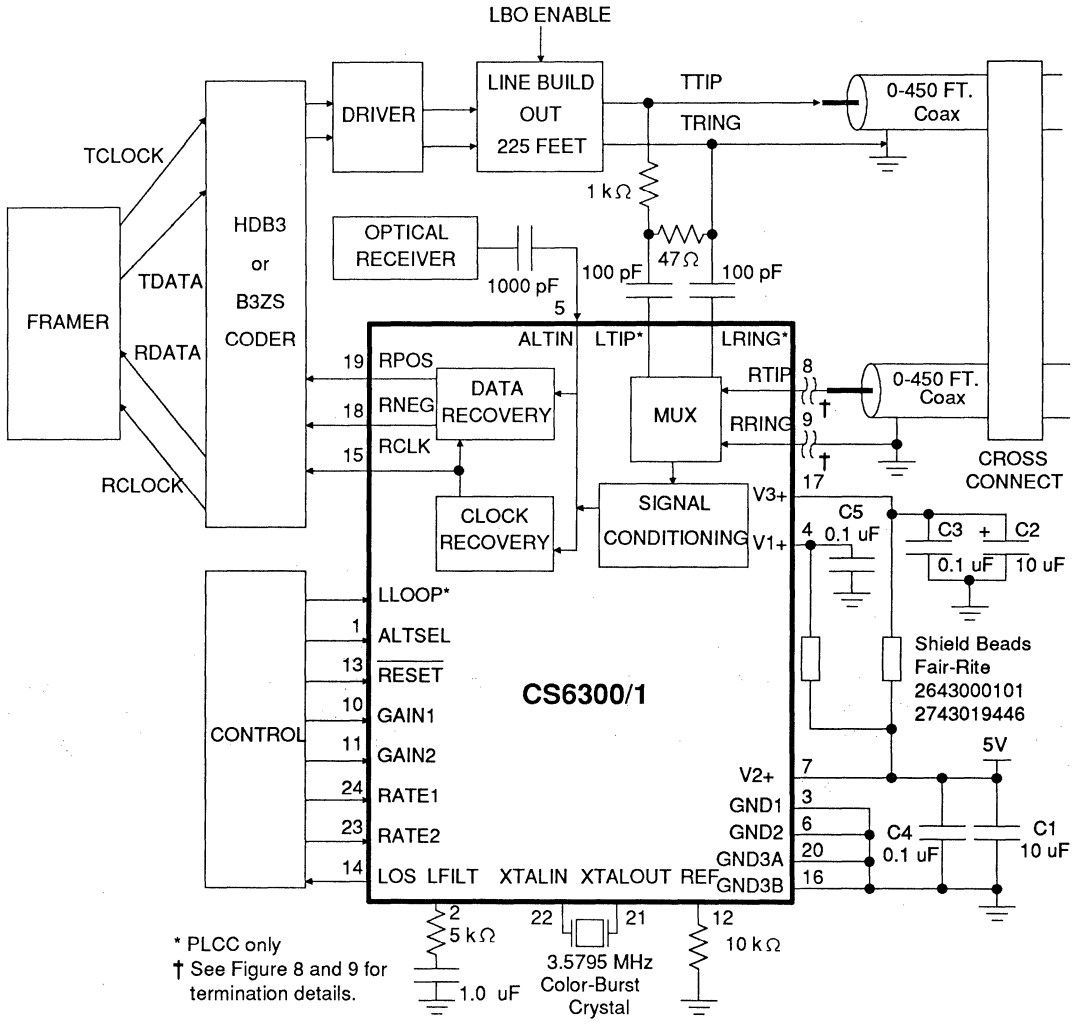


Figure 7. Basic Application circuit

The CS6300/1 provides the basic receiver functions of a high-speed line card as shown in Figure 7. The receiver extracts data and clock from a B3ZS or HDB3 coded signal and outputs clock and synchronized data. The CS6300/1 can be either transformer-coupled or capacitor-coupled to the cable as shown in Figures 8 and 9.

Noise-coupling must be minimized along the path from cable to RTIP/RRING. Any noise coupled into RTIP/RRING directly degrades the signal-to-noise ratio of the input signal.

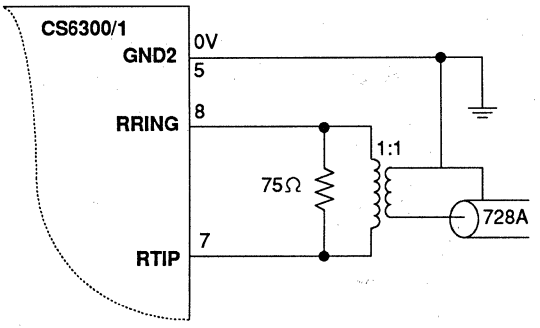


Figure 8. Transformer-Coupled Receiver

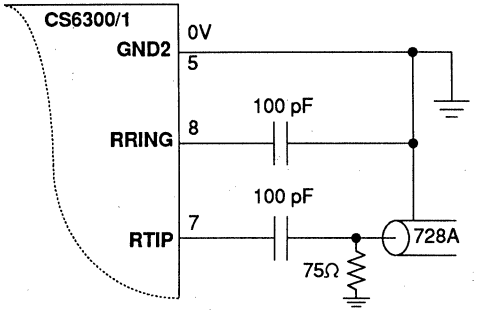


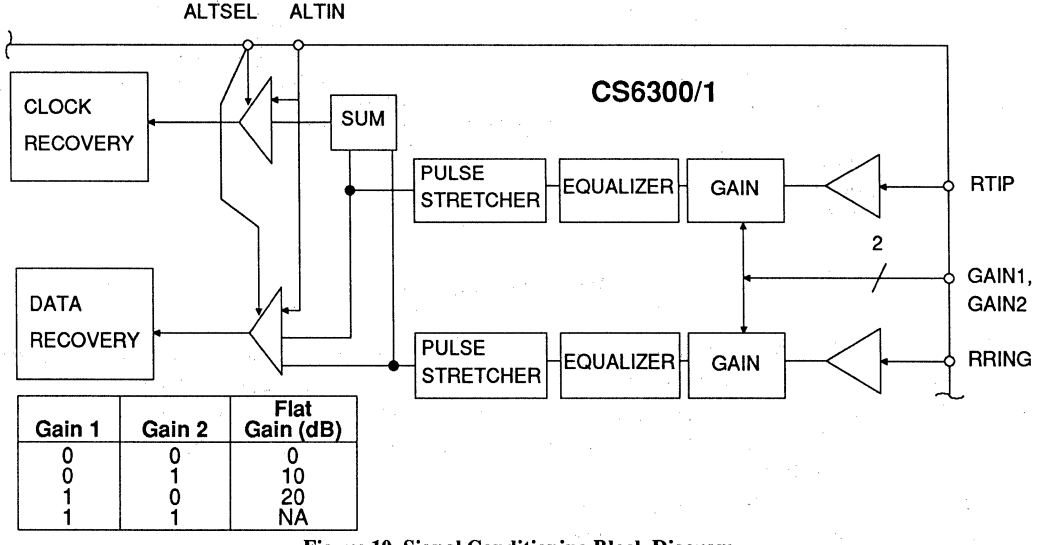
Figure 9. AC-Coupled Receiver

Signal Conditioning

The signal conditioning circuit is shown in Figure 10. In normal operation, the receiver is sensitive to signals down to approximately 170mV in amplitude. For monitor ports, 20 dB of flat gain can be selected (via the GAIN1 and GAIN2 pins). For systems using a resistive splitter (e.g., to support line protection switching), 10 dB of gain can be selected. Refer to the table in Figure 10.

The equalization is variable and is based upon the level of the incoming signal after the flat gain stage.

In the CS6300, the equalizer works as follows. When the peak of the amplified signal equals about 300mV, the equalizer compensates as appropriate for a nominal DSX-3/STS-1 pulse as



Gain 1	Gain 2	Flat Gain (dB)
0	0	0
0	1	10
1	0	20
1	1	NA

Figure 10. Signal Conditioning Block Diagram

attenuated by 450 feet of 728A cable. When the peak of the amplified signal equals about 600mV, the equalizer compensates as appropriate for a nominal DSX-3/STS-1 pulse. The equalizer adjusts continually as the signal strength varies between 180 and 850 mV.

In the CS6301, the equalizer works as follows. When the peak of the amplified signal equals about 250mV, the equalizer compensates as appropriate for a nominal G.703 pulse as attenuated by 12 dB of cable. When the peak of the amplified signal equals about 1000mV, the equalizer compensates as appropriate for a transmitted G.703 pulse. The equalizer adjusts continually as the signal strength varies between 250 and 1200 mV.

The pulse stretcher increases the jitter tolerance of the receiver by stretching the incoming pulse.

Clock Recovery

The receiver uses a Master/Slave Phase Lock Loop (PLL) to recover clock. The Master PLL has its center frequency set using one of four options discussed in the Master Clock Input Options section below. The same control voltage that is generated to center the frequency of the Master VCO is also used to center the frequency of the Slave VCO. This insures continuous frequency lock of the Slave PLL, and also insures immunity to false lock. The Slave VCO is phase locked to the received data stream.

If a valid input signal is assumed to be already present at RTIP/RRING, the maximum time between the application of device power and error-free operation is typically 20 ms. If power has already been applied and input data is then lost, the interval between the restoration of valid data and error-free operation is nominally 1.0 ms and typically no longer than 4 ms.

An external loop filter is used by the slave PLL, allowing the jitter tolerance and transfer function to be tailored for a variety of applications. The component values for the series resistor and capacitor are 5 kΩ and 1.0 µF respectively (two 0.47 µF capacitors may be used in lieu of the 1.0 µF capacitor). The components should be placed as close to the chip as possible. Noise coupling into the LFILT pin may degrade PLL performance. A low-leakage (e.g., ceramic) capacitor should be used.

Master Clock Input Options

An external reference clock is used to set the frequency of the Master PLL. The reference clock does not need to have exactly the same frequency as the line signal since the reference is used only to center the PLLs close to the desired rate. A delta frequency of 1-2 % between line signal and reference allows normal operation of the CS6300/1. Decreasing the delta will improve RCLK accuracy upon loss of signal. Four alternative reference clock options are provided:

RATE1=0; RATE2=0: Quartz crystal is attached to XTALIN/XTALOUT. In the CS6300, the crystal's frequency is multiplied by 12.5 to provide a reference clock for T3 applications. Using a color-burst crystal, the Master VCO will typically vary from 44.736 MHz by 173 ppm. Other crystals can be used to decrease the delta ppm. For example, using a 3.5752 MHz crystal will typically decrease the delta ppm to 50 ppm. In the CS6301, the crystal's frequency is multiplied by 10.

RATE1=1; RATE2=0: Quartz crystal is attached to XTALIN/XTALOUT. The crystal's frequency is multiplied by 14.5 to provide a reference clock for STS-1 applications. Using a color-burst crystal, the Master VCO will typically vary from 51.84 Mhz by 1,210 ppm. Other crystals can be used to decrease the delta ppm. For example, using a 3.5789 MHz crystal will typically decrease the delta ppm to 50 ppm.

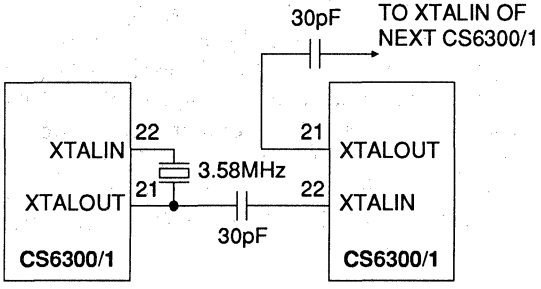


Figure 11 -Sharing One Quartz Crystal Among CS6300/1s

RATE1=0; RATE2=1: A line-rate clock (e.g. 34.386 MHz, 44.736 MHz or 51.84 MHz) should be input to XTALIN, and XTALOUT should be left floating.

RATE1=1; RATE2=1: A 34.386-div-8 MHz, 44.736-div-8 MHz or 51.84-div-8 MHz clock should be input to XTALIN, and XTALOUT should be left floating.

External Crystal Requirements

When used, a parallel-resonant crystal should be attached to pins XTALIN and XTALOUT. Crystal requirements are given in the Recommended Operating Conditions table. Figure 11 shows how to share crystals among multiple IC's. The equivalent circuit to ground on XTALOUT must be less than or equal to 15 pF.

Data Recovery

Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Loss of Signal

Receiver loss of signal is indicated upon receiving 128 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high.

When receiving signals from a coax cable, or during loopback, LOS operates as follows. As shown in Figure 12, if the incoming signal level (after the gain and equalization stages) falls below a threshold of typically 85 mV, the output clock of the master VCO is muxed directly into the slave VCO, replacing the received data as the signal source for the slave VCO. This replacement of the signal source improves the frequency accuracy of the slave VCO, since the slave VCO is normally trained to only within ±5% of the frequency of the master VCO. The signal source for the slave VCO reverts back to the received data signal when the incoming signal level (after the gain and equalization stages) rises to a threshold of typically 115 mV, LOS returns to logic zero upon detection of 33.3% ones density (based on 3 ones out of 9 bit periods).

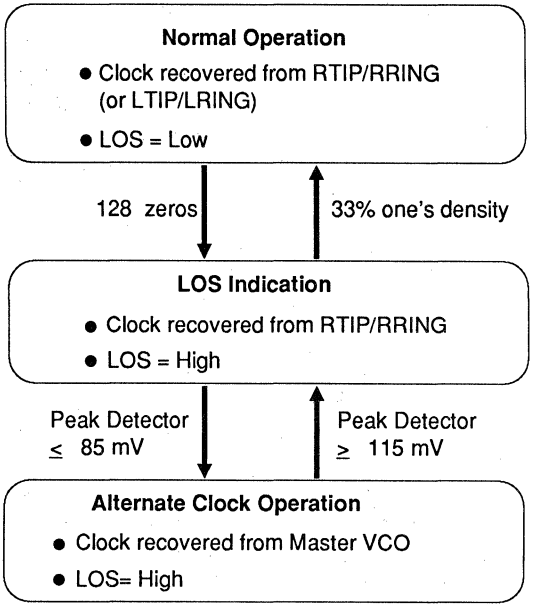


Figure 12 - Loss of Signal state diagram when ALTSEL is not active

When receiving signals on ALTIN, LOS operates as follows. As shown in Figure 13, if 128 zeros are detected, the output clock of the master VCO is muxed directly into the slave VCO, replacing the received data as the signal source for the slave VCO. This replacement of the signal source improves the frequency accuracy of the slave VCO, since the slave VCO is normally trained to only within ±5% of the frequency of the master VCO. The signal source for the slave VCO reverts back to the received data signal upon detection of 33.3% ones density (based on 3 ones out of 9 bit periods), and LOS returns to a logic zero.

Under all normal and LOS conditions, the slave VCO frequency is output on RCLK, and the recovered data is output on RPOS/RNEG. A Power-On reset or a manual reset sets LOS high.

Alternate Input

The signal conditioning circuit can be bypassed by setting ALTSEL high. When ALTSEL is high, an NRZ data signal can be input on pin ALTIN. An ECL signal (e.g., the output of an optical receiver module) can AC coupled into ALTIN. CMOS and TTL signals should be attenuated to a ~0.8V_{p-p} signal before being AC-coupled into ALTIN.

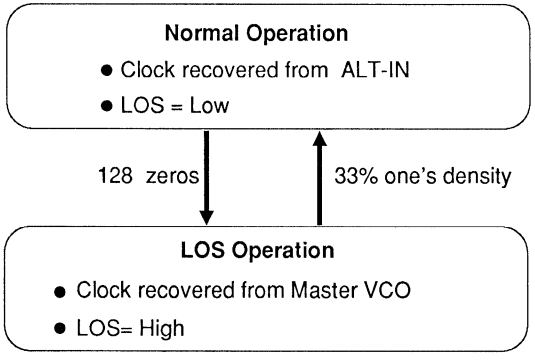


Figure 13 - Loss of Signal state diagram when ALTSEL is active

Power On Reset/Reset

Upon power-up, the CS6300/1 performs a reset. The CS6300/1 does not normally require a manual reset. For example, the PLLs are continuously calibrated through the Master/Slave architecture foregoing any requirement to recalibrate the receiver when in operation. However, a manual reset can be requested by setting $\overline{\text{RESET}}$ low for least 200 ns. The manual reset procedure is the same as the power-up reset procedure. Reset will initiate on the rising edge of $\overline{\text{RESET}}$.

Local Loopback (PLCC Package only)

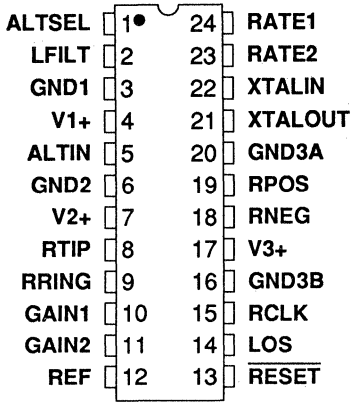
On the PLCC package, an additional set of receiver inputs (LTIP and LRING) are provided to support local loopbacks. The input pin LLOOP can be used to select between LTIP/LRING and RTIP/RRING. Figure 7 shows a recommended circuit for connecting transmitter outputs into the LTIP and LRING input ports. The series resistors decrease the signal by 20 dB, minimizing crosstalk effects during normal reception from RTIP/RRING. Because the signal is 20 dB down, the appropriate GAIN1/GAIN2 selection should be made during local loopback.

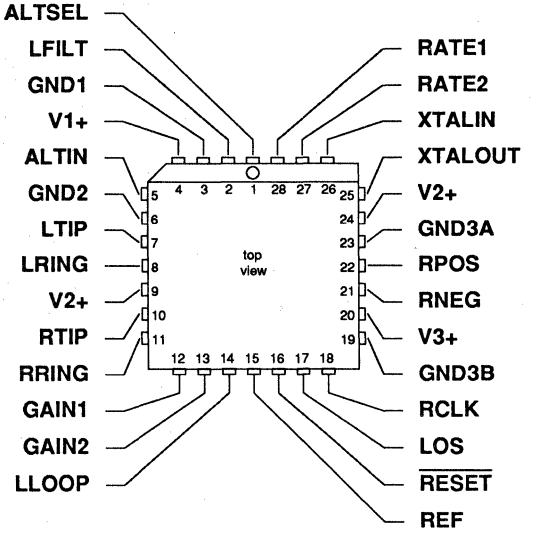
Power Supply

The device operates from a single 5 Volt supply. The V1+ and GND1 inputs power the master PLL. The V2+ and GND2 inputs power the slave PLL and other circuitry on the device. The V3+ and GND3 inputs power the digital I/O pins.

The recommended power supply decoupling circuit is illustrated in Figure 7. Good quality high-frequency, low lead-inductance capacitors should be used. All capacitors should be as close to the device as possible, and the connection between the shield beads and C2/C3/C5 should be as short as possible.

PIN DESCRIPTIONS





The CS6300 and CS6301 are available in a 24-pin skinny DIP, and in a 28-pin PLCC.

Power Supplies

V1+, V2+, V3+ - Positive Power Supply

Positive power supplies for the device; typically +5 volts.

GND 1, GND2, GND3A, GND3B - Ground

Power supply grounds for the device; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Input and Output

RATE1 and RATE2 define the functionality of these pins. When RATE2 is low a crystal is attached to XTALIN and XTALOUT. One crystal can be shared among multiple IC's as shown in Figure 11. When RATE2 is high, a clock signal is input to XTALIN and XTALOUT should be left floating.

Control

RATE1, RATE2 - Master PLL Rate Selection

Used to determine the source of the reference clock for the Master PLL. When RATE2 is low, a quartz crystal is attached to XTALIN/XTALOUT, and RATE1 determines the multiplier used with the crystal (multiply by 10 (CS6301) or 12.5 (CS6300) when RATE1 = high; multiply by 14.5 when RATE1 = low). When RATE2 is high, a clock signal is input into XTALIN and XTALOUT must be left floating, and RATE1 defines the input frequency. When RATE1 is low, a line rate clock should be input; when RATE1 is high, a clock of one-eighth the line rate should be input.

ALTSEL - Alternate Signal Selection

This digital input controls a multiplexor which selects NRZ input for the clock/data recovery circuit. High selects ALTIN; low selects RTIP/RRING.

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LLOOP - Local Loopback Selection (PLCC Only)

This digital input controls a multiplexor which selects local loopback input for the clock/data recovery circuit. High selects LTIP/LRING; low selects RTIP/RRING.

$\overline{\text{RESET}}$ - Circuit Reset

A manual reset is made by setting $\overline{\text{RESET}}$ low for least 200 ns. Reset will initiate on the rising edge of $\overline{\text{RESET}}$.

Inputs

RTIP, RRING - Receive Tip, Receive Ring

The B3ZS, or HDB3, receive signal is input to these pins. Refer to Figures 8 and 9. Data and clock are recovered and output on RPOS/RNEG and RCLK.

LTIP, LRING - Loopback Tip, Loopback Ring (PLCC Only)

A B3ZS, or HDB3, signal can be input to these pins. These signals are input to the receiver when LLOOP is held high.

ALTIN - Alternate Data Input

Allows NRZ format input data to be input into the clock and data recovery circuit, bypassing the RTIP/RRING receiver signal conditioning circuit. The ALTIN input is activated by setting ALTSEL high.

GAIN1, GAIN2 - Receiver Gain Control

Setting GAIN1 and GAIN2 low programs the receiver to accepts standard signals on RTIP and RRING inputs (0 dB of flat gain). Setting GAIN1 high and GAIN2 low programs the input buffer to provide 20 dB of flat gain. Setting GAIN1 low and GAIN2 high programs the input buffer to provide 10 dB of flat gain. Setting both GAIN1 and GAIN2 high is reserved.

REF - Reference Resistor Input

A 10 kΩ ±1%, 100 ppm/degree C resistor should be connected from REF to ground.

LFILT - Loop Filter Input

A 5 kΩ ±10% resistor and a 1.0 µF ±10% capacitor should be connected in series between LFILT and ground.

Status

LOS - Loss of Signal

LOS goes to a logic 1 when 128 consecutive zeros have been detected. LOS returns to a logic 0 when a 33.3% ones density signal returns (determined by receipt of 3 ones within 9 bit periods).

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data

Data and clock are recovered from the RTIP and RRING inputs and are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. RPOS and RNEG are stable and valid on the rising edge of RCLK. When an alternative data stream is input on ALTIN (selected by setting ALTSEL = high), the output data is on RPOS, and RNEG is low.

INTRODUCTION

Crystal offers two jitter attenuator circuits. The CS61600 PCM jitter attenuator uses a 16-bit FIFO and a variable oscillator to provide up to 40 dB of jitter reduction in a 1.544 to 2.048 MHz data stream. Also offered is the CS80600, a general purpose high speed (4.5 to 8.5 MHz) jitter attenuator. This part may be used in conjunction with the TMS380 device family to double the number of stations connected to 4 MHz IEEE 802.5 token ring local area network. The CS80600 slows the accumulation of data-dependent jitter, allowing more stations and repeaters to be inserted on the ring without overflowing the elastic buffer of the active system monitor. The input to the CS80600 is clock and data which have been recovered by the TMS38051/52. Jitter is removed by the CS80600 using an 8-Manchester symbol FIFO and a variable oscillator. The dejittered clock and data are then input to the TMS38020.

USER'S GUIDE

Device:	CS61600	CS80600
Data Rates	1.544 MHz or 2.048 MHz	4.5-8.5 MHz
Size of FIFO	16	8
Package	14 pin DIP	14 pin DIP

CONTENTS

Semiconductor Corporation

CS61600

PCM Jitter Attenuator

Features

- Unique Clock-Tracking Circuitry Filters 50 Hz or Higher Frequency Jitter for T1 and PCM-30 Applications
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS61600 from Crystal Semiconductor accepts T1 (1.544 Mb/s) or CCITT standard (2.048 Mb/s) data and clock inputs, and tolerates at least 7 (and up to 14) unit intervals, peak-to-peak, of jitter. Before outputting data and clock, jitter is attenuated using an internal clock-tracking variable oscillator and a 16 bit FIFO elastic store.

The jitter attenuation function can be determined by appropriate specification of the external crystal.

The CS61600 is transparent to data format, and is intended for application in carrier systems, switching systems, Local Area Network gateways and multiplexers.

ORDERING INFORMATION

CS61600-ID1 - 14 Pin CERDIP; T1 and 2.048 MHz
CS61600-IP1 - 14 Pin Plastic DIP; T1 and 2.048 MHz

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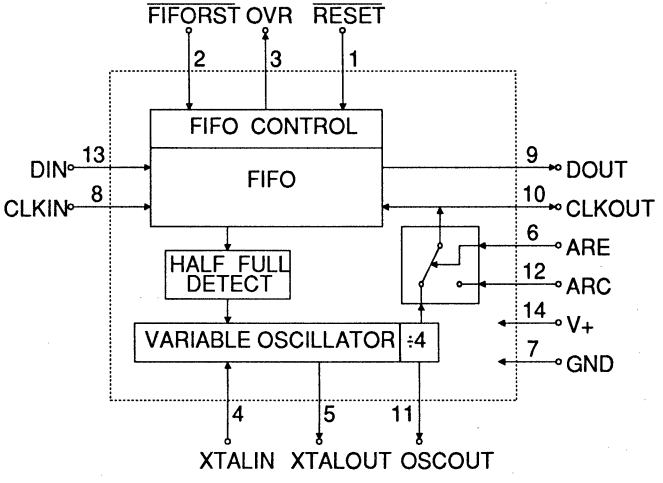
Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V+ - GND	- 0.3	7.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+ -GND	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	- 40	25	85	°C

DIGITAL CHARACTERISTICS (T_A = -40°C to 85°C; V+ = 5V ± 10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 2 & 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 2 & 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	± 10.0	uA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

ANALOG CHARACTERISTICS (T_A = -40°C to 85°C; V+ = 5V ± 10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Power Dissipation	P_D	-	50	85	mW
Input Jitter Tolerance		7	-	14*	Unit Intervals

* Depends on accuracy of crystal with respect to CLKIN frequency. See *Applications* section.

SWITCHING CHARACTERISTICS (T_A = -40°C to 85°C; V+ = 5V ± 10%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	T1	f_c	-	6.176000	-	MHz
	CCITT (Note 5)		-	8.192000	-	
CLKIN Frequency	T1	f_{in}	-	1.544	-	MHz
	CCITT (Note 6)		-	2.048	-	
CLKOUT Frequency	T1	f_{out}	-	1.544	-	MHz
	CCITT (Note 6)		-	2.048	-	
Clock Pulse Width	T1	t_{pwh}	-	324	-	ns
		t_{pwl}	-	324	-	
	CCITT (Note 7)	t_{pwh}	-	244	-	ns
		t_{pwl}	-	244	-	
Acceptable CLKIN range (Note 8)			-	±130	-	ppm
Duty Cycle (Note 9)			-	50	-	%
Rise Time, All Digital Outputs (Note 10)		t_r	-	36	100	ns
Fall Time, All Digital Outputs (Note 10)		t_f	-	17	100	ns
DIN to CLKIN Falling Setup Time		t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time		t_h	50	-	-	ns
CLKOUT Falling To DOUT Propagation Delay		t_{phl}	-	-	200	ns

Note:
5. Crystal should have sufficient pull range when in the oscillator circuit, to meet the system's frequency tolerance requirement over the operating temperature range. See *Applications* section for more information on crystals.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter) over time, CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Crystal must have at least ± 130ppm pull range over operating temperature range.
9. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
10. At C_L = 50pF.

5

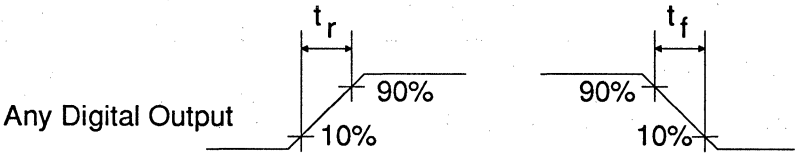


Figure 1. Signal Rise and Fall Characteristics

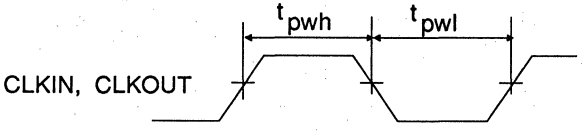


Figure 2. Clock Signal Quality

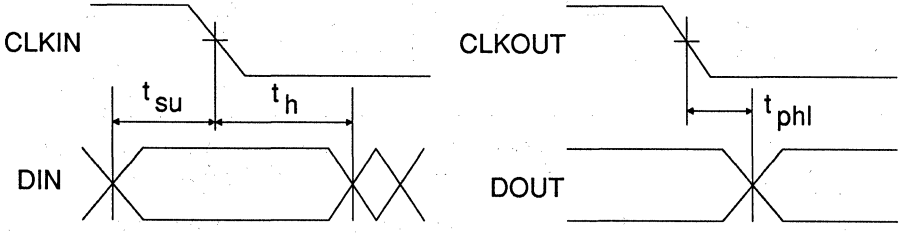


Figure 3. Switching Characteristics

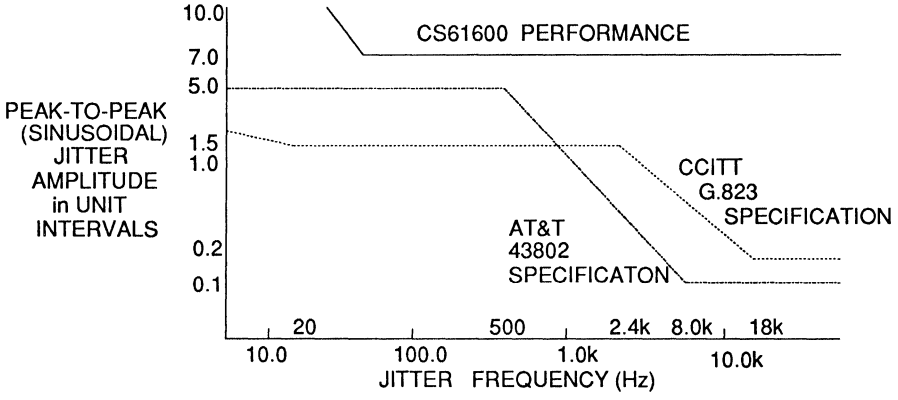


Figure 4. Input Jitter Tolerance

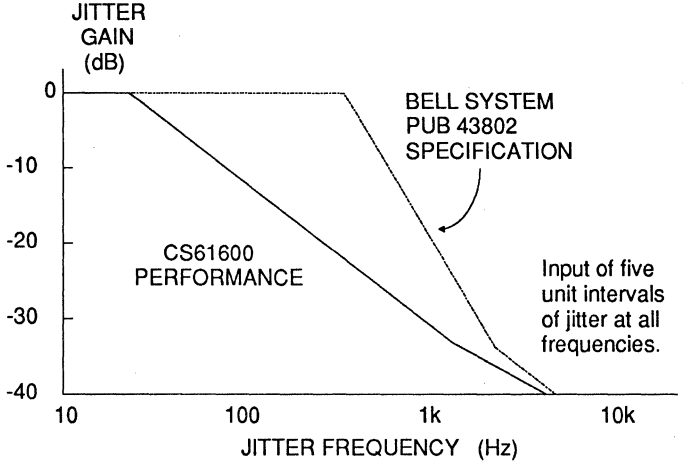


Figure 5. Jitter Attenuation Characteristic

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS61600 will tolerate and attenuate at least seven unit intervals of jitter from clock and data signals of 1.544 MHz and 2.048 MHz. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS61600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter receives little attenuation. This performance characteristic is shown graphically in Figure 6.

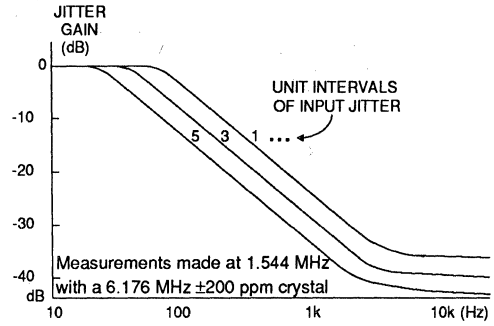


Figure 6. Jitter Attenuation Characteristics

Using the CS61600 in a Slave Configuration

It is possible to use an externally generated clock signal to clock data out of the CS61600. When an external clock is used, a crystal is not necessary. The external clock is input to the Alternate Read Clock input, ARC (pin 12). Holding the Alternate Read Enable pin, ARE (pin 6), high directs the CS61600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS61600 will be prone to underflow or overflow, and data will be lost. See the *Applications* section of this data sheet for more information on the use of an alternate clock.

Oscillator and Crystal

The CS61600 requires an external 6.176000 MHz (8.192000 MHz for CCITT) crystal be connected to pins XTALOUT and XTALIN. The oscillator circuit divides the crystal frequency by four, and switches various capacitive loads to provide a clock that swings in five steps from at least 1.544 MHz - 130 ppm to at least

1.544 MHz + 130 ppm (2.048 MHz - 50 ppm to 2.048 MHz + 50 ppm for CCITT). The crystal oscillator must be able to reach these signal frequency tolerances over the system's operating temperature range. The oscillator adjusts to and holds the average frequency of the signal input to CLKIN.

Some applications specify a narrower frequency tolerance. In these cases, it is possible to improve jitter attenuation performance by specifying a crystal with less pull range. A narrow pull range crystal has the effect of shifting the curves shown in Figure 6 to the left. Care must be taken to ensure that the crystal/oscillator will reach the signal's frequency extremes over the operating temperature range of the system. More information on specifying and testing crystals is provided in the *Applications* section at the back of this data sheet.

FIFO Overflow/Underflow

Because the oscillator clock, which is used to empty the FIFO, has a wider frequency range than the standard T1 input signal, the FIFO should never underflow or overflow. However, if underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an overflow occurs, the 16 bits of data in the FIFO are lost. An underflow condition causes the next 16 bits read from the FIFO to be invalid. In either case, the CS61600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the overflow flag, OVR.

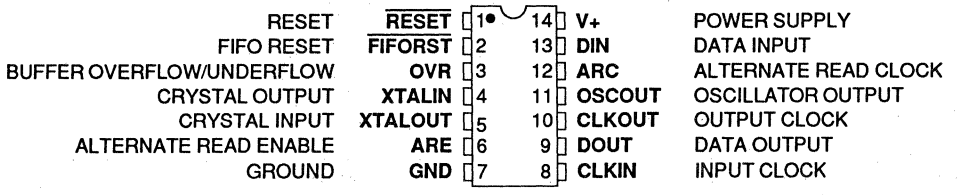
FIFO Reset

Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS61600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. ***However, the outputs of the CS61600 are undefined if $\overline{\text{FIFORST}}$ is held low for more than 500 ms.*** The FIFO reset function will set the FIFO write and read pointers to the first and eighth locations respectively. The oscillator will continue to run and CLKOUT will be held low.

Power-Up Reset

Upon power up, the CS61600 goes through an initialization procedure which requires approximately 3 ms. During this initialization procedure, OVR is held high. After initialization is complete, OVR goes low. When the clock signal is input to CLKIN, the CS61600 will immediately try to lock onto the clock signal on CLKIN. At this point, the FIFO may overflow, and the $\overline{\text{RESET}}$ pin should be toggled to clear the overflow/underflow flag, OVR.

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, PIN 14.

Typically +5V volts.

GND - Ground, PIN 7.

Ground reference.

Oscillator

XTALIN, XTALOUT - Crystal Input 1, 2; PINS 4, 5.

6.176 MHz or 8.192 MHz crystal inputs. A 200 kohm resistor should be connected across these pins. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.

When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.

Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss. When $\overline{\text{FIFORST}}$ is low, the OSCOUT output is disabled.

ARE - Alternate Read Enable, PIN 6.

For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.

Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.

Input data is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.

When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.

Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.

Output data with jitter attenuated. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.

Jitter reduced clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.

Output of on-chip oscillator, divided by four. This pin should be left floating for normal operation.

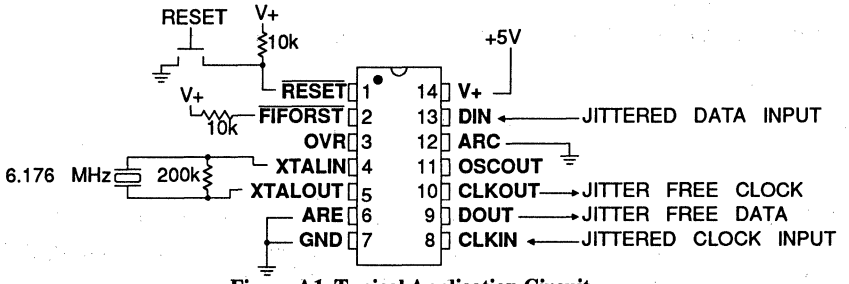


Figure A1. Typical Application Circuit

APPLICATIONS

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61600. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for PCM-30 applications.

General Applications

The CS61600 will tolerate and attenuate at least seven unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS61600 will tolerate more jitter; up to 14 unit intervals will be tolerated under optimal conditions.

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 1.544 MHz - 130 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 1.544 MHz + 130 ppm.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS61600. If the center frequency of the oscillator is precisely four times the CLKIN frequency, and the crystal has at least the specified pull range, the CS61600 will tolerate 14 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some T1 applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS61600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A2 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS61600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer.

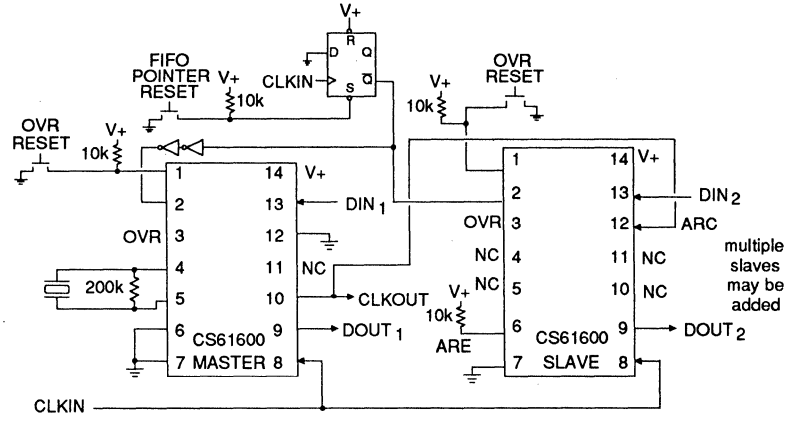


Figure A2. Master / Slave configuration

For this configuration to function properly, the positions of the FIFO read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied together. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS61600 to drive the subsequent CS61600 will induce some propagation delay. These potential timing problems should be considered when cascading CS61600s.

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T1 signal clock) goes away. Figure A3 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

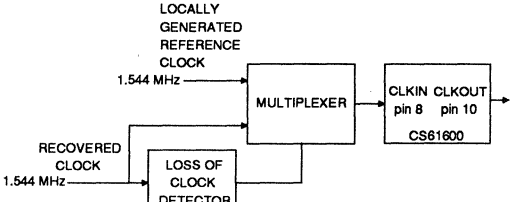


Figure A3. Maintaining Clock Integrity

Jitter Attenuation at Different Clock Rates

The CS61600 can be used to attenuate jitter at frequencies below 2.048 MHz. For signal frequencies above about 900 kHz, selection of the appropriate crystal will suffice. For jitter attenuation of lower frequency signals, an external divider is required. Figure A4 shows how the CS61600 can be configured for low frequency jitter attenuation.

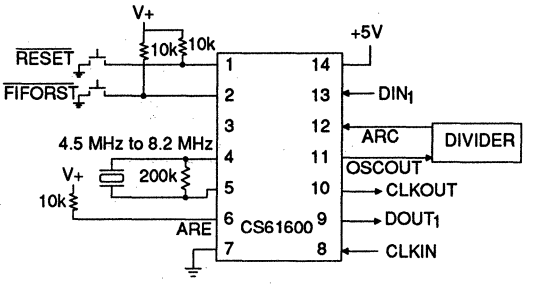


Figure A4. Low Clock Frequency Jitter Attenuation

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 32, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

Semiconductor Corporation

CS80600

High Speed Jitter Attenuator

Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs and removes up to ±3 data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

Applications

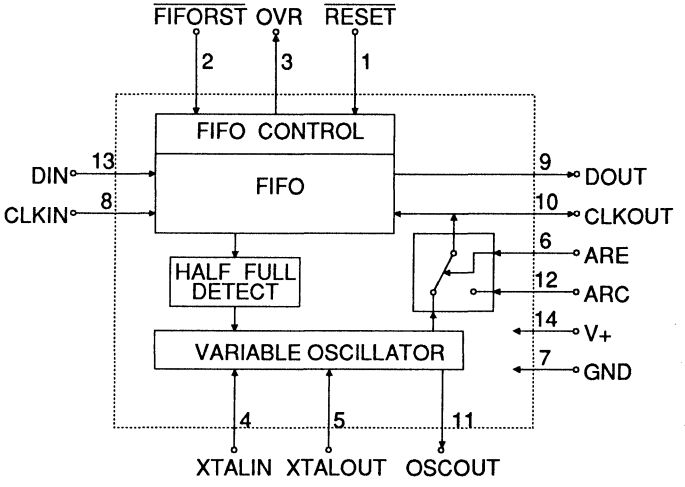
- **Token Ring:** The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adaptor cards, in active wiring concentrators, and in repeators.
- **PCM:** TIC, T2, and CEPT2 and second order multiplexors.

ORDERING INFORMATION

CS80600-P - 14 Pin Plastic DIP

5

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V+ - GND	-	7.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-	100	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	125	°C

Note: 1. Device can tolerate transients of up to 100mA without latching up.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	0	25	70	°C
Power Dissipation	P_D	20	50	85	mW
Input Jitter Tolerance	-	3	-	7	Unit Intervals

DIGITAL CHARACTERISTICS (T_A = 0°C to 70°C; V+ = 5V ± 10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 2 & 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 2 & 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10.0	uA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C; V+ = 5V ± 10%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 5)	f_c	4.500	-	8.500	MHz
CLKIN Frequency	(Note 6)	f_{in}	-	f_c	-	MHz
CLKOUT Frequency	(Note 6)	f_{out}	-	f_c	-	MHz
Clock Pulse Width		t_{pwl}	-	$1/(2f_c)$	-	ns
	(Note 7)	t_{pwl}	-	$1/(2f_c)$	-	ns
Duty Cycle	(Note 8)	-	-	50	-	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	36	-	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	17	-	ns
DIN to CLKIN Falling Setup Time		t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time		t_h	50	-	-	ns
CLKOUT Falling To DOUT Propagation Delay		t_{phl}	-	-	60	ns
$\overline{\text{RESET}}$ Pulse Width		-	100	-	-	ns
$\overline{\text{FIFORST}}$ Pulse Width		-	100	-	-	ns

Note:
5. Crystal must meet specifications described in *Applications* Section of this data sheet.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter), over time CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
9. At maximum load of 1.6mA and 50pF.

5

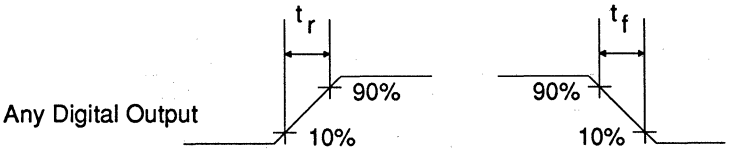


Figure 1. Signal Rise and Fall Characteristics

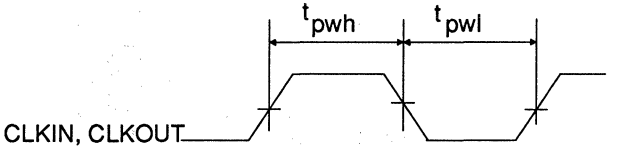


Figure 2. Clock Signal Quality

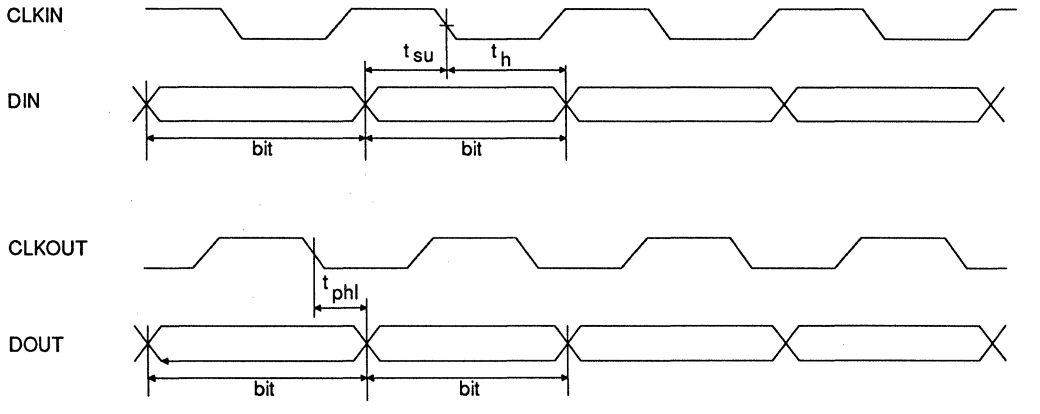


Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS80600 will tolerate and attenuate at least three unit intervals of jitter from a 4.5MHz to 8.5MHz data and clock signal. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS80600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter recieves little attenuation. This performance characteristic is shown graphically in Figure 4.

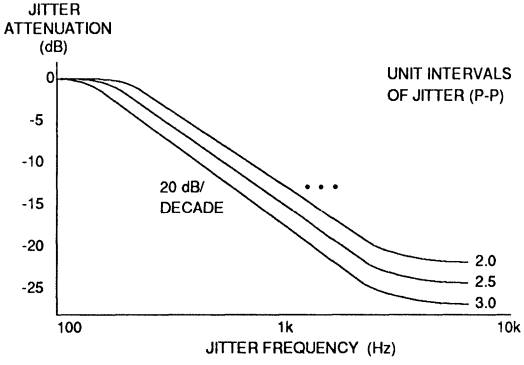


Figure 4 - Jitter Attenuation Characteristics for 8MHz Nominal Frequency

Clock Operation

The CS80600 requires an external crystal. Exacting crystal specifications must be met to ensure proper operation of the curcuit. Information on specifying crystals for the CS80600 is provided in the *Applications* section which appends this data sheet.

It is possible to use an externally generated clock signal to clock data out of the CS80600. The external clock is input to the Alternate Read Clock input, (ARC, pin 12). Holding the Alternate Read Enable pin high (ARE, pin 6), directs the CS80600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS80600 will be prone to underflow or overflow and data will be lost.

5

FIFO Overflow/Underflow

If underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an overflow occurs, the eight bits of data in the FIFO are lost. An underflow condition causes the next eight bits read from the FIFO to be invalid. In either case, the CS80600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the OVR flag.

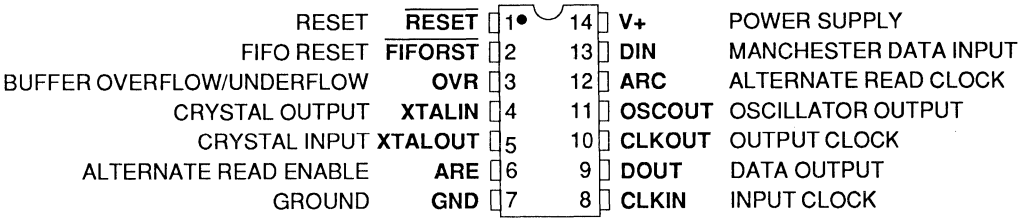
FIFO Reset

Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS80600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. ***However, the outputs of the CS80600 are undefined if $\overline{\text{FIFORST}}$ is held low for more than 500 ms.*** The FIFO reset function will set the FIFO write and read pointers to the first and fourth locations respectively. The oscillator will continue to run and CLKOUT will continue to be output.

Power-Up Reset

Upon power up, the CS80600 goes through an initialization procedure which requires approximately 3 ms. During power-up reset, the overflow pin, OVR, is held high. When initialization is complete, the OVR pin goes low and the CS80600 is ready to lock on to an input clock signal on CLKIN.

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, PIN 14.
Typically +5V volts.

GND - Ground, PIN 7.
Ground reference.

Oscillator

XTALIN; XTALOUT - Crystal Input; Crystal Output; PINS 4, 5.
A 20 kΩ resistor should be connected across these pins parallel with the crystal. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.
When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.
Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss.

ARE - Alternate Read Enable, PIN 6.
For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.
Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.
Data input is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.
When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.
Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.
Data output with jitter removed. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.
Jitter free clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.
Output of the crystal oscillator.

APPLICATIONS

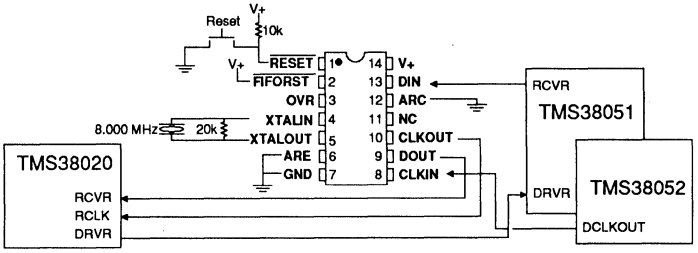


Figure A1. Basic LAN Application suggested for TMS380 Chip Set

Token Ring Operation

The CS80600 can be used, as shown in Figure A1 with the TMS380 Token Ring adaptor chip-set in station adaptors, active wiring concentrators and/or repeaters to attenuate jitter that accumulates in a ring. Figure A1 has the effect of masking frequency deviations from the TMS38020 and preventing the "Hardware Error Process" from triggering. In this case, error recovery occurs as the result of higher level procedures.

Figure A2 allows the "Hardware Error Process" to occur. When the CS80600 overflows or underflows, a MUX is used to pass the out-of-frequency clock data around the CS80600 for a fixed number of bits. After those number of bits are passed, the CS80600 is switched back into the circuit. This allows the TMS38020 to observe a wide frequency variation.

Figure A3 shows how the CS80600 can be used to generate a FRAQ signal, thereby allowing the TMS38051/52 PLL to be controlled in a repeater without the use of the TMS38020.

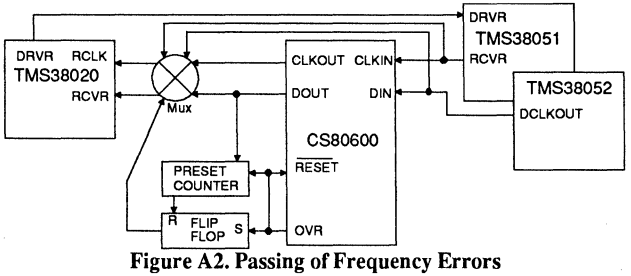


Figure A2. Passing of Frequency Errors

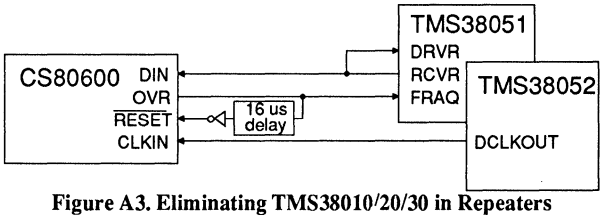


Figure A3. Eliminating TMS38010/20/30 in Repeaters

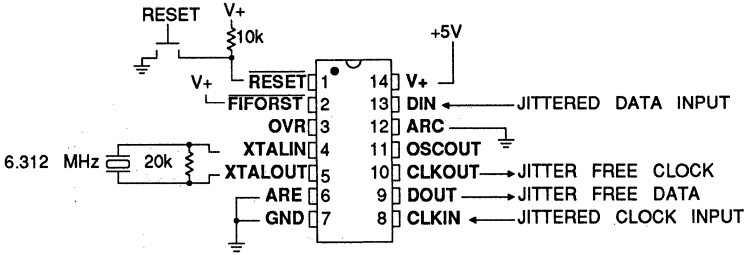


Figure A4. Typical Jitter Attenuation Curcuit

T2 Operation

The CS80600 may be connected as shown in Figure A4 for jitter attenuation in T2 applications.

Selecting an Oscillator Crystal

Figure A5 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS80600. The value of this capacitor is controlled by logic internal to the CS80600. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

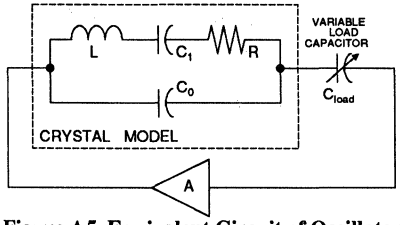


Figure A5. Equivalent Circuit of Oscillator

The important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the value of C_o and C_1. C_1 can be used to control the series resonant frequency of the crystal. The minimum values of C_{load} and C_o set the parallel resonant frequency. Together, C_1, C_o and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application.
2) The frequency drift of the crystal over the operating temperature range.
3) The variability in load capacitance from IC to IC.
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_1. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_1 (greater series resonant frequency) results in less pull range, while the larger the C_1 (lower series resonant frequency), the larger the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L-C_H)}(C_L+C_H+2C_0) \quad \text{(C's in pF)} \quad (1)$$

f_S = series resonant frequency of crystal
f_N = Nominal Signal Frequency
- should be 8.000000 MHz for LAN
- should be 6.312000 MHz for T2
- should be 8.448000 MHz for CEPT2

Δf = required pull range of crystal in Hz (Δppm x f_N)
C_L = load capacitance for low frequency oscillation (average is ~44.0 pF)
C_H = load capacitance for high frequency oscillation (average is ~9.5 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1+C_{load}+C_0}{C_{load}+C_0}\right)^{1/2} \quad (2)$$

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_0 and C_1 can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

The setup shown in Figure A6 can be used to test crystals. When no CLKIN signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

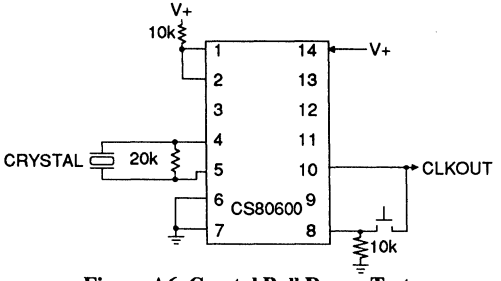


Figure A6. Crystal Pull Range Test

General Applications

The CS80600 will tolerate and attenuate at least three unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS80600 will tolerate more jitter; up to seven unit intervals will be tolerated under optimal conditions.

NOMINAL INPUT SIGNAL FREQUENCY 8.000000 MHz				CRYSTAL FREQUENCY FOR CORRESPONDING LOAD CAPACITANCE
C_L in pf	FREQUENCY TOLERANCE OF INPUT SIGNAL ±100 ppm			
$C_{low\ freq}$ min 41.0	-170 ppm 7998640	$C_{high\ freq}$ max 10.7	+170 ppm 8001360	
ASSUMING ±50 ppm TEMPERATURE DRIFT FROM 0°- 70° C				
MAXIMUM ALLOWABLE PULL RANGE: 400 ppm				

Table A1. LAN Crystal Requirements

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 8.000 MHz - 100 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 8.000 MHz + 100 ppm. In either case, the CS80600 will tolerate at least 3 unit intervals of jitter.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS80600. If the center frequency of the oscillator is precisely the CLKIN frequency, and the crystal has at least the specified pull range, the CS80600 will tolerate 7 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS80600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A7 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS80600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer. For this configuration to function properly, the positions of the FIFO the read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied together. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

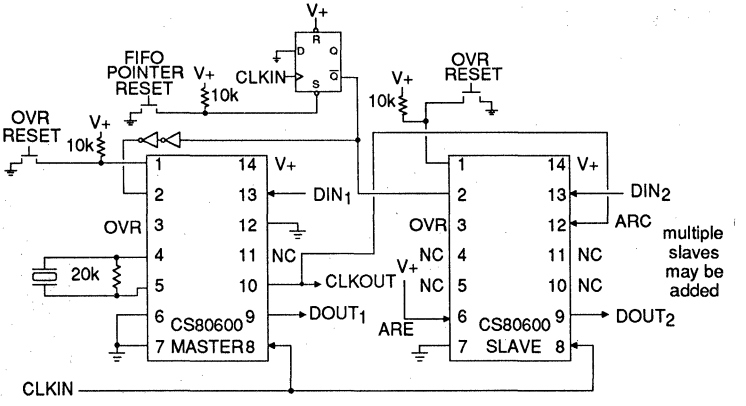


Figure A7. Master/Slave Configuration

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS80600 to drive the subsequent CS80600 will induce some propagation delay. These potential timing problems should be considered when cascading CS80600s.

Creating Phase Coherent Clocks From Two Clock/Data Streams

The master/slave configuration can be used to align two independent clock/data streams as long as the clocks of both signals are at exactly the same average frequency. The schematic shown in Figure A7 is used to implement this application, but CLKIN signals are independent, not tied together. This application will attenuate jitter as long as the jitter input to either device plus the difference in unit intervals between the clock signals does not exceed seven unit intervals. Note that more jitter can be tolerated if the guidelines described at the beginning of this section are followed.

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T2 or CEPT2 signal clock) goes away. Figure A8 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

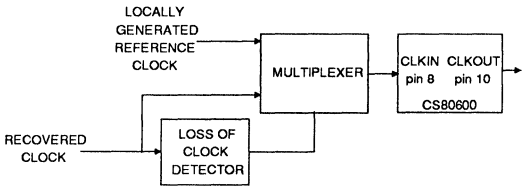


Figure A8. Maintaining Clock Integrity

Jitter Attenuation at Different Clock Rates

The CS80600 can be used to attenuate jitter at frequencies below 4.5 MHz. For signal frequencies above about 4.5 MHz, selection of the appropriate crystal will suffice. For jitter attenuation of lower frequency signals, an external divider is required. Figure A9 shows how the CS80600 can be configured for low frequency jitter attenuation.

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 128, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

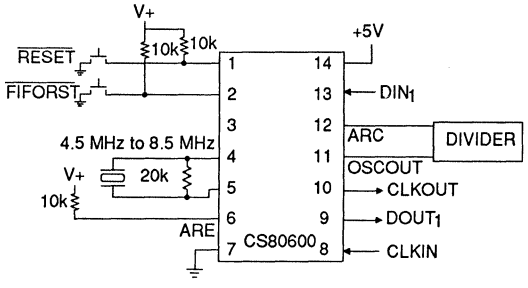


Figure A9. Low Frequency Jitter Attenuation

• Notes •

INTRODUCTION

Crystal's industry-standard DTMF receivers, CS8870, CS202, CS203 and CS204 exhibit performance which exceeds that of competitive devices. The Crystal CS202/3/4 family requires half the power of industry alternatives, provides 22 dB more dial-tone rejection and has better latch-up immunity than products available from other vendors. The receivers incorporate filters to guarantee the best possible signal-to-noise ratio. This allows highly accurate decoding of telephone tones into digital outputs.

USER'S GUIDE

Device:	CS202/3 DTMF Receiver	CS204 DTMF Receiver	CS8870 DTMF Receiver
Package Size (# pins)	18	14	18
Signal Sensitivity	-32 dBm	-32 dBm	-29 dBm
Dial Tone Tolerance	22 dB	22 dB	22 dB
Acceptable Twist	10 dB	10 dB	10 dB
Typical Power Consumption	6 mA	6 mA	6 mA
Tone Pairs Detected	12 or 16	16	16
Output Format	Hex/Binary	Hex	Hex
Package	18 pin DIP	14 pin DIP	18 pin DIP

CONTENTS

Semiconductor Corporation

CS202/3

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Detects 12 or 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex or Binary 2-of-8 Output
- Synchronous or Handshake Controlled Output
- Built-in Filter for Dial Tone Rejection
- 18 Pin Package
- Single 5 Volt ±10% Power Supply
- Early Detect Output
- Pin Compatible with SSI 202/SSI 203

General Description

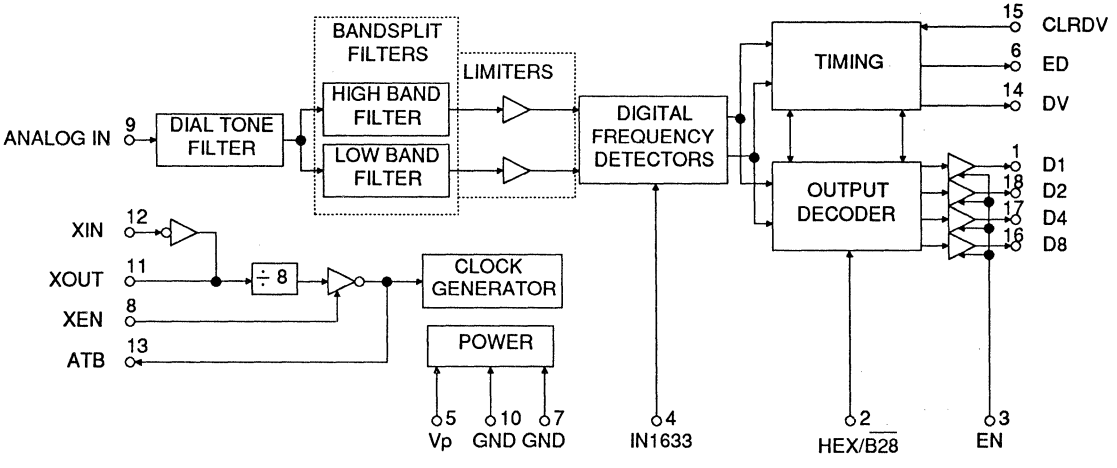
The CS202 and CS203 are fully integrated DTMF (Dual Tone Multifrequency) receivers that decode the tone pairs used in standard dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

ORDERING INFORMATION

CS202-P - 18 Pin Plastic DIP
CS203-P - 18 Pin Plastic DIP
All standard 300 mil DIPs

6

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	Vp - GND	-	7.0	V
Input Voltage, Any Pin Except Analog in	V_{in}	- 0.5	Vp + 0.5	V
Input Voltage, Analog In	V_{in}	Vp - 10	Vp + 0.5	V
Input Current, Any Pin (Note 1)	I_{in}	-	±10.0	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_P	4.5	5.0	5.5	V
Crystal Frequency	F_C	3.5759	3.5795	3.5831	MHz
Ambient Operating Temperature	T_A	0	25	70	°C

DIGITAL CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7Vp	-	Vp	Volts
Low-Level Input Voltage	V_{IL}	0	-	0.3Vp	Volts
High-Level Output Voltage 200 uA Load (Note 2)	V_{OH}	Vp - 0.5	-	Vp	Volts
Low-Level Output Voltage 400 uA Load (Note 2)	V_{OL}	0	-	0.5	Volts

Note: 2. Does not include XOUT.

Specifications subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current (Note 3)	I_p	-	6.0	12	mA
Frequency Detect Bandwidth	BW	± (1.5+2Hz)	±2.3	± 3.5	% of f_o
Detection Amplitude (Note 4)	-	- 32	-	- 2	dBm
Twist (Note 5)	-	-	±10	-	dB
60 Hz Tolerance	-	-	0.8	-	V_{rms}
Dial Tone Tolerance (Note 6, 10)	-	-	22	-	dB
Talk Off (Note 7)	-	-	2	-	hits
Power Supply Noise (Note 8)	-	-	10	-	mV_{p-p}
Noise Tolerance (Note 7, 10)	-	-	- 12	-	dB
Input Impedance at ANALOG IN (Note 9)	Z_{in}	100//15	-	-	kohm// pF

Notes:
3. T_A = 25°C
4. Each tone. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
5. Twist = high tone/low tone.
6. Precise dial tone frequencies of 350Hz ± 2% and 440Hz ± 2%.
7. MITEL tape #CM 7290
8. Bandwidth limited (3kHz) Gaussian noise.
9. V_{in} = (V_p - 10V) to V_p
10. Referenced to lower amplitude tone

6

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter		Symbol	Min	Typ	Max	Units
Tone Time:	for detect	t_{on}	40	-	-	ms
	for reject	t_{on}	-	-	20	ms
Pause Time:	for detect	t_{off}	40	-	-	ms
	for reject	t_{off}	-	-	20	ms
Detect Time		t_d	25	-	46	ms
Release Time		t_r	25	-	50	ms
Data Setup Time		t_{su}	7	-	-	us
Data Hold Time		t_h	7	9	10	us
DV Clear Time		t_{cl}	-	160	250	ns
CLRDV Pulse Width		t_{pw}	200	-	-	ns
ED Detect Time		t_{ed}	5	-	22	ms
ED Release Time		t_{er}	0.5	-	18	ms
Output Enable Time (Note 11) C_L = 50 pF, R_L = 1 kohm		t_{en}	-	200	300	ns
Output Disable Time (Note 11) C_L = 35 pF, R_L = 500 ohms		t_{dis}	-	150	200	ns
Output Rise Time (Note 11) C_L = 50 pF		t_{rise}	-	200	300	ns
Output Fall Time (Note 11) C_L = 50 pF		t_{fall}	-	160	250	ns

Note: 11. R_L and C_L are parallel impedances.

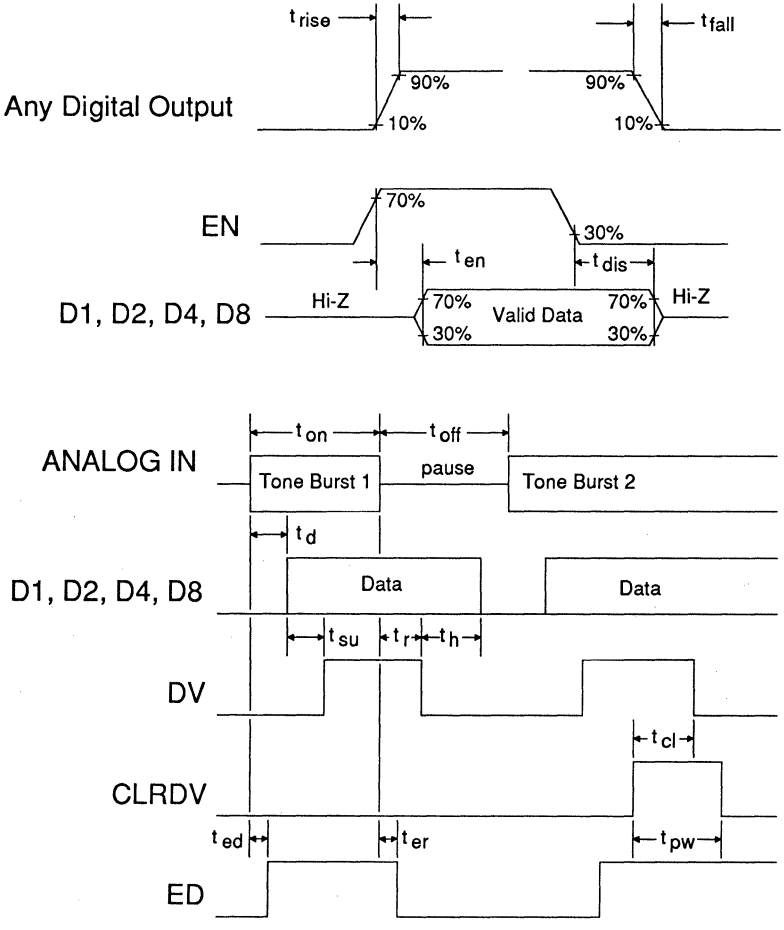


Figure 1 - Timing Diagram

GENERAL DESCRIPTION

The CS202 and CS203 are complete Dual Tone Multifrequency (DTMF) Receivers designed to detect 12 or 16 digits in either a 2-of-7 or 2-of-8 tone selection scheme. These devices provide all of the necessary filtering and require only an external 3.5795 MHz colorburst crystal and a resistor to provide a reference clock. Both devices are designed using a high-density, low-power CMOS technology, and provide the best performance at the lowest cost.

The CS202 and CS203 have filtering on board to guarantee the best signal-to-noise performance possible. The DTMF signal is passed through a dial tone reject filter to reduce dial tone interference, and is then separated into low and high groups using two bandsplit filters. The output of each bandsplit filter contains frequency components from only one DTMF tone group.

Table 1 - DTMF Dialing Matrix

Low-Band	High-Band			
	Column 1 1209 Hz	Column 2 1336 Hz	Column 3 1477 Hz	Column 4 1633 Hz
Row 1 697 Hz	1	2	3	A
Row 2 770 Hz	4	5	6	B
Row 3 852 Hz	7	8	9	C
Row 4 941 Hz	*	0	#	D

For a valid DTMF signal to be detected, each group must simultaneously contain only one valid DTMF tone. Detection of the two tones is accomplished with a digital algorithm. The sinusoidal filter output waveforms pass through a pair of hard limiters. The decoder takes the resultant square waves and measures their periods. This period measurement varies with jitter created by any extraneous signals within the signal passed to the limiter. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the three or four expected tones. If both bands have a valid tone decoded, the ED signal (CS203 only) will go high.

After two valid tones have been recognized by the decoder, the tones are subjected to a detect timing cycle. The two tones must remain valid for 20 to 40 ms for DV to go high, indicating that a valid digit has been decoded. This prevents voices or other in-band noise from creating a false trigger.

After a valid digit is indicated, the timing circuit will then enable a timing chain that detects drop-outs. If a signal drop of less than 20 ms duration occurs, it will be ignored. This timing prevents false triggering due to keybounce or other signal interruptions. Any drop-out in excess of 40 ms is considered a valid release; the receiver is reset (DV goes low), and all decoded outputs are cleared for the next decode.

Interfacing to the CS202 and CS203

The CS202 and CS203 have analog, data and control interfaces. The analog interface determines how an analog voice channel is connected. The data interface controls the method of extracting output data. The control interface determines what signals are detected and how they are presented to the data interface.

The analog interface consists of only one signal: ANALOG IN. The ANALOG IN signal can be either DC-coupled or AC-coupled using a 0.01µF capacitor. Care must be taken not to exceed the voltage requirements of the pin. It is also desirable to add a simple RC lowpass filter to bandlimit the input to the voice band (100 Hz to 3.4 kHz) so that high frequency noise near the 55.9 kHz internal sampling frequency is not aliased into the voice band by the internal switched-capacitor filters.

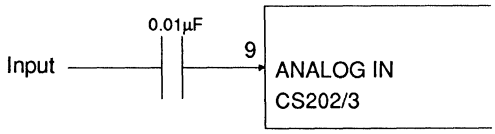


Figure 2 - AC - Coupled Input

The data interface is structured as either a strobed (synchronous) or handshake output. In the strobe mode, CLRDV is held low and DV is used as a data clock to strobe valid information from the data pins (D1, D2, D4, D8). The handshake mode is useful in an edge-triggered environment. The DV pin is used to generate an interrupt which forces the system to read information from the data pins. The interrupt (DV), is then cleared by taking CLRDV high momentarily. When there is a need to interface the receivers to a bus, the CS202 and CS203 can be three-state controlled by the EN pin. The EN pin must be held high to take the devices out of the high impedance state and into a data output mode. Conversely, taking EN low will force the devices into high impedance states and prevent bus conflicts.

Table 2 - Digital Encoding of DTMF Signal

Digit	Hexadecimal				Binary 2-of-8			
	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

The control interface is represented by the HEX/$\overline{B28}$ pin and the IN1633 pin. Both of these pins control the output data. The HEX/$\overline{B28}$ pin will place the output in a hex format when tied high, and will put it into a binary coded 2-of-8 output format when held low. The IN1633 pin is used to select either the 12 digit or the 16 digit format. When this pin is high, the devices will consider any tone pairs containing the 1633Hz signal (digits A, B, C and D) as invalid signals. When this pin is low, all tones are decoded.

Clock Generation

The CS202 and CS203 provide two separate means of clock generation, internal and external. With internal clock generation, a 3.5795 MHz crystal is tied between XIN and XOUT, a 1MΩ resistor is tied in parallel with the crystal to guarantee oscillation, and the XEN signal is tied high enabling the crystal oscillator. In this mode, the ATB pin is a 447.443 kHz clock output which can be used to drive up to 10 other CS202 and CS203 devices that are in the external clock mode.

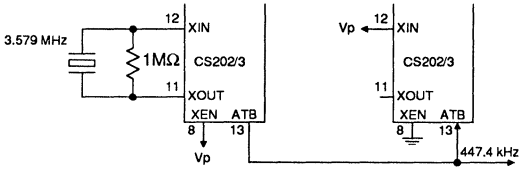
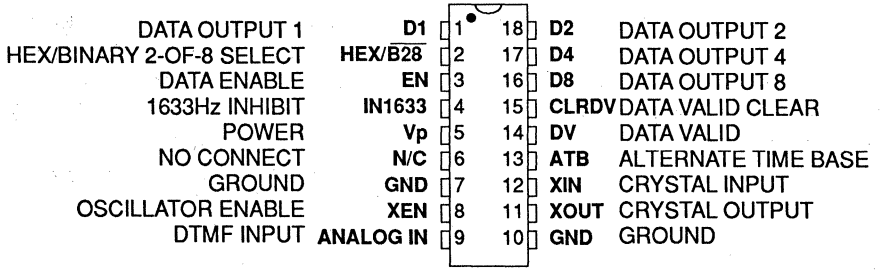


Figure 3 - Clock Options

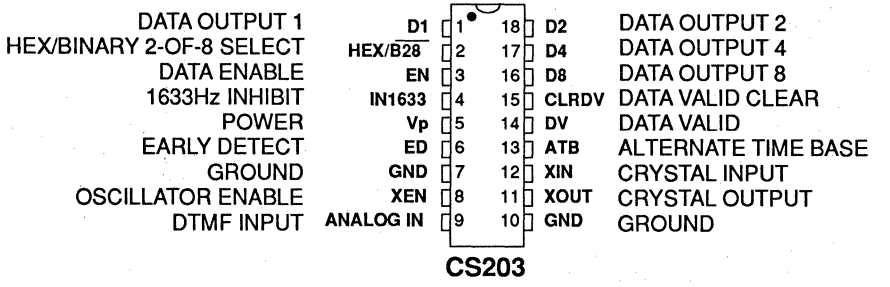
The external clock mode is obtained by tying XIN high and XEN low. In this mode, the internal oscillator output is placed in a high impedance state, and ATB is used to input a 447.443 kHz clock.

Power Supply

The CS202 and CS203 operate on a 5V ± 10% power supply. As with any circuit that combines analog and digital signals, good power supply decoupling is recommended. For best performance, a 0.1µF non-polarized (mylar, ceramic, etc.) capacitor should be tied between Vp and GND. Additional low frequency protection can be achieved with a 10µF electrolytic capacitor connected in parallel with the 0.1µF capacitor. The decoupling capacitors should be situated as close to the device as possible.



CS202



CS203

PIN DESCRIPTIONS

Power Supplies

Vp - Positive Power Supply, PIN 5.
Nominally, +5 volts.

GND - Ground, PINS 7 and 10.
Negative power supply pins. Normally connected to system ground (0 volts). Pin 10 must be connected to ground. Pins 7 and 10 are connected together internally so that an external connection of pin 7 to ground is optional. If pins 7 and 10 are both connected to ground, they should be tied to the same ground trace on the PCB.

Oscillator

XIN - Crystal Input, PIN 12.
Input pin for the crystal oscillator. One lead of the crystal and its bias resistor are tied to this pin.

XOUT - Crystal Output, PIN 11.
Crystal oscillator output pin. One lead of the bias resistor and crystal are tied to this pin.

XEN - Oscillator Enable, PIN 8.
Setting XEN to logic 1 puts the device in the internal clock mode. The on chip oscillator is used as the clock and the ATB pin is configured to output 447.443 kHz ($f_{OSC}/8$). Setting XEN to logic 0 puts the device in the external clock mode. In the external clock mode, a clock signal input to the ATB pin is used to clock the device; the internal oscillator is not used.

ATB - Alternate Time Base, PIN 13.
In the internal clock mode (XEN = 1), ATB will output a 447.443 kHz clock ($f_{OSC}/8$). In the external clock mode (XEN = 0), a 447.443 kHz clock should be input to the ATB pin.

Inputs

ANALOG IN - DTMF Input, PIN 9.
Signal channel input. The DTMF tones to be decoded are input into this pin.

IN1633 - 1633 Hz Inhibit, PIN 4.
Setting IN1633 to logic 1 causes the device to not decode tone pairs which contain 1633 Hz tones. If IN1633 is set to logic 0, the device will decode all 16 DTMF tone pairs.

HEX/$\overline{B28}$ - Hex/$\overline{B28}$, Binary 2-of-8 Select, PIN 2.
Setting HEX/$\overline{B28}$ to logic 1 causes the code corresponding to the decoded DTMF signal to be output in a Hexadecimal format. Data will be output in a Binary 2 of 8 format if HEX/$\overline{B28}$ is set to logic 0.

EN - Data Enable, PIN 3.

Holding EN at logic 1 enables the data outputs. Setting EN to logic 0 causes the data outputs to go to a high impedance state.

CLRDV - Data Valid Clear, PIN 15.

Setting CLRDV to a logic 1 clears a data valid indication on DV.

Outputs

D1; D2; D4; D8 - Data Outputs, PINS 1; 18; 17; 16.

A code corresponding to a decoded DTMF signal is output on these pins. This output can be in hexadecimal ($\overline{HEX}/B28 = 1$) or binary 2 of 8 ($\overline{HEX}/B28 = 0$).

DV - Data Valid, PIN 14.

DV goes to logic 1 when the code corresponding a valid tone pair is present on the data outputs.

ED - Early Detect (CS203 Only), PIN 6.

Indicates data detection prior to processing through the timing circuitry. It is subject to false triggering and drop-outs but can be used to determine if signals are reaching the decoder.

Miscellaneous

N/C - No Connect (CS202 Only), PIN 6.

Not internally bonded.

Semiconductor Corporation

CS204

DTMF Receiver

Features

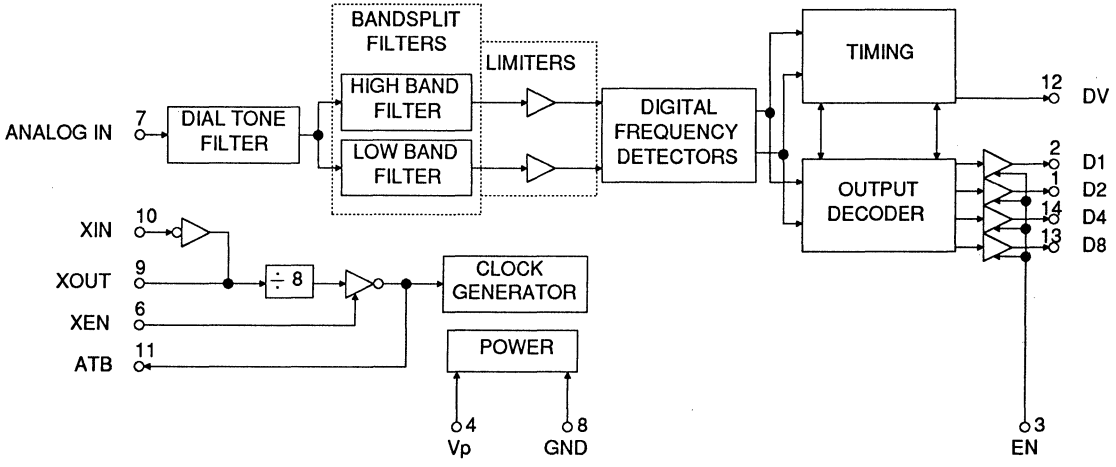
- Full Receiver Implementation
- Central Office Quality
- Detects All 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex Output
- Built-in Filter for Dial Tone Rejection
- 14 Pin Package
- Single 5 Volt ±10% Power Supply
- Low Power CMOS Technology
- Pin Compatible with SSI 204

General Description

The CS204 is a fully integrated DTMF (Dual Tone Multi-frequency) receiver that decodes the tone pairs used in standard tone dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

ORDERING INFORMATION
CS204-P - 14 Pin Plastic DIP
Standard 300 mil DIPs

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	Vp - GND	-	7.0	V
Input Voltage, Any Pin Except Analog in	V_{in}	- 0.5	Vp + 0.5	V
Input Voltage, Analog In	V_{in}	Vp - 10	Vp + 0.5	V
Input Current, Any Pin (Note 1)	I_{in}	-	±10.0	mA
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	- 65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 1. Transient currents of up to 100mA will not cause latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_p	4.5	5.0	5.5	V
Crystal Frequency	F_C	3.5759	3.5795	3.5831	MHz
Ambient Operating Temperature	T_A	0	25	70	°C

DIGITAL CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7Vp	-	Vp	Volts
Low-Level Input Voltage	V_{IL}	0	-	0.3Vp	Volts
High-Level Output Voltage 200 uA load (Note 2)	V_{OH}	Vp - 0.5	-	Vp	Volts
Low-Level Output Voltage 400 uA load (Note 2)	V_{OL}	0	-	0.5	Volts

Note: 2. Does not include XOUT.

Specifications subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current	I_p	-	6.0	12	mA
Frequency Detect Bandwidth	BW	± (1.5+ 2Hz)	±2.3	± 3.5	% of f_0
Detection Amplitude (note 3)	-	- 32	-	- 2	dBm
Twist (note 4)	-	-	±10	-	dB
60 Hz Tolerance	-	-	0.8	-	V_{rms}
Dial Tone Tolerance (note 5, 9)	-	-	22	-	dB
Talk Off (note 6)	-	-	2	-	hits
Power Supply Noise (note 7)	-	-	10	-	mV_{p-p}
Noise Tolerance (note 6, 9)	-	-	- 12	-	dB
Input Impedance at ANALOG IN (note 8)	Z_{in}	100//15	-	-	kohm// pF

Notes:
3. Each tone. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
4. Twist = high tone/low tone.
5. Precise dial tone frequencies of 350Hz ± 2% and 440Hz ± 2%.
6. MITEL tape #CM 7290
7. Bandwidth limited (3kHz) Gaussian noise.
8. V_{in} = (V_p - 10V) to V_p
9. Referenced to lower amplitude tone

6

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Tone Time:					
for detect	t_{on}	40	-	-	ms
for reject	t_{on}	-	-	20	ms
Pause Time:					
for detect	t_{off}	40	-	-	ms
for reject	t_{off}	-	-	20	ms
Detect Time	t_d	25	-	46	ms
Release Time	t_r	25	-	50	ms
Data Setup Time	t_{su}	7	-	-	us
Data Hold Time	t_h	7	9	10	us
Output Enable Time (note 10) C_L = 50 pF, R_L = 1 kohm	t_{en}	-	200	300	ns
Output Disable Time (note 10) C_L = 35 pF, R_L = 500 Ohms	t_{dis}	-	150	200	ns
Output Rise Time (note 10) C_L = 50 pF	t_{rise}	-	200	300	ns
Output Fall Time (note 10) C_L = 50 pF	t_{fall}	-	160	250	ns

Note: 10. R_L and C_L are parallel impedances.

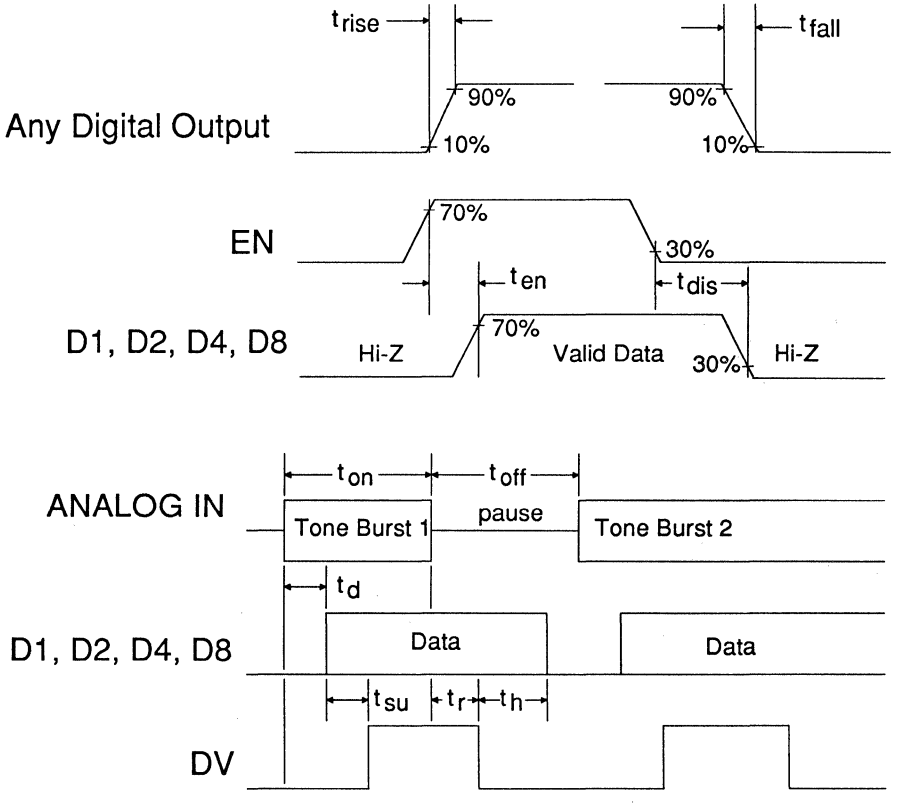


Figure 1 - Timing Diagram

GENERAL DESCRIPTION

The CS204 is a complete Dual Tone Multifrequency (DTMF) Receiver designed to detect 16 digits in a 2-of-8 tone selection scheme. This part provides all of the necessary filtering and requires only an external 3.5795 MHz colorburst crystal and a resistor to provide a reference clock. This device is designed using a high-density, low-power CMOS technology and provides the best performance at the lowest cost.

The CS204 has filtering on board to guarantee the best signal-to-noise performance possible. The DTMF signal is passed through a dial tone reject filter to reduce dial tone interference, and is then separated into low and high groups using two bandsplit filters. The output of each bandsplit filter contains frequency components from only one DTMF tone group.

Table 1 - DTMF Dialing Matrix

Low-Band	High-Band			
	Column 1 1209 Hz	Column 2 1336 Hz	Column 3 1477 Hz	Column 4 1633 Hz
Row 1 697 Hz	1	2	3	A
Row 2 770 Hz	4	5	6	B
Row 3 852 Hz	7	8	9	C
Row 4 941 Hz	*	0	#	D

For a valid DTMF signal to be detected, each group must simultaneously contain only one valid DTMF tone. Detection of the two tones is accomplished with a digital algorithm. The sinusoidal filter output waveforms pass through a pair of hard limiters. The decoder takes the resultant square waves and measures the period. This period measurement varies with jitter created by any extraneous signals within the signal passed to the limiter. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the four expected tones. After two valid tones have been recognized by the decoder, the tones are subjected to a detect timing cycle. The two tones must remain valid for 20 to 40 ms for DV to go high, indicating that a valid digit has been decoded. This prevents voices or other in-band noise from creating a false trigger.

After a valid digit is indicated, the timing circuit will then enable a timing chain that detects drop-outs. If a signal drop of less than 20 ms occurs, it will be ignored. This timing prevents false triggering due to key bounce or other signal interruptions. Any drop-out in excess of 40 ms is considered a valid release; the receiver is reset (DV goes low), and all decoded outputs are cleared for the next decode.

Interfacing to the CS204

The CS204 has analog and data interfaces. The analog interface determines how an analog voice channel is connected. The data interface is used to extract information from the receiver.

The analog interface consists of only one signal: ANALOG IN. The ANALOG IN signal can be either DC-coupled or AC coupled using a 0.01µF capacitor. Care must be taken to not exceed the voltage requirements of the pin. On-chip capacitor coupling guarantees that the signal is properly referenced internally. It is also desirable to add a simple RC lowpass filter to bandlimit the input to the voice band (100 Hz to 3.4 kHz) so that high frequency noise near the 55.9 kHz internal sampling frequency is not aliased into the voice band by the internal switched-capacitor filters.

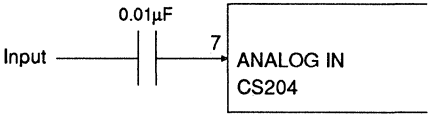


Figure 2 - AC-Coupled Input

The data interface is structured as a synchronous output. Data is extracted from the receiver by using the DV pin as either an output strobe or by scanning and externally detecting the positive-going edge of DV. Data is considered valid only when DV is high.

Clock Generation

The CS204 provides two separate means of clock generation, internal and external. With internal clock generation, a 3.5795 MHz crystal is tied between XIN and XOUT, a 1MΩ resistor is tied in parallel with the crystal to guarantee oscillation, and the XEN signal is tied high enabling the crystal oscillator. In this mode, the ATB pin is a 447.443 kHz clock output which can be used to drive up to 10 other CS202, CS203 or CS204 devices that are in the external clock mode. The external clock mode is obtained by tying XIN high and XEN low. In this mode, the internal oscillator output is placed in a high impedance state, and ATB is used to input a 447.443 kHz clock.

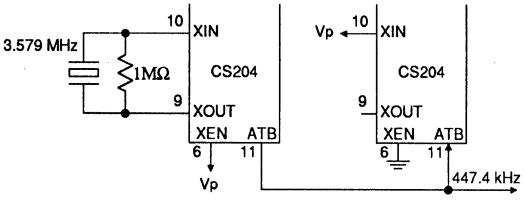


Figure 3 - Clock Options

Power Supply

The CS204 operates from a 5 volts ± 10% power supply. As with any circuit that combines analog and digital signals, good power supply decoupling is recommended. For best performance, a 0.1µF non-polarized (mylar, ceramic, etc.) capacitor should be tied between Vp and GND. Additional low frequency protection can be achieved with a 10µF electrolytic capacitor connected in parallel with the 0.1µF capacitor.

Table 2 - Output Codes

Digit	Hexadecimal			
	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

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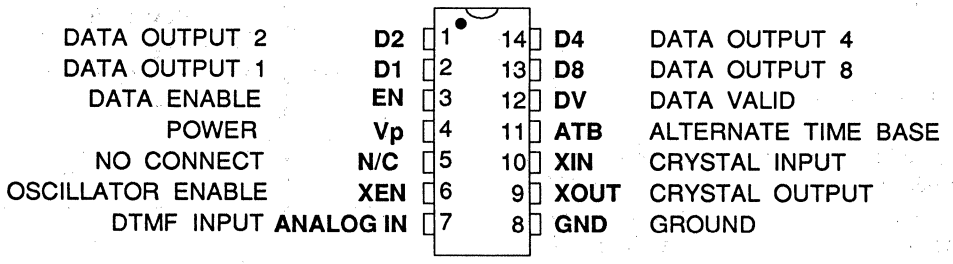
PIN DESCRIPTIONS



Power Supplies

Vp - Positive Power Supply, PIN 4.
Nominally +5 volts.

GND - Ground, PIN 8.
Most negative power supply pin. Normally connected to system ground (0 volts).

Oscillator

XIN - Crystal Input, PIN 10.
Input pin for the crystal oscillator. One lead of the crystal and its bias resistor are tied to this pin.

XOUT - Crystal Output, PIN 9.
Crystal oscillator output pin. One lead of the bias resistor and crystal are tied to this pin.

XEN - Oscillator Enable, PIN 6.
Setting XEN to logic 1 puts the device in the internal clock mode. The on chip oscillator is used as the clock and the ATB pin is configured to output 447.443 kHz ($f_{OSC}/8$). Setting XEN to logic 0 puts the device in the external clock mode. In the external clock mode, a signal input to the ATB pin is used to clock the device; the internal oscillator is not used.

ATB - Alternate Time Base, PIN 11.
In the internal clock mode (XEN=1), ATB will output a 447.443 kHz clock ($f_{OSC}/8$). In the external clock mode (XEN=0), a 447.433 kHz clock should be input to the ATB pin.

Inputs

ANALOG IN - DTMF Input, PIN 7.
Signal channel input. The DTMF tones to be decoded are input into this pin.

EN - Data Enable, PIN 3.
Holding EN at logic 1 enables the data outputs. Setting EN to logic 0 causes the data outputs to go to a high impedance state.

Outputs

D1; D2; D4; D8 - Data Outputs, PINS 2; 1; 14; 13.
A code corresponding to a decoded DTMF signal is output on these pins in a hexadecimal format.

DV - Data Valid, PIN 12.
DV goes to logic 1 when the code corresponding to a valid tone pair is present on the data outputs.

Miscellaneous

N/C - No Connect, PIN 5.
Not internally bonded.

• Notes •

Semiconductor Corporation

CS8870

DTMF Receiver

Features

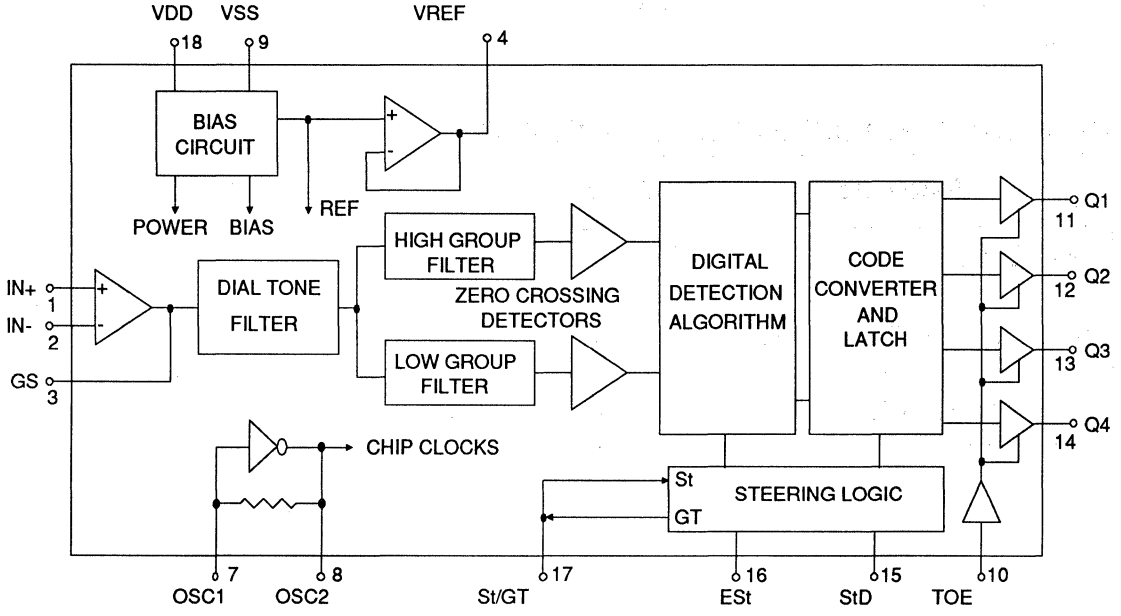
- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitvity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870B

General Description

The CS8870 is a fully integrated DTMF (Dual Tone Multifrequency) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using Crystal's CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

ORDERING INFORMATION
CS8870-IP - 18 Pin Plastic DIP

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V_{DD}-V_{SS}	-	6.0	Volts
Input Voltage	V_{in}	V_{SS}-0.3	V_{DD}+0.3	Volts
Input Current, Any Pin *	I_{in}	-	10	mA
Power Dissipation **	P_D	-	1000	mW
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

*Transient currents of up to 100mA will not cause latch-up.
**Derate above 75°C at 16 mW/°C; all leads soldered to board.

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_{DD} -V_{SS}	4.75	5.0	5.25	Volts
Ambient Operating Temperature	T_A	0	25	70	°C
Crystal Frequency	f_C	3.5759	3.5795	3.5831	MHz

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter	Symbol	Min	Typ *	Max	Units
Supply Current	I_{DD}	-	6.0	10.0	mA
Power Consumption		-	30	45	mW
Input Impedance, pins 1 & 2 (note 12)	R_{IN}	-	10	-	Mohms
Steering Threshold Voltage	V_{TSt}	2.2	-	2.5	V
Signal Levels for Valid Input (each tone of composite signal) (notes 1, 2, 3, 5, 6, 9)		- 29 27.5	- -	+1 883	dBm mVrms
Twist (notes 2,3,6,9,13)		-	±10	-	dB
Frequency Detect Bandwidth (notes 2,3,5,9)		±1.5% ±2Hz	-	±3.5%	
Third Tone Tolerance (notes 2,3,4,5,9,10)		-	- 16	-	dB
Noise Tolerance (notes 2,3,4,5,7,9,10)		-	- 12	-	dB
Dial Tone Tolerance (notes 2,3,4,5,8,9,11)		-	+ 22	-	dB
Clock Output (OSC 2, pin 8) Capacitive Load		-	-	30	pF
V_{REF} Output Voltage No Load	V_{REF}	2.4	-	2.8	V
V_{REF} Output Resistance	R_{OR}	-	10	-	kohms

Parameters measured using test circuit shown in Figure 4.
*Typical figures for design only; not guaranteed and not subject to production testing.

Notes:
1. dBm referenced to power of 1mW into 600Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration of 40ms, tone pause of 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones of the composite signal have equal amplitudes.
6. Tone pair is deviated by ± 1.5% ± 2Hz
7. Bandwidth limited to 3kHz Gaussian noise.
8. Precise dial tone frequencies of 350Hz ± 2% and 440Hz ± 2%.
9. For error rate of better than 1 in 10,000.
10. Referenced to lowest frequency component of DTMF signal.
11. Referenced to minimum valid accept level.
12. Input frequency of 1kHz.
13. Twist = high tone/low tone.

ANALOG CHARACTERISTICS Gain Setting Amplifier

(T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ*	Max	Units
Input Leakage Current (note 14)	I_{IN}	-	100	-	nA
Input Resistance	R_{IN}	-	10	-	Mohms
Input Offset Voltage	V_{OS}	-	25	-	mV
Common Mode Rejection (note 15)	CMRR	-	60	-	dB
Power Supply Rejection (note 16)	PSRR	-	60	-	dB
DC Open Loop Voltage Gain	A_{VOL}	-	65	-	dB
Open Loop Unity Gain Bandwidth	f_C	-	1.5	-	MHz
Output Voltage Swing (note 17)	V_O	-	4.5	-	Vp-p
Tolerable Capacitive Load, GS pin	C_L	-	100	-	pF
Tolerable Resistive Load, GS pin	R_L	-	50	-	kohms
Common Mode Range (note 18)	V_{CM}	-	3.0	-	Vp-p

*Typical figures for design only; not guaranteed and not subject to production testing.

Notes: 14. $V_{SS} \le V_{IN} \le V_{DD}$
15. $-3.0V \le V_{IN} \le +3.0V$
16. At 1kHz
17. $R_L \ge 100k\Omega$ to V_{SS}
18. Unloaded

SWITCHING CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; fc = 3.579545MHz)

Parameter	Symbol	Min	Typ*	Max	Units
Tone Present Detection Time	t_{DP}	5	11	14	ms
Tone Absent Detection Time	t_{DA}	0.5	4	8.5	ms
Tone Duration Accept+	t_{REC}	-	-	40	ms
Tone Duration Reject+	$\overline{t_{REC}}$	20	-	-	ms
Interdigit Pause Accept+	t_{ID}	-	-	40	ms
Interdigit Pause Reject+	t_{DO}	20	-	-	ms
Propagation Delay (St to Q) (note 19)	t_{PQ}	-	8	11	us
Propagation Delay (St to StD) (note 19)	t_{PStD}	-	12	-	us
Output Data Set Up (Q to StD) (note 19)	t_{QStD}	-	3.4	-	us
Propagation Delay (TOE to Q) (note 20) ENABLE	t_{PTE}	-	50	-	ns
DISABLE	t_{PTD}	-	300	-	ns
Clock Input Rise Time	t_{LHCL}	-	-	110	ns
Clock Input Fall Time	t_{HLCL}	-	-	110	ns
Clock Input Duty Cycle	DC_{CL}	40	50	60	%

Parameters measured using test curcuit shown in Figure 4.
*Typical figures for design only; not guaranteed and not subject to production testing.
+User adjustable; see *General Description* on page 30.

Notes: 19. TOE = V_{DD}
20. R_L = 10kΩ, C_L = 50pF

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DIGITAL CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter		Symbol	Min	Typ*	Max	Units
Digital Inputs	"0" level	V_{IL}	-	-	1.5	V
	"1" level	V_{IH}	3.5	-	-	
Digital Outputs (note 21)	"0" level	V_{OL}	-	-	0.03	V
	"1" level	V_{OH}	4.97	-	-	
Output Low (Sink) Current (note 22)		I_{OL}	1	2.5	-	mA
Output High (Source) Current (note 23)		I_{OH}	0.4	0.8	-	mA
Input Leakage Current (note 24)		I_{IH}, I_{IL}	-	0.1	-	uA
Pull Up Source Current (note 25)		I_{SO}	-	7.5	15	uA

*Typical figures for design only; not guaranteed and not subject to production testing.

Notes: 21. No Load
22. V_{OUT} = 0.4V
23. V_{OUT} = 4.6V
24. V_{IN} = V_{SS} or V_{DD}
25. TOE(pin 10) = 0V

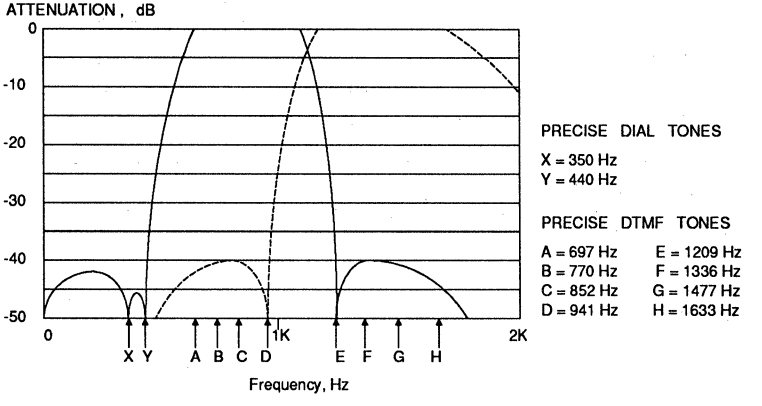
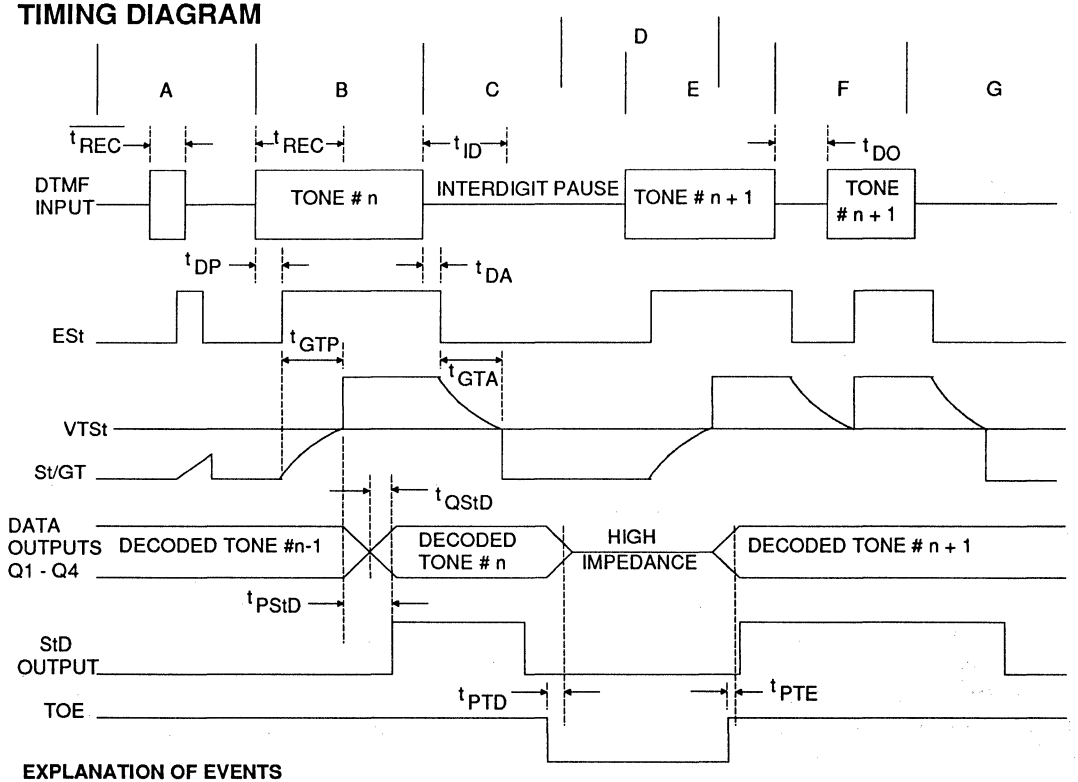


Figure 1 - Filter Characteristics

TIMING DIAGRAM



EXPLANATION OF EVENTS

A. Short tone burst is detected, but duration is invalid.
B. Tone # n is detected, and duration is valid. Decoded to outputs.
C. End of tone # n detected and duration is valid. Outputs remain latched until next valid tone.
D. Three state outputs are disabled (high impedance).
E. Tone # n + 1 is detected and validated. Decoded to outputs.
F. Three state outputs are enabled. Momentary dropout of tone # n + 1 does not register at outputs.
G. End of tone # n + 1 detected and validated. Outputs remain latched until next valid tone.

DEFINITION OF SYMBOLS

ESt - EARLY STEERING OUTPUT - Indicates detection of valid DTMF signal.
St/GT - STEERING INPUT/GUARD TIME OUTPUT - Drives external timing circuit.
Q1-Q4 - DATA OUTPUTS - Gives code corresponding to decoded tone pair.
StD - DELAYED STEERING OUTPUT - Indicates that valid signals have been present (or absent) for the required time.
TOE - TONE OUTPUT ENABLE (Input) - Holding TOE low causes Q1-Q4 to go to high impedance state.

$t_{\overline{REC}}$ - DTMF signal duration too short to be detected as valid.
t_{REC} - Minimum signal duration required for valid recognition.
t_{ID} - Minimum acceptable time between valid signals.
t_{DO} - Maximum allowable dropout of DTMF signal.
t_{PTD} - Propagation Delay, Disable
t_{PTE} - Propagation Delay, Enable
t_{DP} - Time to detect presence of valid signal.
t_{DA} - Time to detect absence of valid signal.
t_{GTP} - Tone Present Guard Time
t_{GTA} - Tone Absent Guard Time.
t_{QStD} - Output Data Setup (Q to StD)
t_{PStD} - Propagation Delay (St to StD)

GENERAL DESCRIPTION

The CS8870 is a complete Dual Tone Multifrequency (DTMF) receiver designed to detect all 16 tone pairs and output a corresponding four bit binary code. This device provides all necessary filtering and requires a minimum of external components. Low power CMOS technology provides the highest performance for the lowest cost.

Filter Section

The CS8870's on chip filtering provides excellent signal-to-noise performance. The DTMF signal is separated into high and low groups using two six pole, bandpass switched capacitor filters. The bandpass filters are elliptical designs with notches placed at 350 Hz and 440 Hz for exceptional dial tone rejection. The output of each bandpass filter contains frequency components from only one DTMF tone group. The filter outputs are smoothed and then limited by high gain comparators, which have hysteresis to reduce sensitivity to unwanted low level signals, jitter, and noise. The comparators' outputs swing from rail to rail at the frequencies of the incoming tones.

Decoder Section

The decoder uses a digital detection algorithm to determine the frequencies of the two tones. The decoder measures the period of the square wave output of the comparators. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the four possible tones in either band. This averaging prevents DTMF simulation by extraneous signals such as voice, while allowing small frequency deviations in the signal. The averaging algorithm has been optimized to provide excellent immunity to "talk-off" and tolerance to the presence of interfering frequencies (third tones) and noise. When both bands simultaneously decode a valid tone, the Early Steering (ESt) output goes high. Should the DTMF signal be lost, the ESt pin will go low.

Steering Circuit

The receiver verifies that the duration of a valid signal is sufficient before registering a decoded tone pair. Tone detection timing is controlled by an external resistor and capacitor (see Figure 2). After a valid tone is present for t_{DP} (Tone Present Detection Time), ESt goes high, and the capacitor discharges through resistor R. The voltage on the St/GT pin changes as a function of the RC time constant, providing the DTMF signal remains valid. When the capacitor voltage (and the voltage on St/GT) reaches the Steering Threshold Voltage, V_{TSt}, the GT output drives the capacitor voltage to VDD. At this point, the four bit code corresponding to the DTMF signal is latched to the outputs. GT remains high as long as ESt remains high. After the output latches settle, the Delayed Steering Output, StD, goes high, indicating that a valid tone pair has been registered. The code is made available at outputs Q1 - Q4 by pulling the three state control input, TOE, to a logic high.

The steering circuit works in reverse to sense the interdigit pause between signals. When the DTMF signal is removed, the capacitor charges. When the Steering Threshold Voltage is reached, GT is pulled to V_{SS}. This circuit also

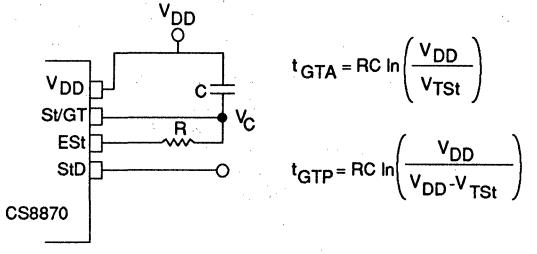


Figure 2 - Basic Steering Circuit

enables the receiver to tolerate signal dropouts too short to be considered a valid pause.

Guard Time Adjustment

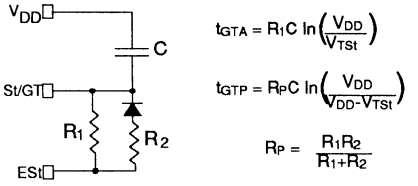
The external timing circuitry shown in Figures 2 and 3, enables the user to adjust the timing to meet specific needs. The following formulas, along with the formulas given in Figure 2, are used to determine the resistor and capacitor values.

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

t_{REC} is the minimum signal duration accepted by the receiver. t_{DP} is the Tone Present Detection Time (the time a valid tone must be present before ESt goes high). t_{ID} is the Interdigit Pause Time. t_{DA} is the Tone Absent Detection Time. Values for t_{DP} and t_{DA} are given in the Switching Characteristics Table. Using the configuration shown in Figure 2, and the recommended capacitor value of 0.1µF, a t_{REC} of 40ms is achieved by using a 390kΩ resistor.

Different circuit configurations may be used to independently select Tone Present Guard Time, t_{GTP}, and Tone Absent Guard Time, t_{GTA}, durations. Using the equations and circuits shown in Figure 3, the designer can meet system specifications which place limits on accept and reject times for tone and pause durations, and tailor system parameters such as "talk-off" and noise immunity. For example, increasing recognition time improves talk-off performance (speech immunity) since it reduces the probability that tones simulated by speech remain valid long enough to register.

a) Decreasing Tone Present Guard Time, t_{GTP} ($t_{GTP} < t_{GTA}$)



b) Decreasing Tone Absent Guard Time, t_{GTA} ($t_{GTP} > t_{GTA}$)

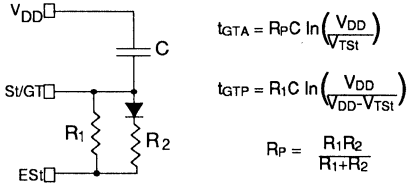


Figure 3 - Steering Circuits for Guard Time Adjustment

Input Configuration

Input signals to the CS8870 pass through an on-chip operational amplifier. A voltage reference, VREF, is provided to bias the input near mid-supply. Figure 4 shows a single ended input configuration with the inputs biased at VREF, and for unity gain. A differential input configuration is shown in Figure 5. The feedback resistor, R5, connected to the op-amp output, GS, can be used to control the gain.

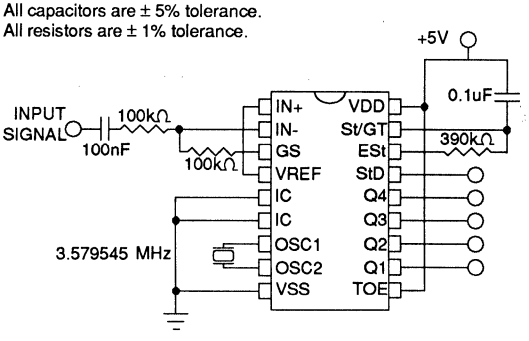
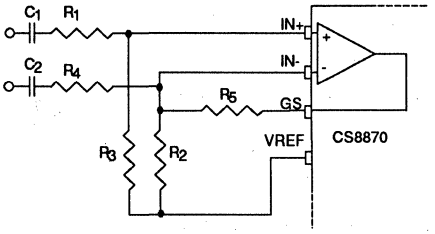


Figure 4 - Single Ended Input Configuration



$C_1 = C_2 = 0.01\mu F$
$R_1 = R_4 = R_5 = 100k\Omega$
$R_2 = 60k\Omega$
$R_3 = 37.5k\Omega$

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{Voltage Gain (Av diff)} = \frac{R_5}{R_1}$$

$$\text{Input Impedance } (Z_{IN} \text{ diff}) = 2\sqrt{R_1 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 5 - Differential Input Configuration

F LOW	F HIGH	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L - LOGIC LOW H - LOGIC HIGH
Z - HIGH IMPEDANCE

Table 1 - Functional Decoding

Crystal Oscillator

An external 3.579545 MHz (TV colorburst) crystal must be connected across pins OSC1 and OSC2 to complete the internal clock circuit. Up to ten CS8870s may be driven by one crystal by connecting the oscillator output, OSC2, with the oscillator input, OSC1, of another device through a 30pf capacitor. Refer to Figure 6.

Logic high on TOE enables the data output pins to output code for the last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See the Functional Decode table, Table 1.

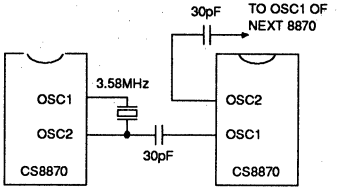


Figure 6 - Oscillator Interconnection

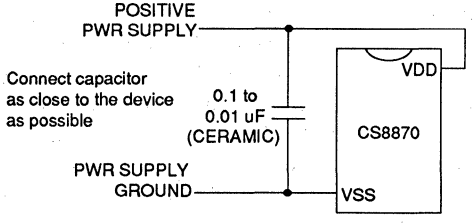
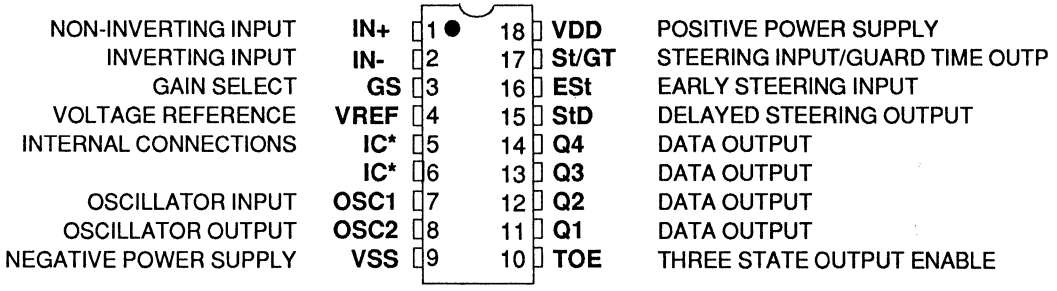


Figure 7. Power Supply Decoupling

PIN DESCRIPTIONS



*Connect to V_{SS}

Power Supplies

VDD - Positive Power Supply Input, PIN 18.

Normally connected to +5 volts. A 0.01µF to 0.1µF ceramic capacitor should be connected as close to the device as possible across V_{DD} and V_{SS}. (See Figure 7).

VSS - Negative Power Supply Input, PIN 9.

Normally connected to 0 volts.

Oscillator

OSC1; OSC2 - Oscillator Input, PIN 7; Oscillator Output, PIN 8.

A 3.579545 MHz crystal connected across these pins completes the internal clock circuit.

Inputs

St/GT - Steering Input/Guard Time Output, PIN 17.

When the voltage on this pin rises past the Steering Threshold Voltage, V_{TSt}, the device registers the detected tone pair, updates the output latch, and drives this pin to a logic high. When the voltage on this pin falls below V_{TSt}, this pin goes to a logic low, freeing the device to accept a new tone pair. The Guard Time Output's function is to reset the external steering time constant. The state of GT is a function of ESt and St.

IN+ - Non-Inverting Input, PIN 1.

Non-inverting input to the front end operational amplifier.

IN- - Inverting Input, PIN 2.

Inverting input to the front end operational amplifier.

TOE - Three State Output Enable, PIN 10.
Logic high on this pin enables outputs Q1 - Q4. Internal pull up.

Outputs

GS - Gain Select, PIN 3.
Connected to the output of the front end operational amplifier. Gain applied to the input can be controlled by a feedback resistor at this pin.

VREF - Voltage Reference, PIN 4.
Voltage on this pin is nominally 2.5 VDC independent of power supply, and may be used to bias inputs at mid supply.

Q1, Q2, Q3, Q4 - Data Outputs, PINS 11, 12, 13, 14.
Logic high on TOE enables pins to output code for last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See Functional Decode Table.

StD - Delayed Steering Output, PIN 15.
Outputs a logic high when voltage on St/GT exceeds V_{TSt} and the output latch has been updated with code from the received tone pair. StD goes to a logic low when voltage on St/GT falls below V_{TSt}.

ESt - Early Steering Output, PIN 16.
Goes to a logic high whenever the detection algorithm detects a valid tone pair. Any loss of a valid DTMF signal causes the output to go to a logic low

IC, IC - Internal Connection, PINS 5, 6.
Both pins must be tied to V_{SS}.

INTRODUCTION

A complete Ethernet/Cheapernet hardware solution is offered by Crystal. The CS8005 is a sophisticated Advanced Ethernet Data Link Controller, which connects to the CS8023A Manchester Code Converter. Connection to the co-ax cable is achieved by the CS83C92C transceiver.

The CS8005 is a high-performance 16-bit Ethernet controller. The CS8005 uses a large dedicated local buffer memory, which off-loads the host CPU and CPU backplane. This local memory, along with a comprehensive command set, allows Ethernet capability to be added with minimal host CPU impact.

The CS8023A Manchester Code Converter is implemented in low-power CMOS, and requires only a single 5 V supply. The CS8023A is implemented in a high-voltage process allowing it to tolerate 16 V fault conditions as required by Ethernet.

Crystal is the first company to bring the benefits of low-power CMOS technology to Ethernet/Cheapernet transceivers. The CS83C92C uses up to 40% less power than the DP8392A and DP8392B. This translates into increased reliability, and compatibility with surface mount technology. The CS83C92C is also the first Ethernet transceiver which is fully compliant with ISO/IEEE 802.3.

CONTENTS

Semiconductor Corporation

CS8005

Advanced Ethernet Data Link Controller

Features

- High Throughput
  - Supports Full 10M BPS Data Rate
  - Back-to-Back Packets
- 64 K-Byte Local Packet Buffer
  - Provides refresh for DRAMs
  - Off-loads host bus
- Conforms to ISO/ISEE 802.3 Standard
- Flexible Bus Interface
  - Intel and Motorola bus modes
  - I/O, string move, DMA access
  - Memory or I/O mapped
  - 8 or 16 bit bus width
- Recognizes One to Six Receive Addresses, Specific, Multicast or Broadcast
- Advanced Error Correction and Handling
  - Automatic re-transmit after a collision
  - Automatically discards bad packets

General Description

The CS8005 has five major blocks: the Transmitter, Receiver, Buffer Controller, Bus Interface and Status and Command Register.

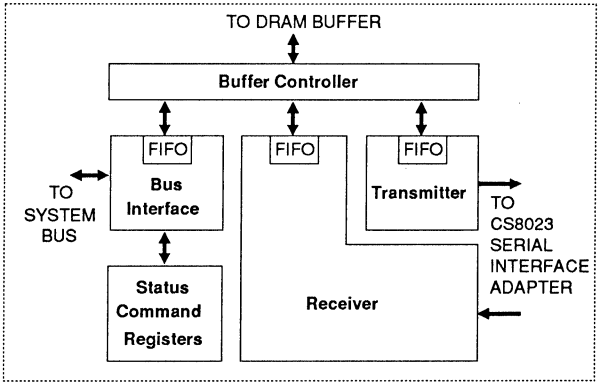
The CS8005 supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, CRC generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses including multicast/broadcast addresses.

The Buffer Controller manages a 64K byte local packet buffer. This block provides arbitration and control for four memory ports: the transmitter, the receiver, the bus interface and an internal DRAM refresh generator. Received packets are temporarily stored until the system either reads or disposes of them, and packets placed there by the system are held for transmission over the link.

The Bus Interface interfaces to the system bus and provides access to internal configuration and status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of Packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called DMA FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the Transmitter or Receiver or refreshing the DRAM.

ORDERING INFORMATION:

CS8005-L	68-pin PLCC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 455-7581

Absolute Maximum Ratings*

Parameter	Min.	Max.	Units
Temperature: Storage	-65	150	°C
Under Bias	-10	+80	°C
All Inputs and Outputs with Respect to Vss	+6	-0.3	V

*Note: Operation at or beyond these limits may cause permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

V_{CC} Supply Voltage	5V ±5%
Ambient Temperature	0°C to 70°C

DC Operating Characteristics (T_A=0 °C to 70 °C; V_{CC}=+5V ±5%; unless otherwise specified)

Parameter		Symbol	Min.	Max.	Unit
Input/Output Leakage	$V_{IN}=V_{CC}$ $V_{IN}=V_{CC}$,	I_{IL}		10 -10	µA µA
Active I_{CC} Current at T_A = 0°C $\overline{CS}$ = V_{IL}, Outputs Open T_A = 0°C		I_{CC}		350	mA
Active I_{CC} Current at T_A = 70°C $\overline{CS}$ = V_{IL}, Outputs Open T_A = 70°C		I_{CC}		280	mA
Input Low Voltage (except $\overline{TXC}$, RXC, CLK)		V_{IL1}	-0.3	0.8	V
Input Low Voltage ($\overline{TXC}$, RXC, CLK)		V_{IL2}	-0.3	0.4	V
Input High Voltage (except $\overline{TXC}$, RXC, CLK)		V_{IH1}	2.0	V_{CC} + 1	V
Input High Voltage ($\overline{TXC}$, RXC, CLK)		V_{IH2}	3.5	V_{CC} + 1	V
Output Low Voltage (except AD0-7)	I_{OL} = 2.1 mA	V_{OL1}		0.40	V
Output Low Voltage (AD0-7)	I_{OL} = 200 µA	V_{OL2}		0.40	V
Output High Voltage (except AD0-7)	I_{OH} = -400 µA	V_{OH1}	2.4		V
Output High Voltage (AD0-7)	I_{OH} = -200 µA	V_{OH2}	2.4		V

A. C. Test Conditions

Output Load:
AD0-AD7, I(load)= ±200 µA
C(load) = 50 pF
All Other Outputs: 1 TTL Gate and C(load) = 100 pF

Input Rise and Fall Times (except TXC, RXC, CLK):
10 ns maximum

Input Rise and Fall Times (TXC, RXC, CLK):
5 ns maximum

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:
Inputs: 1V and 2V
Outputs: 0.8V and 2V

Capacitance (See Note 1; T_A = 25 °C, F = 1 MHz)

Parameter		Symbol	Min.	Max.	Units
Input Capacitance	V_{IN} = 0	C_{IN}		15	pF
Output Capacitance	V_{OUT} = 0	C_{OUT}		15	pF

Note: 1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.

Electrostatic Discharge Characteristics

Parameter		Symbol	Typ	Units
E.S.D. Tolerance (Note 2)	Mil-STD 883 Meth. 3015	V_{ZAP}	>2000	V

Notes: 2. Characterized not tested

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A. C Characteristics (CLK=20MHz; T_A = 0°C to 70°C; V_{CC} = 5V±5%; unless otherwise specified)

Table A. Bus Write Cycle — BUSMODE = 0

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Address Setup Time	t_{AVCSL}	30		ns
2	R/$\overline{W}$ Setup Time	t_{RWLCSL}	30		ns
3	$\overline{CS}$ Pulse Width	t_{CSLCSH}	100		ns
4	Data Setup Time	t_{DVCSH}	70		ns
5	Data Hold Time	t_{CSHDX}	20		ns
6	$\overline{DTACK}$ Assertion Delay (Note 3)	t_{CSLDTL}		60	ns
7	$\overline{DTACK}$ Deassertion Delay	t_{CSHDTH}		60	ns
8	$\overline{DTACK}$ Hi-Z Delay	t_{DTHDTZ}		50	ns
9	Address Hold Time	t_{CSHAX}	20		ns
10	R/$\overline{W}$ Hold Time	t_{CSHRWX}	20		ns
11	$\overline{CS}$ High Time (Note 4)	t_{CSHCSL}	200*		ns
12	Write Recovery Time: a. FIFO Data Write (Note 5) b. Configuration Regs (Notes 5,6) c. Pointer Regs. (Note 7)	t_{CSHDTL}		 800 800 1800	ns ns ns ns
13	$\overline{EN}$ Assert Delay	t_{CSLENL}		50	ns
14	$\overline{EN}$ Deassert Delay	t_{CSHENH}		50	ns
15	$\overline{CS}$ Assert to $\overline{DTACK}$ Valid	t_{CSLDTV}		50	ns

Notes:
3. The trailing edge of $\overline{CS}$ initiates an internal write sequence. Should another $\overline{CS}$ occur during this time, the assertion of $\overline{DTACK}$ will be delayed until the internal write sequence has finished.
4. After changing the Buffer Code (Config. Reg. #1 bits 0-3) Ref. #11 must be increased to 800ns before a Buffer Window access is done in order to allow time for the new Buffer Code to propagate internally.
5. Write Recovery Time is for 16 bit writes. If BUSSIZE = 0 (8bit writes), subtract 200 ns.
6. Configuration Registers are: Command/Status register, Configuration Register #1&2, Interrupt Vector Register, and Station Address Registers.
(Ref. #12, TCSHDTL).
7. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register Transmit End Area Register, and DMA register. If BUSSIZE = 0, subtract 600 ns.

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{CS}$ must be high for at least 350 ns.

Specifications are subject to change without notice.

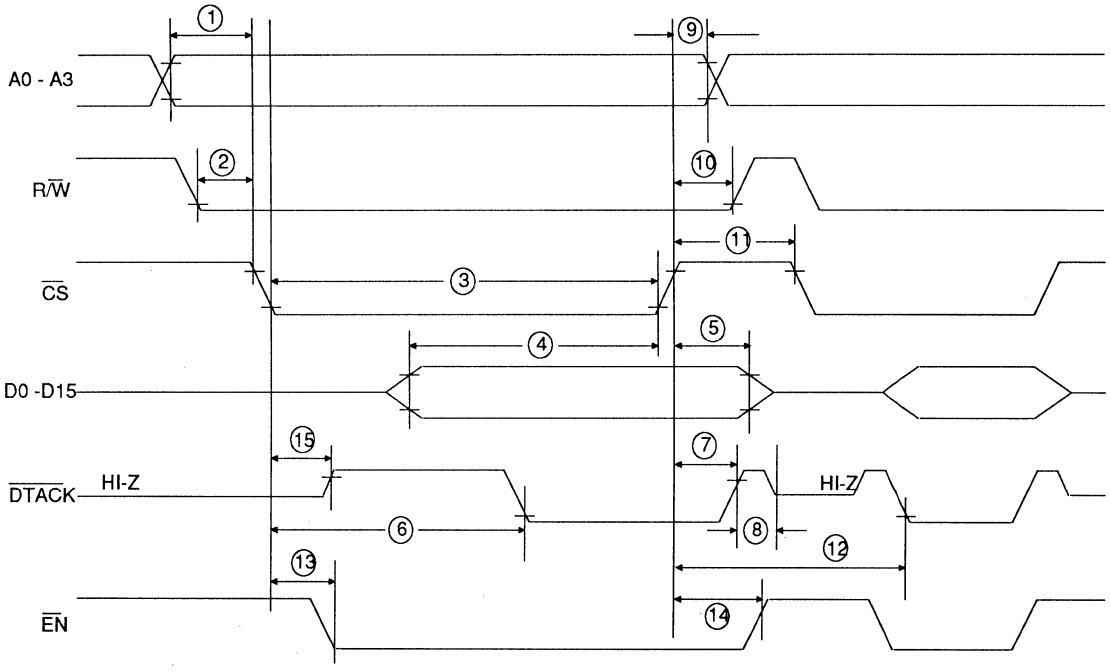

Figure A. Bus Write Cycle Timing Diagram — BUSMODE = 0

7

A. C. Characteristics (Continued)

Table B. Bus Read Cycle — BUSMODE = 0

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Address Setup Time	t_{AVCSL}	30		ns
2	R/$\overline{W}$ Setup Time	t_{RWHCSL}	30		ns
3	$\overline{DTACK}$ Assert Delay a. FIFO Data (Note 8) b. Configuration Regs. (Note 9) c. Other Pointer Regs. (Note 10)	t_{CSLDTL}		 60 800 1800	ns ns ns ns
4	Time from $\overline{DTACK}$ Asserted to Data Valid	t_{DTLDV}		50	ns
5	$\overline{CS}$ Pulse Width	t_{CSLCSH}	100		ns
6	$\overline{DTACK}$ Deassertion Delay	t_{CSHDTH}		60	ns
7	$\overline{DTACK}$ Hi-Z Delay	t_{DTHDTZ}		50	ns
8	Data Hi-Z Delay	t_{CSHDZ}		100	ns
9	Data Hold Time	t_{CSHDX}	20		ns
10	R/$\overline{W}$ Hold Time	t_{CSHRWX}	20		ns
11	Address Hold Time	t_{CSHAX}	20		ns
12	$\overline{CS}$ High Time	t_{CSHCSL}	200*		ns
13	$\overline{APEN}$ Assert Delay	t_{CSLAPL}		400	ns
14	$\overline{APEN}$ Deassert Delay	t_{SHAPH}		50	ns
15	$\overline{EN}$ Assert Delay	t_{CSLENL}		50	ns
16	$\overline{EN}$ Deassert Delay	t_{CSHENH}		50	ns
17	$\overline{CS}$ Assert to $\overline{DTACK}$ Valid	t_{CSLDTV}		50	ns

Notes: 8. The Bus Interface prefetches one word (byte) of FIFO data. Thus, data is generally available immediately and $\overline{DTACK}$ will assert within 50 ns. Following the read, the Bus Interface will fetch the next word (byte) of data. Should another data read occur before the Bus Interface has completed the prefetch, $\overline{DTACK}$ will be delayed until the prefetch is completed. The assert delay in this case is 650 ns max (450 ns in 8 bit mode).

9. Configuration Registers are: Command/Status Register, Configuration Register # 1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. If BUSSIZE = 0 (8 bit reads), subtract 200 ns.

10. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register. If BUSSIZE = 0, subtract 600 ns.

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{CS}$ must be high for at least 350 ns.

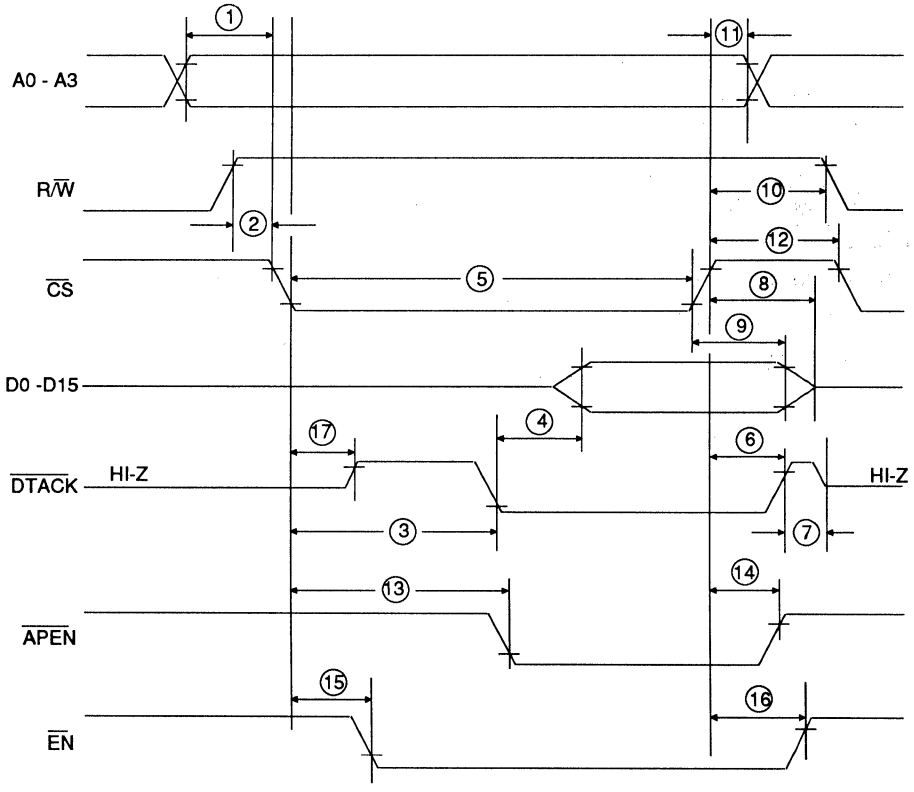

Figure B. Bus Read Cycle Timing Diagram — BUSMODE = 0

A. C. Characteristics (Continued)

Table C. Interrupt Cycle — BUSMODE = 0

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Time from $\overline{DTACK}$ Assert to Data Valid	t_{DTLDV}		50	ns
2	$\overline{DTACK}$ Assert Delay	t_{IALDTV}		600	ns
3	Data Hold from $\overline{IACK}$ Deassert	t_{IAHDX}	20		ns
4	Data Hi-Z from $\overline{IACK}$ Deassert	t_{IAHDZ}		100	ns
5	$\overline{DTACK}$ Deassert Delay	t_{IAHDTH}		60	ns
6	$\overline{DTACK}$ Hi-Z Delay	t_{DTHDTZ}		50	ns
7	R/$\overline{W}$ Setup Time	t_{RWHIAL}	30		ns
8	R/$\overline{W}$ Hold Time from $\overline{IACK}$	t_{IAHRWX}	20		ns
9	$\overline{EN}$ Assert Delay	t_{IALENL}		50	ns
10	$\overline{EN}$ Deassert Delay	t_{IAHENH}		50	ns
11	$\overline{IACK}$ Assert to $\overline{DTACK}$ Valid	t_{IALDTV}		50	ns

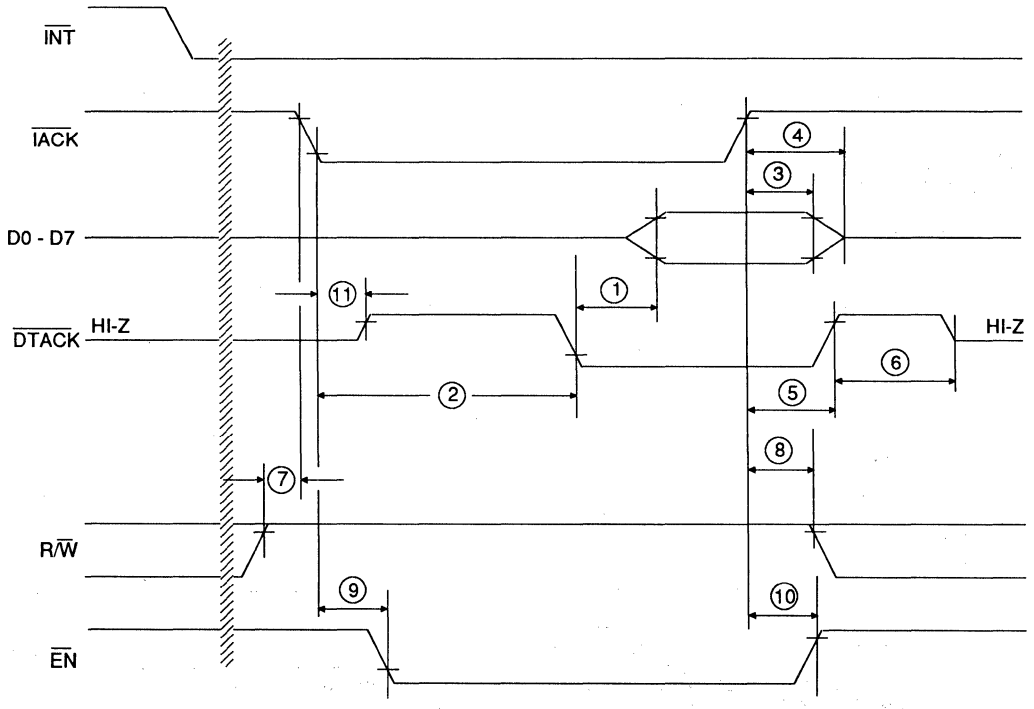

Figure C. Interrupt Cycle Timing Diagram — BUSMODE = 0

A. C Characteristics (Continued)

Table D. DMA Read Cycle — BUSMODE = 0

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	R/$\overline{W}$ Setup Time	t_{RWHDAL}	30		ns
2	$\overline{DACK}$ Pulse Width (Note 11)	t_{DALDAH}	100		ns
3	Time from $\overline{DTACK}$ Asserted to Data Valid	t_{DTLDV}		50	ns
4	Data Hold Time	t_{DAHDX}	20		ns
5	Data Hi-Z Delay	t_{DAHDZ}		100	ns
6	$\overline{DACK}$ High Time	t_{DAHDAL}	200*		ns
7	R/$\overline{W}$ Hold Time	t_{DAHRWX}	20		ns
8	$\overline{TERMCT}$ Asserted While $\overline{DACK}$ Asserted	t_{DALTCL}	125		ns
9	$\overline{DREQ}$ Delay (Note 12)	t_{TCLDRH}		175	ns
10	DREQ Delay After End of DMA Burst (Note 13)	t_{DALDRH}		100	ns
11	$\overline{DTACK}$ Assertion Delay (Note 14)	$t_{DALDTL1}$		60	ns
12	$\overline{DTACK}$ Deassertion Delay	t_{DAHDTH}		60	ns
13	$\overline{DTACK}$ Hi-Z Delay	t_{DTHDTZ}		50	ns
14	$\overline{EN}$ Assert Delay	t_{DALENL}		50	ns
15	$\overline{EN}$ Deassert Delay	t_{DAHENH}		50	ns
16	$\overline{DACK}$ Assert to $\overline{DTACK}$ Valid	t_{DALDTV}		50	ns
17	Read Recovery Time (Notes 15,16)	$t_{DALDTL2}$		800	ns

NOTE: 11. $\overline{DACK}$ must be asserted until $\overline{DTACK}$ is asserted and for a minimum of 100 ns.

12. $\overline{DACK}$ and $\overline{TERMCT}$ must both be active at the same time and for a minimum of 125 ns. The de-assertion of $\overline{DREQ}$ is timed from the last one to assert.
13. Ref. #10 t_{DALDRH} applies for normal DMA burst terminations – not those due to TERMCT.
14. This delay applies only if the 8005 is "ready" when $\overline{DACK}$ is asserted i.e. the first read of a burst, or a read that occurs after the Ref. #17 $t_{DALDTL2}$ period has elapsed.
15. The BIU pre-fetches FIFO data. Thus, data is available immediately for the first read of any burst. Once the BIU detects a read operation, it begins fetching the next byte or word of data. This occurs during the Ref. #17 $t_{DALDTL2}$ period. If a subsequent $\overline{DACK}$ occurs within the Ref. #17 $t_{DALDTL2}$ period, $\overline{DTACK}$ will stay de-asserted until the FIFO data has been fetched. If the subsequent $\overline{DACK}$ does not occur until after the Ref. #17 $t_{DALDTL2}$ period has elapsed, then the 8005 is "ready" and Ref. #11 $t_{DALDTL1}$ applies.
16. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{DACK}$ must be high for at least 350 ns.

All the timing in this table also appies when reading data with programmed I/O; $\overline{CS}$ replaces $\overline{DACK}$ and the $\overline{DREQ}$ and $\overline{TERMCT}$ signals do not apply. A0-A3 setup times are the same as R/$\overline{W}$.

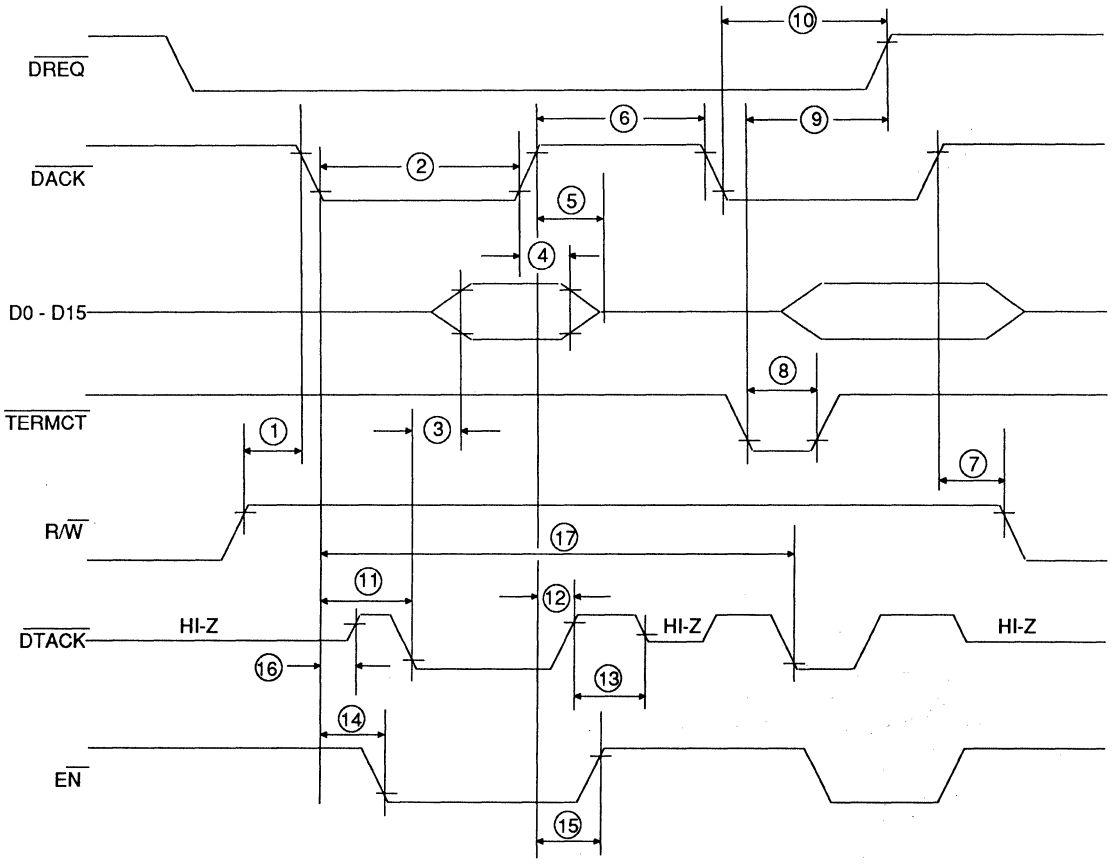

Figure D. DMA Read Cycle Timing Diagram — BUSMODE = 0

A. C. Characteristics (Continued)

Table E. DMA Write Cycle — BUSMODE = 0

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	R/$\overline{W}$ Setup Time	t_{RWLDAL}	30		ns
2	$\overline{DACK}$ Pulse Width (Note 17)	t_{DALDAH}	100		ns
3	Data Setup Time	t_{DVDAH}	70		ns
4	Data Hold Time	t_{DAHDX}	20		ns
5	$\overline{DACK}$ High Time	t_{DAHDAL}	200*		ns
6	$\overline{TERMCT}$ Asserted While $\overline{DACK}$ Asserted	t_{DALTCL}	125		ns
7	R/$\overline{W}$ Hold Time	t_{DAHRWX}	20		ns
8	$\overline{DREQ}$ Delay (Note 18)	t_{TCLDRH}		175	ns
9	DREQ Delay After End of DMA Burst (Note 19)	t_{DALDRH}		100	ns
10	$\overline{DTACK}$ Assertion Delay (Note 20)	t_{DALDTL}		60	ns
11	$\overline{DTACK}$ Deassertion Delay	t_{DAHDTH}		60	ns
12	$\overline{DTACK}$ Hi-Z Delay	t_{DTHDTZ}		50	ns
13	$\overline{EN}$ Assert Delay	t_{DALENL}		50	ns
14	$\overline{EN}$ Deassert Delay	t_{DAHENH}		50	ns
15	$\overline{DACK}$ Assert to $\overline{DTACK}$ Valid	t_{DALDTV}		50	ns
16	Write Recovery Time (Notes 21,22)	t_{DAHDTL}		800	ns

Notes: 17. $\overline{DACK}$ must be asserted until $\overline{DTACK}$ is asserted and for a minimum of 100 ns.

18. $\overline{DACK}$ and $\overline{TERMCT}$ must both be active at the same time and for a minimum of 125 ns. The de-assertion of $\overline{DREQ}$ is timed from the last one to assert.

19. Ref. #9 t_{DALDRH} applies for normal DMA burst terminations – not those due to TERMCT.

20. This delay applies only if the 8005 is "ready" when $\overline{DACK}$ is asserted i.e. the first write of a burst, or a write that occurs after Ref. # 16 t_{DAHDTL} period has elapsed.

21. The trailing edge of $\overline{DACK}$ initiates an internal write sequence that lasts a maximum of 800 ns in 16 bit mode. Should another $\overline{DACK}$ occur during this period, $\overline{DTACK}$ will remain de-asserted until Ref. #16 t_{DAHDTL} period has elapsed. If the subsequent $\overline{DACK}$ does not occur until after the internal write sequence has ended, then the 8005 is "ready" and Ref. # 10 t_{DALDTL} applies.

22. Subtract 200 ns when BUSSIZE = 0 (8 bit mode).

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{DACK}$ must be high for at least 350 ns.

All the timing in this table also applies when writing data with programmed I/O; $\overline{CS}$ replaces $\overline{DACK}$ and the $\overline{DREQ}$, $\overline{TERMCT}$ signals do not apply. A0-A3 times are the same as R/$\overline{W}$.

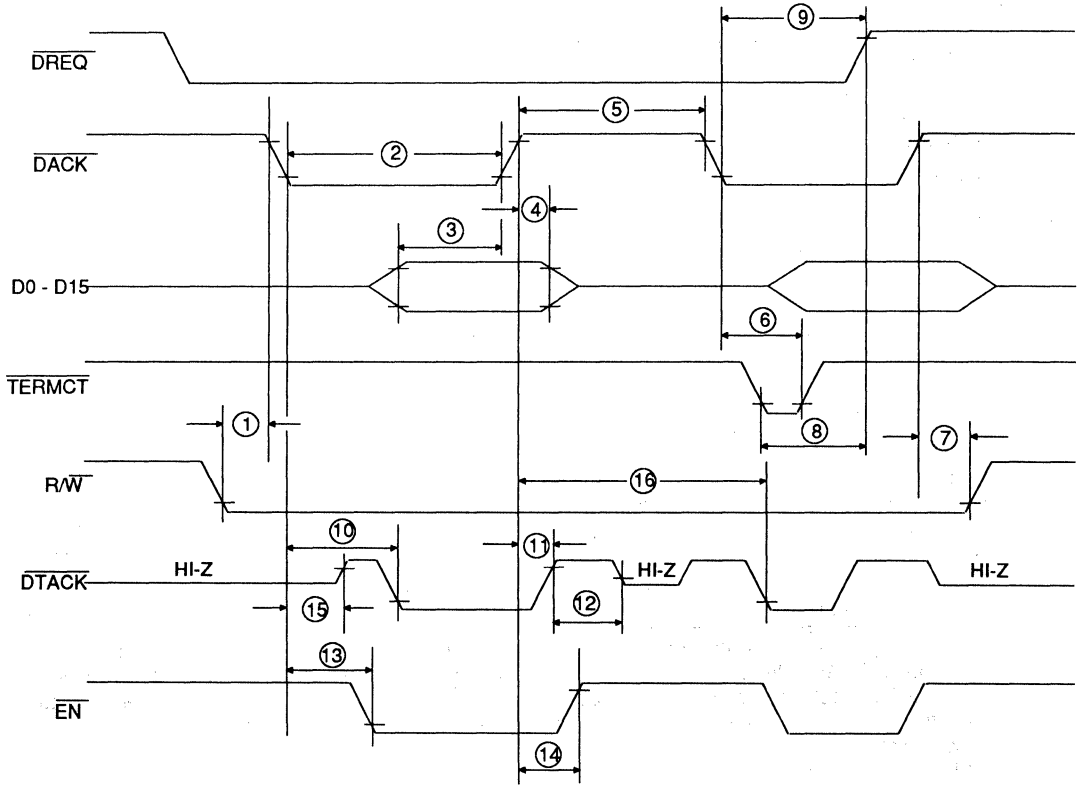

Figure E. DMA Write Cycle Timing Diagram — BUSMODE = 0

A. C. Characteristics (Continued)

Table F. Bus Write Cycle — BUSMODE = 1

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Address Setup Time	t_{AVWL}	30		ns
2	$\overline{CS}$ Setup Time	t_{CSLWL}	30		ns
3	$\overline{IOW}$ Pulse Width	t_{WLWH}	100		ns
4	Data Setup Time	t_{DVWH}	70		ns
5	Data Hold Time	t_{WHDX}	20		ns
6	READY Deassert Delay	t_{WLRYL}		35	ns
7	$\overline{CS}$ Asserted to READY Valid (Note 23)	t_{CSLRYV}		50	ns
8	READY Delay to Hi-Z	t_{CSHRYZ}		50	ns
9	Address Hold Time	t_{WHAX}	20		ns
10	$\overline{CS}$ Hold Time	t_{WHCSH}	20		ns
11	$\overline{IOW}$ High Time (Note 24)	t_{WHWL}	200*		ns
12	Write Recovery Time:	t_{WHRYH}			ns
	a. FIFO Data Write (Note 24)			800	ns
	b. Configuration Regs. (Notes 25, 26)			800	ns
	c. Pointer Registers. (Note 27)			1800	ns
13	$\overline{EN}$ Assert Delay	t_{CSLENL}		50	ns
14	$\overline{EN}$ Deassert Delay	t_{CSHENH}		50	ns

Notes: 23. The trailing edge of $\overline{IOW}$ initiates an internal write sequence. Should another $\overline{IOW}$ occur during this sequence, READY de-asserts (Ref. # 6 t_{WLRYL}) and then asserts after the internal write sequence has finished (Ref. #12 t_{WHRYH}). If the subsequent $\overline{IOW}$ does not occur until after the internal write sequence has ended, then Ref. # 6 t_{WLRYL} has no meaning since READY does not de-assert under this condition.

24. After changing the Buffer Code (Config. Reg. #1 bits 0-3), Ref. #11 must be increased to 800 ns before a Buffer Window access is done in order to allow time for the new Buffer Code to propagate internally.
25. Recovery time is for 16 bit writes. If BUSSIZE = 0 (8 bit writes), subtract 200 ns.
26. Configuration Registers are: Command/Status Register, Configuration Register #1, & 2, Interrupt Vector Register, and Station Address Registers.
27. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Register. If BUSSIZE = 0, subtract 600 ns.

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{IOW}$ must be high for at least 350 ns.

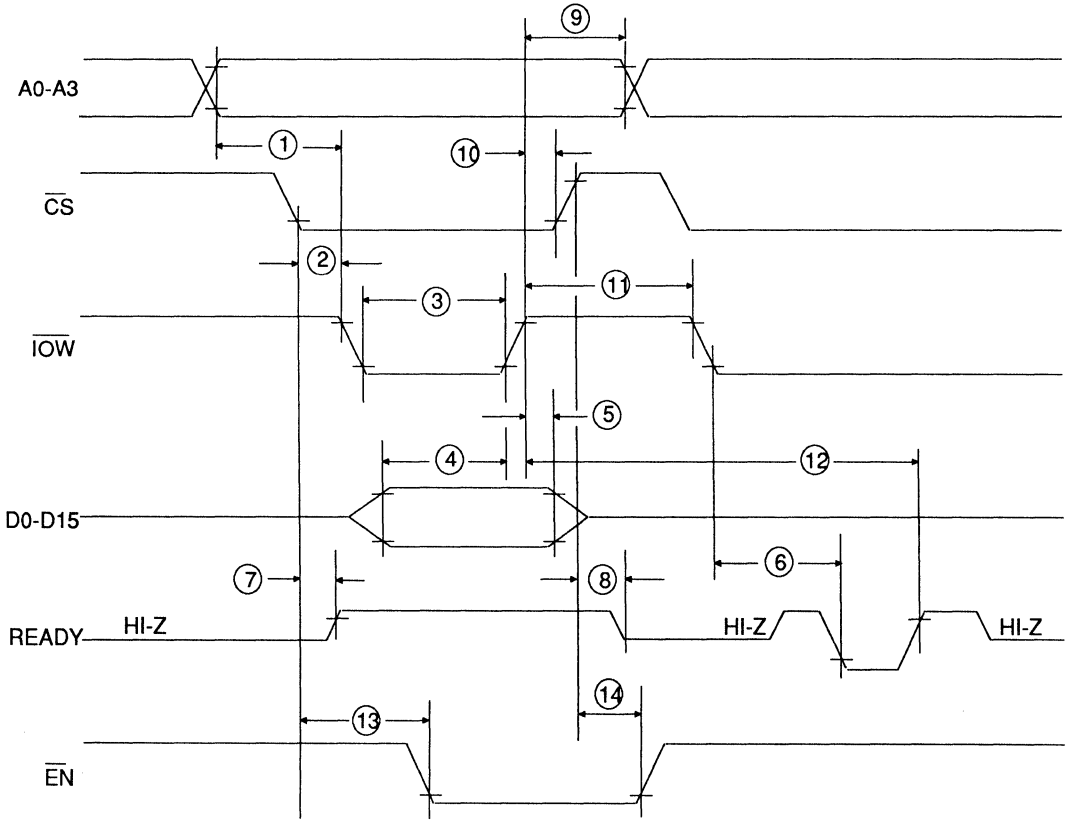

Figure F. Bus Write Cycle Timing Diagram — BUSMODE = 1

A. C. Characterisitcs (Continued)

Table G. Bus Read Cycle — BUSMODE = 1

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Address Setup Time	t_{AVRL}	30		ns
1a	$\overline{CS}$ Setup Time	t_{CSLRL}	30		ns
2	$\overline{IOR}$ High Time	t_{RHRL}	200*		ns
3	READY Assert Delay a. FIFO Data (Note 28) b. Configuration Regs. (Note 29) c. Pointer Registers. (Note 30)	t_{RLRYH}		 35 800 1800	ns ns ns ns
4	READY Deassertion Delay	t_{RLRYL}		35	ns
5	READY Assert to Data Valid	t_{RYHDV}		50	ns
6	READY Delay to Hi-Z	t_{CSHRYZ}		50	ns
7	Data Hold Time	t_{RHDX}	20		ns
8	Data Delay to Hi-Z	t_{RHDZ}		100	ns
9	Address Hold Time	t_{RHAX}	20		ns
10	$\overline{CS}$ Hold Time	t_{RHCSH}	20		ns
11	$\overline{IOR}$ Pulse Width	t_{RLRH}	100		ns
12	$\overline{APEN}$ Assert Delay	t_{RLAPL}		400	ns
13	$\overline{APEN}$ Deassert Delay	t_{RHAPH}		50	ns
14	$\overline{EN}$ Assert Delay	t_{CSLENL}		50	ns
15	$\overline{EN}$ Deassert Delay	t_{CSHENH}		50	ns
16	$\overline{CS}$ Assert to READY Valid	t_{CSLRYV}		50	ns

Notes: 28. The Bus Interface prefetches one word (byte) of FIFO data. Thus, data is generally available immediately and READY will not de-assert during a data read. Following the read, the Bus Interface will fetch the next word (byte) of data. Should another data read occur before the Bus Interface has completed the prefetch, READY will first de-assert and then assert after the prefetch is completed. The assert delay in this case is 800 ns max (600 ns in 8 bit mode).

29. Configuration Registers are: Command/Status Register, Configuration Register # 1, & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. If BUSSIZE = 0 (8 bit reads), subtract 200 ns.

30. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register. If BUSSIZE = 0, subtract 600 ns.

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{IOR}$ must be high for at least 350 ns.

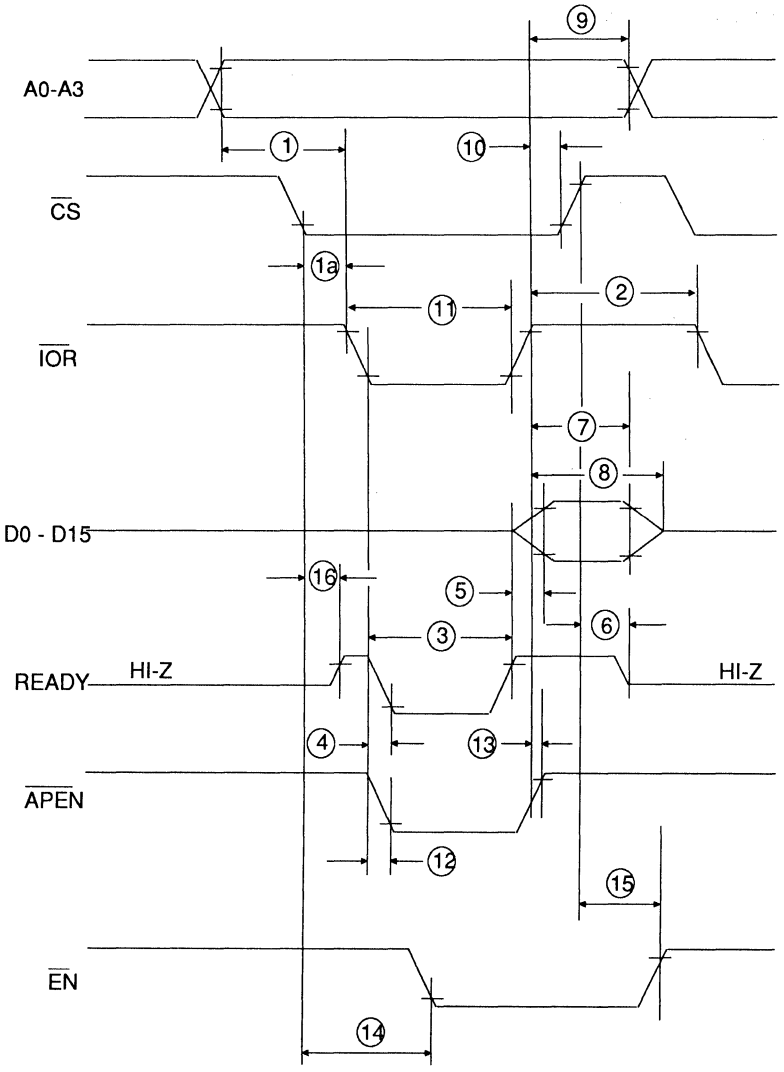

Figure G. Bus Read Cycle Timing Diagram — BUSMODE = 1

A. C. Characteristics (Continued)

Table H. Interrupt Cycle — BUSMODE = 1

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	READY Assert to Data Valid	t_{RYHDV}		50	ns
2	READY Deassertion Delay	t_{RLRYL}		35	ns
3	READY Assert Delay	t_{RLRYH}		600	ns
4	Data Delay to Hi-Z	t_{RHDZ}		100	ns
5	READY Delay to Hi-Z	t_{IAHRYZ}		50	ns
6	Data Hold from $\overline{IOR}$	t_{RHDX}	20		ns
7	$\overline{IACK}$ Setup Time	t_{IALRL}	30		ns
8	$\overline{EN}$ Assert Delay	t_{IALENL}		50	ns
9	$\overline{EN}$ Deassert Delay	t_{IAHENH}		50	ns
10	$\overline{IACK}$ Assert to READY Valid	t_{IALRYV}		50	ns
11	$\overline{IACK}$ Hold Time from $\overline{IOR}$	t_{RHIAH}	20		ns

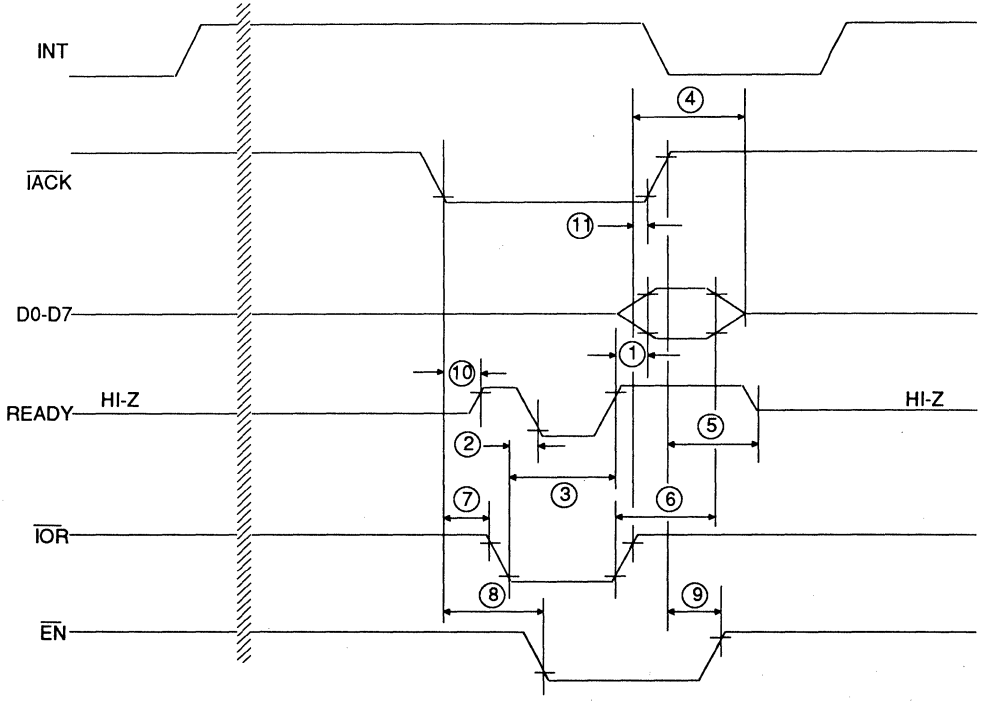

Figure H. Interrupt Cycle Timing Diagram — BUSMODE = 1

A. C. Characteristics (Continued)

Table I. DMA Write Cycle — BUSMODE = 1

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	$\overline{DACK}$ Setup Time	t_{DALWL}	30		ns
2	$\overline{IOW}$ Pulse Width (Note 31)	t_{WLWH}	100		ns
3	Data Setup Time	t_{DVWH}	70		ns
4	Data Hold Time	t_{WHDX}	20		ns
5	$\overline{IOW}$ High Time	t_{WHWL}	200*		ns
6	TERMCT Asserted While $\overline{DACK}$ Asserted	t_{TCHTCL}	125		ns
7	DREQ Delay from TERMCT (Note 32)	t_{TCHDRL}		175	ns
8	DREQ Delay from $\overline{IOW}$ (Note 33)	t_{WLDRL}		100	ns
9	$\overline{DACK}$ Hold Time	t_{WHDAH}	20		ns
10	$\overline{EN}$ Assert Delay	t_{DALENL}		50	ns
11	$\overline{EN}$ Deassert Delay	t_{DAHENH}		50	ns
12	READY Deassert Delay (Note 34)	t_{WLRYL}		35	ns
13	Write Recovery Time (Note 35)	t_{WHRYH}		800	ns
14	READY Delay to Hi-Z	t_{DAHRYZ}		50	ns
15	$\overline{DACK}$ Asserted to READY Valid	t_{DALRYV}		50	ns

Notes: 31. $\overline{IOW}$ must be asserted until READY is asserted and for a minimum of 100 ns.

32. $\overline{DACK}$ and TERMCT must both be asserted at the same time and for a minimum of 125 ns. The de-assertion of DREQ is timed from the last one to assert.

33. Ref. #8 t_{WLDRL} applies for normal DMA burst terminations – not those due to TERMCT.

34. The trailing edge of $\overline{IOW}$ initiates an internal write sequence that lasts a maximum of 800 ns in 16 bit mode. Should another $\overline{IOW}$ occur during this period, READY de-asserts (Ref. #12 t_{WLRYL}) and then asserts after the internal write sequence has finished (Ref. #13 t_{WHRYH}). If the subsequent $\overline{IOW}$ does not occur until after the internal write sequence has ended, then Ref. #12 t_{WLRYL} has no meaning since READY does not de-assert under this condition.

35. Subtract 200 ns when BUSSIZE = 0 (8 bit mode).

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{IOW}$ must be high for at least 350 ns.

All the timing in this table also applies when writing data with programmed I/O; $\overline{CS}$ replaces $\overline{DACK}$ and the $\overline{DREQ}$, TERMCT signals do not apply. A0-A3 times are the same as $\overline{CS}$.

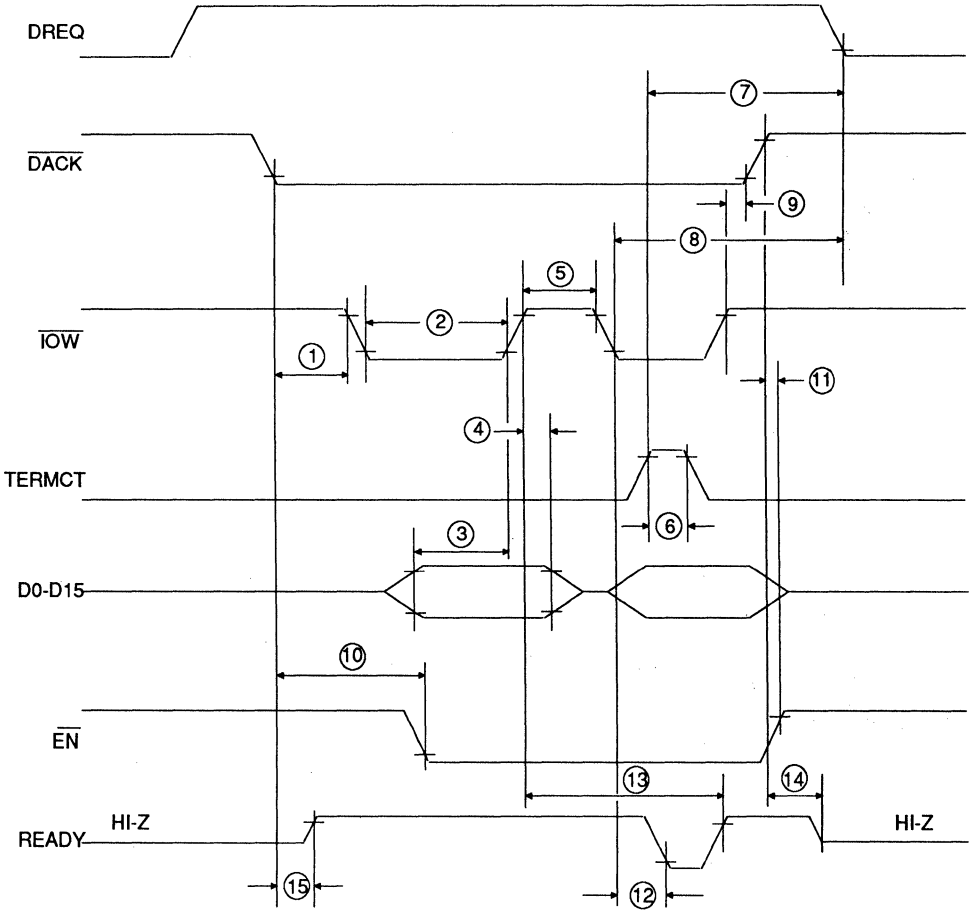

Figure I. DMA Write Cycle Timing Diagram — BUSMODE = 1

A. C. Characteristics (Continued)

Table J. DMA Read Cycle — BUSMODE = 1

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	$\overline{DACK}$ Setup TIme	t_{DALRL}	30		ns
2	$\overline{IOR}$ Pulse Width (Note 36)	t_{RLRH}	100		ns
3	READY Asserted to Data Valid	t_{DVRYH}		50	ns
4	Data Hold Time	t_{RHDX}	20		ns
5	$\overline{IOR}$ High Time	t_{RHRL}	200*		ns
6	TERMCT Asserted While $\overline{DACK}$ Asserted	t_{TCHTCL}	125		ns
7	DREQ Delay from TERMCT (Note 37)	t_{TCHDRL}		175	ns
8	DREQ Delay from $\overline{IOR}$ (Note 38)	t_{RLDRL}		100	ns
9	$\overline{DACK}$ Hold Time	t_{RHDAH}	20		ns
10	Data Hi-Z Delay	t_{RHDZ}		100	ns
11	$\overline{EN}$ Assert Delay	t_{DALENL}		50	ns
12	$\overline{EN}$ Deassert Delay	t_{DAHENH}		50	ns
13	READY Deassert Delay (Note 39)	t_{RLRYL}		35	ns
14	Read Recovery Time (Note 40)	t_{RLRYH}		800	ns
15	READY Delay to Hi-Z	t_{DAHRYZ}		50	ns
16	$\overline{DACK}$ Assert to READY Valid	t_{DALRYV}		50	ns

Notes: 36. $\overline{IOR}$ must be asserted until READY is asserted and for a minimum of 100 ns.

37. $\overline{DACK}$ and TERMCT must be asserted at the same time and for a minimum of 125 ns. The de-assertion of DREQ is timed from the last one to assert.

38. Ref. #8 t_{RLDRL} applies for normal DMA burst terminations – not those due to TERMCT.

39. The Bus Interface pre-fetches FIFO data. Thus, data is available immediately for the first read of any burst. Once the Bus Interface detects a read operation, it begins fetching the next byte or word of data. This occurs during the Ref. #14 t_{RLRYH} period. If a subsequent $\overline{IOR}$ occurs within the Ref. #14 t_{RLRYH} period, READY will de-assert (Ref. #13 t_{RLRYL}) and then assert after the FIFO data has been fetched. If the subsequent $\overline{IOR}$ does not begin until Ref. #14 has ended, then Ref. #13 has no meaning since READY does not de-assert under this condition.

40. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).

* The 200 ns minimum time applies to reads(writes) to(from) the same register. If the current register being written or read differs from the preceeding register, $\overline{IOR}$ must be high for at least 350 ns.

All the timing in this table also applies when reading data with programmed I/O: $\overline{CS}$ replaces $\overline{DACK}$ and the $\overline{DREQ}$, TERMCT signals do not apply. A0-A3 times are the same as $\overline{CS}$.

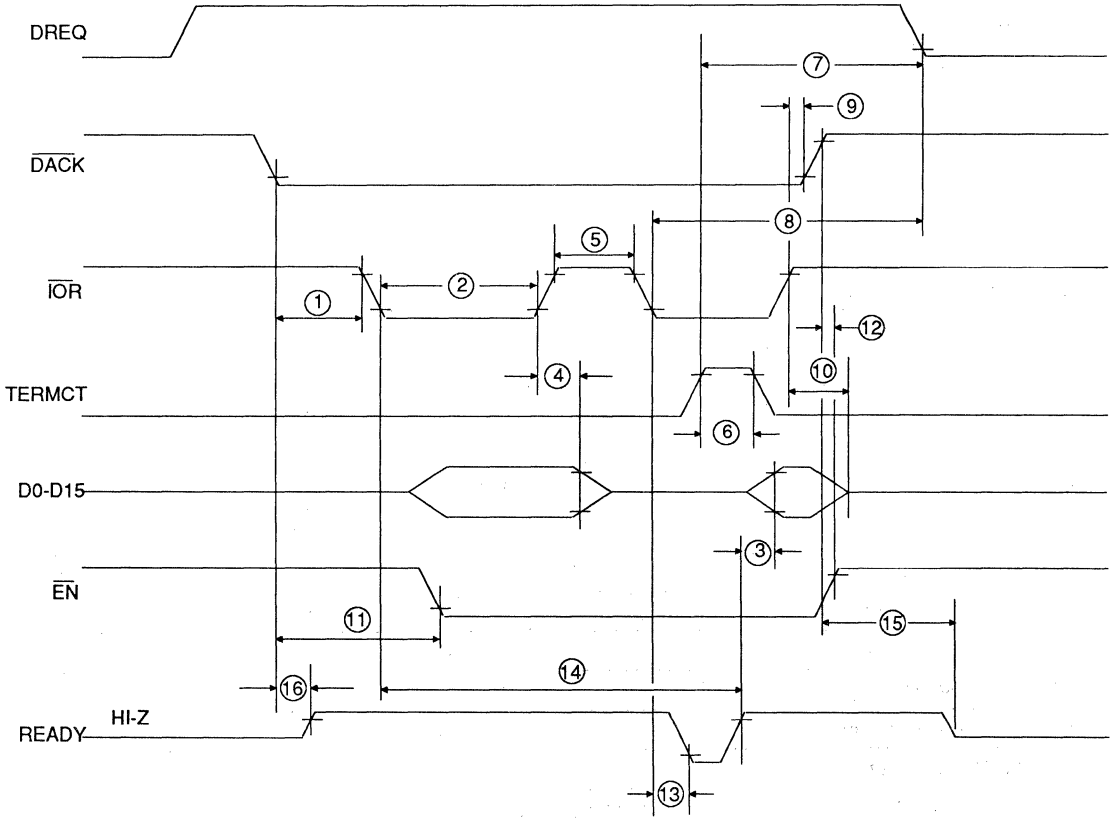

Figure J. DMA Read Cycle Timing Diagram — BUSMODE = 1

A. C. Characteristics (Continued)

Table K. Local Buffer Read or Write Cycle

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Row Address Hold Time	t_{RSLAX}	100		ns
2	Row Address Setup Time	t_{AVRSL}	25		ns
3	$\overline{RAS}$ Pulse Width High	t_{RSHRSL}	200		ns
4	Column Address Hold Time	t_{CSLAX}	45		ns
5	Column Address Setup Time	t_{AVCSL}	10		ns
6	$\overline{CAS}$ Pulse Width — High	t_{CSHCSL}	60		ns
7	$\overline{CAS}$ Pulse Width — Low	t_{CSLCSH}	110		ns
8	Address Hi-Z to $\overline{G}$ Low Time	t_{AZGL}	0		ns
9	$\overline{G}$ Setup Time to $\overline{CAS}$	t_{GLCSH}	70		ns
10	$\overline{G}$ to Data Valid	t_{GLDV}		40	ns
11	Data Hold from CAS Deassert	t_{CSHDX}	0		ns
12	Data Hi-Z from CAS Deassert	t_{CSHDZ}		40	ns
13	Read or Write Cycle Time a. Single Cycle b. Page Mode	t_{AVAV}	 600 200		 ns ns
14	Data Setup Time	t_{DVWL}	5		ns
15	Data Hold Time	t_{WLDX}	60		ns
16	Write Pulse Width	t_{WLWH}	60		ns
17	$\overline{CAS}$ Setup to $\overline{W}$	t_{CSLWL}	60		ns
18	Write Setup Time	t_{WLCSH}	40		ns
19	$\overline{RAS}$ Cycle Time	t_{RSLRSL}	600		ns

Note: TMS 4464-10, -12 or equivalent satisfies the above timing.

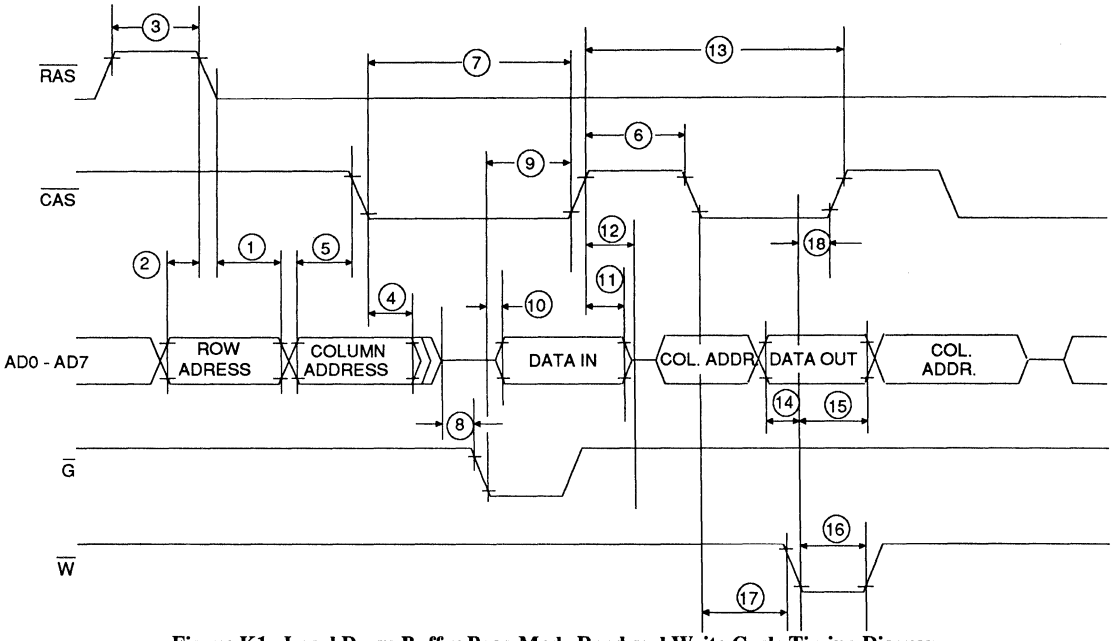

Figure K1. Local Dram Buffer Page-Mode Read and Write Cycle Timing Diagram

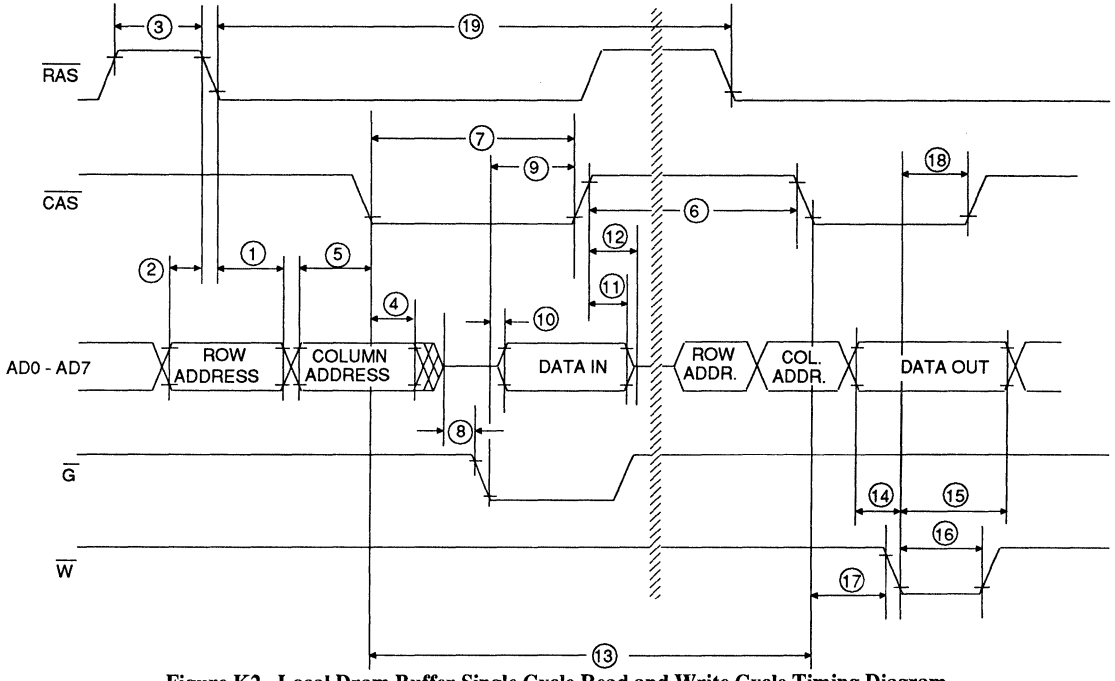

Figure K2. Local Dram Buffer Single Cycle Read and Write Cycle Timing Diagram

A. C. Characteristics (Continued)

Table L. Local Buffer Refresh Cycle

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	Address Setup Time to $\overline{RAS}$	t_{AVRSL}	25		ns
2	Address Hold Time from $\overline{RAS}$	t_{RSLAX}	100		ns
3	$\overline{RAS}$ Pulse Width	t_{RSLRSH}	200		ns
4	$\overline{RAS}$ Cycle Time	t_{RSLRSL}	400		ns

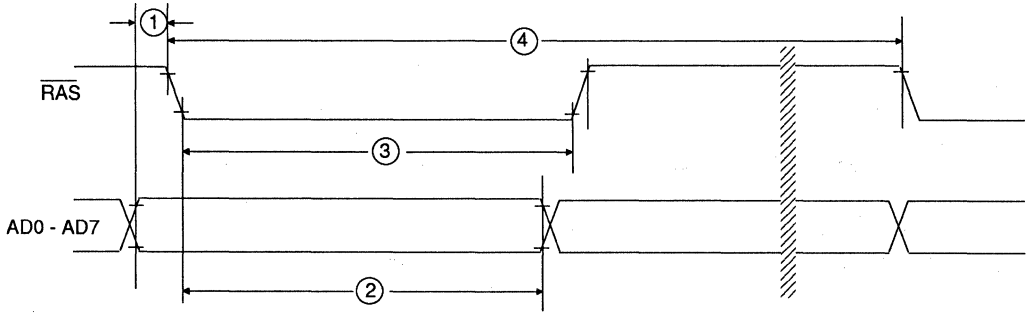

Figure L. Local Dram Buffer Refresh Cycle Timing Diagram

A. C. Characteristics (Continued)

Table M. Serial Interface Timing

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	$\overline{TXC}$/RXC Cycle Time	t_{CKHCKH}	100		ns
2	$\overline{TXC}$/RXC High Width	t_{CKHCKL}	40		ns
3	$\overline{TXC}$/RXC Low Width	t_{CKLCKH}	40		ns
4	TXD Delay from $\overline{TXC}$	t_{CKLDV}		60	ns
5	RXD Setup to RXC	t_{DVCKH}	30		ns
6	RXD Hold Time from RXC	t_{CKHDX}	20		ns
7	TXEN Delay from $\overline{TXC}$	t_{CKLTEH}		60	ns
8	TXEN Hold Time from $\overline{TXC}$	t_{CKLTEL}	20		ns
9	CSN Setup to RXC	t_{CSHCKH}	20		ns
10	CSN Hold Time from RXC	t_{CKHCSL}	20		ns
11	COLL Pulse Width	t_{CHCL}	200		ns

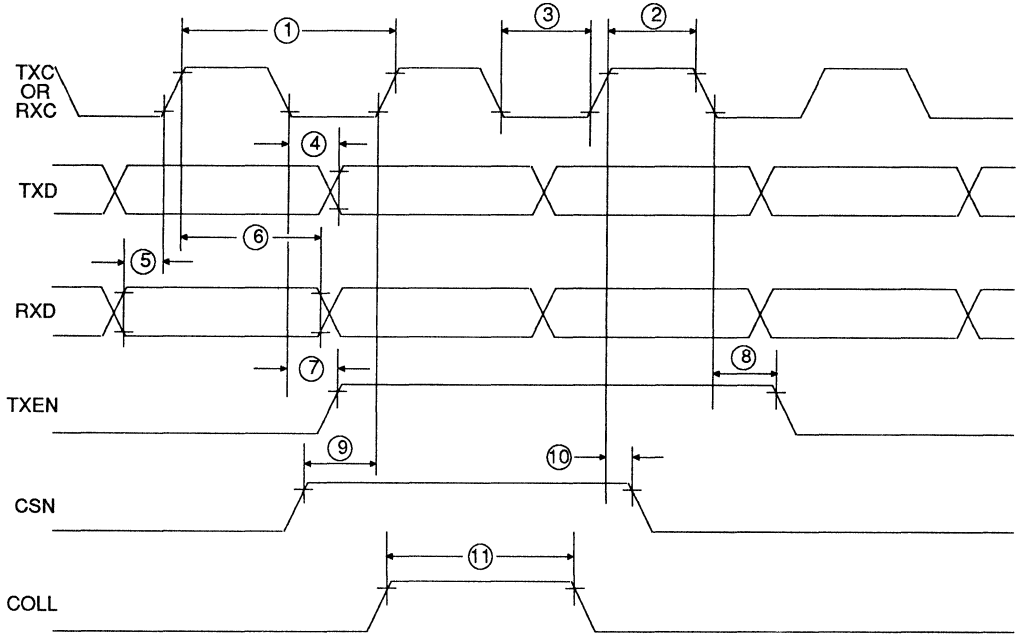

Figure M. Serial Transmit & Receive Interface Timing

A. C. Characteristics (Continued)

Table N. Master Clock and Reset Timing

Ref. #	Parameter	Symbol	Min.	Max.	Units
1	CLK Pulse Width High	t_{CKHCKL}	15	25	ns
2	CLK Pulse Width Low	t_{CKLCKH}	15	25	ns
3	CLK Cycle Time	t_{CKHCKH}	49.9	50.1	ns
4	Reset Pulse Width	t_{RSLRSH}	1		µs

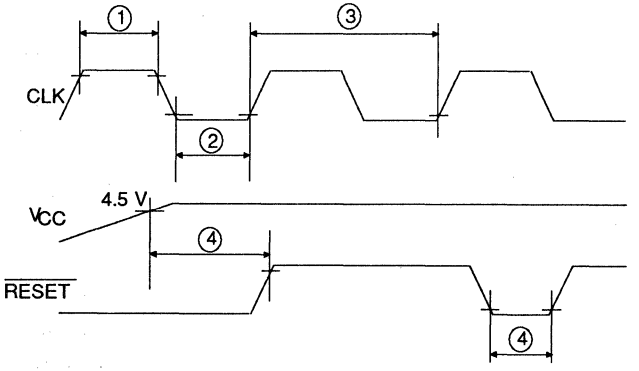

Figure N. Master Clock and Reset Timing

Block Diagram Description

The CS8005 has three major blocks: the AEDLC Advanced Ethernet Data Link Controller, Buffer Controller and Bus Interface.

The CS8005 supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, CRC generation/stripping, transmission deferral, collision handling and address recognition of up to 6 receive addresses as well as multicast/broadcast addresses. CTRLO and $\overline{\text{LPBK}}$ are general purpose outputs that can be used to control, for example, the loopback function of the CS8023A Manchester Code Converter. For non-IEEE 802.3 applications such as serial backplane buses, support is also provided for 2 byte address recognition, reduced slot time and reduced preamble length.

The Buffer Controller provides management for a 64K byte local packet buffer consisting of two 64K x 4 dynamic RAMS. This block provides arbitration and control for four different memory

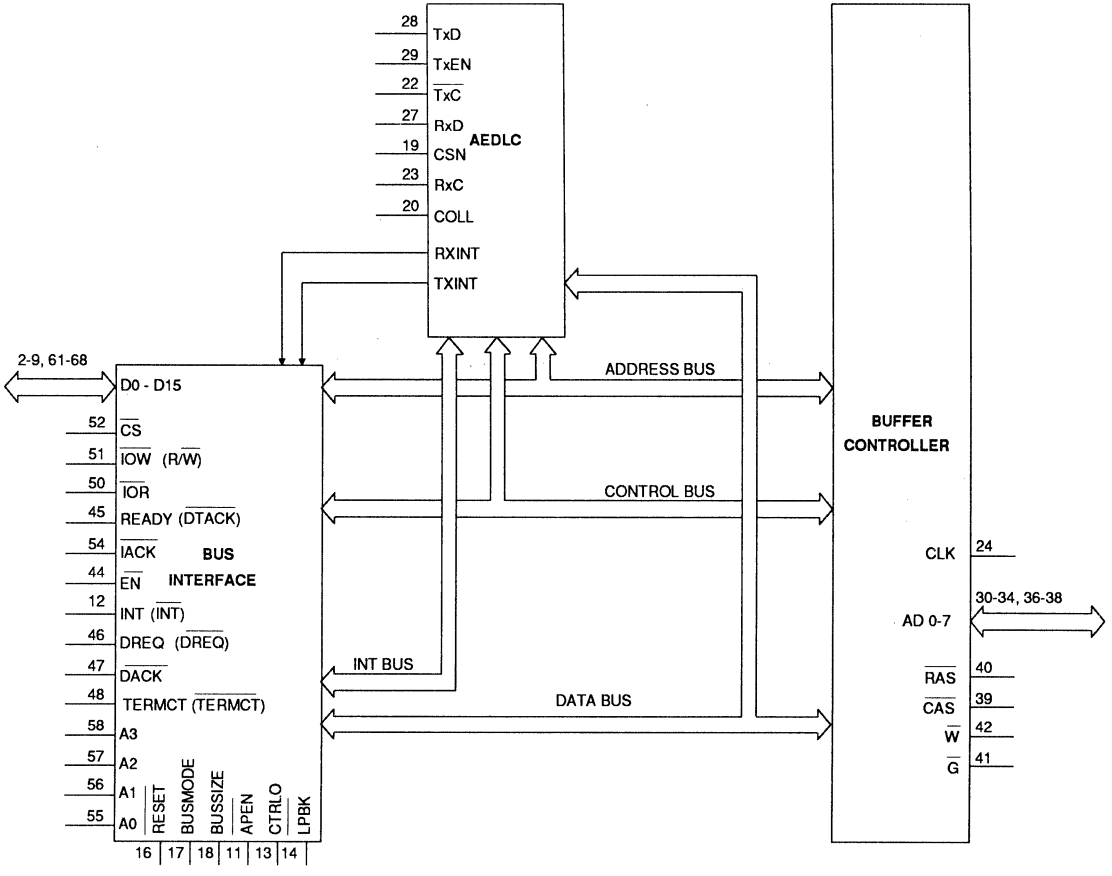

Figure 1. CS8005 Block Diagram

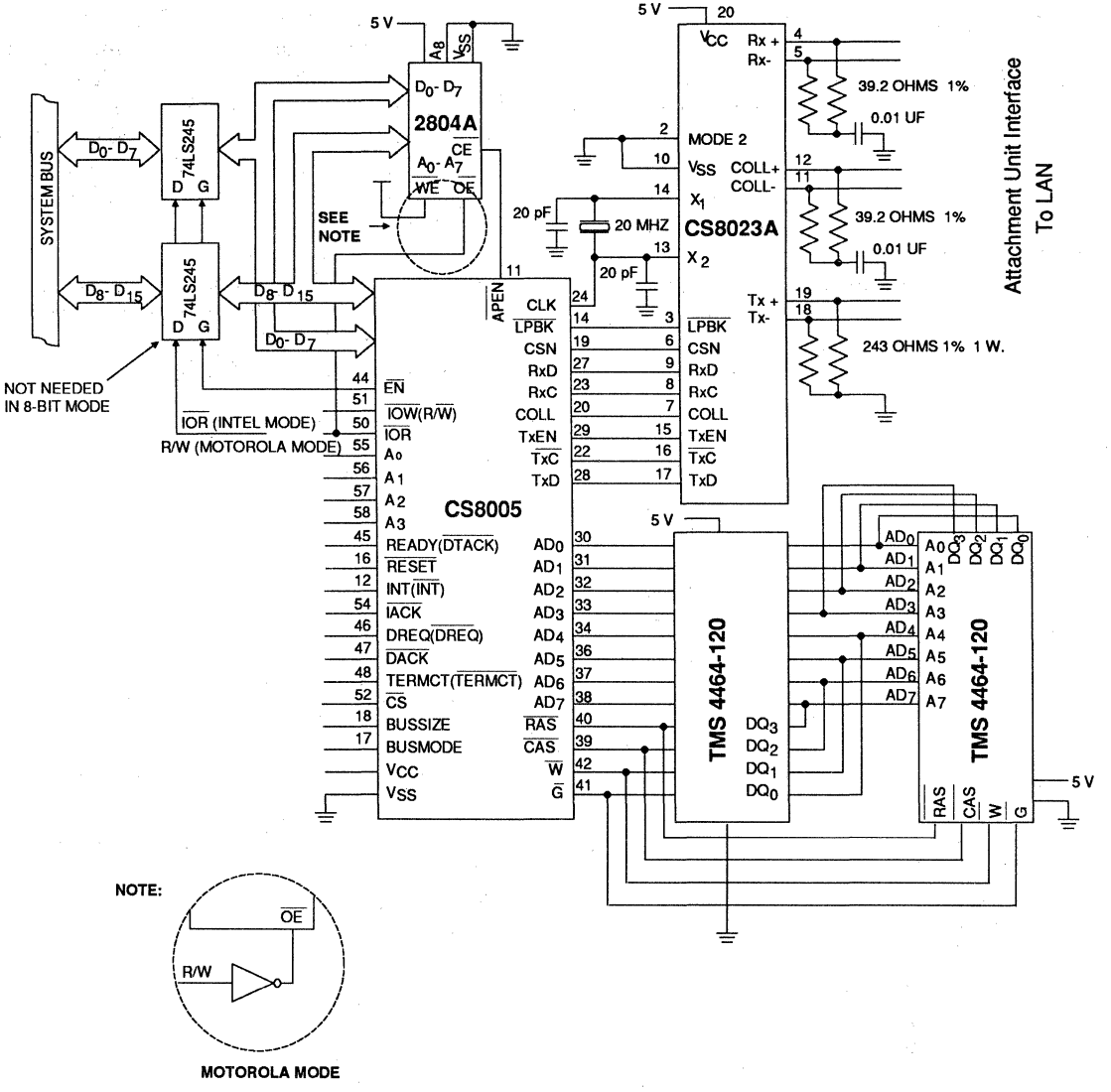

Figure 2. CS8005 Interconnection Diagram

ports: the CS8005 Transmitter, for network transmit packets; the CS8005 Receiver, for received frames; the Bus Interface, for system data and control; and an internal DRAM refresh generator. To minimize pin count, dynamic RAM addresses and data are time multiplexed on a single 8 bit bus. A control line and an 8 bit address is also provided to permit reading from a locally attached EEPROM or PROM. This permits configuring a P.C. board with its receive address(es) and configuration data independent of the network layer software used.

The Buffer Controller interfaces to the system bus and provides access to internal configuration/status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called DMA FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the Transmitter or Receiver or refreshing the DRAM. Both 8 and 16 bit transfers are supported, and byte ordering on a 16 bit bus is under software control. The CS8005 supports both Intel-compatible and Motorola-compatible buses.

The CS8005 Interconnect Diagram

The interconnect diagram shows the CS8005 in a typical system configuration, connecting to the LAN via an CS8023A Manchester Code Converter. The Attachment Unit Interface connects to an Ethernet (10BASE5); Cheapernet (10BASE2); or a twisted pair (10BASE-T) network.

Separate TMS 4464-120 64K DRAMs store received packets, or packets waiting for transmission. AD0 -AD7 address both RAMs. Data is exchanged on the AD leads, DQ0 - DQ3 to one RAM, and DQ4 - DQ7 to the other RAM. The System Bus exchanges data with the Buffer Controller in the CS8005. Two bi-directional data buffers (74LS45) interface 16-bit data, only one buffer is used for 8-bit data. The 2804 PROM stores the node address. The CS8005 has six 6-byte address fields.

Buffer Management

The Buffer Controller manages a 64K byte packet buffer into which packets that are received are temporarily stored until the system either reads or disposes of them and packets placed there by the system are held for transmission over the link. The buffer is logically divided into separate receive and transmit areas of selectable size. The transmit area always originates at address 0. Each packet in the buffer is prefixed by a header of 4 bytes that contains command and status information and a 16 bit pointer to the start of the next packet in the buffer.

To transmit packets, the system loads one or more packets of data, complete with header information, into the transmit area of the buffer and commands the CS8005 to begin transmission, starting from the address contained in the Transmit Pointer. When transmission is complete, the CS8005 updates the status byte in the header and interrupts the system if so programmed. The Transmit Pointer automatically wraps to location 0 when the Transmit Buffer Limit (TBL) is reached.

The Buffer Controller manages the buffer area as a circular buffer with automatic wraparound. As data is received from the CS8005 it is stored in the buffer beginning at the location specified by the Receive Pointer. The Receive Pointer will wrap from FF,FF to Transmit Buffer Limit + 1,00. For example, if TBL = 80 the Receive Pointer wraps to 81,00. If the Receive Pointer reaches Write Protect Pointer (WPP),00 an overflow has occurred. The Receiver is turned off and an interrupt is issued. Restarting the Receiver is accomplished by freeing up buffer space and turning the Receiver back on.

Transmit Packet Format

Each Packet to be transmitted consists of a four byte header and up to 65,532 bytes of data which are placed into the local buffer via the Bus Interface. The header contains the following information in the indicated order:

1. Most significant byte of the address of the next packet header.
2. Least significant byte of the address of the next packet header.
3. A transmit command byte.
4. A transmit status byte which should be initialized to zero by the system and will contain status for this packet when transmission is complete.

Bytes 1 and 2, called the Next Packet Pointer, point to the location immediately following the last byte of the packet, which is the first byte of the next packet header, if it exists. In 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used. Byte 1 is the more significant byte.

Byte 3 is the Transmit Command byte. It contains information to guide the controller in processing the packet associated with this block.

Bit 0: Xmit Babble Interrupt Enable. The CS8005 will transmit packets as large as the Transmit buffer can hold but will abort transmission of oversized packets if this bit is set to a one. If Tx Interrupt Enable is set, an interrupt will be issued. This condition is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC. If babble occurs with bit 0-Xmit Babble Int. Enable set to a 1 on byte 3 - the Transmit Command byte, the Transmitter will abort transmission and turn itself off. When the bit is set to 0, no interrupt is generated, and the Transmitter is not turned off, but a status bit is set in the Status Header.

Bit 1: Xmit Collision Interrupt Enable. When set to a one, an interrupt will be generated if a collision occurs during a transmit attempt. The transmitter will attempt to transmit the packet again (after an appropriate delay) up to 15 times, issuing an interrupt for each collision.

Bit 2: 16 Collisions Enable. When set to a one, a Transmit Interrupt will be generated if 16 collisions occur during a transmit attempt, and the transmitter will be turned off. If Tx Interrupt Enable is set, an interrupt will be issued. When set to 0, no interrupt is generated. The transmitter will continue to the next packet if there is one, and a status bit is set in the Status Header.

Bit 3: Xmit Success Interrupt Enable. When set to a one, a Transmit Interrupt will be generated if the transmission is successful, that is, fewer than 16 collisions occurred.

Bit 4: Not used.

Bits 5 and 6: Decode these bit as follows:

Chain Continue (Bit 6)	Data Follows (Bit 5)	Action Taken by Transmitter
0	0	Null Header: the transmitter turns off without sending a packet
0	1	Transmitter sends appended packet and then turns off
1	0	Skip Header: the transmitter skips current packet, and goes on to the next packet using the Next Packet Pointers
1	1	Transmitter sends appended packet; then goes on to next packet.

These two bits are the only control bits required for transmit packet chaining and the CS8005 ignores the Done bit (Transmit Status byte, bit 7). For additional information on chaining packets see the Applications section of this data sheet.

Bit 7: Xmit/Receive. If this bit is a one, the current header is for a packet to be transmitted. If this bit is a zero, the packet header will be processed as a header only and no data follows (bit 5).

Byte 4 is the Transmit Status byte, which is written by the Buffer Controller upon conclusion of each packet transmission or retransmission attempt. It provides for reporting of both normal and error termination conditions of each transmission.

Bit 0: Xmit Babble. If set to a one, transmit babble occurred during the transmission attempt. This is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC. If babble occurs with bit 0-Xmit Babble Int. Enable set to a 1 on byte 3, the Transmit Command byte, the transmitter will abort transmission and turn itself off.

Bit 1: Xmit Collision. If set to a one, a collision occurred during the transmission attempt.

Bit 2: 16 Collisions. If set to 1, 16 collisions occurred during the transmission attempt.

Bit 3, 4, 5 and 6: Reserved.

Bit 7: Done. If set to a one, the controller has completed all processing of the packet associated with this header (either the packet has been sent successfully or 16 collisions occurred) and there is now valid status in the Status byte.

The data field follows the fourth byte.

Receive Packet Format

Each Packet received is preceded by a four byte header and is placed into the local buffer via the Buffer Controller. The header contains the following information in the indicated order:

1. Most significant byte of the address of the next packet header.
2. Least significant byte of the address of the next packet header.
3. Header Status byte.
4. Packet Status byte .

Bytes 1 and 2, called the Next Packet Pointer, point to the first byte of the next receive packet header. The next packet header starts immediately after the end of the current packet. The packet length is equal to the difference between the starting addresses of the two packet headers minus four. If the value of the Next Packet Pointer is less than the current one, the pointer has wrapped around from the end of the buffer to the Receive Start Area (the Receive Start Area equals the Transmit Buffer Limit address + 1). When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.

The third byte of the header contains header information associated with this packet.

Bits 0 through 5: Not Used.

Bit 6: Data Follows. If this bit is set to a one, there is received packet delta following the header ready to be processed. If this bit is a zero, no additional packet data is available in the chain and the following buffer will be used for the next incoming packet.

Bit 7: Xmit/Receive. This bit is always set to 0 by the controller to indicate a receive packet header.

The fourth byte of the header, called the Packet Status byte, contains status information resulting from processing the packet associated with this block.

Bit 0: Oversize Packet. If this bit is a one, the packet was larger than 1514 bytes, excluding the Preamble and CRC fields. The CS8005 will accept an oversize packet and generate an interrupt if Rx Interrupt Enable is set to one.

Bit 1: CRC Error. If this bit is a one, a CRC Error occurred in this frame. CRC status is captured on byte boundaries, so that 7 or less dribble bits will not cause a CRC error.

Bit 2: Dribble Error. Packets are integral multiples of octets (bytes). If this bit is a one, the received packet did not end on an octet (byte) boundary.

Bit 3: Short Packet. If this bit is a one, the packet contained less than 64 bytes including CRC. Short packets are properly received as long as they are at least 6 bytes long; packets with less than 6 bytes will only be received if the match mode bits in Configuration Register #1 specify promiscuous mode, multicast/broadcast is selected and the first bit of the destination address is a 1, or the 2-byte address mode has been selected.

Bits 4 , 5 and 6: Not used.

Bit 7: Done. If this bit is a one, the controller has completed all processing of this packet and there are now valid pointers and status in this header. The user may now move this packet out of the local buffer, if desired, and reuse this buffer space.

The data field follows this byte, unless this is a header only packet.

Registers

There are nine directly accessible 16 bit registers in the CS8005, one of which is used as a "window" into indirectly accessed registers as well as the local buffer memory. Access is controlled by chip select, I/O read, I/O write and four address inputs, A0-A3. The following description assumes a 16 bit wide system interface; as such, the low order address input, A0, is shown as "X", a don't care. In 8 bit mode, input pin A0 selects bits 0 through 7 of the register when a zero, and bits 8 through 15 when a one. Note that the byte swap bit does not affect the byte order of these registers.

All "not used" bits should be set to 0 to maintain future compatibility. When read, "not used" bits read as '1'.

Command Register, A3-0 = 000X (Write only)

Bit 0: DMA Interrupt Enable. When set to a 1, completion of a DMA operation, as signaled by Terminal Count, will generate an interrupt.

Bit 1: Rx Interrupt Enable. When set to a 1, this bit enables interrupts whenever a packet becomes available in the packet buffer.

Bit 2: Tx Interrupt Enable. When set to a 1, this bit enables interrupts for completion of transmit operations. See the Transmit Header Command byte description for conditions that can cause an interrupt.

Bit 3: Buffer Window Interrupt Enable. Setting this bit to a one enables interrupts for Buffer Window register reads from the packet buffer.

Bit 4: DMA Interrupt Acknowledge. Setting this bit to a one causes a pending DMA interrupt to be cleared.

Bit 5: Rx Interrupt Acknowledge. Setting this bit to a one causes a pending Receive interrupt to be cleared.

Bit 6: Tx Interrupt Acknowledge. Setting this bit to a one causes a pending Transmit interrupt to be cleared.

Bit 7: Buffer Window Interrupt Acknowledge. Setting this bit to a one causes a pending Buffer Window interrupt to be cleared.

Bit 8: Set DMA On. Setting this bit to a one enables the DMA request logic. If the DMA FIFO is set to the read direction, a DMA Request will be asserted when the DMA FIFO has enough bytes to satisfy the burst size. If the DMA FIFO is in the write direction the DMA Request will be asserted immediately. Clearing this bit has no effect. Setting this bit with bit 11 set will force a DMA Interrupt, provided the DMA Interrupt Enable bit is set, which permits

testing the interrupt without actually performing DMA operations.

Bit 9: Set Rx On. Setting this bit to a one enables the Receiver. Clearing this bit to a 0 has no effect. Setting this bit with bit 12 set will force an interrupt, provided the Receive Interrupt Enable bit is set, which permits testing the interrupt without receiving packet data.

Bit 10: Set Tx On. Setting this bit to a 1 enables the Transmitter. The Buffer Controller will read the header information pointed to by the Transmit pointer and process the packet accordingly (see transmit packet header description). The conditions for interrupting upon completing packet processing are specified in the Transmit Header Command byte, which is stored in the buffer memory. Setting this bit with bit 13 set will force a transmit interrupt for test purposes.

Bit 11: Set DMA Off. Setting this bit to a one disables the DMA Request logic.

Bit 12: Set Rx Off. Setting this bit to a one disables the receive logic. If the CS8005 is actively receiving a packet when bit 12 is set, the Receiver will be disabled immediately without finishing the packet and without updating any receive packet header which may be in progress. Bit 9 Rx On will be '1' until the receiver is disabled.

Bit 13: Set Tx Off. Setting this bit to a one disables the transmitter. If a packet is being transmitted when this bit is set, transmission of the packet will immediately be aborted.

Bit 14: FIFO Read. When set to a one, the DMA FIFO direction is set to read from the packet buffer. The FIFO direction should not be changed from a write to a read until it is empty (see FIFO status bits).

Bit 15: FIFO Write. When set to a one, the DMA FIFO direction is set to write to the packet buffer. Changing the DMA FIFO direction clears the DMA FIFO.

Status Register, A3-0=000X (Read only)

Bit 0: DMA Interrupt Enable. When set, this bit indicates that interrupts are enabled for terminal count during a DMA operation.

Bit 1: Rx Interrupt Enable. When set, this bit indicates that interrupts are enabled for receive events.

Bit 2: Tx Interrupt Enable. When set, this bit indicates that interrupts are enabled for transmit events.

Bit 3: Buffer Window Interrupt Enable. When set, this bit indicates that interrupts are enabled for Buffer Window reads from the packet buffer.

Bit 4: DMA Interrupt. When set, this bit indicates that DMA has been terminated, either due to terminal count or the DMA On bit being written off. If the associated Interrupt Enable bit is set, an interrupt will also be asserted.

Bit 5: Rx Interrupt. When set, this bit indicates that a Receive packet chain is available. If the associated Interrupt Enable bit is set, an interrupt is also asserted.

Bit 6: Tx Interrupt. When set, this bit indicates that a Transmit interrupt condition has occurred. The following are valid Tx Interrupt conditions: Xmit Babble, Xmit Collisions, Xmit 16 Collisions and Xmit Success. If the Tx Interrupt enable bit is set, an interrupt is also asserted.

Bit 7: Buffer Window Interrupt. When set, this bit indicates that data has been read from the local buffer into the DMA FIFO and is ready to be read via the Bus Interface. If the associated interrupt enable bit has been set, an interrupt is asserted.

Bit 8: DMA On. When set, this bit indicates that the DMA logic is enabled. When Terminal Count is asserted during a DMA transfer, this bit will be reset to indicate that the DMA activity has been completed. When reset, this bit three-states the DREQ pin.

Bit 9: Rx On. When set, this bit indicates that the Receiver is enabled. This bit remains set during active reception of a packet and turns 'off' at the end of reception if bit 12 Rx off is set.

Bit 10: Tx On. When set, this bit indicates that the Transmitter is enabled.

Bits 11 & 12: Not used.

Bit 13: DMA FIFO Full. When set, this bit indicates that the DMA FIFO is full.

Bit 14: DMA FIFO Empty. When set, this bit indicates that the DMA FIFO is empty.

Bit 15: FIFO Direction. When set, this bit indicates that the DMA FIFO is in the read direction; when cleared, it indicates that the DMA FIFO is in the write direction. After hardware or software reset, this bit is cleared.

Configuration Register 1, A3-0=001X

Bits 0-3: Buffer Code. These four bits are the Buffer Window Code bits, which determine the source of Buffer Window register reads and the destination of buffer window register writes. Buffer code bits 3-0 should be set to '1000' by pointing to local buffer memory before turning FIFO to read direction to perform reads.

Buffer Code Selection Table

Buffer Code Bits				Buffer Window Reg. Contents
3	2	1	0	
0	0	0	0	Receive addr. reg. 0
0	0	0	1	Receive addr. reg. 1
0	0	1	0	Receive addr. reg. 2
0	0	1	1	Receive addr. reg. 3
0	1	0	0	Receive addr. reg. 4
0	1	0	1	Receive addr. reg. 5
0	1	1	0	Address PROM
0	1	1	1	Transmit Buffer Limit
1	0	0	0	Local buffer
1	0	0	1	Interrupt vector
1	0	1	X	Reserved — do not use
1	1	X	X	Reserved — do not use

Bits 4-5: DmaBurstInterval. These two bits specify the interval between DMA requests.

5	4	Burst Interval
0	0	Continuous
0	1	800 nanoseconds
1	0	1600 nanoseconds
1	1	3200 nanoseconds

If configured for continous mode, the DMA request will persist until Terminal Count is asserted.

DMA Burst Size Selection

Bits 6-7: DmaBurstSize. These two bits specify the DMA Burst Transfer count.

7	6	# of DMA Tranfers/Burst
0	0	1
0	1	4
1	0	8
1	1	16 (Illegal in word mode)

Bits 8-13: These six bits select which of the receive address register sets (each register set contains 6 bytes) will be used to compare incoming destination addresses. Bit 8 corresponds to receive address register set 0, bit 9 to register set 1, ... bit 13 to register set 5. A '1' in any bit enables that Receive Address register set for reception. These bits are both read and write.

Bits 14-15: These two bits define the match modes for the Receiver logic.

15	14	Match Mode Description
0	0	Specific addresses only
0	1	Specific + broadcast addresses
1	0	Above + multicast addresses
1	1	All frames (promiscuous mode)

Configuration Register 2, A0-A3=010X

Bit 0: ByteSwap. The normal order for packing packet bytes into a 16 bit word is low byte first, i.e., the first byte of a packet is contained in bits 0 through 7, the second byte in bits 8 through 15. Setting this bit to a 1 causes the high and low order bytes to be swapped for data reads and writes to the Buffer Window Register when the CS8005 is in 16 bit mode. Control registers are not affected. This bit has no effect when the CS8005 is in 8 bit mode. It should not be changed when a DMA is in progress. Changing this bit will not affect the sequence of receive data bytes in the local buffer memory since the swap occurs on the system (Bus Interface) side of the buffer memory. This bit is both read and write.

Bit 1: AutoUpdWPP. If this bit is set to 1, the Write Protect Pointer will be updated with the most significant byte of the DMA pointer whenever the Buffer Controller crosses a packet buffer page while reading DMA data. In this way, as buffer memory space is released by reading from it, free buffer space is automatically allocated to the Receive logic. Turn Auto Upd WPP off before enabling reads from transmit space.

Bit 2: Not Used. This bit should be written to '0' for future compatibility.

Bit 3: CRC Error Enable. When set, the receiver will accept packets with CRC errors, place them in the local buffer and indicate that a packet is available via the Rx Interrupt Status bit. If the CRC Error Enable bit is set and the Tx Interrupt Enable bit is also set, one Rx interrupt will occur in response to a CRC error.

Bit 4: Dribble Error. When set, the receiver will accept packets with a byte alignment error. If the Dribble Error bit is set and the Rx Interrupt Enable bit is also set, one Rx interrupt will occur in response to a dribble error.

Bit 5: Short Frame Enable. When set, packets of less than 512 bits (64 bytes) exclusive of preamble and start packet delimiter bits, will be received and placed in the local buffer. Packets shorter than 6 bytes (2 bytes if bit 8 = 1) will always be rejected unless the Receiver is in promiscuous mode (all addresses match) or multicast/broadcast mode and the packet is a multicast/broadcast packet. If the Short Frame Enable bit is set and the Rx Interrupt bit is also set, one Rx interrupt will occur in response to a short frame.

Bit 6: SlotSelect. This bit selects the slot time used to calculate backoff time following a collision. When a 0, which is the state after reset, the slot time is 512 bits and meets the IEEE 802.3 standard; when a 1, the slot time is 128 bits, the interframe spacing is 24 bits and the collision jam is 2 bytes long, which is useful for smaller networks such as serial backplane buses.

Bit 7: PreamSelect. When this bit is a 0, which is the state after reset, the CS8005 automatically transmits an IEEE 802.3 compatible 64 bit preamble; when set to 1, the user must supply the preamble as part of the packet data. The preamble must still follow the 802.3 form in order to be recognized by other CS8005's, but may have arbitrary length. Note that a minimum of 16 preamble bits are required by the CS8005 on reception.

Bit 8: AddrLength. This bit selects the length of address to be used in address matching. When a 0, which is the state after reset, the length is 6 bytes, which conforms with the IEEE 802.3 standard; when set to 1 the length is 2 bytes, which is useful in limited networks such as serial backplane buses.

Bit 9: RecCrc. If set to a 1, received packets will include the CRC. If set to a 0, which is the state after reset, the 4 byte CRC will be stripped when received.

Bit 10: XmitNoCrc. If set to a 1, the Transmitter will not append the 4 byte frame check sequence to each packet transmitted. This is useful in local loopback to perform diagnostic

checks, since it allows the software to provide its own CRC as the last four bytes of a packet to check the Receiver CRC logic. It is initialized to 0 after hardware or software reset.

Bit 11: Loopback. This bit controls the External Loopback pin. When set to a 1, the loopback output pin is at Vol; after reset or when cleared to a 0, the External Loopback output pin is at Voh.

Bit 12: CTRLO This bit controls the Control Output pin. When set to a 1, the CTRLO pin is at Voh; when cleared to 0 or after reset, this pin is at Vol.

Bits 13-14: Not used. Reserved for future use.

Bit 15: Reset. Writing a 1 to this bit is the same as asserting the hardware reset. Reset should be followed by a 4 µs wait before attempting another access. This bit reads as a 0.

Write Protect Pointer, A3-0 = 0110

Bits 0-7: WPP. The Write Protect Pointer contains the high order byte of the local buffer address at which the Receive logic must stop to prevent writing over previously received packets. If the Receive logic reaches this address it will stop; the Receiver will be turned off and an interrupt will be issued. The Receiver can be re-started by freeing up buffer space and turning the Receiver back 'ON' again. This register can be updated automatically by setting bit 1 in Configuration Register #2, which causes WPP to be updated each time the high byte of the DMA_Ptr is updated by the Buffer Controller during reads via the DMA FIFO. It is both read and write.

Buffer Window Register, A3-0 = 100X

This register provides access to the area specified by the Buffer Code bits (bits 0-3) in Configuration Register #1. When the Buffer Code points to either the buffer memory (Buffer Code =1000_2), or the address PROM (Buffer Code = 0110_2), the address of the data transferred through this register is determined by the DMA pointer. All Buffer Code registers are byte wide except data.

Receive Pointer Register, A3-0 = 101X

The Receive Pointer provides a 16 bit address that points to the next buffer memory location into which data or header information will be placed by the Receive logic. The low order 8 bits contain the least significant byte of the address. Prior to enabling the Receiver, this register should be set to point to the beginning of the Receive Area in the local buffer. This initial value should be remembered by system software since it will be the address of the first byte of the header block of the first packet received. While receiving, the Receive Pointer will be incremented for each byte stored into the local buffer. When the Receive Pointer increments past hex FFFF the most significant byte will be set equal to the value of the Transmit Buffer Limit + 1 and the least significant byte will be set to 00. Reading this register may be done at any time. It should be written only when the receiver is idle.

Transmit Pointer Register, A3-0 = 110X

The Transmit Pointer points to the current location being accessed by the Transmit logic. Before starting the Transmitter, software loads this register with the address of the beginning of a transmit packet chain.

DMA Address Register, A3-0 = 111X

The DMA address register provides 16 bits of address information to the local buffer memory and 8 bits of address to the address PROM, depending on the buffer code written into Configuration Register 1. Its normal use is to provide an auto-incremented address to the local buffer so that the packet data can be moved via the Bus Interface. When the DMA Address register is loaded, the DMA FIFO is cleared. Therefore it is important to ensure that the DMA FIFO is empty if it is in the write direction before loading the DMA register. When writing a packet to be transmitted,

the DMA Address register automatically wraps around to 0000 when the Transmit Buffer Limit (contained in an indirect register, Buffer Code 0111) has been reached. When reading receive packets, the DMA Address register automatically wraps around to the Receive Start Area (Transmit Buffer Limit + 1,00) when address hex FFFF has been read.

Indirectly Accessed Registers

Infrequently used registers, such as, those normally loaded only when initially configuring the CS8005, are accessed indirectly by first loading the Buffer Code bits in Configuration Register #1 with a code that points to the desired register. Reads and writes occur through the Buffer Window register. All indirect registers (a total of 38) are 8 bits wide, thus only D0-D7 are used.

Receive Address Registers

The CS8005 contains six 48-bit Receive Address registers, which permits one network connection to provide up to 6 different server functions. Each of these Receive Address registers is comprised of six 8-bit registers which must be loaded through the Buffer Window Register. Only those Receive Address registers to be enabled for address matching need to be loaded.

To load a Receive Address register, first turn the Receiver off. Select the desired address register number (0-5) by writing the Buffer Code bits in Configuration Register #1. Next do 6 sequential byte writes to the Buffer Window register as follows: Write the least significant byte of the 6 byte Receive Address; its low order bit, bit 0, will be the first bit received. Next write the remaining 5 bytes in ascending order. To read a Receive Address register, first turn the receiver off by setting bit 12, Rx off, on the Command register and verifying that the Receiver is off. Then select the desired station number by writing the Buffer Code bits in Configuration Register #1. Do 6 sequential reads to the Buffer Window Register; the first byte read will be the least significant byte. If the CS8005 is configured to match 2 byte instead of 6 byte addresses, only the first 2 station address bytes are significant, although all 6 will read and write properly.

Transmit Buffer Limit Pointer

The 8-bit value of this pointer defines, with 256 location granularity, the end of the Transmit Packet Buffer area by specifying the highest value permitted in the most significant byte of the Transmit Pointer Register and, when loading a packet to be transmitted, the DMA Address register. It also indirectly defines the Receive Start Area address, since the Buffer Controller automatically calculates the high order byte of the address by adding 1 to the Transmit Buffer Limit pointer. To read or write this value, set Buffer Code = 0111, and do a read or write to the Buffer Window Register.

Interrupt Vector Register

This Read/Write register is accessed through the Buffer Window register when the Buffer Code in Configuration Register #1 is 9. It contains an 8 bit vector which is placed on data bits D0-D7 during an Interrupt Acknowledge cycle. If BUSMODE = 0, an Interrupt Acknowledge cycle is defined by $\overline{INT}$ = 0, $\overline{IACK}$ = 0, and R/$\overline{W}$ = 1. When BUSMODE = 1, an Interrupt Acknowledge cycle is defined by INT = 1, $\overline{IACK}$ = 0, and $\overline{IOR}$ = 0.

Other Buffer Window Register Uses

Address PROM Access

The CS8005 supports access to up to 256 bytes of configuration data contained in a PROM or EEPROM. This can be used for any purpose, such as storing receive addresses, register configurations, network connection data, etc. The address to the PROM is supplied by the DMA register through data bus bits D8-D15; the data

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Example of Chained Receive Frames

Bit #	7	6	5	4	3	2	1	0	
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	0	0	0	0	0	0	0	0	Next receive packet header goes here.
Addr. ptr2	0	0	0	0	0	0	0	0	
Header status	0	0	0	0	0	0	0	0	Last header in chain.
Packet status	0	0	0	0	0	0	0	0	

Packet Header Bytes

Transmit Header Command Byte (Byte #3)

7	6	5	4	3	2	1	0
1	Chain Con-tinue	Data Fol-lows	Not Used	Xmit Success Enable	16 Coll. Enable	Coll. Int. Enable	Babble Int. Enable

Receive Header Status Byte (Byte #3)

7	6	5	4	3	2	1	0
0	Data Fol-lows	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

Transmit Packet Status Byte (Byte #4)

7	6	5	4	3	2	1	0
Done	←	Reserved		→	16 Coll.	Colli-sion	Bab-ble

Receive Packet Status Byte (Byte #4)

7	6	5	4	3	2	1	0
Done	Not Used	Not Used	Not Used	Short Frame	Drib. Error	CRC Error	Over-size

CS8005 Configuration and Pointer Registers

Command (write only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Write	FIFO Read	Set Tx Off	Set Rx Off	Set DMA Off	Set Tx On	Set Rx On	Set DMA On	Buffer Window Ack	Tx Int Ack	Rx Int Ack	DMA Int Ack	Buffer Window Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Status (read only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Dir	FIFO Empty	FIFO Full	Not Used	Not Used	Tx On	Rx On	DMA On	Buffer Window Int	Tx Int	Rx Int	DMA Int	Buffer Window Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Configuration Register #1 (A3-0 = 001X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addr Match Mode	Addr Match Mode	Sta. 5 Enable	Sta. 4 Enable	Sta. 3 Enable	Sta. 2 Enable	Sta. 1 Enable	Sta. 0 Enable	DMA Burst Size	DMA Burst Size	DMA Burst Intvl	DMA Burst Intvl	Buffer Code 3	Buffer Code 2	Buffer Code 1	Buffer Code 0

Configuration Register #2 (A3-0 = 010X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	Not Used	Not Used	Control Output	Loop-Back	Xmit No CRC	Recv. CRC	Addr Leng.	Xmit No Pream	Slot Time Sel.	Short Frame Enable	Drib. Error Enable	CRC Error Enable	Not Used	Auto Update REA	Byte Swap

Write Protect Pointer (A3-0 = 0110[2])

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	Write Protect Pointer							

Receive Pointer Register (A3-0 = 101X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT RECEIVE BYTE															

Transmit Pointer Register (A3-0 = 110X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT TRANSMIT BYTE															

DMA Address Register (A3-0 = 111X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR SYSTEM READS OR WRITES															

Buffer Window Register (A3-0 = 100X[2])

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFFER CODE BITS DETERMINE SOURCE/DESTINATION FOR READS AND WRITES															

Receive Address Register Format
2 of 6 Receive Address Registers Shown

7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE RECEIVE ADDRESS REGISTER 0 BYTE 0 BUFFER CODE = 0000							
RECEIVE ADDRESS REGISTER 0 BYTE 1 BUFFER CODE = 0000							
RECEIVE ADDRESS REGISTER 0 BYTE 2 BUFFER CODE = 0000							
RECEIVE ADDRESS REGISTER 0 BYTE 3 BUFFER CODE = 0000							
RECEIVE ADDRESS REGISTER 0 BYTE 4 BUFFER CODE = 0000							
RECEIVE ADDRESS REGISTER 0 BYTE 5 BUFFER CODE = 0000 MOST SIGNIFICANT BYTE							

7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE RECEIVE ADDRESS REGISTER 1 BYTE 0 BUFFER CODE = 0001							
RECEIVE ADDRESS REGISTER 1 BYTE 1 BUFFER CODE = 0001							
RECEIVE ADDRESS REGISTER 1 BYTE 2 BUFFER CODE = 0001							
RECEIVE ADDRESS REGISTER 1 BYTE 3 BUFFER CODE = 0001							
RECEIVE ADDRESS REGISTER 1 BYTE 4 BUFFER CODE = 0001							
RECEIVE ADDRESS REGISTER 1 BYTE 5 BUFFER CODE = 0001 MOST SIGNIFICANT BYTE							

lines from the PROM are connected to D0-D7. Chip select for the PROM is provided by output $\overline{\text{APEN}}$. Before accessing this PROM, ensure that Transmit, Receive and DMA sections of the CS8005 are disabled. Next load the PROM starting address which you wish to access into both the low byte and the high byte of DMA register. Set the Buffer Code bits in Configuration Register #1 to point to the address PROM. Each access to the Buffer Window register will chip enable the PROM, permitting reads. Successive accesses will increment the DMA register to point to the next byte in the PROM. If a 16 bit wide bus is used, the address supplied to the PROM will also be read on D8-D15.

Buffer Access

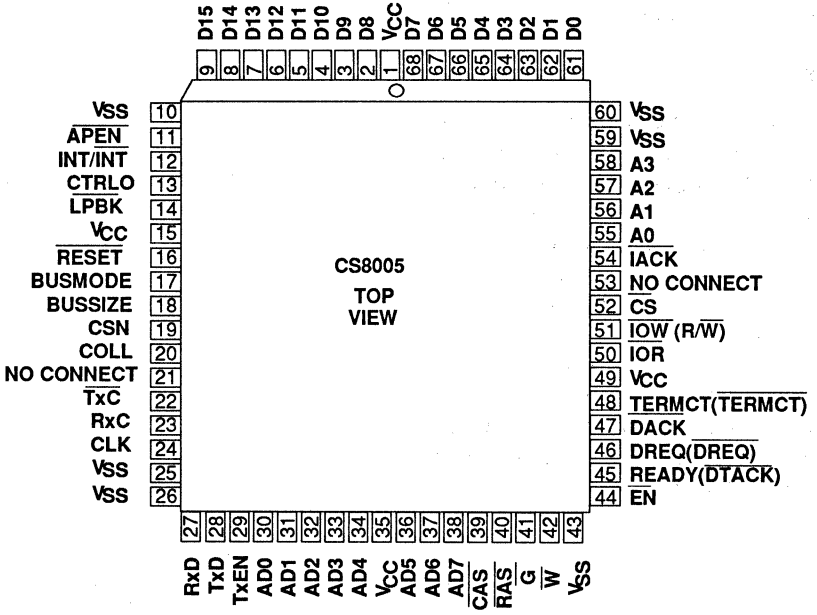
The normal state of the Buffer Code bits, once the CS8005 has been initialized with station addresses and buffer areas have been allocated, is with Packet Buffer selected. Access to the local packet buffer is provided by the DMA register, which automatically increments after each byte or word transfer. To write to the local buffer, set the buffer code to select the desired buffer destination, set the FIFO direction to write (Command Register bits 14 and 15), load a starting address into the DMA register and write to the Buffer Window register. To read from the local buffer, the same steps as above must be followed except that the FIFO direction should be changed to the read direction after the DMA register has been written. This is the simplest way to access the local buffer as it requires no system DMA activity. It also permits network layer software to read network control data at the beginning of a received packet to determine if it is necessary to move the packet into global memory for further processing or simply reuse the area occupied by the packet by updating the Write Protect Pointer. For fastest transfer speed, e.g., to move packet data, an exter-

nal system DMA Controller is supported via the DMA Request output, DMA Acknowledge input and Terminal Count input signals.

Asynchronous Bus Control

The CS8005 supports asynchronous bus control via the READY/$\overline{\text{DTACK}}$ pin. By using READY/$\overline{\text{DTACK}}$, the cycle time minimums listed in the tables A through J need not be observed. READY/$\overline{\text{DTACK}}$ takes care of these cycle times. This greatly simplifies the task of interfacing to the CS8005 and also results in a higher overall data rate. To acheive the highest possible data rate, all data transfers should terminate within 100 ns of READY/$\overline{\text{DTACK}}$ being asserted. This permits a sustained system bus transfer rate of 3.33 Mbytes/sec in 16 bit mode or 2.5 Mbytes/sec in 8 bit mode.

PIN DESCRIPTION



D0-D15, Pins 61-68, 2-9

A 16 bit bidirectional system data bus. If BUSSIZE = 0, the bus is configured as 8 bits and D8-D15 are not used for data transfer. Byte order for local buffer data transfers on a 16 bit bus is software configured. D8-D15 are used to provide address information to the optional external address PROM in both 8 and 16 bit modes.

$\overline{EN}$, Pin 44

An output which can be used to control the three-state control pin of external bi-directional drivers such as the 74LS245.

$\overline{APEN}$, Pin 11

Active low address PROM enable output.

$\overline{IOW}$(R/$\overline{W}$), Pin 51

If BUSMODE = 1, this input defines the current bus cycle as a write. If BUSMODE = 0, this input defines the bus cycle as a read if a 1 or a write if a 0.

$\overline{IOR}$ ($\overline{LDS}$*), Pin 50

If BUSMODE = 1, this input defines the current bus cycle as a read. If BUSMODE = 0, this input is not used.

*$\overline{LDS}$ is not currently implemented. Future versions of the CS8005 will implement the $\overline{LDS}$ function on this pin when in Motorola compatible mode.

$\overline{CS}$, Pin 52

The chip select input, used to access internal registers and the packet buffer.

A0-A3, Pins 55-58

Address select inputs used to select internal registers for reading or writing. A0 is not used in 16-bit mode.

$\overline{DACK}$, Pin 47

An input used to acknowledge granting of the system bus for external DMA transfers. When DREQ is active, $\overline{DACK}$ functions as a chip select for reads and writes.

DREQ ($\overline{DREQ}$), Pin 46

An output to an external DMA controller used to signal that a DMA request is being made. This signal is high active when BUSMODE = 1, low active when BUSMODE = 0. A three-state output.

TERMCT ($\overline{TERMCT}$), Pin 48

An input which signals that the last byte or word of a DMA access is on the bus. When BUSMODE = 1, this input is high active; when BUSMODE = 0, it is low active.

READY ($\overline{DTACK}$), Pin 45

A three-state output. When BUSMODE = 1, this output functions as a READY pin (Intel compatible); when BUSMODE = 0, this output is $\overline{DTACK}$ (Motorola compatible).

INT/($\overline{INT}$), Pin 12

When BUSMODE = 1, this is a high active interrupt output; when BUSMODE = 0 this output is low active.

$\overline{IACK}$, Pin 54

Active low interrupt acknowledge input. When this input is asserted and INT is also asserted, the contents of the Interrupt Vector register are placed on D0-D7.

$\overline{RESET}$, Pin 16

The low active reset input. Asserting $\overline{RESET}$ clears all configuration and pointer to 00. Following reset, a wait of 4 µs is necessary before accessing the part.

BUSMODE, Pin 17

An input which selects Intel-compatible bus signals when high or Motorola-compatible bus signals when low.

BUSSIZE, Pin 18

An input that selects the 8-bit system bus when low or 16-bit system bus when high.

AD0-AD7, Pins 30-34, 36-38

A multiplexed address and data bus used to provide row and column address and read/write data to the packet buffer dynamic RAM.

$\overline{RAS}$, Pin 40

Row Address Strobe to the packet buffer memory.

$\overline{CAS}$, Pin 39

Column Address Strobe to the packet buffer memory. Page mode addressing is used when possible to speed access to the buffer.

$\overline{W}$, Pin 42

An output to the dynamic RAM buffer that indicates the current cycle is a write.

$\overline{G}$, Pin 41

An output to the dynamic RAM buffer that enables read data onto the AD bus.

TxEN, Pin 29

An output to the Manchester Code Converter that indicates a transmission is in progress.

$\overline{TxC}$, Pin 22

An input from the Manchester Code Converter that is used to synchronize transmitted data.

TxD, Pin 28

The transmit data output to the Manchester Code Converter.

RxC, Pin 23

An input from the Manchester Code Converter used to synchronize received data.

RxD, Pin 27

The receive data input from the Manchester Code Converter.

COLL, Pin 20

The collision input from the Manchester Code Converter.

CSN, Pin 19

The carrier sense input from the Manchester Code Converter.

CTRLO, Pin 13

Control/Output, a general purpose control pin, level follows bit 12 of Configuration Register #2.

$\overline{LPBK}$, Pin 14

The loopback control output.

CLK, Pin 24

The master 20 MHz input clock.

No Connect, Pins 21 & 53*

*Future versions of the CS8005 will use pin 53 to implement Byte High Enable ($\overline{BHE}$) for Intel mode or Upper Data Strobe ($\overline{UDS}$) for Motorola mode. Setting this pin high or low on the current CS8005 will not affect the CS8005 and will allow systems to be adapted to use the feature, when it is available.

APPLICATIONS

Transmit Packet Chaining

Bits 5 (Data Follows) and 6 (Chain Continue) of the Transmit Command Byte control transmit chaining as described in the Transmit Packet Format section. Here is some additional information regarding the functionality of these bits and a description on how to add to a packet chain while the transmitter is transmitting.

- Note that the "Skip Header" can be used to relocate the Transmit Pointer to the beginning of another packet chain.

- Note that the Chain Continue bit (bit 6) of the last packet in a chain can be used to terminate a packet chain. Alternatively, placing a Null Header following the last packet of a chain can also be used to terminate the chain.

To add to a packet chain while the Transmitter is transmitting the chain, the following procedure is recommended:

A. Set Chain Continue = 1 and Data Follows = 1 on all packet headers that have data to transmit.

B. Before starting the Transmitter, write a Null Header (4 bytes of zeros) immediately following the last packet in the chain.

C. Start the transmitter.

D. To add packet(s) to the chain:
   1. Write the next packet data immediately following the Null Header.
   2. Optional: Write one or more complete packets with complete headers following the one in step 1.
   3. Write another Null Header following the new packet(s).
   4. (Last) Over-write the first Null Header with the correct header data for the packet.

   If the Transmitter catches up with you, it will stop at the first Null Header and, if Tx Int Enable is 1, will generate an interrupt. It will not "de-rail" or mis-read a header if the headers are written in natural order.

Receive Packet Chaining

The Receiver writes a Null Header (four bytes of zeros) into the Receive Packet Buffer to start the reception procedure. If the system processor reads a Null Header, it should interpret it as the end of the packet chain, and should discontinue reading packets. When the packet is received, the Receiver returns to the Null Header and over-writes the header with the new packet information (the next packet pointer and status information). If Rx Int Enable = 1, the Receiver will interrupt the processor when another packet arrives, so that the processor can resume reading received packets. If interrupts are not used, the processor must poll the Rx Int status bit to learn when another packet has arrived. See item 1 under "Hints for Programmers," below.

Detecting 2-Byte Broadcast Address

The CS8005 will not detect Broadcast Address (Configuration Register 1, bits 15 & 14 = 0 1 (binary) in the 2-byte address mode (Configuration Register 2, bit 8 = 1) unless an additional Receive Address Register is Enabled. This additional address value must be "FF, FF, FF, FF, FF, FF" (hex).

Extra Byte at End of Packet Error

An extra byte at the end of the packet data field will occur if the packet has 7 dribble bits. this appended byte is the first byte of the CRC Field. In most LAN environments, this will not be a problem because 7 dribble bits will not occur on an otherwise good packet. (Dribble bits usually indicate a collision or an aborted transmission attempt). However, if a workaround is needed, the following methods can be used.

Detection Methods

- Comparing the Length Field value with the actual length of the packet. A length value can be detected as a numerical value less than or equal to 1500 (decimal), 05DC (hexadecimal). Values greater than that are type codes. (Note that some protocols in use on Ethernet systems do not code the Length Field for length, but instead use it for packet type. For such systems this detection method is invalid.)

- In a system which always transfers an even number of bytes, an odd byte count will indicate this error.

- Other error-detection schemes, where included in the higher levels of the protocol stack, may be used.

Correction Procedures

Either of the following methods will suffice:

- Set the Receive CRC Bit, bit #9 of Configuration Register #2. This will cause the CS8005 to include the CRC Field when storing the packet in the Local Buffer. If a byte count error is not detected, further processing of the packet must include stripping off four bytes from the end of the packet. If an extra byte is detected, strip off five bytes.

- Discard the packet and request a retransmission.

Hints for Programmers

Avoiding Multiple Null Headers in the Receive Buffer

When the receiver is turned on, it writes a null header at the current location of the Receive Pointer. The null header consists of four bytes of all zeros which indicates that no additional packets are available in local buffer. When the next packet is received, the null header is updated with the Next Packet Pointer and Status information for the new packet. The Next Packet Pointer is also the current location of the Receive Pointer. If the receiver is turned off either under software control or by the occurance of a receive buffer overflow, it will terminate operations only after writing a null header. (In the case of the buffer overflow, a partial null header will be written if there is not enough space for a full null header, but at least one byte of zeros will be written in all cases. If the last byte of a full null header is written in the last available byte of a local buffer, an overflow will be indicated). If the receiver is turned back on, it writes an additional null header after the first. This disrupts the relationship between the Next Packet and the Receive Pointers. If the Receive Pointer is not corrected, a null header (or partial null header) will remain in the local buffer and in the case of an overflow, information which has not yet been read will be overwritten. This problem is avoided as follows: *Before turning the receiver on under any circumstances, start by loading the Receive Pointer (to the previous header's Next Packet Pointer, for example), then turn the receiver on.*

Partial Null Headers

Normally, the null header written at the end of a receive packet consists of four bytes at 00 (hex). However, an overflow condition may leave insufficient memory space to write a complete null header. The CS8005 will write a partial null header, but in all cases, at least one byte of 00 (hex) will be written, and the packet's header will be updated. When reading receive packets, if the first byte of a header reads as 00 (hex), stop. That is sufficient to indicate that there are no more receive packets available since 00XX cannot be an address in the receive buffer (the transmit buffer must be at least 256 bytes).

Resetting DMA Pointer After Encountering a Null Header

When a null header is encountered during a memory read, the DMA FIFO will contain 1 to 16 bytes of old data. When a new packet arrives, the null header and following buffer space are overwritten with new information. The DMA FIFO must be reloaded with the correct data. To clear the FIFO and load the current contents of the local buffer, set the DMA Pointer to the starting address of the newly arrived data. This starting address is the Next Packet Pointer of the previous header which should be stored in system memory to serve this purpose.

Reading the Transmit Buffer

In the Read Mode, the DMA Pointer will not wrap around in the Transmit Buffer. Pointer wrap around must be implemented in software. Otherwise, after reading data at the highest address within the Transmit Buffer, the DMA Pointer will exit the Transmit Buffer entering the Receive Buffer at its lowest address. In the write mode, the pointer wraps around automatically.

Reading the Buffer

Each time the FIFO Read bit is to be set (Command Register, bit 14), or the DMA Pointer is to be loaded with a new value, the following proceedure must be used.

1) Buffer Code (Configuration Register #2, bits 3-0) should be set to "8" (Local Buffer).

2) FIFO Direction (Comand Register, bit 15) should be set to "WRITE."

3) If the FIFO is not empty, wait until the write to the buffer is complete.

4) If FIFO EMPTY (Status Register, bit 14 = 1), load the new value to the DMA Pointer (if necessary).

5) Set FIFO Direction to "READ" (Command Register, bit 15 = 1).

6) Wait for Buffer Window interrupt (indicates data in the FIFO is ready).

7) Read the data.

A faulty buffer read can occur for either of the following circumstances:

1) - BUSSIZE = 1 (16-Bit mode)
   - Buffer Code not equal to "8"
   - FIFO Read bit set to "1" or DMA Pointer updated while FIFO direction is READ
2) - BUSSIZE = 0 (8-bit mode)
   - DMA Pointer is updated while FIFO direction is READ.

Semiconductor Corporation

CS8023A

Manchester Code Converter

Features

- Compliant with ISO/IEEE 802.3 and Ethernet Rev. 1
- Works with the CS8005 and Intel 82586 LAN Controllers.
- Manchester Data Encoding/Decoding and Receiver Clock Recovery
- Loopback Capability for Diagnostics and Isolation
- Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission.
- Transceiver Interface High Voltage (16V) Short Circuit Protection
- Low Power CMOS Technology with Single 5V Supply.

General Description

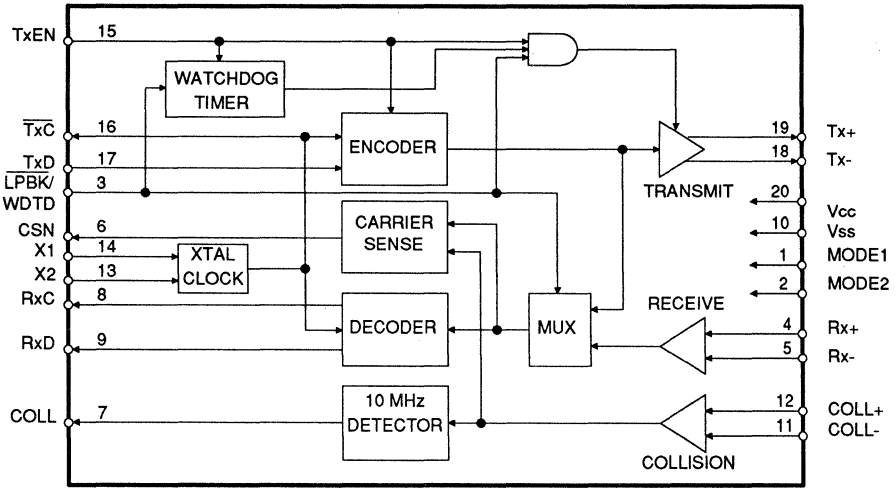
The CS8023A Manchester Code Converter provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the CS8005 CSMA/CD Data Link Controller or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The CS8023A is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the CS8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

Together with the CS8005 and CS83C92C, the CS8023A provides a high performance minimum cost interface for any system to Ethernet.

ORDERING INFORMATION:

	Plastic DIP
CS8023A-P	20-Pin
CS8023A-L	20-Pin PLCC



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Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

Absolute Maximum Ratings*

Parameter	Min	Max	Units
Storage Temperature	-65	+150	°C
All Input and Output Voltage	-0.3	V_{CC}+0.3	V
V_{CC}	-0.3	7	V
(Rx±,Tx±, COLL ±) High Voltage Short Circuit Immunity	-0.3	16	V

*Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DC Characteristics (T_A = 0°C to 150°C; V_{CC} = 5V ±10%)

Parameter		Symbol	Min	Max	Units
Input Leakage Current (except MODE1, MODE2 Receive and Collision Pairs)	(0 ≤ V_{IN} ≤ V_{CC})	I_{IL}	-	10	µA
MODE1 Input Leakage Current	(0 ≤ V_{IN} ≤ V_{CC})	I_{IL}	-	200	µA
Receive and Collision Pairs (Rx±, COLL ±) Input Leakage Current	(V_{IN} = 0)	I_{IL}	-	2	mA
V_{CC} Current	(All Inputs, Outputs Open)	I_{CC}	-	75	mA
TTL Input Low Voltage		V_{IL}	-0.3	0.8	V
TTL Input High Voltage X1 Input High Voltage	(except X1)	V_{IH} V_{IH}	2.0 3.5	V_{CC} + 0.3 V_{CC} + 0.3	V V
TTL Output Low Voltage except $\overline{TxC}$	(I_{OL} = 2.1 mA)	V_{OL}	-	0.4	V
$\overline{TxC}$ Output Low Voltage	(I_{OL} = 4.2 mA)	V_{OL}	-	0.4	V
TTL Output High Voltage (except RxC, $\overline{TxC}$, RxD) RxC, $\overline{TxC}$, RxD Output High Voltage	(t_{OH} = -400 µA) (t_{OH} = -400 µA)	V_{OH} V_{OH}	2.4 -	- 3.9	V V
Differential Output Swing	(78Ω Termination Resistor and 243Ω Load Resistors)	V_{ODF}	±0.55	±1.2	V
Common Mode Output Voltage	(78Ω Termination Resistor and 243Ω Load Resistors)	V_{OCM}	V_{CC} - 2.5	V_{CC} - 1	V
Tx± Backswing Voltage During Idle (Shunt Inductive Load ≤ 27 µH)		V_{BKSV}	-	0.1	V
Input Differential Voltage	(measured differentially)	V_{IDF}	±0.3	±1.2	V
Input Common Mode Voltage		V_{ICM}	0	V_{CC}	V
Input Capacitance	(Note 1)	C_{IN}	-	15	pF
Output Capacitance	(Note 1)	C_{OUT}	-	15	pF

Note: 1. Characterized. Not tested

Specifications are subject to change without notice.

A.C. Test Conditions

Output Loading TTL Output	1 TTL gate and 20 pF capacitor
Differential Output	243Ω resistor and 10 pF capacitor from each pin to Vss and a termination 78Ω resistor load resistor in parallel with a 27 µH inductor between the two differential output pins
Differential Signal Delay Time Reference Level	50% point of swing
Differential Output Rise and Fall Time	20% to 80% points
RxC, $\overline{TxC}$, X1 High and Low Time	High time measured at 3.0V Low time measured at 0.6V
RxD, RxC, $\overline{TxC}$, X1 Rise and Fall Time	Measured between 0.6V and 3.0V points
TTL Input Voltage (except X1)	0.8V to 2.0V with 10ns rise and fall time
X1 Input Voltage	0.8V to 3.5V with 5ns rise and fall time
Differential Input Voltage	At least ±300mV with rise and fall time of 10ns measured between -0.2V and +0.2V

20 MHz TTL Clock Input Timing (T_A=0 °C to 70 °C; V_{CC}=5V±10%)

Parameter	Symbol	Min	Max	Units
X1 Cycle Time	t_1	49.995	50.005	ns
X1 High Time	t_2	15	-	ns
X1 Low Time	t_3	15	-	ns
X1 Rise Time	t_4	-	5	ns
X1 Fall Time	t_5	-	5	ns
X1 to $\overline{TxC}$ Delay Time	t_{5A}	10	45	ns

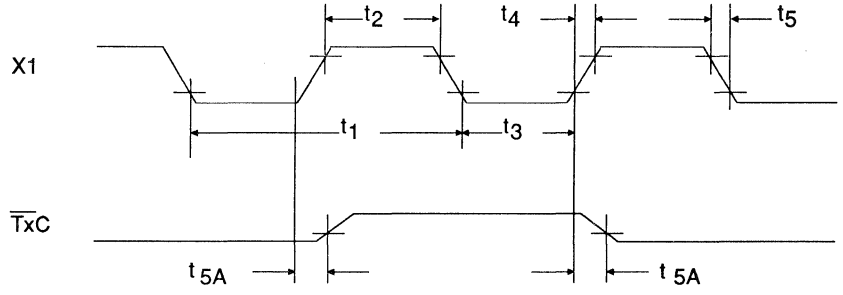


Figure 1. 20 MHz TTL Clock Timing

Transmit Timing (T_A = 0°C to 70°C; V_{CC} = 5V±10%)

Parameter		Symbol	Min	Max	Units
$\overline{TxC}$ Cycle Time	(Note 2)	t_6	99.99	100.01	ns
$\overline{TxC}$ High Time		t_7	40	-	ns
$\overline{TxC}$ Low Time		t_8	40	-	ns
$\overline{TxC}$ Rise Time	(Note 2)	t_9	-	5	ns
$\overline{TxC}$ Fall Time	(Note 2)	t_{10}	-	5	ns
TxEN Setup Time if Mode 2=0 TxEN Setup Time if Mode 2=1		t_{11}	40 55	- -	ns ns
TxD Setup Time if Mode 2=0 TxD Setup Time if Mode 2=1		t_{12}	40 55	- -	ns ns
Bit Center to Bit Center Time	(Note 2)	t_{13}	99.5	100.5	ns
Bit Center to Bit Boundary Time	(Note 2)	t_{14}	49.5	50.5	ns
Tx+ and Tx - Rise Time	(Note 2)	t_{15}	-	5	ns
Tx+ and Tx - Fall Time	(Note 2)	t_{16}	-	5	ns
Transmit Active Time From The Last Positive Transition		t_{17}	200	-	ns
From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 100 mV of 0 V	(Note 2)	t_{17A}	400	600	ns
From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 40 mV of 0 V	(Note 2)	t_{17B}	-	7000	ns
Tx+ and Tx- Output Delay Time		t_{18}	-	70	ns
TxD Hold Time if Mode 2=0 TxD Hold Time if Mode 2=1		t_{19}	15 0	- -	ns ns
TxEN Hold Time if Mode 2=0 TxEN Hold Time if Mode 2=1		t_{20}	15 0	- -	ns ns

NOTE: 2. Characterized. Not tested.

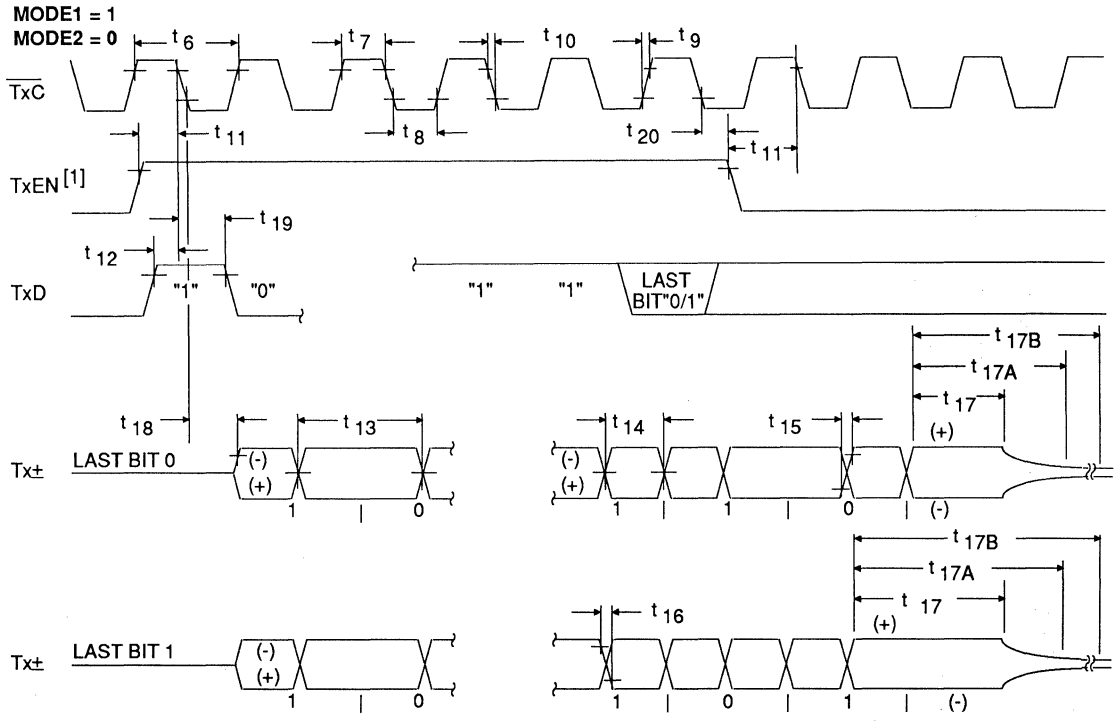
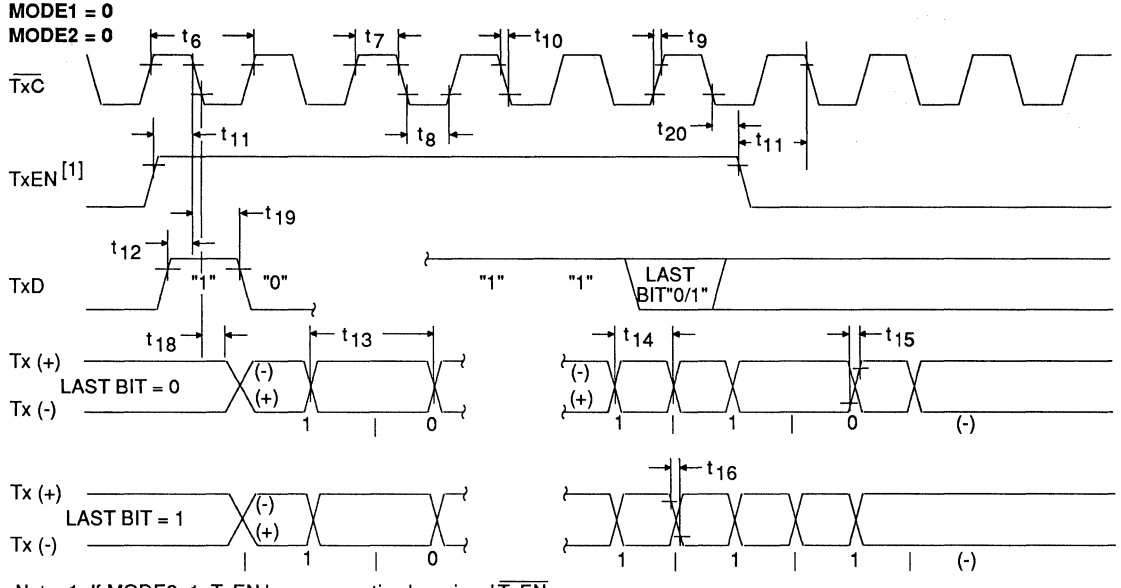


Figure 2. Transmit Timing

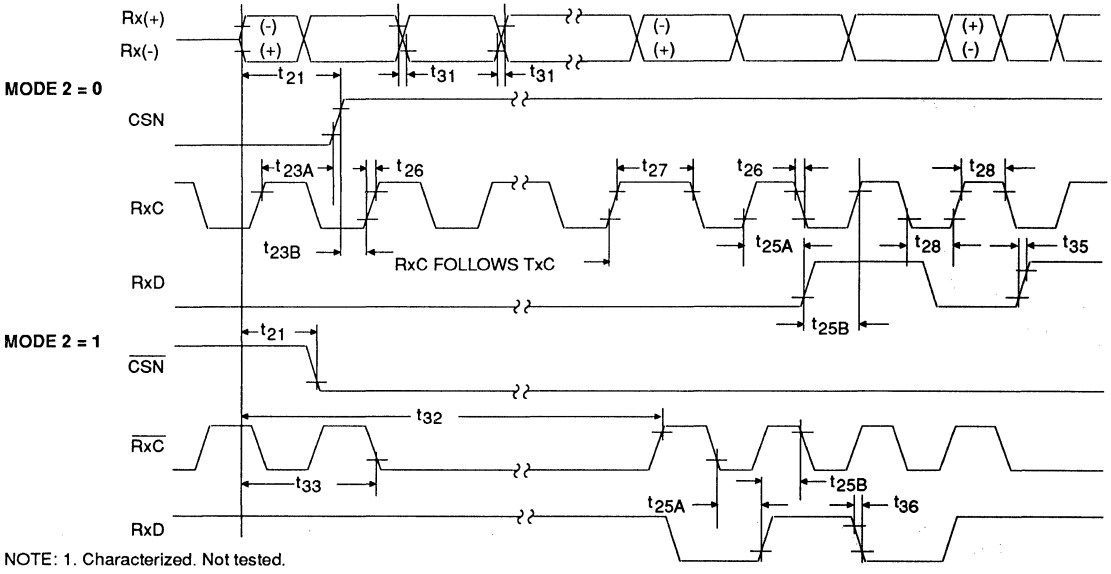


Note: 1. If MODE2=1, TxEN becomes active low signal $\overline{\text{TxEN}}$

Figure 3. Transmit Timing

Receive Timing (T_A = 0°C to 70°C; V_{CC} = 5V±10%)

Parameter	Symbol	Min	Max	Units
$\overline{CSN}$ Assert Delay Time	t_{21}	-	240	ns
$\overline{CSN}$ Deasserts Delay Time (measured from Last Bit Boundary)	t_{22}	-	240	ns
$\overline{CSN}$ Hold Time	t_{23A}	30	-	ns
$\overline{CSN}$ Set up Time	t_{23B}	30	-	ns
$\overline{CSN}$ Deassertion Delay Time	t_{24}	10	35	ns
RxD Hold Time	t_{25A}	30	-	ns
RxD Set up Time	t_{25B}	30	-	ns
RxC, $\overline{RxC}$ Rise and Fall Time (Note 2)	t_{26}	-	5	ns
During Clock Switch RxC Keeps High, $\overline{RxC}$ Keeps Low Time (Note 2)	t_{27}	40	200	ns
RxC, $\overline{RxC}$ High and Low Time	t_{28}	40	-	ns
RxC, $\overline{RxC}$ Clock Cycle Time (during) Data Period (Note 2)	t_{29}	95	105	ns
CSN Inhibit Time (on Transmission Node only)	t_{30}	4.3	4.6	µs
Rx+/Rx– Rise and Fall Time	t_{31}	-	10	ns
$\overline{RxC}$ Held Low Duration from First Valid Negative-Going Transition (Note 2)	t_{32}	1.15	1.35	µs
RxC Stops Delay Time from First Valid Negative-Going Transition	t_{33}	-	240	ns
Rx+/Rx– Begin Return to Zero from Last Positive-Going Transition (Note 2)	t_{34}	160	-	ns
RxD Rise Time (Note 2)	t_{35}	-	10	ns
RxD Fall Time (Note 2)	t_{36}	-	10	ns



NOTE: 1. Characterized. Not tested.

Figure 4. Receive Timing – Start of Packet

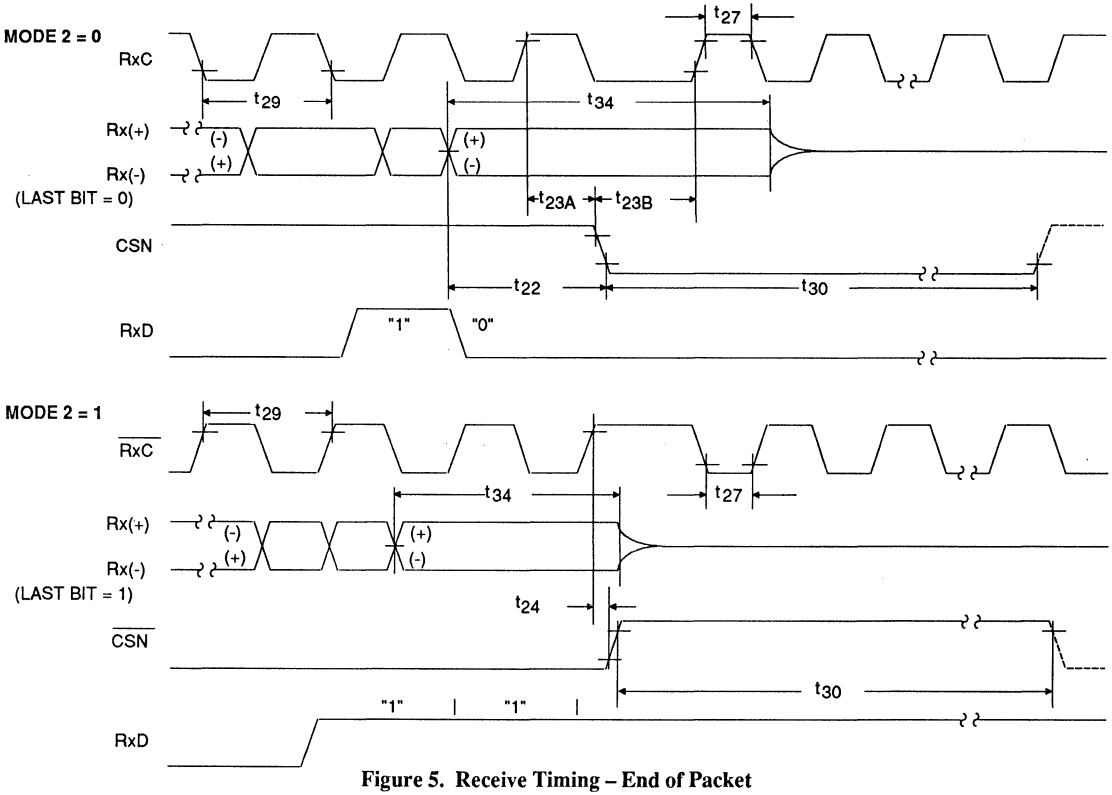


Figure 5. Receive Timing – End of Packet

Collision Timing (T_A=0 °C to 70°C; V_{CC}=5V ±10%)

Parameter	Symbol	Min	Max	Units
COLL+ /COLL- Cycle Time	t_{51}	86	118	ns
COLL+/COLL- Rise and Fall Time	t_{52}	-	10	ns
COLL+/COLL- High and Low Time	t_{53}	35	70	ns
COLL+/COLL- Width (measured at -0.3 V)	t_{54}	26	-	ns
COLL Asserts Delay Time	t_{55}	-	300	ns
COLL Deasserts Delay Time	t_{56}	-	500	ns
CSN Asserts Delay Time	t_{57}	-	400	ns
CSN Deasserts Delay Time	t_{58}	-	600	ns

Notes:
3. COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
4. If COLL+ and COLL - arrives within 4.5µs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
5. When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active.
6. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 µs.
7. If MODE 2=1, then COLL and CSN are inverted.

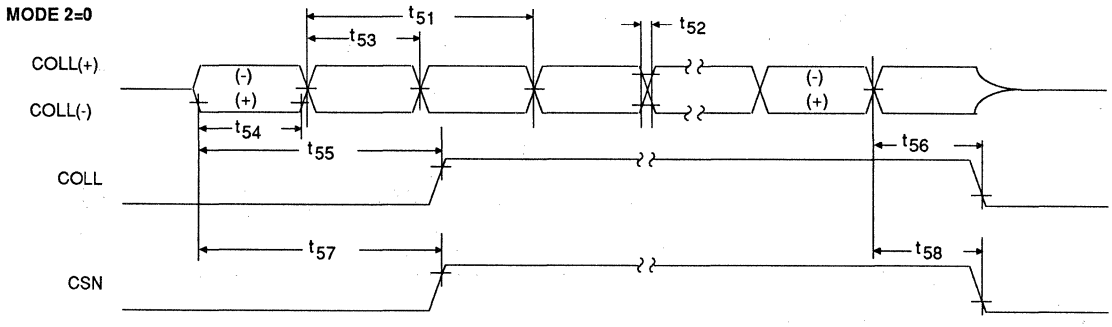


Figure 6. Collision Timing

Loopback Timing (T_A=0°C to 70°C; V_{CC}=5V±10%)

Parameter	Symbol	Min	Max	Units
LPBK Setup Time	t_{61}	500	-	ns
LPBK Hold TIme	t_{62}	5	-	µs
In Collision Simulation, COLL Signal Delay Time	t_{63}	475	625	ns
COLL Duration Time	t_{64}	600	750	ns

Note: 8. PLL needs 12-bit cell times to aquire lock, RxD is invalid during this period. RxC is low for 1.35 µs (max) if MODE2 = 1. RxD = 0 if MODE2 = 0. RxD = 1 if MODE2 = 1.

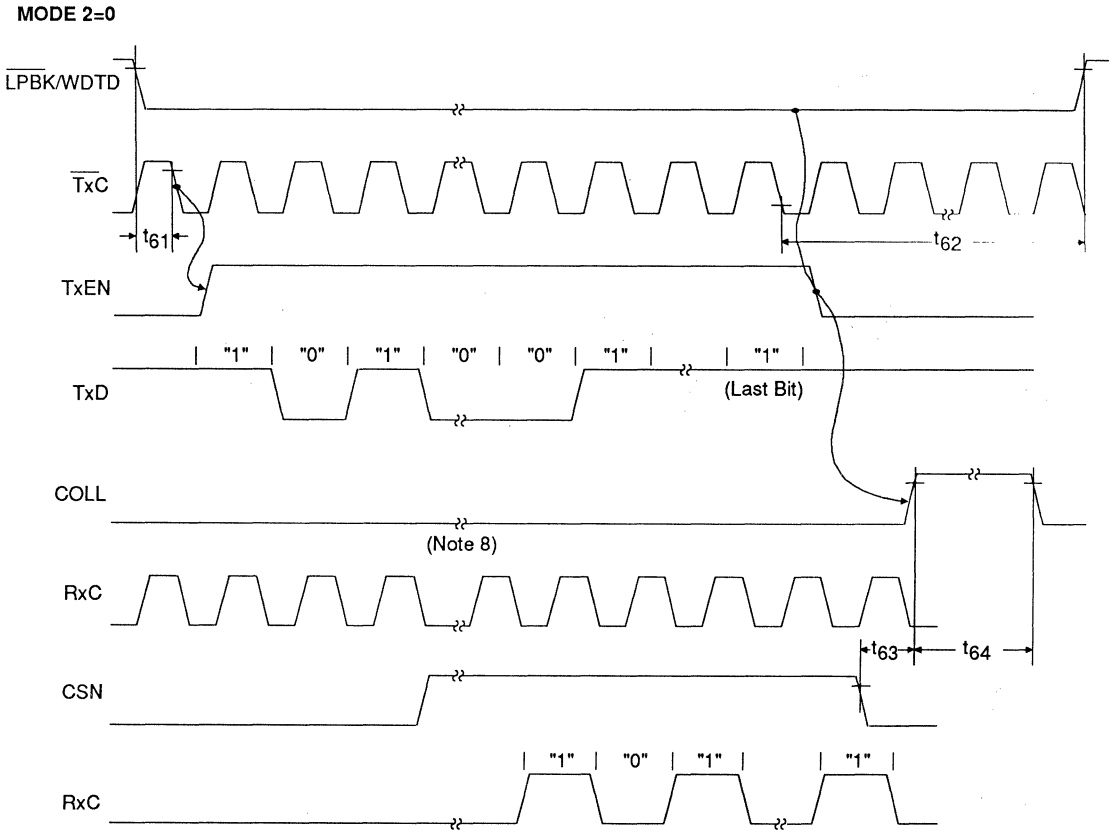


Figure 7. Loopback Timing

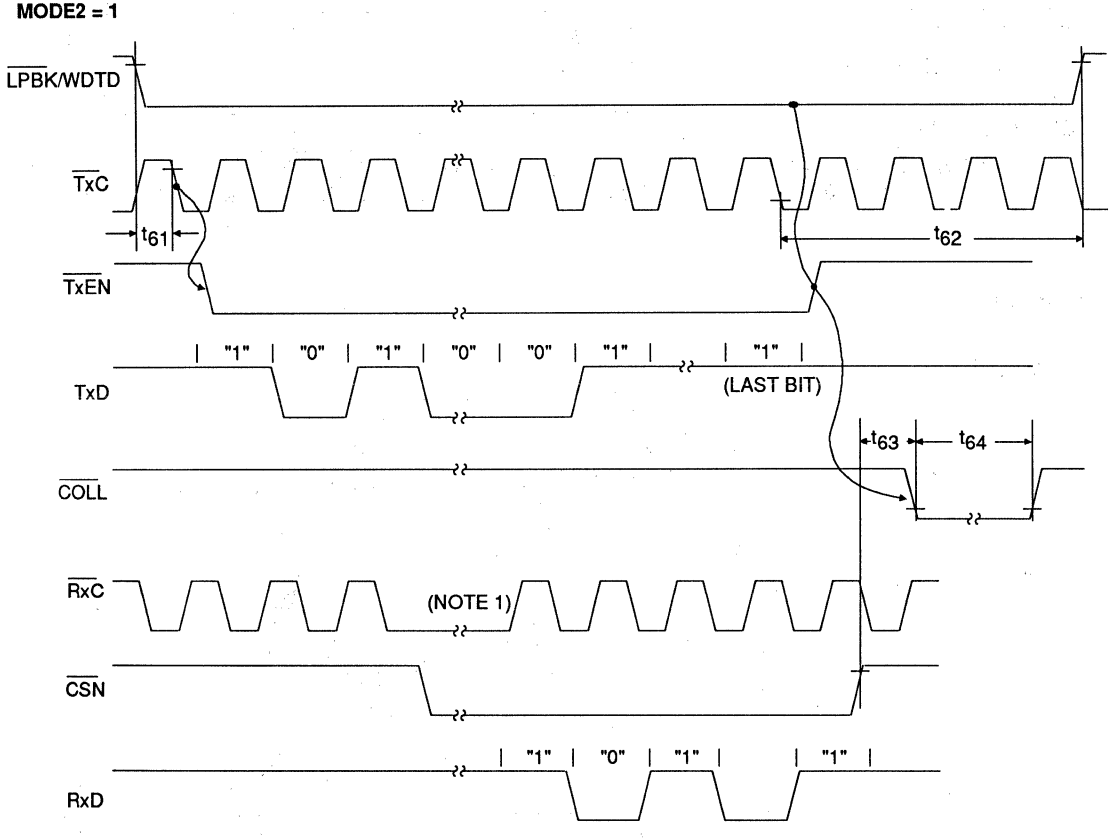


Figure 8. Loopback Timing – (Cont.)

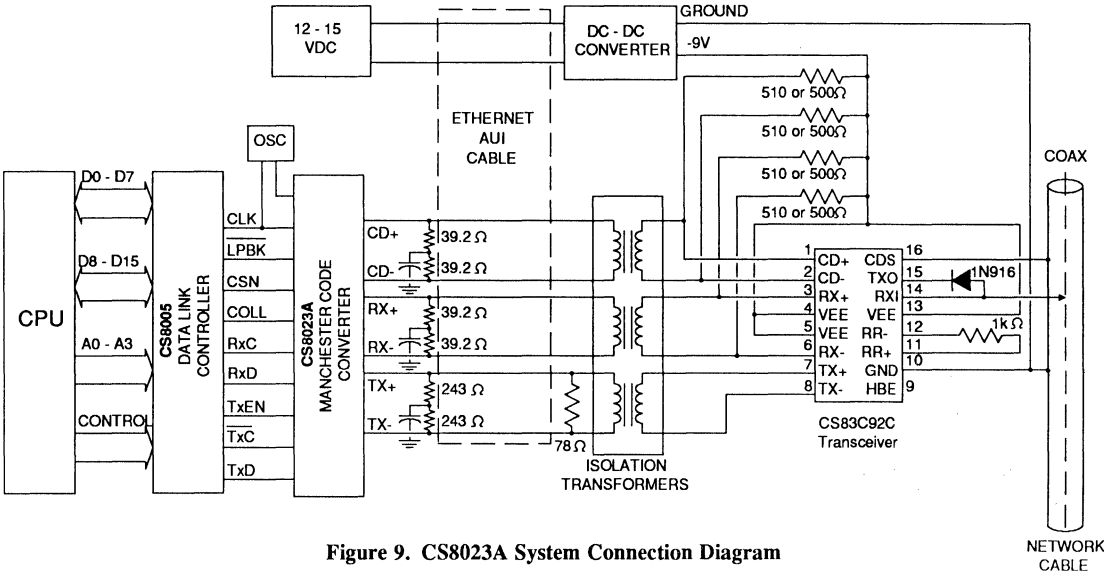


Figure 9. CS8023A System Connection Diagram

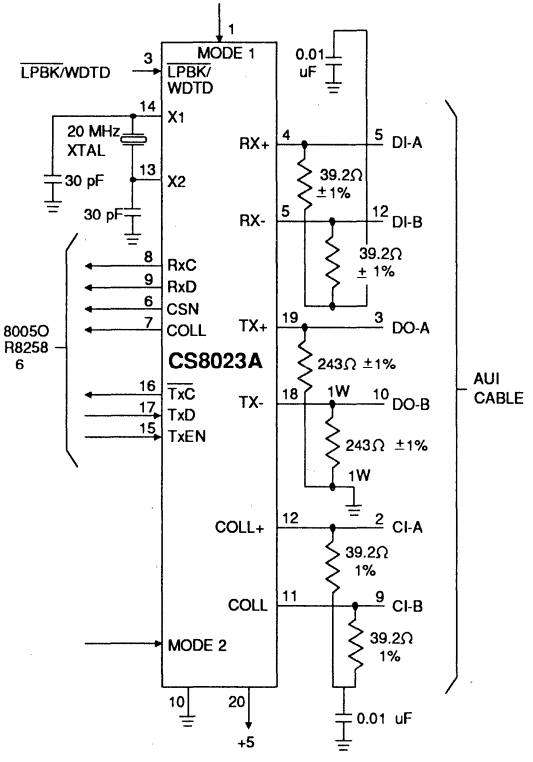


Figure 10. CS8023A Interface

Functional Description

The CS8023A Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The CS8023A recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1", and a negative going transition for a "0" (See Figure 11). The encoding is accomplished by exclusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

Clock Generator

The Internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz ±0.01% transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complement of the data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

Data encoding and transmission begin with TxEN going active; the first transition is always positive for TX- and negative for TX+. In IEEE mode, at the termination of a transmission, TxEN goes inactive and transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and the transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero. To eliminate DC current in the transformer during idle, Tx± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than 0.1 V.

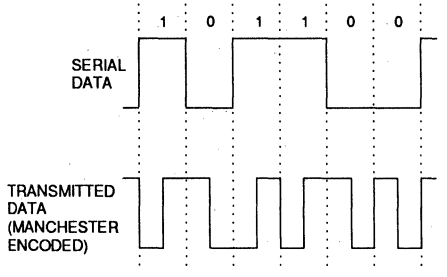


Figure 11. Manchester Coding

Watchdog timer

A 25 ms watchdog timer is built on chip. It can be enabled or disabled by the $\overline{\text{LPBK}}$/WDTD signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

Differential Input Circuit (Rx+ and Rx-, COLL+ and COLL-)

As shown in Figure 12, the differential input for Rx+ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2Ω ±1% resistors in series for proper impedance matching.

The center tap has a 0.01 µF capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signals less than -140 mV in amplitude or narrower than 15ns (10 ns for collision pair) are always rejected, signals greater than -300 mV and wider than 30 ns (18 ns for collision pair) are always accepted.

Manchester Decoder and Clock Recovery Circuit

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition

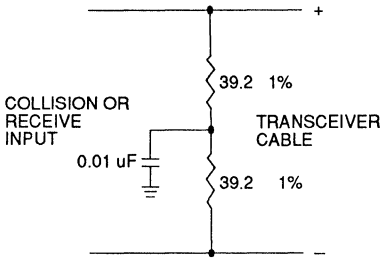


Figure 12. Differential Input Terminator

width asymmetry not greater than +8.25ns to -25ns within 12 bit cell times worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to -8.25 ns. The RxC high or low time will always be greater than 40 ns. If MODE2 is high or floating, RxC will be held low for 1.2 µs maximum while the PLL is acquiring lock. If MODE2 is low, RxC follows $\overline{TxC}$ for the first 1.2 µs and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of the frame, after the node has finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5 µs regardless of the state of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhibit period after packet reception. During clock switching, $\overline{RxC}$ may stay high for 200ns maximum.

Collision Circuit

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz ±15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with RxC. However, if a collision arrives during inhibit period 4.5 µs from the time CSN was deasserted, CSN will not be reasserted.

Loopback

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except the differential output driver and the differential input receiver circuits which are disabled during loopback. At the end of frame transmission, the CS8023A also generates a 650 ns long COLL signal 550 ns after CSN was deasserted to simulate the IEEE 802.3 SQE test. The watchdog timer remains enabled in this mode.

Compatibility with Other LAN Controllers

Crystal's CS8023A is compatible with other LAN Controllers, such as the 82586, when Pin 2 (MODE2) of the CS8023A is floating or tied to V_{CC}. In this mode of operation, timing and polarity on the controller interface lines are compatible, with the 82586 specifications dated March 1984.

Use of Time Domain Reflectometry in the 82586 is not recommended since the TDR transmission does not have a valid preamble.

Crystal Specification

Resonant Frequency (CL = 20 pF) . . . 20 MHz
±0.005% 0-70 °C
and ±0.003% at 25 °C
Type . . . . . Fundamental Mode
Circuit . . . . . Parallel Resonance
Load Capacitance (CL) 20pF
Shunt Capacitance (CO) . . . . . 7pF Max.
Equivalent Series Resistance (R1) . . 25Ω Max.
Motional Capacitance (C1) . . . . .0.02 pF Max
Drive Level 2mW

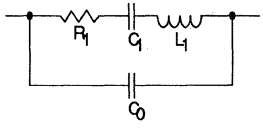
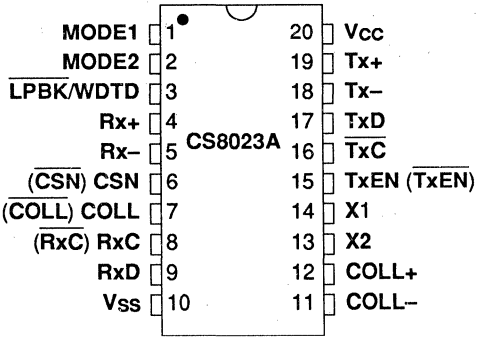
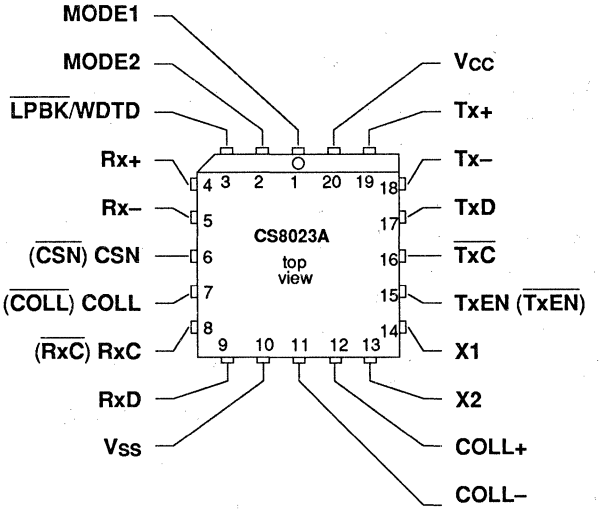


Figure 13. Equivalent circuit of crystal

Pin Descriptions





Power Supply and Clock

VCC - Power Supply, Pin 20

+5V

VSS - Ground, Pin 10

Ground reference

X1 and X2 clock (Inputs), Pins 14 and 13

Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.

Controller Interface

RxC ($\overline{RxC}$) - Receive Clock (Output), Pin 8

This signal is the 10 MHz (nominal) recovered clock from the phase decoder circuit. It is switched to $\overline{TxC}$ when no incoming data is present from which a true receive clock is derived. RxC is MOS and TTL compatible. If the MODE2 signal is high, RxC is inverted ($\overline{RxC}$) and there is a 1.25 µsec discontinuity at the beginning of frame reception.

RxD - Receive Data (Output), Pin 9

The RxD signal is the recovered data from the phase decoder. During idle periods, the RxD pin is LOW under normal conditions. However, if the MODE2 signal is HIGH, the RxD output will be HIGH during idle. RxD is TTL and MOS level compatible. RxD is active HIGH.

CSN ($\overline{CSN}$) - Carrier Sense (Output), Pin 6

The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with RxC. TTL compatible. CSN is normally active HIGH, unless MODE2 is HIGH, in which case $\overline{CSN}$ is active LOW.

$\overline{TxC}$ - Transmit Clock (Output), Pin 16

A 10 MHz signal derived from the internal oscillator. This clock is always active. $\overline{TxC}$ is TTL and MOS level compatible.

TxD - Transmit Data (Input), Pin 17

TxD is the NRZ serial input data to be transmitted. The data is clocked into the CS8023A by $\overline{TxC}$. TxD is active HIGH and TTL compatible.

TxEN ($\overline{TxEN}$) - Transmit Enable (Input), Pin 15

Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with $\overline{TxC}$. TxEN goes active with the first bit of transmission. TxEN is TTL compatible. If MODE2 is HIGH, TxEN is inverted.

COLL ($\overline{COLL}$) - Collision (Output), Pin 7

When asserted, this pin indicates to the controller the simultaneous transmission of two or more stations on network cable. COLL is TTL Compatible. If MODE2 is HIGH, COLL is inverted.

Transceiver Interface

Rx+ and Rx- - Differential Receiver Input Pair (Input), Pins 4 and 5

Differential receiver input pair which brings the encoded receive data to the CS8023A. The last transition is always positive-going to indicate the end of the frame.

COLL+ and COLL- - Differential Collision Input Pair (Input), Pins 12 and 11

This is a 10 MHz ±15% differential signal from the transceiver indicating collision. The duty cycle should not be worse than 60%/40% - 40%/60%. The last transition is positive-going. This signal will respond to signals in the range of 5 MHz to 11.5 MHz. Collision signal may be asserted if 'MAU not available' signal is present.

Tx+ and Tx- - Differential Transmit Output Pair (Output), Pins 19 and 18

Differential transmit pair which sends the encoded data to the transceiver. The cable driver buffers are source follower and require external 243Ω resistors to ground as loading. These resistors must be rated at 1 watt to withstand the fault conditions specified by IEEE 802.3. If MODE1=1, after 200 ns following the last transition, the differential voltage is slowly reduced to zero volts in 8 µs to limit the back swing of the coupling transformer to less than 0.1 V.

Miscellaneous

MODE1 - (Input), Pin 1

This pin is used to select between AC or DC coupling. When it is tied high or left floating, the output drivers provide differential zero signal during idle (IEEE 802.3 specification). When pin 1 is tied low, then the output is differentially high when idle (Ethernet Rev.1 specification).

MODE2 - (Input), Pin 2

The MODE2 Input signal is normally active LOW. In this configuration, the CS8023A operates in a mode compatible with the Crystal CS8005. An alternate mode of operation may be achieved by configuring the MODE signal active HIGH, or by allowing it to float HIGH with its internal pullup. In this configuration, RxC, TxEN, CSN and COLL become active LOW. In addition, RxD is HIGH during idle, and RxC has 1.2 µs discontinuity during signal acquisition.

$\overline{\text{LPBK}}$/WDTD - $\overline{\text{Loopback}}$/Watchdog Timer Disable (Input), Pin 3

Normal Operation: For normal operation this pin should be HIGH or tied to V_{CC}. In normal operation the watchdog timer is enabled.

Loopback:

When this pin is brought low, the Manchester encoded transmit data from TxD and $\overline{\text{TxC}}$ is routed through the receiver circuit and sent back onto the RxD and RxC Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.

Watchdog Timer Disable:

When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for longer than 25 ms, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx+ and Tx- lines. The watchdog timer is automatically reset each time TxEN is deasserted.

Semiconductor Corporation

CS83C92C

Coaxial Transceiver Interface

Features

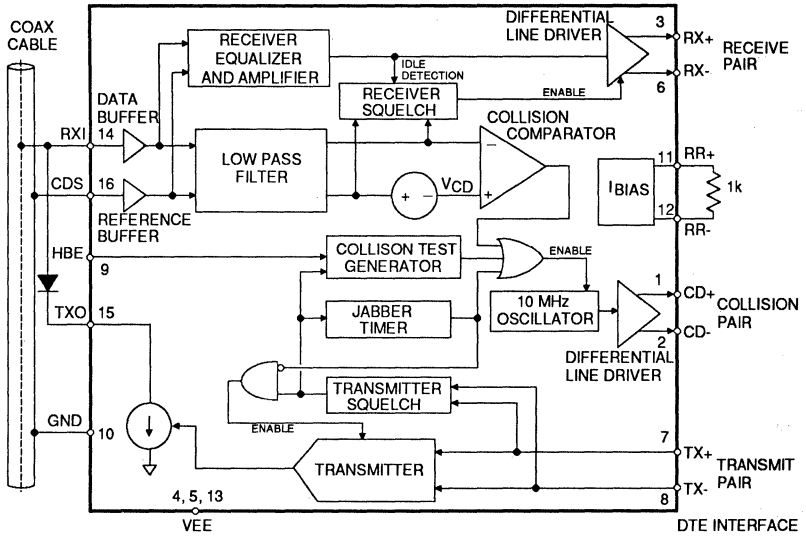
- Implemented in High Voltage Low Power CMOS
- Fully Compatible with National DP8392A and DP8392B
- Compliant ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Transceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive Mode Collision Detection
- Standard 16-pin DIP Package

General Description

The CS83C92C Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 Ethernet Data Link Controller and the CS8023A Serial Interface Adapter. The CS83C92C is fully compatible with the DP8392A/B but the CS83C92C is built in CMOS technology (hence the 83"C"92) and is compliant with ISO/IEEE 802.3 (hence the "C" suffix).

For an Ethernet network, the CS83C92C Transceiver is mounted on the Ethernet COAX cable, and connects to the station equipment through an AUI cable. In a Cheapernet network, the CS83C92C Transceiver is usually mounted on the LAN adapter in the station equipment, where it connects to the Cheapernet COAX through a BNC connector.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



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Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to ground)	VEE	-	-12.0	V
Package Power Rating at 25°C (Note 1)	P_P	-	3.5	W
Input Voltage	V_{IN}	GND + 0.3	VEE - 0.3	V
I/O Current (RXI, RR+, TX+, TX-, CDS, HBE) (TXO) (Note 2) (CD+, CD-, RX+, RX-)	I_{OUT}	- - -	±10 +10 / -100 +40 / -10	mA mA mA
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	-65	150	°C
ESD Protection (All pins)		1000	-	V

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Plastic DIP package only, package is PC board mounted. Derate at the rate of 28.6 mW/°C.
2. Transient currents of up to 200mA will not cause SCR latch-up.

ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter	Symbol	Min	Typ	Max	Units
Recommended Supply Voltage	VEE	-	-9.0	-	V
Supply Current (V_{EE} to GND) Nontransmitting Transmitting	I_{EE}	- -	-55 -100	-80 -130	mA mA
Receiver Input Bias Current (RXI)	I_{RXI}	-2	-	+25	µA
Transmiter Output DC Current (TXO)	I_{TDC}	37	41	45	mA
Transmitter Output AC Current (TXO)	I_{TAC}	±28	-	I_{TDC}	mA
Collision Threshold (Receive Mode)	V_{CD}	-1.45	-1.53	-1.58	V
Differential Output Voltage (RX±, CD±) (Note 3)	V_{OD}	±475	-	±1300	mV
DC Common Mode Output Voltage (RX±, CD±) (Note 4)	V_{OC}	-	-2.0	-	V
Idle State Differential Offset Voltage (RX±, CD±)	V_{OB}	-	-	±40	mV
Transmitter Squelch Threshold (TX±) (Note 5)	V_{TS}	-175	-225	-300	mV
Input Capacitance (RXI)	C_X	-	1.2	-	pF
Shunt Resistance - Nontransmitting (RXI)	R_{RXI}	100	-	-	kΩ
Shunt Resistance - Transmitting	R_{TXO}	10	-	-	kΩ

Notes: 3. Improved Spec. compared to 8392A and B - as required to meet ISO/IEEE 802.3 specifications.
4. V_{OC} has no impact on system performance since twisted pairs are transformer isolated.
5. For a minimum pulse width of ≥ 40 ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	max	Units
DC Supply Voltage, VEE (GND = 0V)	8.55	-	9.45	V
Operating Temperature	0	-	70	°C
RR± Resistor	990	-	1010	Ω

SWITCHING CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0 V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter		Symbol	Min	Typ	Max	Units
Receiver Startup Delay (RXI to RX±)	(Note 6)	t_{RON}	-	4	5	bits
Receiver Idle Detection Time on Coax Cable		t_{ROFF}	-	200	-	ns
Receiver Propagation Delay (RXI to RX±)		t_{Rd}	-	15	50	ns
Differential Outputs Rise Time (RX±, CD±)		t_{Rr}	-	4	7	ns
Differential Outputs Fall Time (RX±, CD±)		t_{Rf}	-	4	7	ns
Receiver and Cable Total Jitter		t_{RJ}	-	±2	-	ns
Transmitter Start-up Delay	(Note 6, 7)	t_{TST}	-	1	2	bits
Transmitter Propagation Delay		t_{Td}	5	25	50	ns
Transmitter Rise Time - 10% to 90% (TXO)	(Note 6)	t_{Tr}	20	25	30	ns
Transmitter Fall Time - 10% to 90% (TXO)	(Note 6)	t_{Tf}	20	25	30	ns
t_{Tr} and t_{Tf} Mismatch		t_{TM}	-	0.5	TBD	ns
Transmitter Skew (TXO)	(Note 8)	t_{TS}	-	±0.5	-	ns
Transmit Turn-on Pulse Width at V_{TS} (TX±)	(Note 9)	t_{TON}	15	20	40	ns
Transmit Turn-off Pulse Width above V_{TS} (TX±)	(Note 6)	t_{TOFF}	200	-	-	ns
Transmit Turn-off Delay		t_{TXOFF}	130	-	190	ns
Collision Turn-on Delay		t_{CON}	-	7	13	bits
Collision Turn-off Delay		t_{COFF}	-	-	20	bits
Collision Frequency (CD±)	(Note 6)	f_{CP}	8.5	-	11.5	MHz
Collision Pulse Width (CD±)	(Note 6)	t_{CP}	40	-	60	ns
CD Heartbeat Delay (TX± to CD±)		t_{HON}	0.6	-	1.6	µs
CD Heartbeat Duration (CD±)		t_{HW}	0.5	1.0	1.5	µs
Jabber Activation Delay (TX± to TXO and CD±)	(Note 6)	t_{JA}	20	29	60	ms
Jabber Reset Timeout (TX± to TXO and CD±)		t_{JR}	250	500	750	ms

Notes:
6. Improved Spec. compared to 8392A and/or B - as required to meet ISO/IEEE 802.3 specifications.
7. The third bit may have code violations. Fourth and subsequent bits transmitted according to spec.
8. Difference in propagation delay in outputing a positive edge as opposed to a negative edge.
9. For minimum pulse amplitude of ≥ -300mV.

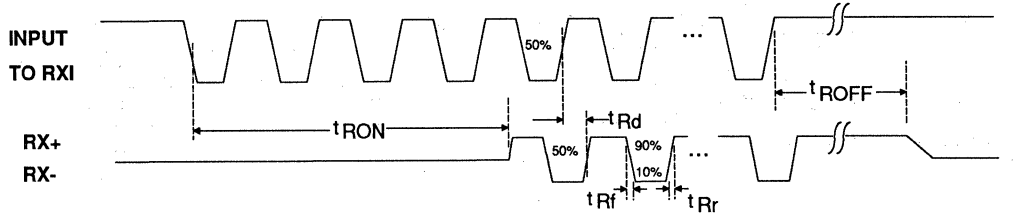


Figure 1. Receiver Timing

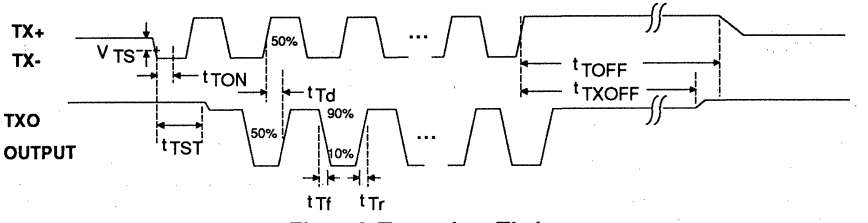


Figure 2. Transmitter Timing

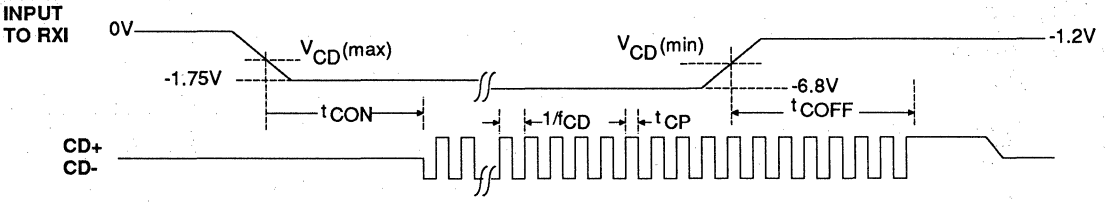


Figure 3. Collison Timing and Test Circuit

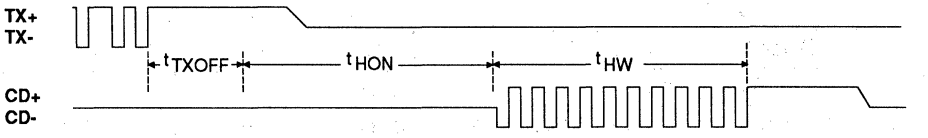


Figure 4. Heartbeat Timing

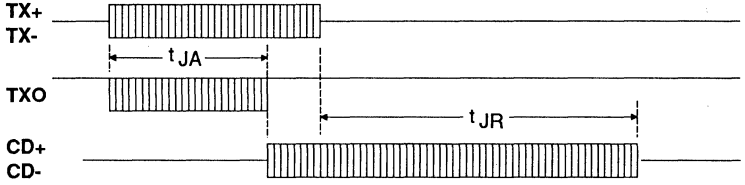


Figure 5. Jabber Timing

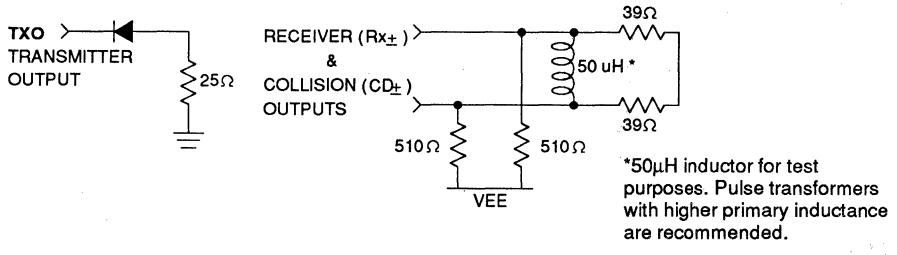


Figure 6. Test Loads

7

THEORY OF OPERATION

The CS83C92C interfaces the LAN station equipment to an Ethernet or Cheapernet COAX cable. The CS83C92C transmitter provides the current drive and pulse shaping required to drive signals onto the COAX, as well as squelch for signals received from the transmit pair, TX±. The receiver section provides equalization and squelch for signals on the COAX. Collisons are continually monitored and indicated by a 10MHz clock output on the CD± pair. The device also has a jabber timer which disables the transmitter and signals the DTE if packets longer than the legal length are transmitted.

In an Ethernet LAN, the CS83C92C mounts on the COAX cable, and connects to the station equipment through a transceiver drop cable (AUI cable). The transceiver drop cable can be up to 50 meters long. For Cheapernet applications, the CS83C92C is usually located in the station equipment, and connects to the Cheapernet COAX (such as RG58) through a BNC connector.

Transmitter

The transmitter accepts differential signals at the TX± inputs from the Manchester Code Converter, and drives these signals onto the network from the TXO output at the signal levels required by IEEE 802.3.

The TXO pin is open drain, and is pulled up to ground by the COAX termination resistors. The rise and fall times of the output pulses are internally conditioned to achieve slew rates of 25ns to reduce harmonics in the transmitted signal. Output drive current levels are set by a bandgap voltage reference and an external 1kΩ 1% resistor connected between the RR± pins. When not transmitting, the TXO output is disabled to prevent noise on the network. An external 1N916 diode must be added to reduce loading and capacitance (in both powered and unpowered conditions) to comply with ISO and IEEE specifications. With the diode in place, the tap capacitance contributed by the CS83C92C is typically less than 2 pF.

The transmit squelch circuit blocks signals input from TX± with pulse widths of less than 15ns or amplitudes of less than -175mV. The squelch circuit turns the transmitter off if the signal stays more positive than -175mV for more than 190ns (end of packet detection).

The TX± pins are transformer coupled to the Manchester Code Converter. In Ethernet applications where a transceiver drop cable (or Access Unit Interface, AUI) is used, a 78Ω resistor should be placed across the end of the cable, near the transformer. This resistor may be eliminated for Cheapernet applications where no AUI cable is used.

Receiver

The receiver input, RXI, connects to the COAX center conductor. The CS83C92C amplifies and equalizes the input signal and passes signals which exceed the receiver squelch level to the Receiver Pair, RX±. Up to five bits may be received at RXI and not transmitted on the RX± pair. The sixth bit will be transmitted, but may have code violations. The seventh and subsequent bits will be transmitted according to specificaton.

The receiver squelch circuit prevents false triggering of the receiver due to noise on the COAX. Signals input to the RXI pin that cause the output of an internal low-pass filter to exceed -140mV$_{DC}$ (typical) will exceed the DC squelch level, and be passed through to the RX± pair. Should the positive pulse width exceed 200ns (typical) the receiver will turn off (end of packet detection). The receiver will stay off if the output of the low-pass filter rises above the squelch threshold within 1µs.

RX± comprise a differential line driver which interfaces to the Manchester Code Converter via an

isolation transformer. RX± go to a differential zero state when idle to prevent DC current from saturating the isolation transformer.

For Ethernet applications, the RX± pins are tied to the VEE supply through 500Ω or 510Ω resistors. In Cheapernet applications, the CS83C92C is generally located on the same card as the Manchester Code Conveter, and 1500Ω pull-down resistors may be used to reduce power consumption.

Collison Detection

The collison detector monitors the COAX center conductor and senses the voltage conditions indicative of a collison. A collison can be detected when two or more stations are concurrently transmitting, whether or not the local transmitter is activated. The detector signals a collison by sending a 10MHz clock signal out on the Collison Pair, CD±, to the Manchester Code Converter.

The CDS pin provides a coaxial ground reference voltage for the collision detector. This pin should be connected to the shield of the COAX, rather than power supply ground, to prevent inaccuracies due to ground drops. A collison is detected when the output voltage of the receiver low-pass filter exceeds the collison voltage threshold, V_{CD}.

The 10MHz clock is internally generated, and used for collison indication and the heartbeat test. This oscillator requires no external components.

If enabled (HBE high), the Heartbeat Test will cause transmission of the 10MHz clock on the CD± pair for 1.0µs, 1.1µs after the end of each transmission if: both the transmitter and receiver were enabled; there was not a collision detected; jabber has not occured.

For Ethernet applications, the CD± pins are tied to the VEE supply through 500Ω or 510Ω resistors. In Cheapernet applications, the CS83C92C is generally located on the same card as the Manchester Code Converter, and the use of 1500Ω pull-down resistors will reduce power consumption.

Jabber Timer

The Jabber Timer monitors the operation of the transmitter using an internal oscillator as a time base. If the transmitter operates continuously for more than 80ms, the jabber timer disables the transmitter and enables the Collison Detector outputs. The Jabber Timer continues to monitor the transmitter squelch output. After the Manchester Code Converter has been silent for 750ms, the output on CD± is terminated, and the transmitter is reenabled for the next valid packet.

P. C. Board Layout

The CS83C92 is built in CMOS technology. It consumes and dissipates far less power than equivalent bipolar circuits. Still, heat dissipation and device reliability will be improved if the VEE pins are connected to a copper plane on the PC board.

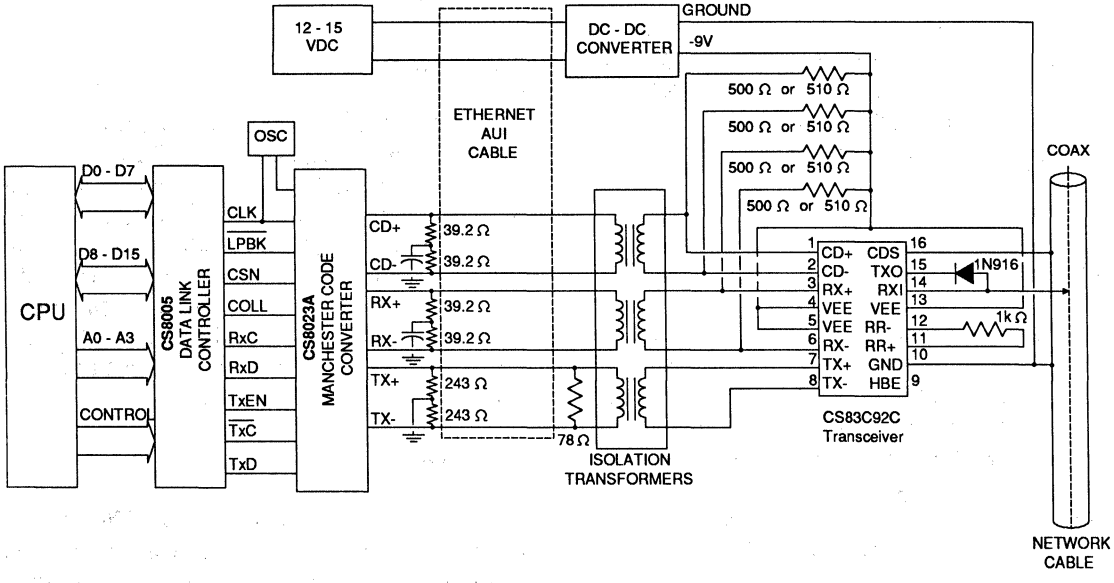
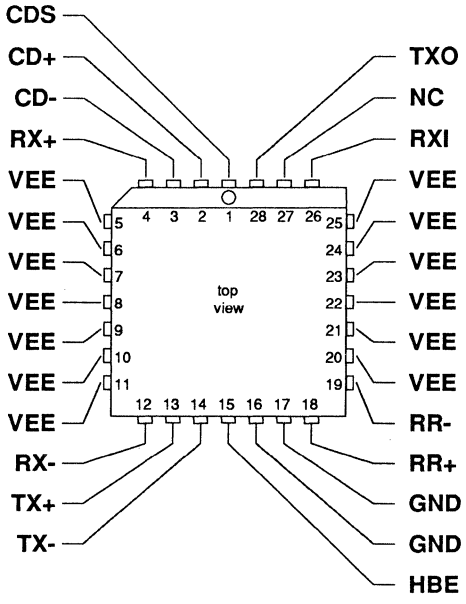


Figure 7. CS83C92C System Connection Diagram

For Ethernet applications, the isolation transformers, the DC to DC converter, and the transceiver are located in the Transceiver assembly, attached to the COAX. For Cheapernet applications, these components are usually mounted on the same board as the Manchester Code Converter (CS8023A) and Data Link Controller (CS8005). The 78Ω and 39.2Ω load resistors terminate the AUI cable, and are not required in systems where the AUI cable is not used (where the distance between the CS8023A and Transceiver is short).

PIN DESCRIPTIONS

Collison Detect Output +	CD+	1	16	CDS	Collison Detect Sense
Collison Detect Output -	CD-	2	15	TXO	Transmitter Output
Receive Data Output +	RX+	3	14	RXI	Receive Input
Negative Power Supply	VEE	4	13	VEE	Negative Power Supply
Negative Power Supply	VEE	5	12	RR-	External Resistor -
Receive Data Output -	RX-	6	11	RR+	External Resistor +
Transmit Data Input+	TX+	7	10	GND	Ground
Transmit Data Input -	TX-	8	9	HBE	Heartbeat Enable



Power Supplies

VEE - Negative Power Supply, Pins 4, 5 and 13.

The -9V supply is connected to these pins. A 0.1µF decoupling capacitor should be connected between this pin and GND.

GND - Ground, Pin 10.

Power supply ground; connects to COAX shield.

Inputs

TX+, TX- - Transmit Inputs, Pins 7 and 8.

Balanced differential line receiver which accepts the signal from the Manchester Code Converter. Signals exceeding transmitter squelch limits are output at TXO with the proper pulse shape. The common mode voltage on TX± is internally set and must not be externally established.

RXI - Network Receiver Input, Pin 14.

Connects to the COAX center conductor. Signals meeting receiver squelch limits are recovered and output on RX±. RXI also detects the collison voltage level.

Outputs

CD+, CD- - Collison Outputs, Pins 1 and 2.

A balanced differential output which drives an internally generated 10MHz signal to the station equipment when a collison is detected, when excessive transmission occurs, or during a CD heartbeat condition. These outputs are open source: when driving a 78Ω transmission line, these pins should be pulled to VEE with 500Ω or 510Ω resistors; for Cheapernet applications, where the CS83C92C is not driving a 78Ω load, use of 1.5kΩ resistors will save power.

RX+, RX- - Receive Data Outputs, Pins 3 and 6.

A balanced differential output which drives the data recovered from the network to the MCC. These outputs are open source: when driving a 78Ω transmission line, these pins should be pulled to VEE with 500Ω or 510Ω resistors; for Cheapernet applications, where the CS83C92C is not driving a 78Ω load, use of 1.5kΩ resistors will save power.

Control

HBE - Heartbeat Enable, Pin 9.

When the HBE pin is connected to ground, the Collision Detect Heartbeat test is enabled. Connecting the HBE pin to VEE disables the Collision Detect test.

RR+, RR- - External Resistor, Pins 11 and 12.

A 1kΩ, 1% resistor should be connected across these pins to set internal operating current levels.

CDS - Collision Detect Sense, Pin 16.

The CDS pin connects directly to the COAX shield, providing a reference for the collision detection voltage level.

Miscellaneous

NC - No Connect, Pin 27 (PLCC only).

This pin should be left floating.

INTRODUCTION

Crystal Semiconductor has dramatically cut the cost for fiber optic links with new low-cost bi-directional OPTIMODEMS™. The CS8123 and CS8124 support full-duplex voice and data communications at speeds to 256 kbps, while using just one fiber optic cable, with a single LED at each end. The CS8125 and CS8126 transmitter replace expensive hybrids with CMOS IC's to provide T1 links over a fiber pair.

Applications for the family of optical data links include: secure (TEMPEST) communication of voice and data at ISDN data rates, communication in electrically noisy environments such as a factory floor, links where the physical size and weight of cables and connectors are a concern, and interbuilding connections which require lightning immunity.

Also available is the CS8127 LED, which is a light emitting/detecting diode (LED). It's high optical efficiency and good responsivity make it ideal for use with the CS8123/4 OPTIMODEM™.

USER'S GUIDE

Device:	CS8123 OPTIMODEM	CS8124 OPTIMODEM	CS8125 T1 Transmitter	CS8126 T1 Receiver
Maximum Data Rate				
Synchronous	-	256 kbps	1.544 MHz	1.544 MHz
Asynchronous	38.4 kHz	38.4 kHz	-	-
Maximum Range	1.3 km	1.3 km	-	-
Number of Cables for Full Duplex Link	1	1	2	2
Package	24 pin 0.6" DIP 44 pin PLCC	24 pin 0.6" DIP 44 pin PLCC	24 pin 0.6" DIP	24 pin 0.6" DIP

CONTENTS

Semiconductor Corporation

CS8123/4

OPTIMODEM™

Features

- Time Compression Multiplexing for full-duplex communication over a single optical fiber
- Synchronous operation from 2.4 kbps to 256 kbps
- Asynchronous operation from dc to 38.4 kbps
- 10^{-9} BER up to 1.3 km
- System diagnostic capabilities
- Four optional secondary control channels provide independent end-to-end transmission links
- Independent transmit and receive clocks

General Description

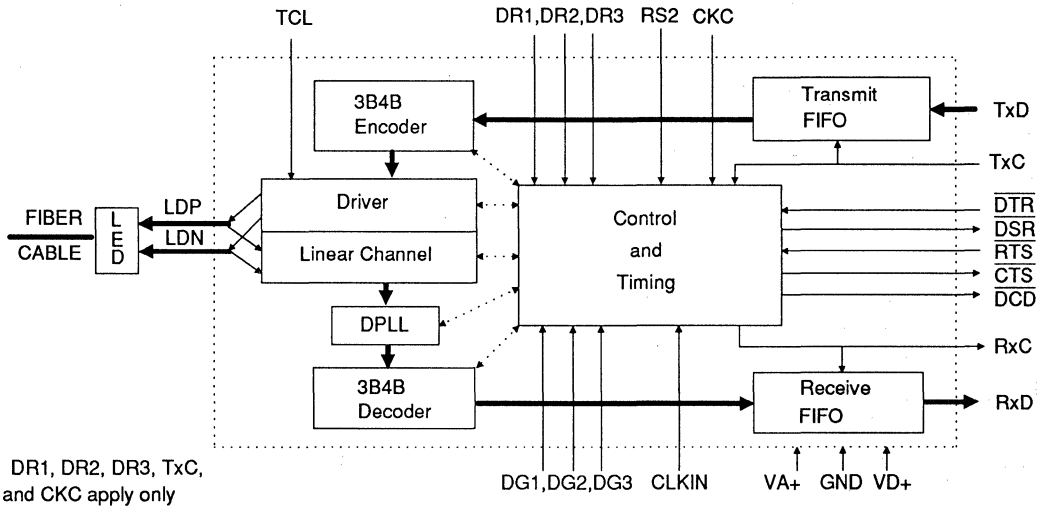
The CS8123 and CS8124 from Crystal Semiconductor Corporation are SMART *Analog*™ full-duplex modem devices that receive and transmit serial binary data over a single fiber-optic cable. Both devices provide the filtering, encoding, decoding, and data buffering to implement a "ping-pong" communication channel

The CS8123 device supports asynchronous communication. The CS8124 device supports asynchronous and synchronous communicatons. The RTS, CTS, DTR, and DSR control lines can be used for RS232C compatible modem control, or end-to-end transmission channels.

SMART *Analog* and OPTIMODEM are trademarks of Crystal Semiconductor Corporation.

Ordering Information:

Model	Package
CS8123-IP5	24 Pin 0.6" DIP
CS8123-IL5	44 Pin PLCC
CS8124-IP5	24 Pin 0.6" DIP
CS8124-IL5	44 Pin PLCC



Note: DR1, DR2, DR3, TxC, RxC, and CKC apply only to the CS8124.

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Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (VA+, VD+ pins)	V+ - GND	- 0.3	6.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current (Note 1) (Any pin except LDP, LDN, VA+, VD+, and GND)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C
Average Power Dissipation	P_D	-	500	mW

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at or beyond these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply		V+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
LED Drive Current	TCL Floating	I_{LDC}	90	100	115	mA
	TCL Grounded	I_{LDC}	-	10	-	mA

DIGITAL CHARACTERISTICS (T_A = -40 °C to 85 °C; VD+, VA+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Note 2)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	(Note 2)	V_{IL}	-	-	0.8	V
High-Level Input Voltage	CLKIN Pin 6	V_{IH}	.9VD+	-	-	V
Low-Level Input Voltage	CLKIN Pin 6	V_{IL}	-	-	.2VD+	V
High-Level Output Voltage I_{OUT} = -40 uA	(Notes 3,4)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA	(Notes 3,4)	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	± 10.0	-	uA
Three-State Leakage Currents		I_{oz}	-	-	± 10	uA

Notes: 2. Input pins are: DR 1/2/3, DG 1/2/3, RS2, CKC, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC.
3. Output pins are: $\overline{DSR}$, $\overline{CTS}$, $\overline{DCD}$, RxD, RxC, TxC.
4. Output drivers will output CMOS logic levels into a CMOS load.

OPERATING CHARACTERISTICS (T_A = -40 °C to 85 °C; VD+ , VA+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Power Consumption, TCL Floating	Ping Pong	P_C	-	210	300	mW
(Notes 5, 6)	Continuous Transmission	P_C	-	375	475	mW
Power Consumption, TCL tied to ground, Ping Pong (Notes 5, 6)		P_C	-	135	-	mW
Power Consumption, Continuous Receive	(Note 6)	P_C	-	125	-	mW
Receiver Input Current Range	-IP5 (Notes 6,7)	I_{IN}	1	-	30	μA_{peak}
LED Capacitance Presented to LDP/LDN		C_T	-	55	80	pF

Notes: 5. Total power dissipated by IC and LED, LED as specified in Table A3.
6. CLKIN Frequency = 9.216 MHz.
7. For a 10^{-9} BER.

SWITCHING CHARACTERISTICS (T_A = -40 °C to 85 °C; VD+, VA+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Frequency		f_c	-	9.216	-	MHz
TxC & RxC Frequency:	Synchronous	f_{ckc}	2.4	-	256	kHz
	Continuous Transmit or Receive	f_{ckc}	-	$f_c/8$	-	kHz
RxD & TxD Data Rate:	Synchronous		2.4	-	256	kHz
(Note 8)	Asynchronous		dc	-	38.4	kHz
RxC & TxC Duty Cycle	(Notes 9, 10)		-	50	-	%
Rise Time, All Digital Outputs	(Note 11)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 11)	t_f	-	-	100	ns
TxD to TxC Rising Setup Time	(Note 10)	t_{su1}	200	-	-	ns
TxC Falling to TxD Hold Time	(Note 10)	t_{h1}	25	-	-	ns
RxD to RxC Rising Setup Time	(Note 10)	t_{su2}	-	$\frac{1}{2\ f_{ckc}}$ -100	-	ns
RxC Rising to RxD Hold Time	(Note 10)	t_{h2}	-	$\frac{1}{2\ f_{ckc}}$ +100	-	ns
Frequency Deviation at TxC Input from Selected Rate	(Notes 10, 12)		-	300	-	ppm
Ext. Clock Oscillator	(Note 9)		40	50	60	%

Notes: 8. CS8124-IP5 units support synchronous communication at 2.4 kbps only in the -40 to +70°C temperature range.
9. Duty cycle is $(t_{pwh}/(t_{pwh} + t_{pwl})) * 100\%$. See Figure 2.
10. CS8124 in synchronous operation (not all DR1/2/3 low).
11. At maximum load of 1.6 mA and 50 pF.
12. In Synchronous mode, data rate selected by DR1/2/3. In Transmit Only mode, selected rate is fc/8. CLKIN frequency must be within ± 50 ppm of specified frequency.

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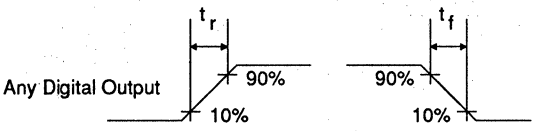

Figure 1. Digital Output Rise and Fall Characteristics

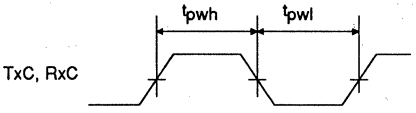

Figure 2. Clock Signal Timing

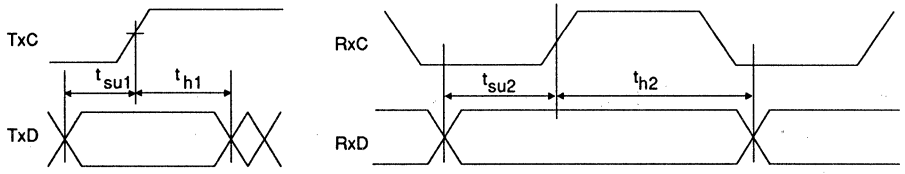

Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

The CS8123/4 OPTIMODEMs receive and transmit serial binary data over a single fiber-optic cable. Refer to Figure 4 for a typical system connection diagram. The modems provide the filtering, encoding, decoding and data buffering to implement a Time Compression Multiplexed "ping-pong" channel. Both modems support full-duplex asynchronous operation up to 38.4 kbps. The CS8124 also supports full-duplex synchronous communication at 2.4, 9.6, 19.2, 64, 160, 192 and 256 kbps.

The $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$ and $\overline{DTR}$ pins can be selectively used in one of two modes: as end-to-end communication channels, or as conventional modem control lines used in handshakes with the OPTIMODEMs (DCE). The two modes are shown in Table 1 and Figure 5

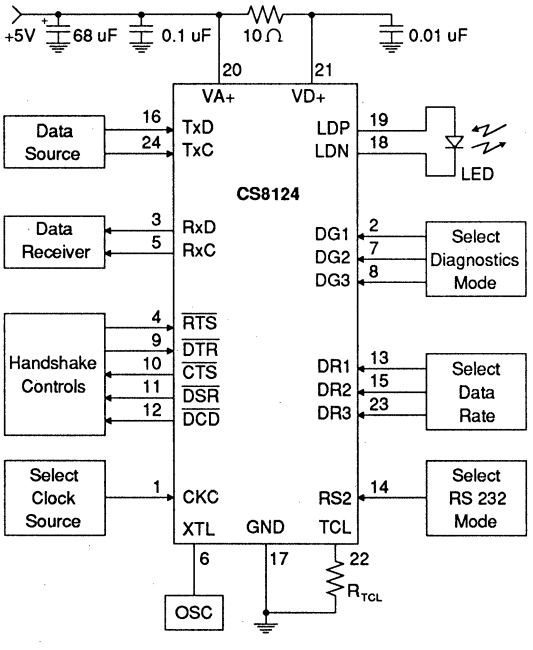

Figure 4. Typical System Connection Diagram

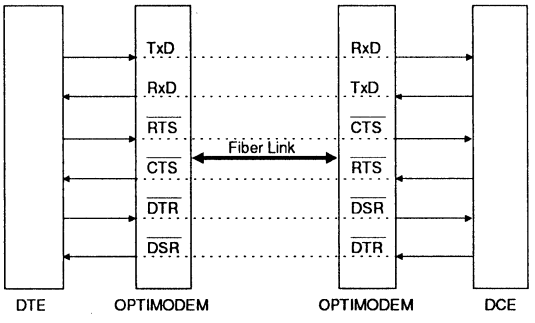

Figure 5. - End-to-End (Transparent) Mode

respectively. The desired mode is selected through the RS2 pin.

In the end-to-end mode, the $\overline{RTS}$ and $\overline{DTR}$ inputs are oversampled at approximately 12 kHz, allowing asynchronous communications at speeds up to 4.8 kHz. The actual data rate achieved will depend upon the jitter tolerance of the circuitry connected to the $\overline{DSR}$ and $\overline{CTS}$ outputs. Oversampling a 4.8 kHz signal at 12 kHz implies 40% jitter (4.8/12) on the rising and falling edges of the $\overline{DSR}/\overline{CTS}$ outputs.

Both modems provide extensive diagnostic and maintenance capabilities. Note that the OPTIMODEM digital signals are standard logic levels. RS232 level translators/buffers are required for interfacing to DTE or DCE equipment.

Efficient 3B4B line encoding is employed to ensure error-free data transmission regardless of ones density. The 3B4B line code technique generates a four-bit binary code which corresponds to three binary input bits. This DC balanced code provides sufficient ones density to satisfy the requirements of the receiver's phase-lock loop while optimizing transmission bandwidth and reducing noise. At the receive end, the four-bit code is converted back to the original three bits before being output on RxD.

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OPTIMODEM (DCE)	DTE
1. Modem powers up, then asserts $\overline{DSR}$.	1. DTE initializes, then asserts $\overline{DTR}$.
2. Recognizes $\overline{DTR}$. Ping-pong synchronization is in progress.	2. Recognizes $\overline{DSR}$ and waits for $\overline{DCD}$.
3. When Synchronization is achieved, asserts $\overline{DCD}$. *	3. Recognizes $\overline{DCD}$, then asserts $\overline{RTS}$.
4. Recognizes $\overline{RTS}$, then asserts $\overline{CTS}$. **	4. Recognizes $\overline{CTS}$, then starts communication with far end. ***

* If synchronization is lost, modem takes $\overline{DCD}$ and $\overline{CTS}$ high.
** If $\overline{RTS}$ goes high, modem takes $\overline{CTS}$ high.
*** DTE takes $\overline{DTR}$ high, then DCE forces $\overline{DCD}$ high.

Table 1. - Modem Control Mode

In order to accomplish ping-pong communication, the near-end and far-end OPTIMODEMs must establish sychronization so that one OPTIMODEM receives while its counterpart transmits. Each OPTIMODEM operates on an internal master clock which is one sixth the oscillator frequency (1.536 MHz for a 9.216 MHz crystal). A machine cycle, which consists of 128 master clock cycles, is divided into four pieces: time to transmit, a delay period, time to receive, and another delay period. The delay times are established during synchronization to adjust positioning of the transmit and receive windows to account for signal propagation time through the length of fiber being used.

The OPTIMODEM attempts to establish synchronization upon power up or reset. In normal operation, both OPTIMODEMs attempt to communicate using a fixed code. The difference in crystal oscillator frequencies at either end will cause the transmit and receive windows of the two OPTIMODEMs to drift with respect to each other. When one OPTIMODEM first recognizes the transmission from its counterpart, it assumes the slave mode and changes its synchronization control word to direct its counterpart to be the master. In the slave mode, the OPTIMODEM will adjust its machine cycle to speed synchronization with the master. Once synchronized, the slave will make small adjustments in machine cycle time to compensate for differences in oscillator frequencies of the two OPTIMODEMs. The OPTIMODEM can tolerate up to 100 ppm difference in oscillator frequencies between the master and slave. See section on Forced-Slave mode for information on quick synchronization.

The CS8123/4 minimizes the number of external components required, using just one LED to both send and receive data on a single fiber. The CS8123/4 can support cables up to 1300 meters as discussed in the section on LED requirements in the *Applications* section which appends this data sheet. Total transmission delay through two OPTIMODEMs and 1.3 km of cable will be, typically, 38 times the data rate bit period, plus 10µs for fiber delay. For example, at 256 kbps, the transmission delay is approximately 158µs.

TRANSMIT SECTION

In the asynchronous mode, the TxC clock is not used and the CS8123/4 accepts data asynchronously on the TxD input pin. The TxD input is oversampled by at least 6.7 times. This data is temporarily stored in the Transmit

FIFO, encoded and then transmitted to the far end OPTIMODEM.

In the synchronous mode, the CS8124 accepts data on the TxD input pin using the TxC clock. This data is stored in the Transmit FIFO, encoded then transmitted down the fiber. The Clock Control (CKC) input is used to select either an internally generated TxC clock or an externally provided TxC clock. The 160 kbps synchronous data rate operates only with an externally-provided transmit clock (TxC).

Clocks

The CS8123 operates asynchronously. The CS8124 may be operated in either the synchronous or asynchronous mode by setting the data rate inputs, DR1, DR2, and DR3. The data rates and settings are shown in Table 2. The OPTIMODEM's internal frequency reference is provided by inputting a clock to the CLKIN pin. This clock's amplitude must be within 10% of the supply voltages and have a duty cycle of 40% to 60%.

The CS8124 provides three clock options:

1) Asynchronous operation: DR1/2/3 = low. RxC and TxC pins of CS8124 are held in a high impedance state.

2) Synchronous with externally provided transmit clock: Not all DR1/2/3 = low; CKC = low. An externally generated clock must be input to the TxC pin at the rate selected by DR1/2/3.

3) Synchronous with internally provided transmit clock: Not all of DR1/2/3 = low; CKC = high. The CS8124 generates the transmit clock and outputs it at the TxC pin.

In the synchronous mode, the two TxC clocks at either end of the link are allowed to deviate from each other by several hundred ppm. Also, an externally provided TxC clock can deviate from the rate selected on DR/1/2/3 by several hundred ppm. In both cases the OPTIMODEMs will make internal adjustments to compensate for the frequency differences. All combinations of internally generated and externally provided clocks for TxC are allowed.

DR1	DR2	DR3	Data Rate (kbps)* with 9.216 MHz crystals
0	0	0	Async : dc to 38.4
0	0	1	2.4
0	1	0	9.6
0	1	1	19.2
1	0	0	64
1	0	1	160**
1	1	0	192
1	1	1	256

* Note that a 56 kbps link can be implemented by using an 8.064 MHz oscillator and the 64 kbps data rate selection.

** The 160 kbps data rate clock must be externally generated.

Table 2 - Data Rate Selection

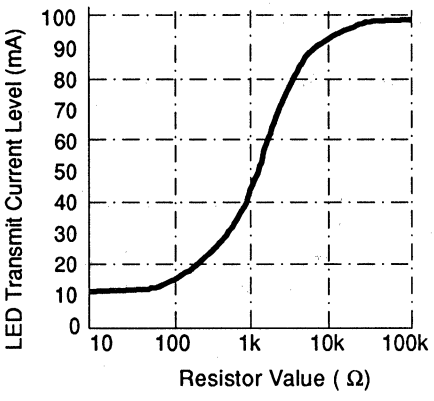


Figure 6. Resistor to Set the Transmit Current Level

Transmit Current Adjustment

The transmit current level is typically 100 mA when TCL is left unconnected. The current level may be adjusted by tying the TCL pin to ground through a resistor as shown in Figure 6. Tying TCL directly to ground selects the minimum drive current of 10 mA. The output drive current corresponding to a given resistor, R_{TCL}, can be calculated using the following equation:

$$I_{drive} = 100 \left(\frac{110 + R_{TCL}}{1100 + R_{TCL}} \right) mA$$

Equation 1

RECEIVE SECTION

The LED detects the data burst from the far-end modem. A digital phase-lock loop performs the timing recovery to maintain synchronization between the master and slave OPTIMODEMs. The recovered signal is decoded and then stored in the Receive FIFO. The Receive FIFO provides the output to the RxD pin. In synchronous mode, the RxC clock is derived from the incoming data. Rising edges of RxC indicate valid RxD data. Clock jitter resulting from the ping-pong operation and 3B4B encoding is reduced by an internal jitter attenuator. The jitter attenuator is not active in the continuous receive mode.

Digital Carrier Detect

A logical zero on the Digital Carrier Detect, ($\overline{DCD}$), output indicates that both ping-pong and 3B4B synchronization has occurred between the near-end and far-end modems and that data transmission can occur. If the receiver loses carrier, the OPTIMODEM automatically resets.

DIAGNOSTIC FEATURES

The CS8123/4 provides several capabilities to facilitate fault isolation and system performance verification. These diagnostic features are selected using the DG1, DG2, and DG3 pins. Table 3 shows the various diagnostic modes and the corresponding setting for DG1/2/3.

Forced-Slave Mode

In normal operation, both OPTIMODEMs in a link start the synchronization process as peers. As synchronization start-up proceeds, either one can assume the role of "master" or "slave". Using the diagnostic input pins it is possible to force the OPTIMODEM to assume the slave mode, which reduces maximum possible start-up time. However, the user must now ensure that only one of the two OPTIMODEMs is in this mode.

There are system configurations where rapid link synchronization is desirable, but it is not possible to select half of the ends to be in Forced-Slave mode due to logistics or hardware configuration limitations. Synchronization in Normal-Operating mode will be slow if the oscillators at either end are almost exactly the same frequency. Holding the CS8123/4 in Forced-Slave mode, DG 1, 2, 3 = 1/1/1, for at least 50 ms at power-up should en-

DG1	DG2	DG3	Diagnostic Mode
0	0	0	Normal Full-Duplex Operation
0	0	1	Local Loopback
0	1	0	Remote Loopback
0	1	1	Remote Loopback with Forced-Slave Mode
1	0	0	Reset
1	0	1	Continuous Receive
1	1	0	Continuous Transmit
1	1	1	Full-Duplex Operation with Forced-Slave Mode

Table 3. Diagnostic Mode Selection

sure rapid and reliable synchronization as long as the two ends of the link are powered up at different times. See the applications section for schematics.

Loopbacks

Two loopback modes are provided on the CS8123/4: local and remote loopbacks. Loopbacks are supported in both asynchronous or synchronous modes, with either internal or external TxC clock. In local loopback mode, the transmit data and clock (if applicable) inputs are looped back inside the near-end CS8123/4 and output on the receive data and clock outputs. This allows the near-end user to verify performance up to the OPTIMODEM. Ping-pong synchronization between the OPTIMODEMs is maintained. Data is still transmitted to the far-end OPTIMODEM. Inputs to the near-end receiver are not output at RxD, and $\overline{DCD}$ is high. Local loopback takes precedence over remote loopback. The local loopback path is the shortest logical path through the OPTIMODEM, and does not include the driver or linear channel.

When remote loopback is selected on the near-end CS8123/4, the near-end OPTIMODEM directs the far-end OPTIMODEM to loop back its received data. This allows the user to verify performance of the complete near-end CS8123/4, the fiber, the LEDs and most of the far-end CS8123/4. The far-end OPTIMODEM also outputs received data and clock (when applicable) at RxD and RxC. When remote loopback is selected and synchronization is achieved, $\overline{DCD}$ goes low on the near-end OPTIMODEM. When remote loopback is in effect, the far-end OPTIMODEM ignores inputs on TxC and TxD and brings $\overline{DCD}$ high.

Continuous Transmit and Receive Modes

The CS8124 has two special operating modes: continuous transmit and continuous receive. In continuous transmit mode, the near-end CS8124 sends the encoded version of the data input on TxD. TxD must be clocked into the part at a rate of approximately one-eighth the crystal frequency. The 3B4B coding is still employed so the actual transmission rate is one-sixth the crystal frequency. As in normal synchronous operation, TxC can be either an input or an output. If TxC is externally generated, its frequency can differ from the nominal frequency by several hundred ppm.

When continuous transmit is selected, the receiver is inoperative, no ping-pongs take place and $\overline{DCD}$ stays high. Measurements can then be made at the output of the near-end LED and at the far-end output of the fiber cable to isolate LED and/or cable failures.

When in the continuous transmission mode, and under control of the $\overline{RTS}$ pin, the OPTIMODEM will generate a repetitive encoded pattern to achieve 3B4B code alignment of the far-end receiver to the transmitter. The far-end receiver takes no special action in response to this pattern, other than normal 3B4B decoding and receiver synchronization. The user must maintain $\overline{RTS}$ high for 50ms. When the user returns $\overline{RTS}$ low, the first data bits input to TxD may be lost (up to 5 bits).

In continuous receive mode, the receiver continually receives data, and outputs the data and clock on the receive outputs, RxD and RxC. The RxC output will be gapped in the following manner: three clock pulses will be followed by one clock hole in a repetitive manner (see Figure 7). $\overline{DCD}$ is held low in the continuous receive mode once synchronization is achieved. The transmitter is inactive in this mode.

When in the continuous transmit or receive mode, the $\overline{DTR}$ input is ignored, and the $\overline{DSR}$ and $\overline{CTS}$ outputs are defined as in Table 4.

For single direction transmission of asynchronous data, select internally generated TxC. Data input on TxD will be sampled at the TxC rate (fc/8) and transmitted to the receive end. The received data will be present at RxD and RxC may be ignored.

RS2 Input	$\overline{DSR}$ Output	$\overline{CTS}$ Output
HIGH	LOW except during reset	Same as $\overline{DCD}$
LOW	Undefined	Undefined

Table 4. Pin Definitions in Continuous Modes

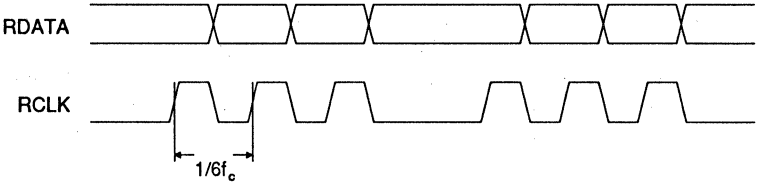
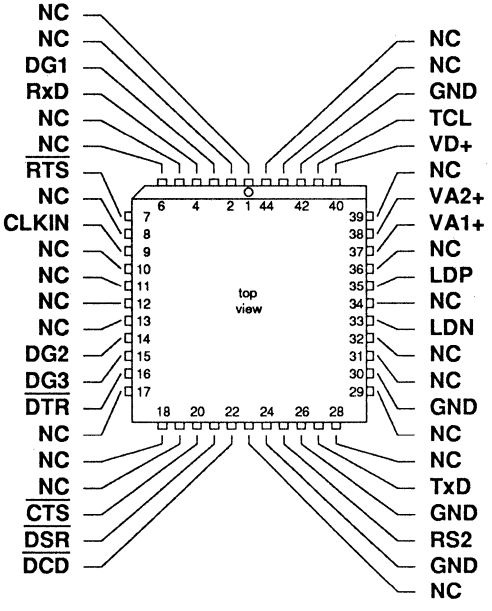


Figure 7. Receiver Output Timing in Continuous Receive Mode

PIN DESCRIPTIONS

CS8123

NO CONNECT	NC	1	24	NC	NO CONNECT
DIAGNOSTIC 1	DG1	2	23	GND	GROUND
RECEIVE DATA	RxD	3	22	TCL	TRANSMIT CURRENT LEVEL
REQUEST TO SEND	$\overline{RTS}$	4	21	VD+	DIGITAL POWER SUPPLY
NO CONNECT	NC	5	20	VA+	ANALOG POWER SUPPLY
CLOCK INPUT	CLKIN	6	19	LDP	LED POSITVE I/O
DIAGNOSTIC2	DG2	7	18	LDN	LED NEGATIVE I/O
DIAGNOSTIC 3	DG3	8	17	GND	GROUND
DATA TERMINAL READY	$\overline{DTR}$	9	16	TxD	TRANSMIT DATA
CLEAR TO SEND	$\overline{CTS}$	10	15	GND	GROUND
DATA SET READY	$\overline{DSR}$	11	14	RS2	RS-232 MODE
DIGITAL CARRIER DETECT	$\overline{DCD}$	12	13	GND	GROUND



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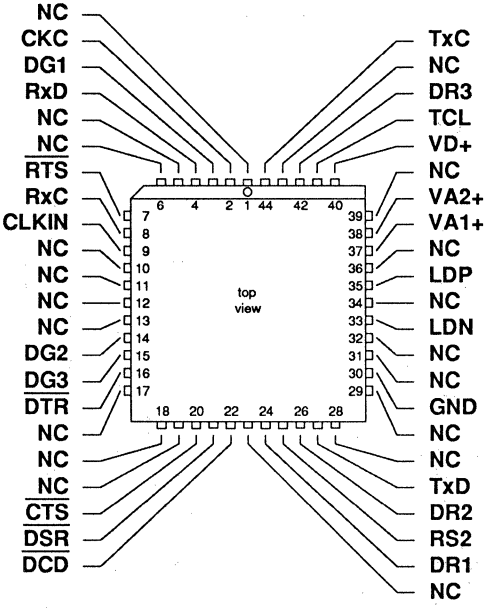
CS8124

CLOCK CONTROL	CKC	1	24	TxC	TRANSMIT CLOCK
DIAGNOSTIC 1	DG1	2	23	DR3	DATA RATE SELECT 3
RECEIVE DATA	RxD	3	22	TCL	TRANSMIT CURRENT LEVEL
REQUEST TO SEND	$\overline{\text{RTS}}$	4	21	VD+	DIGITAL POWER SUPPLY
RECEIVE CLOCK	RxC	5	20	VA+	ANALOG POWER SUPPLY
CLOCK INPUT	CLKIN	6	19	LDP	LED POSITIVE I/O
DIAGNOSTIC 2	DG2	7	18	LDN	LED NEGATIVE I/O
DIAGNOSTIC 3	DG3	8	17	GND	GROUND
DATA TERMINAL READY	$\overline{\text{DTR}}$	9	16	TxD	TRANSMIT DATA
CLEAR TO SEND	$\overline{\text{CTS}}$	10	15	DR2	DATA RATE SELECT
DATA SET READY	$\overline{\text{DSR}}$	11	14	RS2	RS-232 MODE
DIGITAL CARRIER DETECT	$\overline{\text{DCD}}$	12	13	DR1	DATA RATE SELECT 1



Pin numbers apply to 24 pin DIP packages

Power Supplies

VA+ - Analog Power Supply, PIN 20.
Typically +5 volts.

VD+ - Digital Power Supply, PIN 21.
Typically +5 volts.

GND - Ground, PIN 17 on CS8124; PINS 13, 15, 17, and 23 on CS8123.
Ground reference.

Oscillator

CLKIN - Clock Input, PIN 6.
Input for externally generated CMOS clock. Standard operation requires a 9.216 MHz (± 50 ppm) clock. Other frequencies may be used to adjust the OPTIMODEM throughput and data rates. As the CLKIN frequency is reduced, the OPTIMODEM's potential link distance increases and the data rates decrease proportionately. Oscillator specifications are given in the Applications section.

Inputs

TxD - Transmit Data, PIN 16.
Data to be transmitted. In the asynchronous mode, the rate of the data can be from dc to 38.4 kbps. In the synchronous mode, data is clocked into the CS8124 on the rising edge of TxC.

TxC - Transmit Clock (CS8124 Only), PIN 24.
When CKC is high, TxC will output a clock at the rate selected by DR1/DR2/DR3. When CKC is low, TxC accepts input clock from an external source. TxC goes into a high impedance state when asynchronous operation is selected. For synchronous operation TxD is sampled on the rising edge of TxC. For synchronous operation at 160kbps, an externally-provided clock must be used.

CKC - Clock Control (CS8124 Only), PIN 1.
Defines the source of the clock signal on TxC for synchronous operation. A low on CKC indicates that external clock is being input on TxC. A high on CKC indicates the the CS8124 is sending out TxC at one of the rates selected on the DR1/DR2/DR3 data rate selection inputs. If CKC is left unconnected (floating), CKC pulls low, selecting the external clock. CKC must be held low for synchronous operation at 160kbps since this case requires an externally-provided clock.

DG1; DG2; DG3 - Diagnostic 1; 2; 3, PINS 2, 7, 8.
Select a diagnostic mode as shown in Table 3 in the *Circuit Description* section. If these pins are left unconnected, (floating), the OPTIMODEM assumes the mode for Normal Operation.

DR1; DR2; DR3 - Data Rate 1; 2; 3 (CS8124 Only), PINS 13, 15, 23.

Select a data rate for the TxC and RxC pins as shown in Table 2 in the *Circuit Description* section. If these pins are left unconnected (floating), the CS8124 defaults to asynchronous operation.

RS2 - RS-232C Control Mode Select, PIN 14.

Selects whether the $\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$ and $\overline{DTR}$ are used in an end-to-end mode, or modem control handshake mode. When RS2 is low, the end-to-end mode is in effect as shown in Figure 4 in the *Circuit Description* section. If RS2 is left unconnected, (floating), the end-to-end mode is in effect. When RS2 is high, the modem control mode, as shown in Table 1 in the *Circuit Description* section, is in effect.

$\overline{DTR}$ - Data Terminal Ready , PIN 9.

In the end-to-end mode, data input on $\overline{DTR}$ is transmitted over the link and presented at the far end as the $\overline{DSR}$ output. The $\overline{DTR}$ input is oversampled at approximately 12 kHz, allowing asynchronous communications at speeds up to 4.8 kHz. The actual data rate achieved will depend upon the jitter tolerance of the circuitry connected to the $\overline{DSR}$ output. Oversampling the 4.8 kHz signal at 12 kHz implies 40% jitter (4.8/12) on the rising and falling edges of the $\overline{DSR}$ output.

In the modem control mode, a logic 0 indicates that the DTE is powered up and initialized. $\overline{DTR}$ has an internal pull down.

$\overline{RTS}$ - Request To Send , PIN 4.

In the end-to-end mode, the $\overline{RTS}$ input is transmitted over the link and presented at the far end as the $\overline{CTS}$ output. The $\overline{RTS}$ input is oversampled at approximately 12 kHz, allowing asynchronous communications at speeds up to 4.8 kHz. The actual data rate achieved will depend upon the jitter tolerance of the circuitry connected to the $\overline{CTS}$ output. Oversampling the 4.8 kHz signal at 12 kHz implies 40% jitter (4.8/12) on the rising and falling edges of the $\overline{CTS}$ output.

In the modem control mode, a logic 0 indicates that the DTE is ready to communicate to the far end. In continuous transmit mode, setting $\overline{RTS}$ to logic 1 causes a repetitive synchronization pattern to be transmitted. $\overline{RTS}$ has an internal pull down.

TCL - Transmit Current Level, PIN 22.

Defines the current driven into LDP/LDN. When left unconnected, the current level is typically 100mA. When tied to ground, output current level is at a minimum of about 10 mA. Current can be set at an intermediate level, (as shown in Figure 5 in the *Circuit Description* section), by tying this pin to ground through a resistor.

Outputs

$\overline{DCD}$ - Digital Carrier Detect, PIN 12.

A low level indicates that the receiver's 3B4B decoder has achieved synchronization with respect to the incoming data stream. $\overline{DCD}$ is always forced high on the OPTIMODEM for which local loopback has been selected, and during a remote loopback selected by the far-end terminal, and when continuous transmit has been selected. Upon loss of digital carrier, the OPTIMODEM initiates a reset.

$\overline{CTS}$ - Clear To Send, PIN 10.

In the end-to-end mode, CTS shows the state of the far-end $\overline{RTS}$ input. Each $\overline{CTS}$/$\overline{RTS}$ pair can be used as a uni-directional data channel. The channel is always asynchronous for both the CS8123 and the CS8124, and is oversampled at a rate of approximately 12 kHz.

In the modem control mode (RS2 = high), a logic 0 indicates that the DTE can begin transmission via the TxD and RxD pins.

$\overline{DSR}$ - Data Set Ready, PIN 11.

In the end-to-end mode, $\overline{DSR}$ outputs the data input on the far end $\overline{DTR}$ pin. Each $\overline{DSR}$/$\overline{DTR}$ pair can be used as a uni-directional data channel. The channel is always asynchronous for both the CS8123 and the CS8124, and is oversampled at a rate of approximately 12 kHz.

In the modem control mode (RS2 = high), a logic 0 indicates that the OPTIMODEM is powered up.

RxD - Received Data, PIN 3.

The data can be read asynchronously (in that mode) or is valid on the rising edge of RxC (in the synchronous mode).

RxC - Received Clock (CS8124 only), PIN 5.

In the synchronous mode, RxD is valid and stable on the rising edge of RxC. RxC goes into a high impedance state when asynchronous operation is selected.

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Inputs/Outputs

LDP; LDN - LED Positive I/O; LED Negative I/O, PIN 19 & 18 .

These bidirectional pins connect directly to the LED, and alternately drive and receive from the LED. LDP connects to the LED anode and LDN connects to the LED cathode. It is absolutely critical that LED be connected to LDP and LDN with the shortest possible traces on the printed circuit board.

APPLICATION NOTES

The use of a CDB8124 or CDB8123 Evaluation Kit to evaluate an OPTIMODEM is highly recommended because system performance is dependent upon the quality of the board layout. In particular, the use of wire-wrapped boards for IC evaluation can result in a non-functional link.

Temperature Effects

LED emission spectrum shifts with temperature, as does the responsivity peak. When LEDs at the opposite ends of link are at different temperatures, the link budget may be decreased. See Table A4.

Fiber Optic Cable

Some specifications for the various cable types are given in Table A1. Table A2 provides some information on cables and manufacturers. There are many variations: contact the manufacturers for more details.

Crystal has used Hewlett-Packard's plastic fibers and associated LEDs (the VERSATILE HFBR-152x family), and observed that the link functioned. These LED's are approximately one-third the cost of the glass-fiber compatible LED's. However, the length of the cable is severely limited by the attenuation characteristics of plastic fiber (about 1dB per meter). The VERSATILE family may prove workable for links of a few meters.

LED Requirements

Typical LED specifications are given in Table A4, and some suggested LEDs are listed in Table A3. It is recommended that the emitted wavelengths of the LED's on each end of a link be the same. The Hafo, HP and Honeywell LED's have different peak wavelengths and power requirements, and should not be interchanged in a system.

Type	Numerical Aperture	Attenuation (dB per km)
200 um PCS	0.40	6.0
100/140um	0.29	4.5
62.5/125 um	0.28	3.75
50/125 um	0.20	3.5
1000 um Plastic	0.50	1000

Table A1 - Typical Cable Specifications

Vendor	Part Number	Package
Crystal Semi	CS8127	ST Fiber DIP
Honeywell	HFE4214-013	ST Fiber DIP
	HFE4404-013	SMA Fiber DIP
Hewlett Packard	HFBR1405	SMA Fiber DIP
	HFBR1415	ST Fiber DIP
ABB Hafo	1A-212	TO-46

Table A3 - Approved LED Vendors

Cable	Manufacturer	Part Number	Phone
200um	Ensign-Bickford Optics Co	HCP-M02000T-A01VS	(203) 678-0371
62.5/125 Ceramic ST	Amphenol Fiber Optics	907-11035-10xxx	(800) 752-5797
100/140 Ceramic ST		907-11036-10xxx	

Table A2 - Fiber Cable and Manufacturer Information

TYPICAL LED SPECIFICATIONS (T_A = 25°C; VA+ = 5V±5%; GND = 0V)

Parameter		Symbol	Typ	Units
Forward Voltage	(I_F = 100 mA)	V_F	1.7	V
Breakdown Voltage	(I_R = 10 µA)	V_{BR}	8.0	V
Series Resistance	(dc)	r_s	8	Ohms
Diode Capacitance (Note A1)	(V_R = 0 V) (f = 1 MHz)	C_T	55	pF
Fiber Coupled Power	(I_F = 100 mA, 100 µm Graded, NA = 0.29)	P_{OC}	116	µW
P_{OC} Temperature Coefficient (Note A2)	(I_F = 100 mA, 100 µm Graded, NA = 0.29)	$\Delta P_{OC}/\Delta T$	-0.025	dB/°C
Response Time	(10 - 90%, I_F = 100 mA No Pre-Bias)	t_r t_f	7 4	ns ns
Responsitivity	(V_R = 0 V)	R_O	0.10	A/W
R_O, Temperature Coeff. (Notes A2, A3)	("+" for detector temp increasing)	$\Delta R_O/\Delta T$	+1.86	mA/W°C
R_O, Wavelength Coeff.	("-" for emitter wavelength increasing	$\Delta R_O/\Delta\lambda$	-3.7	%/nm
Leakage Current	(V_R = 1 V)	I_D	1.0	nA

Notes: A1. For low capacitance diodes, an additional capacitor must be added to meet this specification.
A2. Industrial Temperature Range (-40°C to 85°C).
A3. Includes Spectral Variance.

Table A4 - LED Specifications

Power Supply Decoupling

VA+, VD+ and GND should be decoupled using the circuit shown in Figure A1. The 68 µF capacitor is required to filter the power supply, and prevent power supply ripple. Ripple can occur at the power supply pins of the device as a result of the different current demands when the OPTIMODEM is transmitting or receiving.

Other circuitry on the same board as the OPTIMODEM should have a separate power supply trace (from the point at which the power supply enters the board). All ICs on the board should be decoupled. OPTIMODEM performance will improve as power supply noise is minimized.

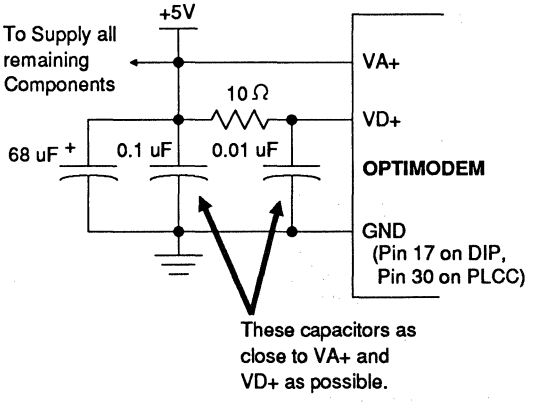

Figure A1 - Power Supply Decoupling

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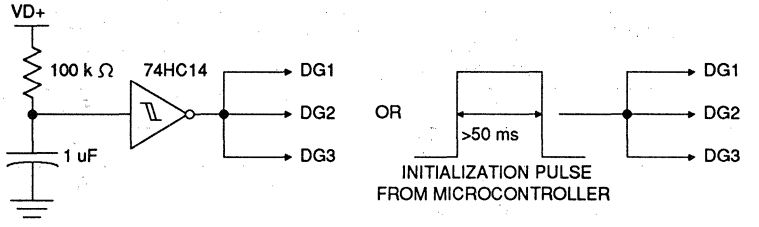


Figure A2. Synchronization Techniques

Fast and Reliable Synchronization

When OPTIMODEMs are operated in normal full-duplex mode, the time required to synchronize may increase as the frequency difference between the two OPTIMODEM master clocks (CLKIN) decreases. To ensure fast synchronization, the following circuitry can be used. The circuits shown in Figure A2 momentarily place the OPTIMODEM into Forced-Slave mode on power-up. Holding the OPTIMODEM in Forced-Slave mode for 50 ms will assure synchronization even if the oscillator frequency at either end is exactly the same. As long as the time at which the two ends of a link are powered is different by 50 ms, the first OPTIMODEM powered will be in Normal-Operation mode, while the second is initialized in Forced-Slave mode. Switching from Forced-Slave to Normal-Operation should not effect synchronization once it has been established.

CABLE	200µm Min	100µm Min	62.5µm Min	50µm Min	Units	Notes
1. Transmit power coupled to fiber	640	116	44	20	µW	From LED vendor @I_F = 100 mA See Equation 1 below
2. LED Responsivity	0.05	0.08	0.09	0.10	A/W	From LED vendor
3. LED Output Current	32000	9280	3960	2000	nA	Responsivity x Power
4. Minimum receive sensitivity	1000	1000	1000	1000	nA	CS8123/4 requirement
5. Budget available for cable and splices	15.1	9.8	6.0	3.0	dB	See Equation 2 below
APPLICATION EXAMPLE						
6. Number of splices	6	4	2	0	splices	System design
7. dB of loss per splice	0.5	0.5	0.5	-	dB	From cable vendor
8. km of cable	1.3	1.3	1.0	0.5	km	System design
9. dB of loss/km cable	6	4.5	3.75	3.5	dB	From cable vendor
10. Total cable/splice loss	10.8	7.8	4.75	1.75	dB	See Equation 3 below
11. Operating Margin	4.3	2.0	1.25	1.25	dB	Power - Losses

Note: LED coupled power must be limited (using TCL pin) so that the signal input to receiver is ≤30 µA

Equation 1: If coupled power is specified in dBm, dBm can be converted to Watts by: $10^{(dBm/10)}$ x .001
Equation 2: 10 x log(I_{in}/LED Output Currrent)
Equation 3: (Number of Splices x dB of loss per splice) + (km of cable x dB of loss per km cable)

Table A5. Worst Case Link Budget Calculation for CS8127 LED Performance at 25°C

Link Budget Calculation

Table A5 gives a link budget assuming *worst case* CS8127 LED performance at 25°C. The link budget calculations are based upon the minimum coupled power and responsivity of a CS8127 LED. Note that the 200 µm cable couples much more power to the LED and is therefore preferable for applications where transmission over significantly long links is required. No matter how much current is input to the OPTIMODEM, timing control structures of the OPTIMODEM limit maximum cable length to 1300 meters at a CLKIN rate of 9.216 MHz.

The link budget calculation is also used to ensure that the OPTIMODEM linear channel is not over-driven (30 µA maximum input allowed). See the CS8127 data sheet for more information on estimating link budgets.

Oscillator Requirements

The internal crystal oscillator circuit has been removed from the OPTIMODEM. An external CMOS clock oscillator is required to operate the OPTIMODEM. The specifications for this oscillator are given in Table A6. Oscillators which meet those specifications are readily available from companies such as CTS Knights, Monitor Products and Fox Electronics.

For systems using more than one OPTIMODEM per board, it is acceptable to clock several OPTIMODEMS with one clock source. Note that if two OPTIMODEMS which are intended to communicate with each other are clocked from the same clock source, synchronization will not occur unless one of the OPTIMODEMS is in the Forced-Slave mode.

Layout Considerations

It is recommended that a judicious amount of ground plane be used around LDN, LDP, and the LED pins (on both sides of the board in case of two-layer boards). Trace length from the LED to the LDN and LDP pins on the OPTIMODEM should be kept to a minimum. The receiver is very sensitive and will be adversely affected by noise. Also, physically isolating the OPTIMODEM from potential noise sources on a circuit board is beneficial.

8

Parameter	Symbol	Min	Typ	Max	Units
Frequency		-	9.216000	-	MHz
Frequency Tolerance		-100	-	100	ppm
Duty Cycle (at $0.5V_{IH}$)		40	-	60	%
High Level Output Voltage (for high-impedance load)	V_{IH}	0.9VD+	-	-	Volts
Low Level Output Voltage (for high-impedance load)	V_{IL}	-	-	0.1VD+	Volts
Rise/Fall Time (10% - 90%)		-	-	10	ns

Table A6. External Clock Oscillator Requirements

•Notes•

Semiconductor Corporation

CS8125/6

T1 Optical Line Interface

Features

- Supports Links at 1.544 MHz up to several km
- Supports both single-mode and multi-mode cable
- Receiver Sensitivity: 1 µA to 30 µA
- Selectable Transmit Power Level, 10 mA to 100 mA
- Optical Dynamic Range of 15 dB
- Monolithic Clock Recovery
- 3B4B Data Encoding/Decoding

General Description

The CS8125 and CS8126 from Crystal Semiconductor Corporation are SMART Analog™ interface devices that receive and transmit serial binary data at T1 rates over two fiber-optic cables. Combined with an external LED and PIN diode, the CS8125/6 provide a low-cost, easy-to-design optical link. Long transmission distances can be achieved by using a LASER diode and single-mode fiber. Functions included are 3B4B encoding/decoding, clock recovery, PIN diode amplification, and control of transmitter power.

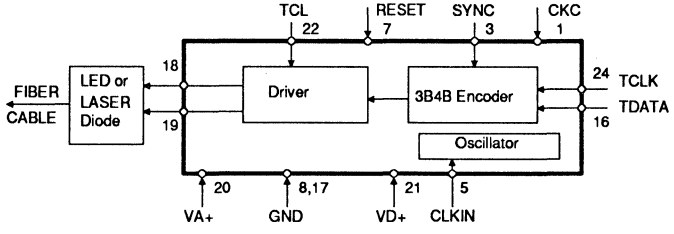
Applications

- Campus Networks
- Secure links
- Links in electrically noisy or hazardous environments

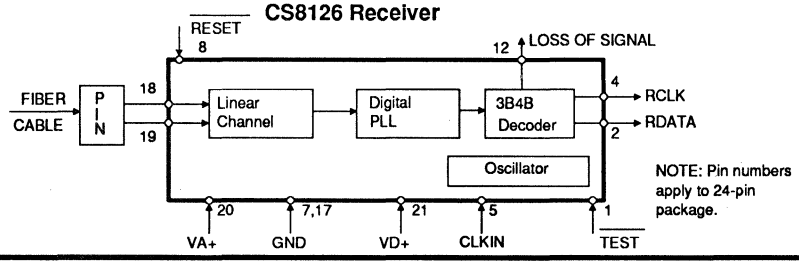
ORDERING INFORMATION:

CS8125-IP5 T1 Transmitter (1.544 Mbps)
CS8126-IP5 T1 Receiver (1.544 Mbps)

CS8125 Transmitter



CS8126 Receiver



NOTE: Pin numbers apply to 24-pin package.

Preliminary Product Information | This document contains information on a new product. Crystal Semiconductor reserves the right to modify this product without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (VA+, VD+ pins)	V+	-0.3	6.0	V
Input Voltage	V_{in}	GND -0.3	(V+) + 0.3	V
Input Current (Note 1) (Any pin except LDP, LDN, VA+, VD+ & GND)	I_{in}	-	10	mA
Storage Temperature	T_{stg}	-65	150	°C
Power Dissipation	P_D	-	500	mW

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at or beyond these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Optical Transmitter Drive Current (Note 2)	I_{out}	90	100	115	mA
Power Consumption, CS8125 (Note 3,4)	P_C	-	375	475	mW
Power Consumption, CS8126 (Note 3,4)	P_C	-	125	150	mW

Note: 2. Measured with TCL floating.
3. Total power dissipated by IC and optical component.
4. Over operating temperature range

DIGITAL CHARACTERISTICS (TA = -40 °C to 85 °C; VA+, VD+ = 5V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 5)	V_{IH}	2.0	-	-	V
High-Level Input Voltage (CLKIN only)	V_{IH}	.9 VD+	-	-	V
Low-Level Input Voltage (Note 5)	V_{IL}	-	-	0.8	V
Low-Level Input Voltage (CLKIN only)	V_{IL}	-	-	.2 VD+	V
High-Level Output Voltage I_{OUT} = -40 uA (Notes 6,7)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA (Notes 6,7)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	± 10.0	-	uA

Notes: 5. Input pins are: TCLK, TDATA, SYNC, $\overline{\text{RESET}}$.
6. Output pins are: RDATA, RCLK, & LOS.
7. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (TA =-40 °C to 85 °C; VA+, VD+ = 5V ± 5%; GND = OV)

Parameter	Symbol	Min	Typ	Max	Units
CS8126 Receiver Input Current	I_{IN}	1	-	30	uA
Transmitter Jitter Tolerance (Note 8)	-	-	12	-	UI p-p

Note: 8. Jitter tolerance increases as jitter frequency decreases.

SWITCHING CHARACTERISTICS (TA = -40 °C to 85 °C; VA+, VD+ = 5V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Frequency	f_c	-	12.352	-	MHz
TCLK & Average RCLK Frequency: (Note 9)	f_{ckc}	-	fc/8	-	kHz
CLKIN, RCLK & TCLK Duty Cycle (Note 10)		45	50	-	%
Rise Time, All Digital Outputs (Note 11)	t_r	-	-	100	ns
Fall Time, All Digital Outputs (Note 11)	t_f	-	-	100	ns
TDATA to TCLK Rising Setup Time	t_{su}	200	-	-	ns
TCLK Falling to TDATA Hold Time	t_h	25	-	-	ns
RDATA to RCLK Rising Setup Time	t_{su}	-	$\frac{1}{2 f_{ckc}}$ -100	-	ns
RCLK Rising to RDATA Hold Time	t_h	-	$\frac{1}{2 f_{ckc}}$ +100	-	ns
Frequency Deviation at TCLK Input from $f_c/8$ (Note 12)		-	-	500	ppm

Notes: 9. Every fourth cycle of RCLK is dropped. The period of those RCLK cycles that are output is $1/6f_c$. See text section on CS8126 optical receiver.
10. Duty cycle is $(t_{pwh}/(t_{pwh} + t_{pwl})) * 100\%$.
11. At maximum load of 1.6 mA and 50 pF.
12. Crystal frequency must be within ± 50 ppm of specified frequency.

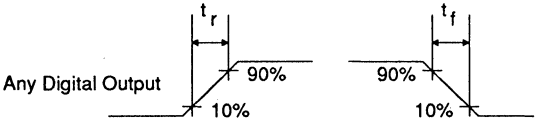


Figure 1. Digital Output Rise and Fall Characteristics

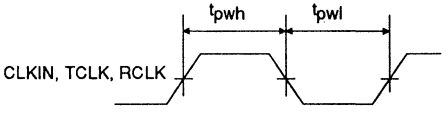


Figure 2. Clock Signal Timing

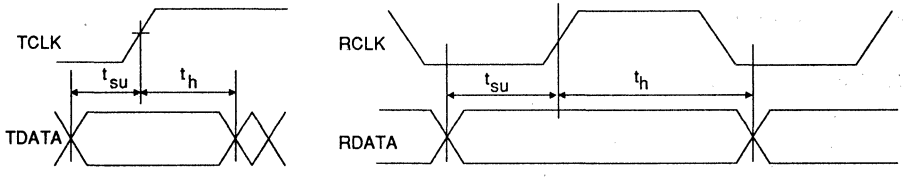


Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

The CS8125 T1 Optical Transmitter and CS8126 T1 Optical Receiver can be used to transport 1.544 Mbps data over several kilometers of multimode fiber. The only external components required are a quartz crystal, an optical emitter (LED) and an optical receiver (PIN diode with biasing circuit), as shown in Figure 6. Transmission distances can be significantly increased by use of single-mode fiber and a LASER diode as an optical transmitter. The only limitation on transmission distance is that sufficient current must be driven into the CS8126 LDN/LDP inputs.

The CS8125 transmitter accepts NRZ input data, sampled on the rising edge of TCLK, and encodes the user data in a 3B4B line code before transmitting onto the fiber. The 3B4B encoding rules are shown in Table 1. 3B4B encoding transmits four bits for every three input to the CS8125 thereby ensuring sufficient ones density to maintain receiver lock even if all zero data is input for transmission. A synchronization pattern can be generated upon user request. The transmit power level is user selectable.

Input binary	Coded binary
001	0011
010	0101
100	1001
011	0110
101	1010
110	1100
000	0010 alternated with 1101
111	1011 alternated with 0100

Table 1. Translation Rules for the 3B4B

The CS8126 receiver accepts 3B4B encoded information, recovers clock, decodes the 3B4B line code and outputs NRZ data which can be sampled using the rising edge of the receive clock output pin, RCLK. A loss of signal output, LOS, indicates when transmission has been interrupted.

Total transmission delay is generally less than 14 bit periods through the CS8125 and 4 bit periods through the CS8126.

CS8125 T1 OPTICAL TRANSMITTER

The CS8125 accepts data on the TDATA input pin on the rising edge of TCLK. The data is encoded using the 3B4B line code before transmission through the external LED or laser. The CS8125 has a current mode driver with sufficient drive current (up to 100 mA) to drive either an LED (for multi-mode cable) or a laser (for single-mode cable).

The transmit current level is typically 100 mA when TCL is left unconnected. The current level may be adjusted, as shown in Figure 4, by tying the TCL pin to ground through a resistor. Tying TCL directly to ground selects the minimum drive current of 10 mA. The output drive current corresponding to a given resistor can be calculated using the following equation:

$$I_{drive} = 100 \left(\frac{110 + R_{TCL}}{1100 + R_{TCL}} \right) mA$$

Equation 1.

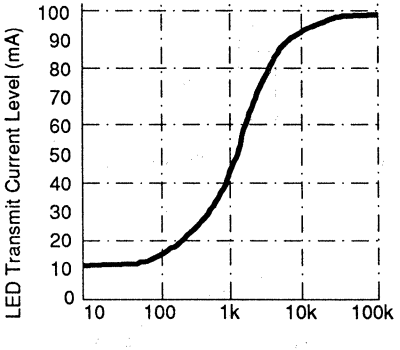


Figure 4. Resistor to Set the Transmit Current Level

The CS8125 requires an 8-times-1.544 MHz external input clock (12.352 MHz). This clock must meet the input requirements of the CLKIN pin: see Table A2 in the Applications section which appends this data sheet. Because of the 3B4B line code used, the actual data rate on the cable is the CLKIN frequency divided by 6.

TCLK may be internally generated or input from an external source based on the state of the Clock Control pin, CKC. If CKC is high, the TCLK output rate is XTL frequency ÷ 8. When CKC is floated or pulled low, TCLK must be externally generated. Externally generated TCLK may deviate from CLKIN ÷ 8 by several hundred ppm. Similarly, the transmit FIFO and internal timing mechanisms can tolerate huge amounts of TCLK jitter.

Under the control of the SYNC pin, the CS8125 will generate a repetitive encoded pattern to achieve 3B4B code alignment of the far-end CS8126 prior to the transmission of data. The far-end CS8126 takes no special action in response to this pattern, other than decoder alignment and normal 3B4B decoding. The CS8126 will synchronize to a random data pattern, but the synchronization time is somewhat unpredictable since it is dependent on the data and the corresponding 3B4B code. The SYNC function ensures receive lock in the shortest possible time.

The synchronization code used is a repetitive 110001 pattern which is encoded as 11000011. The user must maintain SYNC high for 50 ms. When the user returns SYNC low, there will be up to 20 bits (typically 12 bits) of undefined data between the end of the synchronization codes and the start of valid user data as the synchronization codes are flushed from the transmit FIFO.

CS8126 T1 OPTICAL RECEIVER

The external PIN diode detects the data from the far-end CS8125. The PIN diode output signal is input to the CS8126 using the biasing circuit shown in the Application Section of this data sheet. A digital phase-lock loop performs the timing recovery. When the CS8126 is sychronized to the incoming signal; LOS, pin 12, goes low. The 3B4B line code is decoded and the recovered signal is output on RDATA, and may be sampled using RCLK. As a result of the 3B4B decoding, RCLK is output at 4/3 the data rate (crystal-divided-by-6 frequency) with every fourth clock dropped as shown in Figure 5. A CS61600 PCM Jitter Attenuator, or a CS61544's or a CS61535A's on-chip transmit jitter attenuator, can be used to eliminate this line code induced jitter.

The CS8126 establishes a machine cycle which is 96 bit periods long. During its machine cycle, the CS8126 determines how to update its digital PLL to maintain lock on the incoming signal, and monitors the 3B4B code. The CS8126 will declare LOS if there are two 3B4B code violations in four (or fewer) machine cycles. When the CS8126 detects loss of signal, the LOS output pin is set high and a device reset

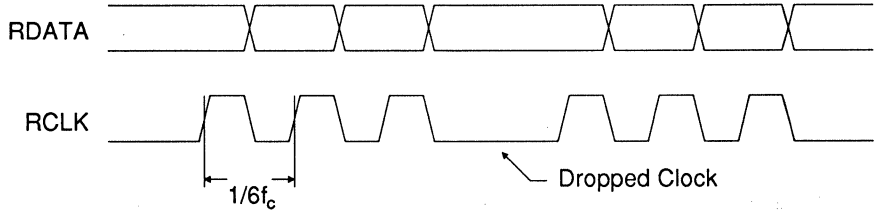


Figure 5. Receiver Output Timing

automatically occurs. A reset clears all internal logic, and the CS8126 attempts to resynchronize to the incoming signal. Synchronization is declared (LOS goes low) when there are no 3B4B code violations for an entire machine cycle. The machine cycle timing is internally established, and not accessable by the user.

When no signal is presented to the LDP/LDN inputs (for example, when no cable is attached to the PIN diode, or if the PIN diode is not attached to LDP/LDN), the LOS output may wink due to nonrandom noise coupling in the receiver. The noise will occasionally mimic a valid 3B4B input code. The typical duration of a LOS low state due to noise is 250 µs. An RC filter can be used on the LOS output to remove the winks. When LOS returns high, the CS8126 does a reset which temporarily interrupts the RCLK output.

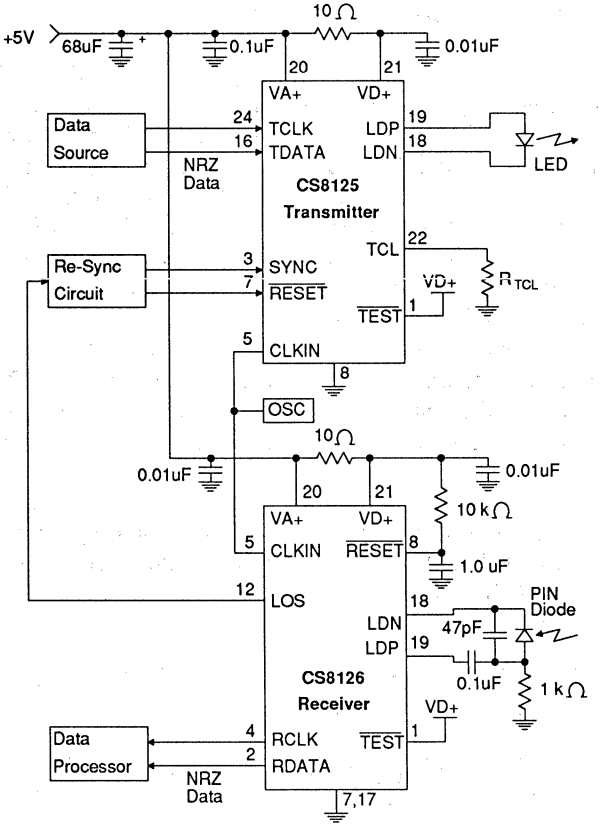
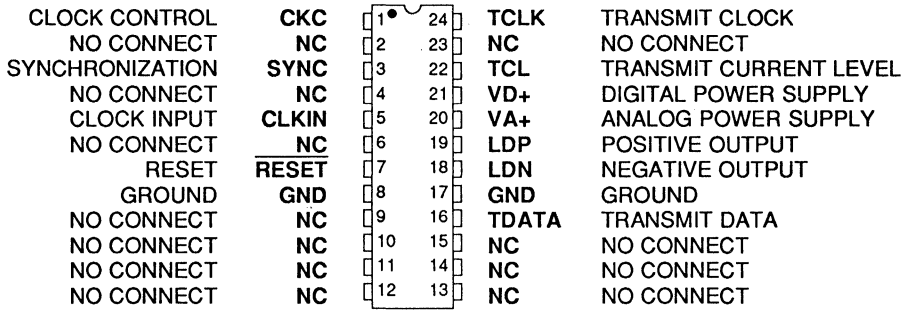


Figure 6. System Connection Diagram For One End of the Communications Link

PIN DESCRIPTIONS



Power Supplies

VA+ - Analog Power Supply, Pin 20.
Typically +5 volts.

VD+ - Digital Power Supply, Pin 21.
Typically +5 volts.

GND - Ground, Pins 8 and 17.
Ground reference.

Oscillator

CLKIN - Clock Imput, Pin 5.
External clock input. T1 operation requires a 12.352 MHz ± 50 ppm external oscillator. Slower frequencies may be used to adjust the data link throughput and data rates. Electrical requirements of the external oscillator are given in Table A2.

Inputs

TDATA, TCLK - Transmit Data, Pin 16; Transmit Clock, Pin 24.
TDATA is data to be transmitted. Data is clocked into the CS8125 on the rising edge of TCLK. TCLK is either a clock input or output depending on the state of the CKC pin. TDATA is sampled on the rising edge of TCLK.

CKC - Clock Control, Pin 1.
CKC defines the source of the TCLK signal. If CKC is left floating or pulled low, an externally-provided clock should be input on TCLK. A high on CKC will result in the CS8125 outputting TCLK at 1.544 MHz (more precisely, at one-eighth of the CLKIN rate).

SYNC - Synchronization Request , Pin 3.

A high level causes a synchronization pattern to be transmitted. SYNC has an internal pull down.

TCL - Transmit Current Level, Pin 22.

Defines the current driven into LDP/LDN. When left unconnected, the current level is typically 100 mA. When tied to ground, output current level is at a minimum of about 10 mA. Current can be set at an intermediate level, (as shown in Figure 4 in the Circuit Description section), by tying this pin through a resistor to ground.

$\overline{\text{RESET}}$ - Reset, Pin 7.

A level sensitive input which causes the CS8125 to reset all of its internal logic when the pin is pulled low. Reset has precedence over every other operational state.

Outputs

LDP; LDN - Laser/LED Positive Output; Laser/LED Negative Output, Pins 19 & 18.

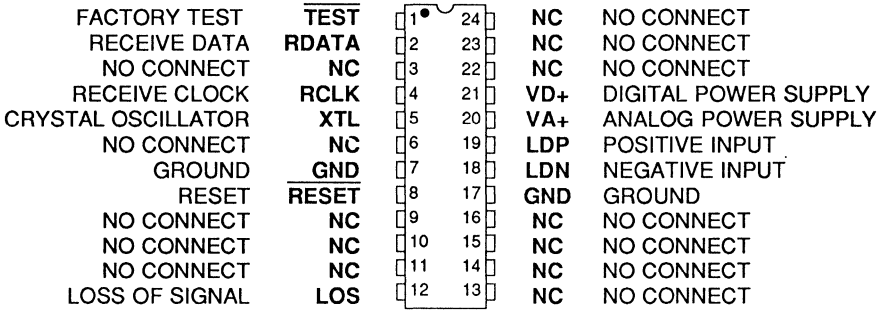
These pins connect directly to the LED or Laser. LDP connects to the optical component anode and LDN connects to the optical component cathode.

No Connects

NC - No Connect, Pins 2, 4, 6, 9-15, 23.

The NC pins must be left floating.

PIN DESCRIPTIONS



Power Supplies

VA+ - Analog Power Supply, Pin 20.
Typically +5 volts.

VD+ - Digital Power Supply, Pin 21.
Typically +5 volts.

GND - Ground, Pins 7 and 17.
Ground reference.

Oscillator

CLKIN - Clock Imput, Pin 5.
External clock input. T1 operation requires a 12.352 MHz ± 50 ppm external oscillator. Slower frequencies may be used to adjust the data link throughput and data rates. Electrical requirements of the exturnal oscillator are given in Table A2.

Inputs

LDP; LDN - PIN Diode Positive Input; PIN Diode Negative Input, Pins 19 & 18.
These pins connect to the PIN diode through the biasing circuit show in the application section.

$\overline{\text{RESET}}$ - Reset, Pin 8.
A level sensitive input to the CS8126 which resets all of its internal logic when the pin is pulled low. After reset, the data recovery circuit must resynchronize to the incoming data stream. Reset has precedence over every other operational state.

$\overline{\text{TEST}}$ - Factory Test, Pin 1.
Must be tied to logic high for normal operation. This pin should be connected to VD+ or to the supply through a 10kΩ resistor.

Outputs

LOS - Loss of Signal, Pin 12.

A high level indicates that the CS8126 is not synchronized. LOS goes low to indicate that the CS8126 is synchronized to the incoming data.

RDATA, RCLK - Received Data, Pin 2; Received Clock, Pin 4.

RDATA is valid and stable on the rising edge of RCLK

No Connects

NC - No Connect, Pins 3, 6, 9-11, 13-16, 22-24.

The NC pins must be left floating.

APPLICATION NOTES

The use of a CDB8125/6 Evaluation Board to evaluate an optical link is highly recommended because system performance is highly dependent upon the quality of the board layout.

Power Supply Decoupling

VA+, VD+ and GND should be decoupled using the circuit shown in Figure A1. The 68 µF capacitor is required to filter the power supply, and prevent power supply ripple, and should placed close to the CS8125/6. The 0.1 µF capacitor and 0.01 µF capacitor should be placed as close as possible to the CS8125/6. Any other ICs on the same board or sharing the same power supply should also be decoupled.

Because of the sensitivity of the analog circuitry to power supply noise, evaluation of the CS8125/6 using wire-wrapped boards is not recommended.

Inexpensive Fiber Optic Cables and LED's

Hewlett-Packard's LED's for plastic fibers (the VERSATILE HFBR-152x family) can be used for very low cost links. These LED's are approximately one-third the cost of the glass-fiber compatible LED's. However, the length of the cable is limited by the attenuation characteristics of plastic fiber (about 1dB per meter).

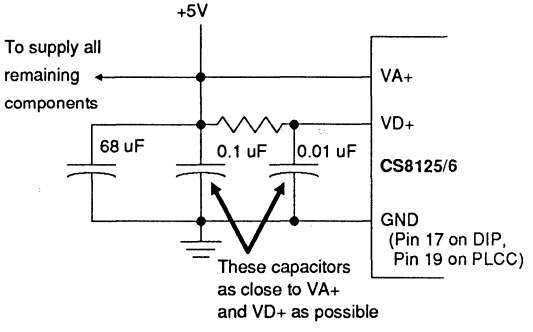


Figure A1. Power Supply Decoupling

Calculating a Link Budget

A link budget is used to determine the range of fiber lengths and operating margin for a CS8125 to CS8126 link. The link budget takes into account: the power coupled to the fiber from the optical transmitter, the loss of the fiber, and the responsivity of the optical receiver. Fiber coupled power and responsivity are significantly affected by temperature. The wavelength of the transmitted light will also change with temperature. Responsivity of the receiver diode will vary with wavelength. Optical transmitters and receivers must be compatible (operate at the same wavelength). Losses due to splices and environmental factors, etc. must be considered when calculating a link budget.

Fiber coupled power depends on the numerical aperture and diameter of the fiber, with larger diameter fiber coupling significantly more light power than small diameter fiber. Fiber coupled power varies in inverse proportion to temperature. The loss of a fiber is generally expressed in dB/km. The larger the diameter of the fiber, the greater the loss of light power. Loss will be slightly greater for short (much less than 1 km) fibers. Responsivity is a measure of the amount of current generated by a diode when light is shined on it and is expressed in amps/watt of light power. Responsivity is dependent on wavelength and varies in proportion to temperature. Table A1 shows some parameters for calculating link budgets for different fiber diameters when using a typical LED transmitter and PIN diode receiver.

To calculate the maximum cable length for 100/140 µm fiber at a fixed temperature, first calculate the amount of light power needed at the PIN diode to generate 1 µA of output current (the minimum required by the CS8126).

$$P_{Rx} = \frac{1\ uA}{0.24\ A/W} = 4.17\ uW$$

8

Cable Type	NA	Fiber Loss	LED Launch Power	PIN Responsivity
200 µm	0.37	6 dB/km	640 µW	0.15 A/W
100/140 µm	0.30	4.5 dB/km	116 µW	0.24 A/W
62.5/125 µm	0.275	3.75 dB/km	44 µW	0.27 A/W
50/125 µm	0.20	3.5 dB/km	20 µW	0.30 A/W

Table A1. Typical Link Budget Values

The allowable loss due to cable and splices is:

Power Margin = 10 log(launched power / P_{Rx})
= 10 log(116µW/4.17µW)
= 14.44 dB

Cable loss is 4.5 dB/km which would allow a transmision distance of 3.21 km, max. Selecting an LED with more output power and a PIN with more responsivity will allow longer transmission distances. It is wise to allow about 3 dB of operating margin, and transmission media loss due to splices or other factors should also be accounted for.

If the ends of the link are expected to be at different temperatures, additional margin should be provided to compensate for loss in performance of the LED and PIN. If the temperature increases or decreases at both ends of the link such that the two ends remain within a few degrees of each other, the link budget will remain essentially the same. Loss in performance at one end is compensated for by improved performance at the other end.

CS8126 PIN Diode Biasing Circuit

The object of the circuit is to provide a 2.5 V reverse bias on the PIN diode, and approximately a 47 pF load to LDP/LDN. In addition, the 47 pF capacitor shunting the LDN & LDP pins ensures the stability of the receiver. With a noisy ground environment, an optional 20 pF capacitor from LDN to ground may be required. This capacitor couples noise into LDN that is equal to noise coupled into LDP by the resistor.

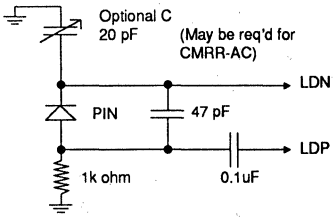


Figure A2. PIN Diode Biasing

Oscillator Specifications

Table A2 gives the specifications for the external clock oscillator.

Layout Considerations

It is recommended that a healthy amount of ground plane be used around LDP and LDN, and the LED pins (on both sides of the board in case of two-layer boards); and also around the oscillator.

Resynchronization Considerations

The RESET-SYNC circuit shown in Figure A3 is intended to ensure minimum synchronization time upon power-up or after a Loss of Signal, LOS, condition occurs. If transmission of a normally functioning link is interrupted, the LOS pin on the CS8126 will go high. The RESET portion

Parameter	Symbol	Min	Typ	Max	Units
Frequency T1		-	12.352000	-	MHz
Frequency Tolerance		-100	-	100	ppm
DutyCycle (at 0.5V_{IH})		0.9VD+	-	55	%
High Level Output Voltage, (for high-impedance load)	V_{IH}	0.9VD+	-	-	Volts
Low Level Output Voltage, (for high-impedance load)	V_{IL}	-	-	0.1VD+	Volts
Rise/Fall Time (10% - 90%)		-	-	10	ns

Table A2. External Clock Oscillator Requirements

of the circuit will cause a short reset of the CS8125. This reset interrupts transmission, thereby causing a LOS condition to occur at the far end of the link, which in turn resets the far end CS8125. Both CS8125s will transition from the RESET condition to the SYNC state, which will ensure minimum synchronization time. The CS8125 will stay in the SYNC state until after the CS8126 has established synchronization.

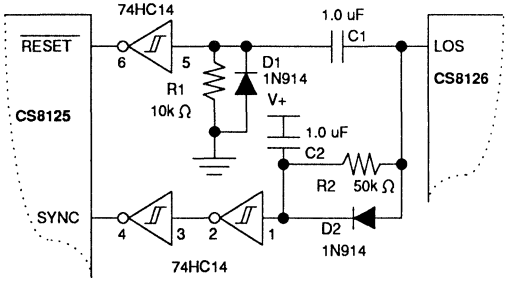


Figure A3. RESET-SYNC Circuit.

Repeating

For recovery and retransmission of the signal, simply connect a CS8126 RCLK and RDATA outputs to the TCLK and TDATA inputs of a CS8125. It is not necessary to clean up the CS8126 RCLK output.

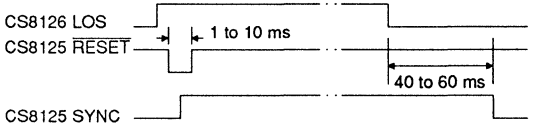


Figure A4. Resynchronization Timing

8

• Notes •

Semiconductor Corporation

CS8127

Light Emitting /Detecting Diode

Features

- Supports bi-direction communication when used with the CS8123 and CS8124 OPTIMODEM™
- Compatible with the CS8125 T1 Optical Driver
- Couples efficiently into 50/125 µm, 62.5/125 µm, 100/140 µm and 200 µm PCS cables
- Power coupled to 50/125 µm cable is typically 40 µW.
- Responsivity as receiver is typically 0.20A/W with 50/125 µm fiber
- ST-Connector

General Description

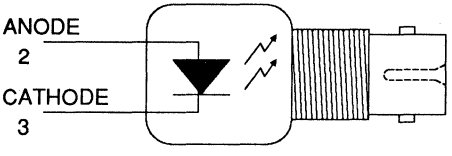
The CS8127 light emitting and detecting diode is designed to support bi-directional, ping-pong communication over a single optical cable. In bi-directional applications, the CS8127 acts alternately as a transmitter and as a receiver. Transmitter output is typically 40µW @ I_F = 100mA. Receiver responsivity is typically 0.20 A/W. At these performance levels, the CS8127 can support CS8123/4 transmission distances of up to 1km using 50/125 fiber with 3dB of headroom.

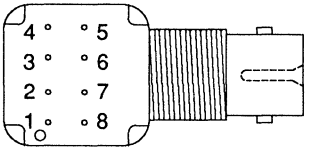
The CS8127 is offered in a Plastic Fiber DIP package compatible with ST type connectors. The CS8127 is intended to operate with graded index multimode fibers with diameters ranging from 50/125 to 200µm.

ORDERING INFORMATION:

CS8127- IP1

I - -40° to +85°C Temperature Range
P - Plastic Fiber DIP package ST type connector
1 - Performance grade (fiber coupled power and responsivity)





BOTTOM VIEW

Pin	Function
1	NC
2	ANODE
3	CATHODE
4	NC
5	NC
6	NC
7	NC
8	NC

8

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Continuous Forward Current	I_F	-	100	mA
Reverse Breakdown Voltage I_R = 10µA		2.0	-	V
Case to Cathode (Anode) Voltage		-	110	V
Storage Temperature	T_{STG}	-65	150	°C
Case Operating Temperature	T_C	-40	85	°C

ELECTRO-OPTICAL CHARACTERISTICS (T_C = 25 °C)

Parameter		Symbol	Min	Typ	Max	Units
Emitter						
Forward Voltage	I_F = 100mA	V_F	-	1.7	2.0	V
Fiber Coupled Power I_F = 100mA (Note 1)	50µm fiber 62.5µm fiber 100µm fiber 200µm fiber	P_{OC}	20 44 116 640	40 88 232 1280	- - - -	µW
Peak Wavelength	I_F = 100mAdc	λ_E	840	850	860	nm
Spectral Bandwidth (-3dB points)	I_F = 100mAdc	$\Delta\lambda$	-	50	-	nm
Response Time 10-90%	1V prebias, I_F = 100mA$_{peak}$	t_R t_F	- -	12 15	20 20	ns
Power Output Temperature Coefficient	50µm fiber I_F = 100mA	$\Delta P_O/\Delta T$	-	-0.01	-	dB/°C
Peak Wavelength Temperature Coefficient	50µm fiber, I_F = 100mA	$\Delta\lambda p/\Delta T$	-	+0.25	-	nm/°C
Detector						
Dark Leakage Current	V_R = 1V	I_D	-	0.5	20	nA
Responsivity λ_D = 850nm (Note 1)	50 µm fiber 62.5µm fiber 100µm fiber 200µm fiber	R	0.10 0.09 0.08 0.05	0.20 0.18 0.16 0.10	- - - -	A/W
Package Capacitance	V_R = 0V, f = 1MHz	C	30	55	80	pF
Response Time, 10-90%	V_R = 0V, λ_D = 850nm	t_R t_F	- -	7 4	20 20	ns ns
Responsivity Temperature Coefficient	50µm fiber λ_D = 850nm	$\Delta R/\Delta T$	-	+0.93	-	%/°C
Responsivity Wavelength Coefficient	50µm fiber λ_D = 850nm	$\Delta R/\Delta\lambda$	-	-3.7	-	%/nm

Note: 1. Parameter tested for 1 m of 50 µm fiber. Values for larger diameter are based on calculations relative to 50 µm fiber.

Specifications are subject to change without notice.

Typical Emitter Performance

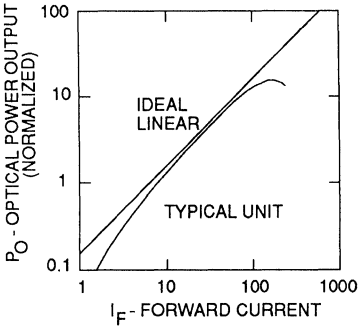


Figure 1. Relative Power Out vs Forward Current

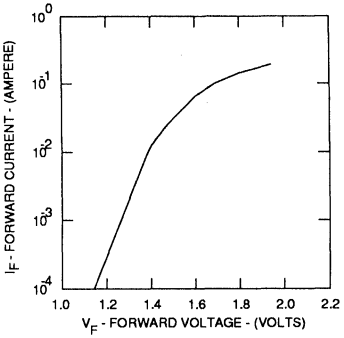


Figure 2. Forward Current vs Forward Voltage

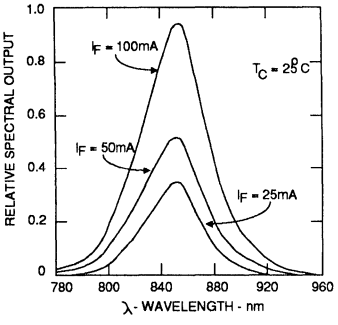


Figure 3. Relative Spectral Output vs Wavelength

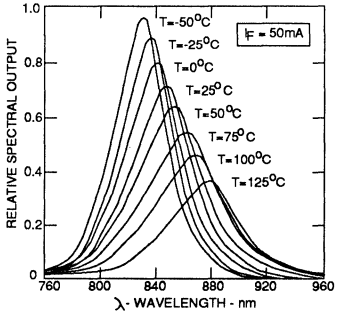


Figure 4. Spectral Output vs Temperature

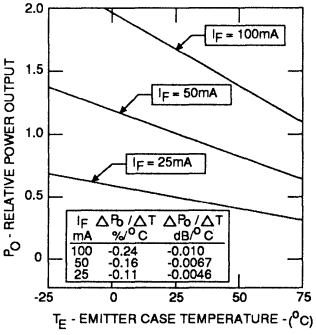


Figure 5. Power Output vs Temperature

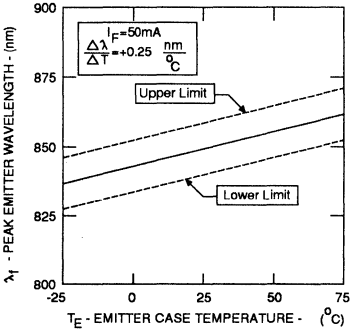


Figure 6. Emitter Peak Wavelength vs Temperature

8

Emitter/Detector Performance

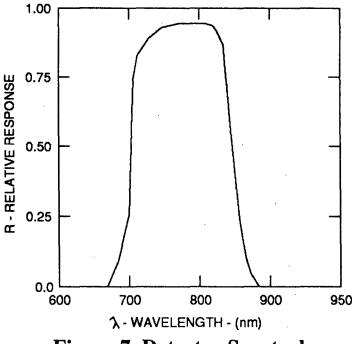


Figure 7. Detector Spectral Response vs Wavelength

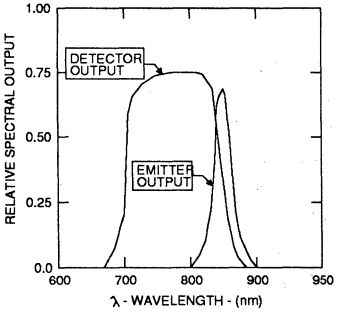


Figure 8. Emitter/Detector Spectral Output vs Wavelength

Typical Detector Performance

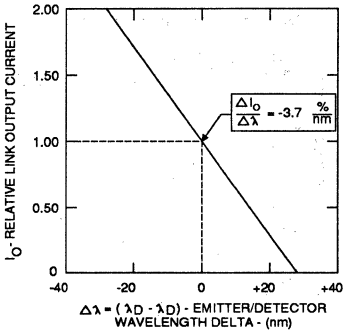


Figure 9. Relative Link Output Current vs Emitter/Detector Wavelength Delta

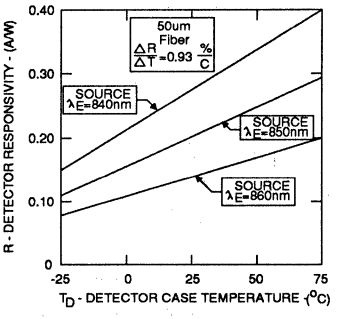


Figure 10. Detector Responsivity vs Detector Temperature

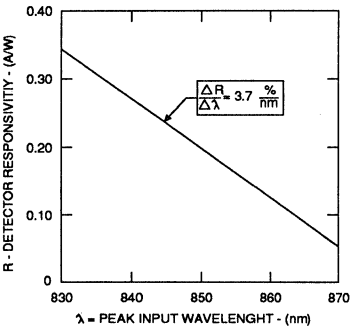


Figure 11. Detector Responsivity vs Wavelength

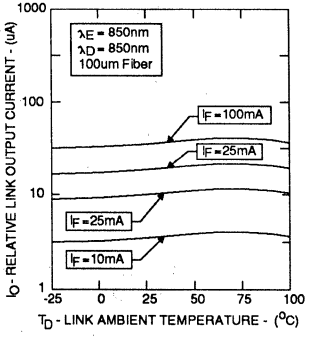


Figure 12. Link Output Currrent vs Link Temperature

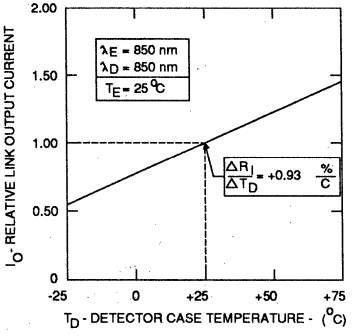


Figure 13. Relative Link Output vs Detector Temperature

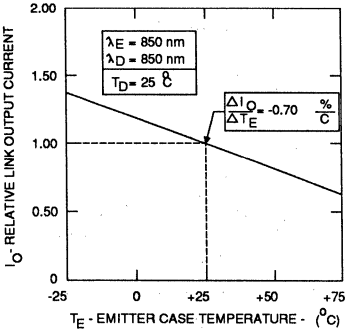


Figure 14. Relative Link Output vs Emitter Temperature

The CS8127 is intended to be used with Crystal's CS8123 and CS8124 OPTIMODEM products. The CS8127 can also be used with the CS8125 PCM transmitter and CS8126 PCM receiver. Excellent light power output and responsivity characteristics distinguish the CS8127 from transmit only LEDs and receive only PIN diodes. The CS8127 is capable of supporting transmission distances of 1 km over 62.5/125 µm fiber with nearly 3 dB of operating margin.

Calculating a Link Budget

A link budget should be calculated to ensure that the current generated by the LED in receive mode is between 1 µA and 30 µA (the limits of the CS8123/4 LDN/LDP inputs). Power coupled to the fiber, the attenuation characteristics of the fiber, loss due to splices or interconnects, the responsivity of the LED, and variations due to temperature must all be considered when calculating a link budget.

The following is an example of a link budget for transmission over 1 km of 62.5/125 µm fiber with both ends at 25°C.

Fiber coupled power for 62.5/125 µm fiber = 44 µW, min
Loss (Fiber attenuation): 3.75 dB/km
Light power at end of fiber: $44x10^{(-3.75/10)}$
= 18.55 µW
Responsivity for 62.5/125 µm fiber: 0.09 A/W, min
Current out of LED (receiving): 18.5 µWx0.09 A/W
= 1.67 µA

Since output power and responsivity are based on minimum performance values for the CS8127, 1.67 µA of output current represents the minimum, worst case output current. The minimum light power needed to generate 1 µA of current is 11.11 µW, so the operating margin is at least 2.25 dB.

Now consider temperature which affects wavelength, transmit power and responsivity. If the temperature increases at both ends of the link by 50°C, calculate the resulting change in performance.

Change in transmitted wavelength:
$\Delta\lambda_E$ = +0.25 nm/°C
850 nm + (0.25 nm/°C)(50°C)
= 862.5 nm
Change in responsivity due to wavelength:
ΔR_λ = -3.7 %/nm
0.09 A/W + (-3.7 %/nm)(12.5 nm)
= 0.09 A/W - 46.2 %
= 0.048 A/W
Change in output power due to temperature:
$\Delta P_{OC(temp)}$ = -0.01 dB/°C
44 µW + (-0.01 dB/°C)(50°C)
= 44 µW - 0.5 dB
= 39.2 µW
Change in responsivity due to temperature:
ΔR_{temp} = +0.93 %/°C
44 µW + (0.93 %/°C)(50°C)
= 0.09 A/W + 46.5 %
= 0.132 A/W
Totals: Transmission change:
44 µW - 11%
= 39.2 µW
Receiver change:
0.09 A/W - 46.2 % + 46.5 %
= 0.09 A/W

The change in performance is minimal as long as both ends are at the same temperature.

Now consider the case where the transmitter is at 50°C and the receiver is at 0°C. Following the same calculations for +25°C delta on the transmitter and -25°C delta for the receiver:

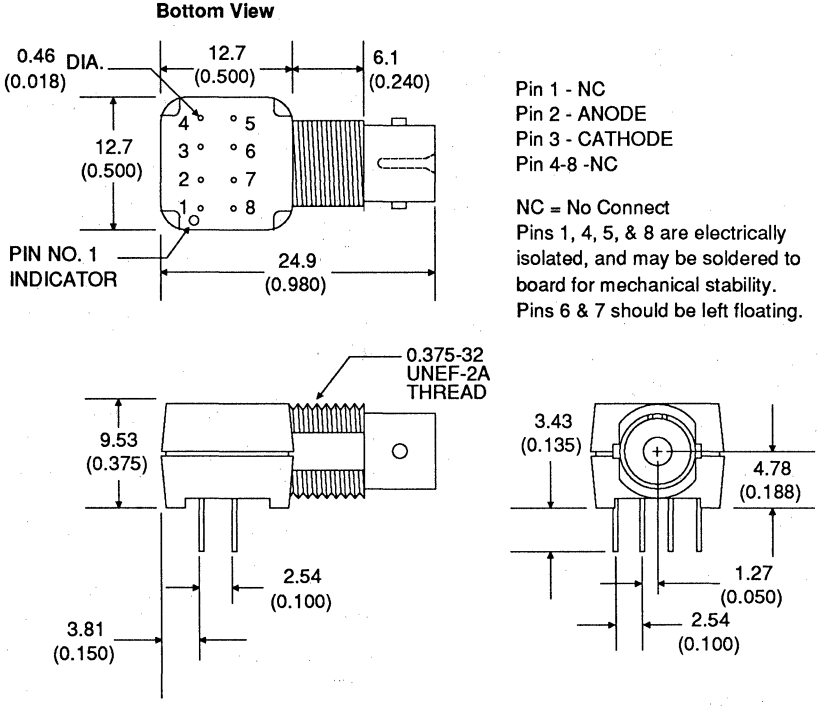
$\Delta\lambda_E$ = +6.25 nm
$\Delta P_{OC(temp)}$ = -0.25 dB or -5.6 %
ΔR_λ = -23.1 %
ΔR_{temp} = -23.3 %

This shows that 5.6 % of the output power, and 46.4 % of the receiver performance is lost which translates to 3.55 dB. The loss of 3.55 dB due to temperature difference between the ends of the link exceeds the 2.25 dB margin calculated for 1 km of 62.5/125 µm fiber. To be assured of reliable operation when the ends of the link will differ by 50°C either the length of 62.5/125 µm fiber must be reduced, or larger diameter fiber is required.

When using large diameter fiber for short distances, take care not to exceed the 30 µA max input current of the CS8123 or CS8124. The TCL pin can be used to limit the output drive current thereby reducing the power coupled to the fiber.

The CS8127 is specified to withstand up to 100 mA of continuous current while the CS8123/4 specifications indicate that their maximum output current is 115 mA. In normal operation, the OPTIMODEM is driving the LED a fifth of the time. In this case, the 115 mA of output currrent is not continuous and will not damage the CS8127.

Mechanical Specifications



All dimensions in millimeters and (inches).

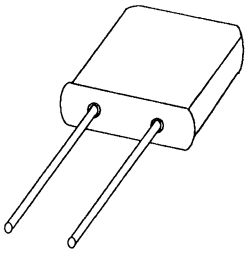
Semiconductor Corporation

CXT9216

Quartz Crystal

Features

- Crystal Intended for Use with CS8123 and CS8124
- Low Equivalent Series Resistance



General Description

The CXT9216 is intended to be used with the CS8123 and CS8124 OPTIMODEM™ chips. The frequency setting and series resistance comply with OPTIMODEM™ requirements.

DISCONTINUED

8

The CS8123 and CS8124 no longer support an on-chip oscillator.

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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• Notes •

INTRODUCTION

The CS1232 compares the system power supply to an on-chip band gap voltage reference and signals if supplies fall below 4.6 volts. This permits the host microprocessor to gracefully power down the system before supplies fail. Critical system parameters can be saved in non-volatile memory for reinitialization when power supplies return to rated levels. The CS1232 also contains a watchdog timer and pushbutton reset circuit. The CS1232 is pin and functionally compatible with the Dallas Semiconductor DS1232

CONTENTS

Semiconductor Corporation

CS1232

Micromonitor

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- 8-pin Mini-DIP or 16-pin SOIC
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

The power status (Vcc) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when Vcc goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after Vcc returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

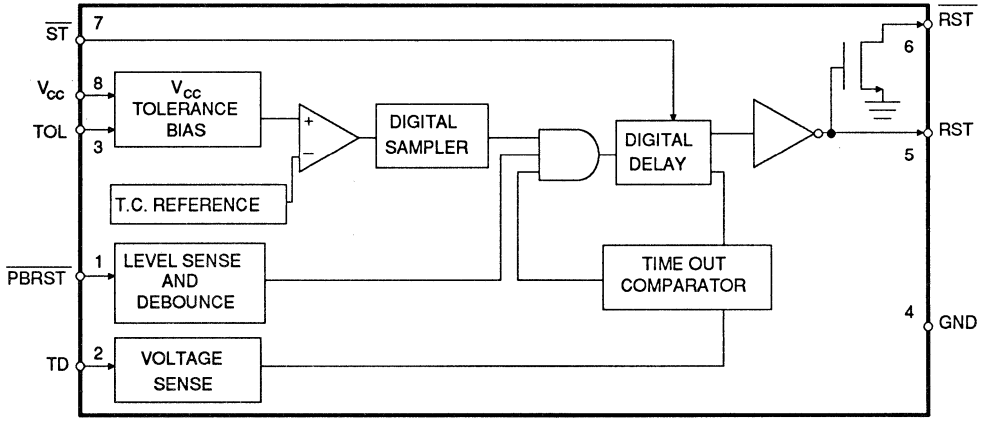
The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

A surface mount 16-pin SOIC is available, as well as an 8-pin Plastic DIP.

ORDERING INFORMATION:

Model	Temp. Range	Package
CS1232- P	0 °C to 70 °C	8-pin Plastic DIP
CS1232-IP	-40 °C to +85 °C	8-pin Plastic DIP
CS1232- S	0 °C to 70 °C	16-pin SOIC
CS1232-IS	-40 °C to +85 °C	16-pin SOIC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter			Symbol	Min	Typ	Max	Units
V_{CC} Trip Point	(Note 1)	TOL = GND	V_{CCTP}	4.50	4.62	4.74	V
		TOL = V_{CC}	V_{CCTP}	4.25	4.37	4.49	V
Operating Current	(Note 2)		I_{CC}	-	0.4	2.0	mA

Notes: 1. All voltages referenced to ground.
2. Measured with outputs open.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
Operating Temperature	CS1232		0	-	+70	°C
	CS1232-I		-40	-	+85	°C
Supply voltage	(Note 1)	V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter			Symbol	Min	Typ	Max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level		(Note 1)	V_{IH}	2.0	-	V_{CC}+0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level		(Note 1)	V_{IL}	-0.3	-	+0.8	V
Output High Current at 2.4 V	RST only		I_{OH}	-8.0	-10.0	-	mA
Output High Voltage at -500 µA	RST only	(Note 3)	V_{OH}	V_{CC}-0.5	V_{CC}-0.1	-	V
Output Low Current at 0.4 V	RST, $\overline{RST}$		I_{OL}	8.0	10.0	-	mA
Input Leakage		(Note 4)	I_{IL}	-1.0	-	+1.0	µA
Input Capacitance		T_A = 25°C	C_{IN}	-	-	5	pF
Output Capacitance		T_A = 25°C	C_{OUT}	-	-	7	pF

Notes: 3. On power-down, RST typically remains within 0.5V of V_{CC} (and $\overline{RST}$ typically remains within 0.5V of GND) until V_{CC} falls below 2.0V.
4. $\overline{PBRST}$ is internally pulled up to V_{CC} with a 100 kΩ resistor. TD is internally pulled up to V_{CC} with a 100 kΩ resistor and pulled down to ground with a 100 kΩ resistor.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Typ	Max	Units
Voltage on Any Pin Relative to Ground	-1.0	-	+7.0	V
Input Current	-	-	±10	mA
Storage Temperature	-55	-	+125	°C
Soldering Temperature	260 °C tor 10 sec			

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{PBRST}$ = V_{IL}	t_{PB}	-	20	-	ms
RESET Active Time	t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	20	-	-	ns
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}	-	-	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V	t_F	300	-	-	µs
V_{CC} Detect to RST and $\overline{RST}$ (Note 5)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V	t_R	0	-	-	ns
$\overline{ST}$ Pulse Period (Note 6) TD pin at Ground	t_{TD}	50.0	150	250	ms
TD pin floating	t_{TD}	250	600	1000	ms
TD pin connected to V_{CC}	t_{TD}	400	1200	2000	ms

Note: 5. t_R = 5 µs
6. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.
7. $\overline{RST}$ is an N-channel open drain output.

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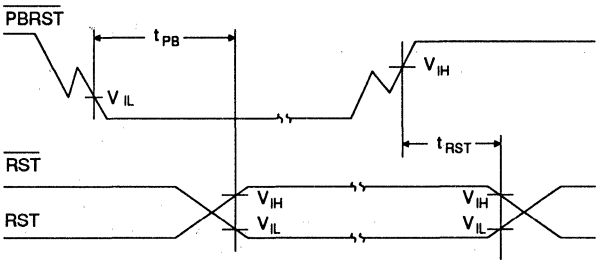
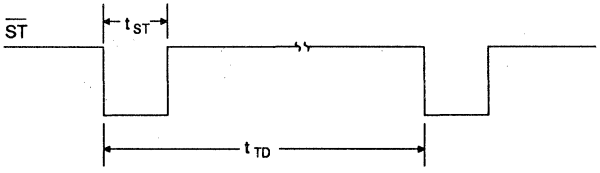
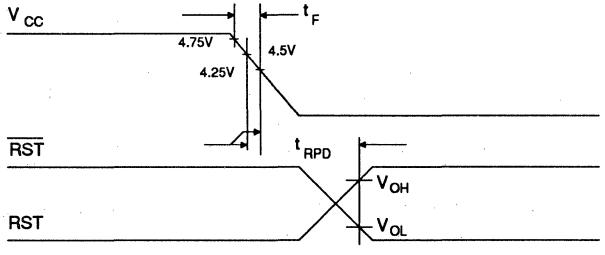


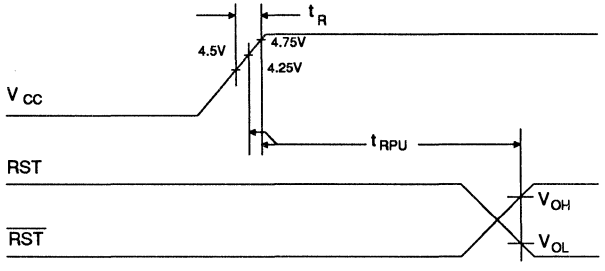
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

POWER SUPPLY MONITOR

The CS1232 will detect out-of-tolerance power supplies for processor-based systems as well as warn of an impending power failure. The TOL digital input pin defines the threshold level for V_{CC}; when the V_{CC} level drops below the TOL defined level, the CS1232 asserts the signals RST and $\overline{RST}$. The threshold level is set to typically 4.37 V if TOL is connected to V_{CC}, and is set to typically 4.62 V if TOL is connected to GND. The processor is allowed to continue until the last possible moment that V_{CC} is valid. Upon return of power, RST and $\overline{RST}$ are active for 250 ms (minimum) to allow stabilization.

PUSHBUTTON RESET CONTROL

$\overline{PBRST}$ is normally connected to a reset pushbutton (see Figure 1). This active low signal is debounced and timed to generate signals of 250 ms (minimum) for RST and $\overline{RST}$. The delay begins when $\overline{PBRST}$ is released from from the low state. $\overline{PBRST}$ has an internal 100 kΩ pull-up resistor.

WATCHDOG TIMER

When RST and $\overline{RST}$ become inactive (normal CPU operation), the watchdog timer starts timing out, using the time set by TD. RST and $\overline{RST}$ are forced active when $\overline{ST}$ is not stimulated for this predetermined time. TD sets the time to be: 150 ms if TD is connected to ground, 600 ms is TD is not connected, or 1.2 seconds with TD connected to V_{CC}. RST and $\overline{RST}$ are driven active for 250 ms (minimum) if no high-to-low transition occurs on the $\overline{ST}$ input pin before time out. Microprocessor address signals, data signals, control signals, and output port bits can be used for the $\overline{ST}$ input pin. These signals cause the watchdog timer to be reset prior to time out indicating normal function of the microprocessor (see Figure 2).

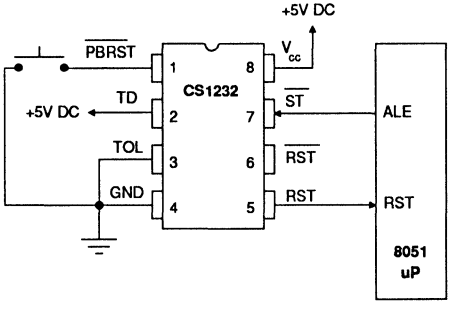


Figure 1. Pushbutton Reset

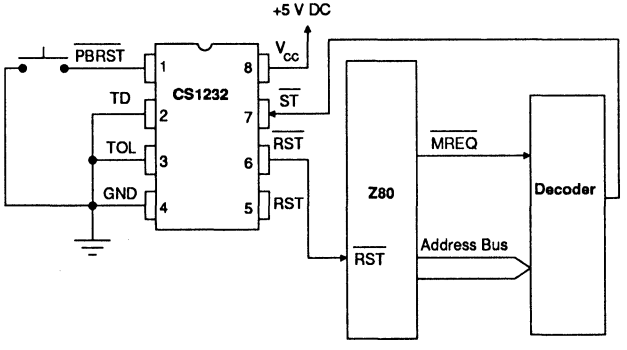


Figure 2. Watchdog Timer

PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	1	8	Vcc	+5 VOLT POWER
TIME DELAY SET	TD	2	7	$\overline{\text{ST}}$	STROBE INPUT
SELECTS Vcc DETECT LEVEL	TOL	3	6	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain)
GROUND	GND	4	5	RST	RESET OUTPUT (Active High)

NO CONNECTION	NC	1	16	NC	NO CONNECT
PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	2	15	Vcc	+5 VOLT POWER
NO CONNECT	NC	3	14	NC	NO CONNECTION
TIME DELAY SET	TD	4	13	$\overline{\text{ST}}$	STROBE INPUT
NO CONNECT	NC	5	12	NC	NO CONNECT
SELECTS Vcc DETECT LEVEL	TOL	6	11	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain)
NO CONNECT	NC	7	10	NC	NO CONNECT
GROUND	GND	8	9	RST	RESET OUTPUT (Active High)

INTRODUCTION

High-quality evaluation boards are available to allow rapid evaluation of Crystal products, often freeing the customer from the task of initial breadboarding. The layout and grounding schemes may be used as guidelines for the customer's own system design. Isolation of system problems can be aided by comparison with the evaluation board operation.

USER'S GUIDE

Device:	Crystal Part Included	Basic Function
CDB6152	CS6152-P	Low Power T1 Line Interface
CDB61534	CS61534-P	PCM Line Interface
CDB61535	CS61535-P	PCM Line Interface
CDB61574	CS61574-P	PCM Line Interface
CDB61575	CS61575-P	PCM Line Interface
CDB6158	CS6158-P	PCM Line Interface
CDB61535A	CS61535A-P	PCM Line Interface
CDB61574A	CS61574A-P	PCM Line Interface
CDB6158A	CS6158A-P	PCM Line Interface
CDB61544	CS61544-P	T1 Line Interface
CDB6159	CS6159-P	Low Power PCM Line Interface
CDB8123	CS8123-P	OPTIMODEM™
CDB8124	CS8124-P	OPTIMODEM™
CDB8125/6	CS8125-P & CS8126-P	Optical Line Interface

CONTENTS

Semiconductor Corporation

CDB6152

Evaluation Board for CS6152

Features

- Socketed CS6152 Line Interface IC
- All Required Components for Complete Line Interface Evaluation
- DIP Switch Configuration of all CS6152 Control Inputs
- LED Status Indicator for CS6152 Driver Performance Monitor Output

General Description

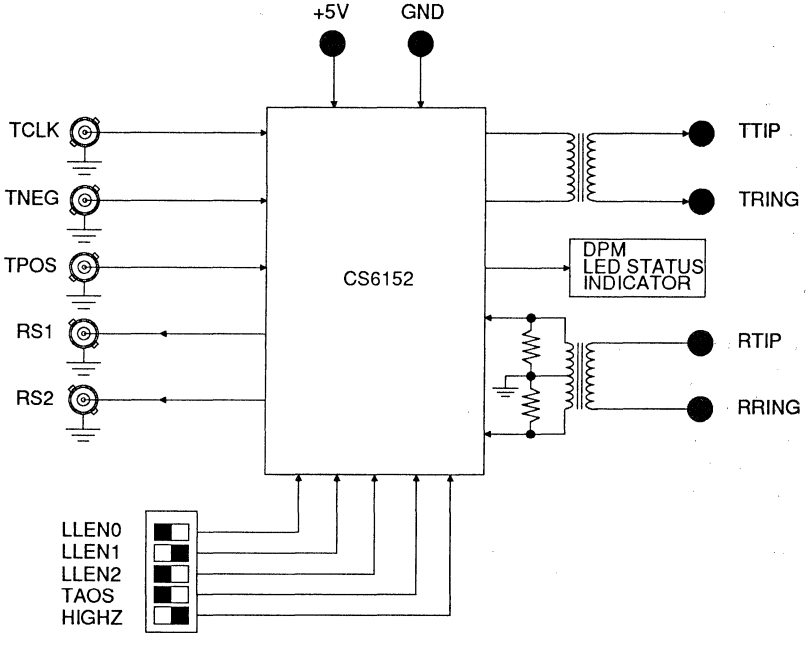
The evaluation board includes a CS6152 line interface IC and all support components required for evaluation. The board is powered by an external 5 Volt supply.

The board features four binding post connectors for connecting two 100Ω twisted pair T1 lines to the transformers on the board. BNC connectors allow easy access to the digital transmit clock and data inputs and the digital receiver data outputs.

An LED status indicator is provided for monitoring the CS6152's Driver Performance Monitor (DPM) output. A DIP switch is provided for configuring the CS6152's control input pins: LEN0, LEN1, LEN2, TAOS, and HIGHZ.

ORDERING INFORMATION: CDB6152

Block Diagram



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

CIRCUIT DESCRIPTION

Power Supply

As shown in the schematic in Figure 1, power is supplied to the evaluation board from an external +5 Volt supply connected to the two binding posts labled +5V and 0V. D1 is a transient suppressor which protects the components on the board from overvoltage damage and reversed supply connections. The supply decoupling recommended in the CS6152 data sheet is provided on the board by C1, C2 and C4. C2 is the 1.0µF decoupling capacitor which decouples TV+ to TGND. Similarly, the parallel combination of C1 (a 0.1µF ceramic capacitor) and C4 (a 68µF capacitor) is used to decouple RV+ to RGND. The CS6152 TV+ and RV+ leads are tied together at the IC.

Transmit Circuit

The CS6152's digital transmitter inputs are brought in through the BNC connectors labeled TCLK, TPOS and TNEG for the transmit clock and NRZ data respectively. The transmitter output is coupled onto a 100Ω twisted pair T1 line at the TTIP and TRING binding posts using a 1:1.36 step-up transformer (X1). C3 is the 0.47µF blocking capacitor recommended in the CS6152 data sheet.

Receive Circuit

The CS6152's receiver inputs are transformer coupled to the T1 twisted pair cable connected to the RTIP and RRING binding posts on the board. A center-tapped, center-grounded, 1:2 transformer, X1, is used to provide equal amplitude pulses of opposite polarity to the RTIP and RRING pins of the CS6152. R1 and R2 are 200Ω resistors which terminate the T1 line with 100Ω. The CS6152's digital receiver outputs are brought out to the BNC connectors labeled RS1 and RS2.

Control Circuit

The CS6152 digital control inputs are configured using the DIP switch SW1. Placing a switch in the "on" position grounds the corresponding pin of the same name placing it in the logic "0" or "off" state. LLEN0, LLEN1 and LLEN2 select the transmitter line length setting as described in the CS6152 data sheet. TAOS selects the transmission of all ones at the TCLK frequency. HIGHZ causes TTIP, TRING, R1 and R2 to enter a high impedance state.

Driver Performance Monitor

An LED status indicator is provided on the board for the Driver Performance Monitor (DPM) output of the CS6152. The LED is turned on to indicate that the CS6152 has transmitted somewhere between 31 to 63 or more consecutive zeros. Note that DPM can not change state if the TCLK signal is removed.

EVALUATION HINTS

1. Be sure to properly terminate TTIP and TRING when evaluating the transmitted signal. For more information on pulse shape evaluation refer to the Crystal application note AN-7 entitled, "Measurement and Evaluation of Pulse Shapes in T1/PCM-30 Transmission Systems".

2. Note that the SW1 position labeled "on" (the closed position) grounds the corresponds pin of the same name on the CS6152 and places the function in the logic "0" or "off" state.

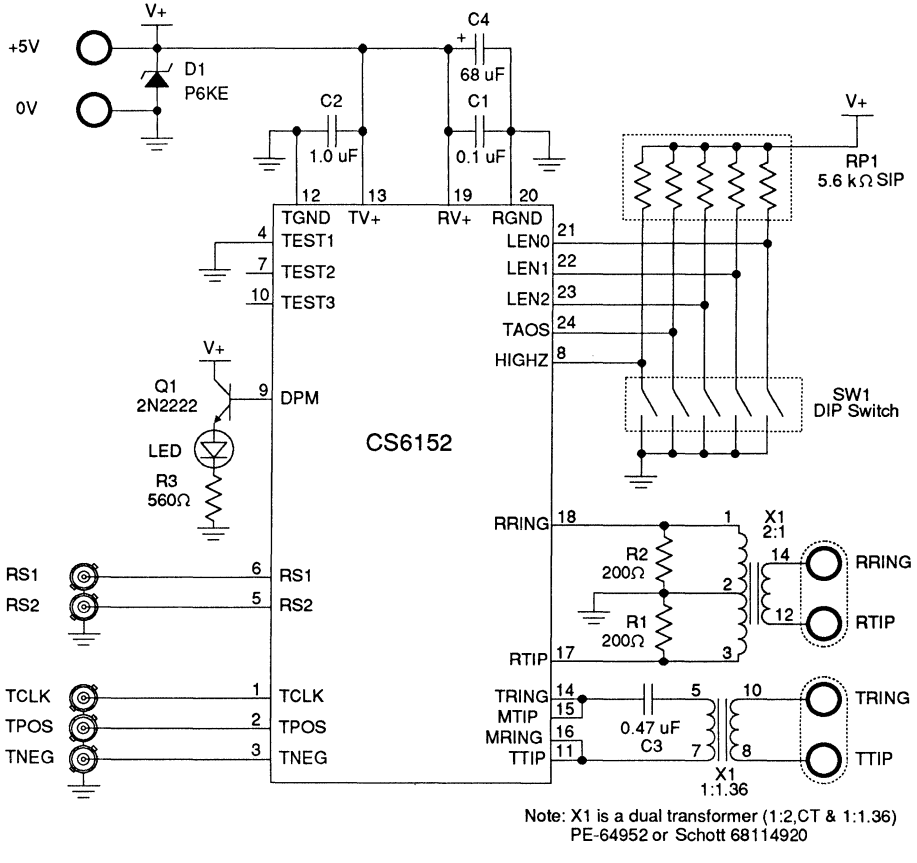


Figure 1. CDB6152 Schematic

•Notes•

PCM Line Interface Demonstration Board

Features

- Socketed Line Interface IC: Either the CS61534, CS61535, CS61574, or CS6158
- All Required Components for Complete Line Interface Functionality
- Slide Switch Selection of Control Inputs
- Reset Circuit
- Mode Selection Circuit (When Applicable)

General Description

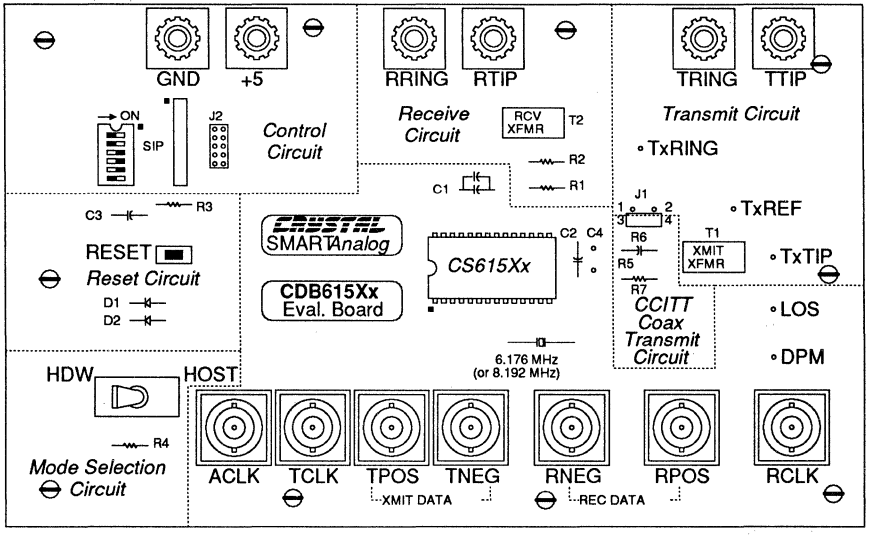
The board comes with a socketed line interface IC plus all the discretes required so that the device's performance can be verified in the lab without having to build a breadboard.

The board has four banana connectors for connecting two 100-to120 ohm twisted pair cables to the line transformers present on the board. Two other banana connectors allow for easy connection of an external five volt power supply. Power supply decoupling capacitors are resident on the board. BNC connectors allow easy access to the Received Clock and Data, the Transmit Clock and Data, and the Alternate Clock. Testing terminals provide access to the Serial Control Interface, DPM, MTIP, MRING, TTIP, TRING, LOS, and center tap of the transmit transformer.

Additional components provided on the board are a crystal, a reset circuit, and a DIP switch for controlling the input pins: LEN0, LEN1, LEN2, TAOS, RLOOP, and LLOOP.

ORDERING INFORMATION: CDB61534, CDB61535, CDB61574, CDB6158

BOARD LAYOUT



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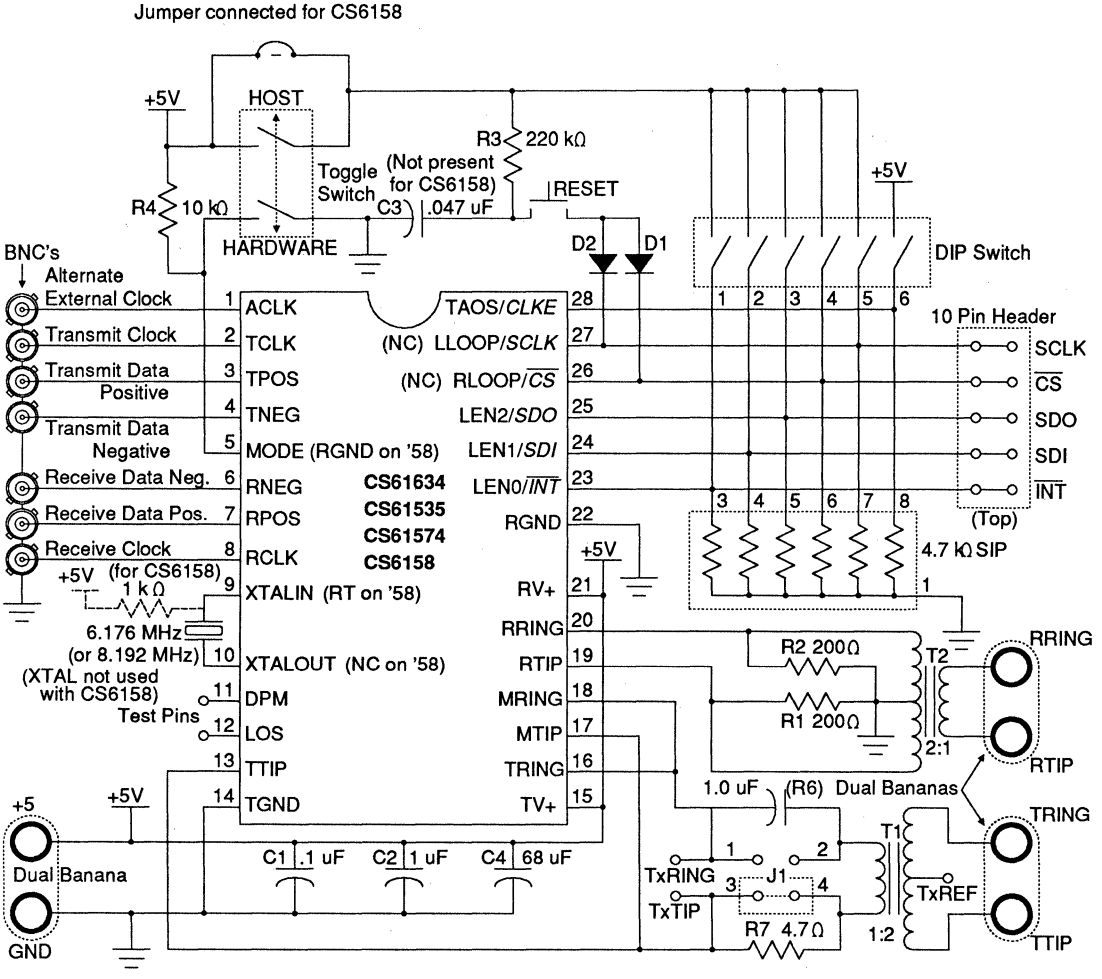
CIRCUIT DESCRIPTION

The PCM Line Interface Demonstration Board is an evaluation tool for Crystal's pin compatible line interface ICs: the CS61534, CS61535, CS61574, and CS6158. The board allows the device to be evaluated with no further breadboarding required. The '34, '35 and '74 boards come with two crystals: a 6.176 MHz crystal installed for T1 operation and a 8.192 MHz crystal which can be installed for PCM-30 operation. As an alternative on the CDB61534, a clock of exactly four times the TCLK frequency can be input to XTALIN, disabling the jitter attenuator.



Note: Pins 23 - 28 are single function on the CS6158, i. e. there is no serial interface.

Figure 1. Eval Board Schematic

Transmit Circuit

The transmit circuit consists of a 1:2 step-up transformer (T1), a blocking capacitor, and banana connectors (TTIP and TRING) for terminating a twisted pair. For operation with 100 or 110Ω twisted pair, connect pin 3 to pin 4 on pin header J1.

To support interfacing to a CCITT coax line (75Ω load, and 2.37V pulse height), a 4.7Ω resistor (R7) is provided to control pulse amplitude and correctly terminate the cable. To use this resistor, remove the jumper connecting 3 and 4 from pin header J1.

Test pins, TxTIP and TxRING, can be used to directly access pins 13 and 16 of the IC. TxREF allows access to the center tap (line side) of the transmit transformer.

Receive Circuit

The receive circuit consists of a center-tapped 1:2 transformer (T2) and banana connectors (RTIP and RRING) for connecting the receive twisted pair. Resistors R1 and R2 are each 200 Ω, providing a 100 Ω termination load for twisted pair applications. The resistors should be replaced by 150Ω resistors for 75Ω CCITT coax cable interface, and 240 Ω resistors for 120 Ω twisted shielded pair interface.

The CS6158 requires a 1.544 MHz (or 2.048 MHz) input signal on ACLKI (the ACLK BNC) for the receiver frequency reference.

Power Supply

The power supply circuit consists of two banana connectors (GND and +5) for connecting to ground and plus five volts. A 1.0 µF decoupling capacitor is supplied for the transmit power supply pins. 0.1µF and 68µF capacitors are supplied for the recieve power supply.

Mode Selection Circuit ('34, '35 & '74 boards only)

The Mode Selection circuit controls pin 5 of the CS61534, CS61535 and CS61574, and selects between host mode and hardware mode. The circuit consists of a toggle switch and a 10kΩ resistor (R4).

Switch	CS615Xx Pin Affected	Switch Position	
		On (right, toward center of board)	Off (left, toward edge of board)
1	LEN0 (23)	Logic High	Logic Low
2	LEN1 (24)		
3	LEN2 (25)		
4	RLOOP (26)	Loopback selected	Loopback not selected
5	LLOOP (27)		
6	TAOS (28)	Transmit all 1's to the line	Normal transmission

Table 1. Switch Position Interpretation

RESET Circuit

The RESET circuit consists of a switch, two diodes (D1, D2), a capacitor (C3) and a resistor (R3). When in the hardware mode and the switch is pushed, the RLOOP and LLOOP pins are momentarily pulled high. RESET is invoked in the host mode by writing a command over SDI.

Control Circuit -Hardware Mode Operation

The control circuit consists of a set of 6 DIP slide switches which control pins 23 through 28 as shown in Table 1. Turning a switch on provides a 5 Volt signal to the corresponding pin.

Control Circuit -Host Mode Operation

The serial bus pins of the CS61534, CS61535 and CS61574 are accessed by connecting to the 10 pin header. Each pin on one side of the header is connected to the adjacent pin on the other side. The DIP slide switch is still used to control CLKE (pin 28). Placing the CLKE slide in the on position, gives RCLK and SCLK polarity compatible with the CS2180A. When CLKE is in the off position, RCLK has the same polarity as in the hardware mode (R8070 compatibility). All of the other DIP switches are disabled in the host mode.

WATCH OUT! Do not switch the board to the hardware mode when it is connected to your serial interface. If any of the dip switches are on, the power supply will be connected to your serial interface, potentially damaging its output circuits.

EVALUATION HINTS

1. Be sure to properly terminate TTIP and TRING when evaluating the transmitted signal.

2. When externally implementing a loopback by connecting RPOS/RNEG to TPOS/TNEG and RCLK to TCLK, be sure to insert an inverter between RCLK and TCLK (i.e., when in the hardware mode, or when in the host mode and CLKE is low).

PCM Line Interface Evaluation Board

Features

- Socketed Line Interface IC: Either the CS61534, CS61535, CS61535A, CS61574, CS61574A, CS61575, CS6158, or CS6158A
- All Required Components for Complete Line Interface Evaluation
- DIP Switch or Serial Interface Configuration of Line Interface
- LED Status Indicators
- Mode Selection Circuit Supporting Host, Hardware, and Extended Hardware Modes

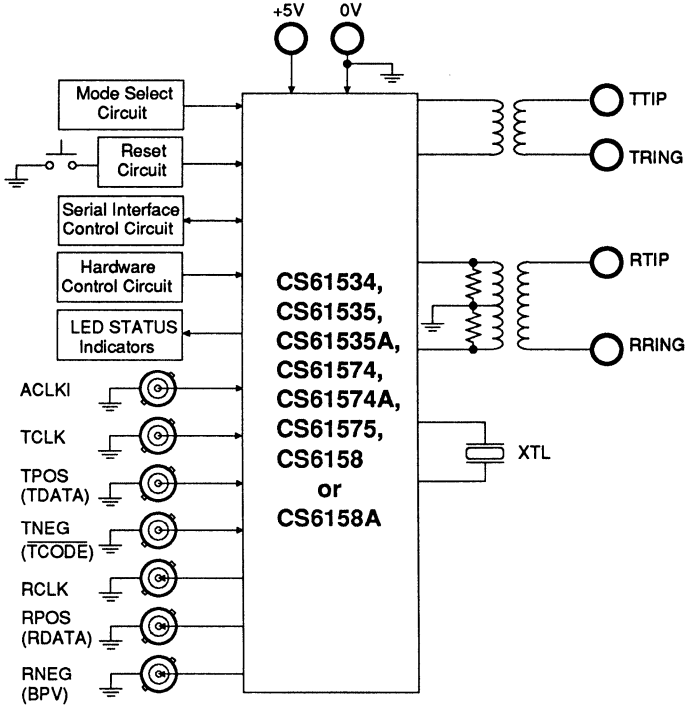
General Description

The evaluation board includes a socketed line interface IC and all support components required for evaluation. The board is powered by an external 5 Volt supply.

The board has four banana connectors for connecting two 100-120 Ω twisted pair cables to the line transformers on the board. The board may also be connected to 75 Ω coax lines. BNC connectors provide easy access to the Received Clock and Data, the Transmit Clock and Data, and the Alternate Clock. LED indicators are provided to monitor all IC status outputs. The line interface may be configured using DIP switches in the Hardware and Extended Hardware modes, or it may be configured using the serial interface in Host mode.

ORDERING INFORMATION: CDB61534, CDB61535
CDB61574, CDB61575, CDB6158,
CDB61535A, CDB61574A, CDB6158A

Block Diagram



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•Notes•

Semiconductor Corporation

CDB61544

PCM Line Interface Demonstration Board

Features

- Socketed CS61544
- Complete Line Interface Function
- Slide Switch Control of Digital Inputs
- Reset Circuit

General Description

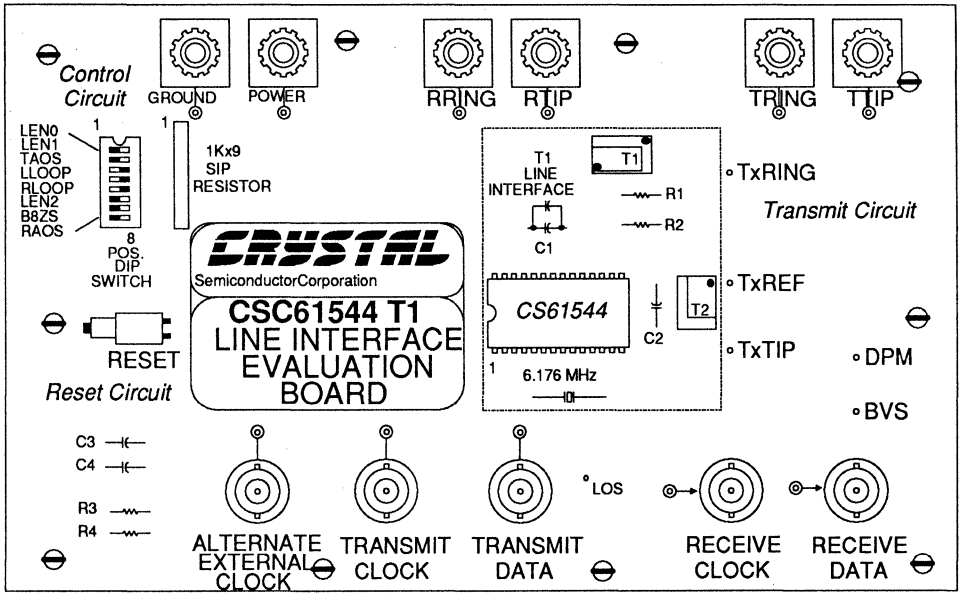
The board comes with a socketed CS61544 IC plus all the discretes so that the CS61544's performance can be verified in the lab without having to first build a breadboard.

The board has four banana connectors for connecting two 100 ohm twisted pair cables to the line transformers present on the board. Two other banana connectors allow for easy connection of an external five volt power supply. Power supply decoupling capacitors are resident on the board. BNC connectors allow easy access to the Received Clock and Data, the Transmit Clock and Data, and the Alternate Clock. Testing terminals provide access to the Serial Control Interface, DPM, MTIP, MRING, TTIP, TRING, LOS, and center tap of the transmit transformer.

Additional components provided on the board are a crystal, a reset circuit, and a DIP switch for controlling the input pins: LEN0, LEN1, LEN2, TAOS, RLOOP, LLOOP, B8ZS, and RAOS.

ORDERING INFORMATION: CBD61544

BOARD LAYOUT



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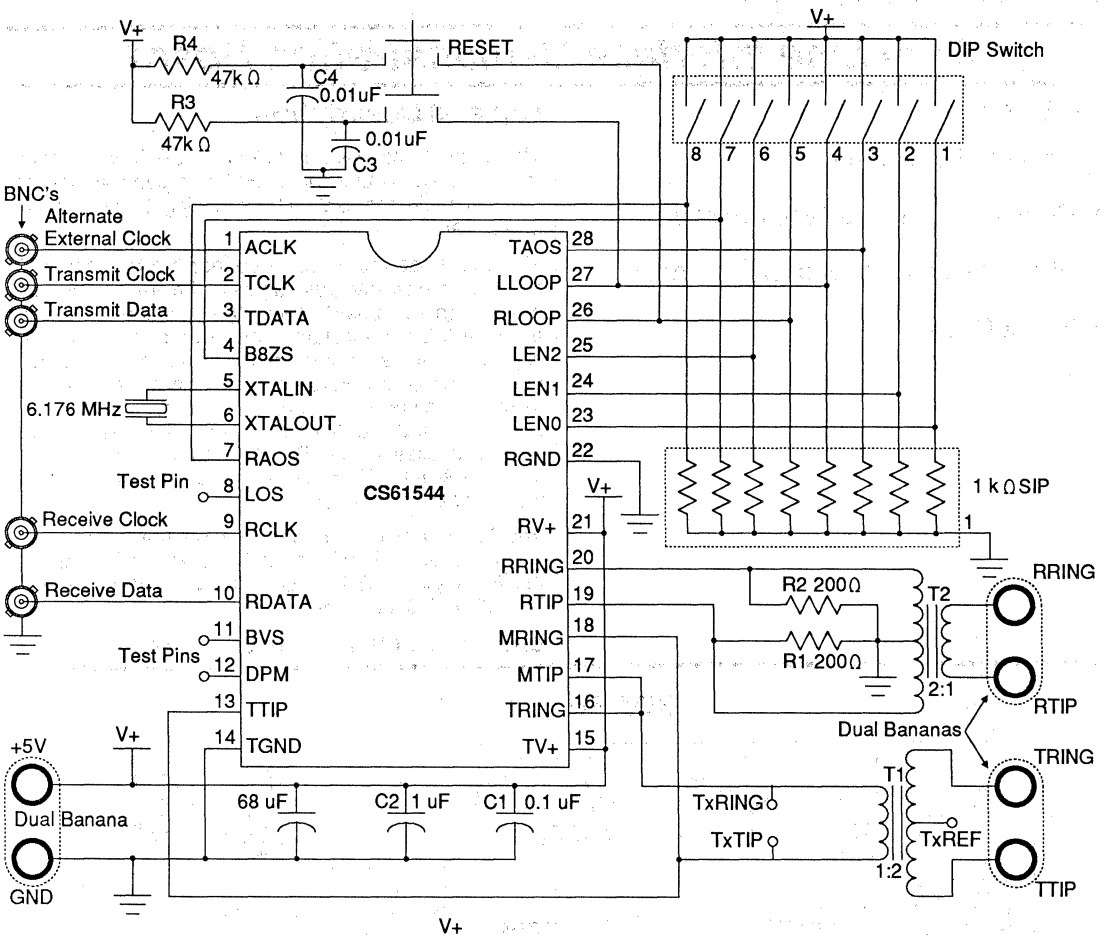
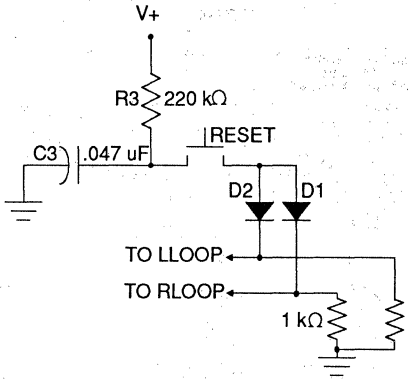




NEW AND IMPROVED RESET CIRCUIT

(NOT PROVIDED, BUT RECOMMENDED FOR SIMILAR DESIGNS)

Semiconductor Corporation

CDB6159

Evaluation Board for CS6159

Features

- Socketed CS61529 Line Interface IC
- All Required Components for Complete Line Interface Evaluation
- DIP Switch Configuration of all CS6159 Control Inputs
- LED Status Indicator for CS6159 Receiver Loss of Signal Output

General Description

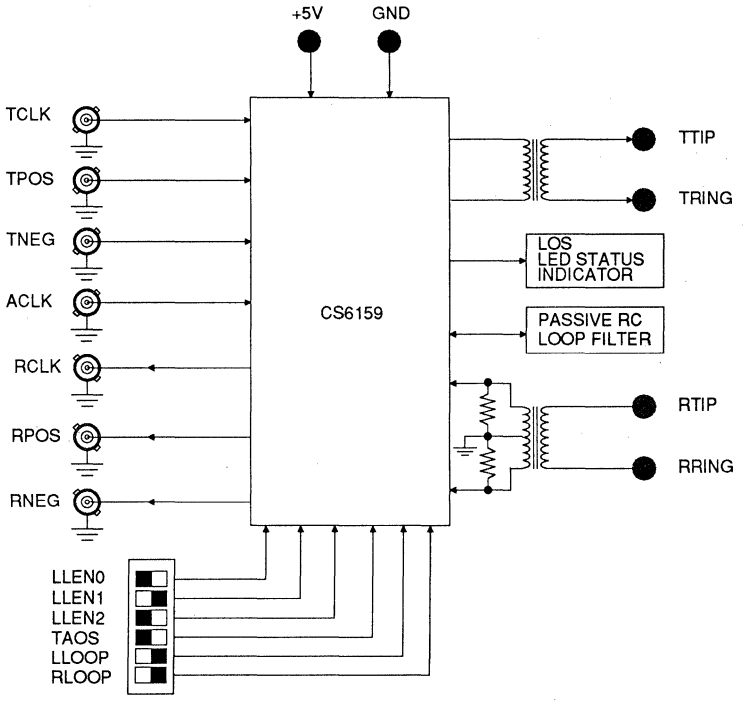
The evaluation board includes a CS6159 line interface IC and all support components required for evaluation. The board is powered by an external 5 Volt supply.

The board features four binding post connectors for connecting two 100Ω twisted pair lines to the transformers on the board. The board may also be connected to 75Ω coax or 120Ω twisted pair lines after replacing the receiver termination resistors and setting a jumper. BNC connectors allow easy access to the digital transmit clock and data inputs and the digital receiver clock and data outputs.

An LED status indicator is provided for monitoring the CS6159's Loss Of Signal (LOS) output. A DIP switch is provided for configuring the CS6159's control input pins: LEN0, LEN1, LEN2, TAOS, LLOOP, and RLOOP.

ORDERING INFORMATION: CDB6159

Block Diagram



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CIRCUIT DESCRIPTION

Power Supply

As shown in the schematic in Figure 1, power is supplied to the evaluation board from an external +5 Volt supply connected to the two binding posts labeled +5V and GND. CR1 is a transient suppressor which protects the components on the board from over-voltage damage and reversed supply connections. The supply decoupling recommended in the CS6159 data sheet is provided on the board by C1, C3 and C4. C4 is the 1.0µF capacitor which decouples TV+ to TGND. Similarly, the parallel combination of C3 (a 0.1µF ceramic capacitor) and C1 (a 68µF electrolytic capacitor) is used to decouple RV+ to RGND. The CS6159 TV+ and RV+ supply traces are tied together at the IC.

Transmit Circuit

The CS6159's digital transmitter inputs are brought in through the BNC connectors labeled TCLK, TPOS and TNEG for the transmit clock and NRZ data respectively. The transmitter output is coupled onto a 100Ω or 120Ω twisted pair line at the TTIP and TRING binding posts using a 1:1.36 step-up transformer (T1). The transmitter output may also be connected to a CCITT 75Ω coax line after the removal of the jumper J1 which places a 10Ω resistor, R3, in series with the transmit transformer. This resistor is used to generate the required CCITT 2.37 V peak pulse amplitude and provide the appropriate equivalent load impedance to TTIP and TRING. C5 is the 0.47µF blocking capacitor recommended in the CS6159 data sheet.

Receive Circuit

The CS6159's receiver inputs are transformer coupled to the line connected to the RTIP and RRING binding posts on the board. A center-tapped, center-grounded 1:2 transformer, T1, is used to provide equal amplitude pulses of opposite polarity to the RTIP and RRING pins of the CS6159. The receive line is terminated by the resistors R5 and R6. As supplied from the factory, R5 and R6 are 200Ω resistors for terminating a 100Ω T1 twisted pair line. R5 and R6 should be replaced with 240Ω resistors for terminating a 120Ω CCITT twisted pair line. For a 75Ω CCITT coax line R5 and R6 should each be 150Ω.

The CS6159's digital receiver clock and data outputs are brought out to the BNC connectors labeled RCLK, RPOS and RNEG respectively. An external reference clock may be supplied via the ACLK connector for substitution on RCLK during loss of signal. An LED status indicator is provided for monitoring the CS6159 Loss Of Signal (LOS) output. The LED is illuminated when LOS is asserted indicating the receipt of 175 consecutive zeros. R1 and C2 are the external PLL loop filter components recommended in the Applications section of the CS6159 data sheet. R2 is the external resistor used to set the PLL's ICO center frequency.

Control Circuit

The CS6159 digital control inputs are configured using the DIP switch S2. Placing a switch in the "on" position grounds the corresponding pin of the same name, placing it in the logic "0" or "off" state. LLEN0, LLEN1 and LLEN2 select the transmitter line length setting, the clock recovery circuit's ICO center frequency and the receiver data slicing level as described in the CS6159 data sheet. RLOOP selects the CS6159's remote loopback mode, and LLOOP selects the local loopback mode. Simultaneously asserting RLOOP and LOOP places the device in the reset state. TAOS selects the transmission of all ones at the TCLK frequency.

EVALUATION HINTS

1. Be sure to properly terminate TTIP and TRING when evaluating the transmitted signal. For more information on pulse shape evaluation refer to the Crystal application note AN-7 entitled, "Measurement and Evaluation of Pulse Shapes in T1/PCM-30 Transmission Systems".

2. Note that the S2 position labeled "on" (the closed position) grounds the corresponding pin of the same name on the CS6159 and places it in the logic "0" or "off" state.

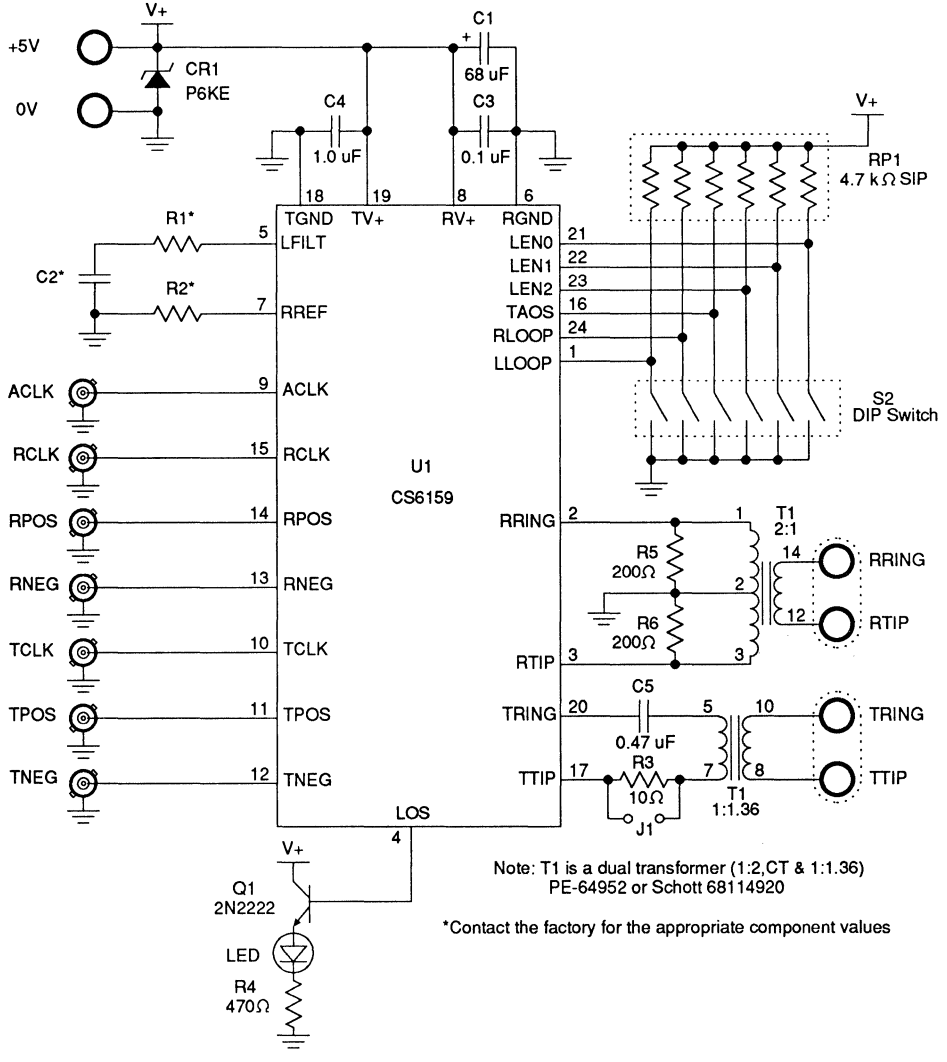


Figure 1. CDB6159 Schematic

•Notes•

Semiconductor Corporation

CDB8123
CDB8124

OPTIMODEM Evaluation Kit

Features

- Kit includes two boards and an optical cable
- Industry standard RS232 DB25 pin serial connector
- Industry standard ST fiber connector
- LED RS232 status indicator
- On board -5V generator for RS232 interface
- Adjustable LED drive current

General Description

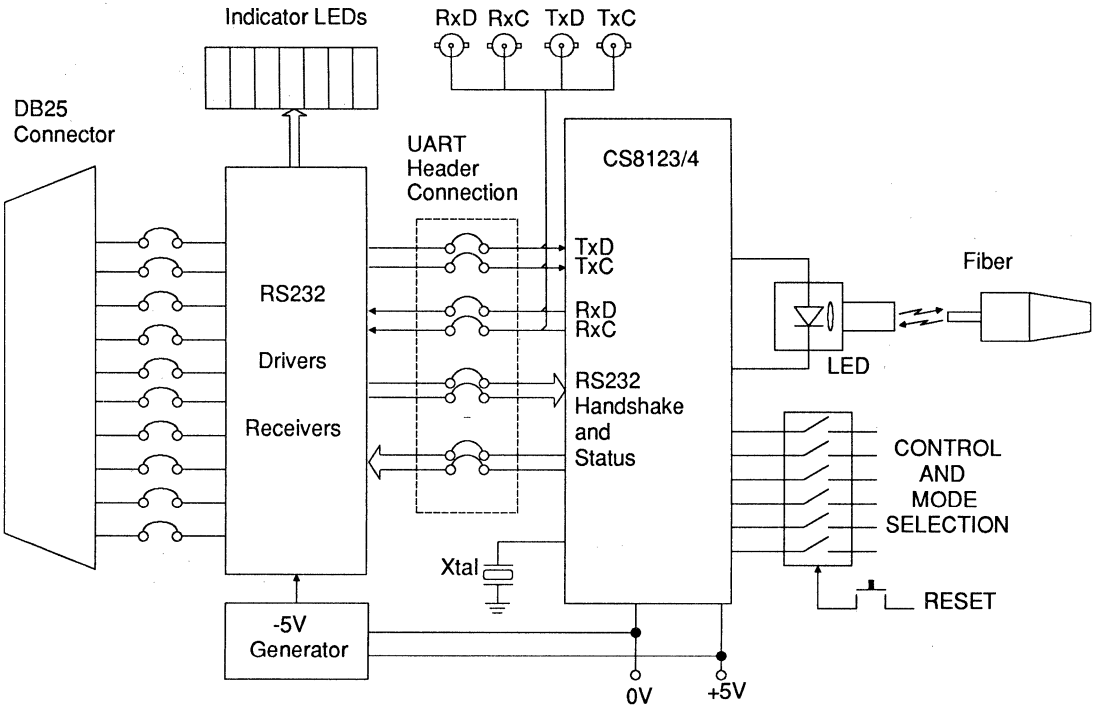
The CDB8123 and CDB8124 Evaluation Kits allows fast evaluation of the CS8123 or CS8124 OPTIMODEM.

Digital serial I/O is via a standard RS232 DB25 pin female connector. Jumpers to allow various different serial I/O modes are provided. In addition, LEDs are provided to show the status of the RS232 control signals and data paths.

BNC connectors are provided to allow easy access to OPTIMODEM clock and data lines, primarily for high speed synchronous evaluation.

The fiber optic cable connector is a standard ST style male version. The board requires a +5V supply. The negative supply for the RS232 drivers is supplied by an on-board inverter circuit.

ORDERING INFORMATION:
CDB8123
CDB8124



10

INTRODUCTION

The CDB8123 and CDB8124 evaluation kits are designed to aid in evaluation of Crystal's CS8123 and CS8124 ICs. In the CDB8124, a CS8124 is provided along with a LED and crystal, as well as ancillary circuits for controlling the CS8124 and interfacing it with a variety of off-board hardware. The CDB8123 contains a CS8123.

The CDB8123 and CDB8124 boards have the same layout and components. The CS8123 does not support synchronous operation (i.e., does not use the TxC and RxC clocks). Therefore when using a CDB8123, the clock control switch, SW2, should be set to its "EXT TxC" position, and the DR1/2/3 DIP switches should be set to the off (zero) position.

CIRCUIT BOARD DESCRIPTION

RS-232 Interface

The board is designed to allow easy interface to RS-232 systems. The 25 position "D" connector, P1, is configured as specified in EIA RS-232 documentation. The 20 pin stake header, J2, is provided so that the signals to and from J1 can be easily reconfigured. For example, to operate two OPTIMODEMS in the End-to-End (transparent) mode between a DTE and DCE, the signals; DTR and DSR, CTS and RTS, and RxD and TxD should be interchanged at J2. For operation in the Modem Control (handshake) mode, signals should be connected straight through using the jumpers provided with the boards.

Though the CS8124 is capable of data rates to 256kbps in the synchronous mode, the RS-232 line drivers are slew rate limited and only capable of operation to about 100kHz. For operation at speeds above 100kHz, interface to the board at connector J1, or via the TxC, TxD, RxC, RxD BNC connectors. Never drive a clock signal into TxC with the OPTIMODEM TxC pin set to output. Always set SW2 to "EXT TxC" when driving TxC externally.

Status LEDs

A set of LEDs has been provided to indicate the status of the control and data signals. The DCD LED on shows that synchronization between the two OPTIMODEMS has been achieved.

OPTIMODEM Pin Access

Stake header J1 allows direct access to the pins of the OPTIMODEM, and can be used to interface the device to external communications circuits such as a USART.

For the CS8124, switch SW2 controls the status of the CKC (clock control) pin, and the TxC signal path. When SW2 is in the "EXT TxC" position, an external TxC must be input to the OPTIMODEM, and the TxC(I) signal path is connected to the OPTIMODEM TxC pin. When SW2 is in the "8123/4 TxC" position, the OPTIMODEM outputs TxC, and the TxC(O) signal path is connected to the OPTIMODEM TxC pin.

Configuration

The SW1 DIP switches control the modes and the data rates of the OPTIMODEM. When a switch is open (off), the corresponding pin is connected to ground. See Tables 2 and 3 of the CS8123/4 data sheet for information on configuring the CS8123/4.

Clocking Options

A 9.216 MHz crystal has been provided with the board, with J3 left open. Optionally, the XTL pin can be driven by an external clock via J3 and the EXTCLK BNC connector. This clock must operate at logic levels of 0.9VD+ high and 0.2VD+ low; and must have a nominal 50% duty cycle.

If a crystal is used, we recommend leaving jumper J3 open to minimize capacitive loading. If the same external clock is used for both boards, one board must be in forced slave mode before synchronization can occur.

Transmit Current Level Adjustment

Potentiometer, R7 can be used to control the amount of power the OPTIMODEM delivers to the LED. Turning the control screw clockwise will increase the resistance from the TCL pin to ground which increases the LED drive current. Note, the OPTIMODEM must be removed in order to measure the potentiometer resistance.

Miscellaneous

We recommend copying the power and ground plane arrangements on the evaluation board for all boards designed to use the CS8123 or CS8124. A small amount of patch area has been provided to allow the addition of other circuitry to the board.

Getting Started

The first step is to link two evaluation boards together using the fiber optic cable provided. Connect each board to a +5V DC power supply and select either transparent or modem control mode. Select the same baud rate for each board and ensure that the diagnostic control pins are set appropriately.

Ping-pong synchronization should occur, which is indicated by $\overline{DCD}$ going low, illuminating the $\overline{DCD}$ LED on both boards. If continuous transmit is selected on one board and continuous receive on the other board, only the board set for continuous receive should indicate digital carrier detect, $\overline{DCD}$.

On the CS8124, if you are having difficulty establishing ping-pong synchronization, verify that the oscillator has started by selecting the "8123/4 TxC" option and observing the TxC(O) output which should be at the data rate selected on DR1/2/3 or one sixth the crystal frequency if in continuous transmit mode. Do not attach a probe to the XTL pin as additional load may kill oscillation.

If the oscillators on both parts are running, try using continuous transmit and receive in both directions to see if a single direction link can be established. Operation of the linear channel is more robust in continuous receive mode because the device does not switch between transmit and receive operation.

The best way to see what is going on is by using the Tektronix 2815 OPTO-Scope. The OPTO-Scope is an oscilloscope with an optical input which has a provision for connecting fiber cable directly into a 'scope input, and displaying a corresponding waveform on the screen just as one would observe a signal on a wire conductor. By using optical couplers, it is possible to observe synchronization and ping-pong operation of the OPTIMODEM.

An alternative to the OPTO-Scope is to use a conventional 'scope, and observe the LDN and LDP pins. Signals on these pins should be observed differentially; that is, use two channels on the oscilloscope, invert the second channel and add it to the first. The receiver probably will not work when a 'scope is connected across the LED.

If connecting two computers together, use the boards as DCEs. Select the modem control mode; RS2 is high. The "straight through" jumper option at J2 is all that is required. In the modem control mode, the OPTIMODEMS effectively swap TxD and RxD, CTS and RTS, and DTR and DSR. (When connecting computers together with a cable, these signals must be swapped in the cable. The OPTIMODEM will perform this function, so the cables should be wired pin to pin.)

To connect a terminal to a computer, use the boards to emulate a cable. Select the end-to-end mode; RS2 is low. The signals, RxD and TxD, CTS and RTS, and DTR and DSR, must be swapped at J2. (For example, In the end-to-end mode, the signal, DTR, asserted by the computer, will come out of the OPTIMODEM at the terminal end as DSR, hence the need for the swap at J2.)

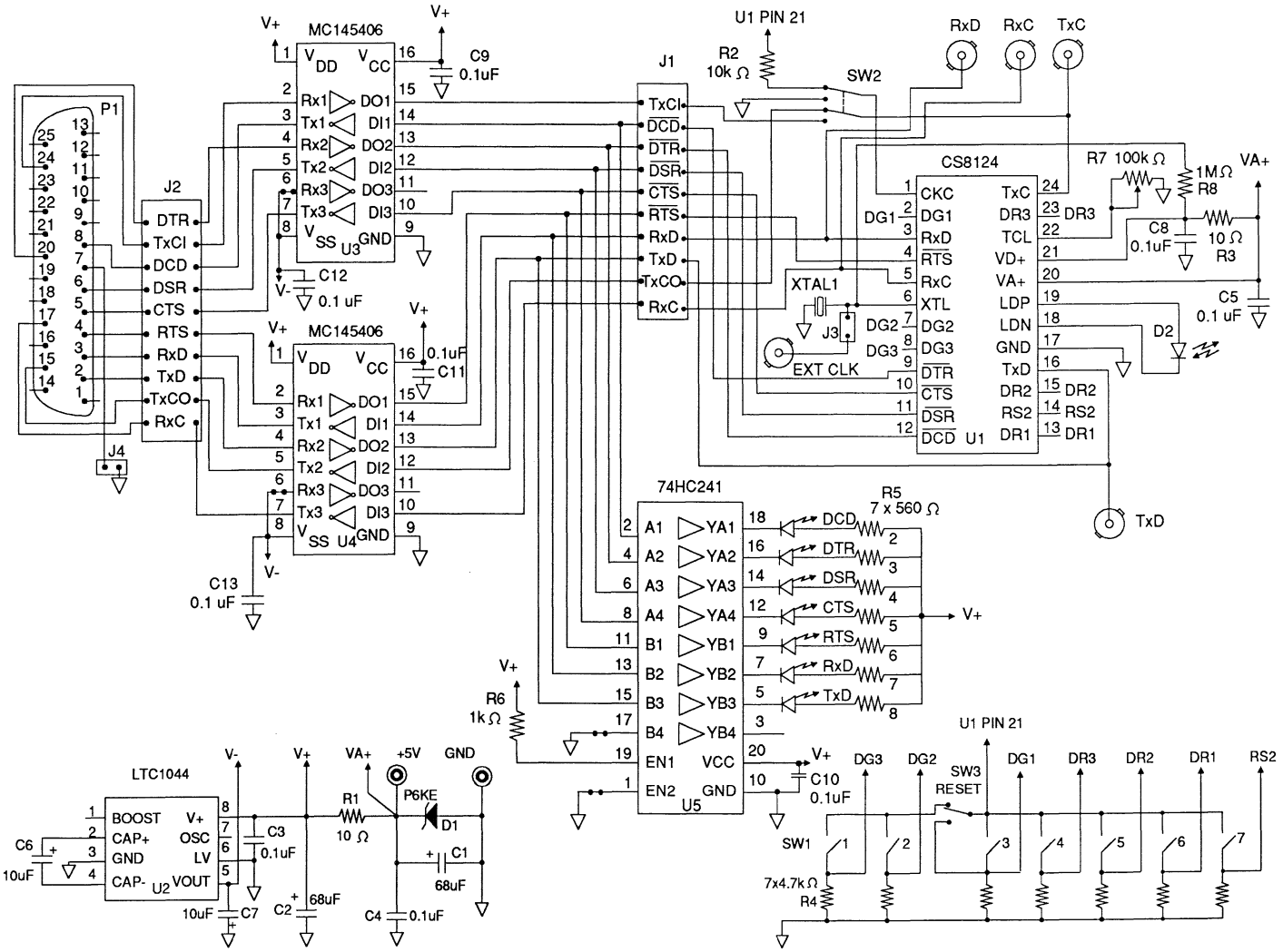


Figure 1. CDB8123/CDB8124 Schematic

•Notes•

Semiconductor Corporation

CDB8125/6

T1 Optical Interface Evaluation Kit

Features

- Kit includes board and an optical cable
- Converts between optically-encoded T1 signal and industry standard DS-1 electrical signal
- Industry standard ST fiber connectors
- Purchase of one kit allows uni-directional testing (1 fiber looped between CS8125 and CS8126 on same board)
- Purchase of two kits allows evaluation of bi-directional links (using 2 fibers)

General Description

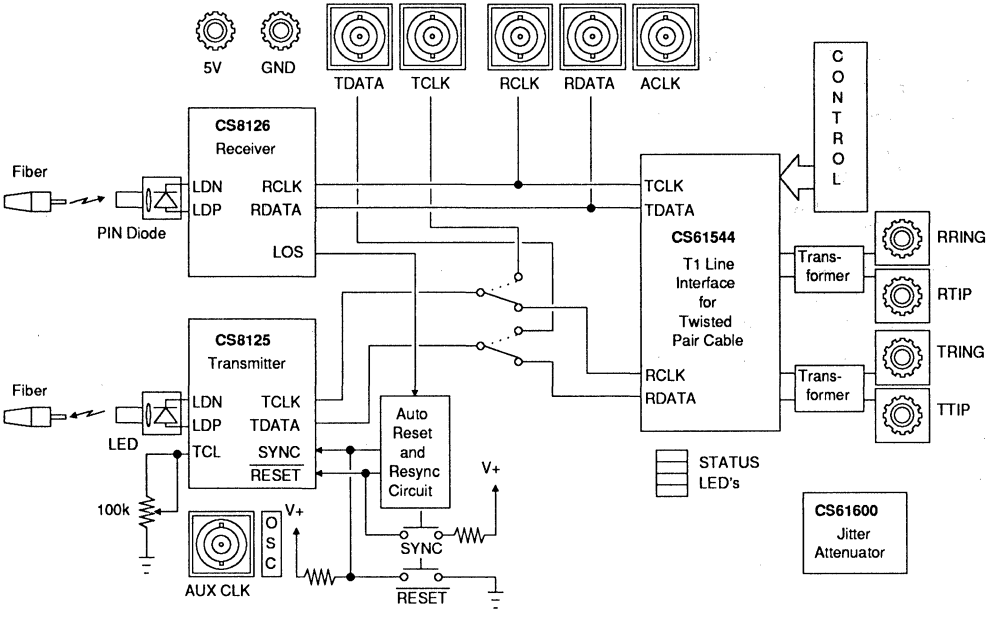
The CDB8125/6 Evaluation Kit allows fast evaluation of the CS8125 and CS8126 T1 Optical Interface ICs.

The kit includes a CS8125, CS8126, LED transmitter, PIN diode detector, a fiber cable, a CS61544 T1 line interface unit and an optional CS61600 jitter attenuator. With the use of the CS61544, the CDB8125/6 constitutes a complete T1 wire to fiber interface. Alternatively, clock and data can be input to the CS8125 and extracted from the CS8126 via BNC connectors. The CS61600 can be added to the circuit to absorb the dropped clock jitter from the CS8126 RCLK output.

Control switches on the CDB8125/6 allow selection of loopbacks and all-ones transmission for the CS61544. LEDs give the status of the loss-of-signal output pins on the twisted-pair receiver (CS61544) and optical receiver (CS8126). An auto reset and resync circuit may also be activated.

The fiber optic cable connectors are a standard ST style male version. The board requires a +5V supply.

ORDERING INFORMATION:
CDB8125/6



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The CDB8125/6

The CDB8125/6 is designed to provide the user with versatility in evaluating the performance and functionality of the CS8125 and CS8126. This board can be configured to hook up directly to most T1/PCM-30 test equipment through the CS61544 interface. Signals input to the CS61544 receiver are recovered and output to the CS8125 for transmission onto the fiber cable. When one board is used, the fiber should be looped from the LED output to the PIN diode input where the CS8126 recovers the clock and data. The recovered clock and data are passed to the CS61544 transmit section where the dropped clock jitter is removed and the data is retransmitted over wire to the test equipment.

Alternatively, clock and data can be input to the CS8125 and the recovered clock and data output of the CS8126 can be observed via the BNC connectors along the board's upper edge. A CS61600 jitter attenuator may be wired into the circuit to remove the dropped clock in the CS8126 RCLK signal.

An auto resync circuit has been implemented which will cause the CS8125 to either momentarily reset, momentarily transmit the sync pattern or both in response to the CS8126 losing sync (CS8126 LOS goes high). Alternatively, these functions can be controlled manually by pushbuttons SW1 and SW3. Initially, we recommend that these functions be controlled manually until the user gains some familiarity with the board. See the CDB8125/6 schematic and layout section for information on how this circuit works.

A potentiometer is used to control the output power of the CS8125. This pot is set at 10 kΩ when the board is assembled and tested at Crystal. This setting provides plenty of output power for driving short fiber lengths. For long cables, it may be necessary to increase the power output by turning the screw clockwise (increasing resistance).

Using The CDB8125/6

Apply +5 V power to the power supply inputs and reset the CS61544, the CS8125 and the CS8126 (depress and release SW2, SW3, "RESET" and SW4 "44 RESET"). Before applying signals, make sure there is no contention of the TCLK signals (i.e. do not simultaneously output TCLK from the CS8125 while inputting it from the 8125 "TCLK" BNC or the RCLK output of the CS61544). Just in case there is TCLK contention, resistor R21 should limit the current.

If there is trouble in looping PCM test equipment through the board and fiber, try using the RLOOP function of the CS61544. RLOOP internally loops recovered clock and data to the transmitter where it is retransmitted over the wire. RCLK and RDATA are still output and can be observed at the CS8125 TCLK and TDATA inputs. The recovered signal from the CS8126 can be observed at both the "8126 RCLK and RDATA" BNC's and CS61544 TCLK and TDATA input pins.

PCM-30 Applications

While the CDB8125/6 is described as capable of operating at either 1.5444 MHz or 2.048 MHz, the CS61544 used on the board is offered by Crystal as a T1 only part. Using the appropriate 8.192 MHz crystal allows the CS61544 to operate at the PCM-30 rate. The CS61544 does not output pulses compliant with CCITT standards, however the pulses selected by LEN2/1/0 = 000 or 011 should suffice for any test or evaluation of board performance (except pulse shape). For PCM-30 applications, Crystal recommends use of one of our PCM-30 compatible line interface chips with transmit side jitter attenuation such as the CS61534, CS61535 or CS61535A.

Movable Jumper Positioning

Jumper J1 selects internally generated or external TCLK. If jumper is left open, TCLK must be supplied from an external source – either the "8125 TCLK" BNC or the RCLK output of the 61544. Installing the J1 jumper causes the CS8125 to output TCLK. Make sure there is no TCLK contention.

Jumper J3 selects the clock source for ACLK for the CS61544. The upper position (towards top of board) selects the "44 ACLK" BNC as the ACLK source. The lower position ties ACLK to TCLK. Note: ACLK is used by the '44 only for TAOS & RAOS.

Jumper J4 selects manual or auto reset for the CS8125. When the jumper is installed in the upper position, manual reset is selected: depressing SW3 resets the CS8125. When the jumper is in the lower position, the CS8125 is momentarily reset when the CS8126 goes into a Loss of Sync, LOS, state.

Jumper J5 selects manual or auto sync pattern transmission. When the jumper is in the upper position, auto sync is enabled. SYNC, pin 3, is held high until the CS8126 leaves the LOS state. When the jumper is in the lower position, selection of SYNC is manual and is controlled by SW1.

Clock/Data Sources

The clock and data signals for the CS8125 can be supplied by the CS61544 or the BNC connectors, as selected by the "TDATA & TCLK" switch in the board's center. With the switch in the "BNC" position, TCLK and TDATA are input to the CS8125 from the "8125 TDATA and TCLK" BNC's and are disconnected from the CS61544

Switching to the "44" position connects the RCLK and RDATA outputs of the CS61544 to the TDATA & TCLK inputs of the CS8125 (jumper J1 should be removed, selecting external TCLK). The CS8126 RCLK and RDATA outputs are always routed to both the "CS8126 RCLK, RDATA" BNC's and the TCLK and TDATA inputs of the CS61544.

Oscillators and Clocks

As delivered, the CDB8125/6 comes with a 12.352 Hz crystal connected to the CS8125 oscillator. The XTL pin of the CS8125 is pulled up to the supply with a 1 MΩ resistor. The OSCOUT pin of the CS8125 is connected to the XTL pin of the CS8126 to provide the CS8126 clock.

If two crystals are used, one each for the CS8125 and CS8126, 1 MΩ pull-up resistors should be used at both R19 and R20. The wire jumper connecting OSCOUT of the CS8125 to XTL of the CS8126 should be removed.

To run the system at 2.048 MHz, an external clock source must be supplied. Either input a 16.384 MHz clock into the "AUX/CLK" BNC or use a crystal oscillator in the "OSC 1" socket (just below the CS8125). The wire jumper on the board's top near the XTAL pin of the CS8126, which connects the OSCOUT pin of the CS8125 to the XTL pin of the CS8126, must be cut or removed. The XTL pin of both the CS8125 and CS8126 should be driven directly from the 16.384 MHz clock source. A wire jumper must be installed to connect the trace from the clock source to the XTL pins. This clock source must swing nearly rail to rail. (Refer to the Digital Characteristics - Input Voltage Levels for the XTL pin.) The 1 MΩ pull-up resistors, R19 and R20, should be removed from the circuit. Note that if a clock oscillator module is used, its output is also present at the "AUX CLK" BNC.

For operation at PCM-30 data rates, the CS61544 and CS61600 will require an 8.192 MHz crystal such as the CXT8192. For both T1 and PCM-30

applications, the CS61544 and CS61600 will operate correctly only if the signal frequency is within ±130ppm (±50 ppm for PCM-30) at the nominal T1 frequency. Crystals supplied by Crystal Semiconductor are recommended for both data rates.

Stand Alone CS8126 Jitter Attenuation

A CS61600 jitter attenuator circuit has been placed in the lower right side of the board. This circuit can be used to remove the CS8126 RCLK jitter which results from the 3B4B decoding (every fourth clock is dropped). This circuit is not connected to anything except power and ground, and has not been tested on the board to ensure functionality. The CS8126 RCLK and RDATA can be picked up at several places on the board and wired over to the CLKIN and DIN pins of the CS61600; likewise for CLKOUT and DOUT. The crystal used by the CS61544 has been socketed and can be removed and inserted in the CS61600 crystal sockets. Note that neither the CS61544 nor the CS61600 will function without a crystal.

CDB8125/6 Schematic

Reset and Sync

The schematic for the CDB8125/6 is shown in Figure 1. Care was taken to lay out the schematic similarly to the board itself to make finding ones way around the board simpler. The auto RESET and SYNC circuit works in the following manner: A Loss of Sync, LOS, causes the LOS pin of the CS8126 to go high. When this condition occurs, the $\overline{\text{RESET}}$ pin will immediately be pulled low for about 5 ms. The SYNC signal will go high when LOS goes high, and stay high until about 30 ms after LOS is deasserted by the near-end CS8126. Diode, D9, prevents a -5V excursion from occurring at the inverter input when LOS goes to ground.

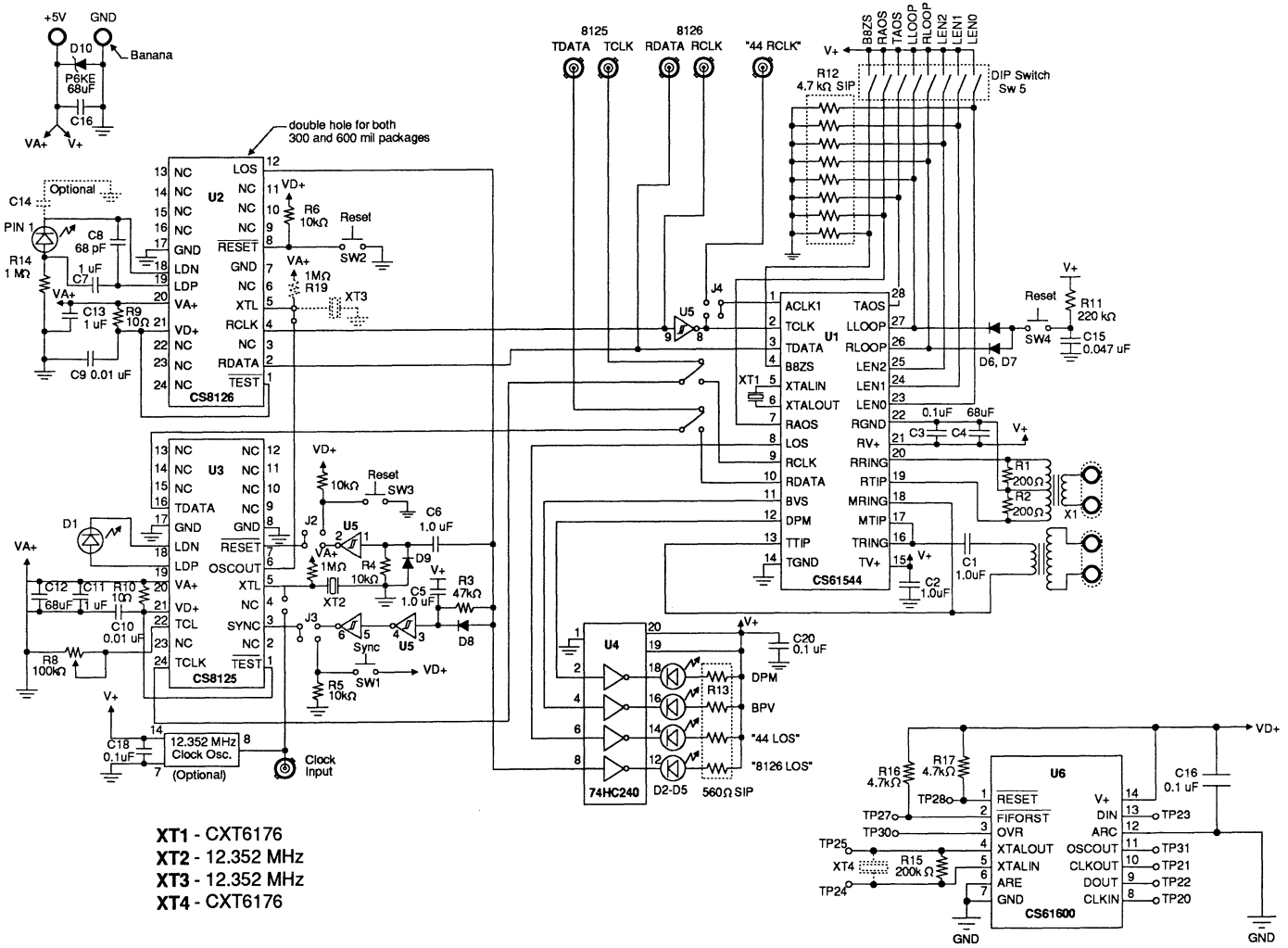
If only one CDB8125/6 is used, looped back on itself, use only the auto sync circuit, with manual reset (jumpers J2 and J3 in the upper positions). If two CS8125/6 systems are linked, both auto reset and auto sync will be useful. If this circuit is active and one of the CS8126's loses sync, it will force a reset on its partner CS8125 which interrupts its transmission thereby forcing the CS8126 at the far end to loose sync. The result is that both ends will reset and transmit the sync pattern.

We don't expect any significant problems with the CS8125 or CS8126 regarding their ability to acquire and maintain synchronization, however use of the CS8125's SYNC function will ensure minimum synchronization time. The RC time constants have been selected to allow more than ample time for the reset and sync.

Layout

There are a few important features to note regarding board layout. The power supply is heavily filtered and routed such that the CS8125, the CS8126 and the rest of the board are supplied from different supply traces. The different supply traces should help in keeping noise coupled into the supply as isolated as possible from the different circuits, particularly the CS8126 which must recover signals at very low levels.

Also note the judicious use of ground plane. Additional ground plane has been used on the bottom of the board around the LED (to reduce transmitted noise) and the PIN diode (to keep the inputs, LDN and LDP, as quiet as possible). Effort was also made to minimize the trace lengths from the LDN and LDP pins to the LED and PIN diode.



XT1 - CXT6176
XT2 - 12.352 MHz
XT3 - 12.352 MHz
XT4 - CXT6176

Figure 1. CDB 8125/6 Schematic

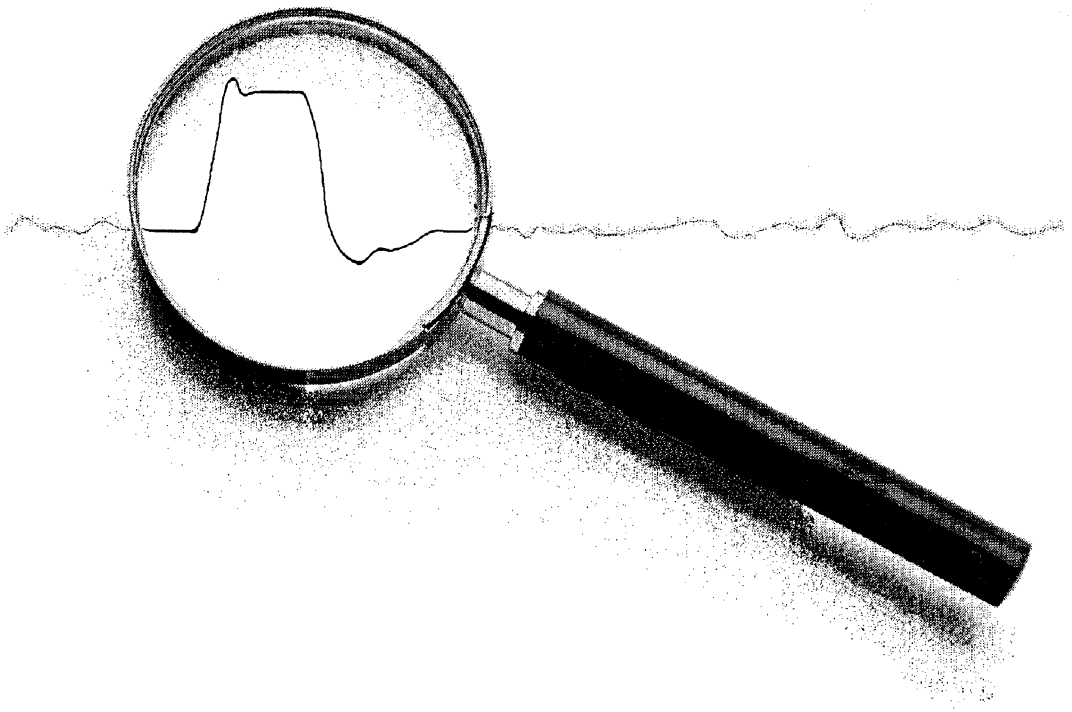
•Notes•

CONTENTS

Application Note

Measurement and Evaluation of Pulse Shapes in T1/PCM-30 Transmission Systems

By Roger Taylor



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Introduction

The T1 (1.544 Mbps) transmission system is widely used in North American public and private telephone networks. An analogous system, PCM-30 (2.048 Mbps), is used outside North America. Both of these primary rate transmission systems must meet exacting pulse shapes as described in AT&T CB-119 and CCITT G.703. (There are other North American T1 specs which differ slightly from CB-119.) Crystal Semiconductor T1 and PCM-30 line interface devices have pulse shaping line drivers whose output pulses are designed to meet the pulse-shape requirements of the specifications stated above. Measuring these pulses to ensure they comply with the specifications is not as straightforward as it may seem. This paper covers pulse shape measurement techniques to allow accurate assessment of T1 and PCM-30 pulse shapes.

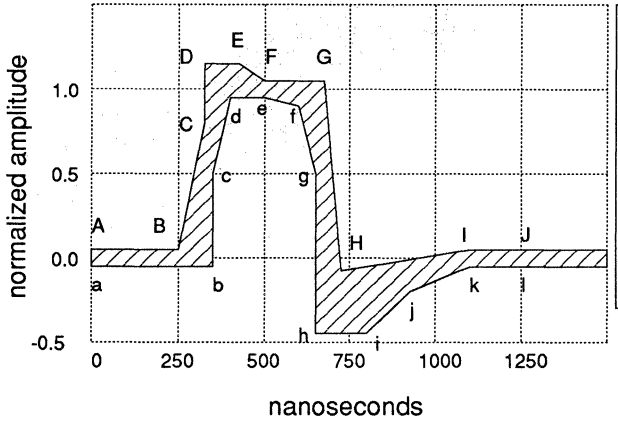
Pulse Shape Requirements

T1 equipment designed for central office use must interface with a DSX-1 cross connect. For most applications, the transmitter is located within 655 feet of the cross connect. All T1 pulses arriving at the cross connect must meet the pulse amplitude and template requirements at the cross connect as shown in Figure 1, whether the originating transmitter is a few feet away or 655 feet away. The line is terminated with a 100 Ω load. The pulse amplitude is measured at the center of the pulse and must be within 20% of 3.0 volts according to CB-119. (Other specs differ slightly; be sure to consult the applicable spec.) If the amplitude requirement is met, the pulse may be linearly scaled to fit within the template.

PCM-30 pulse shapes are specified in Rec. G.703. In this case, the pulses are measured at the output of the line driver only, and *not* required to meet the pulse template over a variety of cable lengths. The pulse must fit the template without scaling.

For 2.048 MHz operation, there are two amplitudes specified depending on the type of cable used. For 75 Ω coax, the pulse height is 2.37 volts ±10%. For 120 Ω symmetrical (shielded-twisted) pair, the specified pulse amplitude is 3.0 volts ±10%. The CCITT G.703 template for 2.048 MHz operation is shown in Figure 2.

CCITT also specifies a template for operation at 1.544 MHz which is shown in Figure 3. This pulse shape is very similar to the pulse shape



Maximum Curve		Minimum Curve	
A	(0, 0.05)	a	(0, -0.5)
B	(250, 0.05)	b	(350, -0.5)
C	(325, 0.80)	c	(350, 0.50)
D	(325, 1.15)	d	(400, 0.95)
E	(425, 1.15)	e	(500, 0.95)
F	(500, 1.05)	f	(600, 0.90)
G	(675, 1.05)	g	(650, 0.50)
H	(725, -0.07)	h	(650, -0.45)
I	(1100, 0.05)	i	(800, -0.45)
J	(1250, 0.05)	j	(925, -0.20)
		k	(1100, -0.05)
		l	(1250, -0.05)

Figure 1. AT&T CB119 T1 pulse template

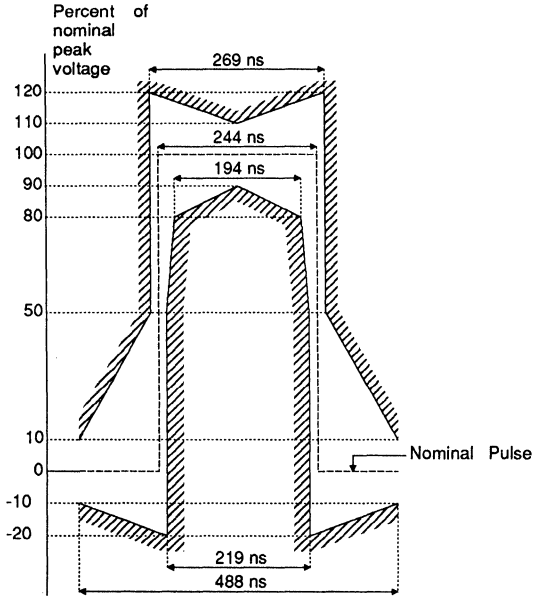


Figure 2. CCITT Rec. G.703 pulse template for 2.048 MHz operation

shown in Figure 1. As in T1 applications, the pulse is required to meet the template at the digital distribution frame. In this case however, the pulse must meet the mask without scaling. The peak undershoot is specified not to exceed 40% of the peak pulse amplitude.

The remainder of this paper discusses procedures which should be used to accurately measure pulse shapes. There is also a section on measuring pulse imbalance and power transmitted levels.

Reflections

When transmitting a high frequency pulse down a transmission line, a portion of the pulse will reflect wherever it encounters an impedance mismatch. The amount of reflection is proportional to the impedance mismatch; the greater the mismatch, the greater the reflection of the pulse. Even hooking two pieces of wire with different characteristic impedances together will cause reflections. In order to avoid reflections in a transmission line, impedance mismatches should

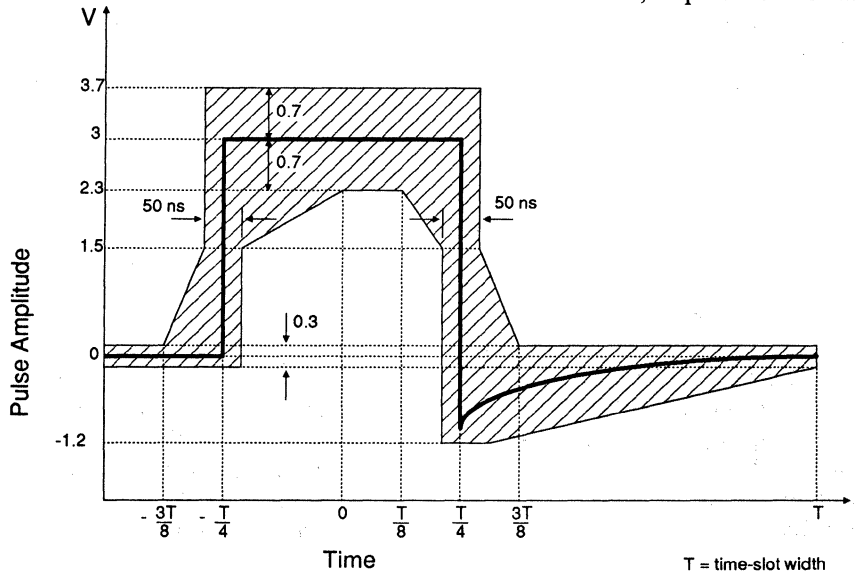


Figure 3 - CCITT Rec. G.703 pulse shape for 1.544 MHz operaton.

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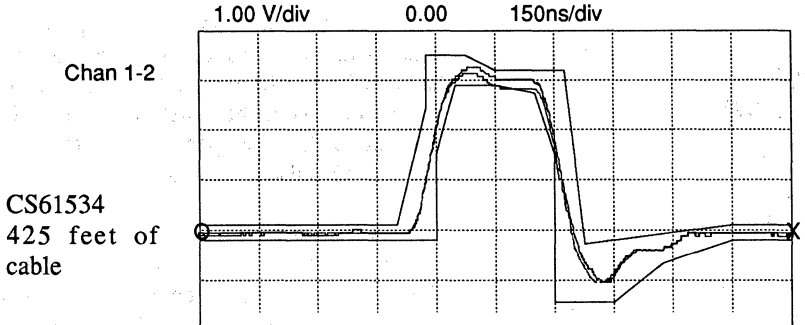


Figure 4 - The smaller pulse's amplitude was reduced by combination with a reflection from a previously transmitted pulse in a repeating 1 out of 2 pattern. The larger pulse is from a 1 out of 16 pattern.

be avoided, and the line should be terminated with a load that is equal to the characteristic impedance of the line. Proper terminations are every bit as important when measuring pulses in the lab as they are in connecting up the network.

Remember that the load specified for T1 pulse shape measurement is 100 Ω. A commonly used cable in T1 applications is Western Electric ABAM cable which has a characteristic impedance in the neighborhood of 110 Ω. This means that even an otherwise optimal test setup will have a reflection at the load. When this reflection returns to the source, it is likely to experience an even greater impedance mismatch at the driver outputs and therefore have a relatively large reflection component at the source.

One way to reduce reflections at the load is to terminate the desired length of cable with a comparatively long piece of the same type of cable which is then terminated with the load resistor. Such a setup begins to approximate an infinite amount of cable which should provide an optimal impedance match for the test length. In addition, any reflection from the load resistor will be attenuated by the resistive loss of the cable and should be insignificant by the time it returns to the measurement point. *However*, for Central Office equipment, the standard test method is as follows: the cable will be disconnected at the DSX-1, terminated with a 100 Ω load resistor, and measured for compliance with the template. This approach should be used in your lab as well.

Reflections in a lab setup can be minimized by eliminating impedance mismatches wherever possible. The best way to eliminate mismatches is to use the same type of test cable everywhere; that is, from the output of the driver to the input to the oscilloscope. Impedance mismatches due to coax test cables, probes, test leads, or any other leads connected to the line will cause reflections.

Data Pattern

The first step in measuring pulse shapes is to notice that the T1 specifications call for an *isolated* pulse. Unless the pulse is sufficiently isolated, reflections on the line can badly corrupt the measured pulse shape. However transmitting a repeating pattern is necessary to trigger the oscilloscope. A repeating one out of 16 pattern (repeating a 1000 0000 0000 0000 AMI data pattern) is recommended to isolate the pulses to allow reflections to die.

Why is the isolated pulse important? Let's assume that a portion of the pulses will be reflected at both ends of the line. As a pulse travels down the

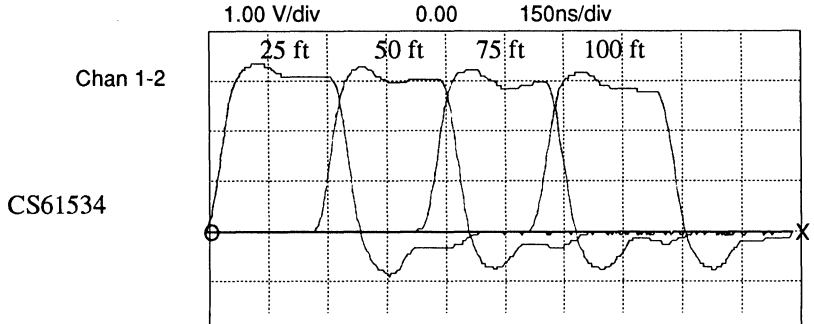


Figure 5 - Four pulse plots are superimposed here to show pulse distortion which is caused by self reflection for cable lenghts of less than 100 feet. Note how the reflection component moves along the pulse as the cable gets longer

line at about 0.66 ft/ns, it will reflect from the termination, reflect from the source, and return to the termination of a 425 ft cable about 1932 ns after it was transmitted, just in time to combine with a pulse transmitted 1296 ns later when it arrives at the load. Depending on the sign of the reflections, this reflected pulse can be either added to or subtracted from the pulse arriving two bit periods later. This is the situation one would observe when transmitting a one out of two pattern as shown in Figure 4. A one out of 16 pattern allows plenty of time between each pulse for reflections to die out of a properly terminated line, allowing accurate measurement of the transmitted pulse.

CCITT specifications for 1.544 MHz operation are very similar to North American T1 specifications in that an isolated pulse is specified and pulses are measured at the distribution frame. There are two significant differences for 2.048 MHz operation. First, G.703 specifies that all pulses must meet the template, not just an isolated pulse, implying that any data pattern is acceptable. Thankfully, the second difference is that pulses are measured at transmitter output rather than after some length of cable, so reflection interaction due to different cable lengths is not a consideration.

Self Reflections

When making pulse shape measurements on short line lengths (generally less than 100 feet), pulses can reflect upon themselves, distorting the pulse shapes of isolated pulses as shown in Figure 5. Nonisolated pulses will likely suffer even greater distortion. Self reflection is unavoidable as long as impedance mismatches exist. Proper termination is crucial when measuring pulse shapes for CCITT G.703 compliance at 2.048 MHz.

Equipment

It is important to understand and identify the sources of error in measurement equipment and choose equipment to minimize any error sources. Since pulses are transformer-coupled to the line, they are differential in nature, so pulse shape measurement should be made in a truly differential manner. Grounding one wire for single ended measurement can introduce uncertainties due to transformer nonidealities, and cable characteristics such as distributed capacitance to a ground, which may be different from the oscilloscope ground. Consider that in making a single ended measurement, one wire is referenced to ground while the other wire is unbalanced.

The exception is transmission over 75Ω coaxial cable at 2.048 MHz. CCITT G.703 states that the outer conductor shall be connected to ground at the output port. Accordingly, measurements of pulse shape should be made with the outer conductor grounded at the oscilloscope input. A single oscilloscope channel is sufficient.

Probes and oscilloscope amplifiers with good balance and high CMRR should be used. Probes, if used, should have low capacitance so pulse distortion is minimized. Unmatched 10X probes may cause significant measurement error due to relative inaccuracies in the 10X attenuation and poor CMRR. Also, the CMRR between two channels of an oscilloscope is rarely specified and is generally very low.

Eliminating the probes altogether is generally preferable. In this case, the same type of cable should be used from the output of the line driver to the input of the oscilloscope. Ideally the load for the cable should be placed at the inputs to the oscilloscope. Some oscilloscopes can be set for internal 50 Ω termination at the inputs. Alternatively, a 50 Ω termination can be connected to both oscilloscope inputs. Providing 50 Ω termination from each wire to ground is analogous to connecting 100 Ω across the two wires, but has the distinct advantage of providing both oscilloscope inputs with signals referenced to the same point rather than having the inputs floating with respect to one another. The 50 Ω resistors should be equal in resistance. Fifty ohm terminating plugs work well and are readily available.

For compliance with CCITT G.703, use 60Ω terminations from both channels to ground when evaluating equipment designed for 120Ω shielded twisted pair, and a 75Ω termination resistor from oscilloscope input to oscilloscope ground for equipment using 75Ω coax. With a little imagination, these terminations can be easily created and attached to the oscilloscope inputs.

Some specifications such as AT&T Publication 43801 call for a 100 Ω resistor connected across TIP and RING. If this setup must be rigidly followed, use either matched differential probes, or the shortest leads possible between the load and the oscilloscope. It may be necessary to use two 50 Ω resistors in series so the oscilloscope can be grounded to a reference point relative to the line so it can trigger. (This is the same as 50 Ω terminators.) These resistors must be accurately matched.

Digital oscilloscopes offer some features such as plotting, amplitude scaling and time and amplitude measurement which makes their use desirable when evaluating pulse shapes. However, be advised that digital oscilloscopes have inherent inaccuracies in the analog to digital conversion and in the sampling process. Most high frequency digital oscilloscopes use either 6-bit or 8-bit A-to-D converters. A six-bit ADC divides a full scale input into only 64 parts, so the quantization error is significant. Any gain error or offset error in the converter, in either channel or between the two channels, will result in amplitude error and distortion of the actual pulse shape. Calibration of a digital oscilloscope is essential to making accurate measurements. Any noise present on the signal or within the converter during the conversion process will result in an error in the conversion. Averaging a fairly large number of samples will help reduce uncertainties caused by noise (quantization or external). Such averaging cannot compensate for ADC nonlinearity errors however.

Sampling uncertainty of digital oscilloscopes must also be considered. If the oscilloscope is sampling at 150 MHz, the sample period is 6.7 ns. For pulse width measurements, the worst case time quantization error is 13.4 ns which can be significant when measuring 244 ns or 324 ns wide pulses. Once again, averaging several samples effectively eliminates any error due to sampling uncertainty.

Digital oscilloscopes are very useful in evaluating pulse shapes. However, the averaging process will tend to mask pulse-to-pulse variations that are undesirable. It is advisable to check the results on an analog oscilloscope which is in calibration.

A oscilloscope with a delayed triggering feature is essential. Delayed triggering allows precise positioning of the isolated pulse on the screen, and also allows the user to amplify and observe a small portion of the pulse which may require greater scrutiny. Delayed triggering also allows for fairly easy comparison of positive and negative pulses for verifying that pulse imbalance requirements are met.

No matter which instruments you have available, a proper test setup is essential. Three good measurement techniques are as follows:

1) An active differential probe such as the Tektronix P6046 allows differential signal processing at the probe tip with very high CMRR. Only a single channel on the oscilloscope is required thus removing CMRR considerations at that point. This probe offers distinct advantage when using a digital oscilloscope in that the addition of the quantization errors of the two channels is avoided. For both analog and digital oscilloscopes channel-to-channel inaccuracy and imbalance are no longer an issue and CMRR is much better.

2) Use a true differential amplifier with good common mode rejection such as the Tektronix 7A13. Run the test wire all the way to the diff amp's input (avoid using test leads for interconnection) and terminate the line at the inputs with 50Ω (60Ω for CCITT 120Ω shielded twisted pair). The only probes that should be considered for use in such measurements are matched probes with high CMRR like the Tektronics P6055. When using probes, make sure they are calibrated.

3) As previously discussed, using a standard two channel oscilloscope has some disadvantages, but may be the only method available for pulse shape measurement. Once again, it is best to run the test wire all the way to the oscilloscope inputs and terminate the line at the oscilloscope inputs. (If probes are necessary, use matched and calibrated probes.) TIP should be connected to one channel and RING to the other channel. Invert channel 2 and add it to channel 1. Always set the oscilloscope inputs for DC coupling to keep the internal oscilloscope capacitors out of the circuit. The amplifiers should always be in the calibrated configuration.

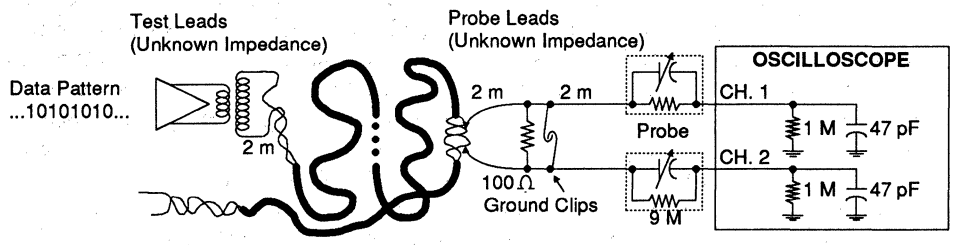
The following figures illustrate pulse measurement techniques and show an example of the error that can be caused by poor techniques. Figures 6 and 7 show some DOs and DON'Ts for measuring pulse shapes. Figure 8 shows the effects of terminating the line with a floating 100 Ω resistor and measuring the signal across the resistor with unmatched probes.

Pulse Shape Evaluation

The pulse displayed on the oscilloscope must be checked for amplitude and conformance to the pulse template. The pulse amplitude is measured at midpulse. The method for checking for conformance with the template depends on the specification. For CCITT specifications, the pulse must fit the template with no scaling allowed. For CB-119, the pulse can be scaled by a linear factor to fit within the template. Figure 9 shows a pulse which has been aligned, scaled and plotted from a digital oscilloscope onto a template.

When evaluating pulse amplitude and template conformance, be sure to test over the line driver's specified operating voltage and temperature ranges. For amplitude measurements, setting the oscilloscope for 0.5 V/div is best, while 1.0 V/div is convenient for template matching.

What's Wrong With This Picture?

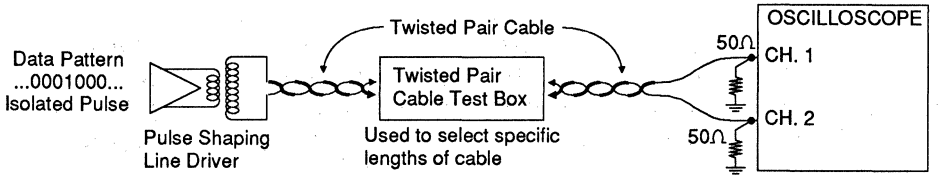


- Numerous impedance mismatches - reflections galore
- Data pattern does not provide an isolated pulse.
- Floating termination - no ground reference for measurement
  (but required by 43801)
- Undetermined tail on cable - improper termination
- Are probes precisely 10:1?
  Have they been calibrated correctly?

Figure 6 - How NOT to measure pulses.

PULSE MEASUREMENT USING TWO CHANNEL OSCILLOSCOPE

- Avoid reflections due to impedance mismatches
  - Despite taking precautions, neither end of the cable will be ideally terminated so watch for reflections from previous or current pulse
  - Use the same type of cable where ever possible



- Oscilloscope should be DC coupled
- High-resolution, digital oscilloscopes are nice because pulses can be precisely scaled and plotted making evaluation easier
- Test cable terminated at oscilloscope input

Figure 7 - Recommended pulse shape measurement test configuration and guidelines.

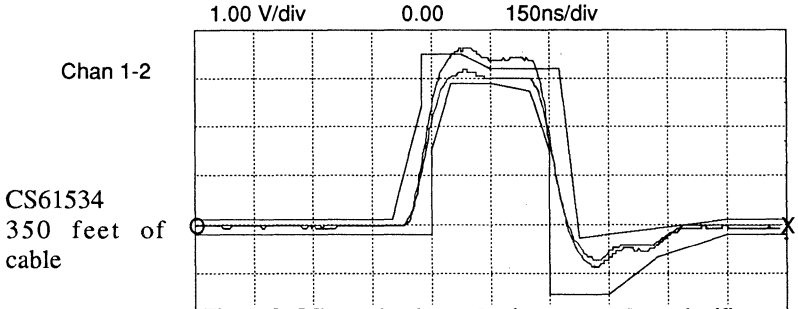


Figure 8 - Mistermination and gain error can have significant effect on pulse amplitude. The larger pulse results from the use of probes which are not well matched, otherwise the test setup for both pulses shown is identical.

Creation of the pulse template against which the displayed pulse is to be evaluated is worthy of consideration. It is important that the template have the correct proportions so that the pulse may be accurately evaluated. In some cases, the template must be created to an absolute scale so it can overlay the pulse or have the pulse plotted over it. Reproduction of the pulse template is very tricky since copiers tend to distort the original. A first generation photocopy can have enough distortion to render the copied template useless. Only through painstaking effort can a useful copy be produced (and if this method is used, make an abundant number of copies once the copied template is accurate).

To evaluate a pulse displayed on the oscilloscope's CRT, create a template which is scaled to the oscilloscope grid on a transparency, align the template to the grid and afix the template to the CRT. Center the pulse in the template. Scaling the pulse by adjusting the amplifier gain is only possible when using a single channel oscilloscope, a differential amplifier, or a digital oscilloscope. When using a two channel oscilloscope, method three, do not use the amplifier's gain adjustment (uncalibrated) to adjust the pulse amplitude to match the template. Adjusting one channel only results in a nonlinear change in the pulse. Additional templates scaled to larger and smaller amplitudes are required.

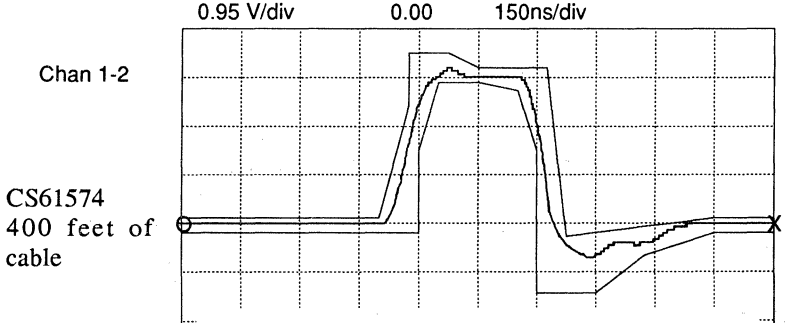


Figure 9 - Plot of a properly terminated, isolated pulse from a CS61574. Note that the amplitude scaling feature of the digital 'scope was used to boost the pulse amplitude and center the pulse in the template

Once everything is satisfactorily aligned, take a picture. It is much easier to describe, complain about or compare pulse shapes on hard copies. A hard copy also provides a permanent record for future reference.

Most digital oscilloscopes have the capability to transfer the image displayed on their screen to a plotter. There are three basic methods of plotting available. The most sophisticated method allows entry of the template parameters to the system so the template is plotted to the appropriate scale along with the pulse.

A second method offered by some systems, allows the operator to align the oscilloscopes plot dimensions to an independently created grid. This method allows the user to create the template to a convenient scale. Using the plotter, the corner points of the oscilloscope's grid are physically aligned with the corner points of the grid on the plotter paper. The plotter then scales the plot of the oscilloscope's grid to fit the grid on to plotter paper. This technique is especially good when using photo copies of an original grid and template. Since the plot is scaled to fit, copier distortion is irrelevant.

The third method involves generating a template for a plotter without a scaling feature. The template must be created to exactly the same size as the plotter's rendition of the oscilloscope grid, and positioned on the plotter paper at precisely the point at which the oscilloscope's display is plotted. The biggest problem here is creating a sufficiently large number of blank templates which are the right size and in the right place so they will line up with the plot. The alternative is to generate a single template on a transparency to overlay the plots, but this approach makes it difficult to evaluate a large number of plots.

An especially nice feature of digital oscilloscopes is the gain scaling which allows the user to linearly scale the pulse either up or down to fit a fixed template. For instance, if the pulse is a little short, the gain may be set for 0.95 V/div, thereby making the pulse a little taller. The horizontal and vertical settings are usually plotted along with the trace, so these settings are recorded as well. Take care to maintain the time scale to a fixed value which corresponds with the template. Pulse width scaling is not allowed.

A note about the CB-119 pulse template: the minimum pulse width allowed is 300 ns, the maximum is 400 ns. If the pulse width is based on a 50% duty cycle of a 1.544 MHz clock, the pulse width will be 324 ns. This allows only 12 ns of margin to either side of the template's minimum curve. When compared to the template, the pulse will look narrow, but it is really all right. (Presumably, the minimum allowable pulse width is kept wide to help maximize receiver jitter tolerance.) The opposite situation exists for CCITT G.703 pulse width specifications which range from 194 ns to 269 ns. A 50% duty cycle pulse, 244 ns, is a little on the wide side.

Positive/Negative Imbalance and Power Levels

Pulse imbalance and signal power level measurement are both intended to ensure that there is no significant DC offset at the termination of the line. Since positive to negative pulse imbalance can result in more power at 1.544 MHz relative to the power at 772 kHz of an all ones signal, meeting the power level specifications also means pulse imbalance is satisfied.

An oscilloscope can be used for checking pulse imbalance between the positive and negative pulses. CB-119 calls for less than 0.5 dB difference between the power of positive and negative pulses. Power is roughly the product of the square of the pulse height and pulse width, so both must be investigated. There should be less than 200 mV difference in amplitude of otherwise identical positive and negative pulses. Variation in the widths of positive and negative pulses of only a few nanoseconds will also result in some pulse imbalance. One good method for comparing posi-

tive and negative pulses is through the use of a digital oscilloscope which is capable of integrating the area of a pulse; this makes for straightforward comparison of the positive and negative pulses.

Measurement of power levels in an all ones pattern is best accomplished with a specialized instrument such as the Hewlett Packard 3586B (HP 3586A for CCITT). This instrument can measure the power in a 2 kHz band at both 772 kHz and 1.544 MHz as required by CB-119. The power in the 2 kHz band at 772 kHz must be between 12.4 dBm and 18.0 dBm, and at least 29 dBm greater than the power in a 2 kHz band at 1.544 MHz . CCITT 1.544MHz specs require the power in a 3 kHz band at 772 kHz be between 12.0 dBm and 19.0 dBm and at least 25 dBm greater than the power in a 3 kHz band at 1.544 MHz. CCITT PCM-30 specs allow ±5% variation in the heights and widths of positive and negative pulses. When using this instrument, take care to terminate the line driver properly. The input impedance of the HP 3586 is selectable but 100 Ω input impedance is not offered. A HP 15508B converter will provide a 110 Ω balanced termination for the line and 75 Ω unbalanced impedance for the input of the instrument.

Alternatively, power levels can be measured using a spectrum analyzer. An estimation of the power at 772 kHz can be made by selection of the appropriate resolution bandwidth of the spectrum analyzer. As long as the power at 772 kHz meets the specification with reasonable guardband, and the difference in amplitudes of the power at 772 kHz and 1.544 MHz is several dB in excess of the spec, precision measurements are probably unnecessary.

• Notes •

Application Note

Jitter Testing Procedures for Compliance with AT&T 62411

By Roger Taylor and Bob Bridge

Introduction: This application note gives guidelines for measuring whether a design is compliant with AT&T 62411 jitter tolerance and attenuation requirements. 62411 compliance is a necessary requirement for *CPE* (Customer Premises Equipment) which is connected to T1 lines provided by AT&T. These T1 lines may be either private-line or central-office access lines. 62411 may not apply to equipment sold to telephone companies, equipment used within a campus environment or equipment used to access an alternative long-distance carrier (e.g., MCI, US Sprint, etc.).

Jitter testing can be performed using the following test equipment:

1) Jitter Generator/Receiver: e.g., Hewlett Packard 3785B
2) "2^{20}-1 QRTS (Quasi-Random Test Sequence) with 1-in-15" Pattern Generator and Receiver
3) Spectrum Analyzer

Similar equipment is available from a number of vendors including: Tekelec, Tektronix, HP, Telecommunications Techniques Corp, Navtel, Network Communications Corp, Phoenix Microsystems and Atlantic Research. For performing jitter tolerance tests, it is very useful to have the capability to create user generated patterns, in addition to the standard patterns, as will be explained later in this document.

Some of these units are integrated pattern generator/receivers and jitter generator/receivers. However, the HP 3875B is the most powerful and most flexible jitter test set available, in part because it uses analog jitter generation and demodulation.

Jitter Tolerance Measurements: The basic test setup is shown in Figure 1. A jittered clock is created by the HP 3785 and then used to clock the Pattern Generator. The Pattern Generator connects to the T1 trunk card using a twisted pair cable. The signal is routed through the T1 trunk card and synchronizer and back through the trunk card to the Pattern Receiver. The Pattern Receiver is then used to measure bit errors. The jitter tolerance of a receiver will vary with the width of the AMI pulses. It is very important that the pattern generators used have consistent pulse widths. (The pulses should meet DSX-1 type pulse requirements as identified in CB-119.)

The jitter frequencies typically checked are: 3, 10, 30, 100, 1k, 2k, 4k, 8k, 16k, 32k, 64k and 100k Hertz. The normal procedure is to select a jitter frequency, and then increase (or decrease) the jitter amplitude until you observe the boundary between no-bit-errors and bit-errors.

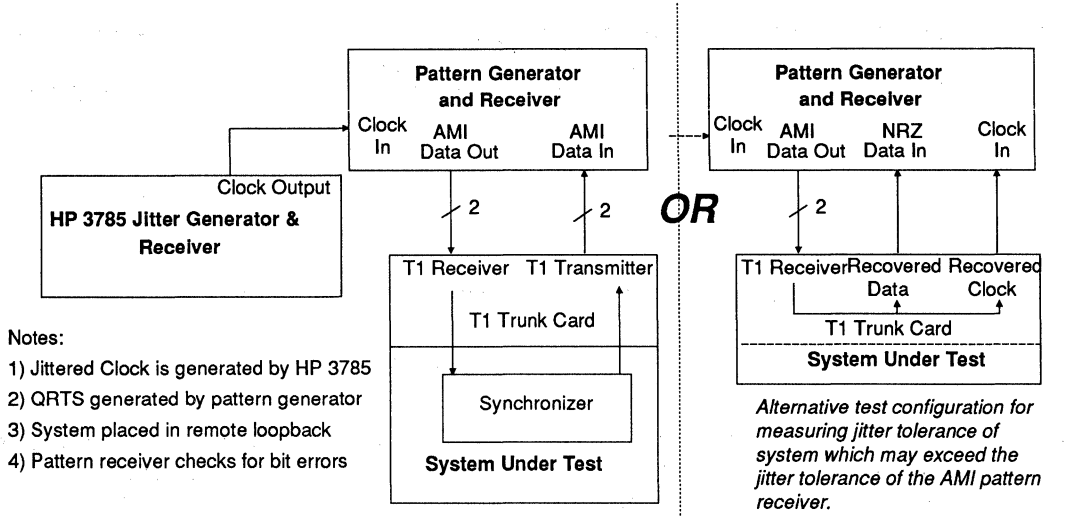


Figure 1 - Test Setup for Jitter Tolerance Measurements

It is important to determine how much the system exceeds the minimum 62411 jitter tolerance requirements since the later attenuation tests are made with three-quarters of the observed tolerance of the system. Larger tolerance levels have the benefit of raising the floor on the acceptable output jitter level during the attenuation tests.

AT&T 62411 testing calls for measuring jitter tolerance using a QRTS data pattern, which is representative of live traffic on the network. But the key to guaranteeing jitter tolerance is to test receiver performance using a data pattern which is representative of the worst case conditions within the QRTS pattern. The most stressful jitter case for a receiver occurs when the maximum deviation from the ideal arrival time occurs between two ones which are separated by a string of zeros. For example, two ones separated by seven zeros can have maximum deviation from ideal arrival time at a jitter frequency of 96,500Hz. (Maximum phase deviation occurs in 1/2 of a jitter period; eight bit periods take 5181.4ns.) Still, this maximum jitter hit is dependant on the relationship of the phase of the jitter with respect to the occurence of the string of zeros.

To truely measure jitter tolerance, one must guarantee that the maximum phase deviation between two consecutive ones separated by zeros will occur (assuming that the maximum allowable consecutive zeros is not exceeded). When using a quasi-random data pattern, it is unlikely that the jittered clock and the zero string in the data pattern will align to produce a maximum phase hit between successive ones unless the condition is tested for a long time. To guarantee 0.4 UI of jitter tolerance at jitter frequencies above 50 kHz, it is best to use a short pattern with repeating strings of 7 to 14 zeros to significantly increase the likelihood of a maximum jitter hit. Tests at Crystal Semiconductor have shown that repeating a data pattern similiar to:

AA AA AA AA 33 33 33 33 33 33 33 03 00 03 00 03 hex

gives good correlation to the QRTS pattern. This pattern is considerably shorter than QRTS (which is 2^{20} - 1 bits long) so the strings of fourteen

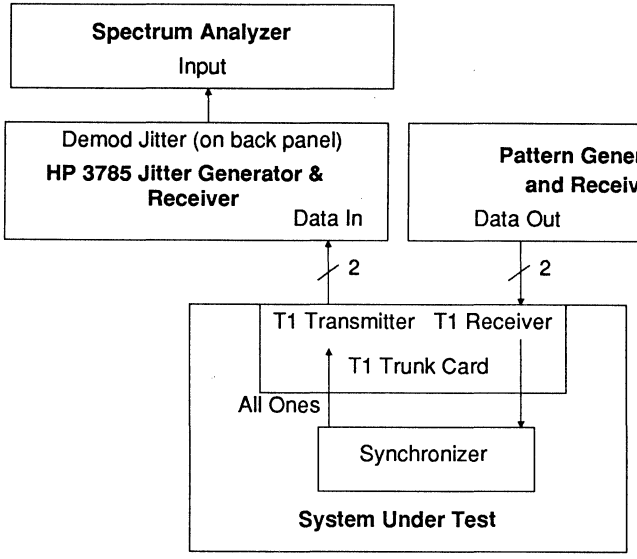
zeros occur often enough for a robust test of jitter tolerance at 51.4 kHz (the worst case jitter frequency for ones separated by 14 zeros). In addition, this pattern has sections of 50% ones, to avoid placing undue strain on the clock recovery circuit. This pattern can be modified or extended for testing different zero strings at different frequencies.

The maximum jitter frequency at which the HP 3785B operates is 77kHz, however 62411 specifies jitter performance to 100kHz. Generally, the jitter tolerance performance of a receiver will have flattened out by 77kHz, so one can assume that if the jitter tolerance curve has flattened out, and if it passes a difficult data pattern such as 2 in 16 at 77kHz, that it will also pass at 100kHz. Hewlett Packard does make a CCITT version of the 3785B - the 3785A which can produce jitter to beyond 100kHz and is available with a T1 option.

A word of caution: not all pattern generators have as much jitter tolerance as they can produce. A pattern generator's receiver which is looking for bit errors in a retransmitted (looped back) signal which has not been jitter attenuated may itself make errors in data recovery leading the tester to falsely believe that the equipment being tested is making errors. Many pattern generators have a provision for accepting recovered clock and NRZ data. A test configuration such as shown on the right hand side of Figure 1 is highly recommended for measuring jitter tolerance of equipment which does not provide jitter attenuation.

Output Jitter Measurements: The basic test setup is shown in Figure 2. The measurement looks at jitter in specific frequency bands:

1) broadband; 0.05 UI,
2) using 10 Hz to 40 kHz filter; 0.025 UI,
3) using 8 kHz to 40 kHz filter; 0.025 UI, and
4) using 10 Hz to 8 kHz filter; 0.020 UI.



Notes:
1) Jitter-free QRTS is generated by pattern generator
2) System is placed in remote loopback
3) HP 3785 demodulates jitter and provides some filters
4) Spectrum analyzer may be used to obtain jitter spectrum

Note: Measurement is much more accurate if All Ones are transmitted to the HP 3785 using the recovered clock.

Figure 2 - Test Setup for Output (Added) Jitter Measurements

The first three of the frequency bands are selected using the filters available on the front panel of the HP 3785B. The output jitter levels are measured using the Received Jitter meter on the HP 3785B. For these measurements, the HP 3785B should be set to its "1" range which is its most sensitive scale. It is important to note that the HP 3785B's published accuracy is ±4% + (≤0.035 UI) for input data patterns, and ±4% + (≤0.025 UI) for input clocks.

Because the published accuracy of the instrument is not sufficient to measure to the small jitter levels required, it is advisable to do some sanity checks. Have the jitter receiver measure the jitter from the jitter free pattern generator. This will provide a "feel" for the HP 3785's measurement floor. It may be appropriate to subtract this result from subsequent measurements.

Furthermore, using an all ones data pattern will improve the instruments accuracy slightly (approaching that for input clocks). If the system under test has a transmit all ones capability, select this function for testing transmitted jitter. The transmit clock used in this case should be same as for normal operation or remote loopback.

Observing the DEMOD JITTER output (available from the back of the HP 3785) on a spectrum analyzer may also prove enlightening. While the sum of the jitter over a frequency band is not readily available, one can observe the jitter spectrum of the demodulated signal, look for jitter spikes rising out of the noise floor, and most importantly, compare the spectrum of the jitter free pattern's source to the transmitter's output, watching for artifacts that may be present in the source or created by the HP 3785 itself.

The HP 3785 does not have internal filters for measuring jitter from 10 Hz to 8 kHz, so measuring jitter in this band requires additional work. Obviously, if the jitter from 10 Hz to 40 kHz is less than 0.020 UI, so is the jitter from 10 Hz to 8 kHz. Jitter in the 10 Hz to 8 kHz band can be mathematically approximated by measuring the jitter in the band from 10 Hz to 40 kHz and jitter and the band from 8 kHz to 40 kHz by using the following formula:

$$b = \sqrt{c^2 - a^2}$$

where b = jitter from 10 Hz to 8 kHz
c = jitter from 10 Hz to 40 kHz
a = jitter from 8 kHz to 40 kHz.

(Jitter in different bands will add as the sum of the squares.)

The most rigorous method is to build a band-pass filter which rolls off at 6dB / octave below 10 Hz and above 8 kHz. This filter is placed between the Demodulated Jitter Output and Measurement Input (both on the rear panel) of the HP 3785.

Jitter Transfer Function Measurements: The basic test setup is shown in Figure 3. The HP 3785 generates jitter at selected frequencies (the same frequencies at which jitter tolerance was measured, up to 32 kHz). The jitter amplitude that is input to the system should be one-half of the system's jitter tolerance.

Jitter attenuation is determined by comparing the amount of jitter in the signal output from the pattern generator (configuration "a") to the amount of jitter contained in the looped-back signal from the system under test (configuration "b"). The amount of jitter output from the jitter generator at each frequency should be 3/4 the receiver's jitter tolerance at that frequency. The range scale used on the HP 3785 jitter receiver should be the same for both measurements.

When the input jitter is large (> 1 UI) *and* the output jitter from the system under test is greater than about 0.1 UI, the value shown on the Received Jitter display is sufficiently accurate. When the received jitter gets small (< 0.1 UI), it becomes necessary to use a spectrum analyzer to determine the jitter attenuation.

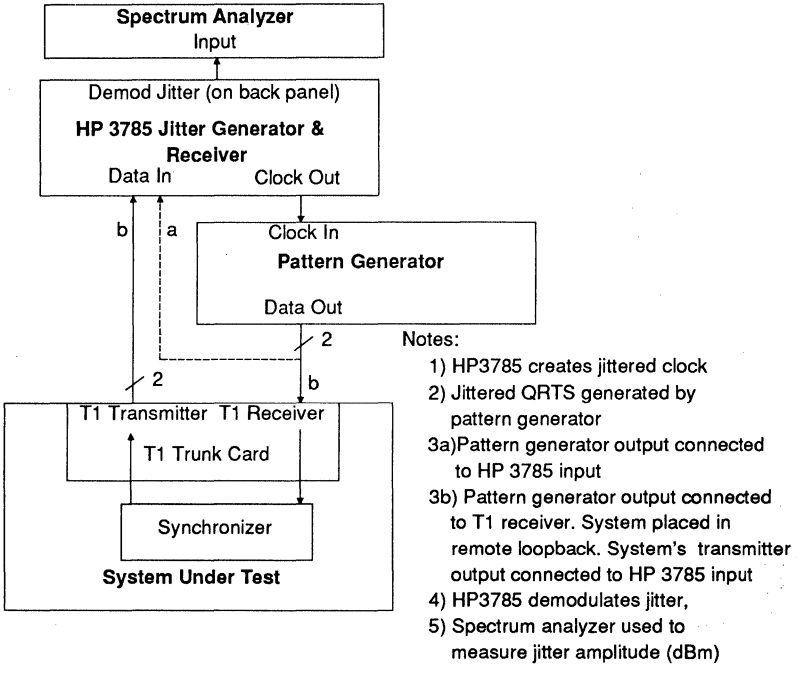


Figure 3 - Measuring Input and Output Jitter Amplitudes

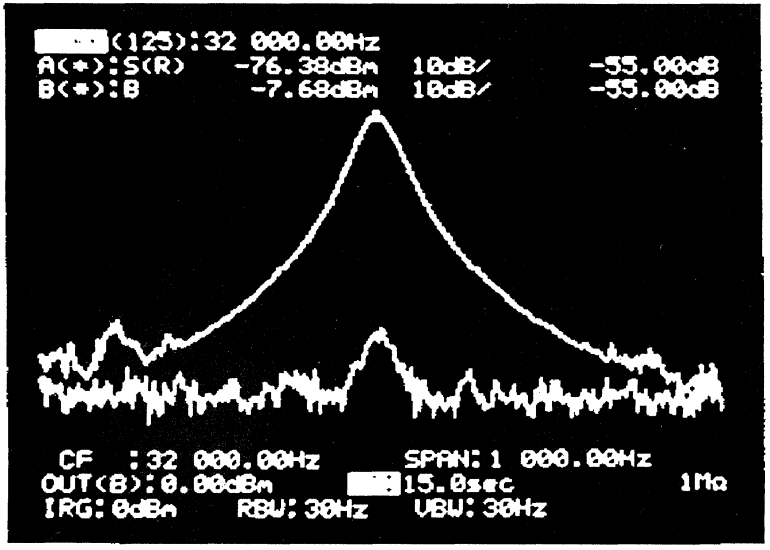


Figure 4 - Spectrum analyzer photograph showing 68.7dB of jitter attenuation at 32kHz.

A spectrum analyzer must be used for two reasons. First, the accuracy of the jitter receiver is only ± 4% + (≤ 0.035 UI); second, the value displayed by the jitter receiver is representative of the jitter over the selected bandwidth, not the jitter at the frequency being tested. Figure 4 shows a spectrum analysis display representing jitter attenuation. The upper curve shows the demodulated jitter present in the AMI data pattern output from the pattern generator. The lower curve shows the demodulated jitter present in the signal from the system under test. The attenuation is the difference in the amplitude of the two curves at the frequency of interest (shown at the top/center of the display).

It is wise to observe the output clock of the jitter attenuator in the time domain using an oscilloscope. This can be done by triggering the oscilloscope with the jitter free clock source, and observing edges of the jitter attenuated clock in the 1ns to 5ns time domain. Observations on a spectrum analyzer focus only on a narrow bandwidth. Anomalies created by the jitter attenuator that may appear at other frequencies would go unnoticed on the spectrum analyzer but the oscilloscope might indicate that more jitter is present. For example if input jitter of 0.3 UI is attenuated by 60dB, the output jitter should be 0.003 UI, which corresponds to about 2ns of time domain jitter. If the oscilloscope indicates something different, further investigation is warranted.

Additional Considerations: When testing for compliance to 62411 it is often a good idea to expand the scope of some of the tests slightly to look for anomalous behavior of the system under test, and evaluate the robustness of the system's design. Here are some suggestions: Evaluate the system's performance as power supply and temperature are varied. ICs using external components (inductors, capacitors, and quartz crystals) may be particularly susceptable to temperature or supply variations.

It is prudent to check performance over the T1 frequency range allowed by the system. AT&T 62411 specifies a frequency tolerance of ±75Hz (±50 ppm). Some circuits will have sensitivity to frequency, and that sensitivity might be amplified by variations in temperature or supply. Verify that the frequency tolerance of the receiver exceeds ±50 ppm, and check for anomalous behavior of the jitter attenuator as the T1 frequency is varied.

Testing for frequency dependance generally requires a frequency source which can be set to within a few Hertz of a desired frequency. The HP 3780A Pattern Generator / Error Detector has an option which allows the user to adjust the output clock frequency with great accuracy to frequencies within 50ppm of 1.544MHz. This clock can be used to externally clock a jitter generator, another pattern generator, or to simply vary the frequency at which the HP 3780A outputs a data pattern.

Verify that the receiver will readily acquire lock on to a data stream which is presented while the receiver is in a "loss of signal" state. This test will show how well the receiver locks on to a T1 signal when it is first input, or recovers from momentary interruption in the signal. Also see if the receiver will false lock when initially presented with a data pattern with low ones density such as a 1 of 8 or 1 of 16 pattern. A good design should immediately lock on to any valid input signal, even one with low ones density.

For loop-timed applications, it may also be important to evaluate the receiver's loss-of-signal, LOS, response. Check the receive circuit's LOS criteria: how many consecutive zeros, or how much pulse amplitude decay before LOS is declared? More importantly, test the circuit's recovered clock output. The recovered clock should smoothly transition to a reference clock when LOS is declared to ensure that no anomalies propagate to the system's backplane timing.

Application Note

AT&T 62411 Design Considerations - Jitter and Synchronization

By Bob Bridge and Greg Stearman

INTRODUCTION

This application note outlines the technical requirements which must be considered when designing a system to meet the AT&T 62411 synchronization and jitter requirements. The first section discusses how the digital network is synchronized. This section is followed by a discussion of the jitter/synchronization requirements for trunk cards and system clocks.

AT&T 62411 is the network interface specification which should be adhered to at the point of demarcation between the AT&T network and the customer premises location. It applies when connecting *CPE* (Customer Premises Equipment) to an AT&T 1.544 MHz access line or private line. Note that 62411 does not usually apply to equipment sold to telephone companies, equipment used internally to a campus environment or equipment used to access an alternative long-distance carrier (e.g., MCI, US Sprint, etc.).

AT&T 62411 has gone through numerous revisions (1983, 1985 and 1988) with the most recent version published in 1990.

SYNCHRONIZATION OF DIGITAL NETWORKS

The digital telephone network is synchronous. "Synchronous" implies that all T1 systems in the network are designed to operate at exactly the same average frequency (1.544 MHz ± 0 ppm). Synchronous operation is required so bits of information are not dropped as data is transfered between the various sinks and sources in the network. Imagine the problem that would occur in the codec of a digital telephone set if the codec were required to perform its A/D conversions and D/A conversions at different clock rates.

Synchronization is achieved via the hierarchical distribution of a Stratum 1 clock (Figure 1). Each carrier has one or more Stratum 1 clocks. The frequency of this master clock is distributed via various transmission media (optical cable, microwave radio and satellite) through a hierarchy of switching systems (toll, tandem and central-office switches) until it finally reaches the CPE. The CPE typically recovers the frequency of the incoming T1 line, and uses that frequency as the basis for its system clock and for retransmitting back toward the network. Typically, the network switching systems have Stratum 2

and 3 clocks, and the customer system has Stratum 3 or 4 clocks. This overall timing plan is defined in ANSI T1.101-1987, Synchronization Interface Standard for Digital Networks.

The engineering of a network needs to ensure that the network will remain locked to a Stratum 1 frequency even upon the failure of one or more trunks that relay the timing information.

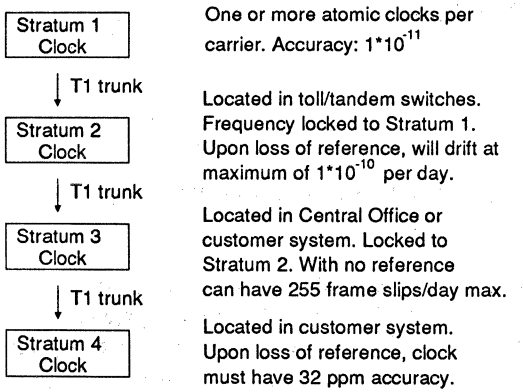


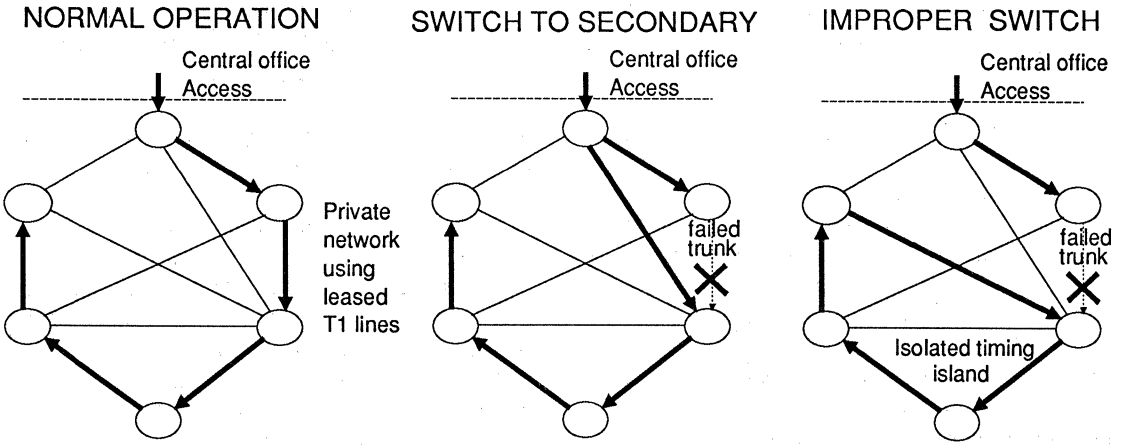
Figure 1 - Digital Timing Hierarchy

Figure 2 shows how a Stratum 1 traceable timing reference is passed through the T1 trunks of a private network. Upon failure of a trunk, a secondary path is used. Upon selection of an inappropriate secondary reference, an isolated timing island (with no master clock source) is created.

Figure 3 shows a typical system configuration where more than one trunk is used to input a traceable timing source into the system. Upon the failure of the primary timing source, a switch is made to a backup timing source. In the rare event that all timing sources fail, the system depends upon the ability of the synchronizer to free-run near the desired frequency.

To prevent chatter, it is important that there be hysteresis in the switch between reference sources. A switch should not be repeated any sooner than 10 seconds after the last switch, and only if one of the following conditions exists:

1) Phase hit of 1000 ns with phase slope $\leq 6.1 \times 10^{-5}$
2) Loss of signal (all zeros) for 0.10 seconds
3) 10^{-3} BER for ≥ 2.5 seconds
4) Excessive Input Jitter amplitude (Figure 8).



Stratum 1 tracable timing reference is transfered on trunks shown with bold lines.

Figure 2 - Multiple Paths to Stratum 1 Clock

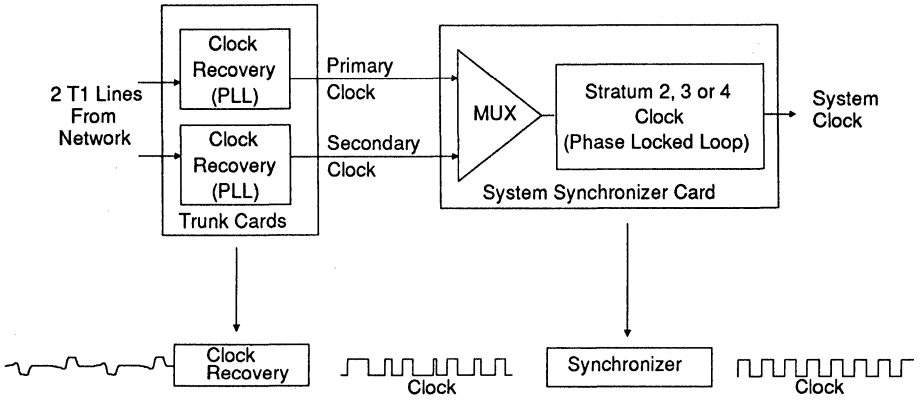


Figure 3 - Multiple Timing Sources Feeding a System Synchronizer

Synchronization plans for private networks can become, in practice, quite complicated. Figure 4 shows a multi-state private network with connections to multiple inter-exchange carriers, multiple local-exchange carriers and an international carrier. Also note that Bell South has trunks to three inter-exchange carriers. In this example, the PBX in Atlanta can be the timing source for the private lines to Long Beach. The Atlanta PBX gets its Stratum 1 traceable source from AT&T via Bell South. The PBX in Long Beach uses this AT&T timing to talk to Europe and to GTE of California.

CPE falls into one of two categories from a synchronization point of view. The CPE can either relay incoming timing to another downstream system, or it can terminate the timing

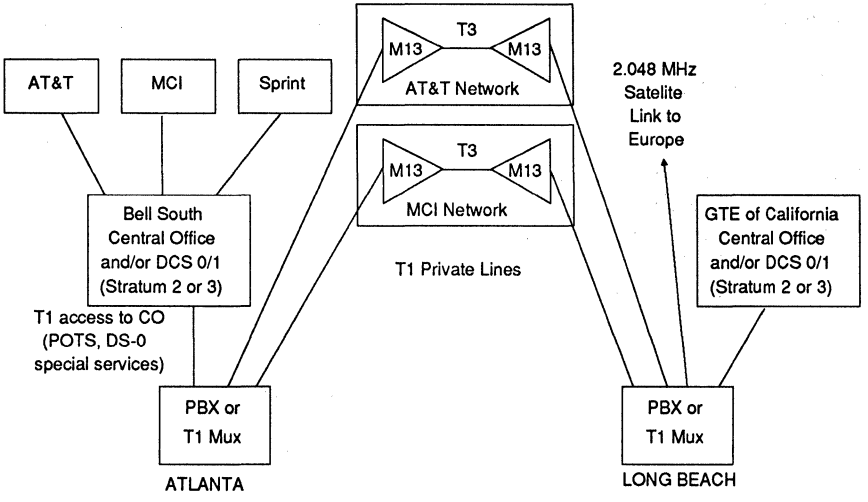


Figure 4 - Example of Private Network

chain. When a system terminates timing, failure of the system does not affect the timing of any downstream systems. This situation is refered to as *loop timing*.

A system synchronizer must meet a variety of requirements, including selecting a timing reference source to use, maintaining lock to that reference clock, tolerating impairments on the timing reference, attenuating jitter, and free-running at a specified frequency accuracy when all references are lost.

These requirements differ between systems that relay (or transfer) timing (Stratum 4 Type I, Stratum 3 or Stratum 2) and loop-timed systems (Stratum 4 Type II) that don't relay timing. In particular, in systems which relay timing, the maximum rate of change of the system synchronizer frequency must be limited (see definition of Maximum Time Interval Error in ANSI T1.101). Controlling the rate of change is important because if the synchronizer oscillates (i.e., overshoots then undershoots the target frequency) while acquiring lock or during degraded timing reference conditions, that frequency deviation can be relayed through all successive downstream systems.

An overview of Stratum requirements are given below:

Stratum 2: This is the highest performance level available to CPE, and is rarely used (except in very sophisticated CPE). The clock must have a free-running accuracy of 1,544,000 ± 0.025 Hz. Redundancy is required so the synchronizer must be duplicated. The external reference clock must be Stratum 1 or 2 since the pull-in range of the synchronizer is only ± 0.05 Hz.

Stratum 3: Stratum three clocks must also be duplicated, and are required to have free-running accuracy of 1,544,000 ± 7.1 Hz. This results in a frame-slip rate (while free running) of ≤ 255 frame slips in the first 24 hours. The external reference clock must be a Stratum 3 or better clock, since the pull in range is only ± 15 Hz.

Stratum 4 (Type I): This is normally the stratum level chosen for multi-T1 line CPE. Free-running frequency requirements are 1,544,000 ± 50 Hz, and the pull-in range is ± 100 Hz Additional pull-in range is recommended, since older equipment in the telephone company buildings are allowed to have output frequency variations of T1 ± 130 ppm (± 200 Hz). Type I does not require redundant clock hardware. However, just like Stratum 2 and 3 clocks, the Type I clock must gracefully handle rearrangements. "Gracefully" means that the rearrangements must not result in abrupt phase discontinuities in the output clock. Examples of rearrangements are:

1) a switching of timing reference (for example from T1 card "n" to card "n+1"),
2) automatic protection switch to a redundant synchronizer card, or
3) any change in clock mode

Stratum 4 (Type II): This is the lowest grade clock available, and normally would be used only in small systems (such as a single-T1 line system). Type II synchronizers cannot be used if the system transfers timing to a downstream system. The synchronizer clock output is required only during successful loop-timing. When loop-timing fails, the system no longer is required to transmit toward the network. There is no requirement on the synchronizer's free-running frequency. Nor is there any requirement to handle rearrangements. During loop-timing the frequency of the clock must be 1,544,000 ± 50 Hz. The pull-in range is 1,544,000 ± 100 Hz.

JITTER IN SYNCHRONOUS NETWORKS

Although the frequency of the T1 signal is well controlled (32 ppm), the signal itself can contain significant amount of jitter. *Jitter* is defined as a short-term variations in the position in time of a signal (or bit) from its ideal position. In other

words, the bit could arrive at a receiver slightly sooner or later than expected. Jitter can cause bit errors or other impairments to occur. When jitter occurs at a 10 Hz or lower rate, it is arbitrarily defined as *wander*. Jitter and wander can be simultaneously present. Figure 5 shows high-frequency jitter superimposed upon low-frequency wander.

Due to the characteristics of the phase-lock loop technology used in trunk cards and system synchronizers, jitter can be more readily filtered than can wander (Figure 6). Normally, most wander which is input on a timing reference source will be relayed to all downstream systems.

A primary source of wander is frequency instability in a system synchronizer during a switch between timing reference sources. Why does the synchronizer need to switch between timing sources? One major source of errors is upstream clock rearrangement (typically two per day will reach Stratum 4 nodes). While acquiring lock to the new source, wander can be created and sent to all the downstream timing sources. Stratum 2 clocks can take hours/minutes to reacquire lock after a switch. Stratum 4 clocks take seconds to reacquire lock. This wander can be amplified by each of the downstream synchronizers, causing an ever-larger wave-of-wander to spread out through the network.

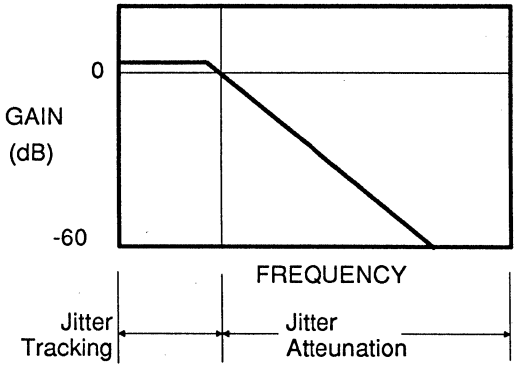


Figure 6 - Jitter Transfer of PLLs

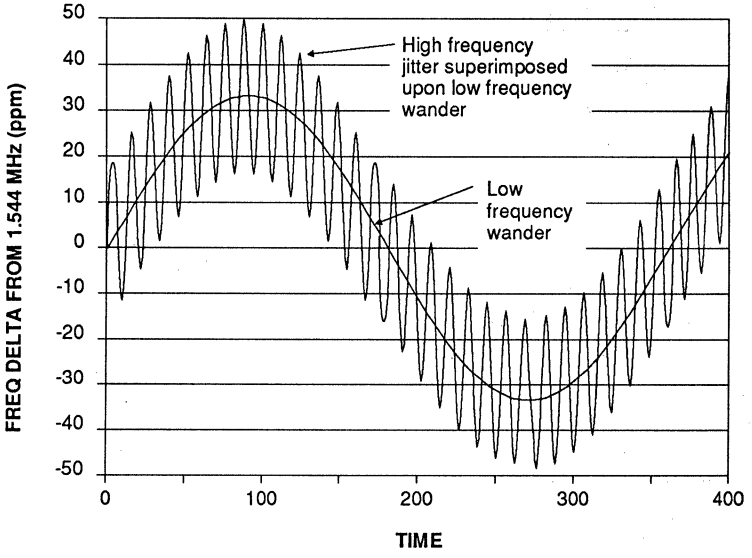


Figure 5 - Jitter Superimposed Upon Wander

The sources of jitter include data-dependent jitter introduced by line repeaters, jitter created by asynchronous multiplexors (such as M13 muxes) and jitter (phase) hits attributed to transient behavior of clock sources or other sudden changes in transmission facilities. Jitter is not a significant problem for equipment as long the trunk card and system synchronizer meets specificed jitter tolerance requirements.

62411 JITTER REQUIREMENTS

The motivation behind 62411 jitter specifications is to ensure robust operation of CPE and the network despite the presence of jitter. The CPE is at the end of a local loop (whose line repeaters can create jitter) and is far removed from the network's Stratum 1 clock. To work robustly, CPE must be extremely jitter tolerant, and must remove significant amounts of the jitter received over the local loop before re-transmitting back toward the network.

Before one can understand 62411 jitter requirements, it is necessary to understand some basic terminology (Figure 7). 62411 measurements are made at the NI (Network Interface) which is the demarcation line between CPE and the AT&T line. The *CSU* (Channel Service Unit) can be either a stand-alone unit (purchased from a CSU manufacturer), or may be integrated into the T1 trunk cards of the system. AT&T views the CSU and system as one entity for 62411 testing. Jitter generated or attenuated by either the CSU or the system will impact jitter testing at the NI.

From 62411's point of view, the system has two critical components, the *digital line termination of the DTE* (more commonly referred to as a T1 trunk card), and a *synchronizer (or clock recovery circuit)* (more commonly referred to as a system clock). 62411's use of the term "clock recovery circuit" should not cause the designer to think that 62411 is referring to a clock recovery circuit in a T1 trunk card. Rather the clock recovery circuit refers to the clock which drives the system and

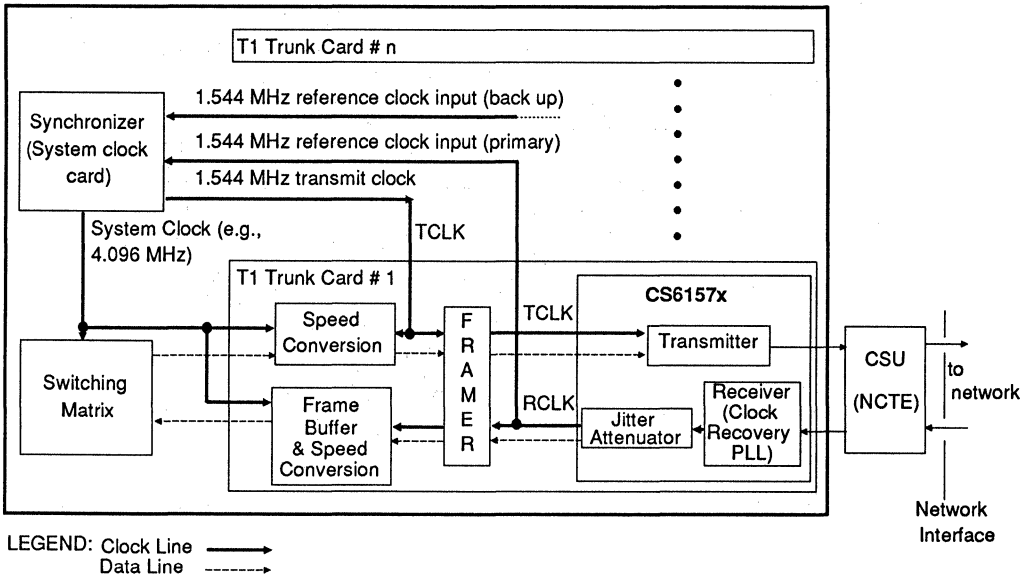


Figure 7 - Basic Terminology of 62411

backplane. Typically the synchronizer outputs a system clock at 4.096 or 8.192 MHz and is phase locked to one of the incoming T1 lines. The assumption behind 62411 is that the synchronizer is the source of jitter attenuation. This assumption is generally appropriate unless the system has a 1.544 MHz backplane or only one T1 line. In this case the synchronizer may in fact not exist as a independent sub-circuit in the system, but rather may be imbedded in the T1 trunk card.

62411 has three types of jitter specifications: input jitter tolerance (also known as jitter accommodation), output jitter generation (also known as intrinsic jitter or additive jitter), and jitter transfer function (also known as jitter attenuation). The requirements for each specification are discussed below.

All 62411 jitter tests are made with a 2^{20}-1 QRTS (Quasi-Random Test Signal) modified to ensure that no more than 14 consecutive zeros are output. The Application Note, "Jitter Testing Procedures for compliance with AT&T 62411" gives a tutorial on test procedures.

Input Jitter Tolerance: Jitter tolerance is specified for both the T1 trunk card and for the synchronizer. In fact, the tolerance requirements are more stringent for the synchronizer than the line card. The more stringent specifications ensure that the synchronizer, which is a critical system element, is extremely robust. The tolerance curves are shown in Figure 8.

Tolerance is specified for jitter frequencies from DC to 100 kHz, and is normally measured at spot frequencies. At a given frequency, the jitter amplitude is increased until bit errors are observed.

The jitter tolerance of the synchronizer is relevant for all loop-timed systems. However, testing of the synchronizer is indirect since the synchronizer

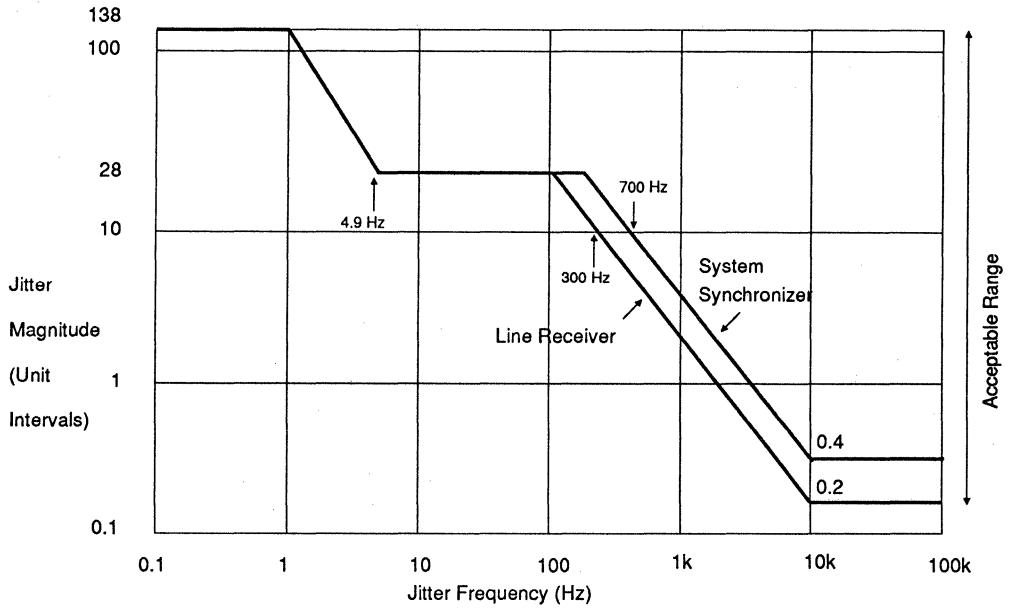


Figure 8 - 1990 AT&T 62411 Jitter Tolerance Requirement

is not directly observable at the NI, and since the trunk card is not required to tolerate as much jitter amplitude as the synchronizer. Rather, the synchronizer is said to fail if loss of synchronization at the NI is observed, or if the system is observed to permanently switch to a back-up (internally-generated) clock. The switch to a back-up clock becomes apparent because of a shift to a new frequency (which may differ from the old frequency by only a few Hz).

62411 states that jitter (wander) tolerance at low frequencies can be limited by the size of a buffer. The required tolerance is one T1 frame (193 bits) plus hysteresis (138 bits). This model assumes that a frame buffer is being employed. Frame buffers allow a system to synchronize multiple, incoming, asynchronous T1 lines at the bit, channel and frame levels. Each incoming T1 line is fed into its own frame buffer (Figure 7). All of the frame buffers are emptied into the switching matrix with all frame bits aligned. If two incoming T1 lines have frequency offsets, one frame buffer will periodically output a frame twice (to compensate for a low input frequency) or will drop a frame (never outputing it to compensate for a high input frequency). This buffer adjustment is referred to as a *controlled frame slip.*

The 193 + 138 = 331 bit-length requirement applies to frame buffers making controlled frame slips. The goal is to have frame slips occur only as a result of long term frequency offsets, not due to jitter (wander). However, only 138 bits are required in a jitter (hysteresis) buffer that does not perform frame slips. In this case, the FIFO depth requirements are defined by the buffer length necessary to tolerate the jitter (wander) without overflow/underflow. The exact length needed to meet the requirements of Figure 8 depends upon the jitter transfer function of the PLL (Figure 6). The PLL will track jitter at low frequencies, and requires a FIFO long enough to contain the maximum input jitter amplitude possible in the jitter attenuation range.

Output Jitter Generation: Output jitter generation is a measurement of how much jitter is output by the system when no jitter is input to the system (using a QRTS). The requirements are measured using band-pass filters to measure jitter at various frequencies, as shown below:

Filter applied	Maximum output jitter
None (Broadband)	0.05 UI peak-peak
10 Hz to 40 kHz	0.025 UI peak-peak
8 kHz to 40 kHz	0.025 UI peak-peak
10 Hz to 8 kHz	0.02 UI peak-peak

Jitter Transfer Function: Jitter transfer describes the ratio of input jitter and output jitter at a given jitter frequency using the following equation:

Transfer Jitter(dB) =
20 log (jitter output/jitter input)

The jitter input and output are measured in peak-to-peak UIs.

If a system contains a Stratum 4 clock, the jitter transfer function must meet the requirements of Figure 9. Figure 9 is irrelevant for systems with Stratum 2 or 3 clocks. Those clocks will attenuate jitter to the "output jitter generation" levels defined in the preceding section.

Since the system synchronizer has its basic frequency locked to the T1 rate of one particular line card, the attenuation test is at the NI associated with that particular line card. QRTS input jitter is applied at spot frequencies in the band 10 Hz to 40 kHz. The input jitter level is three-quarters of the system's jitter tolerance. Output jitter is measured using narrow frequency windows (1 Hz in 10-100 Hz range, 4 Hz in 100-1000 Hz range and 10 Hz above 1kHz). Jitter must be between the two bands, (a) and (b), shown in Figure 9. In the vicinity of 10 kHz, the output jitter level, after

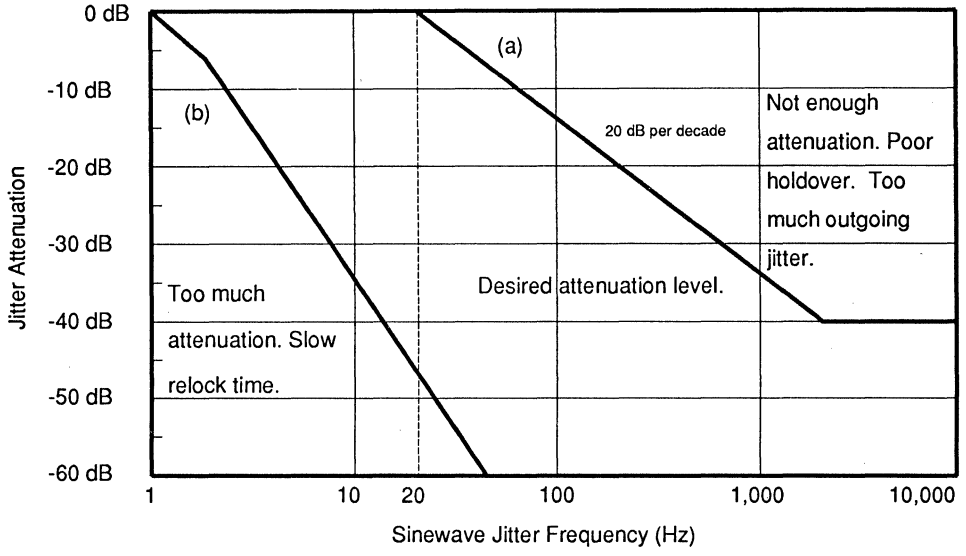


Figure 9 - 1990 AT&T 62411 Jitter Transfer Requirement

attenuation, must typically be in the range of 0.001 to 0.002 UIs (or 0.65 to 1.3 ns).

The curve (b) indicates an attenuation level which must not be exceeded. Too much attenuation can be harmful. The negative effects can include increasing the number of frame slips that occur in the central office, and increasing the time needed to reacquire lock after a loss of signal condition.

Jitter peaking is not allowed above 10 Hz. Peaking is defined as a higher amplitude of output jitter than input jitter (at any frequency, not just at the frequency under test). Peaking is especially undesirable at low frequencies which lie within the tracking range (and not the attenuation range) of downstream PLLs. Analog PLLs can easily have peaking at the "knee" of the jitter transfer curve (just before attenuation starts).

In digitally controlled PLLs, another phenomenon, jitter aliasing, can often be observed. With jitter aliasing, jitter which appears at one frequency is attenuated and shifted to another frequency. Jitter aliasing is especially undesirable when the frequency is shifted down to the tracking range of the downstream PLLs. The 1990 version of 62411 has added language to address aliasing, requiring that broadband jitter in the 10 Hz to 300 Hz range should be attenuated by -25 dB (measured using an 10 kHz to 40 kHz filter), and by -35 dB (measured using an 8 kHz to 40 kHz filter).

T1 TRUNK CARD DESIGN CONSIDERATIONS

A number of architectural choices face the trunk card designer. One is whether to integrate the CSU onto the trunk card. The application note, "T1 Long-Haul Physical Layer Interface", is recommended to designers of integrated CSU's.

Another design choice is whether to use a Line Interface IC that provides jitter attenuation. For Stratum 4 Type II systems that don't relay timing and utilize a 1.544 MHz backplane clock, the answer is simple. By using a CS61574,

CS61574A, or CS61575 on the trunk card, the Type II clock is provided on the trunk card by the line interface RCLK output, and no separate synchronizer card needs to be designed. If the Type II system has multiple T1 lines, then the line interface IC's may be connected as shown in Figure 10. In this configuration, the master 1.544 MHz system clock is provided by the top CS61574A or CS61575 in the figure. The system clock will normally be recovered from the T1 line connected to the top line interface until the line interface enters the Loss of Signal state. Upon Loss of Signal (175 ±75 zeros), the CS61574A and CS61575 will substitute ACLKI (if present) for the recovered clock at the input of the jitter attenuator. The jitter attenuator filters any phase hits resulting from the switch before the clock is output on RCLK. In this configuration the RCLK output of the top line interface will always remain locked to one of the T1 recovered clocks. Each line interface that experiences Loss of Signal will pass on the recovered clock from the line interface preceeding it in the chain. When the master experiences Loss of Signal, the line interface nearest the master that is not in the Loss of Signal State will provide the 1.544 MHz system clock. If all line interfaces experience Loss of Signal, the reference clock is used instead. This configuration is advantageous for multi-line loop timed applications because it provides a jitter-free 1.544 MHz line recovered timing reference (ideally traceable to Stratum 1) even if there is only one functioning T1 line reference available. This capability helps to maximize the system's ability to successfully maintain loop timing on as many T1 lines possible.

However, for three reasons, the configuration shown in Figure 10 is not appropriate for systems which transfer timing (i.e., Stratum 4 Type I or Stratum 2 or 3). First, the CS61574A and CS61575 switch to a secondary reference clock upon Loss of Signal and not upon the conditions outlined in 62411 (summarized previously in the "Synchronization of Digital Networks" section) for systems that transfer timing. Furthermore, the CS61574A and CS61575 may not meet the maximum time interval error (MTIE ≤1μs) and phase change slope (81 ns in any 1.326 ms) requirements which apply during rearrangements. Systems which transfer timing must utilize a system synchronizer and the control circuitry requried to judiciously switch between reference sources, and the synchronizer's 1.544 MHz PLL is responsible for insuring the MTIE and phase slope requirements are met. Finally, the configuration in Figure 10 does not necessarily enforce a well defined network synchronization plan. Such a plan is essential in a network throughout which timing is transferred. A synchronization plan defines an appropriate manner in which timing rearrangements may be made without creating network timing problems such as self-locked timing islands (refer back to Figure 2). The configuration in Figure 10 will not necessarily prevent the fallback to an inappropriate timing reference (eg., a line already loop timed to this node). Therefore, when using the configuration shown in Figure 10, it is important that there be a field-installable definition of how the chain is configured.

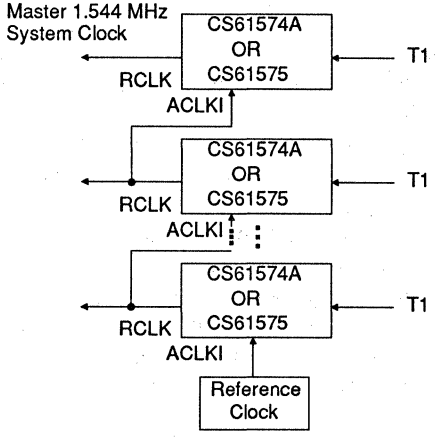


Figure 10 - Cross Coupling of Recovered Clocks (Stratum 4 Type II)

The use of a Line Interface IC with jitter attenuation also provides advantages for Stratum 4 Type I systems and Stratum 2 or 3 systems. By using a CS61574, CS61574A or CS61575 on the trunk card, the synchronizer becomes easier to design. Since the CS61574 exceeds jitter tolerance requirements and outputs an essentialy jitter-free recovered-clock, the synchronizer has reduced jitter tolerance requirements, and will see phase hits only when the switch is made between primary and secondary references. This frees the synchronizer designer to concentrate on meeting the holdover frequency, MTIE and reference switching criteria requirements.

SYSTEM CLOCK CARD DESIGN CONSIDERATIONS

As shown in Figure 7, the synchronizer provides the master clock for the system. It typically runs at a multiple of 8 kHz (the PCM frame rate), and generates a backplane clock at the rate of 2.048 MHz, 4.096 or 8.192 MHz.

A block diagram of a synchronizer is shown in Figure 11. This diagram shows multiple T1 lines being available as reference clocks for the synchronizer. A MUX is used to select one of the lines. The output of the MUX is fed through a CS61574 used only as jitter attenuator (accomplished by placing the CS61574 in local loop back mode). This jitter attenuation stage shields

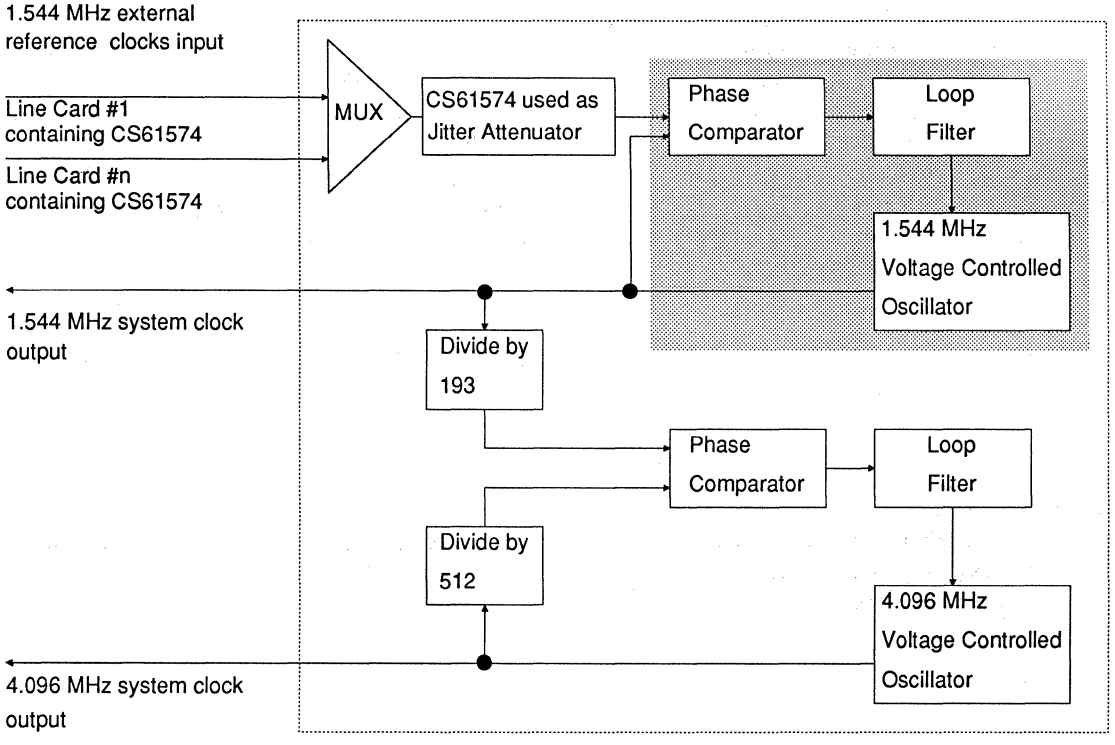


Figure 11 - Block Diagram of System Synchronizer

the 1.544 MHz Phase Locked Loop (PLL) from significant phase and frequency discontinuities which can result from either the loss of signal on the active reference clock input, or the switching of the MUX. The 1.544 MHz PLL provides a clean 1.544 MHz output clock for transmitting back toward the network. The system backplane clock is also locked to the 1.544 MHz clock using a second PLL. This system backplane clock does not need to meet 62411 jitter transfer specifications, since it is not used to clock data back to the network (Figure 7).

The system synchronizer clock card design is greatly simplified in systems which employ CS61574's, CS61574A's or CS61575's on the T1 trunk cards. In such a system, jitter performance requirements (jitter transfer, jitter tolerance and intrinsic jitter) are met by the line interface IC. The 1.544 MHz PLL does not need to be designed with the narrow closed loop bandwidth required for 62411 (i.e., jitter attenuation starting at 6 Hz). Wider closed loop bandwidth simplifies the design of the PLL and promotes stability. For example, VCO (Voltage Controlled Oscillator) phase noise is suppressed in a system which has wider closed loop bandwidth. The fact that VCO stability is improved by wider closed loop bandwidth (feedback) means that it is often possible to use a VCO instead of a more expensive VCXO (Voltage Controlled Crystal Oscillator) in the 1.544 MHz synchronizer PLL of a Stratum 4 (Type I) system. VCXO based designs offer excellent stability even in low bandwidth applications and are recommended for use in Stratum 3 systems. Although the synchronizer does not need to be the primary source of jitter attenuation in a system utilizing line interface IC's with jitter attenuation, the synchronizer PLL should not exhibit jitter peaking (jitter gain). It is easier to design a PLL which does not exhibit jitter peaking when a significant amount of jitter attenuation is not required.

Not only does the use of a CS61575 based trunk card design relax the jitter performance constraints imposed on the synchronizer's 1.544 MHz PLL, but it also eliminates the holdover (free-running) frequency accuracy requirement. Because the CS61574A and CS61575 will gracefully transition from the line recovered clock to a reference clock upon Loss of Signal, the 1.544 MHz PLL will always have an appropriate timing reference to stay phase locked to and will never need to free-run. The holdover frequency accuracy of the system will be that of the 1.544 MHz reference clock supplied to the line interface IC's.

With the other design constraints greatly relaxed, the PLL may be designed specifically to meet the dynamic performance required by 62411. To do this, the PLL must be designed with adequate damping to meet the Maximum Time Interval Error (MTIE) and phase change slope requirements discussed earlier.

There are several types of components from which the synchronizer PLL's may be constructed. Monolithic PLL IC's like the 74HC4046A offer excellent performance and minimal circuit board space requirements. For more information on PLL design using the 74HC4046A, refer to (2) - (4). The free design program (3) offered by Signetics is an excellent tool for evaluating and optimizing a 74HC4046A PLL Design.

Recommended References on PLL design are:

1. Gerdner, Floyd M: Phaselock Techniques, John Wiley & Sons, New York, 1979. (ISBN: 0-471-04294-3)

2. Volgers, B.: "Phase-Locked Loop Circuits: 74HC/HCT4046A & 74HC/HCTR7046A HCMOS Designer's Guide", Signetics/Phillips Components. (Ordering Code: 98-2908-350)

3. Signetics/Phillips Components: HCMOS Phase-Locked-Loop Design Program . (For IBM compatible computers)

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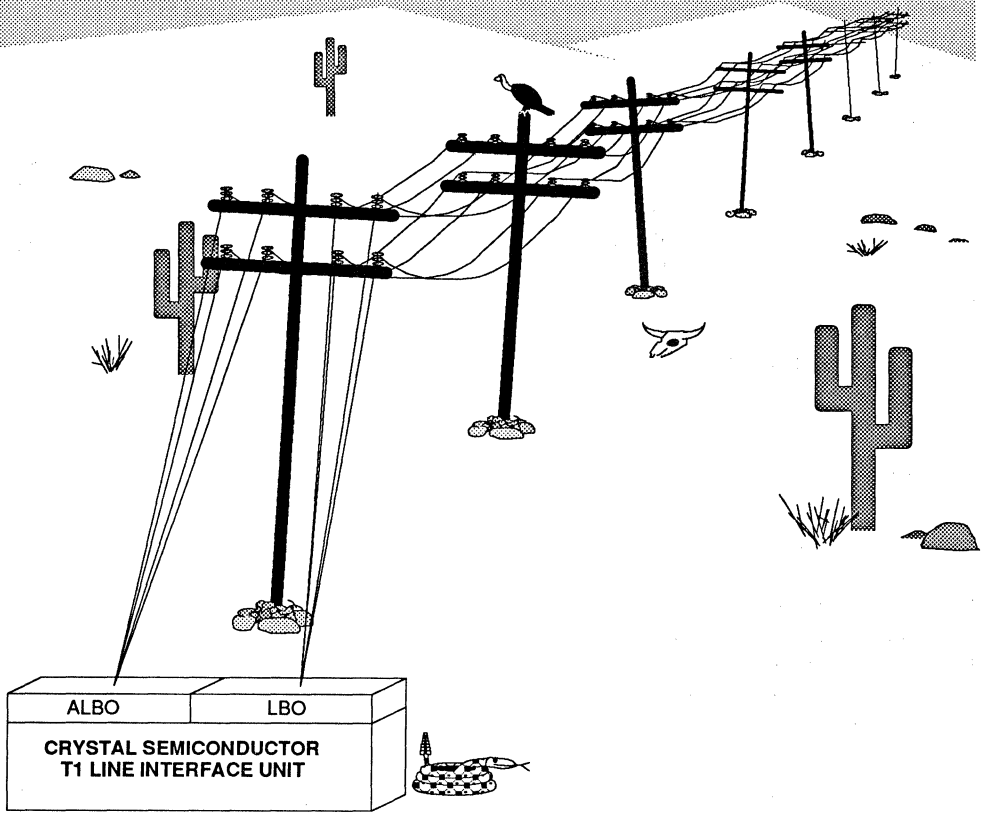
• Notes •

Application Note

T1 Long-Haul Physical Layer Interface

by

Greg Stearman
Roger Taylor



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INTRODUCTION

This application note describes how the T1 line interface IC's offered by Crystal Semiconductor may be used with the receiver gain and equalization network from a repeater IC, and a discrete transmitter pulse shaping network, to implement a complete physical layer long-haul T1 line interface. This design is intended to comply with FCC Part 68 and AT&T 62411 requirements. Generally, the CS61574, CS61574A and CS61575 are best suited for this application because receive side jitter attenuation is provided. The circuits described herein can also be directly applied to the CS61534, CS61535, CS61544, CS6158 and CS6158A (all but the CS61544 are pin compatible but offer different architectures and performance).

The combination of a CS61574, CS61574A, or CS61575 line interface IC and a repeater IC front-end provides increased functionality and performance over that available with traditional repeater only designs. The CS61574, CS61574A, and CS61575 internally provide jitter attenuation of the recovered clock, local and remote loop-backs, loss of signal detection, reference clock fall back, and host processor configuration and supervision. These functions must be implemented in discrete circuitry in a repeater only design at additional cost. Furthermore, the CS61574, CS61574A, and CS61575 provide clock recovery which *eliminates the need for the repeater's LC tank.*

Most T1 applications may be classified in one of two general categories: short distance or intraoffice DSX-1 applications, and long distance applications. Crystal Semiconductor's CMOS line interface products offer complete solutions for all types of intraoffice T1 applications. The addition of receiver gain and equaslization, and transmitter output pulse shaping allows these line inter faces to be used for applications such as office reqeaters and Channel Service Units (CSU's), which are used to connect Customer Premises Equipment (CPE) to a telephone company network.

The circuits described in this application note may be used in the implementation of a stand-alone CSU, or may be used to eliminate a stand-alone CSU by integrating the long-houl physical layer interface onto each T1 line card in the CPE. An integrated CSU approach is attractive because it eliminates duplication of transmitting, receiving, framing and monitoring fuctions in the CSU and terminal equipment, thereby reducing system cost and complexity.

Long-haul applications are characterized by the use of line repeaters to regenerate and retime the signal at intermediate points along its transmission path. The distance between line repeaters in long-haul applications may be several times the transmission distances covered in intraoffice applications. Because of the longer transmission distances, long-haul receivers must provide both gain and equalization to the incoming signal to compensate for the significant attenuation and low-pass characteristic of the transmission line. This gain and equalization is referred to as Automatic Line Build Out, ALBO.

On the other hand, intraoffice applications do not need receiver equalization or as much receiver sensitivity as long-haul applications. Intraoffice applications use transmitter pre-equalization to compensate for a specific amount of cable attenuation in order to ensure that a robust pulse arrives at the receiver.

Long-haul line interfaces also require transmitter pre-equalization, referred to as Line Build Out, LBO. The LBO network provides simulated cable attenuation in applications where the transmission distance to the first line repeater in the network is relatively short. This attenuation prevents the repeater's receiver, which is optimized for receiving signals attenuated by maximum calbe length, from being overdriven by a large amplitude signal.

RECEIVER INTERFACE

The receivers in Crystal's T1 line interface ICs all offer excellent sensitivity, typically 15 dB below the DSX level. This receiver sensitivity far exceeds that required for DSX-1 applications, but it is still less than that typically required for many long-haul applications. For applications which require additional sensitivity, an automatic gain and equalization, or ALBO, stage can be used as a front-end for the line interface receiver to provide the increased sensitivity.

The external ALBO network may be easily realized by using the ALBO circuit found in a conventional repeater IC. Such circuits typically contain one or two ALBO diodes which are used to form an adaptive attenuation network in front of a high gain preamplifier. The preamplifier is designed to provide both the gain and equalization required to compensate for the maximum amount of cable attenuation anticipated.

Since a long-haul receiver must also be able to recover high amplitude signals transmitted over shorter distances additional attenuation is required for these signals before they are amplified by the preamplifier equalization stage. The ALBO diode attenuation network provides the correct amount of additional attenuation required to prevent overdriving the preamplifier stage by acting as an Automatic Gain Control (AGC).

Because the preamplifier input signal is maintained at a constant amplitude the preamplifier's differential outputs are also a constant amplitude representation of the equalized input signal and may be directly ac-coupled into the RTIP and RRING receiver input pins of the Crystal T1 line interface IC. When used in this way, the repeater serves only as an analog gain and equalization stage and performs no clock or data recovery. Instead, these functions are performed by the clock and data recovery circuits in the Crystal T1 line interface IC, and the tunable LC tank circuit, normally used with the repeater, is eliminated. The clock and data recovery circuits of the CS61574, CS61574A, and CS61575 exceed the most demanding 62411 jitter tolerance requirements.

Eliminating the repeater's LC tank is of great benefit. LC tank clock recovery circuits require manual tuning (a production nightmare) and will drift out-of-tune in response to aging and/or mechanical stress. LC tanks are also prone to producing data dependent jitter, a problem shared with most clock recovery architectures.

CPE designs using repeater LC tank clock recovery require an external system synchronizer which is capable of jitter attenuation for 62411 compliance. The CS61574, CS61574A and CS61575 feature a receiver jitter attenuator which meets the requirements defined in AT&T 62411 (1990 version), so that the recovered clock of these ICs may be used directly as a Stratum 4 Type II jitter-free system timing reference. Compliance with AT&T 62411 is a neccessary requirement for Customer Premises Equipment which is connected to T1 lines provided by AT&T.

Two receiver ALBO applications circuits for use with the Crystal T1 line interface ICs are presented here. Both applications circuits were built and tested using the CS61574. The first is based upon the PMI LIU-01 repeater IC and discrete components. The second is based upon the Exar XR-C277 (PMI RPT-82) and the Exar TM-044H hybrid. Both circuits were adapted from the manufacturer's recommended applications circuits for T1 operation using #22 A.W.G. unshielded twisted pair cable. In both circuits, many of the external repeater support components unnecessary for this application, including the LC tank, are removed. Similar networks may be designed for CEPT applications or T1 applications which use other types of cable.

LIU-01 ALBO APPLICATIONS CIRCUIT

The ALBO network realized using the PMI LIU-01 is shown in Figure 1. This network does require several external components but offers excellent receiver sensitivity. The use of surface mount components and careful board layout minimizes the board space requirements of this network. The PMI LIU-01 features dual ALBO diodes which give it the dynamic range required to recover full amplitude input signals, as well as those attenuated by up to 38 dB of cable loss. Repeaters utilizing only one ALBO diode (like the XR-C277 used in the next applications circuit) have less dynamic range and have difficulty recovering full amplitude input signals. The preamplifier outputs of the LIU-01 are ac-coupled to the CS61574 RTIP and RRING receiver input pins using a 0.01µF capacitor and a 10kΩ resistor to ground.

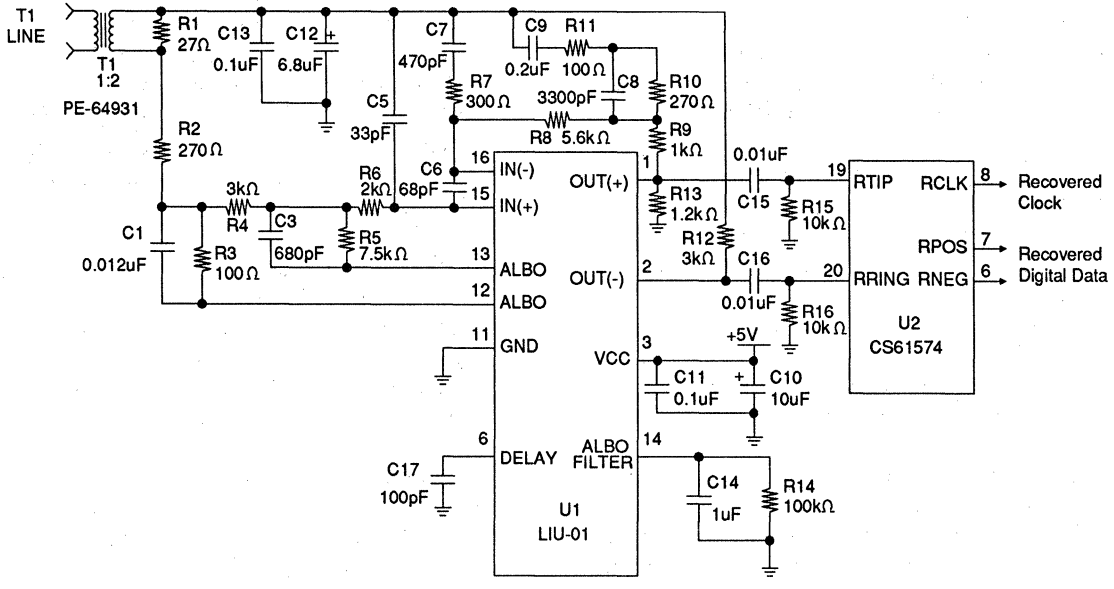

Figure 1. CS61574 and ALBO Network Using PMI's LIU-01 Repeater

XR-C277 ALBO APPLICATIONS CIRCUIT

The network based upon the Exar XR-C277 (or PMI RPT-82) and the EXAR TM-044H hybrid module is shown below in Figure 2. This network uses a diode to generate the two supply voltages required by the XR-C277 from a single +5 Volt supply. The preamplifier outputs of the XR-C277 are ac-coupled to the CS61574 RTIP and RRING receiver input pins using a 0.01 µF capacitor and a 10 kΩ resistor to ground. Most of the passive components required to realize the ALBO network have been consolidated into the hybrid module easing board space and layout requirements. This network has good sensitivity and recovered signals after as much as 34 dB of cable loss. However, it had difficulty recovering full amplitude pulses (those attenuated by less than about 5 dB) because it employs only one ALBO diode.

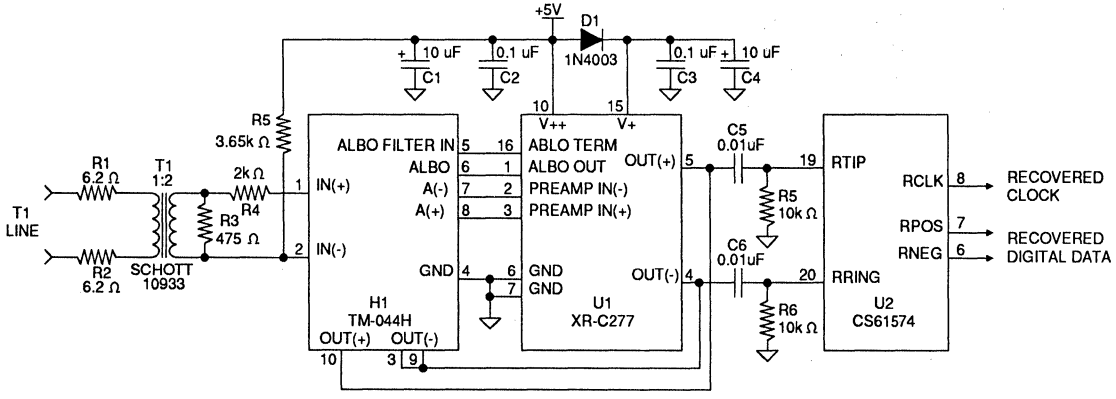

Figure 2. CS61574 and ALBO Network Using Exar's XR-C277 and TM-044H Hybrid

Figure 3 shows the XR-C277 ALBO input and output waveforms. The upper trace in the oscilloscope photograph is the ALBO input signal measured differentially across the points labeled "T1 LINE." The input signal has been attenuated by approximately 20 dB of cable loss. The middle trace is the ALBO output signal measured with respect to ground at the RRING pin of the CS61574. The lower trace is the ALBO output signal measured with respect to ground at the RTIP pin of the CS61574.

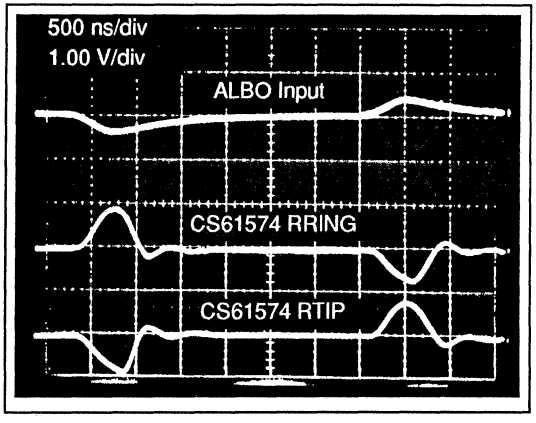

Figure 3. ALBO Input and Output Waveforms

TRANSMITTER INTERFACE

On the transmit side, a Line Build Out (LBO) stage is required between the Crystal line interface and the transformer to realize the -7.5 dB and -15 dB output pulse options required for the network interface by FCC Part 68. All of the line interface ICs already produce the 0 dB output pulse specified by Part 68. This LBO network provides 0 dB, 7.5 dB, or 15 dB of switch selectable attenuation at 772 kHz in the transmit path. The network is placed in the transmit path between the line interface and the transformer so that it is protected by the transformer and any additional line protection circuitry in the secondary. The required attenuation characteristic is specified in FCC Part 68 by a transfer function. Each of the two identical LBO sections in the network presented in Figure 4 below implements a two-pole approximation of this transfer function.

The LBO is a matched network designed to provide the 25Ω equivalent load expected by the CS61534, CS61535, CS61574 and CS6158 output drivers when the 25Ω equivalent line load is placed across the LBO output. For Option B (-7.5 dB) output pulses one of two identical attenuation networks is switched into the transmit path. For Option C (-15 dB) output pulses both networks are placed in series in the transmit path. Contact the factory for the changes required to adapt the LBO in Figure 4 for use with the transmitter drivers in the CS6152, CS61535A, CS61574A, CS61575, CS6158A and CS6159.

The network in Figure 4 was tested for FCC Part 68 compliance in two ways. First, the output pulses were measured against the pulse templates derived from Part 68 using a CS61574. Figure 5 shows the CS61574's 0 dB output pulse (selected with LEN2/1/0 = 010) overlaid with the Option A template. Figures 6 and 7 show the -7.5 dB and -15 dB output pulses respectively, overlaid with the appropriate output templates. Careful board layout is required to meet the Option C template as shown in Figure 6.

Finally, attenuation measurements were made on an all ones pattern at 772 kHz using a spectrum analyzer. Figure 8 shows the attenuation of the LBO network's Option B output (with respect to the 0 dB Option A pulse) which was measured to be -7.3 dB at 772 kHz. Similarly, the attenuation of the LBO network's Option C output (with respect to the 0 dB Option A pulse) was measured to be -15.0 dB at 772 kHz.

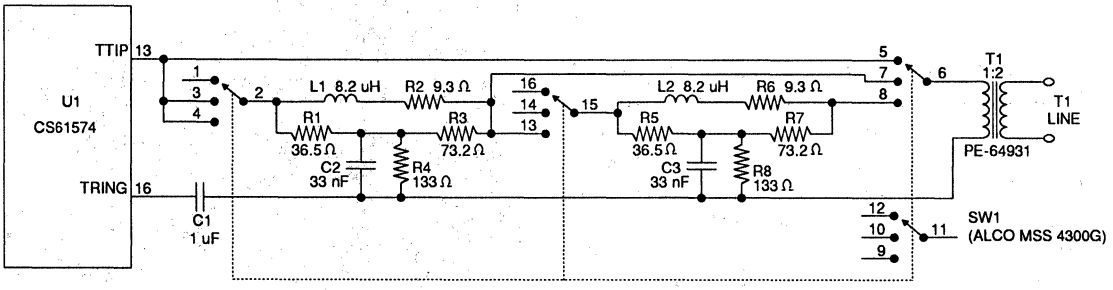

Figure 4. CS61574 LBO Network Used to Generate 0dB, -7.5dB, and -15dB Output Options

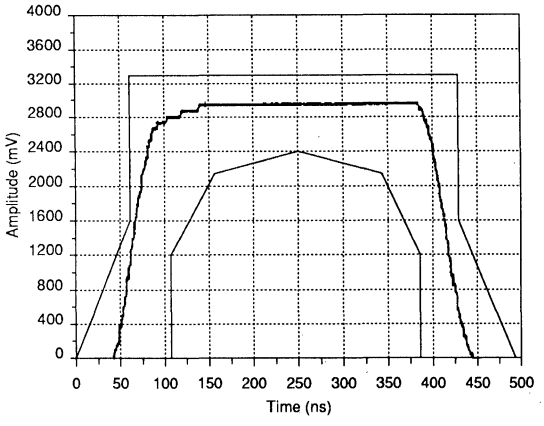

Figure 5. LBO FCC Part 68 Option A Pulse

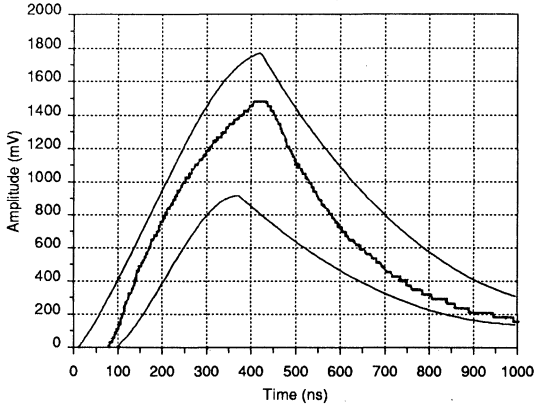

Figure 6. LBO FCC Part 68 Option B Pulse

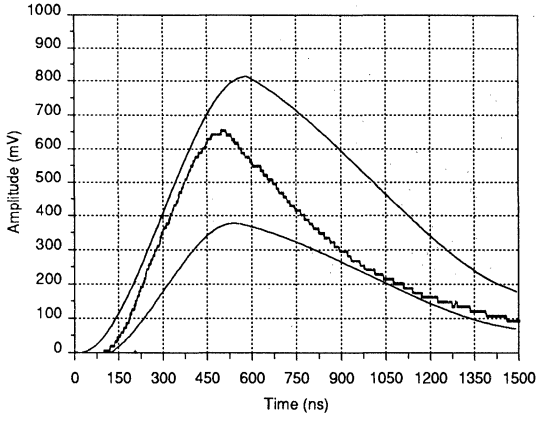

Figure 7. LBO FCC Part 68 Option C Pulse

REFERENCES

1. "LIU-01 Serial Data Receiver" (Data Sheet), Precision Monolithics, Inc.

2. Mike Jachowski: "Improved T1 PCM Receiver for #22 AWG Unshielded Twisted-Pair Wire", AN118, Precision Monolithics, Inc.

3. "XR-C277 Low-Voltage PCM Repeater" (Data Sheet), Exar Corporation.

4. "TM-044H T1 Repeater Equalization Hybrid Module" (Data Sheet), Exar Corporation.

5. "Part 68- Connection of Terminal Equipment to the Telephone Network", U.S. Federal Communications Commission, OCT. 1985.

6. "Accunet T1.5 Service Description and Interface Specifications", TR 62411, AT&T, DEC. 1988.

7. Jeremy Parsons: "Are You Using the Right Stress Patterns?", Telephony Magazine, pp. 150-158, 16 April 1990.

8. M. Kursat Kimyacioglu: "Implement Bell T1C PCM Repeater Using Just Two ICs", EDN Magazine, pp. 195-200 , 21 March 1985.

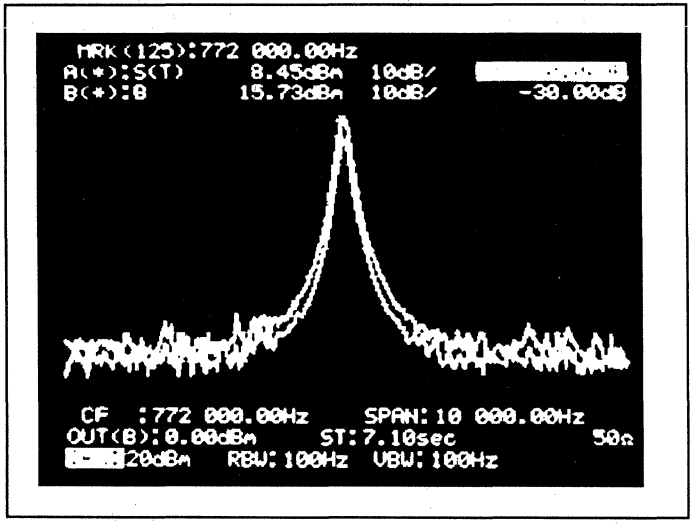

Figure 8. LBO FCC Part 68 Option B (-7.5dB) Attenuation at 772 kHz

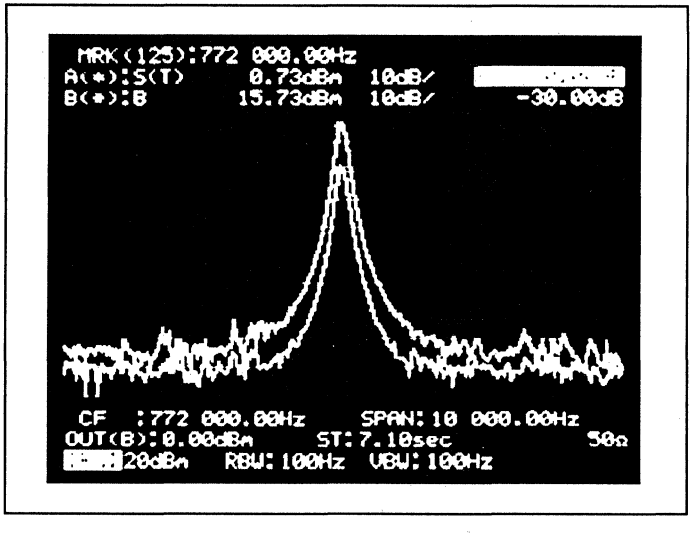

Figure 9. LBO FCC Part 68 Option C (-15dB) Attenuation at 772 kHz

CONTENTS

DEFINITION OF PRELIMINARY PART TYPES

Before a part is in full production, Crystal will supply preliminary parts. There are two varieties:

I.Engineering Sample (ES)

Engineering sample "ES" is a product which has not been completely characterized or where qualification has not reached the first lot 500 hours read point. ES product will be assembled per manufacturing specs at qualified assembly sites. All units will be tested to a published data sheet and applicable errata sheet (if needed). Any ES units which are tested only at room temperature will receive a supplemental brand "25°". As soon as automated temperature testing is available for this device, all subsequent ES units will be 100% temperature tested.

The following premium - temperature product grades will always be 100% tested at temperature:

TELECOMMUNICATIONS - "M" grade
DATA ACQUISITION - "A", "B", "C", "S", "T", and "U" grades

II. Engineering Prototype (EP)

Engineering Prototype is an engineering prototype of a device which works sufficiently for beta site purposes.

DEFINITION OF DATA SHEET TYPES

Each product developed by Crystal will be supported by technical literature where the data sheets progress through the following levels of refinement:

I. Product Preview

This is a 1-to-4 page document which describes the main features and specifications for a product that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

II. Preliminary Product Information

This is the first document completely describing a new product. It contains an overview, specifications, timing diagrams, theory of operation, pin-out diagram, applications information, ordering guide and mechanical information. The numbers in this data sheet are based on prototype silicon performance and on worst-case simulation models. The specifications represent the designer's best estimate for the "real" numbers. Min and max values are included where possible. The purpose of this document is to provide system designers with technical information sufficiently detailed to guarantee that they can safely begin active development.

III. Final Data Sheet

This is an updated version of the preliminary data sheet reflecting actual production performance of the final product. Updates include tighter specifications, more min and max values, and any application information that has arisen during the early life of the part. The purpose of this document is to communicate the confirmed performance of products which have passed qualification, been fully characterized, and are in production.

PRODUCT HANDLING IDENTIFIER INDEX
ASSEMBLY PROCESSING IDENTIFIERS

HANDLING IDENTIFER	PRODUCT FLOW-TITLE DOCUMENT NUMBER	SPECIAL PROCESSING COMMENTS
A	Commercial Hi-Rel	160 hours burn-in @ 125 °C

RADIATION RESISTANCE PERFORMANCE

Crystal products are manufactured using 2 and 3 micron CMOS processes. While not able to withstand large doses of radiation, our products are suitable for operation in low to medium dose applications. Indeed, the self calibrating architecture of many of the A/D Converters is able to compensate for the effects of radiation.

Crystal will assist customers to test parts for radiation resistance by supplying free, data-logged parts. In exchange, we would like the parts returned to us, so that we can measure their post-radiation performance. In addition, we would like a copy of any report that is generated, along with permission to publish the report for other customer's information.

Several customer's have already undertaken radiation testing of our A/D Converters. Please contact the factory for the latest information and copies of the radiation performance reports.

RELIABILITY METHODS

I. CONCEPT OF RELIABILITY

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in a more quantitative sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can best be summarized by the reliability life or "bathtub" curve (Figure 1). The reliability performance is characterized by three phases: infant mortality, useful life, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period is aptly named wearout. Using proper design guidelines and device applications, this period is shifted well beyond the lifetime required by the user.

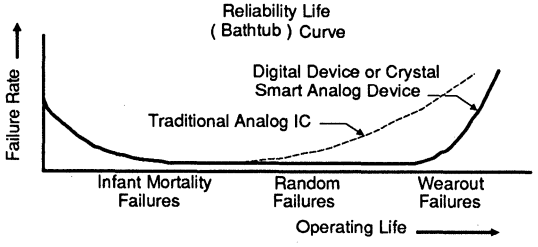

Figure 1.

An item of great importance in evaluating reported reliability characteristics is the definition of a failure. Crystal's definition of a failure is any device that fails to meet ANY data sheet parameter. Crystal's digital self-calibration techniques provide stable performance over temperature and life. Traditional Analog IC's and hybrids exhibit wearout mechanisms very early in the life of the product. One competitor's analog-to- digital converter's linearity error stability is specified at +/- .00075 % per 1000 hours at 25 °C. Stability degradation at 70 °C is unspecified and is likely to be accelerated greatly as temperature increases. The dashed line of Figure 1 is typical of the wearout seen in a competitor's Analog IC or hybrid. As you can see, wearout begins much earlier than a digital device or a mixed analog and digital chip utilizing Crystal's SMART analog design architecture and CMOS wafer technology.

II. CRYSTAL SEMICONDUCTOR RELIABILITY STRESSING

These stresses are done on every new product, assembly house or fabrication subcontractor. The Crystal acceptance criteria and goals are as described in Table 1 of the Quality and Reliability information in section 1 of this data book.

Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate thermally-activated failure mechanisms through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level to further stress the oxides of the device. All devices used in life stress are sampled directly from the production flow with no special processing or pre-screening. Stressing is performed per MIL STD 883, method 1015, condition D (dynamic signals). These dynamic conditions simulate as much as possible actual operating conditions in an application.

Both infant mortality operating life stress (168 hrs at 125 °C) and long term operating life (typically 1000 hrs at 125 °C) are reported . Infant mortality life simulates approximately 6-8 months in the field at 70 °C and is reported as %/168 hrs. Long term life simulates the total failure seen in the field and is expressed in FITS (failures in time). 1 FIT = 1 failure per billion device-hours. Derating of long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60 % upper confidence limit (UCL) and .7 electron volts (eV) activation energy are used in this calculation.

85 °C/85% R.H.

85 °C/ 85% R.H. is an environmental stress performed at a temperature of 85 °C and at a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal-voltage static bias is applied, with minimum power consumption, to the device, to accelerate the electrolytic corrosion of the metallization. Failures are expressed in % /time with 168, 500, and 1000 hour cumulative results reported.

Autoclave

Autoclave is also an environmental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are 121 °C, 100% relative humidity, and 1 atmosphere of pressure (15 psig), with no bias applied to the circuit. Corrosion of the die is the expected failure mechanism. Stressing is usually performed for 144 hours. Failures are expressed in %/time with 48, 96, and 144 hour results reported.

Temperature Cycling

Temperature cycling typically accelerates the effects of the thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010, Condition C (-65 °C to +150 °C). Stressing is done in an air environment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in %/cycles, with 100, 500, and 1000 cycle results reported.

Thermal Shock

The objective of thermal shock is basically the same as that of temperature cycling - to exercise the difference in thermal expansion coefficients within the integrated circuit package and die. Thermal shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, method 1011, Condition B (-55 °C to +125 °C). In one cycle of thermal shock, devices are placed in a flourocarbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with flourocarbon at 125 °C for five minutes. Stressing is performed for 500 cycles. Failures are expressed in %/cycles, with results reported at 100, 200, and 500 cycles.

High Temperature Storage Life

Storage life is an environmental stress where temperature is the only stress. Stressing is performed per MIL STD 883, method 1008, Condition C. (150 °C). Stressing is performed to 1000 hours. Failures are expressed in %/hours, with results reported at 168, 500, and 1000 hours.

Electrostatic Discharge

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883 method 3015, which simulates the resistance (1500Ω) and capacitance (100 pF) of the human body. Also the machine model test is performed with a 0Ω resistance and a capacitance of

200 pF to simulate, as its name implies, a typical insertion tool, handler, etc. that comes in contact with the leads of a semiconductor device.

Latchup

Latchup testing is performed to ascertain whether a device can sustain SCR latchup due to a DC current input. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a positive and negative DC current forced into it. This test is performed per the standard test procedure recognized by JEDEC.

C dv/dt Latchup Testing

This test is performed to evaluate the susceptibility of a CMOS device's power pin to instantaneous ESD discharge into a power supply pin or a rapid ramp of a power pin during power up. Positive and negative pulses are supplied to the power supply pins with a change in voltage of greater than 500 V/µs and a 0 to 5 V risetime of less than 15 ns. Ground, V_{SS}, and the pin under test are connected to ground. The supply current is monitored for excessive current.

III. FAILURE RATE CALCULATIONS

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. Thermally accelerated failure rates can be derated to actual operating conditions by commonly accepted mathematical models.

Operating life stress is usually reported in the derated form. That is, operating life is performed at 125 °C and results are reported for an equivalent time at a typical operating stress temperature for an application, generally 25 °C, 55 °C, or 70 °C. Failure rates for other temperatures are calculated using a computed acceleration factor.

There are many probability models used in reliability analysis for calculating failure rates. The simplest form of calculating a failure rate (F.R.) would be to divide the number of failures observed after test (N) by the number of device-hours of stress.

$$\text{F.R.} = \frac{N}{D \cdot H} \qquad (1)$$

where D is the number of devices stressed and H is the number of stress hours. If this number is multiplied by 10^9 we obtain the failure rate expressed as Failure In Time (FIT). FITS are expressed as failures per billion device operating hours.

$$\text{FITS} = (\text{F.R.})(10^9) \qquad (2)$$

However, using equation (1) allows only for a failure rate calculation at the stress temperature. In order to apply the equation to the desired use temperature we use the well-known Arrhenius relationship to determine the thermal acceleration factor, F_a. One hour of device operation at temperature T_1 is equivalent to F_a hours of operation at temperature T_2. The activation energy, EA, is an important parameter in the Arrhenius equation and is discussed below. The Arrhenius equation is:

$$F_a(T_1 \rightarrow T_2) = e^{-\frac{EA}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \qquad (3)$$

where k = Boltzman's Constant (8.63×10^{-5} eV/°K) and T_1 is the accelerated stress junction temperature and T_2 is the desired use operating junction temperature in degrees Kelvin.

Junction temperatures, T_1 and T_2, should be used in determining acceleration factors. This temper-

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ture can be obtained from the equation below.

$$T_j = T_a + \theta_{ja} P_d \quad (4)$$

where T_a is the operating ambient temperature and θ_{ja} is the package thermal dissipation (°C/ W) and P_d is the device power dissipation.

Crystal utilizes a low power CMOS process which typically raises the junction temperature about 7 to 15 °C, whereas analog bipolar IC's and hybrids can have power dissipations in the 1 W range. These differences in device junction operating temperatures can greatly affect the acceleration factors. For example, let's calculate the acceleration factors of a device with a power dissipation of 1 watt packaged in a 40 pin ceramic package. This is equivalent to a junction temperature change from 160 °C to 60 °C and from Table 2 the acceleration factor is 277. A typical Crystal device junction temperature is 10 °C higher than the ambient which results in a junction temperature change from 135 °C to 35 °C. This results in an acceleration factor of 636, as shown in Table 2. By comparing the results in Table 2 one can see how derating to a lower use temperature or failing to consider junction temperature when calculating acceleration factors can result in greatly differing failure rates.

TEMPERATURE CHANGE	ACCELERATION FACTOR
125 --> 70 °C	26.3
125 --> 55 °C	77.5
125 --> 25 °C	933.0
135 --> 35 °C	636
160 --> 60 °C	277

TABLE 2
ACCELERATION FACTORS FOR DIFFERENT TEMPERATURES (E. A. = .7 eV)

E . A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

TABLE 3
ACCELERATED FACTORS FOR DIFFERENT ACTIVATION ENERGIES (125 ° C --> 70° C)

Table 3 compares acceleration factors for different activation energies. Using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal uses an activation energy of .7 eV, a conservative value, compared to the .8 eV to 1.0 eV used by other analog IC vendors.

We now take the failure rate equation (1) at accelerated temperatures expressed in FITS and factor in the acceleration factors from the Arrhenius relationships considering junction temperatures and arrive at the equation below.

$$FITS = \frac{10^9 N}{DHF_a} \quad (5)$$

Using composite Crystal data through the 1st quarter of 1988, a failure rate at 25°C can be calculated by substituting in equation (5) above:

N = 23
D•H = 5,371,036
Fa = 702 (Assuming .7 eV and stress temperature of 125°C, using junction temperature derating)

D•H is the summation of the devices stressed at each readpoint multipled by that number of stress hours.

Substituting we get:

$$FITS\ 25°C = \frac{(10^9)(23)}{(5{,}371{,}036)(702)} = 6.1$$

The Weibull distribution is often used for product life predictions because it can describe increasing and decreasing failure rates. Also the Weibull dis-

tribution has both a shape parameter, β, and a scaling parameter, α. This is very useful in accurately describing the shape and scaling of the "bathtub" curve. These more accurate descriptions of the failure rate of the Weibull distribution make this method superior to the uniform failure distribution described in Equation (1). The Weibull probability distribution function (PDF) f(t) is the probability of failure between time t and t + dt.

$$f(t) = \frac{\beta}{\alpha} t^{(\beta-1)} e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (6)$$

The Weibull PDF can also be expressed as a function of the Reliability function, R(t), and the instantaneous failure rate function, h(t), therefore:

$$f(t) = h(t)R(t) \qquad (7)$$

The Reliability function is found by integrating the Weibull PDF from t to ∞. This function is the probability that a device will survive to time t.

$$R(t) = \int_{t}^{\infty} f(t')dt' = e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (8)$$

The instantaneous failure rate function is the probability that a device will fail between time t and t+dt:

$$h(t) = -\frac{1}{R}\frac{dR}{dt} = \frac{\beta}{\alpha} t^{(\beta-1)} \qquad (9)$$

The Reliability function is used to calculate the shape parameter, β, and the time scale parameter, α. The shape parameter is the key function in shaping the infant mortality portion of the "bathtub" curve. A β of 1 indicates a uniform failure rate, β > 1 indicates wearout and β < 1 indicates a declining failure rate. To use Weibull statistics, failures that occur during operating life stresses are used to produce values of R(t). Failure times and R(t) values can be combined to estimate α and β. We first take the natural logarithm of both sides of equation (8).

$$\ln\left(\frac{1}{R(t)}\right) = \frac{t^{\beta}}{\alpha}$$

We again take the natural logarithm and obtain:

$$\ln\left[\ln\frac{1}{R(t)}\right] = \beta \ln(t) - \ln(\alpha) \qquad (10)$$

This last equation is now in the form of a linear function. Using linear regression techniques or Weibull plotting paper we obtain the Weibull shape and scale parameter. Most semiconductor manufacturers perform a burn-in screening on devices to insure that the end customer receives a population of devices that have minimal infant mortality and are from the useful life period of the reliability "bathtub" curve. It is very important to include this data for the entire lifetime of the device to obtain an accurate curve fit for obtaining α and β.

Once the parameters α and β for the Weibull distribution are known we utilize R(t) to calculate FITS. Crystal uses a 20 year lifetime in its FIT calculations and typically uses a 48 hour burn-in at 125 °C hence:

t_{20} = 20 yrs = 175,200 hours
t_1 = 48 hours

The number of devices that will fail in the twenty year lifetime following burn-in is given by:

$$N = D\,[R(t_1) - R(t_1 + t_{20})] \qquad (11)$$

where D is the total number of devices stressed. The number of device-hours accumulated in 20 years can be estimated by counting the devices surviving after 20 years.

$$DH \geq D \cdot R(t_1+t_{20}) \cdot t_{20} \qquad (12)$$

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Using equation (2) for expressed failures in FITS we obtain the equation below for a Weibull distribution

$$FITS \leq 10^9 \frac{D\,[\,R(t_1) - R(t_1 + t_{20})]}{D \bullet R(t_1 + t_{20}) \bullet (t_{20})}$$

$$= \frac{10^9\,[\,R(t_1) - R\,(t_1+t_{20})]}{R(t_1+\,t_{20}) \bullet (t_{20})} \qquad (13)$$

The above equation applies only at the stress temperature. In order to apply the equation to the desired use temperature we factor in the acceleration factors, F_a, from the Arrhenius relationship as it relates to time in the reliability function. Therefore in equation (12) above we replace $R(t_1 + t_{20})$ by $R(t_1 + t_{20}/Fa)$. Note that the device lifetime t_{20} is still 20 years but the reliability function must have the acceleration factor considered for derating to use temperature. Using composite Crystal data through the first quarter of 1988, and using from equation (10), $\beta = .19$ and $\alpha = 521$ and $Fa = 702$ yields a failure rate at 25 °C of 9.7 FITS.

This failure rate is a more accurate measure of Crystal reliability than that provided by the constant failure rate model of equation (5).

Reliability evaluations involve only samples of an entire population of devices. Therefore a confidence level, (CL), should be placed on the average failure rate. At any time a sample is stressed from a population there exists a finite chance of failures. If many separate samples were stressed from the same population and failure rates plotted, a normal distribution of failure rates would occur. Therefore, valid statistical methods for a normal distribution should be used to determine the desired CL. Confidence levels for reliability analysis are expressed in upper confidence levels (UCL), typically at 60% or 90% depending on the criticality of the device's application. The total sample size stressed is critical in defining the UCL. Therefore rather large sample sizes must be stressed to more accurately demonstrate the true failure rate. A larger spread will exist between the 50% and 90% UCL distribution for smaller sample sizes due to the greater probability that the sample stressed was not representative of the entire population.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85 °C/85%R.H., usually have their actual results reported, due to the lack of widely recognized derating models. These are usually expressed as %failure / stress time. An example of this would be a temperature cycling failure rate expressed as %/ 1000 cycles. These failure rates should have a confidence level associated with the data given. For environmental stresses, Crystal publishes data with a 90% confidence level. To calculate this failure rate with confidence levels, the following binomial probability statistics calculations are made:

$$P_c = P_a + Z\frac{[P_a\,(100 - P_a)]^{1/2}}{n} \qquad (14)$$

where P_c is the failure rate with confidence level, P_a is the observed failure rate in percentage defective, n is the number of samples stressed, and Z is the value of the standard normal probability distribution associated with the desired confidence level. (Z = 1.28 for 90% UCL.) This calculation agrees with the widely accepted lot tolerance percent defective, LTPD, plans that are based on 90 % upper confidence.

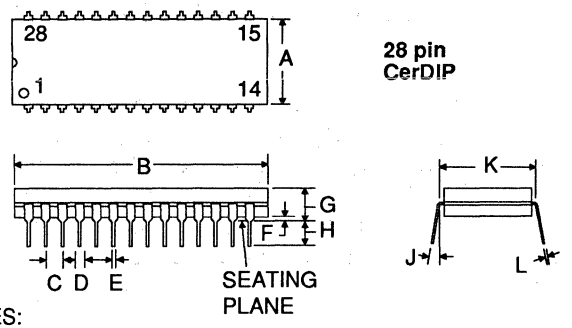
Of course it is not satisfactory to have accurate methods on reporting failure rates without having programs and methods in place to continuously improve the reliability of the product. Crystal uses methodologies in every level of the company to provide the highest possible quality and reliability standards of its products.

Using the reliability calculation methods of Maxim, an analog IC quality leader, Crystal achieves a failure in time (FIT) rate of 6.1 parts per billion operating hours. This compares favorably with Maxim's own performance of 6.8 FITs. Crystal's reliability is also established for devices requiring far greater analog accuracy than its competitors' products.

In summary Crystal Semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability of its devices and has active programs in place to continuously improve the quality and reliability of its devices.

For further information on a summary of Crystal's methods of insuring high quality and reliability standards see the Quality and Reliability information in section 1 of this data book, or contact Crystal's Reliability and Quality Assurance Department at the factory.

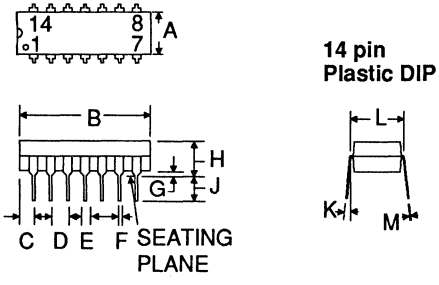
MECHANICAL DATA



28 pin
CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	36.45	37.85	1.435	1.490
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

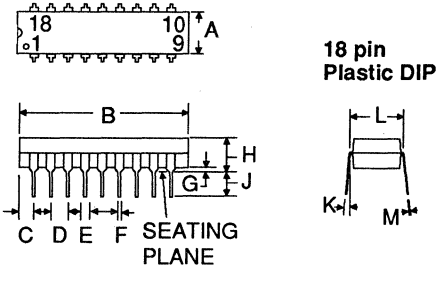
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



14 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.54	19.56	0.730	0.770
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

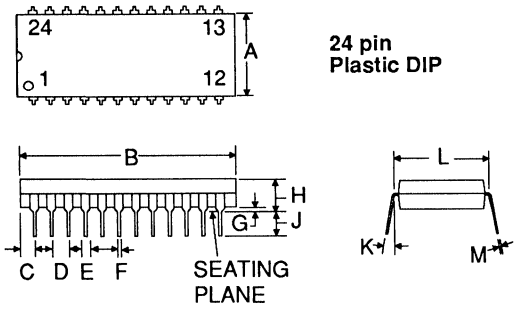
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



18 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	22.22	23.24	0.875	0.915
C	1.02	1.52	0.040	0.060
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

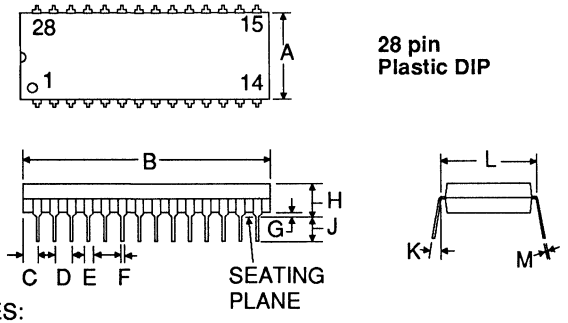
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin Plastic DIP

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	13.72	14.22	0.540	0.560
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin Plastic DIP

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
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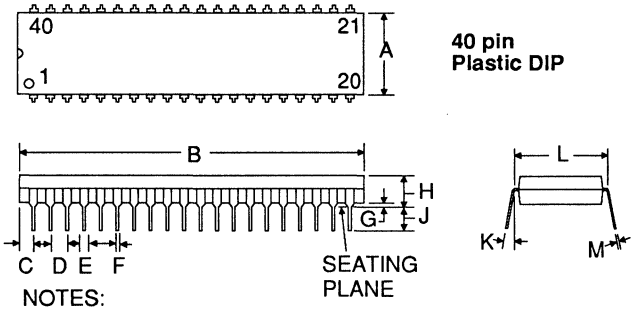
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



40 pin Plastic DIP

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	13.72	14.22	0.540	0.560
B	51.69	52.45	2.035	2.065
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
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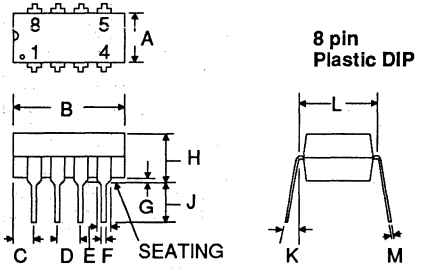


8 pin Plastic DIP

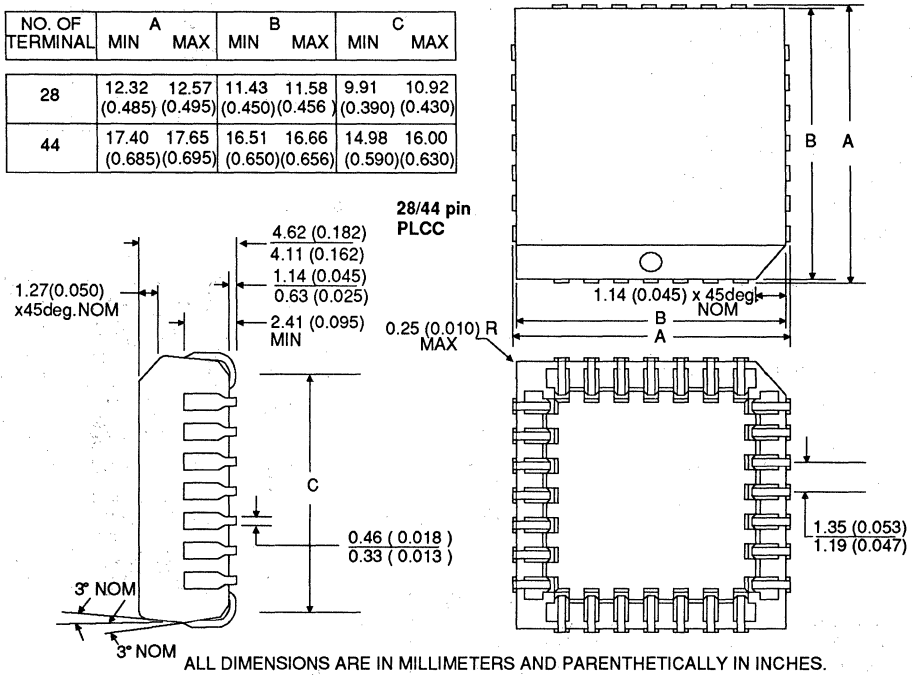
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)

28/44 pin PLCC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

CONTENTS

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