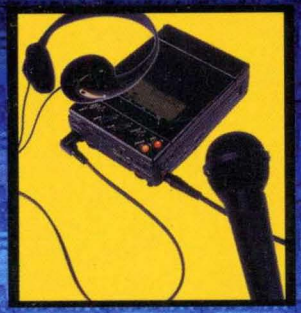
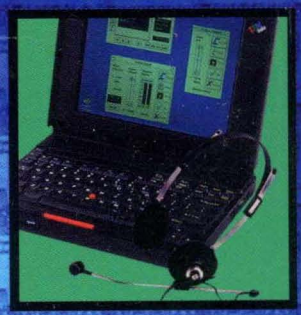
1994 CRYSTAL SEMICONDUCTOR AUDIO DATABOOK

CRYSTAL SEMICONDUCTOR
AUDIO DATABOOK

CRYSTAL





CRYSTAL

MODEL INDEX

Crystal Semiconductor Corporation

Digital Audio Products Data Book

January 1994

Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.A.:

4,709,225; 4,849,662; 4,804,863; 4,748,418; 4,746,899; 4,805,198; 4,851,841; 4,943,807; 4,939,516; 5,055,846; 4,918,454; 4,941,156; 4,988,954; 5,068,660; 5,079,550; 5,039,989; 5,012,244; 5,088,107; 5,087,914; 5,061,925; 5,111,451; 5,117,200; 5,121,080; 5,140,279; 5,150,386; 5,157,395; 5,172,115; 5,187,390; 5,196,850; 5,198,782; 5,208,597; 5,212,659; 5,220,483; 5,245,344; 5,247,210; 5,248,970; 5,257,026.

Germany:

3,642,070; 3,736,735; 3,737,279; 3,733,682; 3,933,552; 4,002,871; 4,127,096; 4,202,180.

Great Britain:

2,184,621; 2,198,306; 2,198,305; 2,195,848; 2,223,879; 2,232,547.

France:

2,591,753; 2,604,839; 2,606,565.

Japan:

1,684,670; 1,736,807; 1,747,991.

CONTENTS

COMPANY INFORMATION

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

CSLXXXX - TPNNH/R

DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.
REVISION IS COVERED IN DATE CODE STAMP.
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING ,ALPHA ONLY

A-COMMERCIAL HIGH-REL
B-MILITARY 883B REV. C PROCESSING

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2 NUMERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED ,ALPHA CHARACTER ONLY,NO NUMERICS

P = PLASTIC DIP	S= 0.3" SOIC
C = CERAMIC SIDEBRAZE	E= CERAMIC LCC
D = CERDIP	J= J-LEAD CERAMIC CHIP CARRIER
L = PLASTIC LEADED CHIP CARRIER,J LEAD	G= GULLWING CERAMIC CHIP CARRIER
U= UNPACKAGED DIE	Q= PLASTIC QUAD FLATPACK

TEMPERATURE SPECIFICATION - REQUIRED,ALPHA CHARACTER ONLY
SIGNAL CONDITIONING/COMMUNICATION:

C =	0 °C	to 70 °C
I =	-40 °C	to 85 °C
M =	-55 °C	to 125 °C

TEMPERATURE/ACCURACY - REQUIRED,ALPHA CHARACTER ONLY
DATA ACQUISITION:

TEMPERATURE	ACCURACY		
	GOOD	BETTER	BEST
0 °C to 70 °C	J	K	L
-40 °C to 85 °C	A	B	C
-55 °C to 125 °C	S	T	U

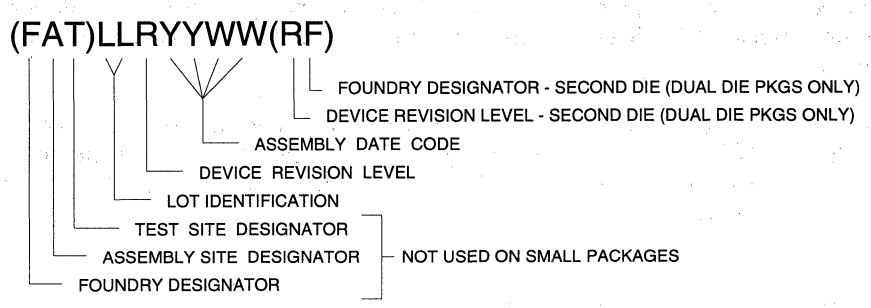
UP TO FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):
3 = DATA ACQ. SUPPORT CIRCUITS
42 = CODECS
43 = D/A CONVERTERS
5 = A/D CONVERTERS
6 = TELECOMMUNICATIONS
7 = SIGNAL CONDITIONING
8 = DATACOMMUNICATIONS

CRYSTAL SEMICONDUCTOR
"CS" = ALL CRYSTAL PRODUCTS;EXCEPT FOR
"CXT" = QUARTZ CRYSTALS
"CDB" = EVALUATION BOARD
"CX" = CUSTOM PRODUCTS

REV5

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



LOT CODE IDENTIFIER - TWO DIGIT ALPHA CHARACTER. IDENTIFIER SEQUENCE WILL BEGIN WITH AA,AB,AC, ETC. EACH LOT WILL RECEIVE A UNIQUE IDENTIFIER REGARDLESS OF DEVICE OR START DATE. SEQUENCE BEGINS AGAIN WITH AA WHEN ZZ HAS BEEN UTILIZED.

COMPANY BACKGROUND

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits. In 1991, Crystal became a wholly owned subsidiary of Cirrus Logic.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

QUALITY AND RELIABILITY INFORMATION

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This commitment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability are active concerns of each Crystal employee. Quality is ingrained in every operation throughout the product life cycle. Some of the key operations are discussed below.

In Product Definition

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

In Design

Conservative CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART Analog product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883C, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch current.

Crystal SMART Analog design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. On-chip digital error correction provides stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer error sources to consider. The result is a less complicated, more reliable system.

In Fabrication and Assembly

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations worldwide. Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and offshore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883C, Method 2010. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection to 3.0 percent LTPD is one of the standard production tests.)

In Test

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.

In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Qualification Criteria Table)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited every six months and routinely monitored. Any major design or process changes are re-qualified.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

In Customer Service

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass" (Crystal Online Marketing, Production, and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continuously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semi-annual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow, training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883C, METHOD 2010. Test die are electrically tested to verify compliance to key process parameters based upon design rule specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until disposition by a material review board. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

Qualification Criteria Table

	Method	Production Level III	Production Level II	World Class Level I	Units
Quality Performance					
Outgoing Quality (elec./vis-mech/ship.)	Crystal Spec.	2500	1500	500	DPM
Fault Coverage (Digital)		n/a	n/a	95%	%
Datasheet Test Coverage (Digital)	Datasheet	100%	100%	100%	%
Datasheet Test Coverage (Analog)	Datasheet	100%	100%	100%	%
ESD - Human Body Model	MIL 3015	1500	2000	4000	V
ESD - Machine Model	MIL3015	--	--	300	V
Latchup - Power Supply[1]	JEDEC 17	Vcc+1V	Vcc+50%	Vcc+50%	V
Latchup - I/O[1]	JEDEC 17	±50	±100	±200	mA
Reliability Performance					
Infant Mortality (48hrs@125°C or equiv.)[2]	MIL 1005	--	--	1000	DPM
Early Life (168hrs@125°C or 1yr. equiv.)[3]	MIL 1005	1/167[4]	500	300	FITS
Operating Life (1000hrs@125°C or 10yr, equiv.)[3]	MIL 1005	500	300	100	FITS
Moisture Performance					
Moisture Resistance - THB (plastic pkgs)	JEDEC 22B	500/5%	1k/5%	1k/3%	hrs/%LTPD per lot[5]
Autoclave (plastic pkgs)	JEDEC 22B	96/5%	144/5%	144/3%	hrs/%LTPD per lot[5]
Mechanical Performance					
Temp Cycle (plastic pkgs)	MIL 1010	500/5%	1k/5%	1k/3%	#cy/%LTPD per lot[5]
Thermal Shock (plastic pkgs)	MIL1011	200/5%	500/5%	1k/3%	#cy/%LTPD per lot[5]
Temp Cycle w/ Hermeticity (hermetic pkgs)	MIL1010/14	500/5%	1k/5%	1k/3%	#cy/%LTPD per lot[5]
Thermal Shock w/ Hermeticity (hermetic pkgs)	MIL 1011/14	200/5%	500/5%	1k/3%	#cy/%LTPD per lot[5]
Soak &VPR (surface mount plastic pkgs)	Crystal Spec.	3/5%	3/3%	3/1%	#cy/%LTPD per lot[5]
Xray	Crystal Spec.	2.50%	2.50%	0.65%	%AQL per lot[5]
Dimensions	MIL 2016	2.50%	2.50%	0.65%	%AQL per lot[5]
Solderability	MIL 2003	2.50%	2.50%	0.65%	%AQL per lot[5]
Lead Integrity & Lead Pull	MIL 2004	2.50%	2.50%	0.65%	%AQL per lot[5]
Mark Permanency	MIL2015	2.50%	2.50%	0.65%	%AQL per lot[5]
Product Integrity					
Design Rule and LVS Checks	Crystal Spec.	yes	yes	yes	
Design for Reliability & Packaging	Crystal Spec.	yes	yes	yes	
Product Characterization	Crystal Spec.	limited	full	statistical	
Test guardbands	Crystal Spec.	some	100%	100%	
Construction Analysis					
Wafer cross section & topo	Crystal Spec.	yes	yes	yes	
SEM metallization	MIL 2018	yes	yes	yes	
Package	Crystal Spec.	yes	yes	yes	

Notes:
1. at High Temperatures (exc. Lev.IV)
2. Point Estimate
3. 55°C, 0.7eV, 60%UCL
4. #accept/n
5. LTPD and AGL criteria in table above apply to each lot tested.
   CUM LTPD and AQL numbers are also required for Level II:

Individual Lot	Cum Lot Requirement
5% LTPD	3% LTPD
3% LTPD	1% LTPD
2.5% AQL	1.0% AQL

• Notes •

CS4328 Digital to Analog Converter

The CS4328 is the industry's first complete stereo digital-to-analog output system. This 18-bit stereo D/A converter uses Crystal's well established oversampling converter techniques.

The CS4328 includes the major system elements of 8X interpolation filter, 64X delta-sigma modulator, 1-bit D/A converter and a 124 dB signal-to-noise ratio analog anti-imaging filter, all in one packaged, tested, solution. The device features patented delta-sigma architectures to maintain excellent distortion performance, even at low signal levels. The output anti-imaging filters are the first to be based on a mixed linear/switched capacitor architecture. This approach is particularly insensitive to clock jitter and allows the benefit of scaling the bandwidth proportionally to the system master clock. The CS4328 is therefore adjustable for both audio and voice band applications. The flexible digital interface makes with CD player circuitry, DAT recorders and DSP's.

CS4303 Digital to Analog Converter

The CS4303 is an all digital I.C. containing an 8X interpolation filter and overall 64X oversampling delta-sigma modulator. Addition of an external analog reconstruction filter yields 107 dB dynamic range with superb low level linearity.

CS4330 Digital to Analog converter

Packaged in an 8 pin SOIC, the CS4330 is the world's smallest stereo audio DAC. This 16-bit complete digital-to-analog output system contains interpolation filters, 128X oversampling delta-sigma modulators, 1-bit D/A converters, and analog filtering. De-emphasis is also included for CD applications.

CONTENTS

Semiconductor Corporation

CS4303

107 dB, D/A Converter for Digital Audio

2

Features

- Stereo Delta-Sigma D/A converter
  8× Interpolation Filter
  64× Delta-Sigma DAC
- Single +5V Operation
- Adjustable System sampling Rates including 32 kHz, 44.1 kHz and 48 kHz
- 107 dB Dynamic Range Over the Audio Bandwidth
- ±0.0002 dB Passband Ripple
- Flexible Serial Input Port
  Supports Multiple Input Formats
  16 or 18 Bit Input Words

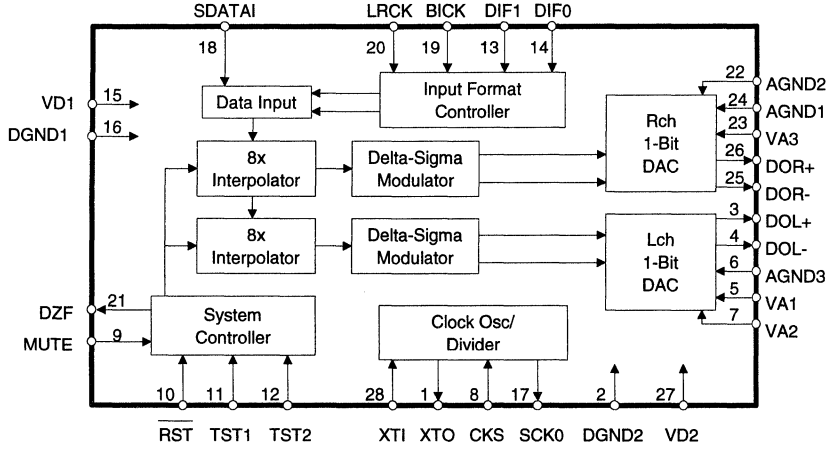
General Description

The CS4303 is a high performance delta-sigma D/A converter for digital audio systems which require wide dynamic range. The CS4303 includes 8× interpolation and a 64× oversampled delta-sigma modulator that outputs a 1-bit signal to an external analog low pass filter. The 1's density of the 1-bit signal is proportional to the digital input.

The CS4303 has a configurable input serial port that provides four interface formats. The master clock rate can be either 256 or 384 times the input word rate, supporting various audio environments.

Ordering Information:

Model	Temp. Range	Package Type
CS4303-KS	0° to 70°C	28-pin plastic SOIC
CS4303-KP	0° to 70°C	28-pin plastic DIP



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VD1, VA1, VA2, VA3, VD2 = +5.0V ; Full-scale Output Sinewave, 991 Hz; Input Word Rate = 48 kHz; BICK = 3.072 MHz; Logic "1" = VD, Logic "0" = DGND)

Parameter			Symbol	Min	Typ	Max	Units
Dynamic Performance							
Dynamic Range	(Note 1)			-	107	-	dB
Total Harmonic Distortion + Noise	(digital fullscale input)		THD+N	-	100	-	dB
Interchannel Isolation				-	115	-	dB
Power supplies							
Power Supply Current	$\overline{RST}$ = High:	VD1		-	27	-	mA
		VA1, VA2, VA3		-	4	-	mA
		VD2		-	2	-	mA
	$\overline{RST}$ = Low:	VD1		-	5	-	mA
		VA1, VA2, VA3		-	0.1	-	mA
		VD2		-	1	-	mA
Power Dissipation	($\overline{RST}$ = High)			-	165	300	mW

Note 1. Assumes ideal conversion of 1-bit data to an analog signal

DIGITAL FILTER CHARACTERISTICS (T_A = 25°C; VD1, VA1, VA2, VA3, VD2 = +5V± 5%; Input Word Rate = 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Pass Band	±0.0002 dB corner		0	-	21.8	kHz
	to -3 dB corner		0	-	23.5	kHz
Stop Band			26.2	-	-	kHz
Pass Band Ripple			-	-	±0.0002	dB
Stop Band Attenuation			90	-	-	dB
Group Delay	(IWR = Input Word Rate)		-	33/IWR	-	s
Deviation from Linear Phase			-	-	0	deg

ABSOLUTE MAXIMUM RATINGS (AGND1, AGND2, AGND3, DGND1, DGND2 = 0V; All Voltages With Respect to Ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:					
Positive Digital		VD	-0.3	6.0	V
Positive Analog	(VA1,VA2,VA3,VD2)	VA	-0.3	6.0	V
|VA - VD|			-	0.4	V
Input Current		I_{IN}	-	±10	mA
Digital Input Voltage			-0.3	VD + 0.3	V
Ambient Operating Temperature			-10	70	°C

Specifications are subject to change without notice.

2

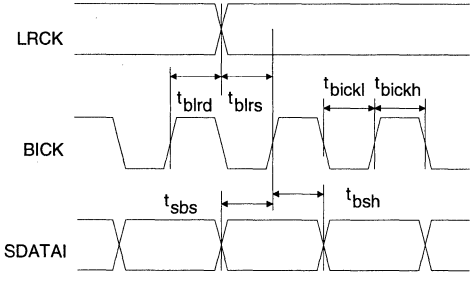
DIGITAL CHARACTERISTICS (T_A = 25°C; VD1, VA1, VA2, VA3, VD2 = 5V ± 5%; Input Word Rate = 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Digital Input Voltage	High-level	V_{IH}	VD - 1.0	-	-	V
	Low-level	V_{IL}	-	-	1.0	V
Digital Output Voltage	High-level I_o = -20µA	V_{OH}	4.4	-	-	V
	Low-level I_o = +20µA	V_{OL}	-	-	0.1	V
Input Leakage Current		I_{IN}	-	±1.0	-	µA

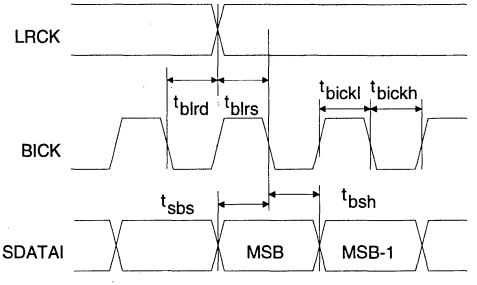
SWITCHING CHARACTERISTICS (T_A = 25 °C; VA1, VA2, VA3, VD1, VD2 = 5V ± 5%; Inputs: Logic 0 = DGND, Logic 1 = VD, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency using Internal Oscillator:						
CKS=H	(384 x Fs)	XTI/XTO	10.7	-	19.2	MHz
CKS=L	(256 x Fs)	-	7.1	-	13.9	MHz
Master Clock Frequency using External Clock:						
CKS=H	(384 x Fs)	XTI/XTO	0.384	-	19.2	MHz
CKS=L	(256 x Fs)	-	0.256	-	13.9	MHz
XTI/XTO Pulse Width Low			21	-	-	ns
XTI/XTO Pulse Width High			21	-	-	ns
BICK Pulse Width Low		t_{bickl}	30	-	-	ns
BICK Pulse Width High		t_{bickh}	30	-	-	ns
BICK Period		t_{bickw}	80	-	-	ns
BICK rising to LRCK edge delay	(Note 2)	t_{blrd}	35	-	-	ns
BICK rising to LRCK edge setup time	(Note 2)	t_{blrs}	35	-	-	ns
SDATAI valid to BICK rising setup time	(Note 2)	t_{sbs}	35	-	-	ns
BICK rising to SDATAI hold time	(Note 2)	t_{bsh}	35	-	-	ns
RST Minimum Pulse Width Low			2 periods of XTI/XTO			

Note: 2. "BICK rising" refers to modes 0, 1, and 3. For mode 2, replace "BICK rising" with "BICK falling."



Serial Data Input Timing (Modes 0, 1 and 3)



Serial Data Input Timing (Mode 2)

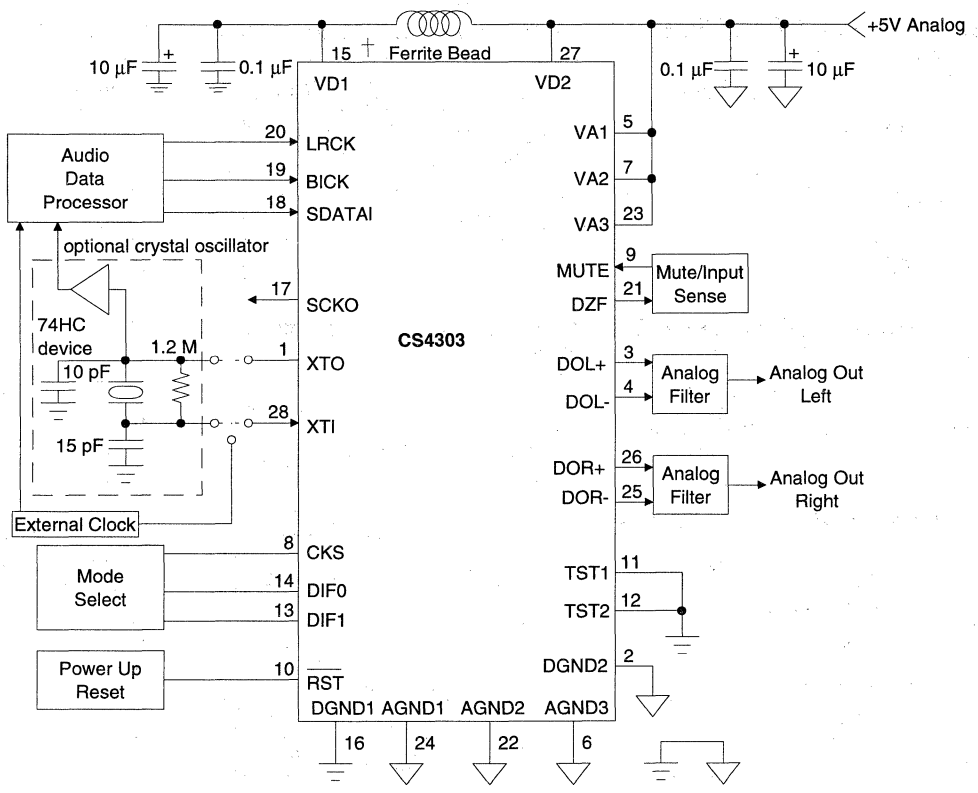


Figure 1. CS4303 Typical Connection Diagram

GENERAL DESCRIPTION

The CS4303 is a stereo digital-to-analog system designed for digital audio. The system accepts data at standard audio frequencies, such as 48 kHz, 44.1 kHz, and 32 kHz. The architecture includes an 8× oversampling filter followed by a 64× oversampled one-bit delta-sigma modulator and 1-bit DAC as shown in Figure 2. The 1-bit data is passed through an external analog low-pass filter to produce the audio signal.

The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of laser trimmed resistive DAC architectures by using an inherently linear 1-bit DAC. The advantages of a 1-bit DAC include: ideal differential linearity, no distortion mechanisms due to resistor matching errors and no linearity drift over time and temperature due to variations in resistor values.

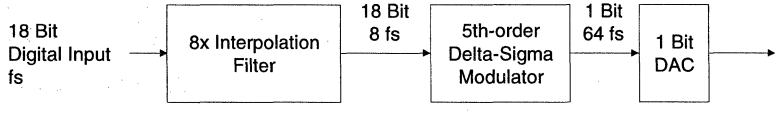


Figure 2. CS4303 Architecture

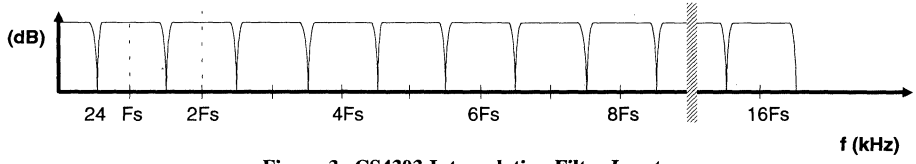


Figure 3. CS4303 Interpolation Filter Input

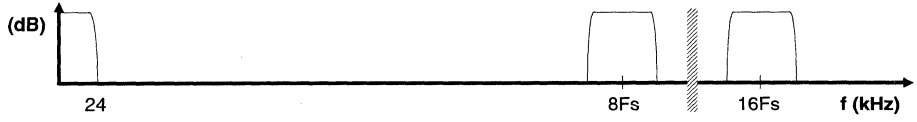


Figure 4. CS4303 Interpolation Filter Output

Digital Interpolation Filter

The digital interpolation filter increases the sample rate by a factor of 8 and eliminates images of the baseband audio signal which exist at multiples of the input sample rate, Fs (Figure 3). This allows for the selection of a less complex analog filter based on out-of-band noise attenuation requirements rather than anti-image filtering. Following the interpolation filter, the resulting frequency spectrum (Figure 4) has images of the input signal at multiples of eight times the input sample rate, 8Fs. These images are removed by the analog filter required to filter the 1-bit data.

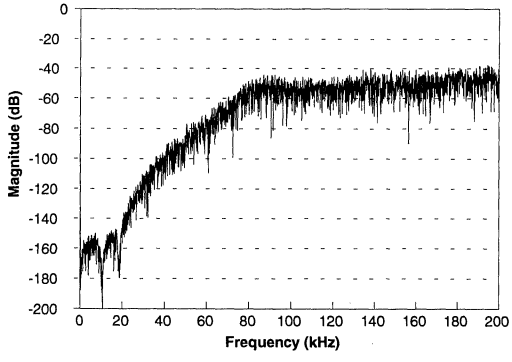


Figure 5. 1-bit Modulator Output (Fs = 48 kHz)

Delta-Sigma Modulator

The interpolation filter is followed by a fifth-order delta-sigma modulator which converts the 8Fs multi-bit interpolation filter output into 1-bit data at 64 times Fs. The frequency spectrum of the 1-bit delta- sigma modulator output is shown in Figure 5 for an Fs of 48 kHz.

One-Bit DAC

The CS4303 incorporates a differential output to maximize the output level and minimize the amount of gain required in the analog filter. Figure 6 shows each output as well as the differentially summed output for an arbitrary 1-bit data stream.

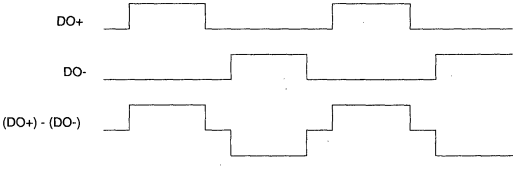


Figure 6. CS4303 Differential Outputs

Return-to-zero coding is utilized where each occurence of a 1 is 75% high and returns low for 25% of the bit period as shown in Figure 7. This technique ensures that the energy within each 1 includes the effects of finite rise and fall times regardless of the previous or next state and minimizes distortion.

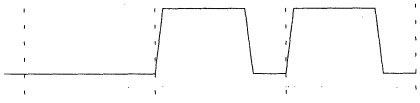


Figure 7. Return to Zero Encoding

SYSTEM DESIGN

System Clock Input

The master clock (XTI/XTO) input to the DAC is used to operate the digital interpolation filter and the delta-sigma modulator. The master clock can be either a crystal placed across the XTI and XTO pins, or an external clock input to the XTI pin with the XTO pin left floating.

The frequency of XTI/XTO is determined by the desired Input Word Rate, IWR, and the setting of the Clock Select pin, CKS. IWR is the frequency at which words for each channel are input to the DAC and is equal to the LRCK frequency. Setting CKS low selects an XTI/XTO frequency of 256× IWR while setting CKS high selects 384× IWR. Table 1 illustrates various audio word rates and corresponding frequencies used in the DAC.

The remaining system clocks, LRCK and BICK, must be synchronously derived from XTI/XTO. If the CS4303 internal oscillator is used, the circuit must be configured and XTO buffered as shown in Figure 1. XTI/XTO can be divided to produce LRCK and BICK using a synchronous counter such as 74HC590. Notice that the value of the capacitor on XTO is 10 pF and the XTI capacitor is 15 pF, which allows for 5 pF of gate and stray capacitance.

LRCK (kHz)	CKS	XTI/XTO (MHz)
32	low	8.192
44.1	low	11.2896
44.1	high	16.9344
48	low	12.288

Table 1. Common Clock Frequencies

Serial Data Interface

Data is input to the CS4303 via three serial input pins; SDATAI is the serial data input, BICK is the serial data clock and LRCK defines the channel and delineation of data. The DAC supports four serial data formats which are selected via the digital input format pins DIF0 and DIF1. The different formats control the relationship of LRCK to SDATAI and the edge of BICK used to latch data. Table 2 lists the four formats, along with the associated figure number. Format 0 is compatible with existing 16-bit D/A converters and digital filters. Format 1 is an 18-bit version of format 0. Format 2 is similar to Crystal ADCs and many DSP serial ports. Format 3 is compatible with the I^2S serial data protocol. Formats 2 and 3 support 18-bit input or 16-bit followed by two zeros. In all four serial input formats, the serial data is MSB-first and 2's-complement format.

Formats 0, 2 and 3 will operate with 16-bit data and 16 BICK pulses as well. See Figure 11 for

DIF1	DIF0	Format	Figure
0	0	0	8
0	1	1	8
1	0	2	9
1	1	3	10

Table 2. Digital Input Formats

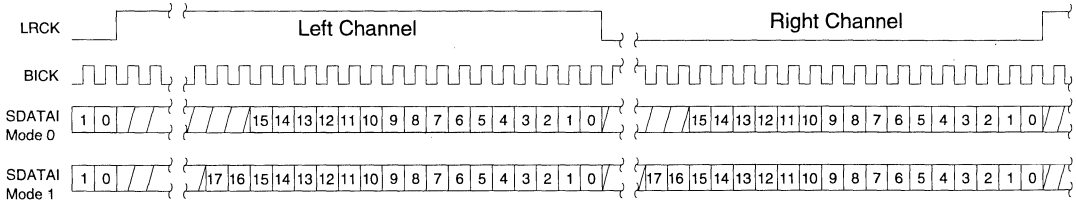


Figure 8. Digital Input Formats 0 & 1

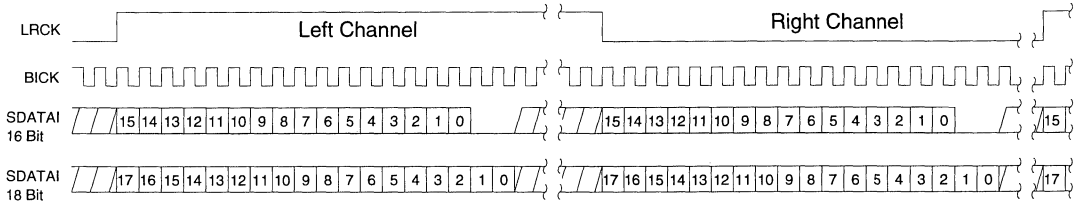


Figure 9. Digital Input Format 2

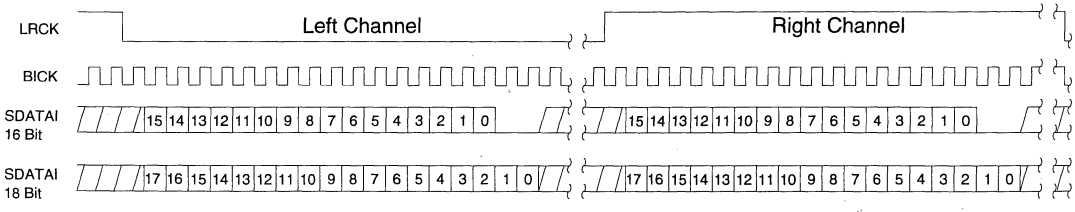


Figure 10. Digital Input Format 3

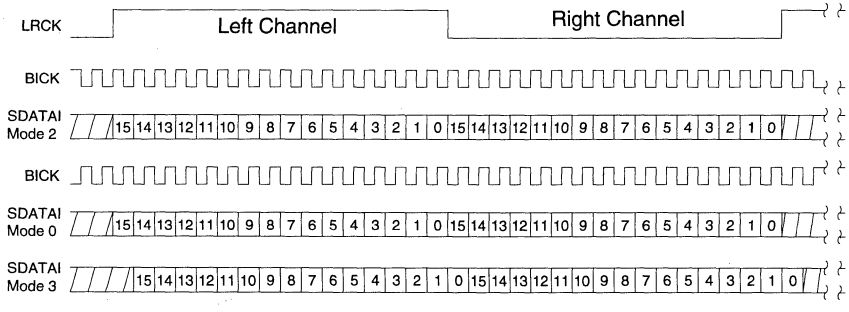


Figure 11. Digital Input Formats 0, 2 and 3 with 16 BICK Periods

16-bit timing. However, the use of BICK = 64× IWR is recommended to minimize the possibility of performance degradation resulting from BICK coupling on the supply voltages.

Reset

$\overline{\text{RST}}$ is an active low signal that resets the digital filter and delta-sigma modulator and synchronizes LRCK with internal control signals. The CS4303 DOL+\- and DOR+\- outputs are forced to zero during reset.

Power-Up Considerations

Upon initial application of power to the DAC, the digital filter registers will be indeterminate. $\overline{\text{RST}}$ should be low during power-up to prevent this erroneous information from being output from the DAC. Bringing $\overline{\text{RST}}$ high will initialize these registers.

Muting

The Mute functions of the CS4303 involve the recognition of 0 input data for 4096 consecutive LRCK cycles. If the MUTE pin is HIGH, the DATA outputs will be forced to 0 following 4096 LRCK cycles with 0 input data. If left LOW, the MUTE circuit will ignore 0 input data. The DZF, Data Zero Flag, pin will go HIGH following 0 input data for 4096 consecutive LRCK cycles regardless of the Mute pin status. The DZF output can be used to control an external muting circuit.

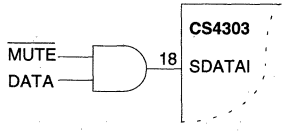


Figure 12. Muting Implementation

A two stage MUTE operation can be implemented by forcing SDATAI to 0 using an AND gate as shown in Figure 12. The first mute occurs following 33 LRCK cycles when the 0 input data propagates to the output of the DAC. Following a total of 4096 LRCK cycles with 0 input data the output of the CS4303 will mute. Upon release of the MUTE command and non-zero input data, the CS4303 output mute will immediately release. However, 33 LRCK cycles are required for input data to propagate to the output.

Analog Output and Filtering

The primary function of the analog filter is to attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The selection of the filter transfer function is based on the optimization of out-of-band noise attenuation, passband amplitude and phase requirements. The computer simulated frequency spectrum of the 1-bit delta-sigma modulator output is shown in Figure 5 for an Fs of 48 kHz. Figures 13-15 show the results of computer simulations demonstrating the attenuation of out-of-band noise with 3, 5 and 7 pole Butterworth filters. The filter corner frequencies were selected to achieve a maximum attenuation of 0.2 dB at 20kHz.

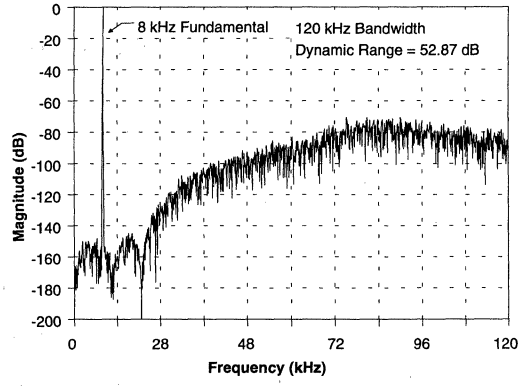


Figure 13. Simulated Noise Attenuation 3rd Order Filter

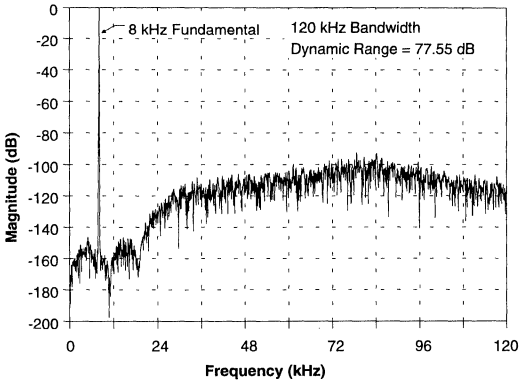


Figure 14. Simulated Noise Attenuation Fifth Order Filter

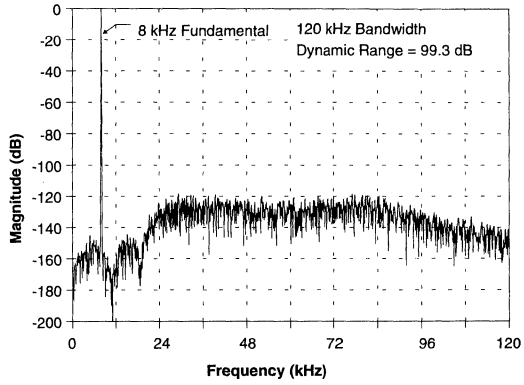


Figure 15. Simulated Noise Attenuation Seventh Order Filter

The suggested filter of Figures 16-19 is a 5-pole Butterworth modified to realize a 6-pole response. Implementing a pole as a passive RC in the input of the analog circuit along with a high slew rate op-amp will eliminate slew rate related distortion. This architecture provides matched loading for the differential outputs and a noise-free pole for additional out-of-band noise attenuation.

Measuring System Performance

The effects of out-of-band noise must be considered when making THD+N and dynamic range measurements. The dynamic range specifications of Figures 13-15 are identical over a 20kHz bandwidth but differ by 46 dB over the 120kHz bandwidth. The proper use of a measurement bandlimiting filter is critical for evaluating the in-band performance of systems with low-order analog filters. The measurement bandwidth must be properly limited to prevent out-of-band energy from dominating the measurements.

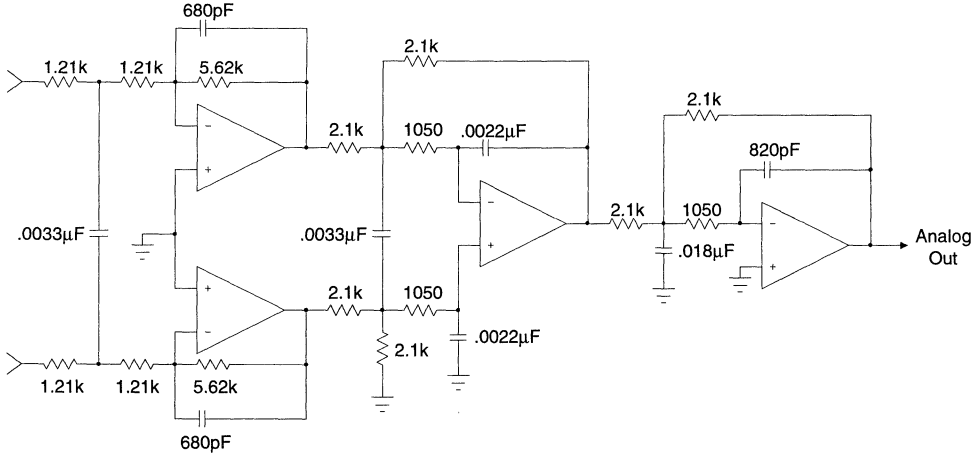


Figure 16. Suggested 6-Pole Analog Filter

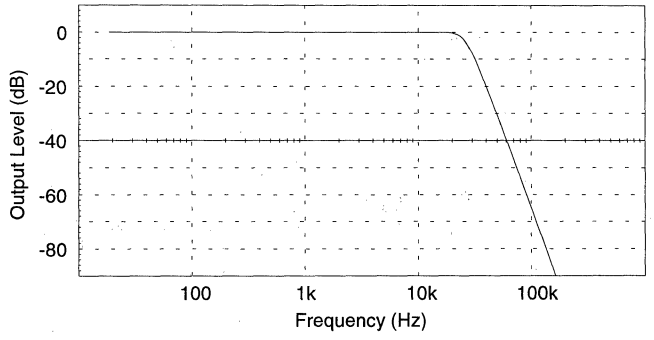


Figure 17. Simulated Analog Filter Frequency Response

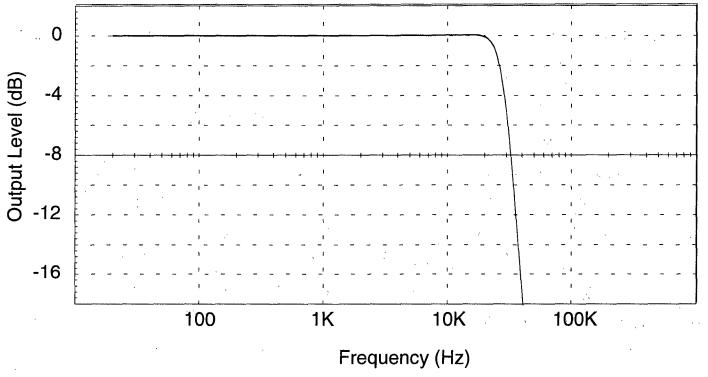


Figure 18. Simulated Analog Filter Frequency Response Expanded Scale

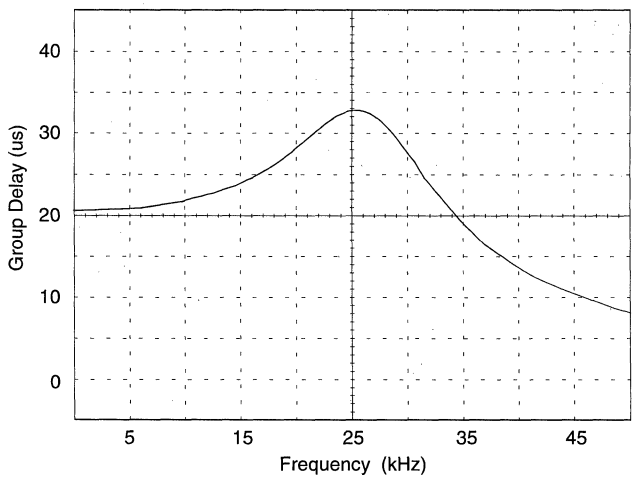


Figure 19. Simulated Analog Filter Group Delay

System Performance Measurements

The following collection of CS4303 measurement plots (IWR = 48 kHz) were taken from a CDB4303 evaluation board with an Audio Precision Dual Domain System One. All FFT plots are 16,384 point. Several of the plots are influenced by inadequate dithering of the test signal.

Figure 20 shows the **unmuted noise**. This data was taken by feeding the CS4303 all zero's. This plot shows the noise shaping characteristics of the delta-sigma modulator combined with the analog filter.

Figure 21 shows the A-weighted **THD+N vs signal amplitude** for a dithered 1kHz input signal. The small variations in THD + N at around -70 dB are caused by inadequate dithering of the test signal. The System One was set to 18-bit triangular dither.

Figures 22 and 23 show the **fade-to-noise linearity**. The input test signal is a dithered 500 Hz sine wave which gradually fades from -60 dB level to -120 dB. During the fading, the output level from the CS4303 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs of -90 dB. The gradual shift of the plot away from zero at signal levels < -100 dB is caused by the background noise starting to dominate the measurement. Figure 22 shows the result with 18-bit dithered data. The 1 dB shift at -95 dB is due to inadequate dither. Figure 23 shows the result with 16-bit dithered data.

Figure 24 shows a 16K **FFT plot result, with a 1 kHz -100 dB 17-bit dithered input**. Notice the lack of distortion components.

Figure 25 shows the **monotonicity test** result plot. The input data to the CS4303 is +1 LSB, -1 LSB four times, then +2 LSB, -2 LSB four times and so on, until +10 LSB, -10 LSB. This data pattern is taken from track 21 of the CD-1 test disk. Notice the increasing staircase envelope, with no decreasing elements. Notice also the clear resolution of the LSB. For this test, one LSB is a 16-bit LSB.

The following tests were done by filtering the analog output of the CS4303 with the System One analyzer 1 kHz notch filter to reduce the peak signal level. The resulting signal was then amplified and applied to the DSP module, avoiding distortion in the System One A/D converter.

Figure 26 shows a **16K FFT Plot with a 1 kHz, 0 dB** input. Notice the low order harmonic distortion at < -100 dB.

Figure 27 shows a **16K FFT Plot with a 1 kHz, -10 dB** input. Notice the almost complete absence of distortion, with a small residual 2nd harmonic below -120 dB.

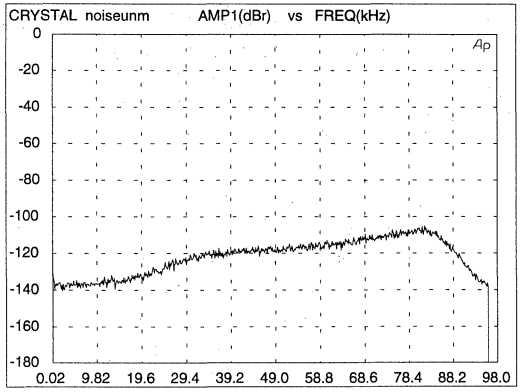


Figure 20. Unmuted Noise

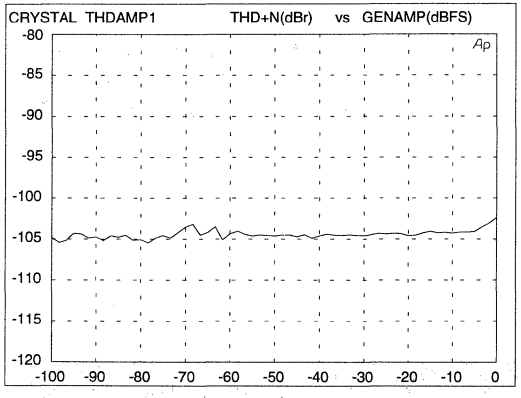


Figure 21. 1 kHz A-weighted THD + N vs Level

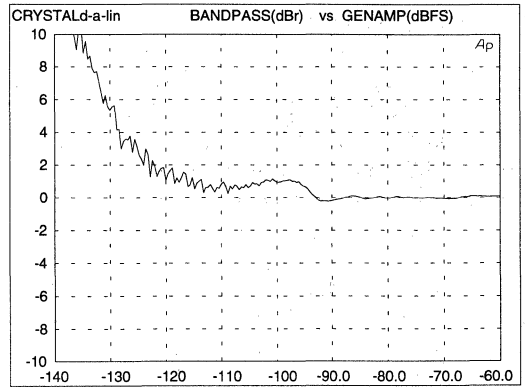


Figure 22. Fade to Noise Dithered 18-bit Linearity

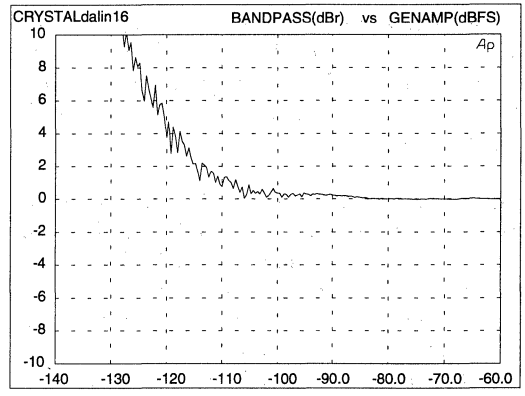


Figure 23. Fade to Noise Dithered 16-bit Linearity

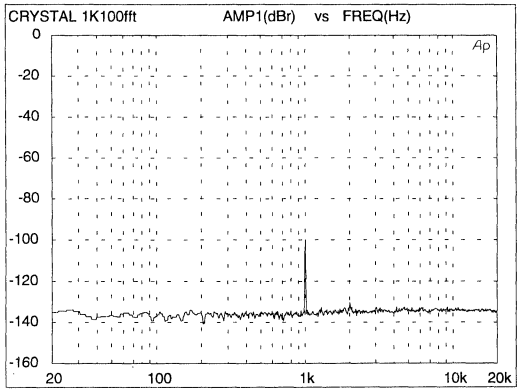


Figure 24. 1 kHz -100 dB FFT

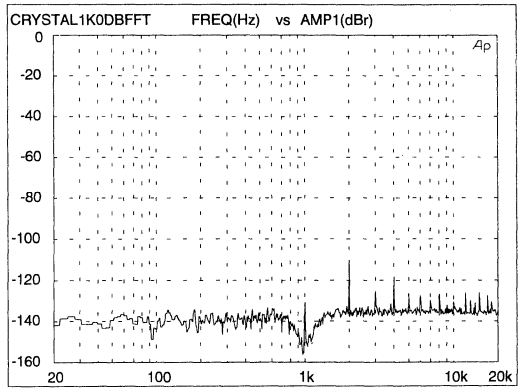


Figure 26. 1kHz 0 dB FFT

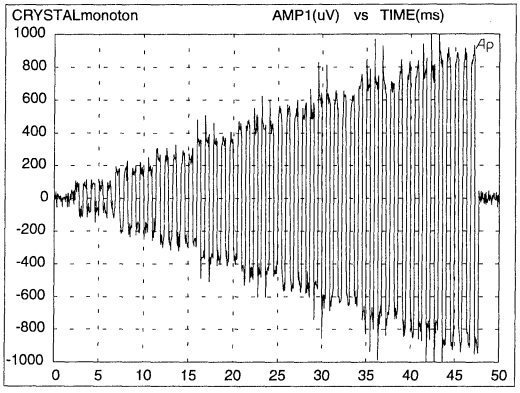


Figure 25. Monotonicity Test (16-bit Data)

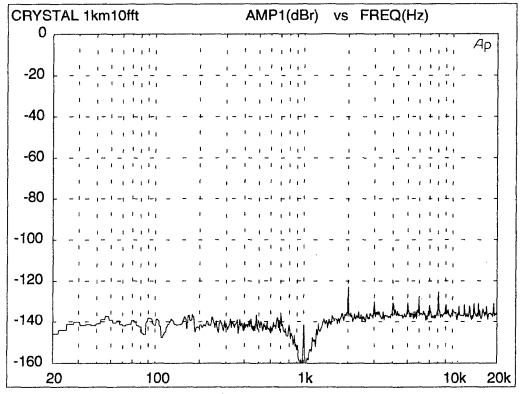
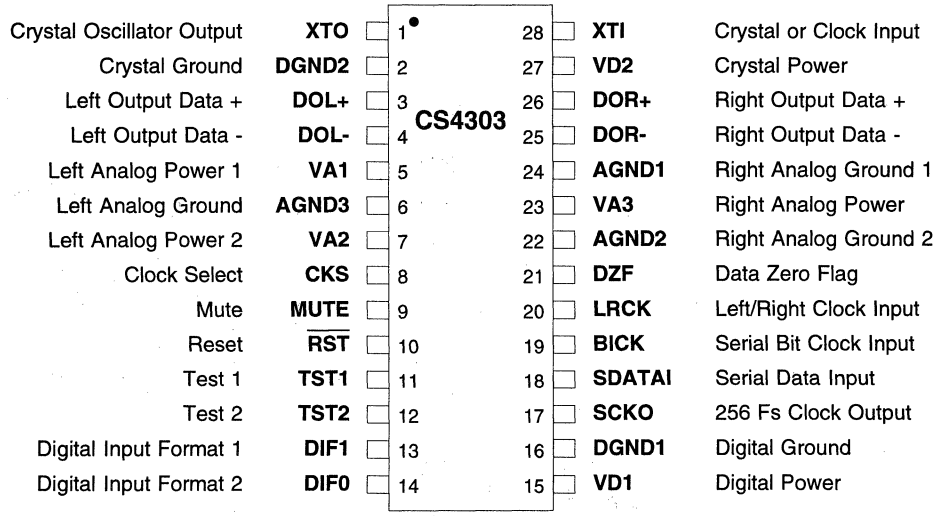


Figure 27. 1 kHz -10 dB FFT

PIN DESCRIPTIONS



Power Supply Connections

VA1, VA2, VA3 - Analog Power, PINS 5, 7, 23.
Positive analog supplies. Nominally +5 volts.

AGND1, AGND2, AGND3 - Analog Grounds, PINS 6, 22, 24.
Analog ground reference.

VD1 - Digital Power, PIN 15.
Positive supply for the digital section. Nominally +5 volts.

DGND1 - Digital Ground, PIN 16.
Ground for the digital section.

VD2 - Crystal Power, PIN 27.
Positive supply for the crystal oscillator. Nominally +5 volts.

DGND2 - Crystal Ground, PIN 2.
Crystal ground reference.

Digital Inputs

XTI - Crystal or Clock Input, PIN 28.

A crystal oscillator can be connected between this pin and XTO, or an external CMOS clock can be input on XTI. The frequency must be either 256× or 384× the input word rate based on the clock select pin, CKS.

MUTE - Mute Input, PIN 9.

This input determines if the CS4303 will recognize an input string of 4096 zeros to initiate a muted output. If left low, the CS4303 will not mute.

DZF - Data Zero Flag, PIN 21.

This pin will go High following 0 input data for 4096 consecutive LRCK cycles regardless of the Mute pin status.

SCKO - Serial Clock Output, PIN 17

Clock output of 256× the input word rate regardless of the CKS pin status.

LRCK - Left/Right Clock, PIN 20.

This input determines which channel is currently active on the Serial Data Input pin, SDATAI. The format of LRCK is controlled by DIF0 and DIF1.

BICK - Serial Bit Input Clock, PIN 19.

Clocks the individual bits of the serial data in from the SDATAI pin. The polarity with respect to the serial data is controlled by DIF0 and DIF1.

SDATAI - Serial Input, PIN 18.

Two's complement MSB-first serial data of either 16 or 18 bits is input on this pin. The data is clocked into the CS4303 via the BICK clock and the channel is determined by the LRCK clock. The format for the previous two clocks is determined by the Digital Input Format pins, DIF0 and DIF1.

DIF0, DIF1 - Digital Input Format, PINS 14, 13.

These two pins select one of four formats for the incoming serial data stream. These pins set the format of the BICK and LRCK clocks with respect to SDATAI. The formats are listed in Table 2.

CKS - Clock Speed Select, PIN 8.

Selects the clock frequency input on the XTI pin. CKS low selects 256× the input word rate (LRCK frequency) while CKS high selects 384×.

$\overline{\text{RST}}$ - Reset, PIN 10.

When reset is low, the filters and modulators are held in reset.

TST1, TST2 - Test Inputs, PINS 11, 12.

Allows access to the CS4303 test modes, which are reserved for factory use. Must be tied to DGND.

Digital Outputs

XTO - Crystal Oscillator Output, PIN 1.

When a crystal oscillator is used, it is tied between this pin and XTI. When an external clock is input, this pin should be left floating.

DOL+, DOL- - Digital Left Channel Output, PINS 3, 4.

Differential digital output data for the left channel.

DOR+, DOR- - Digital Right Channel Output, PINS 26, 25.

Differential digital output data for the right channel.

Semiconductor Corporation

CDB4303

Evaluation Board for CS4303

Features

- Demonstrates techniques used to achieve 104 dB Dynamic Range and fullscale THD+N > 101 dB.
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

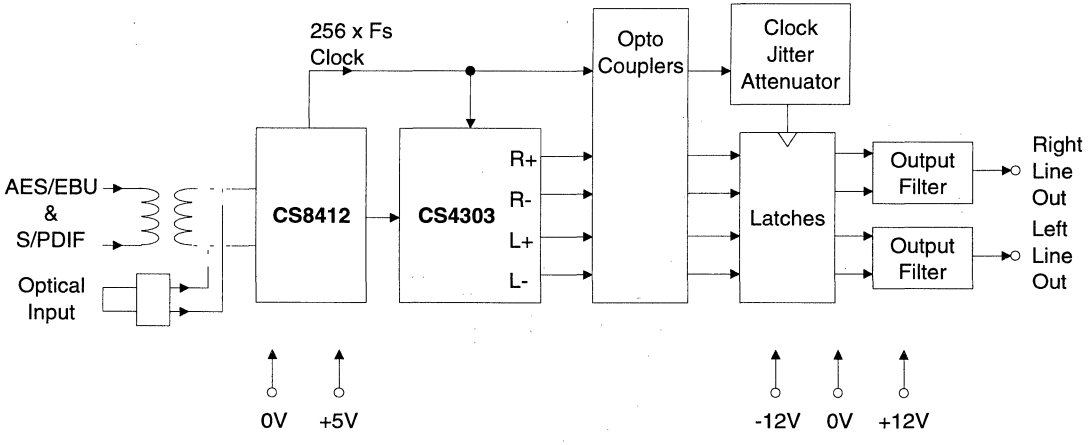
General Description

The CDB4303 evaluation board is an excellent means for quickly evaluating of the CS4303 18-bit, stereo D/A converter. The board is configured to accept digital audio data via coax or optical interfaces. Analog outputs are provided via RCA connectors for both channels. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply.

The CDB4303 includes optocouplers, clock jitter attenuator, off-chip 1-bit latch, analog filtering and a CS8412 digital audio receiver I.C. The CS8412 provides the system timing necessary to operate the CS4303 and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data.

ORDERING INFORMATION: CDB4303

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

CS4303 Audio DAC

The CDB4303 is an example application of the CS4303 which includes optocouplers, a Phase Lock Loop / VCXO and external latches. These techniques allow for maximum isolation and control of potential error mechanisms.

A description of the CS4303 including the functions of CKS, MUTE, DIF0 and DIF1 are discussed in the CS4303 data sheet. The recommended jumper positions for the evaluation board are listed in Table 2. A power-up and user activated reset circuit is provided by D11, R7, C6, U4 and SW2.

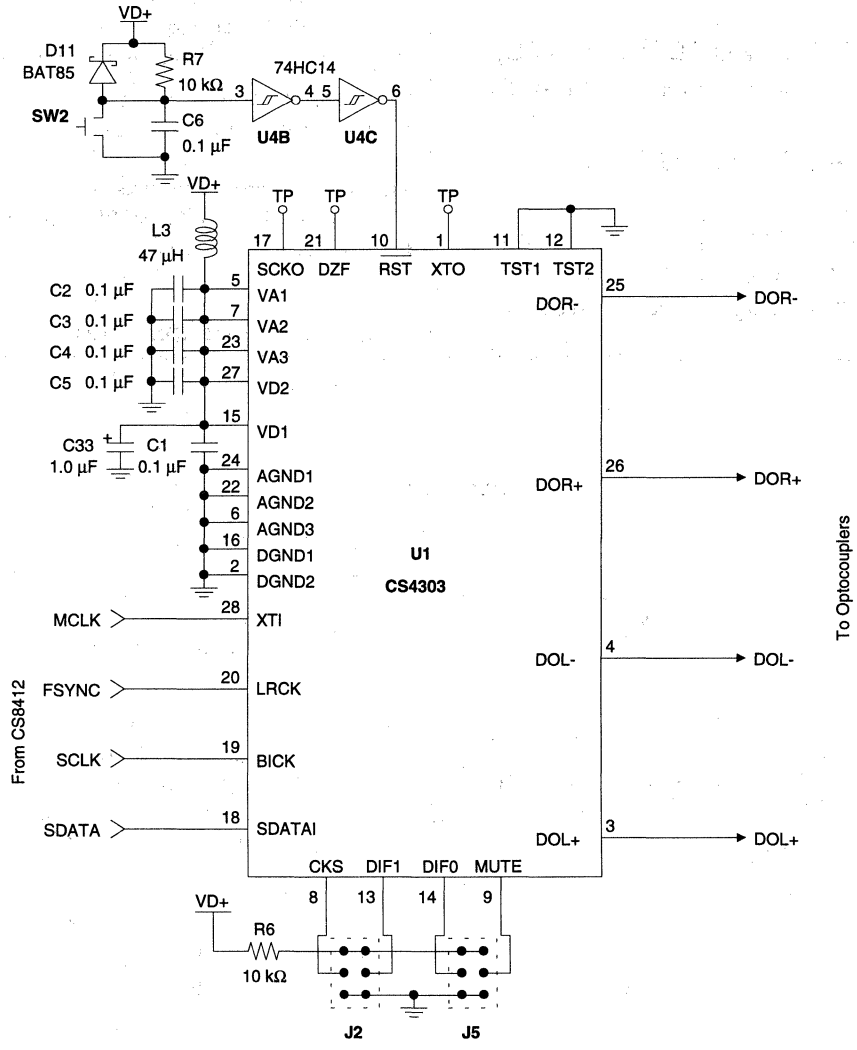


Figure 1. CS4303 DAC Connections

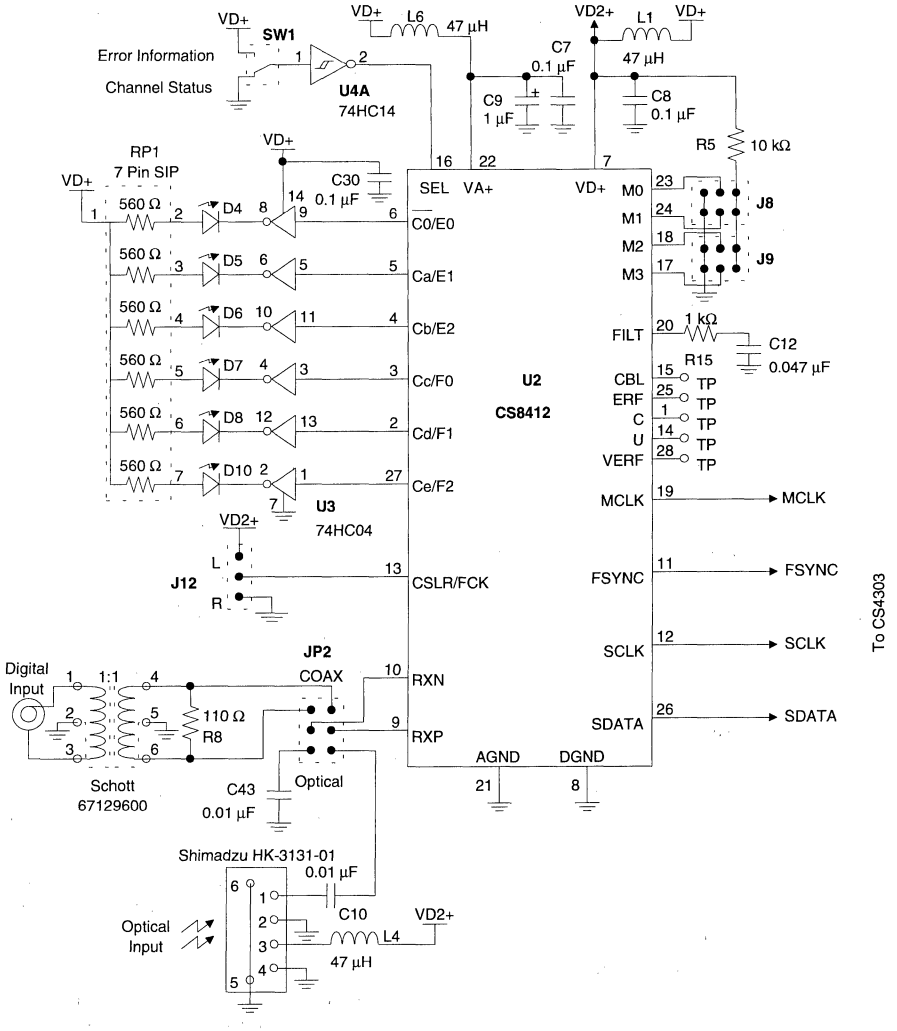


Figure 2. CS8412 Digital Audio Receiver Connections

CS8412 Digital Audio Receiver

The system receives and decodes standard AES/EBU and S/PDIF data formats using a CS8412 Digital Audio Receiver as shown in Figure 2. The data input circuit can be configured to accept either professional or consumer modes via coax or optical means. The outputs of the CS8412 include a serial bit clock, serial data, a word clock and a 256Fs master clock

The operation of the CS8412 is covered in detail in the CS8412 data sheet and includes a description of the AES/EBU and S/PDIF hardware and data formats. Refer to Table 2 for the CDB4303 jumper options for the CS8412. The circuit is factory configured for AES/EBU and can be modified for S/PDIF by substituting a 75 ohm resistor for R8.

The LEDs, D4-D8 and D10, perform two functions. When S1 is in the Channel Status position, the LEDs display the channel status information for the channel selected by J12. The channel status information is explained in the CS8412 data sheet.

When S1 is in the Error Information position, the LEDs D4-D6, display encoded error information that can be decoded by consulting the CS8412 data sheet. Encoded sample frequency information is displayed on LEDs D7,D8 and D10 provided a proper clock is being applied to the FCK pin of the CS8412. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8412. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of J12 should be selected if the FCK pin is being driven by a clock signal.

Optocouplers

Optocouplers provide effective isolation between the analog circuitry and digital circuit noise, Figure 3. Hewlett-Packard HCPL-7101 optocouplers were chosen since they have built in CMOS input buffers and operate at 40MHz. The high output slew rate of the optocouplers yields minimum corruption of the signal edges and low jitter on the clock. The input side of the optocouplers is well decoupled, since the LED's create significant current spikes. The output side of the optocouplers is referenced to analog ground and the data optocouplers are powered with a separate +5V power regulator, U16. A large physical gap between the pins of each side of the optocoupler package was maintained on the circuit board to ensure maximum digital to analog isolation.

1-Bit Latch

The external CMOS latch, Figure 3, used to time the data is a 74AC11074 from Texas Instruments. This dual D-type flip-flop was chosen because of its center power and ground connections, which reduce internal inductances and the possibility of the supplies being modulated by the output signal. The device also has a high output drive capability which allows minimizing the input impedance of the analog filter for noise considerations.

The power supplies to the latch are the voltage references for the 1-bit data. Each latch is powered from a separate +5V regulator, U14 and U15, to decrease interaction between channels and minimize noise. Extreme care was taken to optimize the supply decoupling with high frequency capacitors positioned very close to the supply and ground pins.

Proper latch supply decoupling is also important to minimize distortion. The one's density of the data produces variations in the latch power supply loading. Modulation of the latch supply voltage by the 1-bit data is effectively multiplying the signal by itself, which produces 2nd harmonic distortion.

There are significant advantages in the use of a dual flip-flop. Due to the differential nature of the DAC output, it is possible to minimize thermal gradients within the latch and improve distortion performance. This can be accomplished by using a separate dual latch for each channel.

The latch clock rising edge is timed so that the set-up and hold time requirements for the data inputs are met with a generous margin.

Clock Jitter Attenuator / VCXO

Clock jitter can originate from the original AES/EBU signal, the VCO in the CS8412, and from the optocouplers. To reduce the clock jitter as much as possible prior to the latch, a Phase Lock Loop (PLL) is used as a jitter attenuator. Figure 4 shows the schematic of the latch clock generator/jitter attenuator. The PLL consists of a

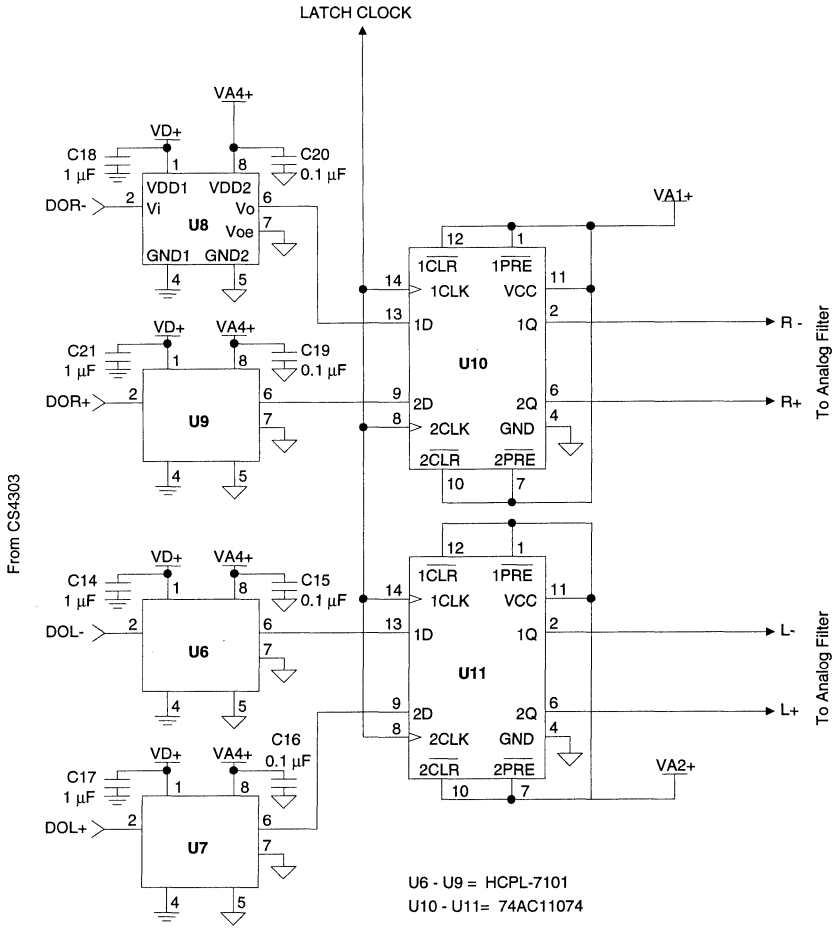


Figure 3. Optocouplers and Latch Circuitry

phase detector, a voltage controlled crystal oscillator and a loop filter.

The phase detector was implemented using an 74AC11086 exclusive or gate. This phase detector introduces a 90 degree phase shift, which results in the correct timing of the output clock for the latch. The phase detector is also inherently free from hysteresis, which improves jitter performance.

The requirement for a low jitter clock led to the choice of a voltage controlled crystal oscillator (VCXO). The VCXO has a limited frequency range and a substitution is required for changes in sample rate. The CDB4303 includes a 11.2896 MHz VCXO for a 44.1 kHz sample rate and and a 12.288 MHz VCXO for a 48 kHz sample rate. The VC7025 VCXO can be obtained from RALTRON (phone number 305-593-6033).

Power for the phase detector and VCXO must be very clean in order to avoid output clock jitter. An independent +5V regulator, U16, for the VCXO and phase detector ensures a minimum amount of coupling between the VCXO/phase

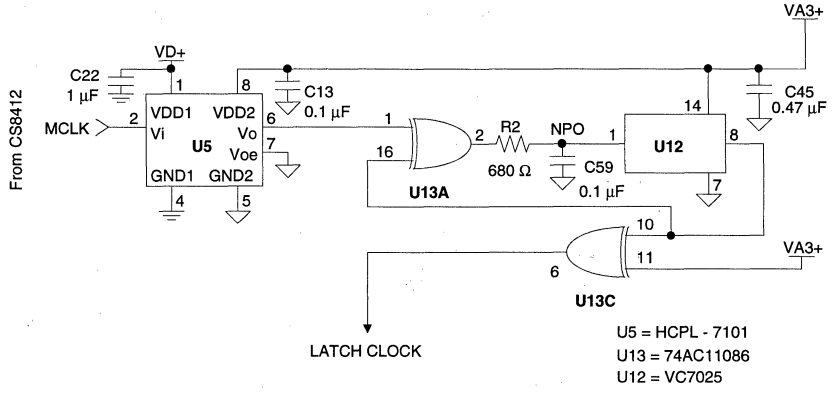


Figure 4. Clock Jitter Attenuator / VCXO

detector and the remaining circuitry via the supply. The layout of the PLL is such that the loop filter is close to the VCXO. This minimizes the possibility of induced noise into the control pin on the VCXO.

Analog Filter

The circuit of Figure 5 is a 5-pole Butterworth modified to realize a 6-pole response. A complete discussion of the circuit including frequency and group delay plots is included in the CS4303 data sheet.

Power Supply Circuitry

Figure 6 shows the evaluation board power supply block diagram. Power is supplied to the evaluation board by five binding posts. The 5 V analog power supply inputs are derived from 12 V using the voltage regulators U14 - U17. The +5 V digital supply for the converter and the

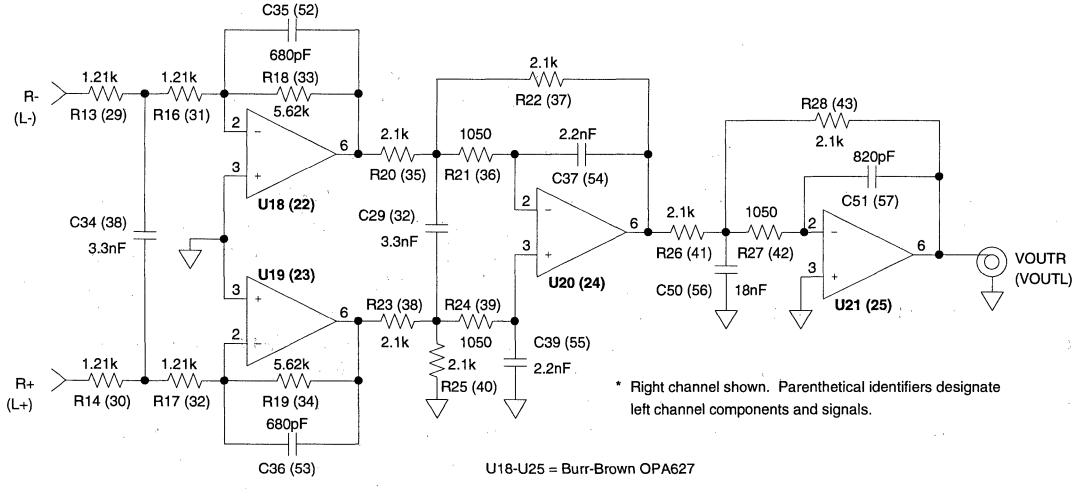


Figure 5. 6-Pole Analog Filter

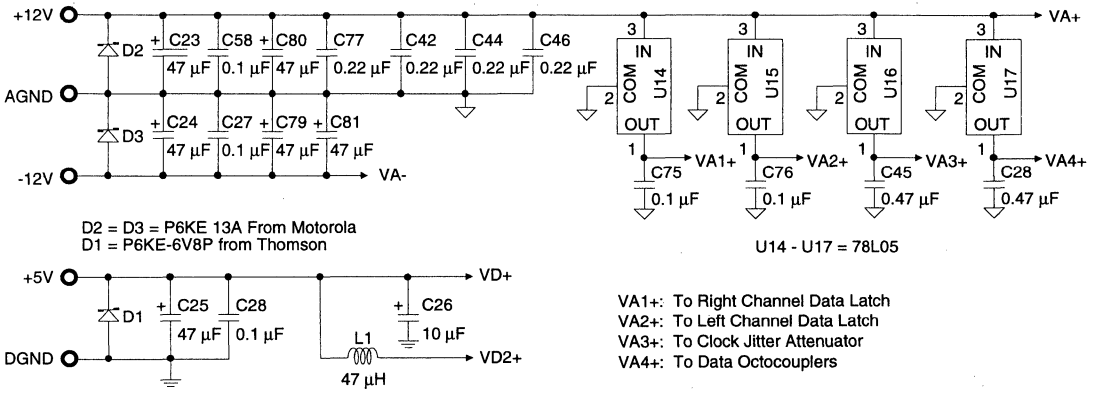


Figure 6. Power Supply

discrete logic on the board is provided by the +5 V and DGND binding posts. D1, D2, and D3 are transient suppressors which also provide protection from incorrectly connected power supply leads. The evaluation board intentionally isolates the analog and digital ground planes. The digital and analog grounds should not be joined at the power supply.

Evaluation of the CDB4303

The DAC system can be evaluated by connection to any digital audio source via either the AES/EBU or S/PDIF interface. This includes a CDB5326/7/8/9, CDB5336/8/9 or CDB5389 Analog-to-Digital-Converter evaluation board as well as a CD or DAT digital output.

The CDB4303 jumpers should be set to the factory default setting of Table 2. The VCXO must be selected for the appropriate system sample frequency.

Evaluation using the CDB5326/7/8/9 or CDB5336/8/9 as a signal source

An analog input of ± 3.68 V will produce a full scale digital output from the CS5336/7/9 and the CS5326/7/8/9. A full scale digital input to the CS4303 will produce a full scale output of ± 2.8V resulting in an overall loss of approximately 2.3 dB from input to output.

Interconnection requires the power supply connections and a shielded twisted pair cable (or optical cable) connecting the digital outputs from the ADC evaluation board to the digital inputs on the CDB4303. It is recommended that the power connections for each board are brought directly from the power supply and not in a "daisy-chain" manner from board to board.

References:

"An 18-Bit Delta-Sigma D/A Processor System Achieving Full-scale THD+N > 100dB" by Steven Green and Steven Harris presented at the 93rd Audio Engineering Society Convention. Preprints are available from the AES and Crystal Semiconductor.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+12	input	+12 Volts from power supply for analog section
-12	input	-12 Volts from power supply for analog section
AGND	input	analog ground connection from power supply
+5	input	+5 Volts from power supply for digital section
DGND	input	digital ground connection from power supply
OUTL	output	left channel analog output
OUTR	output	right channel analog output
OPTICAL INPUT	input	digital audio interface optical input
DIGITAL INPUT	input	digital audio interface coax input

Table 1. System Connections

JUMPER	PURPOSE		POSITION	FUNCTION SELECTED
J12	selects channel for CS8412 channel status information		L R	See CS8412 data sheet for details
JP2	selects digital audio input source		COAX OPTI	activates the coax input activates the optical input
J8, J9	CS8412 mode select	M0 M1 M2 M3	*Low *Low *Low *Low	See CS8412 data sheet for details
J2, J5	CS4303 mode select	DIF0 DIF1	*Low *High	See CS4303 data sheet for details
J2	CS4303 clock select	CKS	*Low High	selects 256Fs master clock selects 384Fs master clock
J5	MUTE		*High Low	Mute function is active disables Mute function

* Default setting from factory

Table 2. Jumper Selectable Options

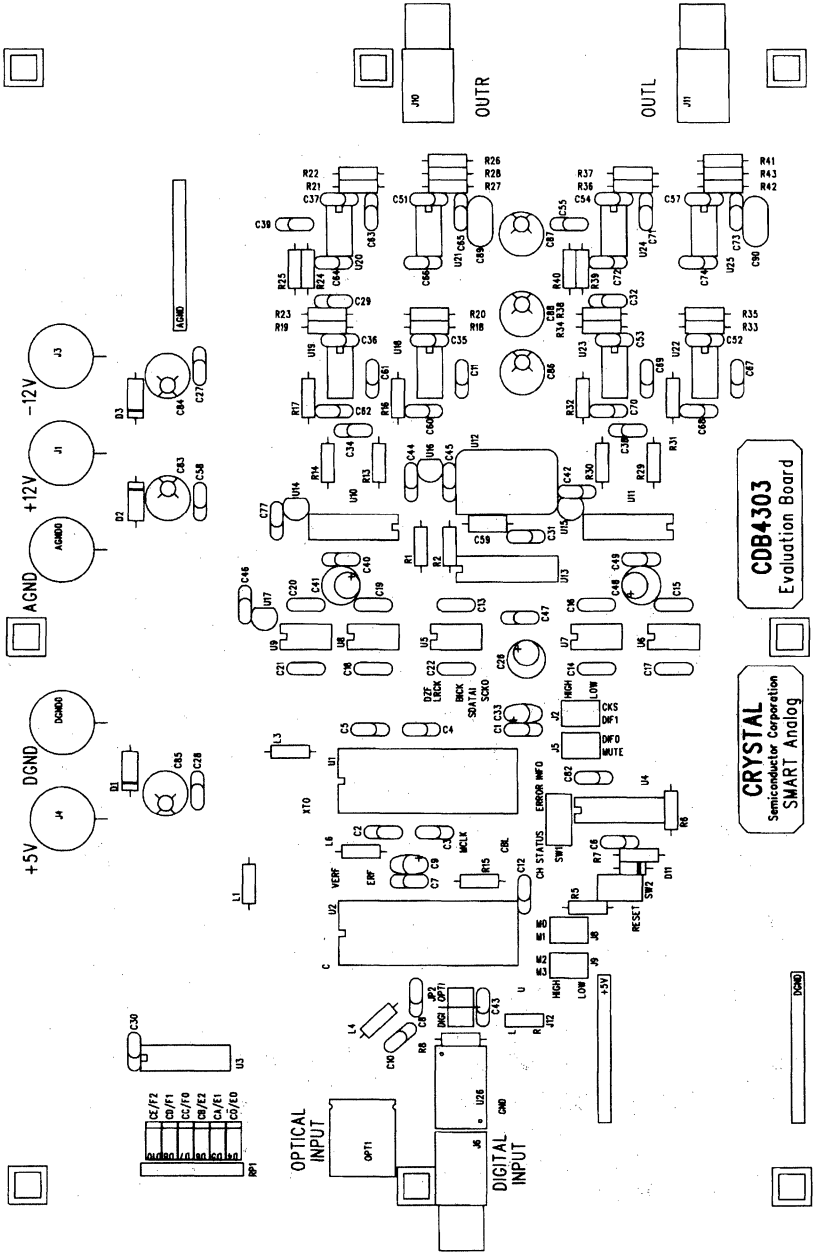


Figure 7. CDB4303 Rev. B. Silk Screen Side

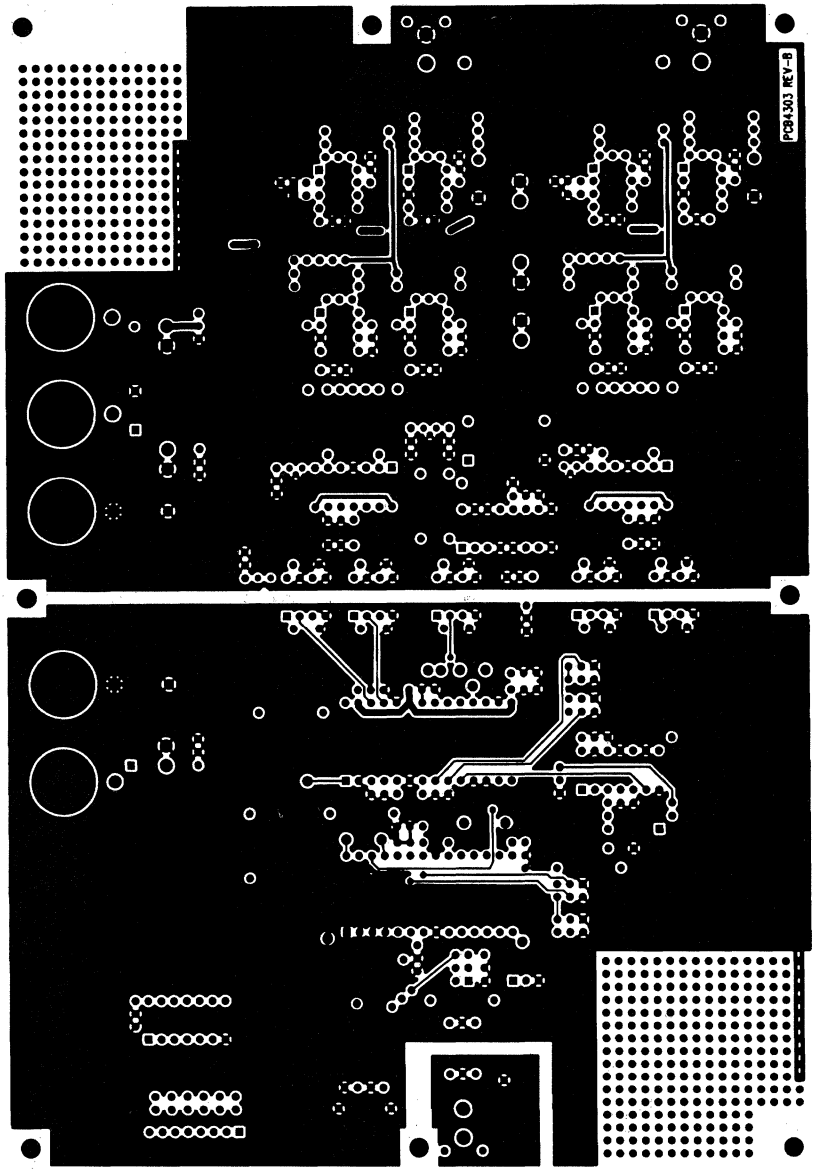


Figure 8. CDB4303 Rev. B. Component Side

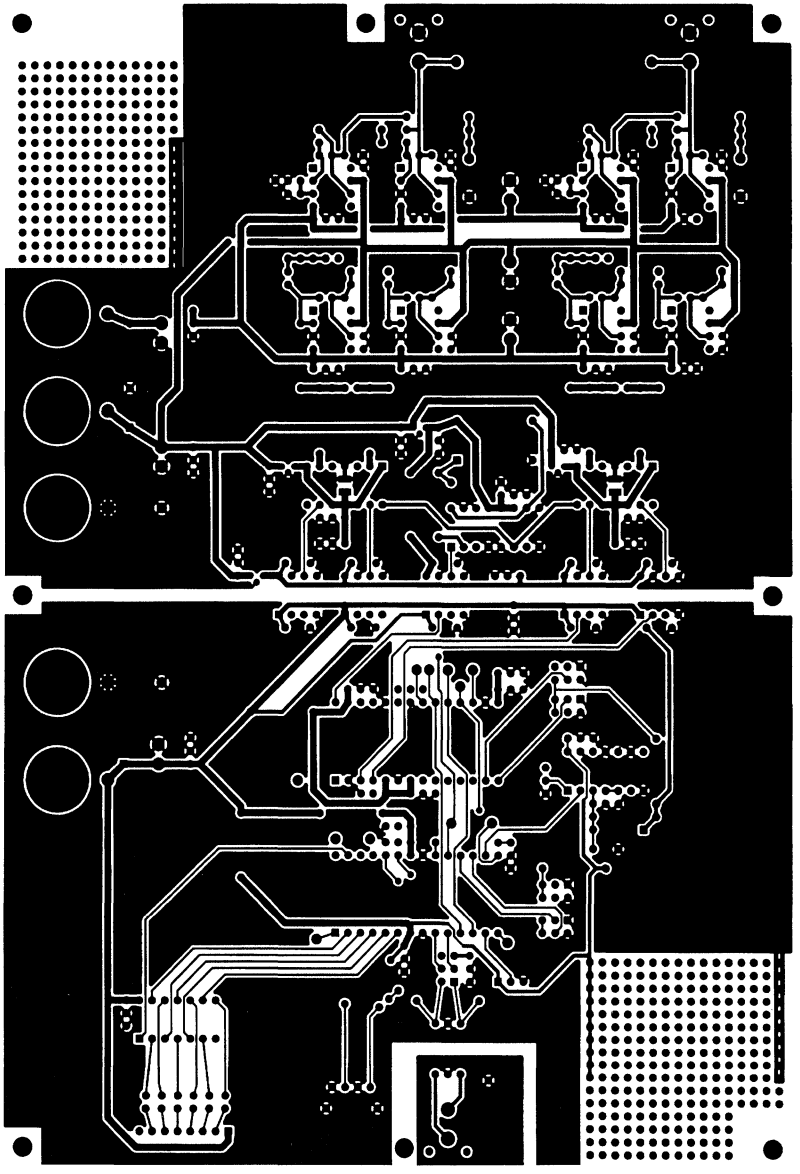


Figure 9. CDB4303 Rev. B. Solder Side

• Notes •

Semiconductor Corporation

CS4328

18-Bit, Stereo D/A Converter for Digital Audio

2

Features

- Complete Stereo DAC System
  - 8× Interpolation Filter
  - 64× Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1kHz & 48kHz
- 120 dB Signal-to-Noise Ratio
- Low Clock Jitter Sensitivity
- Completely Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
  - No External Components Needed
- Flexible Serial Interface for Either 16 or 18 bit Input Data

General Description

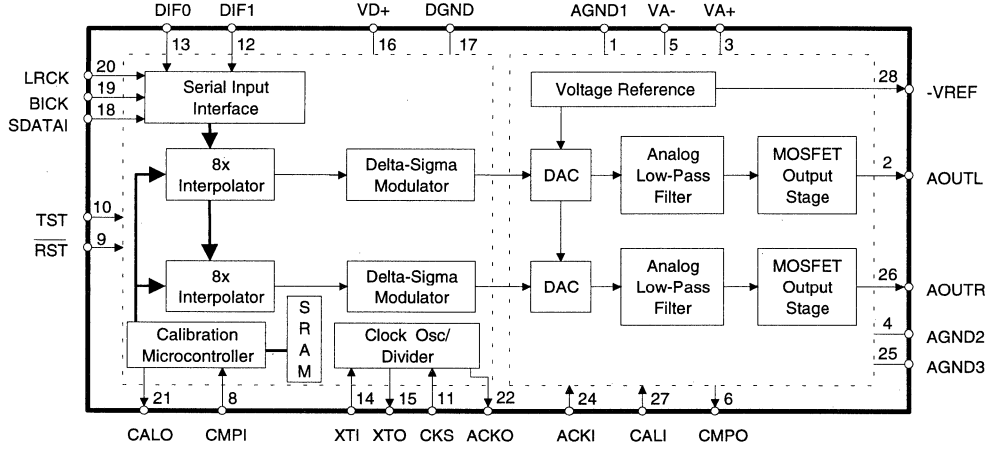
The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8× digital interpolation filter followed by a 64× oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

The master clock can be either 256 or 384 times the input word rate, supporting various audio environments.

ORDERING INFORMATION:

CS4328-KP	0 to 70 °C	28-pin Plastic DIP
CS4328-KS	0 to 70 °C	28-pin Plastic SOIC
CS4328-BP	-40 to +85 °C	28-pin Plastic DIP
CS4328-BS	-40 to +85 °C	28-pin Plastic SOIC
CDB4328	CS4328 Evaluation Board	



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C for K grade, T_A = -40 to +85 °C for B grade; VA+,VD+ = 5V; VA- = -5V; Logic "1" = VD+; Logic "0" = DGND; Full-Scale Output Sinewave, 991 Hz; Input Word Rate = 48 kHz; Input Data = 18 Bits; BICK = 3.072 MHz; R_L = 10kΩ; Measurement Bandwidth is 10 Hz to 20 kHz, unweighted; unless otherwise specified.)

Parameter*	Symbol	CS4328-K Min	CS4328-K Typ	CS4328-K Max	CS4328-B Min	CS4328-B Typ	CS4328-B Max	Units
Specified Temperature Range	T_A	0		+70	-40		+85	°C
Resolution		16	-	-	16	-	-	Bits
Dynamic Performance								
Signal-to-Noise Ratio (A-weighted) (Note 1)	SNR	120	-	-	120	-	-	dB
Total Harmonic Distortion + Noise (A-Weighted)	THD+N							
0 dB Output,		-	-93	-90	-	-88	-85	dB
-20 dB Output,		-	-77	-73	-	-75	-70	dB
-60 dB Output,		-	-37	-33	-	-35	-30	dB
Deviation From Linear Phase (Note 2)	-	-	± 0.5	-	-	± 0.5	-	deg
Passband: to -3 dB corner (Notes 3, 4)	-	0	to	23.5	0	to	23.5	kHz
to 0.00025 dB corner (Notes 3, 4)		0	to	21.6	0	to	21.6	kHz
Frequency Response 10 Hz to 20 kHz (Note 2)	-	-0.05	+0.1	+0.2	-0.05	+0.1	+0.2	dB
Passband Ripple (Note 4)	-	-	-	0.00025	-	-	0.00025	dB
StopBand (Note 3)	-	26.4	-	-	26.4	-	-	kHz
StopBand Attenuation (Note 2)	-	90	-	-	90	-	-	dB
Group Delay (IWR = Input Word Rate)	tgd	-	33/IWR	-	-	33/IWR	-	s
Interchannel Isolation (1 kHz)	-	-100	-110	-	-95	-105	-	dB
dc Accuracy								
Interchannel Gain Mismatch	-	-	0.1	-	-	0.1	-	dB
Gain Error	-	-	-	± 5	-	-	± 5	%
Gain Drift	-	-	150	-	-	150	-	ppm/°C
Offset Error (after calibration)	-	-	-	± 1	-	-	± 1	mV
Analog Output								
Full Scale Output Voltage	VOUT	3.8	4.0	4.2	3.8	4.0	4.2	Vpp
Power Supplies								
Power Supply Current: VA+	IA+	-	40	55	-	40	55	mA
VA-	IA-	-	-40	-55	-	-40	-55	mA
VD+	ID+	-	50	60	-	50	60	mA
Power Dissipation	-	-	650	850	-	650	850	mW
Power Supply Rejection Ratio (1 kHz)	PSRR	-	50	-	-	50	-	dB

Notes:
1. Idle channel, digital input all zeros.
2. Combined digital and analog filter characteristics.
3. The passband and stopband edges scale with frequency. For input word rates, IWR, other than 48 kHz, the 0.00025 dB passband edge is 0.45×IWR and the stopband edge is 0.55×IWR.
4. Digital filter characteristics.

* Definitions are at the end of this data sheet. Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS

(TA = 25 °C; VA+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30%VD+	V
High-Level Output Voltage at Io = -20µA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20µA	V_{OL}	-	-	0.1	V
Input Leakage Current (Note 5)	I_{in}	-	-	1.0	µA

Note: 5. TST, DIF0 & DIF1 have internal pull-down devices, nominally 90kΩ.

ABSOLUTE MAXIMUM RATINGS (AGND1-3, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	Negative Analog	VA-	0.3	-6.0	V
	|VA+ - VD+|		-	0.4	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD+)+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND1, AGND2, AGND3, DGND = 0V; all voltages with respect to ground)

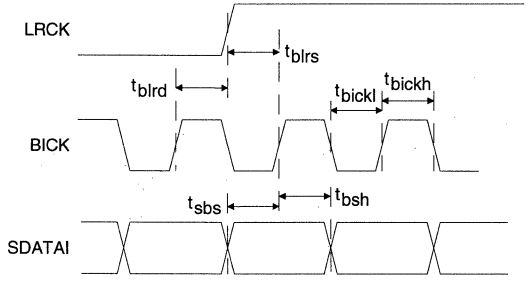
Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	|VA+ - VD+|		-	-	0.4	V

SWITCHING CHARACTERISTICS

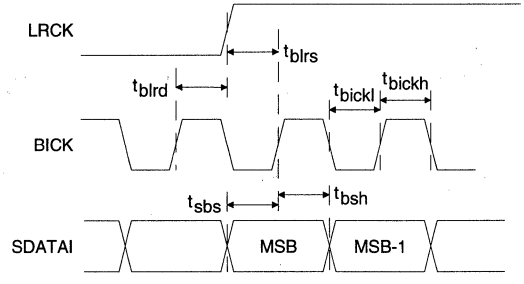
(T_A = 25 °C; VA+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency using Internal Oscillator:					
CKS=H	XTI/XTO	10.7	-	19.2	MHz
CKS=L	-	7.1	-	13.9	MHz
Master Clock Frequency using External Clock:					
CKS=H	XTI/XTO	0.384	-	19.2	MHz
CKS=L	-	0.256	-	13.9	MHz
XTI/XTO Pulse Width Low	-	21	-	-	ns
XTI/XTO Pulse Width High	-	21	-	-	ns
BICK Pulse Width Low	t_{bickl}	30	-	-	ns
BICK Pulse Width High	t_{bickh}	30	-	-	ns
BICK Period	t_{bickw}	80	-	-	ns
BICK rising to LRCK edge delay (Note 6)	t_{blrd}	35	-	-	ns
BICK rising to LRCK edge setup time (Note 6)	t_{blrs}	35	-	-	ns
SDATAI valid to BICK rising setup time (Note 6)	t_{sbs}	35	-	-	ns
BICK rising to SDATAI hold time (Note 6)	t_{bsh}	35	-	-	ns
$\overline{RST}$ Minimum Pulse Width Low	2 periods of XTI/XTO				

Note: 6. "BICK rising" refers to modes 0, 1, and 3. For mode 2, replace "BICK rising" with "BICK falling."



Serial Input Timing (Modes 0, 1, &3)



Serial Input Timing (Mode 2)

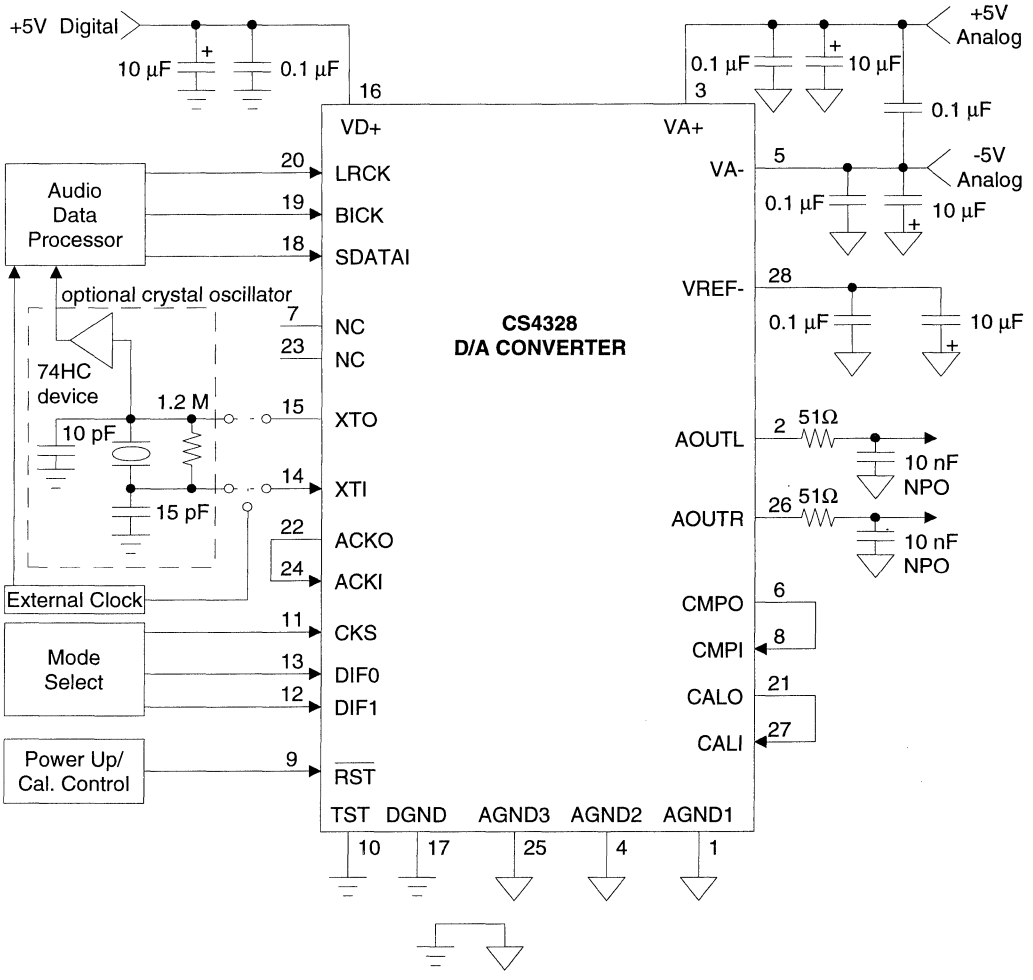


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS4328 is a complete stereo digital-to-analog system designed for digital audio. The system accepts data at standard audio frequencies, such as 48 kHz, 44.1 kHz, and 32 kHz; and produces line-level outputs.

The architecture includes an 8× oversampling filter followed by a 64× oversampled one-bit delta-sigma modulator. The output from the one bit modulator controls the polarity of a reference voltage which is then passed through an ultra-linear analog low-pass filter. The result is line-level outputs with no need for further filtering.

SYSTEM DESIGN

Very few external components are required to support the DAC. Normal power supply decoupling components and voltage reference bypass capacitors are all that's required.

System Clock Input

The master clock (XTI/XTO) input to the DAC is used to operate the digital interpolation filter and the delta-sigma modulator. The master clock can be either a crystal placed across the XTI and XTO pins, or an external clock input to the XTI pin with the XTO pin left floating.

The frequency of XTI/XTO is determined by the desired Input Word Rate, IWR, and the setting of the Clock Select pin, CKS. IWR is the frequency at which words for each channel are input to the DAC and is equal to LRCK frequency. Setting CKS low selects an XTI/XTO frequency of 256× IWR while setting CKS high selects 384× IWR. The ACKO pin will always be 128× IWR and is used by the analog low-pass smoothing filter. Table 1 illustrates various audio word rates and corresponding frequencies used in the DAC.

LRCK (kHz)	CKS	XTI/XTO (MHz)	ACKO (MHz)
32	low	8.192	4.096
32	high	12.288	4.096
44.1	low	11.2896	5.6448
44.1	high	16.9344	5.6448
48	low	12.288	6.144
48	high	18.432	6.144

Table 1. Common Clock Frequencies

The remaining system clocks, LRCK and BICK, must be synchronously derived from XTI/XTO. If the CS4328 internal oscillator is used, the circuit must be configured and XTO buffered as shown in Figure 1. XTI/XTO can be divided to produce LRCK and BICK using a synchronous counter such as 74HC590. Notice that the value of the capacitor on XTO is 10 pF and the XTI capacitor is 15 pF, which allows for 5 pF of gate and stray capacitance.

It is also possible to divide ACKO, 128× IWR, to derive BICK and LRCK. However, external circuitry must be used to apply a "kick-start" pulse to LRCK in order to activate ACKO. The sequence for the cancellation of RESET, beginning of calibration and activation of ACKO is shown in Figure 2 with the required transitions indicated by arrows. A momentary loss of XTI/XTO or power will require a "kick-start" pulse to resume operation.

Serial Data Interface

Data is input to the CS4328 via three serial input pins; SDATAI is the serial data input, BICK is the serial data clock and LRCK defines the channel and delineation of data. The DAC supports four serial data formats which are selected via the digital input format pins DIF0 and DIF1. The different formats control the relationship of LRCK to SDATAI and the edge of BICK used to

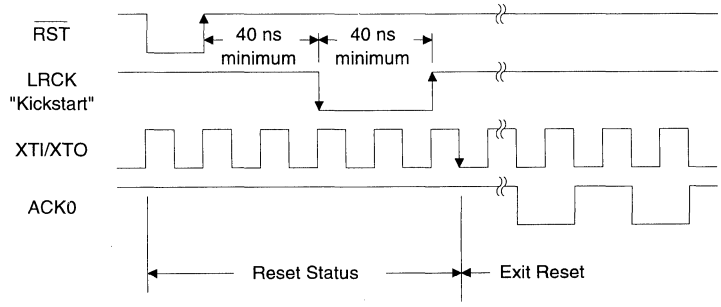


Figure 2. RESET Cancellation Timing

latch data. Table 2 lists the four formats, along with the associated figure number. Format 0 is compatible with existing 16-bit D/A converters and digital filters. Format 1 is an 18-bit version of format 0. Format 2 is similar to Crystal ADCs and many DSP serial ports. Format 3 is compatible with the I^2S serial data protocol. Formats 2 and 3 support 18-bit input or 16-bit followed by two zeros. In all four serial input modes, the serial data is MSB-first and 2's-complement format.

Formats 0, 2 and 3 will operate with 16-bit data and 16 BICK pulses as well. See Figure 6 for 16-bit timing. However, the use of BICK = 64× IWR is recommended to minimize the possibility of performance degradation resulting from BICK coupling into VREF-.

DIF1	DIF0	Mode	Figure
0	0	0	3
0	1	1	3
1	0	2	4
1	1	3	5

Table 2. Digital Input Formats

Reset and Offset Calibration

$\overline{RST}$ is an active low signal that resets the digital filter and the delta-sigma modulator, synchronizes LRCK with internal control signals and starts an offset calibration cycle upon exiting reset. When $\overline{RST}$ goes low, CALO goes high and stays high until the end of an offset calibration cycle. An offset calibration cycle takes 1024 IWR cycles to complete. CALO must be connected to CALI and CMPO must be connected to CMPI for offset calibration. During an offset calibration the analog output is forced to zero.

Power-Up Considerations

Upon initial application of power to the DAC, offset calibration and digital filter registers will be indeterminate. $\overline{RST}$ should be low during power-up to activate an internal mute and prevent this erroneous information from being output from the DAC. Bringing $\overline{RST}$ high will begin a calibration cycle and initialize these registers.

Muting

There are two types of mutes that can be implemented with the CS4328. The first is a -50 dB

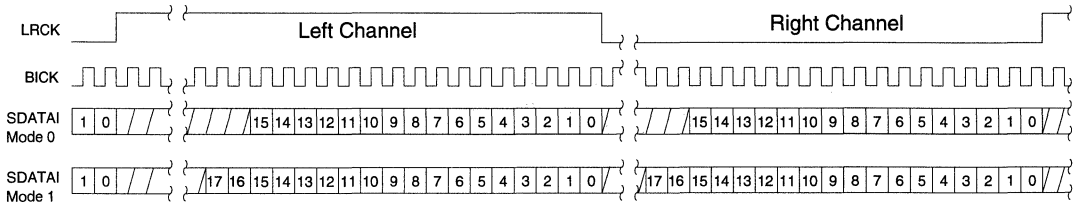


Figure 3. Digital Input Formats 0 & 1

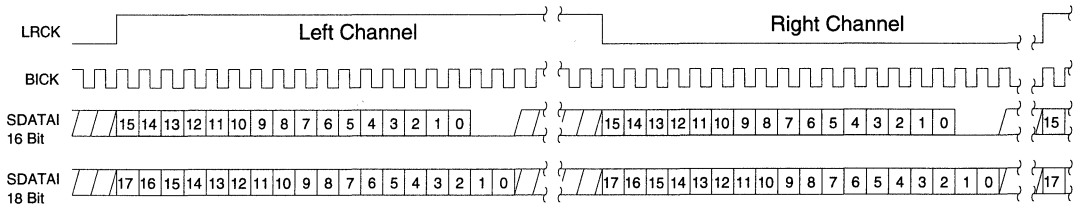


Figure 4. Digital Input Format 2

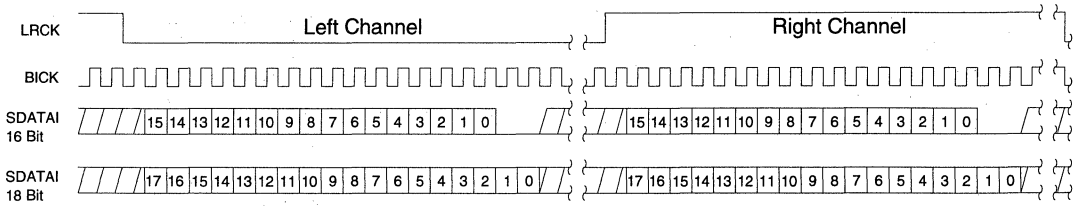


Figure 5. Digital Input Format 3

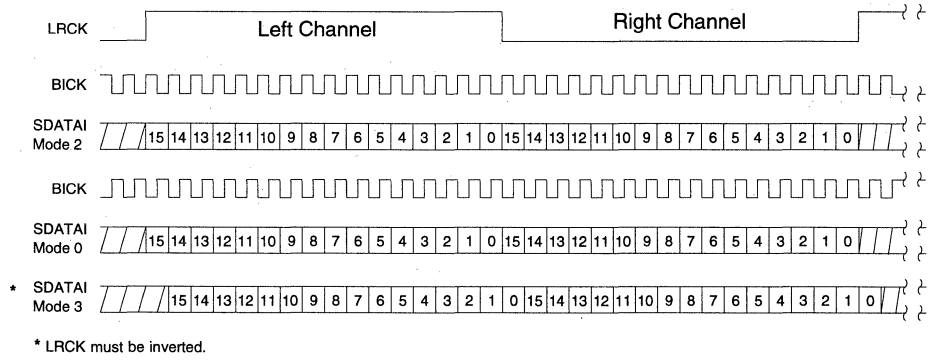


Figure 6. Digital Input Formats 0, 2 and 3 with 16 BICK Periods

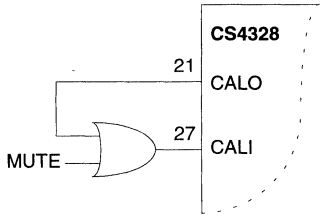


Figure 7. -50dB Muting

mute which can be activated by forcing the CALI pin high. Figure 7 shows how to implement a -50 dB mute using an OR gate. The propagation of the gate will be the only delay in moving the CS4328 to a muted state.

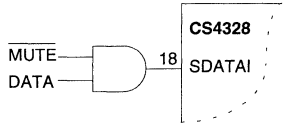


Figure 8. -120 dB Muting

The second mute option is a two stage operation which involves forcing SDATAI to 0 using an AND gate as shown in Figure 8. The first mute occurs following 33 LRCK cycles when the 0 input data propagates to the output of the DAC. The rms noise present at the output will typically be 93 dB below fullscale. Following a total of 4096 LRCK cycles with 0 input data the output of the CS4328 will mute and lower the output rms noise to a minimum of 120 dB below fullscale. Upon release of the MUTE command and non-zero input data the CS4328 output mute will immediately release. However, 33 LRCK cycles are required for input data to propagate to the output of the CS4328.

Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4328 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply and VA- connected to a clean -5 volt supply. VD+, which powers the digital interpolation filter and delta-sigma modulator, may be powered from the system +5 volt logic supply. Decoupling capacitors should be located as near to the CS4328 as possible.

The printed circuit board layout should have separate analog and digital regions with individual ground planes. The CS4328 should straddle the ground plane break as shown on the CDB4328 Evaluation board. Optional jumpers for connecting these planes should be included near the DAC, where power is brought on to the board and near the regulators. All signals, especially clocks, should be kept away from the VREF- pin to avoid unwanted coupling into the CS4328. The VREF- decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF- to Pin 1 AGND and to minimize the path between VREF- and the capacitors. Extensive use of ground plane fill on both the analog and digital sections of the circuit board will yield large reductions in radiated noise effects. An application note "*Layout and Design Rules for Data Converters*" is printed in the Application Note section of this book.

Analog Output and Filtering

Full scale analog output for each channel is typically 4V peak-to-peak. The analog outputs can drive load impedances as low as 600Ω and are short-circuit protected to 20mA.

The CS4328 analog filter is a 5th order switched-capacitor filter followed by a second-order continuous-time filter. The switched-capacitor filter is clock dependent and will scale with the IWR frequency. The continuous-time filter is fixed and not related to IWR. A low-pass filter consisting of a 51Ω resistor and a .01 µF NPO capacitor is recommended on the analog outputs.

Performance Plots

The following collection of CS4328 measurement plots (IWR = 48 kHz) were taken with an Audio Precision Dual Domain System One. All FFT plots are 16,384 point.

Figure 9 shows the **frequency response** with a 48 kHz input word rate. The response is very flat out to half the input word rate.

Figure 10 shows the **muted noise** with all zeros data into the CS4328. This plot is dominated by the noise floor of the System One.

Figure 11 shows the **unmuted noise**. This data was taken by feeding the CS4328 continuous zeros, but pulling CALI low. This unmutes the output stage of the CS4328. This plot shows the noise shaping characteristics of the delta-sigma modulator combined with the analog filter.

Figure 12 shows the A-weighted **THD+N vs signal amplitude** for a dithered 1kHz input signal. Notice that there is no increase in distortion as the signal level decreases. This indicates very good low-level linearity, one of the key benefits of the delta-sigma technique.

Figure 13 shows the **fade-to-noise linearity** test result using track 20 of the CBS CD-1. The input test signal is a dithered 500 Hz sine wave which gradually fades from -60 dB level to -120 dB. During the fading, the output level from the CS4328 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs of -90 dB. The gradual shift of the plot away from zero at signal levels < -100 dB is caused by the background noise starting to dominate the measurement.

Figure 14 shows the **impulse response**, taken from the single positive full scale value on track 17 of the CD-1 test disk. Notice the high degree of symmetry, indicating good phase linearity.

Figure 15 shows a 16K **FFT plot result, with a 1 kHz -90 dB dithered input**. Notice the complete lack of distortion components and tones.

Figure 16 shows a bandlimited, 10 Hz to 22 kHz, **time domain plot** of the CS4328 output with a **1 kHz, -90 dB dithered** input. Notice the clear residual sine wave shape, in the presence of noise.

Figure 17 shows the **monotonicity test** result plot. The input data to the CS4328 is +1 LSB, -1 LSB four times, then +2 LSB, -2 LSB four times and so on, until +10 LSB, -10 LSB. This data pattern is taken from track 21 of the CD-1 test disk. Notice the increasing staircase envelope, with no decreasing elements. Notice also the clear resolution of the LSB. For this test, one LSB is a 16-bit LSB.

The following tests were done by filtering the analog output of the CS4328 with the System One analyzer 1 kHz notch filter to reduce the peak signal level. The resulting signal was then amplified and applied to the DSP module, avoiding distortion in the System One A/D converter.

Figure 18 shows a **16K FFT Plot with a 1 kHz, 0 dB** input. Notice the low order harmonic distortion at < -100 dB.

Figure 19 shows a **16K FFT Plot with a 1 kHz, -10 dB** input. Notice the almost complete absence of distortion, with a small residual 2nd harmonic at -110 dB.

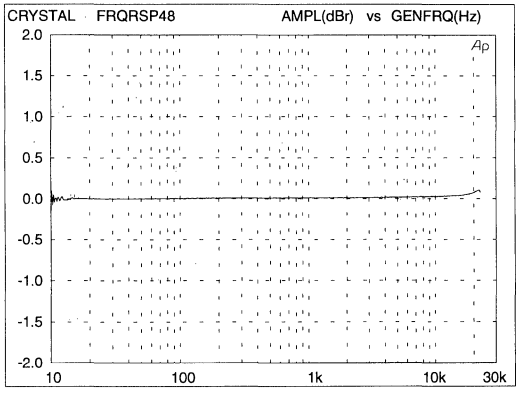


Figure 9. Frequency Response (48 kHz word rate)

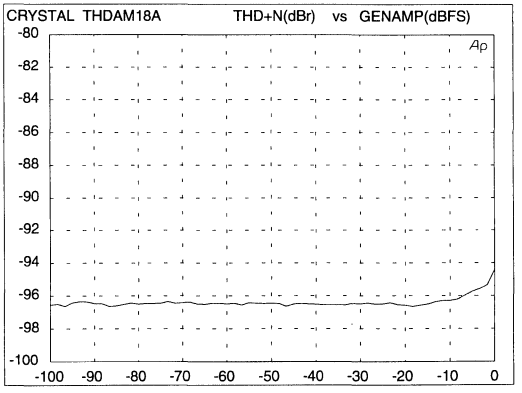


Figure 12. THD+N vs 18-bit Input Signal Level

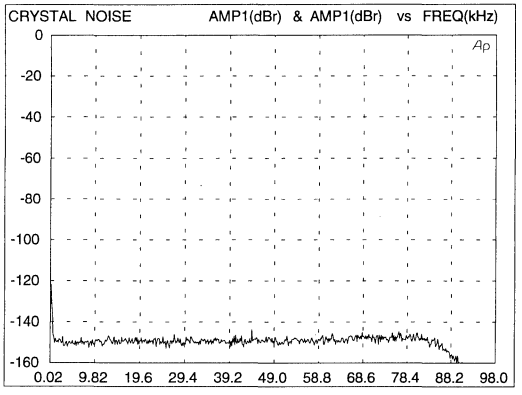


Figure 10. Muted Idle Channel Noise

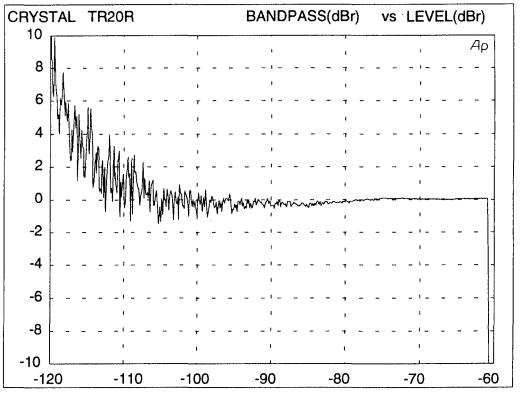


Figure 13. Fade-to-Noise Linearity

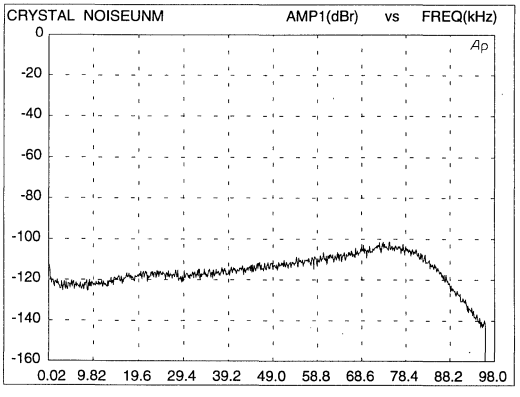


Figure 11. Unmuted Idle Noise

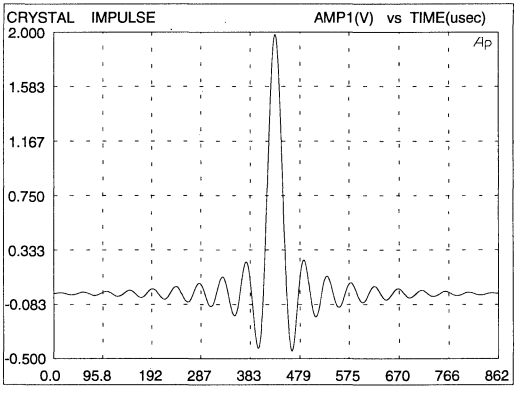


Figure 14. Impulse Response

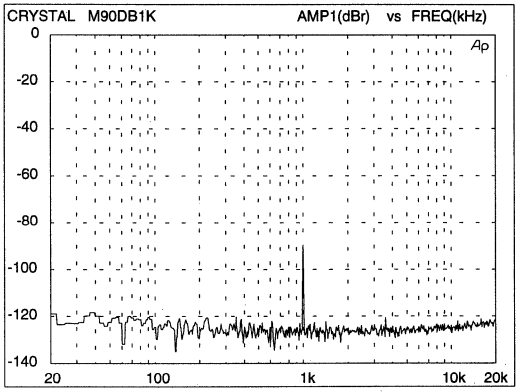


Figure 15. 1 kHz, -90 dB Input FFT Plot

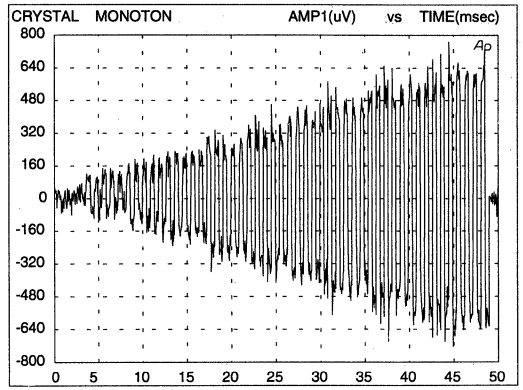


Figure 17. Monotonicity Test (16-bit data)

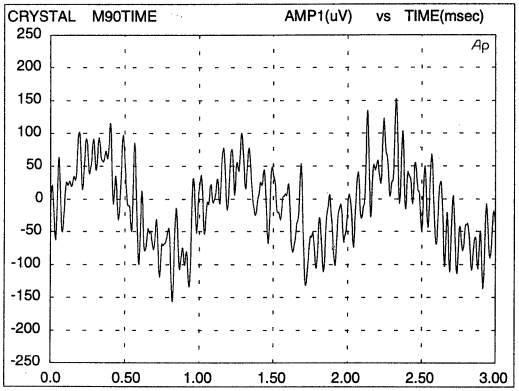


Figure 16. 1 kHz, -90 dB Input Time Domain Plot

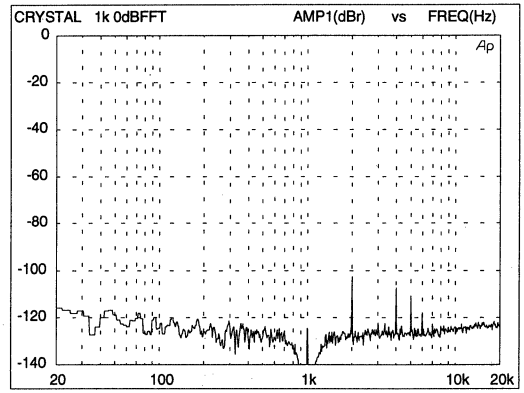


Figure 18. 1 kHz, 0 dB Input FFT Plot

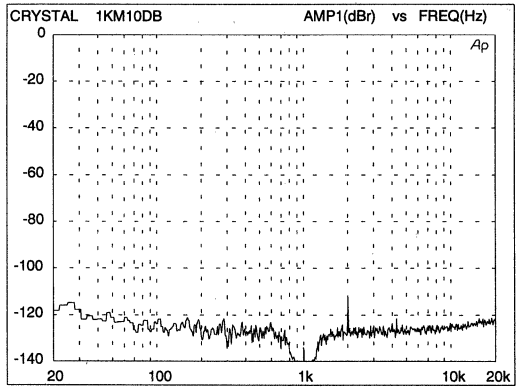


Figure 19. 1 kHz, -10 dB Input FFT Plot

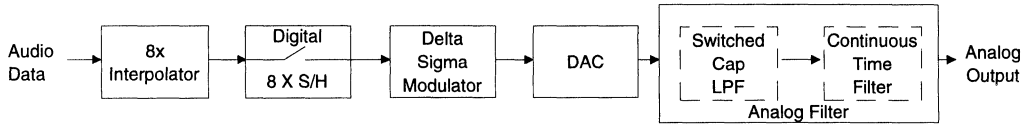


Figure 20. CS4328 Architecture

THEORY OF OPERATION

The CS4328 architecture can be considered in five blocks: Interpolation, sample/hold, delta-sigma modulation, D/A conversion, and analog filtering.

Audio data is input to the CS4328 digital interpolation filter which removes images of the input signal that are present at multiples of the input sample frequency, Fs (Figure 21). Following the interpolation stage, the resulting frequency spectrum has images of the input signal at multiples of eight times the input sample frequency, 8× Fs (Figure 22). Eliminating the images between Fs and 8× Fs greatly relaxes the requirements of the analog filtering, allowing the suppression of images while leaving the audio band of interest unaltered.

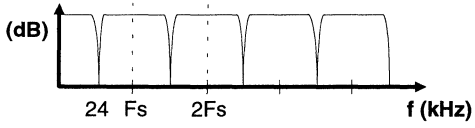


Figure 21. Input Data Spectrum

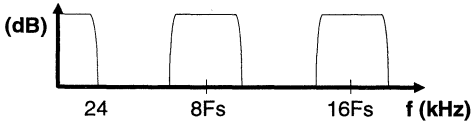


Figure 22. 8X Interpolated Data Spectrum

The CS4328 interpolation stage is followed by a sample-and-hold function where the data points from the interpolator are held for eight (64× Fs) clock cycles. The resulting frequency response is a sinx/x characteristic with zeros at 8× Fs multiples. The sinx/x zeros completely attenuate signals at 8× Fs and largely suppress the remaining energy of the images (Figure 23). The 8× interpolation followed by the 8× sample-and-

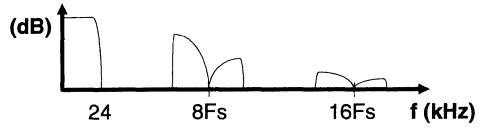


Figure 23. Spectrum After S/H

hold results in data at a rate of 64× Fs.

The delta-sigma modulator takes in the 64× Fs data (3.072 MHz for 48kHz sampled systems) and performs fifth-order noise shaping. In the digital modulator of the CS4328, 18-bit audio data is modulated to a 1-bit, 64× Fs signal. The 5th-order noise shaper allows 1-bit quantization to support 18-bit audio processing by suppressing quantization noise in the bandwidth of

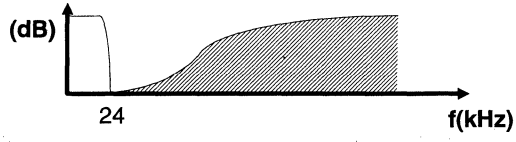


Figure 24. Modulator Output Spectrum

interest. Figure 24 shows the frequency spectrum of the modulator output.

The CS4328's digital modulator is followed by a D-to-A converter that translates the 1-bit signal into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched

capacitor, where the polarity of each packet is controlled by the 1-bit signal. The result is a 1-bit D/A conversion process that is very insensitive to clock jitter. This is a major improvement over previous generations of 1-Bit D/A converters where the magnitude of charge in the D/A process is determined by switching a current reference for a period of time defined by periods of the master clock.

The final stage of the CS4328 is made up of a 5th order switched-capacitor low pass filter and a 2nd order continuous time filter. The switched-capacitor filter eliminates out-of-band energy resulting from the noise shaping process (Figure 25). The switched-capacitor stage scales with the master clock signal being applied to the CS4328. The final stage is a 2nd order continuous time filter that eliminates high frequency energy that appears at multiples of the 64× Fs sample rate (Figure 26).

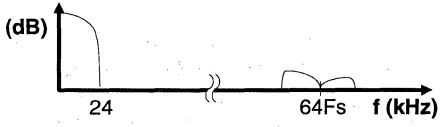


Figure 25. Spectrum After Switched-Capacitor Filter

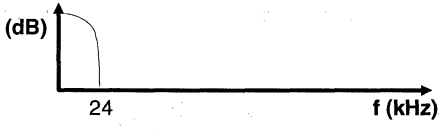


Figure 26. Spectrum After Continuous Time Filter

Figures 27-30 are computer simulations of the combined response of the CS4328 digital and analog filters with an input word rate of 48 kHz.

Figure 27 shows the individual and combined phase response of the CS4328 filters. Notice the digital filter equalization of the analog filter to produce a linear phase response.

Figures 28-30 are plots of the CS4328 magnitude response.

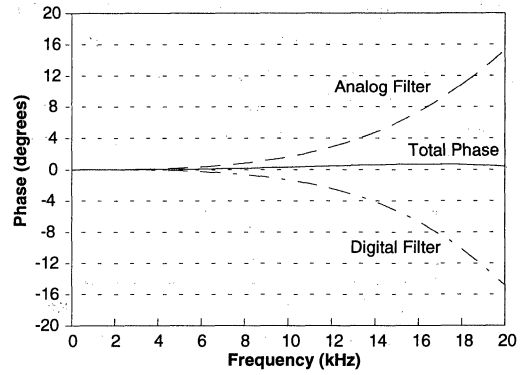


Figure 27. Deviation From Linear Phase

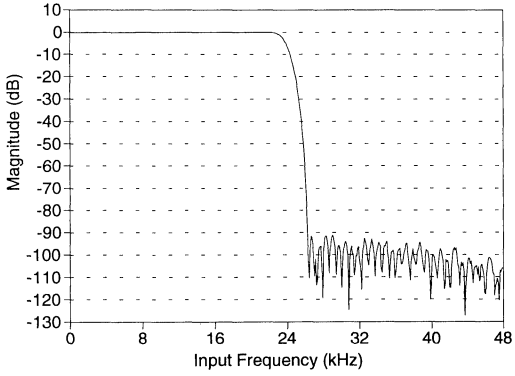


Figure 28. Combined Digital and Analog Filter Frequency Response

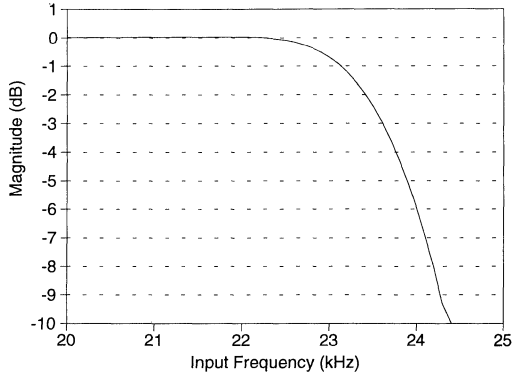


Figure 29. Combined Digital and Analog Filter Frequency Response

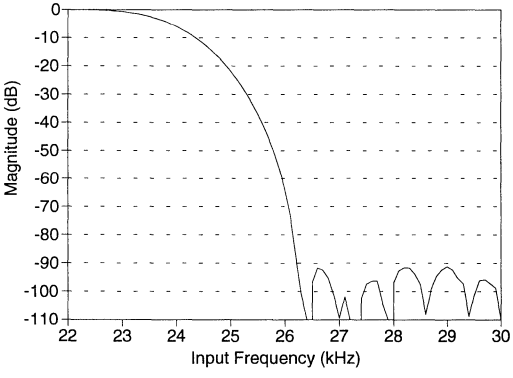
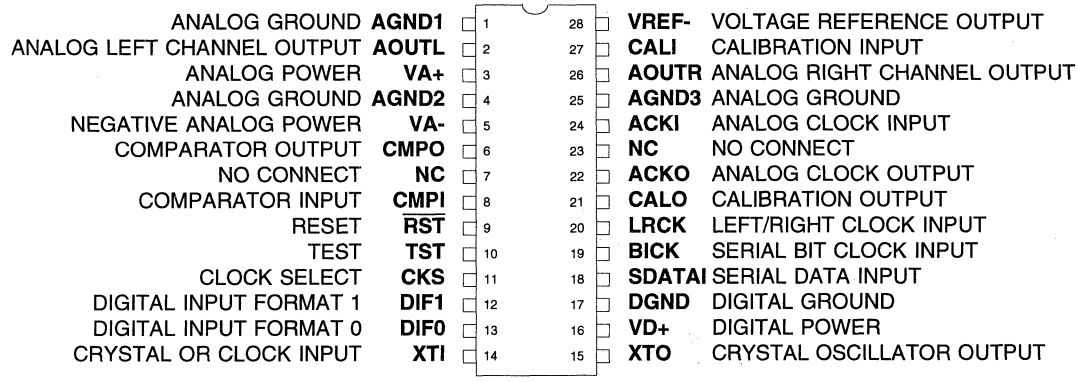


Figure 30. Combined Digital and Analog Filter Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 3.
Positive analog supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND1, AGND2, AGND3 - Analog Grounds, PINS 1, 4, 25.
Analog ground reference.

VD+ - Positive Digital Power, PIN 16.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 17.
Digital ground for the digital section.

Analog Outputs

VREF- - Voltage Reference Output, PIN 28.
Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

AOUTL - Analog Left Channel Output, PIN 2.
Analog output for the left channel. Typically 4V peak-to-peak for a full-scale input signal.

AOUTR - Analog Right Channel Output, PIN 26.
Analog output for the right channel. Typically 4V peak-to-peak for a full-scale input signal.

Digital Inputs

XTI - Crystal or Clock Input, PIN 14.

A crystal oscillator can be connected between this pin and XTO, or an external CMOS clock can be input on XTI. The frequency must be either 256× or 384× the input word rate based on the clock select pin, CKS.

ACKI - Analog Clock Input, PIN 24.

This is the master clock input for the analog section of the chip and must be 128× the input word rate. ACKI is typically connected to the Analog Clock Ouput pin, ACKO.

CALI - Calibration Input, PIN 27.

Input to the analog section that is used during offset calibration. Normally connected to the Calibration Output pin, CALO.

CMPI - Comparator Input, PIN 8

Input to the digital section that is used during offset calibration. Normally connected to the Comparator Output pin, CMPO.

LRCK - Left/Right Clock, PIN 20.

This input determines which channel is currently being input on the Serial Data Input pin, SDATAI. The format of LRCK is controlled by DIF0 and DIF1.

BICK - Serial Bit Input Clock, PIN19.

Clocks the individual bits of the serial data in from the SDATAI pin. The edge used to latch SDATAI is controlled by DIF0 and DIF1.

SDATAI - Serial Data Input, PIN 18.

Two's complement MSB-first serial data of either 16 or 18 bits is input on this pin. The data is clocked into the CS4328 via the BICK clock and the channel is determined by the LRCK clock. The format for the previous two clocks is determined by the Digital Input Format pins, DIF0 and DIF1

DIF0,DIF1 - Digital Input Format, PINS 13, 12

These two pins select one of four formats for the incoming serial data stream. These pins set the format of the BICK and LRCK clocks with respect to SDATAI. The formats are listed in Table 2.

CKS - Clock Speed Select, PIN 11.

Selects the clock frequency input on the XTI pin. CKS low selects 256× the input word rate (LRCK frequency) while CKS high selects 384×.

$\overline{\text{RST}}$ - Reset and Calibrate, PIN 9.

When reset is low the filters and modulators are held in reset. When reset goes high, an offset calibration is initiated.

Digital Outputs

XTO - Crystal Oscillator Output, PIN 15.

When a crystal oscillator is used, it is tied between this pin and XTI. When an external clock is input, this pin should be left floating.

ACKO - Analog Clock Output, PIN 22.

This output is 128× the input word rate (LRCK frequency). Normally connected to the Analog Clock Input pin, ACKI.

CALO - Calibration Output, PIN 21.

Used during offset calibration. Must be connected to the Calibration Input pin, CALI.

CMPO - Comparator Output, PIN 6.

Used during offset calibration. Must be connected to the Comparator Input pin, CMPI.

Miscellaneous

NC - No Connection, PINS 7, 23.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 10.

Allows access to the CS4328 test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Signal-to-Noise Ratio - The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth with an input of all zeros.

Frequency Response - A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (AGND). Units in mV.

Semiconductor Corporation

CDB4328

CS4328 Evaluation Board

Features

- Demonstrates recommended layout and grounding arrangements
- CS4328 Supports multiple input formats
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Operation with on-board CS8412 or externally supplied system timing

General Description

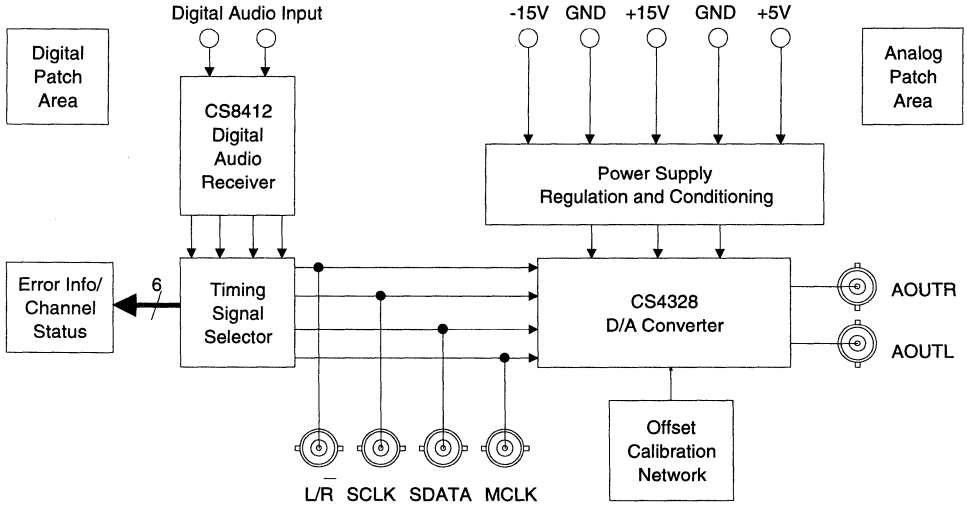
The CDB4328 evaluation board allows fast evaluation of the CS4328 18-bit, stereo D/A converter. The board provides an analog output interface via BNC connectors for both channels. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply.

Also included is a CS8412 digital audio receiver I.C., which will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The CS8412 can provide the system timing necessary to operate the CS4328.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION: CDB4328

Block Diagram



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Power Supply Circuitry

Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The ±5 V analog power supply inputs of the converter are derived from ± 15 V using the voltage regulators U5 and U6. The +5 V digital supply for the converter and the discrete logic on the board is provided by the +5 V and DGND binding posts. D1, D2, and D3 are transient suppressors which also provide protection from incorrectly connected power supply leads. C1-C8 provide general power supply filtering for the analog supplies. As shown in Figure 2, C20-C24 provide localized decoupling for the converter VA+ and VA- pins. Note that C22 is connected between VA- and VA+ and not VA- and AGND. The evaluation board uses both an analog and a digital ground plane which are connected at J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

Offset Calibration & Reset Circuitry

Figure 1, shows the offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Digital to Analog Converter's $\overline{RST}$ pin initiating an offset calibration cycle. Pressing and releasing S2 also initiates an offset calibration cycle.

Serial Data Interface

Figure 1 shows that there are two options for inputing serial data into the CS4328. Serial data can be provided via the SDATA BNC connector on the evaluation board. BNC connectors for SCLK, the serial data input clock, and L/$\overline{R}$, the clock that defines the channel and delineates the data, are also provided on the evaluation board. This information can also be provided by the on-board CS8412. JP3 selects the source of SDATA, SCLK, and L/$\overline{R}$ that will be provided to the converter. JP3 selections are shown in Table 1.

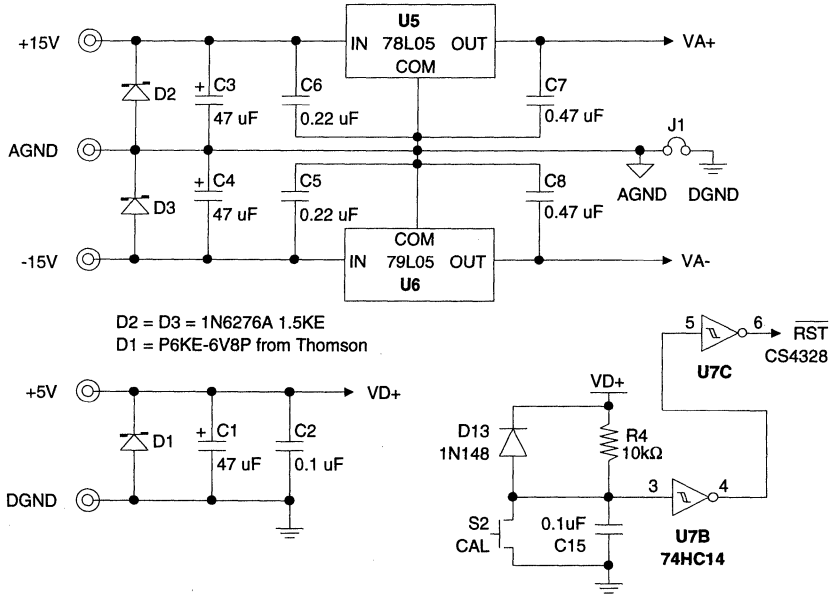


Figure 1. Power Supply and Reset Circuitry

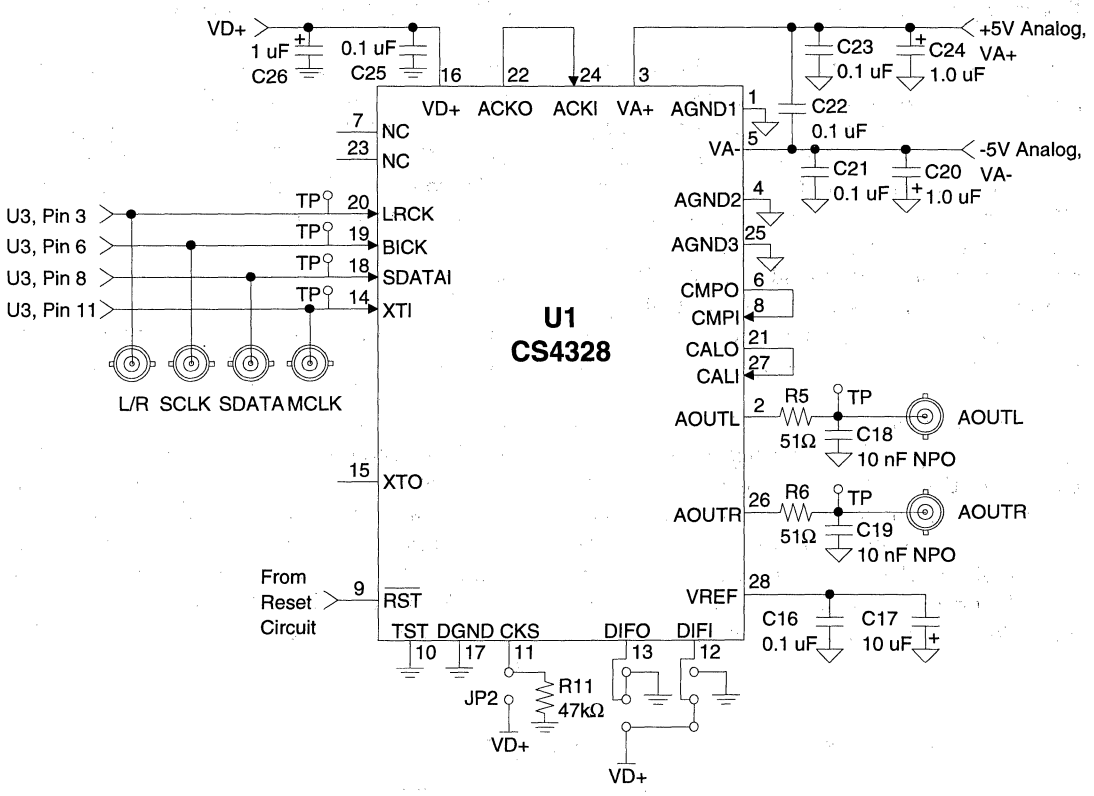


Figure 2. CS4328 DAC Connections

The CS4328 supports four serial data input formats. The selection of which is made via the digital input format pins DIF0 and DIF1. The different formats control the relationship of L/$\overline{R}$ to SDATA and the edge of SCLK used to latch the data. Consult the CS4328 data sheet for an explanation of the different formats.

Position	Input Option Selected
EXT CLK	SDATA,SCLK, L/$\overline{R}$ provided by an external source.
8412	SDATA,SCLK, L/$\overline{R}$ provided by the CS8412

Table 1. JP3 Selectable Options

System Timing

The master clock input to the CS4328 can be provided by several sources. JP3 selects the source of the master clock that is to be supplied to the XTI pin of the converter. When EXT CLK is selected, the master clock is provided by one of two sources. The 12.288 MHz clock signal provided by U8 can be used as the master clock for both the CS4328 and the external system that provides the serial data to the board. The other option is for a master clock that is synchronized to the external serial data coming into the board, be used as the master clock for the CS4328 as well. However, if an external

master clock is to be used, U8 must be removed from it's socket to prevent the two clock signals from interfering with one another. When 8412 is selected by JP3, the master clock for the CS4328 is provided by the MCK output of the CS8412. The CKS pin of the CS4328 can be pulled either high or low via JP2. This determines whether the master clock frequency has to be 384X or 256X the input word rate. Consult the CS4328 data sheet for the common master clock frequencies table.

Analog Outputs

The analog outputs are available at 2 BNC connectors labeled AOUTL and AOUTR. R5 and C18 remove the remaining very high frequency components from the left channel output signal while R6 and C19 do so for the right channel output signal.

Digital Audio Standard Interface

Included on the evaluation board is a CS8412 Digital Audio Interface Receiver. This device can receive and decode data according to the AES/EBU, S/PDIF, and EIAJ-340 interface standard. Figure 3 shows the schematic for the CS8412. The input is coupled to the device through a transformer that is included on the board. The input to the device can be configured to accept either professional or consumer input modes. Consult the CS8412 data sheet for an explanation of the two input modes.

The LEDs, D4-D8, perform two functions. When S1 is in the Channel Status position, the LEDs display the channel status information for the channel selected by JP1. When S1 is in the Error Information position, the LEDs D4-D6, display encoded error information that can be decoded by consulting the CS8412 data sheet. Encoded sample frequency information is displayed on LEDs D7-D9 provided a proper clock is being applied to the FCK pin of JP1. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8412. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option should be selected if the FCK pin of JP1 is being driven by a clock signal.

Serial Output Interface

The SDATA, SCLK, L/$\overline{R}$, and MCLK BNC connectors can also be used to provide a serial output interface for the CS8412. With JP3 in the 8412 position, the outputs from the CS8412 can be brought off the board to an external evalution system. This data can be configured in one of seven selectable formats. These formats are outlined in the CS8412 data sheet.

CDB5336/7/8/9 Interface to CDB4328

Many users find it informative to evaluate a combined ADC and DAC system connected together yielding analog input and analog output. This can be accomplished by interconnecting a CDB5326/7/8/9 or CDB5336/7/8/9 to a CDB4328 evaluation board. The following information contains several techniques to accomplish this goal. There are two general points which need to be mentioned. An analog input of ± 3.68 V will produce a full scale digital output from the CS5336/7/8/9 and the CS5326/7/8/9. A full scale digital input to the CS4328 will produce a full scale output of ± 2 V resulting in an overall loss of approximately 5.2 dB from input to output. Also it is recommended that the power connections for each board are brought directly from the power supply and not in a "daisy-chain" manner from board to board.

Connecting the CDB4328 to the CDB5336/7/8/9 can be accomplished using one of two methods:

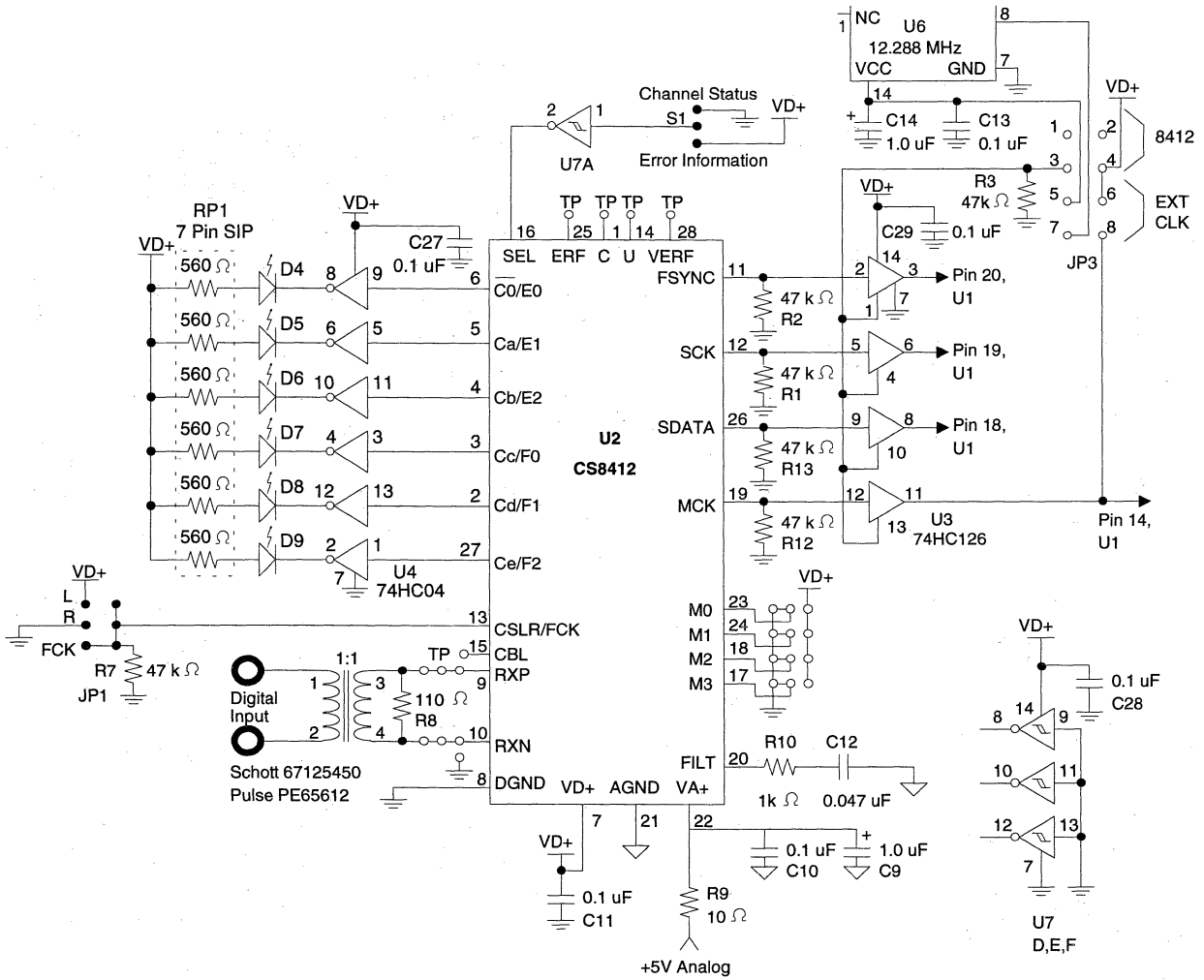


Figure 3. CS8412 Digital Audio Receiver Connections

CDB4328 to CDB5336/7/8/9 - Method 1

This method uses the AES/EBU Digital Audio Interface which is supported by the CS8402 AES/EBU Transmitter and the CS8412 AES/EBU Receiver. The data and clock information is transmitted from the CDB5336/7/8/9 to the CDB4328 via this interface.

CDB4328 Configuration for Method 1

The CS8412 is configured to output data in Format 0 (M0,M1,M2 and M3 low) and the CDB4328 must be set to receive data in the corresponding Format 2 (DIF1 high and DIF0 low). Modify the jumpers located near pins 12 and 13 of the CS4328. Please note that Format 0 for the CS8412 corresponds to the Format 2 for the CS4328. JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 and is set low for a ratio of 256.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be in the 8412 position to allow the CDB4328 to access the multiple clocks generated from the CS8412 and disable the oscillator U8.

CDB5336/7/8/9 Configuration for Method 1

P4 selects an option to invert the SCLK for the CS8402 and the parallel interface. The positions of P4 are labeled and the jumpers should be in the appropriate position for the ADC being used. P7 should be set to "internal" to allow the use of the master clock on the CDB5336/7/8/9. CMODE is set low for a master clock to sample rate ratio of 256.

CDB5336/7/8/9 and CDB4328 Interconnection for Method 1

Interconnection requires the power supply connections and a shielded twisted pair cable connecting the digital outputs from the CDB5336/7/8/9 to the digital inputs on the CDB4328.

CDB4328 to CDB5336/7/8/9 - Method 2

Method 2 of interfacing the CDB5336/7/8/9 and the CDB4328 requires a direct interface through the EXTCLKIN, SCLK, SDATA, and L/R BNC connectors. This technique also requires minor modifications to the CDB5336/7/8/9.

CDB4328 Configuration for Method 2

The CS4328 is set to accept data in format 3 (DIF0 and DIF1 high). JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 (pin 11) is set low for a ratio of 256.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be removed to access the multiple clocks from the CDB5336/7/8/9 and disable the oscillator U8.

A left channel input will appear as a right channel output in this configuration. To correct this the L/R clock must be inverted prior to the CS4328 L/R input. This can be implemented by modifying the CDB4328 as follows: Cut the trace at the L/R BNC connecter on the CDB4328. Cut the trace at U7 pin 9. Place a jumper between U7 pin 9 and the L/R BNC. Place a jumper between U7 pin 8 and U1 pin 20.

CDB5336/7/8/9 Configuration for Method 2

The CS5336/7/8/9 data output contains 16 bits of audio data as well as 3 tag bits and a left/right indicator. These additional bits need to be removed before transmission to the CDB4328. This can be done by making use of the FSYNC pulse which frames the audio data bits. This has been implemented on the CDB5336/7/8/9 and can be utilized with a minor modification: cut

the trace at the SDATA BNC connector and place a jumper between the SDATA BNC and U8 pin 11. CMODE is set LOW for a master clock of 256 times the sample rate. P7 must have both the internal and external jumpers installed. This will route the master clock to the EXTCLKIN BNC for connection to the CDB4328 MCLK.

If a CS5336/8 is installed an additional modification is required to invert the SCLK prior to transmission to the CDB4328. This can be implemented as follows: cut the trace at the SCLK BNC and install a jumper between U7 pin 4 and the SCLK BNC.

CDB5336/7/8/9 and CDB4328 Interconnection for Method 2

Shielded coaxial cables with BNC connectors should be used to make the following connections: L/R to L/$\overline{R}$, SCLK to SCLK, SDATA to SDATA, EXTCKIN to MCLK.

CDB4328 Interfacing to the CDB5326/7/8/9

A method of interfacing the CDB5326/7/8/9 and the CDB4328 requires a direct interface through the EXTCLKIN, SCLK, SDATA, and L/R BNC connectors. This technique requires modifications to the CDB5326/7/8/9 to derive the proper clock frequencies. This is done by utilizing a 12.288 MHz clock and supplying a clock to the CDB5326/7/8/9 at 6.144 MHz.

CDB4328 Configuration

The CS4328 must be set to receive data in format 2 (DIF1 high and DIF0 low). Modify the jumpers located near pins 12 and 13 of the CS4328. JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 and is set low for a 256 ratio.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be removed to access the multiple clocks from the CDB5326/7/8/9. Remove the 12.288 MHz oscillator (U8).

CDB5326/7/8/9 Configuration

Remove the clock source jumper (P2). Remove the 6.144 MHz oscillator (U2) and replace with the 12.288 MHz oscillator from the CDB4328.

Install a divide by 2 function on the CDB5326/7/8/9 digital patch area. Use a 74HC74 with the D input connected to the $\overline{Q}$ output. Connect the oscillator output to the 74HC74 clock input. Connect the $\overline{Q}$ output to U1 pin 23.

Position P2 to connect the oscillator output to the EXTCLKIN.

CDB5326/7/8/9 and CDB4328 Interconnection

Shielded coaxial cables with BNC connectors should be used to make the following connections: L/$\overline{R}$ to L/$\overline{R}$, SCLK to SCLK, SDATA to SDATA, EXTCLKIN to MCLK.

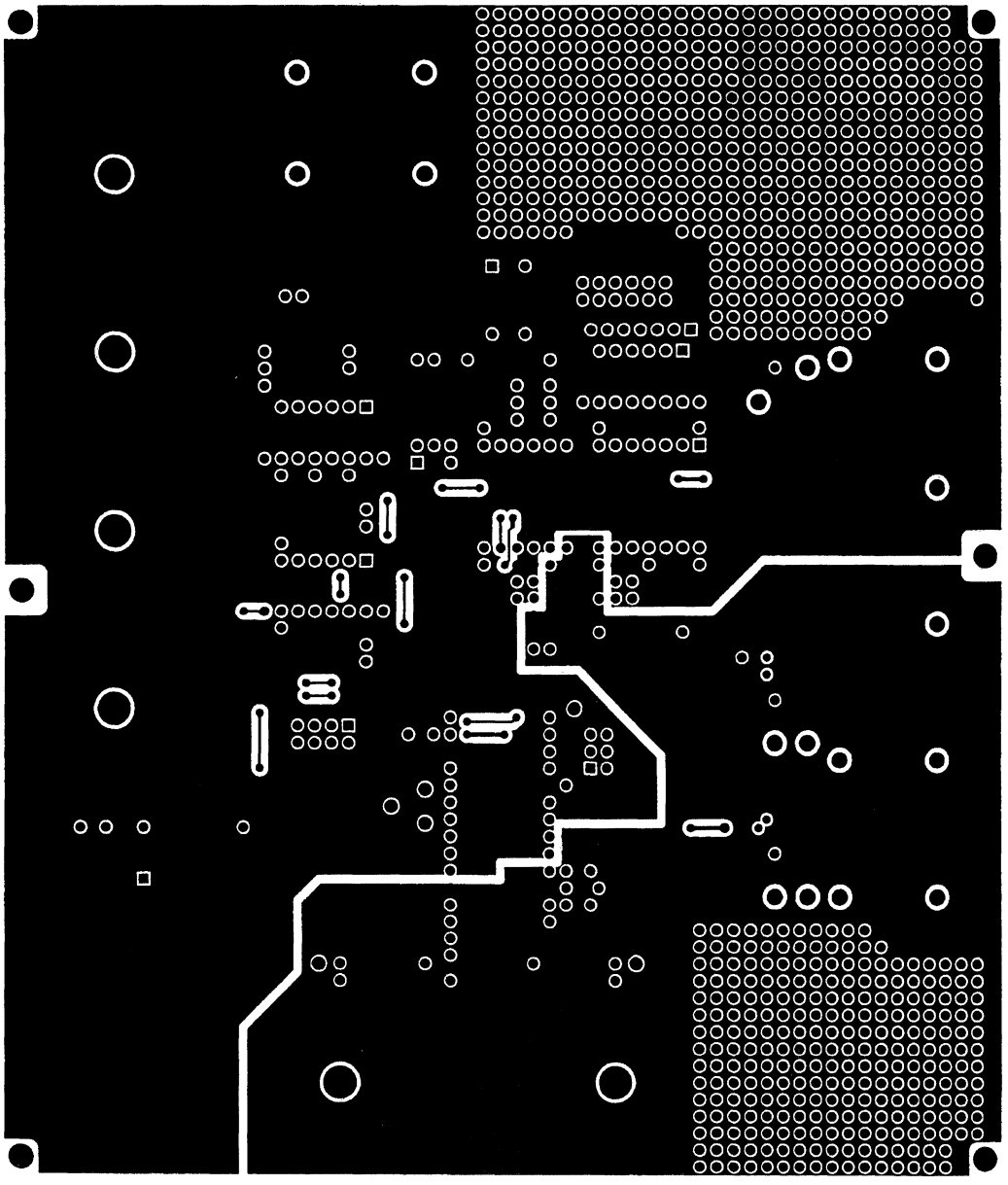


Figure 4. Top Ground Plane Layer (NOT TO SCALE)

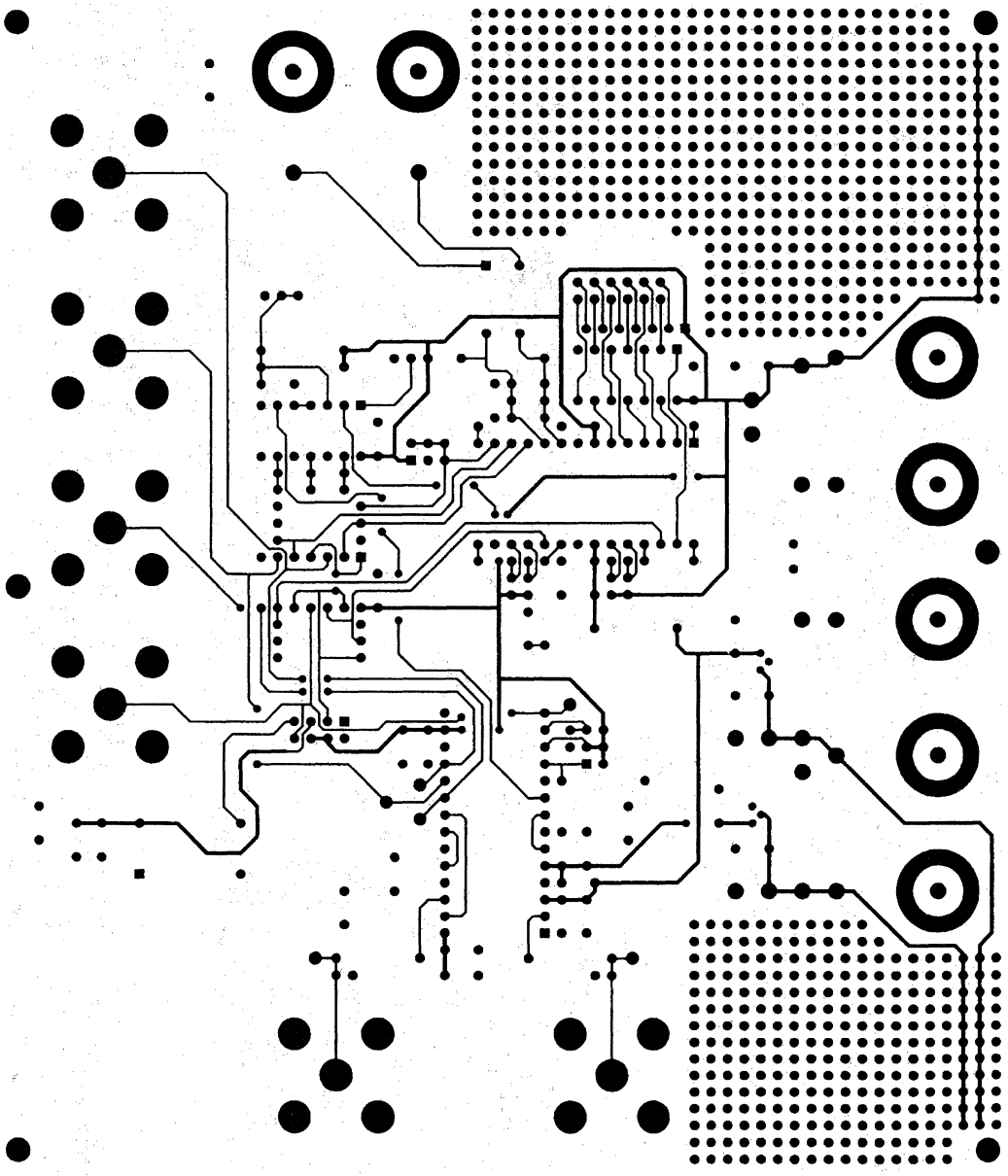


Figure 5. Bottom Trace Layer (NOT TO SCALE)

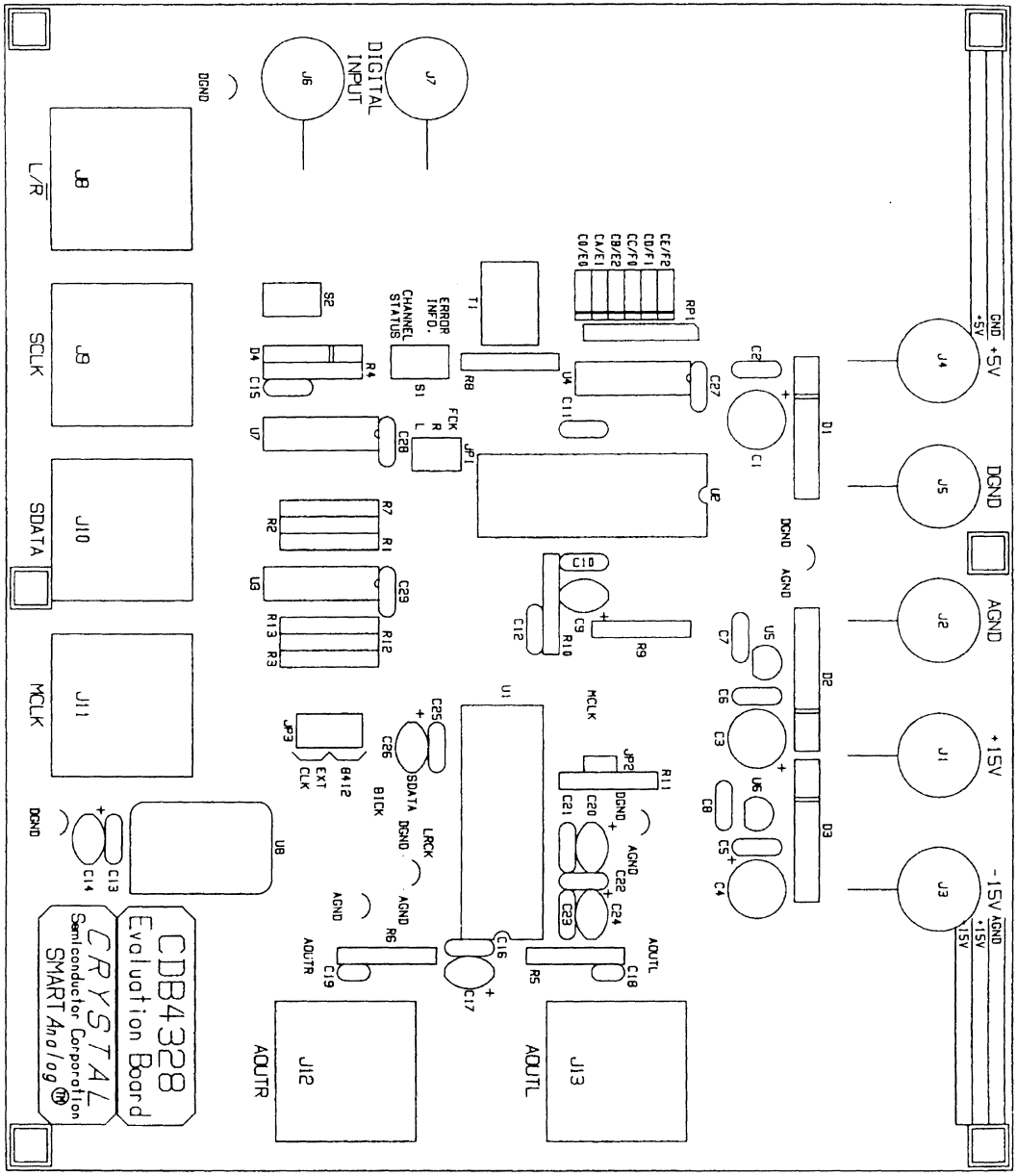


Figure 5. Silk Screen Layer (NOT TO SCALE)

•Notes•

Semiconductor Corporation

CS4330

8 Pin Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System Interpolation, D/A, Output Analog Filtering
- 96 dB Dynamic Range
- 0.003% THD + N
- On-Chip Digital De-emphasis
- Low Clock Jitter Sensitivity
- Single +3 to +5V power Supplies
- Completely Filtered Line Level Outputs Linear Phase Filtering

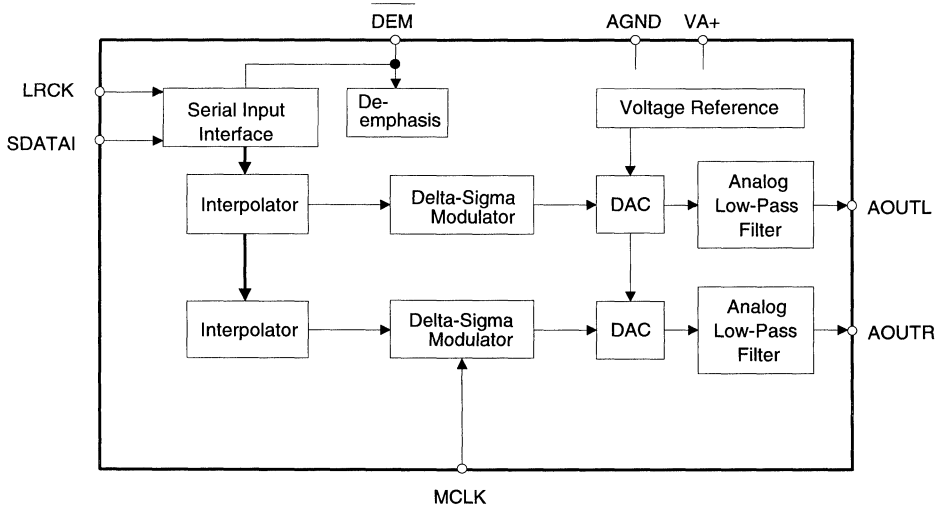
General Description

The CS4330 is a complete, stereo digital-to-analog output system in a small 8 pin package. It includes interpolation, D/A conversion and output analog filtering. The CS4330 is based on delta-sigma modulation where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4330 contains on-chip digital de-emphasis and operates from a single +3V to +5V power supply, and it consumes only 50 mW of power with a 3V power supply. These features make it ideal for portable CD players and other portable playback systems.

ORDERING INFORMATION

CS4330-KP	0 to 70°C	8-pin Plastic DIP
CS4330-KS	0 to 70°C	8-pin Plastic SOIC



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this porduct without notice.

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• Notes •

CS5326/7/8/9 and CS5336/8/9 Delta-Sigma Audio A/D Converters

This new class of device features 64X oversampling, using a Delta-Sigma architecture with resolutions of 16 or 18-bits. Output word rates can be from 1 kHz to 50 kHz. These stereo parts have 2 sample and holds, dual Delta-Sigma modulators, two anti-aliasing and decimation filters, and a voltage reference, all in a 28-pin package. Performance measurements include 95 dB dynamic range in stereo mode, up to 100 dB in mono mode, along with 0.0015% THD.

CS5345 Low Power A/D Converter

The CS5345 is a single chip, 16-bit, stereo A/D converter requiring only 100mW of power from a single +5V supply. The part features two analog delta-sigma modulators, two digital decimation filters and a voltage reference in an SOIC package.

CS5349 Single Supply, Stereo A/D Converter for Digital Audio.

The CS5349 is a complete, 16-bit analog-to-digital converter for stereo digital audio systems that require a single +5V supply. Similar to the CS5339, the CS5349 features 64X oversampling Delta Sigma conversion with on-chip sample and hold, filtering and voltage reference in a 28-pin package.

CS5389 & CS5390 Professional Audio Analog to Digital Converters

The CS5389 is Crystal's newest audio A/D converter aimed at the professional audio market. Dual differential inputs, with special modulator design, yield a dynamic range of 107 dB. Excellent noise rejection and low idle tones yield a superbly performing A/D Converter.

The CS5390 is pin compatible with the CS5389, and offers increased dynamic range and 20-bit output data words.

Audio A/D Converter Comparison Table

Device	CS5326	CS5327	CS5328	CS5329	CS5336	CS5338	CS5339	CS5349	CS5389	CS5390
Number of Bits	16	16	18	18	16	16	16	16	18	20
Dynamic Range (dB)	95	95	100*	100*	95	95	95	90	107	110
SOIC Package	-	-	-	-	✓	✓	✓	✓	-	-
Filter Passband (kHz)	0-22	0-20	0-22	0-20	0-20	0-22	0-22	0-22	0-22	0-22
Filter Transition Band (kHz)	22-26	20-24	22-26	20-24	20-26	22-28	22-28	22-28	22-28	22-28
Stop Band Attenuation (dB)	-86	-86	-86	-86	-80	-80	-80	-80	-80	-98
Overrange Tag Bits	-	-	-	-	✓	✓	✓	✓	-	
Left/Right Tag Bits	-	-	-	-	✓	✓	✓	✓	-	
Master Clocking Mode	-	-	-	-	✓	✓	✓	✓	✓	✓
SCLK active edge	↑	↑	↑	↑	↑	↑	↓	↓	↓	↓
Master Clock Frequency (XFs)	128	128	128	128	256/384	256/384	256/384	256/384	256/384	256/384
Power Supply Voltages (V)	±5	±5	±5	±5	±5	±5	±5	+5	±5	±5
Operation < 30 kHz without TEST Mode	-	-	-	-	✓	✓	✓	✓	✓	✓
Power Consumption mW	450	450	450	450	400	400	400	325	550	550

* In Mono Mode

All frequencies are with an output word rate of 48 kHz

CONTENTS

• Notes •

Semiconductor Corporation

CS5326 CS5327 CS5328 CS5329

16 & 18-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  - 30 kHz to 50 kHz
- Low Noise and Distortion
  - 95 dB dynamic range, 16-Bit
  - 97 dB dynamic range, 18-Bit
  - 100 dB dynamic range, 19-Bit Mono
  - 0.0015% THD
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.001dB Passband Ripple
  - 86dB Stopband Rejection
- Low Power Dissipation: 450 mW
  - Power-Down Mode for Portable Applications

General Description

The CS5326, CS5327, CS5328 & CS5329 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16 or 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

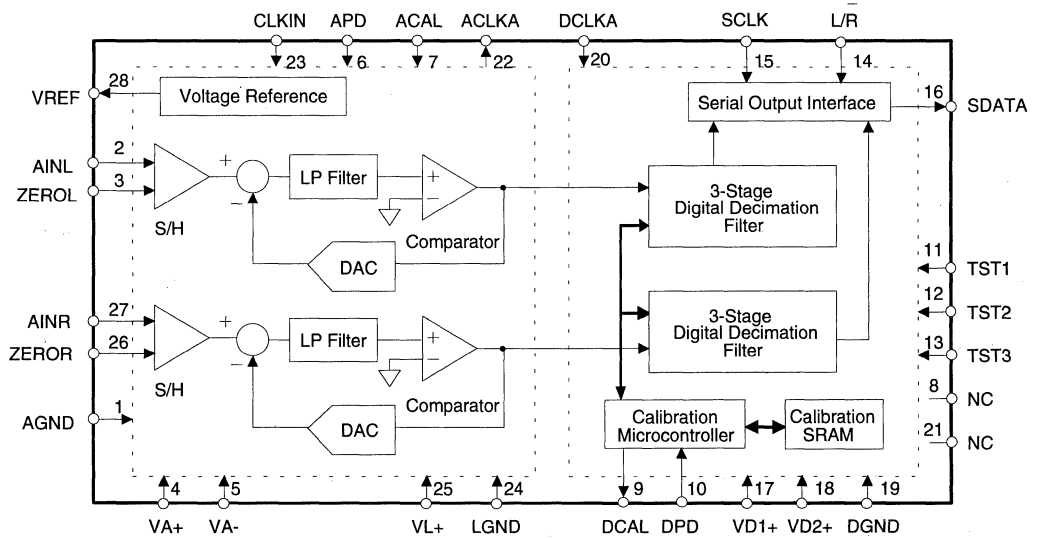
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5326 & CS5327 are 16-bit ADCs, achieving 95 dB dynamic range. The CS5328 & CS5329 are 18-bit ADCs with 97 dB dynamic range in stereo mode and 100 dB dynamic range in mono mode.

The CS5326 & CS5328 have digital filters which are compatible with CD requirements. The CS5327 & CS5329 have filters which guarantee no aliasing. The filters have linear phase, 0.001 dB passband ripple, and >86 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP.

ORDERING INFORMATION: Page 3-23



ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VL+,VD1+,VD2+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 4kHz; CLKIN = 6.144MHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; Digital Inputs: Logic 1 = VD+, Logic 0 = DGND; unless otherwise specified.)

Parameter*			Symbol	Specification min	typ	max	Units
Resolution		CS5326, CS5327		16			Bits
		CS5328, CS5329		18			Bits
Dynamic Performance							
Dynamic Range		CS5326, CS5327		92.7	95.7		dB
		CS5328, CS5329		94.7	97.1		dB
(Note 1)	Mono	CS5328, CS5329			100.1		dB
Signal-to-		CS5326, CS5327		90.7	92.7		dB
(Noise + Distortion)		CS5328, CS5329	S/(N+D)	92.5	94.5		dB
(Note 1)	Mono	CS5328, CS5329			97		dB
Total Harmonic Distortion							
Vin = ± FS			THD	0.003	0.0015		%
Vin = -20 dB					0.001		%
Interchannel Phase Deviation					0.0001		Degrees
Interchannel Isolation (dc to 20 kHz)				100	106		dB
dc Accuracy							
Interchannel Gain Mismatch					0.01	0.05	dB
Gain Error					± 1	± 5	%
Gain Drift					50		ppm/ ^{o} C
Bipolar Offset Error		CS5326, CS5327			± 5	± 15	LSB (16-bit)
(After Calibration)		CS5328, CS5329			± 20	± 60	LSB (18-bit)
Analog Input							
Input Voltage Range	(± Full Scale)		VIN	± 3.50	± 3.68		Volts
Input Impedance			ZIN		65		kΩ
Power Supplies							
Power Supply Current	(VA+) + (VL+)		IA+		25	35	mA
with APD,DPD low	VA-		IA-		25	35	mA
(Normal Operation)	(VD1+) + (VD2+)		ID+		40	55	mA
Power Supply Current	(VA+) + (VL+)		IA+		10	15	uA
with APD,DPD high	VA-		IA-		10	15	uA
(Power-Down Mode)	(VD1+) + (VD2+)		ID+		5	7	mA
Power Consumption	(APD, DPD Low)		PDN		450	625	mW
	(APD, DPD High)		PDS		25	35	mW
Power Supply Rejection Ratio (dc to 26 kHz)			PSRR		54		dB
(26 kHz to 3.046 MHz)					100		dB

Notes: 1. Mono means connecting AINL & AINR together and adding together the output words from each channel.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD1+,VD2+= 5V ± 5%; VA- = -5V ± 5%; CLKIN = 6.144MHz)

Parameter		Symbol	Min	Typ	Max	Units
Passband (-3 dB)	CS5326, CS5328		0		23.5	kHz
(-3 dB)	CS5327, CS5329		0		21.6	kHz
(-0.001 dB)	CS5326, CS5328		0		21.8	kHz
(-0.001 dB)	CS5327, CS5329		0		20.0	kHz
Passband Ripple					0.001	dB
Stopband	CS5326, CS5328		26		3046	kHz
	CS5327, CS5329		24		3052	kHz
Stopband Attenuation	(Note 2)		86			dB
Group Delay		t_{gd}		4274/CLKIN		s
Group Delay Variation vs. Frequency		$\triangle t_{gd}$			0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for a CLKIN of 6.144MHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±21.8kHz for the CS5326 & CS5328, or n x 3.072MHz ±20.0kHz for the CS5327 & CS5329 , where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD1+,VD2+= 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (CLKIN)	V_{IH}	(VD+) - 1.0	-	-	V
Low-Level Input Voltage (CLKIN)	V_{IL}	-	-	1.0	V
High-Level Input Voltage (except CLKIN)	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage (except CLKIN)	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD1+,VD2+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	VA+	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	−4.75	−5.0	−5.25	V
Analog Input Voltage	(Note 3)	V_{AIN}	−3.68	-	3.68	V
CLKIN Frequency		f_{CLK}	3.84	-	6.4	MHz
SCLK Frequency		f_{SCLK}	f_{CLK} /2	-	f_{CLK}	Hz
L/$\overline{R}$ Frequency		$f_{L/\overline{R}}$	f_{CLK} /128	-	f_{CLK} /128	Hz

Notes: 3. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification.

SWITCHING CHARACTERISTICS

(T_A = 25 °C; VA+, VL+, VD1+ , VD2+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

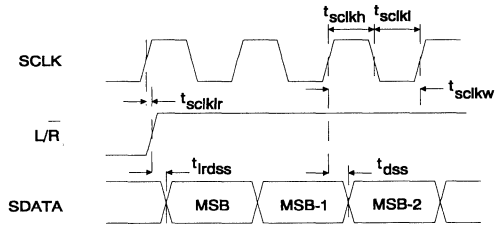
Parameter	Symbol	Min	Typ	Max	Units
CLKIN Period	t_{clkw}	155	-	260	ns
CLKIN Low	t_{clkl}	50	-	-	ns
CLKIN High	t_{clkh}	50	-	-	ns
CLKIN Rising to ACLKA edge (Note 4)	t_{clka}	40	-	100	ns
ACLKA Falling to L/$\overline{R}$ Edge (Note 4)	t_{aclr}	-140	-	140	ns
CLKIN Rising to L/$\overline{R}$ Edge (Note 4) ACLKA to CLKIN phase correct ACLKA to CLKIN phase unknown	t_{clr}	 -10 -10	 - -	 170 30	ns
SCLK Pulse Width Low	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High	t_{sclkh}	60	-	-	ns
SCLK Period	t_{sclkw}	155	-	-	ns
SCLK Rising to SDATA Valid	t_{dss}	-	-	45	ns
L/$\overline{R}$ edge to MSB Valid	t_{lrdss}	-	-	50	ns
SCLK Rising to L/$\overline{R}$ edge	t_{sclklr}	-40	-	40	ns
DPD, APD pulse width	t_{pd}	150	-	-	ns
CLKIN Falling to APD Falling	t_{apdclk}	-30	-	30	ns

Notes: 4. It is recommended that L/$\overline{R}$ be generated by dividing ACLKA by 64. If CLKIN is used to generate L/$\overline{R}$, a longer CLKIN to L/$\overline{R}$ delay may be tolerated if the phase of ACLKA is determined through the use of the APD pin. When high, the APD pin resets the divide-by-two circuit that generates ACLKA from CLKIN (that is, ACLKA is reset to "0"). APD should be brought low on a falling edge of CLKIN. This falling edge should be chosen such that L/$\overline{R}$ edges nominally occur at ACLKA falling edges.

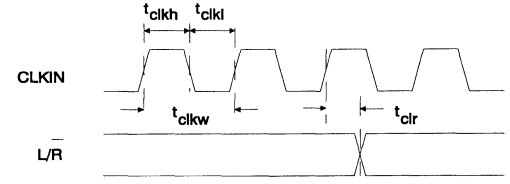
ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD1+,VD2+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V_{INA}	(VA-)- 0.3	(VA+)+ 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

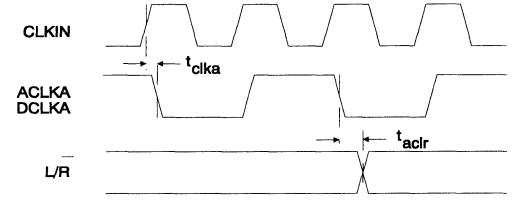
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.



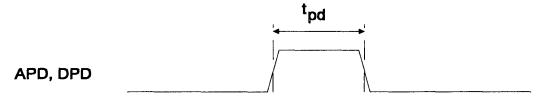
Serial Data Timing



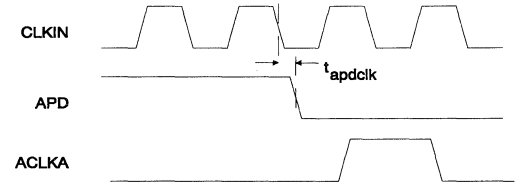
Channel Selection Timing Using L/R Derived From CLKIN/128



Channel Selection Timing Using L/R Derived from ACLKA/64



Power Down Timing



ACLKA Phase Determination using APD

GENERAL DESCRIPTION

The CS5326, CS5327, CS5328 and CS5329 are 16 & 18-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64× sampling rate. A three-stage digital filter then constructs pairs of 16-bit or 18-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of ± 3.68 volts. Any zero offset can be internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16 or 18-bit numbers. Typical power consumption of only 450 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these

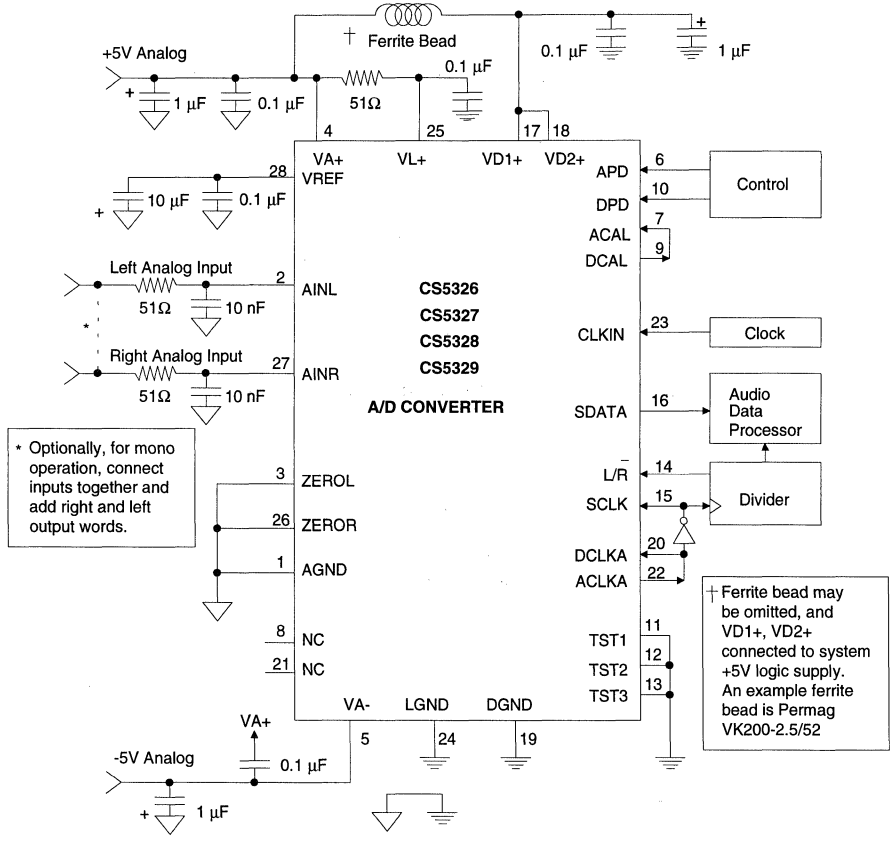


Figure 1. Typical Connection Diagram

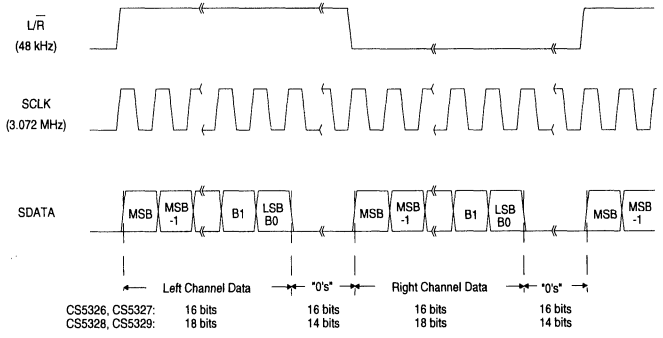


Figure 2. Data Output Timing

ADCs, see the references at the end of this data sheet.

SYSTEM DESIGN WITH THE CS5326/7/8/9

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required.

Clocks and Data Output Format

All timing and control inputs to the ADC can be easily generated from a master system clock. This clock, connected to the CLKIN pin on the device, must be exactly equal to 128 times the desired output word rate. Standard digital audio rates are 32 kHz, 44.1 kHz and 48 kHz, requiring master clock rates of 4.096 MHz, 5.6448 MHz and 6.144 MHz, respectively.

The CLKIN signal should be greater than 4 volts for a logic one and less than 1 volt for a logic zero. This is to minimize any clock related jitter in the sampling process, which can smear high frequency signals. Indeed, a low jitter (such as a crystal-based) clock is recommended.

Data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The rising edge of SCLK causes the part to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. Even so, a rising SCLK edge must occur coincident (within the timing tolerance) with the L/$\overline{R}$ edge for internal housekeeping purposes.

It is recommended to connect SCLK to ACLKA, as shown in Figure 1. Fourteen or sixteen trailing zero's will be clocked out on SDATA as part of each data word, as shown in Figure 2. ACLKA's frequency is the analog modulator sampling rate, and if a lower frequency is used for SCLK, slight degradation of the ADC dynamic range can occur due to interference effects.

Selection of left channel or right channel data is accomplished using the L/$\overline{R}$ input pin. The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled inputs.

Rising edges of L/$\overline{R}$ are used to synchronize the digital filter; therefore L/$\overline{R}$'s frequency must be CLKIN/128. It is preferable to generate L/$\overline{R}$ by dividing ACLKA by 64. If CLKIN is used to generate L/$\overline{R}$, it is best to determine the phase of ACLKA through the use of the APD pin. (When high, the APD pin resets the internal divide-by-two circuit that generates ACLKA. See Figure 4 for an example circuit.) If ACLKA phase is left indeterminate, then the CLKIN to L/$\overline{R}$ delay must

be shorter than the smaller delay shown in the Switching Characteristics table (see Note 4.).

Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically ± 3.68 volts.

The ADC samples the analog inputs at 3.072 MHz for a 6.144 MHz CLKIN. For the CS5326 & CS5328 the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5327 & CS5329 the digital filter rejects all noise between 24 kHz and (3.072 MHz-24 kHz). However, the filter will not reject frequencies right around 3.072 MHz. Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51 Ω resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins.

The on-chip voltage reference output is brought out to the VREF pin. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 20 mW. In addition, exiting the power-down state initiates the offset calibration procedure. This can be important for digital audio applications since any initial offset manifests itself as an audible power-on click.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle, whereas APD going low sets the phase of the ACLKA signal. If not using the power down feature and if not using APD to set the phase of ACLKA, APD should be tied to ground. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10 µF, as stated in the "Power-Up Considerations" section.

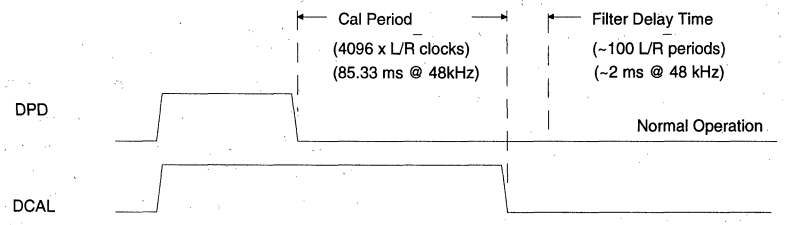


Figure 3. Initial Calibration Cycle Timing

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 3, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to ground the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present on the front end.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 100 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals. The transition is simply the natural filter response and is, of course, graceful.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference, however, can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows powering the part from single ±5 volt supplies. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. The VREF decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF to Pin 1 AGND and to minimize the path between VREF and the capacitors.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Multiple ADC's

In systems where multiple ADC's are used, care must be taken to ensure that the ACLKA phases are synchronized if simultaneous sampling is desired. In the absence of this synchronization, the sampling difference could be one CLKIN cycle (typically 162 ns). If this difference is unacceptable, the parts may be synchronized to within several nanoseconds by using the circuit shown in Figure 4. This circuit ensures that when the ADC's come out of power-down mode, ACLKA will have the same phase between all ADC's. The APD signal is used to reset the internal divide-by-two flip-flop which generates ACLKA. The circuit also ensures that L/$\overline{R}$ and SCLK occur at the correct time.

PERFORMANCE

FFT Tests

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 5 shows the spectral purity of the CS5326 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 94.63 dB.

Figure 6 shows the CS5326 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at -112 dB.

Figure 7 shows the low-level performance of the CS5326. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 8 shows the same very low input amplitude performance, but at 9kHz input frequency.

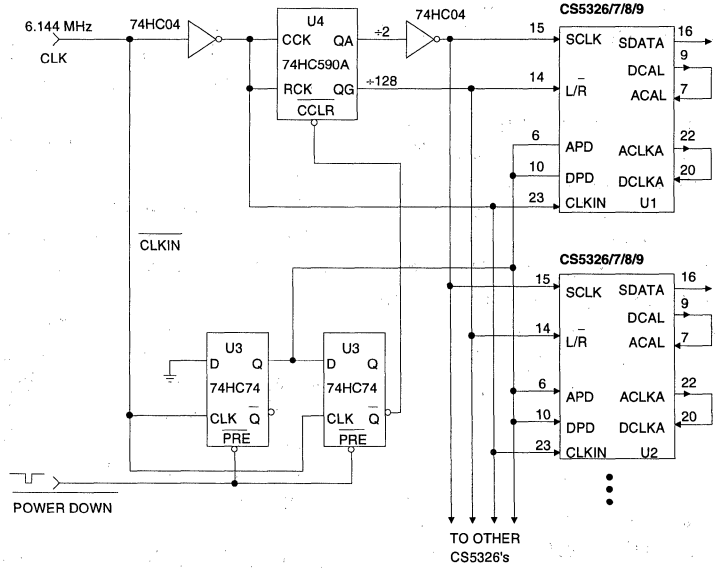


Figure 4. Connections for Synchronization of Multiple CS5326/7/8/9 ADC's.

Figure 9 shows the CS5327 FFT plot with an input signal of 1 kHz at -10 dB. This is very similar to the CS5326 plot, but notice the reduction in the noise floor between 22 kHz and 24 kHz. This is caused by the digital filter attenuating the noise in its transition band.

Figure 10 shows a plot of Signal to (Noise + Distortion) versus input amplitude relative to full

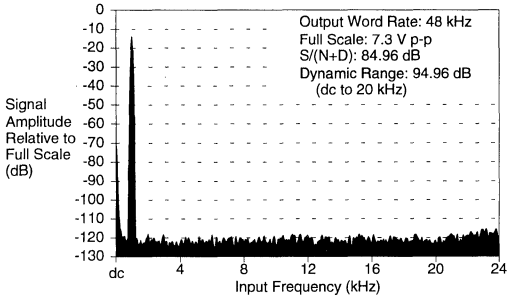


Figure 5. CS5326 FFT Plot with -10 dB, 1 kHz Input

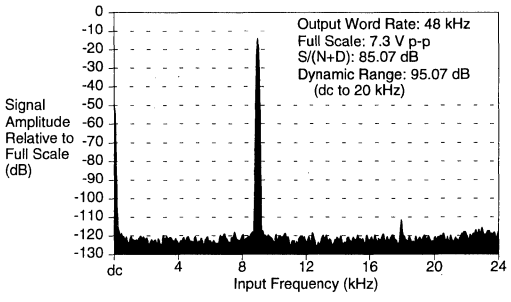


Figure 6. CS5326 FFT Plot with -10 dB, 9 kHz Input

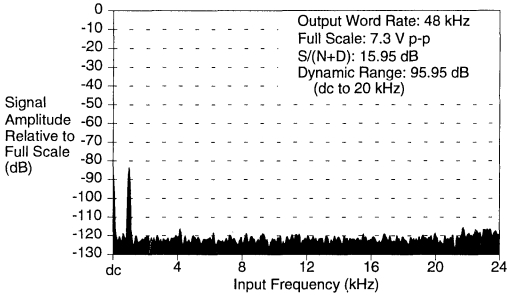


Figure 7. CS5326 FFT Plot with -80 dB, 1 kHz Input

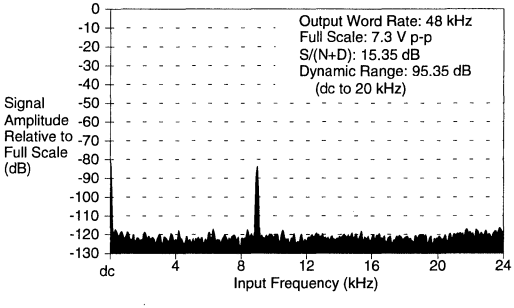


Figure 8. CS5326 FFT Plot with -80 dB, 9 kHz Input

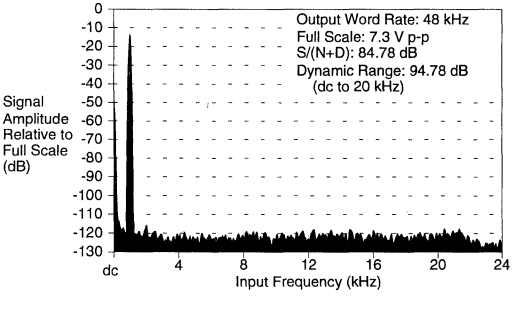


Figure 9. CS5327 FFT Plot with -10 dB, 1 kHz Input

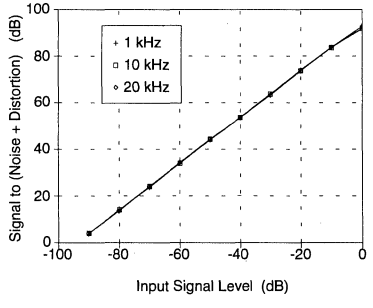


Figure 10. CS5326, CS5327 Signal to Noise+Distortion Ratio vs. Input Level

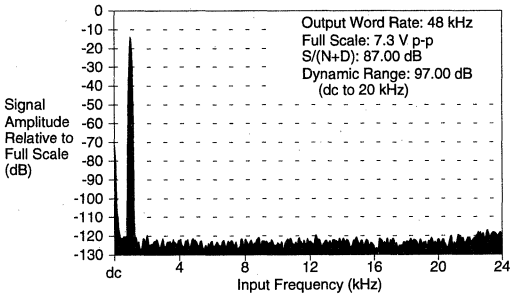


Figure 11. CS5328 FFT Plot with -10 dB, 1 kHz Input

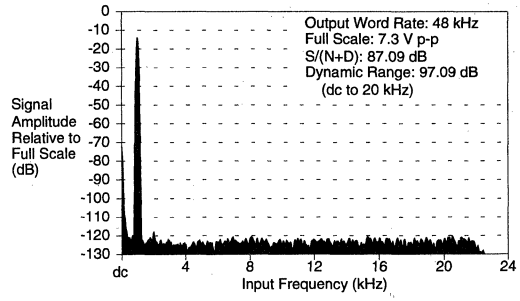


Figure 12. CS5329 FFT Plot with -10 dB, 1 kHz Input

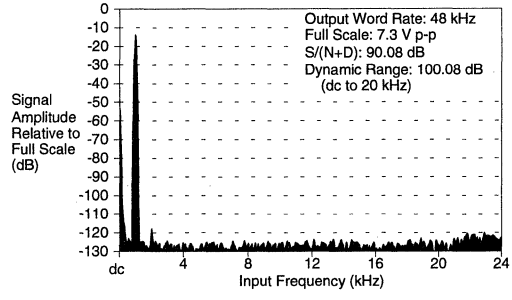


Figure 13. CS5328 in Mono Mode FFT Plot with -10 dB, 1 kHz Input

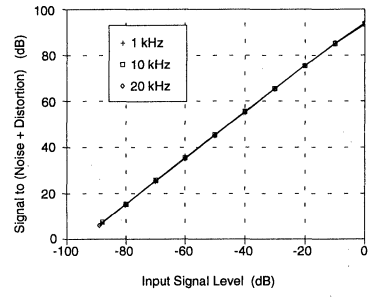


Figure 14. CS5328 Signal to Noise+Distortion Ratio vs. Input Level

scale. For an ideal ADC, this plot would be a straight line at 45° for all input frequencies between dc and half the output word rate. The measured data from a CS5326 shows both the excellent high frequency performance as well as the maintenance of good performance with low input levels.

Figure 11 shows the18-bit CS5328 FFT plot. Notice the 2 dB improvement in dynamic range over the CS5326.

Figure 12 shows the18-bit CS5329 FFT plot. Notice the filter cut-off at 22 kHz, and the 2 dB improvement in dynamic range over the CS5327.

Figure 13 shows the CS5328 operated in 19-bit mono mode, with the two inputs joined together, and the output words added. Notice the 3 dB improvement over Figure 11.

Figure 14 shows a plot of Signal to Noise + Distortion versus Input Level for the 18-bit CS5328. Notice the improvement in values over Figure 10.

DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the

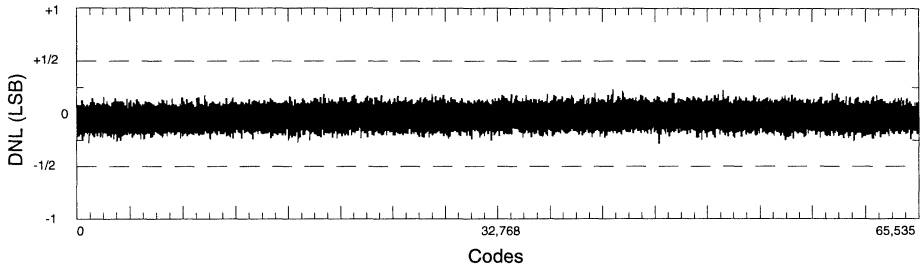


Figure 15. CS5326 Differential Non-Linearity Plot

codewidths. Figure 15 shows the excellent Differential Non-Linearity of the CS5326. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within ± 0.2 LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 10 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

Digital Filter

Figures 16 through 21 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz, with a CLKIN frequency of 6.144 MHz. The filter frequency response will scale precisely with changes in CLKIN frequency. The passband ripple is flat to ± 0.001 dB maximum. Stopband rejection is greater than 86 dB.

Figures 16,18 &20 show the CS5326 and CS5328 filter characteristics. Figure 20 is an expanded view of the transition band.

Figures 17,19 & 21 show the CS5327 and CS5329 filter characteristics. Figure 21 is an expanded view of the transition band. Notice how the filter enters the stopband at exactly 24 kHz, which is half the output word rate, thereby guaranteeing no aliasing.

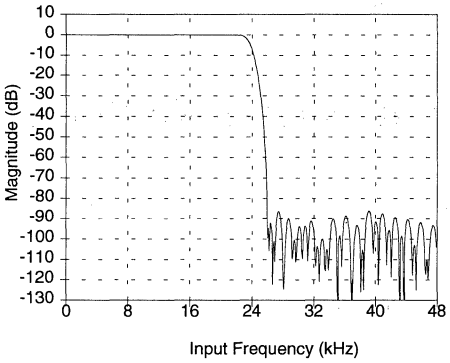


Figure 16. CS5326 /8 Digital Filter Stopband Rejection

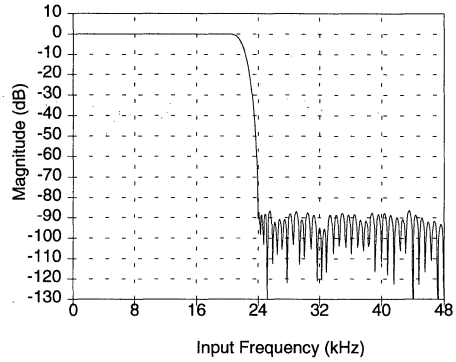


Figure 17. CS5327/9 Digital Filter Stopband Rejection

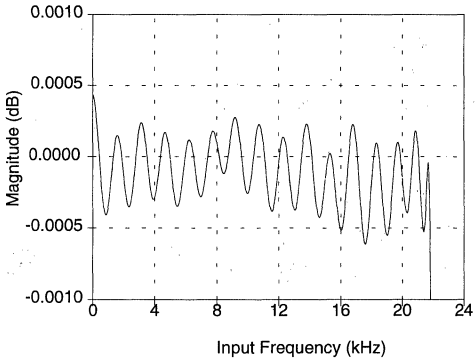


Figure 18. CS5326/8 Digital Filter Passband Ripple

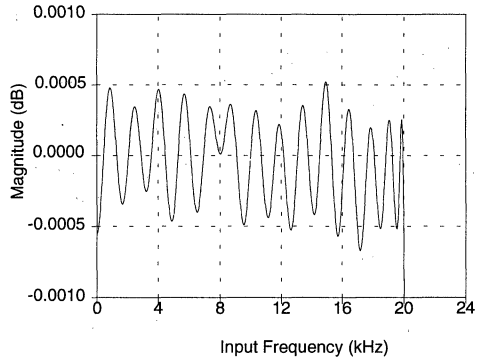


Figure 19. CS5327/9 Digital Filter Passband Ripple

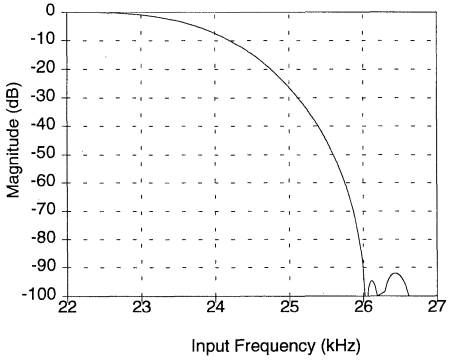


Figure 20. CS5326/8 Digital Filter Transition Band

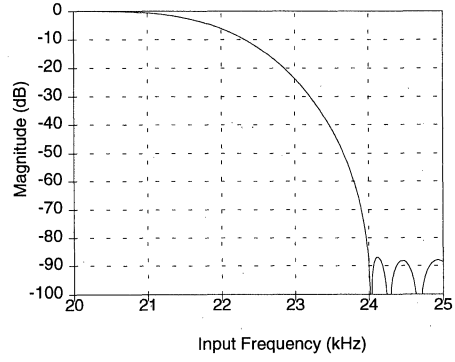
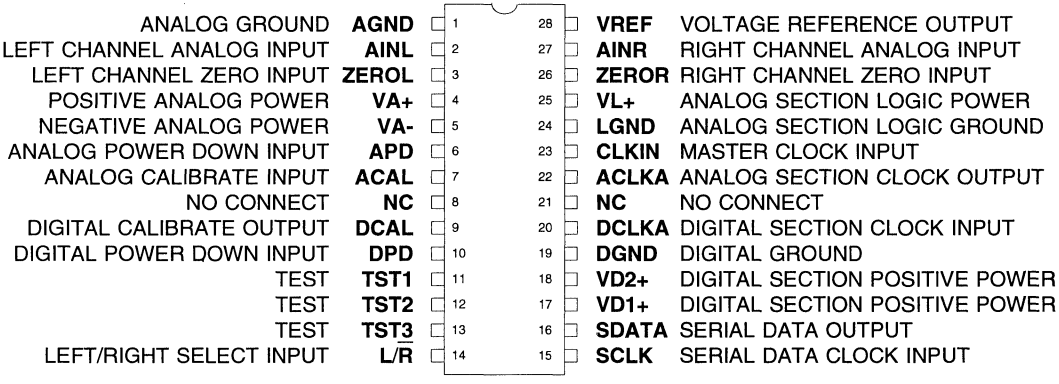


Figure 21. CS5327/9 Digital Filter Transition Band

PIN DESCRIPTIONS



3

Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 25.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 24
Ground for the logic portions of the analog section.

VD1+, VD2+ - Positive Digital Power, PINS 17, 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27
Analog input connections for the left and right input channels. Nominally ±3.68 volts full scale.

ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks..

Analog Outputs

VREF - Voltage Reference Output, PIN 28.

Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

Digital Inputs

CLKIN - Master Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators sample rate. Sampling rates, output rates, and digital filter characteristics scale to CLKIN frequency. CLKIN frequency of 6.144 MHz corresponds to an output word rate of 48 kHz per channel.

DCLKA - Digital Section Input Clock, PIN 20.

This clock is used to clock the modulator output data into the digital section. Must be connected to ACLKA.

SCLK - Serial Output Data Clock, PIN 15.

Data bits are output on the rising edge of SCLK.

L/$\overline{R}$ - Left/Right Select, PIN 14.

Select the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. Thereafter, CLKIN, SCLK and L/$\overline{R}$ should run synchronously. L/$\overline{R}$ must be equal to CLKIN/128. Although the outputs of each channel are transmitted at different times, the two words in a L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high the analog circuitry is in power-down mode. It also causes the analog section to reset the clock output (ACLKA). APD is normally connected to DPD when using the power down feature.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/$\overline{R}$ periods (85.33 ms with a 6.144 MHz clock). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

Digital Outputs

ACLKA - Analog Section Output Clock, PIN 22.

This clock is CLKIN/2. It is used by the digital section to clock in the modulator output data. ACLKA must be connected to DCLKA. The phase of ACLKA may be reset by using APD.

SDATA - Serial Data Output, PIN 16.

Data bits are presented MSB first, in 2's complement format.

DCAL - Digital Calibrate Output, PIN 9.

This pin rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 6.144 MHz CLKIN). May be connected to ACAL. (See Figure 3)

Miscellaneous

NC - No Connection, PINS 8,21.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST1, TST2, TST3 -Test Inputs, PINS 11, 12, 13.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error -The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

Differential Non-Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

REFERENCES (All reprinted in the back of this data book)

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Filter Enters Stopband	Temperature	Package
CS5326-KP	16-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5327-KP	16-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5328-KP	18-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5329-KP	18-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP

CDB5326	CS5326 Evaluation Board
CDB5327	CS5327 Evaluation Board
CDB5328	CS5328 Evaluation Board
CDB5329	CS5329 Evaluation Board

Semiconductor Corporation

CDB5326 CDB5327 CDB5328 CDB5329

Evaluation Board for CS5326, CS5327, CS5328 and CS5329

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, S/PDIF & CP-340 Compatible Digital Audio
- Buffered Serial Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

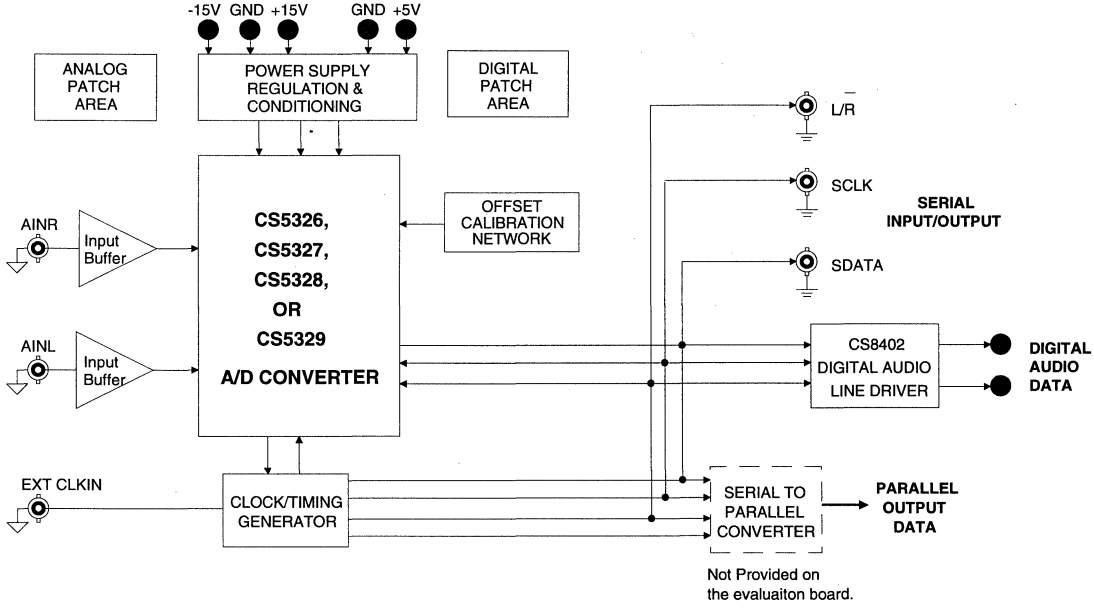
General Description

The CDB5326 and CDB5327 evaluation boards allow fast evaluation of the CS5326 and CS5327 16-bit, stereo A/D converters. The CDB5328 and CDB5329 evaluation boards allow fast evaluation of the CS5328 and CS5329 18-bit, stereo A/D converters. The boards generate all converter timing signals and provide a serial output interface. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:

CDB5326, CDB5327, CDB5328, CDB5329



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

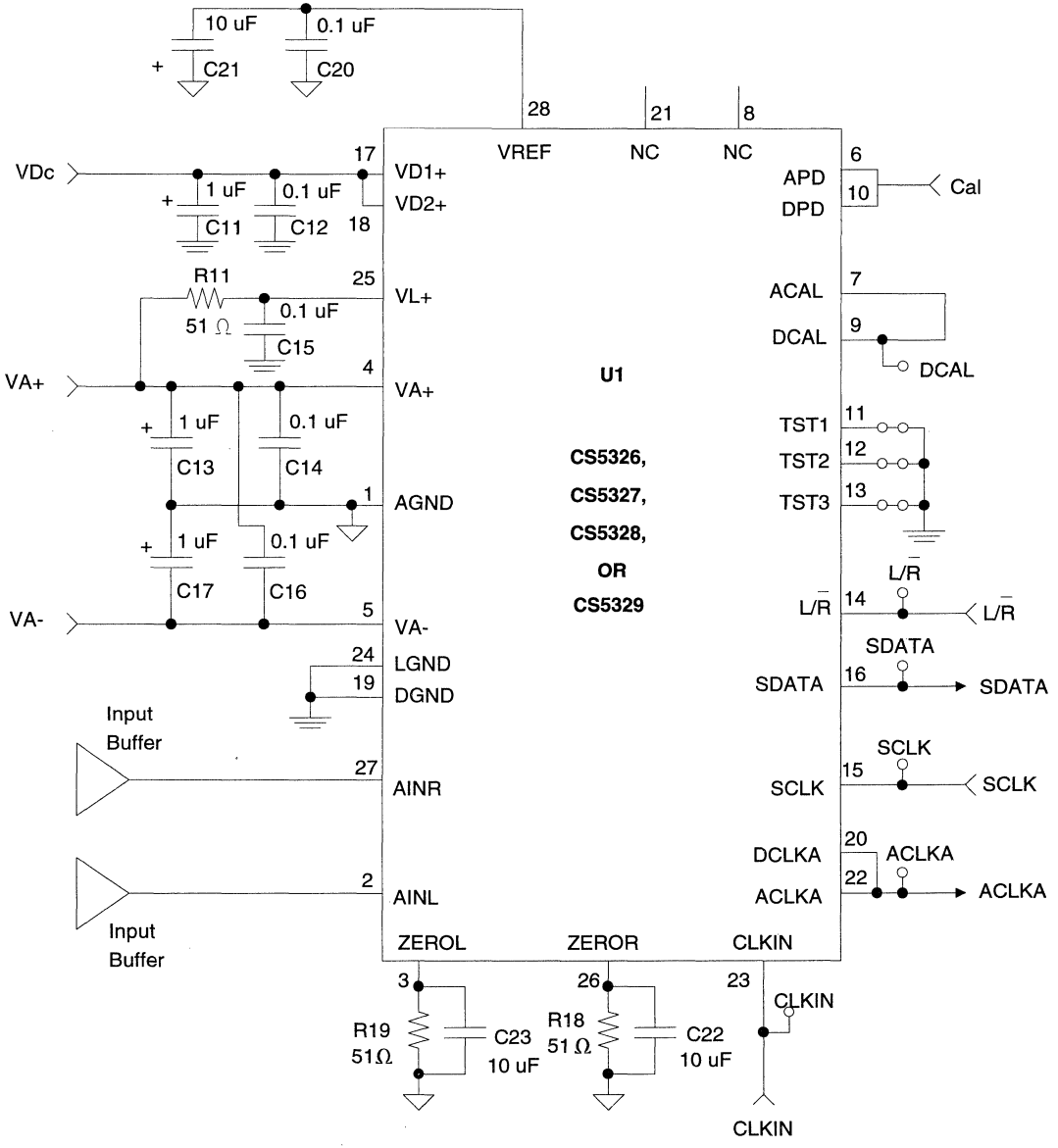


Figure 1. ADC Connections

Power Supply Circuitry

The schematic diagram in Figure 2 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The ±5 Volt analog power supply inputs of the converter are derived from ±15 Volts using the voltage regulators U3 and U5. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts with isolation provided by L1, L2 and L3. D1, D2 and D3 are transient suppressors which also provide protection from incorrectly connected power supply leads. C1-C6 provide general power supply filtering for the analog supplies. C13, C14, C16 and C17 provide localized decoupling for the converter VA+ and VA- pins as shown in Figure 2. Note that C16 is connected between VA- and VA+ and not VA- and AGND. R11 and C15 provide isolation for the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point. This ground plane arrangement isolates digital logic noise from the analog circuitry.

Analog Input Buffer and Protection Circuitry

As shown in Figure 2, the analog input signals are connected to the board via the BNC connectors labeled AINL and AINR. The input buffer and protection circuit is comprised of U10, R12-R15, Philips BAT-85 schottky diodes D5-D8, and the 5.6V zener diodes D9-D10. The Crystal Application Note "ADC Input Buffer and Protection Techniques" discusses this circuit and component selection criteria. Jumpers have been included to allow the input buffers to be easily bypassed and terminated.

RC filters, R16/C18 and R18/C19, provide antialias filtering and the optimum source impedance for the ADC analog inputs. The ZEROR and ZEROL inputs of the ADC are tied to analog ground through identical filters to duplicate the output impedance of the analog buffers for use during offset calibration.

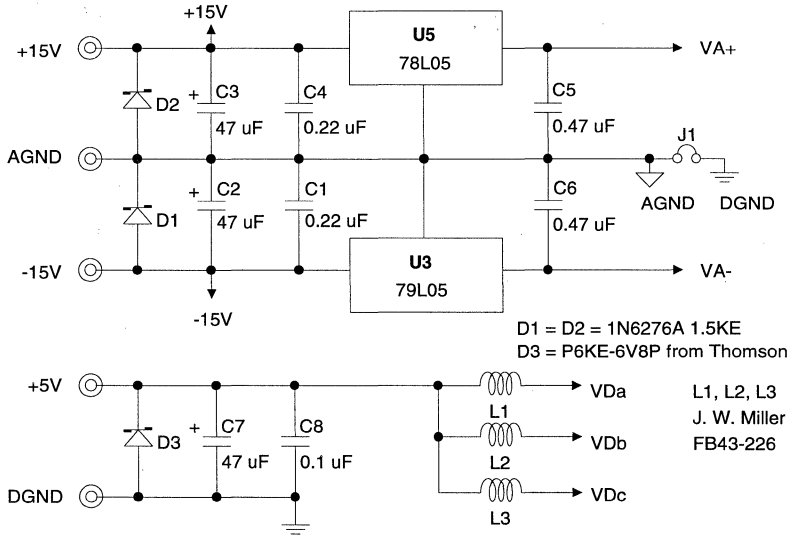


Figure 2. Power Supply Circuitry

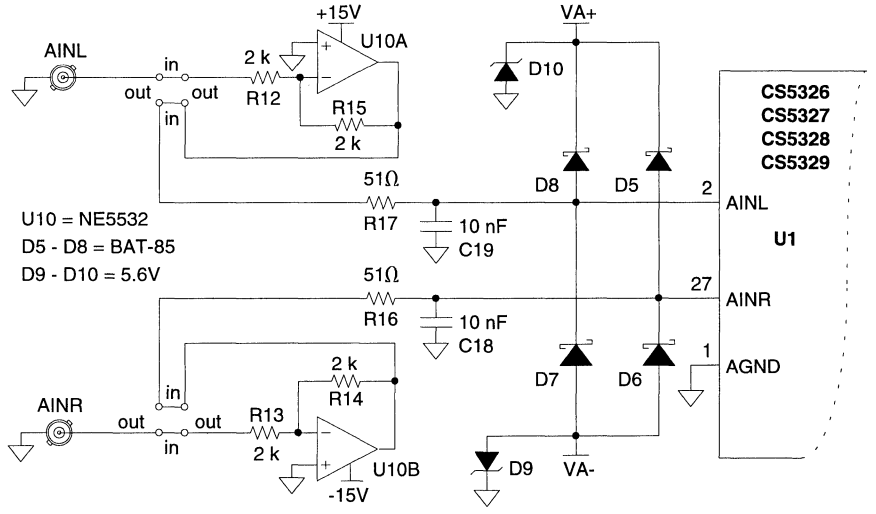


Figure 3. ADC Input Buffer and Protection Circuitry

CLOCK/TIMING GENERATOR

A 12.288 MHz clock signal is provided by the onboard oscillator X1. U9B performs a divide by 2 of the clock signal to supply a 6.144 MHz clock to the ADC and the Digital Audio Line Driver to support a 48kHz sample rate. An external master clock may be connected to the EXTCLKIN BNC connector if the onboard oscillator is removed.

As recommended in the converter's data sheet, ACLKA is inverted and connected to SCLK to clock data out of the converter at half the CLKIN frequency as shown in Figure 5. To generate the L/$\overline{R}$ signal, ACLKA is divided by 64 with the counter U7 shown in Figure 9. Since U7 is an asynchronous counter that advances on falling edges of ACLKA, U8A insures that L/$\overline{R}$ meets the t_{clr}, t_{aclr}, and t_{scklr} timing requirements specified in the converter's data sheet. The divide by 32 output of U7 is also used to generate the LCLK signal for use with an external parallel output interface.

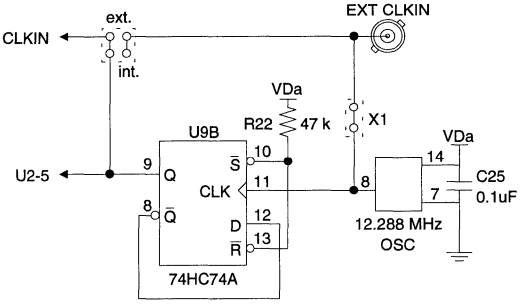


Figure 4. Clock Generator

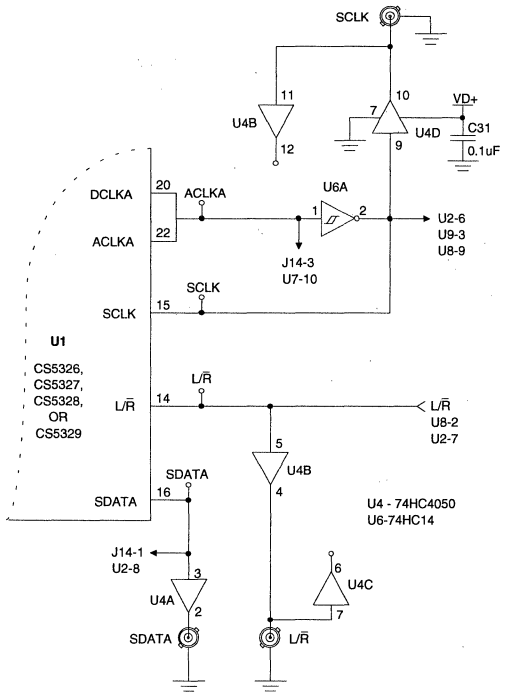


Figure 5. Serial Input/Output

Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, and L/$\overline{R}$ BNC connectors on the evaluation board. These outputs are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. Serial data is clocked out of the converter by the SCLK signal at half of the master clock frequency. Note that in this configuration the serial output data is clocked out during the first part of each L/$\overline{R}$ cycle. After the data for the selected channel has been clocked out, zeros are clocked out during the remaining SCLK cycles before L/$\overline{R}$ changes state.

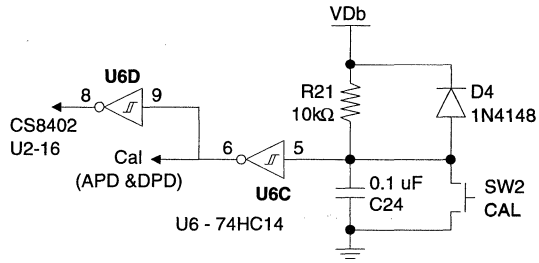


Figure 6. Offset Calibration Circuit

Reset/Offset Calibration Circuit

The circuit of Figure 6 provides a pulse to the Analog to Digital Converter's DPD and APD pins initiating an offset calibration cycle. This pulse will also reset U2, the Digital Audio Line Driver. The circuit is activated on power-up and when SW2 is closed.

Configuring the Board for External Timing

An external master clock may be supplied to the board directly via the EXTCLKIN input if the on board oscillator, X1 is removed. The board's SCLK and L/$\overline{R}$ connectors may also be configured to accept input signals. This is accomplished with a simple modification. Holes in the SCLK and L/$\overline{R}$ traces have been added to accommodate installing jumper wires and to facilitate breaking traces. Drilling through the surface pad of one of these holes with a small twist drill effectively breaks the trace and allows it to be driven by another source attached at an adjacent hole. This technique can be used to connect the converter to externally generated SCLK and L/$\overline{R}$ signals during system development. Note that the SCLK trace must be broken at U6A pin 2 and U4D pin 9 before it may be configured as an input. Similarly, the L/$\overline{R}$ trace must be broken at U4B pin 4 and U8 pin 2 before the BNC connector may be configured as an input.

Digital Audio Standard Interface

Included on the evaluation board is a CS8402 Digital Audio Line Driver. This device can implement AES/EBU, S/PDIF and EIAJ CP-340 interface standards. Figure 7 shows the schematic for the CS8402. The C, U and V bits can be driven from external logic using the CBL output for block synchronization. SW1 provides 8 DIP switches to select various modes and bits for the CS8402. Table 3 lists the settings for the professional mode which is the default setting for the evaluation board from the factory. Switch 8 selects between professional and consumer modes; however, the CS8402 output to the transformer must be modified, as shown in Figure 8, to be compatible with the consumer interface. Table 5 lists the switch settings for consumer mode. If the C input is used, the input bits are logically OR'ed with the appropriate DIP switch bits. In Tables 3 and 5, the 'C' bits listed in the comment section are taken from the Digital Audio Interface specifications. As an example, switch 4 in the professional mode (Table 3) controls $\overline{C9}$ which is the inverse of channel status bit 9 (also listed as byte 1, bit 1 in the CS8402 data sheet). Channel status bit 9 is one of four bits indicating channel mode. Therefore, using DIP switch 4, only two of the available channel modes may be selected. The C input port may be used to select other channel modes. See the CS8401 & CS8402 data sheet for more information on the operation of the CS8402.

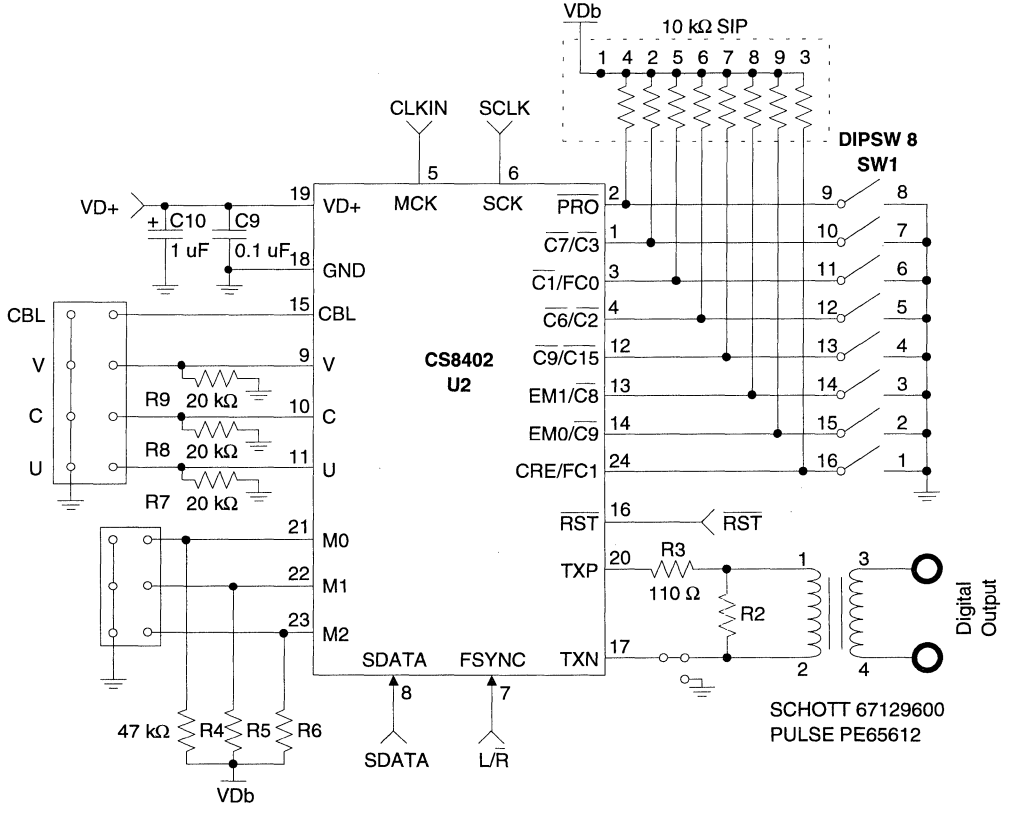


Figure 7. Digital Audio Line Connections

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15	input	+15 Volts from power supply
-15	input	-15 Volts from power supply
AGND	input	analog ground connection from power supply
+5	input	+5V for ADC VD1+ / VD2+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
L/$\overline{R}$	output	left /right channel signal
SDATA	output	serial output data
SCLK	output	serial output clock
J14	output	serial output data
Digital Output	output	CS8402 digital output via transformer

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J13	selects channel for serial to parallel conversion	*L	left channel data presented on J14
		R	right channel data presented on J14
		B	left then right channel data alternately presented on J14
J12	selects 16-bit or 18-bit parallel output word size	16	16-bit data on J14 for CS5326 and CS5327
		18	18-bit data on J14 for CS5327 and CS5329

* Default setting from factory

Table 2. System Connections

Switch#	0=Closed, 1=Open	Comment
8	$\overline{PRO}$=0	Professional Mode, C0=1 (default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated (channel status bytes 14-17 and byte 22)
5, 7	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
6	$\overline{C1}$	C1 - $\overline{Audio}$
default	1 0	0 - Normal Audio 1 - Non-Audio
4	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
3, 2	EM1, EM0	C2,C3,C4 - Emphasis
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 µs 111 - CCITT J.17

Table 3. CS8402 Switch Definitions - Professional Mode

M2	M1	M0	Format
0	0	0	0 - FSYNC & SCK Output
0	0	1	1 - Left/Right, 16-24 Bits
0	1	0	2 - Word Sync, 16-24 Bits
0	1	1	3 - Reserved
1	0	0	4 - Left/Right, I^2S Compatible
1	0	1	5 - LSB Justified, 16 Bits
1	1	0	6 - LSB Justified, 18 Bits
1	1	1	7 - MSB Last, 16-24 Bits

Table 4. CS8402A Audio Port Modes

* Default setting for CDB5326/7/8/9.

Switch#	0=Closed, 1=Open	Comment
8	$\overline{PRO}$=1	Consumer Mode, C0=0 (Note 1)
1, 6	FC1, FC0	C24,C25,C26,C27 - Sample Frequency (encoded 2 of 4 bits)
	0 0	0000 - 44.1 kHz
	0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
7	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1	000 - None
	0	100 - 50/15 µs
5	$\overline{C2}$	C2 - Copy/Copyright
	1	0 - Copy Inhibited/Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
4	$\overline{C15}$	C15 - Generation Status
	1	0 - Definition is based on category code.
	0	1 - See CS8402 Data Sheet, Appendix A
3, 2	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	0 0	1100000 - Digital Audio Tape - DAT

Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R3 to 374Ω, add R2 at 90.9Ω, cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided (see Figure 8). For a full explanation of the consumer hardware interface, see the CS8402 data sheet, Appendix B.

Table 5. CS8402 Switch Definitions - Consumer Mode

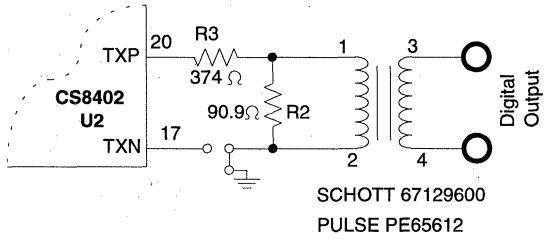


Figure 8. Hardware Connections for Consumer Mode

External Parallel Output Interface

Figure 10 is a suggested circuit which assembles 16-bit or 18-bit words from the serial data output on J14. J12, Figure 9, on the evaluation board selects the word size which should be set to "16" for use with the CS5326 and CS5327 and "18" for use with the CS5328 and CS5329. Each bit of serial data is clocked out of the converter on the rising edge of SCLK and shifted into the 24-bit shift register formed by U11, U12 and U13 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U11, U12 and U13 the data is latched onto P3 by the rising edge of LCLK.

J13, Figure 9, selects the channel whose output data will be converted to parallel form and presented on P3. With J13 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the falling edge of LCLK is used to clock the parallel data into the digital signal processor. LCLK may be jumpered from P1 to the "X" position of P3. Alternatively, a handshake protocol implemented with DACK and $\overline{\text{DRDY}}$ may be used to transfer data to the signal processor. The fall of $\overline{\text{DRDY}}$ informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that $\overline{\text{DRDY}}$ will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.

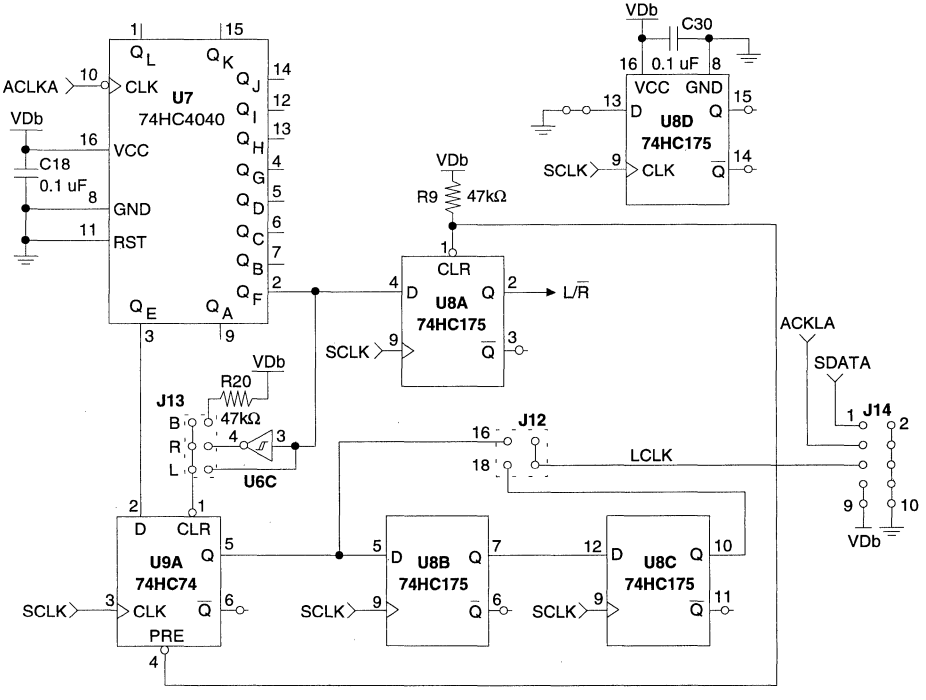


Figure 9. Timing Generator

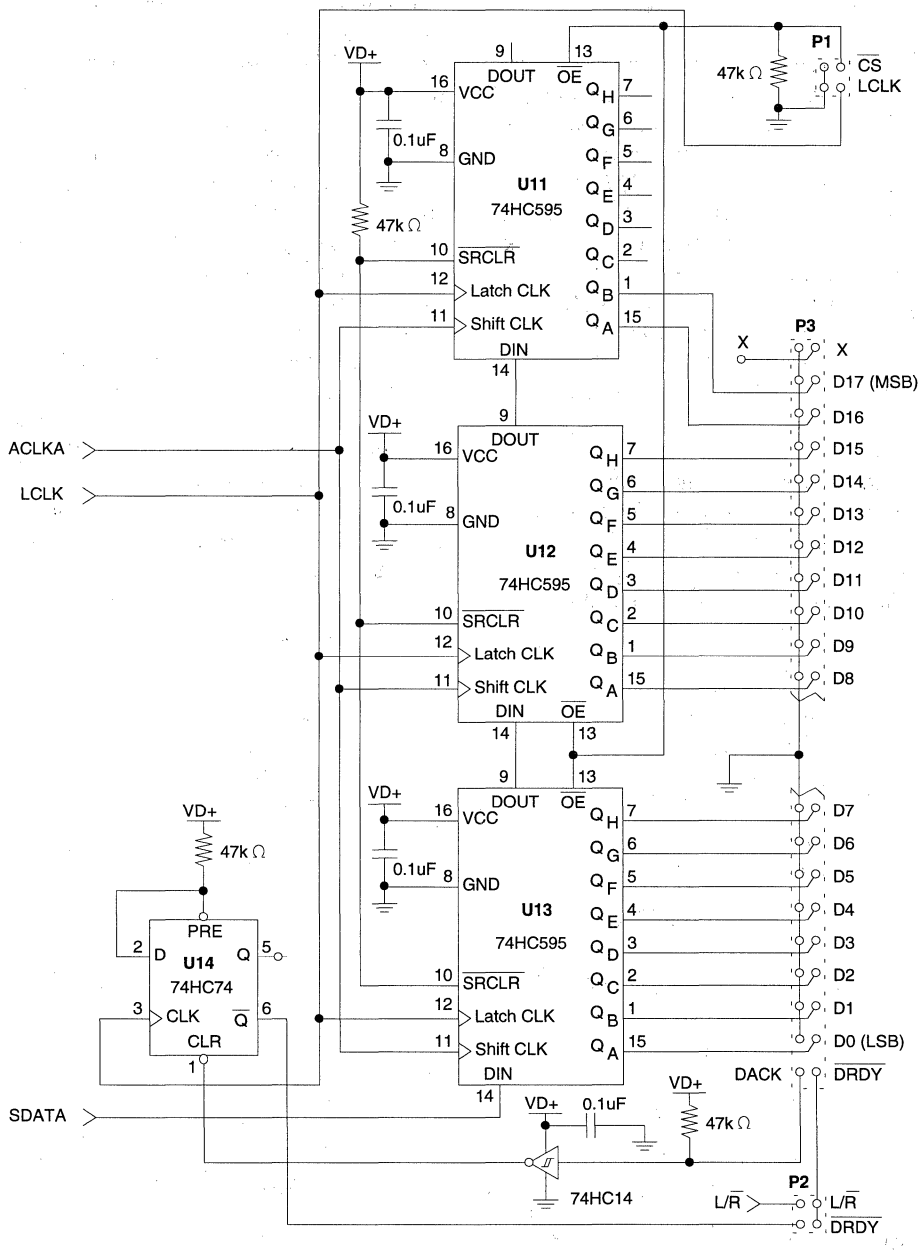


Figure 10. Suggested Serial to Parallel Interface
(Not provided on the evaluation board)

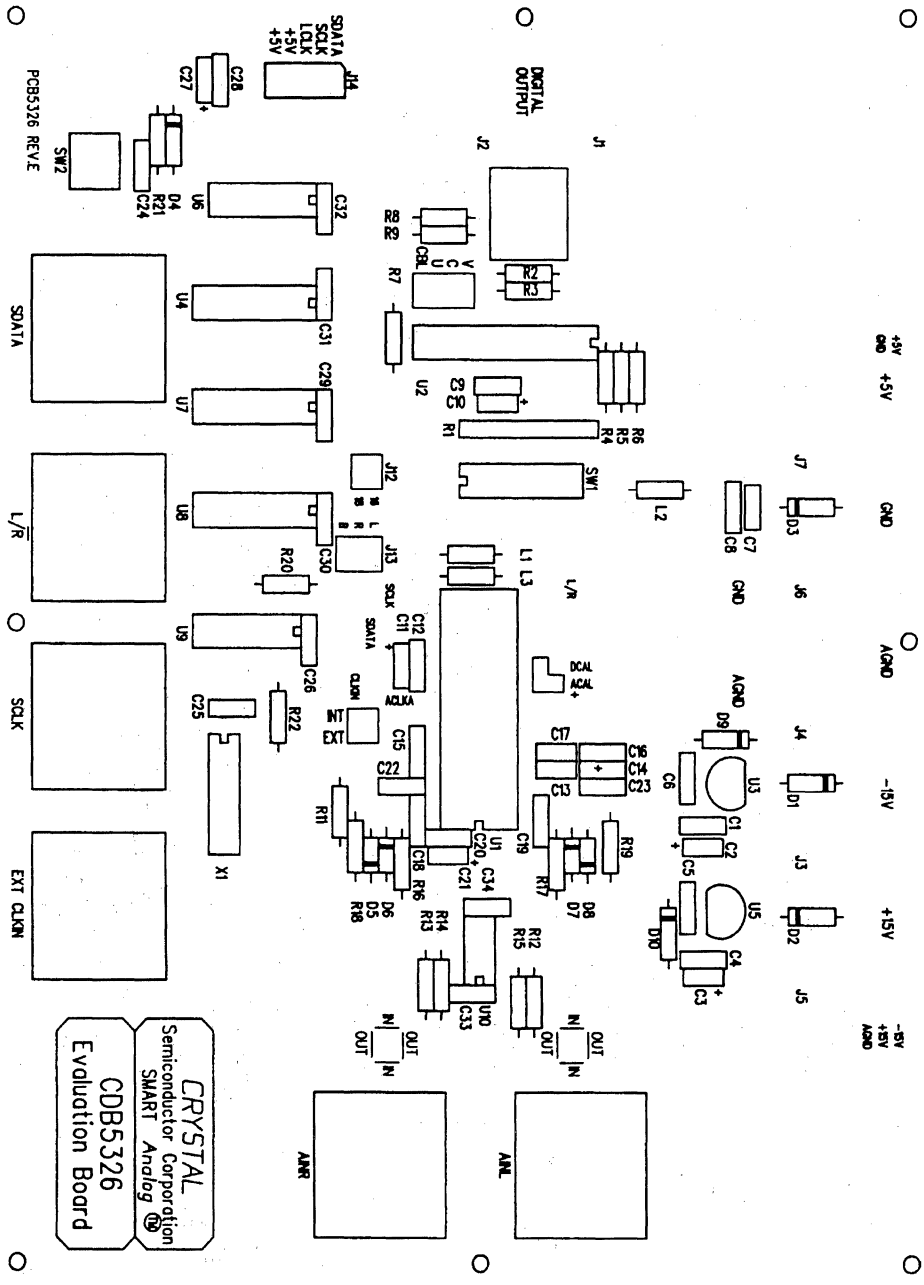


Figure 11. CDB5326/7/8/9 Rev. E. Layout

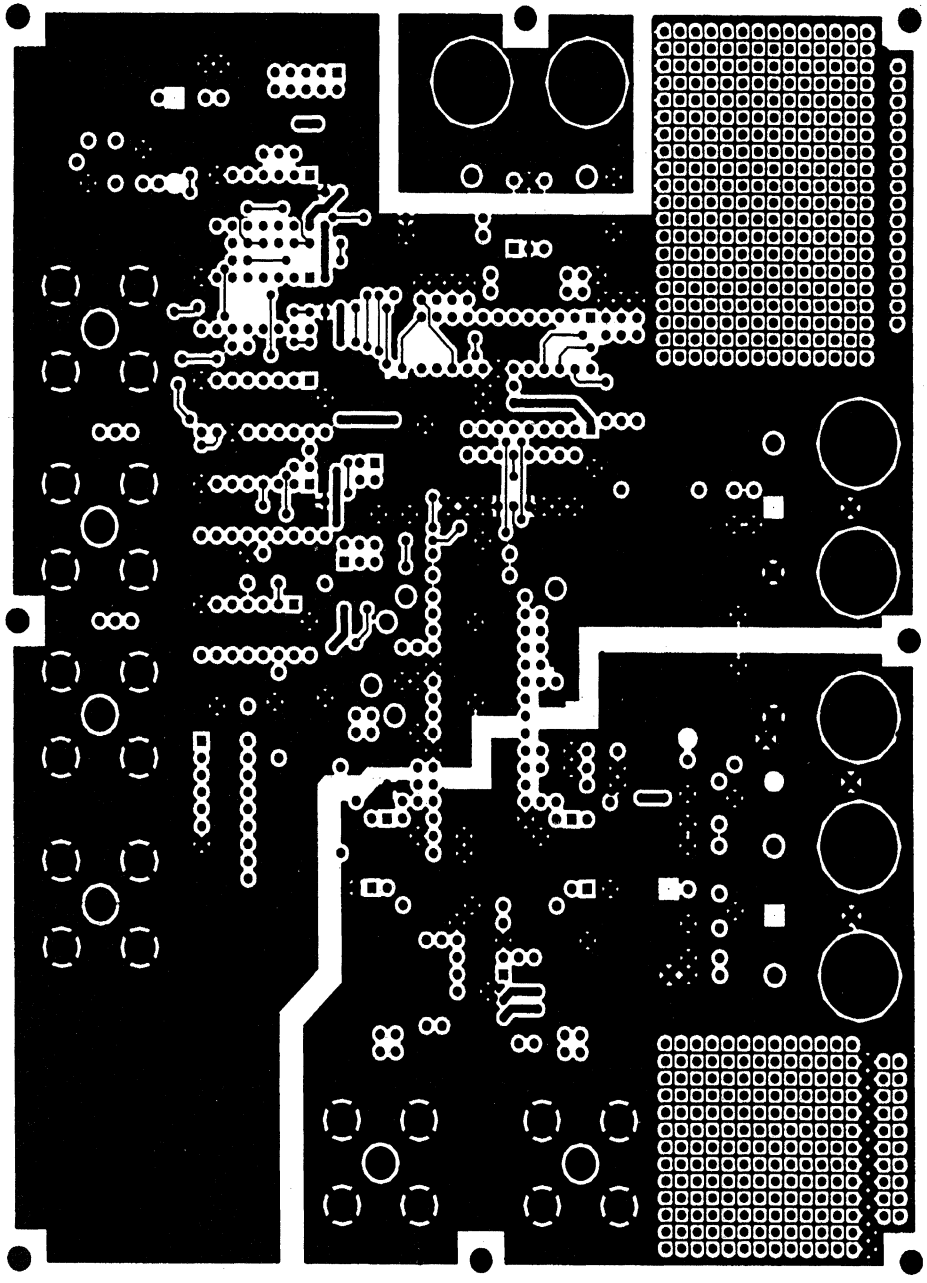


Figure 12. CDB5326/7/8/9 Rev. E. Component Side

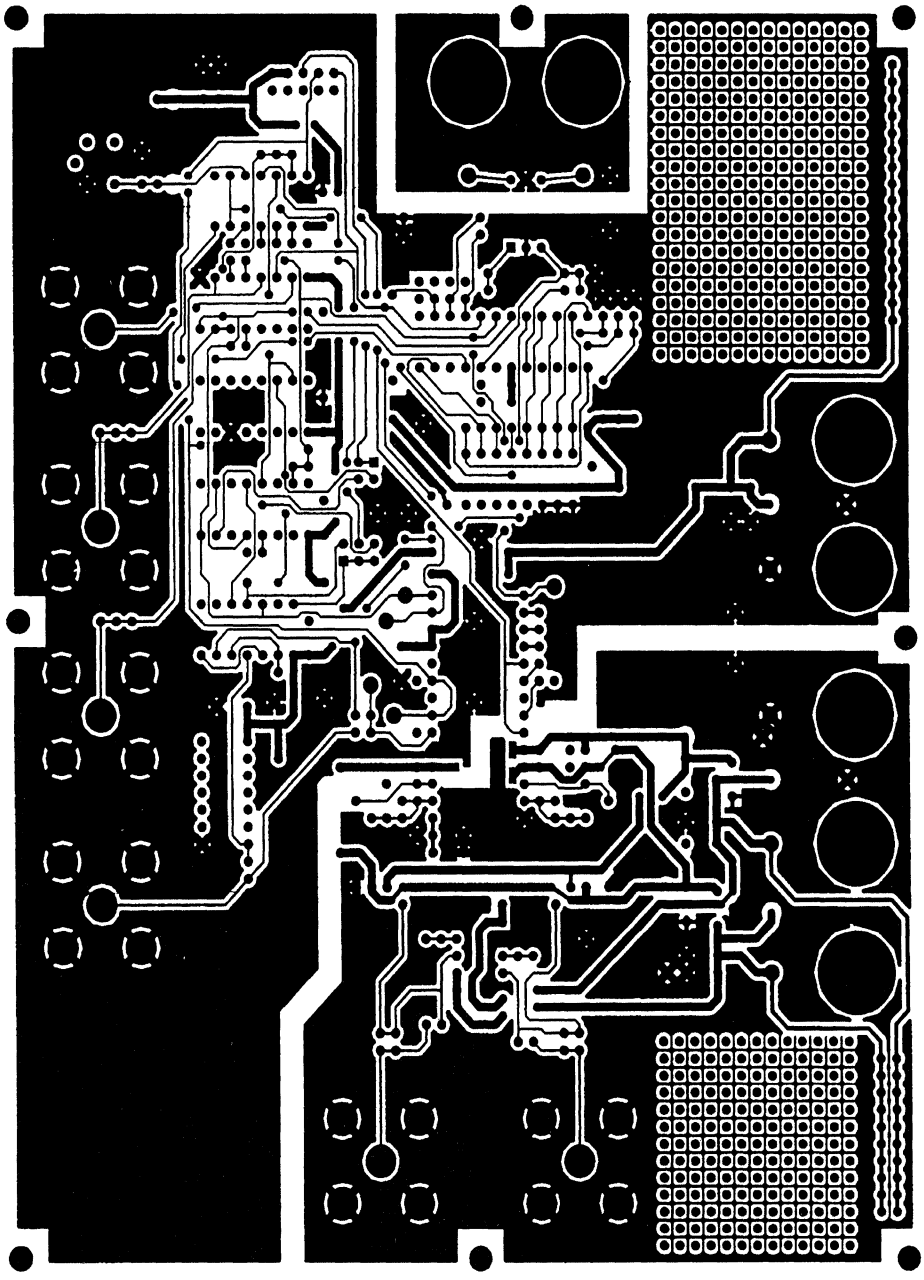


Figure 13. CDB5326/7/8/9 Rev. E. Solder Side

• Notes •

Semiconductor Corporation

16-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion >90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 400 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5336, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

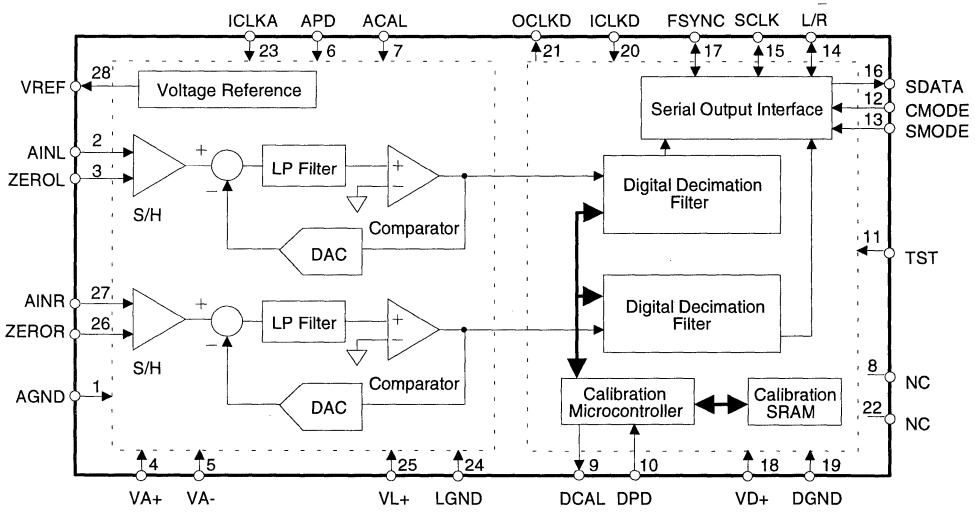
The ADCs use delta-sigma modulation with 64X over-sampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5339 has an SCLK which clocks out data on falling edges.

The CS5336 has a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package. Extended temperature range versions of the CS5336 are also available.

ORDERING INFORMATION: See Page 3-59



ANALOG CHARACTERISTICS

(Logic 0 = GND; Logic 1 = VD+; K grade: T_A = 25°C; B and T grades: $T_A = T_{MIN}$ to T_{MAX}; VA+, VL+,VD+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter	Symbol	CS5336,8,9-K Min	Typ	Max	CS5336-B Min	Typ	Max	CS5336-T Min	Typ	Max	Units
Specified Temperature Range	T_A	0	to	70	-40	to	+85	-55	to	+125	°C
Resolution		16	-	-	16	-	-	16	-	-	Bits
Dynamic Performance											
Dynamic Range		92.7	95.7	-	90	93.5	-	84	92	-	dB
Signal-to-(Noise + Distortion); THD+N	S/(N+D)	90.7	92.7	-	85	89	-	82	86	-	dB
Signal to Peak Noise		-	96	-	-	95	-	-	94	-	dB
Total Harmonic Distortion	THD	.0025	.001	-	.005	.001	-	.013	.005	-	%
Interchannel Phase Deviation		-	.0001	-	-	.0001	-	-	.0001	-	°
Interchannel Isolation (dc to 20 kHz)		100	106	-	90	106	-	83	96	-	dB
dc Accuracy											
Interchannel Gain Mismatch		-	0.01	0.05	-	.01	.05	-	.01	0.1	dB
Gain Error (includes Vref tolerance)		-	±1	±5	-	±2	±5	-	±3	±6	%
Gain Drift (includes Vref drift, Note 1)		-	25	-	-	70	-	-	70	-	ppm/°C
Bipolar Offset Error (Note 2)		-	±5	±15	-	±10	±30	-	±16	±65	LSB
Offset Drift (Note1)		-	15	-	-	20	-	-	20	-	ppm/°C
Analog Input											
Input Voltage Range (±Full Scale)	VIN	±3.5	±3.68	-	±-3.5	±3.68	-	±3.5	±3.68	-	V
Input Impedance	ZIN	-	65	-	-	65	-	-	65	-	kΩ
Power Supplies											
Power Supply Current (VA+)+(VL+)	IA+	-	25	35	-	25	35	-	25	35	mA
with APD, DPD low VA-	IA-	-	-25	-35	-	-25	-35	-	-25	-35	mA
(Normal Operation) VD+	ID+	-	30	45	-	30	45	-	30	50	mA
Power Supply Current (VA+)+(VL+)	IA+	-	10	50	-	10	50	-	10	50	µA
with APD, DPD high VA-	IA-	-	-10	-50	-	-10	-50	-	-10	-50	µA
(Power-Down Mode) VD+	ID+	-	10	400	-	10	400	-	10	400	µA
Power Consumption (APD, DPD Low)	PDN	-	400	575	-	400	575	-	400	600	mW
(APD, DPD High)	PDS	-	0.15	2.5	-	0.15	2.5	-	0.15	2.5	mW
Power Supply (dc to 26 kHz)	PSRR	-	54	-	-	54	-	-	54	-	dB
Rejection Ratio (26 kHz to 3.046 MHz)		-	100	-	-	100	-	-	100	-	dB

Notes:
1. This parameter is guaranteed by design and/or characterization.
2. After calibration with DCAL connected to ACAL, and ZEROL & ZEROR terminated to AGND with an impedance matched to the AINR & AINL source impedance. Executing a calibration with ACAL tied low (See Power Down and Offset Calibration section) will yield an offset error of typically less than ± 5LSB.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%; Output word rate of 48 kHz)

Parameter			Symbol	Min	Typ	Max	Units
Passband	(-3 dB)	CS5336		0	to	22	kHz
	(-3 dB)	CS5338, CS5339		0	to	24	kHz
	(-0.01 dB)	CS5336		0	to	20	kHz
	(-0.01 dB)	CS5338, CS5339		0	to	22	kHz
Passband Ripple				-	-	± 0.01	dB
Stopband		CS5336		26	to	3046	kHz
		CS5338, CS5339		28	to	3044	kHz
Stopband Attenuation		(Note 3)		80	-	-	dB
Group Delay (OWR = Output Word Rate)			t_{gd}	-	18/OWR	-	s
Group Delay Variation vs. Frequency			$\triangle t_{gd}$	-	-	0.0	us

Notes: 3. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±22kHz for the CS5338 & CS5339, or n x 3.072MHz ±20.0kHz for the CS5336, where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to GND)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V_{INA}	(VA-)- 0.3	(VA+)+ 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

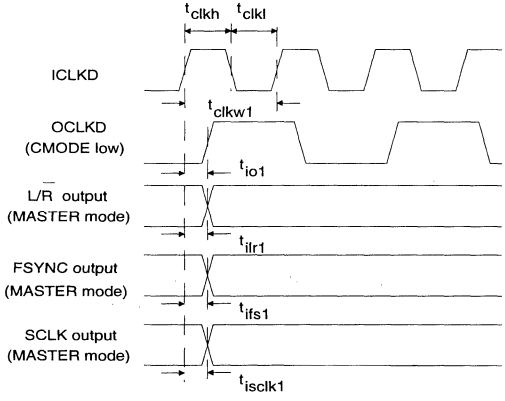
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

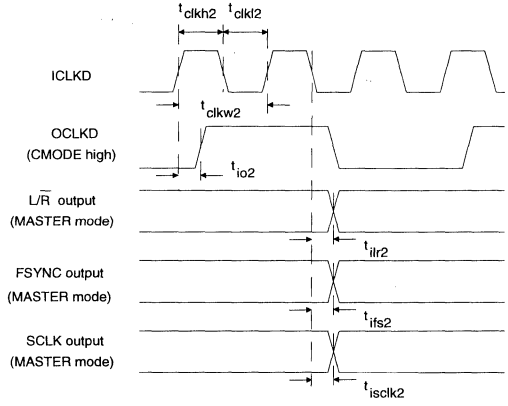
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low) (Note 6)	t_{clkw1}	78	-	3906	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	2604	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 4)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK rising to SDATA valid (MASTER mode, Note 5)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK rising to L/$\overline{R}$ (MASTER mode, Note 5)	t_{mslr}	-20	-	20	ns
SCLK rising to FSYNC (MASTER mode, Note 5)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK rising to SDATA valid (SLAVE mode, Note 5)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Falling SCLK to L/$\overline{R}$ edge delay (SLAVE mode, Note 5)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to falling SCLK setup time (SLAVE mode, Note 5)	t_{slr2}	30	-	-	ns
Falling SCLK to rising FSYNC delay (SLAVE mode, Note 5)	t_{sfs1}	30	-	-	ns
Rising FSYNC to falling SCLK setup time (SLAVE mode, Note 5)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	2 x tclkw	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}	-	4096	-	1/OWR

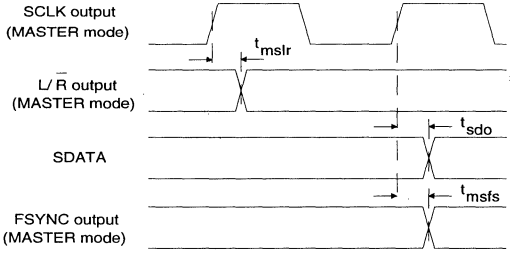
Notes:
4. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).
5. SCLK is shown for CS5336, CS5338. SCLK is inverted for CS5339.
6. Specifies minimum output word rate (OWR) of 1 kHz.



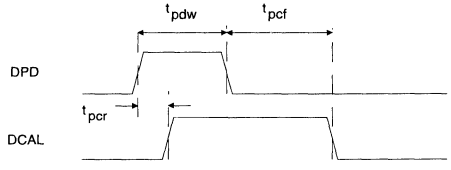
ICLKD to Outputs Propagation Delays (CMODE low)



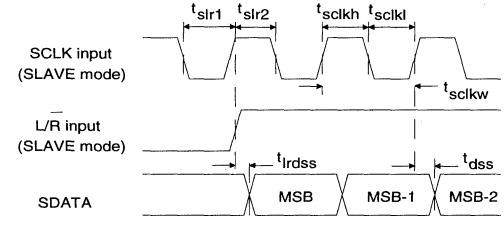
ICLKD to Outputs Propagation Delays (CMODE high)



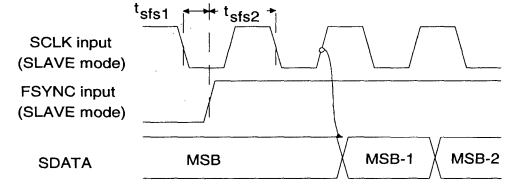
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	VA+	V
	Positive Logic	VL+	4.75	5.0	VA+	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	−4.75	−5.0	−5.25	V
Analog Input Voltage	(Note 7)	V_{AIN}	−3.68	-	3.68	V

Notes: 7. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification. Additional tag bits are output to indicate the amount of overdrive.

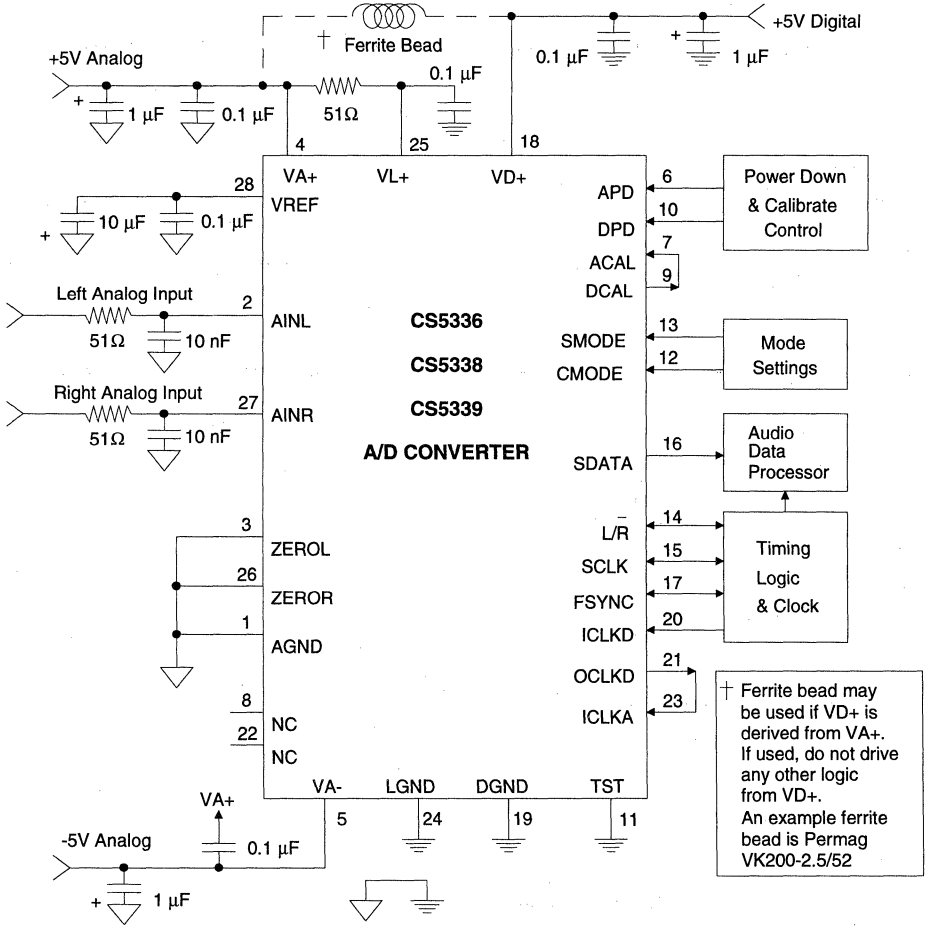


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5336, CS5338, and CS5339 are 16-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of ± 3.68 volts. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 400 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these ADCs, see the references at the end of this data sheet.

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

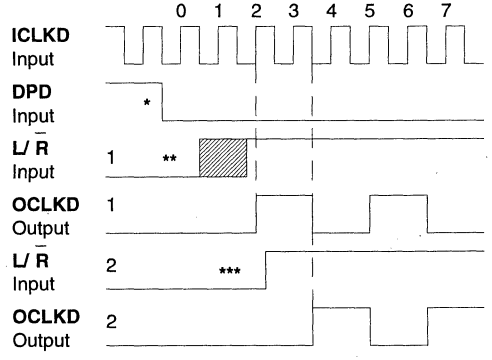
SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when CMODE



* DPD low is recognized on the next ICLKD rising edge (#0)
** L/$\overline{R}$ rising before ICLKD rising #2 causes OCLKD -1
*** L/$\overline{R}$ rising after ICLKD rising #2 causes OCLKD - 2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

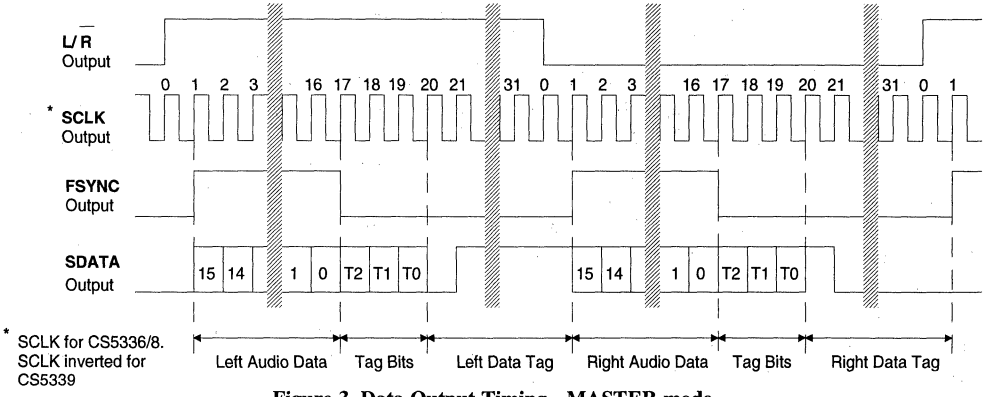


Figure 3. Data Output Timing - MASTER mode

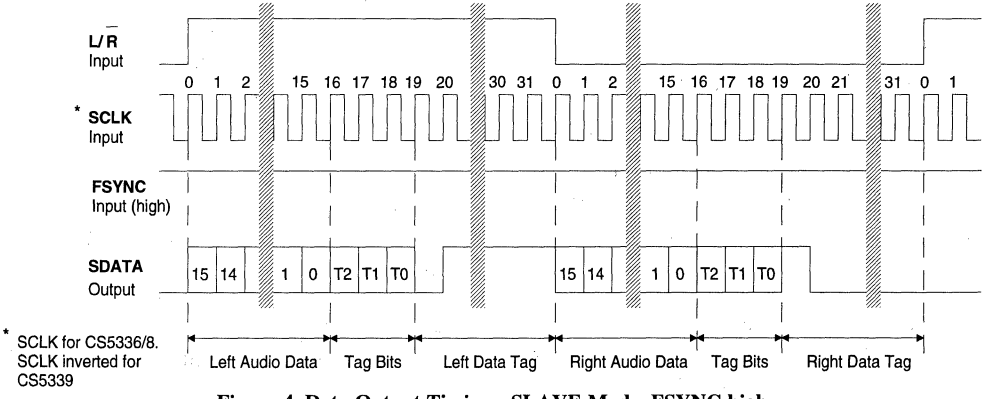


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between L/$\overline{R}$ edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode, L/$\overline{R}$ and SCLK are inputs. L/$\overline{R}$ must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The rising edge of SCLK causes the ADC to

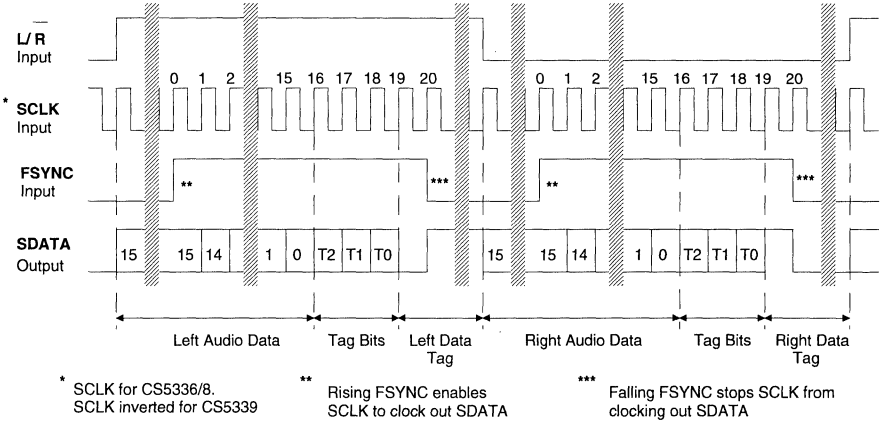


Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled

output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the L/$\overline{R}$ edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the L/$\overline{R}$ edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to position in time the data bits onto a common serial bus.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next L/$\overline{R}$ edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

In all modes, SCLK is shown for the CS5336 and CS5338, where data bits are clocked out on rising edges. SCLK is inverted for the CS5339.

Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125.x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

Table 2. Tag Bit Definition

Certain serial modes align well with various interface requirements. A CS5339 in MASTER mode, with an inverted L/$\overline{R}$ signal, generates I^2S (Philips) compatible timing. A CS5336 in MASTER mode, using FSYNC, interfaces well with a Motorola DSP56000. A CS5336 in SLAVE mode emulates a CS5326 style interface, and also links up to a DSP56000 in network mode.

Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically ± 3.68 volts.

The ADC samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). For the CS5336, the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5338 and CS5339, the digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51 Ω resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage reference output is brought out to the VREF pin. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 150 µW. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down feature, APD should be tied to AGND. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not

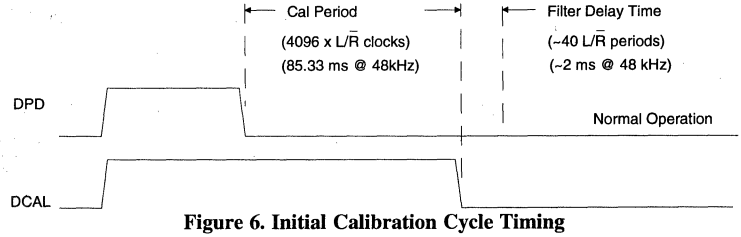


Figure 6. Initial Calibration Cycle Timing

greater than 10 µF, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 6, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multiplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 40 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean ± 5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF to Pin 1 AGND and to minimize the path between VREF and the capacitors. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Synchronization of Multiple CS5336/8/9

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD and APD pins to a single control signal and supplying the same ICLKD and L/$\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5336/8/9 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD/APD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD/APD pins to the same control signal and insuring that the DPD/APD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

FFT Tests

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 7 shows the spectral purity of the CS5336 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 95.41 dB.

Figure 8 shows the CS5336 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at 110 dB down.

Figure 9 shows the low-level performance of the CS5336. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 10 shows the same very low input amplitude performance, but at 9kHz input frequency.

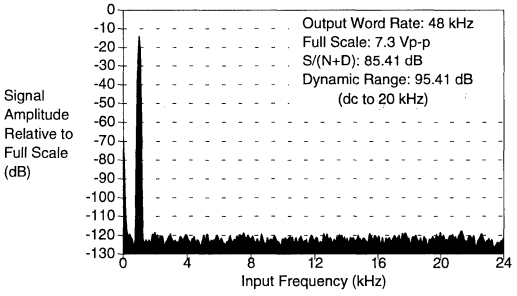


Figure 7. CS5336 FFT Plot with -10 dB, 1 kHz Input

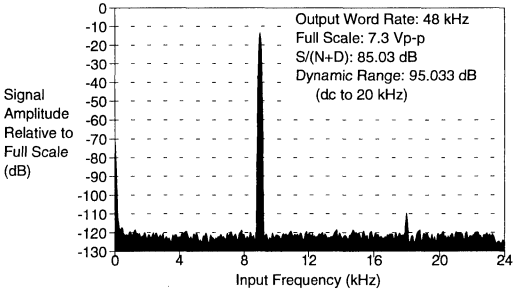


Figure 8. CS5336 FFT Plot with -10 dB, 9 kHz Input

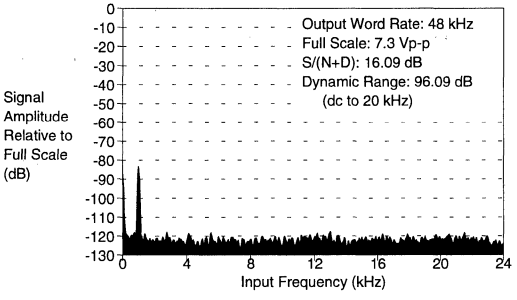


Figure 9. CS5336 FFT Plot with -80 dB, 1 kHz Input

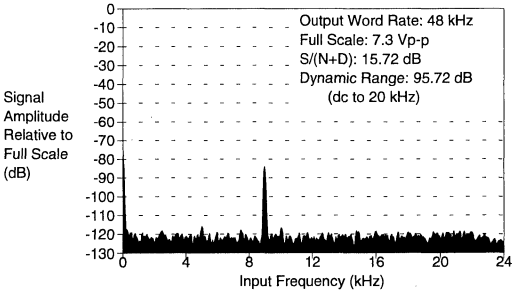


Figure 10. CS5336 FFT Plot with -80 dB, 9 kHz Input

DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the codewidths. Figure 11 shows the excellent Differential Non-Linearity of the CS5336. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within ± 0.2 LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 11 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

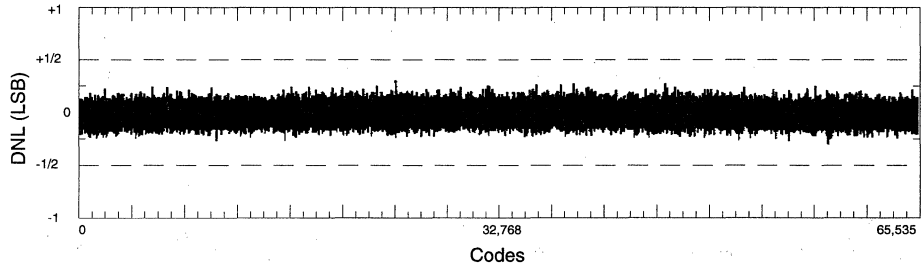


Figure 11. CS5336 Differential Non-Linearity Plot

Digital Filter

Figures 12 through 17 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to ± 0.01 dB maximum. Stopband rejection is greater than 80 dB.

Figures 12,14 &16 show the CS5338 and CS5339 filter characteristics. Figure 17 is an expanded view of the transition band.

Figures 13,15 & 17 show the CS5336 filter characteristics. Figure 17 is an expanded view of the transition band.

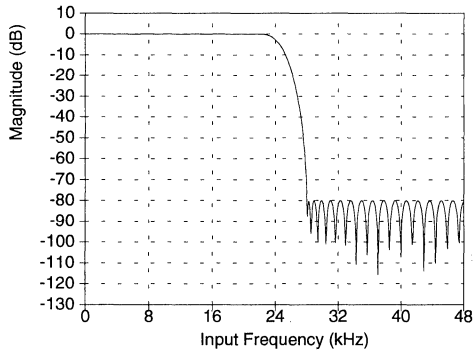


Figure 12. CS5338/9 Digital Filter Stopband Rejection

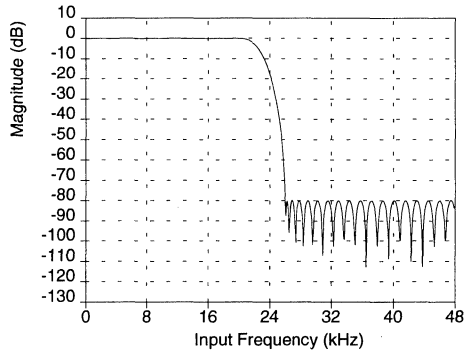


Figure 13. CS5336 Digital Filter Stopband Rejection

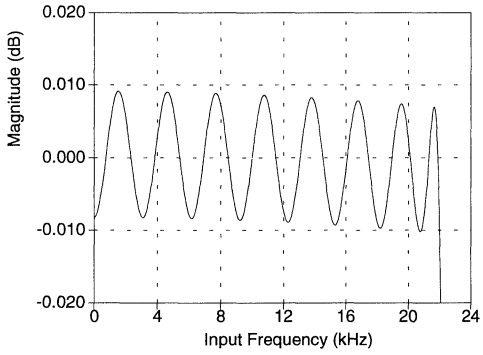


Figure 14. CS5338/9 Digital Filter Passband Ripple

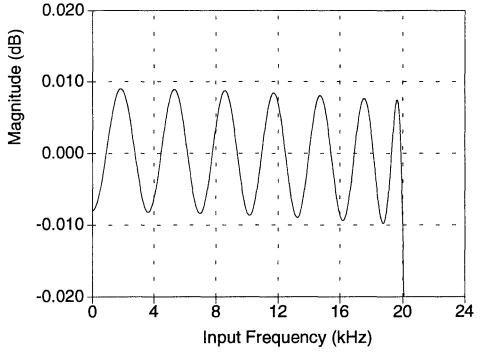


Figure 15. CS5336 Digital Filter Passband Ripple

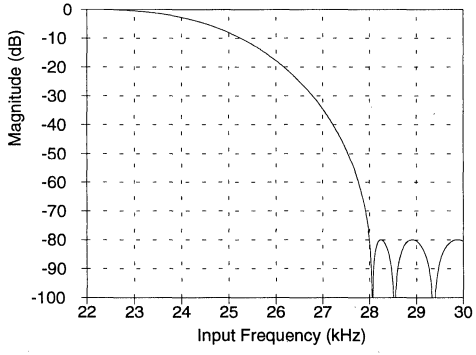


Figure 16. CS5338/9 Digital Filter Transition Band

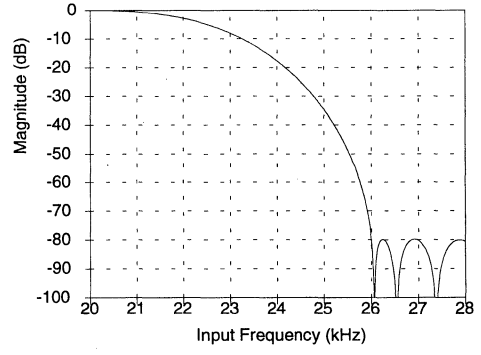
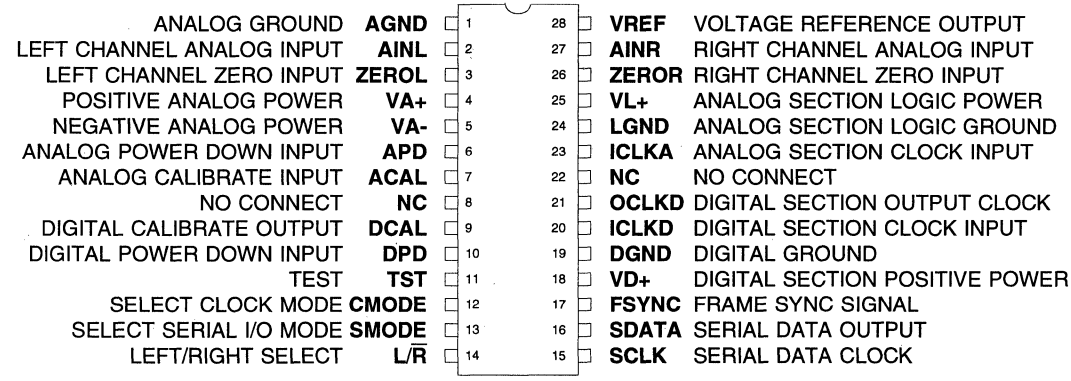


Figure 17. CS5336 Digital Filter Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 25.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 24
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27
Analog input connections for the left and right input channels. Nominally ±3.68 volts full scale.

ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks.

Analog Outputs

VREF - Voltage Reference Output, PIN 28.

Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 20.

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 $L/\overline{R}$ periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

CMODE - Clock Mode Select, PIN 12.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 13.

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and L/$\overline{R}$ are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/$\overline{R}$ are all inputs. In slave mode, L/$\overline{R}$, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

SDATA - Serial Data Output, PIN 16.

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 21.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 15.

Data is clocked out on the rising edge of SCLK for the CS5336 and CS5338. Data is clocked out on the falling edge of SCLK for the CS5339.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/$\overline{R}$ changes.

L/$\overline{R}$ - Left/Right Select, PIN 14.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/$\overline{R}$ is high, left channel data is on SDATA, except for the first SCLK cycle. When L/$\overline{R}$ is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/$\overline{R}$ changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. L/$\overline{R}$ frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 17.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/$\overline{R}$ transitions. If it is desired to delay the data bits from the L/$\overline{R}$ edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/$\overline{R}$ edge, independent of the state of FSYNC.

Miscellaneous

NC - No Connection, PINS 8, 22.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 11.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Signal-to-(Noise plus Distortion) Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

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1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5336-KP	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-BP	16-bits	22 kHz	↑ active	-40 to +85 °C	28-pin Plastic DIP
CS5338-KP	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5339-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-KS	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5336-BS	16-bits	22 kHz	↑ active	-40 to +85 °C	28-pin SOIC
CS5338-KS	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5339-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5336-TC	16-bits	22 kHz	↑ active	-55 to +125 °C	28-pin Sidebrazed Ceramic DIP

CDB5336	CS5336 Evaluation Board
CDB5338	CS5338 Evaluation Board
CDB5339	CS5339 Evaluation Board

Semiconductor Corporation

CDB5336
CDB5338 CDB5339

Evaluation Board for CS5336, CS5338 & CS5339

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, S/PDIF & CP-340 Compatible Digital Audio
- Buffered Serial Output Interface
- 16-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

General Description

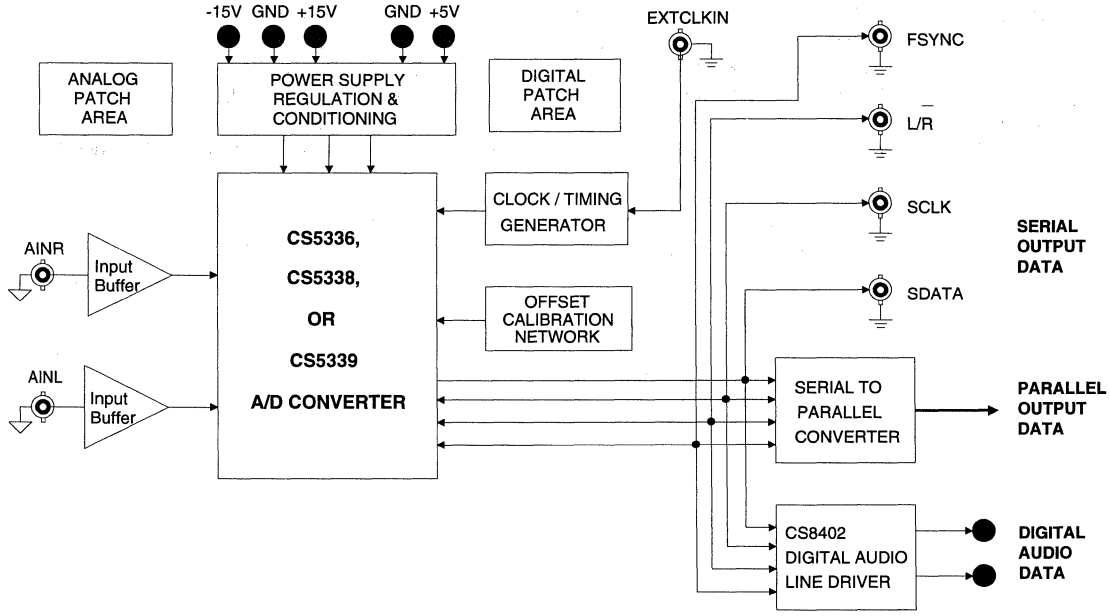
The CDB5336, CDB5338 & CDB5339 evaluation boards allow fast evaluation of the CS5336, CS5338 and CS5339 16-bit, stereo A/D converters. The boards generate all converter timing signals and provide both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

Also included is a CS8402 digital audio transmitter I.C., which can generate AES/EBU, S/PDIF & EIAJ CP-340 compatible audio data.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:

CDB5336, CDB5338, CDB5339



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Power Supply Circuitry

The schematic diagram in Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The ±5 Volt analog power supply inputs of the converter are derived from ±15 Volts using the voltage regulators U10 and U11. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts. D1, D2 and D4 are transient suppressors which also provide protection from incorrectly connected power supply leads. C25-C28, C30 and C31 provide general power supply filtering for the analog supplies. As shown in Figure 2, C10-C13 provide localized decoupling for the converter VA+ and VA- pins. Note that C13 is connected between VA- and VA+ and not VA- and AGND. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the converter's VD+ input directly from the VA+ supply. Note that the trace connecting the VD+ power to the VD+ of the converter must be broken before L1 may be installed. R5 and C7 low-pass filter the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point by J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

Offset Calibration & Reset Circuit

Figure 1, shows the optional offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Analog-to-Digital Converter's DPD pin initiating an offset calibration cycle. Releasing SW1 also initiates an offset calibration cycle. P6 (see Figure 2) selects the signal source used during offset calibration. In the "AIN" position, the AINL and AINR inputs are selected during calibration, while in the "ZERO" position, the ZEROL and ZEROR inputs are selected.

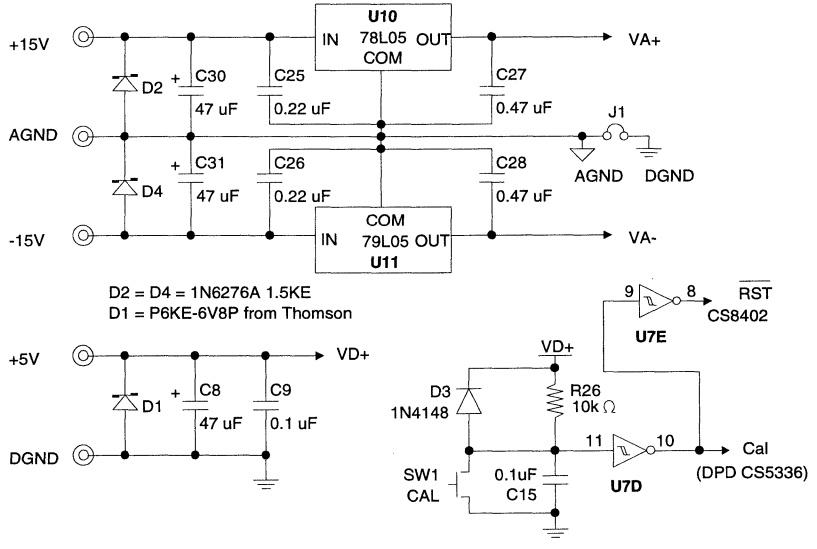


Figure 1. Power Supply and Reset Circuitry

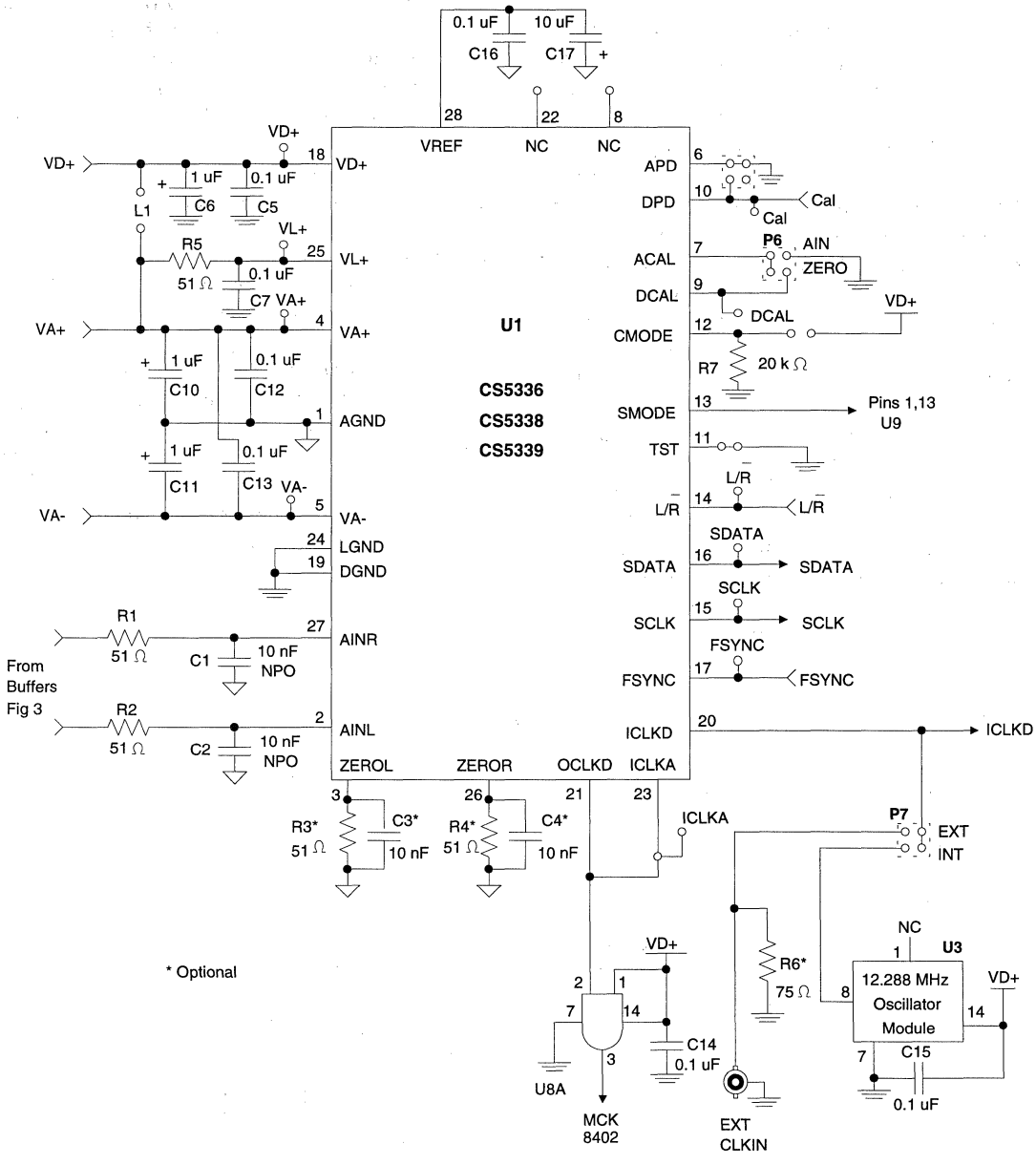


Figure 2 ADC Connections

Analog Inputs

As shown in Figure 2, the analog input signals are connected to the CS5336 via an RC network. R1 and C1 provide antialiasing and optimum source impedance for the right analog input channel while R2 and C2 do so for the left channel. The ZEROR and ZEROL inputs are tied to the analog ground plane on the board as shipped from the factory, but space is provided for an optional RC section on each. These RC sections may be added to model the output impedance of the analog signal source to minimize offset error during calibration.

Figure 3 shows the optional input buffer circuit. This can be used as an example input buffer circuit for your application. If the ADC is driven from a 50Ω source impedance signal generator, the input buffer amplifiers may be bypassed. Place P8 and P9 jumpers in the OUT position, and short circuit R1 and R2. This ensures that the ADC is driven from a 50Ω source resistance. Also remove U13 op-amp, to remove the 1kΩ load impedance.

Timing Generator

P7 selects the master clock source supplied to the ICLKD pin of the converter. As shipped from the factory, P7 is set to the "INT" position to select the 12.288 MHz clock signal provided by U3. An external master clock signal may be connected to the EXTCLKIN connector and selected by placing P7 in the "EXT" position. Note that R6, tied between EXTCLKIN and GND, is available for impedance matching an external clock source. The board is shipped with SMODE high, which selects MASTER timing mode. In this mode, SCLK, L/$\overline{R}$ and FSYNC are all outputs, generated by the converter from ICLKD.

Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, FSYNC and L/$\overline{R}$ BNC connectors on the evaluation board. These out-

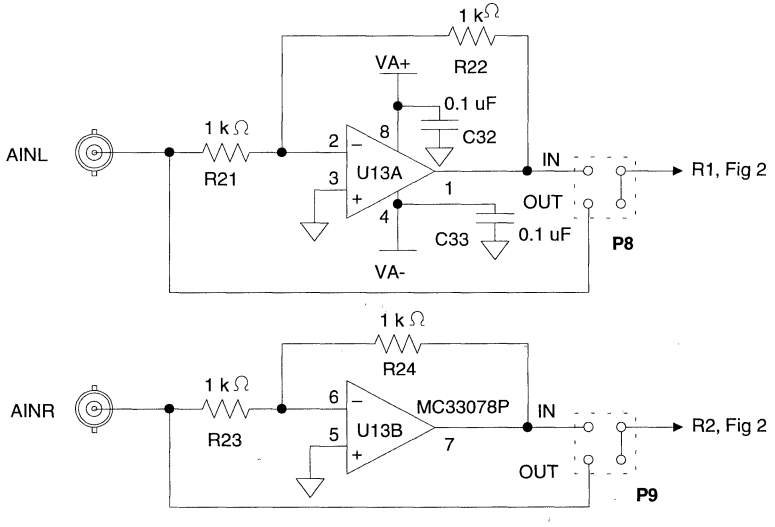


Figure 3. Input Buffer Circuit

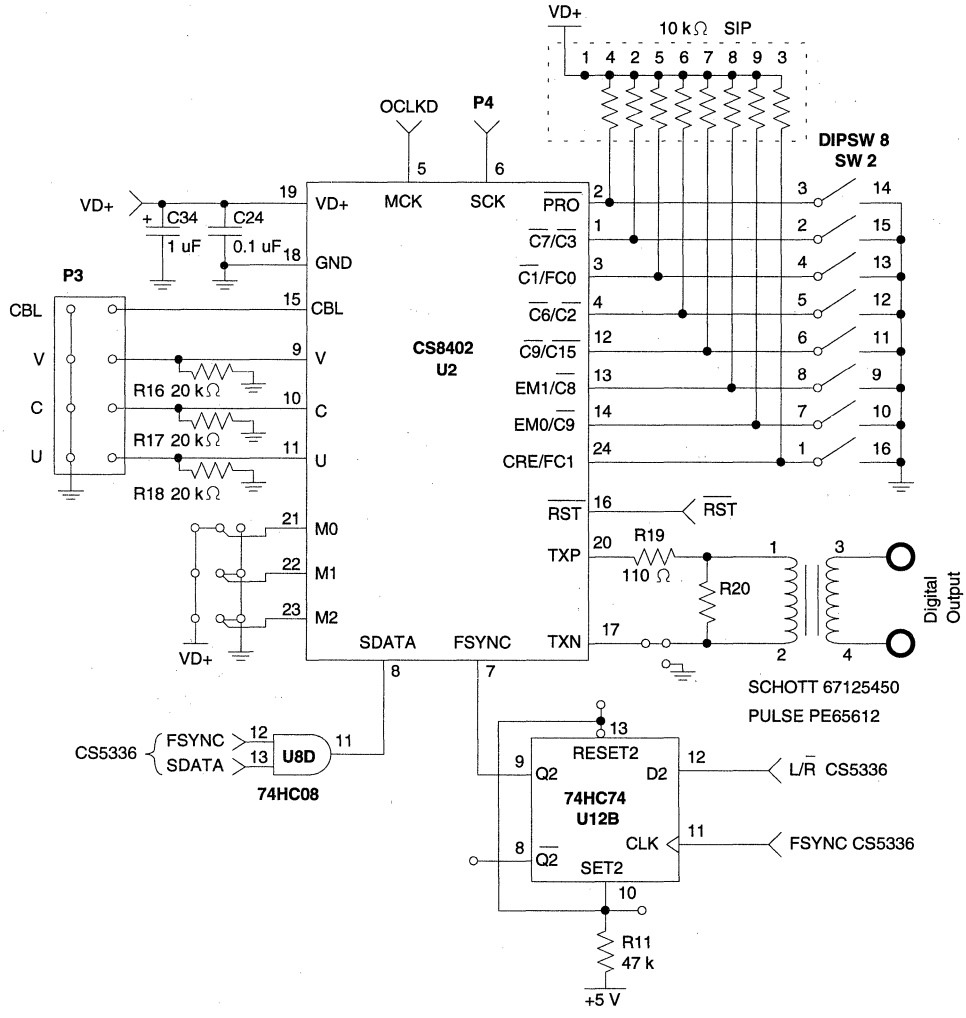


Figure 4. CS8402 Digital Audio Line Driver Connections

puts are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. If slave mode is selected by pulling SMODE low, then U9 (74HC243) will change to the opposite direction, and act as an input buffer. U9 is provided to protect against inadvertent external driving of SCLK, L/R and FSYNC while in MASTER mode. U9 is not necessary in your application circuit.

Jumper P4 allows the board to be configured for either the CS5336/38, or the CS5339, which have opposite polarities of SCLK.

Parallel Output Interface

Figure 6 depicts the parallel output interface on the evaluation board. 16-bit words are assembled from the serial data output of the converter. Each bit of serial data is clocked out of the converter

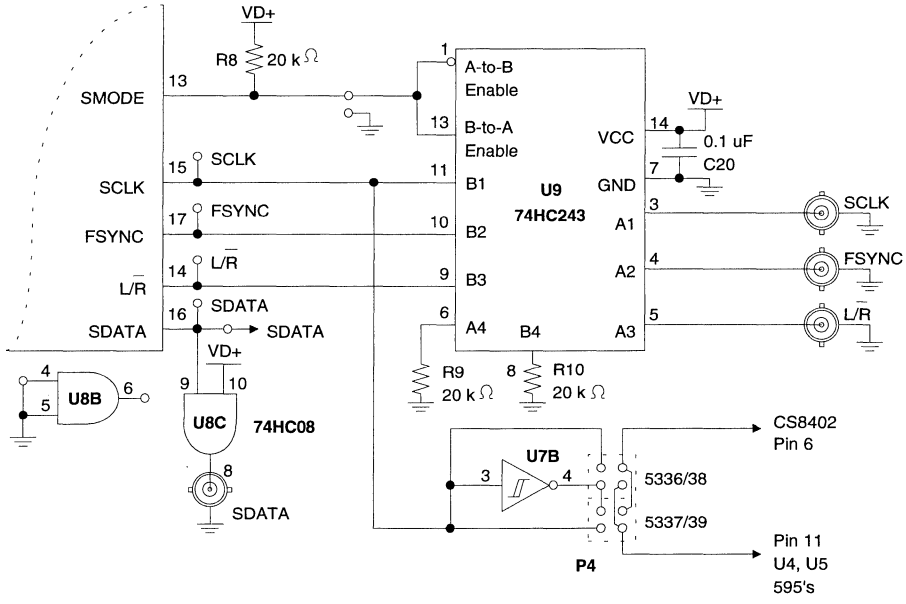


Figure 5. Serial Output Interface

on the rising edge of SCLK and shifted into the 16-bit shift register formed by U4 and U5 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U4 and U5 the data is latched onto P1 by a delayed version of FSYNC.

P5 selects the channel whose output data will be converted to parallel form and presented on P1. With P5 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the edges of L/$\overline{R}$ may be used to clock the parallel data into the digital signal processor. (Set jumper P2 into the L/$\overline{R}$ position.) Alternatively, a handshake protocol implemented with DACK and $\overline{DRDY}$ may be used to transfer data to the signal processor. (Set jumper P2 to the $\overline{DRDY}$ position.) The fall of $\overline{DRDY}$ informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that $\overline{DRDY}$ will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.

Digital Audio Standard Interface

Included on the evaluation board is a CS8402 Digital Audio Line Driver. This device can implement AES/EBU, S/PDIF and EIAJ CP-340 interface standards. Figure 4 shows the schematic for the CS8402. P3 allows the C, U and V bits to be driven from external logic using the CBL output for block synchronization. SW2 provides 8 DIP switches to select various modes and bits for the CS8402. Table 3 lists the settings for the professional mode which is the default setting for the evaluation board from the factory. The third switch selects between professional

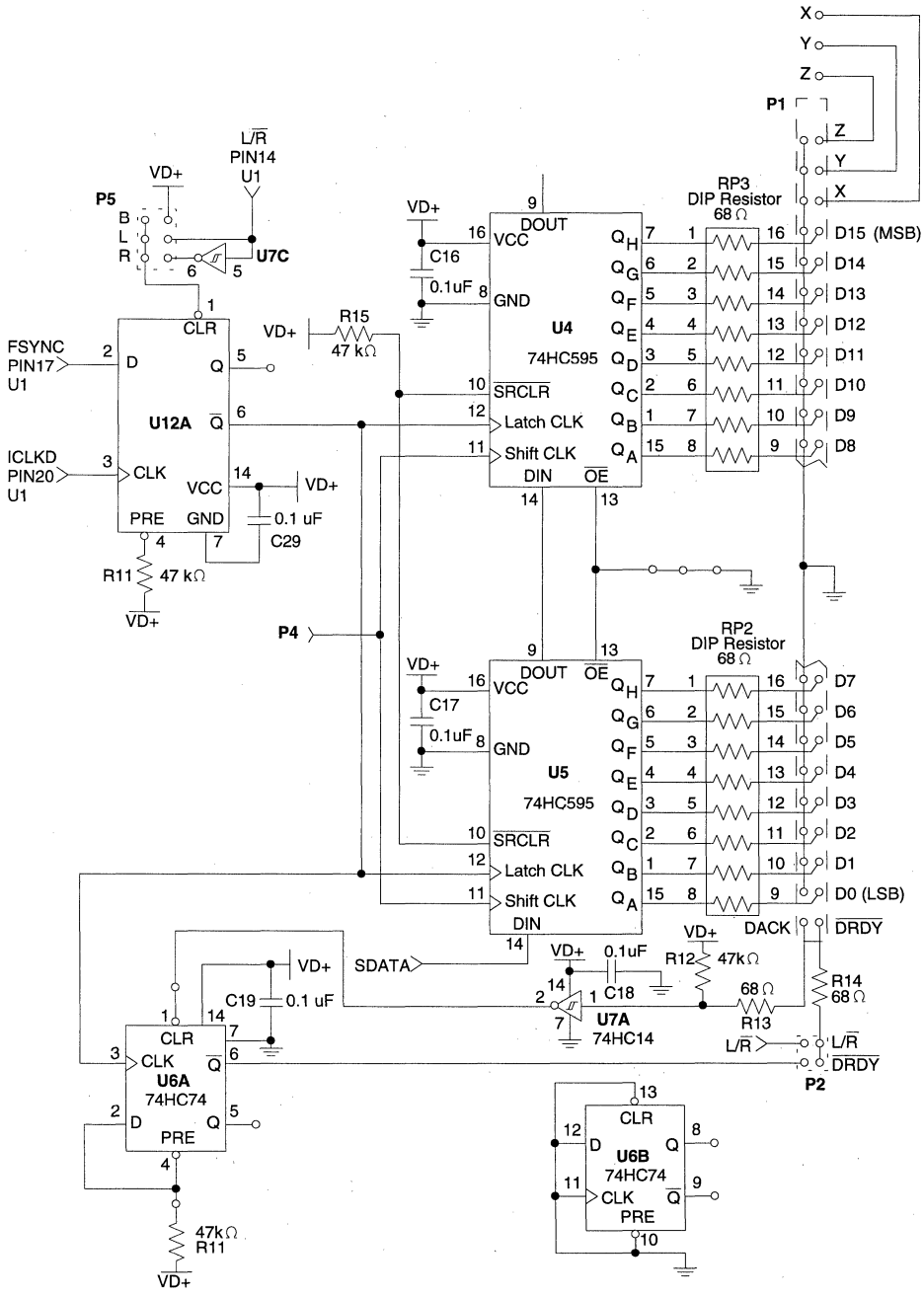


Figure 6. Parallel Output Interface

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15	input	+15 Volts from power supply
-15	input	-15 Volts from power supply
AGND	input	analog ground connection from power supply
+5	input	+5V for ADC VD+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
L/$\overline{R}$	output/input	left /right channel signal
SDATA	output	serial output data
SCLK	output/input	serial output clock
FSYNC	output/input	data framing signal
DIGITAL OUTPUT	output	CS8402 digital output via transformer
P3	output/input	CS8402 C,U,V inputs; CBL output
P1	output	parallel output data

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
P6	selects offset calibration input source	AIN	AINL and AINR selected during offset calibration
		*ZERO	ZEROL and ZEROR selected during offset calibration
P7	selects master clock source for CS5326 CLKIN	*INT	CLKIN provided by U3
		EXT	CLKIN provided by EXTCLKIN BNC
P5	selects channel for serial to parallel conversion	*L	left channel data presented on P1
		R	right channel data presented on P1
		B	left then right channel data alternately presented on P1
P2	selects L/$\overline{R}$ or $\overline{DRDY}$ as the output status signal presented on P1	*$\overline{DRDY}$	$\overline{DRDY}$ selected to signal the arrival of new data for the selected channel
		L/$\overline{R}$	L/$\overline{R}$ selected
P8, P9	selects optional input buffers	*IN	Buffer amplifier in circuit
		OUT	Buffer amplifier bypassed
P4	selects device type	5337/39	Correct SCLK for CS5337 & CS5339
		5336/38	Correct SCLK for CS5336 & CS5338

* Default setting from factory

Table 2. Jumper Selectable Options

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=0	Professional Mode, C0=1 (default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated (channel status bytes 14-17 and byte 22)
5, 2	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	$\overline{C1}$	C1 - $\overline{Audio}$
default	1 0	0 - Normal Audio 1 - Non-Audio
6	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8, 7	EM1, EM0	C2,C3,C4 - Emphasis
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 µs 111 - CCITT J.17

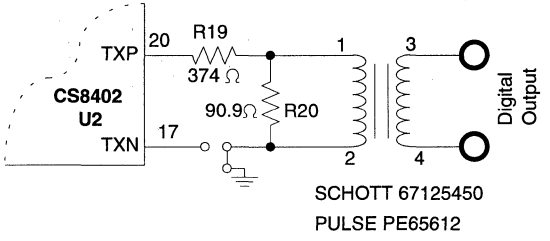
Table 3. CS8402 Switch Definitions - Professional Mode

and consumer modes; however, the CS8402 output to the transformer must be modified, as shown below Table 4, to be compatible with the consumer interface. Table 4 lists the switch settings for consumer mode. If the C input of connector P3 is used, the input bits are logically OR'ed with the appropriate DIP switch bits. In Tables 3 and 4, the 'C' bits listed in the comment section are taken from the Digital Audio Interface specifications. As an example, switch 6 in the professional mode (Table 3) controls $\overline{C9}$ which is the inverse of channel status bit 9 (also listed as byte 1, bit 1 in the CS8402 data sheet). Channel status bit 9 is one of four bits indicating channel mode. Therefore, using DIP switch 6, only two of the available channel modes may be selected. The C input port on connector P3 may be used to select other channel modes. See the CS8401 & CS8402 part data sheet for more information on the operation of the CS8402.

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=1	Consumer Mode, C0=0 (Note 1)
1, 4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency (encoded 2 of 4 bits)
	0 0	0000 - 44.1 kHz
	0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
2	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1	000 - None
	0	100 - 50/15 µs
5	$\overline{C2}$	C2 - Copy/Copyright
	1	0 - Copy Inhibited/Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
6	$\overline{C15}$	C15 - Generation Status
	1	0 - Definition is based on category code.
	0	1 - See CS8402 Data Sheet, Appendix A
8, 7	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	0 0	1100000 - Digital Audio Tape - DAT

Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R19 to 374Ω and add R20 at 90.9Ω. Then, as shown in the figure below, cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided. For a full explanation of the consumer hardware interface, see the CS8402 data sheet, Appendix B.

Table 4. CS8402 Switch Definitions - Consumer Mode



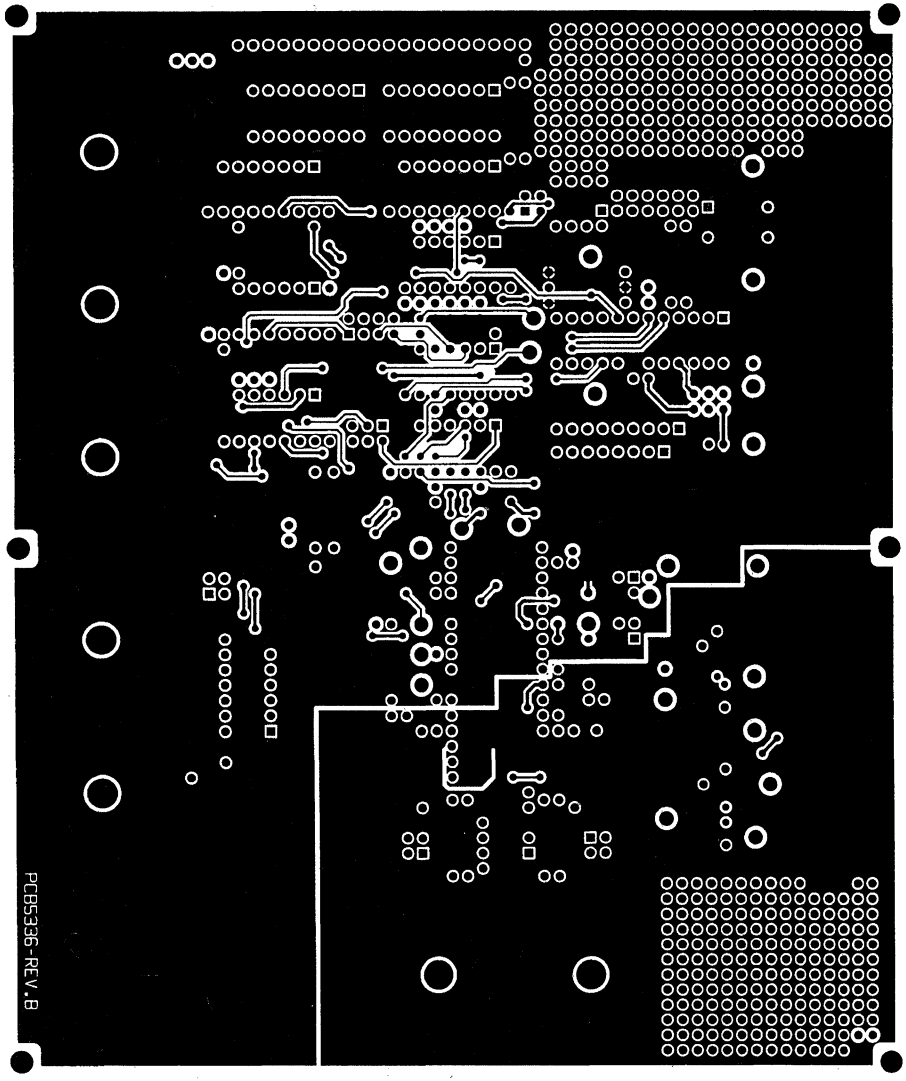


Figure 7. Top Ground Plane Layer (NOT TO SCALE)

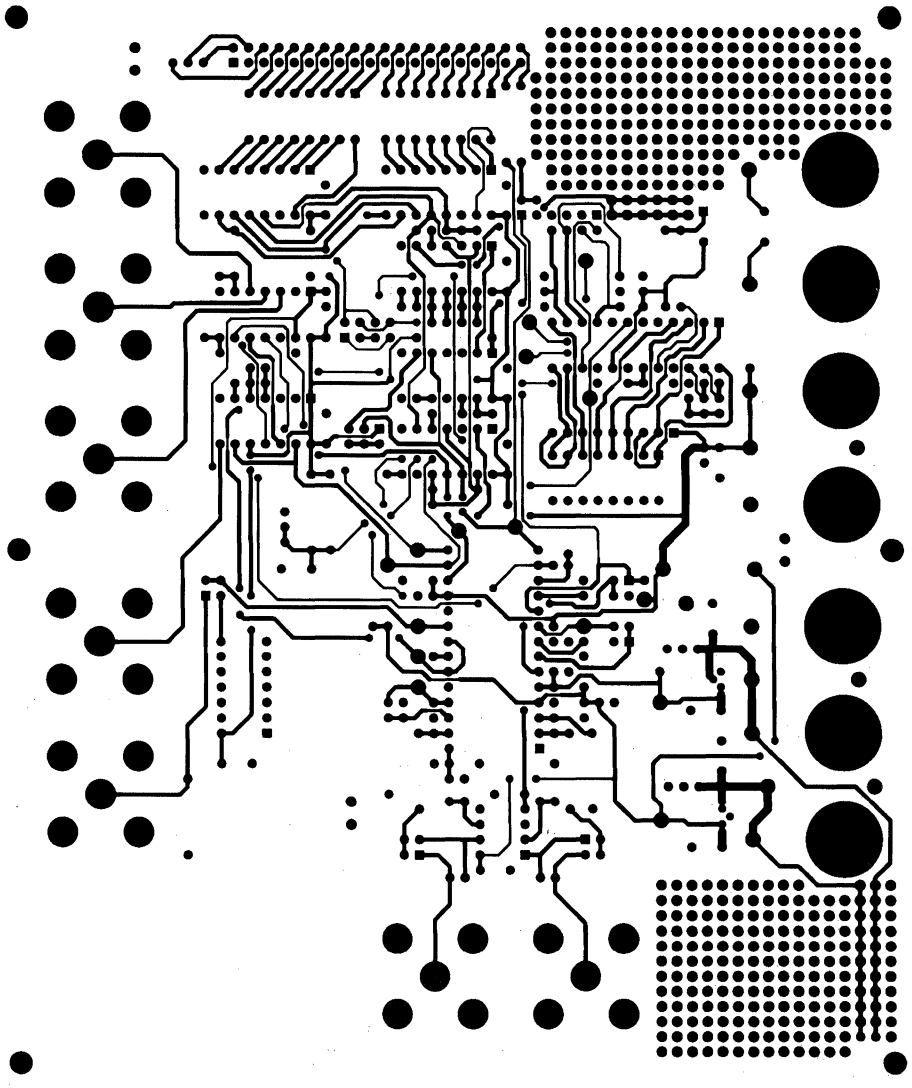


Figure 8. Bottom Trace Layer (NOT TO SCALE)

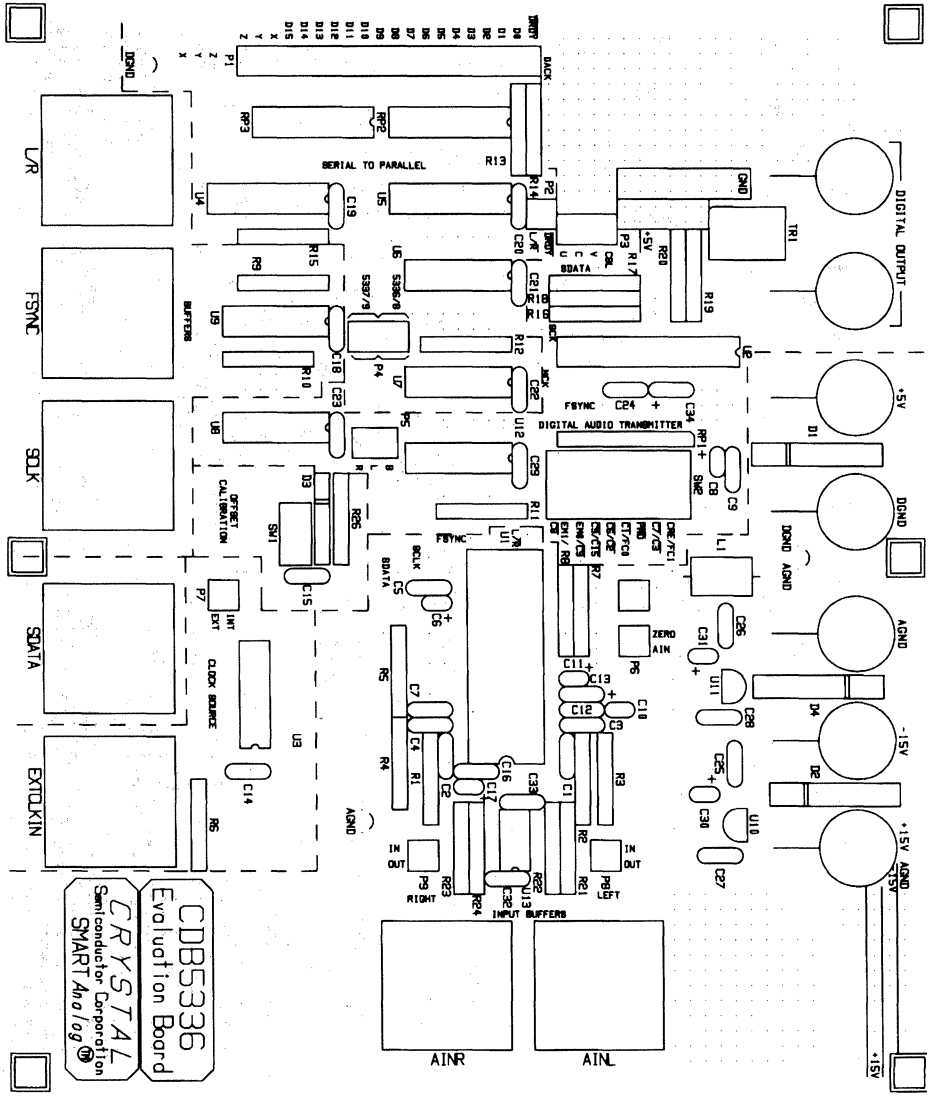


Figure 9. Component Layout (NOT TO SCALE)

Semiconductor Corporation

CS5345

Low Power, Stereo A/D Converter for Digital Audio

Features

- Single +5 V Power Supply
- 91 dB Dynamic Range
- Linear Phase Digital Anti-Alias Filtering
  0.05dB Passband Ripple
  73.5dB Stopband Rejection
- Low Power Dissipation: 100 mW
  Power-Down Mode for Portable Applications
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Internal 64X Oversampling
- Evaluation Board Available

General Description

The CS5345 is a complete stereo analog-to-digital converter which performs anti-alias filtering, sampling and analog-to-digital conversion generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

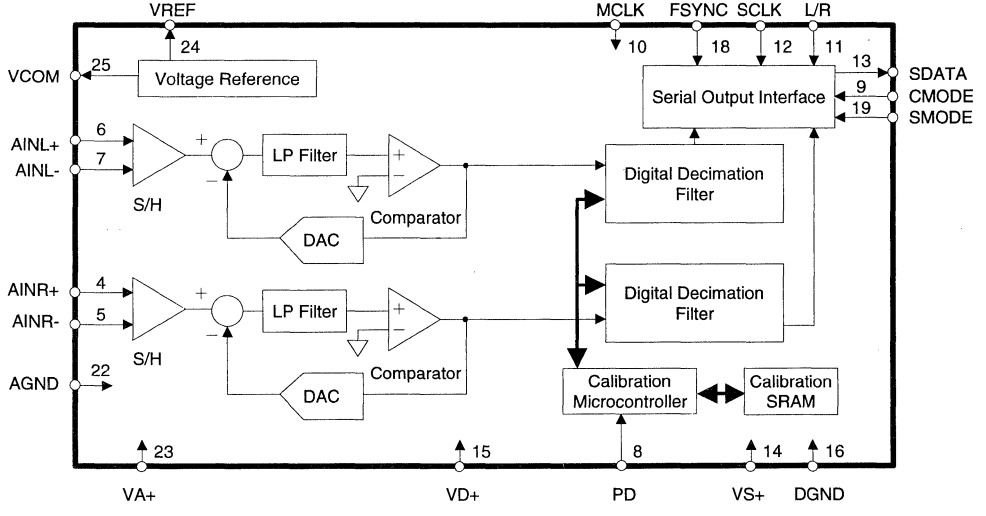
The CS5345 operates from a single +5V supply and requires only 100 mW for normal operation, making it ideal for battery-powered applications.

The ADC uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The linear-phase digital filter has a passband of dc to 22 kHz, 0.05 dB passband ripple and >73.5 dB stopband rejection.

The device is available in a 0.3" wide 28-pin SOIC surface mount package.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS5345-KS	0° to 70°C	28-pin plastic SOIC
CDB5345		Evaluation Board



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VS+, VD+ = 5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 150Ω with 1500 pF across AIN+, AIN-; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified, Logic 0=0V, Logic 1=VD+.)

Parameter		Symbol	Min	Typ	Max	Units
Resolution			16	-	-	Bits
Dynamic Performance						
Dynamic Range	A-weighted		- -	91 88	- -	dB dB
Total Harmonic Distortion+Noise	0dB -20dB -60dB	THD+N	- - -	-86 -68 -28	- - -	dB dB dB
Total Harmonic Distortion	0dB	THD	-	.0018	-	%
Interchannel Phase Deviation			-	0.0001	-	Degree
Interchannel Isolation	(dc to 20 kHz)		-	100	-	dB
dc Accuracy						
Interchannel Gain Mismatch			-	0.05	-	dB
Gain Error			-	±2	±5	%
Gain Drift			-	60	-	ppm/°C
Bipolar Offset Error	(After Calibration)		-	±5	±30	LSB
Analog Input						
Differential Input Voltage Range (Full Scale) (Note 1)		VIN	3.46	3.75	4.06	Vpp
Input Impedance		ZIN	-	85	-	kΩ
Power Supplies						
Power Supply Current Normal Operation	VA+ (VD+) + (VS+)	IA+ ID+	- -	10.5 9.5	16 14	mA mA
Power Supply Current Power-Down Mode	VA+ (VD+) + (VS+)	IA+ ID+	- -	50 50	- -	µA µA
Power Dissipation Power Down			- -	100 0.5	150 -	mW mW

Notes: 1. The peak-to-peak input voltage range for each input is equal to {(VA+)-VREF}x0.625. The nominal value for (VA+) - VREF is 3 Volts. The differential peak-to-peak input voltage is equal to twice the individual voltage range. (See Figure 5)

* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 °C; VA+, VS+, VD+ = 5V ± 5%; Output word rate (Fs) of 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Passband	(-0.05 dB)		-	0 to 18	-	kHz
	(-2.8 dB)		-	0 to 22	-	kHz
	(-6.5 dB)		-	0 to 24	-	kHz
Passband Ripple			-	-	±0.05	dB
Stopband			32	-	3040	kHz
Stopband Attenuation	(Note 2)		73.5	-	-	dB
Group Delay (OWR = Output Word Rate)	(Note 3)	t_{gd}	-	8/OWR	-	s
Group Delay Variation vs. Frequency		Δt_{gd}	-	-	0.0	µs

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 3.072MHz ±18kHz where n = 0,1,2,3...).

3. Group delay for OWR = 48kHz, t_{gd} = 8/48kHz = 167µs

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VS+, VD+ = 5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70% VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20 µA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20 µA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Positive Digital	VD+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies		Iin	-	-	±10	mA
Analog Input Voltage		V_{INA}	-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Temperature (power applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

(T_A = 25 °C; VA+, VS+, VD+ = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VA+, VS+, VD+; C_L = 20 pF)

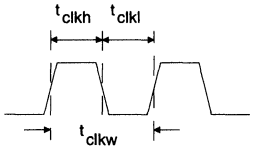
Parameter	Symbol	Min	Typ	Max	Units
MCLK Period (CMODE low)	t_{clkw1}	78.13	-	781.3	ns
MCLK Low (CMODE low)	t_{clkl1}	31.25	-	-	ns
MCLK High (CMODE low)	t_{clkh1}	31.25	-	-	ns
MCLK Period (CMODE high)	t_{clkw2}	52.0	-	520.8	ns
MCLK Low (CMODE high)	t_{clkl2}	20.83	-	-	ns
MCLK High (CMODE high)	t_{clkh2}	20.83	-	-	ns
L/R duty cycle		25	-	75	%
SCLK Period	t_{sclkw}	312.5	-	-	ns
SCLK Pulse Width Low	t_{sclkl}	100	-	-	ns
SCLK Pulse Width High	t_{sclkh}	100	-	-	ns
SCLK falling to SDATA valid	t_{dss}	-	-	70	ns
L/R edge to MSB valid	t_{lrdss}	-	-	70	ns
PD pulse width	t_{pdw}	150	-	-	ns
PD falling to SDATA valid	t_{pcf}	-	8224/OWR	-	s
Rising SCLK to L/R edge delay	t_{slr1}	30	-	-	ns
L/R edge to rising SCLK setup time	t_{slr2}	30	-	-	ns
SCLK Falling to FSYNC delay	t_{fs}	-70	-	+70	ns

RECOMMENDED OPERATING CONDITIONS

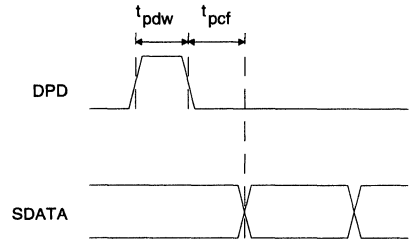
(AGND, DGND = 0V; all voltages with respect to ground)

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	(Note 5)	VA+	4.75	5.0	5.25	V
	Positive Digital		VD+	4.75	5.0	5.25	V
	Positive Substrate		VS+	4.75	5.0	5.25	
Differential Analog Input Voltage		(Notes 1&6)	V_{IN}	-	3.75	-	Vpp
Analog Input Bias Voltage				-	0.5VA+	-	V

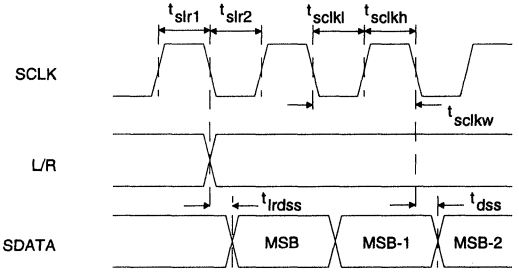
Notes: 5. VD+ must be within 0.3V of VA+.
6. The output codes will clip at full scale with differential input signals >3.75 Vpp.



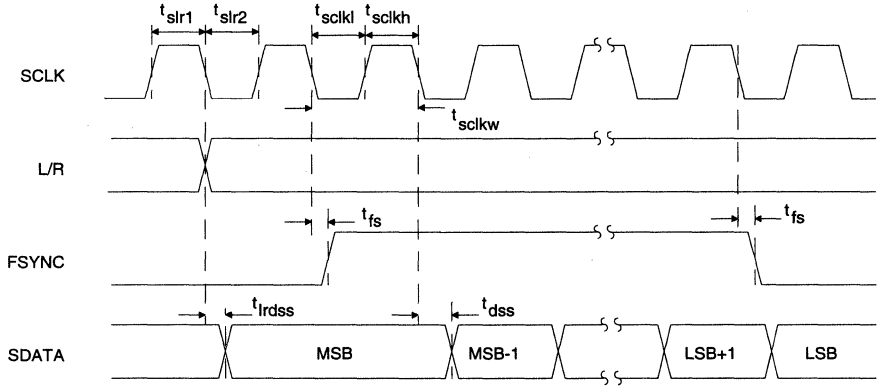
MCLK Definition



Power Down & SDATA Valid



SCLK to L/R & SDATA-Mode 1 (SMODE High), FSYNC Ignored
Mode 2 - FSYNC High (SMODE Low)



SCLK to L/R, SDATA & FSYNC - Mode 2 - FSYNC Controlled (SMODE Low)

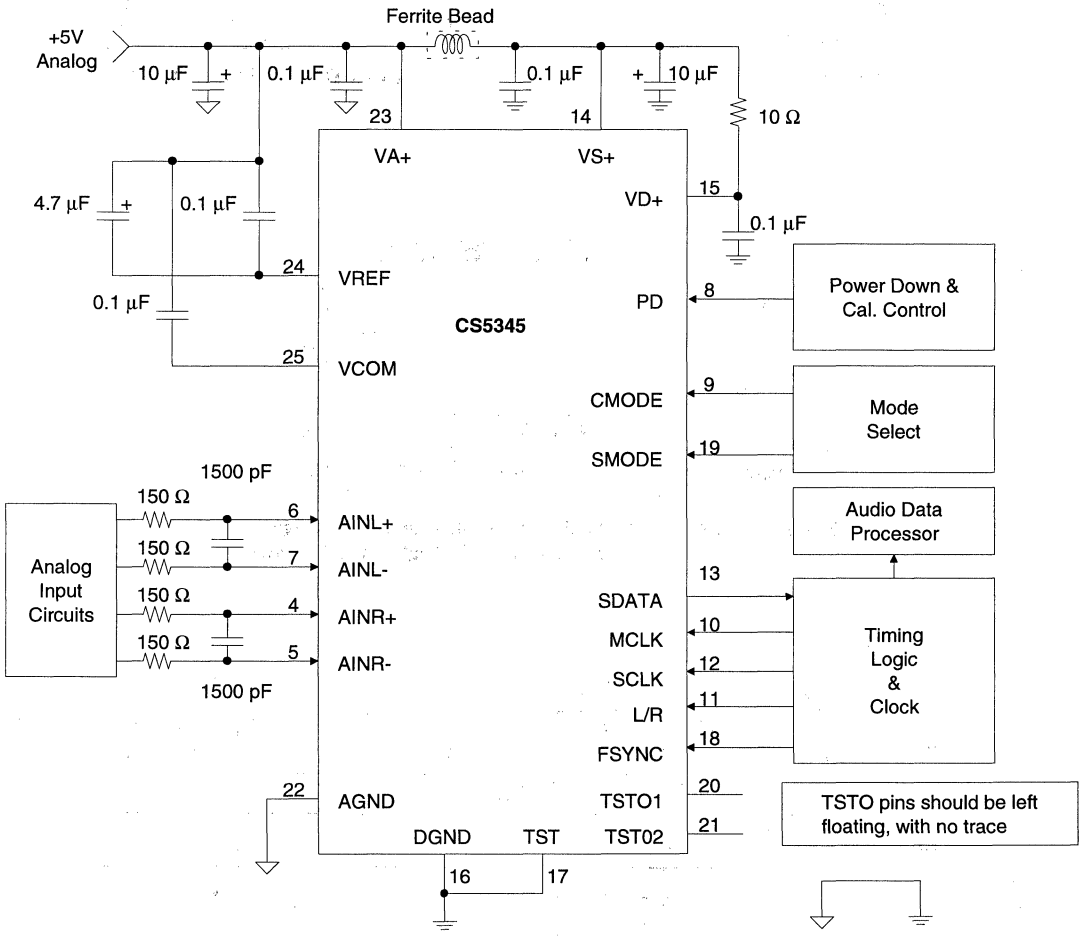


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5345 is a 16-bit, 2-channel A/D converter designed for stereo digital audio applications that require a single +5V supply. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for a differential input signal range of 3.75 Vpp. Offsets are internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption is 100 mW. This can be further reduced to .05 mW using the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside this ADC, see the references at the end of this data sheet.

L/R (kHz)	CMODE	MCLK (MHz)	SCLK (MHz)
32	low	8.192	2.048
32	high	12.288	2.048
44.1	low	11.2896	2.8224
44.1	high	16.9344	2.8224
48	low	12.288	3.072
48	high	18.432	3.072

Table 1. Common Clock Frequencies

SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3

Master Clock Input

The master input clock (MCLK) into the ADC runs the digital filter and it is used to generate the delta-sigma modulator sampling clock. CMODE high will set the required MCLK frequency to 384 X the output word rate (OWR), while CMODE low will set the required MCLK frequency to 256 X OWR. Table 1 shows some common clock frequencies.

Serial Data Interface

The serial data interface has 2 possible modes of operation. L/R, SCLK and FSYNC are inputs in both interface modes. L/R must be derived from MCLK and be equal to the OWR. SCLK should also be derived from MCLK and be equal to the delta-sigma modulator sample rate (64 X OWR) to eliminate the possibility of interference tones in the output data. An SCLK frequency of 32 X OWR is possible but may cause interference tones. Data bits are clocked out via the SDATA pin using SCLK, L/R and FSYNC inputs. The serial nature of the output data results in the left and right data words being read at different times. However, the words within a L/R cycle represent simultaneously sampled analog inputs.

Mode 1 (SMODE high) is shown in Figure 2. The falling edge of SCLK causes the ADC to output each data bit. Notice the one SCLK cycle delay between L/R edges and the data MSB. FSYNC is ignored and should be tied either High or Low in this mode. Mode 1 is compatible with I^2S.

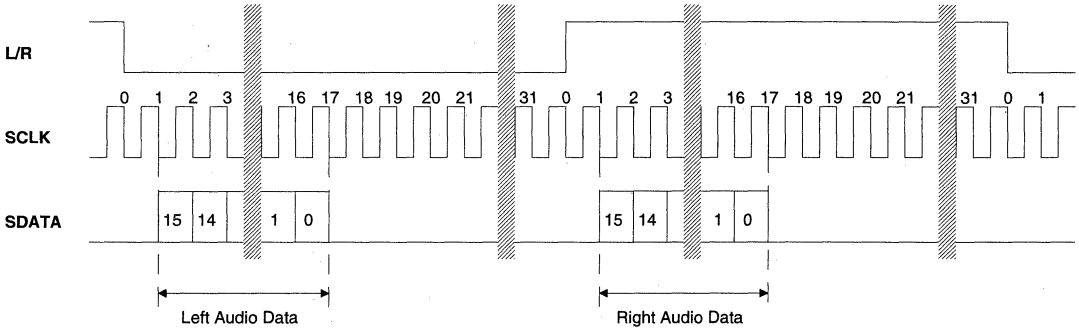


Figure 2. Data Output Timing - Mode 1 (FSYNC High or Low)

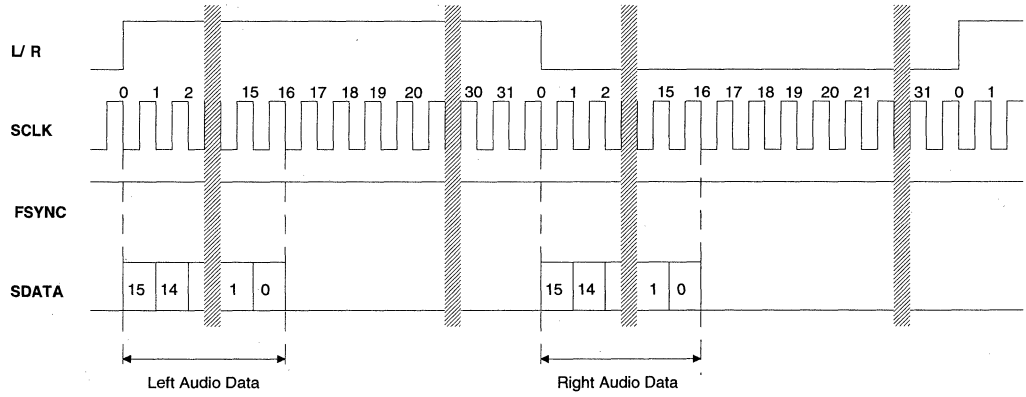


Figure 3. Data Output Timing - Mode 2 - FSYNC High

Mode 2-FSYNC High (SMODE low) is shown in Figure 3. The falling edge of SCLK causes the ADC to output each data bit with the exception of the MSB which is clocked out by the L/R edge.

In Mode 2-FSYNC Controlled, as shown in Figure 4, only the MSB is clocked out after the L/R edge with FSYNC low, SCLK is ignored. When it is desired to output data, bringing FSYNC high will enable SCLK to clock out data. This feature is particularly useful to position the data bits in time onto a common serial bus.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 1.88 Vpp centered at +2.5 V. The + and - input signals are 180° out of phase resulting in a differential input voltage of 3.75 Vpp. Figure 5 shows the input signal levels for full scale.

The CS5345 samples the analog inputs at 3.072 MHz for a 12.288 MHz MCLK (CMODE low). The digital filter rejects all noise between

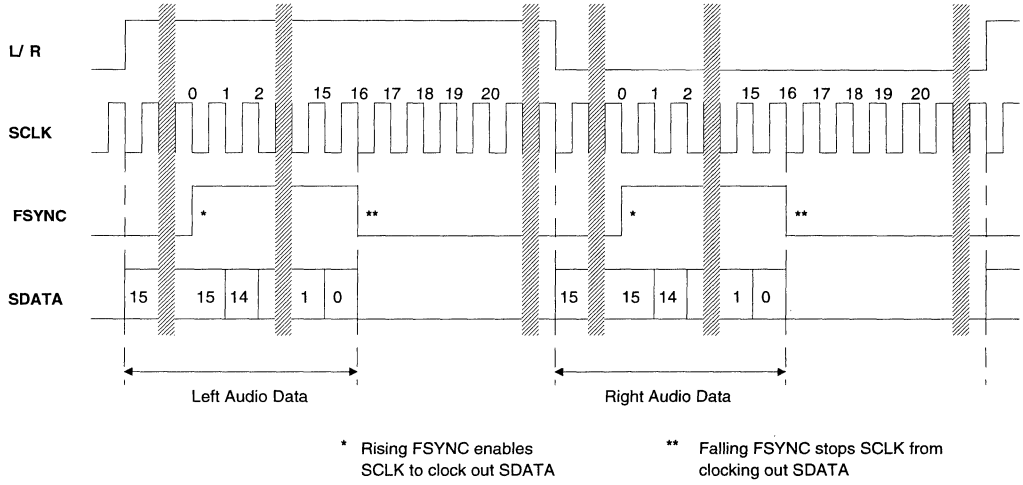


Figure 4. Data Output Timing- Mode 2 - FSYNC Controlled

32 kHz and (3.072 MHz-32 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 150 Ω resistor in series with each analog input and a 1500 pF capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these will degrade signal linearity. NPO, COG and polyester film capacitors are acceptable. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

Figure 6 is a suggested active input buffer circuit which provides a differential signal and level shifts up to +2.5 V. This circuit has been implemented on the CDB5345 evaluation board which is available from Crystal Semiconductor.

The on-chip voltage reference ((VA+) - 3.0 V) is connected to VREF (pin 24). A 4.7 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached between VREF and VA+ eliminates the effects of high frequency noise. Notice that VREF is decoupled to VA+ not AGND. This requirement is a result of the modulator sampling between VREF and VA+. No load current may be taken from the VREF output pin.

An additional on-chip voltage reference {(VA+) - 2.5 V)}is connected to VCOM (pin 25). This output may be used to bias the analog input circuitry if a high impedance, low-bias current buffer is used.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 0.5 mW. PD is the power down pin for the device. When high, it places the analog and digital circuitry in the power-down mode. Bringing this pin low will release the power-down mode and initiate a calibration sequence.

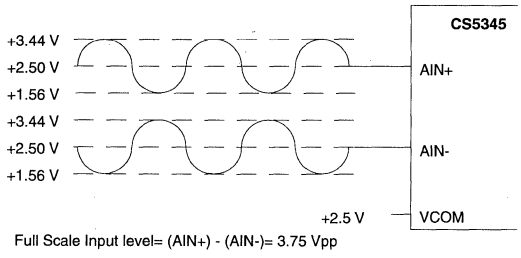


Figure 5. Full Scale Input Voltage

The delta-sigma modulator +/- inputs are internally disconnected from the AIN pins and shorted together during calibration. The digital section of the device measures and stores a value corresponding to the DC offset of each channel in the calibration registers. This calibration value is then subtracted from all future conversions during normal operation. 8224 L/R cycles are required for a calibration sequence. A short delay of approximately 18 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals. During calibration, the digital output of both channels is forced to a 2's complement zero.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered, either through the application of power or by exiting the power-down mode. The voltage reference takes a longer time to reach a final value due to the presence of large external capacitance on the VREF pin. The calibration period is optimized to allow the reference to settle for capacitor values of up to 4.7 µF. The use of larger capacitors can cause erroneous calibration or make the device inoperable and is not recommended.

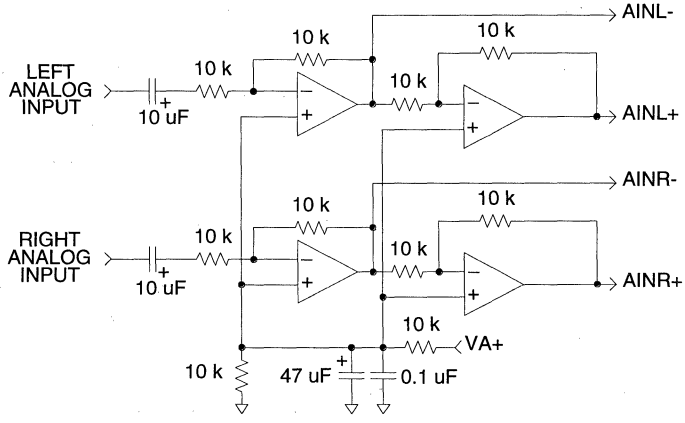


Figure 6. Example Input Buffer Circuit

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 V supply. VS+ and VD+ should be powered from VA+ via a ferrite bead to minimize noise coupling. To further minimize noise coupling into the ADC, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The Crystal Semiconductor application note "*Layout and Design Rules for Data Converters*" is available Crystal Semiconductor data books and should be considered required reading. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the CS5345.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Synchronization of Multiple CS5345

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling.

Synchronous sampling is achieved by connecting all PD pins to a single control signal and supplying the same L/R and MCLK to all converters.

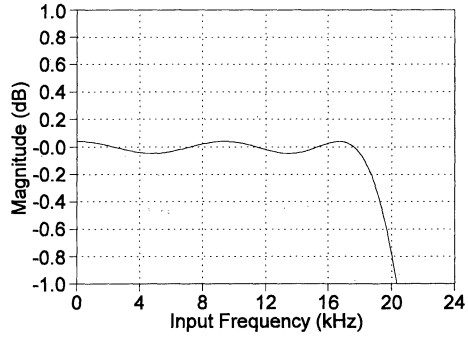


Figure 8. CS5345 Digital Filter Passband Ripple

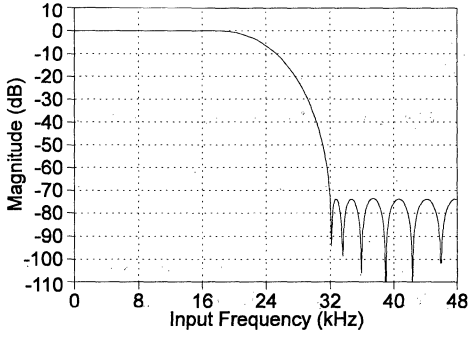


Figure 7. CS5345 Digital Filter Stopband Rejection

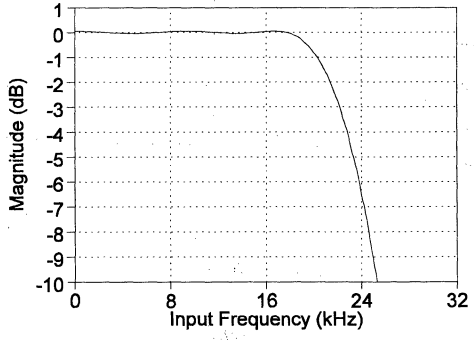


Figure 9. CS5345 Digital Filter Transition Band

PERFORMANCE

Digital Filter

Figures 7, 8, and 9 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple

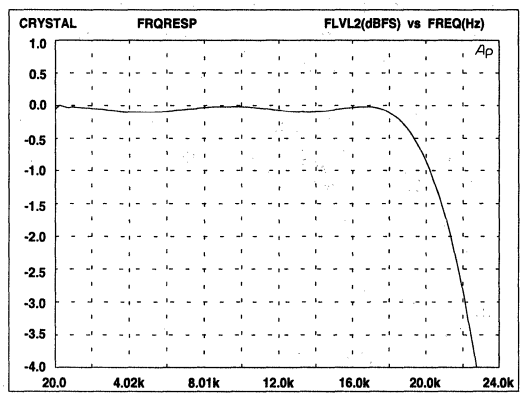


Figure 10. Frequency Response

is flat to ± 0.05 dB maximum.

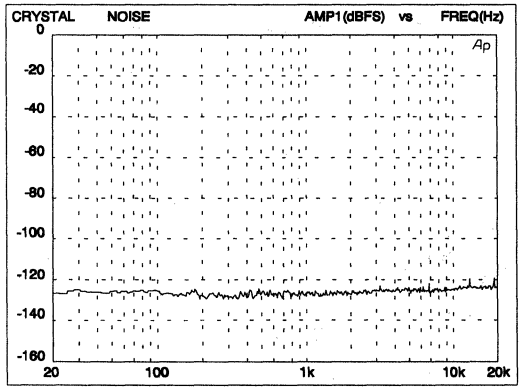


Figure 11. Noise Floor

Performance Measurements

All the following performance measurements were taken using an Audio Precision System

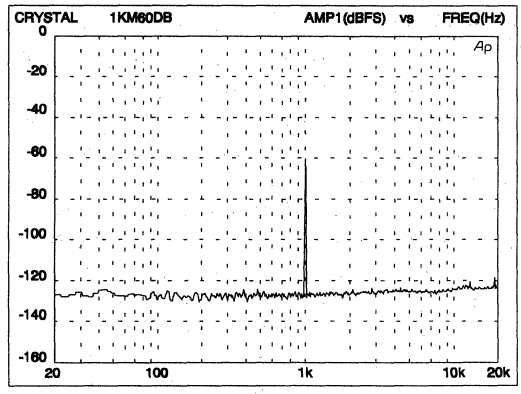


Figure 12. 1 kHz -60 dB

One Dual Domain tester. The CS5345 was in a CDB5345 evaluation board, running at 48 kHz word rate and interfaced to the System One via the digital audio interface using a CS8402 transmitter.

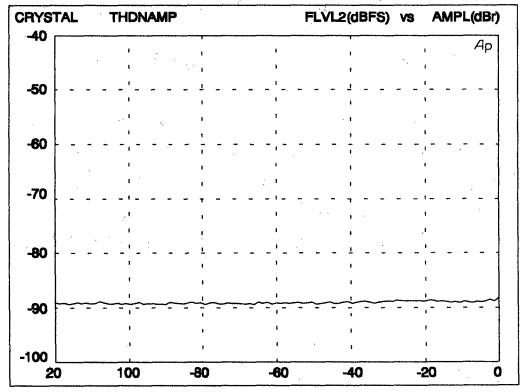


Figure 13. THD+N vs Input Level at 1kHz

Figure 10 shows the CS5345 frequency response.

Figure 11 shows the noise floor with zero input signal level. A 16 K point FFT was used.

Figure 12 shows a 1 kHz, -60 dB input signal FFT plot. Notice the lack of harmonic distortion

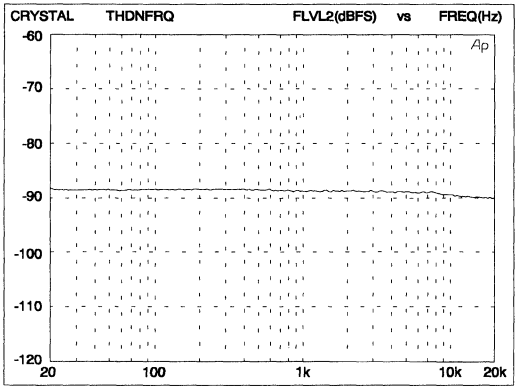


Figure 14. THD+N vs Frequency at -1dB

components. This is a direct result of the perfect differential non-linearity of the delta-sigma architecture

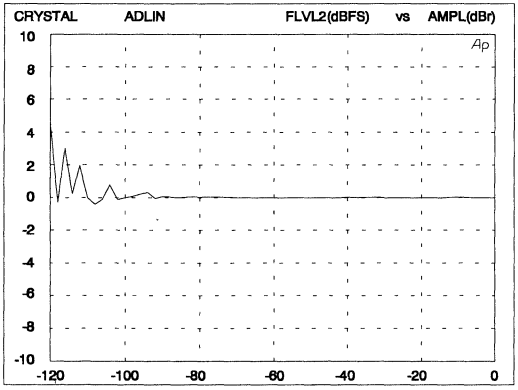


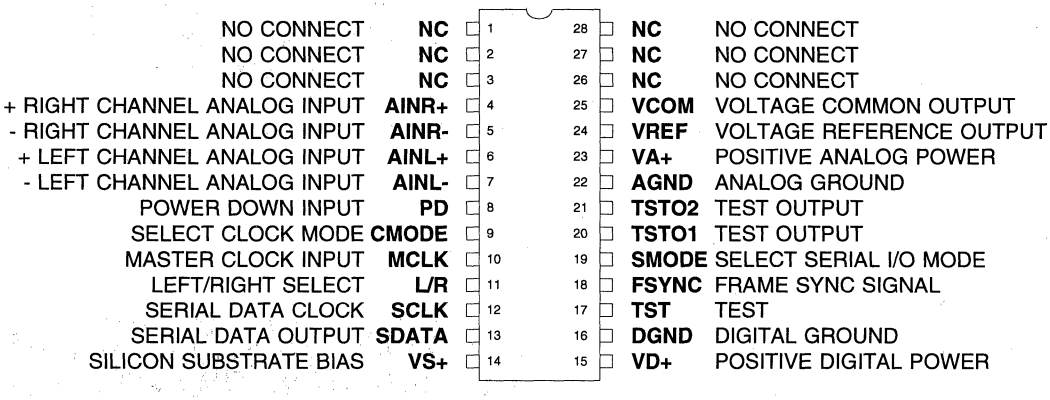
Figure 15. Output Level Error vs Input Level

Figure 13 shows the THD+N versus input level at 1 kHz. This plot indicates an unweighted dynamic range of 88 dB.

Figure 14 shows THD+N versus frequency at -1 dB input.

Figure 15 shows the linearity of the CS5345. The input signal is at 500 Hz and is varied from 0 dB (full scale) to -120 dB. At each input level, the output level is measured and compared to the perfect value. Any deviation is plotted as a deviation away from 0 dB. Notice the close conformance to perfect linearity, until the noise starts to influence the readings at about -100 dB.

PIN DESCRIPTIONS



Power Supply Connections

VA+- Analog Power, PIN 23

Positive supply for the analog section. Nominally +5 volts.

VS+ - Digital Power, PIN 14

Positive supply for the silicon substrate. Nominally +5 volts.

VD+ - Digital Power, PIN 15

Positive supply for the digital section. Nominally +5 volts.

AGND - Analog Ground, PIN 22

Analog ground reference.

DGND - Digital Ground, PIN 16

Digital ground for the digital section.

Analog Inputs

±AINL, ±AINR - Differential Left and Right Channel Analog Inputs, PINS 6, 7, 4, 5

Analog input connections for the left and right input channels. A nominal differential input voltage of 3.75 Vpp will produce a full scale digital output.

Analog Outputs

VREF - Voltage Reference Output, Pin 24

Internal voltage reference output. Nominally (VA+) - 3.0 V. Must be bypassed to VA+ with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF electrolytic capacitor.

VCOM - Voltage Common Output, PIN 25

Nominally (VA+) - 2.5 volts. May be used to bias the analog input circuitry if an additional buffer is used.

Digital Inputs

MCLK - Master Input Clock, PIN 10

Sampling rates, output rates and digital filter characteristics scale to MCLK frequency. MCLK frequency is either 256 or 384 X the output word rate (see CMODE). For example, a 12.288 MHz MCLK corresponds to an output word rate of 48 kHz per channel with CMODE low.

SCLK - Serial Data Clock, PIN 12

SCLK is an input clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). Data is clocked out on the falling edge of SCLK. See the descriptions of Data Output Mode 1 and Mode 2.

L/R - Left/Right Select, PIN 11

L/R is an input which selects the left or right channel for output on SDATA. The L/R frequency must be at the output word rate. Although the outputs of each channel are transmitted at different times, the two words in an L/R cycle represent simultaneously sampled analog inputs.

Left channel data is on SDATA when L/R is low in Mode 1 (SMODE high). Right channel data is on SDATA when L/R is high. The MSB data bit appears on SDATA one SCLK cycle after L/R changes.

Left channel data is on SDATA when L/R is high in Mode 2 (SMODE low). Right channel data is on SDATA when L/R is low. The rising edge of L/R clocks out the MSB of the left channel data. The falling edge of L/R clocks out the MSB of the right channel data.

PD - Analog Power Down, PIN 8

Device power-down command. The analog and digital circuitry are in power-down mode when PD is logic high.

CMODE - Clock Mode Select, PIN 9

CMODE should be tied low to select an MCLK frequency of 256 X the output word rate. CMODE should be tied high to select an MCLK frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 19

SMODE must be tied high to select serial interface Mode 1. SMODE must be tied low to select serial interface Mode 2. In all interface modes, L/R, FSYNC and SCLK should be derived from MCLK using external dividers.

FSYNC - Frame Synchronization Signal, PIN 18

In Mode 1 (SMODE high), FSYNC is ignored but must be connected to VD+ or DGND.

In Mode 2 (SMODE low), FSYNC is an input which controls the output of data on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/R transitions. If it is desired to delay the data bits from the L/R edge, then FSYNC must be low during the delay period. Bringing FSYNC high will enable SCLK to clock out of the SDATA bits. Note that the MSB will be clocked out based on the L/R edge, independent of the state of FSYNC.

Digital Outputs

SDATA - Serial Data Output, PIN 13

Audio data bits are presented MSB first, in 2's complement format.

Miscellaneous

NC - No Connection, PINS 1, 2, 3, 26, 27, 28

No internal connection.

TSTO1, TSTO2 -Test Pins, PIN 20, 21

These pins are factory test outputs and must not be connected to any external component or length of PC trace.

TST - Test Input, PIN 17

Allows access to the CS5345 test modes. Must be connected to digital ground for normal operation.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Total Harmonic Distortion+Noise - The ratio of the rms sum of all spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), excluding signal, to the rms value of the signal.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal . Units in LSBs.

REFERENCES - All reprinted in this data book.

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Semiconductor Corporation

CDB5345

Evaluation Board for CS5345

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, SPDIF & EIAJ-340 Compatible Digital Audio
- Demonstrates CS8402 Generation of System Clocks
- Buffered Serial Output Interface
- Digital and Analog Patch Areas

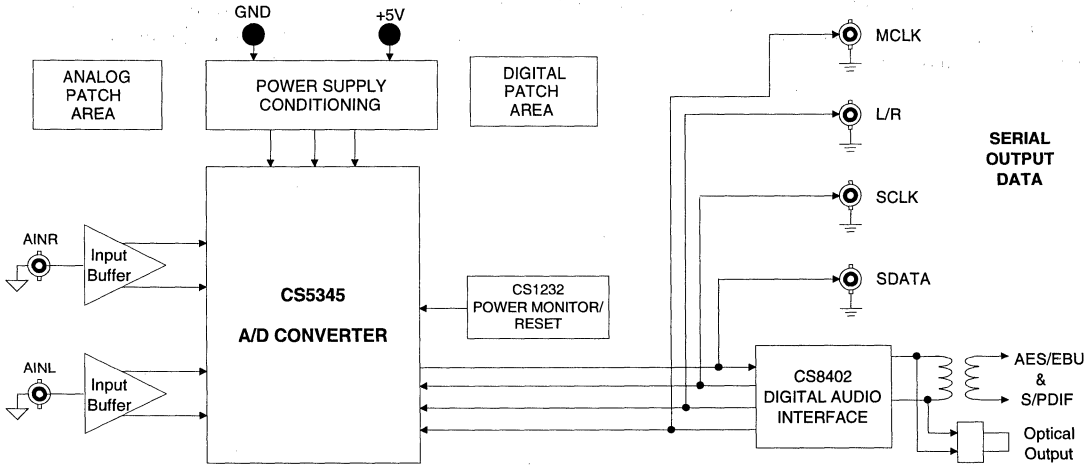
General Description

The CDB5345 evaluation board allows fast evaluation of the CS5345 16-bit, stereo A/D converter. The board generates all converter timing signals and provides serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

Also included is a CS8402 digital audio transmitter I.C., which can generate AES/EBU, SPDIF & EIAJ-340 compatible audio data via standard phono and optical connectors.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION: CDB5345



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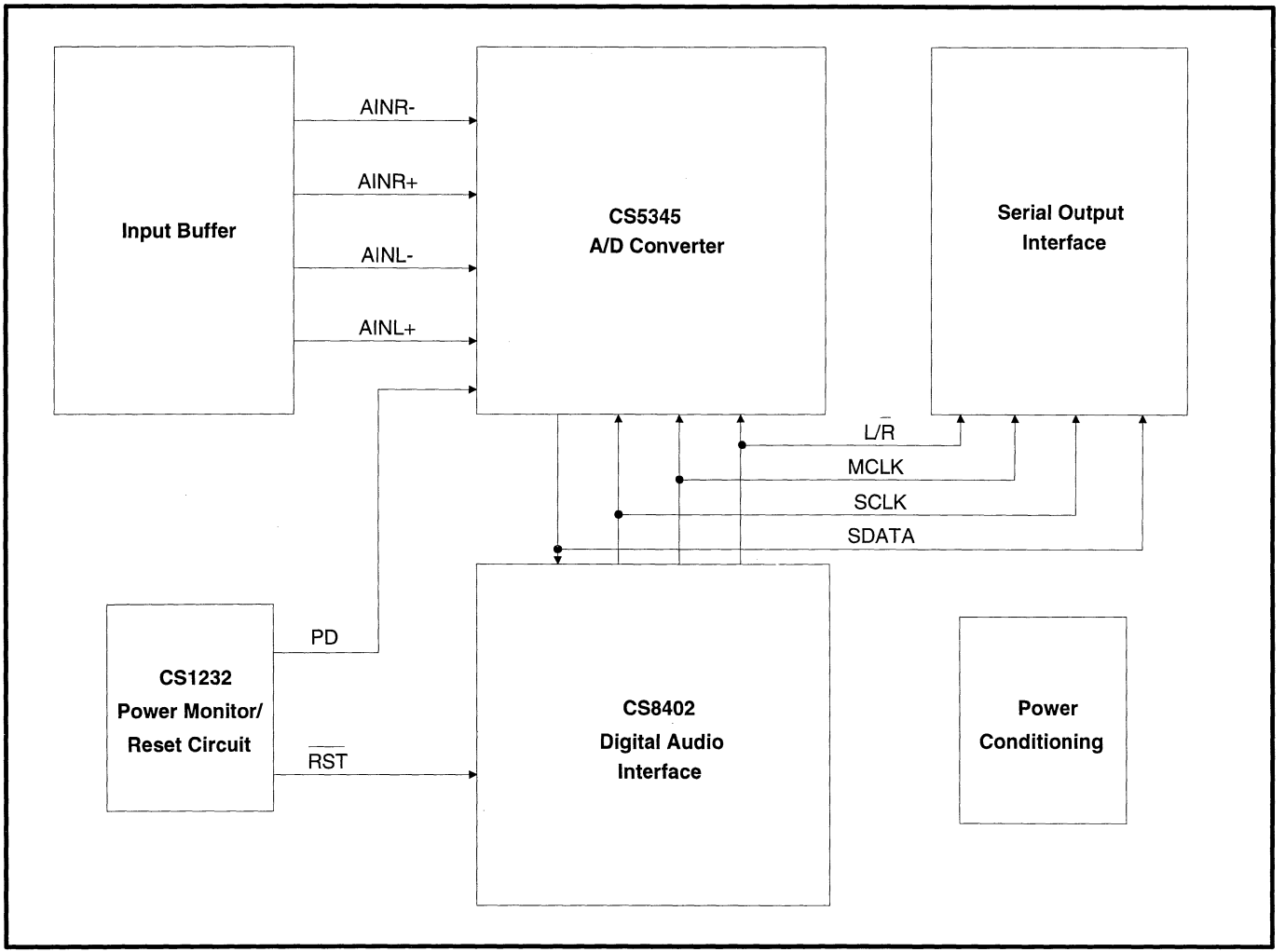


Figure 1. CDB5345 Overview

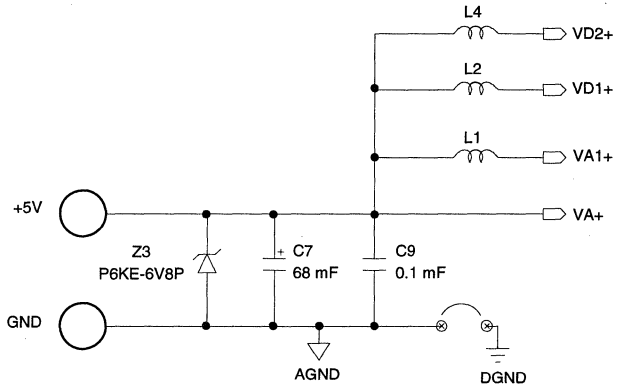


Figure 2. Power Conditioning

Power Supply Circuitry

The schematic diagram in Figure 2 shows the evaluation board power supply circuitry. Power and ground for the evaluation board are made via the two binding posts. The +5 Volt analog power supply (VA+) powers the analog input buffers, Figure 5. The ADC analog supply, VA1+, is derived from VA+ via the ferrite bead, L1, to minimize noise coupling.

The +5 Volt digital supply for the discrete logic is derived from the VA+ through the ferrite bead, L2. Z3 is a transient suppresser which also provides protection from incorrectly connected power supply leads. C7 and C9 provide general power supply filtering for the analog supply. C13 and C17 provide localized decoupling for the converter VA+ pin, Figure 4. The evaluation board uses both an analog and a digital ground plane which are connected at a single point. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

The ADC substrate bias voltage, VS+, and digital supply voltage, VD+, are derived from VA1+ through the ferrite bead L3, Figure 4. Notice the lowpass filter, R18 and C18 / C19, between VS+ and VD+. VD+ is not used to power any other

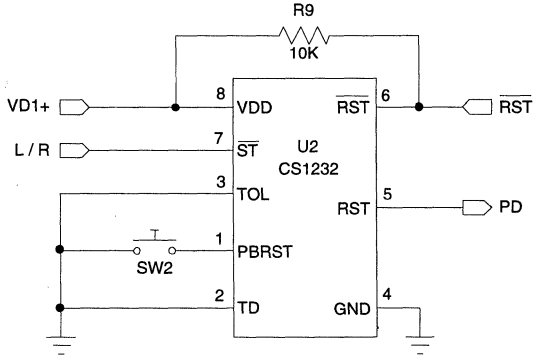


Figure 3. Power Monitor/Reset Circuit

digital logic on the evaluation board, which is necessary to minimize digital noise on VA1+.

Power monitor & Reset Circuit

The power monitor / clock monitor / reset function has been implemented using the Crystal Semiconductor CS1232 Micromonitor, Figure 3. The power-monitor threshold for the CS1232 has been configured to issue a reset command to the CS5345 PD and the CS8402 $\overline{\text{RST}}$ pins when the supply voltage ,VD1+, is below 4.62V. The command will remain asserted for approximately 250 ms after the supply voltage exceeds the threshold. This prevents erroneous data from being output from the evaluation board on power-up and initiates a CS5345 calibration sequence when the supply voltages have stabilized. This also ensures that the CS5345 calibration data will be replaced if a momentary loss of power occurs. A CS5345 calibration sequence can also be initiated manually with SW2. The CS1232 also implements a system watchdog timer and monitors the L/R clock.

Analog Inputs

As shown in Figure 4, the analog input signals are connected to the CS5345 via an RC network. R1-R4 and C1-C4 provide antialiasing and opti-

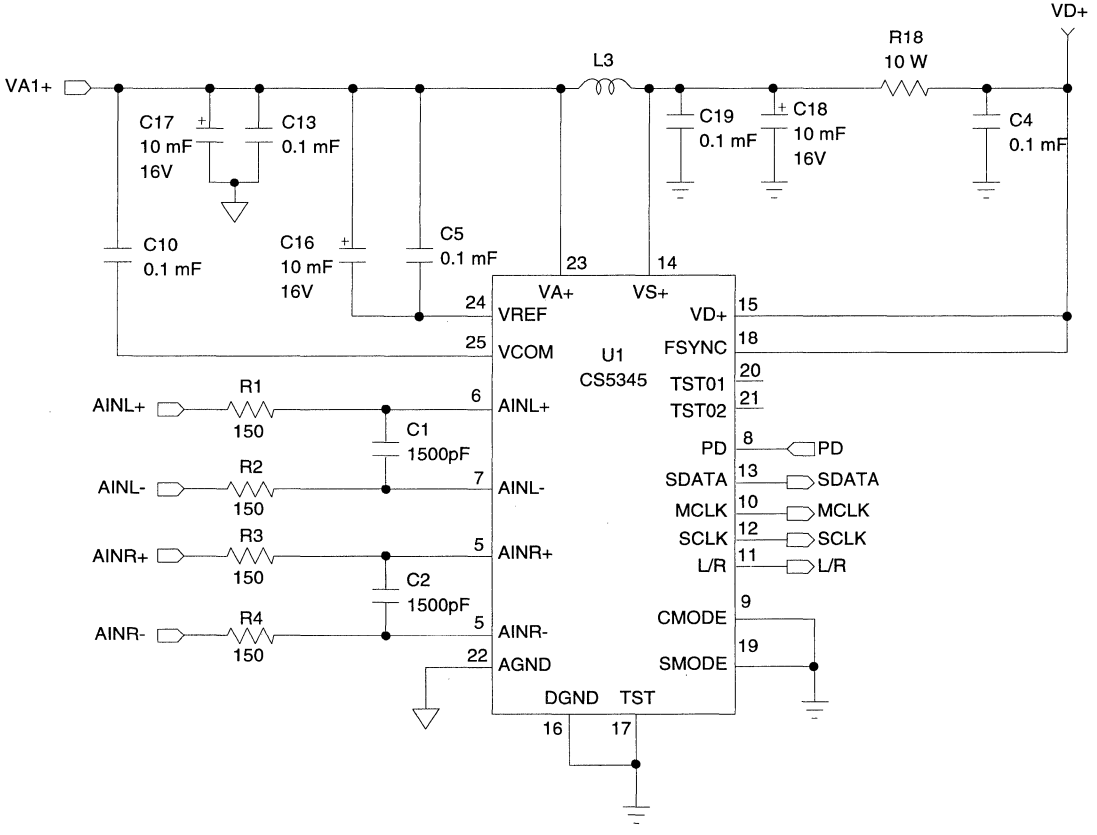


Figure 4. ADC Connections

mum source impedance for the analog input channels.

Figure 5 shows the input buffer circuit. This circuit converts single-ended inputs to differential and elevates the center point of the differential singles to approximately +2.5 V.

CS5345 Configuration

The CS5345 is configured for Mode 2-FSYNC high. MCLK is set for 256 X OWR by CMODE low. Refer to the CS5345 data sheet for a complete description of the CS5345 operation.

Digital Audio Standard Interface and Clock Generation

The CS8402 Digital Audio Interface Transmitter is included on the evaluation board. This device can implement either AES/EBU, S/PDIF or EIAJ-340 interface standards. The CDB5345 digital audio interface circuit, Figures 6 and 7, is the standardized implementation of S/PDIF with both coax and optical outputs.

The CS8402 is configured to operate in Mode 1 which allows the CS8402 to generate L/R and $\overline{\text{SCLK}}$ from MCLK. This not only simplifies the design but also lowers the number of components on the evaluation board. See the CS8401 / CS8402 data sheet for more information on the operation of the CS8402.

Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, and L/R BNC connectors on the evaluation board. These outputs are buffered, as shown in Figure 8, in order to isolate the converter from the digital signal processor.

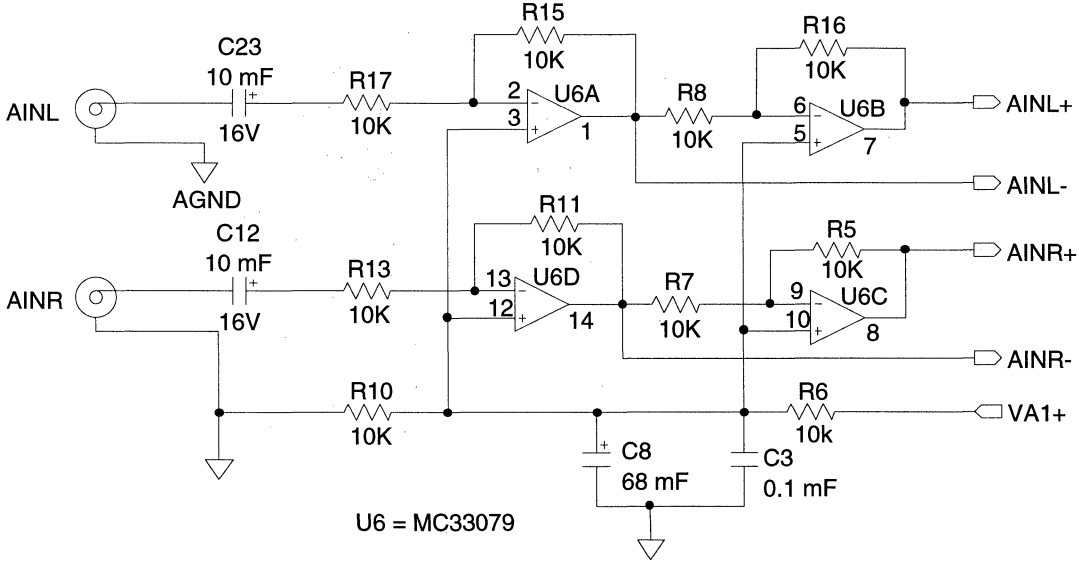


Figure 5. Input Buffer Circuit

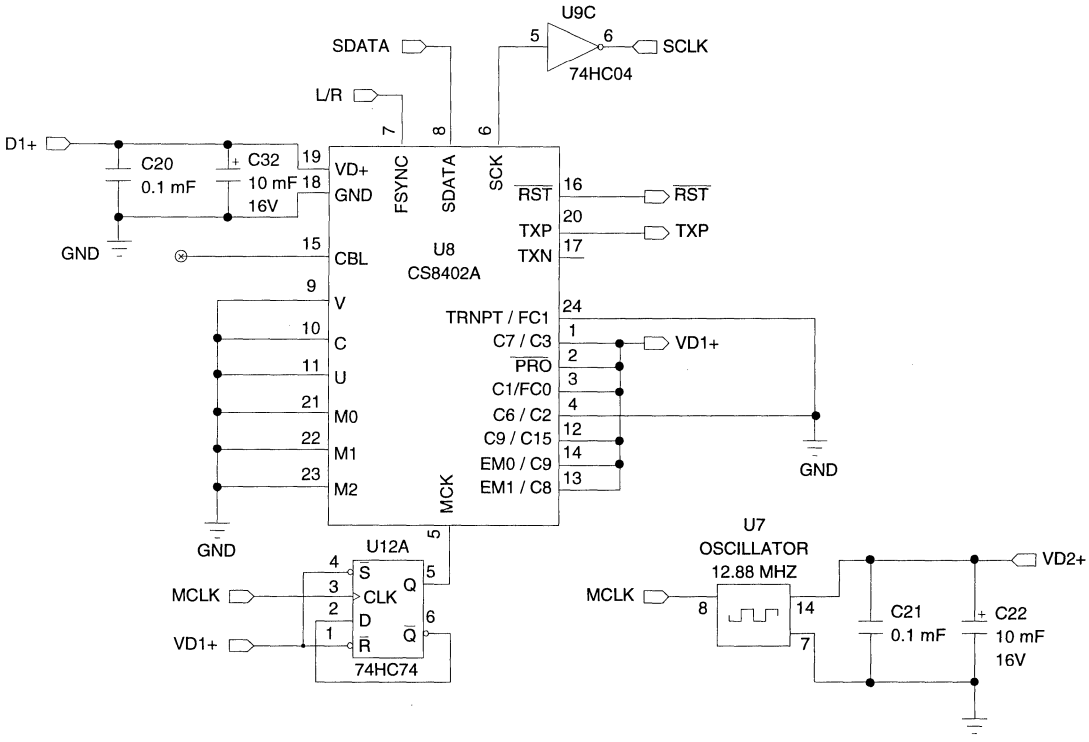


Figure 6. CS8402 Digital Audio Interface Connections

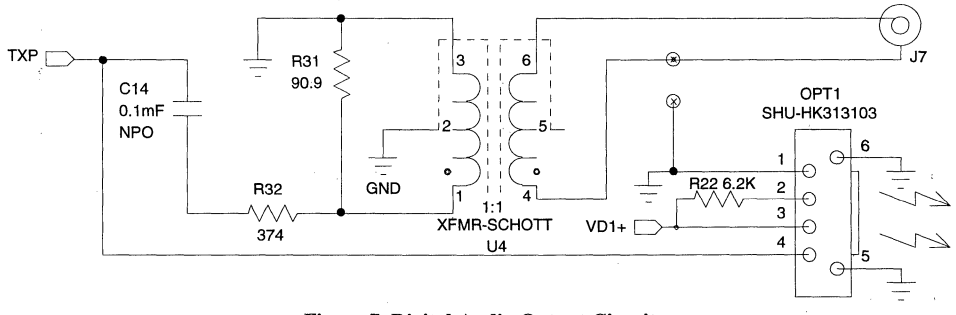


Figure 7. Digital Audio Output Circuit

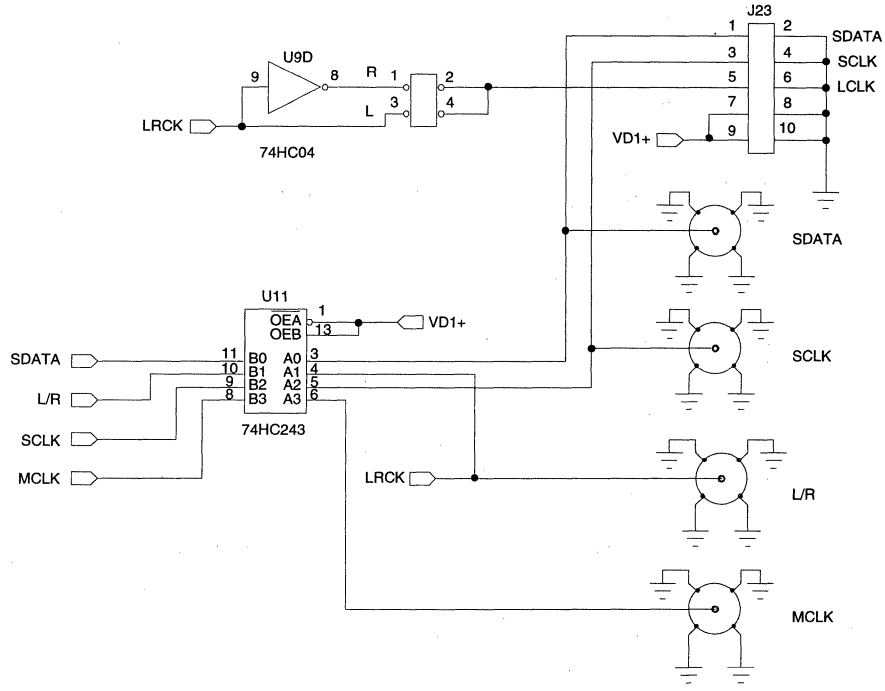
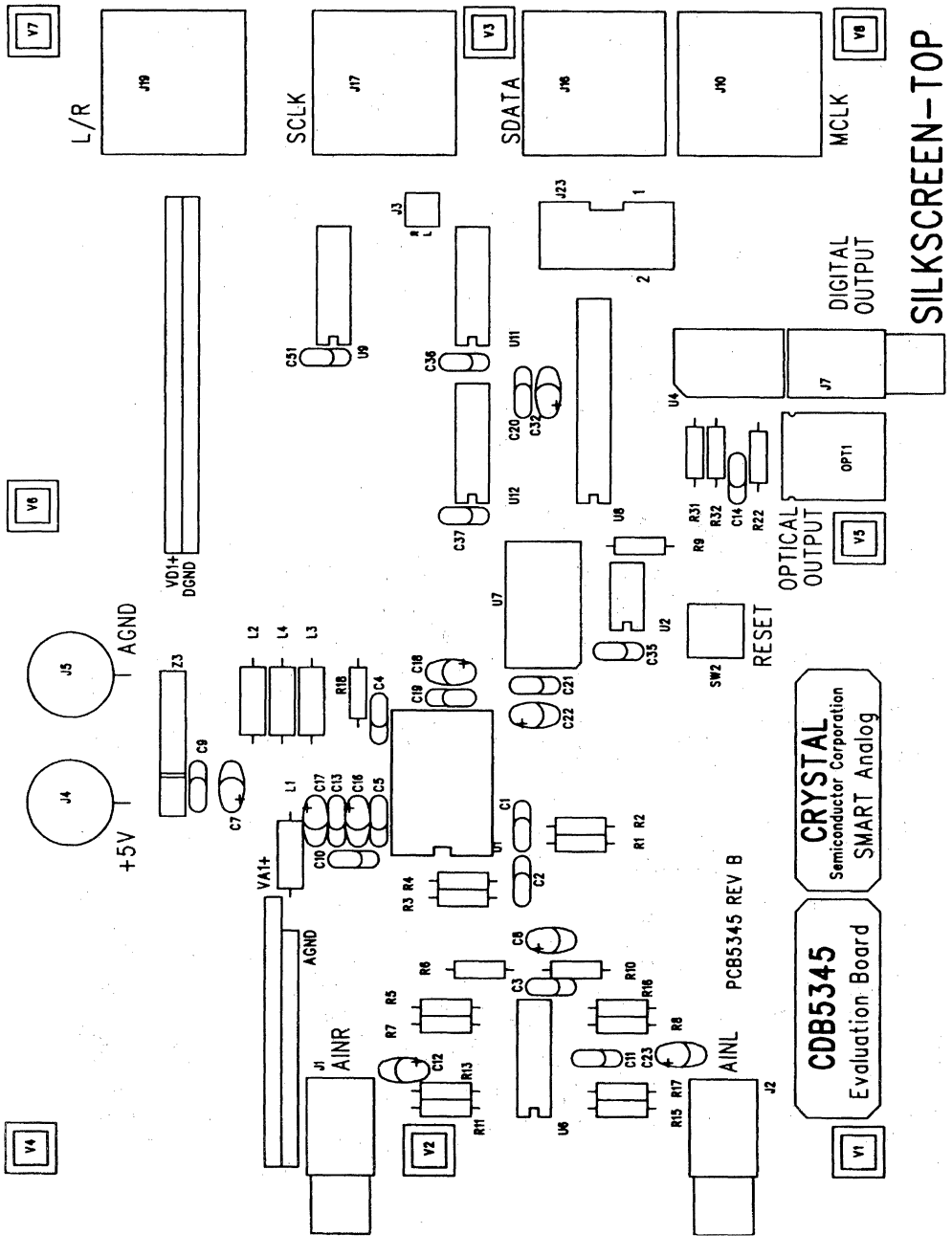


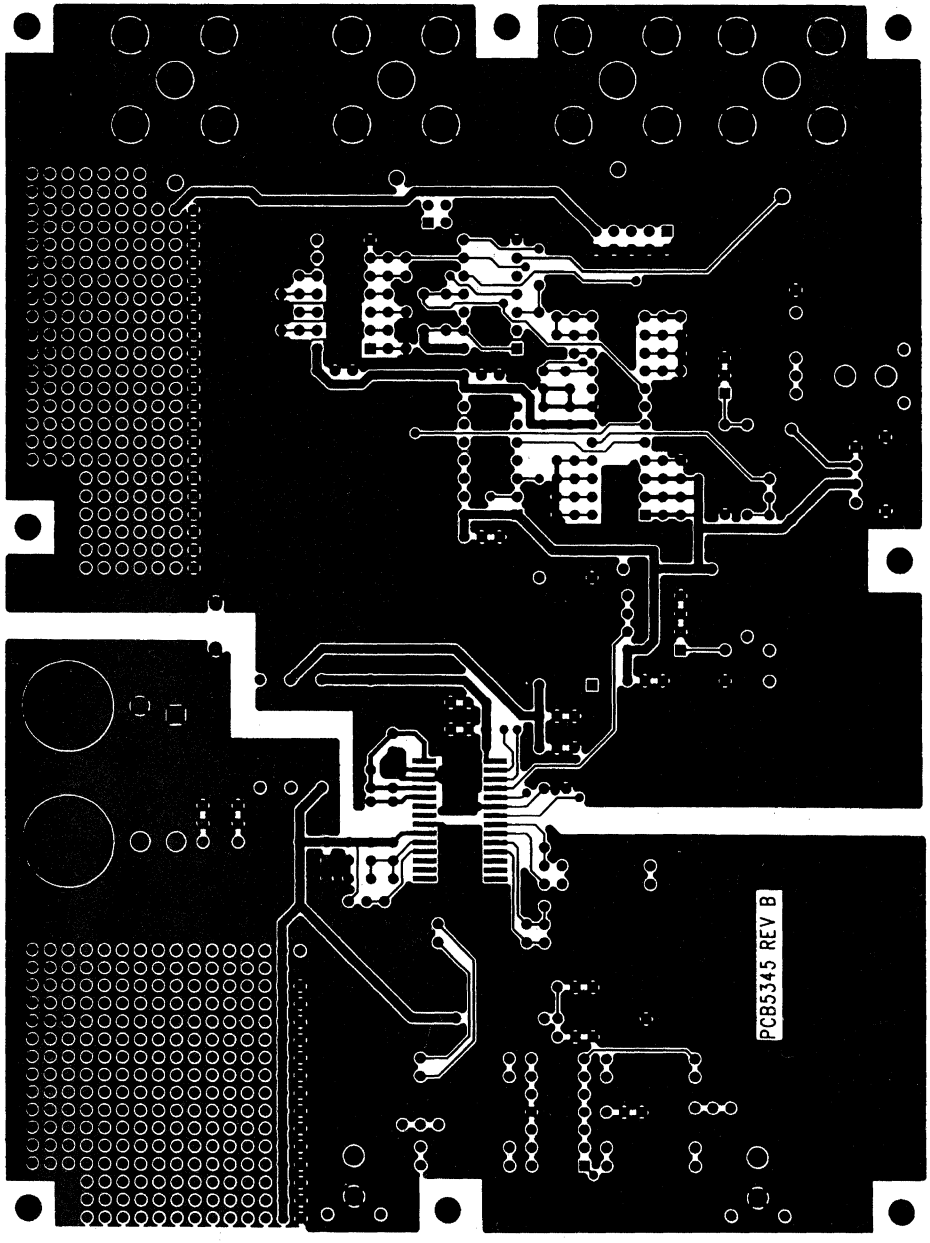
Figure 8. Serial Output Interface

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 ANALOG	input	+5 Volts from analog power supply
AGND	input	analog ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
MCLK	output	master clock output
L/R	output	left/right channel signal
SDATA	output	serial output data
SCLK	output	serial output clock
DIGITAL OUTPUT	output	CS8402 digital output via transformer
OPTICAL OUTPUT	output	CS8402 Digital output via optical

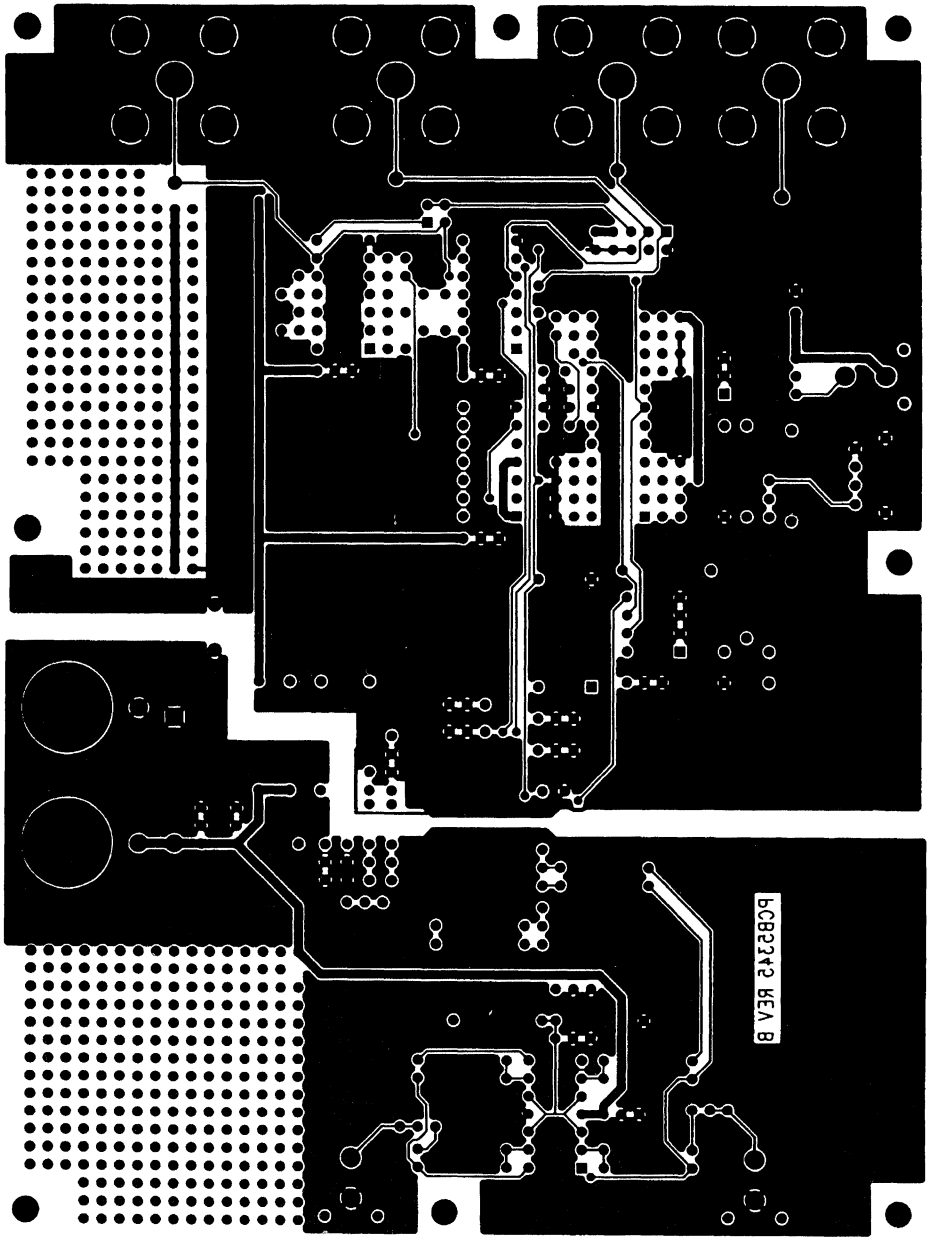
Table 1. Systems Connections



Silk Screen Layer (NOT TO SCALE)



Component Side Layer (NOT TO SCALE)



Solder Side Layer (NOT TO SCALE)

• Notes •

Semiconductor Corporation

CS5349

Single Supply, Stereo A/D Converter for Digital Audio

3

Features

- Single +5 V Power Supply
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 90 dB Dynamic Range
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 300 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

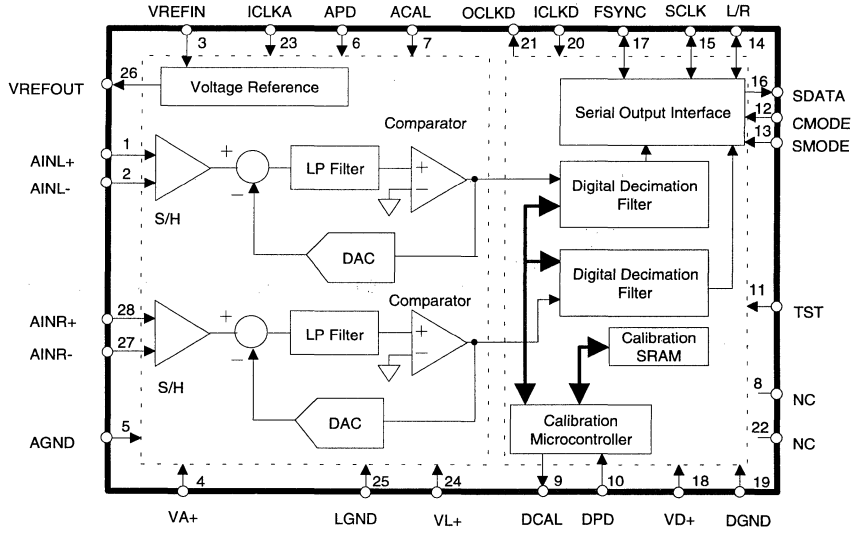
The CS5349 is a complete analog-to-digital converter which operates from a single +5V supply. It performs sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The ADC uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5349 has an SCLK which clocks out data on falling edges and a filter passband of dc to 24 kHz. The filter has linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The device is available housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package.

ORDERING INFORMATION: Page 3-121



Crystal Semiconductor Corporation
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ANALOG CHARACTERISTICS

(T_A = 25°C for K grade, T_A = -40 °C to +85 °C for B grade; VA+, VL+,VD+ = 5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 100Ω with 500 pF across AIN+, AIN-; VREFIN connected to VREFOUT; DCAL Connected to ACAL; Master Mode; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter*	Symbol	CS5349-K Min	CS5349-K Typ	CS5349-K Max	CS5349-B Min	CS5349-B Typ	CS5349-B Max	Units
Specified Temperature Range	T_A		0 to 70			-40 to +85		°C
Resolution		16	-	-	16	-	-	Bits
Dynamic Performance								
Dynamic Range		88	90	-	86	90	-	dB
Signal-to-(Noise+Distortion) THD+N	S/(N+D)	85	87	-	84	87	-	dB
Total Harmonic Distortion V_{in} = -10 dB, 1kHz	THD	-	0.001	0.005	-	0.001	0.005	%
Interchannel Phase Deviation		-	0.0001	-	-	0.0001	-	Degrees
Interchannel Isolation (dc to 20 kHz)		-	100	-	-	100	-	dB
dc Accuracy								
Interchannel Gain Mismatch		-	0.05	-	-	0.05	-	dB
Gain Error		-	±2	±5	-	±2	±5	%
Gain Drift		-	50	-	-	50	-	ppm/°C
Bipolar Offset Error (After Calibration)		-	±3	±10	-	±3	±10	LSB
Offset Calibration Range (ACAL Low)		-	±100	-	-	±100	-	mV
Analog Input								
Differential Input Voltage Range (Full Scale) (Note 1)	VIN	3.8	4.0	-	3.8	4.0	-	Vpp
Input Impedance	ZIN	-	50	-	-	50	-	kΩ
Power Supplies								
Power Supply Current (VA+)+(VL+)	IA+	-	30	40	-	30	40	mA
with APD, DPD low VD+	ID+	-	35	45	-	35	45	mA
(Normal Operation)								
Power Supply Current (VA+)+(VL+)	IA+	-	10	-	-	10	-	µA
with APD, DPD high VD+	ID+	-	100	-	-	100	-	µA
(Power-Down Mode)								
Power Dissipation (APD, DPD Low)	PDN	-	325	425	-	325	425	mW
(APD, DPD High)	PDS	-	0.5	-	-	0.5	-	mW
Power Supply Rejection Ratio (dc to 26 kHz)	PSRR	-	50	-	-	50	-	dB
(Note 2) (26 kHz to 3.046 MHz)		-	90	-	-	90	-	dB

Notes: 1. Input voltage range is equal to ±{(VA+)-VREFIN}x0.8. (See Figure in Analog Connection Section)

* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD+ = 5V ± 5%; Output word rate of 48 kHz)

Parameter	Symbol	Min	Typ	Max	Units
Passband (-3 dB)		0	to	24	kHz
(-0.01 dB)		0	to	22	kHz
Passband Ripple		-	-	± 0.01	dB
Stopband		28	to	3044	kHz
Stopband Attenuation (Note 2)		80	-	-	dB
Group Delay (OWR = Output Word Rate)	t_{gd}	-	18/OWR	-	s
Group Delay Variation vs. Frequency	$\triangle t_{gd}$	-	-	0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±22kHz where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Positive Logic	VL+	-0.3	-	(VA+)+0.3	V
	Positive Digital	VD+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies		Iin	-	-	±10	mA
Analog Input Voltage	(AIN and VREFIN pins)	V_{INA}	-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Temperature (power applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

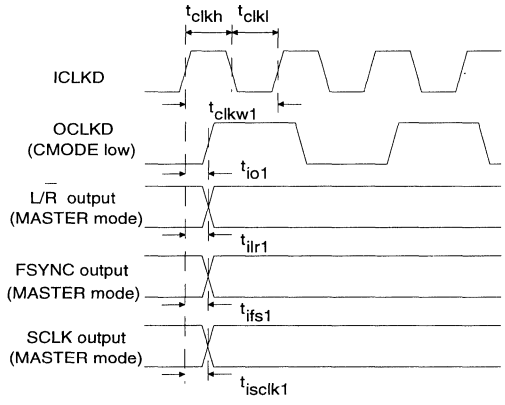
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

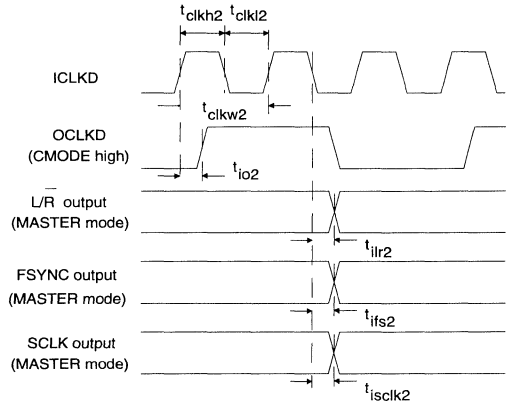
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VA+, VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t_{clkw1}	78	-	3906	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	2604	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK falling to SDATA valid (MASTER mode)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK falling to L/$\overline{R}$ (MASTER mode)	t_{mslr}	-20	-	20	ns
SCLK falling to FSYNC (MASTER mode)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid (SLAVE mode)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Rising SCLK to L/$\overline{R}$ edge delay (SLAVE mode)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to rising SCLK setup time (SLAVE mode)	t_{slr2}	30	-	-	ns
Rising SCLK to rising FSYNC delay (SLAVE mode)	t_{sfs1}	30	-	-	ns
Rising FSYNC to rising SCLK setup time (SLAVE mode)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	$2t_{clkw}$	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}		4096		1/OWR

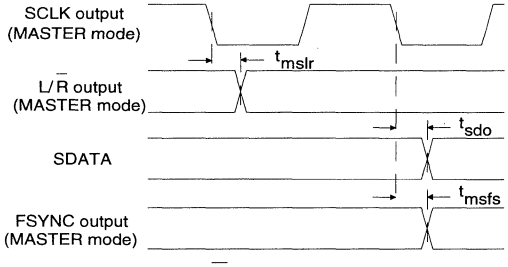
Notes: 3. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).



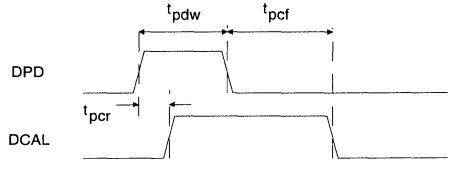
ICLKD to Outputs Propagation Delays (CMODE low)



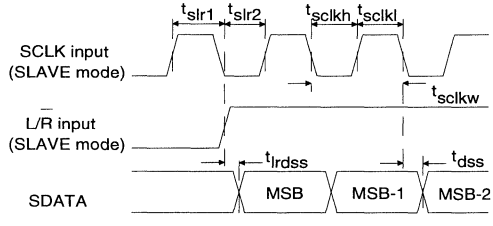
ICLKD to Outputs Propagation Delays (CMODE high)



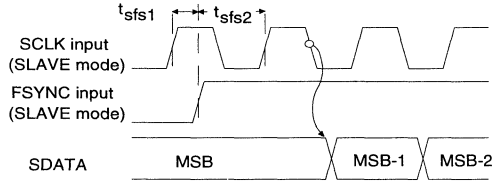
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	(Note 5)	VD+	4.75	5.0	5.25	V
	Positive Logic		VL+	4.75	5.0	VA+	V
	Positive Analog		VA+	4.75	5.0	5.25	V
Differential Analog Input Voltage		(Note 6)	V_{AIN}	3.8	4.0	-	Vpp
Analog Input Bias Voltage			V_{BIAS}	-	0.5VA+	-	V

Notes: 5. VD+ must be within 0.3V of VA+.

6. The output codes will clip at full scale with input signals >4Vpp, but <8Vpp. Input signals >8Vpp will cause indeterminate output codes. These voltages are subject to the gain error tolerance specification. Additional tag bits are output to indicate a near to clipping and overdrive condition.

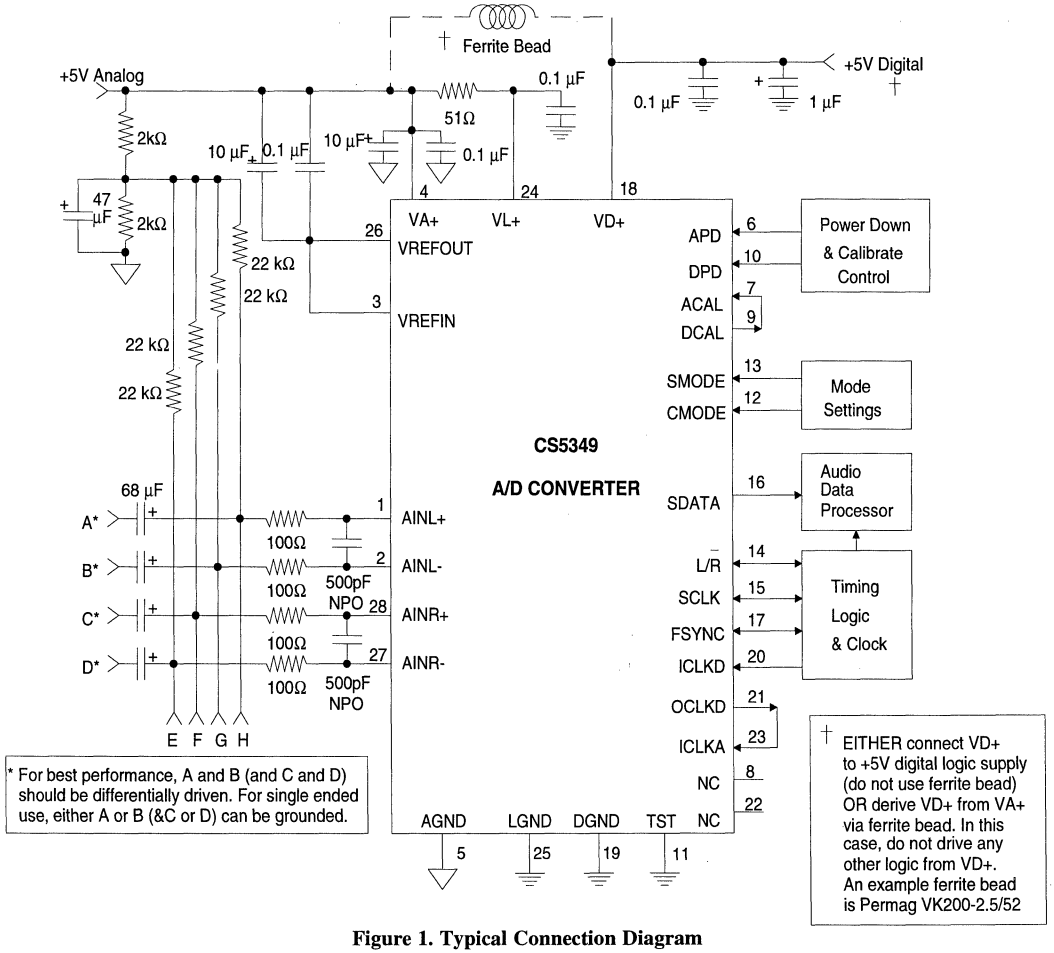


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5349 is a 16-bit, 2-channel A/D converter designed specifically for stereo digital audio applications that require a single +5V supply. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for a differential input signal range of 4Vpp. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 300 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside this ADC, see the references at the end of this data sheet.

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

SYSTEM DESIGN

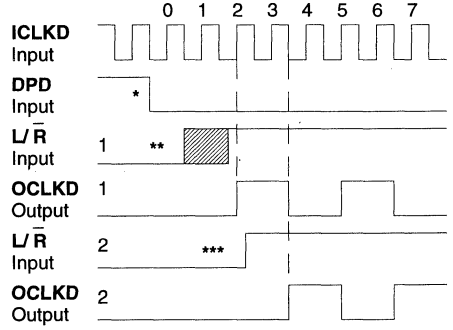
Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when



* DPD low is recognized on the next ICLKD rising edge (#0)
** L/$\overline{R}$ rising before ICLKD rising #2 causes OCLKD -1
*** L/$\overline{R}$ rising after ICLKD rising #2 causes OCLKD - 2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

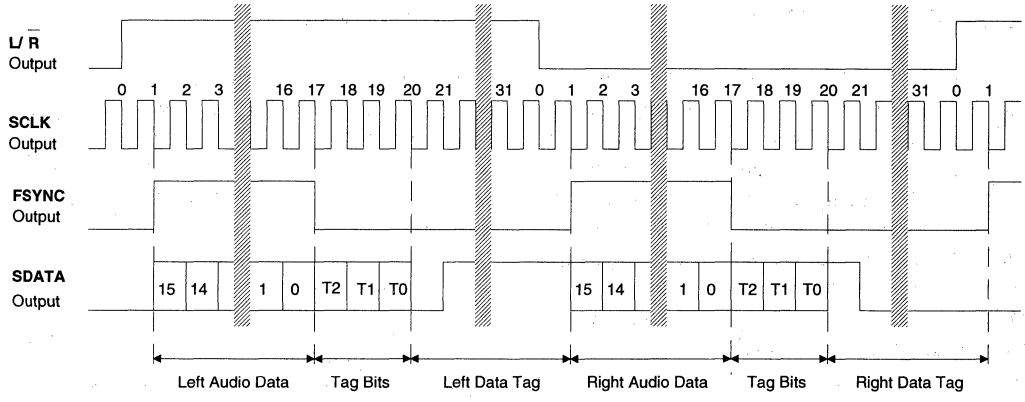


Figure 3. Data Output Timing - MASTER mode

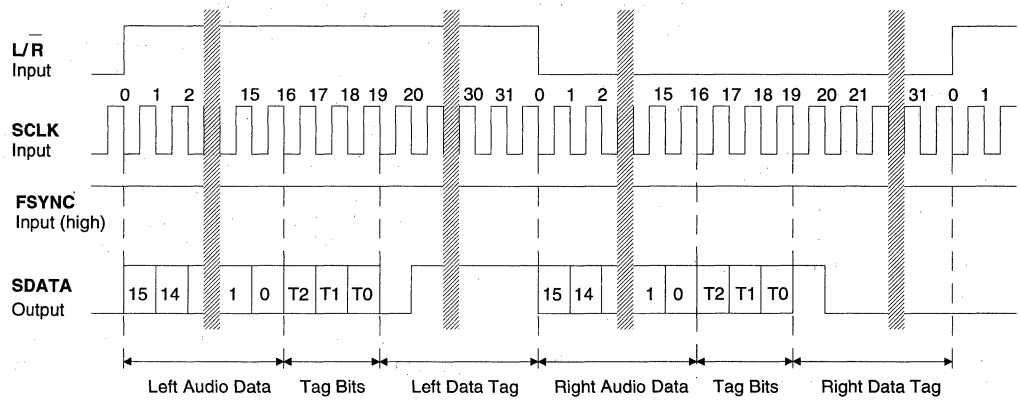


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

CMODE is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between L/$\overline{R}$ edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode, L/$\overline{R}$ and SCLK are inputs. L/$\overline{R}$ must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK

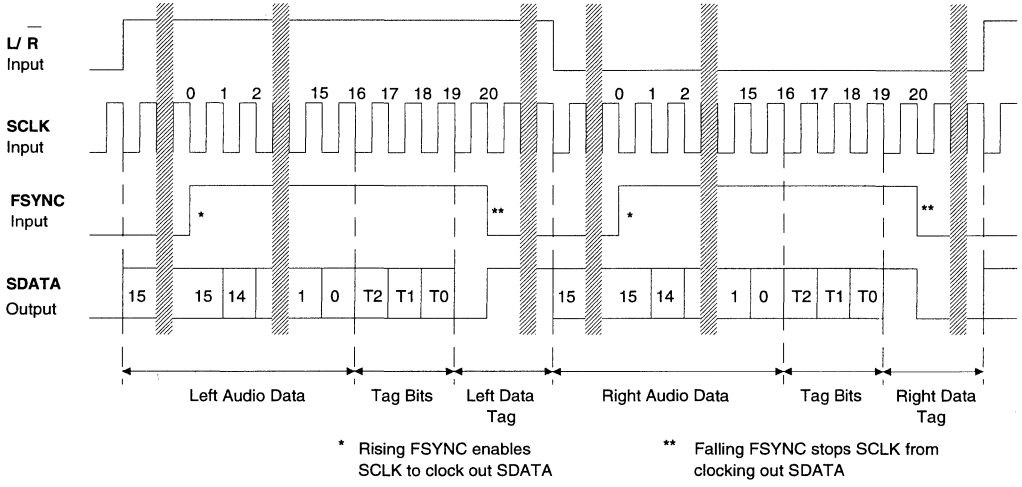


Figure 5 Data Output Timing-SLAVE Mode, FSYNC controlled

and L/$\overline{R}$ inputs. The falling edge of SCLK causes the ADC to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the L/$\overline{R}$ edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the L/$\overline{R}$ edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to position in time the data bits onto a common serial bus.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next L/$\overline{R}$ edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

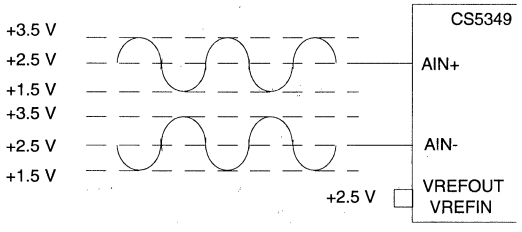
Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125 x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

Table 2. Tag Bit Definition

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 2 Vpp centered at +2.5 V. The + and - input signals are 180° out of phase resulting in an effective input voltage of 4 Vpp. Figure 6 shows the input signal levels for full scale.



Full Scale Input level= (AIN+) - (AIN-)= 2 Vp or 4 Vpp

Figure 6. Full Scale Input Voltage

The CS5349 samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). The digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 100 Ω resistor in series with the analog input, and a 500 pF NPO or COG capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these will degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

As an alternative to Figure 1 input arrangements, Figure 7 shows an active input buffer circuit which produces a differential output and level

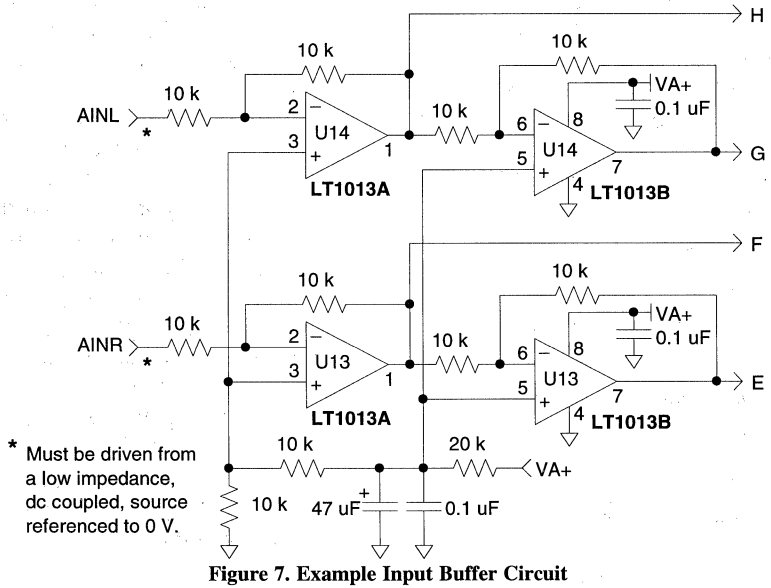


Figure 7. Example Input Buffer Circuit

shifts up to +2.5 V. This circuit must be driven from a source which is referred to 0V dc. If this circuit is used, then the level shifting and AC coupling components shown in Figure 1 are not required.

The on-chip voltage reference output (2.5 V) is brought out to the VREFOUT pin, and normally connected to VREFIN. External reference voltages between 1.5 V and 3.0 V may be used. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached between VREFIN and VA+ eliminates the effects of high frequency noise. No load current may be taken from the VREFOUT output pin.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 0.5 mW. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down feature, APD should be tied to AGND. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10 µF, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input comes from either the analog input signals or by the value obtained from shorting the differential inputs together. This input is determined by the state of the ACAL pin. With ACAL low, the calibration input is obtained from the analog inputs. With ACAL in a high state, the differential inputs are disconnected from the device input pins and shorted internally to provide the calibration input value.

As shown in Figure 8, the DCAL output is high during calibration, which takes 4096 $L/\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage resulting from the shorted inputs. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multiplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any

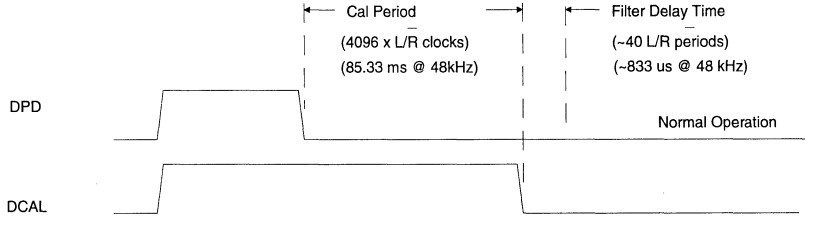


Figure 8. Initial Calibration Cycle Timing

power-on click that might otherwise be experienced. A short delay of approximately 40 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+ and VL+ connected to a clean +5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Synchronization of Multiple CS5349

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD and APD pins to a single control signal and supplying the same ICLKD and L/$\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5349 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD/APD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD/APD pins to the same control signal and insuring that the

DPD/APD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

Digital Filter

Figures 10 through 12 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to ± 0.01 dB maximum. Stopband rejection is greater than 80 dB. Figure 12 is an expanded view of the transition band.

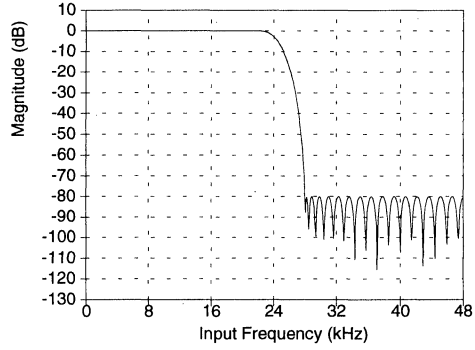


Figure 10. CS5349 Digital Filter Stopband Rejection

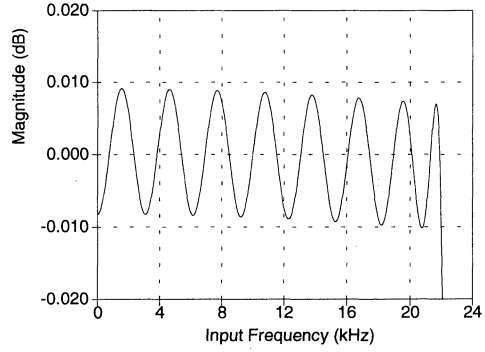


Figure 11. CS5349 Digital Filter Passband Ripple

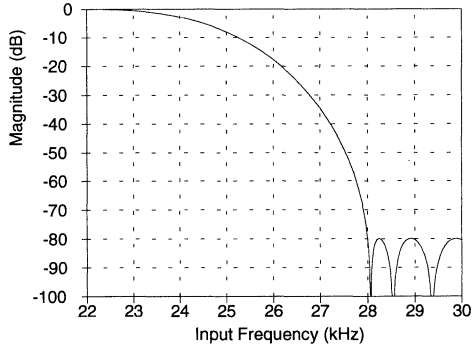


Figure 12. CS5349 Digital Filter Transition Band

Performance Measurements

All the following performance measurements were taken using an Audio Precision System One Dual Domain tester. The CS5349 was in a CDB5349 evaluation board, running at 48 kHz word rate and interfaced to the System One Via the AES/EBU input using a CS8402 AES/EBU transmitter.

Figure 13 shows the frequency response, which is essentially flat.

Figure 14 shows the noise floor with zero input signal level. A 16 K point FFT was used.

Figure 15 shows a 1 kHz, -10 dB input signal FFT plot. Notice the low 2nd harmonic at -110 dB.

Figure 16 shows a 1 kHz, -80 dB input signal FFT plot. Notice the lack of harmonic distortion components. This is a direct result of the perfect differential non-linearity, which is one of the benefits of the delta-sigma technique.

Figure 17 shows the THD+N versus input level at 1 kHz. This plot indicates a dynamic range of 90 dB, with a small increase in distortion with a full scale input.

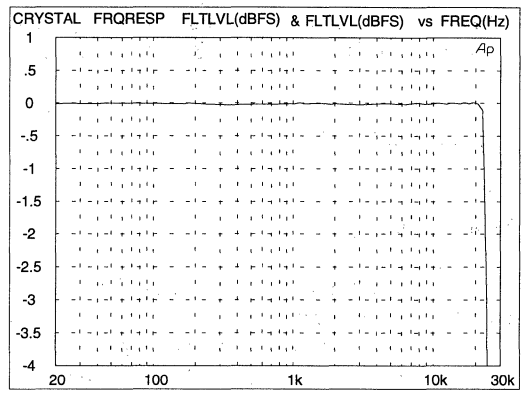


Figure 13. Frequency Response

Figure 18 shows THD+N versus frequency at -10 dB input. This indicates a value of 90 dB, with minor degradation at high frequency.

Figure 19 shows the linearity of the CS5349. The input signal is at 500 Hz and is varied from 0 dB (full scale) to -120 dB. At each input level, the output level is measured and compared to the perfect value. Any deviation is plotted as a deviation away from 0 dB. Notice the close conformance to perfect linearity, until the noise starts to influence the readings at about -100 dB.

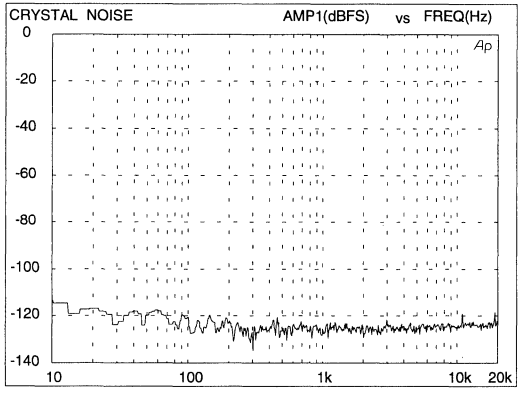


Figure 14 Noise Floor

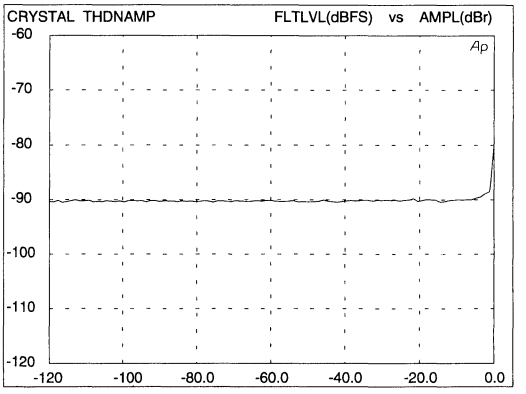


Figure 17. THD+N vs Input level at 1 kHz

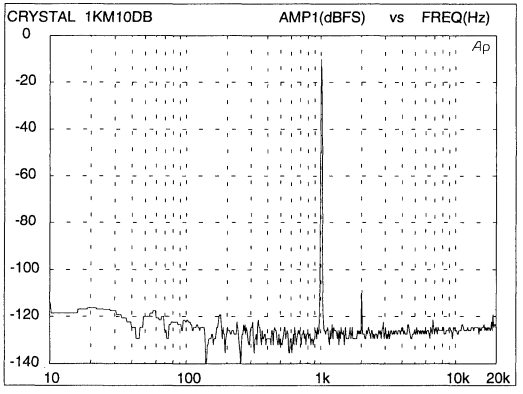


Figure 15. 1 kHz, -10 dB input FFT

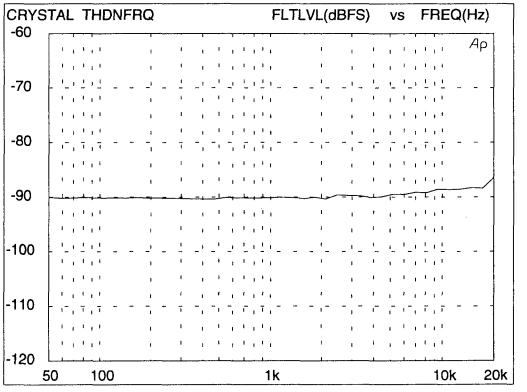


Figure 18. THD+N vs Frequency at -10 dB

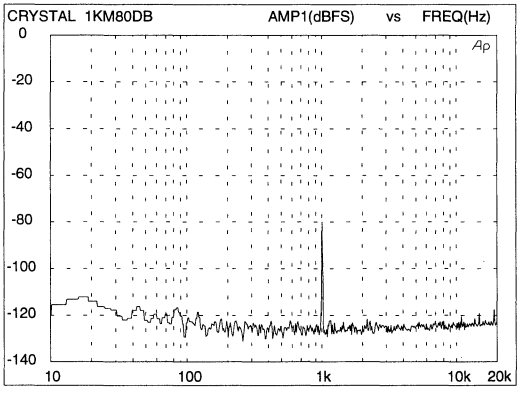


Figure 16. 1 kHz, -80 dB input FFT

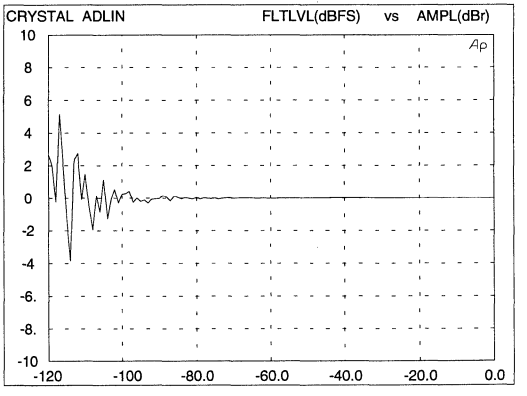
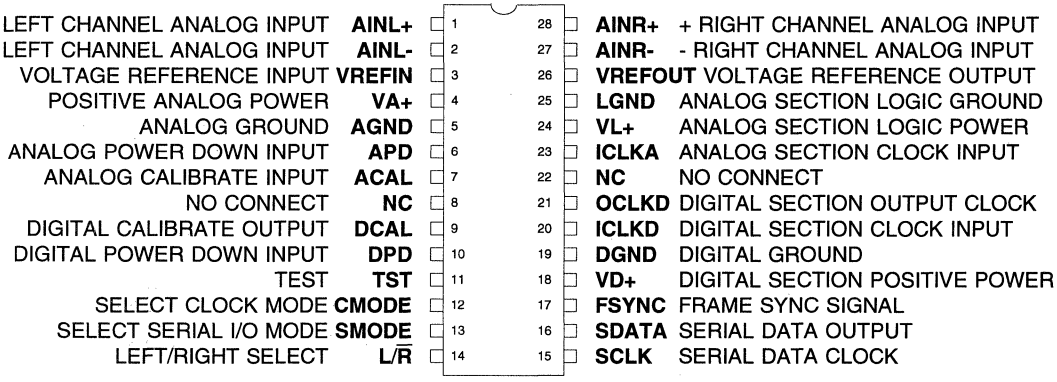


Figure 19. Output level Error vs. Input level at 500 Hz

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 24.
Positive logic supply for the analog section. Nominally +5 volts.

AGND - Analog Ground, PIN 5.
Analog ground reference.

LGND - Logic Ground, PIN 25
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

±AINL, ±AINR - Differential Left and Right Channel Analog Inputs, PINS 1, 2, 27, 28
Analog input connections for the left and right input channels. Nominally 4Vpp full scale.

VREFIN - Voltage Reference Input, Pin 3
Normally tied to VREFOUT for 4Vpp differential input levels.

Analog Outputs

VREFOUT - Voltage Reference Output, PIN 26.

Nominally +2.5 volts. Must be bypassed to VA+ with a 0.1 µF ceramic capacitor in parallel with a 10 µF electrolytic capacitor. Normally connected to VREFIN.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, a 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 20.

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/R periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator differential inputs to be shorted together. May be connected to DCAL.

CMODE - Clock Mode Select, PIN 12.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 13.

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and L/R are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/R are all inputs. In slave mode, L/R, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

SDATA - Serial Data Output, PIN 16.

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/R periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 21.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 15.

Data is clocked out on the falling edge of SCLK.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/R changes.

L/$\overline{R}$ - Left/Right Select, PIN 14.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/R edges occur 1 SCLK cycle before FSYNC rises. When L/R is high, left channel data is on SDATA, except for the first SCLK cycle. When L/R is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/R changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/R starts the MSB of the left channel data. L/R frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/R cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 17.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/R transitions. If it is desired to delay the data bits from the L/R edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/R edge, independent of the state of FSYNC.

Miscellaneous

NC - No Connection, PINS 8, 22.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 11.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

REFERENCES - All reprinted in this data book.

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5349-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5349-BP	16-bits	24 kHz	↓ active	-40°C to 85 °C	28-pin Plastic DIP
CS5349-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5349-BS	16-bits	24 kHz	↓ active	-40°C to 85 °C	28-pin SOIC

CDB5349 CS5349 Evaluation Board

"KP" and "KS" suffix parts are guaranteed to operate over 0°C to 70°C, but tested only at 25°C. "BP" and "BS" suffix parts are tested at the temperature extremes -40°C and +85°C.

Semiconductor Corporation

CDB5349

Evaluation Board for CS5349

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, SPDIF & EIAJ-340 Compatible Digital Audio
- Buffered Serial Output Interface
- 16-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

General Description

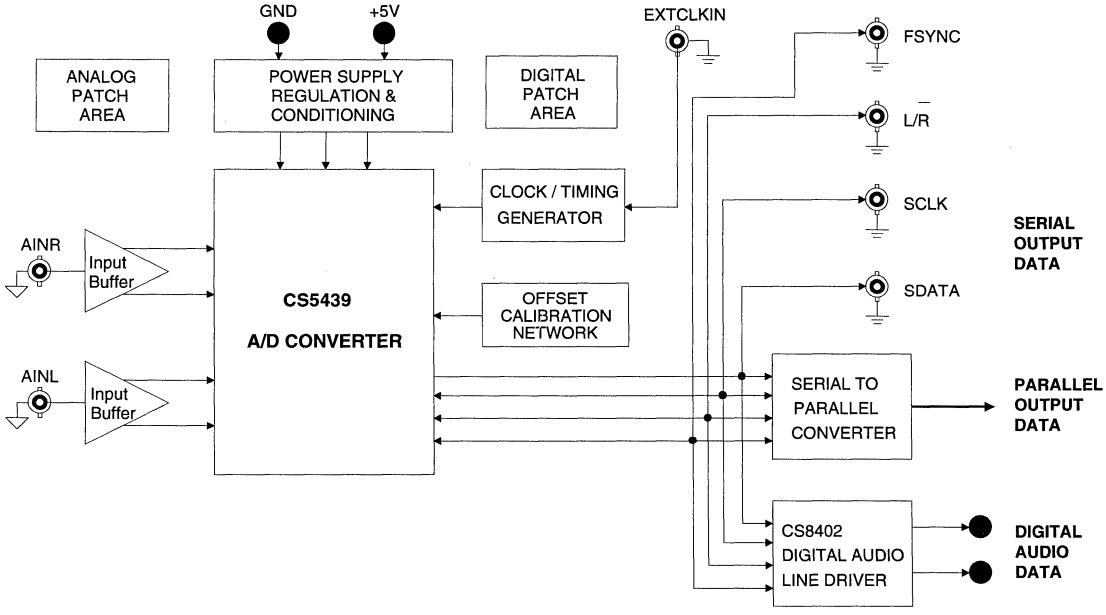
The CDB5349 evaluation board allows fast evaluation of the CS5349 16-bit, stereo A/D converter. The board generates all converter timing signals and provides both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

Also included is a CS8402 digital audio transmitter I.C., which can generate AES/EBU, SPDIF & EIAJ-340 compatible audio data.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:

CDB5349



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Power Supply Circuitry

The schematic diagram in Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by four binding posts. The +5 Volt analog power supply input for the converter is provided by the +5V and AGND binding posts. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts. D1 and D2 are transient suppressers which also provide protection from incorrectly connected power supply leads. C30 provides general power supply filtering for the analog supply. As shown in Figure 2, C10 and C12 provide localized decoupling for the converter VA+ pin. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the converter's VD+ input directly from the VA+ supply. Note that the trace connecting VD+ to L1 must be broken before L1 may be installed. R5 and C7 low-pass filter the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point by J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

Offset Calibration & Reset Circuit

Figure 1, shows the optional offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Analog to Digital Converter's DPD pin initiating an offset calibration cycle. Releasing SW1 also initiates an offset calibration cycle. P6 (see Figure 2) selects the signal source used during offset calibration. In the "AIN" position, the AINL and AINR inputs are selected during calibration. In the "ZERO" position, the AINL and AINR inputs are disconnected and the differential inputs shorted for calibration.

Analog Inputs

As shown in Figure 2, the analog input signals are connected to the CS5349 via an RC network.

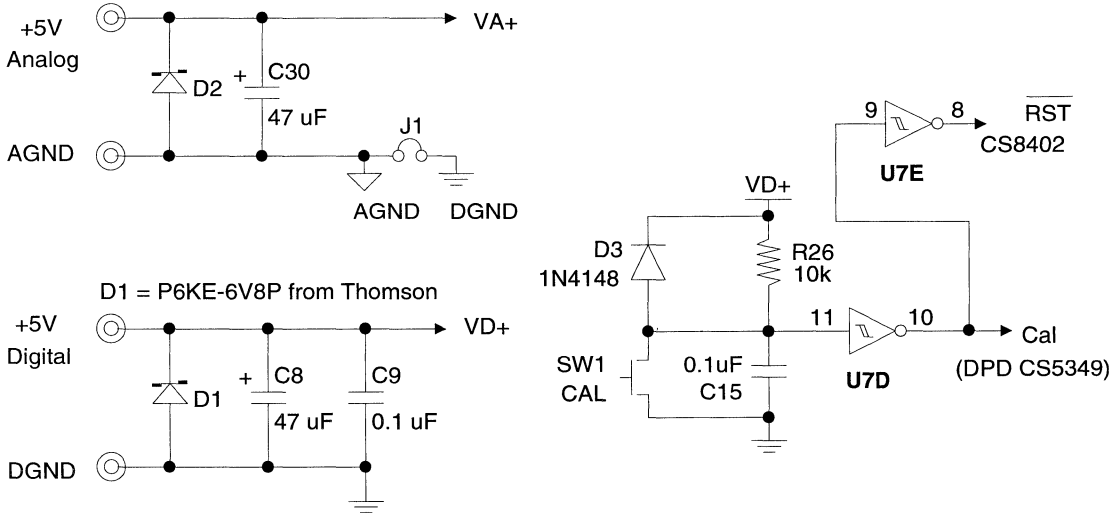


Figure 1. Power Supply and Reset Circuitry

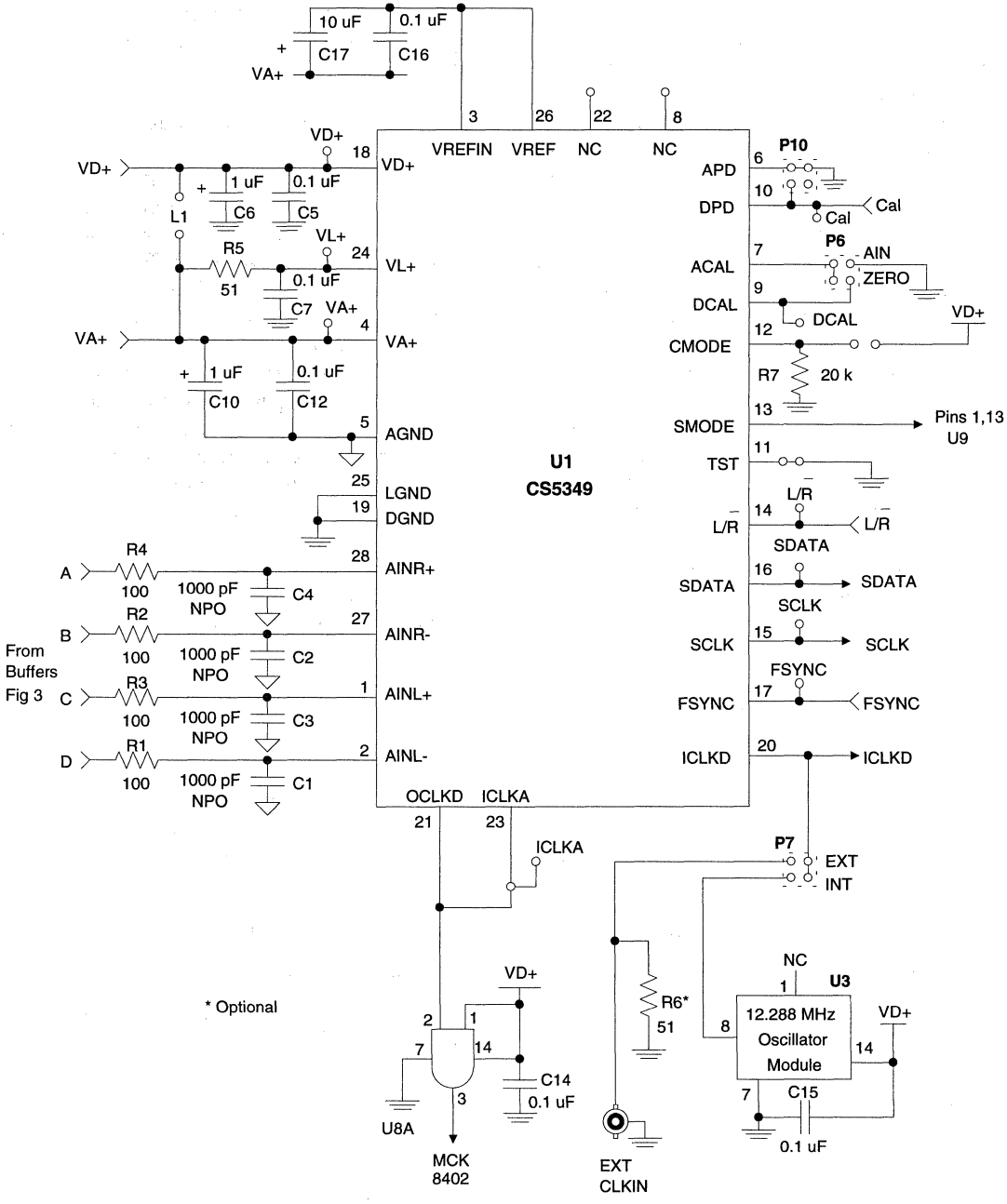


Figure 2. ADC Connections

R1-R4 and C1-C4 provide antialiasing and optimum source impedance for the analog input channels.

Figure 3 shows the input buffer circuit. This circuit converts the single ended inputs to differential, and also elevates the center point of the differential singles to approximately +2.5 VThis can be used as an example input buffer circuit for your application.

Timing Generator

P7 selects the master clock source supplied to the ICLKD pin of the converter. As shipped from the factory, P7 is set to the "INT" position to select the 12.288 MHz clock signal provided by U3. An external master clock signal may be connected to the EXTCLKIN connector and selected by placing P7 in the "EXT" position. Note that R6, tied between EXTCLKIN and GND, is available for impedance matching an external clock source. The board is shipped with SMODE high, which selects MASTER timing mode. In this mode, SCLK, L/$\overline{R}$ and FSYNC are all outputs, generated by the converter from ICLKD.

Digital Audio Standard Interface

Included on the evaluation board is a CS8402 Digital Audio Line Driver. This device can implement AES/EBU, S/PDIF and EIAJ-340 interface standards. Figure 4 shows the schematic for the CS8402. P3 allows the C, U and V bits to be driven from external logic. SW2 provides 8 DIP switches to select various modes and bits for the CS8402. An output transformer is included. A position for R20 is included to allow use in the consumer output mode. See the CS8401 & CS8402 part data sheet for more information on the operation of the CS8402.

Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, FSYNC and L/$\overline{R}$ BNC connec-

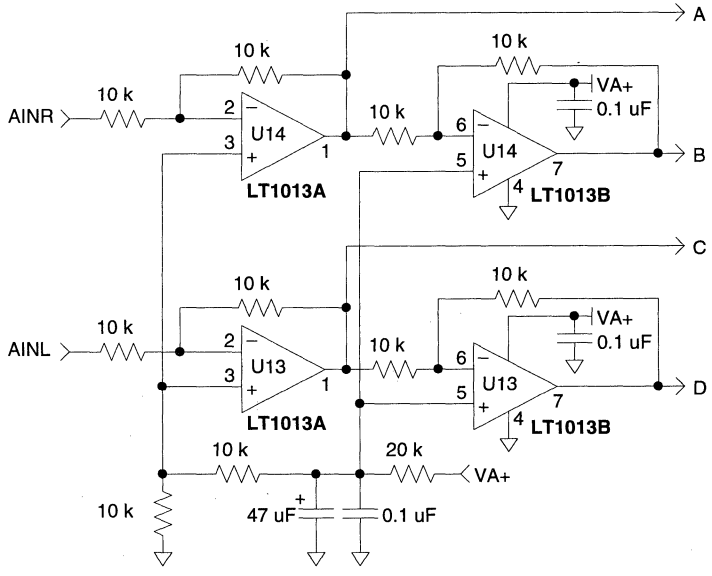


Figure 3. Input Buffer Circuit

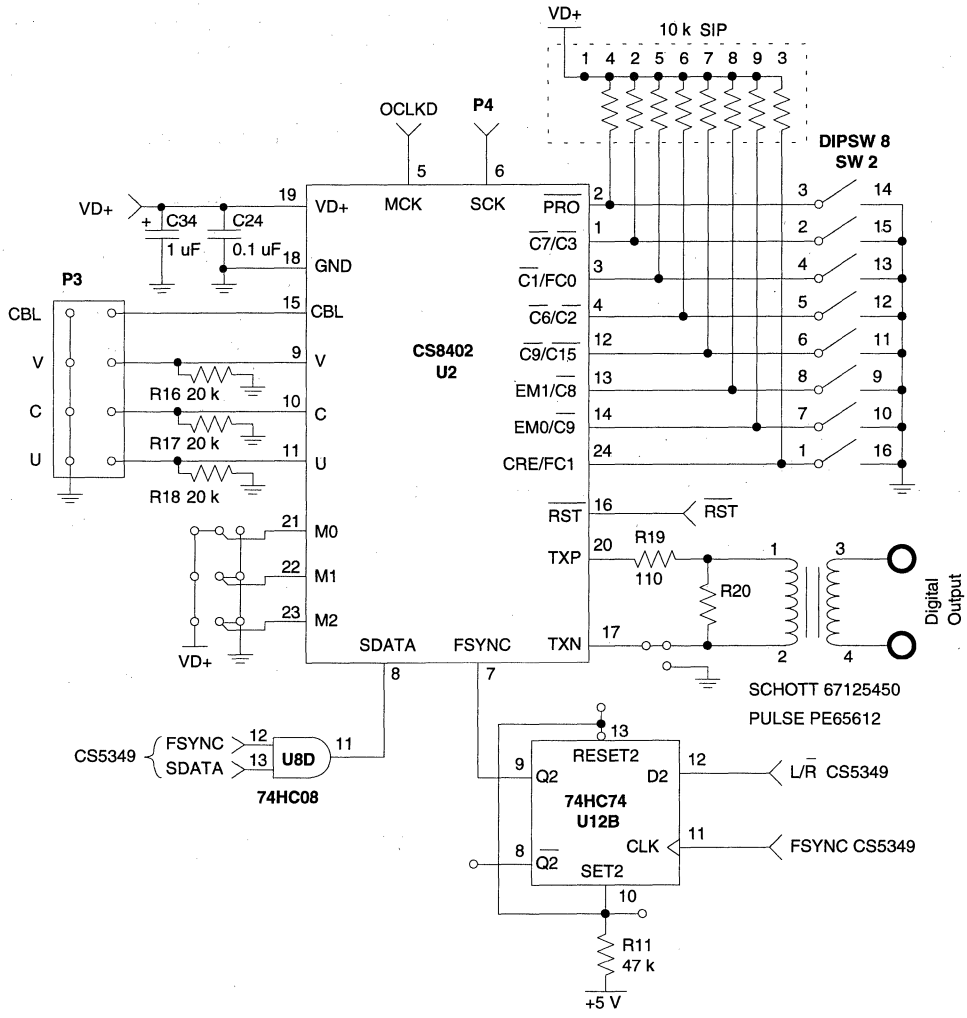


Figure 4. CS8402 Digital Audio Line Driver Connections

tors on the evaluation board. These outputs are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. If slave mode is selected by pulling SMODE low, then U9 (74HC243) will change to the opposite direction, and act as an input buffer. U9 is provided to protect against inadvertent external driving of SCLK, L/$\overline{R}$ and FSYNC while in MASTER mode. U9 is not necessary in your application circuit.

Jumper P4 allows the board to be configured for either the CS5346, or the CS5349, which have opposite polarities of SCLK.

Parallel Output Interface

Figure 6 depicts the parallel output interface on the evaluation board. 16-bit words are assembled from the serial data output of the converter. Each bit of serial data is clocked out of the converter

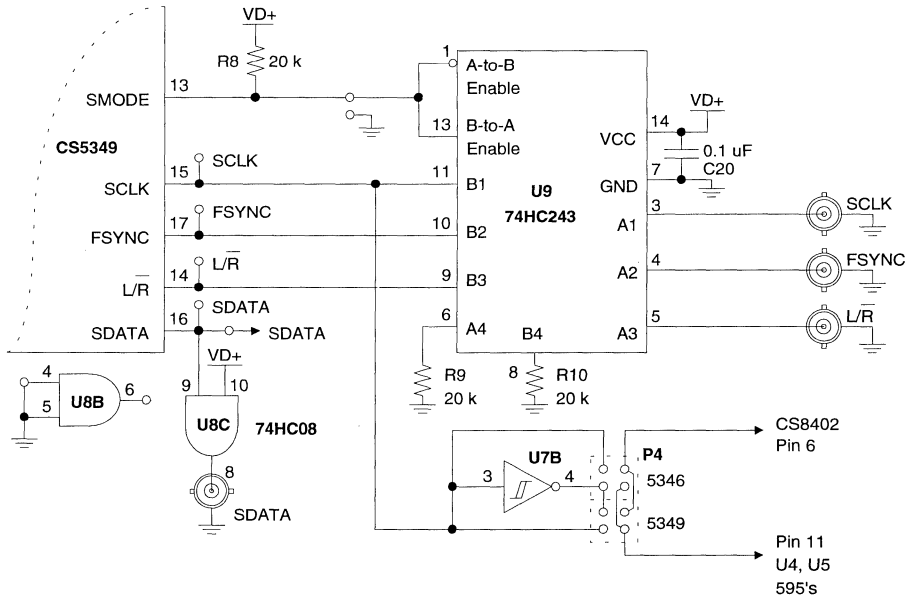


Figure 5. Serial Output Interface

on the rising edge of SCLK and shifted into the 16-bit shift register formed by U4 and U5 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U4 and U5 the data is latched onto P1 by a delayed version of FSYNC.

P5 selects the channel whose output data will be converted to parallel form and presented on P1. With P5 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the edges of L/$\overline{R}$ may be used to clock the parallel data into the digital signal processor. (Set jumper P2 into the L/$\overline{R}$ position.) Alternatively, a handshake protocol implemented with DACK and $\overline{DRDY}$ may be used to transfer data to the signal processor. (Set jumper P2 to the $\overline{DRDY}$ position.) The fall of $\overline{DRDY}$ informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that $\overline{DRDY}$ will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.

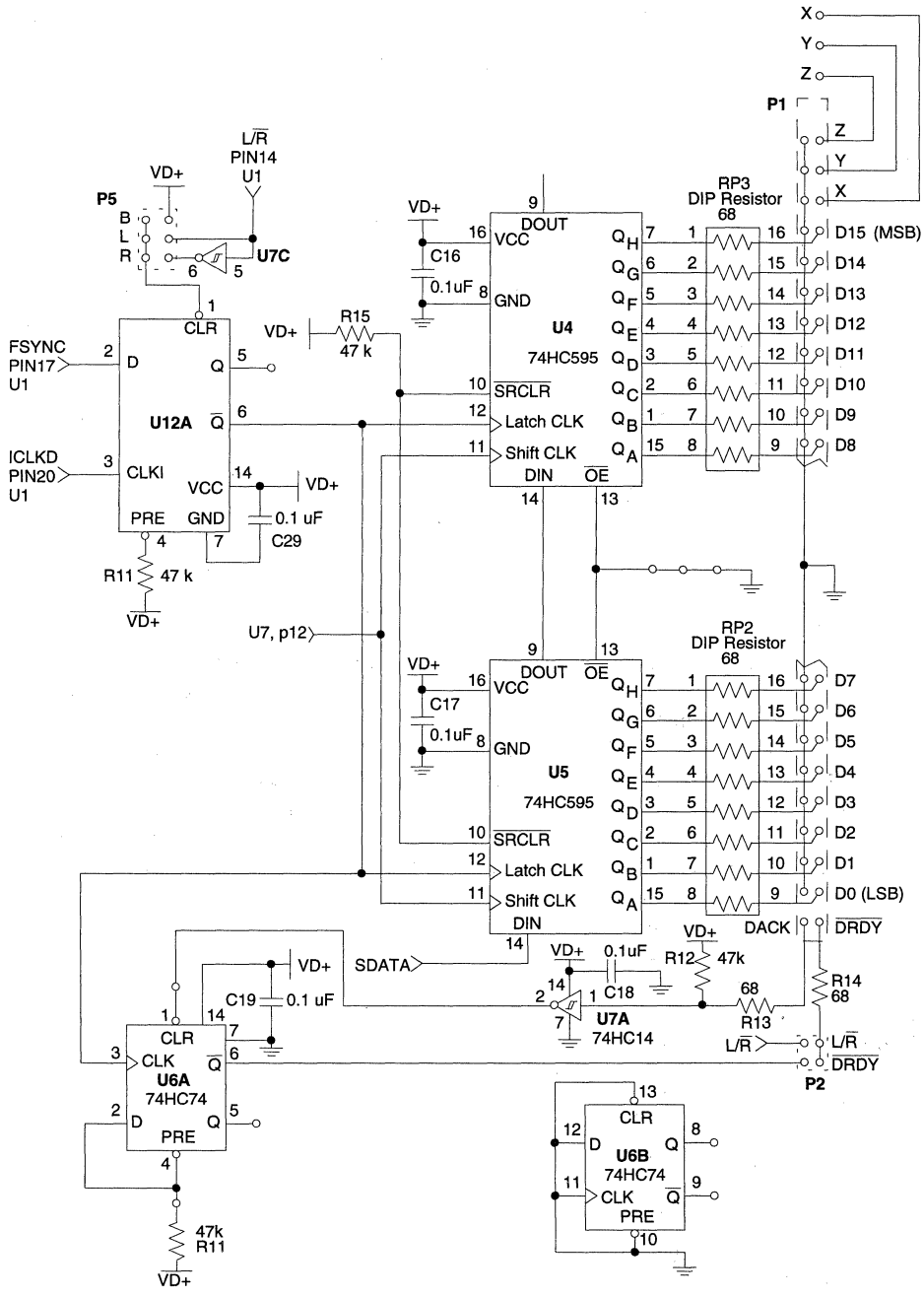


Figure 6. Parallel Output Interface

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 ANALOG	input	+5 Volts from analog power supply
AGND	input	analog ground connection from power supply
+5 DIGITAL	input	+5V digital supply for ADC VD+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
$\overline{L/R}$	output/input	left /right channel signal
SDATA	output	serial output data
SCLK	output/input	serial output clock
FSYNC	output/input	data framing signal
DIGITAL OUTPUT	output	CS8402 digital output via transformer
P3	output/input	CS8402 C,U,V inputs; CBL output
P1	output	parallel output data

Table 1. Systems Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
P6	selects signal offset or shorted inputs for calibration	AIN	offset cal to signal input
		ZERO	offset cal to shorted inputs
P7	selects master clock source for CS5349	*INT	CLKIN provided by U2
		EXT	CLKIN provided by EXTCLKIN BNC
P5	selects channel for serial to parallel conversion	*L	left channel data presented on P5
		R	right channel data presented on P5
		B	left then right channel data alternately presented on P5
P2	selects $\overline{L/R}$ or $\overline{DRDY}$ as the output status signal presented on P1	*$\overline{DRDY}$	$\overline{DRDY}$ selected to signal the arrival of new data for the selected channel
		$\overline{L/R}$	$\overline{L/R}$ selected
P4	selects device type	5349	Correct SCLK for CS5349
		5346	Correct SCLK for CS5346

* Default setting from factory

Table 2. Jumper Selectable Options

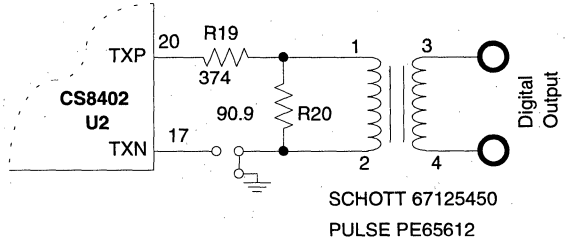
Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=0	Professional Mode C0=1(default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated
2,5	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	$\overline{C1}$	C1 - Audio
default	1 0	0 - Normal Audio 1 - Non-Audio
6	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8,7	EM1, EM0	C2,C3,C4 - Emphasis (2 of 3 bits)
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 µs 111 - CCITT J.17

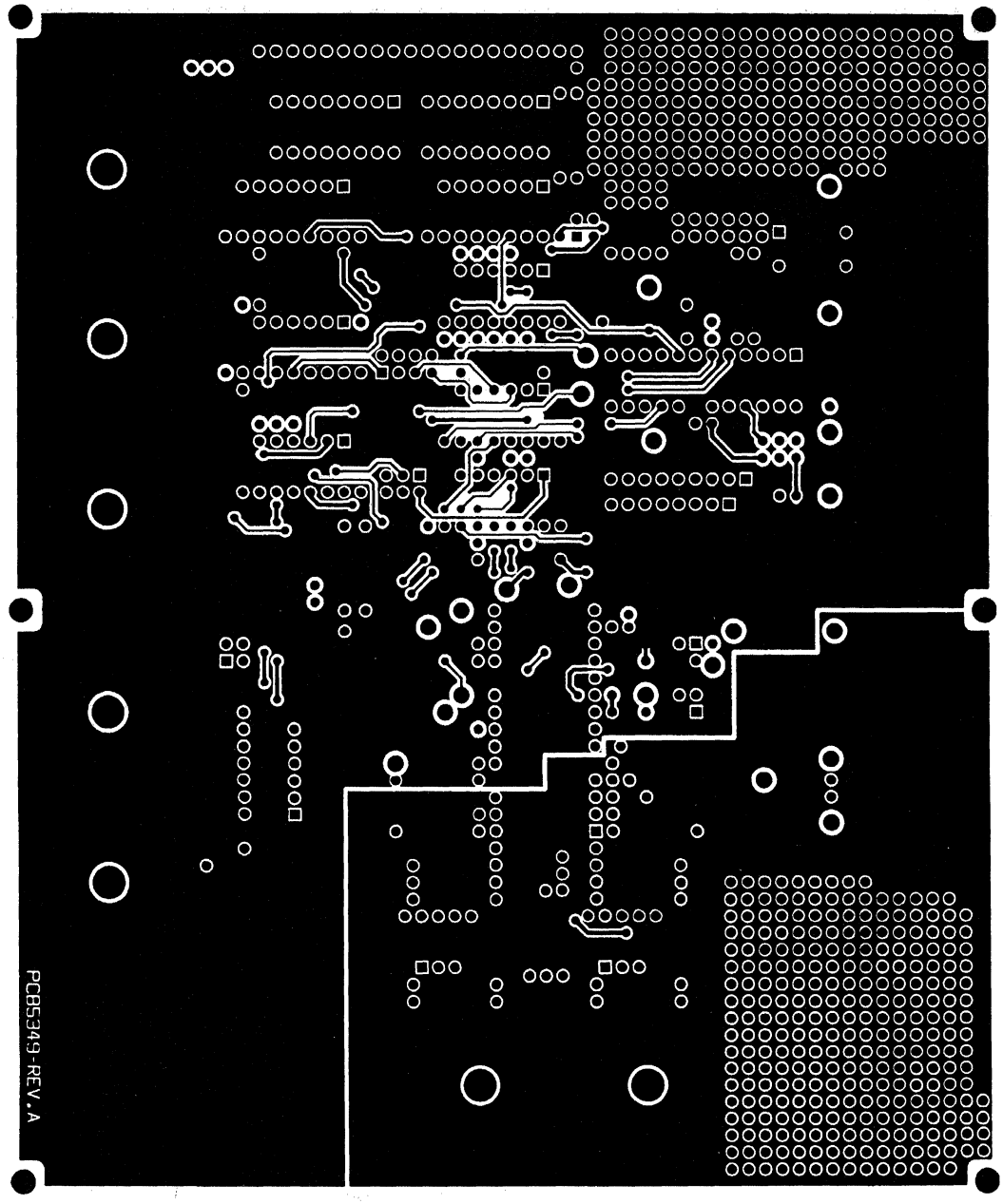
Table 3. Switch Definitions - Professional Mode

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=1	Consumer Mode C1=0 (Note 1)
1,4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency
	0 0	0000 - 44.1 kHz
	0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
2	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1	000 - None
	0	100 - 50/15 µs
5	$\overline{C2}$	C2 - Copy/Copyright
	1	0 - Copy Inhibited/Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
6	$\overline{C15}$	C15 - Generation Status
	1	0 - Definition is based on category code.
	0	1 - See CS8402 Data Sheet, App. A
8,7	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	0 0	1100000 - Digital Audio Tape - DAT

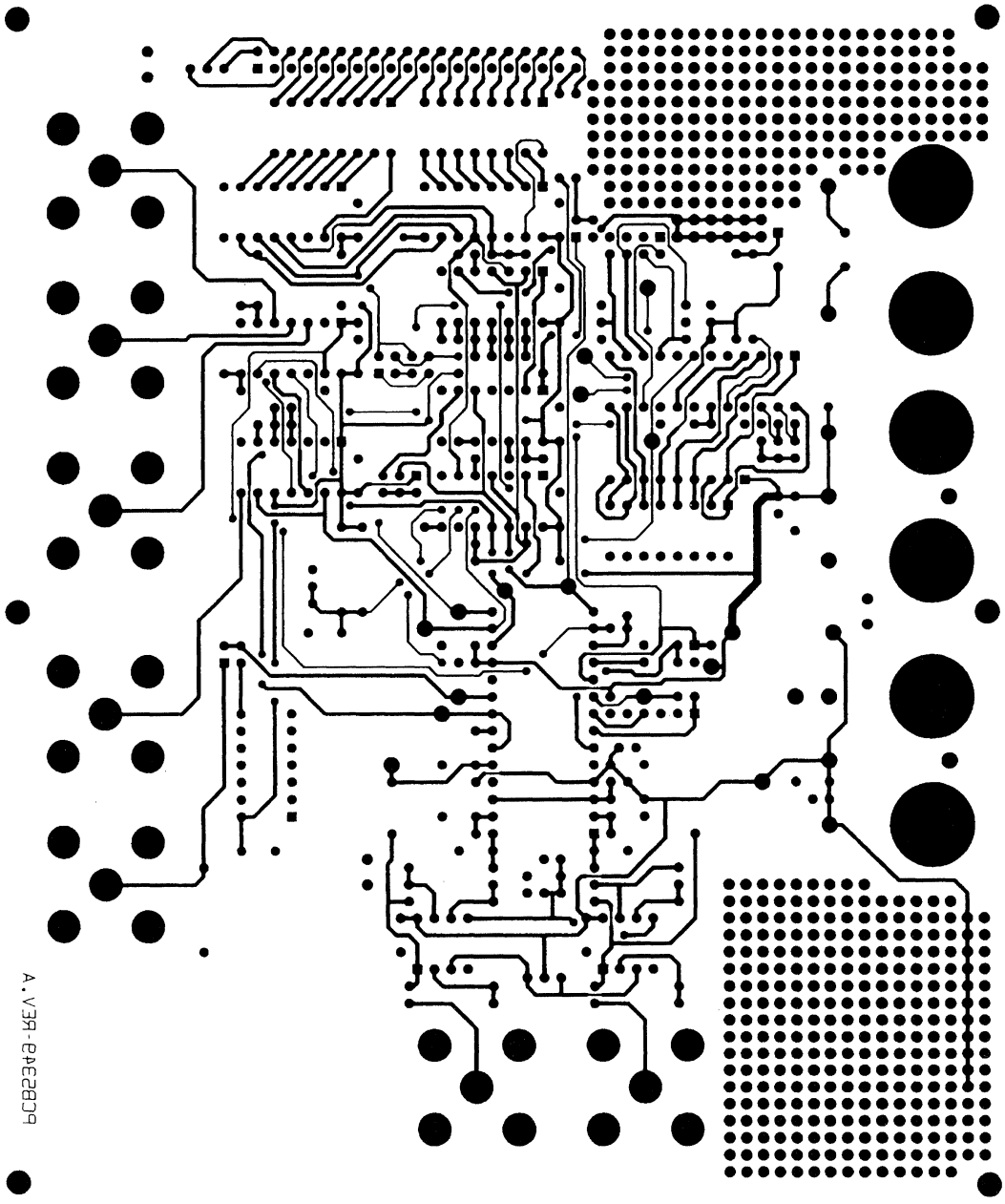
Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R19 to 374Ω and add R20 at 90.9Ω. Then, as shown in the figure below, cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided. For a full explanation, see the CS8402 data sheet, Appendix B.

Table 4. Switch Definitions - Consumer Mode

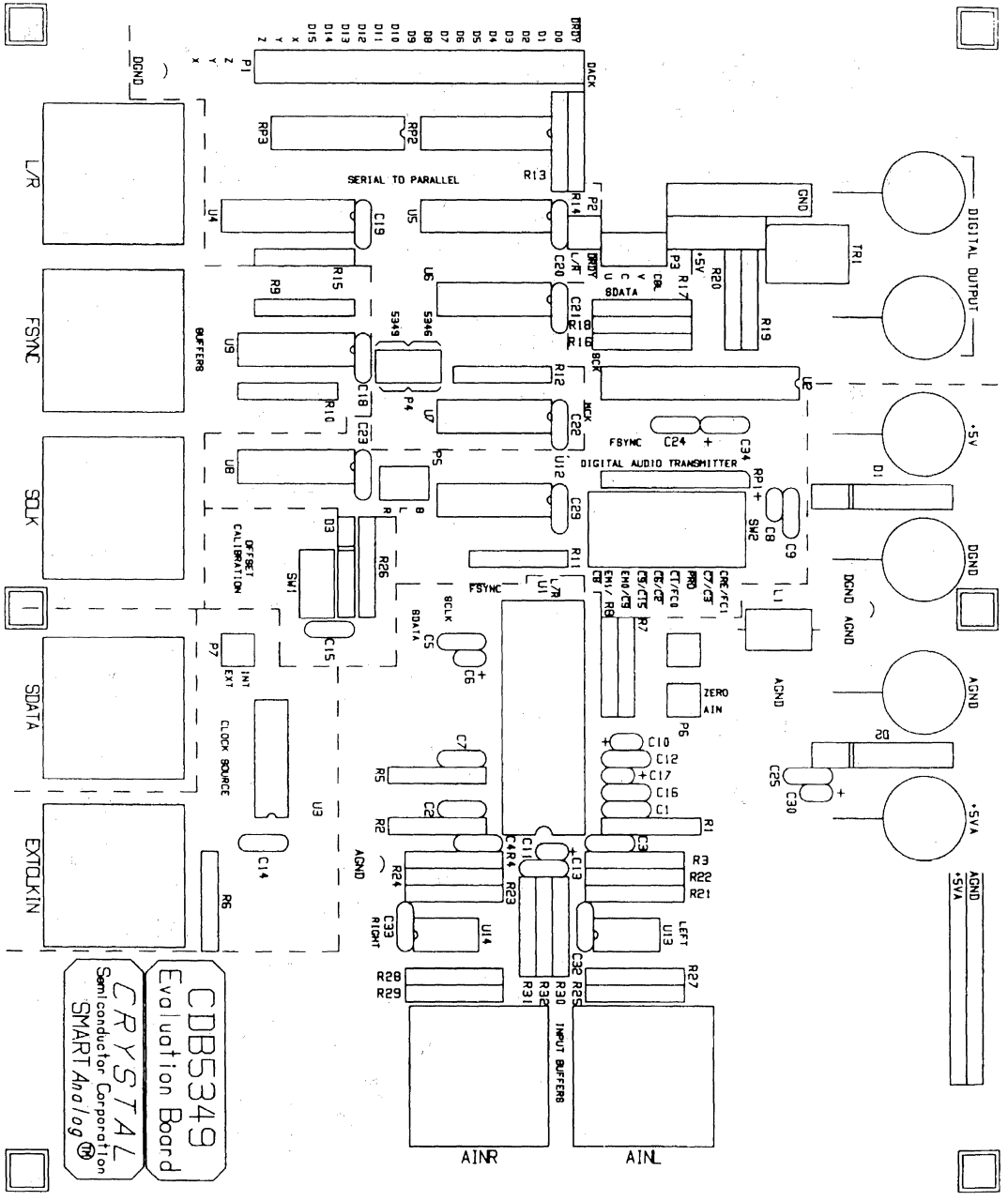




Top Ground Plane Layer (NOT TO SCALE)



Bottom Trace Layer (NOT TO SCALE)



Silk Screen Layer (NOT TO SCALE)

Semiconductor Corporation

CS5389

18-Bit, Stereo A/D Converter for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 107 dB Dynamic Range (A-Weighted)
- Low Noise and Distortion 100 dB THD + N
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
- Low Power Dissipation: 550 mW Power-Down Mode
- Evaluation Board Available

General Description

The CS5389 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5389 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

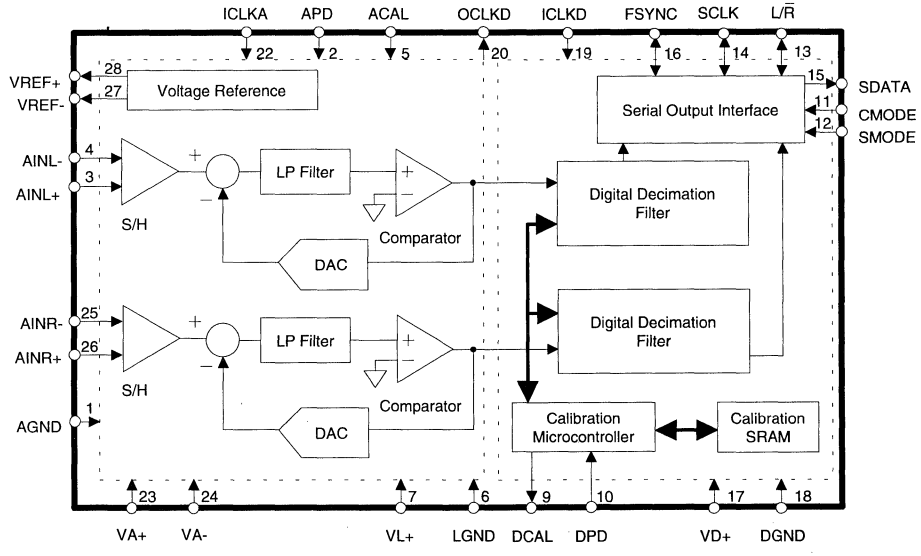
The CS5389 has a filter passband of dc to 24kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The CS5389 is targeted for the most demanding professional audio systems requiring wide dynamic range and low noise and distortion.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS5389-KP	0° to 70°C	28-pin Plastic DIP

3



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VL+,VD+ = 5V; VA- = -5V; Full-scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 39Ω with 6.8 nF across AIN+, AIN-; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD+;

Parameter		Symbol	Min	CS5389-K Typ	Max	Units
Resolution			18	-	-	Bits
Dynamic Performance						
Dynamic Range			102	104	-	dB
	(A-weighted)		-	107	-	dB
Total Harmonic Distortion + Noise		THD+N				
	0 dB		-	-100	-	dB
	-20 dB		-	-84	-82	dB
	-60 dB		-	-44	-42	dB
Interchannel Phase Deviation			-	0.0001	-	°
Interchannel Isolation			106	120	-	dB
dc Accuracy						
Interchannel Gain Mismatch			-	0.05	-	dB
Gain Error			-	±1	±5	%
Gain Drift			-	50	150	ppm/°C
Bipolar Offset Error (After Calibration)			-	±5	±20	LSB
Offset Calibration Range			-	±50	-	mV
Analog Input						
Full-scale Differential Input Voltage (Note 1)		V_{IN}	14.0	14.72	-	Vpp
Input Impedance		Z_{IN}	-	25	-	kΩ
Common-Mode Rejection		CMRR	-	115	-	dB
Power Supplies						
Power Supply Current	(VA+)+(VL+)	I_{A+}	-	37.5	55	mA
with APD, DPD low	VA-	I_{A-}	-	37.5	55	mA
(Normal Operation)	VD+	I_{D+}	-	35.0	50	mA
Power Supply Current	(VA+)+(VL+)	I_{A+}	-	100	-	µA
with APD, DPD high	VA-	I_{A-}	-	100	-	µA
(Power-Down Mode)	VD+	I_{D+}	-	100	-	µA
Power Consumption	(APD, DPD Low)	PDN	-	550	800	mW
	(APD, DPD High)	PDS	-	1.5	-	mW
Power Supply	(dc to 28 kHz)	PSRR	-	65	-	dB
Rejection Ratio	(28 kHz to 3.046 MHz)		-	100	-	dB

Notes: 1. Specified for a fully differential input ±{(AINR+)-(AINR-)}.The ADC accepts input voltages up to the analog supplies (VA+, VA-). Full-scale outputs will be produced for differential inputs beyond V_{IN}. This value is subject to the gain error tolerance specification

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%; Output word rate of 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Passband	(-3dB)		0	-	24	kHz
	(-0.01 dB)		0	-	22	kHz
Passband Ripple			-	-	±0.01	dB
Stopband			28	-	3044	kHz
Stopband Attenuation	(Note 2)		80		-	dB
Group Delay (OWR = Output Word Rate)		t_{gd}	-	18/OWR	-	s
Group Delay Variation vs Frequency		Δt_{gd}	-	-	0.0	µs

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are (n x 3.072MHz) ±22kHz, where n = 0,1,2,3...

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30%VD+	V
High-Level Output Voltage at I_O = -20 µA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at I_O = 20 µA	V_{OL}	-	-	0.1	V
Input Leakage Current	I_{in}	-	1.0	-	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Negative Analog	VA-	+0.3	-	-6.0	V
	Positive Logic	VL+	-0.3	-	+6.0	V
	Positive Digital	VD+	-0.3	-	+6.0	V
	|VA+ - VD+|		-	-	0.4	V
	|VA+ - VL+|		-	-	0.4	V
	|VD+ - VL+|		-	-	0.4	V
Input Current	Any Pin Except Supplies	I_{in}	-	-	±10	mA
Peak Analog Input Voltage (AINL+/- and AINR +/- pins)		V_{IN}	(VA-)-0.4	-	(VA+)+0.4	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

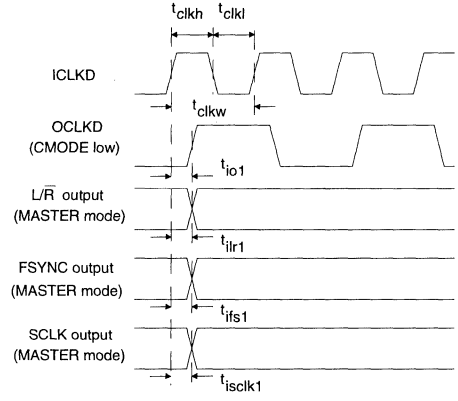
WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

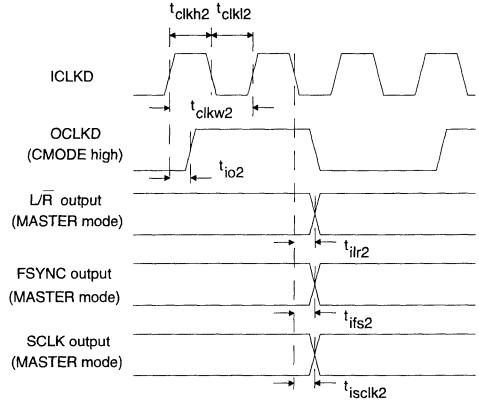
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t_{clkw1}	78	-	3906	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	2604	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK falling to SDATA valid (MASTER mode)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK falling to L/$\overline{R}$ (MASTER mode)	t_{mslr}	-20	-	20	ns
SCLK falling to FSYNC (MASTER mode)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid (SLAVE mode)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Rising SCLK to L/$\overline{R}$ edge delay (SLAVE mode)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to rising SCLK setup time (SLAVE mode)	t_{slr2}	30	-	-	ns
Rising SCLK to rising FSYNC delay (SLAVE mode)	t_{sfs1}	30	-	-	ns
Rising FSYNC to rising SCLK setup time (SLAVE mode)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	2 x t_{clkw}	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}		4096		1/OWR

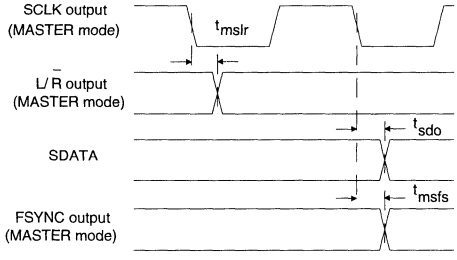
Notes: 3. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).



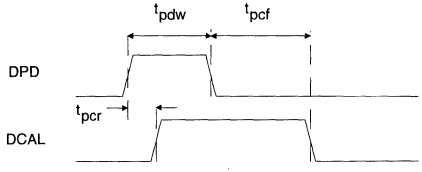
ICLKD to Outputs Propagation Delays (CMODE low)



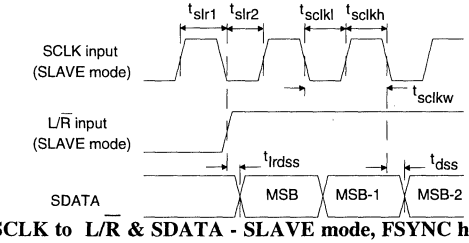
ICLKD to Outputs Propagation Delays (CMODE high)



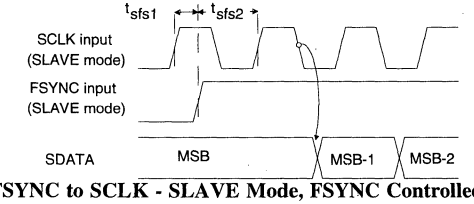
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	|VA+ - VD+|	-	-	-	0.4	V

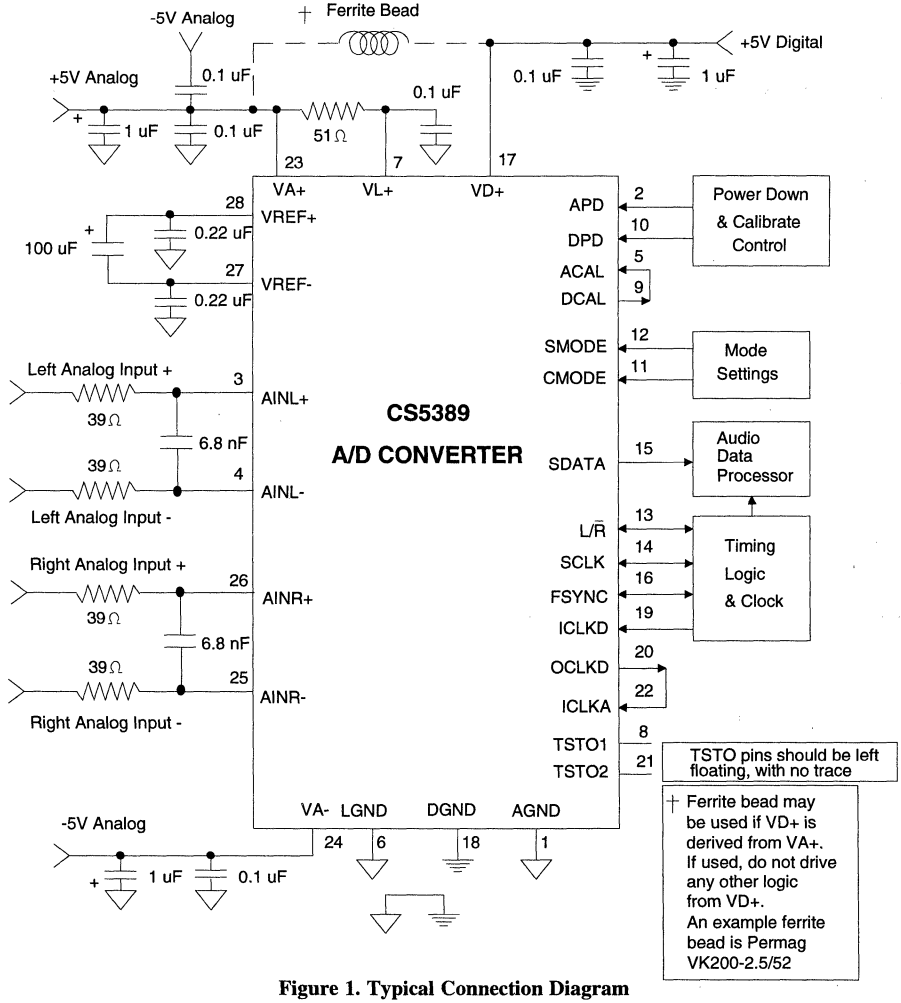


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5389 is an 18-bit, stereo A/D converter designed specifically for stereo digital audio applications. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 18-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and it does not require external sample-and-hold amplifiers or voltage references.

On-chip voltage references provide for a differential input signal range of ± 14.72 volts. Any offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 18-bit numbers. Typical power consumption of only 550 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter and is used to generate the modulator sampling clock. The required ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the ICLKD frequency to 384 X OWR, while CMODE low will set the ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when CMODE is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD di-

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

vided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

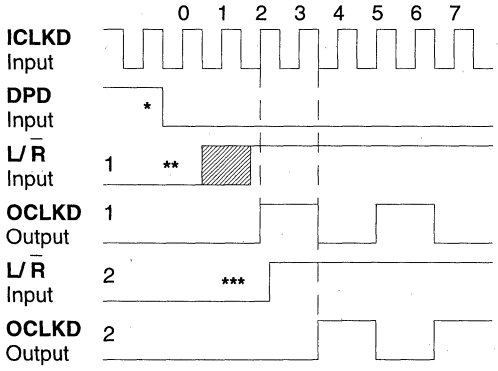


Figure 2. ICLKD to OCLKD Timing with CMODE high (384XOWR)

Serial Data Interface

MASTER mode and SLAVE mode are the 2 primary modes of operation for the serial data output interface.

Master Mode

SCLK, L/$\overline{R}$ and FSYNC are outputs derived from ICLKD in Master mode, Figure 3. Notice the one SCLK cycle delay between L/$\overline{R}$ edges, SDATA and FSYNC. FSYNC brackets the 16 most significant data bits.

Slave Mode

L/$\overline{R}$, FSYNC and SCLK become inputs in SLAVE mode. L/$\overline{R}$ must be externally derived from ICLKD and be equal to the Output Word Rate. SCLK should be equal to 64 X OWR though other frequencies are possible but may degrade system performance due to interference effects. FSYNC may be high or used to control SDATA. With FSYNC high, data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The falling edge of SCLK causes the ADC to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge, as shown in Figure 4.

SCLK is ignored with FSYNC low and only the MSB is clocked out after the L/$\overline{R}$ edge in SLAVE mode / FSYNC controlled as shown in Figure 5. Bringing FSYNC high will enable SCLK to clock data out. This feature is particularly useful to multiplex multiple channels.

Certain serial modes align well with various interface requirements. A CS5389 in MASTER mode, with an inverted L/$\overline{R}$ signal, generates I^2S (Philips) compatible timing. A CS5389 (with an inverted SCLK) in SLAVE mode emulates a CS5326 style interface and also links to a DSP56000 in network mode.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 7.36 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 14.72 Vpp. Figure 6 shows the input signal levels for full scale.

The analog modulator samples the input at 3.072 MHz (64 x Fs) for an output word rate of 48 kHz. The digital filter will reject signals between 22 kHz and 3.072 MHz - 22 kHz. However, there is no rejection for input signals which are (n x 3.072 MHz) +/- 22 kHz, where n = 0,1,2,... A 39 Ω resistor in series with the ana-

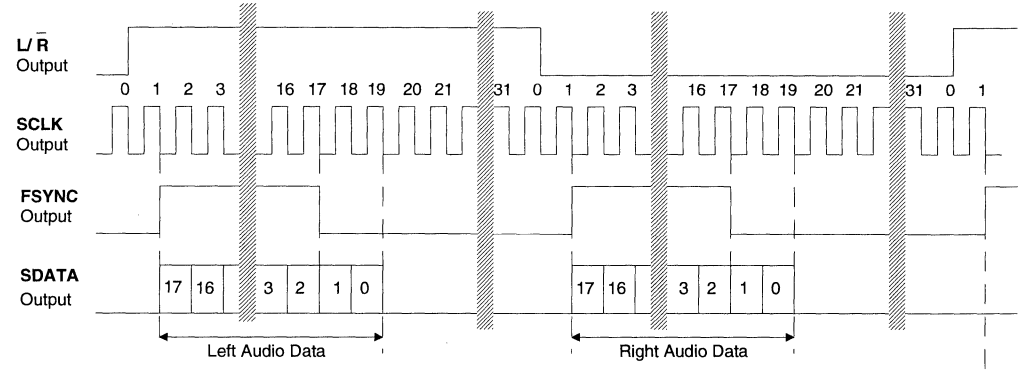


Figure 3. Data Output Timing - MASTER mode

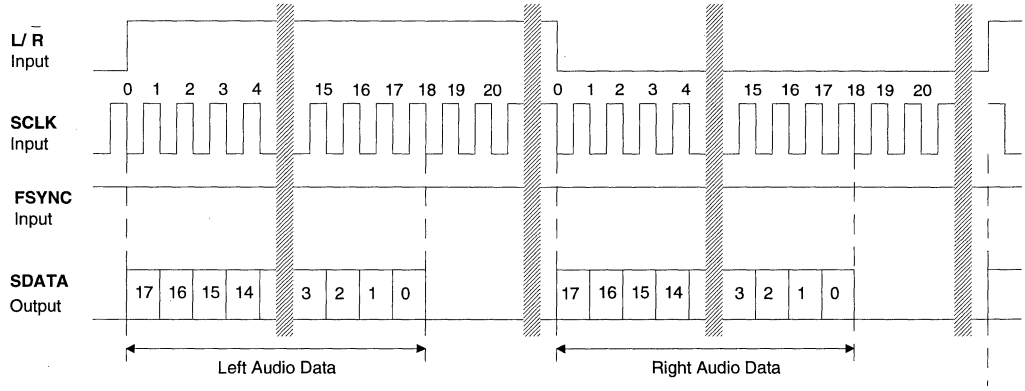
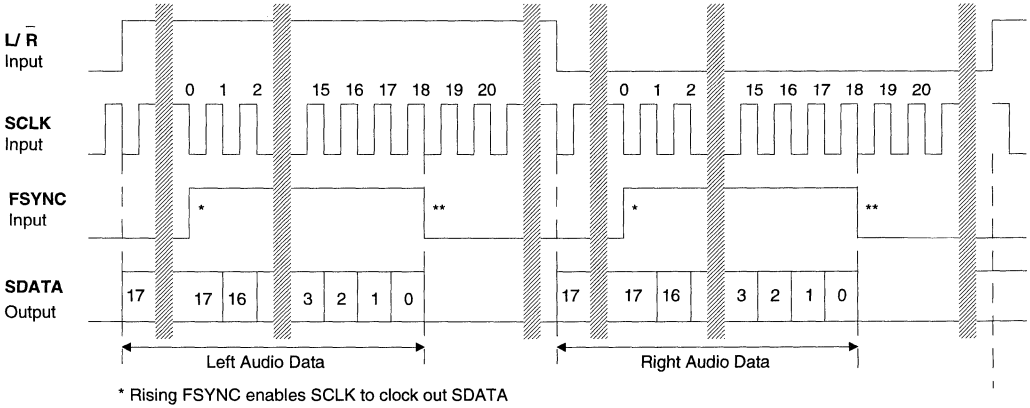


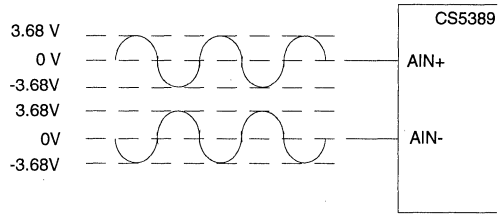
Figure 4. Data Output Timing - SLAVE Mode, FSYNC high



* Rising FSYNC enables SCLK to clock out SDATA

** Falling FSYNC stops SCLK from clocking out SDATA

Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled



Full Scale Input level= (AIN+) - (AIN-)= 14.72 Vpp

Figure 6. Full Scale Input Voltage

log input and a 6.8 nF NPO or COG capacitor between the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage references are available at the VREF+ and VREF- pins for the purpose of decoupling only. The circuit traces attached to these pins must be minimal in length and no load current may be taken from VREF+ or VREF-. The recommended decoupling scheme, Figure 1, is a 100 µF electrolytic capacitor across VREF+ and VREF- and two 0.22 µF ceramic capacitors connected from VREF+ to GND and VREF- to GND.

Power-Down and Offset Calibration

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode wherein typical power consumption drops to 1.5 mW.

Bringing DPD low exits power-down and initiates an offset calibration cycle. During the calibration cycle, the digital section measures the offset of each channel and stores a corresponding value in the calibration registers. This value is subtracted from future conversions to produce an offset free conversion. The calibration inputs are obtained from the analog input pins (ACAL low) or AGND (ACAL high).

The offsets generated by the input circuitry are included when calibration is performed using the analog input pins (ACAL low). DCAL should be used to control a multiplexer which grounds the user's front-end in this mode. The DCAL output will remain high for 4096 L/$\overline{R}$ clock cycles during calibration as shown in Figure 7.

A delay of approximately 50 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

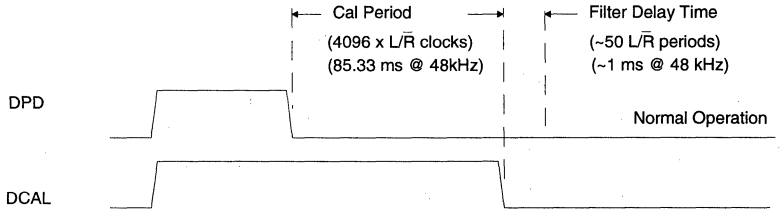


Figure 7. Initial Calibration Cycle Timing

The modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. The voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF+ and VREF- pins. A time delay of approximately 10 ms/µF is required between APD going low and DPD going low to allow for VREF settling. The typical connection diagram of Figure 1 requires a 1 second delay.

APD should be tied to AGND if the analog power down feature is not required. When using the analog power down feature, DPD and APD may be tied together if the capacitor across VREF+ and VREF- is not greater than 10 µF. Figure 17 shows that a slight increase in distortion will result for signals below 1 kHz and within 6 dB of fullscale due to less than optimum VREF decoupling. Figure 17 demonstrates this effect at a -4 dB input level.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean ± 5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF+ and VREF- pins in order to avoid unwanted coupling into the modulators. The VREF+ and VREF- decoupling capacitors, particularly the 0.22 µF, must be positioned to minimize the electrical path from VREF+ and VREF- to Pin 1, AGND. The CDB5389 evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Synchronization of Multiple CS5389

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD pins to a single control signal and supplying the same ICLKD and L/$\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5389 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD pins to the same control signal and insuring that the DPD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

Digital Filter

Figures 8 and 9 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to ± 0.01 dB maximum. Stopband rejection is greater than 80 dB. Figure 10 is an expanded view of the transition band.

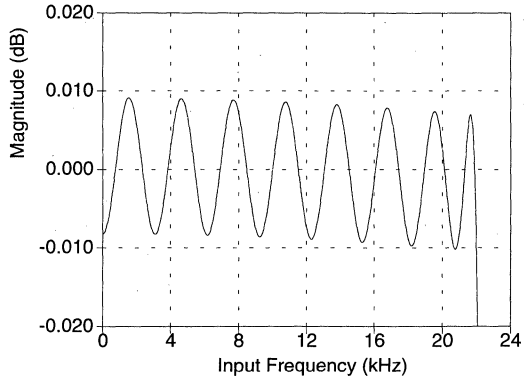


Figure 9. CS5389 Digital Filter Passband Ripple

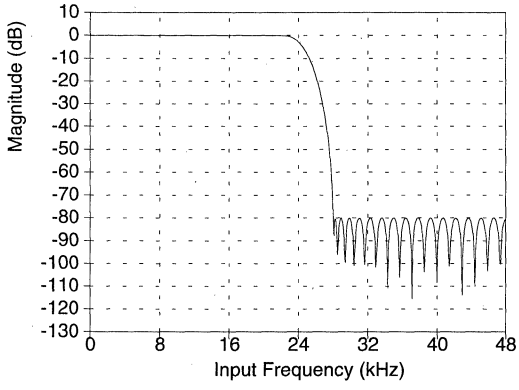


Figure 8. CS5389 Digital Filter Stopband Rejection

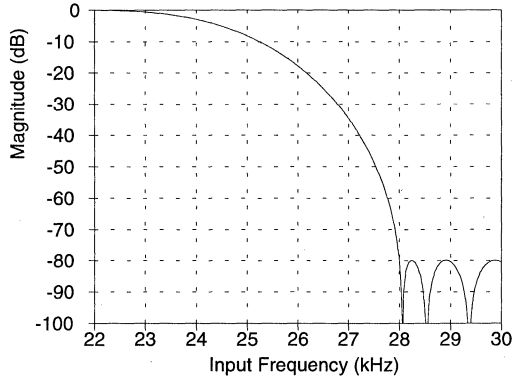


Figure 10. CS5389 Digital Filter Transition Band

Performance Measurements

All the following performance measurements were taken using an Audio Precision System One Dual Domain tester. The CS5389 was in a CDB5389 evaluation board, running at 48 kHz word rate and interfaced to the System One via the AES/EBU input using a CS8402 AES/EBU transmitter.

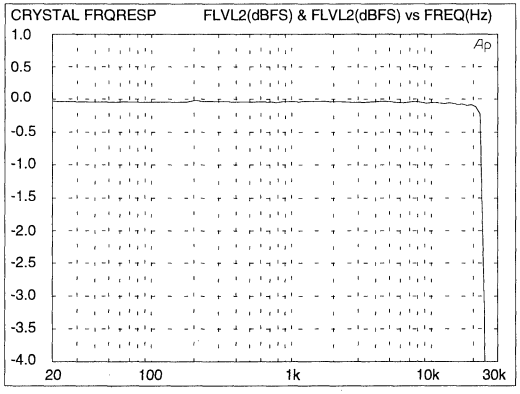


Figure 11. Frequency Response

Figure 11 shows the CS5389 frequency response.

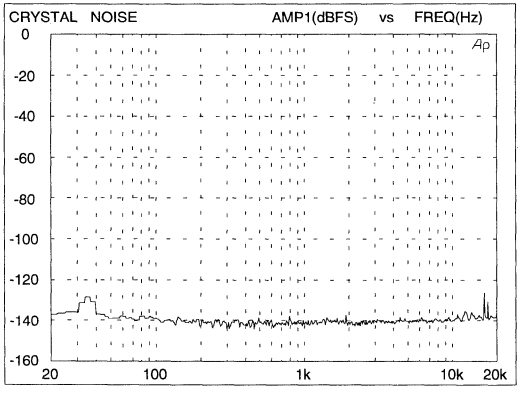


Figure 12. Noise Floor

Figure 12 shows the noise floor with zero input signal level. A 16 K point FFT was used.

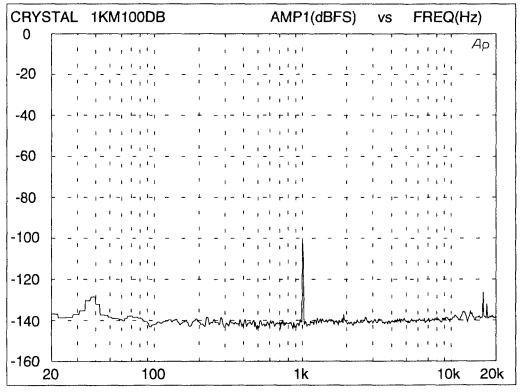


Figure 13. 1 kHz, -100 dB input FFT

Figure 13 shows a 1 kHz, -100 dB input signal FFT plot. Notice the lack of harmonic distortion components. This is a direct result of the perfect differential non-linearity of the delta-sigma architecture

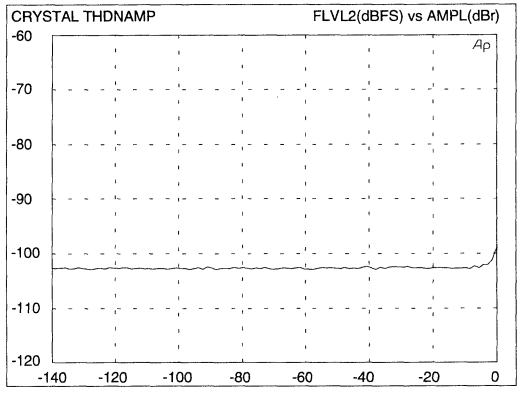


Figure 14. THD+N vs Input level at 1 kHz

Figure 14 shows the THD+N versus input level at 1 kHz. This plot indicates a dynamic range of 104 dB, with a small increase in distortion with a full scale input.

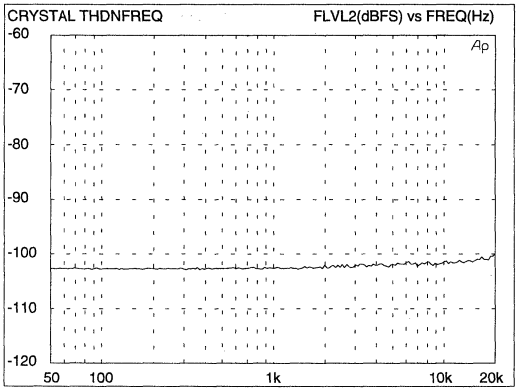


Figure 15. THD+N vs Frequency at -10 dB

Figure 15 shows THD+N versus frequency at -10 dB input. This indicates a value of 101 dB, with minor degradation at high frequency.

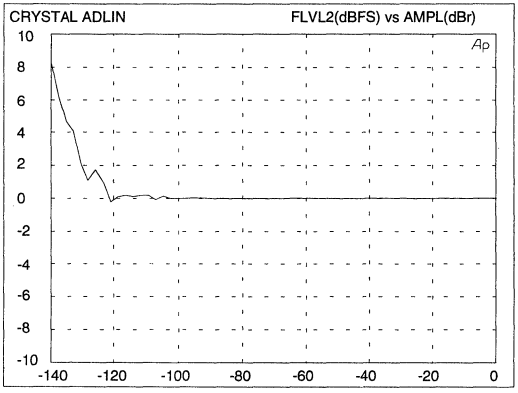


Figure 16. Output level Error vs. Input level at 500 Hz

Figure 16 shows the linearity of the CS5389. The input signal is at 500 Hz and is varied from 0 dB (full scale) to -140 dB. At each input level, the output level is measured and compared to the perfect value. Any deviation is plotted as a deviation away from 0 dB. Notice the close conformance to perfect linearity, until the noise starts to influence the readings at about -120 dB.

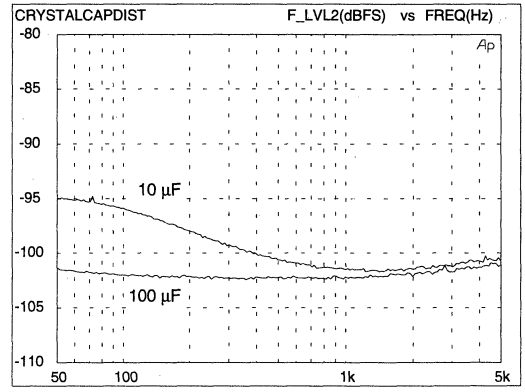
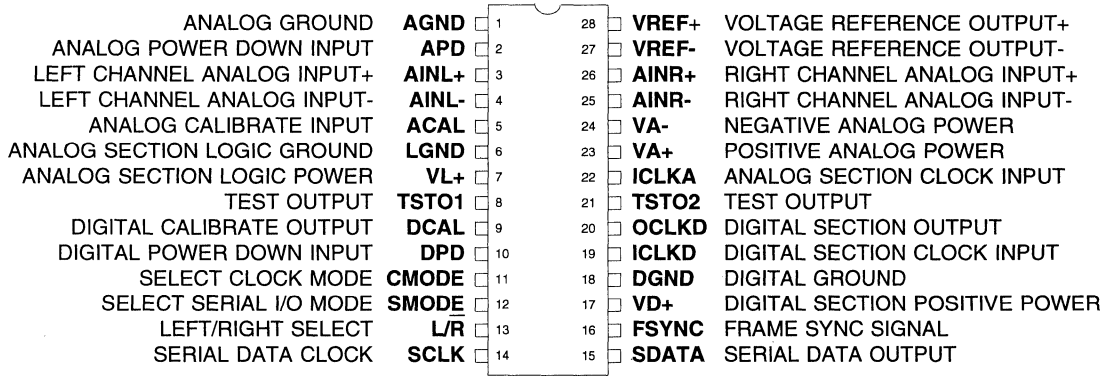


Figure 17. THD+N vs. FREQ at -4 dB 10 µF and 100 µF VREF Decoupling

Figure 17 demonstrates the effects of VREF decoupling at a -4 dB input level.

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 23.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 7.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 24.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 6.
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 17.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 18.
Digital ground for the digital section.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Inputs, PINS 25, 26
Analog input connections for the right channel differential inputs. Nominally 14.72 Vpp (differential) for full scale.

AINL+, AINL- - Differential Left Channel Analog Inputs, PINS 3,4.

Analog input connections for the right channel differential inputs. Nominally 14.72 Vpp (differential) for full scale.

Analog Outputs

VREF-, VREF+ - Voltage Reference Outputs, PINS 27,28.

Nominally +3.68 volts (VREF+) and -3.68 volts (VREF-) volts. Note the negative output polarity on VREF-. See Figure 1 for recommended capacitive decoupling.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 22.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 19.

ICLKD clocks the digital filter and is the source for modulator sampling clock, OCKLD. The required ICLKD frequency is determined by the desired output word rate and the CMODE pin. If CMODE is low, ICLKD is 256 X the desired output word rate. If CMODE is high, ICLKD is 384 X the output word rate. For example, with CMODE low, ICLKD is 12.288 MHz for an output word rate of 48 kHz.

APD - Analog Power Down, PIN 2.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. APD should be connected to AGND if analog power-down is not used.

DPD - Digital Power Down, PIN 10.

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 $L/\overline{R}$ periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 5.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to AGND respectively. Should be connected to DCAL.

CMODE - Clock Mode Select, PIN 11.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 12.

SMODE should be tied high to select the serial interface master mode. SCLK, FSYNC and L/$\overline{R}$ are outputs generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/$\overline{R}$ are all inputs. In slave mode, L/$\overline{R}$, FSYNC and SCLK need to be derived from ICLKD using external dividers.

3

Digital Outputs

SDATA - Serial Data Output, PIN 15.

Audio data bits are presented MSB first, in 2's complement format.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 20.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 14.

Data is clocked out on the falling edge of SCLK.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/$\overline{R}$ changes.

L/$\overline{R}$ - Left/Right Select, PIN 13.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/$\overline{R}$ is high, left channel data is on SDATA, except for the first SCLK cycle. When L/$\overline{R}$ is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/$\overline{R}$ changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. L/$\overline{R}$ frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 16.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the sixteenth SDATA audio data bit .

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/$\overline{R}$ transitions. If it is desired to delay the data bits from the L/$\overline{R}$ edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/$\overline{R}$ edge, independent of the state of FSYNC.

Miscellaneous

TSTO1, TSTO2 - Test Output, PINS 8, 21.

These two pins are bonded out for factory test outputs. They must not be connected to any external component or any length of PC trace.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (rms) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale.

Total Harmonic Distortion plus Noise - The ratio of the rms sum of all spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), excluding signal, to the rms value of the signal.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. (1/2 LSB below AGND). Units in LSBs.

REFERENCES - All, except 1), are reprinted in this data book.

1) "A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

3) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

4) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Semiconductor Corporation

CS5390

20-Bit, Stereo A/D Converter for Digital Audio

Features

- 110 dB Dynamic Range (A-Weighted)
- THD + N better than -100dB
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  >100dB StopBand Attenuation
  0.005dB Passband Ripple
- Low Power Dissipation: 550 mW
  Power-Down Mode
- Pin Compatible with CS5389
- Evaluation Board Available

General Description

The CS5390 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

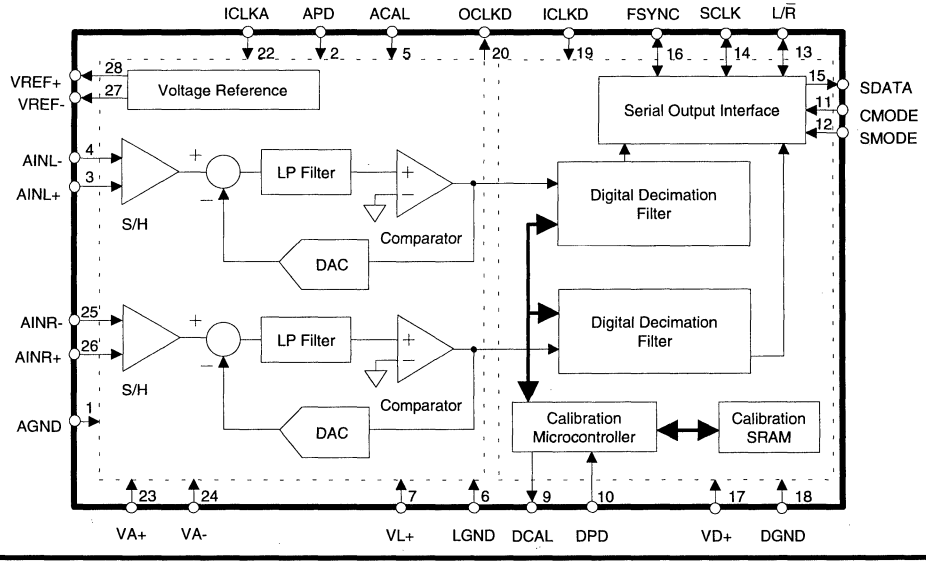
The CS5390 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5390 has a filter passband of dc to 21.7kHz. The filters have linear phase, 0.005 dB passband ripple, and >100 dB stopband rejection.

The CS5390 is targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise. Pin compatibility with the CS5389 allows a simple upgrade path without hardware changes.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS5390-KP	0° to 70°C	28-pin Plastic DIP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VL+,VD+ = 5V; VA- = -5V; Full-scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 39Ω with 6.8 nF across AIN+, AIN-; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD+;

Parameter	Symbol	Min	CS5390-K Typ	Max	Units
Resolution		20	-	-	Bits
Dynamic Performance					
Dynamic Range		TBD	107	-	dB
(A-weighted)		-	110	-	dB
Total Harmonic Distortion + Noise	THD+N				
0 dB		-	-100	-	dB
-20 dB		-	-87	TBD	dB
-60 dB		-	-47	TBD	dB
Interchannel Phase Deviation		-	0.0001	-	°
Interchannel Isolation		106	120	-	dB
dc Accuracy					
Interchannel Gain Mismatch		-	0.05	-	dB
Gain Error		-	±1	±5	%
Gain Drift		-	50	150	ppm/°C
Bipolar Offset Error (After Calibration)		-	±5	±20	LSB
Offset Calibration Range		-	±50	-	mV
Analog Input					
Full-scale Differential Input Voltage (Note 1)	V_{IN}	14.0	14.72	-	Vpp
Input Impedance	Z_{IN}	-	25	-	kΩ
Common-Mode Rejection	CMRR	-	115	-	dB
Power Supplies					
Power Supply Current (VA+)+(VL+)	I_{A+}	-	37.5	55	mA
with APD, DPD low VA-	I_{A-}	-	37.5	55	mA
(Normal Operation) VD+	I_{D+}	-	35.0	TBD	mA
Power Supply Current (VA+)+(VL+)	I_{A+}	-	100	-	µA
with APD, DPD high VA-	I_{A-}	-	100	-	µA
(Power-Down Mode) VD+	I_{D+}	-	100	-	µA
Power Consumption (APD, DPD Low)	PDN	-	550	TBD	mW
(APD, DPD High)	PDS	-	1.5	-	mW
Power Supply (dc to 29 kHz)	PSRR	-	65	-	dB
Rejection Ratio (29 kHz to 3.046 MHz)		-	90	-	dB

Notes: 1. Specified for a fully differential input ±{(AINR+)-(AINR-)}.The ADC accepts input voltages up to the analog supplies (VA+, VA-). Full-scale outputs will be produced for differential inputs beyond V_{IN}. This value is subject to the gain error tolerance specification

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%; Output word rate of 48 kHz)

Parameter	Symbol	Min	Typ	Max	Units
Passband (-0.005 dB)		0	-	21.7	kHz
Passband Ripple		-	-	±0.005	dB
Stopband		29	-	3043	kHz
Stopband Attenuation (Note 2)		100		-	dB
Group Delay (OWR = Output Word Rate)	t_{gd}	-	18/OWR	-	s
Group Delay Variation vs Frequency	Δt_{gd}	-	-	0.0	µs

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are (n x 3.072MHz) ±21.7kHz, where n = 0,1,2,3...

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30%VD+	V
High-Level Output Voltage at I_O = -20 µA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at I_O = 20 µA	V_{OL}	-	-	0.1	V
Input Leakage Current	I_{in}	-	1.0	-	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Negative Analog	VA-	+0.3	-	-6.0	V
	Positive Logic	VL+	-0.3	-	+6.0	V
	Positive Digital	VD+	-0.3	-	+6.0	V
	|VA+ - VD+|		-	-	0.4	V
	|VA+ - VL+|		-	-	0.4	V
	|VD+ - VL+|		-	-	0.4	V
Input Current	Any Pin Except Supplies	I_{in}	-	-	±10	mA
Peak Analog Input Voltage (AINL+/- and AINR +/- pins)		V_{IN}	(VA-)-0.4	-	(VA+)+0.4	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

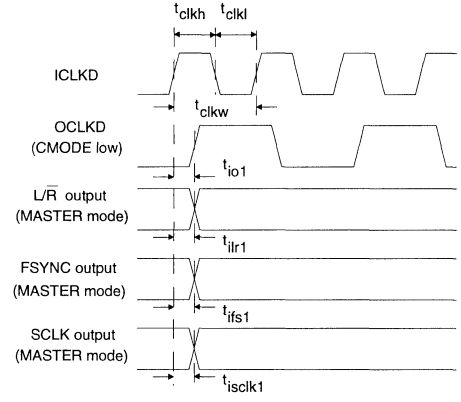
WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

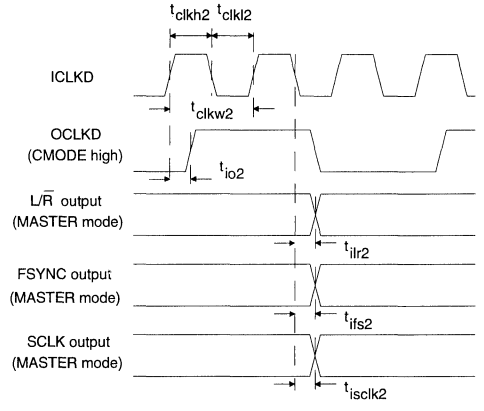
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t_{clkw1}	78	-	390.6	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	260.4	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK falling to SDATA valid (MASTER mode)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK falling to L/$\overline{R}$ (MASTER mode)	t_{mslr}	-20	-	20	ns
SCLK falling to FSYNC (MASTER mode)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid (SLAVE mode)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Rising SCLK to L/$\overline{R}$ edge delay (SLAVE mode)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to rising SCLK setup time (SLAVE mode)	t_{slr2}	30	-	-	ns
Rising SCLK to rising FSYNC delay (SLAVE mode)	t_{sfs1}	30	-	-	ns
Rising FSYNC to rising SCLK setup time (SLAVE mode)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	2 x t_{clkw}	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}		4096		1/OWR

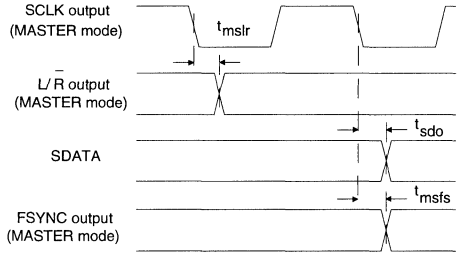
Notes: 3. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).



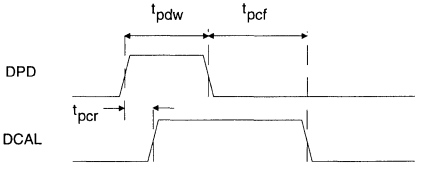
ICLKD to Outputs Propagation Delays (CMODE low)



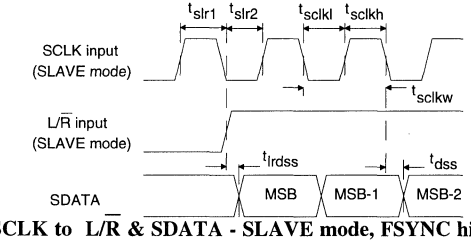
ICLKD to Outputs Propagation Delays (CMODE high)



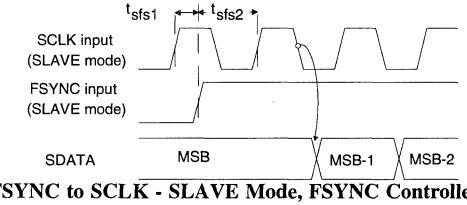
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	|VA+ - VD+|	-	-	-	0.4	V

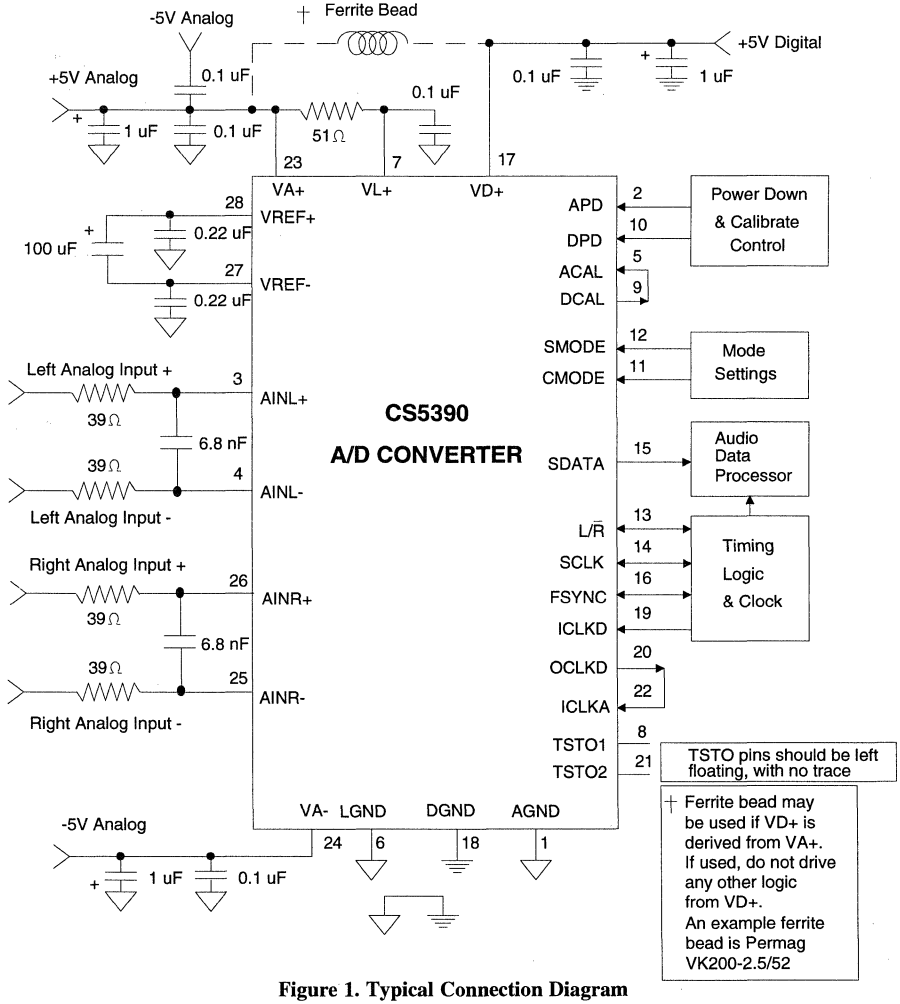


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5390 is a 20-bit, stereo A/D converter designed specifically for stereo digital audio applications. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 20-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and it does not require external sample-and-hold amplifiers or voltage references.

On-chip voltage references provide for a differential input signal range of 14.72 Vpp. Any offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 20-bit numbers. Typical power consumption of only 550 mW can be further reduced by use of the power-down mode.

The CS5390 is pin compatible with the CS5389, and it offers wider dynamic range and twenty bit resolution. The pin compatibility of the CS5390 provides a simple upgrade path to systems currently using the CS5389.

For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter and is used to generate the modulator sampling clock. The required ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the ICLKD frequency to 384 X OWR, while CMODE low will set the ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when CMODE is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface

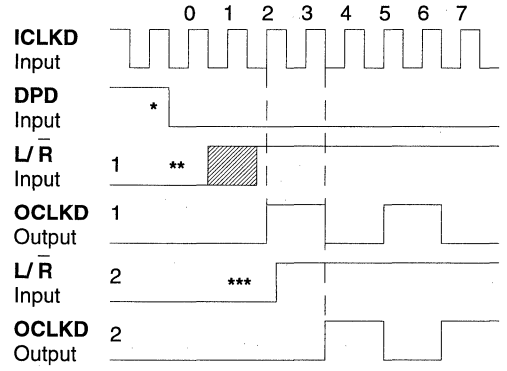


Figure 2. ICLKD to OCLKD Timing with CMODE high (384XOWR)

MASTER mode and SLAVE mode are the 2 primary modes of operation for the serial data output interface.

Master Mode

SCLK, L/$\overline{R}$ and FSYNC are outputs derived from ICLKD in Master mode, Figure 3. Notice the one SCLK cycle delay between L/$\overline{R}$ edges, SDATA and FSYNC. FSYNC brackets the 16 most significant data bits.

Slave Mode

L/$\overline{R}$, FSYNC and SCLK become inputs in SLAVE mode. L/$\overline{R}$ must be externally derived from ICLKD and be equal to the Output Word Rate. SCLK should be equal to 64 X OWR though other frequencies are possible but may degrade system performance due to interference effects. FSYNC may be high or used to control SDATA. With FSYNC high, data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The falling edge of SCLK causes the ADC to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge, as shown in Figure 4.

SCLK is ignored with FSYNC low and only the MSB is clocked out after the L/$\overline{R}$ edge in SLAVE mode / FSYNC controlled as shown in Figure 5. Bringing FSYNC high will enable SCLK to clock data out. This feature is particularly useful to multiplex multiple channels.

Certain serial modes align well with various interface requirements. A CS5390 in MASTER mode, with an inverted L/$\overline{R}$ signal, generates I^2S (Philips) compatible timing. A CS5390 (with an inverted SCLK) in SLAVE mode emulates a CS5326 style interface and also links to a DSP56000 in network mode.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 7.36 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 14.72 Vpp. Figure 6 shows the input signal levels for full scale.

The analog modulator samples the input at 3.072 MHz (64 x Fs) for an output word rate of 48 kHz. The digital filter will reject signals between 21.7 kHz and 3.072 MHz - 21.7 kHz. However, there is no rejection for input signals which are (n x 3.072 MHz) +/- 21.7 kHz, where n = 0,1,2,... A 39 Ω resistor in series with the analog input and a 6.8 nF NPO or COG capacitor between the inputs will attenuate any noise energy

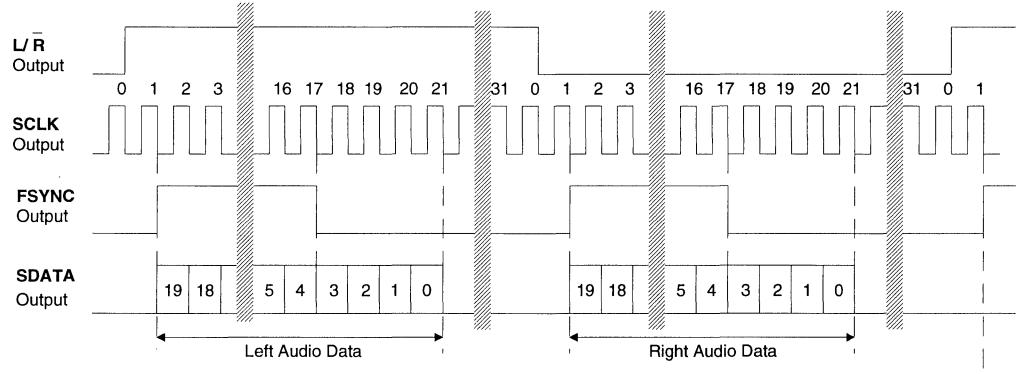


Figure 3. Data Output Timing - MASTER mode

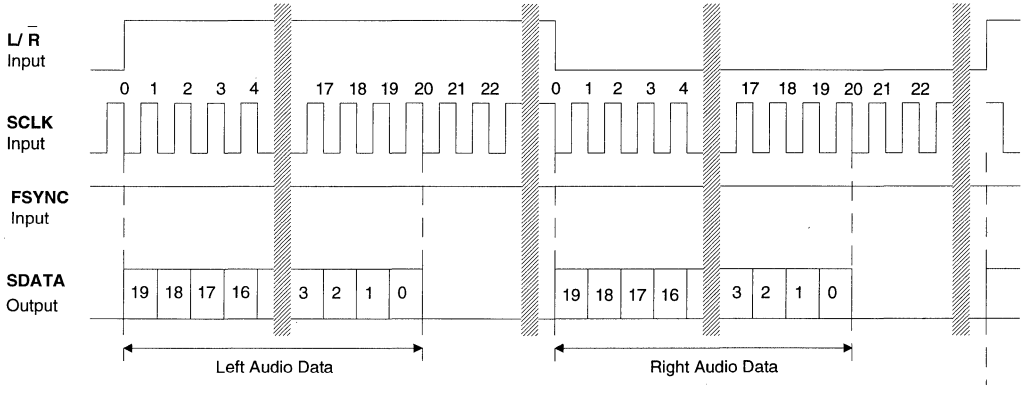
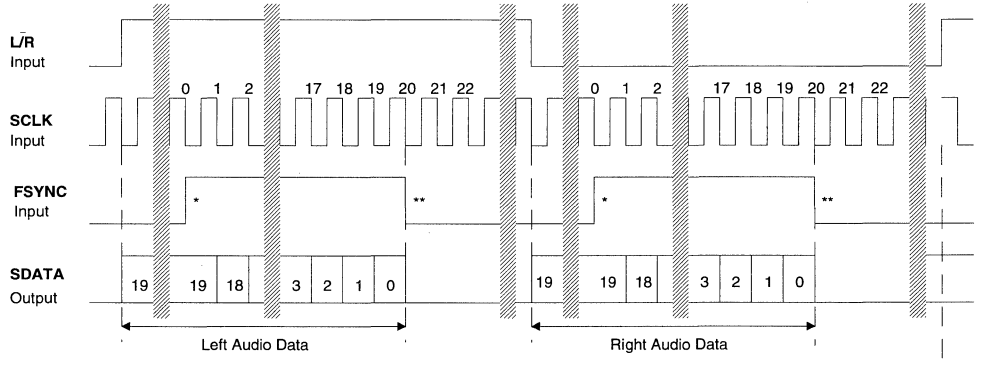


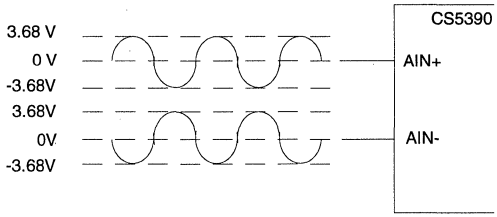
Figure 4. Data Output Timing - SLAVE Mode, FSYNC high



* Rising FSYNC enables SCLK to clock out SDATA

** Falling FSYNC stops SCLK from clocking out SDATA

Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled



Full Scale Input level= (AIN+) - (AIN-)= 14.72 Vpp

Figure 6. Full Scale Input Voltage

at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage references are available at the VREF+ and VREF- pins for the purpose of decoupling only. The circuit traces attached to these pins must be minimal in length and no load current may be taken from VREF+ or VREF-. The recommended decoupling scheme, Figure 1, is a 100 µF electrolytic capacitor across VREF+ and VREF- and two 0.22 µF ceramic capacitors connected from VREF+ to GND and VREF- to GND.

Power-Down and Offset Calibration

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode wherein typical power consumption drops to 1.5 mW.

Bringing DPD low exits power-down and initiates an offset calibration cycle. During the calibration cycle, the digital section measures the offset of each channel and stores a corresponding value in the calibration registers. This value is subtracted from future conversions to produce an offset free conversion. The calibration inputs are obtained from the analog input pins (ACAL low) or AGND (ACAL high).

The offsets generated by the input circuitry are included when calibration is performed using the analog input pins (ACAL low). DCAL should be used to control a multiplexer which grounds the user's front-end in this mode. The DCAL output will remain high for 4096 L/$\overline{R}$ clock cycles during calibration as shown in Figure 7.

A delay of approximately 50 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-

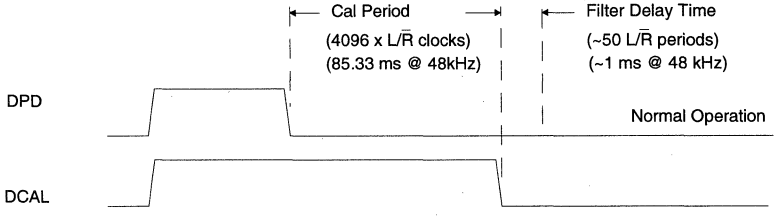


Figure 7. Initial Calibration Cycle Timing

down mode. The voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF+ and VREF- pins. A time delay of approximately 10 ms/µF is required between APD going low and DPD going low to allow for VREF settling. The typical connection diagram of Figure 1 requires a 1 second delay.

APD should be tied to AGND if the analog power down feature is not required. When using the analog power down feature, DPD and APD may be tied together if the capacitor across VREF+ and VREF- is not greater than 10 µF.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean ± 5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF+ and VREF- pins in order to avoid unwanted coupling into the modulators. The VREF+ and VREF- decoupling capacitors, particularly the 0.22 µF, must be positioned to minimize the electrical path from VREF+ and VREF- to Pin 1, AGND. The CDB5390 evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Additional printed circuit board design and circuit design hints are included in the application note, "Layout and Design Rules for Data Converters" and the Audio Engineering Society paper "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" which are included in the Crystal Semiconductor data book application section.

Synchronization of Multiple CS5390

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD pins to a single control signal and supplying the same ICLKD and L/$\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5390 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD pins to the same control signal and insuring that the DPD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

Digital Filter

Figures 8 - 10 show the performance of the digital filter included in the ADC. All plots are normalized to the output word rate, Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with the output word rate.

Stopband rejection, figure 8, is greater than 100 dB. Figure 9 shows the passband ripple of ± 0.005 dB maximum. Figure 10 is an expanded view of the transition band.

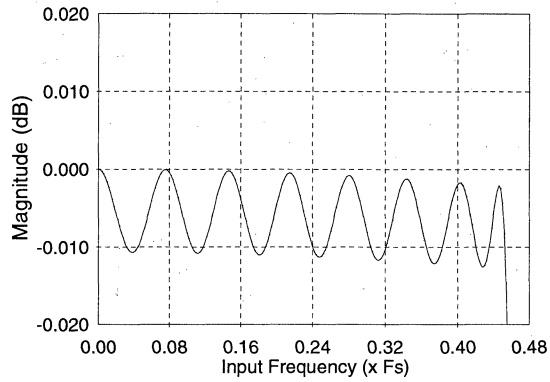


Figure 9. CS5390 Digital Filter Passband Ripple

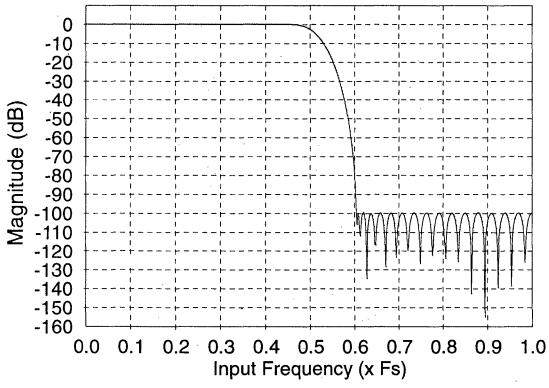


Figure 8. CS5390 Digital Filter Stopband Rejection

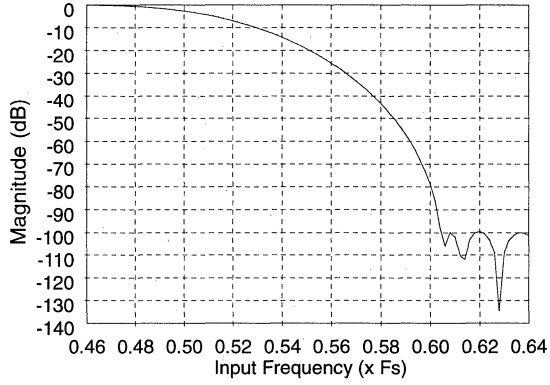
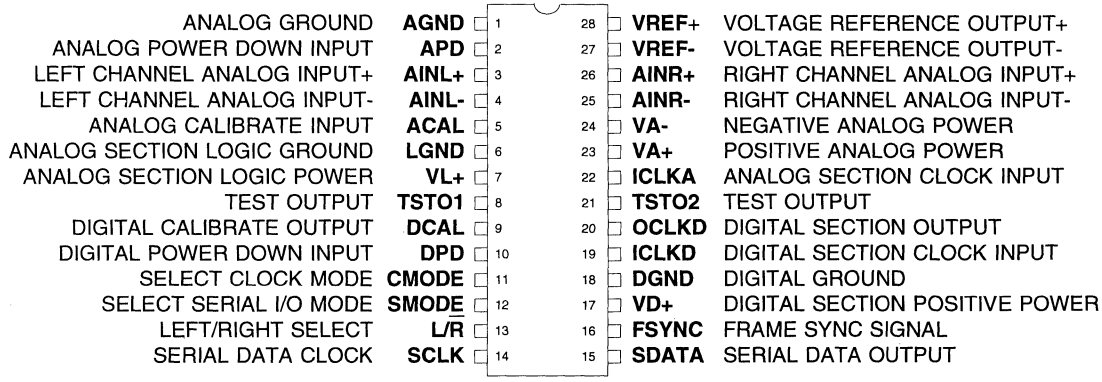


Figure 10. CS5390 Digital Filter Transition Band

PIN DESCRIPTIONS



3

Power Supply Connections

VA+ - Positive Analog Power, PIN 23.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 7.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 24.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 6.
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 17.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 18.
Digital ground for the digital section.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Inputs, PINS 25, 26.
Analog input connections for the right channel differential inputs. Nominally 14.72 Vpp (differential) full scale.

AINL+, AINL- - Differential Left Channel Analog Inputs, PINS 3,4.

Analog input connections for the right channel differential inputs. Nominally 14.72 Vpp (differential) full scale.

Analog Outputs

VREF-, VREF+ - Voltage Reference Outputs, PINS 27,28.

Nominally +3.68 volts (VREF+) and -3.68 volts (VREF-) volts. Note the negative output polarity on VREF-. See Figure 1 for recommended capacitive decoupling.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 22.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 19.

ICLKD clocks the digital filter and is the source for modulator sampling clock, OCKLD. The required ICLKD frequency is determined by the desired output word rate and the CMODE pin. If CMODE is low, ICLKD is 256 X the desired output word rate. If CMODE is high, ICLKD is 384 X the output word rate. For example, with CMODE low, ICLKD is 12.288 MHz for an output word rate of 48 kHz.

APD - Analog Power Down, PIN 2.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. APD should be connected to AGND if analog power-down is not used.

DPD - Digital Power Down, PIN 10.

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 $L/\overline{R}$ periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 5.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to AGND respectively. Should be connected to DCAL.

CMODE - Clock Mode Select, PIN 11.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 12.

SMODE should be tied high to select the serial interface master mode. SCLK, FSYNC and L/$\overline{R}$ are outputs generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/$\overline{R}$ are all inputs. In slave mode, L/$\overline{R}$, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

SDATA - Serial Data Output, PIN 15.

Audio data bits are presented MSB first, in 2's complement format.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 20.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 14.

Data is clocked out on the falling edge of SCLK.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/$\overline{R}$ changes.

L/$\overline{R}$ - Left/Right Select, PIN 13.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/$\overline{R}$ is high, left channel data is on SDATA, except for the first SCLK cycle. When L/$\overline{R}$ is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/$\overline{R}$ changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. L/$\overline{R}$ frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 16.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the sixteenth SDATA audio data bit .

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/$\overline{R}$ transitions. If it is desired to delay the data bits from the L/$\overline{R}$ edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/$\overline{R}$ edge, independent of the state of FSYNC.

Miscellaneous

TSTO1, TSTO2 - Test Output, PINS 8, 21.

These two pins are bonded out for factory test outputs. They must not be connected to any external component or any length of PC trace.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (rms) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Total Harmonic Distortion plus Noise - The ratio of the rms sum of all spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), excluding signal, to the rms value of the signal.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. (1/2 LSB below AGND). Units in LSBs.

REFERENCES - All, except 1), are reprinted in this data book.

1) "A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

3) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

4) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

5) " 18-Bit Stereo D/A Converter with Integrated Digital and Analog Filters" by Nav Sooch ,Jeffery W. Scott, T. Tanaka, T. Sugimoto and C. Kubomura. Presented at the 91st Convention of the Audio Engineering Society, October 1991.

6) " An 18-Bit Delta-Sigma D/A Processor System Achieving Full-Scale THD+N>100dB" by Steven R. Green, Steven Harris and Brent Wilson. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

7) " How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

Semiconductor Corporation

Evaluation Board for CS5389 / CS5390

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, S/PDIF & EIAJ CP-340 Compatible Digital Audio
- Buffered Serial Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

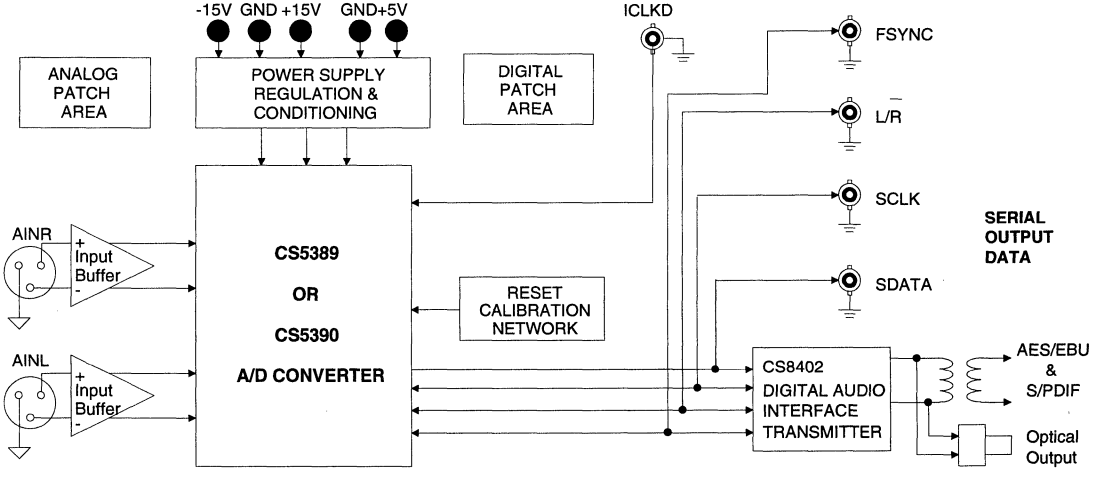
General Description

The CDB5389/CDB5390 evaluation board allows fast evaluation of the CS5389 18-bit or CS5390 20-bit, stereo A/D converter. The board generates all converter timing signals and provides a serial output interface. Evaluation requires a digital signal processor, a low-distortion signal source and a power supply.

Also included is a CS8402 digital audio interface transmitter which generates AES/EBU, S/PDIF & EIAJ CP-340 compatible audio data. The digital audio data is available via XLR, RCA phono and optical connectors

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION: **CDB5389**
CDB5390



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

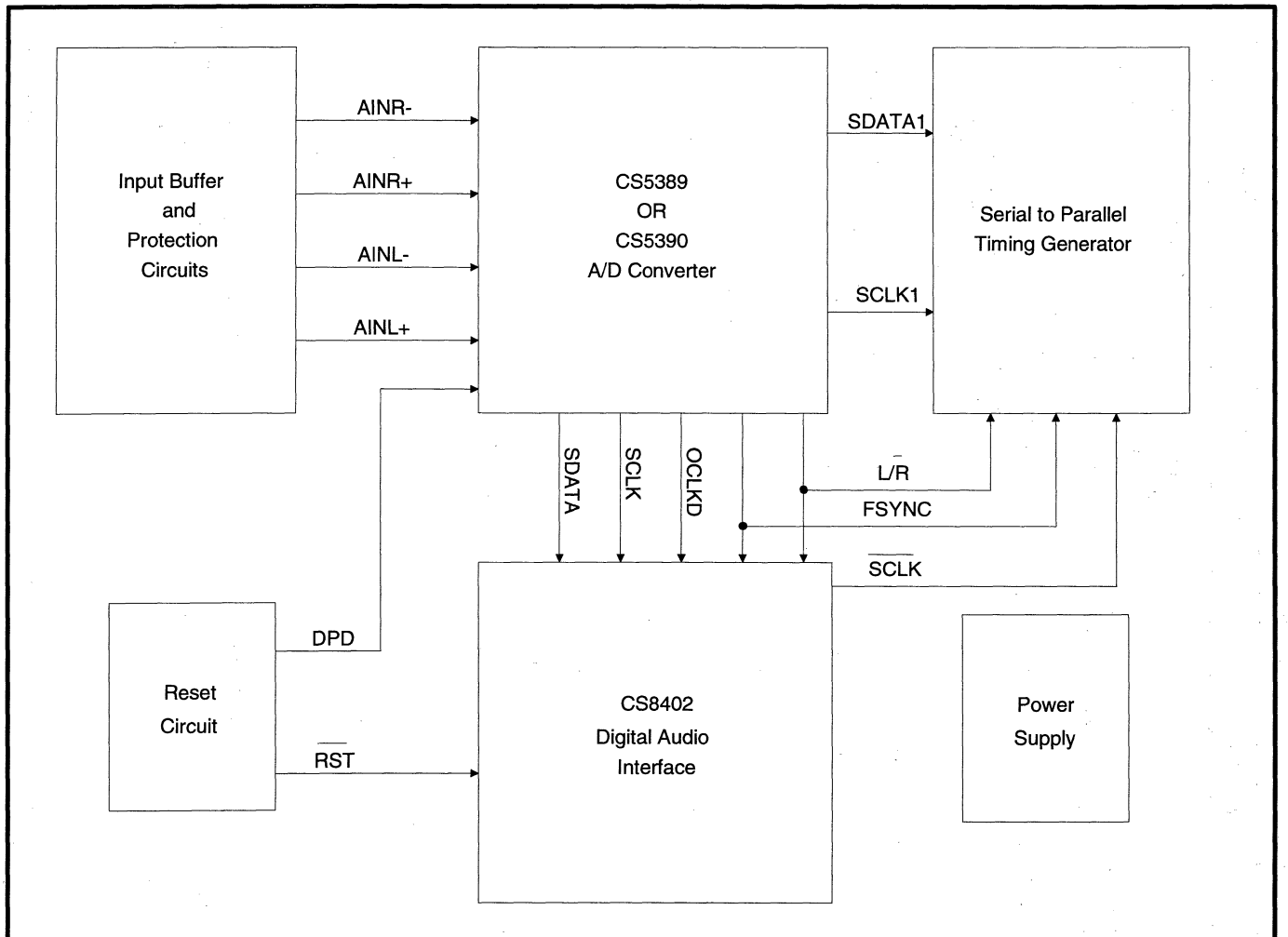


Figure 1. CDB5389/CDB5390 Overview

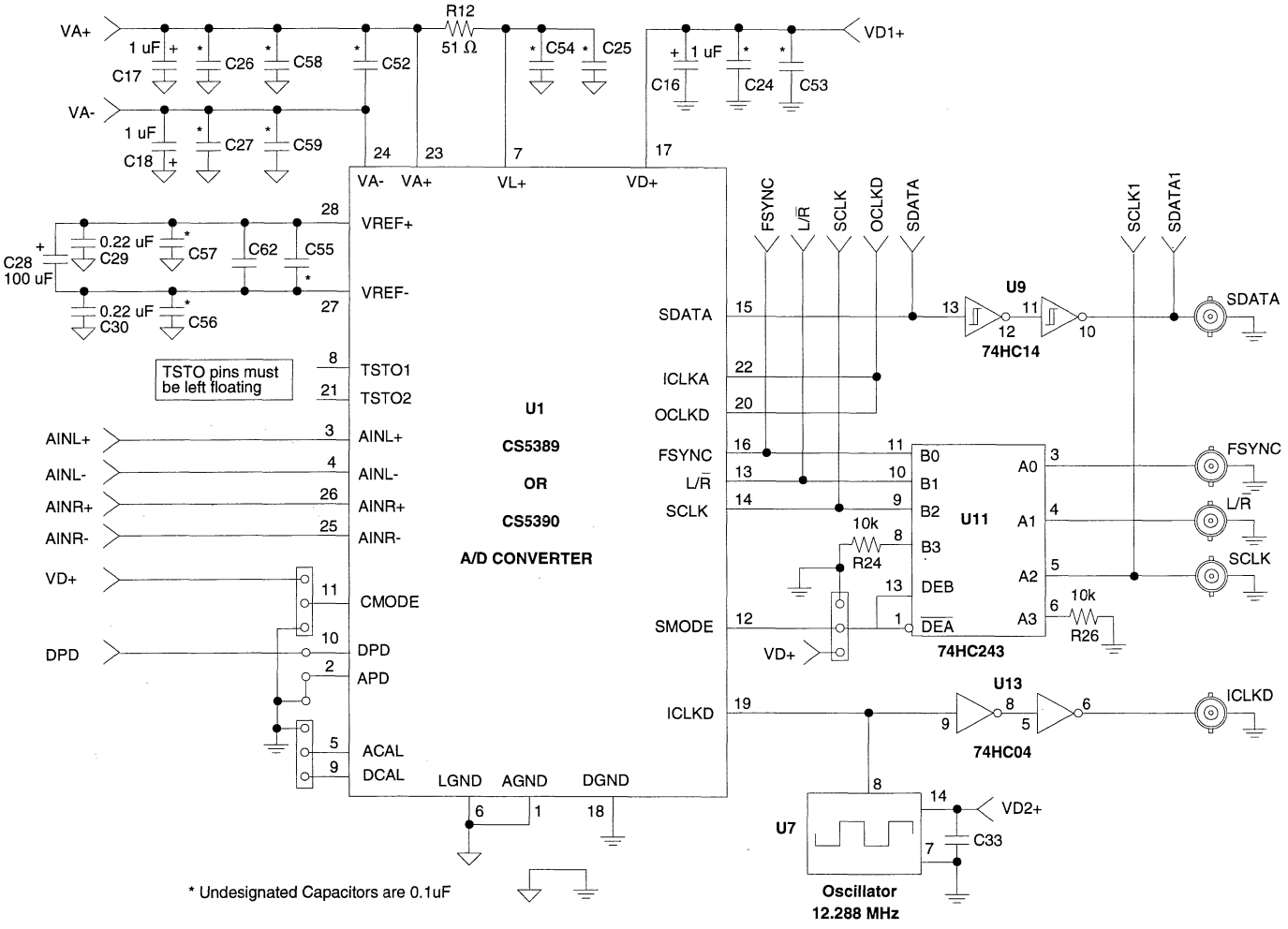


Figure 2. CS5389/CS5390 Connections

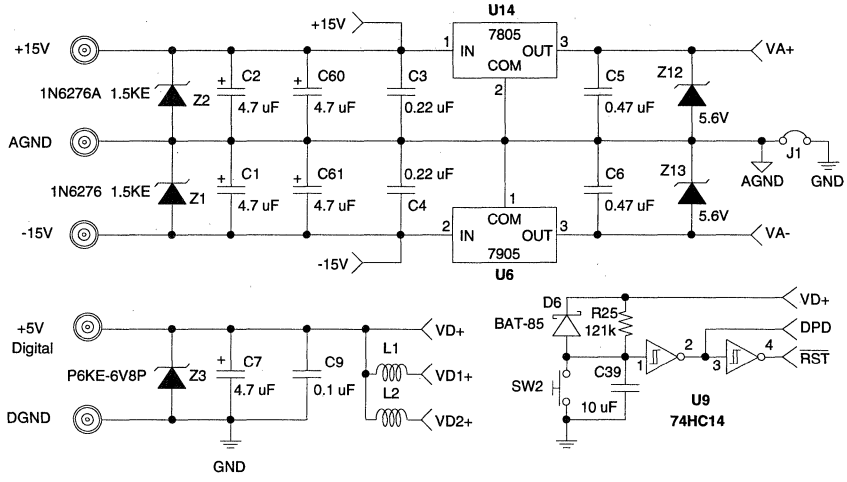


Figure 3. Power Supply and Reset Circuitry

Power Supply Circuitry and Grounding

Power is supplied to the evaluation board by five binding posts as shown in Figure 3. The ±5 Volt analog power supplies for the converter are derived from the ±15 Volt supplies using the voltage regulators U6 and U14. C1-C6 provide general power supply filtering for the analog supply. C60 and C61 are included to prevent signal coupling between the left and right analog input circuits. Z12 and Z13 are related to the CS5389 input protection circuits.

The +5 Volt digital supply for the converter and discrete logic is provided by the +5V and DGND binding posts. Z1, Z2, and Z4 are transient suppressers which also provide protection from incorrectly connected power sources

Localized decoupling for the CS5389/CS5390 VA+ and VA- pins is provided by C17, C18, C26, C27, C58, C59 and C52 as shown in Figure 2. Note that C52 is connected between VA- and VA+. R12, C54 and C25 provide a low-pass filter for the analog logic power supply pin, VL+.

The evaluation board uses separate analog and digital ground planes which are connected by J1. This arrangement isolates the digital logic from the analog circuitry.

Reset Circuit & Offset Calibration

The reset circuit provided on the evaluation board is shown in Figure 3. Upon power-up, this circuit provides RST for the CS8402 and a pulse to the CS5389/CS5390 DPD pin initiating an offset calibration cycle. Reset and offset calibration can also be initiated by pressing SW2.

The ACAL jumper selects the source used for offset calibration. In the "DCAL" position, the the differential inputs of the CS5389/CS5390 are disconnected from the AINL+/- and AINR+/- input pins and internally connected to AGND. In the "GND" position, the AINL+/- and AINR+/- input pins remain connected to the input pins and the offsets present at the inputs are included in the calibration.

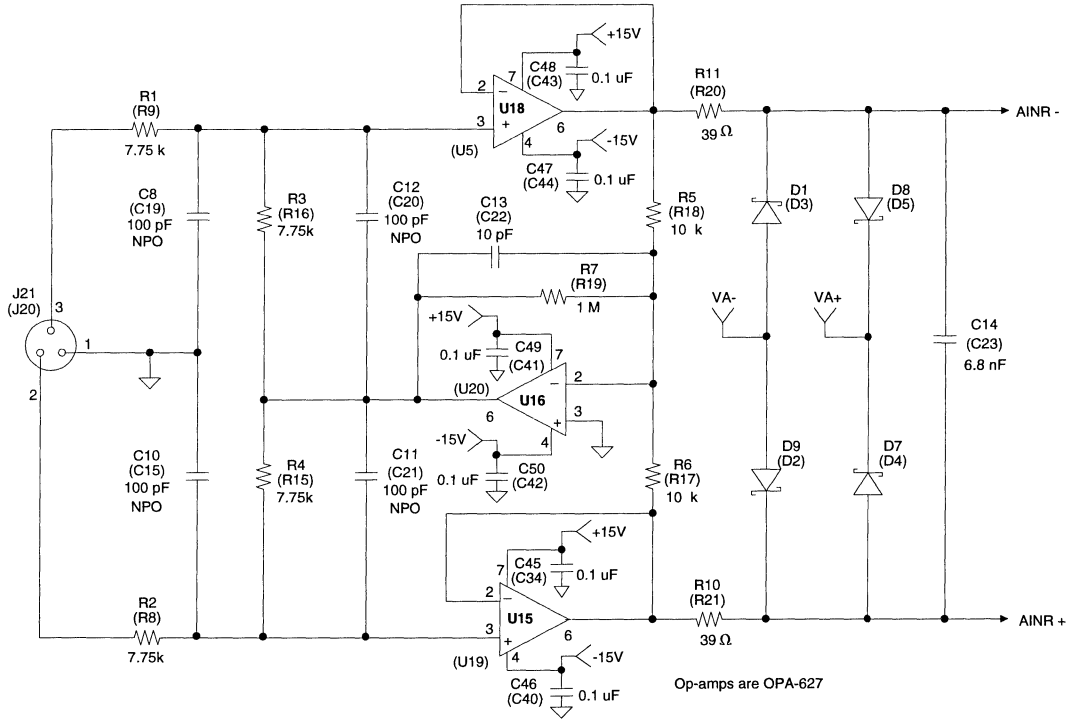


Figure 4. Right Channel Input Buffer and Protection Circuit (Left Channel Designators in Parenthesis)

Input Buffer and Protection Circuits

The differential input circuit of Figure 4 is an ideal match for the CS5389/CS5390 and professional audio applications. The circuit will accept a differential or single-ended signal of either polarity and provide a differential signal to the CS5389/CS5390. The circuit also incorporates the 6 dB of attenuation required to scale professional audio levels to the input voltage range of the CS5389/CS5390. A nominal input level of 20 dBV to the evaluation board will achieve fullscale digital code from the CS5389/CS5390. The common-mode rejection of the system is limited by the passive component matching of the input buffer circuit. The analog input connector is a standard female XLR with Pin 2 positive, Pin 3 return and Pin 1 shield.

The RC network comprised of R10-R11 and C14 provide anti-alias filtering and the optimum source impedance for the CS5389/CS5390 right channel inputs. R20-R21 and C23 duplicate this function for the left channel. Details of the input protection circuit comprised of D1-D5, D7-D9

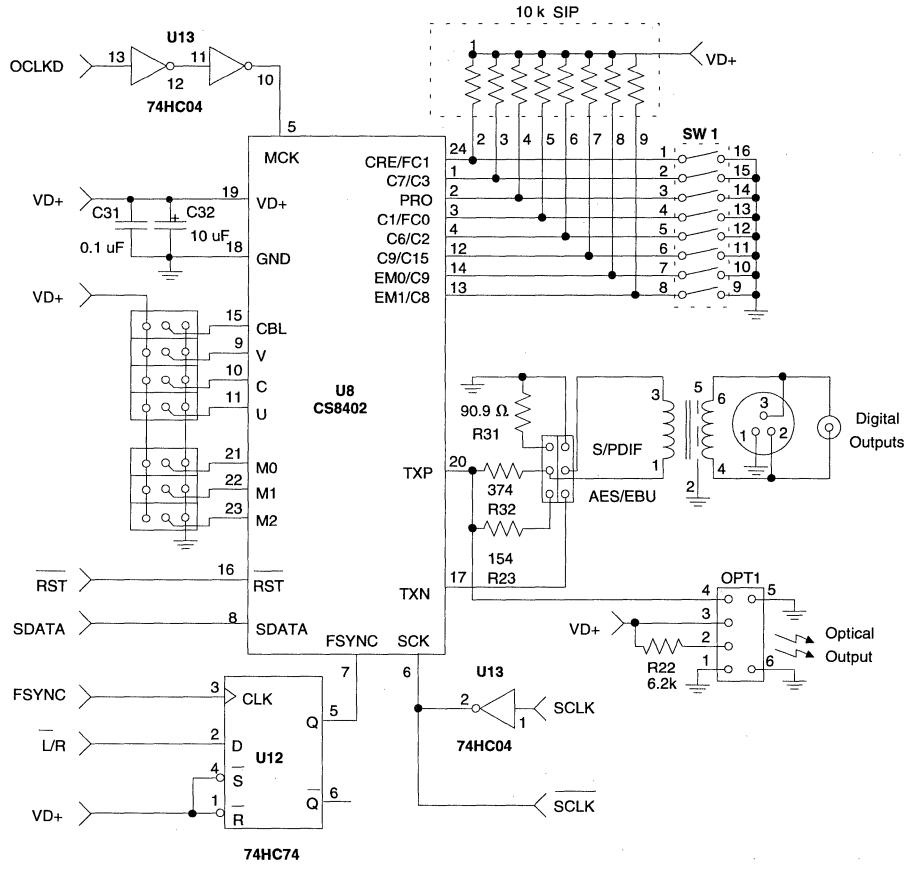


Figure 5. CS8402 Digital Audio Interface

and Z12-Z13 from Figure 3 can be found in the applications note "ADC Input Buffer and Protection Techniques" in the Crystal Semiconductor Vol I data book.

CS8402 Digital Audio Interface

Figure 5 shows the CS8402 circuitry which implements AES/EBU, S/PDIF and EIAJ CP-340 digital audio interface standards. Jumpers are included to allow hardware configuration for either AES/EBU or S/PDIF (and CP-340) modes. The input data formats listed in Table 4 can be selected with M0-M2. SW1 provides 8 DIP switches to select various modes and bits for the CS8402. The C, U and V bits are configured to allow easy access from external logic. See the CS8401 / CS8402 data sheet for detailed information on the operation of the CS8402 and the digital audio standards.

Serial Output Interface

A serial output interface is provided by the ICKLD, SDATA, SCLK, FSYNC and L/$\overline{R}$ BNC

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15V	input	+15 Volts from analog power source
-15V	input	-15 Volts from analog power source
AGND	input	analog ground connection from power source
+5V	input	+5 Volts digital source
DGND	input	digital ground connections from power source
AINL	input	left channel differential / single-ended analog input
AINR	input	right channel differential / single-ended analog input
ICLKD	output	master clock output
$\overline{L}$/R	output/input	left/right channel signal
SDATA	output	serial output data
SCLK	output/input	serial output clock
FSYNC	output/input	data framing signal
DIGITAL OUTPUTS	output	CS8402 digital output via transformer
OPTICAL OUTPUT	output	CS8402 digital output via optical
J23	output	serial timing generator outputs

Table 1. Systems Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
ACAL	selects signal offset or shorted inputs for calibration	GND *DCAL	offset cal to signal input offset cal to shorted inputs
CMODE	selects master clock to sample rate ratio for CS5389	384 *256	384 x sample rate 256 x sample rate
SMODE	selects master/slave operation for CS5389 and I/O status of transceiver U11	*MASTER SLAVE	Timing generation onboard External clock generation
V	CS8402 Validity Bit	High *Low	
C	CS8402 Channel Status Bit	High *Low	
CBL	CS8902 Channel StatusBlock	No Jumper	This pin is an output and is not jumpered
U	CS8402 User Bit	High *Low	
AES/EBU S/PDIF	Hardware configuration for digital audio outputs	*AES/EBU S/PDIF	
J8	Channel selection for serial to parallel conversion	*R L Both	
M0	Selects data format for CS8402	*High Low	
M1	Selects data format for CS8402	High *Low	
M2	Selects data format for CS8402	High *Low	

*Default setting from factory

Table 2. Jumper Selectable Options

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=0	Professional Mode C0=1(default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated
2,5	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	$\overline{C1}$	C1 - Audio
default	1 0	0 - Normal Audio 1 - Non-Audio
6	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8,7	EM1, EM0	C2,C3,C4 - Emphasis (2 of 3 bits)
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 µs 111 - CCITT J.17

Table 3. Switch Definitions - Professional Mode (Factory Setting)

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}$=1	Consumer Mode C0=0
1,4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency
	0 0 0 1 1 0 1 1	0000 - 44.1 kHz 0100 - 48 kHz 1100 - 32 kHz 0000 - 44.1 kHz, CD Mode
2	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1 0	000 - None 100 - 50/15 µs
5	$\overline{C2}$	C2 - Copy/Copyright
	1 0	0 - Copy Inhibited/Copyright Asserted 1 - Copy Permitted/Copyright Not Asserted
6	$\overline{C15}$	C15 - Generation Status
	1 0	0 - Definition is based on category code. 1 - See CS8402 Data Sheet, App. A
8,7	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
	1 1 1 0 0 1 0 0	0000000 - General 0100000 - PCM encoder/decoder 1000000 - Compact Disk - CD 1100000 - Digital Audio Tape - DAT

Table 4. Switch Definitions - Consumer Mode

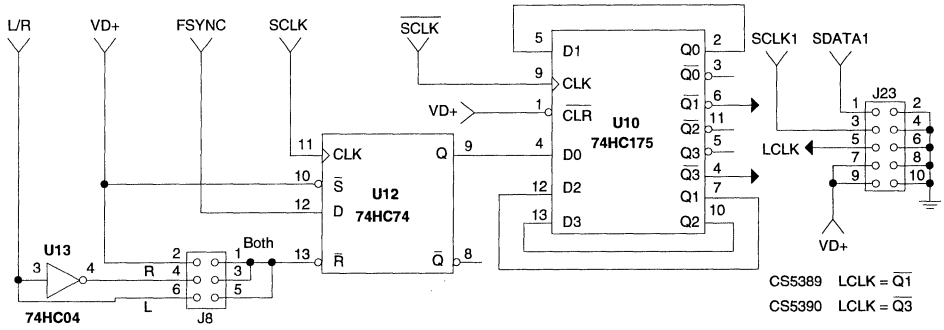


Figure 6. Serial to Parallel Timing Generator

connectors. These outputs are buffered, as shown in Figure 2, in order to isolate the converter from external circuitry. The SMODE jumper not only selects the Master or Slave mode for the CS5389/CS5390 but also controls the direction of the 74HC243 transceiver, U11.

Serial to Parallel Conversion

Serial to parallel conversion can be implemented with the timing generator of Figure 6 and the user supplied circuit shown in Figure 7. Each bit of serial data is clocked out of the CS5389/CS5390 and shifted into the 24-bit shift register formed by U11, U12 and U13 on the falling edge of SCLK. After all data bits for the selected channel have been shifted into U11, U12 and U13 the data is latched onto P3 by the rising edge of LCLK. The 74HC175 shift register delays the falling edge of FSYNC to provide an appropriate LCLK

J8, Figure 6, selects the channel whose output data will be converted to parallel form and presented on P3. With J8 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the falling edge of LCLK is used to clock the parallel data into the digital signal processor. LCLK may be jumpered from P1 to the "X" position of P3. Alternatively, a handshake protocol implemented with DACK and $\overline{\text{DRDY}}$ may be used to transfer data to the signal processor. The fall of $\overline{\text{DRDY}}$ informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that $\overline{\text{DRDY}}$ will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.

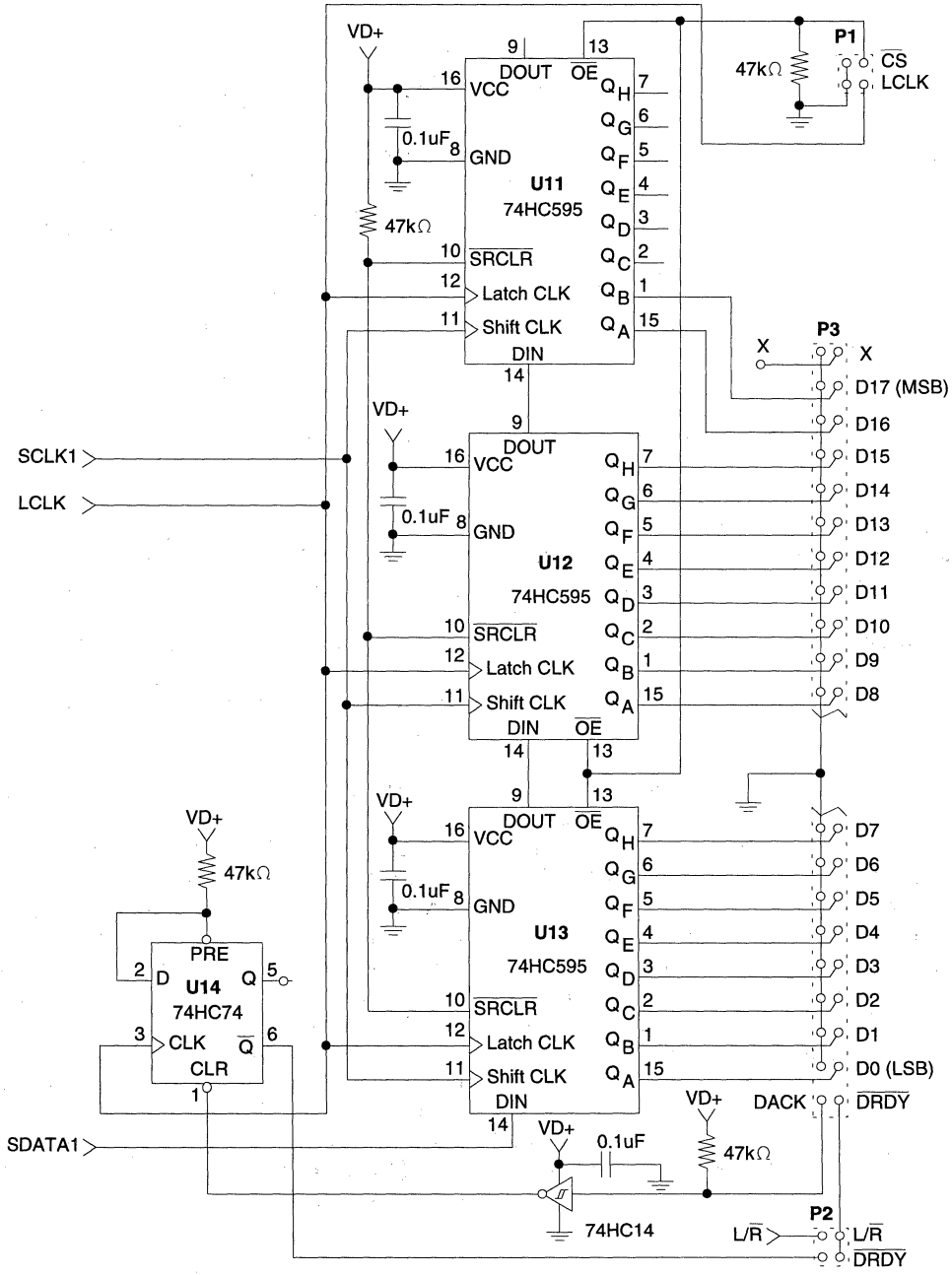
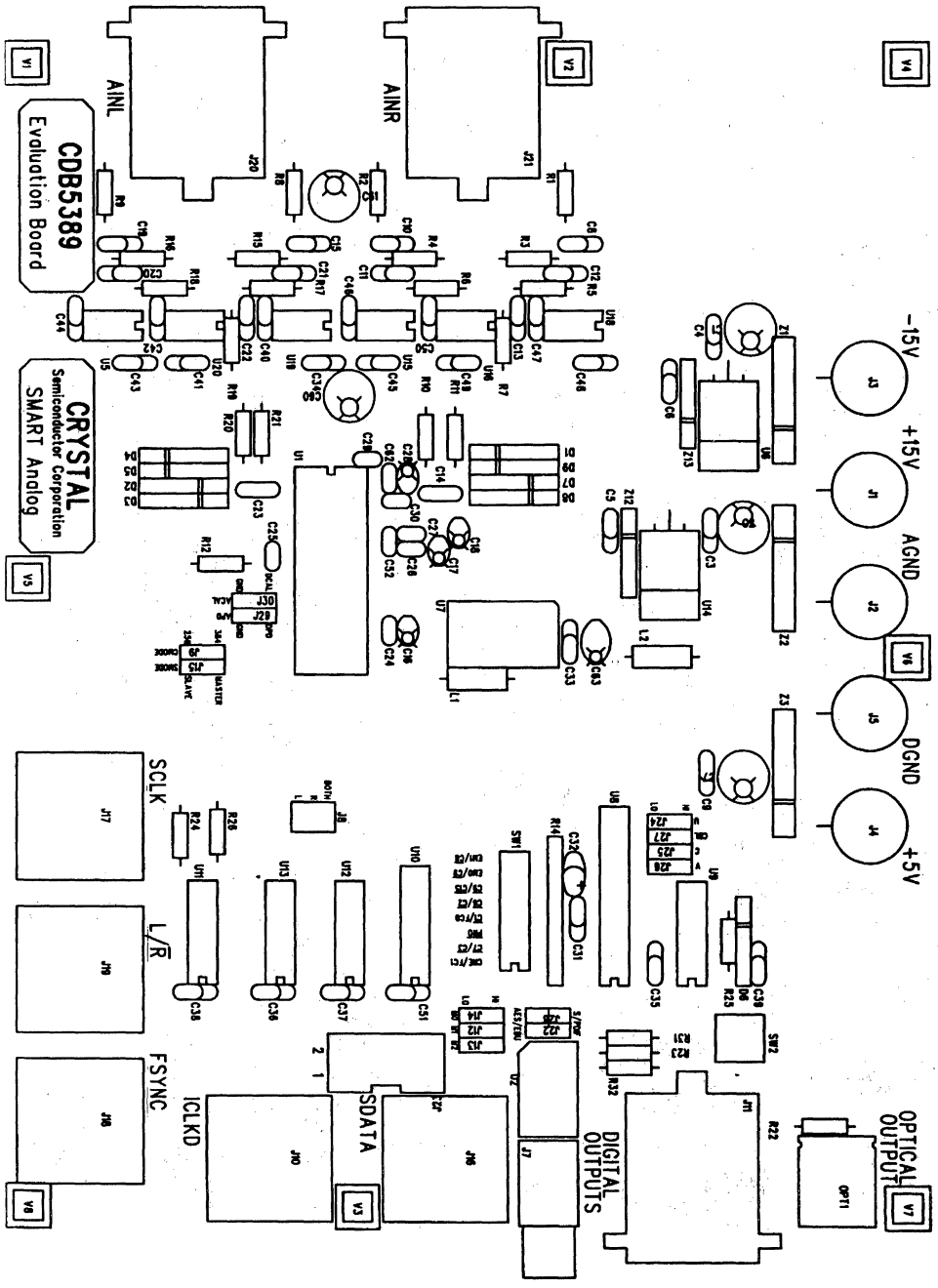
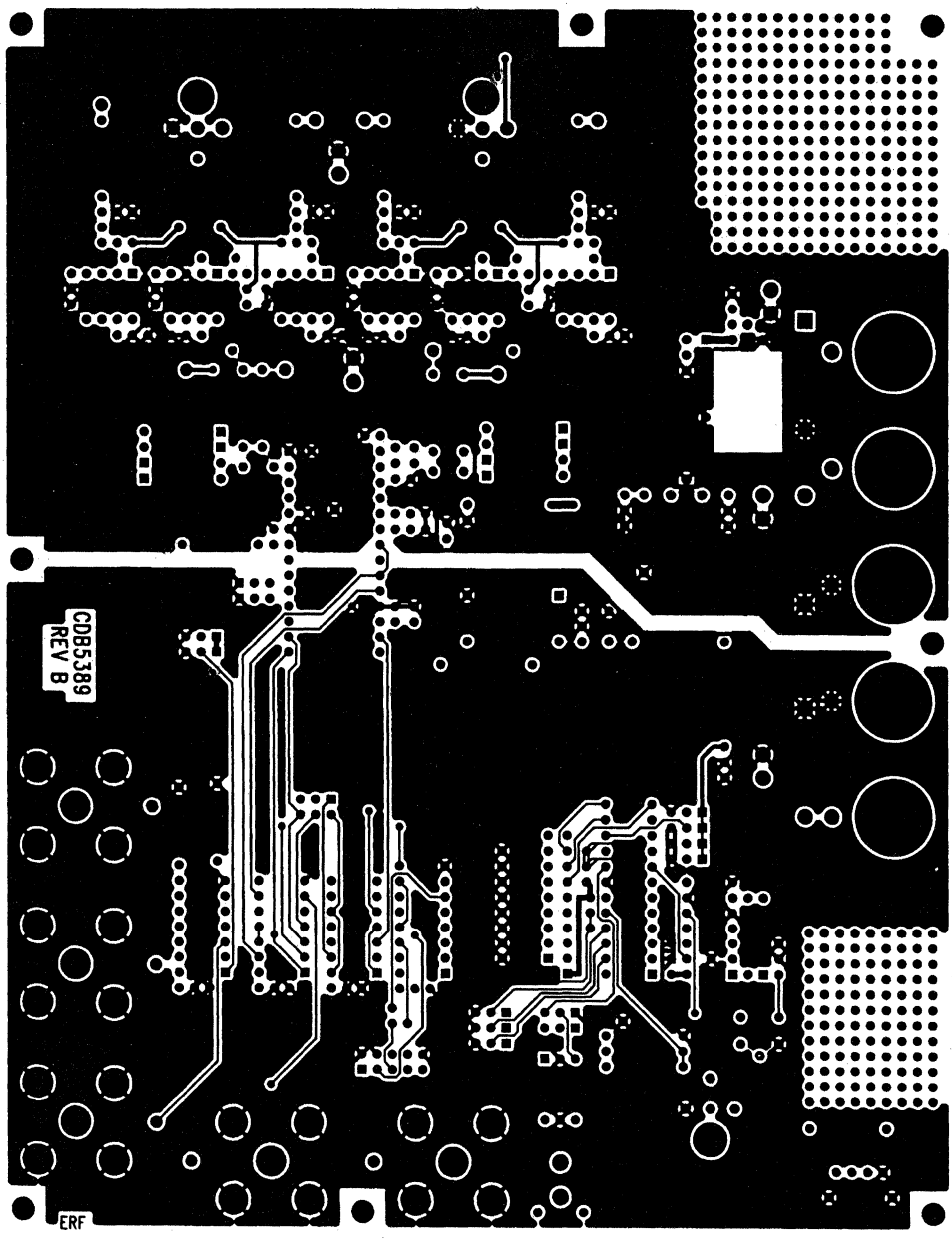


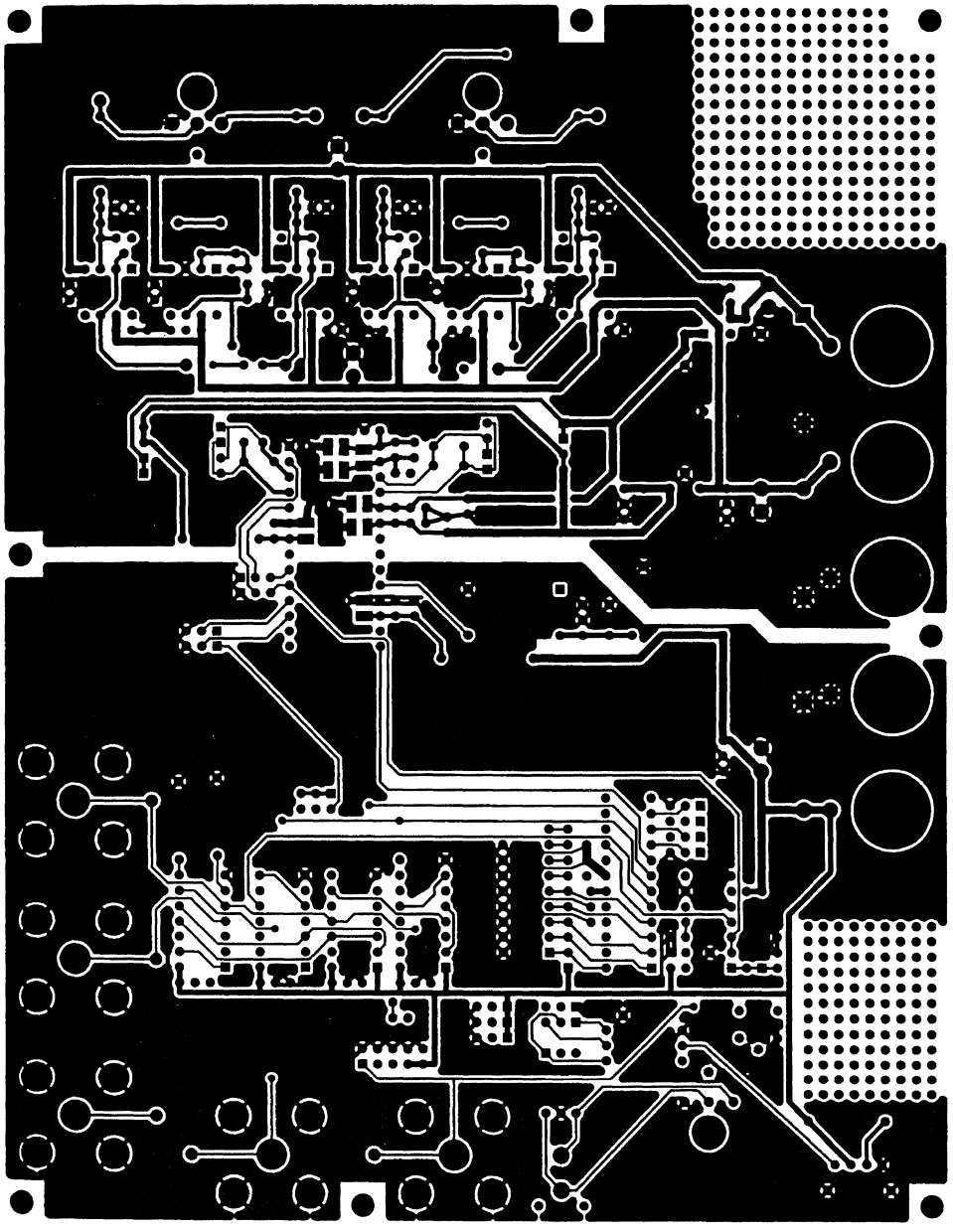
Figure 7. Serial to Parallel Converter
(Not Included with CDB5389/CDB5390)



Silk Screen Layer



Component Side Layer



Solder Side Layer

• Notes •

CS4131 PC-ISA bus to CS4215 Interface

The CS4131 is an interface device which connects to an PC-ISA bus on one side, and connects to the CS4215 audio codec on the other. Registers inside the CS4131 are clocked out serially to control the CS4215.

CS4215 Serial Interface Audio Codec

The CS4215 is a single 44 pin PLCC package containing 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. Also included is a microphone preamplifier, stereo headphone driver, crystal oscillators and a mono monitoring output. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a serial bus.

CS4216 Serial Interface Audio Codec

The CS4216 is a single 44 pin PLCC package containing 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a serial bus.

CS4225 Two ADC, Four DAC Codec

Intended for automotive and surround sound applications, the CS4225 includes two 16-bit ADCs and four 16-bit DACs. The analog inputs have level adjustment and the analog outputs include an output level attenuator. The device has many clocking modes, including using the on-chip PLL for locking onto an audio sample rate clock. The CS4225 runs from +5V and has a low power standby mode.

CS4231 PC ISA Bus Multimedia Audio Codec

The CS4231 is a single chip with 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. Also included is ADPCM compression and decompression, MPC compatible mixer, timer register for audio/visual synchronization and 16 samples deep FIFOs for record and playback. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a parallel bus which meets the PC-ISA bus standard.

CS4248 PC ISA Bus Multimedia Audio Codec

The CS4248 is a single chip with 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a parallel bus which meets the PC-ISA bus standard.

Software

To support the multimedia codec family, a wide range of software is available. Windows and NT drivers are available for the CS4231 and CS4248 multimedia codecs. A comprehensive diagnostics package assists in the debug of boards. In addition, voice recognition and text-to-speech synthesis software demonstrates some of the capabilities of an audio equipped PC.

CONTENTS

• Notes •

Semiconductor Corporation

CS4131

Multimedia Digital Audio Controller

Features

- Direct Interface of CS4215 to ISA Bus
- Support for stereo digital audio up to 48 kHz sample rate at 16 bit resolution.
- 16 bit DMA transfers of 8 or 16-bit audio data to and from host PC.
- Full 10 bit I/O address decode for more flexible I/O space usage and EISA bus compatibility.
- 68 Pin PLCC

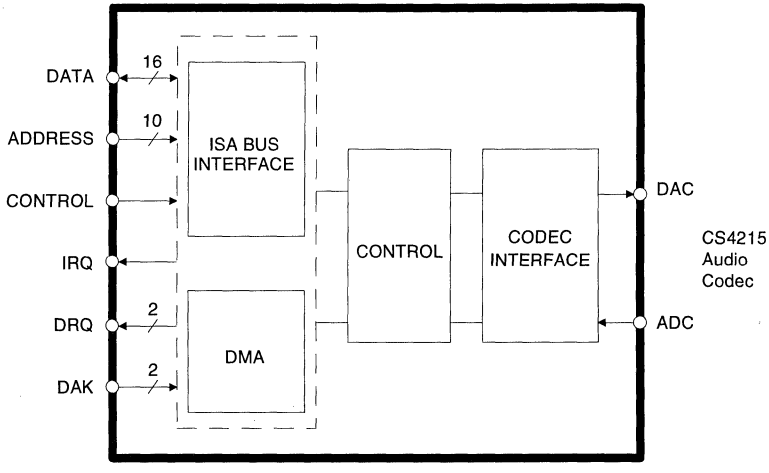
General Description

The CS4131 is a monolithic integrated circuit that provides a digital audio interface between the Crystal CS4215 audio Codec and a personal computer. The CS4131 implements all timer and control functions necessary to record and play back sampled digital audio at sample rates up to 48 kHz. The device is housed in a 68 pin PLCC or 64 pin TQFP.

4

ORDERING INFORMATION:

CS4131-CL	0 to 70°C	68-pin PLCC
CS4131-CQ	0 to 70°C	64-pin TQFP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

DIGITAL CHARACTERISTICS (T_A = 25 °C)

Parameter	Symbol	Min	Max	Unit
Low Level Output Voltage @I_{OL} max	V_{OL}		+0.4	V
High Level Output Voltage @I_{OH} min	V_{OH}	+2.4		V
High Level Output Current @V_{OH} max	I_{OH}			
2 mA driver			-2	mA
4 mA driver			-4	mA
8 mA driver			-8	mA
12 mA driver			-12	mA
Low Level Output Current @ V_{OL} max	I_{OL}			
2 mA driver			+2	mA
4 mA driver			+4	mA
8 mA driver			+8	mA
12 mA driver			+12	mA
Output tristate current	IOZ	-10	+10	µA
Power Consumption	P_O		150	mW
TTL Inputs				
Low Level Input Voltage (TTL level buffer)	V_{ILTTL}		+0.8	V
High Level Input Voltage (TTL level buffer)	V_{IHTTL}	+2.0		V
Low Level Input Current	I_{IL}		-1	µA
High Level Input Current	I_{IH}		+1	µA
Input Pull-Up Current	I_{IL}	-33	-496	µA
Input Pull-Down Current	I_{IH}	33	496	µA
Schmitt Negative Threshold	V_{t-}	0.8		V
Schmitt Positive Threshold	V_{t+}		2.4	V
Schmitt Hysteresis	V_h	0.4		V
CMOS Inputs				
Low Level Input Voltage (CMOS level buffer)	V_{ILCMOS}		0.3*V_{DD}	V
High Level Input Voltage (CMOS level buffer)	V_{IHCMOS}	0.7*V_{DD}		V
Low Level Input Current	I_{IL}		-1	µA
High Level Input Current	I_{IH}		+1	µA
Input Pull-Up Current	I_{IL}	-33	-496	µA
Input Pull-Down Current	I_{IH}	33	496	µA
Schmitt Negative Threshold	V_{t-}	0.2*V_{DD}		V
Schmitt Positive Threshold	V_{t+}		0.8*V_{DD}	V
Schmitt Hysteresis	V_h	1.0		V

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply Voltage		V_{DD}	-0.3	+7.0	V
DC Input Voltage		V_{IN}	-0.3	V_{DD}+0.3	V
DC Input Current	T_A = 25 °C	I_{IN}	-10	+10	mA
Storage Temperature		T_{stg}	-55	+125	°C
Lead Temperature	10 seconds	T_{lead}		300	°C

4

RECOMMENDED OPERATING CONDITIONS (T_A = 25°C)

Parameter	Symbol	Min	Max	Units
DC Supply Voltage	V_{DD}	+4.5	+5.5	V
Ambient Temperature	T_A	0	+70	°C

SWITCHING CHARACTERISTICS (T_A = 25 °C; V_{DD} = 4.75V to 5.25 V), outputs loaded with 10pF, ISA data lines with 15pF; Input Levels: Logic 0 = 0V, Logic 1 = V_{DD}

Parameter	Symbol	Min	Max	Unit
Writes to CS4215; 8-bit IO slave mode				
Address, AEN setup to $\overline{IOWC}$ inactive	t_1	7		ns
Address, AEN hold from $\overline{IOWC}$ inactive	t_2	12		ns
Data setup to $\overline{IOWC}$ inactive	t_3	3		ns
Data hold from $\overline{IOWC}$ inactive	t_4	16		ns
$\overline{IOWC}$ active time	t_{4A}	96		ns
Reads from CS4215; 8-bit IO slave mode (Note 1)				
Data valid from $\overline{IORC}$ active	t_5	6	35	ns
Data hold from $\overline{IORC}$ inactive	t_6	4	24	ns
$\overline{IORC}$ active time	t_{6A}	48		ns
Writes to CS4215; 16-bit DMA slave mode (Note 2)				
DRQ inactive from $\overline{DACK}$ active (8-bit mono and stereo, 16-bit mono)	t_7		34	ns
DRQ inactive from $\overline{IOWC}$ or $\overline{IORC}$ active (16-bit stereo)	t_8		41	ns
Data setup to $\overline{IOWC}$ inactive	t_9	3		ns
Data hold from $\overline{IOWC}$ inactive	t_{10}	17		ns
$\overline{IOWC}$ inactive time	t_{11}	90		ns
$\overline{IOWC}$ active time	t_{12}	96		ns
Reads from CS4215; 16-bit DMA slave mode (Note 2)				
$\overline{IORC}$ active time	t_{13}	48		ns
Data valid from $\overline{IORC}$ active	t_{14}	6	34	ns
Data hold from $\overline{IORC}$ inactive	t_{15}	3	25	ns
$\overline{IORC}$ Inactive Time	t_{16}	90		ns
CS4131 Reset				
Internal registers reset from RESDRV active	t_{17}	5	26	ns
RESDRV pulse width (Required by CS4215)	t_{18}	500		ns
Control Bit Outputs (Note 3)				
New control bit output values from $\overline{IOWC}$ inactive	t_{19}	10	32	ns

Notes:
1. These specifications assume an ISA compliant controller which provides an address setup and hold to $\overline{IORC}$.
2. These specifications assume an ISA compliant controller which provides a $\overline{DACK}$ setup and hold relative to $\overline{IOWC}$ for writes to the CS4215, and relative to $\overline{IORC}$ for reads from the CS4215.
3. These outputs cover the signals that are reflections of control bit registers. These include SERD/C, PDN, and $\overline{AUDRST}$.

SWITCHING CHARACTERISTICS (Continued)

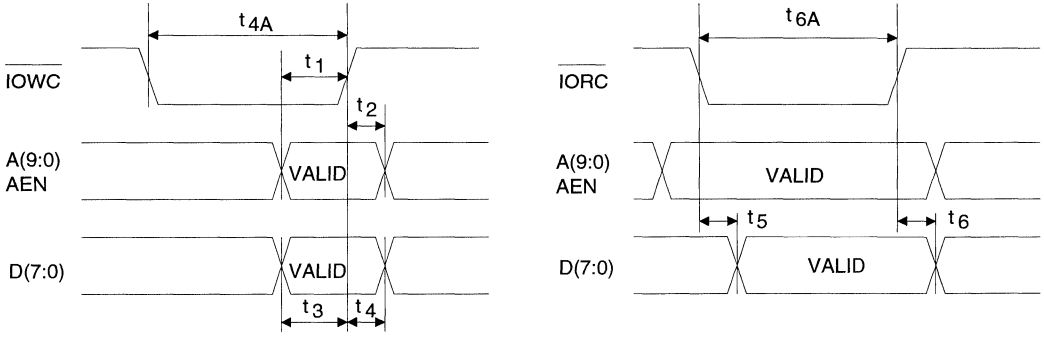
Parameter	Symbol	Min	Max	Unit
Interrupt Output				
"Threshold" DMA operation to INTOUT active	t_{20}	2 BCLK + 4	3 BCLK + 24	ns
INTCLRBIT active write to INTOUT inactive	t_{21}	1 BCLK + 5	2 BCLK + 29	ns
External Buffer Control (Note 4)				
$\overline{IOWC}$ active to $\overline{DBUFENx}$ active	t_{22}	5	29	ns
$\overline{IOWC}$ inactive to $\overline{DBUFENx}$ inactive	t_{23}	10	65	ns
$\overline{IORC}$ active to DBUFDIR active (programmed I/O mode)	t_{24}	4	22	ns
$\overline{IORC}$ active to $\overline{DBUFEN0}$ active (programmed I/O mode)	t_{25}	11	64	ns
$\overline{IORC}$ inactive to $\overline{DBUFENx}$ inactive (both programmed I/O and DMA mode)	t_{26}	5	28	ns
$\overline{IORC}$ inactive to DBUFDIR inactive (programmed I/O mode)	t_{27}	11	65	ns
$\overline{DACK0}$ or $\overline{DACK1}$ active to DBUFDIR active (DMA mode)	t_{28}	4	22	ns
$\overline{DACK0}$ or $\overline{DACK1}$ inactive to DBUFDIR inactive (DMA mode)	t_{29}	5	30	ns
$\overline{IORC}$ active to $\overline{DBUFENx}$ active (DMA mode)	t_{30}	5	29	ns
Serial Bus Interface; CS4215 Master Mode				
SCLK Period	t_{31}	125		ns
SCLK high time	t_{32}	50		ns
SCLK low time	t_{33}	50		ns
FSYNC setup to SCLK falling	t_{34}	3		ns
FSYNC hold from SCLK falling	t_{35}	17		ns
SDIN setup to SCLK falling	t_{36}	3		ns
SDIN hold from SCLK falling	t_{37}	14		ns
SCLK rising to SDOUT	t_{38}	5	46	ns
TSOUT setup to SCLK falling	t_{39}	3		ns
TSOUT hold from SCLK falling	t_{40}	14		ns

Notes: 4. $\overline{DBUFENx}$ refers to $\overline{DBUFEN0}$ or $\overline{DBUFEN1}$

4

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Unit
Serial Bus Interface; CS4215 Slave Mode				
SCLK period. Is BCLK divided by eight	t_{41}	800	1200	ns
SCLK high time	t_{42}	300	700	ns
SCLK low time	t_{43}	300	700	ns
SCLK rising to FSYNC	t_{44}	7	40	ns
SDIN setup to SCLK falling	t_{45}	3		ns
SDIN hold from SCLK falling	t_{46}	14		ns
SCLK rising to SDOUT	t_{47}	5	46	ns
TSOUT setup to SCLK falling	t_{48}	3		ns
TSOUT hold from SCLK falling	t_{49}	14		ns



a. Write Timing b. Read Timing

Figure 1. CS4131 in 8-bit I/O Slave Mode

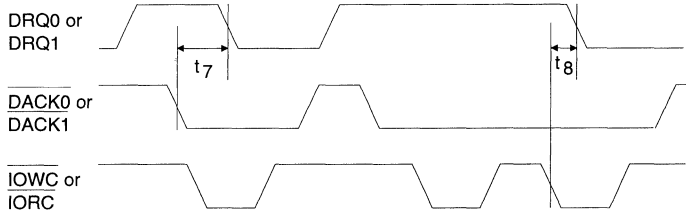
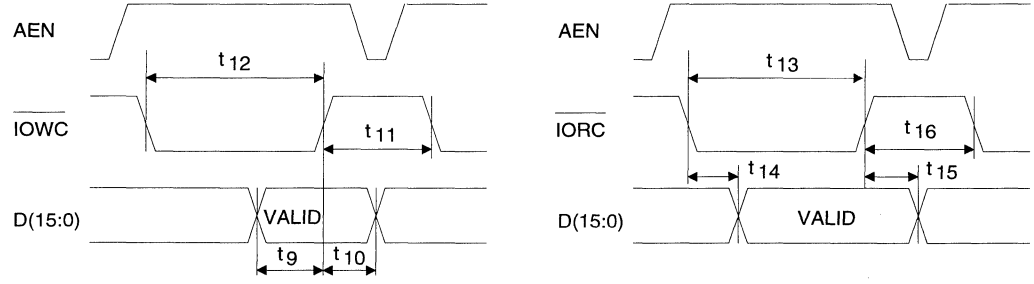


Figure 2. DMA Deassertion



a. Write Timing b. Read Timing

Figure 3. CS4131 in 16-bit DMA Slave Mode

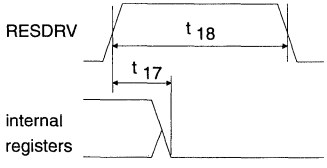


Figure 4. CS4131 Reset Timing

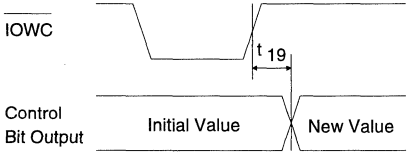


Figure 5. Control Bit Output Timing

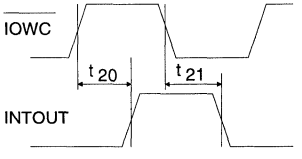


Figure 6. CS4131 Interrupt Output Timing

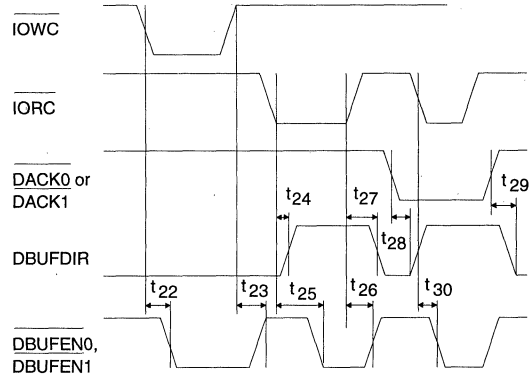
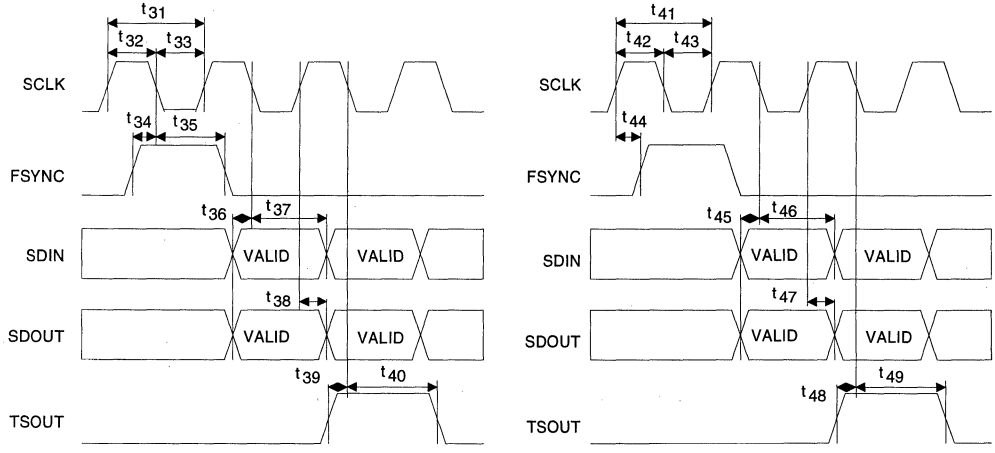


Figure 7. CS4131 External Buffer Control Timing



a. CS4215 in Master Mode

b. CS4215 in Slave Mode

Figure 8. Serial Bus Interface Timing

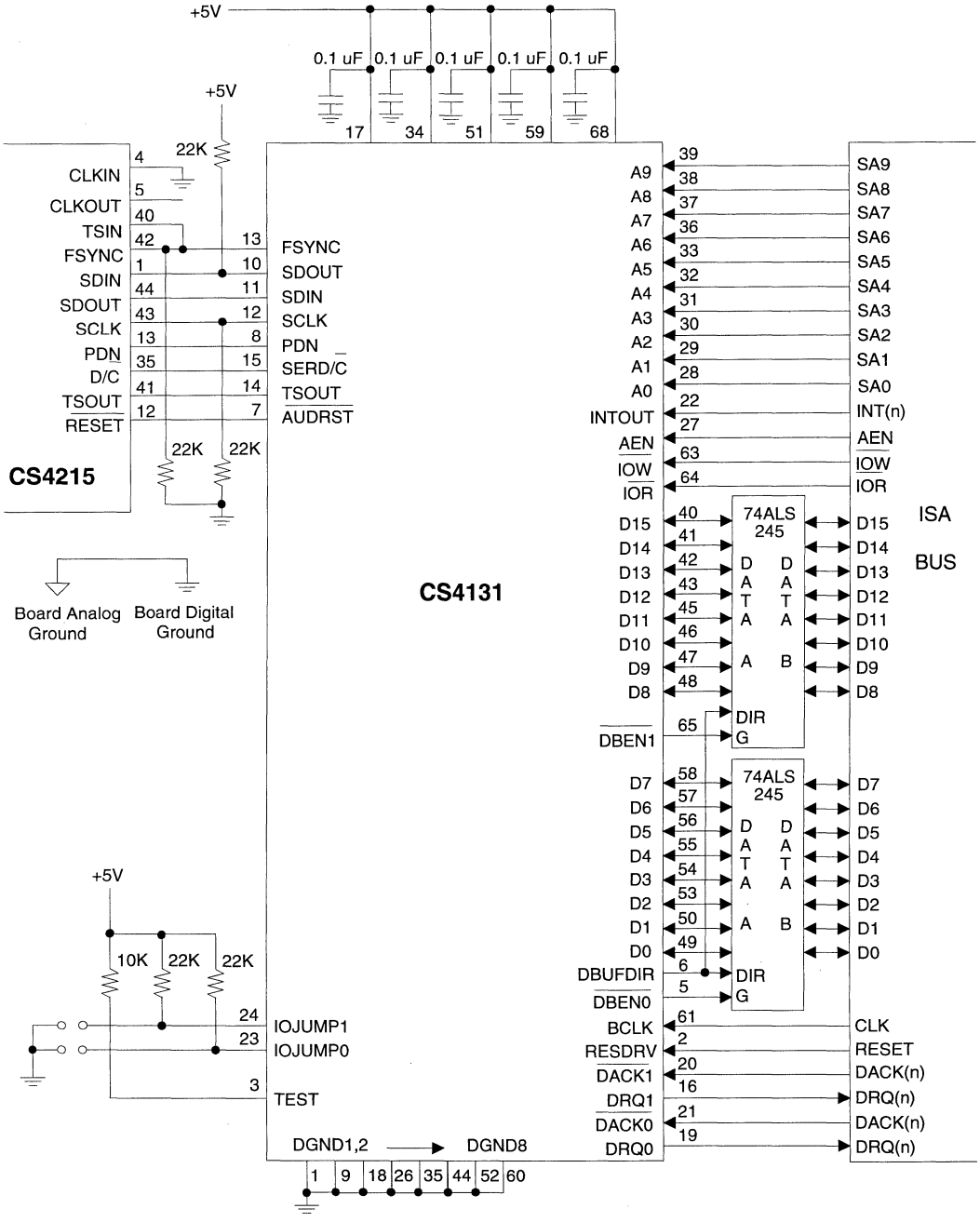


Figure 9. Typical Connection

FUNCTIONAL DESCRIPTION

Overview

The CS4131 provides an interface between the CS4215 and the 16-bit ISA bus. The CS4131 resides on the ISA bus found in the class of desktop computers known as "PC-compatibles", or PC's. It can act as both an I/O and DMA slave.

As an 8-bit I/O slave, the CS4131 decodes its own 16-byte I/O range, from among four possible base addresses, that can be selected via two external pins. The CS4131 is used as an I/O slave primarily to set up its mode of operation.

The CS4131 also acts as a 16-bit DMA slave. It is physically connected to one or two DMA channels. It can use either channel for both input and output, or use one channel for input and the other for output. The CS4131 can tristate one or both DMA request lines to free up the channels it is not using. It is used as a DMA slave for sample transfers to and from the CS4215 Codec.

The CS4131 provides one interrupt request (IRQ) line to notify the software driver when the audio data ring buffer needs servicing.

The CS4131 can sink 12 mA on each data bus pin. For use in systems that require stronger drive on the ISA data lines, two pins are provided to control an external 74ALS245 buffer. In a local bus implementation, no buffers are typically required.

Component Requirements

External pullups or pulldowns may be connected to the two IOJUMP pins if the system designer requires a base I/O location other than the default 240H. The global tristate input is pulled-up internally.

An external pullup is required on SDOUT, and external pulldowns are required on SCLK and FSYNC. Series termination resistors may be added depending on layout proximity of the CS4131 and CS4215. For close spacing, they will not be necessary.

Two 74ALS245 data buffers may be added if the 12 mA drive provided by the CS4131 is insufficient for system requirements. The "A" side of the buffers should connect to the CS4131 data bus and the "B" side of the buffers should connect to the PC data bus.

Connecting to the CS4215

The CS4131 connects to the CS4215 serial interface lines. The CS4131 requires that the CS4215 operate in master mode while recording or playing back samples. It also requires that FSYNC and TSIN be tied together on the CS4215, and the CS4215 be programmed in 128 bits per frame mode (see Control Time Slot 3 in the CS4215 data sheet). The CS4131 always receives FSYNC from the CS4215, except during Control Mode.

Transfer of Data

Write Operation

For writes to the CS4215, the CS4131 takes parallel data from the data bus and shifts it out to the Codec one bit at a time. Before shifting the data out, the CS4131 appends control bits to the data packet, and orders the data correctly according to mono/stereo and 8/16-bit conditions. When fresh data is needed for another packet, the CS4131 issues a DMA request, receives new data, and repeats the shift out operation.

Read Operation

For reads of the CS4215, the CS4131 receives a packet from the CS4215, strips off the relevant bytes according to mono/stereo and 8/16-bit conditions, and loads them into 8-bit registers. It then issues a DMA request, and the ensuing DMA read operation transfers the data from the CS4131 registers to main memory.

Control Mode Operation

For control mode operations, the CS4131 drives D/$\overline{C}$ LO to the CS4215, and takes over driving the SCLK and FSYNC lines. The control packet is formed in the CS4131 by means of I/O writes, and then shifted out under CS4131 control after an I/O write to the CS4131 results in an FSYNC.

The CS4131 acts as an 8-bit slave for programmed I/O operations, and as a 16-bit DMA slave. It is capable of meeting timing for extended ISA "TYPE A" DMA, or for the standard ISA DMA timings.

Reset

The ISA reset signal, RESDRV, resets all registers in the CS4131. The control register bits are all reset low. See descriptions of the control registers for bit interpretations.

I/O Slave Operations

The CS4131 operates as an 8-bit I/O slave meeting standard ISA timing. It occupies a 16-byte address range, with its base address set by the two IOJUMP input pins.

Internal Decode

The CS4131 register set occupies 16 contiguous I/O addresses, beginning at a base address determined by logic levels of the two I/O jumper pins as follows:

IOJUMP1	IOJUMPO	CS4131 Registers Base Address
0	0	240H
0	1	050H
1	0	260H
1	1	250H

Note: in an EISA-based system, the CS4131 can receive a slot-specific AEN, resulting in a base address of X240 for example, when IOJUMP0 and 1 are both 0, and AENX is connected to the CS4131.

Register Set

Table 1 shows the CS4131 register set.

Timeslot Registers

The TIMESLOT registers are used to load and unload the serial shift register.

Figure 10 shows the TIMESLOT and shift register data path.

The data written to the TIMESLOT registers is used to load the shift register that in turn, supplies the CS4215. The data read from the TIMESLOT registers originates from the CS4215, and is held in the registers until it can be written to main system memory (DRAM). To read what was just written to the TIMESLOT registers, the programmer must put the CS4215 into loopback mode, assert FSYNC, and wait at least 70 µs for the shift loopback operation to complete. The TIMESLOT registers can be read back at that point.

TIMESLOT registers 1 through 4 can be written either via programmed I/O writes or DMA operations. Which registers are written to or read

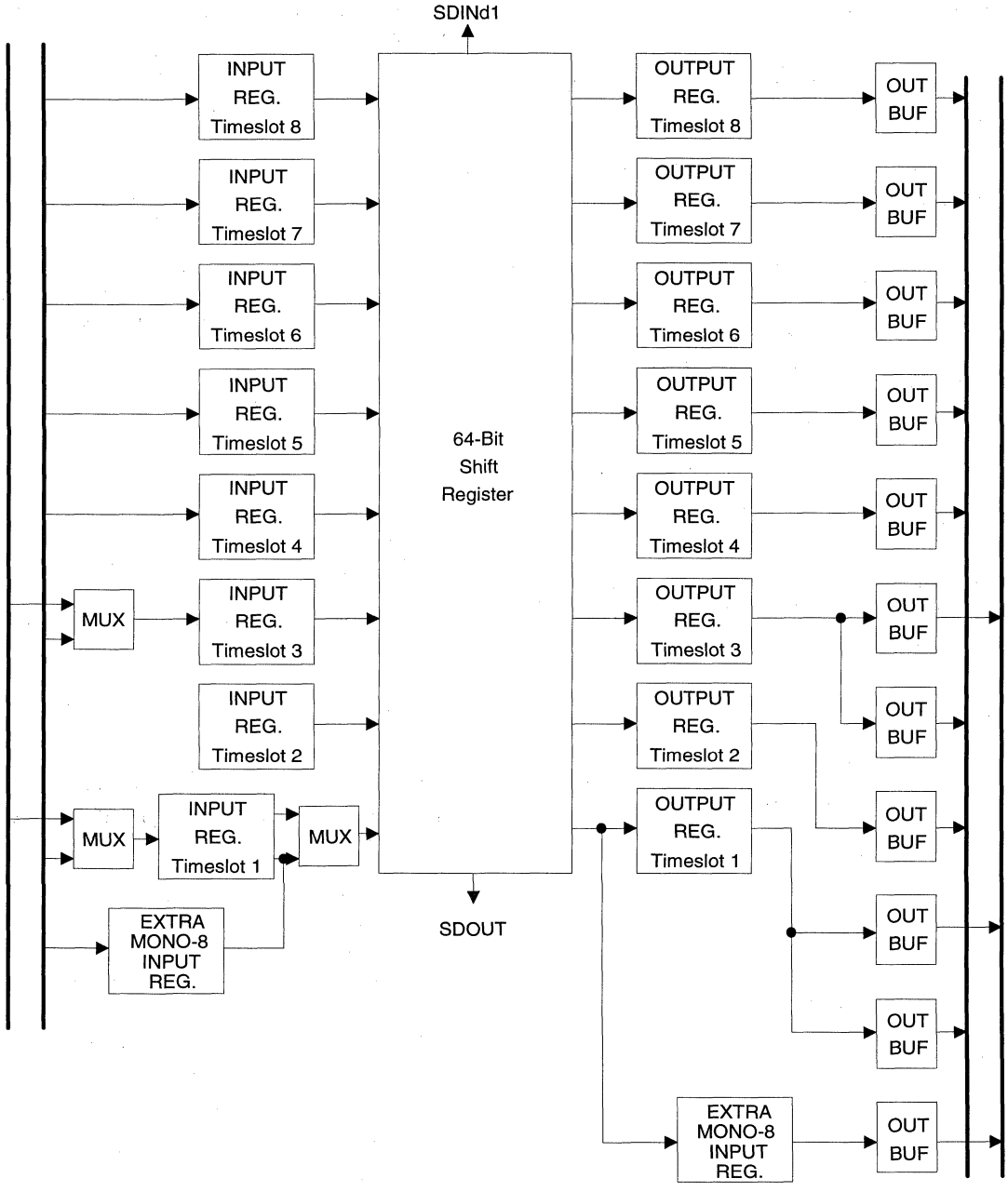


Figure 10 Register Data Path.

Register Name	Offset Address	Function
TIMESLOT1	0000	Byte 1 of packet
TIMESLOT2	0001	Byte 2 of packet
TIMESLOT3	0010	Byte 3 of packet
TIMESLOT4	0011	Byte 4 of packet
TIMESLOT5	0100	Byte 5 of packet
TIMESLOT6	0101	Byte 6 of packet
TIMESLOT7	0110	Byte 7 of packet
TIMESLOT8	0111	Byte 8 of packet
CONTROL REGISTER A	1000	Control register - CS4131 configuration bits.
CONTROL REGISTER B	1001	Control register - CS4131 configuration bits.
DIE REVISION	1010	Holds revision level of the CS4131. First revision holds the signature A0H.
FRAME COUNT READ	1011	Holds current value of internal frame bit counter. Read-only register used for chip test.
STATUS POLL	1100	Holds bits that can be read by software to determine packet transfer and interrupt flag status.
DMA COUNTER LSB READ	1101	Holds current value of LSB of DMA. Read only register used for chip test.
DMA COUNTER MSB READ	1110	Holds current value of MSB of DMA. Read only register used for chip test.
DMA COUNTER LOAD	1111	Upper byte of word that is used to initialize the DMA counter.

Table 1. Register Set Table

Bit	Name	Function
0	DMAOEN	When high, enables DMA from DRAM to CS4131 (Writes to CS4215).
1	DMAIEN	When high, enables DMA from CS4131 to DRAM (Reads of the CS4215).
2	ID/$\overline{C}$	Directly controls SERD/$\overline{C}$ pin on CS4215. When low, puts the CS4215 in control mode.
3	ICMD	When high, allows the CS4131 to drive the bidirectional SCLK and FSYNC lines that connect the CS4131 and CS4215.
4	STEREO	When high, tells the CS4131 that it should assume that the CS4215 is operating in stereo modes.
5	WIDTH16	When high, tells the CS4131 that it should assume that the CS4215 is operating with 16-bit samples.
6	IPDN	Directly controls PDN pin on the CS4215. When high, puts CS4215 into a powered down, "sleep" state. Systems that depend on the CMOUT signal of the CS4215 to always be active should never set this bit high.
7	FSYNCBIT	When ICMD is active, a write of high to this bit will cause a single FYSNC bit to be output to the CS4215. This initiates a control packet transmission. Note that no succeeding write of 0 is required.

Table 2. Control Register A Bit Definitions

Control Register B

Bit	Name	Function
0	DMACNTSEL	When high, DMA writes to CS4131 increment the DMA cycle counter. When low, DMA reads from CS4131 increment the counter.
1	DMAMOD0	Defines DMA pin usage (see DMA mode table), pg. 14
2	DMAMOD1	Defines DMA pin usage (see DMA mode table), pg. 14
3	INTCLRBIT	A write of high to this bit will clear the INT line driven by CS4131. Not that no succeeding write of 0 is required.
4	DMACNTRST	When high, resets the DMA cycle counter.
5	$\overline{\text{SERBUSEN}}$	When low, enables the CS4131 to drive serial bus lines. When high, CS4131 tristates its drivers for these lines.
6	AUDRST	When high, resets the CS4215 and also puts the CS4131 into serial loopback mode.
7	CLRSREN	When high, disables shift operations in the 64-bit shift register.

Table 3. Control Register B Bit Definitions

Status Poll Register

Bit	Name	Function
0	RCVD_TSOUT	Set high when TSOUT received at completion of packet transfer. Reset by read from Timeslot 1.
1	SENT_PKT	Packet sent out to CS4215. Set high at beginning of packet transfer. Reset by write to Timeslot 1.
6	INTOVF	Interrupt overflow. Goes active when a DMA counter terminal count is reached before a pending interrupt for a previous DMA counter terminal count was serviced. Reset by a write of high to INTCLRBIT in Control Register B
7	INTFLG	Interrupt request activated by CS4131 when DMA terminal count is reached. Reflects state of INTOUT pin. Reset by a write of high to INTCLRBIT in Control Register B.

Table 4. Status Poll Register Bit Definitions

from during DMA is determined by the CS4131 byte packing algorithm, described later.

TIMESLOT registers 5 through 8 are only written to via programmed I/O. They do not receive DMA service because they are usually static during sample playback and record operations. Keeping these register values stored in the CS4131 also reduces ISA bus bandwidth requirements.

TIMESLOT registers 5 through 8 can be written to while DMA activity is in progress. These registers may be written to asynchronously, but should be synchronized with the loading of the main shift register as follows:

1) Wait for the RCVD_TSOUT (in Status Poll Register) to go low.
2) Wait for RCVD_TSOUT to go high.
3) Write to time slot Register 5-8 immediately.

DMA Counter LSB Read

This register holds the current value of the LSB of the 16-bit DMA counter. This register is used

for chip test purposes to increase the fault coverage of the test. It is not needed by the software drivers, although it may be used for diagnostics if deemed necessary.

DMA Counter MSB Read

This register holds the current value of the MSB of the 16-bit DMA counter. This register is used for chip test purposes to increase the fault coverage of the test. It is not needed by the software drivers, although it may be used for diagnostics if deemed necessary.

DMA Counter Load Register

The DMA Counter Load register sets the initial count value for the DMA cycle counter. The DMA cycle counter is a 16-bit counter. Its lower eight bits are initialized to zero. The Counter Load Register only initializes the upper eight bits. The DMA counter is an up counter, incrementing its value on each DMA transfer. The DMACNTSEL bit in Control Register B sets the counter to increment on reads or writes.

The load value programmed in the register is inverted before loading into the DMA counter. For example, if the load value programmed was 01H, the counter will be initialized to FE00H. The counter will count 512 DMA operations before an interrupt is generated by the count value reaching FFFFH.

The number of DMA operations before interrupt generation = ((load register value+1) * 256).

Writes to CS4215 Codec

ISA Bus Operation

When DMA is enabled for writes to the CS4215 (via the DMAIEN bit in Control Register A), the CS4131 issues a DMA request (DRQ) as soon as the current contents of the TIMESLOT registers are loaded into the shift register in preparation for a packet output. Once this load occurs, the TIMESLOT registers are free to be loaded with data for the next packet output. (The DMA channel used is determined by the programming of the DMAMOD bits in Control Register B.) The DMA acknowledge ($\overline{DACK}$) will return from the system board DMA controller. While $\overline{DACK}$ is active, the DMA controller will execute one or two write cycles to the CS4131. The two cycle case occurs when the CS4131 indicates 16-bit stereo mode. Note that the DMA controller should always be programmed in demand mode. At the beginning of the last cycle that the CS4131 requires, it will deassert its DRQ signal. The data is now in the TIMESLOT register, ready to be loaded into the shift register when the next packet is needed by the CS4131.

Note that the DMA latency required for no sample underruns is approximately equal to the sample period. For example, a 44k Sample/sec rate has a latency requirement of about 22µs, while a 8 k sample/sec rate has a latency requirement of about 125 µs.

Serial Bus Operation

The activation of FSYNC by the CS4215 begins this operation. The CS4131 responds to the FSYNC sampled on the falling edge of SCLK by driving data out on its SDOUT pin on the next rising edge of SCLK. This continues for each SCLK, until the clock after TSOUT is sampled on a falling edge of SCLK.

Reads of the CS4215 Codec

ISA Bus Operation

When DMA is enabled for reads of the Codec (via the DMAIEN bit in Control Register A), the CS4131 issues a DMA request (DRQ) as soon as a packet is loaded into the TIMESLOT registers. The DMA channel used is determined by the

programming of the DMAMOD bits in Control Register B. The DMA acknowledge ($\overline{DACK}$) will return from the system board DMA controller. While $\overline{DACK}$ is active, the DMA controller will execute one or two read cycles from the CS4131. The two cycle case occurs when the CS4131 indicates 16-bit stereo mode. Note that the DMA controller should always be programmed in demand mode. At the beginning of the last cycle that the CS4131 requires, it will deassert its DRQ signal. The DMA cycle will complete with the sample data completely transferred from the CS4215 to the CS4131 to DRAM.

Note that the DMA latency required for no sample overruns is approximately equal to the sample period. For example, a 44k Sample/s rate has a latency requirement of about 22µs.

Serial Bus Operation

The activation of FSYNC by the CS4215 begins this operation. The CS4131 responds to FSYNC sampled on the falling edge of SCLK by loading data from SDIN into the shift register on the next rising edge of SCLK. This continues for each SCLK, until the clock after TSOUT is sampled on a falling edge of SCLK

Byte Ordering and Packing

8-bit Mono Reads

One DMA read operation serves for two samples. A DMA request only occurs after every second sample. The ensuing DMA read contains the first sample data on D(7:0) and the second sample data on D(15:8). Therefore, the first sample received in time goes into the lower memory location.

8-bit Stereo Reads

A DMA request is issued for each sample. The left channel data is driven on D(7:0) and the right channel data on D(15:8). Therefore, the left channel data goes into the lower memory location.

16-bit Mono Reads

A DMA request is issued for each sample. The most significant byte of the sample is driven on D(15:8) and the least significant byte on D(7:0). Therefore, the least significant byte goes into the lower memory location. This conforms to the little-endian standard of Intel x86 processors.

16-bit Stereo Reads

Two DMA reads of the CS4131 are required to load a single packet. These two reads are accomplished with a single DMA request, using the demand transfer mode of the DMA controller. The first DMA read will have the left channel most significant byte on D(15:8), and left channel least significant byte on D(7:0). The second DMA read will have the right channel most significant byte on D(15:8), and right channel least significant byte on D(7:0). The resulting filled memory will look like this:

Memory Offset	Contents
0	Left channel LSB
1	Left channel MSB
2	Right channel LSB
3	Right channel MSB

8-bit Mono Writes

One DMA write operation serves for two samples. A DMA request only occurs after every second sample. The CS4131 will use the data on

DMAMOD1	DMAMOD0	DMA Channel Usage
0	0	Neither channel used. Both DRQ0 and DRQ1 tristated. INTOUT is tristated, too.
0	1	DMA channel 0 is used for both reads from and writes to the CS4215. INTOUT enabled.
1	0	DMA channel 1 is used for both reads form and writes to the CS4215. INTOUT enabled.
1	1	DMA channel 0 is used for reads from the CS4215. DMA channel 1 is used for writes to the CS4215. INTOUT enabled.

Table 5. DMA Mode Table

D(7:0) for its first packet, and the data on D(15:8) for its second packet.

During pause of play (suspended DMA), the CS4131 will still send alternating samples from TIMESLOT1 register and the extra storage register. To avoid an output of Fs/2, set the WIDTH16 bit in Control Register A. When DMA resumes, this bit can be reset.

8-bit Stereo Writes

A DMA request is issued for each sample. The CS4131 will use the data on D(7:0) as left channel data, and the data on D(15:8) as right channel data.

16-bit Mono Writes

A DMA request is issued for each sample. The CS4131 will use the data on D(7:0) as the least significant byte of the sample data, and the data on D(15:8) as the most significant byte of the sample data.

16-bit Stereo Writes

Two DMA writes from the CS4131 are required to unload a single packet. These two writes are accomplished with a single DMA request, using the demand transfer mode of the DMA controller. The first DMA write will expect the left channel most significant byte on D(15:8), and left channel least significant byte on D(7:0). The second DMA write will expect the right channel most significant byte on D(15:8), and right channel least significant byte on D(7:0) The required memory map is shown below:

Memory Offset	Contents
0	Left channel LSB
1	Left Channel MSB
2	Right channel LSB
3	Right channel MSB

DMA and Interrupt Issues

DMA Mode Selection

The CS4131 provides the flexibility of software-selectable DMA channels. Note that the CS4131 must utilize 16-bit DMA channels, which are typically channels 5, 6, and 7 in ISA systems. The channel usage is set by the DMAMOD bits of Control Register B, as shown in Table 5.

DMA Counter

The DMA counter is used to count the number of either DMA writes to the CS4215 or DMA reads from the CS4215, depending upon the setting of the DMACNTSEL bit found in Control Register B. When the counter reaches its terminal value of FFFFH, the INTOUT output of the CS4131 is activated. This interrupt can signal the

software driver that the sample ring buffer in DRAM needs to be serviced. The counter is set to its initial value via the DMA Counter Load Register. This register sets the upper eight bits of the counter to the inverse of the value that is programmed into it. The lower eight bits of the counter are always initialized to FE00H. The counter will count 512 DMA operations before an interrupt is generated by the count value reaching FFFFH.

The number of DMA operations before interrupt generation = ((load register value+1) * 256).

After the counter reaches FFFFH, it rolls over and begins counting again at the value programmed by the DMA Counter Load Register.

Interrupt Output

Generation

The INTOUT signal is generated when the DMA counter reaches FFFFH. it remains active until cleared via the I/O write described below. The state of INTOUT is mirrored in the INTFLG bit in the Status Poll Register.

Clearing

The INTOUT signal is cleared by writing a high to the INTCLRBIT found in Control Register B. If left active in the register, this high will not prevent a succeeding INTOUT from being asserted. Therefore, there is no need to write a low to INTCLRBIT after the first write of a high.

CS4215 Control Mode

Enabling of SCLK and FSYNC

The CS4131 will drive SCLK and FSYNC when the ICMD bit found in Control Register A is high. It is recommended that this bit only be set high when ID/$\overline{C}$ in the same register is low. This will prevent contention with the CS4215 on these lines.

The CS4131 enables these lines synchronously to the new SCLK that will be driven. In other words, when these lines are enabled, there will be no spikes or runt pulses on SCLK, and FSYNC will be initially driven to a clean low. The CS4131 also disables these lines synchronously to SCLK, ensuring that there are no clock spikes or runt pulses.

The synchronization carries a time penalty, so allow 2 µs after the I/O write that modifies ICMD before assuming that the action of the write (SCLK/FSYNC enable or disable) is complete.

SCLK frequency

The SCLK generated by the CS4131 for control mode operations is formed by a divide-by-eight of the ISA BCLK input. Therefore, it will operate at a nominal frequency of 1 MHz.

FSYNC generation

FSYNC is generated for the CS4215 control mode by writing a high to the FSYNCBIT found in Control Register A. Note that no succeeding write of a low is required.

Under normal operation, a second FSYNC cannot be generated until the TSOUT from the first one is received. This can cause a problem with the CS4215, as it does not return TSOUT from the first FSYNC it receives when it goes into control mode. To work around this problem, observe the following procedure.

1) Generate initial FSYNC with FSYNCBIT.

2) Wait a minimum of 100 µs.

3) Allow a second FSYNC to be sent by pulsing the CLRSREN bit found in Control Register B high, then low.

4) Send a second FSYNC by writing to Control Register A with FSYNCBIT high.

5) Read Status Poll Register until RCVD TSOUT is active.

Now the CS4215 should be returning TSOUT to each FSYNC and FSYNC can be asserted using a polling procedure instead of using software timers:

1) Read and write to offset 0 to clear Status Poll Register bits.

2) Generate FSYNC.

3) Read Status Poll Register to determine if TSOUT has been received by the CS4131. If so, read and write to offset 0 to clear Status Poll Register bits.

CS4215 Reset

The CS4215 is reset by two conditions:

1) ISA Bus reset initiated by RESDRV. This also resets all CS4131 logic.

2) XAUDRST bit found in Control Register B is high. Note that this bit also puts the CS4131 into serial loopback mode. XAUDRST does not reset CS4131 logic - it only puts it into loopback mode.

Selective Tristate of Serial Lines

The CS4131 serial lines that interface to the CS4215 are tristated by the CS4131 when the $\overline{\text{SERBUSEN}}$ bit found in Control Register B is driven inactive (high). Note that these lines are not tristated upon power up reset.

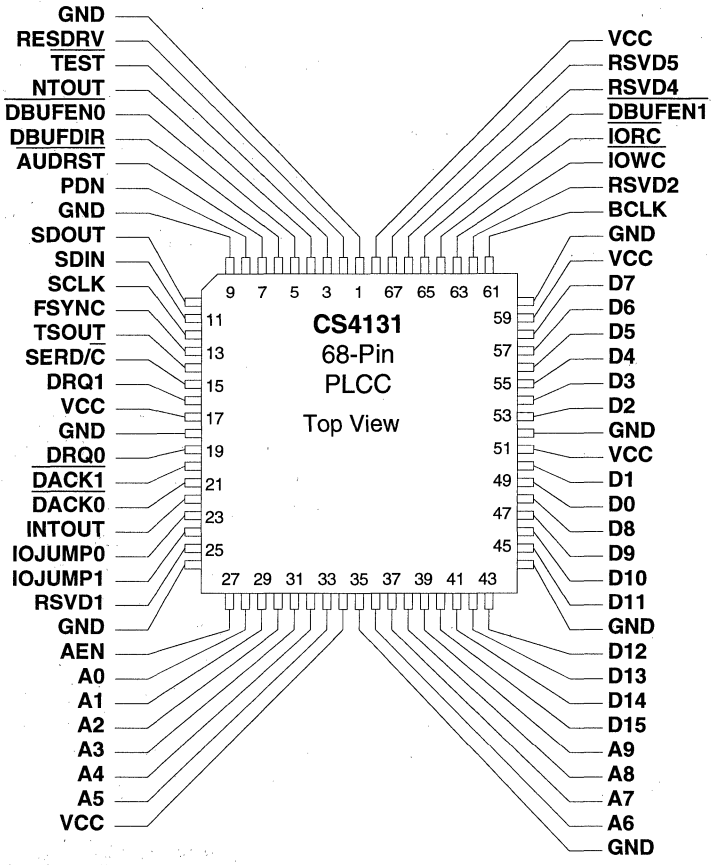
External Buffer Control

The CS4131 data bus lines can sink up to 12 mA per pin. For system applications where greater drive is required, the CS4131 provides control lines for two external 74ALS245 type buffers. The 74ALS245's should have their "A" sides connected to the CS4131, and their "B" sides connected to the ISA data bus. The CS4131 $\overline{\text{DBUFEN0}}$ output should be connected to the $\overline{\text{EN}}$ input of the 74ALS245 that connects to the low order byte of the ISA data bus, and the $\overline{\text{DBUFEN1}}$ output should be connected to the $\overline{\text{EN}}$ input of the 74ALS245 that connects to the high order byte of the ISA data bus. The CS4131 DBUFDIR output should be connected to the DIR input of both 74ALS245's.

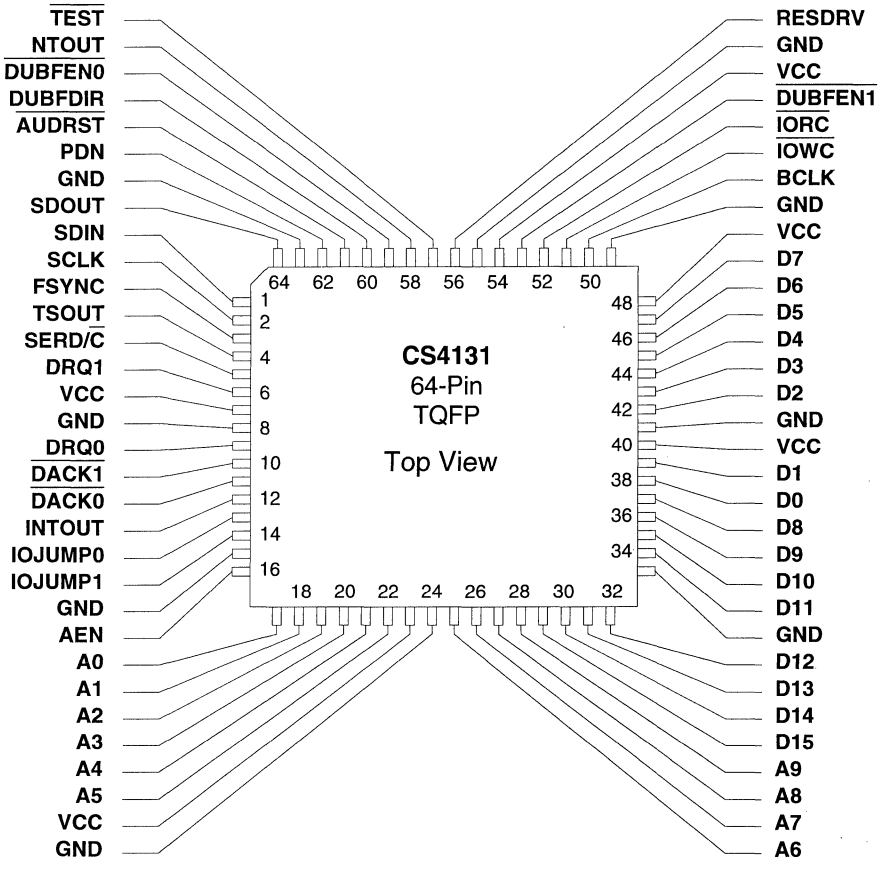
The Loopback Mode

The CS4131 loopback mode is a useful tool for diagnostics. When XAUDRST is active, the shift register output is looped around to its input. After a full frame send, the data written to the TIMESLOT registers can be read back at the same addresses. When in loopback mode, FSYNC must be generated via the FSYNCBIT for a loopback operation. An internal-only version of TSOUT is generated by the CS4131, so the RCVD TSOUT bit may be used to determine when the frame shift operation is complete. Alternatively, a wait after sending FSYNC of about 100 µs may be used.

PIN DESCRIPTIONS



PIN DESCRIPTIONS



Serial Interface Pins

FSYNC - Frame Sync, Pin 13(L), 3(Q)
Frame Synchronization Signal. 4mA CMOS I/O.

SDOUT - Serial Data Output, Pin 10(L), 20(Q)
Serial data out to CS4215. 4mA CMOS Output.

SDIN - Serial Data In, Pin 11(L), 1(Q)
Serial data in from CS4215. CMOS Input, Weak Pull Up.

SCLK - Serial Clock, Pin 12(L), 2(Q)
Serial Clock Signal. 4mA CMOS I/O.

PDN - Power Down, Pin 8(L), 18(Q)
4mA CMOS Output.

SERD/$\overline{C}$ - Serial Data/Control, Pin 15(L), 5(Q)
Serial data/control word indicator. 4mA CMOS Output.

TSOUT - Timeslot Out, Pin 14(L), 4(Q)
End of frame indicator from CS4215. CMOS Input, Weak Pull Down.

$\overline{AUDRST}$ - Pin 7(L), 61(Q)
Reset for CS4215. 4mA CMOS Output

ISA Bus Control

DRQ1 - DMA Channel 1 Request, Pin 16(L), 6(Q)
12mA TTL Output.

DRQ0 - DMA Channel 0 Request, Pin 19(L), 9(Q)
12mA TTL Output.

$\overline{DACK1}$ - DMA Channel 1 Acknowledge, Pin 20(L), 10(Q)
Schmitt TTL Input.

$\overline{DACK0}$ - DMA Channel 0 Acknowledge, Pin 21(L), 11(Q)
Schmitt TTL Input

INTOUT - Interrupt Out, Pin 22(L), 12(Q)
12mA TTL Output.

$\overline{IORC}$ - Pin 64(L), 52(Q)
ISA I/O read signal used for CPU-driven I/O and DMA operations. Schmitt TTL Input.

$\overline{IOWC}$ - Pin 63(L), 51(Q)
ISA I/O write signal used for CPU-driven I/O and DMA operations. Schmitt TTL Input.

AEN - Pin 27(L), 16(Q)
Address can be decoded from address bus when low. TTL Input.

ISA Clock and Reset

BCLK - Bus Clock, Pin 61(L), 50(Q)
Schmitt TTL Input.

RESDRV - ISA Bus Reset Signal, Pin 2(L), 56(Q)
Schmitt TTL Input.

A4 - A9 - Address Lines Used for Decode Register Block, Pins [32, 33, 36 - 39(L)] [21, 22, 25-28(Q)]

TTL Inputs.

A0 - A3 - Address Lines Used for Register Selection, Pins [28 - 31(L)] [17-20(Q)]

TTL Inputs.

D0 - D15 - Parallel Data Bus Bits, Pins [49, 50, 53-58, 48 - 45, 43 - 40(L)] [38, 39, 42-47, 37-34, 32-29(Q)]

12mA TTL I/O.

IOJUMP1 - I/O Jumper 1, Pin 24(L), 14(Q)

Jumper to determine I/O base address. CMOS Input, Weak Pull Up.

IOJUMP0 - I/O Jumper 0, Pin 23(L), 13(Q)

Jumper to determine I/O base address. CMOS Input, Weak Pull Up.

External Buffer Control

$\overline{\text{DBUFEN0}}$ - Data Buffer Enable 0 Pin 5(L), 59(Q)

Enable for external '245 type data buffer that may connect low order byte of ISA and CS4131 data buses. 8mA TTL Output.

$\overline{\text{DBUFEN1}}$ - Data Buffer Enable 1, Pin 65(L), 53(Q)

Enable for external '245 type data buffer that may connect high order byte of ISA and CS4131 data buses. 8mA TTL Output.

DBUFDIR - Data Buffer Direction, Pin 6(L), 60(Q)

Direction control for both '245 type data buffers that may connect ISA and CS4131 data buses. 8mA TTL Output.

Power and Ground Pins

VCC - Digital Power Supply, Pins [17, 34, 51, 59, 68(L)] [7, 23, 40, 48, 54(Q)]

GND - Digital Ground, Pins [1, 9, 18, 26, 35, 44, 52, 60(L)] [55, 63, 8, 15, 24, 33, 41, 49(Q)]

Miscellaneous

$\overline{\text{TEST}}$ - Pin 3(L), 57(Q)

Tristates all outputs except NTOUT for test purposes. CMOS input, Weak Pull Up.

NTOUT - NAND Tree Output, Pin 4(L), 58(Q)

2mA CMOS Output.

RSVD1, 2, 4, 5 - Pins 25, 62, 66, 67(L)

Reserved

Semiconductor Corporation

CS4215

16-Bit Multimedia Audio Codec

Features

- Sample Frequencies from 4 kHz to 50 kHz
- 16-bit Linear, 8-bit Linear, μ-Law, or A-Law Audio Data Coding
- Programmable Gain for Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Level Analog Inputs
- Headphone, Speaker, and Line Outputs
- On-chip Anti-Aliasing/Smoothing Filters
- Serial Digital Interface

General Description

mwave The CS4215 is an Mwave™ audio codec.

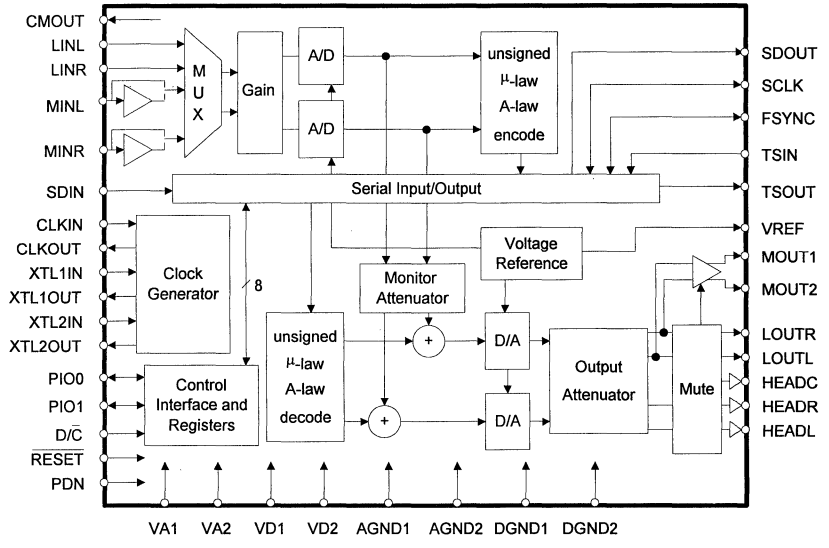
The CS4215 is a single-chip, stereo, CMOS multimedia codec that supports CD-quality music, FM radio-quality music, telephone-quality speech, and modems. The analog-to-digital and digital-to-analog converters are 64×oversampled delta-sigma converters with on-chip filters which adapt to the sample frequency selected.

The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker driver, results in a very small footprint.

Ordering Information:

CS4215-KL	0°C to 70°C	44-pin PLCC
CS4215-KQ	0°C to 70°C	100-pin TQFP
CDB4215	Evaluation Board	



This data sheet was written for Revision E CS4215 codecs and later. For differences between Revision E and previous versions, see *Appendix A*.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2; Full Scale Input Sine wave, No Gain, No Attenuation 1 kHz; Conversion Rate = 48 kHz; No Gain, No Attenuation, SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Slave mode; Unless otherwise specified.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution			16	-	-	Bits
ADC Differential Nonlinearity			-	-	±0.9	LSB
Instantaneous Dynamic Range	Line Inputs Mic Inputs	IDR	80 72	84 78	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	- -	- -	0.012 0.032	% %
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs		- -	80 60	- -	dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Frequency Response (Note 1)	(0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Input Gain	Line Inputs Mic Inputs		-0.2 19.8	- -	23.5 44	dB dB
Gain Step Size			-	1.5	-	dB
Absolute Gain Step Error			-	-	0.75	dB
Offset Error with HPF = 0 (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	±150 ±10 ±400	±400 ±150 -	LSB
Offset Error with HPF = 1 (Notes 1,2) (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	0 0 0	±5 ±5 ±5	LSB
Full Scale Input Voltage:	(MLB=0) Mic Inputs (MLB=1) Mic Inputs Line Inputs		0.250 2.50 2.50	0.28 2.8 2.8	0.310 3.10 3.10	Vpp V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 3)		20	-	-	kΩ
Input Capacitance			-	-	15	pF
CMOUT Output Voltage (Maximum output current = 400 µA)	(Note 4)		1.9	2.1	2.3	V

Notes:
1. This specification is guaranteed by characterization, not production testing.
2. Very low frequency signals will be slightly distorted when using the HPF.
3. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance.
4. DC current only. If dynamic loading exists, then CMOUT must be buffered or the performance of ADC's and DAC's may be degraded.

* Parameter definitions are given at the end of this data sheet.

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ANALOG CHARACTERISTICS (Continued)

Parameter *			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity				-	-	±0.9	LSB
Total Dynamic Range			TDR	-	95	-	dB
Instantaneous Dynamic Range (OLB = 1)	(All Outputs)		IDR	80	85	-	dB
Total Harmonic Distortion (OLB = 1)	Line Out	(Note 5)	THD	-	-	0.025	%
	Headphone Out	(Note 6)		-	-	0.2	%
	Speaker Out	(Note 6)		-	-	0.32	%
Interchannel Isolation	Line Out	(Note 5)		-	80	-	dB
	Headphone Out	(Note 6)		-	40	-	dB
Interchannel Gain Mismatch	Line Out			-	-	0.5	dB
	Headphone			-	-	0.5	dB
Frequency Response (Note 1)	(0 to 0.45 Fs)			-0.5	-	+0.2	dB
Programmable Attenuation	(All Outputs)			0.2	-	-94.7	dB
Attenuation Step Size				-	1.5	-	dB
Absolute Attenuation Step Error				-	-	0.75	dB
Offset Voltage	Line Out			-	10	-	mV
Full Scale Output Voltage with OLB = 0	Line Output	(Note 5)		2.55	2.8	3.08	V_{pp}
	Headphone Output	(Note 6)		3.6	4.0	4.4	V_{pp}
	Speaker Output-Differential	(Note 6)		7.3	8.0	8.8	V_{pp}
Full Scale Output Voltage with OLB = 1	Line Output	(Note 5)		1.8	2.0	2.2	V_{pp}
	Headphone Output	(Note 6)		1.8	2.0	2.2	V_{pp}
	Speaker Output-Differential	(Note 6)		3.6	4.0	4.4	V_{pp}
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase				-	-	1	Degree
Out of Band Energy	(22 kHz to 100 kHz)	Line Out		-	-60	-	dB
Power Supply							
Power Supply Current (Note 7)	Operating			-	110	140	mA
	Power Down			-	0.5	2	mA
Power Supply Rejection	(1 kHz)			-	40	-	dB

Notes: 5. 10 kΩ, 100 pF load. Headphone and Speaker outputs disabled.
6. 48 Ω, 100 pF load. For the headphone outputs, THD with 10kΩ, 100pF load is 0.02%.
7. Typically, 50% of the power supply current is supplied to the analog power pins (VA1, VA2) and 50% is supplied to the digital power pins (VD1, VD2). Values given are for unloaded outputs.

A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	s

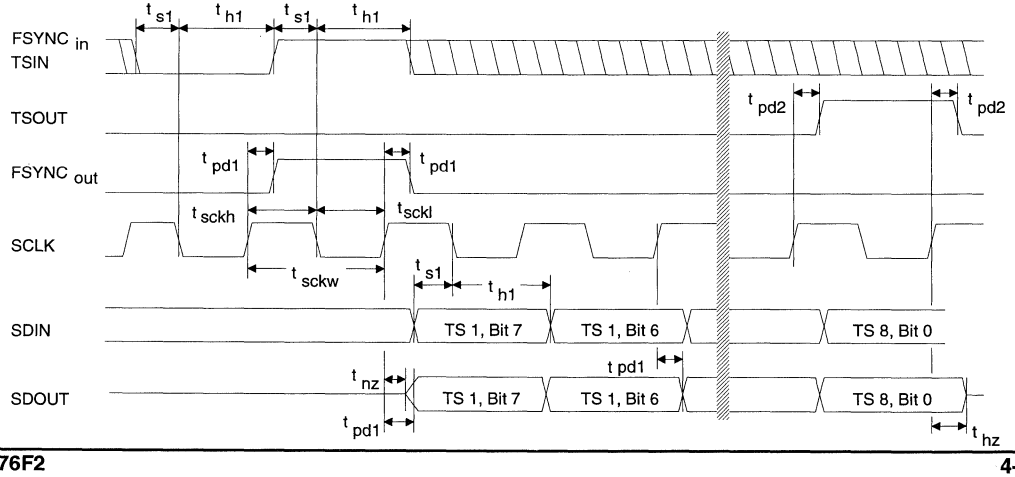
DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = 5V)

Parameter	Symbol	Min	Max	Units
High-level Input Voltage	V_{IH}	(VD1,VD2)-1.0	(VD1,VD2)+0.3	V
Low-level Input Voltage	V_{IL}	-0.3	1.0	V
High-level Output Voltage at I_O = -2.0 mA	V_{OH}	(VD1,VD2)-0.2	-	V
Low-level Output Voltage at I_O = 2.0 mA	V_{OL}	-	0.1	V
Input Leakage Current (Digital Inputs)		-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	10	µA

SWITCHING CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2)

Parameter		Symbol	Min	Typ	Max	Units
SCLK period	Master Mode, XCLK = 1 (Note 8)	t_{sckw}	-	1/(Fs*bpf)	-	s
	Slave Mode (XCLK = 0)	tsckw	80	-	-	ns
SCLK high time	Slave Mode, XCLK = 0 (Note 9)	tsckh	25	-	-	ns
SCLK low time	Slave Mode, XCLK = 0 (Note 9)	tsckl	25	-	-	ns
Input Setup Time		t_{s1}	15	-	-	ns
Input Hold Time		t_{h1}	10	-	-	ns
Input Transition Time	10% to 90% points		-	-	10	ns
Output delay		tpd1	-	-	28	ns
SCLK to TSOUT		tpd2	-	-	30	ns
Output to Hi-Z state	Timeslot 8, bit 0	t_{hz}	-	-	12	ns
Output to non-Hi-Z	Timeslot 1, bit 7	t_{nz}	15	-	-	ns
Input Clock Frequency	Crystals		-	-	27	MHz
	CLKIN (Note 10)		1.024	-	13.5	MHz
Input Clock (CLKIN) low time			30	-	-	ns
Input Clock (CLKIN) high time			30	-	-	ns
Sample rate		Fs	4	-	50	kHz
RESET low time	(Note 11)		500	-	-	ns

Notes:
8. In Master mode with BSEL1,0 set to 64 or 128 bits per frame (bpf), the SCLK duty cycle is 50%. When BSEL1,0 is set to 256 bpf, SCLK will have the same duty cycle as CLKOUT. See Internal Clock Generation section.
9. In Slave mode, FSYNC and SCLK must be derived from the master clock running the codec (CLKIN, XTAL1, XTAL2).
10. Sample rate specifications must not be exceeded.
11. After powering up the CS4215, RESET should be held low for 50 ms to allow the voltage reference to settle.



ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

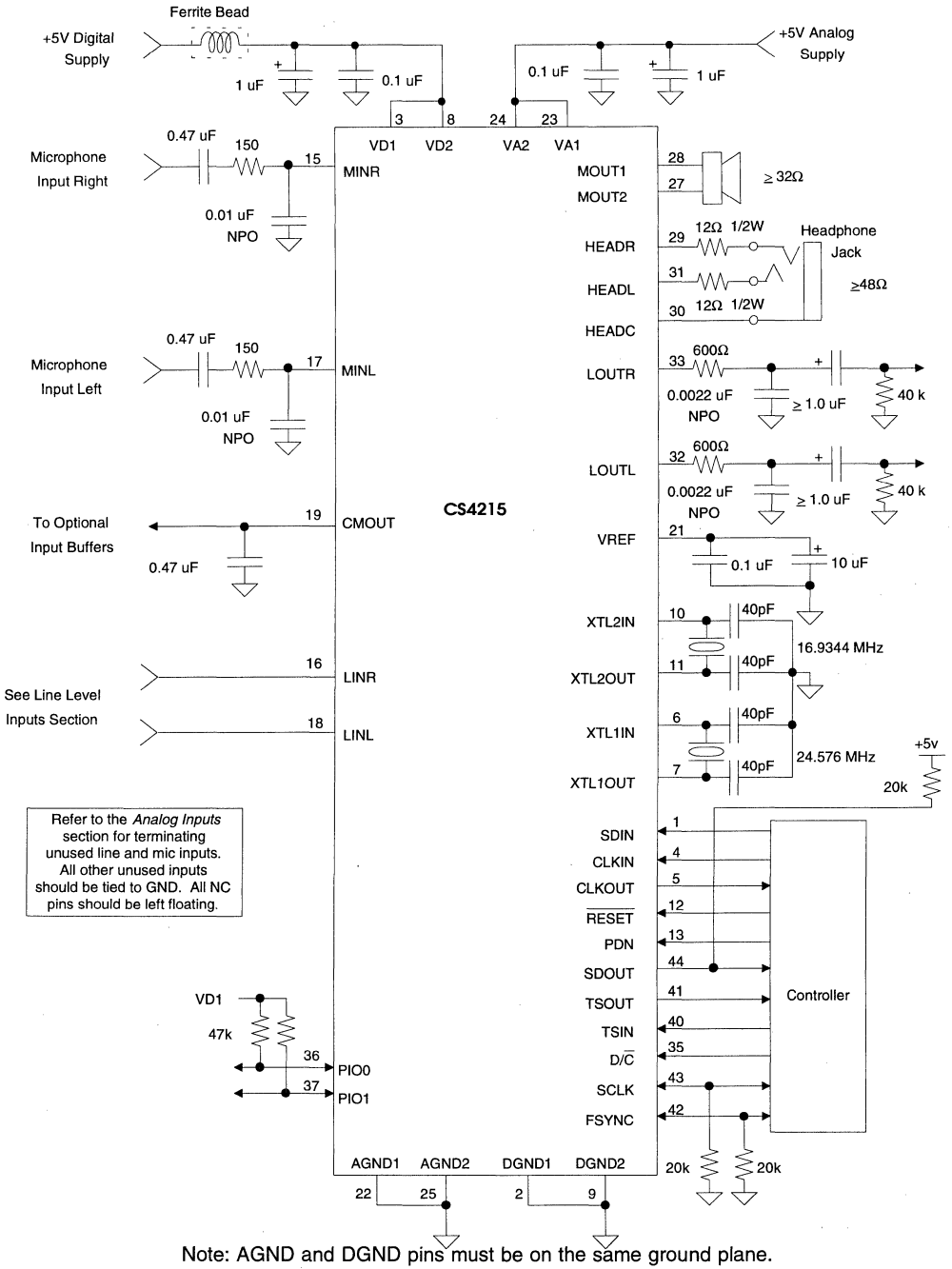
Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1,VD2 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current	(Except Supply Pins)		-	±10.0	mA
Analog Input Voltage			-0.3	(VA1, VA2)+0.3	V
Digital Input Voltage			-0.3	(VD1, VD2)+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital (Note 8) Analog (Note 8)	VD1,VD2 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	25	70	°C

Note: 8. |VD - VA| must be less than 0.5 Volts (one diode drop).



Note: AGND and DGND pins must be on the same ground plane.

Figure 1. Recommended Connection Diagram

FUNCTIONAL DESCRIPTION

Overview

The CS4215 has two channels of 16-bit analog-to-digital conversion and two channels of 16-bit digital-to-analog conversion. Both the ADCs and the DACs are delta-sigma converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. Special features include a separate microphone input with a 20 dB programmable gain block, an optional 8-bit μ-law or A-law encoder/decoder, pins for two crystals to set alternative sample rates, direct headphone drive and mono speaker drive.

Control for the functions available on the CS4215, as well as the audio data, are communicated to the device over a serial interface. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Data must be continually written for proper operation. Multiple CS4215 devices may be attached to the same data lines.

Analog Inputs

Figure 1, the recommended connection diagram, shows examples of the external analog circuitry recommended around the CS4215. An internal multiplexer selects between line level inputs and microphone level inputs.

Input filters using a 150 Ω resistor and a .01 μF NPO capacitor to ground are required to isolate the input op-amps from, and provide a charge reserve for, the switched-capacitor input of the codec. The RC values may be safely changed by a factor of two.

The HPF bit in Control Time Slot 2 provides a high pass filter that will reduce DC offset on the analog inputs. Using the high pass filter will cause slight distortions at very low frequencies.

Unused analog inputs that are not selected have a very high input impedance, so they may be tied to AGND directly. Unused analog inputs that are selected should be tied to AGND through a 0.1uF capacitor. This prevents any DC current flow.

Line Level Inputs

LINL and LINR are the line level input pins. These pins are internally biased to the CMOUT voltage. Figure 2 shows a dual op-amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 V_{rms} to

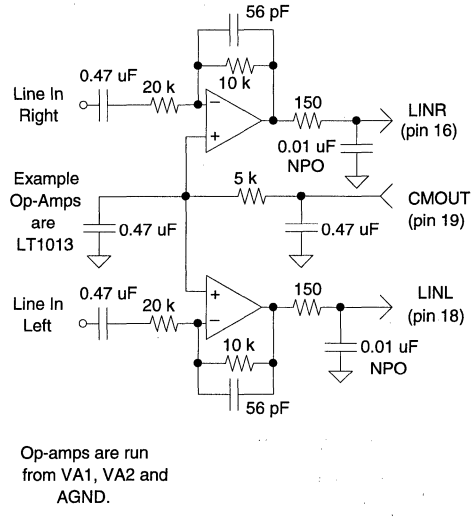


Figure 2. DC Coupled Input.

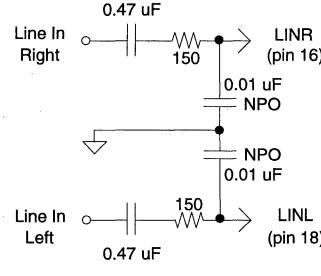


Figure 3. AC Coupled Input.

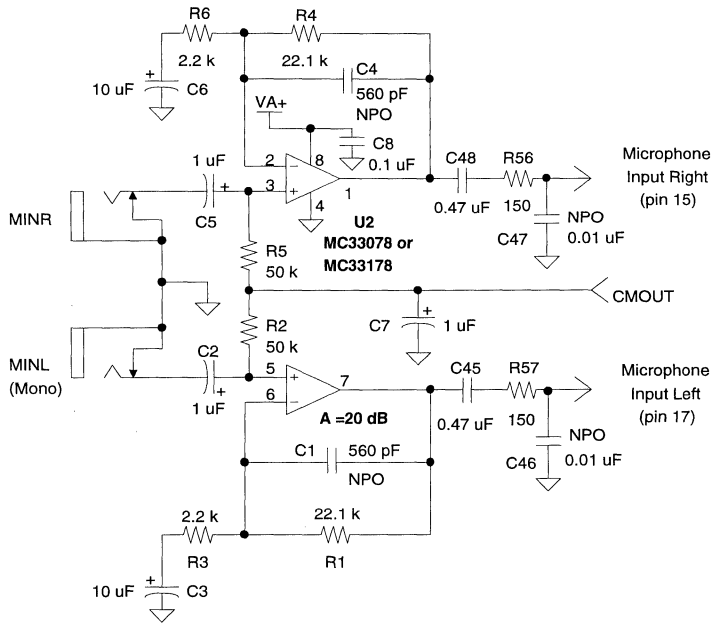


Figure 4. Optional Microphone Input Buffer

1 V_{rms}. The CMOUT reference level is used to level shift the signal. This level shifting allows the line inputs to be DC coupled into the CS4215. Minimum ADC offset results when the line inputs are DC coupled (see Analog Characteristics Table).

Figure 3 shows an AC coupled input circuit for signals centered around 0 Volts. The anti-aliasing RC filter presents a low impedance at high frequencies and should be driven by a low impedance source.

Microphone Level Inputs

Internal amplifiers with a programmable 20 dB gain block are provided for the microphone level inputs, MINR and MINL. Figure 4 shows a single-ended input microphone pre-amplifier stage with a gain of 23 dB. AC coupling is mandatory for these inputs since any DC offset on the input will be amplified by the codec.

The 20 dB gain block may be disabled using the MLB bit in Control Time Slot 1. When disabled, the inputs become line level with full scale inputs of 1 Vrms.

Adjustable Input Gain

The signals from the microphone or the line inputs are routed to a programmable gain circuit which provides up to 22.5 dB of gain in 1.5 dB steps. Level changes only take effect on zero crossings to minimize audible artifacts, often referred to as "zipper noise". The requested level change is forced if no zero crossing is found after 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Analog Outputs

The analog outputs of the DACs are routed via an attenuator to a pair of line outputs, a pair of

headphone outputs and a mono monitor speaker output.

Output Level Attenuator

The DAC outputs are routed through an attenuator, which provides 0 dB to 94.5 dB of attenuation, adjustable in 1.5 dB steps. Level changes are implemented using both analog and digital attenuation techniques. Level changes only take effect on zero crossings to minimize audible artifacts. The requested level change is forced if an analog zero crossing does not occur within 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Line Outputs

LOUTR and LOUTL output an analog signal, centered around the CMOUT voltage. The minimum recommended load impedance is 8 kΩ. Figure 1 shows the recommended 1.0 µF DC blocking capacitor with a 40 kΩ resistor to ground. When driving impedances greater than 10 kΩ, this provides a high pass corner of 20 Hz. These outputs may be muted.

Headphone Outputs

HEADR and HEADL output an analog signal, centered around the HEADC voltage. The default headphone output level (OLB = 0) contains an optional 3 dB gain over the line outputs which provides reasonable listening levels, even with small amplitude digital sources. These outputs have increased current drive capability and can drive a load impedance as low as 48 Ω. External 12 Ω series resistors reduce output level variations with different impedance headphones. The common return line from driving headphones should be connected to HEADC, which is biased to the CMOUT voltage. This removes the need for AC coupling, and also controls where the return currents flow. All three headphone output lines are short-circuit protected. These outputs may be muted.

Speaker Output

MOUT1 and MOUT2 differentially drive a small loudspeaker, whose impedance should be greater than 32 Ω. The signal is a summed version of the right and left line output, tapped off prior to the mute function, but after the attenuator. The speaker output may be independently muted. With OLB = 0, the speaker output also contains a 3 dB gain over the line outputs. When OLB = 1, the speaker outputs are driven at the same level as the line outputs.

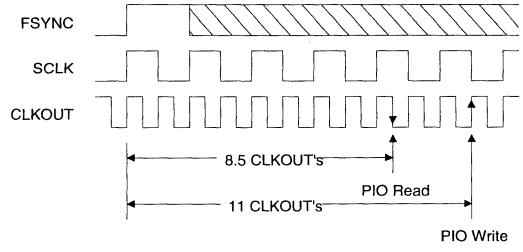
Some small speakers distort heavily when presented with low frequency energy. A high-pass filter helps eliminate the low frequency energy and can be implemented by AC coupling both speaker terminals with a resistor to ground, on the speaker side of the DC blocking capacitors. The values selected would depend on the speaker chosen, but typical values would be 22 µF for the capacitors, with the positive side connected to the codec, and 50 kΩ resistors. This circuit is contained on the CDB4215 evaluation board as shown in the end of this data sheet.

Input Monitor Function

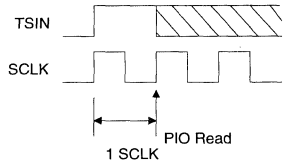
To allow monitoring of the input audio signal, the output of the ADCs can be routed through a monitor path attenuator, then digitally mixed into the input data for the DACs (see the front page block diagram). Changes in the input gain or output level settings directly affect the monitor level. If full scale data from the ADCs is added to full scale digital data from the serial interface, clipping will occur.

Calibration

Both output offset voltage and input offset error are minimized by an internal calibration cycle.



Data Mode -Read and Write



Control Mode - Read Only

Notes:
1. DATA MODE READ - The data is sent out via SDOUT on the next frame.
2. CONTROL MODE READ - The data is sent out, via SDOUT, the same frame.
3. DATA MODE READ, WRITE - are tied to the rising edge of FSYNC and CLKOUT. They are independent of SCLK.
4. CONTROL MODE READ - The PIO pins are sampled by a rising edge of SCLK.

Figure 5. PIO Pin Timing

At least one calibration cycle must be invoked after power up. A calibration cycle will occur immediately after leaving the reset state. A calibration cycle will also occur immediately after going from control mode to data mode (D/$\overline{C}$ going high). When powering up the CS4215, or exiting the power down state, a minimum of 50 ms must occur, to allow the voltage reference to settle, before initiating a calibration cycle. This is achieved by holding $\overline{\text{RESET}}$ low or staying in control mode for 50 ms after power up or exiting power down mode. The input offset error will be calibrated for whichever input channel is selected (microphone or line, using the IS bit). Therefore, the IS bit should remain steady while the codec is calibrating, although the other bits input to the codec are ignored. Calibration takes 194 FSYNC cycles and SDOUT data bits will be zero during this period. The A/D Invalid bit, ADI (bit 7 in data time slot 6), will be high during calibration and will go low when calibration is finished.

Parallel Input/Output

Two pins are provided for parallel input/output. These pins are open drain outputs and require external pull-up resistors. Writing a zero turns on the output transistor, pulling the pin to ground; writing a one turns off the output transistor, which allows an external resistor to pull the pin high. When used as an input, a one must be written to the pin, thereby allowing an external device to pull it low or leave it high. These pins can be read in control mode and their state is recorded in Control Register 5. These pins can be written to and read back in data mode using Data Register 7. Figure 5 shows the Parallel Input/Output timing.

Clock Generation

The master clock operating the CS4215 may be generated using the on-chip crystal oscillators, or by using an external clock source. In all data modes SCLK and FSYNC must be synchronous to the selected master clock.

If the master clock source stops, the digital filters will power down after 5 µs to prevent overheating. If FSYNC stops, the digital filters will power down after approximately 1 FSYNC period. The CS4215 will not enter the total power down state.

Internal Clock Generation

Two external crystals may be attached to the XTL1IN, XTL1OUT, XTL2IN and XTL2OUT pins. Use of an external crystal requires additional 40 pF loading capacitors to digital ground (see Figure 1). XTAL1 oscillator is intended for use at 24.576 MHz and XTAL2 oscillator is intended for use at 16.9344 MHz, although other frequencies may be used. The gain of the internal inverter is slightly higher for XTAL1, ensuring proper operation at >24 MHz frequencies. The crystals should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to a 40 pF capacitor on each leg). If XTAL1 or XTAL2 is not selected as the master clock, that particular crystal oscillator is powered down to minimize interference. If a crystal is not needed, the XTL-IN pin should be grounded. An example crystal supplier is CAL Crystal, telephone number (714) 991-1580.

FSYNC and SCLK must be synchronous to the master clock. When using the codec in slave mode with one of the crystals as master clock, the controller must derive FSYNC and SCLK from the crystals, i.e. via CLKOUT. Note that CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low.

An internally generated clock which is 256 times the sample rate (FSYNC rate) is output (CLKOUT) for potential use with an external AES/EBU transmitter, or another CS4215. No glitch occurs on CLKOUT when selecting alternate clock sources. CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low, assuming one of the crystal oscillators is selected, or either CLKIN or SCLK is the master clock source and is continuous. The duty cycle of CLKOUT is 50% if the master clock is one of the crystal oscillators and the DFR bits are 0, 1, 2, 6 or 7. If the DFR bits are 3 or 5, the duty cycle is 33% (high time). If the DFR bits are 4 then CLKOUT has the timing shown in Figure 6. If the master clock is SCLK or CLKIN, the duty cycle of CLKOUT will be the same as the master clock source.

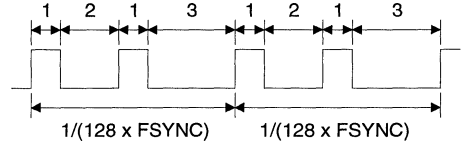


Figure 6. CLKOUT duty cycle using the on-chip crystal oscillator when DFR = 4 (typically FSYNC = 37.8 kHz)

External Clock

An external clock input pin (CLKIN) is provided for potential use with an external AES/EBU receiver, or an already existing system clock. When MCK2 = 0, the input clock must be exactly 256 times the sample rate, and FSYNC and SCLK must be synchronous to CLKIN. When MCK2 = 1 the DFR bits allow various divide ratios off the CLKIN frequency.

Alternatively, an external high frequency clock may be driven into XTL1IN or XTL2IN. The correct clock source must be selected using the MCK bits. Manipulating DFR bits will allow various divide ratios from the clock to be se-

lected. SCLK and FSYNC must be synchronous to the external clock.

As a third alternative, SCLK may be programmed to be the master clock input. In this case, it must be 256 times Fs.

Serial Interface

The serial interface of the CS4215 transfers digital audio data and control data into and out of the device. Multiple CS4215 devices may share the same data lines. DSP's supported include the Motorola 56001 in network mode and a subset of the 'CHI' bus from AT&T/Intel.

Serial Interface Signals

Figure 7 shows an example of two CS4215 devices connected to a common controller. The Serial Data Out (SDOUT) and Serial Data In (SDIN) lines are time division multiplexed between the CS4215s.

The serial interface clock, SCLK, is used for transmitting and receiving data. SCLK can be generated by one of the CS4215s, or it can be input from an external SCLK source. When generated by an external source, SCLK must be synchronous to the master clock. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK. The SCLK frequency is always equal to the bit rate.

The Frame Synchronizing signal (FSYNC) is used to indicate the start of a frame. It may be output from one of the CS4215s, or it may be generated from an external controller. If FSYNC is generated externally, it must be high for at least 1 SCLK period, and it must fall at least 2 SCLKs before the start of a new frame (see Figure 8). It must also be synchronous to the master clock. The frequency of FSYNC is equal to the system sample rate (see Figure 8). Each CS4215 requires 64 SCLKs to transfer all the data. The SCLK frequency can be set to 64, 128, or 256 bits per frame, thereby allowing for 1, 2 or 4 CS4215s connected to the same bus.

In a typical multi-part scenario, one CS4215 (the master) would generate FSYNC and SCLK, while the other CS4215s (the slaves) would receive FSYNC and SCLK. The CLKOUT of the master would be connected to the CLKIN of each slave device as shown in Figure 7. Then, the master device would be programmed for the desired sample frequency (assuming one of the crystals is selected as the clock source), the number of bits per frame, and for SCLK and FSYNC to be outputs. The slave devices would be programmed to use CLKIN as the clock source, the same number of bits per frame, and for SCLK and FSYNC to be inputs. Since CLKOUT is al-

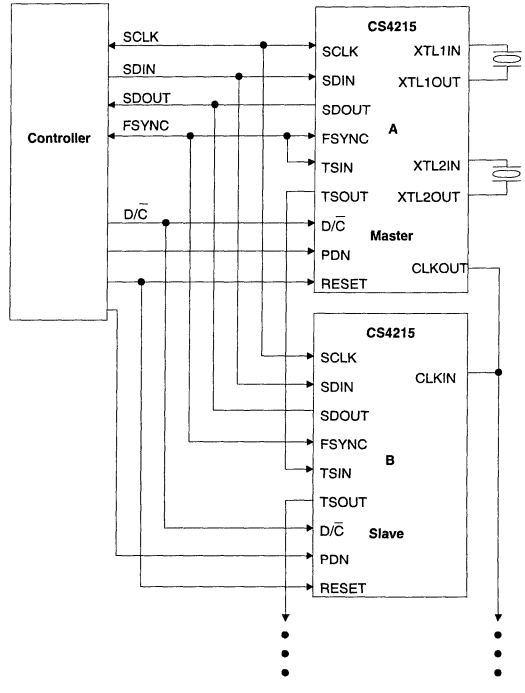


Figure 7. Multiple CS4215's

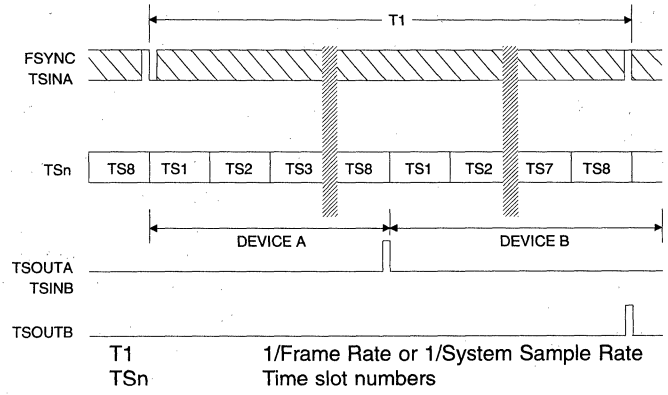


Figure 8. Serial Interface Timing for 2 CS4215's

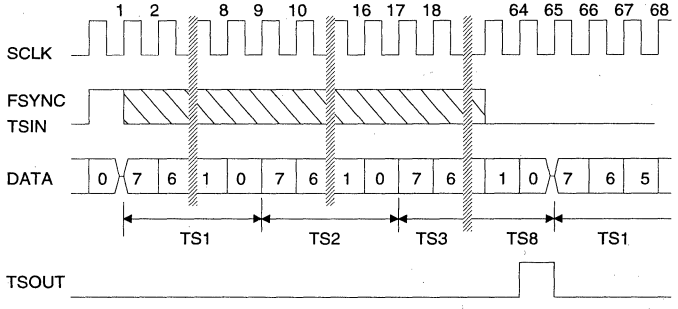


Figure 9. Frame Sync and Bit Offset Timing

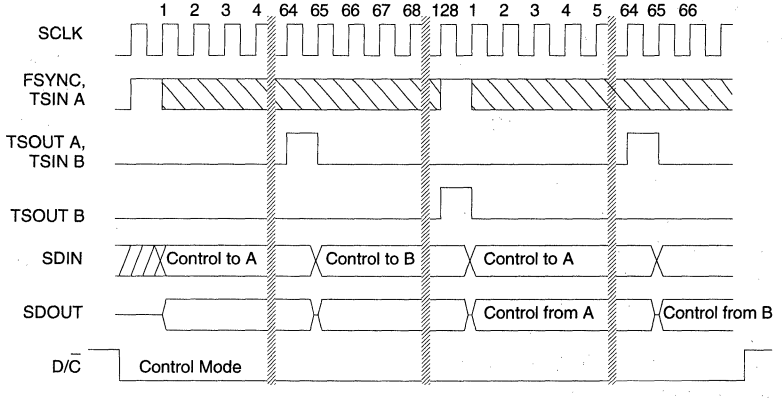


Figure 10. Control Mode Timing for 2 CS4215's

ways 256 times the sample frequency and scales with the selected sample frequency on the master, the slave devices will automatically scale with changes in the master codec's sample frequency.

CS4215s are time division multiplexed onto the bus using the Time Slot Out (TSOUT) and Time Slot In (TSIN) signals. TSOUT is an output signal that is high for one SCLK bit time, and indicates that the CS4215 is about to release the bus. TSIN is an input signal that informs the CS4215 that the next time slot is available for it to use. The first device in the chain uses FSYNC as its TSIN signal. All subsequent devices use the TSOUT of the previous device as its TSIN input. TSIN must be high for at least 1 SCLK period and fall at least 2 SCLKs before start of a new frame.

Serial Interface Operation

The serial interface format has a variable number of time slots, depending on the number of CS4215s attached to the bus. All time slots have 8 bits. Each CS4215 requires 8 time slots (64 bits) to communicate all data (see Figure 9).

CONTROL MODE

The Control Mode is used to set up the CS4215 for subsequent operation in Data Mode by loading the internal control registers. Control mode is asserted by bringing D/$\overline{C}$ low. If D/$\overline{C}$ is low during power up, then the CS4215 will enter control mode immediately. The SCLK and FSYNC pins are tri-stated, and the CS4215 will receive SCLK and FSYNC from an external source. If the CS4215 is in master mode (SCLK and FSYNC are outputs) and D/$\overline{C}$ is brought low, then SCLK & FSYNC will continue to be driven for a minimum of 4 and a maximum of 12 SCLKs, if the ITS bit = 0. If ITS is 1, SCLK and FSYNC will three-state immediately after D/$\overline{C}$ goes low. If D/$\overline{C}$ is brought low when the codec is programmed as master with ITS=0, the codec will timeout and release FSYNC and SCLK within 100µs. The values in the control registers for control of the serial ports are ignored in control mode. The data received on SDIN is stored into the control registers which have addresses matching their time slots. The data in the registers is transmitted on SDOUT with the time slot equal to the register number (see Figure 10).

The steps involved when going from data mode to control mode and back are shown in the flow chart in Figure 11.

Control Formats

The CS4215 control registers have the functions and time slot assignments shown in Table 1. The register address is the time slot number when D/$\overline{C}$ is 0. Reserved bits should be written as 0 and could be read back as 0 or 1. When comparing data read back, reserved bits should be masked. The SDOUT pin goes into a high-impedance state prior to Time Slot 1 and after Time Slot 8. The data listed below the register is its reset state.

The parallel port register is used to read and write the two open-drain input/output pins. The outputs are all set to 1 on RESET. PIO bits are read only in control mode. Note that, since PIO signals are open drain signals, an external device

Time slot	Description
1	Status
2	Data Format
3	Serial Port Control
4	Test
5	Parallel Port
6	RESERVED
7	Revision
8	RESERVED

Table 1. Control Registers

may drive them low even when they have been programmed as highs. Therefore, the value read back may differ from the value written. In the data mode, (D/$\overline{C}$=1), this register can be read and written to through the serial port as part of the Input Settings Registers. In control mode, (D/$\overline{C}$=0) these bits can only be read.

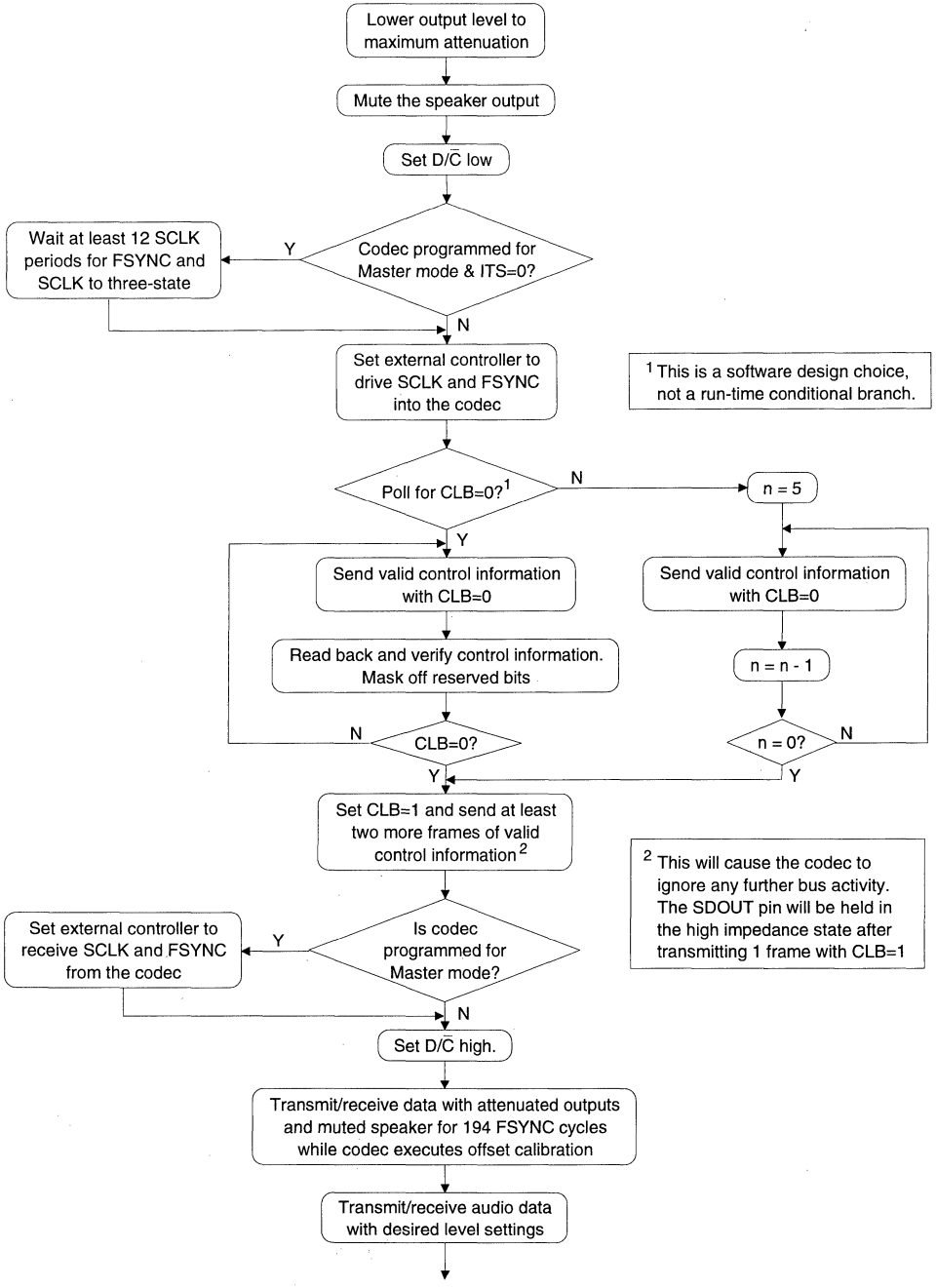


Figure 11. Control Mode Flow Chart

Control Time Slot 1, Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**0**	**0**	**1**	**MLB**	**OLB**	**CLB**	**RSRV**	
Reset (R)	0	0	1	0	0	1	X	X

BIT	NAME	VALUE		FUNCTION
RSRV	Reserved Bits			Must be written as 0.
CLB	Control Latch Bit	1	*R*	Ensures proper transition between control and data mode.
OLB	Output Level Bit	0	*R*	Line full scale outputs are 2.8 Vpp (1Vrms) Headphone full scale output is 4.0 Vpp. Speaker full scale output is 8.0 Vpp.
		1		Line and Headphone full scale outputs are 2.0 Vpp. Speaker full scale output is 4.0 Vpp.
MLB	Microphone Level	0	*R*	20 dB Fixed Gain Enabled Full scale microphone inputs are 0.288 Vpp.
		1		20 dB Fixed Gain Disabled Full scale inputs are 2.88 Vpp.

Control Time Slot 2, Data Format Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HPF**	**RSRV**	**DFR2**	**DFR1**	**DFR0**	**ST**	**DF1**	**DF0**
Reset (R)	0	X	0	0	0	0	0	1

BIT	NAME	VALUE			FUNCTION		
DF1-0	Data Format Selection	0 0	0		16-bit 2's-complement linear.		
		0 1	1	*R*	8-bit μ–Law.		
		1 0	2		8-bit A-Law.		
		1 1	3		8-bit unsigned linear.		
ST	Stereo Bit	0		*R*	Mono Mode.		
		1			Stereo Mode.		
DFR2-0	Data Conversion Frequency Selection				CLKIN (÷)	XTAL1(kHz) 24.576 MHz	XTAL2 (kHz) 16.9344 MHz
		0 0 0	0	*R*	3072	8	5.5125
		0 0 1	1		1536	16	11.025
		0 1 0	2		896	27.42857	18.9
		0 1 1	3		768	32	22.05
		1 0 0	4		448	NA	37.8
		1 0 1	5		384	NA	44.1
		1 1 0	6		512	48	33.075
		1 1 1	7		2560	9.6	6.615
RSRV	Reserved Bit				Must be written as 0		
HPF	High Pass Filter	0		*R*	Disabled.		
		1			Enabled. A Digital High Pass Filter is used to force the ADC DC offset to zero.		

Control Time Slot 3, Serial Port Control Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ITS**	**MCK2**	**MCK1**	**MCK0**	**BSEL1**	**BSEL0**	**XCLK**	**XEN**
Reset (R)	0	0	0	0	1	0	0	1

BIT	NAME	VALUE			FUNCTION
XEN	Transmitter Enable	0			Enable the serial data output.
		1		*R*	Disable (high-impedance state) serial data output.
XCLK	Transmit Clock	0		*R*	Receive SCLK and FSYNC from external source SLAVE Mode
		1			Generate SCLK and FSYNC MASTER Mode
BSEL1-0	Select Bit Rate	0 0	0		64 bits per frame.
		0 1	1		128 bits per frame.
		1 0	2	*R*	256 bits per frame.
		1 1	3		Reserved.
MCK2-0	Clock Source Select	0 0 0	0	*R*	SCLK is master clock, 256 bits per frame. BSEL must equal 2, and XCLK must equal 0.
		0 0 1	1		XTAL1, 24.576 MHz, is clock source.
		0 1 0	2		XTAL2, 16.9344 MHz, is clock source.
		0 1 1	3		CLKIN is clock source, and must be 256xFs.
		1 0 0	4		CLKIN is clock source, DFR2-0 select sample frequency.
ITS	Immediate Three-State	0		*R*	SCLK and FSYNC three-state up to 12 clocks after D/C goes low.
		1			SCLK and FSYNC three-state immediately after D/C goes low.

Control Time Slot 4, Test Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**TEST**						**ENL**	**DAD**
Reset (R)	0	0	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DAD	Loopback Mode	0	*R*	Digital-Digital Loopback.
		1		Digital-Analog-Digital Loopback.
ENL	Enable Loopback Testing	0	*R*	Disable.
		1		Enable.
TEST	Test bits			The TEST bits must be written as zero, otherwise special factory test modes may be invoked.

Control Time Slot 5, Parallel Port Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**RSRV**					
Reset (R)	1	1	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.
PIO1-0	Parallel I/O Bits	1 1 3 *R*	See the Parallel Input/Output Section.

Control Time Slot 6, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 7, Version Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**				**VER3**	**VER2**	**VER1**	**VER0**
Reset (R)	X	X	X	X	0	0	1	0

BIT	NAME	VALUE	FUNCTION
VER3-0	Device Version Number	0 0 0 0 0 0 0 0 1 1 0 0 1 0 2 *R*	"C". See *Appendix A.* "D". See *Appendix A.* "E". This Data Sheet
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 8, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

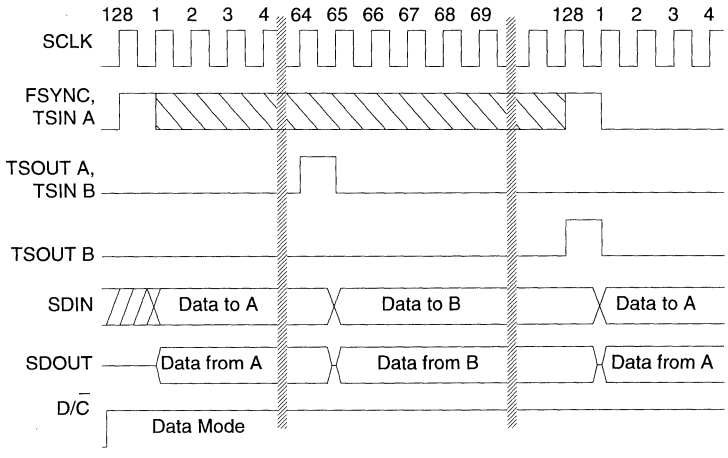


Figure 12. Data Mode Timing for 2 CS4215's

DATA MODE

The data mode is used during conversions to pass digital data between the CS4215 and external devices. The frame sync rate is equal to the value of the conversion frequency set by the DFR2-DFR0 bits of the Data Format register. Each frame has either 64, 128, or 256 bit times depending on the BSEL bits in the Serial Control register. Control of gain, attenuation, input selection and output muting are embedded in the data stream.

Time slot	Description
1	Left Audio MS8 bits
2	Left Audio LS8 bits
3	Right Audio MS8 bits
4	Right Audio LS8 bits
5	Output Setting
6	Output Setting
7	Input Setting
8	Input Setting

Table 2. Data Registers

Data Formats

All time slots contain 8 bits. The MSB of the data is transmitted/received first. The CS4215 data registers have the functions and time slot assignments shown in Table 2. The register address is the time slot number when D/$\overline{C}$ is 1. The SDOUT pin goes into a high-impedance state prior to time slot 1 and after Time Slot 8 (see Figure 12).

The CS4215 supports four audio data formats: 16-bit 2's-complement linear, 8-bit unsigned linear, 8-bit A-Law, and 8-bit μ-Law. Figure 13 illustrates the transfer characteristic for 16-bit and 8-bit linear formats. Note that a digital code

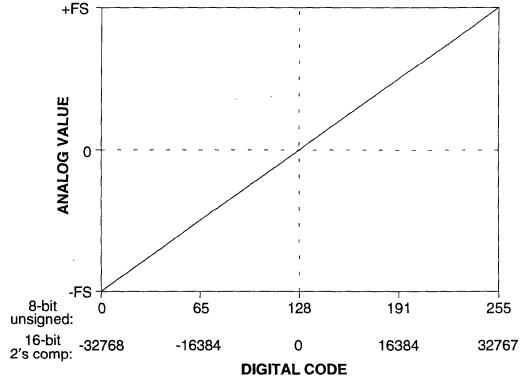


Figure 13. Linear Data Formats

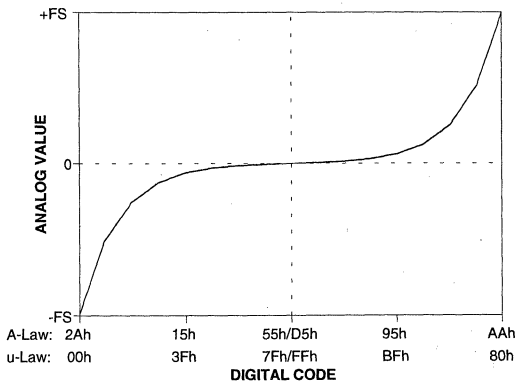


Figure 14. Companded Data Formats

of 128 (80 Hex) is considered analog zero for the 8-bit unsigned format.

A non-linear coding scheme is used for the companded formats as shown in Figure 14. This scheme is compatible with CCITT G.711. Companding uses more precision at lower amplitudes at the expense of less precision at higher amplitudes. μ-Law is equivalent to 13 bits at low signal levels and A-Law is equivalent to 12 bits. This low-level dynamic range is obtained at the expense of large-signal dynamic range which, for both μ-Law and A-Law, is equivalent to 6 bits. The CS4215 internally operates at 16 bits. The companded data is expanded to the upper 13 (12) bits for the DACs and compressed from the upper 13 (12) bits to 8 bits for the ADCs.

Data Time Slot 1&2, Left Channel Audio Data

Time slot 1 and 2 contain audio data for the left channel. In mono modes, only the left channel data is used, however both the right and left output DACs are driven. In 8-bit modes, only time slot 1 is used for the data.

Data Time Slot 3&4, Right Channel Audio Data

Time slot 3 and 4 contains audio data for the right channel. In mono modes, the right ADC outputs zero and the right DAC uses the left digital data. In 8-bit modes, only time slot 3 is used for the data.

Figure 15 summarizes all the time slot bit allocations for the 4 data modes and for control mode.

Reset

$\overline{\text{RESET}}$ going low causes all the internal control registers to be set to the states shown with each register description. $\overline{\text{RESET}}$ must be brought low and high at least once after power up. $\overline{\text{RESET}}$ returning high causes the CS4215 to execute an offset calibration cycle. $\overline{\text{RESET}}$ or D/$\overline{\text{C}}$ returning high should occur at least 50 ms after the power supply has stabilized to allow the voltage reference to settle.

Data Time Slot 5, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HE**	**LE**	**LO5**	**LO4**	**LO3**	**LO2**	**LO1**	**LO0**
Reset (R)	0	0	1	1	1	1	1	1

BIT	NAME	VALUE		FUNCTION
LO5-0	Left Channel Output Attenuation Setting	1 1 1 1 1 1 63	*R*	1.5dB attenuation steps. LO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB
LE	Line Output Enable	0 1	*R*	Analog line outputs off (muted). Analog line outputs on.
HE	Headphone Output Enable	0 1	*R*	Headphone output off (muted). Headphone output on.

Data Time Slot 6, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ADI**	**SE**	**RO5**	**RO4**	**RO3**	**RO2**	**RO1**	**RO0**
Reset (R)	1	0	1	1	1	1	1	1

BIT	NAME	VALUE		FUNCTION
RO5-0	Right Channel Output Attenuation Setting	1 1 1 1 1 1 63	*R*	1.5dB attenuation steps. RO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB Not used in mono modes.
SE	Speaker Enable	0 1	*R*	Speaker off (muted). Speaker on.
ADI	A/D Data Invalid	0 1	 *R*	A/D data valid. A/D data invalid. Busy in calibration.

Data Time Slot 7, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**OVR**	**IS**	**LG3**	**LG2**	**LG1**	**LG0**
Reset (R)	1	1	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
LG3-0	Left Channel Input Gain Setting	0 0 0 0	*R*	1.5dB gain steps. LG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
IS	Input Select	0 1	*R*	Line level inputs (LINL, LINR). Microphone level inputs (MINL, MINR).
OVR	Overrange	0	*R*	When read as 1, this bit indicates that an input over-range condition has occurred. The bit remains set until cleared by writing 0 into the register. Writing a 1 enables the overrange detection. The bit will remain 0 until an over-range occurs. Serial port clear has priority over internal settings.
PIO1-0	Parallel I/O	1 1 3	*R*	Parallel input/output bits.

Data Time Slot 8, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**MA3**	**MA2**	**MA1**	**MA0**	**RG3**	**RG2**	**RG1**	**RG0**
Reset (R)	1	1	1	1	0	0	0	0

BIT	NAME	VALUE		FUNCTION
RG3-0	Right Channel Input Gain Setting	0 0 0 0	*R*	1.5dB gain steps. RG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
MA3-0	Monitor Path Attenuation	1 1 1 1 15	*R*	6dB attenuation steps. MA3 is the MSB. 0 = no attenuation, 1111 = mute.

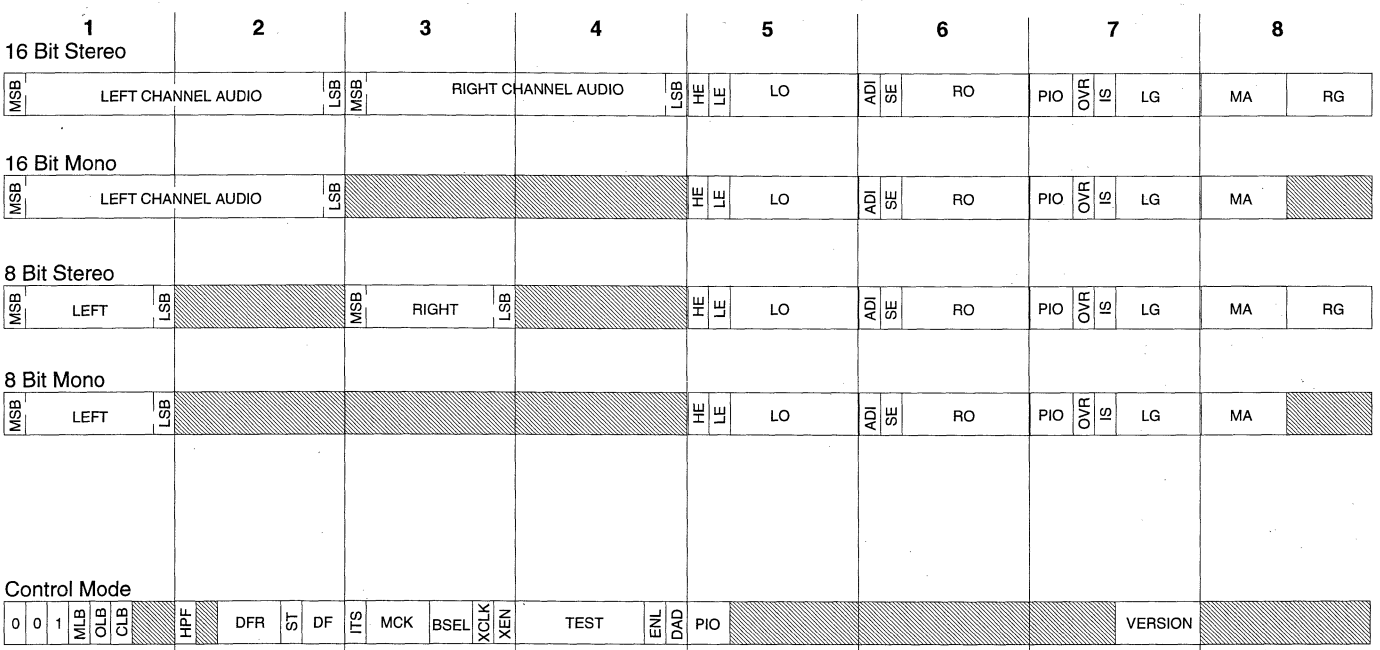


Figure 1 5. Time Slot/Register Overview

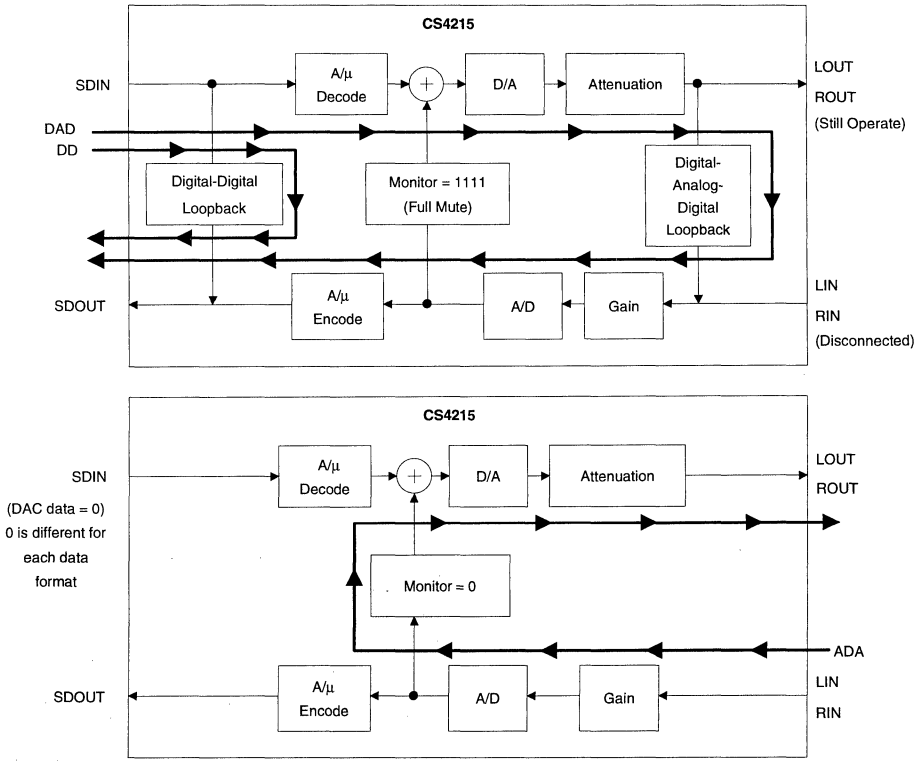


Figure 16. DD, DAD & ADA Loopback Paths

Power Down Mode

Bringing the PDN pin high puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down will change all the control registers to the reset state shown under each Control Time Slot register. In the power down mode, the TSOUT pin will follow the TSIN state with less than 10 ns delay.

After returning to normal operation from power down, an offset calibration cycle must be executed. Either bringing $\overline{\text{RESET}}$ low then high, or updating the control registers, will cause an offset calibration cycle. In either case, a delay of 50 ms must occur after PDN goes low before executing the offset calibration. This allows the internal voltage reference time to settle.

LOOPBACK TEST MODES

The CS4215 contains three loopback modes that may be used to test the codec. Two of the loopback test modes are designed to allow the host to perform a self-test on the CS4215. The third mode allows laboratory testing using external equipment.

Host Self-Test Loopback Modes

Since the CS4215 is a mixed-signal device, it is equipped with an internal register that will enable the host to perform a two-tiered test on power-up or as needed. The loopback test is enabled by setting the Enable Loopback bit, ENL, in control register 4. The first tier of loopback is a digital-digital loopback, DD, which is selected by clearing the DAD bit in control register 4

(see Figure 16). DD loopback checks the interface between the host and the CS4215 by taking the data on SDIN and looping it back onto SDOUT, with the data on SDOUT being one frame delayed from the data on SDIN. The host can verify that the data received is exactly the same as the data sent, thereby indicating the interface between the two devices and the digital interface on the CS4215 are operating properly. The output DAC's are functional in DD loopback. Now that the interface has been verified, the rest of the CS4215 can be tested using the second tier of loopback.

The second tier of loopback is a digital-analog-digital loopback, DAD, which is selected by setting the DAD bit in control register 4. DAD loopback checks the analog section of the CS4215 by connecting the right and left analog outputs, after the output attenuator, to the analog inputs of the gain stage. This allows testing of most of the CS4215 from the host by sending a known digital signal to the DACs and monitoring the digital signal from the ADCs. During DAD loopback, the monitor attenuator must be set at maximum (full mute), and the analog outputs may be individually muted. The analog inputs are disconnected internally. The flow of test data for both DD and DAD loopback modes is illustrated in the top portion of Figure 16.

Analog-to-Analog Loopback Mode

A third loopback mode is achieved by setting the monitor attenuator to zero attenuation and sending the DACs digital zero via SDIN. This loopback is termed analog-digital-analog, ADA, since the selected analog input will now appear on the enabled analog outputs. Since this test is controlled by external stimulus and the host is not involved (except to send the DACs zeros), it is generally considered a laboratory test as opposed to a self test. The bottom portion of Figure 16 illustrates the ADA signal flow through the CS4215. Note that this test requires the host send analog zeros to the DAC. Each data format has a different code for zero. See Figures 13 and 14.

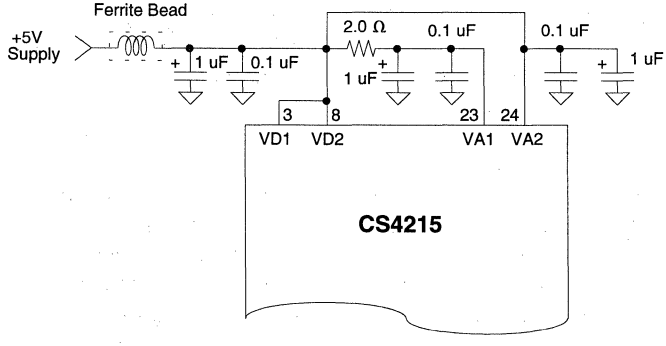
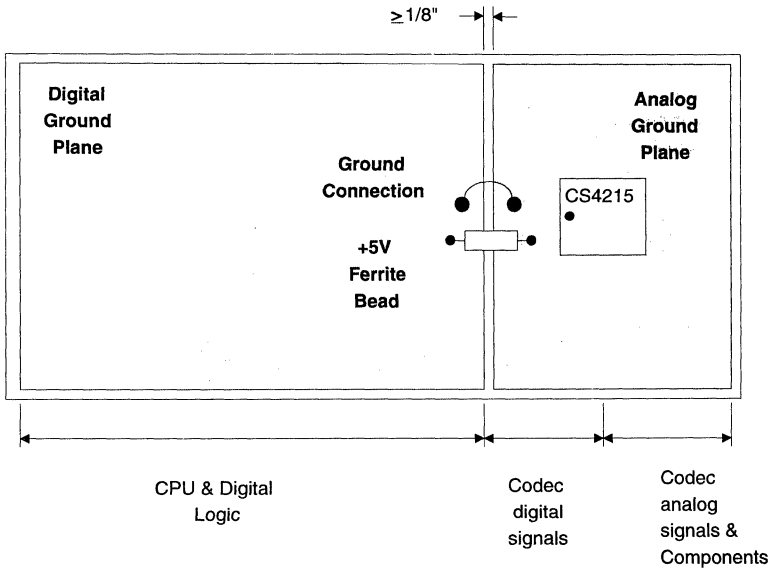


Figure 17. Optional Power Supply Arrangement



Note that the CS4215 is oriented with its digital pins towards the digital end of the board.

Figure 18. Suggested Layout Guideline

POWER SUPPLY AND GROUNDING

When using separate supplies, the digital power should be connected to the CS4215 via a ferrite bead, positioned closer than 1" to the device (see Figure 1). The codec VA1, VA2 pins should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 17. VA1 supplies analog power to the ADCs and DACs while VA2 supplies power to the output power drivers (headphones and speaker). The large currents necessary for VA2 are not flowing through the 2.0 Ω resistor, and therefore do not corrupt the VA1 converter supply.

The CS4215 along with associated analog circuitry, should be positioned near to the edge of the circuit board, and have its own, separate, ground plane. On the CS4215, the analog and digital grounds are internally connected; therefore, the four ground pins must be externally connected with zero impedance between ground pins. The best solution is to place the entire chip on a solid ground plane as shown in Figure 18. Preferably, it should also have its own power plane. A single connection between the CS4215 ground and the board ground should be positioned as shown in Figure 18.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4215 assuming a surface-mount socket and leaded decoupling capacitors. Surface-mount sockets are useful since the pad locations are exactly the same as the actual chip; therefore, given that space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts the top layer containing signal traces and assumes the bottom or inter-layer contains a solid analog ground plane. The important points with regards to this diagram are that the ground plane is SOLID under the codec and connects all codec ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is

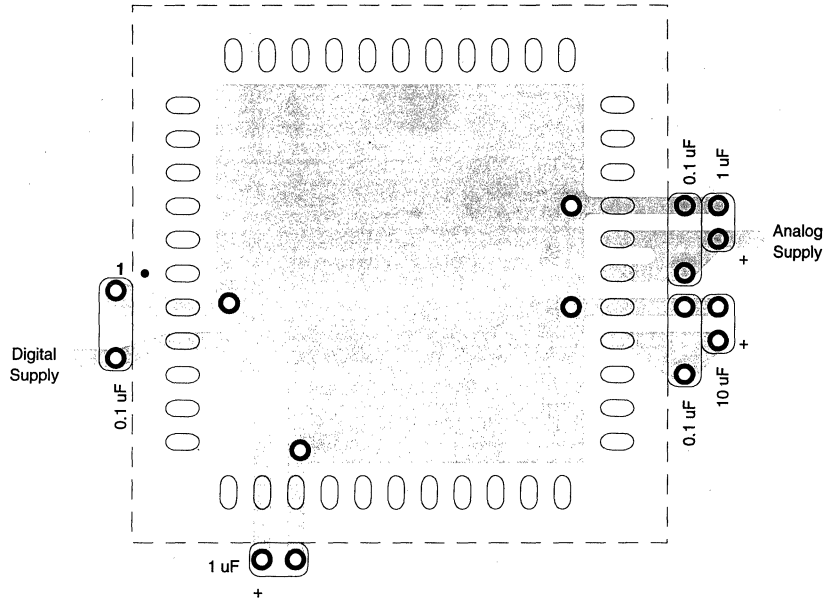


Figure 19. CS4215 Decoupling Layout Guideline

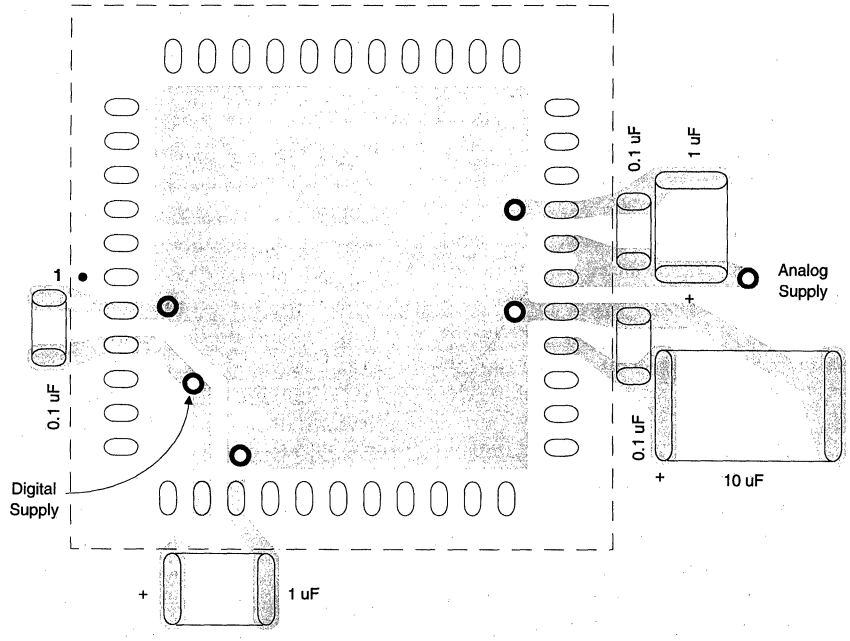


Figure 20. CS4215 Surface Mount Decoupling Layout

placed closest to the codec. Vias are placed near the AGND and DGND pins, under the IC, and should be attached to the solid analog ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces bringing the power to the codec should be wide thereby keeping the impedance low.

Although not shown in the figures, the trace layers (top layer in the figures) should have ground plane fill in-between the traces to minimize coupling into the analog section. See the CDB4215 evaluation board data sheet for an example layout.

If using all surface-mount components, the decoupling capacitors should still be placed on the layer with the codec and in the positions shown in Figure 20. The vias shown are assumed to attach to the appropriate power and analog ground layers. Traces bringing power to the codec should be as wide as possible to keep the impedance low. For the same reason, vias should be large for power and ground runs.

If using through-hole sockets, effort should be made to find a socket with the minimum height which will minimize the socket impedance. When using a through-hole socket, the vias under the codec in Figure 19 are not needed since the pins serve the same function.

ADC and DAC Filter Response Plots

Figures 21 through 27 show the overall frequency response, passband ripple and transition band for the CS4215 ADCs and DACs. Figure 27 shows the DACs' deviation from linear phase. Fs is the selected sample frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency. Fs is also the FSYNC frequency.

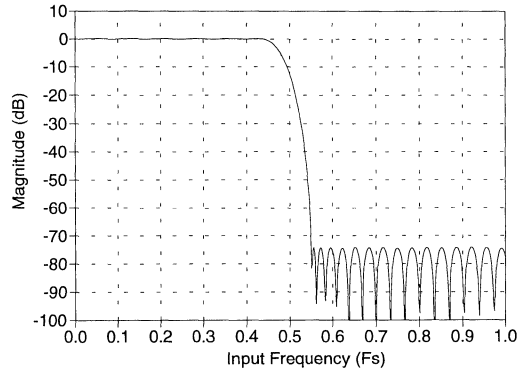


Figure 21. ADC Frequency Response

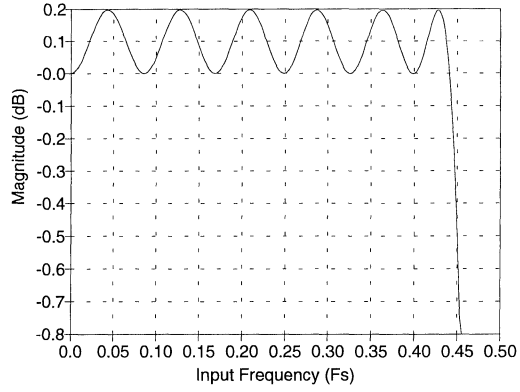


Figure 22. ADC Passband Ripple

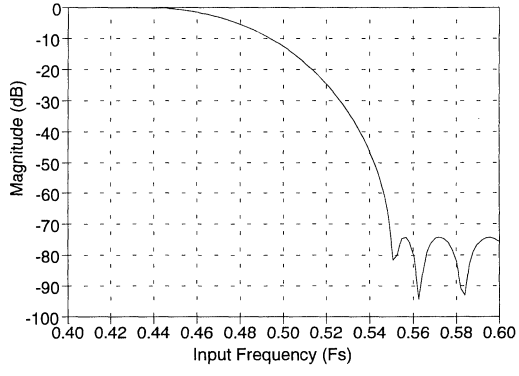


Figure 23. ADC Transition Band

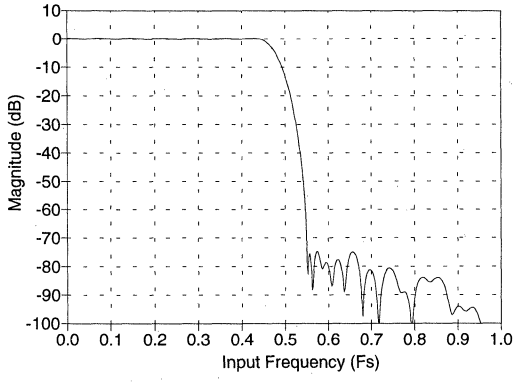


Figure 24. DAC Frequency Response

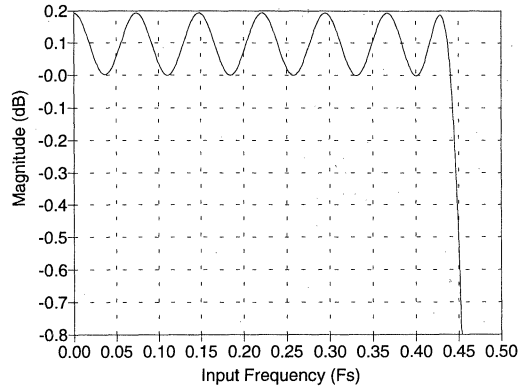


Figure 25. DAC Passband Ripple

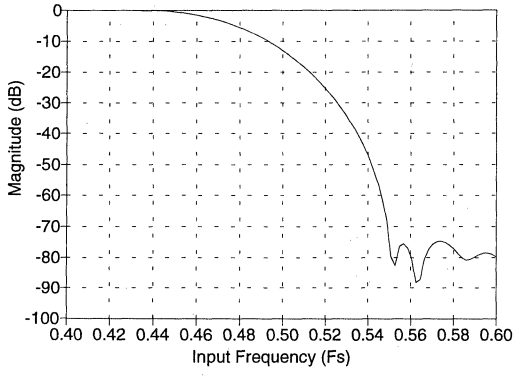


Figure 26. DAC Transition Band

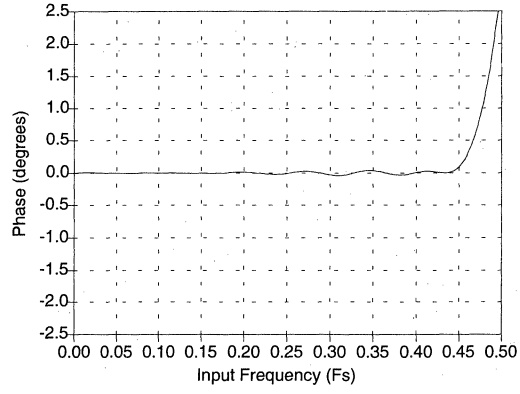
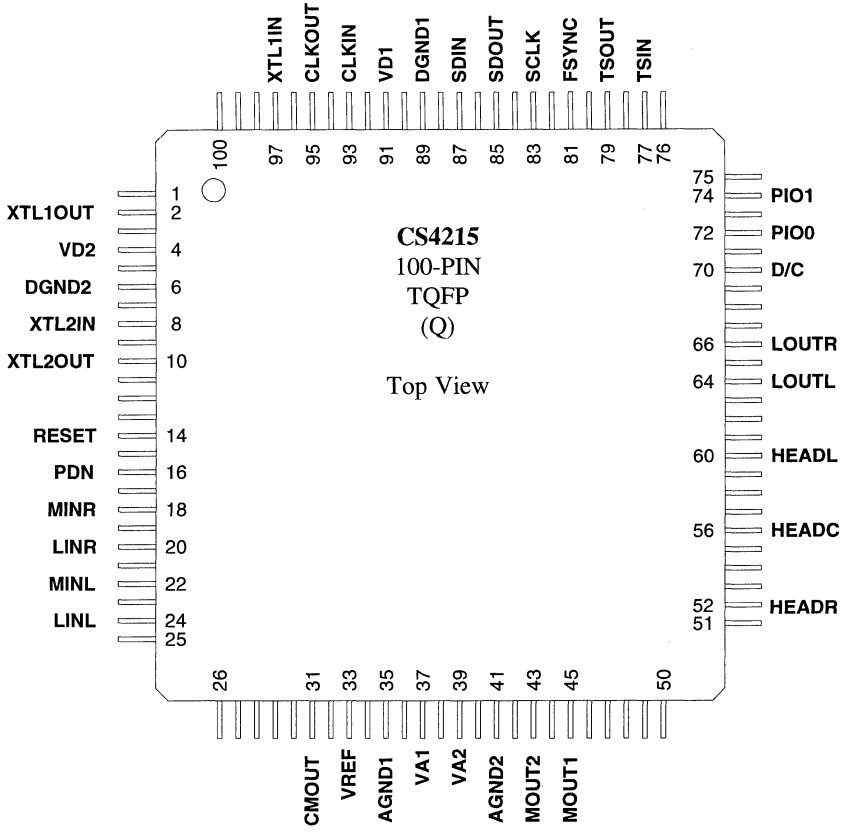
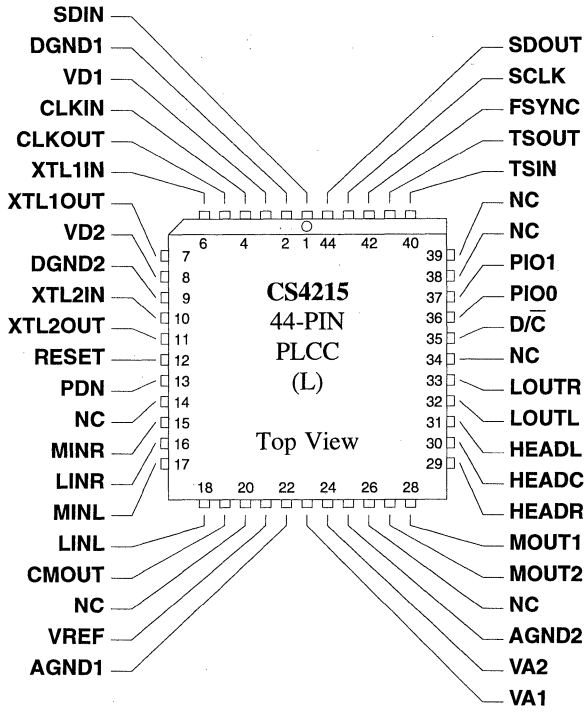


Figure 27. DAC Deviation from Linear Phase

PIN DESCRIPTIONS



Note: All unlabeled pins are No Connects



Power Supply

VA1, VA2 - Analog Power Input, Pins 23(L), 24(L), 37(Q), 39 (Q)
+5 V analog supply.

AGND1, AGND2 - Analog Ground, Pins 22(L), 25(L), 35(Q), 41(Q)
Analog ground. Must be connected to DGND1, DGND2 with zero impedance.

VD1, VD2 - Digital Power Input, Pins 3(L), 8(L), 91(Q), 4(Q)
+ 5 V digital supply.

DGND1, DGND2 - Digital Ground, Pin 2(L), 9(L), 89(Q), 6(Q)
Digital ground. Must be connected to AGND1, AGND2 with zero impedance.

Analog Inputs

LINL, LINR - Left and Right Channel Line Level Inputs, Pins 18(L), 16(L), 24(Q), 20(Q)
Line level input connections for the right and left channels.

MINL, MINR - Left and Right Channel Microphone Inputs, Pins 17(L), 15(L), 22(Q), 18(Q)
Microphone level input connections for the right and left channels.

Analog Outputs

LOUTR, LOUTL - Line Level Outputs, Pins 33(L), 32(L), 66(Q), 64(Q)
One pair of line level outputs are provided. The output level for right and left outputs can be independently varied. These outputs can be muted.

HEADR, HEADL - Headphone Outputs, Pins 29(L), 31(L), 52(Q), 60(Q)
HEADR and HEADL are intended to drive a pair of headphones. Additional current drive, along with an optional +3 dB of gain, ensures reasonable listening levels. These outputs can be muted.

HEADC - Common Return for Headphone Outputs, Pin 30(L), 56(Q)
HEADC is the return path for large currents when driving headphones from the HEADR and HEADL outputs. This pin is nominally at 2.1 V.

CMOUT - Common Mode Output, Pin 19(L), 31(Q)
Common mode voltage output. This signal may be used for level shifting the analog inputs. The load on CMOUT must be DC only, with an impedance of not less than 10kΩ. CMOUT should be bypassed with a 0.47 µF to AGND. CMOUT is nominally at +2.1V.

MOUT1, MOUT2 - Mono Speaker Outputs, Pins 28(L), 27(L), 45(Q), 43(Q)
Mono external loudspeaker differential output connections. The loudspeaker output is a mix of left and right line outputs. Independent muting of the speaker is provided. MOUT1 and MOUT2 output voltage is nominally at 2.1 V with no signal.

VREF - Voltage Reference Output, Pin 21(L), 33(Q)
The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10 µF capacitor in parallel with a 0.1 µF capacitor to the adjacent AGND1 pin. No other external load may be connected to this output.

Digital Interface Signals

SDIN - Serial Data Input, Pin 1(L), 87(Q)
Audio data for the DACs and control information for all functions is presented to the CS4215 on this pin.

SDOUT - Serial Data Output, Pin 44(L), 85(Q)
Audio data from the ADCs and status information concerning all functions is written out by the CS4215 onto this pin.

SCLK - Serial Port Clock, Pin 43(L), 83(Q)

SCLK rising causes the data on SDOUT to be updated. SCLK falling latches the data on SDIN into the CS4215. The SCLK signal can be generated off-chip, and input into the CS4215. Alternatively, the CS4215 can generate and output SCLK in data mode.

FSYNC - Frame Sync Signal, Pin 42(L), 81(Q)

The Frame Synchronizing Signal is sampled by SCLK, with a rising edge indicating a new frame is about to start. FSYNC frequency is always the system sample rate. Each frame may have 64, 128 or 256 data bits, allowing for 1, 2 or 4 CS4215s connected to the same bus. FSYNC may be input to the CS4215, or may be generated and output by the CS4215 in data mode. When FSYNC is an input, it must be high for at least 1 SCLK period. FSYNC can stay high for the rest of the frame, but must return low at least 2 SCLKs before the next frame starts.

TSIN - Time Slot Input, Pin 40(L), 77(Q)

TSIN high for at least 1 SCLK cycle indicates to the CS4215 that the next time slot is allocated for it to use. TSIN is normally connected to the TSOUT pin of the previous device in the chain. TSIN should be connected to FSYNC for the 1st (or only) CS4215 in the chain.

TSOUT - Time Slot Output, Pin 41(L), 79(Q)

TSOUT goes high for 1 SCLK cycle, indicating that the CS4215 is about to release the data bus. Normally connected to the TSIN pin on the next device in the chain.

D/$\overline{C}$ - Data/Control Select Input, Pin 35(L), 70(Q)

When D/$\overline{C}$ is low, the information on SDIN and SDOUT is control information. When D/$\overline{C}$ is high, the information on SDIN and SDOUT is data information.

PDN - Power Down Input, Pin 13(L), 16(Q)

When high, the PDN pin puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down causes all the control registers to change to the default reset state. In the power down mode, the TSOUT pin remains active, and follows TSIN delayed by less than 10 ns.

$\overline{\text{RESET}}$ - Active Low Reset Input, Pin 12(L), 14(Q)

Upon reset, the values of the control information (when D/$\overline{C}$ = 0) will be initialized to the values given in the Reset Description section of this data sheet.

Clock and Crystal Pins

XTL1IN, XTL1OUT, XTL2IN, XTL2OUT - Crystals 1 and 2 Inputs and Outputs, Pins 6(L), 7(L), 10(L), 11(L), 97(Q), 2(Q), 8(Q), 10(Q)

Input and output connections for crystals 1 and 2. One of these oscillators may provide the master clock to run the CS4215.

CLKIN - External Clock Input, Pin 4(L), 93(Q)

External clock input optionally used to clock the CS4215. The CLKIN frequency must be 256 times the maximum sample rate (FSYNC frequency).

CLKOUT - Master Clock Output, Pin 5(L), 95(Q)

Master clock output, whose frequency is always 256 times the system sample rate (FSYNC frequency). CLKOUT is active only in data mode and is low during control mode.

Miscellaneous Pins

PIO0, PIO1 - Parallel Input/Output, Pins 36(L), 37(L), 72(Q), 74(Q)

These pins are provided as general purpose digital parallel input/output and have open drain outputs. An external pull-up resistor is required. They can be read in control mode, and read and written to in data mode.

Note: All unlabeled pins are No Connects which should be left floating.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

Total Dynamic Range

The rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (ie. attenuation bits for the DACs at full attenuation.) Units in dB.

Instantaneous Dynamic Range

The dynamic range available at any instant in time. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces to harmonic distortion components of the noise to insignificance. Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms value of a signal's first five harmonic components to the rms value of the signals fundamental component. THD is calculated for the ADCs using an input signal which is 3dB below typical full-scale, and is referenced to typical full-scale. A digital full-scale output is used to calculate THD for the DACs.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Step Size

Typical delta between two adjacent gain or attenuation values. Units in dB.

Absolute Step Error

The deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the full-gain/attenuation value (i.e. end points). Units in dB.

Out-of-Band Energy

The ratio of the rms sum of the energy from 0.46xFs to 2.1xFs compared to the rms full-scale signal value. Tested with 48kHz Fs giving an out-of-band energy range of 22kHz to 100kHz.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input at CMOUT. For the DACs, the deviation of the output from CMOUT with mid-scale input code. Units in volts.

APPENDIX A

This data sheet describes version 2 of the CS4215. Therefore, this appendix is included to describe the differences between versions 0,1 and version 2. This information is only useful for users that still have version 0 and version 1 devices since version 2 devices will supplant the earlier versions. The version number can be found in control mode, time slot 7. The version can also be identified by the revision letter stamped on the top of the actual chip. The revision letter immediately precedes the data code on the second line of the package marking (See *General Information* section of the Crystal Data Book). Version 0 corresponds to chip revision C, version 1 corresponds to chip revision D, and version 2 corresponds to chip revision E. Future chip revisions (ie. F, G, H) may still be version 2 since the version number only changes if there is a register change to the part that will affect driver software.

The Functional Differences Between Version 0(Rev. C) and Version 1(Rev. D)

1. FSYNC on version 0 must be ONLY one SCLK period high, whereas on version 1 FSYNC must be AT LEAST one SCLK period high.

2. When driving an external CMOS clock into one of the XTL-IN pins, version 0 devices must have a series resistor of at least 1kΩ between the CS4215 and the clock source. The resistor is needed because the codec will put XTL-IN to ground (on version 0 only) when that crystal is not selected, as is the case on power-up. In version 1 the XTL-IN pins are floated when not selected; therefore, the series resistor is not needed on version 1. Version 1 will work properly if the resistor is included.

3. The OLB and ITS bits do not exist on version 0. Writing these bits as zero makes both versions function identically; therefore, version 1 is backwards compatible with version 0.

4. When entering control mode, CLKOUT stops 4 to 12 clocks later and may start up briefly when switching master clock sources on version 0. On version 1 CLKOUT stops within two clocks and doesn't start up until data mode is entered.

5. In version 0 the headphone and speaker outputs are not short-circuit protected, whereas in version 1 they are short-circuited protected.

The functional differences between Version 1(Rev. D) and Version 2(Rev. E)

1. The MLB, HPF, and MCK2 bits in control mode do not exist in version 0 or version 1. Writing these bits as zero makes all versions functionally identical; therefore, version 2 is backwards compatible with previous versions.

2. The A/D invalid bit, ADI, in data mode does not exist in version 0 or version 1.

3. The 8-bit unsigned data format (DF1,0=3) does not exist in version 0 or version 1.

4. SDOUT contained random data during calibration in versions 0 and 1. SDOUT outputs zeros during calibration in version 2.

Semiconductor Corporation

CDB4215

CS4215 Evaluation Board

Features

- Easy DSP Hook-Up
- Correct Grounding and Layout
- Microphone Pre-Amplifier
- Line Input Buffer
- Digital Patch Area

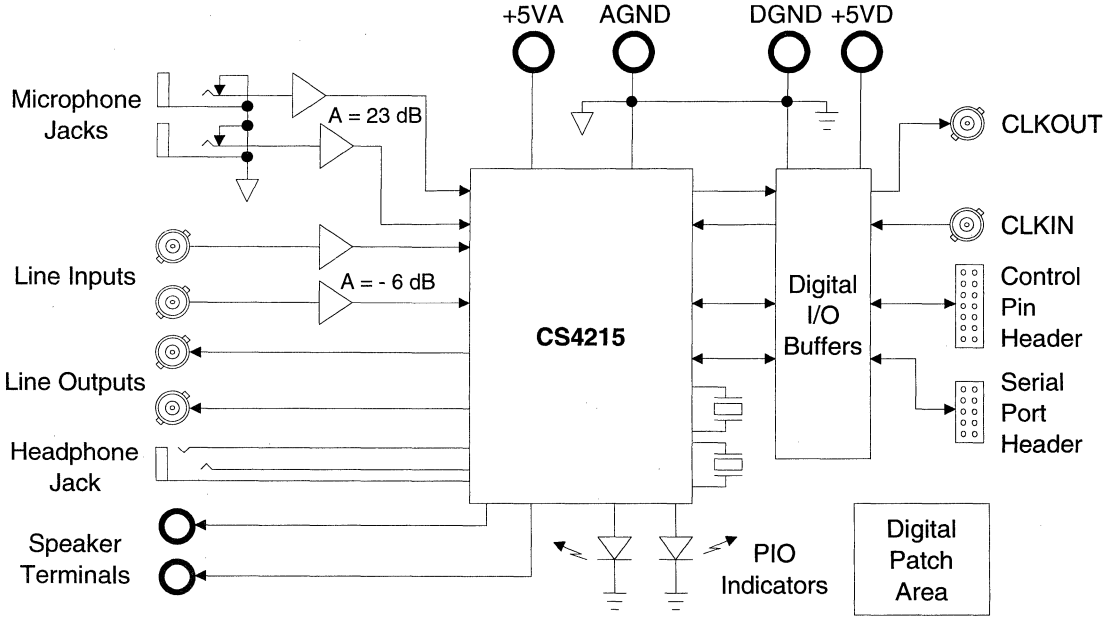
General Description

The CDB4215 evaluation board allows easy evaluation of the CS4215 audio multimedia codec. Analog inputs provided include two 1/4" microphone jacks and two BNC line inputs. Analog outputs provided are two BNC line outputs, one stereo 1/4" headphone jack and one pair of speaker terminals.

Digital interfacing is facilitated by two buffered ribbon cable headers. One contains the serial port and the other contains the codec control pins.

ORDERING INFORMATION: CDB4215

4



Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

GENERAL INFORMATION

The CDB4215 is designed to provide an easy platform for evaluating the performance of the CS4215 Multimedia Audio Codec. The board provides a buffered serial interface for easy connection to the serial port of a DSP or other serial device. A single +5 V power supply is all that is required to power the evaluation board.

The line input buffers are designed to accept standard CD-level inputs of 2 V_{RMS} and BNC-to-phono adapters are included to support various test setups. The microphone inputs consist of two 1/4" mono jacks that are designed to accept standard single-ended dynamic or condenser microphones.

The line outputs are supplied via BNC jacks with two more BNC-to-phono adapters. The headphone output is supplied via a 1/4" stereo jack and will drive headphones of 48 Ω or greater. This includes most "walkman" style headphones. Speaker terminals are provided and can be connected to speakers with an impedance of 32 Ω or greater.

The film plots of the board are included to provide an example of the optimum layout, grounding, and decoupling arrangement for the CS4215.

POWER SUPPLY CIRCUITRY

Figure 1 illustrates a portion of the CDB4215 schematic and includes the CS4215 codec along with power supply circuitry. Power is supplied to the board via two sets of binding posts, one for digital and one for analog. The analog supply must be +5 Volts and supplies power for the entire codec (both digital and analog power supply pins) along with the analog input buffers for the line and microphone inputs. The digital supply is also +5 Volts and supplies power to the digital header buffer circuitry. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the codec from the digital supply. Selection of L1 will depend on the characteristics of the noise on the digital supply used.

ANALOG INPUTS

The analog inputs consist of a pair of 1/4" jacks for two microphones, and a pair of BNC's for line level inputs. BNC-to-phono adapters are included to allow testing of the line inputs using coax or standard audio cables.

The line-level inputs go through a buffer, Figure 2, with a gain of 0.5 which allows input signals of up to 2 V_{RMS}.

The two microphone inputs are single-ended and are designed to work with both condenser and dynamic mics. The microphone input buffer circuit, shown in Figure 3, has a gain of 23 dB thereby defining a full-scale input voltage to the mic jacks of 19.5 mVpp.

ANALOG OUTPUTS

The CDB4215 includes three analog output paths: a pair of line output BNC's, a stereo 1/4" headphone jack, and a pair of mono speaker terminals.

The CS4215 drives the line outputs into an R-C filter and then to a pair of BNC's. As with the line inputs, BNC-to-phono adapters are provided for flexibility. The line outputs can drive an impedance of 10 kΩ or more, which is the typical input impedance of most audio gear.

The stereo headphone output can drive headphones with an impedance of 48 Ω or greater. This includes most "walkman" style headphones.

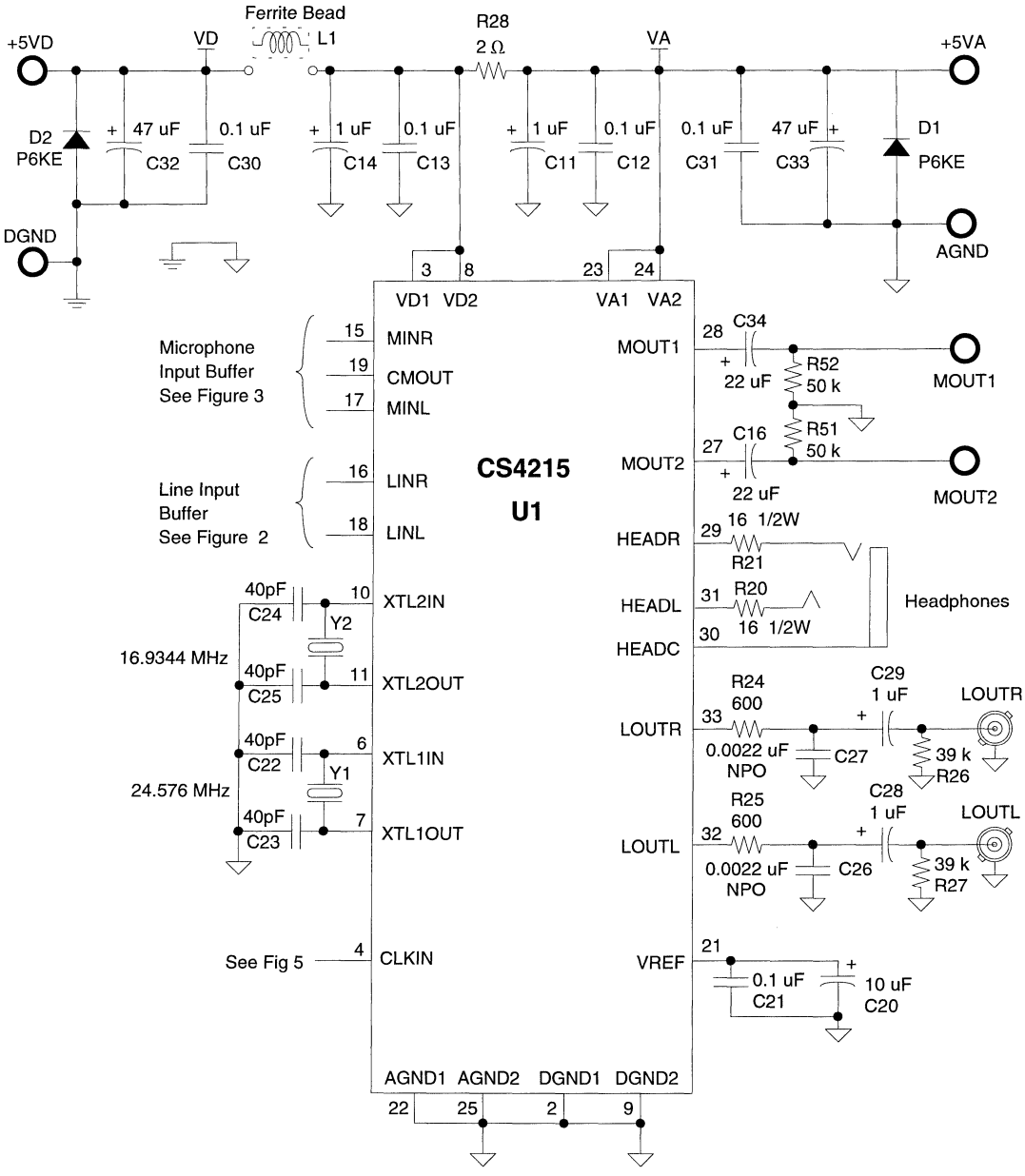


Figure 1. CS4215 & Power Supplies

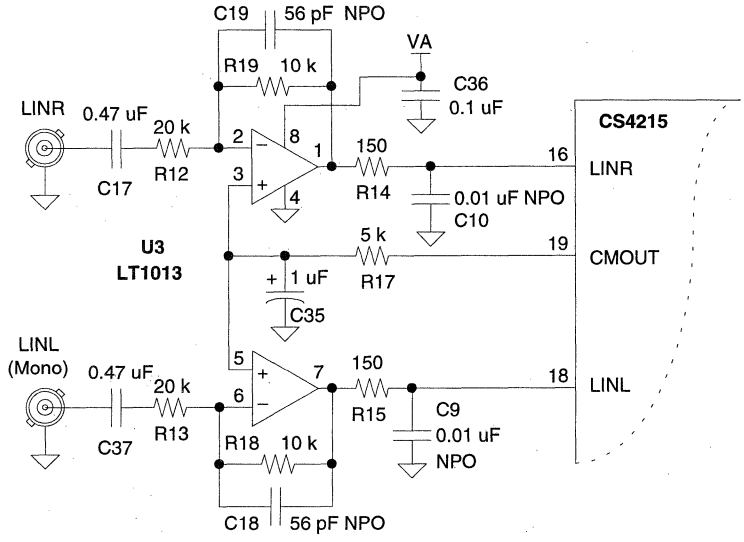


Figure 2. Line Input Buffer

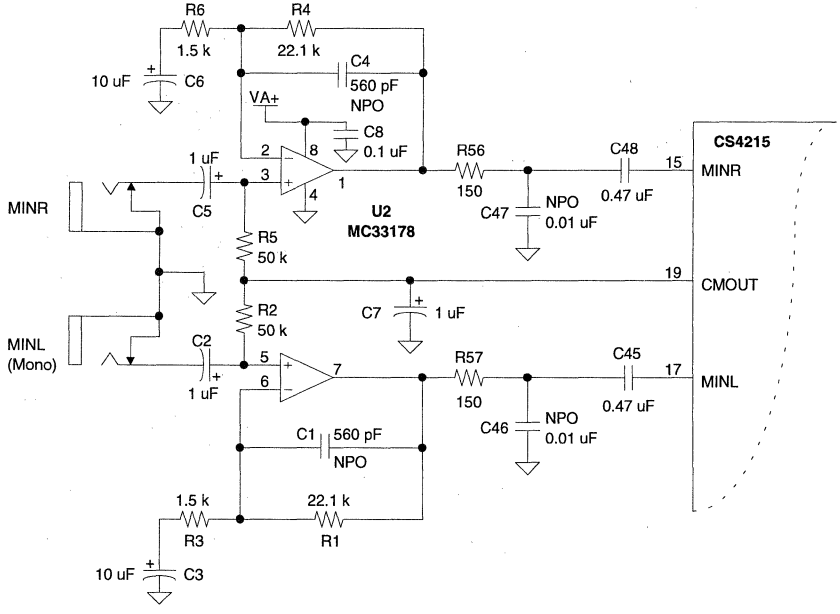


Figure 3. Microphone Input Buffer

Speaker terminals are provided and are labeled MOUT1 and MOUT2. Speakers connected to the terminals must have an impedance of 32 Ω or greater. DC blocking capacitors are included to form a high-pass filter with the speaker impedance. This filter blocks very low frequency signals which can heavily distort some inexpensive speakers.

SERIAL INTERFACE

The CDB4215 is primarily designed to evaluate the CS4215 is single chip mode, i.e. only one codec on the serial bus. This is the default state for the CDB4215 and is defined by having the P4 jumper in the "1CHIP" position, see Figure 4, which connects FSYNC to TSIN. This connection defines the board codec's time slots as the first 64 bits of the frame. The only signals that need to be connected to the DSP are the five signals on header J15. The serial interface is illustrated in Figure 4.

If the goal is to connect multiple CDB4215s on the same serial port, jumper P4 must be in the "MULTI" position which disconnects TSIN from FSYNC. The MULTI position also connects an unbuffered SDOUT to header J14. This header pin, SDOUTUB, must be used in lieu of SDOUT since SDOUT is buffered and does not go high impedance during other codec's time slots. Using the multi-chip scenario, the TSIN header pin must be connected to the previous codec's TSOUT line and the first codec's TSIN must be connected, via the header, to FSYNC.

Note that when P4 is in the 1CHIP mode, the SDOUTUB pin on header J14 is not connected to the SDOUT pin on the CS4215 and is floating.

There are two scenario's that must be addressed when connecting the CDB4215 to a DSP: one is when the codec is the master in data mode and the other is when the codec is a slave in data mode. In control mode the codec is always a slave and FSYNC and SCLK must be driven from the DSP. Since the evaluation board buffers all the signals between the codec and the DSP, the board must "know" which of the two modes is being used. Jumper P3 selects the particular mode.

Codec Master Data Mode

When the codec is to be programmed as a master in data mode, the direction of FSYNC and SCLK have to be changed between control mode and data mode. In this case the P3 jumper must be set for "M/S" which uses the D/$\overline{C}$ signal to control the direction of the buffers (U7) for SCLK and FSYNC. When P3 is set to M/S, the buffers drive the J15 header in data mode and receives FSYNC and SCLK from the header in control mode.

Codec Slave Data Mode

When the codec is to be programmed as a slave in data mode, FSYNC and SCLK are always inputs to the codec. In this mode P3 must be set to "SLAVE" which configures the FSYNC and SCLK buffers to always receive FSYNC and SCLK from the J15 header.

As stated in the CS4215 data sheet, when the codec is programmed in slave mode, XCLK = 0 in control mode, SCLK and FSYNC are inputs and must be derived from the same clock used as the master clock for the codec. Although SCLK and FSYNC must be frequency locked to the master clock, there is no phase requirement.

CONTROL PINS

All control pins, located on header J14, are defined as pins that are not essential to the DSP serial port when used in 1CHIP mode.

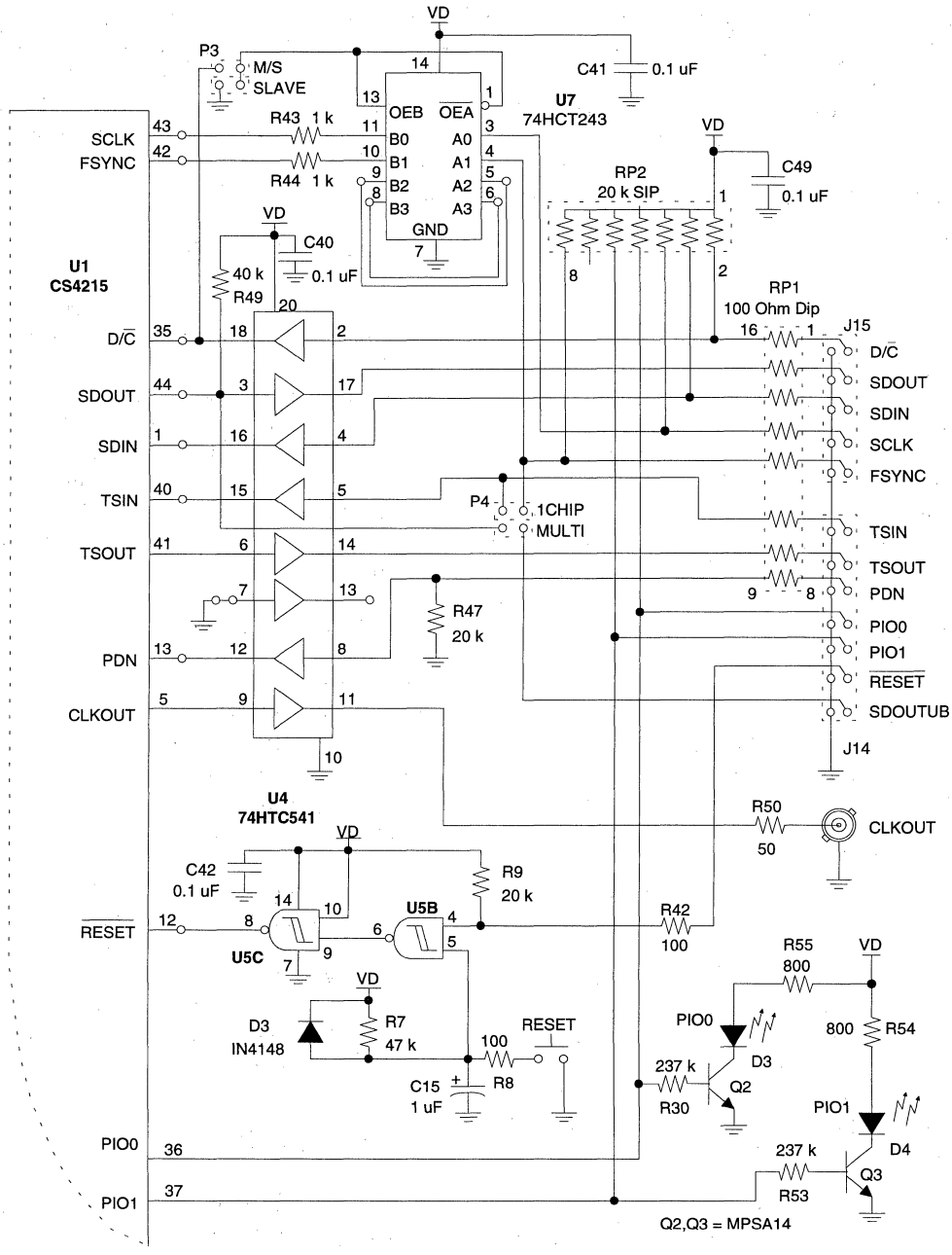


Figure 4. Digital Interface

PDN and $\overline{RESET}$

Power down, PDN, controls the PDN pin on the codec. The line has an on-board pull-down resistor thereby defining the default state as powered. This pin only needs to be controlled if the power down feature is used.

$\overline{RESET}$ controls the $\overline{RESET}$ pin on the codec and is pulled up on the board. This defines the default state as not reset. This pin only needs to be controlled if the reset feature on the codec is needed. Since the codec does require a reset at power up, a power-up reset circuit is included on the board. A reset switch is also included to reset the device without having to remove the power supply. The power-up reset plus switch are logically OR'ed with the $\overline{RESET}$ pin on header J14.

PIO Lines

The parallel input/output, PIO, lines are pulled up on the evaluation board. If they are to be used as inputs, they should be driven by open-collector gates since inadvertently setting the PIO bits low in software will force the external lines low. The PIO lines are available on header J14.

The PIO lines also go through a high-impedance buffer and drive LED's on the evaluation board. When the LED is on, the corresponding bit is 1 or high. The LED's provide a visual indication that may be used to verify that the software is writing the bits correctly.

CLOCKS

The CDB4215 can accommodate all clocking modes supported by the CS4215. A CLKIN BNC, as shown in Figure 5 allows the CLKIN pin on the CS4215 to be used as the master clock source. The two crystals listed in the CS4215 data sheet are also provided and support all the audio and multimedia standard sample frequencies. The master clock is selected via a CS4215 internal register from control mode.

The CLKOUT BNC is a buffered version of the CLKOUT pin on the CS4215. CLKOUT is always 256 times the programmed sample frequency in data mode. CLKOUT is held low in control mode.

LAYOUT ISSUES

Figure 6 contains the silk screen, Figure 7 contains the top-side copper layer, and Figure 8 contains the bottom-side copper layer of the CDB4215 evaluation board. These plots are included to provide an example of how to layout a PCB for the codec. Two of the more important aspects are the position of the ground plane split, which is next to the part - *NOT UNDER IT*, and the ground plane fill between traces on both layers, which minimizes coupling of radiated energy.

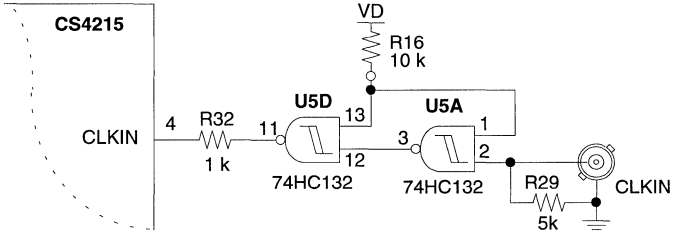


Figure 5. CLKIN

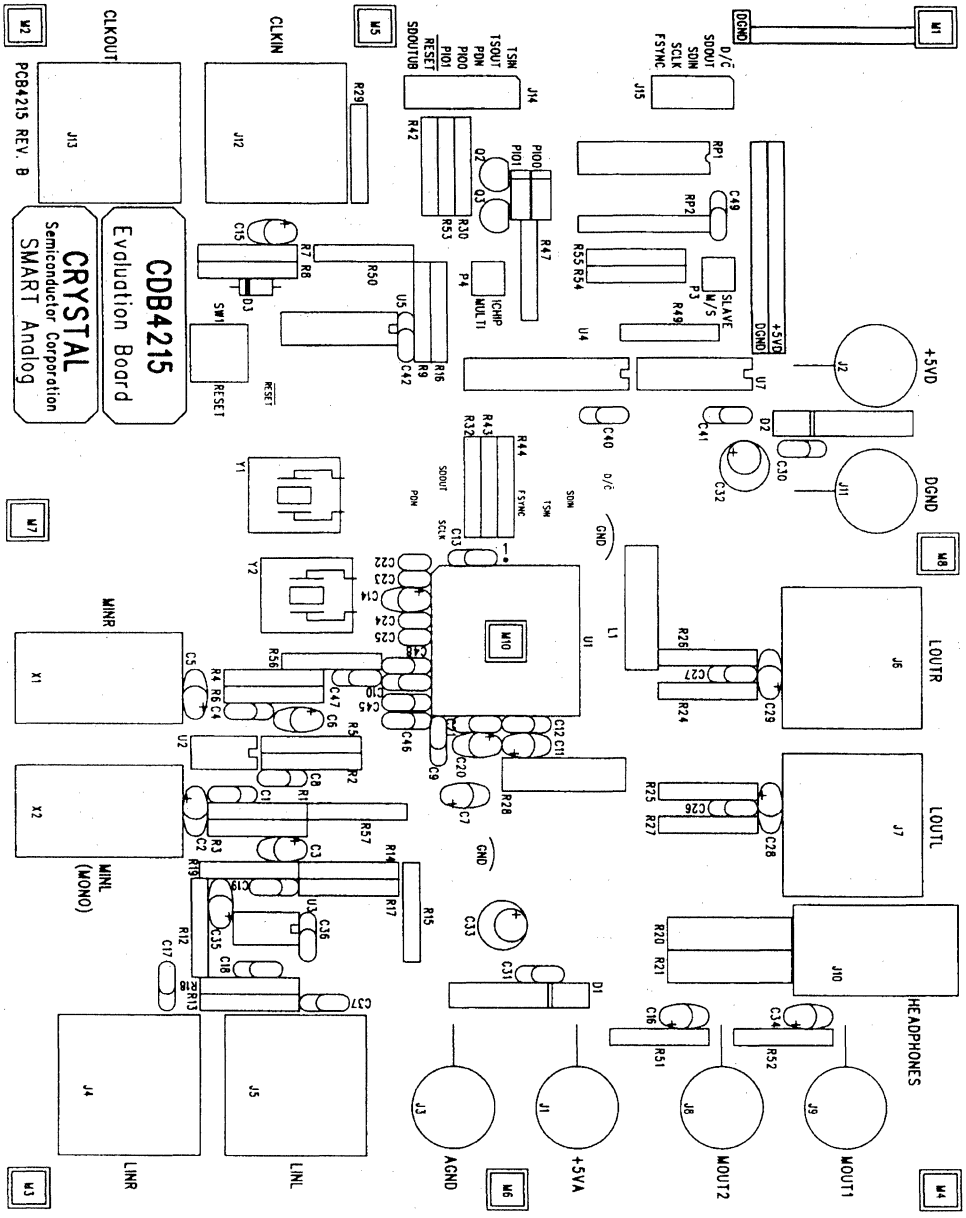


Figure 6. CDB4215 Board Silkscreen (Not to Scale)

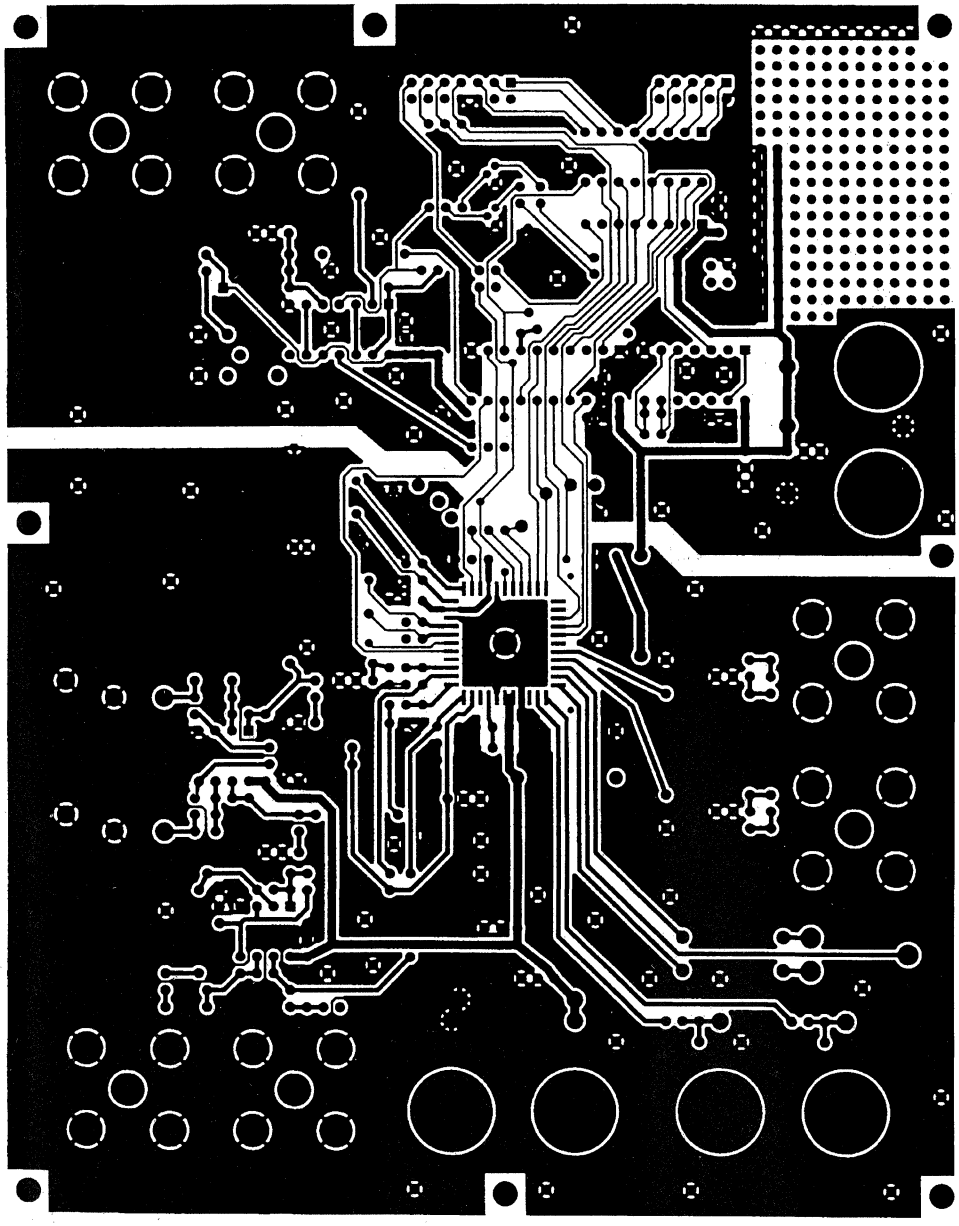


Figure 7. CDB4215 Compont Side Layout (Not to Scale)

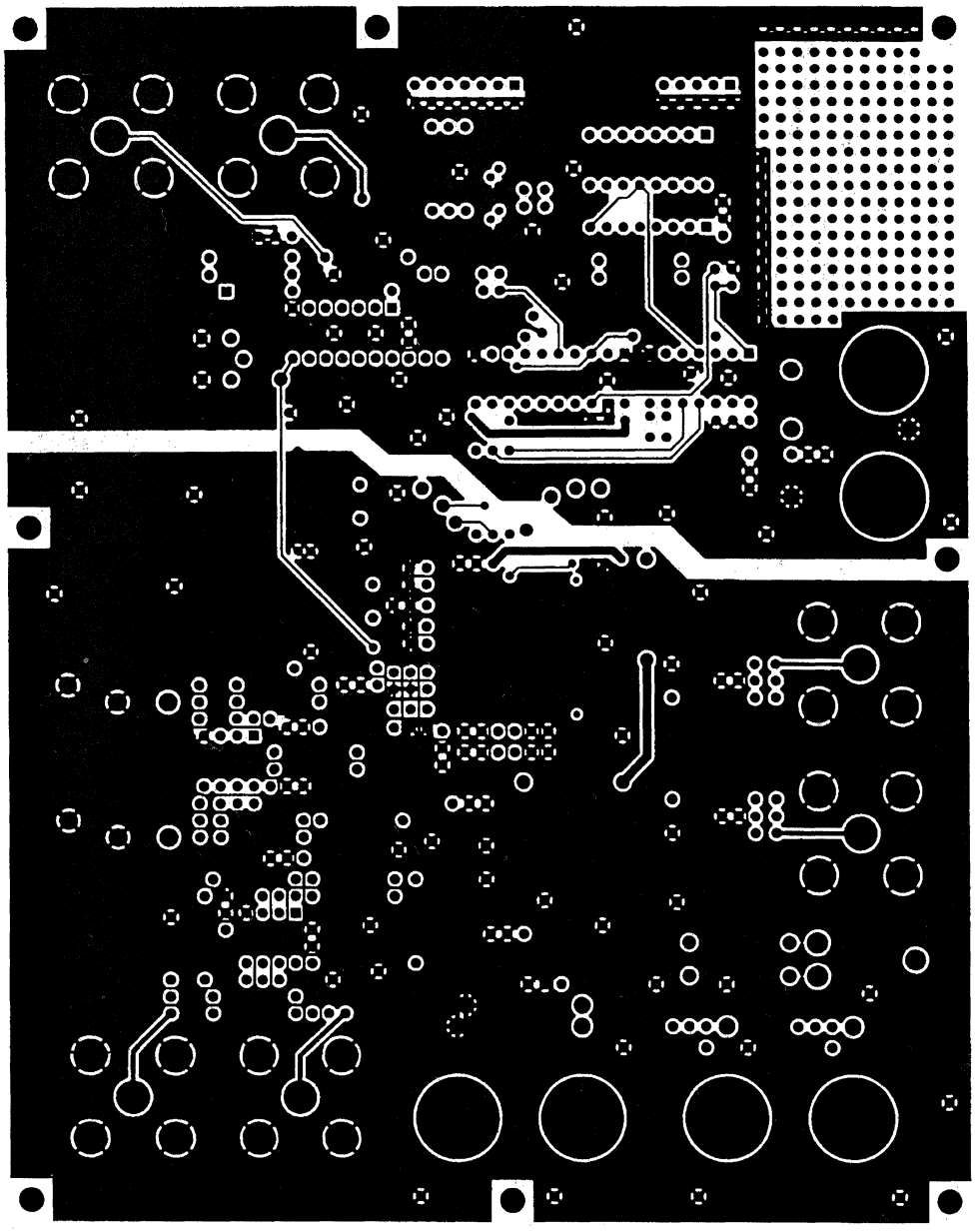


Figure 8. CDB4215 Solder Side Layout (Not to Scale)

Semiconductor Corporation

CS4216

16-Bit Stereo Audio Codec

Features

- CMOS Stereo Audio Input/Output System
  - Delta-Sigma A/D Converters
  - Delta-Sigma D/A Converters
  - Input Anti-Aliasing and Output Smoothing Filters
  - Programmable Input Gain and Output Attenuation
- Sample Frequencies of 4 kHz to 50 kHz
- CD Quality Noise and Distortion < 0.01 %THD
- Internal 64X Oversampling
- Low Power Dissipation: 80 mA
  1 mA Power-Down Mode

General Description

mwave The CS4216 is an Mwave™ audio codec.

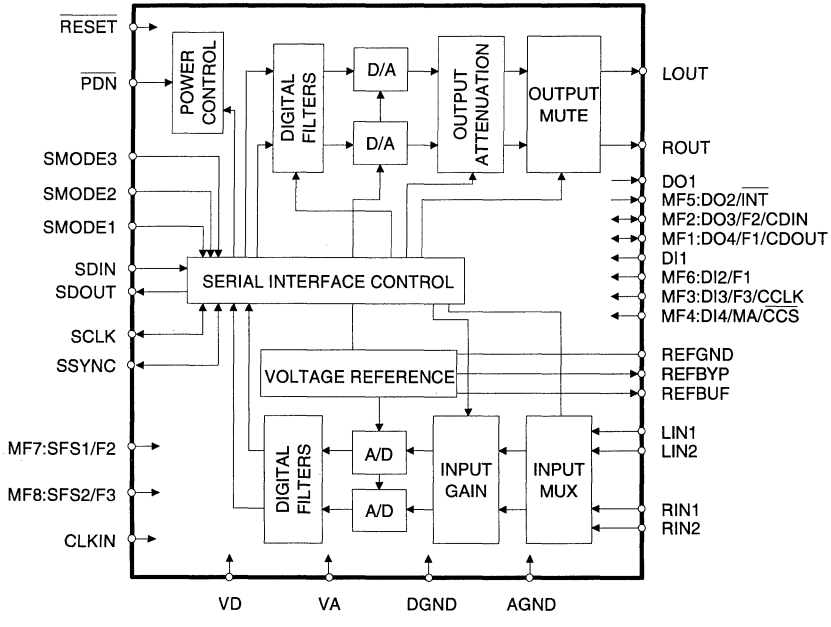
The CS4216 Stereo Audio Codec is a monolithic CMOS device for computer multimedia, automotive, and portable audio applications. It performs A/D and D/A conversion, filtering, and level setting, creating 4 audio inputs and 2 audio outputs for a digital computer system. The digital interfaces of left and right channels are multiplexed into a single serial data bus with word rates up to 50 kHz per channel. Up to 4 CS4216 devices can be attached to a single hardware bus.

Both the ADCs and the DACs use delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter which eliminates the need for external anti-aliasing filters. The DACs include output smoothing filters on-chip.

Ordering Information:

CS4216-KL	0° to 70°C	44-pin PLCC
CS4216-KQ	0° to 70°C	44-pin TQFP
CDB4216	Evaluation Board	

4



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature		T_A	0	25	70	°C

ANALOG CHARACTERISTICS (T_A = 25°C; VA, VD = +5V; Input Levels: Logic 0 = 0V, Logic 1 = VD; 1 kHz Input Sine Wave; CLKIN = 24.576 MHz; SM1; Conversion Rate = 48 kHz; SCLK = 12.288 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Unless otherwise specified.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution			16	-	-	Bits
ADC Differential Nonlinearity	(Note 1)		-	-	±0.9	LSB
Instantaneous Dynamic Range		IDR	80	85	-	dB
Total Harmonic Distortion		THD	-	-	0.01	%
Interchannel Isolation			-	80	-	dB
Interchannel Gain Mismatch			-	-	±0.5	dB
Frequency Response	(Note 1)		-0.5	-	+0.2	dB
Programmable Input Gain Span			21	22.5	24	dB
Gain Step Size			-	1.5	-	dB
Absolute Gain Step Error			-	-	0.75	dB
Gain Drift			-	100	-	ppm/°C
Offset Error	DC Coupled Inputs		-	±10	±100	LSB
	AC Coupled Inputs		-	±150	±400	LSB
Full Scale Input Voltage			2.5	2.8	3.1	V_{pp}
Input Resistance	(Notes 1,2)		20	-	-	kΩ
Input Capacitance	(Note 1)		-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, not production testing.
2. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance.

* Parameter definitions are given at the end of this data sheet.

Mwave™ is a trademark of the IBM Corporation.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *	Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.					
DAC Resolution		16	-	-	Bits
DAC Differential Nonlinearity (Note 1)		-	-	±0.9	LSB
Total Dynamic Range	TDR	-	93	-	dB
Instantaneous Dynamic Range	IDR	80	83	-	dB
Total Harmonic Distortion (Note 4)	THD	-	-	0.02	%
Interchannel Isolation (Note 4)		-	80	-	dB
Interchannel Gain Mismatch		-	-	±0.5	dB
Frequency Response (Note 1)		-0.5	-	+0.2	dB
Programmable Output Attenuation Span (Note 3)		-45	-46.5	-	dB
Attenuation Step Size (Note 3)		-	1.5	-	dB
Absolute Attenuation Step Error (Note 3)		-	-	0.75	dB
Gain Drift		-	100	-	ppm/°C
REFBUF Output Voltage (Note 5) Maximum output current= 400 µA		1.9	2.2	2.5	V
Offset Voltage		-	10	-	mV
Full Scale Output Voltage (Note 4)		2.5	2.8	3.1	V_{pp}
Deviation from Linear Phase (Note 1)		-	-	1	Degree
Out of Band Energy (22 kHz to 100 kHz)		-	-60	-	dB
Power Supply					
Power Supply Current (Note 6) Operating		-	80	100	mA
Power Down		-	-	1	mA
Power Supply Rejection (1 kHz)		-	40	-	dB

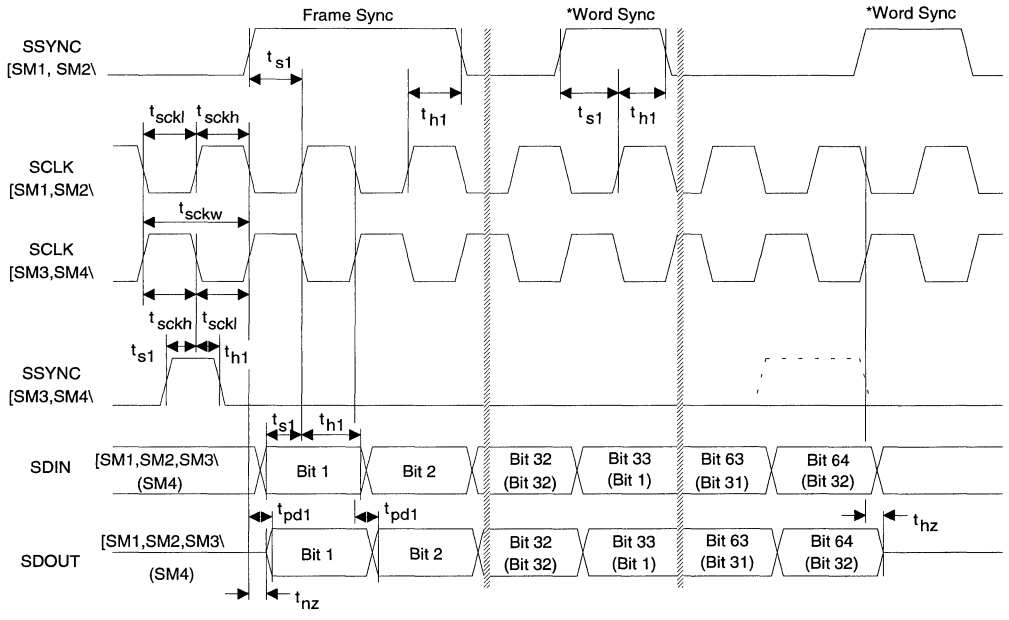
Notes: 3. Tested in SM3, Slave sub-mode, 128 BPF.
4. 10 kΩ, 100 pF load.
5. REFBUF load current must be DC. To drive dynamic loads, REFBUF must be buffered. AC variations in REFBUF current may degrade ADC and DAC performance.
6. Typically current: VA = 30mA, VD = 50mA. Power supply current does not include output loading.

* Parameter definitions are given at the end of this data sheet.

SWITCHING CHARACTERISTICS (T_A = 25°C; VA, VD = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD)

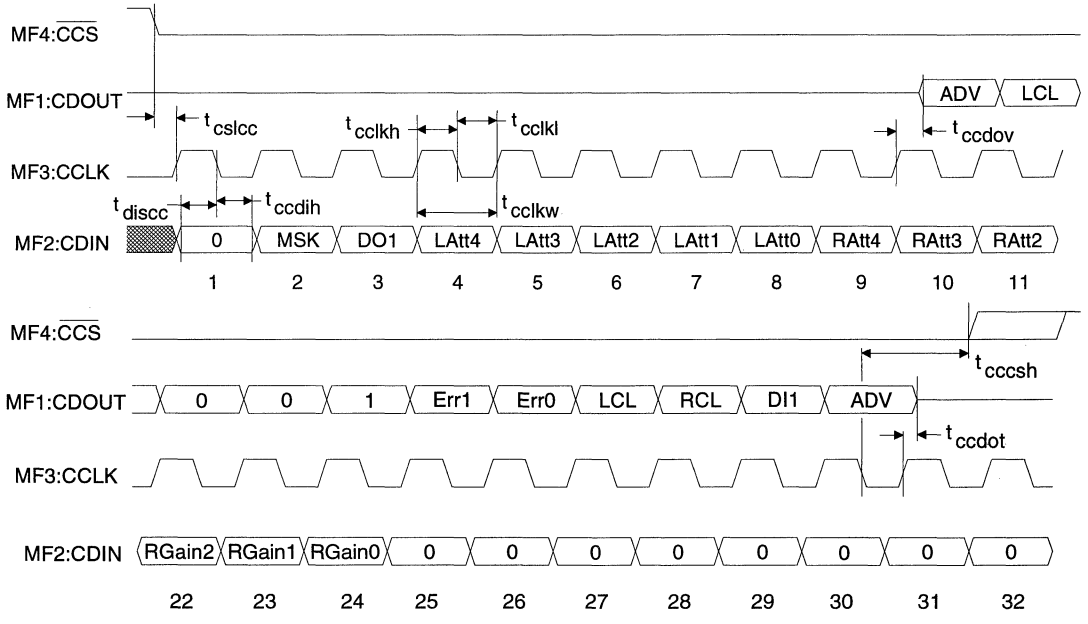
Parameter		Symbol	Min	Typ	Max	Units
Input clock (CLKIN) frequency	SM1: SM2, SM3, SM4:	CLKIN CLKIN	2.048 1.024	24.576 12.288	25.6 12.8	MHz MHz
CLKIN low time		t_{ckl}	15	-	-	ns
CLKIN high time		t_{ckh}	15	-	-	ns
Sample Rate	(Note 1)	Fs	4	-	50	kHz
DI pins setup time to SCLK edge	(Note 1)	t_{s2}	10	-	-	ns
DI pins hold time from SCLK edge	(Note 1)	t_{h2}	8	-	-	ns
DO pins delay from SCLK edge		t_{pd2}	30	-	-	ns
SCLK and SSYNC output delay from CLKIN rising	Master Mode (Note 1)	t_{pd3}	-	-	50	ns
SCLK period	Master Mode (Note 7) Slave Mode	t_{sckw}	- 75	1/(Fs*bpf) -	- -	s ns
SCLK high time	Slave Mode	t_{sckh}	30	-	-	ns
SCLK low time	Slave Mode	t_{sckl}	30	-	-	ns
SDIN, SSYNC setup time to SCLK edge	Slave Mode	t_{s1}	15	-	-	ns
SDIN, SSYNC hold time from SCLK edge	Slave Mode	t_{h1}	10	-	-	ns
SDOUT delay from SCLK edge		t_{pd1}	-	-	28	ns
Output to Hi-Z state	bit 64 (Note 1)	t_{hz}	-	-	12	ns
Output to non-Hi-Z	bit 1 (Note 1)	t_{nz}	15	-	-	ns
$\overline{\text{RESET}}$ pulse width low			500	-	-	ns
$\overline{\text{CCS}}$ low to CCLK rising	SM4 (Note 1)	t_{cslcc}	25	-	-	ns
CDIN setup to CCLK falling	SM4 (Note 1)	t_{discc}	15	-	-	ns
CCLK low to CDIN invalid (hold time)	SM4 (Note 1)	t_{ccdih}	10	-	-	ns
CCLK high time	SM4 (Note 1)	t_{cclhh}	25	-	-	ns
CCLK low time	SM4 (Note 1)	t_{cclhl}	25	-	-	ns
CCLK Period	SM4 (Note 1)	t_{cclkw}	75	-	-	ns
CCLK rising to CDOUT data valid	SM4 (Note 1)	t_{ccdov}	-	-	30	ns
CCLK rising to CDOUT Hi-Z	SM4 (Note 1)	t_{ccdot}	-	-	30	ns
CCLK falling to $\overline{\text{CCS}}$ high	SM4 (Note 1)	t_{cccsh}	0	-	-	ns

Notes: 7. When the CS4216 is in master mode (SSYNC and SCLK outputs), the SCLK duty cycle is 50%. The equation is based on the selected sample frequency (Fs) and the number of bits per frame (bpf).

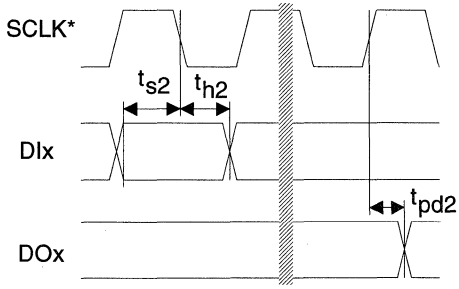


* Optional

Serial Audio Port Timing

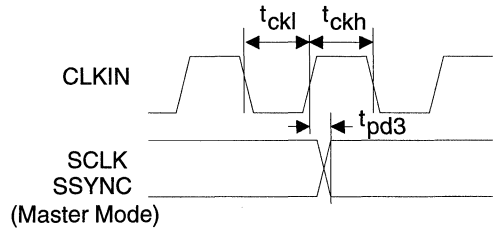


Serial Mode 4. Control Data Serial Port Timing



* SCLK is inverted for SM1 and SM2

DI/DO Timing



SCLK & SSYNC Output Timing (Master Mode)

DIGITAL CHARACTERISTICS (T_A = 25°C; VA, VD = 5V)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}	VD-1.0	-	-	V
Low-level Input Voltage	V_{IL}	-	-	1.0	V
High-level Output Voltage at I_O = -2.0 mA	V_{OH}	VD-0.3	-	-	V
Low-level Output Voltage at I_O = +2.0 mA	V_{OL}	-	-	0.1	V
Input Leakage Current (Digital Inputs)		-	-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	-	10	µA
Output Capacitance	C_{OUT}	-	-	15	pF
Input Capacitance	C_{IN}	-	-	15	pF

A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.2	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		80	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-		0.0	µs

4

D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	µs

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies: Digital	VD	-0.3	-	6.0	V
Analog	VA	-0.3	-	6.0	V
Input Current (Except Supply Pins)		-	-	±10.0	mA
Analog Input Voltage		-0.3	-	VA+0.3	V
Digital Input Voltage		-0.3	-	VD+0.3	V
Ambient Temperature (Power Applied)		-55	-	+125	°C
Storage Temperature		-65	-	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

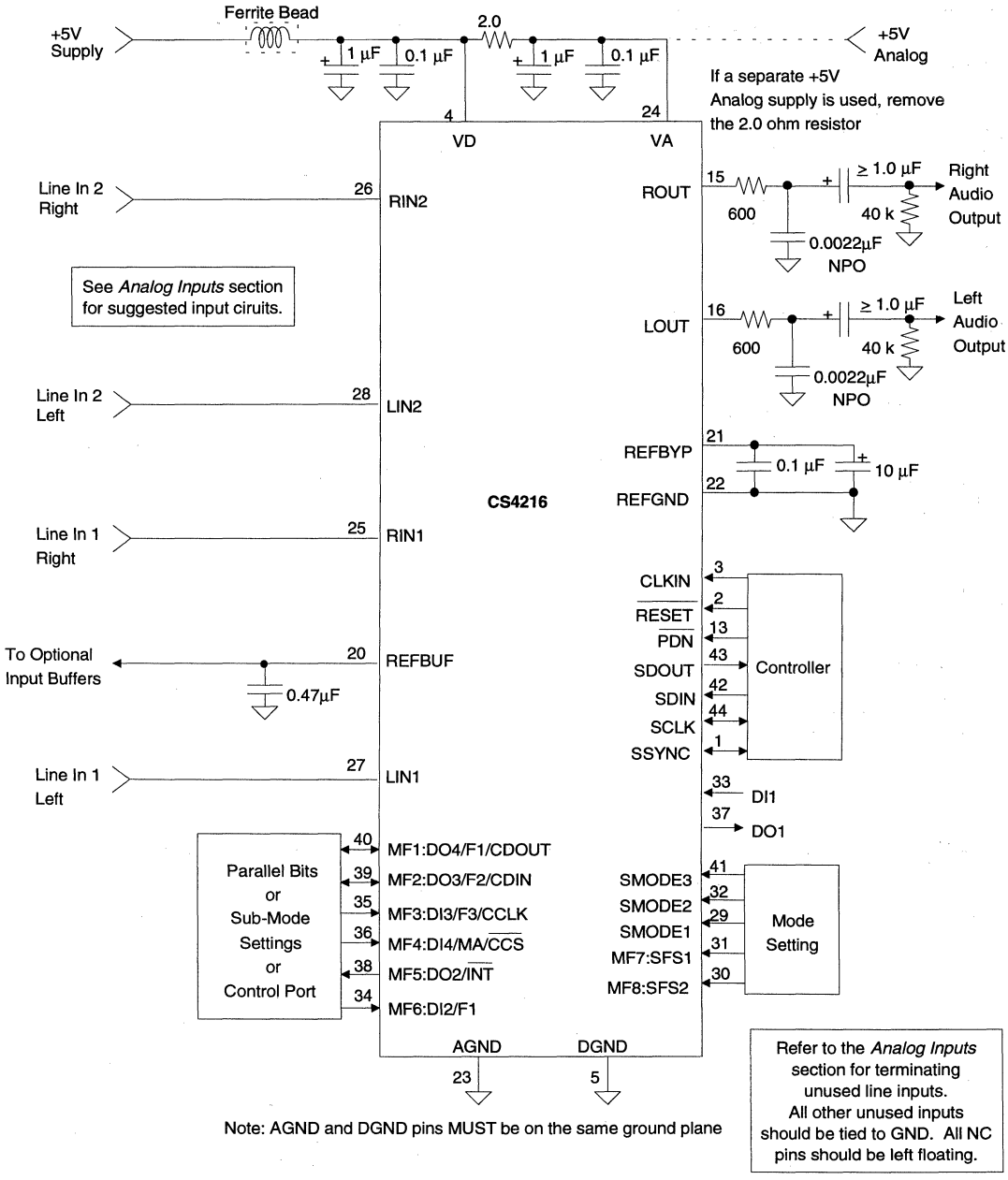


Figure 1. Typical Connection Diagram

OVERVIEW

The CS4216 contains two analog-to-digital converters, two digital-to-analog converters, adjustable input gain, and adjustable output level control. Since the converters contain all the required filters in digital or sampled analog form, the filters' frequency responses track the sample rate of the CS4216. Only a single-pole RC filter is required on the analog inputs and outputs. The RC filter acts as a charge reserve for the switched-capacitor input and buffers op-amps from a switched-capacitor load. Communication with the CS4216 is via a serial port, with separate pins for data into the device, and data from the device. The filters and converters operate over a sample rate range of 4 kHz to 50 kHz.

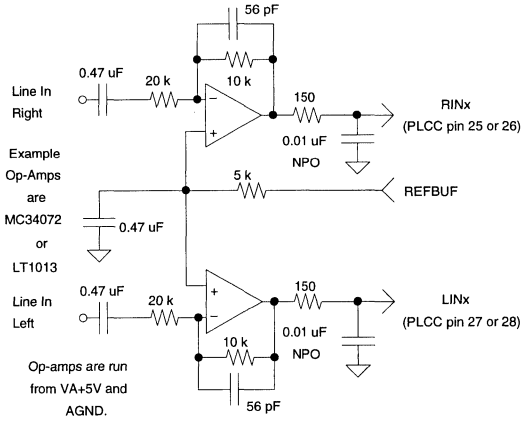


Figure 2. DC Coupled Input.

FUNCTIONAL SPECIFICATIONS

Analog Inputs and Outputs

Figure 1 illustrates the suggested connection diagram to obtain full performance from the CS4216. The line level inputs, LIN1 or LIN2 and RIN1 or RIN2, are selected by an internal input multiplexer. This multiplexer is a source selector and is not designed for switching between inputs at the sample rate.

Unused analog inputs that are not selected have a very high input impedance, so they may be tied to AGND directly. Unused analog inputs that are selected should be tied to AGND through a 0.1 µF capacitor. This prevents any DC current flow.

The analog inputs are single-ended and internally biased to the REFBUF voltage (nominally 2.2 V). The REFBUF output pin can be used to level shift an input signal centered around 0 Volts as shown in Figure 2. The input buffers shown have a gain of 0.5, yielding a full scale input sensitivity of 2 V_{rms} with the CS4216 programmable gain set to 0. If the source impedance is very low, then the inputs can be AC coupled with a series 0.47 µF capacitor, eliminating the need for external op-amps (see Figure 3). However, the use of AC coupling capacitors will increase DC offset at 0dB gain (see Analog Characteristics Table).

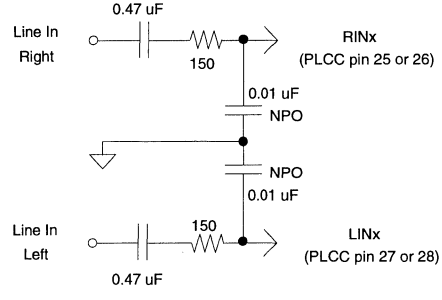


Figure 3. AC Coupled Input

The analog outputs are also single-ended and centered around the REFBUF pin. AC coupling capacitors of >1 µF are recommended.

Offset Calibration

Both input and output offset voltages are minimized by internal calibration. Offset calibration occurs after exiting a reset or power down condition. During calibration, which takes 194 frames, output data from the ADCs will be all zeros, and will be flagged as invalid. Also, the DAC outputs will be muted. After power down mode or power up, $\overline{\text{RESET}}$ should be held low for a minimum of 50 ms to allow the voltage reference to settle.

Input Gain and Output Level Setting

Input gain is adjustable from 0 dB to +22.5 dB in 1.5 dB steps. In serial modes SM1 and SM2, the output level attenuation is adjustable from 0 dB to -22.5 dB. In serial modes SM3 and SM4, the output level attenuation is adjustable from 0 dB to -46.5 dB. Both input and output gain adjustments are internally made on zero-crossings of the analog signal, to minimize "zipper" noise. The gain change automatically takes effect if a zero crossing does not occur within 512 frames.

Muting and the ADC Valid Counter

The mute function allows the output channels to be silenced. It is the controlling processor's responsibility to reduce the signal level to a low value before muting, to avoid an audible click. The outputs should be muted before changing the sample frequency.

The serial data stream contains a "Valid Data" indicator for the A/D converters which is false until enough clocks have passed since reset, or low-power (power down mode) operation to have valid A/D data from the filters, i.e., until calibration time plus the full latency of the digital filters has passed.

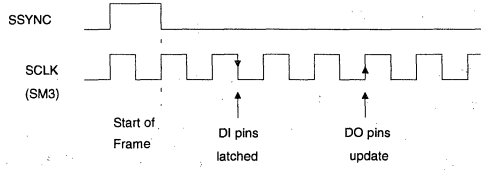


Figure 4. Digital Input/Output Timing

Parallel Digital Input/Output Pins

Parallel digital inputs are general purpose pins whose value is reflected in the serial data output stream to the processor. Parallel digital outputs provide a way to control external devices using bits in the serial data input stream. All parallel digital pins, with the exception of DI1 and DO1, are multifunction and are defined by the serial mode selected. Serial modes 1 and 2 define all multifunction pins as general purpose digital inputs and outputs. In Serial mode 3 only two digital inputs and two digital outputs are available. In serial mode 4 only one digital input and digital output exists. Figure 4 shows when the DI pins are latched, and when the DO pins are updated in SM3 and SM4.

Reset and Power Down Modes

Reset places the CS4216 into a known state and must be held low for at least 50 ms after power-up or a hard power down. Reset must also occur when the codec is in master mode and a change in sample frequency is desired. In reset, the digital outputs are driven low. Reset sets all control data register bits to zero.

Hard power down mode may be initiated by bringing the $\overline{\text{PDN}}$ pin low. All analog outputs will be driven to the REFBUF voltage which will then decay to zero. All digital outputs will be driven low and then will go to a high impedance state. Minimum power consumption will occur if CLKIN is held low. After leaving the power down state, $\overline{\text{RESET}}$ should be held low for 50 ms to allow the analog voltage reference to settle before calibration is started.

Alternatively, soft power down may be initiated, in slave mode, by reducing the SCLK frequency below the minimum CLKIN/12. In soft power down the analog outputs are muted and the serial data from the codec will indicate invalid data and the appropriate error code. The parallel bit I/O is still functional in soft power down mode. This is, in effect, a low power mode with only the parallel bit I/O unit functioning.

Audio Serial Interface

In serial modes 1, 2, and 3, the audio serial port uses 4 pins: SDOUT, SDIN, SCLK and SSYNC. SDIN carries the D/A converters' input data and control bits. Input data is ignored for frames not allocated to the selected CS4216. SDOUT carries the A/D converters' output data and status bits. SDOUT goes to a high-impedance state during frames not allocated to the selected CS4216. SCLK clocks data in to and out of the CS4216. The rising edge of SCLK clocks data out on SDOUT. The falling edge latches data on SDIN into the port (SCLK polarity is inverted in Serial Modes 1&2). SSYNC indicates the start of a frame and/or sub-frame. SCLK and SSYNC must be synchronous to the master clock.

Serial mode 4 is similar to serial mode 3 with the exception of the control information. In serial mode 4 the control information is entered through a separate asynchronous control port. Therefore, the audio serial port only contains audio data which reduces the number of bits on the audio port from 64 to 32 per codec.

The serial port protocol is based on frames consisting of 1, 2, or 4 sub-frames. The frame rate is the system sample rate. Each sub-frame is used by one CS4216 device. Up to 4 CS4216s may be attached to the same serial control lines. SFS1 and SFS2 are tied low or high to indicate to each CS4216 which sub-frame is allocated for it to use.

Serial Data Format

In serial modes 1, 2, and 3, a sub-frame is 64 bits in length and consists of two 16-bit audio values and two 16-bit control fields. In serial mode 4 a sub-frame is 32 bits in length and only contains the two 16-bit audio values; the control data is loaded through a separate port. The audio data is MSB first, 2's complement format. The sub-frame bit assignments for serial modes 1, 2, and 3, are numbered 1 through 64 and are shown in Figures 5 and 6. Control data bits all reset to zero.

CS4216 SERIAL INTERFACE MODES

The CS4216 has 4 serial port modes, selected by the SMODE1, SMODE2 and SMODE3 pins. In all modes, CLKIN, SCLK and SSYNC must be derived from the same clock source. SM1 is an easy interface to ASICs that use a change in the SCLK-to-CLKIN ratio to determine the sample

SMODE PINS			Serial	SCLK Bit	Sub-frame	Bits per	SCLK &	Master
3	2	1	Mode	Center	Width	Frame (BPF)	SSYNC	Frequency
0	0	0	SM1	Rising	64 bits	256	Slave	CLKIN = 512xFs
0	0	1	SM2	Rising	64 bits	256	Slave	SCLK = 256xFs
0	1	0	SM3	Falling	64 bits	64/128/256	Master/Slave	CLKIN/SCLK = 256xFs
0	1	1	**Factory Test mode**					
1	x	x	SM4	Falling	32 bits†	32/64/128†	Master/Slave	CLKIN = 256xFs

†Contains audio data only. Control information is entered through a separate serial port.

Table 1. Serial Port Modes

INPUT DATA BIT DEFINITIONS

Sub-frame bits 1 to 16

Left DAC Audio Data, MSB first, 2's complement coded.

Sub-frame Bits 17 to 24

17	18	19	20	21	22	23	24
0	0	0	0	EXP	MUTE	ISL	ISR

EXP Expand bit
Reserved. Must be set to zero.

MUTE Mute D/A Outputs
0 - Normal Outputs
1 - Mute Outputs

ISL Select Left Input Mux
0 - Select LIN1
1 - Select LIN2

ISR Select Right Input Mux
0 - Select RIN1
1 - Select RIN2

Sub-frame Bits 25 to 32

25	26	27	28	29	30	31	32
LG3	LG2	LG1	LG0	RG3	RG2	RG1	RG0

LG3-LG0 Sets left input gain.
LG3 is the MSB. LG0 represents 1.5 dB.
0000 = no gain.
1111 = +22.5 dB gain

RG3-RG0 Sets right input gain.
RG3 is the MSB. RGO represents 1.5 dB.
0000 = no gain

Sub-frame Bits 33 to 48

Right DAC audio data MSB first, 2's complement coded.

Sub-frame Bits 49 to 50

Must be zero.

Sub-frame Bits 51 to 60

	51	52	53	54	55	56	57	58	59	60
*	LA4	LA3	LA2	LA1	LA0	RA4	RA3	RA2	RA1	RA0
†	0	0	LA3	LA2	LA1	LA0	RA3	RA2	RA1	RA0

LA4-LA0 Sets left output attenuation

†SM1, 2	*SM3,4
LA3 is the MSB.	LA4 is the MSB.
0000 = no attenuation	00000 = no attenuation
1111 = -22.5 dB	11111 = -46.5 dB
LA0 represents 1.5 dB.	

RA4-RA0 Sets right output attenuation

†SM1, 2	*SM3,4
RA3 is the MSB.	RA4 is the MSB.
0000 = no attenuation	00000 = no attenuation
1111 = -22.5 dB	11111 = -46.5 dB
RA0 represents 1.5 dB.	

Sub-frame Bits 61 to 64

61	62	63	64
DO1	DO2	DO3	DO4

DO1-DO4 Set the logic level on the 4 digital output pins. In SM3 DO3 and DO4 are not available. In SM4 DO2, DO3, & DO4 are not available.

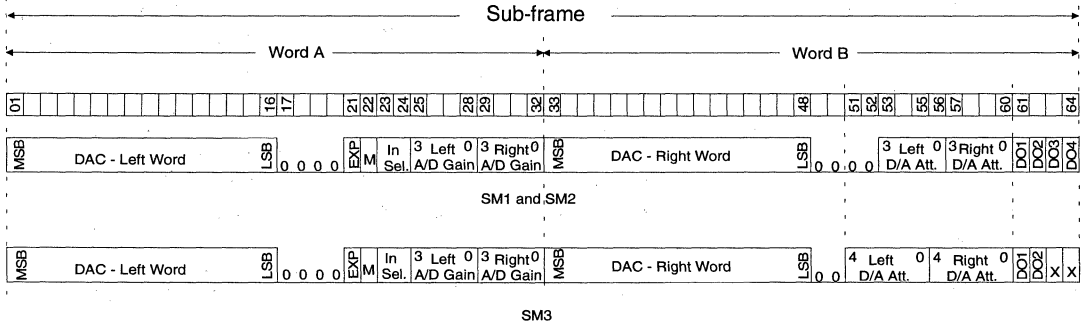


Figure 5. Serial Data Input Format - SM1, SM2, and SM3.

OUTPUT DATA BIT DEFINITIONS

Sub-frame Bits 1 to 16

Left ADC Audio Data, MSB first, 2's complement coded.

Sub-frame Bits 17 to 24

17	18	19	20	21	22	23	24
RESERVED				0	ADV	LCL	RCL

ADV ADC Valid data bit.
0 - Invalid ADC data
1 - Valid ADC data
Indicates ADC has completed initialization after power-up, low power mode, or mute.

LCL Left ADC clipping indicator
0 - Normal
1 - Clipping

RCL Right ADC clipping indicator
0 - Normal
1 - Clipping

RESERVED bits can be 0 or 1

Sub-frame Bits 25 to 32

25	26	27	28	29	30	31	32
ER3	ER2	ER1	ER0	Ver3	Ver2	Ver1	Ver0

ER3-ER0 Error Word
0000 - Normal – No errors.
0001 - Input Sub-frame Bit 21 is set. Control data will not be loaded
0010 - Sync Pulse is incorrect. Causes the analog output to mute.
0011 - SCLK is outside the allowable range. Analog output mutes.

Ver3-Ver0 CS4216 Version Number
0000 = "A" (see Appendix A)
0001 = "B", "C", . . . (This data sheet)

Sub-frame Bits 33 to 48

Right ADC Audio Data, MSB first, 2's complement coded.

Sub-frame Bits 49 to 60

These bits are reserved, and can be 0 or 1.

Sub-frame Bits 61 to 64

61	62	63	64
DI1	DI2	DI3	DI4

DI1-DI4 These bits follow the state of the Digital Input pins. In SM3 DI3 and DI4 are used and unavailable. In SM4 DI2, DI3, & DI4 are not available as input bits.

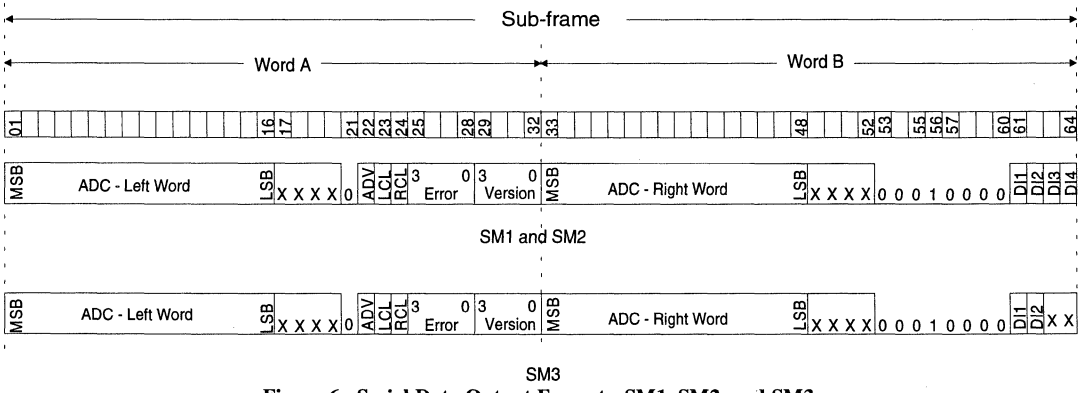


Figure 6. Serial Data Output Format - SM1, SM2, and SM3.

frequency. SM2 is similar to SM1 except that CLKIN is not used and SCLK becomes the master clock and is fixed at 256×Fs. SM3 was designed as an easy interface to general purpose DSPs and provides extra features such as one more bit of attenuation, a master mode, and variable frame sizes. SM4 is similar to SM3 but splits the audio data from the control data thereby reducing the audio serial bus bandwidth by half. The control data is transmitted through a control serial port in SM4.

Table 1 lists the serial port modes available, along with some of the differences between modes. The first three columns in Table 1 select the serial mode. The "SCLK Bit Center" column indicates whether SCLK is rising or falling in the center of a bit period. The "Sub-frame Width" column indicates how many bits are in an individual codec's sub-frame. SM4 differs from all other modes by separating the control data from the audio data. In both SM1 and SM2, there are 256 bits per frame which allows up to four codecs to occupy the same bus. In SM3 and SM4, the number of bits per frame is programmable. In SM1 and SM2, SCLK and SSYNC must be generated externally; whereas, in SM3 and SM4 the CS4216 can optionally generate those signals. In all modes, SCLK and SSYNC must be synchronous to the master clock. The last column in Table 1 lists the master frequency used by the codec. In SM1, the master frequency, input on CLKIN, is 512 times the highest sample frequency available. In SM2, the master frequency is fixed at 256 times the sample frequency and, in this mode, SCLK is the master clock. In SM3, the master frequency is 256 times the highest frequency available and is input on CLKIN or SCLK, based on the submode used. In SM4, the master frequency is also 256 times the highest frequency available and is input on CLKIN.

SERIAL MODE 1, SM1

Serial Mode 1 is a slave mode selected by setting SMODE3 = SMODE2 = SMODE1 = 0. SCLK and SYNC must be synchronous the master clock. SM1 uses a two bit wide (minimum) frame sync with an optional word sync. In this mode, SSYNC low for one SCLK period followed by SSYNC high for a minimum of two SCLK periods indicates the beginning of a frame. The first bit of the frame starts with the rising edge of SSYNC. An optional word sync, being one SCLK period high, may be used to indicate the start of a new 32-bit word. Figures 5 and 6 contain the serial data format for SM1. In this serial mode, the ratio of two clocks are used to select sample frequency. These are the master clock CLKIN and the serial clock SCLK. CLKIN should be set to $512 \times Fs_{max}$, where Fs_{max} is the maximum required sample rate. SCLK must be externally set to a value of CLKIN/N, such that SCLK equals 256 times the desired sample rate. The codec uses the ratio between CLKIN and SCLK to set the internal sample frequency and causes the CS4216 to go into soft power down mode if the SCLK frequency drops to <CLKIN/12. Even if only 1 CS4216 is used, the timing for 4 devices must be maintained. Table 2 shows some example sample rates for SM1.

Sample Rate kHz	SCLK MHz	CLKIN MHz	N
48	12.288	24.576	2
32	8.192	24.576	3
24	6.144	24.576	4
19.2	4.9152	24.576	5
16	4.096	24.576	6
12	3.072	24.576	8
9.6	2.4576	24.576	10
8	2.048	24.576	12
7.2	1.843	22.116	12
44.1	11.2896	22.5792	2

Table 2. SM1 - Example Clock Frequencies

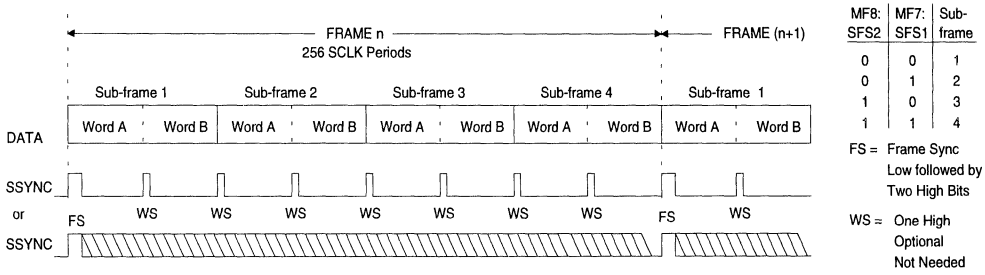


Figure 7. SM1, SM2 - 256 Bits per Frame.

SERIAL MODE 2, SM2

Serial Mode 2 is enabled by setting SMODE3 = SMODE2 = 0, and SMODE1 = 1. SM2 is similar to SM1 except that SCLK is fixed at 256 × Fs and is the master clock instead of CLKIN. The CLKIN pin is ignored in this mode and should be tied low. In SM2, the sample frequency will scale linearly with the frequency of SCLK. Up to four codecs may occupy the serial bus since each codec requires only 64 bit periods and a frame is fixed at 256 bit periods. The serial data format is the same as SM1 and is illustrated in Figures 5 and 6.

The multifunction pins in SM2 are defined identically to SM1. See *Serial Mode 1, SM1* section for more details.

SERIAL MODE 3, SM3

Serial Mode 3 is enabled by setting SMODE3 = 0, SMODE2 = 1 and SMODE1 = 0. This mode is designed to interface easily to DSPs and has the added versatility of a programmable number of bits per frame, a master mode, and one extra bit of D/A attenuation. In SM3, two of the parallel digital input bits and two of the parallel digital output bits are available.

Master Clock Frequency

In SM3, the master clock, CLKIN, must be $256 \times Fs_{max}$. For example, given a 48 kHz maximum sample frequency, the master clock frequency must be 12.288 MHz. SCLK and SSYNC must be synchronous to CLKIN.

D/A Attenuation

SM3 has one more bit per channel allocated for D/A attenuation which doubles the attenuation range. Figure 5 illustrates the serial data in, SDIN, sub-frame for all SM3 sub-modes. The upper portion of this figure shows modes SM1 and SM2 where the D/A attenuation is located in Word B, bits 53 through 60. Four bits allow attenuation on each channel from 0 dB down to -22.5 dB using 1.5 dB steps. In SM3 the attenuation bits are still located in Word B, but start at bit 51 of the sub-frame. This allows five bits of attenuation per channel instead of four, producing an attenuation range for each channel from 0 dB down to -46.5 dB.

In SM3 MF5:DO2 is a general purpose output and MF6:DI2 is a general purpose input. The other six multifunction pins are used to select sub-modes under SM3.

SM3 is divided into two sub-modes, Master and Slave. In Master sub-mode, the CS4216 generates SSYNC and SCLK, while in Slave sub-mode SSYNC and SCLK must be generated

externally. In Master sub-mode, the serial port signal transitions are controlled with respect to the internal analog sampling clock to minimize the amount of digital noise coupled into the analog section. Since SSYNC and SCLK are externally derived in Slave sub-mode, optimum noise management cannot be obtained; therefore, Master sub-modes should be used whenever possible.

Master Sub-Mode (SM3)

Master sub-mode is selected by setting MF4:MA = 1, which configures SSYNC and SCLK as outputs from the CS4216. During power down, SSYNC and SCLK are driven high impedance, and during reset they both are driven low. In Master sub-mode the number of bits per frame determines how many codecs can occupy the serial bus and is illustrated in Figure 8.

Bits Per Frame (Master Sub-Mode)

MF8:SFS2 selects the number of bits per frame. The two options are MF8:SFS2 = 1 which selects 128 bits per frame, and MF8:SFS2 = 0 which selects 64 bits per frame.

Selecting 128 bits per frame (MF8:SFS2 = 1) allows two CS4216s to operate from the same serial bus since each codec requires 64 bit periods. The sub-frame used by an individual codec is selected using MF7:SFS1. MF7:SFS1 = 0 selects sub-frame 1 which is the first 64 bits following the SSYNC pulse. MF7:SFS1 = 1 selects sub-frame 2 which is the last 64 bits of the frame.

Selecting 64 bits per frame (MF8:SFS2 = 0) allows only one CS4216 to occupy the serial port. Since there is only one sub-frame (which is equal to one frame), MF7:SFS1 is defined differently in this mode. MF7:SFS1 selects the format of SSYNC. MF7:SFS1 = 0 selects an SSYNC pulse one SCLK period high, directly preceding the data as shown in the center portion of Figure 8. This format is used for all other Master and Slave sub-modes in SM3. If MF7:SFS1 = 1, an alternate SSYNC format is chosen in which SSYNC is high during the entire Word A (32 bits), which includes the left sample, and low for the entire Word B (32 bits), which includes the right sample. This alternate format for SSYNC is illustrated in the bottom portion of Figure 8 and is only available in Master sub-mode with 64 bits per frame. A more detailed timing diagram for the 64 bits-per-frame Master sub-mode is shown in Figure 9.

Sample Frequency Selection (Master Sub-Mode)

In SM3, Master sub-mode, the multifunction pins MF1:F1, MF2:F2, and MF3:F3 are used to select the sample frequency divider. Table 3 lists the decoding for the sample frequency select pins where the sample frequency selected is CLKIN/N. Also shown are the sample frequencies obtained by using one of two example master clocks: either 12.288 MHz or 11.2896 MHz. The codec must be reset when changing sample frequencies to allow the codec to calibrate to the new sample frequency.

Slave Sub-Mode (SM3)

In SM3, Slave sub-mode is selected by setting MF4:MA = 0 which configures SSYNC and SCLK as inputs to the CS4216. These two signals must be externally derived from CLKIN. In Slave sub-mode, the phase relationship between SCLK/SSYNC and CLKIN cannot be controlled since SCLK and SSYNC are externally derived. Therefore, the noise performance may be slightly worse than when using the master sub-mode.

The number of sub-frames on the serial port is selected using MF1:F1 and MF2:F2. In Slave sub-mode MF3:F3 works as a general purpose input. Figures 10 through 12 illustrate the Slave sub-mode formats.

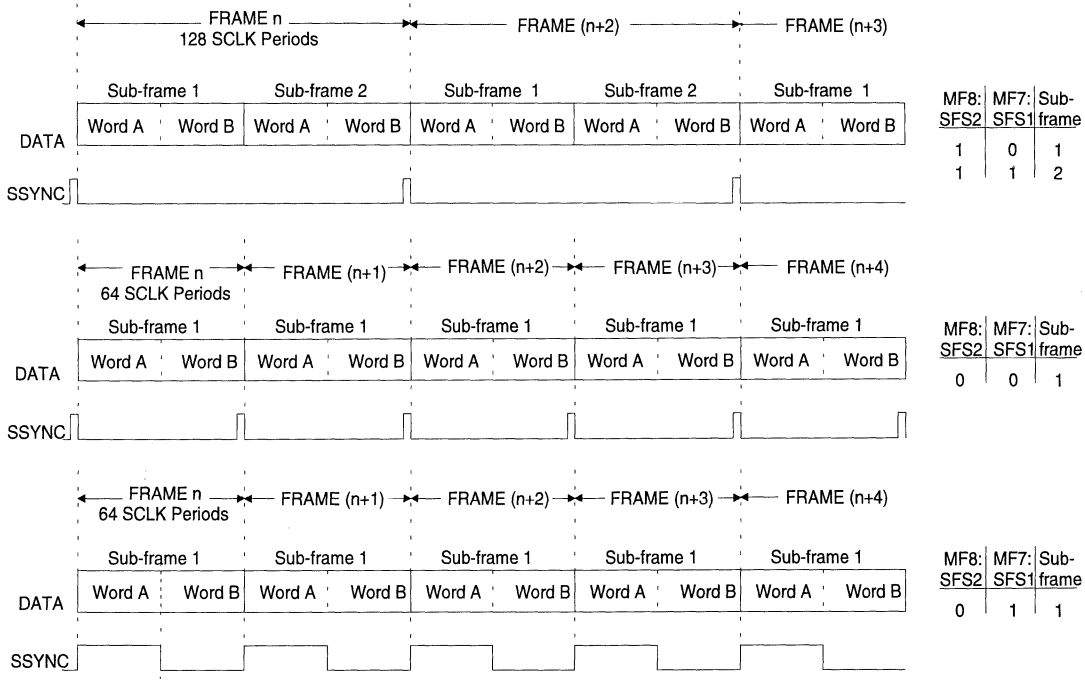


Figure 8. SM3, Master Sub-Mode.

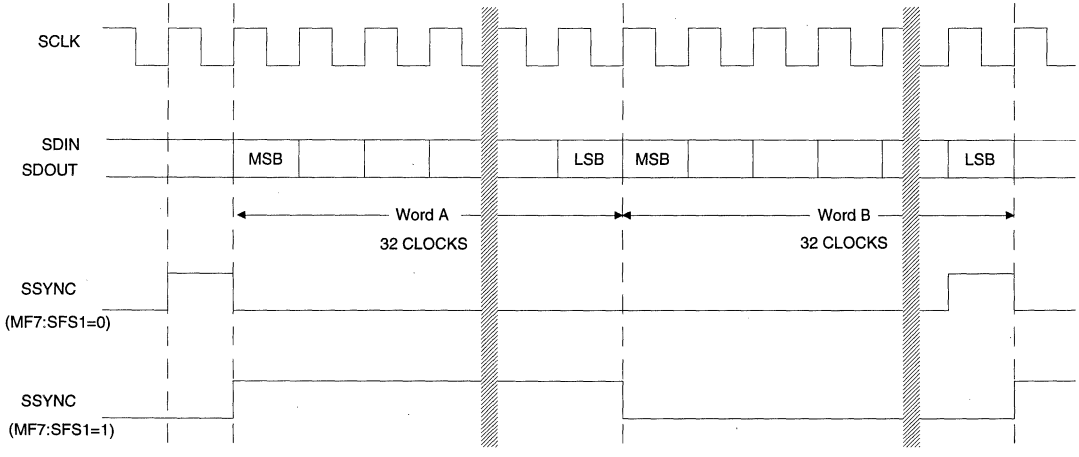


Figure 9. Detailed Master Sub-Mode, 64 BPF.

Bits per Frame (Slave Sub-Mode)

In Slave sub-mode, MF1:F1 and MF2:F2 select the number of bits per frame which determines how many CS4216's can occupy one serial port. Table 4 lists the decoding for MF1:F1 and MF2:F2.

When set for 64 SCLKs per frame, one device occupies the entire frame; therefore, a sub-frame is equivalent to a frame. MF7:SFS1 and MF8:SFS2 must be set to zero. See Figure 10.

When set for 128 SCLKs per frame, two devices can occupy the serial port, with MF7:SFS1 selecting the particular sub-frame. MF8:SFS2 must be set to zero. See Figure 11.

When set for 256 SCLKs per frame (MF1:F1, MF2:F2 = 10), four devices can occupy the serial port. In this format both MF8:SFS2 and MF7:SFS1 are used to select the particular sub-frame. See Figure 12.

In all three of the above Slave sub-mode formats, the frequency of the incoming SCLK signal, in relation to the master clock provided on the CLKIN pin, determines the sample frequency. The CS4216 determines the ratio of SCLK to CLKIN and sets the internal operating frequency accordingly. Table 5 lists the SCLK to CLKIN frequency ratio used to determine the codec's sample frequency. To obtain a given sample frequency, SCLK must equal CLKIN divided by the number in the table, based on the number of bits per frame. As an example, assuming 64 BPF (bits per frame) and CLKIN = 12.288 MHz, if a sample frequency of 24 kHz is desired, SCLK must equal CLKIN divided by 8 or 1.536 MHz.

When MF1:F1 = MF2:F2 = 1, SCLK is used as the master clock and is assumed to be 256 times the sample frequency. In this mode, CLKIN is ignored and the sample frequency is linearly scaled with SCLK. (The CLKIN pin must be tied low.) This mode also fixes SCLK at 256 bits per frame with MF7:SFS1 and MF8:SFS2 selecting the particular sub-frame.

MF1: F1	MF2: F2	MF3: F3	N	Fs (kHz) with CLKIN	
				12.288 MHz	11.2896 MHz
0	0	0	256	48.00	44.10
0	0	1	384	32.00	29.40
0	1	0	512	24.00	22.05
0	1	1	640	19.20	17.64
1	0	0	768	16.00	14.70
1	0	1	1024	12.00	11.025
1	1	0	1280	9.60	8.82
1	1	1	1536	8.00	7.35

Table 3. SM3-Master, Fs Select

MF1: F1	MF2: F2	Bits per Frame	Sample Frequency/ SCLK
0	0	64	ratio to CLKIN sensed
0	1	128	ratio to CLKIN sensed
1	0	256	ratio to CLKIN sensed
1	1	256	fixed†. = 256×Fs

† SCLK is master clock. CLKIN is not used.

Table 4. SM3-Slave, Bits per Frame.

SCLK to CLKIN Ratio			Fs (kHz) with CLKIN	Fs (kHz) with CLKIN
BPF 256	BPF 128	BPF 64	12.288 MHz	11.2896 MHz
1	2	4	48.00	44.10
1.5	3	6	32.00	29.40
2	4	8	24.00	22.05
2.5	5	10	19.20	17.64
3	6	12	16.00	14.70
4	8	16	12.00	11.025
5	10	20	9.60	8.82
6	12	24	8.00	7.35

Table 5. SM3-Slave, Fs Select.

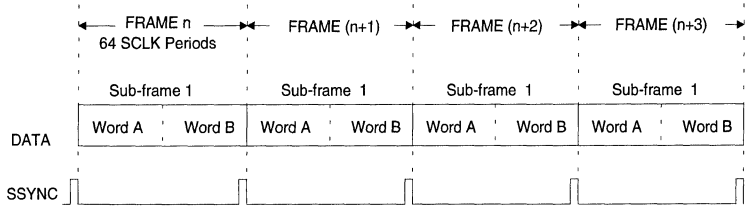
SERIAL MODE 4, SM4

Serial mode 4 is enabled by setting SMODE3 = 1. Both Master and Slave sub-modes are available and are selected by setting the SMODE2 and SMODE1 pins as shown in Table 6. In Master sub-mode, the phase relationship between SCLK/SSYNC and CLKIN is controlled to minimize digital noise coupling into the analog section. Therefore, Master sub-mode may yield slightly better noise performance than Slave sub-mode. In Slave sub-mode, SCLK and SSYNC must be synchronous to the master clock.

In serial mode 4, SM4, the CLKIN frequency must be 256 times the highest sample frequency needed. Also, SM4 has five attenuation bits for each D/A output channel. SM4 differs from SM3 in that SM4 splits the audio data from the control data with the control data input on an independent serial port. This reduces the audio serial bus bandwidth in half, providing an easier interface to low-cost DSPs. The audio serial port sub-frame is illustrated in Figure 13 for SM4.

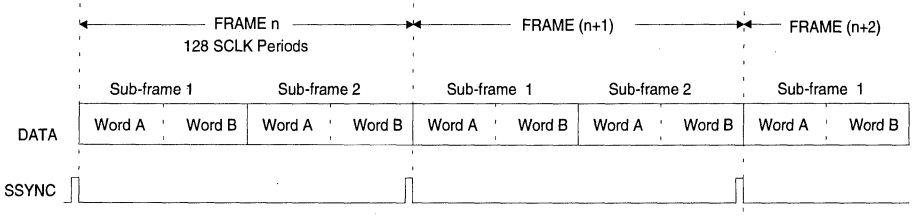
Interrupt Pin - MF5:$\overline{INT}$

Serial Mode 4 also defines the multifunction pin MF5:$\overline{INT}$ as an open-collector interrupt pin. In SM4, this pin requires a pullup resistor and will go low when the ADV bit or DI1 pin change, or a rising edge on the LCL or RCL bits, or by exiting an SCLK out of range condition (Error = 3). The interrupt may be masked by setting the MSK bit in the control serial data port.



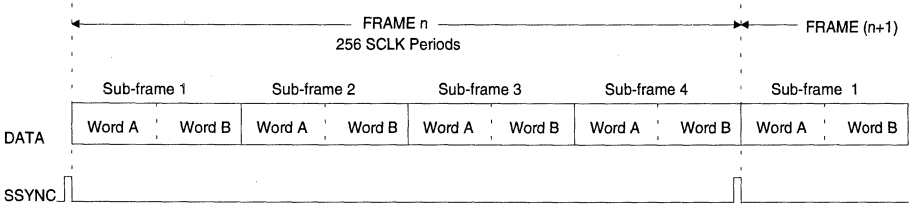
MF8: SFS2	MF7: SFS1	Sub-frame
0	0	1

Figure 10. SM3-Slave - 64 BPF; MF1:F1, MF2:F2 = 00



MF8: SFS2	MF7: SFS1	Sub-frame
0	0	1
0	1	2

Figure 11. SM3-Slave - 128 BPF; MF1:F1, MF2:F2 = 01



MF8: SFS2	MF7: SFS1	Sub-frame
0	0	1
0	1	2
1	0	3
1	1	4

Figure 12. SM3-Slave - 256 BPF; MF1:F1, MF2:F2 = 10

MF5:$\overline{INT}$ is reset by reading the control serial port.

Master Sub-Mode (SM4)

Master sub-mode configures SSYNC and SCLK as outputs from the CS4216. During power down, SSYNC and SCLK are driven high impedance, and during reset they both are driven low. There are two SM4 Master sub-modes. One allows 32 bits per frame and the other allows 64 bits per frame. As shown in Table 6, the SMODE1 and SMODE2 pins select the particular Master sub-mode (as well as the Slave sub-mode). When SMODE1 is set to zero, SMODE2 selects either Master sub-mode with 32-bit frames, or Slave sub-mode.

SMODE1,SMODE2 = 00 selects Master sub-mode where a frame = sub-frame = 32 bits. This sub-mode allows only one codec on the audio serial bus, with the first 16 bits being the left channel and the second 16 bits being the right channel. The *Applications of SM4* section contains more information on low-cost implementations of this sub-mode.

SMODE1	SMODE2	SM4, Sub-Mode
0	0	Master, 32 BPF
0	1	Slave, 128/64/32 BPF
1	0	Master, 64 BPF, TS1
1	1	Master, 64 BPF, TS2

Table 6. SM4 Sub-Modes.

SMODE1 = 1 selects Master sub-mode with a frame width of 64 bits. This sub-mode allows up to two codecs to occupy the same bus. SMODE2 is now used to select the particular time slot. If SMODE2 = 0 the codec selects time slot 1, which is the first 32 bits. If SMODE2 = 1 the codec selects time slot 2, which is the second 32 bits.

In Master sub-mode, multifunction pins MF6:F1, MF7:F2, and MF8:F3 select the sample frequency as shown in Table 7. This table indicates how to obtain standard audio sample frequencies given one of two CLKIN frequencies: 12.288 MHz or 11.2896 MHz. Other CLKIN frequencies may be used with the corresponding sample frequencies being CLKIN/N. The codec must be reset when changing sample frequencies to allow a new calibration to occur.

Slave Sub-Mode (SM4)

In SM4, Slave sub-mode is selected by setting SMODE1,SMODE2 = 01. This mode configures SSYNC and SCLK as inputs to the CS4216. These two signals must be externally derived from CLKIN. Since the CS4216 has no control over the phase relationship of SSYNC and

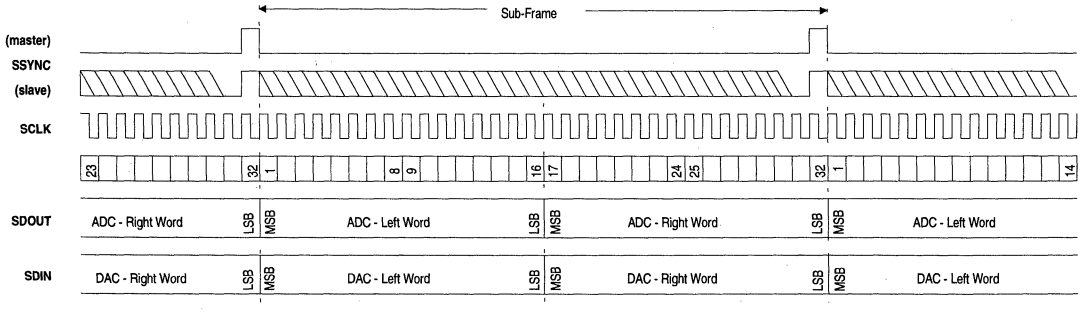


Figure 13. SM4-Audio Serial Port, 32 BPF

SCLK to CLKIN, the noise performance in Slave sub-mode may be slightly worse than when using Master sub-mode. The CS4216 internally sets the sample frequency by sensing the ratio of SCLK to CLKIN; therefore, for a given CLKIN frequency, the sample frequency is selected by changing the SCLK frequency.

SM4-Slave allows up to four codecs to occupy the same audio serial port. Table 8 lists the pin configurations required to set the serial audio port up for 32, 64, or 128 bits-per-frame (BPF). Since each codec requires one sub-frame of 32 bits, 64 bits-per-frame allows up to two codecs to occupy the same audio serial port, and 128 bits-per-frame allows up to four codecs to occupy the same audio serial port. When set up for more than one codec on the bus, other pins are needed to select the particular time slot (TS) associated with each codec. MF8:SFS2 selects the time slot when in 64 BPF mode, and MF8:SFS2 and MF7:SFS1 select one of four time slots when in 128 bits-per-frame mode. Table 8 lists the decoding for time slot selection.

In SM4-Slave, the frequency of the incoming SCLK signal, in relation to CLKIN, determines the sample frequency on the CS4216. The CS4216 determines the ratio of SCLK to CLKIN and sets the internal sample frequency accordingly. Table 9 lists the SCLK to CLKIN frequency ratio used to determine the codec's sample frequency. SCLK must equal CLKIN divided by the number in the table, based on the selected bits per frame. As an example, assuming 32 BPF and CLKIN = 11.2896 MHz, if a sample frequency of 11.025 kHz is desired, SCLK must equal CLKIN divided by 32 or 352.8 kHz.

Serial Control Port (SM4)

Serial Mode 4 separates the audio data from the control data. Since control data such as gain and attenuation do not change often, this mode reduces the bandwidth needed to support the audio serial port.

The control information is entered through a separate port that can be asynchronous to the audio port and only needs to be updated when changes in the control data are needed. After a reset or power down, the control port must be written once to initialize it if the port will be accessed to read or write control bits. This initial write is considered a "dummy" write since the data is ignored by the codec. A second write is needed to configure the codec as desired. Then, the control port only needs to be written to when a change is desired, or to obtain the status information. The control port does not function if the master clock is not operating. When the control

MF6: F1	MF7: F2	MF8: F3	N	Fs (kHz) with CLKIN	
				12.288 MHz	11.2896 MHz
0	0	0	256	48.00	44.10
0	0	1	384	32.00	29.40
0	1	0	512	24.00	22.05
0	1	1	640	19.20	17.64
1	0	0	768	16.00	14.70
1	0	1	1024	12.00	11.025
1	1	0	1280	9.60	8.82
1	1	1	1536	8.00	7.35

Table 7. SM4-Master, Fs Select

MF6: F1	MF7: SFS1	MF8: SFS2	Bits Per Frame (BPF)	Time Slot (TS)
0	0	0	32	1
0	0	1	Reserved	
0	1	0	64	1
0	1	1	64	2
1	0	0	128	1
1	1	0	128	2
1	0	1	128	3
1	1	1	128	4

Table 8. SM4-Slave, Audio Port BPF & TS Select

port is used asynchronously to the audio port, the noise performance may be slightly degraded due to this asynchronous digital noise.

Since control data does not need to be accessed each audio frame, an interrupt pin, MF5:$\overline{INT}$, is included in this mode and will go low when status has changed. The control port serial data format is illustrated in Figure 14. The control port uses one of the multifunction pins as a chip select line, MF4:$\overline{CCS}$, that must be low for entering control data. Although only 23 bits contain useful data on MF2:CDIN, a minimum of 31 bits must be written. If more than 31 bits are written without toggling MF4:$\overline{CCS}$, only the first 31 are recognized. MF1:CDOUT contains status information that is output on the rising edge of MF3:CCLK. Status information is repeated at the end of the frame, bits 25 through 30, to allow a simple 8-bit shift and latch register to store the most important status information using the rising edge of MF4:$\overline{CCS}$ at the latch control (see Figure 17).

SCLK to CLKIN Ratio			Fs (kHz)	Fs (kHz)
BPF 128	BPF 64	BPF 32	with CLKIN 12.288 MHz	with CLKIN 11.2896 MHz
2	4	8	48.00	44.10
3	6	12	32.00	29.40
4	8	16	24.00	22.05
5	10	20	19.20	17.64
6	12	24	16.00	14.70
8	16	32	12.00	11.025
10	20	40	9.60	8.82
12	24	48	8.00	7.35

Table 9. SM4-Slave, Fs Select.

Applications of SM4

Figure 15 illustrates one method of using serial mode 4 wherein a DSP controls the audio serial port and a microcontroller controls the control port. Each controller is run independently and the micro updates the control information only when needed, or when an interrupt from the CS4216 occurs.

Figure 16 illustrates the minimum interface to the CS4216. In this application, the DSP sends and receives stereo DAC and ADC information. The CS4216 is configured for 32 bits per frame, Master sub-mode. The control data resets to all zeros, which configures the CS4216 as a simple stereo codec: no gain, no attenuation, line inputs #1, and not muted.

Figure 17 illustrates how to use all the CS4216 features with a low cost DSP that cannot support the interrupt rate of SM3. Using SM4 (32 bits

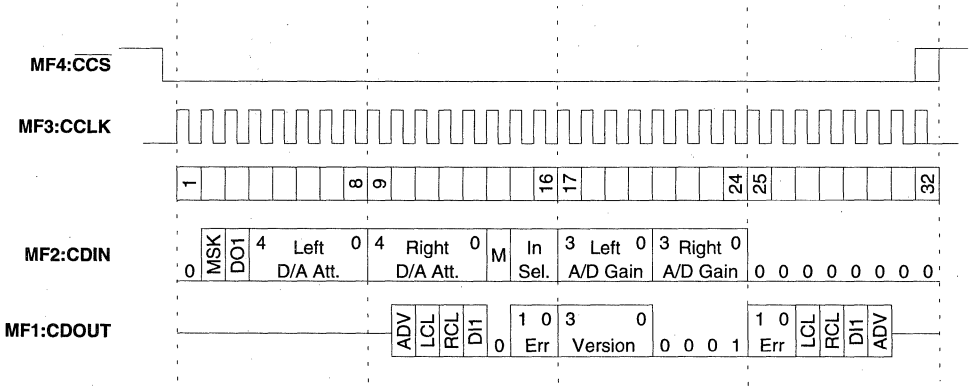


Figure 14. SM4 - Control Serial Port

per frame, Master sub-mode) reduces the DSP interrupts in half since the control data is split from the audio data. This circuit is comprised of three independent sections which may individually be eliminated if not needed.

To load control data into the codec, three HC597's are utilized. These are both latches that store the DSP-sent control data, and shift registers that shift the data into the codec. The codec uses an inverted SSYNC signal to copy the latches to the shift registers every frame. In this diagram the DSP is assumed to have a data bus bandwidth of at least 24 bits. If the DSP has less than 24_bits, the three HC597s must be split into two addresses. Since the HC597 internal latches are copied to the shift registers, the latches continually hold the DSP-sent data; therefore, the DSP only needs to write data to the latches when a change is desired.

The second section is comprised of an HC595 shift register and latch that is clocked by an inverted SCLK The data shifted into the HC595 is transferred to the HC595's latch by the SSYNC signal. This HC595 captures the 8 bits prior to the SSYNC signal (which is also MF4:$\overline{CCS}$) going high. As shown in Figure 14, and assuming the MF4:$\overline{CCS}$ (SSYNC) signal rises at bit 32, the 8-bits prior to MF4:$\overline{CCS}$ rising are a copy of all the important status bits. This allows one shift register to capture all the important information. The interrupt pin cannot reliably be used in this configuration since the interrupt pin is cleared by reading the control port which occurs asynchro-

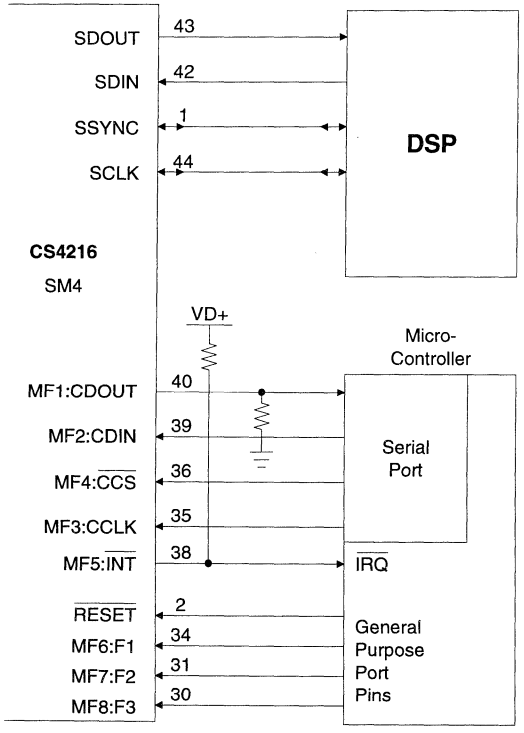


Figure 15. SM4 - Microcontroller Interface

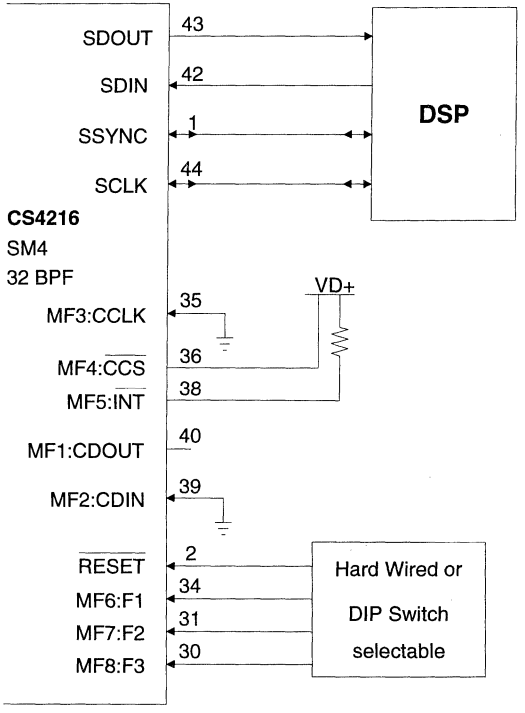


Figure 16. SM4 - Minimum DSP Interface

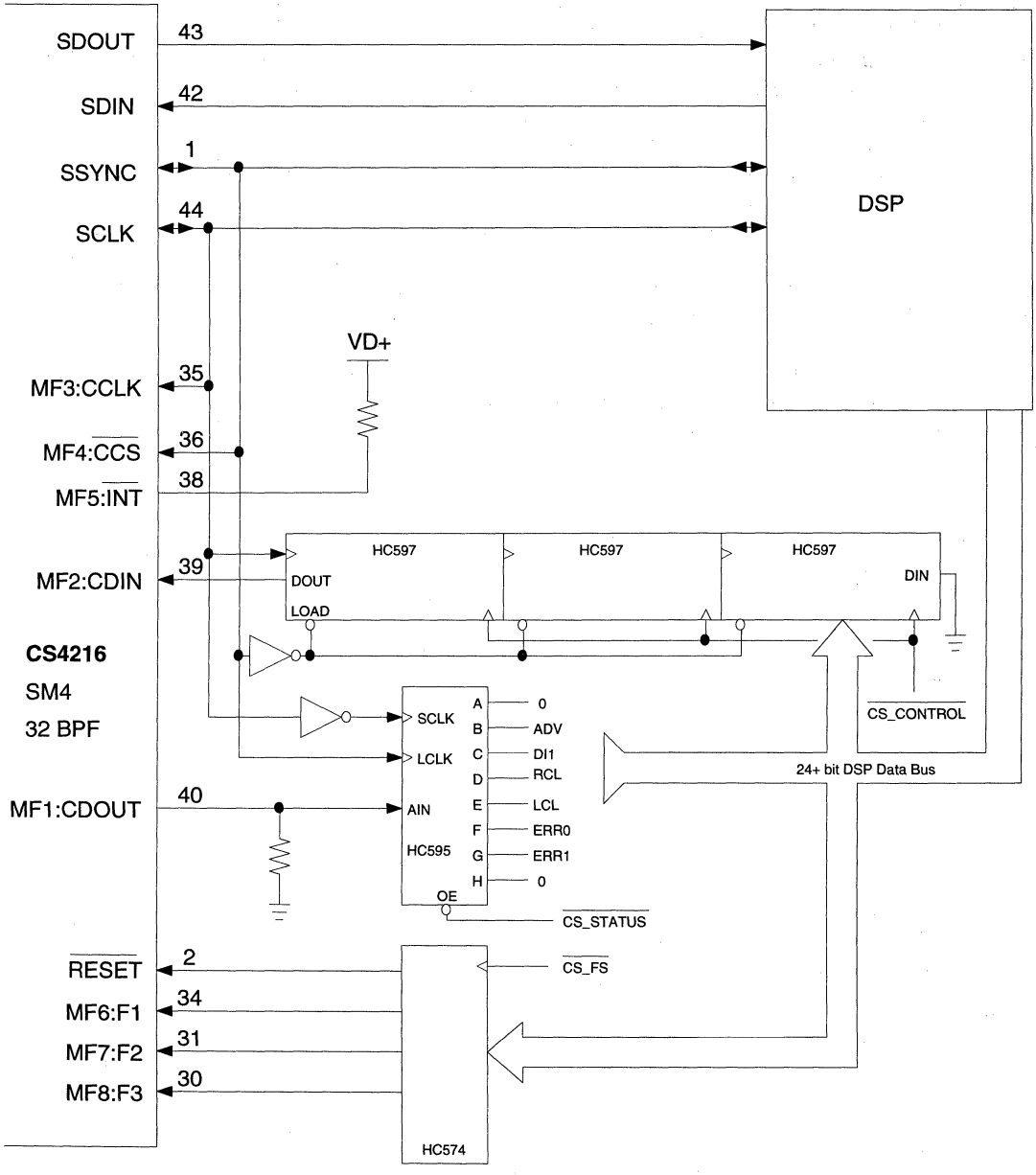


Figure 17. SM4 - Enhanced DSP Interface

nously (every audio frame) with respect to the interrupt occurrence.

The third section is only needed if sample frequencies need to be changed. This section is comprised of an HC574 octal latch that can be replaced by general purpose port pins if available. This section controls the sample frequency selection bits: MF6:F1, MF7:F2, MF8:F3 and the $\overline{\text{RESET}}$ pin. The codec must be reset when changing sample frequencies.

Power Supply and Grounding

The CS4216, along with associated analog circuitry, should be positioned in an isolated section of the circuit board, and have its own, separate, ground plane. On the CS4216, the analog and digital grounds are internally connected; therefore, the AGND and DGND pins must be externally connected with no impedance between them. The best solution is to place the entire chip on a solid ground plane as shown in Figure 18. Preferably, it should also have its own power plane. The +5V supply must be connected to the CS4216 via a ferrite bead, positioned closer than 1" to the device. The VA supply can be derived from VD, as shown in Figure 1. Alternatively, a separate +5V analog supply may be used for VA, in which case, the 2.0 Ω resistor between VA and VD should be removed. A single connection between the CS4216 ground (analog ground) and the board digital ground should be positioned as shown in Figure 18.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4216 assuming a surface-mount socket and leaded decoupling capacitors. Surface-mount sockets are useful since the pad locations are identical to the chip pads; therefore, assuming space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts the top layer, containing signal traces, and assumes the bottom or inter-layer contains a fairly solid ground plane. The important points are that there is solid ground plane under the codec on the same layer as the codec and it connects all ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is placed closest to the codec. Vias are placed near the AGND and DGND pins, under the IC, and should attach to the solid ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces and vias bringing power to the codec should be large, which minimizes the impedance.

Although not shown in the figures, the trace layers (top layer in the figures) should have ground plane fill in-between the traces to minimize coupling into the analog section. See the CDB4216 evaluation board as an example.

If using all surface-mount components, the decoupling capacitors should be placed on the same layer as the codec and in the positions shown in Figure 20. The vias shown are assumed to attach to the appropriate power and ground layers. Traces and vias bringing power to the codec should be as large as possible to minimize the impedance.

If using a through-hole socket, effort should be made to find a socket with minimum height,

which will minimize the socket impedance. When using a through hole socket, the vias under the codec in Figure 19 are not needed since the pins serve the same function.

ADC and DAC Filter Response Plots

Figures 21 - 26 shows the overall frequency response, passband ripple and transition band for the CS4216 ADCs and DACs. Figure 27 shows the DACs' deviation from linear phase.

Fs is defined as the selected sample frequency and is also the SSYNC frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency.

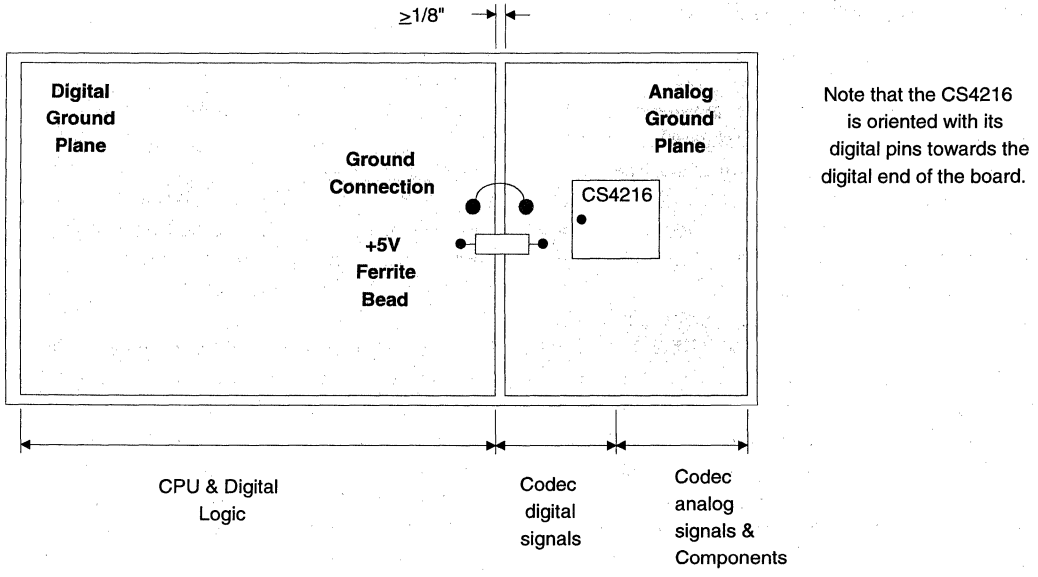


Figure 18. CS4216 Board Layout Guideline

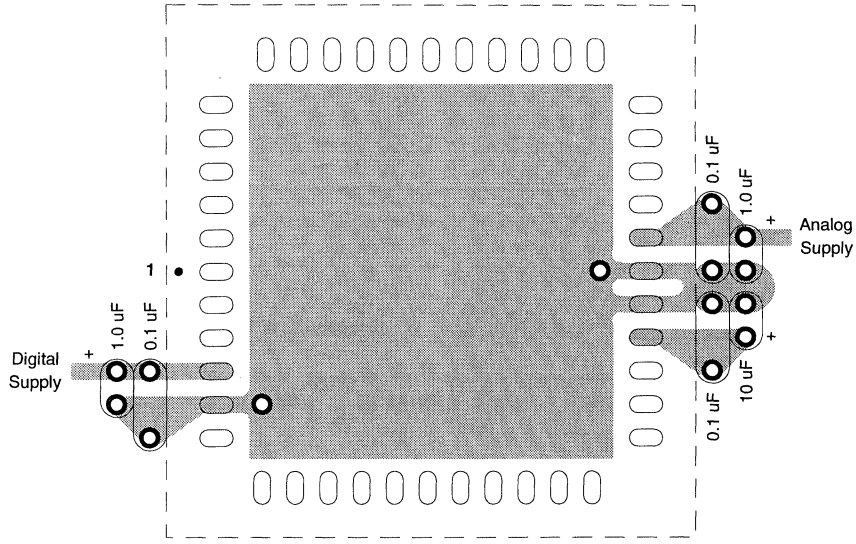


Figure 19. CS4216 Decoupling Layout Guideline

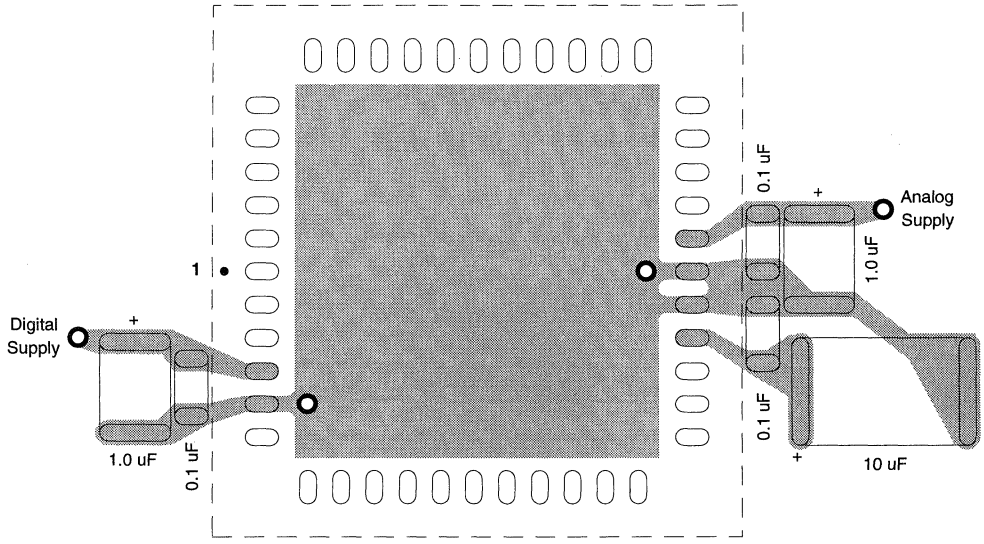


Figure 20. CS4216 Surface Mount Decoupling Layout

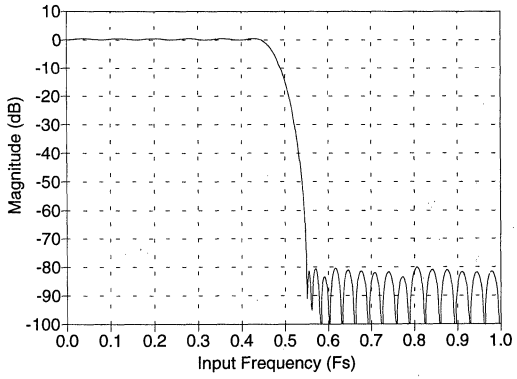


Figure 21. CS4216 ADC Frequency Response

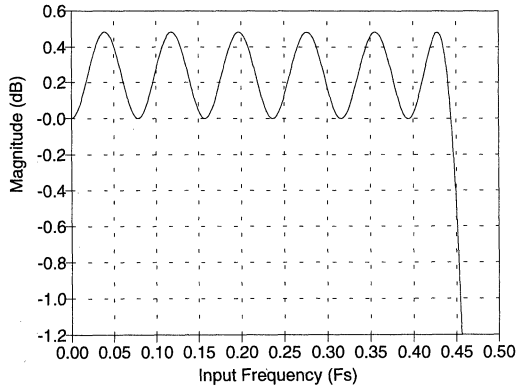


Figure 22. CS4216ADC Passband Ripple

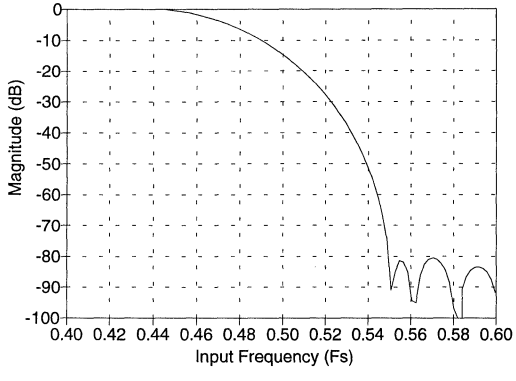


Figure 23. CS4216 ADC Transition Band

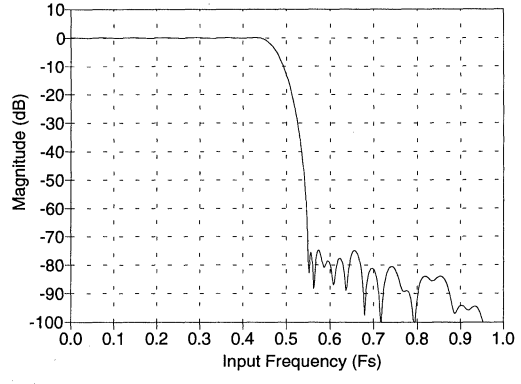


Figure 24. CS4216 DAC Frequency Response

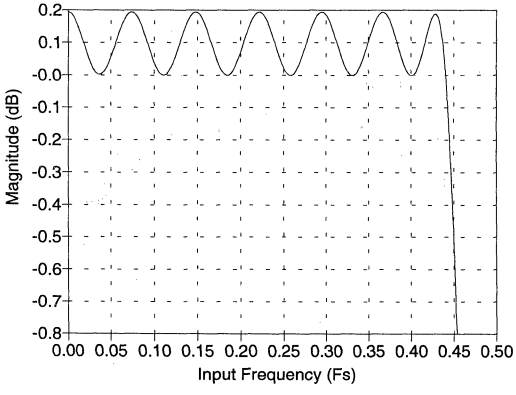


Figure 25. CS4216 DAC Passband Ripple

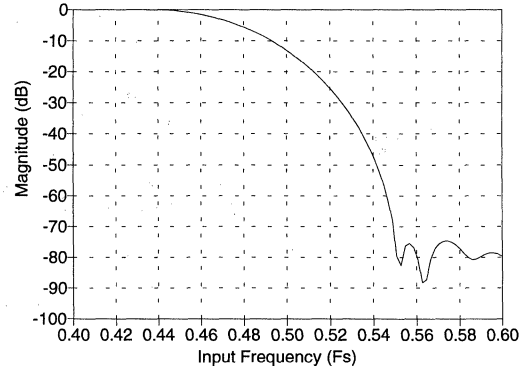


Figure 26. CS4216 DAC Transition Band

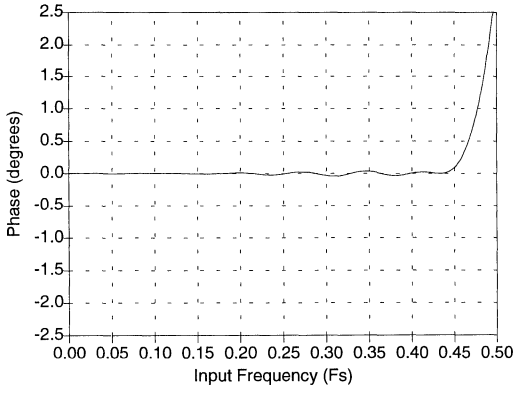
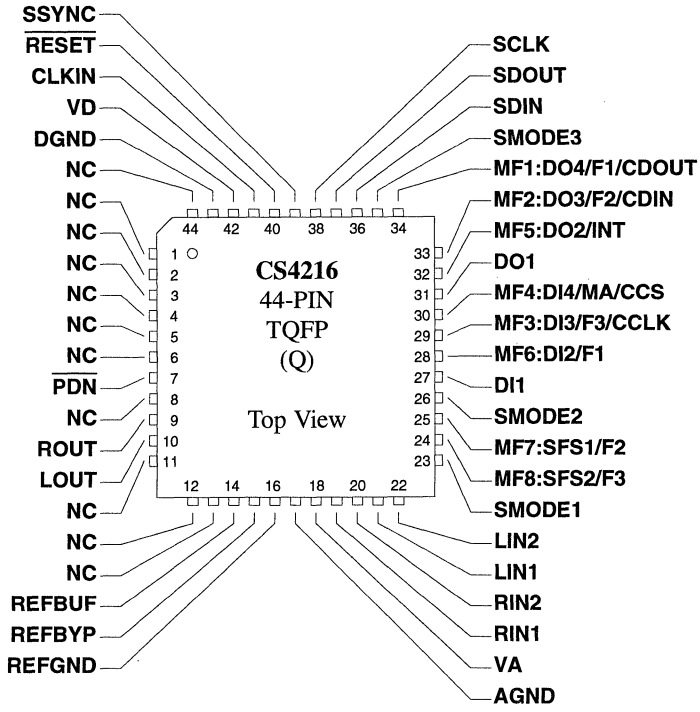
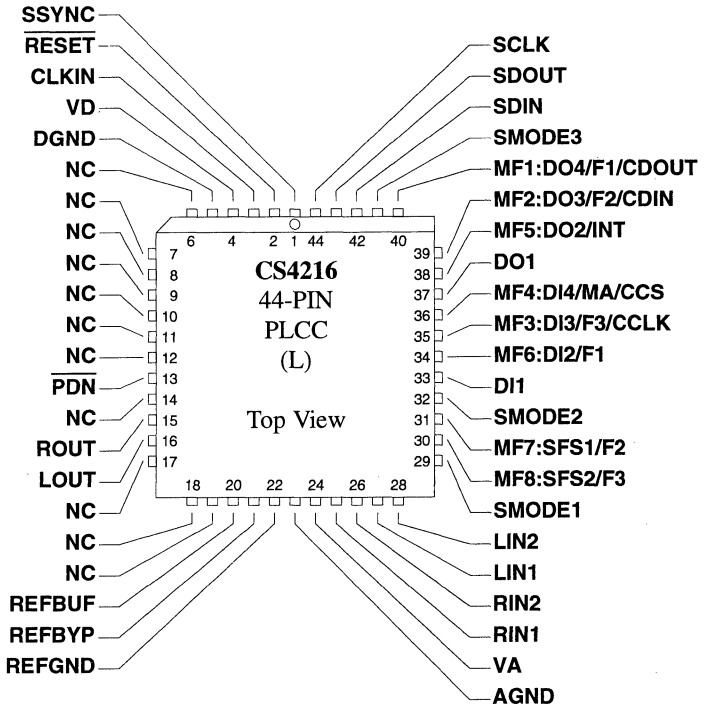


Figure 27. CS4216 DAC Deviation from Linear Phase

PIN DESCRIPTIONS



SM	MF1	MF2	MF3	MF4	MF5	MF6	MF7	MF8
1	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
2	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
3	F1	F2	F3	MA	DO2	DI2	SFS1	SFS2
4-SL	CDOUT	CDIN	CCLK	$\overline{CCS}$	$\overline{INT}$	F1	SFS1	SFS2
4-MA	CDOUT	CDIN	CCLK	$\overline{CCS}$	$\overline{INT}$	F1	F2	F3



SM	MF1	MF2	MF3	MF4	MF5	MF6	MF7	MF8
1	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
2	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
3	F1	F2	F3	MA	DO2	DI2	SFS1	SFS2
4-SL	CDOUT	CDIN	CCLK	$\overline{CCS}$	$\overline{INT}$	F1	SFS1	SFS2
4-MA	CDOUT	CDIN	CCLK	$\overline{CCS}$	$\overline{INT}$	F1	F2	F3

Power Supply

VD - Digital +5V Supply, PIN 4(L), 42(Q).
+5V digital supply.

VA - Analog +5V Supply, PIN 24(L), 18(Q).
+5V analog supply.

DGND - Digital Ground, PIN 5(L), 43(Q).
Digital ground. Must be connected to AGND with zero impedance.

AGND - Analog Ground, PIN 23(L), 17(Q).
Analog ground. Must be connected to DGND with zero impedance.

Analog Inputs

RIN1 - Right Input #1, PIN 25(L), 19(Q).
Right analog input #1. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

RIN2 - Right Input #2, PIN 26(L), 20(Q).
Right analog input #2. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

LIN1 - Left Input #1, PIN 27(L), 21(Q).
Left analog input #1. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

LIN2 - Left Input #2, PIN 28(L), 22(Q).
Left analog input #2. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

Analog Outputs

ROUT - Right Channel Output, PIN 15(L), 9(Q).
Right channel analog output. Maximum signal is 1 Vrms centered at REFBUF.

LOUT - Left Channel Output, PIN 16(L), 10(Q).
Left channel analog output. Maximum signal is 1 Vrms centered at REFBUF.

REFBYP - Analog Reference Decoupling, PIN 21(L), 15(Q).
A 10 µF and 0.1 µF capacitor must be attached between REFBYP and REFGND.

REFGND - Analog Reference Ground Connection, PIN 22(L), 16(Q).
Connect to AGND.

REFBUF - Buffered Reference Out, PIN 20(L), 14(Q).
A nominal +2.2 V output for setting the bias level for external analog circuits.

Serial Digital Audio Interface Signals

SDIN - Serial Port Data In, PIN 42(L), 36(Q).
Digital audio data to the DACs and level control information is received by the CS4216 via SDIN.

SDOUT - Serial Port Data Out, PIN 43(L), 37(Q).
Digital audio data from the ADCs and status information is output from the CS4216 via SDOUT.

SCLK - Serial Port Bit Clock, PIN 44(L), 38(Q).
SCLK controls the digital audio data on SDOUT and latches the data on SDIN.

SSYNC - Serial Port Sync Signal, PIN 1(L), 39(Q).
Indicates the start of a digital audio frame in SM3 and SM4, and also the start of a word in SM1 & SM2.

SMODE1 - Serial Mode Select, PIN 29(L), 23(Q).
One of three pins that select the serial mode and function of the multifunction pins.

SMODE2 - Serial Mode Select, PIN 32(L), 26(Q).
One of three pins that select the serial mode and function of the multifunction pins.

SMODE3 - Serial Mode Select, PIN 41(L), 35(Q).
One of three pins that select the serial mode and function of the multifunction pins. This pin has an internal pull-down making this revision backwards compatible with a previous version (Revision A or Version3-Version0 bits = 0000).

Multifunction Digital Pins

MF1:DO4 - Parallel Digital Bit Output #4 in SM1/SM2, PIN 40(L), 34(Q).
In serial modes 1 and 2 this pin reflects the value of the DO4 bit in the sub-frame.

MF1:F1 - Format bit 1 in SM3, PIN 40(L), 34(Q).
In serial mode 3 this pin is a format bit and is used as one of three sample frequency select pins when in master mode, or as one of two bits-per-frame select pins when in slave mode.

MF1:CDOUT - Control Data Output in SM4, PIN 40(L), 34(Q).
In serial mode 4 this pin is the data output for the control port which contains status information.

MF2:DO3 - Parallel Digital Bit Output #3 in SM1/SM2, PIN 39(L), 33(Q).
In serial modes 1 and 2 this pin reflects the value of the DO3 bit in the sub-frame.

MF2:F2 - Format bit 2 in SM3, PIN 39(L), 33(Q).
In serial mode 3 this pin is a format bit and is used as one of three sample frequency select pins when in master mode, or as one of two bits-per-frame select pins when in slave mode.

MF2:CDIN - Control Data Input in SM4, PIN 39(L), 33(Q).
In serial mode 4 this pin is the control port data input which contains data such as gain and attenuation settings as well as input select, mute, and digital output bits.

MF3:DI3 - Parallel Digital Bit Input #3 in SM1/SM2/SM3 (Slave), PIN 35(L), 29(Q).
In serial modes 1 and 2 this pin value is reflected in the DI3 bit in the sub-frame.

MF3:F3 - Format bit 3 in SM3 (Master), PIN 35(L), 29(Q).
In serial mode 3 this pin is a format bit and is used as one of three sample frequency select pins when in master mode. In slave mode, the pin reverts to being a general purpose input.

MF3:CCLK - Control Data Clock in SM4, PIN 35(L), 29(Q).
In serial mode 4 this pin is the control port serial bit clock which latches data from CDIN on the falling edge, and outputs data onto CDOUT on the rising edge.

MF4:DI4 - Parallel Digital Bit Input #4 in SM1/SM2, PIN 36(L), 30(Q).

In serial modes 1 and 2 this pin value is reflected in the DI4 bit in the sub-frame.

MF4:MA - Master Sub-Mode in SM3, PIN 36(L), 30(Q).

In serial mode 3 this pin selects either master or slave mode. When MF4:MA = 1, the codec is in master mode and outputs SSYNC and SCLK. When MF4:MA = 0, the codec is in slave mode and receives SSYNC and SCLK from an external source that must be frequency locked to CLKIN.

MF4:$\overline{\text{CCS}}$ - Control Data Chip Select in SM4, PIN 36(L), 30(Q).

In serial mode 4 this pin is the control port chip select signal. When low, the control port data is clocked in CDIN and status data is output on CDOUT. When $\overline{\text{CCS}}$ goes high, control data is latched internally. This data remains active until new data is clocked in. The control port may also be asynchronous to the audio data port.

MF5:DO2 - Parallel Digital Bit Output #2 in SM1/SM2/SM3, PIN 38(L), 32(Q).

In serial modes 1, 2, and 3 this pin reflects the value of the DO2 bit in the sub-frame.

MF5:$\overline{\text{INT}}$ - Interrupt in SM4, PIN 38(L), 32(Q).

In serial mode 4 this pin is an active low interrupt signal that is maskable using the MSK bit in the control port serial data stream. $\overline{\text{INT}}$ is an open-collector output and requires and external pull-up resistor. Assuming the mask bit is not set, and interrupt is triggered by a change in ADV or DI1, or a rising edge on LCL or RCL, or a exiting an SCLK out of range condition (Error = 3)

MF6:DI2 - Parallel Digital Bit Input #2 in SM1/SM2/SM3, PIN 34(L), 28(Q).

In serial modes 1, 2, and 3 this pin value is reflected in the DI2 bit of the sub-frame.

MF6:F1 - Format Bit 1 in SM4, PIN 34(L), 28(Q).

In serial mode 4 this pin is a format bit and is used as one of three sample frequency select pins when in master mode. In slave mode, MF6:F1 helps determine the number of sub-frames within a frame.

MF7:SFS1 - Sub-Frame Select 1 in SM1/SM2/SM3/SM4-SL, PIN 31(L), 25(Q).

In serial modes 1, 2, and 3, MF7:SFS1 helps select the sub-frame that this particular CS4216 is allocated. In slave sub-mode of serial mode 4, this pin is one of two pins used as a sub-frame select when MF6:F1 = 1 (128-bit frames). When MF6:F1 = 0, this pin is used to select the frame sizes of 32 or 64 bits.

MF7:F2 - Format Bit 2 in SM4-MA, PIN 31(L), 25(Q).

In master sub-mode of serial mode 4, this pin is used as one of three sample frequency select pins.

MF8:SFS2 - Sub-Frame Select 2 in SM1/SM2/SM3/SM4-SL, PIN 30(L), 24(Q).

In serial modes 1, 2, 3, and slave sub-mode of 4, MF8:SFS2 helps select the sub-frame that this particular CS4216 is allocated.

MF8:F3 - Format Bit 3 in SM4-MA, PIN 30(L), 24(Q).

In master sub-mode of serial mode 4, this pin is a format bit and is one of three sample frequency select pins.

Miscellaneous

$\overline{\text{RESET}}$ - Reset Input, PIN 2.(L), 40(Q).

Resets the CS4216 into a known state, and must be initiated after power-up or power-down mode. Releasing $\overline{\text{RESET}}$ caused the CS4216 to initiate a calibration sequence. $\overline{\text{RESET}}$ should also be initiated when changing sample frequencies in any master sub-mode.

CLKIN - Master Clock, PIN 3(L), 41(Q).

CLKIN is the master clock that operates the internal logic. In serial mode 1, CLKIN = 512×hFs, where hFs is the highest sample frequency needed. Different sample frequencies are obtained by changing the ratio of SCLK to CLKIN. In serial mode 2, CLKIN is not used and must be tied low. In serial modes 3 and 4, CLKIN is 256×hFs, where different sample frequencies are obtained by either changing the ratio of SCLK to CLKIN in slave mode, or changing the format pin values (F2-F0) in master mode.

$\overline{\text{PDN}}$ - Power Down, PIN 13(L), 7(Q).

This pin, when low, causes the CS4216 to go into a power down state. $\overline{\text{RESET}}$ should be held low for 50 ms when exiting the power down state to allow time for the voltage reference to settle.

DI1 - Parallel Digital Bit Input #1, PIN 33(L), 27(Q).

This pin value is reflected in the DI1 bit in the sub-frame.

DO1 - Parallel Digital Bit Output #1, PIN 37(L), 31(Q).

This pin reflects the value of the DO1 bit in the sub-frame.

NC - No Connection, PINS 6, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19(L)
PINS 44, 1, 2, 3, 4, 5, 6, 8, 11, 12, 13(Q).

These pins should be left floating with no trace attached to allow backwards compatibility with future revisions. They should not be used as a convenient path for signal traces.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words from the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms value of a signal's first five harmonic components to the rms value of the signals fundamental component. THD is calculated using an input signal which is 3dB below typical full-scale, and is referenced to typical full-scale.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel, with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over the passband. Tested over the frequency band of 10 Hz to 20 kHz, with the sample frequency of 48 kHz. Units in dB.

Step Size

Typical delta between two adjacent gain or attenuation values. Units in dB.

Absolute Gain/Attenuation Step Error

The deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the full-gain/attenuation value (i.e. end points). Units in dB.

Offset Error

For the ADCs, the deviation of the output code from the mid-scale with the selected input at REFBUF. For the DACs, the deviation of the output from REFBUF with mid-scale input code. Units in LSB's for the ADCs and volts for the DACs.

Out of Band Energy

The ratio of the rms sum of the energy from 0.46×Fs to 2.1×Fs compared to the rms full-scale signal value. Tested with 48 kHz Fs giving a out-of-band energy range of 22 kHz to 100 kHz.

APPENDIX A

This data sheet describes version 1 of the CS4216. Therefore, this appendix is included to describe the differences between version 0 and version 1. This information is only useful for users that still have version 0 since version 1 devices will supplant the earlier version. The version number is contained in the serial data line, bits 29 - 32 on SDOUT in SM1-SM3 and, bits 17 - 20 on CDOUT in SM4. The version number can also be identified by the revision letter stamped on the top of the actual chip. The revision letter immediately precedes the data code on the second line of the package marking (See *General Information* section of the Crystal Data Book). Version 0 corresponds to chip revision A, and version 1 corresponds to chip revisions B, and C. The functionally and performance of revisions B and C are identical. Likewise, future chip revisions (i.e. D, E, F, . . .) may still be version 1 since the version number only changes if there is a software change to the part.

Functional Differences Between Version 0 (Rev. A) and Version 1 (Revs. B, C)

1. In version 0, serial mode 4 (SM4) does not exist; the SMODE3 pin is a no connect. In version 1 the SMODE3 pin contains an internal pull-down resistor making this version backwards compatible with version 0 sockets.

2. SSYNC on version 0 must be ONLY one SCLK period high in SM3 or 2 SCLK periods high in SM1 and SM2 to indicate the start of a frame. Also, on version 0 in SM1 or SM2, SSYNC must be EXACTLY one SCLK period high, at the beginning of each word. In version 1, SSYNC can be high for an arbitrary number of SCLKs beyond the one in SM3 or two in SM1 and SM2. Also in SM1 and SM2, the one-SCLK-wide SSYNCs at each word are not needed. In version 1, SM3 and SM4, the codec only looks for a low-to-high edge of SSYNC to start a frame; in SM1 and SM2 a low-to-high edge of SSYNC, being high for two SCLK periods, starts a frame.

Semiconductor Corporation

CDB4216

CS4216 Evaluation Board

Features

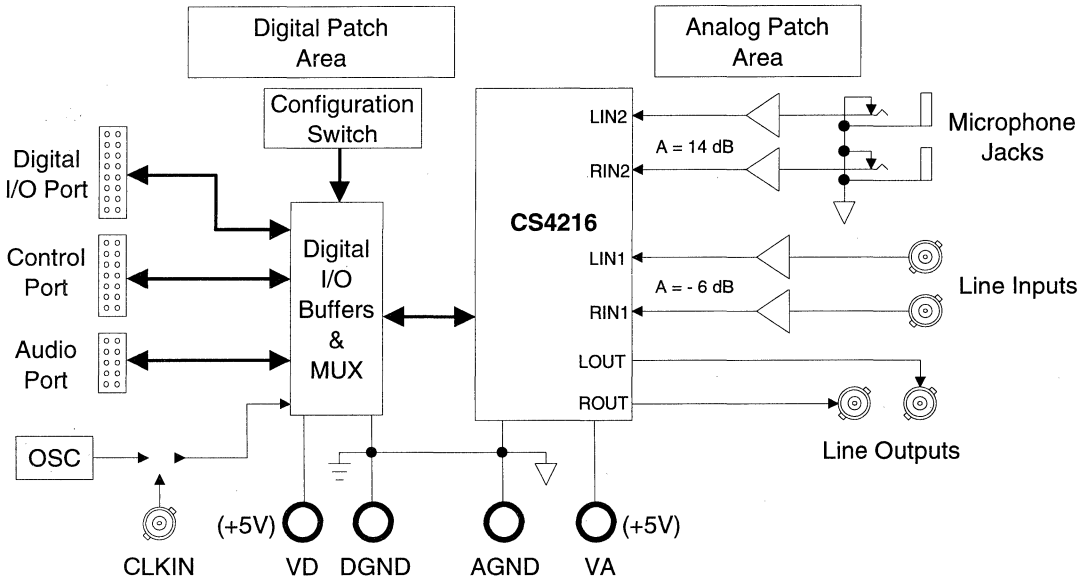
- Easy DSP Hook-Up
- Analog-in To Analog-out Loopback Mode
- Correct Grounding and Layout
- Microphone Pre-amplifier
- Line Input Buffer
- Digital and Analog Patch Areas

General Description

The CDB4216 evaluation board allows easy evaluation of the CS4216 audio multimedia codec. Analog inputs provided include two BNC line inputs for LIN1 and RIN1, and two 1/4" microphone jacks on the LIN2 and RIN2 lines. Analog outputs are available on two BNCs.

Digital interfacing is facilitated using one to three of the buffered ribbon cable headers. All four serial modes of the CS4216 are supported using a simple DIP switch which is decoded to select the proper mode and sub-mode.

ORDERING INFORMATION: CDB4216



GENERAL DESCRIPTION

The CDB4216 was designed to provide an easy platform for evaluating the performance of the CS4216 Stereo Audio Codec. Since the evaluation board contains a proper layout and is performance tested, the user can concentrate on engineering the rest of the system thereby reducing the development time. The layout should also be used as a guideline for obtaining the best possible performance from the CS4216. Lastly, the board can be used as a benchmark and debugging tool for user developed PCBs.

The evaluation board supports all serial modes and includes decode circuitry to ease the selection of the serial mode and sub-mode of interest. All serial interfaces are buffered for easy connection to the serial port of a DSP or other serial device. The board can also be placed in a loop back mode where the digital data is looped back allowing an analog in to analog out testing vehicle without an external processor. A single +5V supply is all that is needed to power the board.

Analog inputs consist of a pair of line input buffers (LIN1, RIN1) designed to accept a maximum audio signal of $2V_{RMS}$ and BNC-to-phono adapters are included to support various test configurations. The second pair of inputs contain a example microphone input buffer supported by two $^{1}/_{4}$" mono jacks that are designed to accept standard single-ended dynamic or condenser microphones.

The line outputs are supplied via BNC connectors with two more BNC-to-phono adapters.

The film plots of the evaluation board are included to provide an example of the optimum layout, grounding, and decoupling arrangement for the CS4216.

SELECTING A SERIAL MODE

The CS4216 supports four serial modes and many sub-modes. Selecting the most appropriate mode for a given application can be time consuming. The CDB4216 contains a DIP switch that simplifies this selection. Since the CS4216 contains many multifunction pins, the DIP switch lets the user select the configuration and two PLDs decode the proper multifunction pin values. Since these PLDs are only used to simplify the configuration of the device, they would not be needed in an end application which would hard wire the configuration pins. Table 4 describes the multifunction pin values for a given DIP switch setting. The PAL equations for DIP switch decoding are given in Figures 8 and 9.

Serial Port Format

Table 1 lists the DIP switches used to select the serial mode. SPF2 and SPF1 select one the four serial modes of the CS4216. MA selects master (MA = 1) or slave and is only useful in serial modes 3 and 4. The majority of users select either serial mode 3, SM3, or serial mode 4, SM4. Serial modes 1 and 2, SM1 and SM2, are primarily designed for ASICs and are less flexible. In master sub-mode, the CS4216 outputs SSYNC and SCLK. In slave sub-mode, SSYNC and SCLK must be externally generated and must be synchronous to CLKIN.

SPF2	SPF1	MA	Serial Mode	
0	0	x	SM1	Slave
0	1	x	SM2	Slave
1	0	0	SM3	Slave
1	0	1	SM3	Master
1	1	0	SM4	Slave
1	1	1	SM4	Master

Table 1. DIP Switch, Serial Modes

Bits per Frame Selection

The next decision is selecting the number of bits per frame which defines how many codecs can sit on the same serial bus. Each codec occupies a sub-frame and 1 to 4 sub-frames make up a frame. A sub-frame is 64 bits in SM1, SM2, and SM3; and 32 bits in SM4. Table 2 lists the possible selections. If the evaluation board serial port is shared with other devices, SDOUTUB must be used instead of SDOUT since SDOUTUB, driven directly from the chip, must only drive the time slot assigned to it. See the *Audio Port Header* section for more information.

BPF		SM1	SM3		SM4	
2	1	SM2	SL	MA	SL	MA
0	0	256	64	64	32	32
0	1	256	128	128	64	64
1	0	256	256	128	128	64
1	1	256	256*	128	128	64

* SCLK is master clock.

Table 2. DIP Switch, Bits per Frame

Time Slot Selection

If the number of bits per frame selected allows for more than one codec sub-frame, then the actual time slot or sub-frame used by the eval board must be selected. This is done with the TS2 and TS1 DIP switches. If the number of bits per frame allows only one codec on the serial bus, then TS2 and TS1 are ignored. Table 3 list the decoding for TS2 and TS1. Time slot 1 is the first sub-frame after SSYNC goes high, time slot 2 is the next sub-frame, and so on.

Sample Frequency Selection - Master Mode

The last decision is selecting the sample frequency in master sub-mode. If configured for slave sub-mode, the sample frequency is the ratio of SCLK to CLKIN as described in the CS4216 Data Sheet. In master mode, three pins are used to select the sample frequency divide. The DIP switches labeled DIV1, DIV2, and DIV3 select the sample frequency and are equivalent to F1, F2, and F3, respectively. The actual F1-F3 pins on the CS4216 are different between SM3 and SM4 as shown in Table 4 at the end of the data sheet. Table 3 and Table 9 of the CS4216 Data Sheet describe the sample frequencies obtained using the on-board oscillator of 11.2896 MHz. As an example, if all DIV switches are off, the sample frequency is 44.1 kHz. With only DIV2 on, the sample frequency is 22.05 kHz.

TS2	TS1	Available Sub-frames		
		4	2	1
0	0	1	1	1
0	1	2	2	1
1	0	3	2	1
1	1	4	2	1

Table 3. DIP Switch, Time Slots

DIP SWITCH MAPPING TO MULTI-FUNCTION PINS

The two PALs on the evaluation board decode the DIP switches to configure the codec into a particular mode. These PALs are not necessary in a design since only one mode is usually used and can be hard wired. Figure 9 and Figure 10 list the PAL equations used for decoding.

Table 4 shows the CS4216 multi-function pin settings for each possible DIP switch configuration. Refer to the CS4216 data sheet to determine pin settings for sample frequencies. Once a suitable mode has been chosen using the evaluation board, this table will show the hard wire configuration for each multi-function pin.

Example Mode Settings

Following are two examples of how to set a serial mode with the DIP switches and then determine the multi-function pin settings for the codec. These modes were chosen for illustration

only, not to suggest that they are better than other modes.

A commonly used mode is SM3, Master, 64 BPF, 44.1kHz sampling rate, and bit-long SSYNC. To configure the codec in this mode, set SPF2=MA=1 and all other DIP switches to zero. From Table 4, the SMODE3, SMODE2, and SMODE1 pins are set to 010, respectively. The DIV1, DIV2, and DIV3 DIP switches will set the sampling frequency by directly mapping to the MF1, MF2, and MF3 pins as 000. The MA DIP switch sets the MF4 pin high for master mode. multi-function pins MF5 and MF6 become the general purpose I/O pins DO2 and DI2, respectively. In this particular mode, MF7 determines the high time for the SSYNC signal. The MF7 pin is set low by the TS1 switch to generate the bit-long SSYNC. In all other applicable cases, the TS1 switch is used for time-slot configuration. 64 BPF is selected by setting the MF8 pin low with the BPF1 switch.

SM4 is a powerful mode which reduces data transfer bandwidth to facilitate easier use with low cost DSPs. As an example, consider SM4, Slave, 64 BPF, Time-slot 2, and a 22.05kHz sampling rate. Set SPF2=SPF1=DIV1=TS1=BPF1=1 and all other DIP switches to zero. Table 4 shows that the SMODE3, SMODE2, and SMODE1 pins will be set to 110, respectively. The multi-function pins MF1-4 will become the control port interface. MF5 serves as the interrupt pin $\overline{\text{INT}}$. BPF2 and BPF1 will set the codec to 64 BPF by mapping directly to the MF6 and MF7 pins as 01, respectively. The second time-slot is chosen with TS1 setting the MF8 pin high. Since the part is in slave mode, the sampling rate must be set by the ratio between CLKIN and SCLK. Assuming that CLKIN has a frequency of 11.2896MHz, this ratio must be eight to give a sampling rate of 22.05kHz (refer to the CS4216 data sheet). In all slave modes, SSYNC and SCLK must be synchronous to the master clock.

LOOPBACK MODE

The CDB4216 may be configured in a simple loop back mode that only requires a power source to operate. No controller of any type is necessary. This mode allows a quick and simple verification of codec operation by sampling the LIN1 and RIN1 inputs, then looping the digital data back to the LOUT and ROUT line outputs. Set SPF2=SPF1=MA=1 and shunt SDOUT to SDIN on stake header J15. This mode uses SM4 with all control settings set to zero, so no gain or attenuation is available.

DIP SWITCHES			SMODE	SMODE	SMODE	CS4216 Multifunction Pins							
SPF2	SPF1	MA	3	2	1	MF1	MF2	MF3	MF4	MF5	MF6	MF7	MF8
0	0	x	0	0	0	DO4	DO3	DI3	DI4	DO2	DI2	TS1	TS2
0	1	x	0	0	1	DO4	DO3	DI3	DI4	DO2	DI2	TS1	TS2
0	1	0	0	1	0	BPF2	BPF1	DI3	MA=0	DO2	DI2	TS1	TS2
0	1	1	0	1	0	DIV1	DIV2	DIV3	MA=1	DO2	DI2	TS1	BPF1
1	1	0	1	1	0	CDOUT	CDIN	CCLK	$\overline{\text{CCS}}$	$\overline{\text{INT}}$	BPF2=0	BPF1	TS1
1	1	0	1	1	0	CDOUT	CDIN	CCLK	$\overline{\text{CCS}}$	$\overline{\text{INT}}$	BPF2=1	TS1	TS2
1	1	1	1	BPF=0	0	CDOUT	CDIN	CCLK	$\overline{\text{CCS}}$	$\overline{\text{INT}}$	DIV1	DIV2	DIV3
1	1	1	1	BPF>0	TS1	CDOUT	CDIN	CCLK	$\overline{\text{CCS}}$	$\overline{\text{INT}}$	DIV1	DIV2	DIV3

Table 4. CS4216 Pin Decode

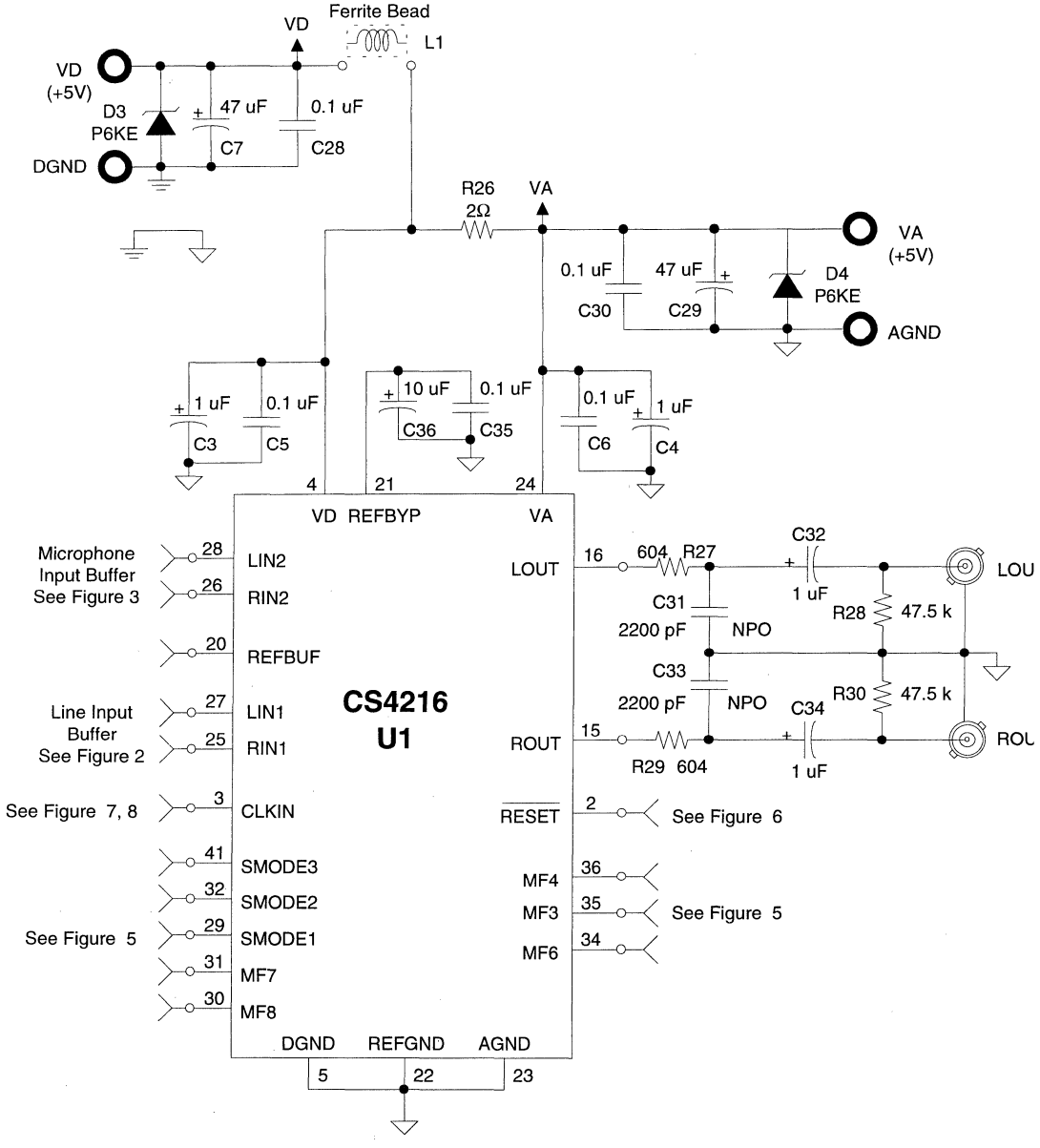


Figure 1. CS4216 and Power Supplies

POWER SUPPLY CIRCUITRY

Figure 1 illustrates a portion of the CDB4216 schematic and includes the CS4216 along with power supply decoupling and circuitry. The evaluation board supports various power supply arrangements. The factory configuration powers the analog portion of the CS4216, along with input buffers, from the VA binding post, which needs a clean +5 Volts. The digital portion of the CS4216 is factory configured to obtain power through a 2Ω resistor from the VA supply. The digital buffers and PLDs obtain power from the VD binding post, which also needs +5 Volts. Although binding posts exist for both digital and analog grounds, only one needs to be connected if a single supply is used for both VA and VD. Note that the CS4216 is entirely on the analog ground plane, close to the ground plane split as required by the CS4216 Data Sheet. Also note that the two ground planes are connected near the two ground binding posts.

Space for a ferrite bead, L1, is provided so that the board may be modified to power the codec from the digital supply. Selection of L1 will depend on the noise characteristics of the digital supply used.

ANALOG INPUTS

The analog inputs consist of a pair of line level inputs and a pair of $^1/_4$" mono jacks for two microphones. BNC-to-phono adapters are included to allow testing of the line inputs using coax or standard audio cables.

The line-level inputs are connected to the CS4216's LIN1 and RIN1 pins. As shown in Figure 2, the line-level inputs go through a buffer set to a gain of 0.5 which allows input signals of up to 2 V_{RMS}. When placed in serial mode 4 with loop back, the LIN1 and RIN1 inputs are used for analog inputs.

The microphone inputs are connected to the CS4216's LIN2 and RIN2 pins. The two microphone inputs are single-ended and are designed to work with both condenser and dynamic microphones. The microphone input buffer, shown in Figure 3, has a gain of 23 dB thereby defining a full-scale input voltage to the microphone jacks of 71 mV_{RMS}. Another 22 dB of programmable gain is available on the CS4216 to amplify smaller microphone signals.

An analog patch area with analog power and ground, included on the CDB4216, provides space to develop other input buffer circuits. Space for headers are included, J19 and J20, to connect to the LIN2 and RIN2 inputs. To use these headers, the microphone traces must be cut.

ANALOG OUTPUTS

The CS4216 drives the line outputs into an R-C filter and then to a pair of BNCs labeled LOUT and ROUT. As with the line inputs, BNC-to-phono adapters are provided for flexibility. The line outputs can drive an impedance of 10 kΩ or more, which is the typical input impedance of most audio gear.

AUDIO PORT HEADER

The CDB4216 is primarily designed to evaluate the CS4216 in single chip mode, i.e. only one codec on the serial bus. This is the factory default state of the CDB4216.

The audio port header J15 provides all buffered signals necessary to connect to the serial port of a DSP or other controller (see Figure 4). SDOUTUB can provide an unbuffered version of SDOUT which can be used when connecting multiple codecs on the same bus. The default configuration does not connect SDOUTUB which may be connected to the SDOUT of the CS4216 through J17 jumper.

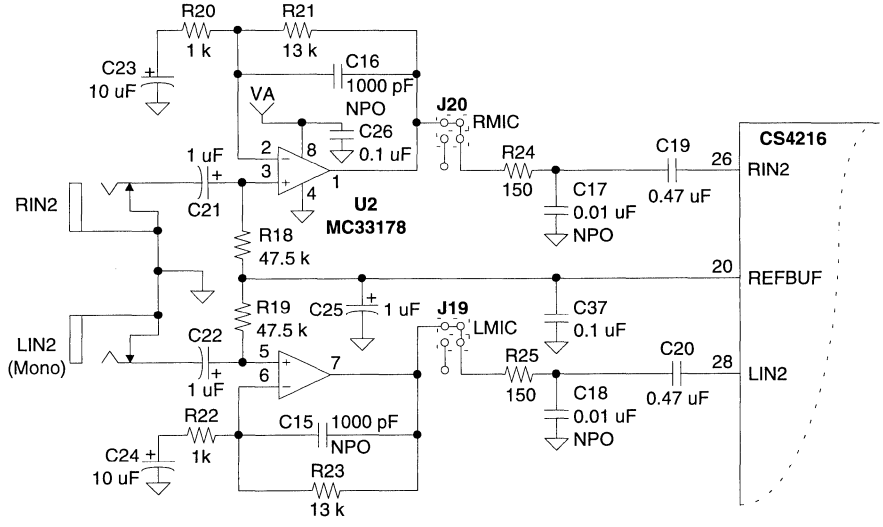


Figure 2. Microphone Input Buffer

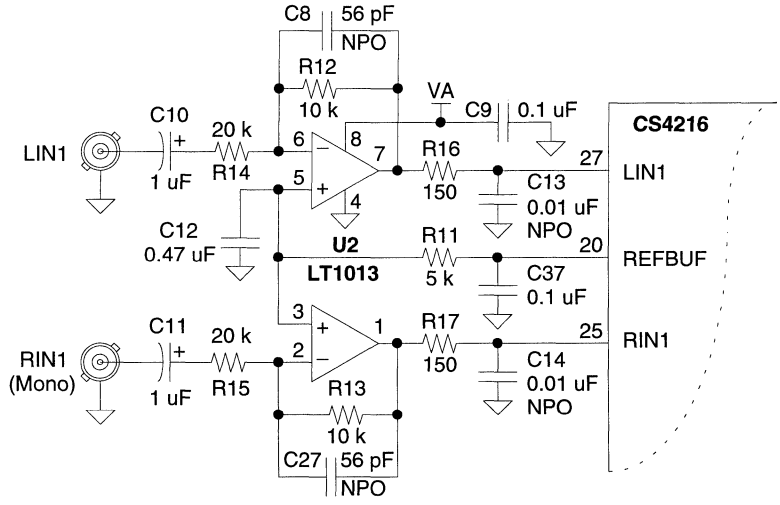


Figure 3. Line Input Buffer

The eval board supports both master and slave sub-modes. In master sub-mode, SSYNC and SCLK are output (and buffered) from the CS4216. In slave sub-mode, SSYNC and SCLK must be provided externally and must be synchronous to the master clock CLKIN.

CONTROL PORT HEADER

The Control Port Header J14 contains the control port pins, available only in SM4, and the $\overline{\text{PDN}}$ and $\overline{\text{RESET}}$ pins.

Serial mode 4, SM4, splits the serial data to the codec into two separate serial ports, the audio port and the control port. The control port pins are available on this header. Since CDOUT is buffered and always driven, it cannot be used on a shared serial port. Although the $\overline{\text{INT}}$ pin on the codec is open drain, the default factory configuration for the eval board is an on-board pull-up resistor and a buffer. Therefore, the $\overline{\text{INT}}$ header pin cannot share an interrupt pin on a processor since it is buffered and will always be driven. By cutting a trace in the J18 jumper, the unbuffered $\overline{\text{INT}}$ signal, labeled U, can be supplied to the header. When using the control port, the LB switch must be off or the control serial port will be blocked.

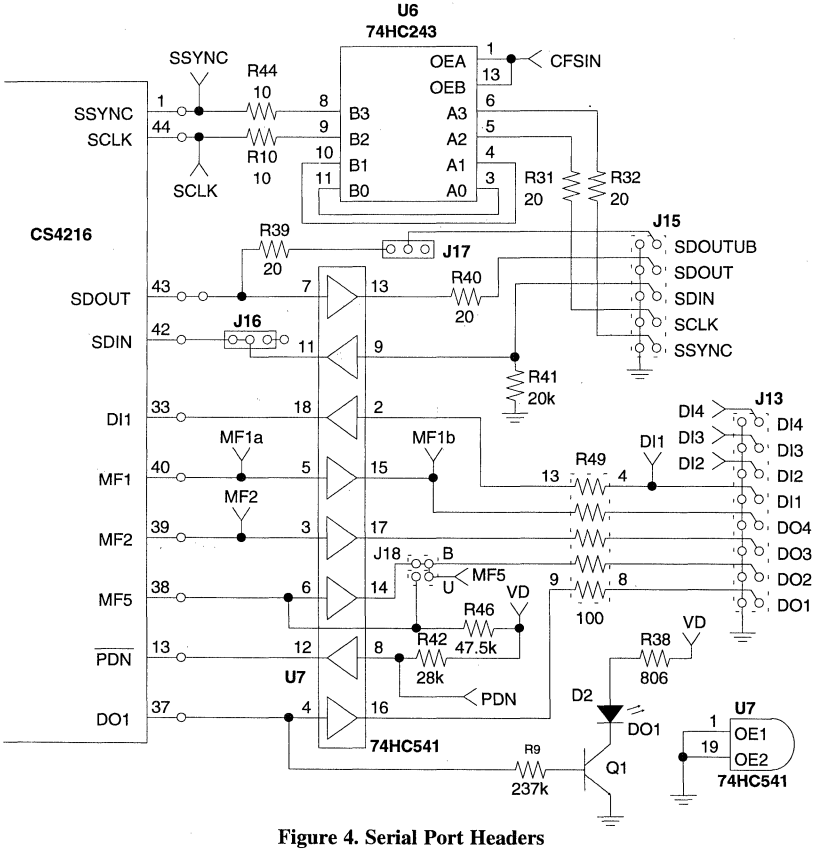


Figure 4. Serial Port Headers

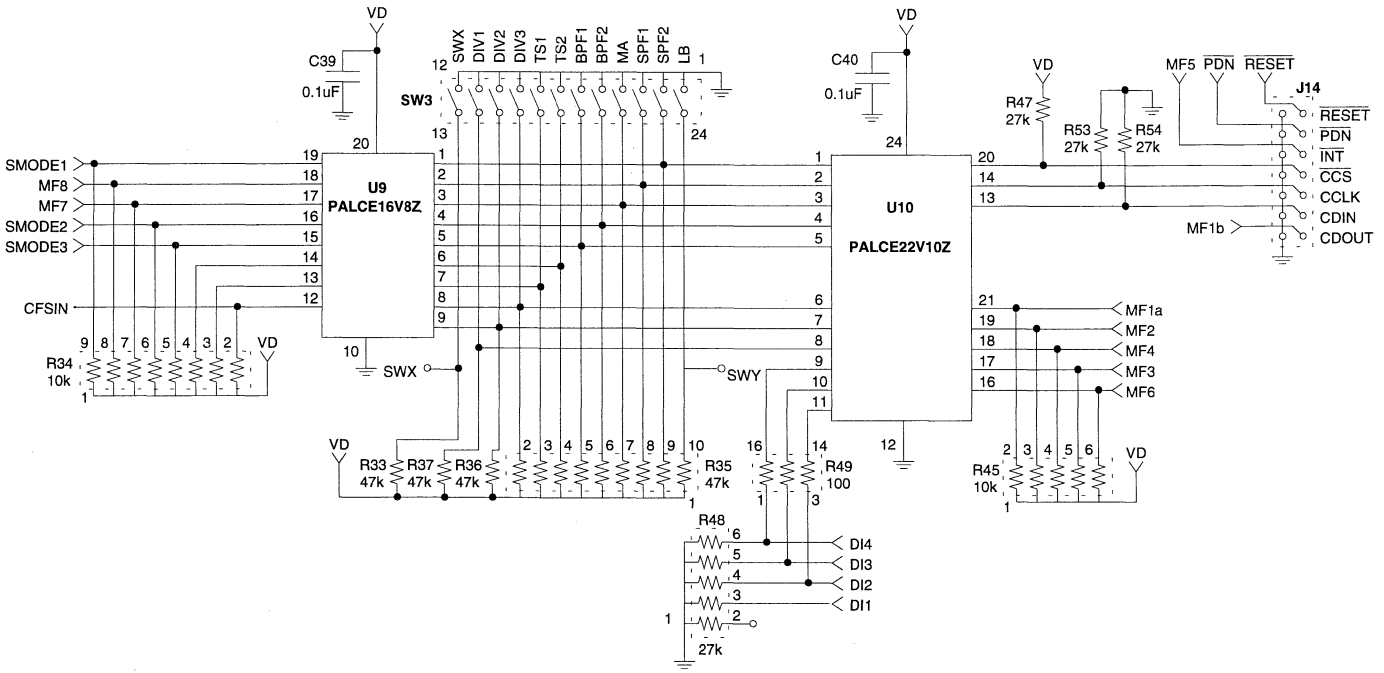


Figure 5. DIP Switch Decode + Digital Header

PDN and RESET

PDN is buffered and controls the PDN pin on the CS4216. PDN contains an on-board pull-up resistor defining the default state as powered. This pin only needs to be controlled when the power down feature is used.

RESET is also buffered and controls the RESET pin on the codec (see Figure 6). RESET has a pull-up resistor on the board defining the default state as not reset or active. This pin only needs to be controlled when the reset feature on the codec is needed. Since the codec requires a reset at power up, a power-up reset circuit is included on the board. A reset switch is also included to allow resetting the device without having to remove the power supply. The power-up reset plus switch are logically ORed with the RESET pin on header J14.

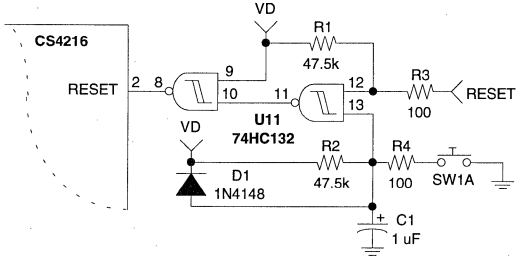


Figure 6. Reset Circuit

DIGITAL I/O HEADER

The Digital I/O Header, J13 shown in Figure 4, contains the four digital inputs, DI1-DI4, and the four digital outputs, DO1-DO4. Note that all digital I/O except DI1 and DO1 are multifunction pins and may not be available in a particular mode. Since DO1 is always a digital output, an LED is connected to DO1 providing a visual indication that software is writing this bit correctly. When the LED is on, DO1 is high.

In SM1 and SM2 all four digital inputs and outputs are available. In SM3, only the first two inputs and outputs are functional. In SM4 only DO1 and DI1 are functional. See the CS4216 Data Sheet for more details.

CLOCKS

The CDB4216 provides an on-board default clock oscillator of 11.2896 MHz (see Figure 7). This allows all 44.1 kHz and derivative sample frequencies in SM3 and SM4. If using SM1, a master clock with a frequency that is 512 times the highest sample rate must be supplied. A CLKIN BNC allows the eval board to be driven from an external source. To select the CLKIN frequency, the J1 jumper must be placed in the EXT position. When the J1 jumper is in the INT position, the on-board oscillator is used as the master clock. Both clock sources are buffered to guarantee a clean signal and proper clock levels to the codec.

If sample frequencies other than the ones provided are needed, the oscillator can be replaced with the proper frequency oscillator. The board accepts crystals and provides the socket Y1 (refer to Figure 8). When using a crystal, U8 must contain an HCU04 unbuffered CMOS inverter. The U8 socket is designed to accept either the HCU04 or a crystal oscillator, and can alternate between the two.

LAYOUT ISSUES

Figure 11 contains the silk screen, Figure 12 contains the component-side copper layer, and Figure 13 contains the solder-side copper layer of the CDB4216 evaluation board. These plots are included to provide an example of how to correctly layout a PCB for the codec.

Grounding and Power

Notice in Figure 12 and Figure 13 how the ground plane split is positioned. The split is

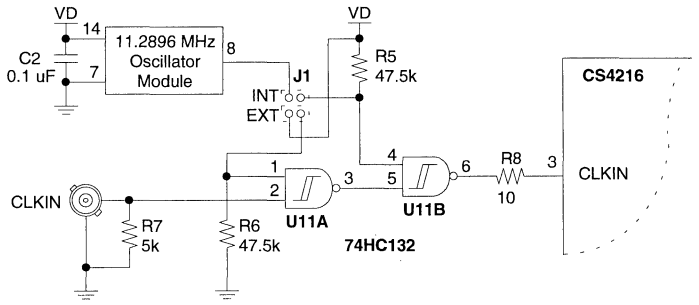


Figure 7. Default Clock Circuit

next to the part - *NOT UNDER IT*. The AGND and DGND pins are connected to the ground plane fill inside the codec pad layout on the component-side layer. This is recommended because AGND and DGND are connected on the codec die and must have a zero impedance between them.

Notice how each ground connection has at least four points in thermal relief. The main board grounds at the terminal connections have eight points in thermal relief. This helps minimize the impedance to the main ground terminal from any particular ground pin, reducing the chance of noise coupling.

Another important design consideration is the ground plane fill between traces on both layers, which minimizes coupling of radiated energy. Ground fill on the digital side of the board helps reduce the amount of noisy digital energy radiated to the sensitive analog side and to a host system. Ground fill on the analog side helps reduce the amount of radiated digital energy that is coupled into the analog circuitry. All ground plane fills must be connected to their respective grounds - floating ground fill is worse than no fill.

All power and ground traces are as thick as the surface mount pads they connect. Thick traces

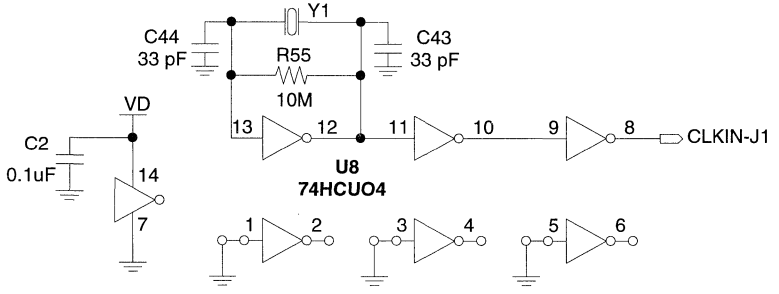


Figure 8. Optional Clock Circuit

minimize impedance, thereby reducing the chance of noise coupling.

Decoupling

Notice how the decoupling capacitors are placed as close as possible to the codec. The 0.1µF capacitors are placed closer than the 10µF or 1µF capacitors. This reduces lead inductance at high frequencies and allows the smaller valued capacitors to attenuate unwanted signals more effectively.

Sockets

The CDB4216 was designed to accommodate either the 44-pin PLCC package or the 44-pin TQFP package. Each evaluation board is shipped with a PLCC codec loaded into a surface mount socket. Notice how the socket pads match the footprint of the PLCC package. Using this socket in a design allows for testing with the socket mounted, and the option to surface mount the codec directly for cost reduction during board production.

```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE           CDB4216
PATTERN         4216S_B
REVISION        4.0B
AUTHOR          C. Sanchez, M. Jordan
COMPANY         Crystal Semiconductor
DATE            5/28/93

CHIP _4216s_b PALCE16V8

;---------------------------------- PIN Declarations ---------------
PIN     1    /SPF2      COMBINATORIAL ; INPUT
PIN     2    /SPF1      COMBINATORIAL ; INPUT
PIN     3    /MA        COMBINATORIAL ; INPUT
PIN     4    /BPF2      COMBINATORIAL ; INPUT
PIN     5    /BPF1      COMBINATORIAL ; INPUT
PIN     6    /TS2       COMBINATORIAL ; INPUT
PIN     7    /TS1       COMBINATORIAL ; INPUT
PIN     8    /DIV3      COMBINATORIAL ; INPUT
PIN     9    /DIV2      COMBINATORIAL ; INPUT
PIN     10   GND
PIN     11   NC
PIN     12   /CFSIN      COMBINATORIAL ; OUTPUT
PIN     13   NC
PIN     14   NC
PIN     15   SMODE3     COMBINATORIAL ; OUTPUT
PIN     16   SMODE2     COMBINATORIAL ; OUTPUT
PIN     17   MF7        COMBINATORIAL ; OUTPUT
PIN     18   MF8        COMBINATORIAL ; OUTPUT
PIN     19   SMODE1     COMBINATORIAL ; OUTPUT
PIN     20   VCC

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

/CFSIN = SPF2 * MA

SMODE3 = SPF2 * SPF1

SMODE2 = SPF2 * /SPF1
         + SPF2 * SPF1 * /MA
         + SPF2 * SPF1 * MA * BPF1 * TS1
         + SPF2 * SPF1 * MA * BPF1 * TS2
         + SPF2 * SPF1 * MA * BPF2 * TS1
         + SPF2 * SPF1 * MA * BPF2 * TS2

SMODE1 = /SPF2 * SPF1
         + SPF2 * SPF1 * MA * BPF1
         + SPF2 * SPF1 * MA * BPF2

MF8 = /SPF2 * TS2
         + SPF2 * /SPF1 * MA * BPF2
         + SPF2 * /SPF1 * MA * BPF1
         + SPF2 * /SPF1 * /MA * BPF2 * TS2
         + SPF2 * SPF1 * /MA * /BPF2 * BPF1 * TS1
```

Figure 9. PALCE16V8H PAL Equations.

```
                + SPF2 * SPF1 * /MA * /BPF2 * BPF1 * TS2
                + SPF2 * SPF1 * /MA * BPF2 * TS2
                + SPF2 * SPF1 * MA * DIV3

MF7 = /SPF2 * TS1
                + SPF2 * /SPF1 * /MA * /BPF2 * BPF1 * TS1
                + SPF2 * /SPF1 * /MA * /BPF2 * BPF1 * TS2
                + SPF2 * /SPF1 * /MA * BPF2 * TS1
                + SPF2 * /SPF1 * MA * TS1
                + SPF2 * SPF1 * /MA * /BPF2 * BPF1
                + SPF2 * SPF1 * /MA * BPF2 * TS1
                + SPF2 * SPF1 * MA * DIV2
```

Figure 9. Continued.

```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE           CDB4216
PATTERN         4216L_B
REVISION        2.0B
AUTHOR          C. Sanchez
COMPANY         Crystal Semiconductor
DATE            4/27/93

CHIP _4216l_b PALCE22V10Z

;---------------------------------- PIN Declarations ---------------
PIN     1       /SPF2           COMBINATORIAL ; INPUT
PIN     2       /SPF1           COMBINATORIAL ; INPUT
PIN     3       /MA             COMBINATORIAL ; INPUT
PIN     4       /BPF2           COMBINATORIAL ; INPUT
PIN     5       /BPF1           COMBINATORIAL ; INPUT
PIN     6       /DIV3           COMBINATORIAL ; INPUT
PIN     7       /DIV2           COMBINATORIAL ; INPUT
PIN     8       /DIV1           COMBINATORIAL ; INPUT
PIN     9       DI4             COMBINATORIAL ; INPUT
PIN     10      DI3             COMBINATORIAL ; INPUT
PIN     11      DI2             COMBINATORIAL ; INPUT
PIN     12      GND
PIN     13      CDIN            COMBINATORIAL ; INPUT
PIN     14      CCLK            COMBINATORIAL ; INPUT
PIN     15      NC
PIN     16      MF6             COMBINATORIAL ; OUTPUT
PIN     17      MF3             COMBINATORIAL ; OUTPUT
PIN     18      MF4             COMBINATORIAL ; OUTPUT
PIN     19      MF2             COMBINATORIAL ; OUTPUT
PIN     20      /CCS            COMBINATORIAL ; INPUT
PIN     21      MF1             COMBINATORIAL ; OUTPUT
PIN     22      NC
PIN     23      NC
PIN     24      VCC

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

MF1 = SPF2 * /SPF1 * MA * DIV1
            + SPF2 * /SPF1 * /MA * BPF2

MF1.TRST = SPF2 * /SPF1

MF2 = SPF2 * /SPF1 * MA * DIV2
            + SPF2 * /SPF1 * /MA * BPF1
            + SPF2 * SPF1 * CDIN

MF2.TRST = SPF2

MF3 = /SPF2 * DI3 + SPF2 * /SPF1 * /MA * DI3
            + SPF2 * /SPF1 * MA * DIV3
            + SPF2 * SPF1 * CCLK

MF4 = /SPF2 * DI4
```

Figure 10. PALCE22V10Z PAL Equations.

```
                + SPF2 * /SPF1 * MA
                + SPF2 * SPF1 * /CCS

MF6 = /SPF2 * DI2 + /SPF1 * DI2
                + SPF2 * SPF1 * MA * DIV1
                + SPF2 * SPF1 * /MA * BPF2
```

Figure 10. Continued.

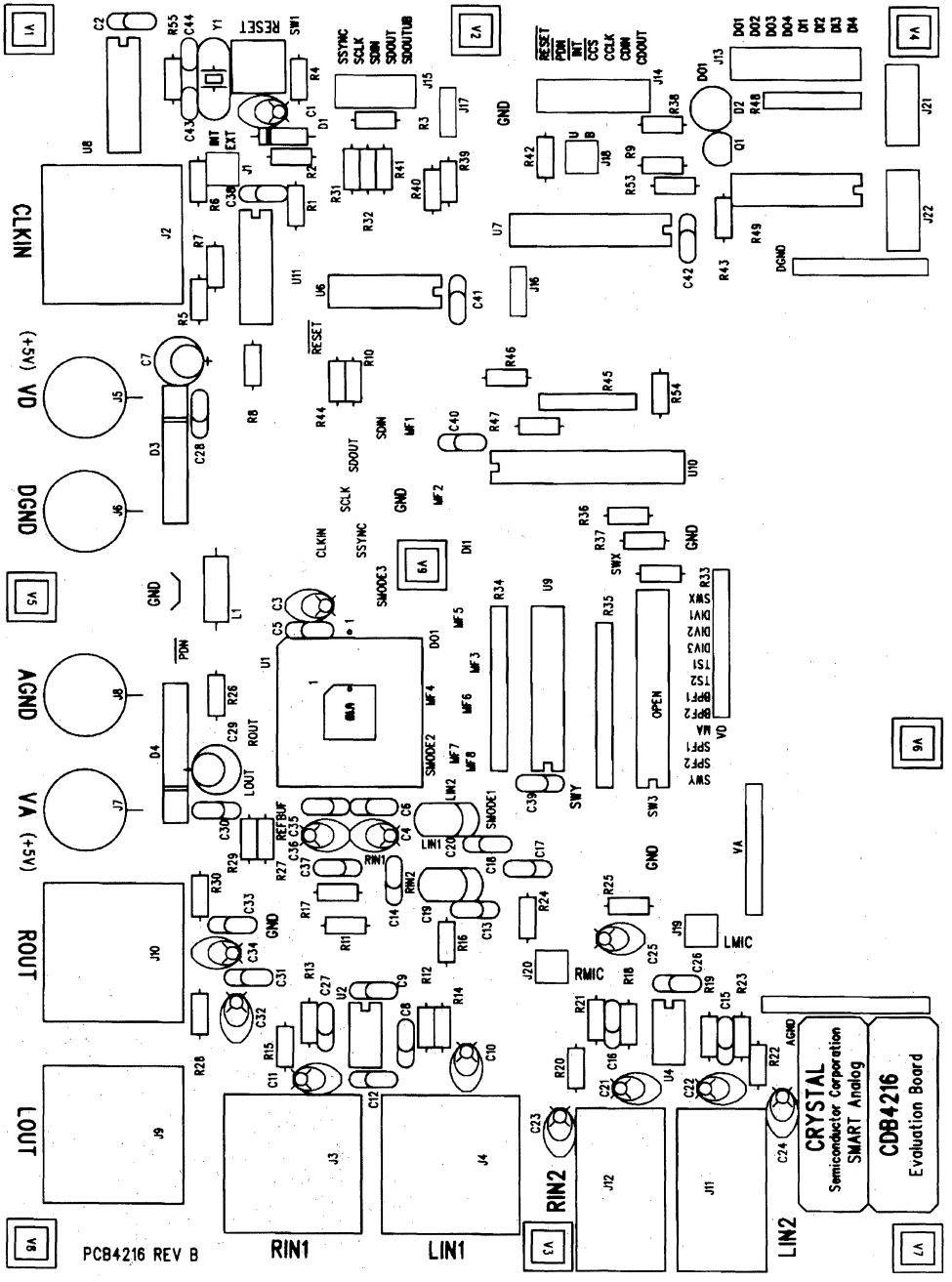


Figure 11. CDB4216 Silkscreen.

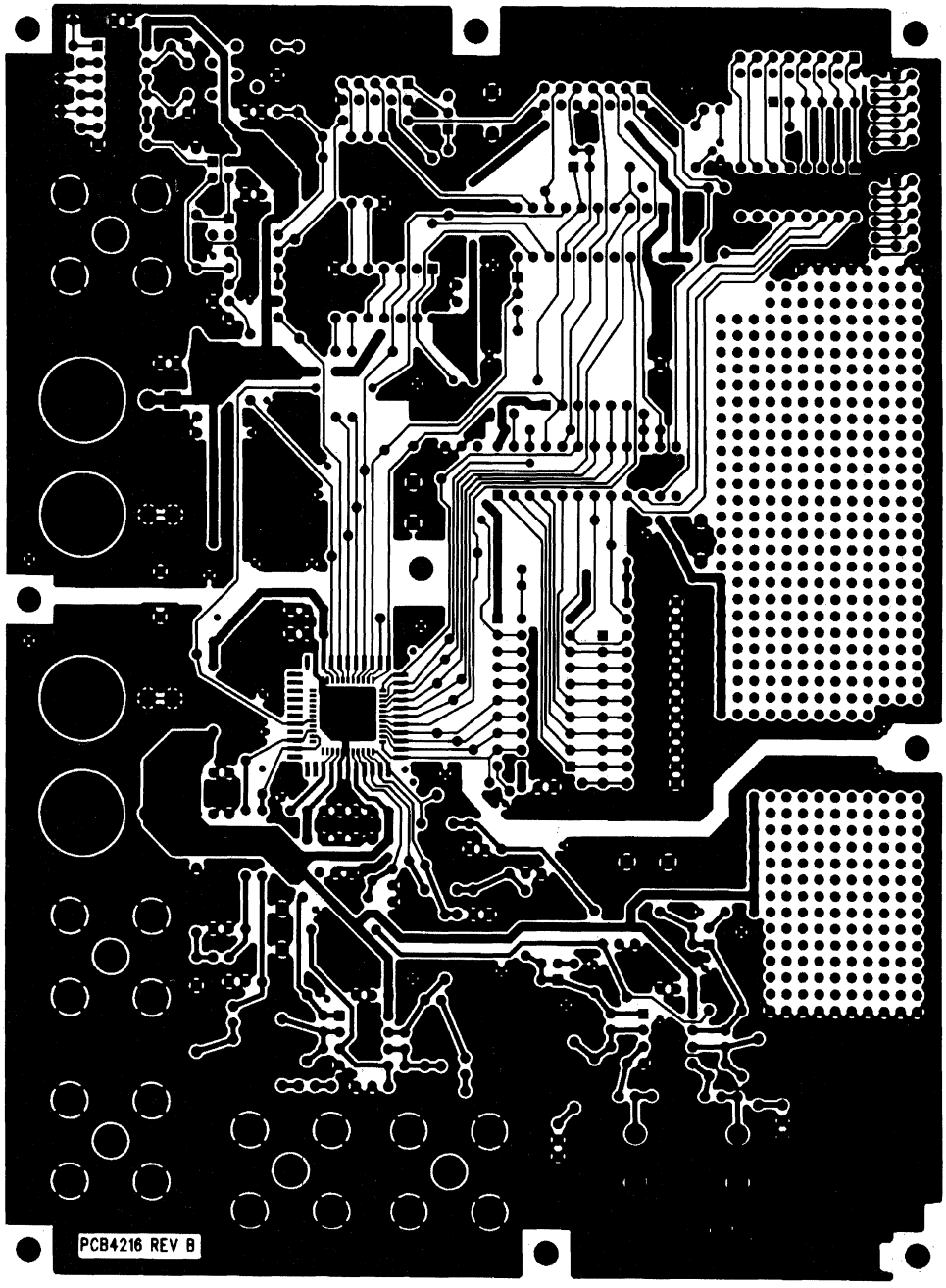


Figure 12. CDB4216 Component-side Layer.

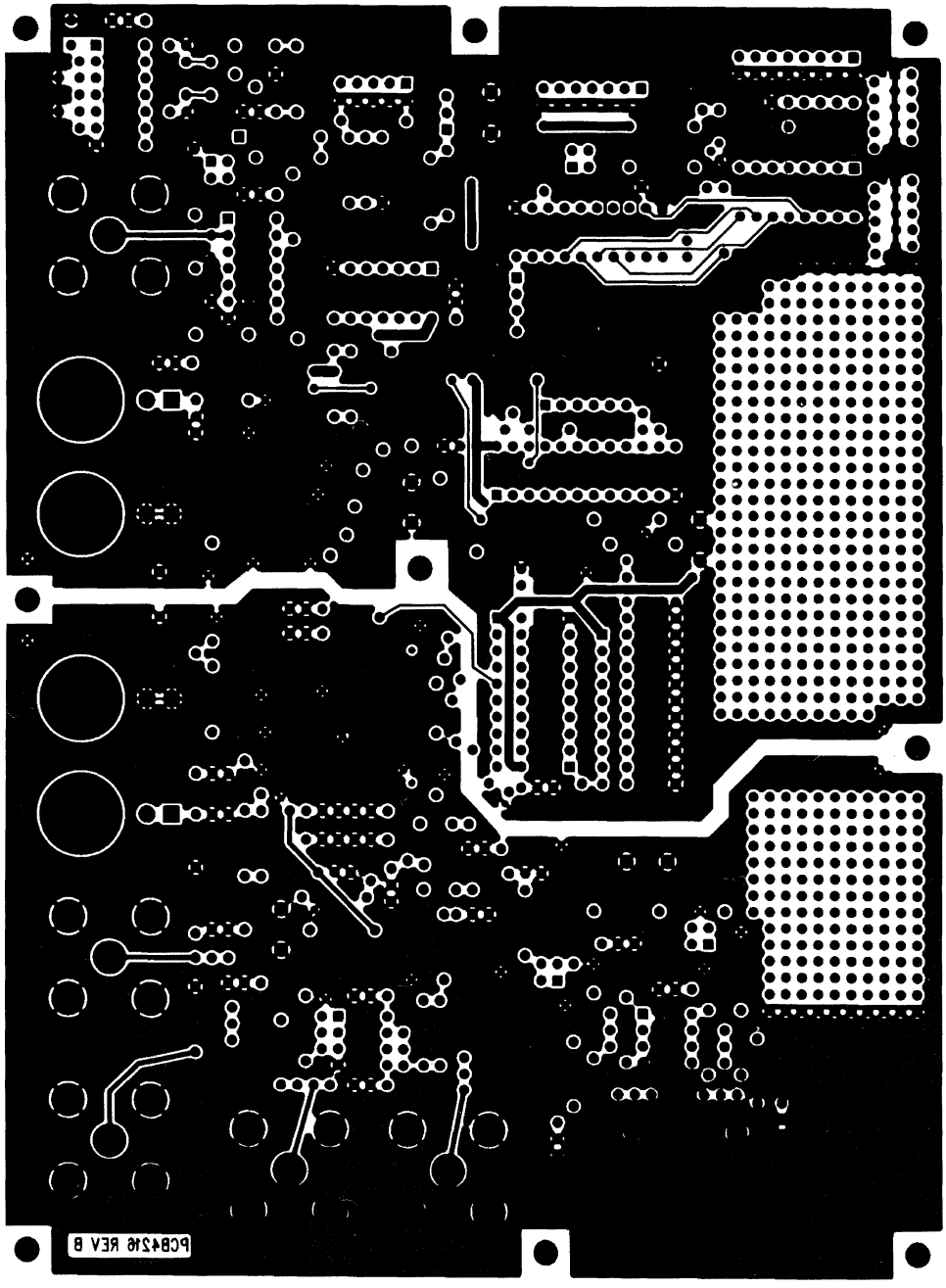


Figure 13. CDB4216 Solder-side Layer.

• Notes •

Semiconductor Corporation

CS4225

Digital Audio Conversion System

Features

- Stereo 16-bit A/D Converters
- Quad 16-bit D/A Converters
- Sample Rates From 4kHz to 50kHz
- >100 dB DAC Signal-to-Noise Ratio
- Variable Bandwidth Auxiliary 12-bit A/D
- Programmable Input Gain & Output Attenuation
- +5V Power Supply
- On-chip Anti-aliasing and Output Smoothing Filters
- Error Correction and De-Emphasis

Description

The CS4225 is a single-chip, stereo analog-to-digital and quad digital-to-analog converter using delta-sigma conversion techniques. Applications include CD-quality music, FM radio quality music, telephone-quality speech. Four D/A converters make the CS4225 ideal for surround sound and automotive applications.

The CS4225 is supplied in a 44-pin plastic package with J-leads (PLCC) or as a die.

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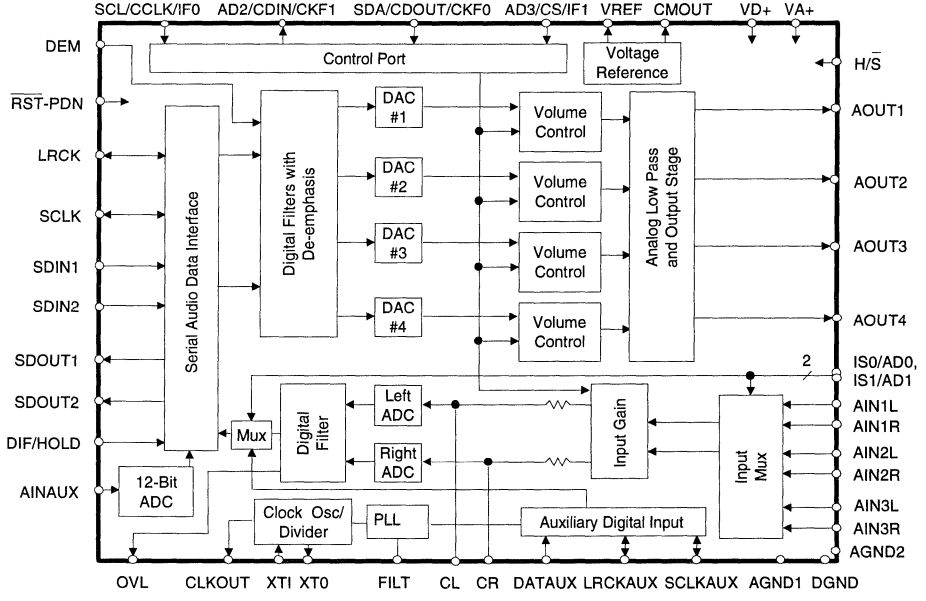
Ordering Information

CS4225-KL	PLCC, 0 °C to +70 °C
CS4225-BL	PLCC, -40 °C to +85 °C
CS4225-YU	die, -40 °C to +85 °C operation
CDB4225	Evaluation Board



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VD+ = +5V; Full Scale Input Sine wave, 1 kHz; Word Clock = 48 kHz (PLL in use); Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in "Recommended Connection Diagram"; SPI mode, Format 0, unless otherwise specified.)

Parameter *	Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.					
ADC Resolution — Audio channels Auxiliary channel		16 12	-	-	Bits Bits
ADC Differential Nonlinearity		-	-	±0.9	LSB
Dynamic Range — Audio channels(A weighted):		82	85	-	dB
Total Harmonic Distortion + Noise (A weighted)	THD+N	-	-85	-82	dB
Interchannel Isolation		-	85	-	dB
Interchannel Gain Mismatch		-	-	.1	dB
Frequency Response — Audio channels(0 to 0.454 Fs):		-3.0	-	+0.2	dB
Programmable Input Gain		-0.2	-	46.7	dB
Gain Step		1.3	1.5	1.7	dB
Offset Error		-	10	-	LSB
Full Scale Input Voltage (Auxiliary and Audio channels):		2.66	2.8	2.94	V_{pp}
Gain Drift		-	100	-	ppm/°C
Input Resistance — (Note 1)		10	-	-	kΩ
Input Capacitance		-	-	15	pF
CMOUT Output Voltage		1.9	2.1	2.3	V

Notes: 1. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance. The input resistance will vary with gain value selected, but will always be greater than the min. value specified.

* Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.						
DAC Resolution			16	-	-	Bits
DAC Differential Nonlinearity			-	-	±0.9	LSB
Total Dynamic Range	(DAC muted,A weighted)		100	-	-	dB
Total Harmonic Distortion	(Note 2)	THD	-	-	0.01	%
Instantaneous Dynamic Range (DAC not muted, Note 2, A weighted)			85	88	-	dB
Interchannel Isolation	(Note 2)		-	85	-	dB
Interchannel Gain Mismatch			-	-	0.2	dB
Frequency Response	(0 to 0.476 Fs)		-3.0	-	+0.2	dB
Programmable Attenuation	(All Outputs)		0.2	-	-117	dB
Attenuation Step			0.88	1.0	1.12	dB
Offset Voltage			-	10	-	mV
Full Scale Output Voltage	(Note 2)		2.66	2.8	2.94	V_{pp}
Gain Drift			-	100	-	ppm/°C
Deviation from Linear Phase			-	-	5	Degrees
Out of Band Energy	(Fs/2 to 2Fs)		-	-60	-	dB
Analog Output Load	Resistance: Capacitance:		8 -	- -	- 100	kΩ pF
Power Supply						
Power Supply Current	Operating Power Down		- -	120 1	TBD TBD	mA mA
Power Supply Rejection	(1 kHz)		-	40	-	dB

Notes: 2. 10 kΩ, 100 pF load.

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16-Bit Audio A/D Decimation Filter Characteristics

(See graphs towards the end of this data sheet)

Parameter	Symbol	Min	Typ	Max	Units
Passband (to -3 dB corner) (Fs is conversion freq.)		0	-	0.454Fs	Hz
Passband Ripple		-	-	±0.1	dB
Transition Band		0.40Fs	-	0.60Fs	Hz
Stop Band		≥ 0.60Fs	-	-	Hz
Stop Band Rejection		75	-	-	dB
Group Delay		-	10/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

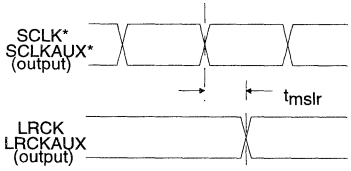
D/A Interpolation Filter Characteristics (See graphs toward the end of this data sheet)

Parameter	Symbol	Min	Typ	Max	Units
Passband (to -3 dB corner) (Fs is conversion freq.)		0	-	0.476Fs	Hz
Passband Ripple		-	-	±0.1	dB
Transition Band		0.442Fs	-	0.567Fs	Hz
Stop Band		≥0.567Fs	-	-	Hz
Stop Band Rejection		50	-	-	dB
Stop Band Rejection with Ext. 2Fs RC filter		57	-	-	dB
Group Delay		-	12/Fs	-	s
Group Delay Variation vs. Frequency		-	-	TBD	µs

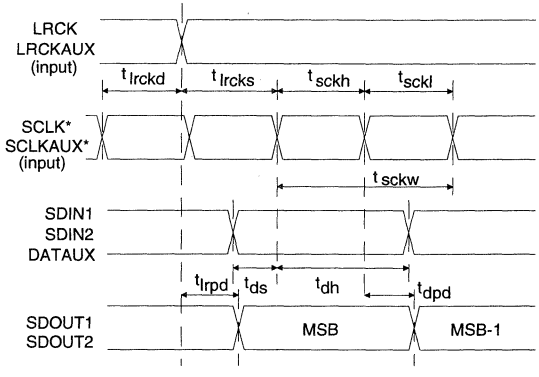
SWITCHING CHARACTERISTICS (T_A = 25°C; VA+, VD+ = +5V, outputs loaded with 30pF)

Parameter		Symbol	Min	Typ	Max	Units
SCLK period		t_{sckw}	80	-	-	ns
SCLK high time		t_{sckh}	25	-	-	ns
SCLK low time		t_{sckl}	25	-	-	ns
Input Transition Time	10% to 90% points		-	-	10	ns
Input Clock Frequency	Crystals XTI		32 32	- -	26000 26000	kHz kHz
Input Clock (XTI) low time			30	-	-	ns
Input Clock (XTI) high time			30	-	-	ns
Input clock jitter tolerance			-	500	-	ps
PLL clock recovery frequency	LRCK, LRCKAUX SCLK, SCLKAUX		32 2.048	- -	50 3.200	kHz MHz
CLKOUT duty cycle			45	50	55	%
Audio ADC's & DAC's sample rate		Fs	4	-	50	kHz
$\overline{RST}$-PDN low time	(Note 5)		500	-	-	ns
MSB output from LRCK edge (Format 1 and 3)		t_{lrpd}	-	-	50	ns
SDOUT output from SCLK edge		t_{dpd}	-	-	50	ns
SDIN setup time before SCLK edge		t_{ds}	-	-	35	ns
SDIN hold time after SCLK edge		t_{dh}	-	-	35	ns
LRCK to SCLK delay (slave mode)		t_{lrckd}	35	-	-	ns
LRCK to SCLK setup (slave mode)		t_{lrcks}	35	-	-	ns
LRCK to SCLK alignment (master mode)		t_{mslr}	-20	-	20	ns

Note: 5. After Powering up the CS4225, $\overline{RST}$-PDN should be held low for 50 ms to allow the voltage reference to settle.



Audio Ports Master Mode Timing



*Active edge of SCLK, SCLKAUX depends on selected format.

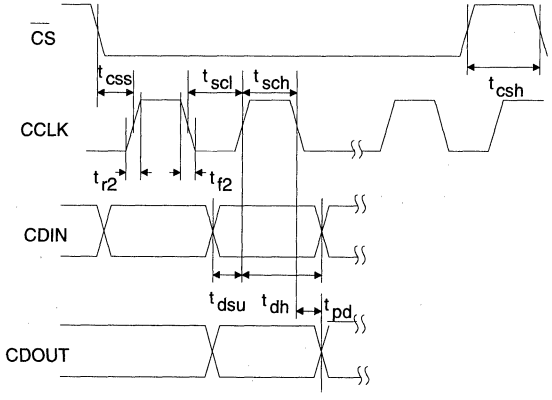
Audio Ports Slave Mode and Data I/O timing

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25°C VD+, VA+ = 5V±10%; Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 30pF)

Parameter		Symbol	Min	Max	Units
SPI Mode ($H/\overline{S}$=0)					
CCLK Clock Frequency		f_{sck}	0	1	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
$\overline{CS}$ Falling to SCK Edge		t_{css}	20		ns
CCLK Low Time		t_{scl}	500		ns
CCLK High Time		t_{sch}	500		ns
CDIN to CCLK Rising Setup Time		t_{dsu}	250		ns
CCLK Rising to DATA Hold Time	CDIN (Note 9)	t_{dh}	50		ns
CCLK Falling to CDOUT stable		t_{pd}		250	ns
Rise Time of CDOUT		t_{r1}		25	ns
Fall Time of CDOUT		t_{f1}		25	ns
Rise Time of CCLK and CDIN		t_{r2}		100	ns
Fall Time of CCLK and CDIN		t_{f2}		100	ns

Notes: 9. Data must be held for sufficient time to bridge the transition time of CCLK.

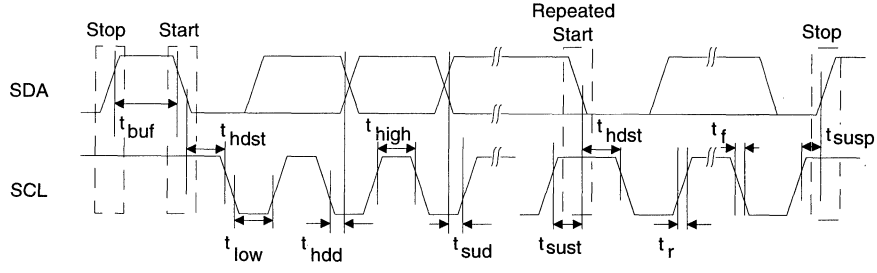


SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25°C; VD+, VA+ = 5V±10%;Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Max	Units
I^2C® Mode (H/$\overline{S}$ = floating) Note 10				
SCL Clock Frequency	f_{scl}	0	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0		µs
Clock Low Time	t_{low}	4.7		µs
Clock High Time	t_{high}	4.0		µs
Setup Time for Repeated Start Condition	t_{sust}	4.7		µs
SDA Hold Time from SCL Falling Note 11	t_{hdd}	0		µs
SDA Setup Time to SCL Rising	t_{sud}	250		ns
Rise Time of Both SDA and SCL Lines	t_r		1	µs
Fall Time of Both SDA and SCL Lines	t_f		300	ns
Setup Time for Stop Condition	t_{susp}	4.7		µs

Notes: 10. Use of the I^2C® bus interface requires a license from Philips.
I^2C® is a registered trademark of Philips Semiconductors.
11. Data must be held for sufficient time to bridge the 300ns transition time of SCL.



ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD	-0.3	-	6.0	V
	Analog	VA	-0.3	-	6.0	V
Input Current	(Except Supply Pins)		-	-	±10.0	mA
Analog Input Voltage			-0.3	-	(VA+)+0.3	V
Digital Input Voltage			-0.3	-	(VD+)+0.3	V
Ambient Temperature	(Power Applied)		-55	-	+125	°C
Storage Temperature			-65	-	+150	°C

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD	4.6	5.0	5.4	V
	Analog	VA	4.6	5.0	5.4	V
Operating Ambient Temperature	CS4225-KL		0	25	70	°C
	CS4225-BL	T_A	-40	25	+85	°C
	CS4225-YU		-40	25	+85	°C

DIGITAL CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V)

Parameter		Symbol	Min	Typ	Max	Units
High-level Input Voltage		V_{IH}	(VD+)-1.0	-	(VD+)+0.3	V
Low-level Input Voltage		V_{IL}	-0.3	-	1.0	V
High-level Output Voltage at I_o = -2.0 mA		V_{OH}	(VD+)-0.3	-	-	V
Low-level Output Voltage at I_o = 2.0 mA		V_{OL}	-	-	0.1	V
Input Leakage Current	(Digital Inputs)		-	-	10	µA
Output Leakage Current	(High-Z Digital Outputs)		-	-	10	µA

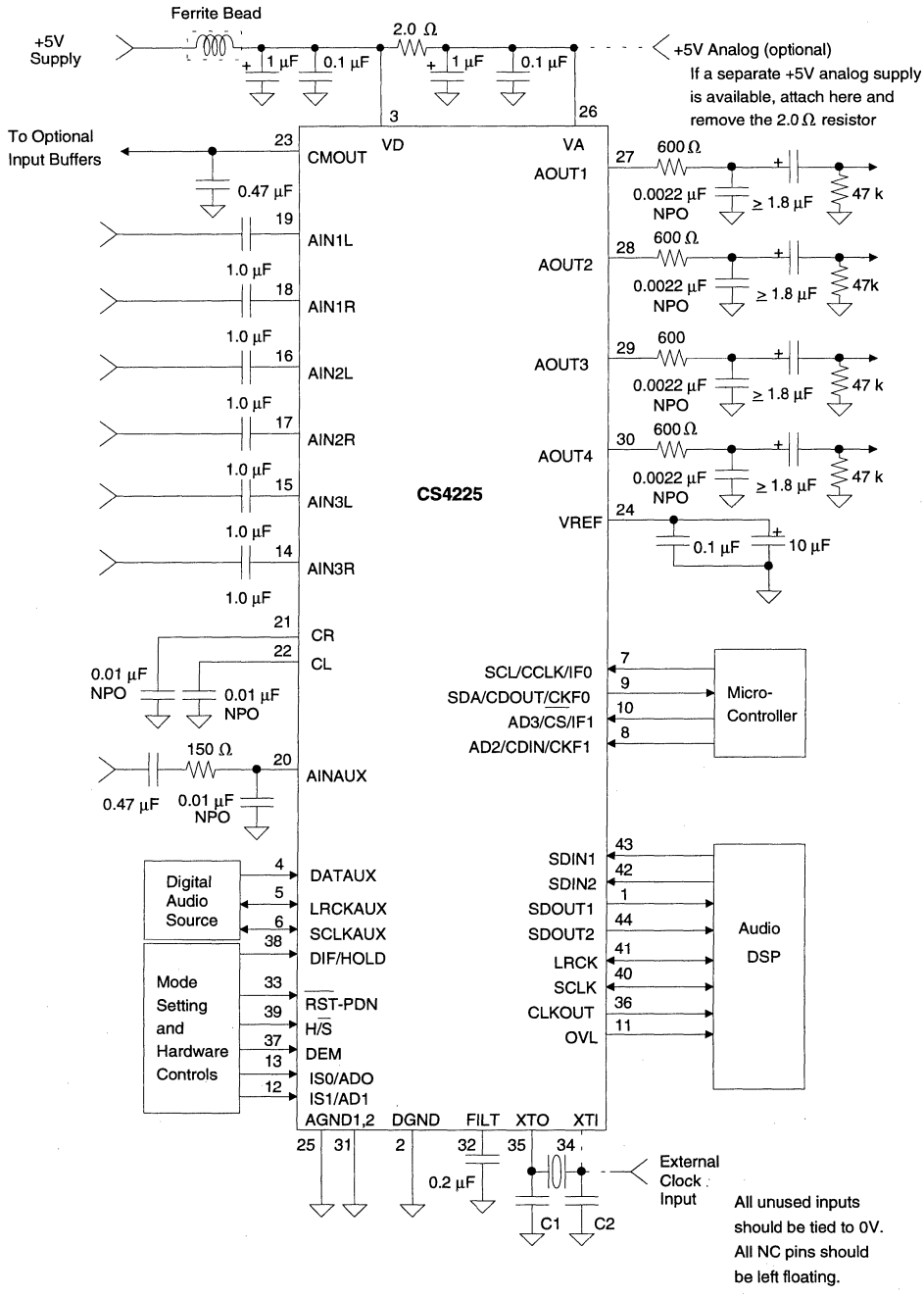


Figure 1 - Recommended Connection Diagram

FUNCTIONAL DESCRIPTION

Overview

The CS4225 has 2 channels of 16-bit analog-to-digital conversion and 4 channels of 16-bit digital-to-analog conversion. An auxiliary 12-bit ADC is also provided. The ADCs and the DACs are delta-sigma type converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation.

Digital audio data for the DACs and from the ADCs is communicated over a serial port. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Control for the functions available on the CS4225 are communicated over a serial microcontroller style interface, or may be set via dedicated mode pins. Figure 1 shows the recommended connection diagram for the CS4225.

Analog Inputs

Line Level Inputs

AIN1R, AIN1L, AIN2R, AIN2L, AIN3R, AIN3L and AINAUX are the line level input pins (See Figure 1). These pins are internally biased to the CMOUT voltage (nominally 2.1V). A 1µF DC blocking capacitor allows signals centered around 0V to be input. Figure 2 shows an optional dual op amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of $2V_{rms}$ to $1V_{rms}$. The CMOUT reference level is used to bias the op amps to approximately one half the supply voltage.

Series DC blocking capacitors eliminate the contribution of signal offset to the A/D converters. The CS4225 offset calibration scheme yields minimum DC offset values assuming that the inputs are AC coupled (DC blocking capacitor present). If a DC blocking capacitor is not used, a greater DC offset will occur. This offset could be as high as ± 70 codes, with no gain.

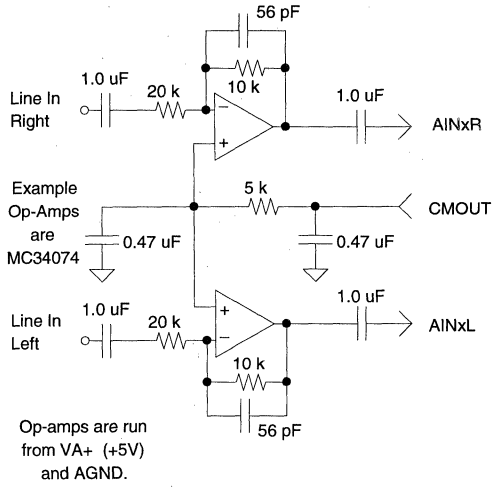


Figure 2 - Optional Line Input Buffer

The input pair for the 16-bit ADCs is selected by IS0 and IS1, which are accessible in the Input Selection Byte in software mode or dedicated pins in the hardware mode. Antialiasing filters follow the input mux, providing antialiasing for the input channels. These filters consist of internal resistors and external capacitors attached to the CR and CL pins. The CR and CL capacitors must be low voltage coefficient type, such as NPO.

The analog signal is input to the 12-bit ADC via the AINAUX pin. An antialiasing filter of 150Ω with 0.01µF to ground is required (See Figure 1) along with a series DC blocking capacitor. The AINAUX signal is normally routed to the 12-bit ADC. This signal may also be routed to the Left 16-bit ADC (replacing the selected left input), under control of the AIM bit in the 12-bit ADC Mode Byte. In this mode, the input antialiasing filters and gain adjustment operates on the AINAUX signal.

Adjustable Input Gain

The signals from the line inputs are routed to a programmable gain circuit which provides up to

46.5dB of gain in 1.5dB steps. The gain is adjustable only by software control. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out of 511 frames (10.6ms at 48kHz frame rate). There is a separate zero crossing detector for each channel.

Analog Outputs

Line Level Outputs

AOUT1, AOUT2, AOUT3 and AOUT4 output a $1V_{rms}$ level for full scale, centered around +2.1V. Figure 1 shows the recommended 1.0µF dc blocking capacitor with a 40kΩ resistor to ground. When driving impedances greater than 10kΩ, this provides a high pass corner of 20Hz. These outputs may be muted.

Output Level Attenuator

The DAC outputs are each routed through an attenuator, which is adjustable in 1dB steps. Output attenuation is available via software control only. Level changes are implemented such that the noise is attenuated by the same amount as the signal (equivalent to using an analog attenuator after the signal source), until the residual output noise is equal to the noise floor in the mute state. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out of 511 frames (10.6ms at 48kHz frame rate). There is a separate zero crossing detector for each channel.

Each output can be independently muted via mute control bits. In addition, the CS4225 has an optional mute on consecutive zeros feature, where each DAC output will mute if it receives 512 consecutive zeros. A single non-zero value will unmute the DAC output.

ADC and DAC Coding

The CS4225 converters use 2's complement coding. Table 1 shows the ADC and DAC transfer functions.

16-bit ADC/DAC		12-bit ADC	
Input/ Output Voltage*	2's Complement Code	2's Complement Code	Input Voltage*
+1.400000	7FFF	7FF	+1.40000
+1.399957	7FFE	7FE	+139864
+0.000064	0001	001	+0.00204
+0.000021	0000	000	+0.00068
-0.000021	FFFF	FFF	-0.00068
-0.000064	FFFE	FFE	-0.00204
-1.399957	8001	801	-1.39864
-1.400000	8000	800	-1.40000

*Nominal voltage relative to CMOUT (Typ 2.1V), no gain or attenuation. Actual measured voltage will be modified by the gain error and offset error specifications.

Table 1 - ADC/DAC Input and Output Coding Table

Calibration

Both output offset voltage and input offset error are minimized by an internal calibration cycle. At least one calibration cycle must be invoked after power up. A calibration will occur any time the part comes out of reset, including the power-up reset. For the most accurate calibration, some time must be allowed between powering up the CS4225, or exiting the power-down state, and initiating a calibration cycle, to allow the voltage reference to settle. This is achieved by holding $\overline{RST}$/PDN low for at least 50ms after power up or exiting power-down mode. Input offset error will be calibrated for all inputs and outputs.

A calibration takes 192 frames to complete, based on the frequency of the VCO of the inter-

nal PLL. The calibration that occurs following a reset will proceed at a rate determined by the free running VCO in software mode (which will be at a Fs of about 40kHz), or the selected clock input in hardware mode.

The CS4225 can be calibrated whenever desired. A control bit, CAL, in the Control Byte, is provided to initiate a calibration. The sequence is:
1) Set CAL to 1, the CS4225 sets $\overline{\text{CALD}}$ to 1 and begins to calibrate.
2) Wait for $\overline{\text{CALD}}$ to go to 0. $\overline{\text{CALD}}$ will go to 0 when the calibration is done.
3) Set CAL to 0 for normal operation.

Clock Generation

The master clock to operate the CS4225 may be generated by using the on-chip crystal oscillator, by using the on-chip PLL, or by using an external clock source. If the active clock source stops for 5µs, the CS4225 will enter a power down state to prevent overheating. In all modes it is desirable to have SCLK & LRCK synchronous to the selected master clock.

Clock Source

The CS4225 requires a high frequency (256 Fs) clock to run the internal logic. The Clock Source bits, CS0/1/2, in the Clock Mode Byte determine the source of the clock. A high frequency crystal can be attached to XTI and XTO, or a high frequency clock can be input into XTI. In both these cases, the internal PLL is disabled, with the VCO shut off. The externally supplied high frequency clock can be 256 Fs, 384 Fs or 512 Fs. The CI0/1 bits in the Clock Mode Byte must be set accordingly. When using the on-chip crystal oscillator, external loading capacitors are required (see Figure 1). High frequency crystals (> 8 MHz) should be parallel resonant, fundamental mode and designed for 20pF loading (equivalent to 40pF to ground on each leg). An example crystal supplier is CAL crystal (714) 991-1580.

Alternatively, the on-chip PLL may be used to generate the required high frequency clock. The PLL input clock is either 1 Fs, 32 Fs or 64 Fs and may be input from the Auxiliary Port, (either LRCKAUX or SCLKAUX), the DSP port, (either LRCK or SCLK), or from XTI/XTO. In this last case, a 1 Fs clock may be input into XTI, or a 1 Fs crystal attached across XTI/XTO. The gain of the internal inverter is adjusted for the low crystal frequency. Using a clock at 64 Fs will result in less PLL clock jitter than a clock at 1 Fs. The PLL will lock onto a new 1 Fs clock within 5,000 Fs periods. If the PLL input clock is removed, the VCO will drift to the low frequency end of its frequency range.

In software mode, bits CS2/1/0 in the Clock Mode Byte establish the clock source and frequency. In Hardware mode, either LRCKAUX is the clock reference, at 1 Fs, or the clock may be input to XTI.

Master Clock Output

CLKOUT is a master clock output provided to allow synchronization of external components. Available CLKOUT frequencies of 1 Fs, 256 Fs, 384 Fs, and 512 Fs, are selectable by the CO0/1 bits of the Clock Mode Byte. When switching between clock sources, CLKOUT will always remain low or high for > 10ns.

Synchronization

In normal operation, the DSP port and Auxiliary port operate synchronously to the CS4225 clock source. It is advisable to mute the DACs when changing from one synchronization source to another to avoid the output of undesirable audio signals as the CS4225 resynchronizes. If data which is not synchronous to the clock source is input to the CS4225, then samples will be dropped or repeated, which will cause audible artifacts. Under such conditions, the CS4225 may not meet all data sheet performance specifications.

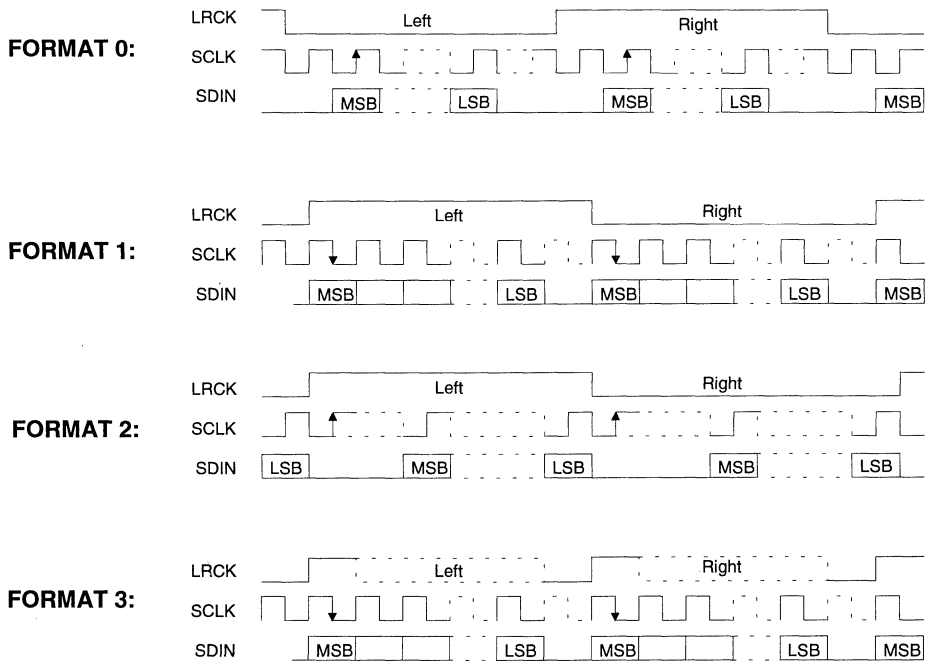


Figure 3 - Audio DSP and Auxiliary Port Data Input Formats.

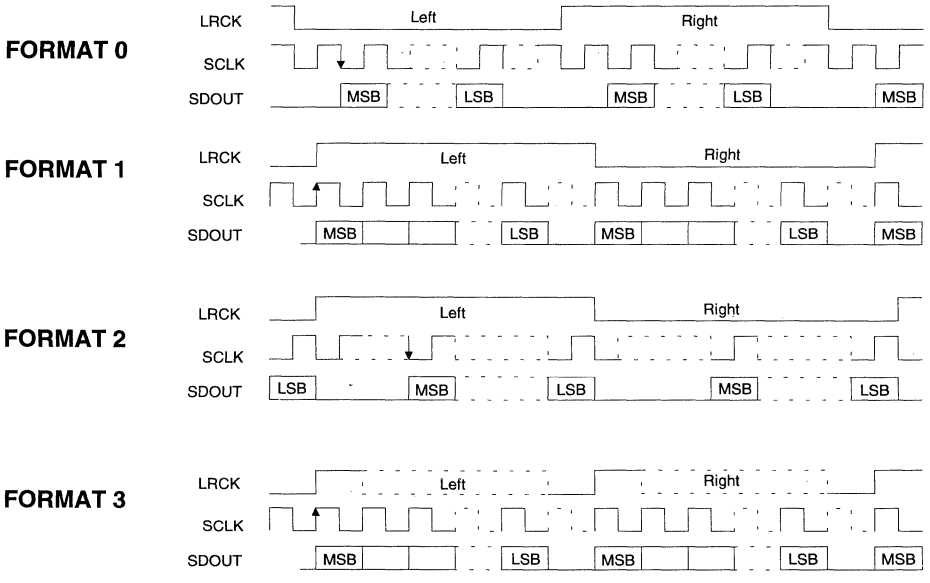


Figure 4 - Audio DSP Port Data Output Formats.

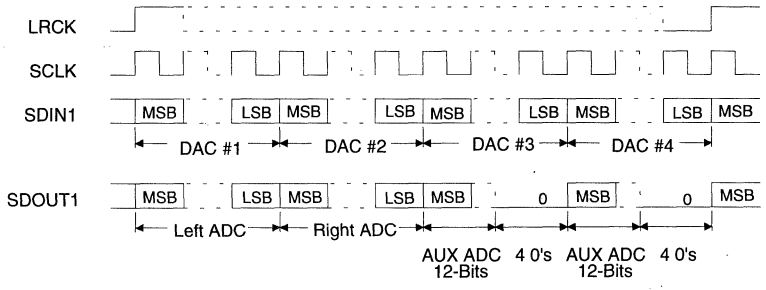


Figure 5 - One data line mode (Format 4)

Digital Interfaces

There are 3 digital interface ports: the audio DSP port, the auxiliary digital audio port and the control port. In hardware mode (H/$\overline{S}$ pin high) the control port is disabled, and various modes can be set via pins. In hardware mode, control of the input gain, output level and some modes are not possible.

Audio DSP Serial Interface Signals

The serial interface clock, SCLK, is used for transmitting and receiving audio data. SCLK can be generated by the CS4225 (master mode) or it can be input from an external SCLK source (slave mode). The number of SCLK cycles in one system sample period is programmable to be 32, 48, or 64. When SCLK is an input, 32 SCLK's per system sample period is not recommended, due to potential interference effects; 64 SCLK's per sample period should be used instead.

The Left/Right clock (LRCK) is used to indicate left and right data, also the start of a new sample period. It may be output from the CS4225, or it may be generated from an external controller. The frequency of LRCK is equal to the system sample rate, Fs.

SDIN1 and SDIN2 are the data input pins, each of which drives a pair of DACs. SDIN1 left data is for DAC #1, SDIN1 right data is for DAC #2, SDIN2 left data is for DAC #3, and SDIN2 right data is for DAC #4. SDOUT1 carries the data from the 2 16-bit ADCs. SDOUT2 carries the data from the 12-bit ADC. The audio DSP port may also be configured so that all 4 DAC's data is input on SDIN1, and all 3 ADC's data is output on SDOUT1.

Audio DSP Serial Interface Formats

The audio DSP port supports 5 alternate formats, shown in Figures 3, 4, and 5. These formats are chosen through the DSP Port Mode Byte in software mode. In hardware mode, four formats are available as selected by the DIF and IF0 pins.

The 12-bit ADC data format is similar to the 16-bit data format. The 12-bit data is positioned to the most significant end of a 16-bit field, with the lower 4 bits set to zero. The resulting 16-bit value is output on SDOUT2 in both the left and right channel positions. The format will be the same as the selected SDOUT1 format.

Figure 5 shows the timing for format 4, where all 4 DAC data words are presented on SDIN1, and the 3 ADC data words are presented on SDOUT1.

Format 5 is a combination mode. The data output is as in Format 1, on the SDOUT1 and SDOUT2 pins. The data input is as in Format 4 on SDIN1. In both format 4 and 5, LRCK duty cycle is 50% if it is an output.

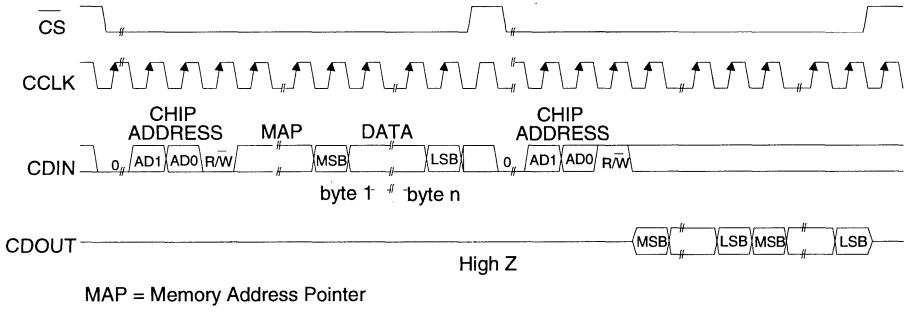


Figure 6 - Control Port Timing, SPI mode

Auxiliary Audio Port Signals

The auxiliary port provides an alternate way to input digital audio signals into the CS4225, and allows the CS4225 to synchronize the system to an external digital audio source. This port consists of clock, data and left/right clock pins named, SCLKAUX, DATAAUX and LRCKAUX. These signals are fed through to the SCLK, SDOUT1 and LRCK pins. There is a two frame delay from DATAAUX to SDOUT1. When the auxiliary port is used, the frequency of LRCKAUX must equal to the system sample rate, Fs, but no particular phase relationship is required.

Auxiliary Audio Port Formats

Input data on DATAAUX is clocked into the part by SCLKAUX using the format selected in the Auxiliary Port Mode Byte. In hardware mode, the auxiliary port format is the same as the DSP port format and is determined by the DIF pin. The auxiliary audio port supports the same 4 formats as the audio DSP port in 2 data line mode. LRCKAUX is used to indicate left and right data samples, and the start of a new sample period. SCLKAUX and LRCKAUX may be output from the CS4225, or they may be generated from an external source, as set by the AMS control bit in Software mode or IF1 in Hardware mode.

Control Port Signals

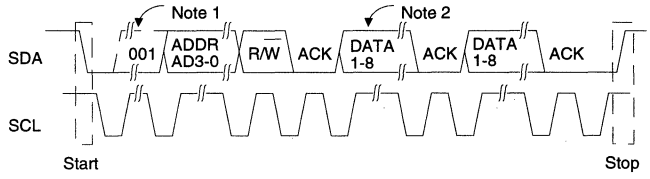
The control port has 2 modes: SPI and $I^2C^®$, with the CS4225 as a slave device. The SPI mode is selected by setting the H/$\overline{S}$ pin low. $I^2C^®$ mode is selected by floating the H/$\overline{S}$ pin. If the H/$\overline{S}$ pin is floated, add a 0.1µF capacitor to ground on the H/$\overline{S}$ pin to minimize noise pickup.

SPI Mode

In SPI mode, $\overline{CS}$ is the CS4225 chip select signal, CCLK is the control port bit clock, (input into the CS4225 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller, and AD0 and AD1 form the chip address.

The pins AD0, AD1 must be tied to one of 4 possible chip addresses. To write to a particular CS4225, the AD0, AD1 bits must match the state of the AD0, AD1 pins for that chip. This allows up to 4 CS4225 devices to co-exist on one control port bus.

Figure 6 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 5 bits on CDIN must be zero. The next 2 bits form the chip address. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be



Note 1: The first 3 address bits for the CS4225 must be 001.
Note 2: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 7 - Control Port Timing, I²C® Mode

low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47kΩ resistor.

The CS4225 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive reads or writes. If INCR is set to a 1, then MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The auto MAP increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

I²C®Mode

In I²C® mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 7. There is no $\overline{CS}$ pin. Pins AD0, AD1, AD2, AD3 form the chip address. The upper 3 bits of the 7 bit address field must be 001. To communicate with a CS4225, the LSBs of the chip address field, which is the first byte sent to the CS4225, should match the settings of the AD0, AD1, AD2, AD3 pins. The eighth bit of the address bit is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. Use of the I²C bus®compatible interface requires a license from Philips. I²C bus® is a registered trademark of Philips Semiconductors.

Control Port Bit Definitions

All registers can be written and read back, except the status report byte, which is read only. See the following bit definition tables for bit assignment information.

Memory Address Pointer (MAP)

B7	B6	B5	B4	B3	B2	B1	B0
INCR	0	0	0	MAP3	MAP2	MAP1	MAP0

MAP3-MAP0 Register Function
- 0 - Reserved
- 1 - Output Attenuator 1
- 2 - Output Attenuator 2
- 3 - Output Attenuator 3
- 4 - Output Attenuator 4
- 5 - Input Gain 1
- 6 - Input Gain 2
- 7 - Auxiliary Port Mode
- 8 - DSP Port Mode
- 9 - Clock Mode
- 10 - Control Byte
- 11 - Status Report Byte
- 12 - Input Channel Select
- 13 - Aux Control Byte
- 14 - Reserved
- 15 - Reserved

INCR Auto Increment Control Bit
- 0 - No auto increment
- 1 - Auto increment on

Output Attenuator Data Byte (1, 2, 3, 4)

B7	B6	B5	B4	B3	B2	B1	B0
0	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT6 to ATT0 Sets Attenuator Level
- 0 - No attenuation
- 127 - 127 dB attenuation
- ATT0 represents 1.00 dB

Input Gain Setting Data Byte (5, 6)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	GN4	GN3	GN2	GN1	GN0

GN4 to GN0 Sets Input Gain
- 0 - No gain
- 31 - 46.5 dB gain
- GN0 represents 1.5 dB

Auxiliary Port Mode Byte (7)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	AMS	ACK1	ACK0	ADF1	ADF0

ADF1 - ADF0 Sets Digital Interface Format
- 0 - Format 0 - I^2S
- 1 - Format 1
- 2 - Format 2
- 3 - Format 3

ACK1 - ACK0 Sets number of bit clocks per Fs period
- 0 - 64
- 1 - 48 - gated 64Fs
- 2 - 32 - gated 64Fs
- 3 - 32 - continuous

AMS AUX Master /Slave control bit
- 0 - port is master (SCLKAUX and LRCKAUX are outputs).
- 1 - port is slave (SCLKAUX and LRCKAUX are inputs).

DSP Port Mode Byte (8)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	DMS	DCK1	DCK0	DDF2	DDF1	DDF0

DDF2 - DDF0 Sets Digital Interface Format
- 0 - Format 0 - I^2S
- 1 - Format 1
- 2 - Format 2
- 3 - Format 3
- 4 - One data pin in, One data pin out mode (Format 4).
- 5 - Output is Format 1 on SDOUT1 and SDOUT2, input is Format 4 on SDIN1.

DCK1 - DCK0 Set number of bit clocks per Fs period
- 0 - 64
- 1 - 48 - gated 64 Fs
- 2 - 32 - gated 64 Fs
- 3 - 32 - continuous

DMS DSP Master /Slave control bit
- 0 - port is master (SLCK and LRCK are outputs).
- 1 - port is slave (SLCK and LRCK are inputs).

Clock Mode Byte (9)

B7	B6	B5	B4	B3	B2	B1	B0
0	CO1	CO0	CI1	CI0	CS2	CS1	CS0

CS1 - CS0 Sets the source of the master clock which runs the CS4225.
0 - Crystal Oscillator or XTI (PLL Disabled)
1 - PLL driven by LRCKAUX at 1 Fs
2 - PLL driven by LRCK at 1 Fs
3 - PLL driven by XTI/XTO (XTI at 1 Fs)
4 - PLL driven by SCLK at 32 Fs
5 - PLL driven by SCLK at 64 Fs
6 - PLL driven by SCLKAUX at 32 Fs
7 - PLL driven by SCLKAUX at 64 Fs

CI1 - CI0 Determines frequency of XTI when PLL is disabled.
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - Reserved

CO1-CO0 Determines CLKOUT frequency
0 - 256 Fs
1 - 384 Fs
2 - 512 Fs
3 - 1 Fs

Control Byte (10)

B7	B6	B5	B4	B3	B2	B1	B0
MUTC	CAL	DEMC	DEM	MUT4	MUT3	MUT2	MUT1

MUT4 to MUT1 Mute Control Bits
0 - Normal Output Level
1 - Selected DAC output muted

DEM Selects De-Emphasis
0 - Normal Flat DAC frequency response
1 - CD De-Emphasis Selected

DEMC Selects De-Emphasis Control Source
0 - De-emphasis is controlled by DEM pin. DEM bit is ignored.
1 - De-emphasis is controlled by DEM bit. DEM pin is ignored.

CAL
0 - Normal Operation
1 - Initiate Calibration

MUTC Controls mute on consecutive zeros function
0 - 512 consecutive zeros will mute DAC
1 - DAC output will not mute on zeros.

Status Report Byte (11)

B7	B6	B5	B4	B3	B2	B1	B0
OVL1	OVL0	OV12	ACK	0	LOCK	$\overline{\text{CALD}}$	0

OVL1 to OVL0 16 - bit ADC overload bits.
00 - Normal ADC input levels
01 - -6 dB level
10 - -3 dB level
11 - Clipping
Indicates one of the ADC's has been overdriven. These bits are "sticky". They will stay set until read, when they will return to 00 if the overload is no longer present.

OV12 12-bit ADC overload bit
0 - normal input
1 - clipped input
This bit is also "sticky"

ACK Control port data check bit
0 - Multiple of 8 clocks received last word (SPI Mode)
1 - Error, not multiple of 8 clocks received.

LOCK PLL lock indicator
0 - PLL not locked. If PLL is selected, DAC outputs will mute
1 - PLL locked

$\overline{\text{CALD}}$
0 - Calibration done
1 - Calibration in progress

Input Selection Byte (12)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	IS1	IS0

IS1 - IS0 Select input channel
0 - Select AIN1
1 - Select AIN2
2 - Select AIN3
3 - Select Auxiliary Digital Input Port

Aux Control Byte (13)

B7	B6	B5	B4	B3	B2	B1	B0
AIM	0	0	0	0	0	0	0

AIM Auxiliary Input Mode Control Bit
0 - AINAUX signal is routed to 12-bit ADC
1 - AINAUX routed to AINL of 16-bit ADC

Reset

$\overline{\text{RST}}$-PDN going low causes all the internal control registers, used in software mode, to be set to the states indicated in Table 1. The reset states are different for hardware mode, see the section on Hardware Mode. $\overline{\text{RST}}$-PDN must be brought low and high at least once after power up. $\overline{\text{RST}}$-PDN returning high causes the CS4225 to execute an offset calibration cycle. $\overline{\text{RST}}$-PDN returning high should occur at least 50ms after the power supply has stabilized.

Power Down Mode

Placing the $\overline{\text{RST}}$-PDN pin into a high impedance state (floating) puts the CS4225 into the power down mode. This may be done by driving the $\overline{\text{RST}}$-PDN pin with a three-state buffer, and setting the buffer to the hi-z state. In power-down mode CMOUT and VREF will not supply current. If the master clock source stops, the CS4225 will power down after 5µs. Power down will change all the control registers to the reset state shown in Table 1.

ATT6 → ATT0	= 127	CS2, CS1,CS0	= 3
GN4 → GN0	= 0	CI1, CI0	= 0
ADF1, ADF0	= 0	CO1, CO0	= 0
ACK1, ACK0	= 0	MUT4 →MUT1	= 1111
AMS	= 1	DEM	= 0
DDF2 → DDF0	= 0	DEMC	= 0
DCK1, DCK1	= 0	MUTC	= 0
DMS	= 1	IS1, IS0	= 0
MAP	= 0	AIM	= 0
CAL	= 0		

Table 1 - Reset State (Software Mode)

After returning to normal operation from power down, an offset calibration cycle must be executed. To leave the power-down state, pull $\overline{\text{RST}}$-PDN low for at least 50ms to allow the internal voltage reference time to settle, then high to initiate an offset calibration cycle.

De-Emphasis

Figure 8 shows the de-emphasis curve. De-emphasis may be enabled under hardware control, using the DEM pin, or by software control using the DEM bit. In software mode, either hardware or software control of de-emphasis may be selected.

The de-emphasis corner frequencies are as shown in Figure 8 for a sample rate of 44.1kHz. Selection of de-emphasis at other sample rates will cause the filter to be applied, but with corner frequencies scaled proportionally to the sample rate.

Hold Function (Software Mode only)

If the digital audio source has an invalid data output pin, then the CS4225 may be configured to cause the last valid analog output level to be held constant. (This sounds much better than a potentially random output level.) HOLD is sampled on the active edge of SCLK. If HOLD is driven high any time during the stereo sample period, both pairs of DAC's hold their current output level, and reject the data currently being input. SDIN input data is ignored while the HOLD pin is high. For normal operation, the HOLD pin must be low.

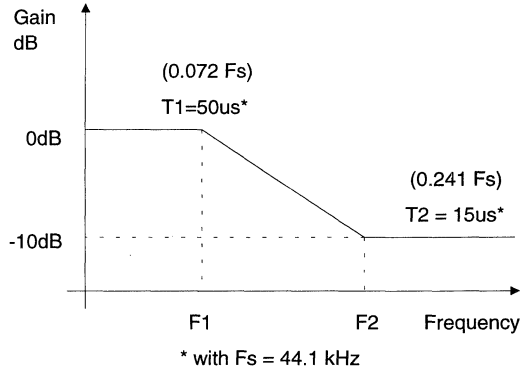


Figure 8 - De-emphasis Curve.

Hardware Mode

Hardware mode is selected by connecting the H/$\overline{S}$ pin to VD. In hardware mode, only certain functions are available:

- de-emphasis,
- digital interface formats 0, 1 and 2, and DSP format 4,
- auxiliary audio port master/slave selection,
- CLKOUT and XTI frequencies are restricted,
- use of PLL is tied to master/slave selection,
- the PLL locks to LRCKAUX only,
- will mute on consecutive zeros.

In addition, the input gain is set to 0dB (no gain), and the attenuator is set to 0dB (no attenuation). The DAC mute bits are set to 0 (not muted). The DSP port and Auxiliary port serial clocks are set to 64 bits per Fs period.

In hardware mode, the DSP port is always in slave mode. The IF1 pin selects the Auxiliary port to be master or slave (low for master, high for slave). When the Auxiliary port is a master, XTI is the clock source and the PLL is off. CKF0 and CKF1 pins define both XTI and CLKOUT frequencies as follows:

CKF1	CKF0	XTI	CLKOUT
0	0	256 Fs	256 Fs
0	1	384 Fs	256 Fs
1	0	512 Fs	256 Fs
1	1	512 Fs	512 Fs

When the Auxiliary port is a slave, LRCKAUX is the clock source at 1 Fs, the PLL is enabled. CKF1 and CKF0 determine CLKOUT as follows:

CKF1	CKF0	CLKOUT
0	0	256 Fs
0	1	384 Fs
1	0	512 Fs
1	1	1 Fs

Functions only available in software mode include:

- input gain adjust & output level adjust,
- digital interface format 3, DSP format 5,
- more clocking flexibility,
- DAC muting,
- setting of number of bit clocks per Fs period,
- turn off mute upon consecutive zeros function,
- 12-bit ADC clipping indicator,
- PLL lock flag,
- routing the AINAUX signal to a 16-bit ADC,
- hold last sample on error.

Power Supply and Grounding

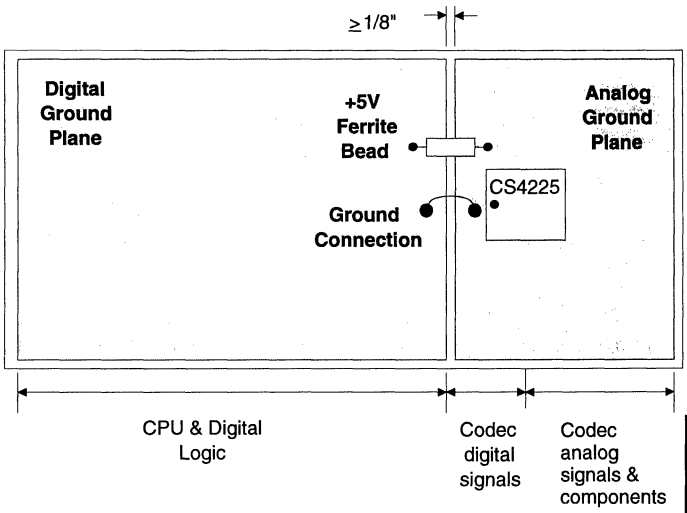
The CS4225, along with associated analog circuitry, should be positioned near to the edge of your circuit board, and have its own, separate, ground plane (see Figure 9). Preferably, it should also have its own power plane. The +5V supply must be connected to the CS4225 via a ferrite bead, positioned closer than 1" to the device. A single connection between the CS4225 ground and the board ground should be positioned as shown in Figure 9. Figure 10 shows the recommended decoupling capacitor layout. Also see Crystal's layout Applications Note, and the CDB4225 evaluation board data sheet for recommended layout of the decoupling components.

The CS4225 will mute the analog outputs if the supply drops below approximately 4 volts.

ADC and DAC Filter Response Plots

Figures 11 through 18 show the overall frequency response, passband ripple and transition band for the CS4225 ADC's and DAC's. Figure 17 shows the DAC's deviation from linear phase.

The 12-bit ADC output is fully decimated to Fs, but is not filtered. Figure 18 shows the noise floor of the output, along with a low frequency full scale signal. External digital filtering is necessary to achieve the desired trade off between measurement bandwidth and dynamic range.



Note that the CS4225 is oriented with its digital pins towards the digital end of the board.

Figure 9. Suggested Layout Guideline

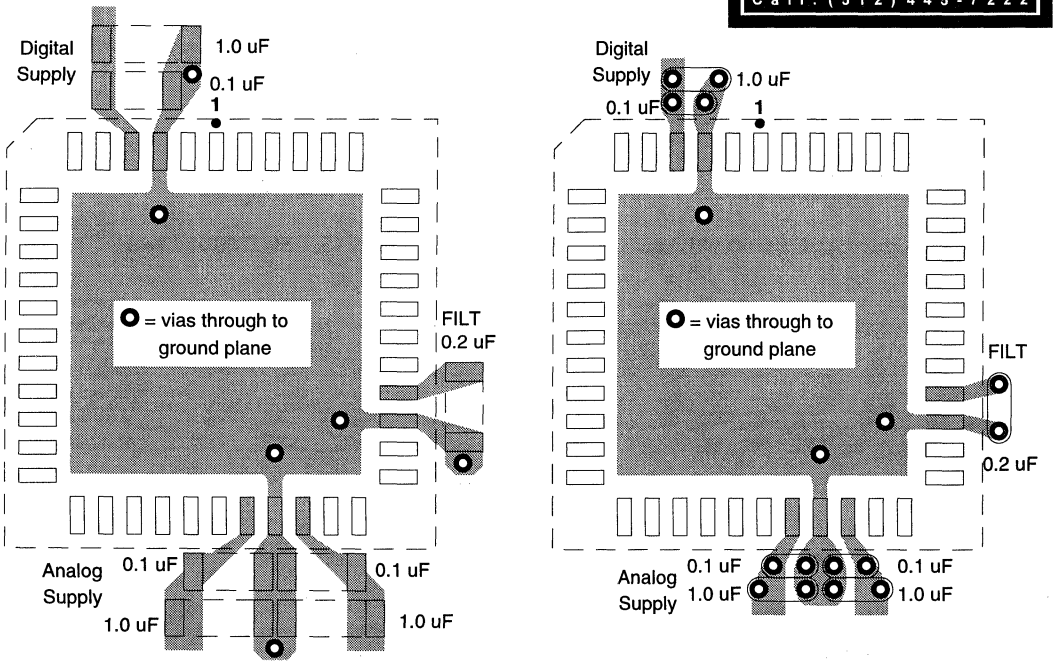


Figure 10. Recommended Decoupling Capacitor Layout

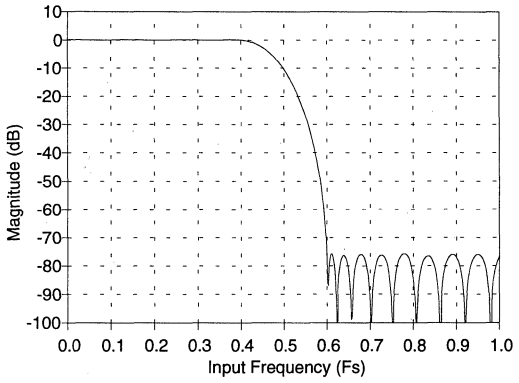


Figure 11. 16-bit ADC Filter Response.

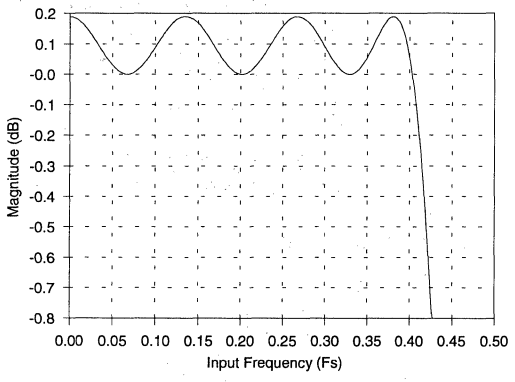


Figure 12. 16-bit ADC Passband Ripple.

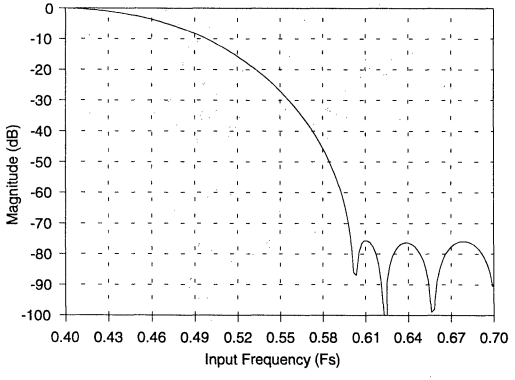


Figure 13. 16-bit ADC Transition Band.

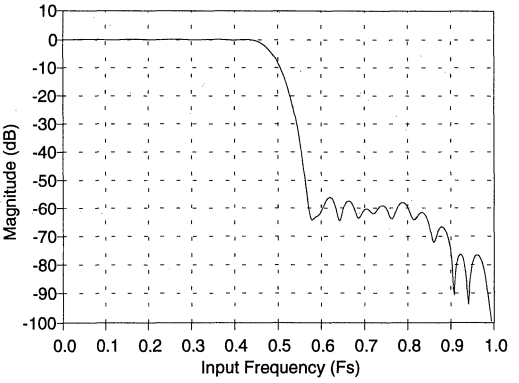


Figure 14. DAC Frequency Response.

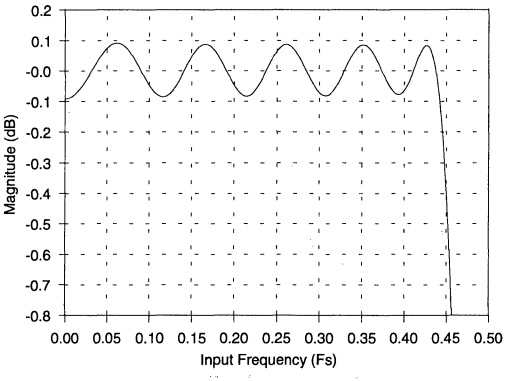


Figure 15. DAC Passband Ripple.

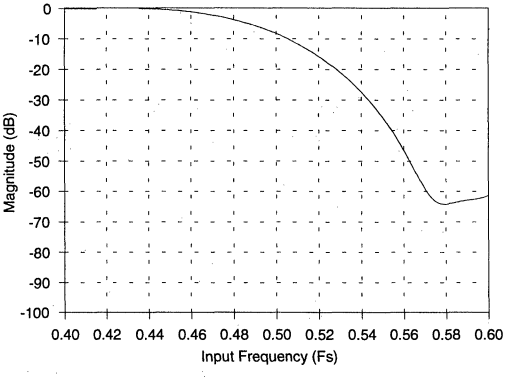


Figure 16. DAC Transition Band.

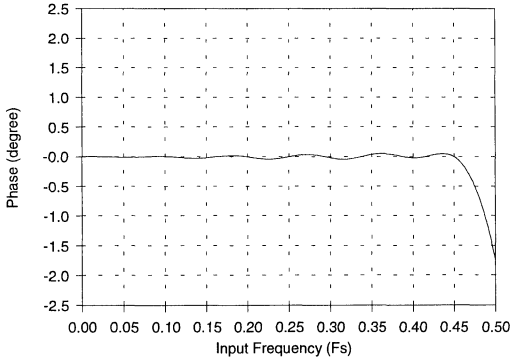


Figure 17. DAC Phase Response.

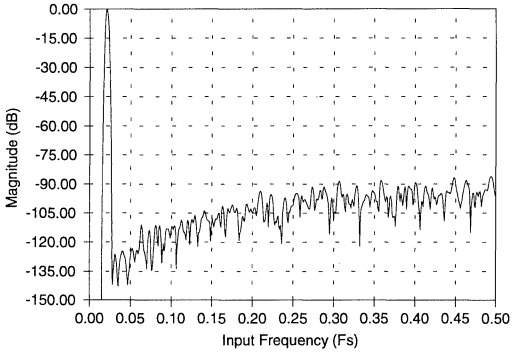
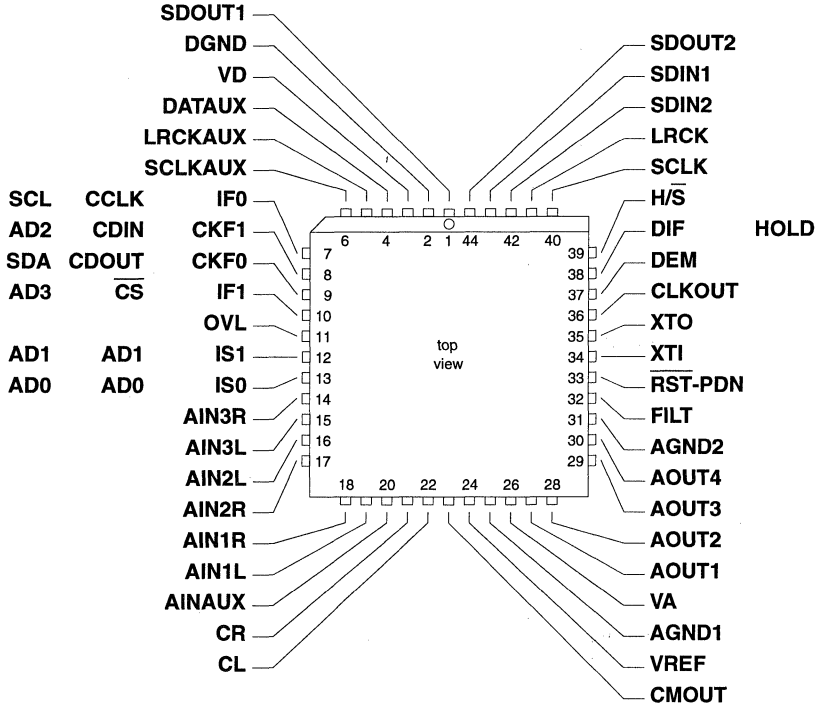


Figure 18. 12-bit ADC Noise with a Low Frequency Full Scale Sine wave input signal.

PIN DESCRIPTIONS



Power Supply

VA - Analog Power Input
+5 V analog supply.

AGND1, AGND2 - Analog Ground
Analog grounds.

VD - Digital Power Input
+ 5 V digital supply.

DGND - Digital Ground
Digital ground.

Analog Inputs

AIN1L, AIN1R - Left and Right Channel Mux Input 1
Analog signal input connections for the right and left channels for multiplexer input 1.

AIN2L, AIN2R - Left and Right Channel Mux Input 2
Analog signal input connections for the right and left channels for multiplexer input 2.

AIN3L, AIN3R - Left and Right Channel Mux Input 3
Analog signal input connections for the right and left channels for multiplexer input 3.

AINAUX - Auxiliary Line Level Input
Analog signal input for the 12-bit A/D converter. In software mode, setting the AIM bit causes AINAUX to replace the left analog input at the multiplexer input.

Analog Outputs

AOUT1, AOUT2, AOUT3, AOUT4 - Audio Outputs
The analog outputs from the 4 D/A converters. Each output can be independently controlled for output amplitude.

CMOUT - Common Mode Output
This common mode voltage output may be used for level shifting when DC coupling is desired. The load on CMOUT must be DC only, with an impedance of not less than 25kΩ. CMOUT should be bypassed with a 0.47µF to AGND.

VREF - Voltage Reference Output, Pin 21
The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10µF capacitor in parallel with a 0.1µF capacitor to the adjacent AGND pin. No other external load may be connected to this output.

Digital Interface Signals

SDIN1 - Serial Data Input 1
Digital audio data for the DACs 1 and 2 is presented to the CS4225 on this pin.

SDIN2 - Serial Data Input 2
Digital audio data for the DACs 3 and 4 is presented to the CS4225 on this pin.

SDOUT1- Serial Data Output 1
Digital audio data from the 16-bit audio ADCs is output from this pin. When selected, DATAAUX is output on SDOUT1.

SDOUT2 - Serial Data Output 2
Digital audio data from the 12-bit audio ADC is output from this pin.

SCLK - DSP Serial Port Clock I/O
SCLK clocks digital audio data into the DACs via SDIN1/2, and clocks data out of the ADCs on SDOUT1/2. Active clock edge depends on the selected format.

LRCK - Left/Right Select Signal I/O

The Left/Right select signal. This signal has a frequency equal to the sample rate. The relationship of LRCK to the left and right channel data depends on the selected format.

$\overline{\text{RST}}$-PDN - Reset and Power-Down Input

The CS4225 must be reset after power up by bringing this pin low, then high. To select power down mode, float this pin, or drive this pin with a three-state buffer, and place the buffer in the Hi-Z state. Low-to-high rise time should be less than 10µs.

DEM - De-emphasis Control

When high, DEM causes the standard Compact Disk de-emphasis frequency response for Fs = 44.1kHz to be applied to the DACs. If H/$\overline{\text{S}}$ is high, this pin is active. If H/$\overline{\text{S}}$ is low, then this pin is enabled by setting the DEMC control bit to 0, and disabled by setting the DEMC control bit to 1.

HOLD/DIF - Digital Interface Format Select Pin / HOLD Control

In software mode, when HOLD is high any time during the sample period, SDIN1 and SDIN2 data is ignored, and the previous "good" sample is presented to the DACs.

In hardware mode, DIF becomes a selection pin which selects audio data I/O formats 0, 1 and 2 (when IF0 is low) using a 3-level selection. Low selects format 0. High selects format 1. Floating selects format 2. Float DIF by tying a 0.01µF capacitor from DIF to ground. In hardware mode, both the auxiliary audio data port and the audio DSP port are set to the same audio format.

SCL/CCLK/IF0 - Serial Control Interface Clock / DSP Interface Mode Select.

In software control mode, SCL/CCLK is the serial control interface clock, and is used to clock control bits into and out of the CS4225.

In hardware control mode, when IF0 is low, the data for DACs 1 and 2 is input on SDIN1, and for DACs 3 and 4 is input on SDIN2. The data from the audio ADCs is presented on SDOUT1 and the data from the 12-bit auxiliary ADC is presented on SDOUT2. In hardware control mode, when IF0 is high, the data for all 4 DACs is input on the SDIN1 pin, and the data from the audio ADCs and the 12-bit auxiliary ADC is output on the SDOUT1 pin. This mode allows a DSP which has only 1 serial input and 1 serial output port to access all the DACs and ADCs.

AD3/$\overline{\text{CS}}$/IF1 - Control Port Chip Select / Interface Control

In $I^2C^®$ software control mode, AD3 is a chip address bit. In SPI software control mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4225.

In hardware control mode, IF1 low sets the auxiliary digital audio input port to be master and IF1 high sets the auxiliary digital audio input port to be slave. In slave mode, the PLL is used to generate the internal 256 Fs clock from LRCKAUX, and to generate CLKOUT.

AD2/CDIN/CKF1 - Serial Control Data In / Interface Control

In $I^2C^®$ mode, AD2 is a chip address bit. In SPI software control mode, CDIN is the input data line for the control port interface.

In hardware control mode, CKF0 and CKF1 controls the clock frequency of CLKOUT.

SDA/CDOUT/CKF0 - Serial Control Data Out / Clock Select

In $I^2C^®$ mode, SDA is the control data I/O line. In SPI software control mode, CDOUT is the output data from the control port interface on the CS4225.

In hardware control mode, CKF0 and CKF1 controls the clock frequency of CLKOUT.

DATAUX - Auxiliary Data Input

DATAUX is the auxiliary audio data input line, usually connected to an external digital audio source.

LRCKAUX - Auxiliary Word Clock Input or Output

In auxiliary slave mode, LRCKAUX is a word clock (at Fs) from an external digital audio source. LRCKAUX can be used as the clock reference for the internal PLL. In auxiliary master mode, LRCKAUX is a word clock output (at Fs) to clock an external digital audio source.

SCLKAUX - Auxiliary Bit Clock Input or Output

In auxiliary slave mode, SCLKAUX is the serial data bit clock from an external digital audio source, used to clock in data on DATAAUX. SCLKAUX can be used as the clock reference for the internal PLL. In auxiliary master mode, SCLKAUX is a serial data bit clock output.

AD0/IS0, AD1/IS1 - Input Select Control Pins

In software mode, these pins are part of the chip address.

In hardware mode, IS0 and IS1 select the audio input source from between 4 pairs of signals (AIN1, AIN2 and AIN3) and DATAUX.

H/$\overline{S}$ - Hardware or Software Control

Setting H/$\overline{S}$ high puts the CS4225 into hardware control mode, where many functions are controlled by dedicated pins. When H/$\overline{S}$ is low, many chip functions are controlled via the control port in SPI mode. When H/$\overline{S}$ is open circuit, then software mode $I^2C^®$ protocol is selected for the control port. When floating H/$\overline{S}$, a 100pF capacitor should be connected from the H/$\overline{S}$ pin to ground, to reduce the possibility of external interference influencing the pin.

OVL - Overload Indicator

If either of the 2 16-bit audio ADCs, or the 12-bit ADC, is clipped, then this pin goes high.

Clock and Crystal Pins

XTI, XTO - Crystal connections

Input and output connections for the crystal which may be used to operate the CS4225. Alternatively, a clock may be input into XTI.

CLKOUT - Master Clock Output

CLKOUT allows external circuits to be synchronized to the CS4225. Alternate output frequencies are selectable by the control port or via hardware pins.

Miscellaneous Pins

FILT - PLL Loop Filter Pin

A 0.22 µF capacitor should be connected from FILT to AGND.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth; expressed in LSBs.

Total Dynamic Range

The ratio between the DAC full scale output and the noise floor with the DAC muted. Units are in dB.

Total Harmonic Distortion + Noise (THD+N)

THD+N is the ratio of the rms value of the input signal to the rms sum of all other spectral components within the measurement bandwidth (10Hz to 20kHz). THD+N is expressed in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Instantaneous Dynamic Range

The S/(N+D) with a 1kHz, -60dB input signal, with 60dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components of the noise to insignificance. Units are in dB.

Interchannel Isolation

The amount of 1kHz signal present on the output of the grounded input channel with 1kHz, 0dB signal present on the other channel. Units are in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10Hz to 20kHz. Units in dB.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected input grounded. For the DAC's, the deviation of the output from zero with mid-scale input code. Units are in volts.

Semiconductor Corporation

CDB4225

CDB4225 Evaluation Board

Features

- CS4225 - Quad DAC, Stereo ADC
- CS8425 Digital Audio Transceiver
- Input Data from Either Audio Processor or via Optical IEC-958 Compatible Digital Audio Transceiver
- Output Data to Serial Interface Port or via Digital Audio Transceiver
- Serial Control Port for Software Control of both CS4225 and CS8425. Supports I^2C and SPI
- Board is Also Hardware Controllable

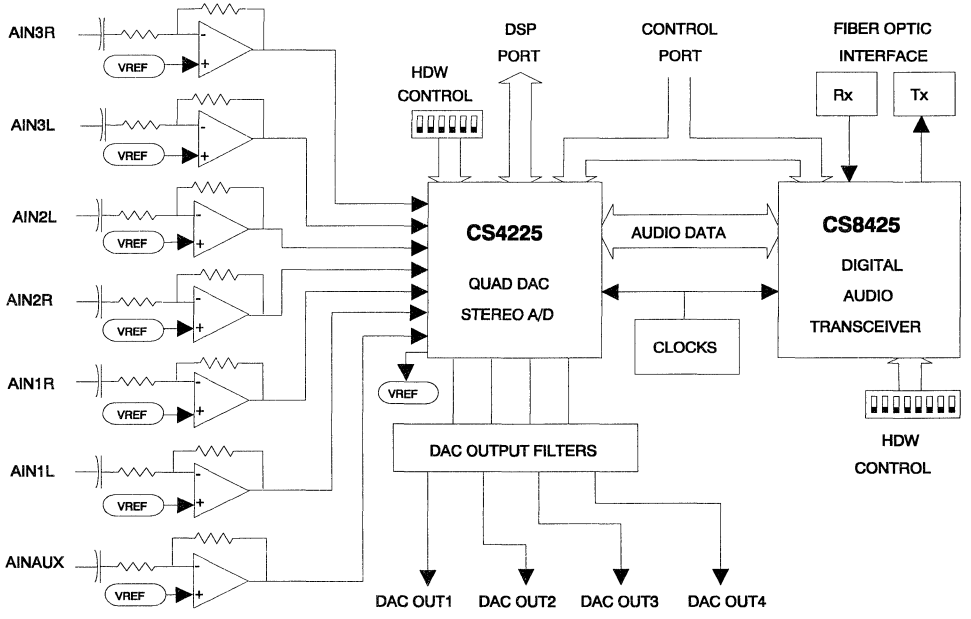
General Description

The CDB4225 is useful for evaluating the performance of both the CS4225 and the CS8425. Audio data can be input to and output from the CS4225 via a serial port which connects to an audio data processor. Alternatively, the CS8425 can serve as the audio data interface, supporting the "consumer" interface over fiber optics.

The board can be configured and controlled by either a peripheral serial control port, or by stand alone hardware interface. The peripheral control options are SPI and I^2C. PC software which supports the board's SPI interface is available, and can be used to set the internal control registers of the CS4225 and CS8425.

ORDERING INFORMATION
CDB4225

4



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

• Notes •

Semiconductor Corporation

CS4231

Parallel Interface, Multimedia Audio Codec

Features

- ADPCM Compression/Decompression
- Free Windows™ Software Drivers
- MPC Compatible Mixer
- Dual DMA Count Registers for Full Duplex Operation
- DMA Transfers with On-chip FIFOs.
- Timer for Audio/Visual Synchronization
- 16 mA Bus Drive Capability
- Digital 3.3/5V Operation
- Pin Compatible with CS4248/AD1848

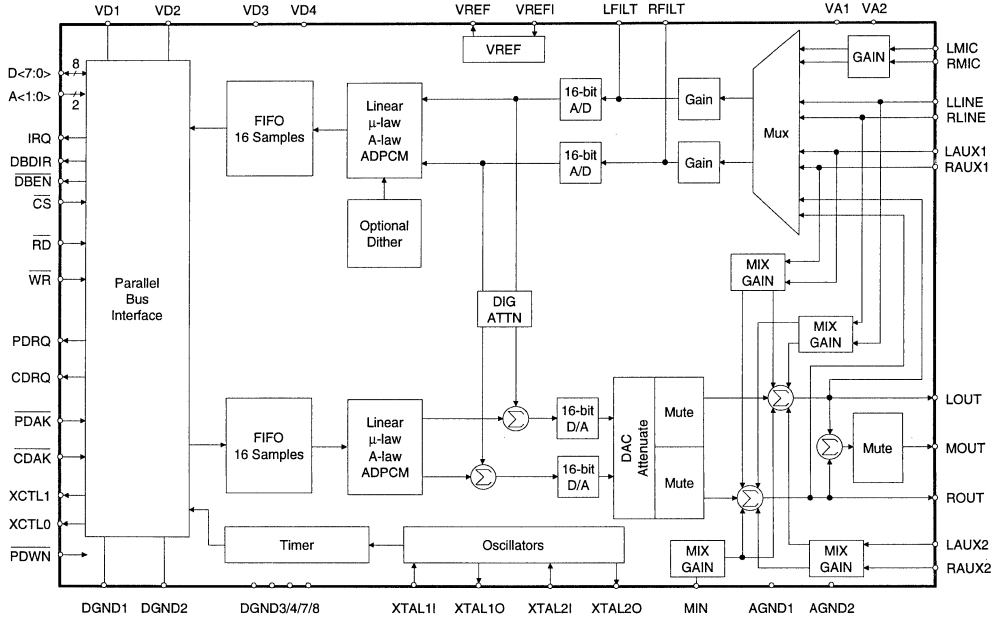
General Description

mwave The CS4231 is an Mwave™ audio codec.

The CS4231 provides 16-bit audio for computer multimedia systems. The CS4231 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data, plus analog mixing and programmable gain and attenuation are included to provide a complete audio subsystem. Free high-performance Windows software drivers are available that support all the CS4231 features including full duplex transfers. The CS4231 is a pin compatible upgrade to the CS4248 and AD1848 (PLCC Version).

ORDERING INFORMATION:

CS4231-KL	0 to 70°C	68-pin PLCC
CS4231-KQ	0 to 70°C	100-pin TQFP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine wave; Conversion Rate = 48 kHz; Measurement Bandwidth is 10 Hz to 20 kHz, 16-bit linear coding.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution	(Note 1)		16	-	-	Bits
ADC Differential Nonlinearity	(Note 1)		-	-	±0.5	LSB
Instantaneous Dynamic Range	Line Inputs (Note 2) Mic Inputs	IDR	80 72	85 77	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	0.02 0.025	0.003 0.01	- -	% %
Signal-to-Intermodulation Distortion			-	90	-	dB
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs Line-to-AUX1 Line-to-AUX2		- - - -	80 80 90 90	- - - -	dB dB dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5	-	dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain		-	10	100	LSB
Gain Error			-	-	5	%
Full Scale Input Voltage:	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2, MIN Inputs		0.266 2.66 2.66	0.29 2.9 2.9	0.31 3.1 3.1	V_{pp} V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 1)		20	-	-	kΩ
Input Capacitance	(Note 1)		-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, not production testing.
2. MGE = 1 and a 10µF capacitor on the VREF pin.

* Parameter definitions are given at the end of this data sheet.

ANALOG CHARACTERISTICS (Continued)

Parameter *			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0 dB); Unless Otherwise Specified.							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity		(Note 1)		-	-	±0.5	LSB
Dynamic Range	- Total - Instantaneous	All Outputs	TDR IDR	- 80	95 85	- -	dB dB
Total Harmonic Distortion		(Note 4)	THD	0.02	0.01	-	%
Signal-to-Intermodulation Distortion				-	85	-	dB
Interchannel Isolation	Line Out	(Note 4)		-	95	-	dB
Interchannel Gain Mismatch		Line Out		-	0.1	0.5	dB
Voltage Reference Output				2.0	2.15	2.3	V
Voltage Reference Output Current		(Note 3)		-	100	-	µA
DAC Programmable Attenuation Span				93	94.5	-	dB
DAC Attenuation Step Size		0 dB to -81 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC Offset Voltage				-	1	10	mV
Full Scale Output Voltage	OLB = 0 OLB = 1	(Notes 4, 5) OUT, MOUT		1.85 2.66	2.0 2.9	2.25 3.2	V_{pp} V_{pp}
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase		(Note 1)		-	-	1	Degree
External Load Impedance				10	-	-	kΩ
Mute Attenuation (0 dB)				80	-	-	dB
Total Out-of-Band Energy	(Note 1)	0.6×Fs to 3 MHz		-	-	-45	dB
Audible Out-of-Band Energy	(Fs = 8kHz)	0.6×Fs to 22 kHz		-	-	-60	dB
Power Supply							
Power Supply Current		Digital, Operating Analog, Operating Total Digital, Power Down Analog, Power Down		- - - - -	55 43 98 - -	65 60 120 1 1	mA mA mA mA mA
Power Supply Rejection	1kHz	(Note 1)		40	-	-	dB

Notes: 3. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.
4. 10 kΩ, 100 pF load.
5. All mixer and output gain tables assume the output level bit, OLB, in indirect register 16 (I16) is set, wherein the input and output full scale values are equal. When OLB=0, the output value is 3 dB below the input value, given no gain or attenuation.

AUXILIARY INPUT MIXERS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine Wave)

Parameter		Symbol	Min	Typ	Max	Units
Mixer Gain Range Span	LINE, AUX1, AUX2 (Note 6) MIN		45 42	46.5 45	- -	dB dB
Step Size	LINE, AUX1, AUX2 MIN		1.3 2.3	1.5 3.0	1.7 3.4	dB dB

Note: 6. All mixer gain values assume OLB=1. If OLB=0, the analog output will be 3 dB below listed settings.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1-VD4 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current Per Pin	(Except Supply Pins)		-10	10	mA
Output Current Per Pin	(Except Supply Pins)		-50	50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage			-0.3	VD+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital Analog	VD1-VD4 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	25	70	°C

DIGITAL FILTER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Passband			0	-	0.40×Fs	Hz
Frequency Response			-0.5	-	+ 0.2	dB
Passband Ripple	(0-0.4×Fs)		-	-	±0.1	dB
Transition Band			0.40×Fs	-	0.60×Fs	Hz
Stop Band			0.60×Fs	-	-	Hz
Stop Band Rejection			74	-	-	dB
Group Delay			-	-	30/Fs	s
Group Delay Variation vs. Frequency	ADCs DACs		- -	- -	0.0 0.1/Fs	µs µs

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DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = 5V; AGND1, AGND2, DGND1-DGND4, DGND7, DGND8 = 0V.)

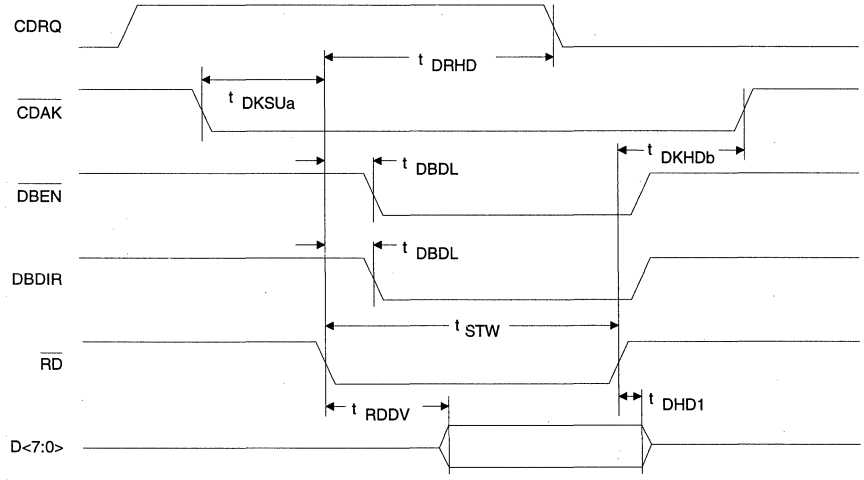
Parameter			Symbol	Min	Max	Units
High-level Input Voltage		Digital Inputs XTAL1I/XTAL2I, $\overline{PDWN}$	V_{IH}	2.0 VD-1.0	VD+ 0.3 VD+ 0.3	V V
Low-level Input Voltage			V_{IL}	-0.3	0.8	V
High-level Output Voltage:	D<7:0> All Others	I_O = -16.0 mA I_O = -1.0 mA	V_{OH}	2.4 2.4	VD VD	V V
Low-level Output Voltage:	D<7:0> All Others	I_O = 16.0 mA I_O = 4.0 mA	V_{OL}	- -	0.4 0.4	V V
Input Leakage Current		(Digital Inputs)	-	-10	10	µA
Output Leakage Current		(High-Z Digital Outputs)	-	-10	10	µA

TIMING PARAMETERS

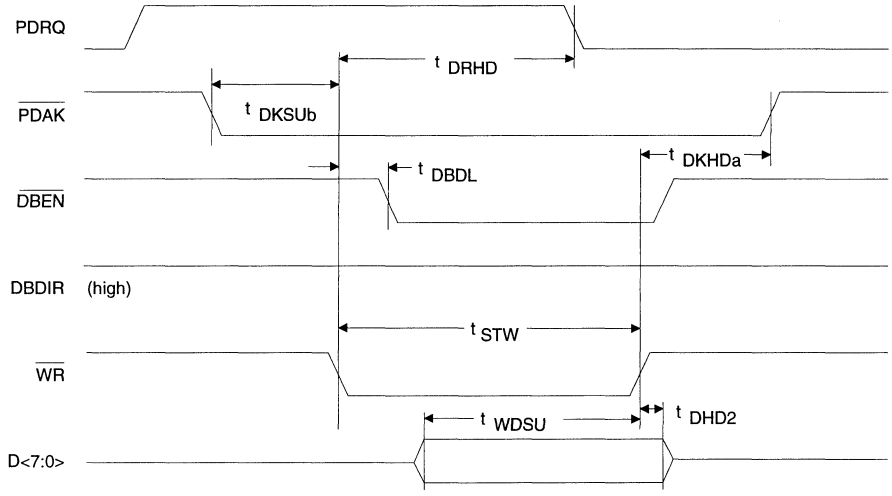
Parameter	Description		Min	Max	Units
t_{STW}	$\overline{WR}$ or $\overline{RD}$ strobe width		90	-	ns
t_{WDSU}	Data valid to $\overline{WR}$ rising edge	(write cycle)	22	-	ns
t_{RDDV}	$\overline{RD}$ falling edge to data valid	(read cycle)	-	60	ns
t_{CSSU}	$\overline{CS}$ setup to $\overline{WR}$ or $\overline{RD}$ falling edge		10	-	ns
t_{CSHD}	$\overline{CS}$ hold from $\overline{WR}$ or $\overline{RD}$ rising edge		0	-	ns
t_{ADSU}	ADDR <> setup to $\overline{RD}$ or $\overline{WR}$ falling edge		22	-	ns
t_{ADHD}	ADDR <> hold from $\overline{WR}$ or $\overline{RD}$ rising edge		10	-	ns

TIMING PARAMETERS (continued)

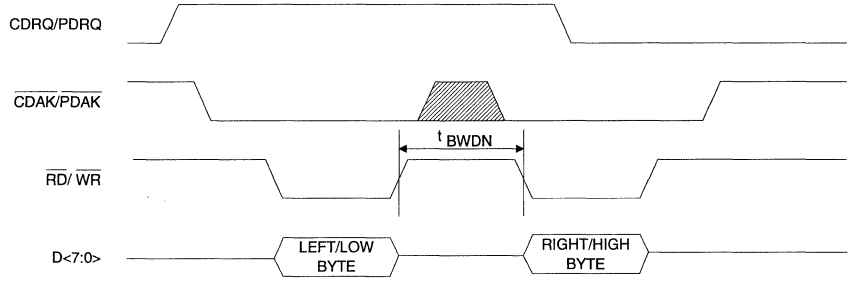
Parameter	Description	Min	Max	Units
t_{SUDK1}	$\overline{DAK}$ inactive to $\overline{WR}$ or $\overline{RD}$ falling edge (DMA cycle completion immediately followed by a PIO cycle)	60	-	ns
t_{SUDK2}	$\overline{DAK}$ active from $\overline{WR}$ or $\overline{RD}$ rising edge (PIO cycle completion immediately followed by DMA cycle)	0	-	ns
t_{DKSUa} t_{DKSUb}	$\overline{DAK}$ setup to $\overline{RD}$ falling edge (DMA cycles) $\overline{DAK}$ setup to $\overline{WR}$ falling edge	25 25	- -	ns ns
t_{DHD2}	Data hold from $\overline{WR}$ rising edge	15	-	ns
t_{DRHD}	DRQ hold from $\overline{WR}$ or $\overline{RD}$ falling edge (assumes no more DMA cycles needed)	0	25	ns
t_{BWDN}	Time between rising edge of $\overline{WR}$ or $\overline{RD}$ to next falling edge of $\overline{WR}$ or $\overline{RD}$	80	-	ns
t_{DHD1}	Data hold from $\overline{RD}$ rising edge	0	20	ns
t_{DKHDa} t_{DKHDb}	$\overline{DAK}$ hold from $\overline{WR}$ rising edge $\overline{DAK}$ hold from $\overline{RD}$ rising edge	25 25	- -	ns ns
t_{DBDL}	$\overline{DBEN}$ or $\overline{DBDIR}$ active from $\overline{WR}$ or $\overline{RD}$ falling edge		40	ns
t_{PDWN}	$\overline{PDWN}$ pulse width low	200	-	ns



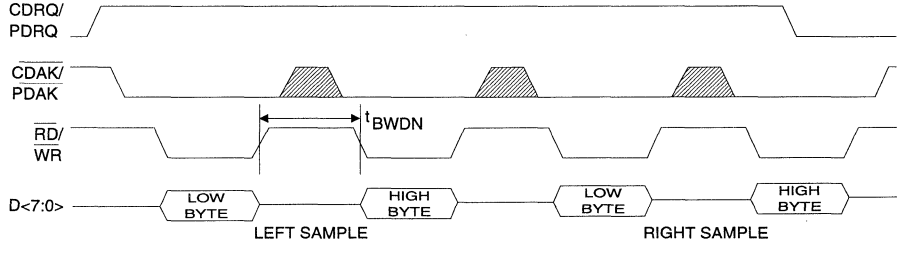
8-Bit Mono DMA Read/Capture Cycle



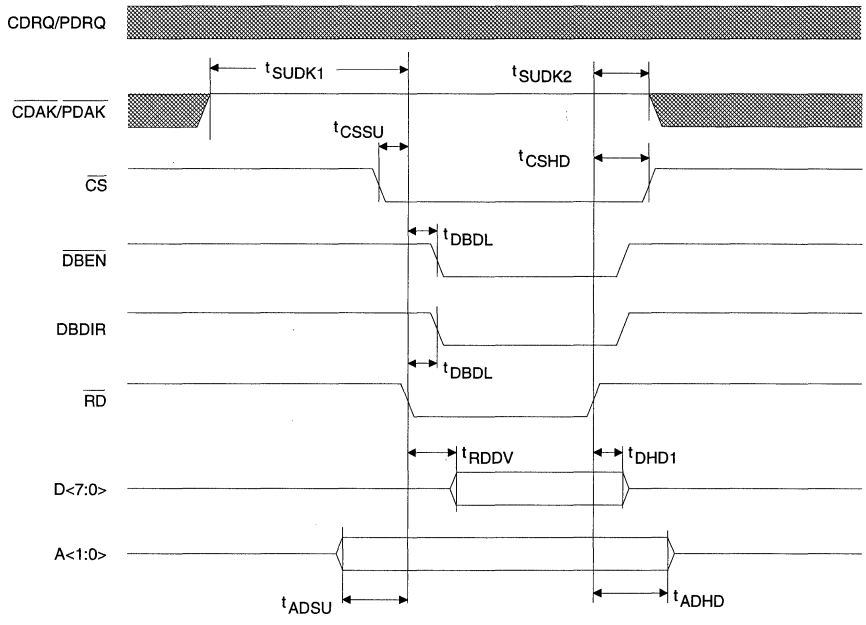
8-Bit Mono DMA Write/Playback Cycle



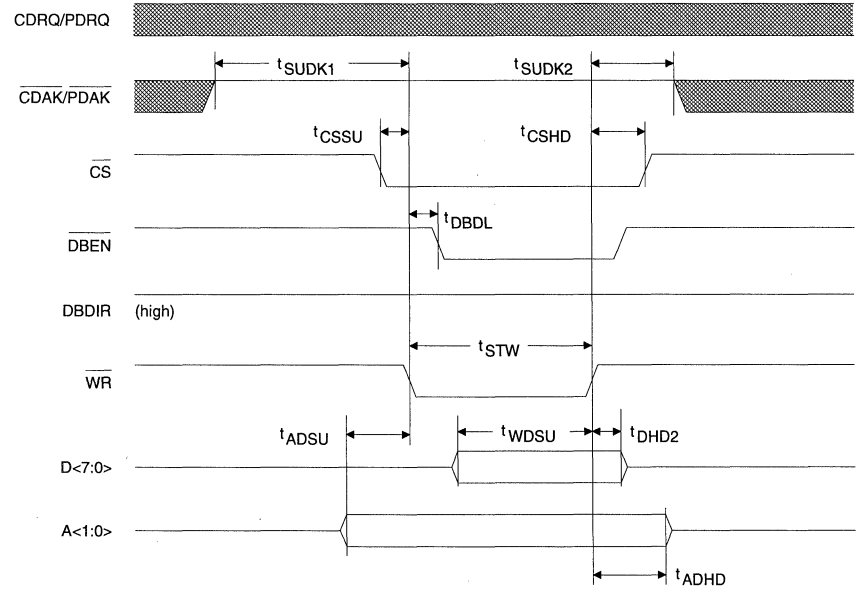
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo DMA Cycle



I/O Read Cycle



I/O Write Cycle

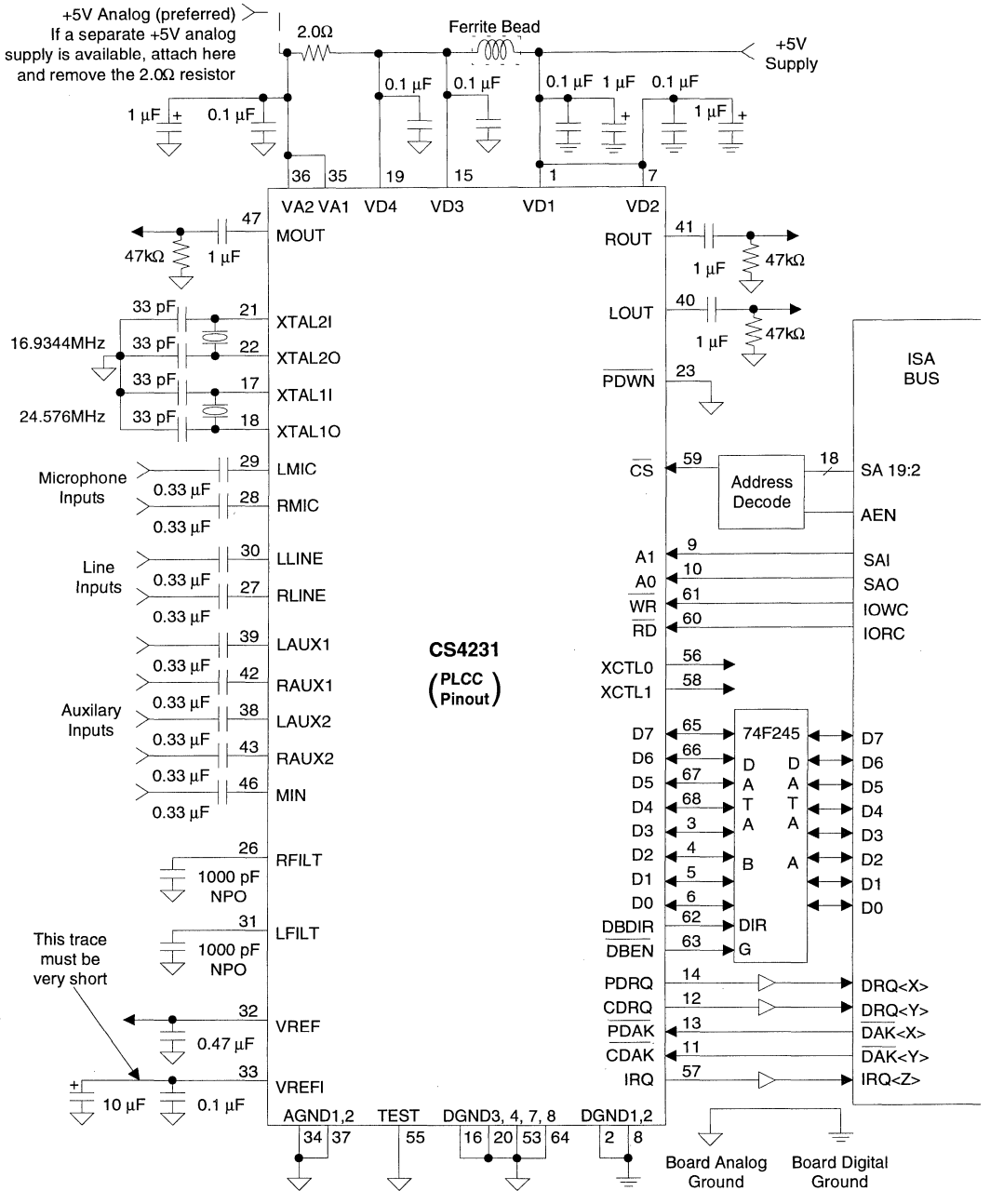


Figure 1. Recommended Connection Diagram
(See Figures 16 & 17 for Layout Recommendations)

GENERAL DESCRIPTION

The CS4231 is a monolithic integrated circuit that provides audio in personal computers or other parallel interface environments. The functions include stereo Analog-to-Digital and Digital-to-Analog converters (ADCs and DACs), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, optional A-Law / μ-Law coding, simultaneous capture and playback (at the same sample rates) and a parallel bus interface. Five analog inputs are provided and three can be multiplexed to the ADC. The line input, two auxiliary inputs and a mono input can be mixed with the output of the DAC with full volume control. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded, 4-bit ADPCM compressed, and 16-bit big Endian. The CS4231 is packaged in a 68-pin PLCC or a 100-pin TQFP.

Enhanced Functions (MODE 2)

The CS4231's initial state is labeled MODE 1 and forces the CS4231 to appear as a CS4248. Enhanced functionality is provided by a second mode on the CS4231. To switch from MODE 1 to MODE 2, the MODE2 bit should be set to one in the MODE and ID register (I12). When MODE 2 is selected, the bit IA4 in the Index Address register (R0) will be decoded as a valid index pointer providing 16 additional registers and increased functionality over the CS4248.

To reverse the procedure, clear the MODE2 bit and the CS4231 will resume operation in MODE 1. Since previous code should write a zero to bit IA4 of the Index Address register (R0), the CS4231 is backwards compatible with the CS4248 and the AD1848.

Mixer Attenuation Control on Line Input

The CS4231 adds mixer attenuation control for the LINE inputs which are then summed into the output mixer. This fourth input to the mixer completes the recommended mixer configuration for MPC Level-2 compliance. The LINE mix register provides 32 volume adjustments in 1.5 dB steps. In addition, there is a one bit mute control.

The additional MODE 2 functions are:

1. Full-Duplex DMA support
2. A programmable timer
3. Mono output with mute control
4. Mono input with mixer volume control
5. ADPCM and Big Endian audio data formats
6. Independent selection of capture and playback audio data formats

ANALOG HARDWARE DESCRIPTION

The analog hardware consist of an MPC Level 2-compatible mixer (four stereo mix sources), three line-level stereo inputs, a stereo microphone input, a mono input, a mono output, and a stereo line output. This section describes the analog hardware needed to interface with these pins.

Analog Inputs

The analog inputs consist of four stereo analog inputs, and one mono input. As shown on this data sheet cover, the input to the ADCs comes from a multiplexer that selects between two analog line-level inputs (LINE, AUX1), a microphone level input (MIC), and the output from the MPC-compatible mixer. The LINE and AUX1 lines also feed the MPC mixer and include individual volume controls. Unused analog inputs should be connected together and then connected through a capacitor to analog ground.

Line-Level Inputs plus MPC Mixer

The analog input interface is designed to accommodate four stereo inputs and one mono input.

Three of these sources are multiplexed to the ADC. These inputs are: a stereo line-level input (LINE), a stereo microphone input (MIC), and a stereo auxiliary line-level input (AUX1). The LINE and AUX1 inputs have a separate path, with volume control, to the output analog mixer which has the additional inputs of a stereo AUX2 channel, a mono input channel, and the output of the DACs. All audio inputs should be capacitively coupled to the CS4231.

Since some analog inputs can be as large as 2 V_{RMS}, the circuit shown in Figure 2 can be used to attenuate the analog input to 1 V_{RMS} which is the maximum voltage allowed for the line-level inputs on the CS4231.

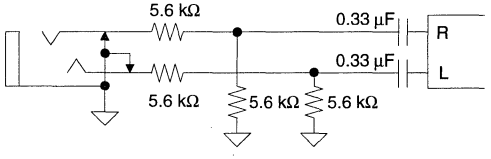


Figure 2. Line Inputs

Microphone Level Inputs

The microphone level inputs, LMIC and RMIC, include a selectable + 20dB gain stage for interfacing to an external microphone. The 20dB gain block can be turned off to provide another stereo line-level input. Figure 3 illustrates a single-ended microphone input buffer circuit that will support lower gain mics.

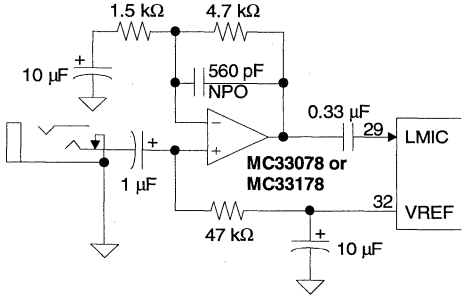


Figure 3. Left or Mono Microphone Input

Mono Input with Attenuation and Mute

The mono input, MIN, is useful for mixing the output of the "beeper" (timer chip), provided in all PCs, with the rest of the audio signals. The attenuation control allows 16 levels in -3dB steps. In addition, a mute control is provided. The attenuator is a single channel block with the resulting signal sent to the output mixer where it is mixed with the left and right outputs. Figure 4 illustrates a typical input circuit for the Mono In. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes. At power-up, the MIN line is unmuted (as is the mono out line) allowing the initial beeps heard, when the computer is initializing, to pass through.

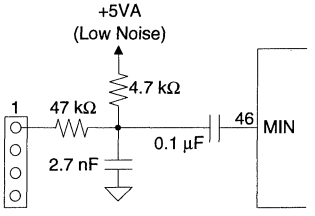


Figure 4. Mono Input

Analog Outputs

The analog output section of the CS4231 provides a stereo line-level output. The other output types (headphone and speaker) can be implemented with external circuitry. LOUT and ROUT outputs should be capacitively coupled to external circuitry. Figure 1 shows the simplicity of the analog output interface.

Mono Output with Mute Control

The mono output, MOUT, is a sum of the left and right output channels, attenuated by 6dB to prevent clipping at full scale. The mono out channel can be used to drive the PC-internal mono speaker using an appropriate drive circuit. This approach allows the traditional PC-sounds

to be integrated with the rest of the audio system. Figure 5 illustrates a typical speaker driver circuit. The mute control is independent of the line outputs allowing the mono channel to mute the speaker without muting the line outputs. The power-up default has MIN and MOUT enabled to provide a pass-through for the beeps heard at power-up.

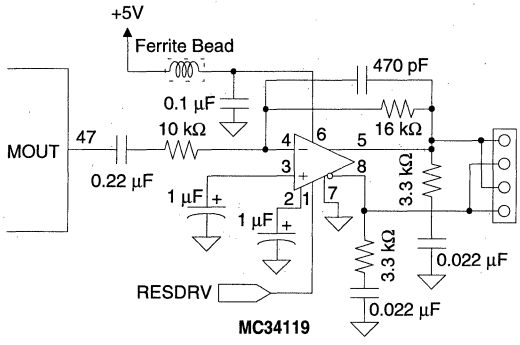


Figure 5. Mono Output

Miscellaneous Analog Signals

The LFILT and RFILT pins must have a 1000 pF NPO capacitor to analog ground. These capacitors, along with an internal resistor, provide a single-pole low-pass filter used at the inputs to the ADCs. By placing these filters at the input to the ADCs, low-pass filters at each analog input pin is avoided.

The VREFI pin is used to lower the noise of the internal voltage reference. A 10µF and 0.1µF capacitor to analog ground should be connected with a short wide trace to this pin. No other connection should be made, as any coupling onto this pin will degrade the analog performance of the codec. Likewise, digital signals should be kept away from VREFI for similar reasons.

The VREF pin is typically 2.1 V and provides a common mode signal for single-supply external circuits. VREF only supports DC loads and should be buffered if AC loading is needed. For typical use, a 0.47 µF capacitor should be connected to VREF. High-gain microphone circuits can be improved by increasing the capacitance to 10 µF.

DIGITAL HARDWARE DESCRIPTION

The digital hardware consist of the data bus, address bus, and control signals needed for the parallel bus, as well as an interrupt and DMA signals.

Parallel Data Interface

The 8-bit parallel port of the CS4231 provides an interface which is compatible with most computer peripheral busses. This parallel interface is designed to operate on the Industry Standard Architecture (ISA) bus, but the CS4231 will easily interface with other buses such as EISA and microchannel. Two types of accesses can occur via the parallel interface: Programmed I/O (PIO) access, and DMA access.

There is no provision for the CS4231 to "hold off" or extend a cycle occurring on the parallel interface. Therefore, the internal architecture of the CS4231 accepts asynchronous parallel bus cycles without interfering with the flow of data to or from the ADC and DAC sections.

FIFOs

The CS4231 contains 16-sample FIFOs in both the playback and capture paths. The FIFOs are transparent and have no programming associated with them.

When playback is enabled, the playback FIFO continually requests data until the FIFO is full, and then makes requests as positions inside the FIFO are emptied, thereby keeping the playback FIFO as full as possible. Thus when the system cannot respond within a sample period, the FIFO

is emptied, avoiding a momentary loss of audio data. If the FIFO runs out of data, the last valid sample can be continuously output to the DACs (if DACZ in I16 is set) which will eliminate pops from occurring.

When capture is enabled, the capture FIFO tries to continually stay empty by making requests every sample period. Thus when the system cannot respond within a sample period, the capture FIFO starts filling thereby avoiding a loss of data in the audio data stream.

High Current Data Bus Drivers

The CS4231 provides 16 mA drivers eliminating the need for off chip drivers in many cases. If a full 24 mA drive is required, the appropriate direction and driver select lines are provided. The current drivers are provided for the data bus, DMA request line, and the interrupt request line.

PIO Registers Interface

The first type of parallel bus access is programmed I/O (PIO) to the four control registers. The control registers allow access to status, audio data, and all indirect registers via the index registers. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the read and write cycles respectively. The PIO register cycle is defined by the assertion of the CS4231 $\overline{CS}$ signal while the DMA acknowledge signals, $\overline{CDAK}$ and $\overline{PDAK}$, are inactive. For read cycles, the CS4231 will drive data on the DATA lines while the host asserts the $\overline{RD}$ strobe. Write cycles require the host to assert data on the DATA lines and strobe the $\overline{WR}$ signal. The CS4231 will latch data into the PIO register on the rising edge of the $\overline{WR}$ strobe. The CS4231 $\overline{CS}$ signal should remain active until after completion of the read or write cycle. I/O cycles are the only type of cycle which can access the internal control and status registers.

The audio data interface typically uses DMA request/grant pins to transfer the digital audio data between the CS4231 and the bus. The CS4231 is responsible for asserting a request signal whenever the CS4231's internal buffers need updating. The logic interfaced with the CS4231 responds with an acknowledge signal and strobes data to and from the CS4231, 8 bits at a time. The CS4231 keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Notice that different audio data types will require a different number of 8-bit transfers.

DMA Interface

The second type of parallel bus cycle on the CS4231 is a DMA transfer. DMA cycles are distinguished from PIO register cycles by the assertion by the CS4231 of a CDRQ (or PDRQ) followed by an acknowledgment by the host by the assertion of $\overline{CDAK}$ (or $\overline{PDAK}$). While the acknowledgment is received from the host, the CS4231 assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines and the $\overline{CS}$ line.

The CS4231 may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a DMA cycle occurs to the CS4231. Once the falling edge of the final $\overline{WR}$ or $\overline{RD}$ strobe of a full sample of a DMA cycle occurs, the DMA request signal is negated immediately. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9), depending on the DMA that is in progress (playback, capture, or both). Termination of DMA transfers may only happen between sample transfers on the bus. If PDRQ and/or CDRQ goes active while resetting PEN and/or CEN, the request must be acknowledged ($\overline{PDAK}$ and/or $\overline{CDAK}$) and a final sample transfer completed. The CS4231 supports up to two DMA channels.

Dual DMA Channel Mode

In dual DMA channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In this mode, capture and playback are enabled and set for DMA transfers. In addition, the dual DMA mode must be set (SDC = 0). The Playback- and Capture-Enables (PEN, CEN, I9) can be changed without a Mode Change Enable (MCE, R0). This allows for proper full duplex control where applications are independently using playback and capture.

Single DMA Channel (SDC) Mode

When two DMA channels are not available, the SDC mode forces all DMA transfers (capture or playback) to occur on a single DMA channel (playback channel). The trade-off is that the CS4231 will no longer be able to perform simultaneous DMA capture and playback.

To enable the SDC mode, set the SDC bit in the Interface Configuration register (I9). With the SDC bit asserted, the internal workings of the CS4231 remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation. However, the capture audio channel is now diverted to the playback channel. This means that the capture DMA request occurs on the PDRQ pin and the $\overline{\text{PDAK}}$ pin is used to acknowledge the capture request. (In MODE 2, the capture data format is always set in register I28.) Note, simultaneous capture and playback cannot occur in SDC mode. If both playback and capture are enabled, the default will be playback.

In SDC mode, the CDRQ pin is logic low (inactive). The $\overline{\text{CDAK}}$ pin is ignored by the CS4231. SDC does not have any affect when using PIO accesses.

Miscellaneous Signals

The power supply providing analog power should be as clean as possible to minimize coupling into the analog section and degrading analog performance. The VD1 and VD2 pins are isolated from the rest of the digital power pins and provide digital power for the asynchronous parallel bus. These two pins can be connected directly to the digital power supply. VD3 and VD4 digital power supply pins provide power to the internal digital section of the codec and should be optimally quieter than VD1 and VD2. This can be achieved by using a ferrite bead as shown in the typical connection diagram in Figure 1. Grounding is covered in the *Grounding and Layout* section.

An interrupt pin, IRQ, is provided to allow for host notification by the CS4231. Since the interrupt is mainly a software function, it is described in more detail under the software section.

Crystals / Clocks

Four pins have been allocated to allow the interfacing of two crystal oscillators to the CS4231: XTAL1I, XTAL1O, XTAL2I, XTAL2O. The crystals should be designed as fundamental mode, parallel resonant, with a load capacitor of between 10 and 20 pF. The capacitors shown in Figure 1, connected to each of the crystal pins, should be twice the load capacitance specified to the crystal manufacturer. The XTAL1 oscillator is designed with slightly more gain to handle higher frequencies, but any crystal with the above specifications should suffice. The standard crystals for audio are:

XTAL1: 24.576 MHz
Fundamental Mode
Parallel Resonant, C_L = 20 pF

XTAL2: 16.9344 MHz
Fundamental Mode
Parallel Resonant, C_L = 20 pF

These crystal frequencies support the standard sample frequencies listed in Table 7.

External CMOS clocks may be connected the crystal inputs (XTAL1I, XTAL2I) in lieu of the crystals. When using external CMOS clocks, the XTAL out pins should be left floating. Extreme care should be used when laying out a board using external clocks since coupling between clocks can degrade analog performance.

Power Down - $\overline{PDWN}$

The $\overline{PDWN}$ signal places the CS4231 into maximum power conservation mode. When $\overline{PDWN}$ goes low, any reads of the codec's parallel interface return 80 hex, all analog outputs are muted, and the voltage reference then slowly decays to ground. The $\overline{PDWN}$ signal should be held low while power is applied to the codec. Once the power supplies have settled, $\overline{PDWN}$ should be brought high which starts an initialization procedure and causes a full calibration cycle to occur. While the codec is initializing, any reads from the parallel interface will return 80 hex and writes will be ignored. When initialization is completed, the registers will contain their reset value as stated in the register section of the data sheet.

$\overline{DBEN}$/DBDIR

If needed, the $\overline{DBEN}$ and DBDIR pins can control an external data buffer to the CS4231. The CS4231 contains 16 mA bus drivers so the external data buffer is only needed when driving a full 24 mA bus. $\overline{DBEN}$ enables the external drivers and DBDIR controls the direction of the data flow. Both signals are normally high, where DBDIR high points the transceiver towards the codec and low points the transceiver towards the data bus. See Figure 1 for a typical connection diagram.

SOFTWARE DESCRIPTION

The CS4231 must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register (I9) or the Data Format registers (I8, I28) are allowed. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes to these bits. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

4

Procedures

Power-Down and Initialization

To put the CS4231 into a power-down mode, the $\overline{PDWN}$ pin is pulled low. In this state the host interface reads 80h indicating that it is unable to respond and all analog circuits are turned off.

To let the CS4231 go through its reset initialization the $\overline{PDWN}$ pin should be set high. This rising edge starts the initialization process in which a full calibration occurs. While the CS4231 is initializing, 80 hex is returned from all reads by the host computer. All writes during initialization of the CS4231 will be ignored. At the end of the initialization, all registers are set to known reset values as documented in the register definition section.

Auto Calibration

The CS4231 has the ability to calibrate the ADCs and DACs. Auto-calibration occurs whenever the CS4231 returns from Mode Change Enable (MCE) AND the ACAL bit in the Interface Configuration register (I9) has been set.

The completion of calibration can be determined by polling the Auto-Calibrate In-Progress bit in the Error Status and Initialization register (ACI, I11). This bit will be high while the calibration is in progress and low once completed. The auto-calibration sequence will take at least 168

sample periods. Transfers enabled during calibrate will not begin until the calibration cycle has completed.

The auto-calibrate procedure is as follows:

1) Place the CS4231 in Mode Change Enable using the MCE bit of the Index Address register (R0).
2) Set the ACAL bit in the Interface Configuration register (I9).
3) Return from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).
4) Wait until 80h NOT returned
5) Wait until ACI (I11) cleared to proceed

Changing Sampling Rate

The internal states of the CS4231 are synchronized by the selected sampling frequency defined in the Data Format registers (I8, I28). The changing of either the clock source or the clock frequency divide requires a special sequence for proper CS4231 operation:

1) Place the CS4231 in Mode Change Enable using the MCE bit of the Index Address register (R0).
2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock Source Select (CSL) bits of the Fs & Playback Data Format register (I8) to the desired value. (The data format may also be changed.)
3) The CS4231 resynchronizes its internal states to the new clock. During this time the CS4231 will be unable to respond at its parallel interface. Writes to the CS4231 will not be recognized and reads will always return the value 80 hex.
4) The host now polls the CS4231's Index Address register (R0) until the value 80 hex is no longer returned.
5) Once the CS4231 is no longer responding to reads with a value of 80 hex, normal operation can resume and the CS4231 can be removed from MCE.
The CSL and CFS bits cannot be changed unless the MCE bit has been set. Attempts to change the Data Format registers (I8, I28) or Interface Configuration register (I9, except CEN and PEN) without MCE set, will not be recognized.

Audio Data Formats

In MODE 1 operation, all data formats of the CS4231 are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The sample frequency is always selected in the Fs and Playback Data Format register (I8). In MODE 1 the same register, I8, determines the audio data format for both playback and capture; however, in MODE 2, I8 only selects the playback data format and the capture data format is independently selectable in the Capture Data Format register (I28).

The CS4231 always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size.

There are four data formats supported by the CS4231 during MODE 1 operation: 16-bit signed (little endian), 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law. See Figures 6 through 9.

Additional data formats are supported in MODE 2 operation: 4-bit ADPCM, and 16-bit

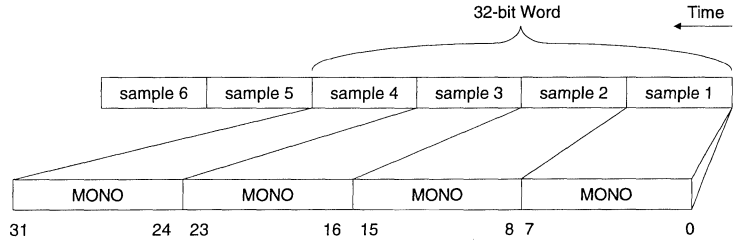


Figure 6. 8-bit Mono, Unsigned Audio Data

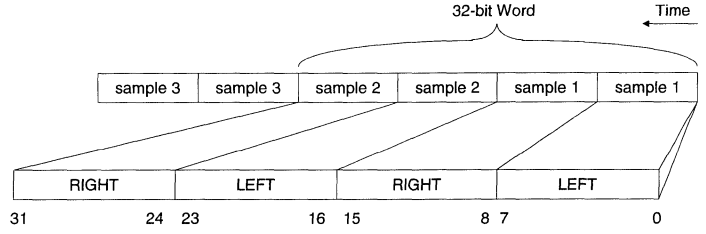


Figure 7. 8-bit Stereo, Unsigned Audio Data

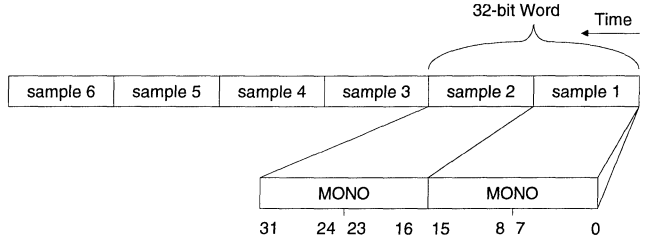


Figure 8. 16-bit Mono, Signed Little Endian Audio Data

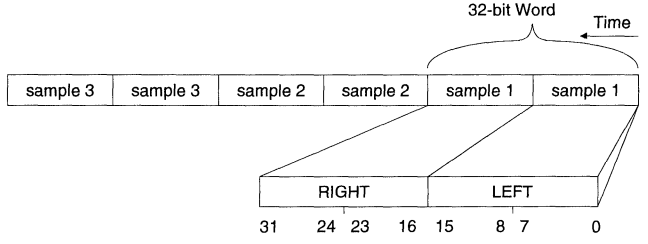


Figure 9. 16-bit Stereo, Signed Little Endian Audio Data

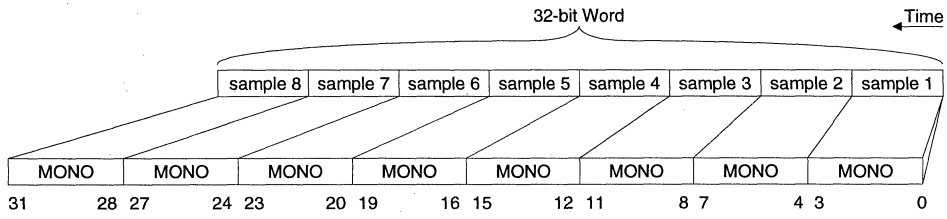


Figure 10. 4-bit Mono, ADPCM Audio Data

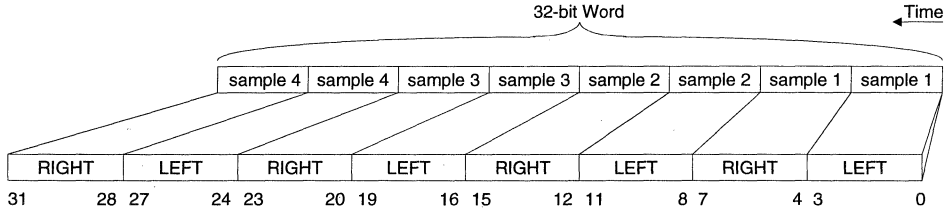


Figure 11. 4-bit Stereo, ADPCM Audio Data

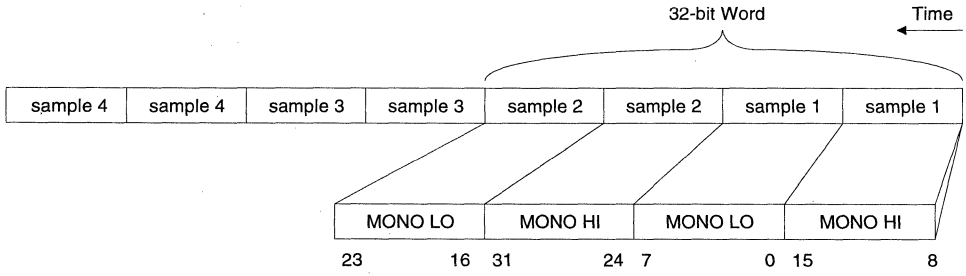


Figure 12. 16-bit Mono, Signed Big Endian Audio Data

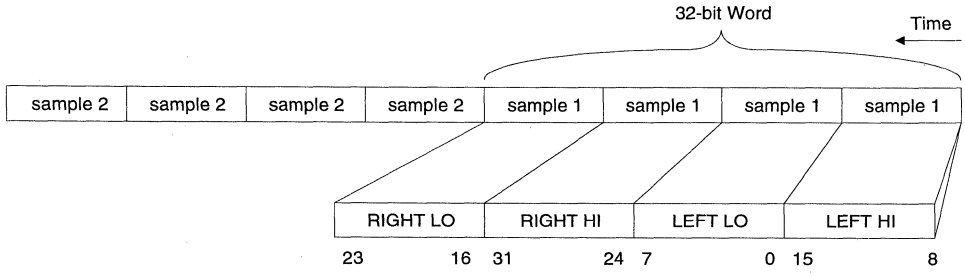


Figure 13. 16-bit Stereo, Signed Big Endian Audio Data

signed big endian. See Figures 10 through 13. With the addition of the big endian and ADPCM audio data formats, the CS4231 is compliant with the IMA recommendations for digital audio data formats (and sample frequencies).

16-bit Signed

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent minimum analog amplitude while 32767 (7FFFh) represents maximum analog amplitude.

8-bit Unsigned

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent minimum analog amplitude while 255 (FFh) represents maximum analog amplitude. The 16-bit signed and 8-bit unsigned transfer functions are shown in Figure 14.

8-bit Companded

The 8-bit companded formats (A-Law and μ-Law) come from the telephone industry. μ-Law is the standard for the United States/Japan while A-Law is used in Europe. Companded audio allows either 64 dB or 72 dB of dynamic range using only 8-bits per sample. This is accomplished using a non-linear companding transfer function which assigns more digitalization codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The μ-Law and A-Law formats of the CS4231 conform to the CCITT G.711 specifications. Figure 15 illustrates the transfer function for both A- and μ-Law. Please refer to the standards mentioned above for an exact definition.

ADPCM Compression/Decompression

In MODE 2, the CS4231 also contains Adaptive Differential Pulse Code Modulation (ADPCM) for improved performance and compression ratios over μ-Law or A-Law. The ADPCM format is compliant with the IMA standard and provides a 4-to-1 compression ratio (i.e. 4 bits are saved for each 16-bit sample captured). For more information on the specifics of the format, contact the IMA at (202) 408-1000. See Figures 10 and 11.

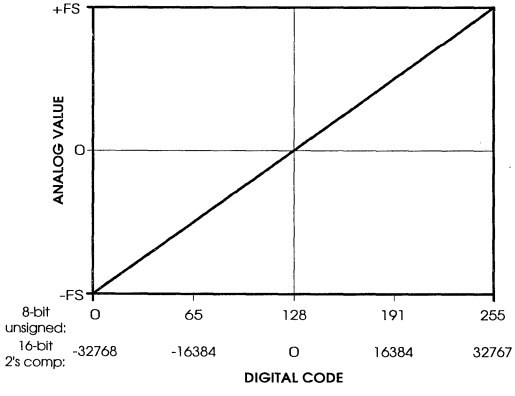


Figure 14. Linear Transfer Functions

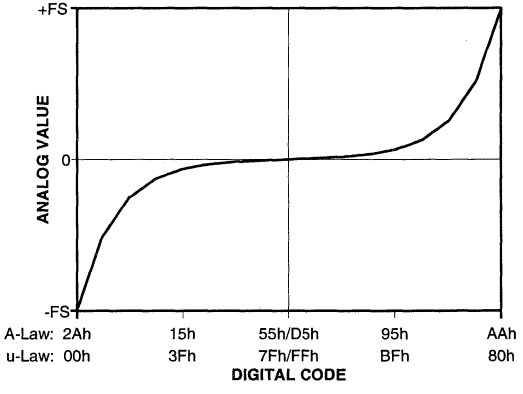


Figure 15. Companded Transfer Functions

When using the ADPCM data format, the DMA Base register count is not on a per sample basis.

DMA Registers

The DMA registers allow easier integration of the CS4231 in ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base registers provide this service.

The act of writing a value to the Upper Base register cause both Base registers to load the Current Count register. DMA transfers are enabled by setting the PEN/CEN bit while PPIO/CPIO is clear. (PPIO/CPIO can only be changed while the MCE bit is set.) Once transfers are enabled, each sample that is transferred by a DMA cycle will decrement the Current Count register (with the exception of the ADPCM format) until zero is reached. The next sample after zero generates an interrupt and reloads the Current Count registers with the values in the Base registers.

For all data formats except ADPCM, the DMA Base registers must be loaded with the number of samples, minus one, to be transferred between "DMA Interrupts". Stereo data contains twice as many samples as mono data; however, 8-bit data and 16-bit data contain the same number of samples. Symbolically:

DMA Base register$_{16}$ = N_S - 1

Where N_S is the number of samples transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

For the ADPCM data format, the contents of the DMA Base registers is calculated differently from any other data format. The Base registers must be loaded with the number of BYTES to be transferred between "DMA interrupts", divided by four, minus one. The same number is used whether the data format is stereo or mono ADPCM. Symbolically:

DMA Base register$_{16}$ = N_b/4 - 1

Where N_b is the number of BYTES transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

Playback DMA Registers

The playback DMA registers (I14/15) are used for sending playback data to the DACs in MODE 2. In MODE 1, these registers (I14/15) are used for both playback and capture; therefore, full-duplex DMA operation is not possible.

When the playback Current Count register rolls under, the Playback Interrupt bit, PI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Playback Interrupt bit, PI (I24).

Capture DMA Registers

The Capture DMA Base registers (I30/31) provide a second pair of Base registers that allow full-duplex DMA operation. With full-duplex operation capture and playback can occur simultaneously. These registers are provided in MODE 2 operation only.

When the capture Current Count register rolls under, the Capture Interrupt bit, CI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Capture Interrupt bit, CI (I24).

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register (I13). This loop-

back routes the digital data from the ADCs to the DACs. This loopback can be digitally attenuated via additional bits in the Loopback Control register (I13). Loopback is then summed with DAC data supplied at the digital bus interface. When loopback is enabled, it will "freerun" synchronous with the sample rate. The digital loopback is shown in the CS4231 Block Diagram on the front cover. This loopback can be used to mix the incoming microphone data with data from the DACs. Since the CS4231 allows selection of different data formats between capture and playback, if the capture channel is set to mono and the playback channel set to stereo, the mono input (mic) data will be mixed into both channels of the output mixer.

If the sum of the loopback and bus data are greater than full scale, CS4231 will send the appropriate full scale value to the DACs (clipping).

Timer Registers

The Timer registers are provided for synchronization, watch dog and other functions where a high resolution time reference is required. This counter is 16 bits and the exact time base, listed in the register description, is determined by the crystal selected.

The Timer register is set by loading the high and low registers to the appropriate values and setting the Timer Enable bit, TE, in the Alternate Feature Enable register (I16). This value will be loaded into an internal Current Count register and will decrement at approximately a 10 µsec rate. When the value of the Current Count register reaches zero, an interrupt will be posted to the host and the Timer Interrupt bit, TI, is set in the Alternate Feature Status register (I24). On the next timer clock the value of the Timer registers will be loaded into the internal Current Count register and the process will begin again. The interrupt is cleared by any write to the Status register (R2) or by writing a "0" to the Timer Interrupt bit, TI, in the Alternate Feature Status register (I24).

Interrupts

The INT bit of the Status register (R2) always reflects the status of the CS4231 internal interrupt state. A roll-over from any Current Count register (DMA playback, DMA capture, or Timer) sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register (R2), or by clearing the appropriate bit or bits (PI, CI, TI) in the Alternate Feature Status register (I24). The IRQ pin of the CS4231 may or may not go active on an interrupt event.

The Interrupt Enable (IEN) bit in the Pin Control register (I10) determines whether the interrupt pin responds to the interrupt event in the CS4231. When the IEN bit is low, the interrupt is masked and the IRQ pin of the CS4231 is forced low. However, the INT bit in the Status register (R2) always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the CS4231 in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the CS4231.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output (assuming DACZ = 0) to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

CS4231 REGISTER MAPPING

	Addr.	Register Name
R0	0	Index Address register
R1	1	Indexed Data register
R2	2	Status register
R3	3	PIO Data register

Table 1. Direct Registers

The two address pins of the CS4231 allow access to four 8-bit registers. Two of these registers provide indirect accessing to more CS4231 registers via an index register. The other two registers provide status information and allow audio data to be transferred to and from the CS4231 without using DMA cycles or indexing.

Physical Mapping

The PIO registers are I/O mapped via four locations. Two address pins provide access to all of the CS4231's registers. The four direct registers are shown in Table 1. The first two direct registers are used to access 32 indirect registers shown in Table 2. As indicated by the arrows, the Index Address register (R0) points to the indirect register that is accessed through the Indexed Data register (R1).

This section describes all the direct and indirect registers. Table 3 details a summary of each bit in each register with Tables 4 through 10 illustrating the majority of decoding needed when programming the CS4231 and are included for reference. Tables 4 through 8 indicate gain settings at internal nodes. If OLB= 1 then the output will reflect the gain setting. If OLB= 0, the output will be attenuated by 3 dB as indicated in the specifications. The CS4231 powers up into the reset state which is defined as MODE 1. MODE 1 is backwards compatible with the CS4248 and only allows access to the first 16 indirect registers. Setting the MODE2 bit in the MODE and ID register (I12) enables

Index	Register Name
I0	Left ADC Input Control
I1	Right ADC Input Control
I2	Left Aux #1 Input Control
I3	Right Aux #1 Input Control
I4	Left Aux #2 Input Control
I5	Right Aux #2 Input Control
I6	Left DAC Output Control
I7	Right DAC Output Control
I8	Fs & Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID (MODE2 bit)
I13	Loopback Control
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left Line Input Control
I19	Right Line Input Control
I20	Timer Low Byte
I21	Timer High Byte
I22	RESERVED
I23	RESERVED
I24	Alternate Feature Status
I25	Version / Chip ID
I26	Mono Input & Output Control
I27	RESERVED
I28	Capture Data Format
I29	RESERVED
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 2. Indirect Registers

MODE 2 which allows access to indirect registers 16 through 31 and enables all the features of the CS4231.

Index Address Register (R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the CS4231 register accessed by the Indexed Data register (R1). These bits are read/write.

IA4 — Allows access to indirect registers 16 - 31. Only available in MODE 2. In MODE 1,this bit is reserved.

MCE — Mode Change Enable: This bit must be set whenever the current mode of the CS4231 is changed. The Data Format (I8, I28) and Interface Configuration (I9) registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". The DAC output is muted when MCE is set.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the status register is set. Independent for playback and capture interrupts.

0 - Transfers Enabled (PDRQ and CDRQ occur uninhibited)
1 - Transfers Disabled (PDRQ and CDRQ only occur if INT bit is 0)

INIT — CS4231 Initialization: This bit is read as 1 when the CS4231 is in a state in which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the CS4231 has left the INIT state), the state of this register is: 010x0000

During initialization and power down, this register CANNOT be written and always reads 10000000 (80h)

Indexed Data Register (R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 — Indexed Data register: These bits are the indirect register referenced by the Indexed Address register (R0).

During initialization and power down, this register can NOT be written and is always read 10000000 (80h)

4

I/O Data Registers

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During initialization and power down, this register CANNOT be written and is always read 10000000 (80h)

Capture I/O Data Register (R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 — Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, and a read of the status has occurred, the state machine and Status register (R2) will point to the first byte of the new sample.

Direct Registers: (R0-R3)

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	INIT	MCE	TRD	IA4†	IA3	IA2	IA1	IA0
R1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R2	1	0	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
R3	1	1	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R3	1	1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers: (I0-I31)

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	-	RAG3	RAG2	RAG1	RAG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDM	-	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	-	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8 §	FMT1†	FMT0	C/$\overline{L}$	S/$\overline{M}$	CSF2	CSF1	CSF0	C2SL
9 §	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	-	-	DEN	-	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	MODE2	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14 *	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15 *	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16	OLB	TE	-	-	-	-	-	DACZ
17	-	-	-	-	-	-	-	HPF
18	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
19	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
20	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
21	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
22	-	-	-	-	-	-	-	-
23	-	-	-	-	-	-	-	-
24	-	TI	CI	PI	CU	CO	PO	PU
25	V2	V1	V0	-	-	CID2	CID1	CID0
26	MIM	MOM	-	-	MIA3	MIA2	MIA1	MIA0
27	-	-	-	-	-	-	-	-
28 §	FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	-	-	-	-
29	-	-	-	-	-	-	-	-
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

† IA4 and FMT2 bits are only available in MODE 2 (IA = 12, bit 6 = 1)
Since IA4 is only available in MODE 2, registers 16-31 are only available in MODE 2

* When in MODE 1, the playback base registers (upper and lower) are used for both playback and capture.

§ MCE must be set before changing any bits in these registers (except CEN and PEN).

Table 3. Register Bit Summary

NOTE: Output level relative to input level assuming OLB=1.

	AG3	AG2	AG1	AG0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	1.5 dB
2	0	0	1	0	3.0 dB
3	0	0	1	1	4.5 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	18.0 dB
13	1	1	0	1	19.5 dB
14	1	1	1	0	21.0 dB
15	1	1	1	1	22.5 dB

Table 4. ADC Input Gain

	A5	A4	A3	A2	A1	A0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.				.			.
.				.			.
.				.			.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 6. DAC & Loopback Attenuation

	MIA3	MIA2	MIA1	MIA0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	-3.0 dB
2	0	0	1	0	-6.0 dB
3	0	0	1	1	-9.0 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	-36.0 dB
13	1	1	0	1	-39.0 dB
14	1	1	1	0	-42.0 dB
15	1	1	1	1	-45.0 dB

Table 7. Mono Mixer Attenuation

	SS1	SS0	ADC Input Multiplexer
0	0	0	Line
1	0	1	Auxiliary 1
2	1	0	Microphone
3	1	1	Line Output Loopback

Table 9. ADC Input Selector

	G4	G3	G2	G1	G0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	**0**	**1**	**0**	**0**	**0**	**0.0 dB**
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.			.			.
.			.			.
.			.			.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 5. AUX1 & AUX2 & LINE Mixer Gain

	CFS2	CFS1	CFS0	XTAL1 24.576 MHz	XTAL2 16.9344MHz
0	0	0	0	8.0 kHz	5.51 kHz
1	0	0	1	16.0 kHz	11.025 kHz
2	0	1	0	27.42 kHz	18.9 kHz
3	0	1	1	32.0 kHz	22.05 kHz
4	1	0	0	N/A	37.8 kHz
5	1	0	1	N/A	44.1 kHz
6	1	1	0	48.0 kHz	33.075 kHz
7	1	1	1	9.6 kHz	6.62 kHz

Table 8. Sample Frequency Select

	FMT1	FMT0	C/$\overline{L}$	Audio Data Format
0	0	0	0	Linear, 8-bit unsigned
1	0	0	1	μ-Law, 8-bit
2	0	1	0	Linear, 16-bit, 2's C, LEnd.
3	0	1	1	A-Law, 8-bit
5	1	0	1	ADPCM, 4-bit IMA
6	1	1	0	Linear, 16-bit, 2'sC, BEnd.

Table 10. Audio Data Format

During initialization and power down, this register can NOT be written and is always read 10000000 (80h)

Playback I/O Data Register (R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 Playback Data Port. This is the control register where playback data is written during programmed IO data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Status Register (R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT

INT Interrupt Status: This indicates the status of the internal interrupt logic of the CS4231. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin of the CS4231.
Read States

0 - Interrupt inactive
1 - Interrupt active

PRDY Playback Data Ready. The Playback Data register (R3) is ready for more data. This bit would be used when direct programmed I/O data transfers are desired.

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

PL/$\overline{R}$ Playback Left/Right Sample: This bit indicates whether data needed is for the Left channel or Right channel.

0 - Right Channel Data
1 - Left Channel or Mono Data

PU/$\overline{L}$ Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel.

0 - Lower Byte needed
1 - Upper Byte needed or any 8-bit mode

SER Sample Error: This bit indicates that a sample was not serviced in time and an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. However, the Alternate Feature Status register (I24) can indicate the exact source of the error.

CRDY Capture Data Ready. The Capture Data register (R3) contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers.

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Left channel or Right channel.

0 - Right Channel Data
1 - Left Channel or Mono Data

CU/$\overline{L}$ Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel.

0 - Lower byte ready
1 - Upper byte or any 8-bit ready

Note on PRDY/CRDY: These two bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one, the device is ready for more data; or when the CRDY is set to one, data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

Indirect Mapped Registers

These registers are accessed by placing the appropriate index in the Index Address register (R0) and then accessing the Indexed Data register (R1). A detailed description of each indirect register is given below. All reserved bits should be written zero and may be 0 or 1 when read. Note that indirect registers 16-31 are only available when the MODE2 bit in MODE and ID register (I12) is set.

Left ADC Input Control (I0)

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LAG3	LAG2	LAG1	LAG0

LAG3-LAG0 Left ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 4.

LMGE Left Mic Gain Enable: This bit enables the 20 dB gain stage of the left mic input signal, LMIC.

LSS1-LSS0 Left ADC Input Source Select. These bits select the input source for the left ADC channel.

0 - Left Line: LLINE
1 - Left Auxiliary 1: LAUX1
2 - Left Microphone: LMIC
3 - Left Line Output Loopback

This register's initial state after reset is: 000x0000

Right ADC Input Control (I1)

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RAG3	RAG2	RAG1	RAG0

RAG3-RAG0 Right ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 4.

RMGE Right Mic Gain Enable: This bit enables the 20 dB gain stage of the right mic input signal, RMIC.

RSS1-RSS0 Right ADC Input Select. These bits select the input source for the right ADC channel.

0 - Right Line: RLINE
1 - Right Auxiliary 1: RAUX1
2 - Right Microphone: RMIC
3 - Right Line Out Loopback

This register's initial state after reset is: 000x0000

Left Auxiliary #1 Input Control (I2)

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0 Left Auxiliary #1, LAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LX1M Left Auxiliary #1 Mute. When set to 1, the left Auxiliary #1 input, LAUX1, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #1 Input Control (I3)

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0 Right Auxiliary #1, RAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RX1M Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Left Auxiliary #2 Input Control (I4)

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2, LAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LX2M Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #2 Input Control (I5)

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2, RAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RX2M Right Auxiliary #2 Mute. When set to 1, the right Auxiliary #2 input, RAUX2, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Left DAC Output Control (I6)

D7	D6	D5	D4	D3	D2	D1	D0
LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5-LDA0 Left DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

LDM Left DAC Mute. When set to 1, the left DAC output to the mixer will be muted.

This register's initial state after reset is: 1x000000.

Right DAC Output Control (I7)

D7	D6	D5	D4	D3	D2	D1	D0
RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5-RDA0 Right DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

RDM Right DAC Mute. When set to 1, the right DAC output to the mixer will be muted.

This register's initial state after reset is: 1x000000.

Fs and Playback Data Format (I8)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	CSF2	CFS1	CFS0	C2SL

C2SL Clock 2 Source Select: This bit selects the clock source used for the audio sample rates for both capture and playback.
CAUTION: See note below about changing these bits

0 - XTAL1 Typically 24.576 MHz
1 - XTAL2 Typically 16.9344 MHz

CFS2-CFS0 Clock Frequency Divide Select: These bits select the audio sample frequency for both capture and playback. The actual audio sample frequency depends on which clock source (C2SL) is selected and its frequency. Frequencies listed as N/A are not available because their sample frequency violates the maximum specifications; however, the decodes are available and may be used with crystals that do not violate the sample frequency specifications.
CAUTION: See note below about changing bits

Divide	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result in alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left channel. In MODE 1, this bit is used for both playback and capture. In MODE 2, this bit is only used for playback, and the capture format is independently selected via I28.

0 - Mono
1 - Stereo

The C/$\overline{L}$, FMT1, and FMT0 bits set the audio data format as shown below. In MODE 1, FMT1, which is forced low, FMT0, and C/$\overline{L}$ are used for both playback and capture. In MODE 2, these bits are only used for playback, and the capture format is independently selected via register I28.

FMT1† D7	FMT0 D6	C/$\overline{L}$ D5	
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

† FMT1 is not available in MODE 1 (forced to 0).

This register's initial state after reset is: 0000000.

Interface Configuration (I9)

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

PEN Playback Enable. This bit enables playback. The CS4231 will generate PDRQ and respond to PDAK signals when this bit is enabled and PPIO=0. If PPIO=1, PEN enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (PDRQ and PIO inactive)
1 - Playback Enabled

CEN Capture Enabled. This bit enables the capture of data. The CS4231 will generate CDRQ and respond to CDAK signals when CEN is enabled and CPIO=0. If CPIO=1, CEN enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 - Capture disabled (CDRQ and PIO inactive)
1 - Capture enabled

SDC Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be zero. This bit forces the CS4231 to use one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the DMA section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

ACAL — Auto-Calibrate Enable: This bit determines whether the CS4231 performs a calibration whenever the Mode Change Enable (MCE) bit changes from 1 to 0. If the ACAL bit is not set, previous calibration values are used, and no calibration takes place.

0 - No auto calibration
1 - Auto calibration enabled

PPIO — Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

CPIO — Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

Note: This register, except bits CEN and PEN, can only be written while in Mode Change Enable. See section on MCE for more details.

This register's initial state after reset is: 00xx1000

Pin Control (I10)

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	res	res	DEN	res	IEN	res

IEN — Interrupt Enable: This bit enables the interrupt pin. The Interrupt pin will reflect the value of the INT bit of the Status register (R2). The interrupt pin is active high.

0 - Interrupt disabled
1 - Interrupt enabled

DEN — Dither Enable: When set, triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit, unsigned data. Dither is only active in the 8-bit unsigned mode.

0 - Dither enabled
1 - Dither disabled

XCTL1-XCTL0 — XCTL Control: These bits are reflected on the XCTL1,0 pins of the CS4231.

0 - TTL logic low on XCTL1,0 pins
1 - TTL logic high on XCTL1,0 pins

This registers initial state after reset is: 00xx0x0x

Error Status and Initialization (I11, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 — Overrange Left Detect: These bits determine the overrange on the left ADC channel. These bits are updated on a sample by sample basis.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

ORR1-ORR0 — Overrange Right Detect: These bits determine the overrange on the Right ADC channel.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS — DRQ Status: This bit indicates the current status of the PDRQ and CDRQ pins of the CS4231.

0 - CDRQ AND PDRQ are presently inactive
1 - CDRQ OR PDRQ are presently active

ACI — Auto-calibrate In-Progress: This bit indicates the state of calibration.

0 - Calibration not in progress
1 - Calibration is in progress

PUR — Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result, if DACZ = 0, the last valid sample will be sent to the DACs. This bit is set when an error occurs and will not clear until the Status register (R2) is read.

COR — Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The old sample will not be overwritten and the new sample will be ignored. This bit is set when an error condition occurs and will not clear until the Status register(R2) is read.

The SER bit in the Status register (R2) is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

This register's initial state after reset is: 00000000

MODE and ID (I12)

D7	D6	D5	D4	D3	D2	D1	D0
1	MODE2	res	res	ID3	ID2	ID1	ID0

ID3-ID0 — Codec ID: These four bits indicate the ID and initial revisions of the codec. Further revisions are expanded in indirect register 25. These bits are read only.

0001 - Revision "B". See Appendix
1010 - Revision "C" on. See register 25 and the Appendix.

MODE2 — MODE 2: Enables the expanded mode of the CS4231. Must be set to enable access to indirect registers 16-31 and their associated features.

0 - MODE 1: CS4248 "look-alike".
1 - MODE 2: Expanded features.

This register's initial state after reset is: 10xx1010

Loopback Control (I13)

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE — Loopback Enable: When set to 1, the ADC data is digitally mixed with data sent to the DACs.

0 - Loopback disabled
1 - Loopback enabled

LBA5-LBA0 — Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

This register's initial state after reset is: 000000x0

Playback Upper Base (I14)

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-PUB0 — Playback Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. The Current Count registers cannot be read. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

This register's initial state after reset is: 0000000

Playback Lower Base (I15)

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-PLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

This register's initial state after reset is: 00000000

Alternate Feature Enable I (I16)

D7	D6	D5	D4	D3	D2	D1	D0
OLB	TE	res	res	res	res	res	DACZ

DACZ — DAC Zero: This bit will force the output of the playback channel to AC zero when an underrun error occurs

1 - Go to center scale
0 - Hold previous valid sample

TE — Timer Enable: This bit, when set, will enable the timer to run and interrupt the host at the specified frequency in the timer registers.

OLB — Output Level Bit: Sets the analog output level. When clear, analog line outputs are attenuated 3dB.

0 - Full scale of 2 Vpp (-3 dB)
1 - Full scale of 2.8 Vpp (0 dB)

This register's initial state after reset is: 00xxxxx0

Alternate Feature Enable II (I17)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	HPF

HPF — High Pass Filter: This bit enables a DC-blocking high-pass filter in the digital filter of the ADC. This filter forces the ADC offset of 0.

0 - disabled
1 - enabled

This register's initial state after reset is: xxxxxxx0.

Left Line Input Control (I18)

D7	D6	D5	D4	D3	D2	D1	D0
LLM	res	res	LLG4	LLG3	LLG2	LLG1	LLG0

LLG4-LLG0 — Left Line, LLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LLM — Left Line Mute. When set to 1, the left Line input, LLINE, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Line Input Control (I19)

D7	D6	D5	D4	D3	D2	D1	D0
RLM	res	res	RLG4	RLG3	RLG2	RLG1	RLG0

RLG4-RLG0 — Right Line, RLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RLM — Right Line Mute. When set to 1, the Right Line input, RLINE, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Timer Lower Byte (I20)

D7	D6	D5	D4	D3	D2	D1	D0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

TL7-TL0 — Lower Timer Bits: This is the low order byte of the 16-bit timer.

This register's initial state after reset is: 00000000.

Timer Upper Byte (I21)

D7	D6	D5	D4	D3	D2	D1	D0
TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

TU7-TU0 — Upper Timer Bits: This is the high order byte of the 16-bit timer. The time base is determined by the clock source selected.

C2SL = 0 - divide XTAL1 by 245 (24.576 MHz - 9.969 µs)

C2SL = 1 - divide XTAL2 by 168 (16.9344 MHz - 9.92 µs)

This register's initial state after reset is: 00000000

RESERVED (I22)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

RESERVED (I23)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Alternate Feature Status (I24)

D7	D6	D5	D4	D3	D2	D1	D0
res	TI	CI	PI	CU	CO	PO	PU

PU — Playback Underrun: This bit, when set, indicates that the DAC has run out of data and a sample has been missed.

PO — Playback Overrun: This bit, when set, indicates that the host attempted to write data into a full FIFO and the data was discarded.

CO — Capture Overrun: This bit, when set, indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case the bit is set and the new sample is discarded.

CU — Capture Underrun: This bit indicates that the host has read more data out of the FIFO than it contained. In this condition, the bit is set and the last valid byte is read by the host.

PI — Playback Interrupt: This bit indicates that an interrupt is pending from the playback DMA count registers.

CI — Capture Interrupt: This bit indicates that an interrupt is pending from the record DMA count registers.

TI — Timer Interrupt: This bit indicates that an interrupt is pending from the timer count registers

The PI, CI, and TI bits are reset by writing a "0" to the particular interrupt bit or by writing any value to the Status register (R2).

This register's initial state after reset is: x0000000

Version / ID (I25)

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	res	res	CID2	CID1	CID0

V2-V0 — Version number. As enhancements are made to the CS4231, the version number is changed so software can distinguish between the different versions.

100 - Revision C, D, & E. This Data Sheet

CID2-CID0 — Chip Identification. Distinguishes between this chip and future chips that support this register set.

000 - CS4231

This register's initial state after reset is: 000xx000

Mono Input & Output Control (I26)

D7	D6	D5	D4	D3	D2	D1	D0
MIM	MOM	res	res	MIA3	MIA2	MIA1	MIA0

MIA3-MIA0 — Mono Input Attenuation. MIA0 is the least significant bit and represents 3 dB attenuation, with 0000 = 0 dB. See Table 7.

MOM — Mono Output Mute. The MOM bit will mute the mono mix output, MOUT. This mute is independent of the line output mute.

0 - no mute
1 - mute

MIM — Mono Input Mute. This bit controls the mute function on the mono input, MIN. The mono input provides mix for the "beeper" function in most personal computers.

0 - no mute
1 - muted

This register's initial state after reset is: 00xx0011.

4

RESERVED (I27)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Capture Data Format (I28)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	res	res	res	res

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the capture audio data stream is formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Selecting mono only captures data from the left audio channel.

0 - Mono
1 - Stereo

The C/$\overline{L}$, FMT1, and FMT0 bits set the capture data format in MODE 2. See Table 10 or register I8 for the bit settings and data formats. The capture data format can be different that the playback data format; however, the sample frequency must be the same and is set in I8. MCE must be set to modify this register.
This register's initial state after reset is: 0000xxxx

RESERVED (I29)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Capture Upper Base (I30)

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-CUB0 Capture Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Capture Base register. Reads from this this register returns the same value that was written.

This register's initial state after reset is: 0000000

Capture Lower Base (I31)

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-CLB0 Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Capture Base register. Reads from this register returns the same value which was written.

This register's initial state after reset is: 00000000

GROUNDING AND LAYOUT

Figure 16 is a suggested layout for the CS4231. Similar to other Crystal codecs, it is recommended that the device be located on a separate analog ground plane. With the CS4231's parallel data interface, however, optimum performance is achieved by extending the digital ground plane across pins 65 through 68 and pins 1 through 8. Pins 2 and 8 are grounds for the data bus and should be electrically connected to the digital ground plane which will minimize the effects of the bus interface due to transient currents during bus switching. Figure 17 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the CS4231. The vias shown go through to the ground plane layer. Vias, power supply traces, and VREF traces should be as large as possible to minimize the impedance.

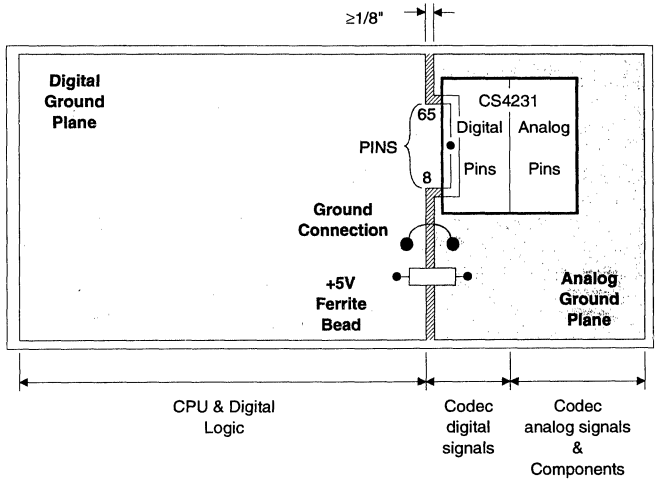


Figure 16. Suggested Layout Guideline

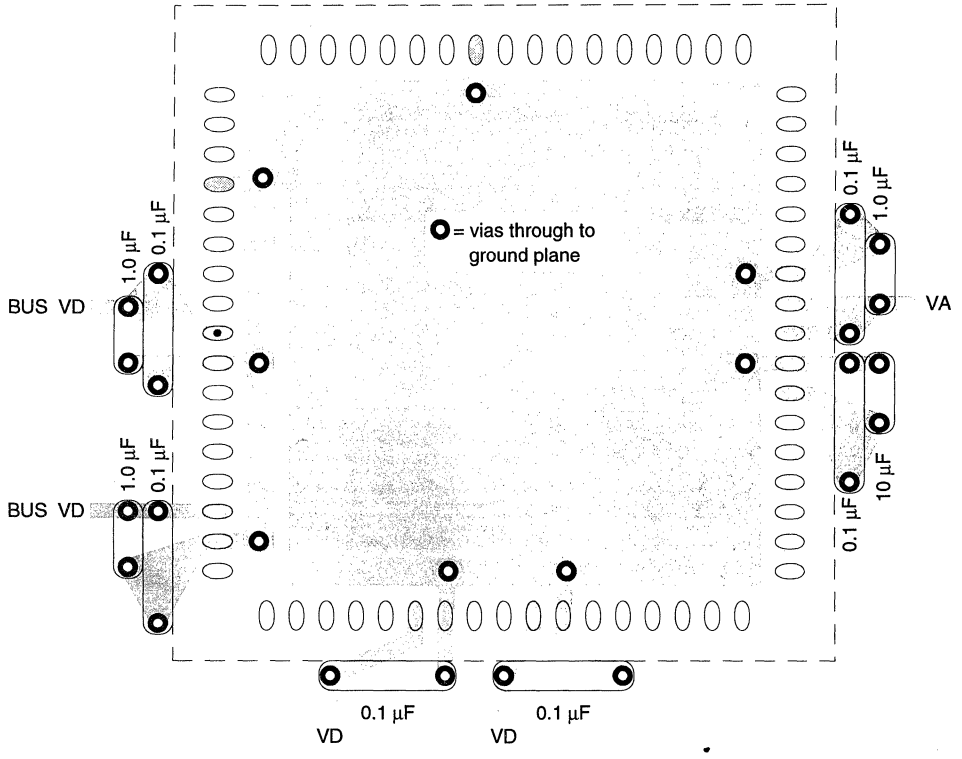


Figure 17. Recommended Decoupling Capacitor Positions

COMPATIBILITY WITH AD1848

The CS4231 is compatible with the AD1848 rev. J silicon and the CS4248 in terms of the applications circuit. The AD1848 rev K requires 0.1 µF capacitors (not 1000 pF) on pins 26 and 31. The CS4231 requires 1000 pF NPO-type capacitors on filter pins 26 and 31 (not 0.1 µF). To achieve compatibility with the CS4231:

1. Correct spacing of pads will ensure that either 0.1 µF capacitors (for the AD1848 rev K) or 1000 pF NPO capacitors (for the CS4248) may be installed.

2. The CS4231 does not require the input anti-aliasing filters included as an input R/C for the AD1848 (5.1kΩ and 560 pF). The additional R/C's can be used with the CS4231 if desired, with no degradation in performance.

3. Although optimum performance is achieved using the ground plane shown in Figure 16, any ground plane scheme that achieves acceptable performance with the AD1848 should work with the CS4231.

4. The AD1848 needs extra power and ground pins. The power pins (V_{DD}) are pins 24, 45, and 54. The ground pins (GNDD) are pins 25 and 44. The CS4231 PLCC package does not use these pins and the appropriate power/ground connections can be made.

5. The Mono In/Mono Out pins do not exist on the AD1848.

6. The AD1848 does not contain 16 mA bus drivers. Therefore, buffers must be used.

7. MODE 2 and all associated features do not exist on the AD1848.

8. The AD1848 does not contain the selectable dither (DEN, I10)

9. The AD1848 is not available in a 100-pin TQFP package.

ADC/DAC FILTER RESPONSE PLOTS

Figures 18 through 23 show the overall frequency response, passband ripple, and transition band for the CS4231 ADCs and DACs. Figure 24 shows the DACs' deviation from linear phase. Since the CS4231 scales filter response based on sample frequency selected, all frequency response plots x-axis' are shown from 0 to 1 where 1 is equivalent to Fs. Therefore, for any given sample frequency, multiply the x-axis values by the sample frequency selected to get the actual frequency.

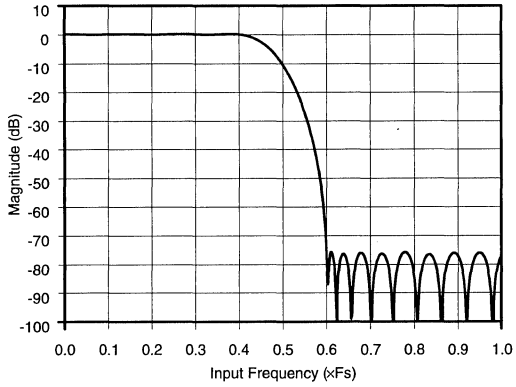


Figure 18. ADC Filter Response.

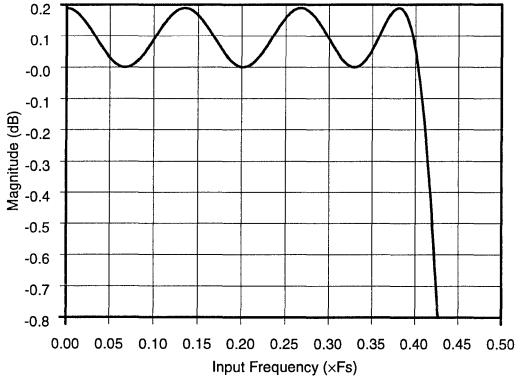


Figure 19. ADC Passband Ripple.

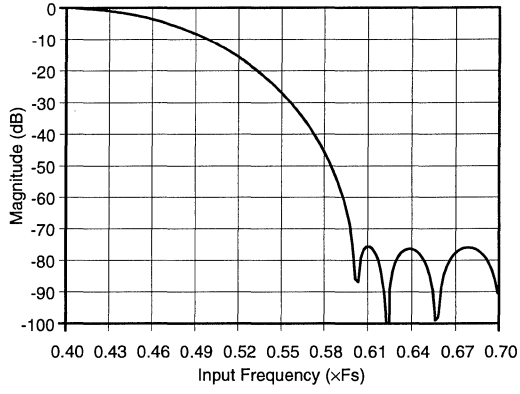


Figure 20. ADC Transition Band.

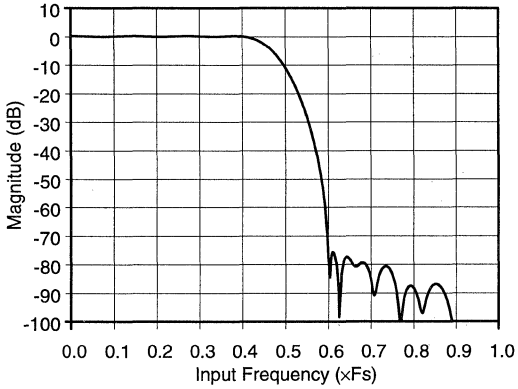


Figure 21. DAC Filter Response.

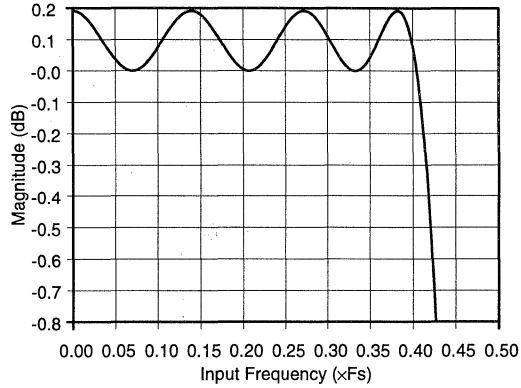


Figure 22. DAC Passband Ripple.

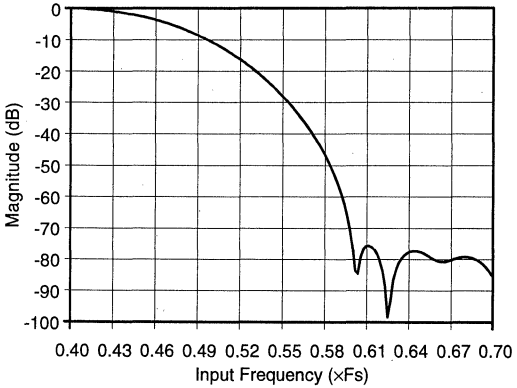


Figure 23. DAC Transition Band.

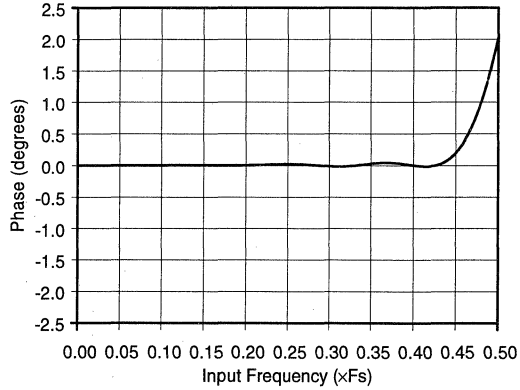
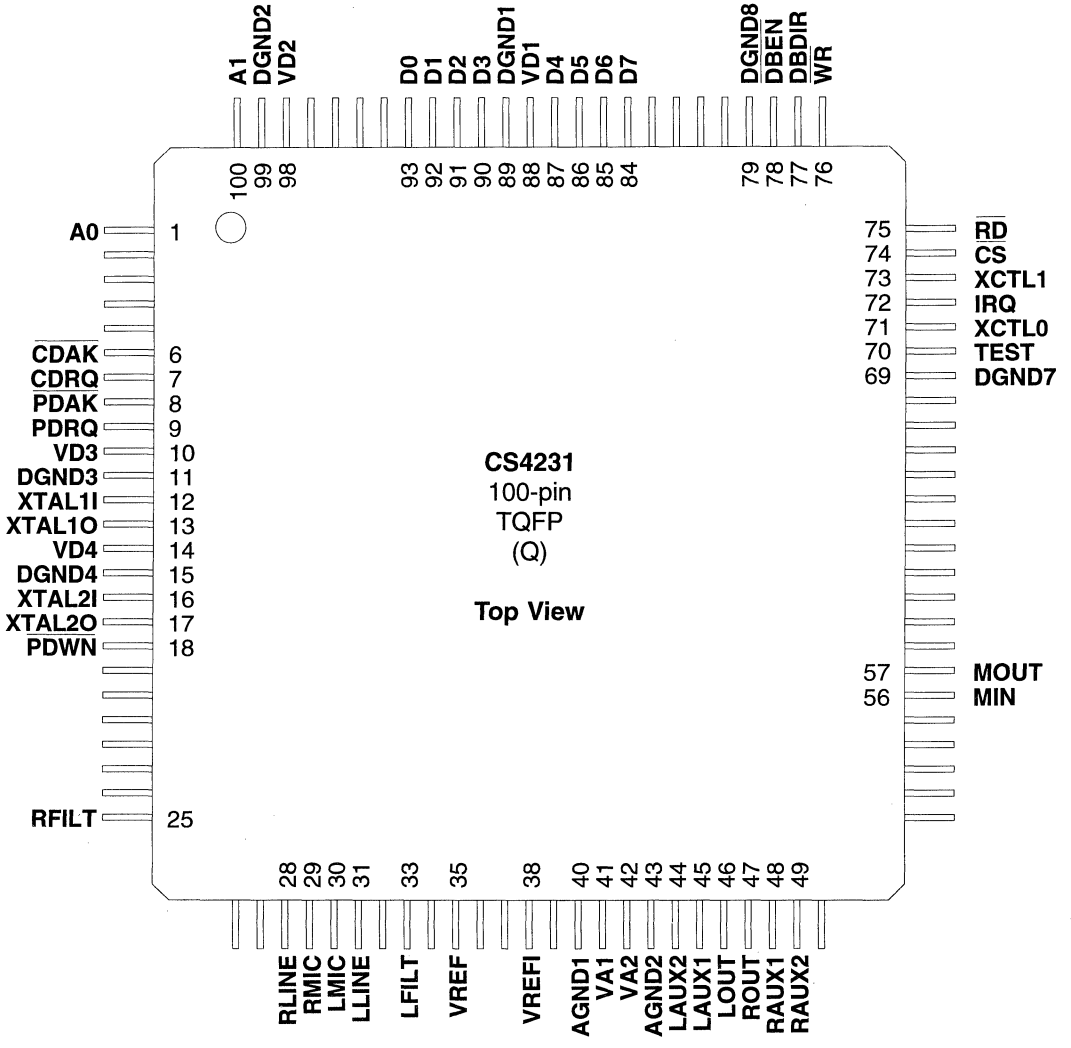
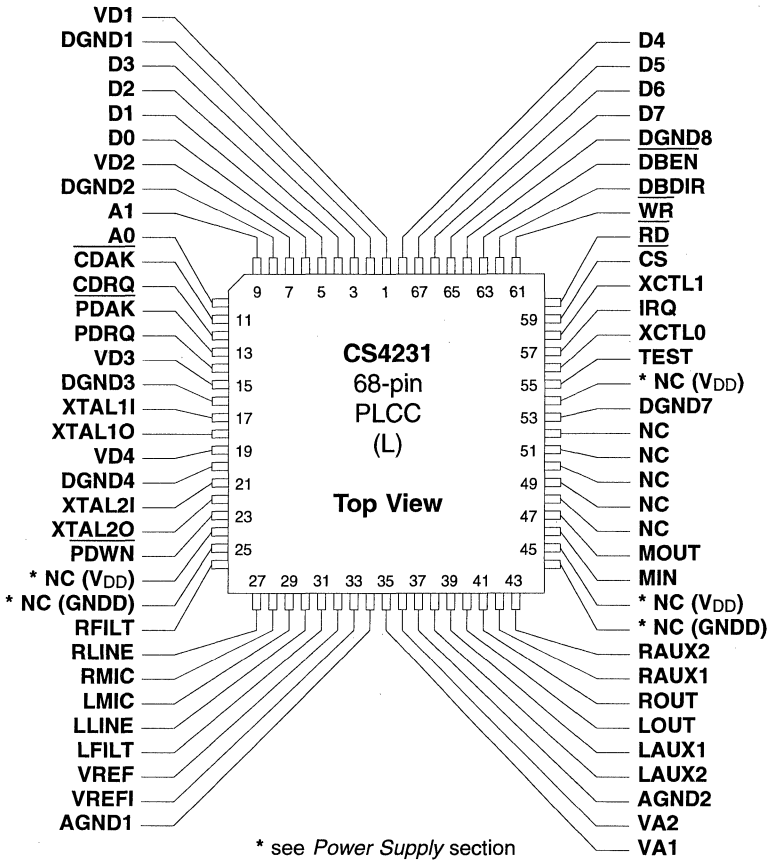


Figure 24. DAC Phase Response.

PIN DESCRIPTIONS





Parallel Bus Interface Pins

CDRQ - Capture Data Request, Output, Pin 12 (L), Pin 7 (Q).

The assertion of this signal indicates that the codec has a captured audio sample ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.

$\overline{\text{CDAK}}$ - Capture Data Acknowledge, Input, Pin 11 (L), Pin 6 ($\overline{\text{Q}}$).

The assertion of this active low signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.

PDRQ - Playback Data Request, Output, Pin 14 (L), Pin 9 (Q).

The assertion of this signal indicates that the codec is ready for more playback data. The signal will remain asserted until the bytes needed for a playback sample have been transferred.

$\overline{\text{PDAK}}$ - Playback Data Acknowledge, Input, Pin 13 (L), Pin 8 (Q).
The assertion of this active low signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.

A< 1:0> - Address Bus, Input, Pin 9, 10 (L), Pin 100, 1 (Q).
These address pins are read by the codec interface logic during an I/O cycle access. The state of these address lines determines which register (R0-R3) is accessed.

$\overline{\text{RD}}$ - Read Strobe, Input, Pin 60 (L), Pin 75 (Q).
This signal defines a read cycle to the codec. The cycle may be an I/O cycle read, or the cycle could be a read from the codec's DMA sample registers.

$\overline{\text{WR}}$ - Write Strobe, Input, Pin 61 (L), Pin 76 (Q).
This signal indicates a write cycle to the codec. The cycle may be an I/O cycle write, or the cycle could be a write to the codec's DMA sample registers.

$\overline{\text{CS}}$ - Chip Select, Input, Pin 59 (L), Pin 74 (Q).
The codec will not respond to any I/O cycle accesses unless this signal is active. This signal is ignored during DMA transfers.

D< 7:0> - Data Bus, Input/Output, Pin 65-68, 3-6 (L), Pin 84-87, 90-93 (Q).
These signals are used to transfer data to and from the CS4248.

$\overline{\text{DBEN}}$ - Data Bus Enable, Output, Pin 63 (L), Pin 78 (Q).
This pin indicates that the bus drivers attached to the CS4248 should be enabled. This signal is normally high.

DBDIR - Data Bus Direction, Output, Pin 62 (L), Pin 77 (Q).
This pin indicates the direction of the data bus transceiver. High points to the CS4231, low points to the host bus. This signal is normally high.

IRQ - Host Interrupt Pin, Output, Pin 57 (L), Pin 72 (Q).
This signal is used to notify the host of events which need servicing.

Analog Inputs

LLINE - Left Line Input, Pin 30 (L), Pin 31 (Q).
Nominally 1 V_{RMS} max analog input for the Left LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I18) also allows routing to the mixer.

RLINE - Right Line Input, Pin 27 (L), Pin 28 (Q).
Nominally 1 V_{RMS} max analog input for the Right LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I19) also allows routing to the mixer.

LMIC - Left Mic Input, Pin 29 (L), Pin 30 (Q).

Microphone input for the Left MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (LMGE = 0) or 0.1 V_{RMS} (LMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I0).

RMIC - Right Mic Input, Pin 28 (L), Pin 29 (Q).

Microphone input for the Right MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (RMGE = 0) or 0.1 V_{RMS} (RMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I1).

LAUX1 - Left Auxiliary #1 Input, Pin 39 (L), Pin 45 (Q).

Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I2) also allows routing to the output mixer.

RAUX1 - Right Auxiliary #1 Input, Pin 42 (L), Pin 48 (Q).

Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I3) also allows routing to the output mixer.

LAUX2 - Left Auxiliary #2 Input, Pin 38 (L), Pin 44 (Q).

Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block (I4) allows routing of the AUX2 channels into the output mixer.

RAUX2 - Right Auxiliary #2 Input, Pin 43 (L), Pin 49 (Q).

Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block (I5) allows routing of the AUX2 channels into the output mixer.

MIN - Mono Input, Pin 46 (L), Pin 56 (Q).

Nominally 1 V_{RMS} max analog input, centered around VREF, that goes through a programmable gain stage (I26) into both channels of the mixer. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system.

Analog Outputs

LOUT - Left Line Level Output, Pin 40 (L), Pin 46 (Q).

Analog output from the mixer for the left channel. Nominally 1 V_{RMS} max centered around VREF when OLB = 1 (I16). When OLB = 0, the output is attenuated 3 dB and is a maximum of 0.707 V_{RMS}.

ROUT - Right Line Level Output, Pin 41 (L), Pin 47 (Q).

Analog output from the mixer for the right channel. Nominally 1 V_{RMS} max centered around VREF when OLB = 1 (I16). When OLB = 0, the output is attenuated 3 dB and is a maximum of 0.707 V_{RMS}.

MOUT - Mono Output, Pin 47 (L), Pin 57 (Q).

When OLB=1 (I16), MOUT is nominally 1 V_{RMS} max analog output, centered around VREF. When OLB=0, the maximum output voltage is 3 dB lower, 0.707 V_{RMS}. This output is a summed analog output from both the left and right output channels of the mixer. MOUT typically is connected to a speaker driver that drives the internal speaker in most computers. Independantly mutable via MOM in I26.

Miscellaneous

XTAL1I - Crystal #1 Input, Pin 17 (L), Pin 12 (Q).

This pin will accept either a crystal with the other pin attached to XTAL1O or an external CMOS clock. XTAL1 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 24.576 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL1O - Crystal #1 Output, Pin 18 (L), Pin 13 (Q).

This pin is used for a crystal placed between this pin and XTAL1I.

XTAL2I - Crystal #2 Input, Pin 21 (L), Pin 16 (Q).

If a second crystal is used, is should be placed between this pin and XTAL2O. The standard crystal frequency is 16.9344 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL2O - Crystal #2 Output, Pin 22 (L), Pin 17 (Q).

This pin is used for a crystal placed between this pin and XTAL2I.

$\overline{\text{PDWN}}$ - Power Down, Input, Pin 23 (L), Pin 18 (Q).

Places CS4231 in lowest power consumption mode. All sections of the CS4231, except the digital bus interface which reads 80h, are shut down and consuming minimal power. The CS4231 is in power down mode when this pin is logic low.

XCTL0, XCTL1 - External Control, Output, Pin 56, 58 (L), Pin 71, 73 (Q).

These signals are controlled by the register bits XCTL0 and XCTL1 in register I10. They can be used to control external logic via TTL levels.

VREF - Voltage Reference, Output, Pin 32 (L), Pin 35 (Q).

All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered. High internal-gain microphone inputs can be slightly improved by placing a 10µF capacitor on VREF.

VREFI - Voltage Reference Internal, Input, Pin 33 (L), Pin 38 (Q).

Voltage reference used internal to the CS4231 must have a 0.1 µF + 10 µF capacitor with short fat traces to attach to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input, Pin 31 (L), Pin 33 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

RFILT - Right Channel Antialias Filter Input, Pin 26 (L), Pin 25 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

TEST - Test, Pin 55 (L), Pin 70 (Q).
This pin must be tied to ground for proper operation.

Power Supplies

VA1, VA2 - Analog Supply Voltage, Pin 35, 36 (L), Pin 41, 42 (Q).
Supply to the analog section of the codec.

AGND1, AGND2 - Analog Ground, Pin 34, 37 (L), Pin 40, 43 (Q).
Ground reference to the analog section of the codec. Internally, these pins are connected to the substrate as are DGND3/4/7/8; therefore, optimum layout is achieved with the AGND pins on the same ground plane as DGND3/4/7/8 (see Figure 17). However, other ground arrangements should yield adequate results.

VD1, VD2 - Digital Supply Voltage, Pin 1, 7 (L), Pin 88, 98 (Q).
Digital supply for the parallel data bus section of the codec.

VD3, VD4 - Digital Supply Voltage, Pin 15, 19 (L), Pin 10, 14 (Q).
Digital supply for the internal digital section of the codec (except for the parallel data bus).

DGND1, DGND2 - Digital Ground, Pin 2, 8 (L), Pin 89, 99 (Q).
Digital ground reference for the parallel data bus section of the codec. These pins are isolated from the other digital grounds and should be connected to the digital ground section of the board (see Figure 17).

DGND3, DGND4, DGND7, DGND8 - Digital Ground, Pin 16, 20, 53, 64(L), Pin 11, 15, 69, 79(Q)
Digital ground reference for the internal digital section of the codec (except the parallel data bus). These pins are connected to the substrate of the die as are the AGND pins. Optimum layout is achieved by placing DGND3/4/7/8 on the analog ground plane with the AGND pins as shown in Figure 17. However, other ground arrangements should yield adequate results.

*** NC (V_{DD}) - No Connect, Pins 24, 45, 54 (L)**
These pins are no connects for the CS4231. When compatibility with the AD1848 is desired, these pins should be connected to the digital power supply. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

*** NC (GNDD) - No Connect, Pins 25, 44 (L)**
These pins are no connects for the CS4231. When compatibility with the AD1848 is desired, these pins should be connected to digital ground. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

TABLE OF CONTENTS:

Semiconductor Corporation

CDB4231/4248

CS4231/4248 Evaluation Board

Features

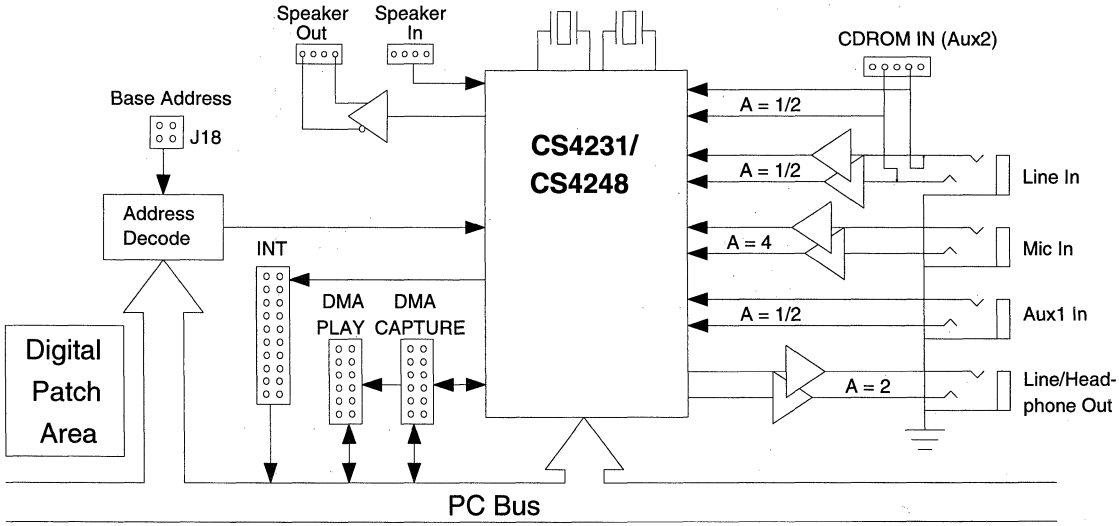
- PC ISA Plug-In Card
- Mono In / Mono Out Support
- Microphone Pre-Amplifier
- Line Out / Headphone Circuit
- Microsoft Windows™ 3.1 Software Support

General Description

The CDB4231/4248 evaluation board supports all the features of the CS4231 and CS4248. The CS4231 is an enhanced version, and is backwards compatible with the CS4248. The DMA, IRQ, and base address are all selectable via on-board jumpers. Four stereo jacks provide MIC in, AUX1 in, LINE in, and Line/Headphone out. In addition, on-board headers provide an internal analog CD-ROM interface via the AUX2 inputs, and support for the mono in and mono out capabilities of the CS4231.

Software that runs under Microsoft Windows™ 3.1 is also provided along with an extensive diagnostics program.

ORDERING INFORMATION: CDB4231, CDB4248



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

GENERAL INFORMATION

The CDB4231/4248 is designed to provide an easy platform for evaluating the performance of the CS4231 or CS4248 Parallel Interface, Multimedia Audio Codec in a PC environment.

Software that operates under the Microsoft Windows™ environment is also included with applets that control all the CS4231 or CS4248 features. This software also provides full Windows™ 3.1 compatibility with extensions to utilize the more powerful CS4231 features in custom code.

Four stereo jacks, externally accessible, allow connection to Microphone inputs, Auxiliary 1 inputs, Line inputs, and Line/Headphone outputs. Headers allow internal connections to a CD-ROM analog output (using the codec's Auxiliary 2 inputs), and speaker pass-through and control via the **SPEAKER IN** (Mono In) and **SPEAKER OUT** (Mono Out) headers.

Additional headers on the board allow the setting of the Base Address, DMA channel, and IRQ for the CS4231. The factory default for the CDB4231 is base address 530h, DMA playback channel 3, DMA capture channel 0 and IRQ 7. The CDB4248 is the same with the exception of the DMA capture header which is not used and has both shorting jumpers removed.

The software must be configured to match the settings on the evaluation board headers for proper operation.

STEREO ANALOG INPUTS

Three of the four external $^1/_8$" stereo jacks are for analog inputs. The stereo **Mic I**, Microphone Input, (Figure 2) contains an op-amp buffer with a gain of 4 dB providing a maximum full scale of 91 mV (with the 20 dB boost inside the codec enabled). For microphones with larger signals, the 20 dB gain block inside the codec can be disabled in software (the "Boost" button in the input applet). The microphone circuit is designed for single-ended microphones which are the most common type available. The J35 header, close to the mic input jack allows selection of a stereo microphone when the jumper is in the 'S' position, or mono input where the jumper is in the 'M' position. In the mono position, a mono mic input would go to both the left and right mic input pins on the codec.

The second input jack is **Ax1 I**, Auxiliary 1 In, (Figure 1) which has an input impedance of approximately 10 kΩ with a maximum full scale into the **Ax1 I** jack of 2 V_{RMS}.

The third stereo input jack is **Line I**, Line In, (Figure 4) which also has a maximum full scale of 2 V_{RMS} and provides a typical audio input impedance of 47 kΩ.

An internal header, labeled **CDROM IN (AUX2)**, (Figure 4) may be used by any internal device for analog mixing into the codec's output mixer via the Auxiliary 2 inputs, AUX2. Since the AUX2 inputs don't have a path to the ADCs, when nothing is plugged into the **Line I** jack, the analog contained on the **CDROM IN** header is summed into the Line inputs of the codec as well as the AUX2 inputs. When a plug is inserted into the **Line I** jack, the **CDROM IN** header is disconnected from the Line inputs (but is still connected to the AUX2 inputs).

STEREO ANALOG OUTPUTS

The CDB4231/4248 contains one stereo analog output labeled **Ln/Hp O**, Line/Headphone Out,

Windows is a registered trademark of Microsoft Corporation

(Figure 5) with a maximum full-scale output of 2 V_{RMS}. This output provides a high-quality line out for use with external power amps or other equipment containing line-level inputs. It is also designed to drive headphones directly with exceptional quality.

MONO INPUT AND OUTPUT

The CS4231 contains a MIN (mono in) pin and a MOUT (mono out) pin that are typically placed in between the internal PC speaker and the beeper chip. The CDB4231 comes with a cable that should be connected between the PC beeper chip and the **SPEAKER IN** header (Figure 1) on the CDB4231 board. The cable wire, pin 1, should be placed on pin 1 of the **SPEAKER IN** header and pin 1 of the beeper header. If the PC beeps do not mix into the codec, try reversing the beeper header connector. This connects the beeper to the MIN pin on the CS4231 and allows traditional PC beeps to be mixed into the audio path.

The **SPEAKER OUT** header (Figure 3) should be connected to the PC speaker. The MOUT pin on the CS4231 is a mix of both left and right channels and has an independent software mute. The quality of this circuit is limited to the quality of the speaker used. Much higher fidelity can be achieved by using a higher quality speaker.

Since the CS4248 does not have MIN and MOUT pins, the CDB4248 board does not provide a cable, and the **SPEAKER IN** and **SPEAKER OUT** headers are non-functional.

BASE ADDRESS

The base address is set using header J18 (Figure 6) and must match the software selected base address. The CDB4231/4248 evaluation board uses 8 I/O addresses. The first four are used to read the board ID of 04. Writes to the first four addresses are ignored. The board ID is output from the ID31 PLD and indicates that the board is Windows Sound System, WSS, compatible (see limitations listed in the *SOFTWARE COMPATIBILITY* section).

The second four addresses are used by the codec. The default for the evaluation board and the software is 530h - no jumpers. The following table lists the available base addresses (along with the associated codec address), with a "1" defined as no shorting jumper and a "0" defined as a shorting jumper installed:

X1	X0	Base Address	Codec Address	
1	1	530h	534h	(default)
1	0	604h	608h	
0	1	E80h	E84h	
0	0	F40h	F44h	

INTERRUPT

Although the hardware supports a wide selection of interrupts, software may have limitations in the available options. See the *SOFTWARE COMPATIBILITY* section for more information.

The interrupt is set using header J2, also labeled **INT**, (Figure 7) and must also match the software selected interrupt. The default for the evaluation board and the software is 7.

DMA SELECTION

Although the hardware supports a wide selection of DMA channels for playback and capture, software may have limitations in the available options. See the *SOFTWARE COMPATIBILITY* section for more information.

The CDB4231 contains two headers for DMA selection: one determines the playback channel and the other, if used, determines the capture

channel for full duplex operation. Two shorting jumpers are needed for the selected DMA channel, one for the DRQ and one for the DACK. Header J20, labeled **DMA PLAY**, (Figure 7) is the primary DMA channel used for both playback and capture on the CS4248 or CS4231 in SDC mode, as well as playback on the CS4231 in full-duplex operation.

Half Duplex - Single DMA Channel

The default configuration for the CDB4231 is full duplex. When the evaluation board is configured for half duplex, both jumpers on the **DMA CAPTURE** header J1, (Figure 7) SHOULD BE REMOVED. Otherwise, contention with other system resources may occur.

The CS4248 does not contain the second set of DMA base registers; therefore, it must be operated in half duplex mode. Since only one DMA channel is needed at any particular time, the CS4248 is usually operated in Single DMA Channel, SDC, mode.

If only one DMA channel is available, the CS4231 can be programmed for SDC mode wherein the playback channel, selected on the **DMA PLAY** header is used for both playback and capture. The default setting for the evaluation board for the **DMA PLAY** header DRQ3/DACK3.

Full Duplex - Two DMA Channels

Full duplex is only supported on the CS4231 (MODE 2 operation) which contains independent capture and playback DMA Base registers.

The J1 header, labeled **DMA CAPTURE**, (Figure 7) is used to support simultaneous capture in the CS4231 full-duplex mode. The default for the CDB4231 evaluation board **DMA CAPTURE** header, J1, is DRQ0/DACK0.

To support full-duplex operation, a unique DMA channel from each header must be selected.

SOFTWARE COMPATIBILITY

The CDB4231/4248 comes with two sets of software: diagnostics and Windows 3.1 drivers. The diagnostics will support all hardware jumper settings. The Windows software will support all hardware settings when configured for generic hardware. When the included Windows software (or any software) is configured or designed for 100% Windows Sound System compatibility, limitations in the hardware selections exist.

The CDB4231/4248 evaluation board includes a board ID PLD, ID31, that indicates to software that the board is Windows Sound System, WSS, compatible. This read-only register is located at the first four addresses (the second four are for the codec). This ID will read back 0x04 from the lower six bits. Although the evaluation board is WSS compatible from the codec register perspective, the auto-select hardware of the WSS board is not included. The DMA and IRQ settings must be configured via on-board jumpers. The four base addresses supported by the evaluation board are the same as specified for WSS hardware.

Windows software, such as the included drivers and applets, that check for a WSS board will read the board ID and assume that the auto-select register needs to be loaded. The auto-select register only allows certain combinations which

must be adhered to when using the evaluation board with this software.

Therefore, to run 100% compatible Windows Sound System, WSS, software, the IRQ and DMA selection must be made from the following:

INT: 7 (default)
10
11

Half Duplex: DMA PLAY:
0
1
3 (CDB4248 default)
DMA CAPTURE:
No jumpers (CDB4248 default)

Full Duplex:

PLAY	CAPTURE	
0	1	
1	0	
3	0	(CDB4231 default)

Note in full duplex, only the three combinations listed are allowed with the last combination being the default for the CDB4231. If the software does not support full duplex, remove the jumpers on the **DMA CAPTURE** header, J1 (Figure 7).

The Crystal Windows software provided with the evaluation board can be configured for 100% WSS compatible hardware and will load the Auto-Select register with the proper DMA and IRQ settings. In 100% WSS mode, the Crystal software will not allow improper settings for the DMA and IRQ.

Some hardware, including the CDB4231/4248, allow selection of DMA and IRQ via on-board jumpers. These jumpers allow a wider selection of configuration options since it is not limited by the Auto-Select register options listed above.

The Crystal Windows 3.1 software (version 1.04 and greater) supports a "generic hardware" switch that forces the software to use the DMA and IRQ settings in the SYSTEM.INI file and assume no Auto-Select register exists. With this switch on, all combinations of DMA and IRQ, supported by the hardware, are allowed. To use this option, the SYSTEM.INI file must contain:

```
[CSBusAud]
GenericHardware=On      ; either On or Off
                        ; Off is default
```

This switch is added to the SYSTEM.INI file by the installation software when the "Generic Hardware" option is selected from the Windows Sound System screen.

WSS SOFTWARE COMPATIBILITY

The CS4231/4248 is compatible with Microsoft Windows Sound System software (version 2.0) with respect to wave audio data support. Since the evaluation board does not contain a synthesizer, the MIDI portion of WSS will not function. When installing the Microsoft software, select Custom Installation and set the base address, IRQ, and DMA channel consistent with the evaluation board jumper settings. Since the board does not contain the extra hardware needed for software configuration of the IRQ and DMA channel, the Auto Installation mode of the Microsoft WSS software is not supported.

The Microsoft WSS hardware and software drivers do not use all the analog inputs. The only hardware supported by the Microsoft WSS hardware and software are a mono microphone input (set jumper on J35 to M), and the stereo Line input jack, **Line I.**

SCHEMATICS

The following pages contain the full schematics for the CDB4231/4248, as well as the PLD equations.

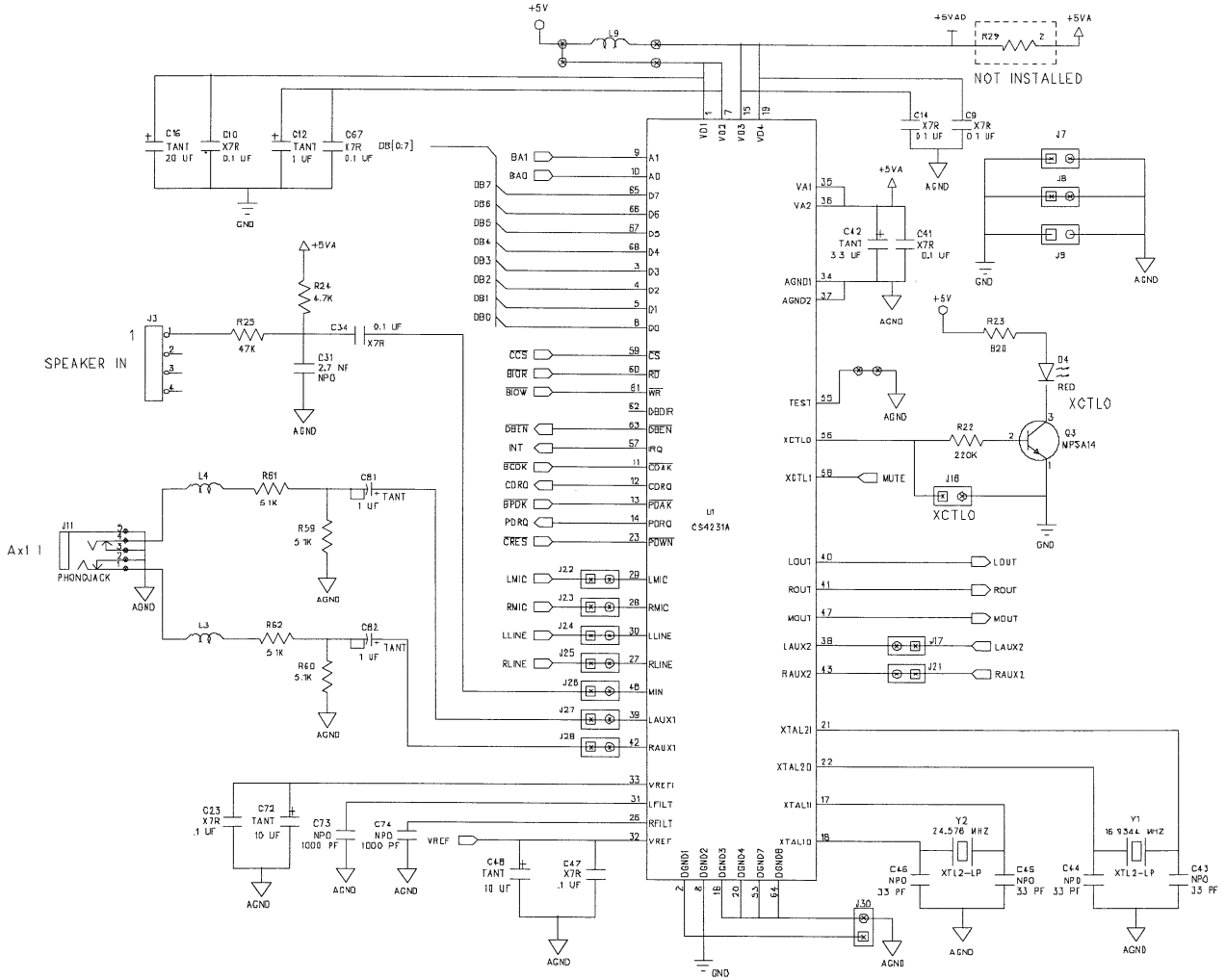


Figure 1. CS4231 & Aux1 In

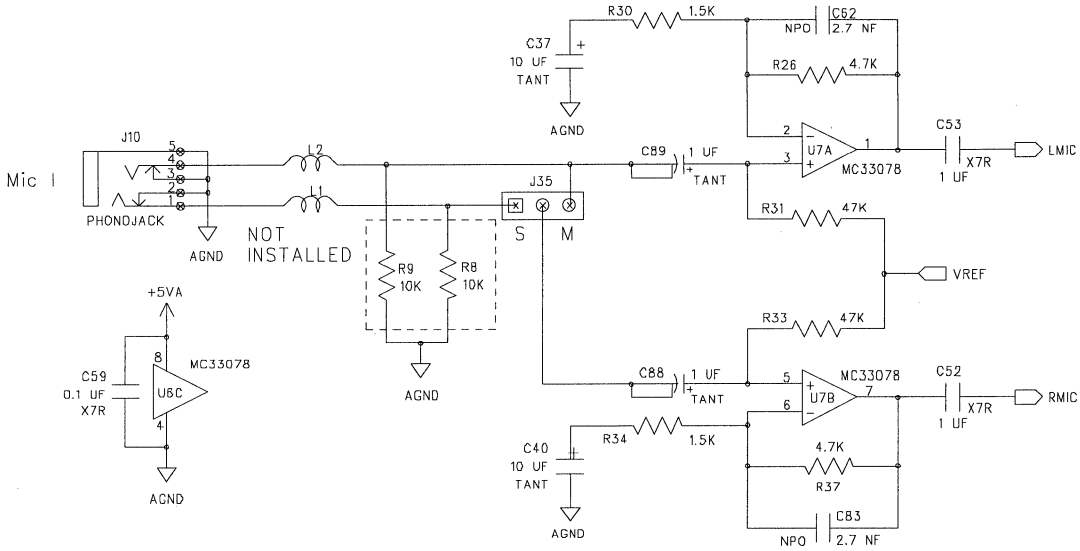


Figure 2. Microphone In

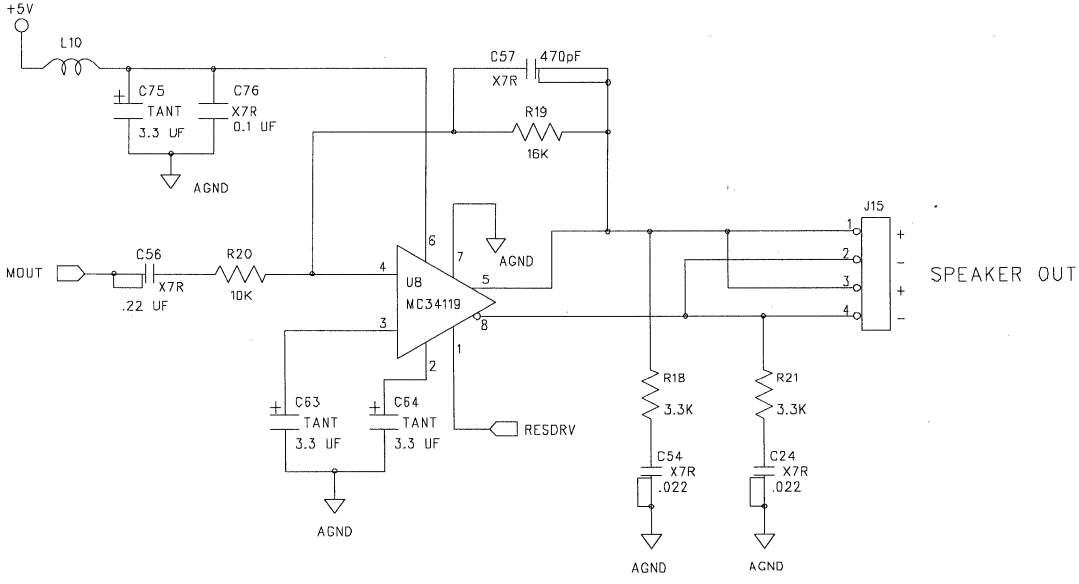


Figure 3. Mono Speaker Out

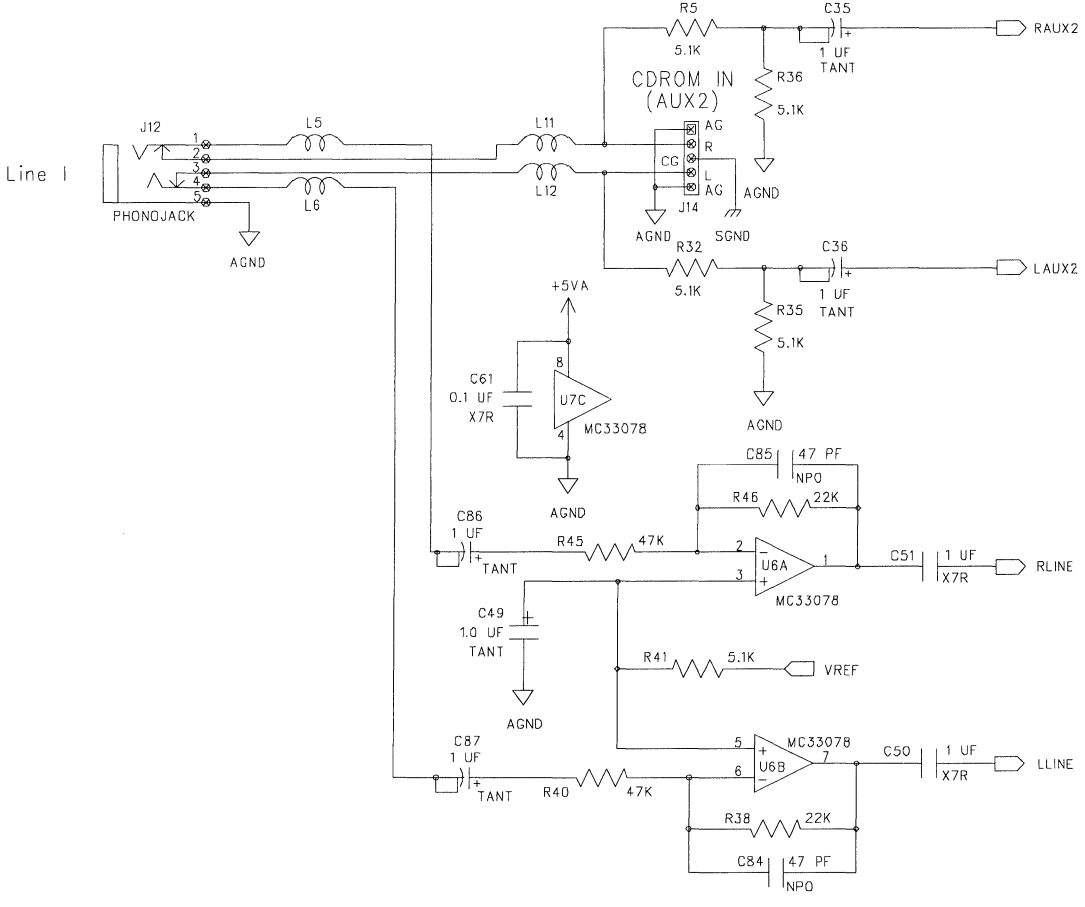


Figure 4. Line In & CDROM In (Aux2)

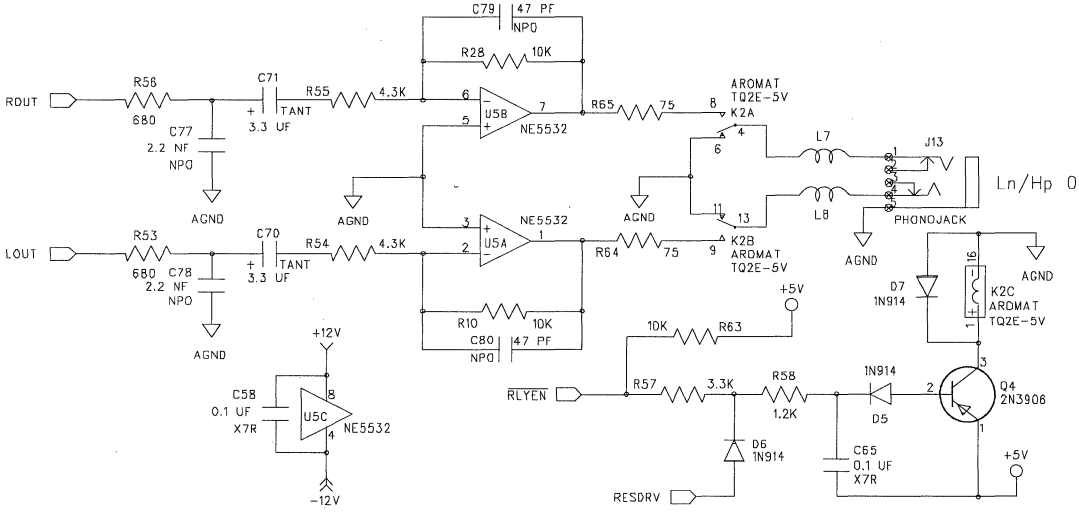


Figure 5. Line/Headphone Out

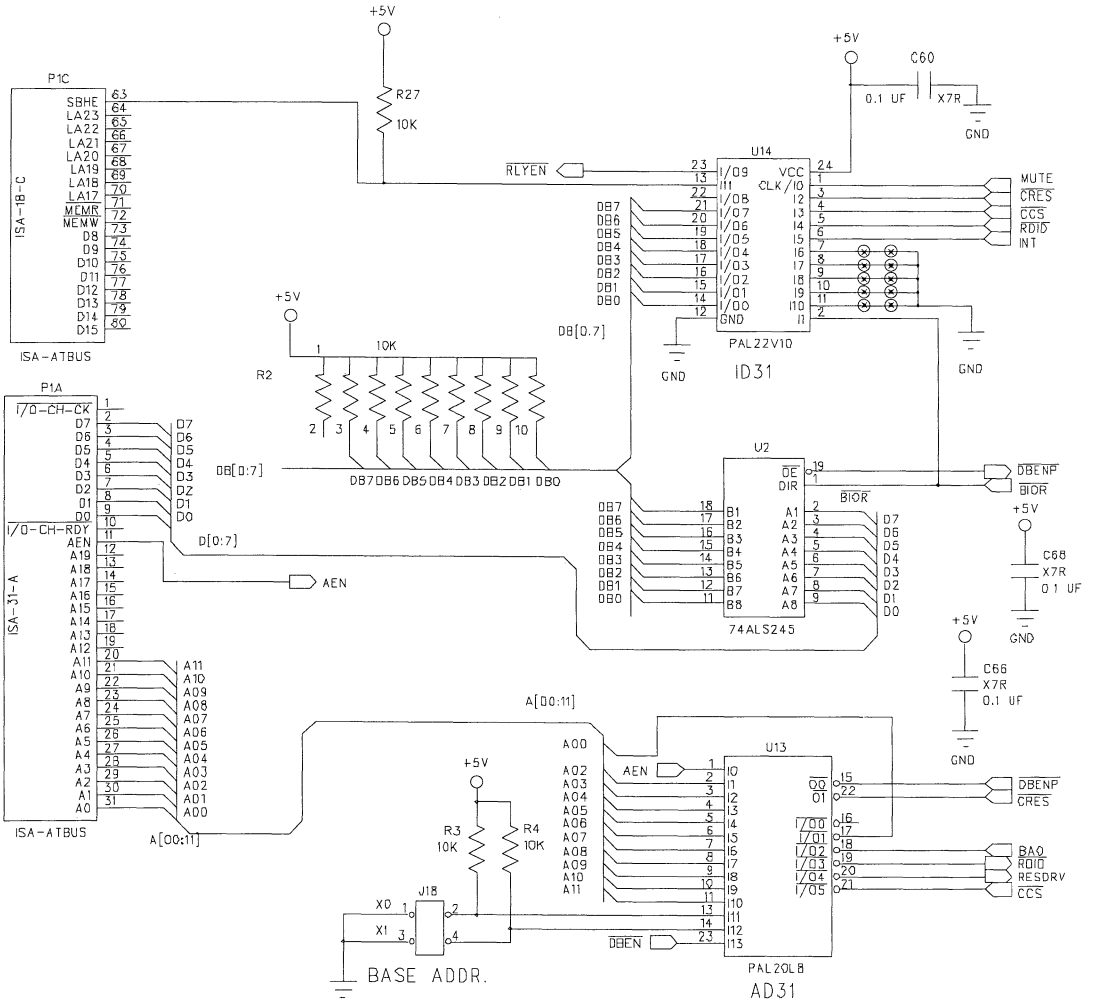


Figure 6. Address Decode and Board ID

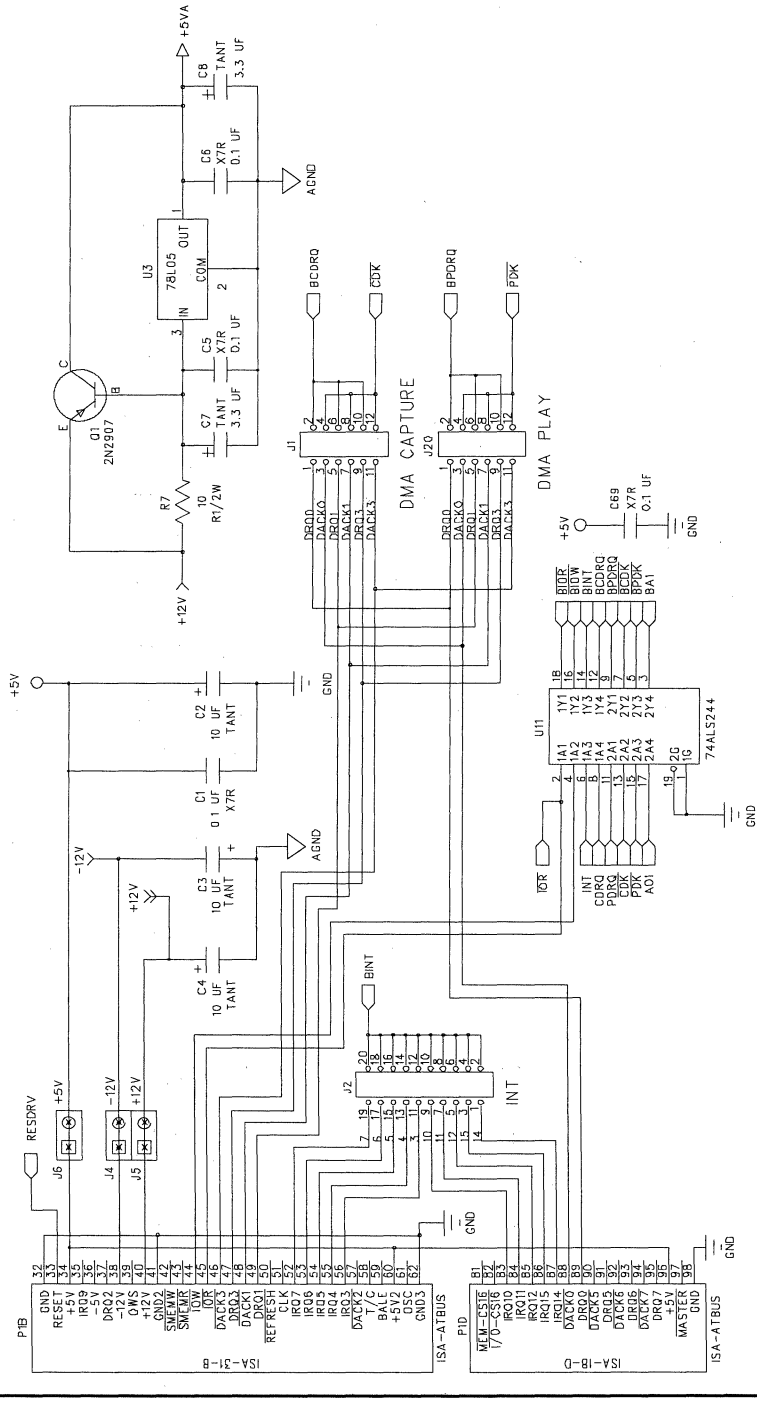


Figure 7. Analog Power & Buffer

```
;PALASM Design Description
; CDB4231 Rev. D
;---------------------------------- Declaration Segment ------------
TITLE     Address Decode for CS4231 and Read ID
PATTERN   AD31.PDS
REVISION  2.0
AUTHOR    Clif Sanchez
COMPANY   Crystal Semiconductor
DATE      10/15/93

CHIP   _AD31   PAL20V8

;---------------------------------- PIN Declarations ---------------
PIN   1            AEN               ; Eight addresses in all.
PIN   2            A2                ; The first four addresses are used by the
PIN   3            A3                ;    board PLD ID31 - address select RDID.
PIN   4            A4                ; The second four addresses are used by the
PIN   5            A5                ;    CS4231/4248.
PIN   6            A6
PIN   7            A7                ; Base Address: X1,X0 (header J18)
PIN   8            A8                ;                   1  1   530-537, codec 534
PIN   9            A9                ;                   1  0   604-60B, codec 608
PIN   10           A10               ;                   0  1   E80-E87, codec E84
PIN   11           A11               ;                   0  0   F40-F47, codec F44

PIN   13           X0                ; I - Address selector X1,X0:
PIN   14           X1                ; I -
PIN   15           /DBENP            ; O - Data Bus Enable Prime for 245 chip
PIN   16           /IOR              ; I - Qualifies Read ID enable
PIN   17           A0                ; I - from bus
PIN   18           BA0               ; O - Buffered A0 (PLD just used for buffer)
PIN   19           /RDID             ; O - Read ID register enable
PIN   20           RESDRV            ; I - Global Reset
PIN   21           /CCS              ; O - Chip Select for Codec
PIN   22           /CRES             ; O - Inverted RESDRV - to codec PWDN pin
PIN   23           /DBEN             ; I - Data Bus Enable from codec

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

/BA0     = /A0

RDID     =  /A11*A10*/A9* A8*/A7*/A6* A5* A4*/A3*/A2*/AEN*IOR* X1* X0 ; 530-533
          + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4*/A3* A2*/AEN*IOR* X1*/X0 ; 604-607
          +  A11*A10* A9*/A8* A7*/A6*/A5*/A4*/A3*/A2*/AEN*IOR*/X1* X0 ; E80-E83
          +  A11*A10* A9* A8*/A7* A6*/A5*/A4*/A3*/A2*/AEN*IOR*/X1*/X0 ; F40-F43

CCS      =  /A11*A10*/A9* A8*/A7*/A6* A5* A4*/A3* A2*/AEN* X1* X0 ; 534-537
          + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4* A3*/A2*/AEN* X1*/X0 ; 608-60B
          +  A11*A10* A9*/A8* A7*/A6*/A5*/A4*/A3* A2*/AEN*/X1* X0 ; E84-E87
          +  A11*A10* A9* A8*/A7* A6*/A5*/A4*/A3* A2*/AEN*/X1*/X0 ; F44-F47

DBENP    = DBEN
          + /A11*A10*/A9* A8*/A7*/A6* A5* A4*/A3*     /AEN* X1* X0 ; 530-537
          + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4*/A3* A2*/AEN* X1*/X0 ; 604-607
          + /A11*A10* A9*/A8*/A7*/A6*/A5*/A4* A3*/A2*/AEN* X1*/X0 ; 608-60B
          +  A11*A10* A9*/A8* A7*/A6*/A5*/A4*/A3*     /AEN*/X1* X0 ; E80-E87
          +  A11*A10* A9* A8*/A7* A6*/A5*/A4*/A3*     /AEN*/X1*/X0 ; F40-F47


CRES     = RESDRV
```

PLD AD31

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE     Read ID + relay enable
PATTERN   ID31.PDS
REVISION  2.0
AUTHOR    Clif Sanchez
COMPANY   Crystal Semiconductor
DATE      10/28/93

CHIP   _ID31   PAL22V10

;---------------------------------- PIN Declarations ---------------
PIN   1            MUTE              ; I - from Codec XCTL1 pin, Software Mute
PIN   2            /BIOR             ; I - buffered /IOR from 244
PIN   3            /CRES             ; I - inverted RESDRV from the AD31 PLD
PIN   4            /CCS              ; I - codec chip select, used for ACCESS
PIN   5            /RDID             ; I - Read ID chip select, from the AD31 PLD
PIN   6            INT
PIN   7            NC
PIN   8            NC
PIN   9            NC
PIN   10           NC
PIN   11           NC

PIN   13           SBHE              ; I
PIN   14           D0                ; O - Data Bus, Enabled for /RDID
PIN   15           D1                ; O   Places Read on the data bus
PIN   16           D2                ; O
PIN   17           D3                ; O
PIN   18           D4                ; O
PIN   19           D5                ; O
PIN   20           D6                ; O
PIN   21           D7                ; O
PIN   22           ACCESS            ; O - True after first read of the codec
PIN   23           /RLYEN            ; O - Relay Enable
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

D0 = GND
D0.TRST = RDID

D1 = GND
D1.TRST = RDID

D2 = VCC
D2.TRST = RDID

D3 = GND
D3.TRST = RDID

D4 = GND
D4.TRST = RDID

D5 = GND
D5.TRST = RDID

D6 = /INT
D6.TRST = RDID

D7 = SBHE
D7.TRST = RDID

ACCESS   = ACCESS * /CRES
         + CCS * BIOR * /CRES

RLYEN = ACCESS * /MUTE
```

PLD ID31

CRYSTAL
Semiconductor Corporation

CS4248

Parallel Interface, Multimedia Audio Codec

Features

- Integrated parallel interface to ISA and EISA buses
- Stereo Digital Audio at sample rates from 4 kHz to 50 kHz with 16-bit resolution.
- DMA Transfers with on-chip FIFOs
- Free Window™ Software Drivers
- Linear, μ-law, and A-law coding
- Pin compatible with the AD1848 (PLCC)

General Description

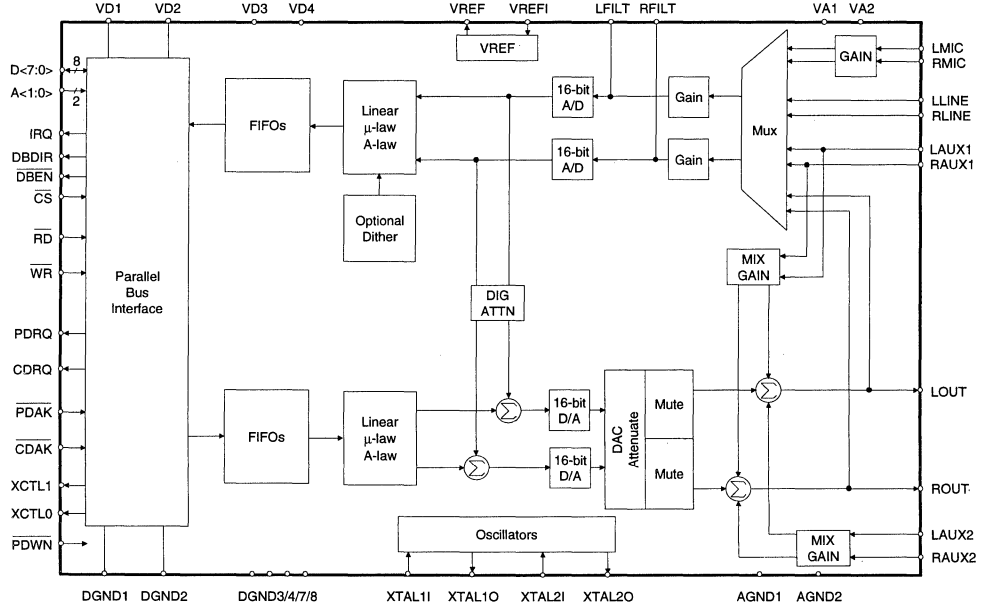
mwave The CS4248 is an Mwave™ audio codec.

The CS4248 is a mixed signal integrated circuit that provides 16-bit audio for computer multimedia systems. The CS4248 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data. The CS4248 combines conversion, analog mixing, and programmable gain and attenuation to provide a complete audio subsystem in a single 68-pin PLCC or 100-pin TQFP package. The CS4248 includes an 8-bit parallel interface to the industry standard ISA bus.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS4248-KL	0 to 70° C	68 pin PLCC
CS4248-KQ	0 to 70° C	100 pin TQFP

4



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS(T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine wave; Conversion Rate = 48 kHz; Measurement Bandwidth is 10 Hz to 20 kHz, 16-bit linear coding.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution	(Note 1)		16	-	-	Bits
ADC Differential Nonlinearity	(Note 1)		-	-	±0.5	LSB
Instantaneous Dynamic Range	Line Inputs (Note 2) Mic Inputs	IDR	80 72	85 77	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	0.02 0.025	0.003 0.01	- -	% %
Signal-to-Intermodulation Distortion			-	90	-	dB
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs Line-to-AUX1 Line-to-AUX2		- - - -	80 80 90 90	- - - -	dB dB dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5	-	dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain		-	10	100	LSB
Gain Error			-	-	5	%
Full Scale Input Voltage:	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2 Inputs		0.266 2.66 2.66	0.29 2.9 2.9	0.31 3.1 3.1	V_{pp} V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 1)		20	-	-	kΩ
Input Capacitance	(Note 1)		-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, not production testing.
2. MGE = 1 and a 10µF capacitor on the VREF pin.

* Parameter definitions are given at the end of this data sheet.

Mwave is a registered trademark of IBM Corporation.

Windows is a registered trademark of Microsoft Corporation.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0 dB); Unless Otherwise Specified.							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity		(Note 1)		-	-	±0.5	LSB
Dynamic Range	- Total - Instantaneous	All Outputs	TDR IDR	- 80	95 85	- -	dB dB
Total Harmonic Distortion		(Note 4)	THD	0.02	0.01	-	%
Signal-to-Intermodulation Distortion				-	85	-	dB
Interchannel Isolation	Line Out	(Note 4)		-	95	-	dB
Interchannel Gain Mismatch		Line Out		-	0.1	0.5	dB
Voltage Reference Output				2.0	2.15	2.3	V
Voltage Reference Output Current		(Note 3)		-	100	-	µA
DAC Programmable Attenuation Span				93	94.5	-	dB
DAC Attenuation Step Size		0 dB to -81 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC Offset Voltage				-	1	10	mV
Full Scale Output Voltage		(Notes 4, 5)		1.85	2.0	2.25	V_{pp}
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase		(Note 1)		-	-	1	Degree
External Load Impedance				10	-	-	kΩ
Mute Attenuation (0 dB)				80	-	-	dB
Total Out-of-Band Energy	(Note 1)	0.6xFs to 3 MHz		-	-	-45	dB
Audible Out-of-Band Energy	(Fs = 8kHz)	0.6xFs to 22 kHz		-	-	-60	dB
Power Supply							
Power Supply Current		Digital, Operating Analog, Operating Total Digital, Power Down Analog, Power Down		- - - - -	55 43 98 - -	65 60 120 1 1	mA mA mA mA mA
Power Supply Rejection	1kHz	(Note 1)		40	-	-	dB

Notes: 3. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.
4. 10 kΩ, 100 pF load.
5. The output level full-scale value is 3 dB below the input full-scale value. This attenuation is not taken into account in the mixer gain tables which show gain internal to the mixer.

AUXILIARY INPUT MIXERS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine Wave)

Parameter			Symbol	Min	Typ	Max	Units
Mixer Gain Range Span	AUX1, AUX2	(Note 6)		45	46.5	-	dB
Step Size	AUX1, AUX2			1.3	1.5	1.7	dB

Note: 6. An addition 3 dB attenuation must be included when comparing the output value to the input value since the analog output full-scale value is 3 dB lower than the analog input full-scale value.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital	VD1-VD4	-0.3	6.0	V
	Analog	VA1,VA2	-0.3	6.0	V
Input Current Per Pin	(Except Supply Pins)		-10	10	mA
Output Current Per Pin	(Except Supply Pins)		-50	50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage			-0.3	VD+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD1-VD4	4.75	5.0	5.25	V
	Analog	VA1,VA2	4.75	5.0	5.25	V
Operating Ambient Temperature		T_A	0	25	70	°C

DIGITAL FILTER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Passband			0	-	0.40×Fs	Hz
Frequency Response			-0.5	-	+ 0.2	dB
Passband Ripple	(0-0.4×Fs)		-	-	±0.1	dB
Transition Band			0.40×Fs	-	0.60×Fs	Hz
Stop Band			0.60×Fs	-	-	Hz
Stop Band Rejection			74	-	-	dB
Group Delay			-	-	30/Fs	s
Group Delay Variation vs. Frequency	ADCs DACs		- -	- -	0.0 0.1/Fs	µs µs

4

DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = 5V; AGND1, AGND2, DGND1-DGND4, DGND7, DGND8 = 0V.)

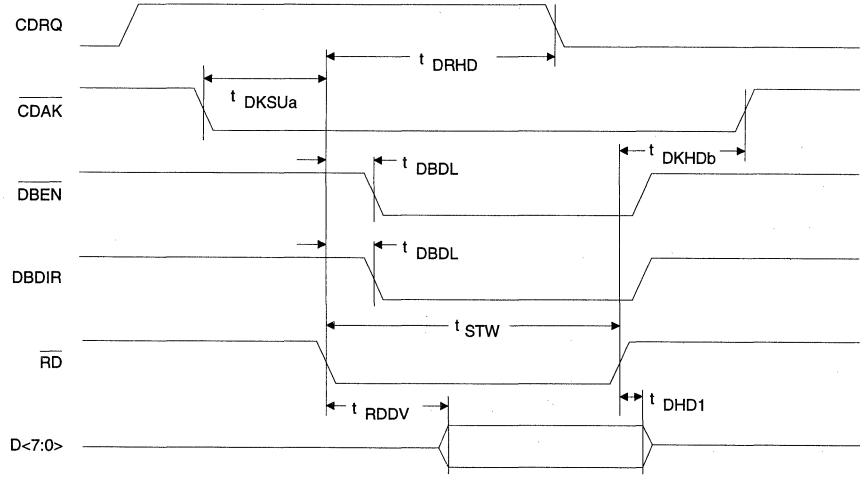
Parameter			Symbol	Min	Max	Units
High-level Input Voltage		Digital Inputs XTAL1I/XTAL2I, PDWN	V_{IH}	2.0 VD-1.0	VD+ 0.3 VD+ 0.3	V V
Low-level Input Voltage			V_{IL}	-0.3	0.8	V
High-level Output Voltage:	D<7:0> All Others	I_O = -16.0 mA I_O = -1.0 mA	V_{OH}	2.4 2.4	VD VD	V V
Low-level Output Voltage:	D<7:0> All Others	I_O = 16.0 mA I_O = 4.0 mA	V_{OL}	- -	0.4 0.4	V V
Input Leakage Current		(Digital Inputs)	-	-10	10	µA
Output Leakage Current		(High-Z Digital Outputs)	-	-10	10	µA

TIMING PARAMETERS

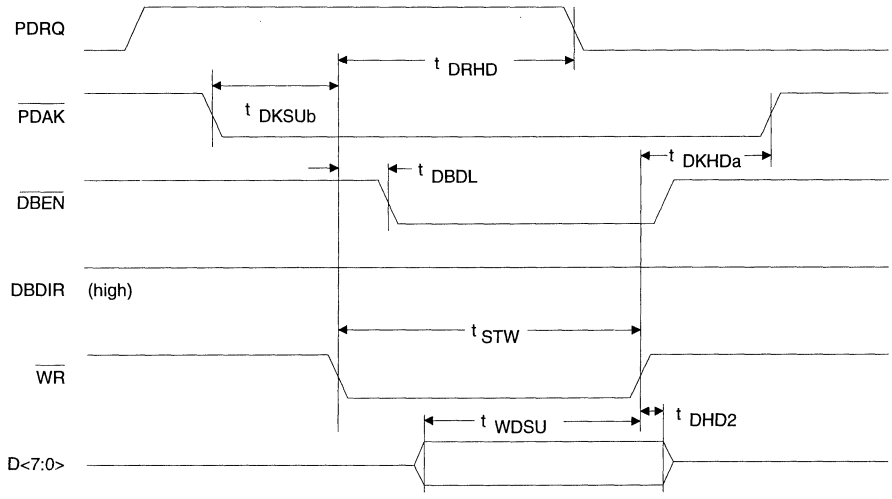
Parameter	Description		Min	Max	Units
t_{STW}	$\overline{WR}$ or $\overline{RD}$ strobe width		90	-	ns
t_{WDSU}	Data valid to $\overline{WR}$ rising edge	(write cycle)	22	-	ns
t_{RDDV}	$\overline{RD}$ falling edge to data valid	(read cycle)	-	60	ns
t_{CSSU}	$\overline{CS}$ setup to $\overline{WR}$ or $\overline{RD}$ falling edge		10	-	ns
t_{CSHD}	$\overline{CS}$ hold from $\overline{WR}$ or $\overline{RD}$ rising edge		0	-	ns
t_{ADSU}	ADDR <> setup to $\overline{RD}$ or $\overline{WR}$ falling edge		22	-	ns
t_{ADHD}	ADDR <> hold from $\overline{WR}$ or $\overline{RD}$ rising edge		10	-	ns

TIMING PARAMETERS (continued)

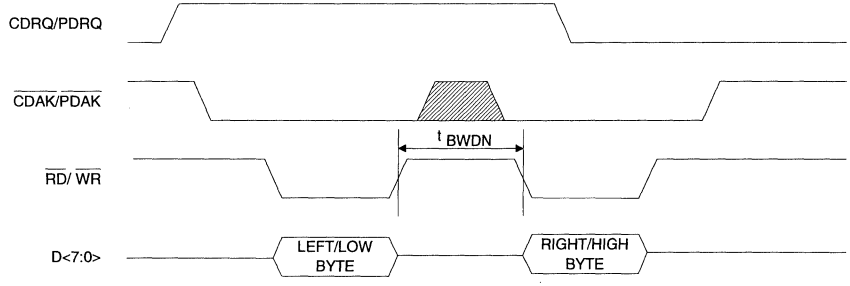
Parameter	Description	Min	Max	Units
t_{SUDK1}	$\overline{DAK}$ inactive to $\overline{WR}$ or $\overline{RD}$ falling edge (DMA cycle completion immediately followed by a PIO cycle)	60	-	ns
t_{SUDK2}	$\overline{DAK}$ active from $\overline{WR}$ or $\overline{RD}$ rising edge (PIO cycle completion immediately followed by DMA cycle)	0	-	ns
t_{DKSUa} t_{DKSUb}	$\overline{DAK}$ setup to $\overline{RD}$ falling edge (DMA cycles) $\overline{DAK}$ setup to $\overline{WR}$ falling edge	25 25	- -	ns ns
t_{DHD2}	Data hold from $\overline{WR}$ rising edge	15	-	ns
t_{DRHD}	DRQ hold from $\overline{WR}$ or $\overline{RD}$ falling edge (assumes no more DMA cycles needed)	0	25	ns
t_{BWDN}	Time between rising edge of $\overline{WR}$ or $\overline{RD}$ to next falling edge of $\overline{WR}$ or $\overline{RD}$	80	-	ns
t_{DHD1}	Data hold from $\overline{RD}$ rising edge	0	20	ns
t_{DKHDa} t_{DKHDb}	$\overline{DAK}$ hold from $\overline{WR}$ rising edge $\overline{DAK}$ hold from $\overline{RD}$ rising edge	25 25	- -	ns ns
t_{DBDL}	$\overline{DBEN}$ or $\overline{DBDIR}$ active from $\overline{WR}$ or $\overline{RD}$ falling edge		40	ns
t_{PDWN}	$\overline{PDWN}$ pulse width low	200	-	ns



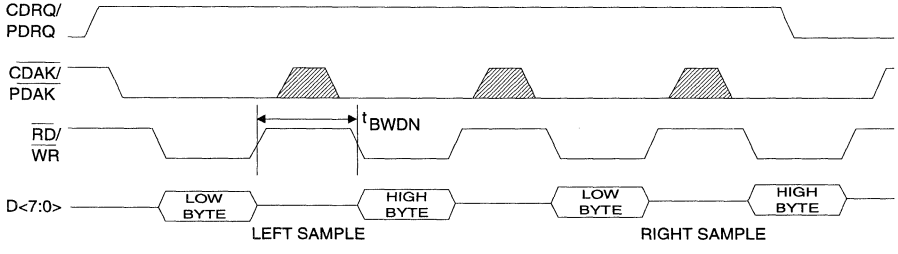
8-Bit Mono DMA Read/Capture Cycle



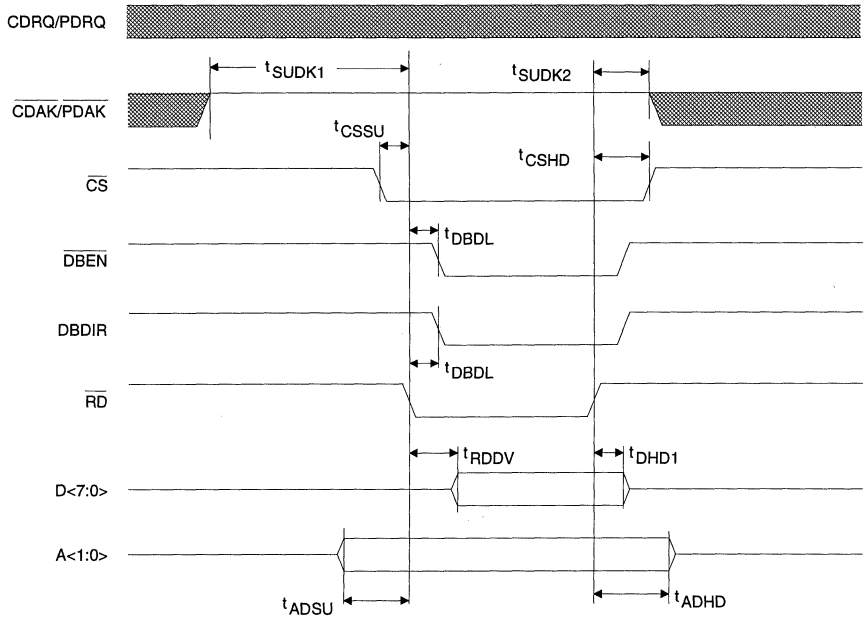
8-Bit Mono DMA Write/Playback Cycle



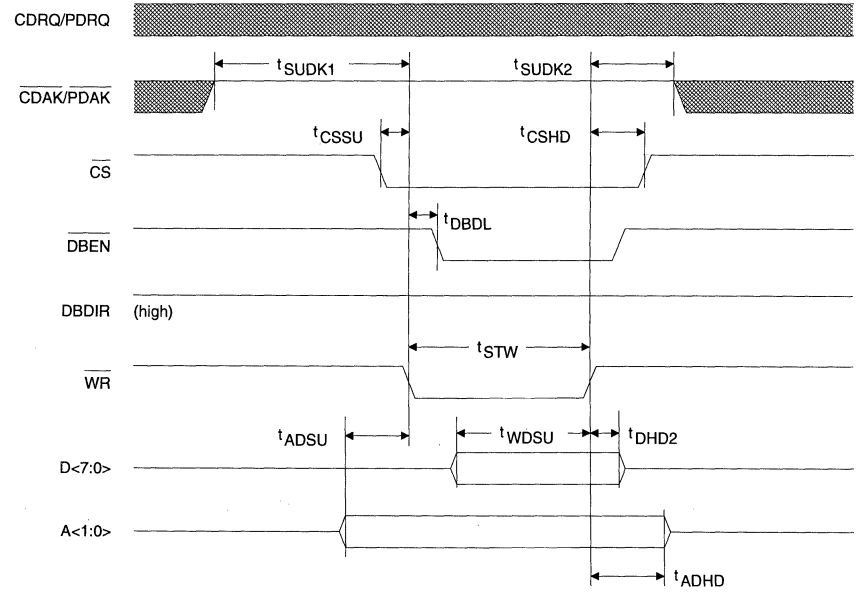
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo DMA Cycle



I/O Read Cycle



I/O Write Cycle

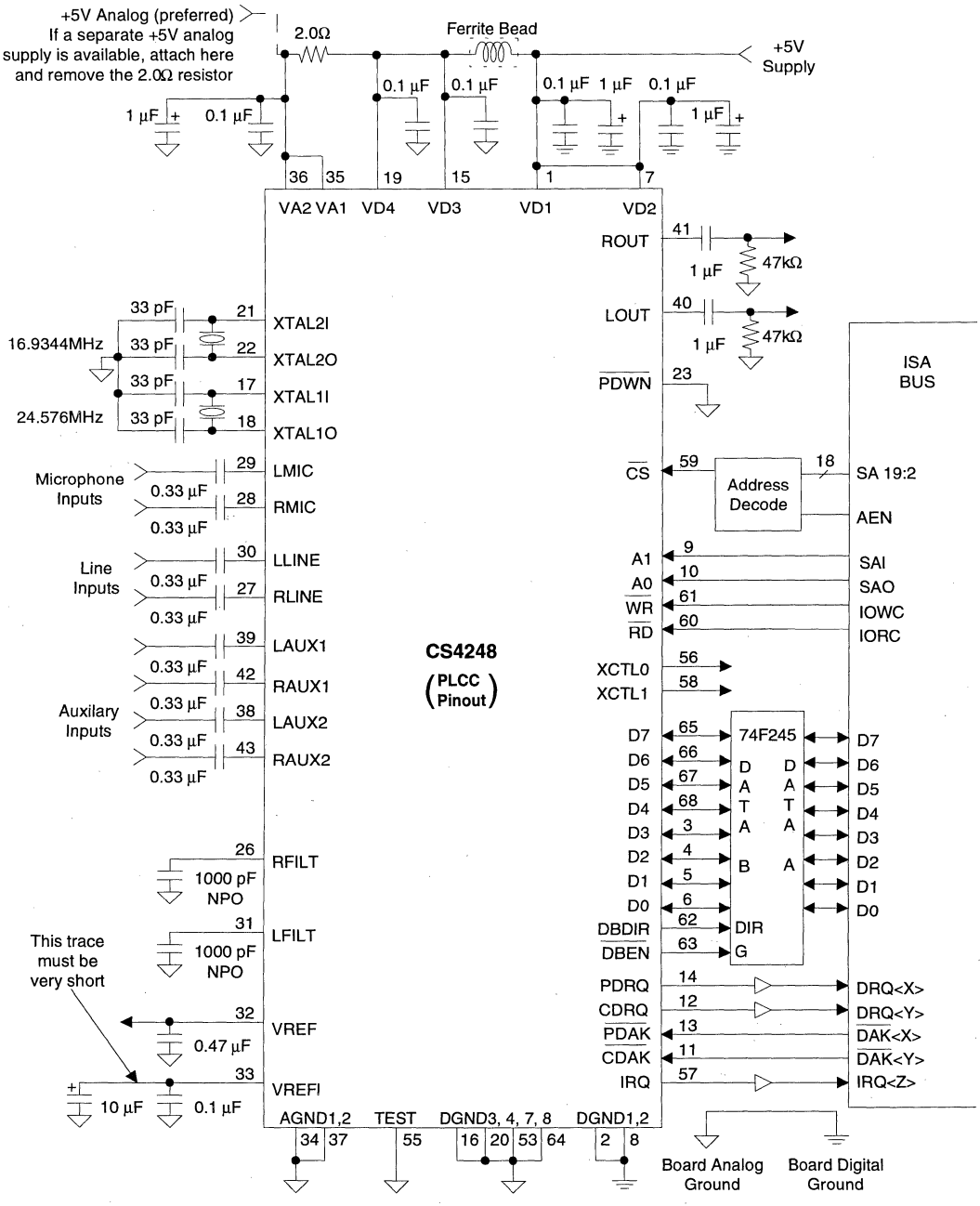


Figure 1. Recommended Connection Diagram
(See also Figures 9 & 10 for Layout Recommendations)

GENERAL DESCRIPTION

The CS4248 is a monolithic integrated circuit that provides audio in personal computers or other parallel interface environments. The functions include stereo Analog-to-Digital and Digital-to-Analog Converters (ADC and DAC), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, selectable A-law / μ-law coding, and a parallel bus interface. Three stereo analog inputs, LINE, MIC, and AUX1, are provided and can be multiplexed to the ADC. AUX1 can be mixed with the output of the DAC along with an additional auxiliary input (AUX2). The only external filtering required is two capacitors. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded. The CS4248 is packaged in a 68-pin PLCC or a 100-pin TQFP.

A number of innovative design techniques are used to minimize audible noise from external sources, data handling errors and during normal operating changes such as volume control. In the event that a data error does occur, the CS4248 provides smooth error masking and eliminates pops and clicks.

FUNCTIONAL DESCRIPTION

Parallel Data Interface

The 8-bit parallel port of the CS4248 provides an interface which is compatible with most computer peripheral busses. The model for this interface is the Industry Standard Architecture (ISA) bus, but the CS4248 will easily interface to other buses such as EISA and micro channel. Two types of accesses can occur via the parallel interface; Programmed I/O (PIO) access, and DMA access.

There is no provision for the CS4248 to "hold off" or extend a cycle occurring on the parallel interface. Therefore, the internal architecture of the CS4248 accepts asynchronous parallel bus cycles without interfering with the flow of data to or from the ADC and DAC sections.

Control Registers Interface

The first I/O cycle access is to the control registers of the CS4248. Timing diagrams are given to show the timing of control register cycles. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the read and write cycles respectively. The control register cycle is defined by the assertion of the CS4248 $\overline{CS}$ signal while the DMA acknowledge signals, $\overline{CDAK}$ and $\overline{PDAK}$, are inactive. For read cycles, the CS4248 will drive data on the DATA lines while the host asserts the $\overline{RD}$ strobe. Write cycles require the host to assert data on the DATA lines and strobe the $\overline{WR}$ signal. The CS4248 will latch data into the control register on the rising edge of the $\overline{WR}$ strobe. The CS4248 $\overline{CS}$ signal should remain active until after completion of the read or write cycle. PIO cycles (non-DMA) are the only type which access the Control Registers.

The data interface typically uses DMA request/grant pins to transfer the digital audio data between the CS4248 and the bus. The CS4248 is responsible for asserting a request signal whenever the CS4248's internal buffers need updating. The logic interfaced with the CS4248 responds with an acknowledge signal and strobes data to and from the CS4248, 8 bits at a time. The CS4248 keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Notice that different audio data types will require a different number of 8-bit transfers.

DMA Interfaces

The second type of parallel bus cycle on the CS4248 is a DMA transfer. DMA cycles are distinguished from control register cycles by the assertion by the CS4248 of a CDRQ (or PDRQ)

followed by an acknowledgment by the host by the assertion of $\overline{CDAK}$ (or $\overline{PDAK}$). While the acknowledgment is received from the host, the CS4248 assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines and the $\overline{CS}$ line.

The CS4248 may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a DMA cycle occurs to the CS4248. Once the falling edge of the final $\overline{WR}$ or $\overline{RD}$ strobe of a full sample of a DMA cycle occurs, the DMA request signal is deasserted immediately. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration Register, depending on the DMA that is in progress (Playback, Capture, or Both). Termination of DMA transfers may only happen between sample transfers on the bus. If PDRQ and/or CDRQ goes active while resetting PEN and/or CEN, the request must be acknowledged ($\overline{PDAK}$ and/or $\overline{CDAK}$) and a final sample transfer completed. The CS4248 supports one or two DMA channels.

Dual Channel DMA Mode

In dual-channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In this mode, capture and playback are enabled and set for DMA transfers. In addition, the SDC bit must be set to zero. The playback and capture enables can be changed without a mode change enable. This allows proper control where applications are independently using playback and capture. Simultaneous capture and playback is not plausible.

Single Channel DMA (SDC) Mode

SDC mode is designed to allow the CS4248 to be used in a computer where two dedicated DMA channels for audio are not available. SDC forces all DMA transfers (capture or playback) to occur on a single DMA channel (the playback channel).

To enable the SDC mode, set the SDC bit (Index 9) to one in the Interface Configuration register. With the SDC bit asserted, the internal workings of the CS4248 remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation. However, the capture audio channel is now diverted to the playback channel. This means that the capture DMA request occurs on the PDRQ pin and the $\overline{PDAK}$ pin is used to acknowledge the capture request. Simultaneous DMA capture and playback is not plausible. If both playback and capture are enabled, the default will be playback.

In SDC mode, the CDRQ pin is logic low (inactive). The $\overline{CDAK}$ pin is ignored by the CS4248. SDC does not have any affect when using Programmed I/O mode.

Interrupt

Interrupts are generated under control of the Current Count register. The Current Count register is not accessible by the host, but is loaded when a write occurs to the upper byte of the Base Count Register. Note that the Base Count registers should be loaded with the buffer size minus one. The Current Count Register decrements on every sample period. Once the Current Count register reaches zero, an interrupt is generated on the next sample.

The INT bit of this Status Register always reflects the status of the CS4248 internal interrupt state. A roll-over from Current Count register sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register.

The Interrupt Enable (IEN) bit in the Pin Control register determines whether the interrupt pin responds to the interrupt event in the CS4248. When the IEN bit has the interrupt disabled, the IRQ pin of the CS4248 is forced low and does not change. However, the INT bit of the status register always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the CS4248 in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the CS4248.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

Noise Management

The CS4248 includes circuitry for noise management resulting from power up and down transients. No audible clicks and pops occur due to power up and down transients or when entering power down mode.

Analog Input Interface

The analog input interface is designed to accommodate four stereo input sources. Three of these sources are multiplexed to the ADC. These inputs are: the stereo line level input, the microphone input, and an auxiliary line level input (AUX1). AUX1 and AUX2 can be analog mixed with the DAC outputs. All audio inputs should be capacitively coupled to the CS4248.

Microphone Level Inputs

The CS4248 includes an selectable +20 dB gain stage for interfacing to an external microphone. Figure 2 shows an example microphone input buffer circuit.

Analog Output Interface

The analog output section of the CS4248 provides a stereo line level output. The other output types (headphone and speaker) are implemented with external circuitry. Left and Right outputs should be capacitively coupled to external circuitry.

Miscellaneous Signals

Four pins have been allocated to allow the interfacing of two crystal oscillator circuits to the CS4248. These pins are XTAL1I, XTAL1O, XTAL2I, AND XTAL2O.

A $\overline{\text{PDWN}}$ signal places the CS4248 into maximum power conservation mode. A 2.1 V reference pin is provided to maintain an audio reference level for single supply input and output audio signals; however, this reference is not maintained in power-down mode.

The $\overline{\text{DBEN}}$ and DBDIR pins are used to control an external data buffer to the CS4248. The CS4248 is capable of driving a 16 mA bus load. Data bus loading requirements greater than 16 mA will require an external buffer. $\overline{\text{DBEN}}$ enables the external drivers and DBDIR controls the direction of the data flow.

CONTROL REGISTER DEFINITION

The two address pins of the CS4248 allow access to four 8-bit registers. Two of these registers allow indirect accessing to more CS4248 registers via an index and data register. The other two registers provide status information and allow direct access to the CS4248's digital audio data without the need to perform DMA cycles.

Changing Transfer Modes

The CS4248 must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register or the Data Format register are allowed. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes to these bits. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register and can be used to monitor the record path during a capture sequence. This loopback routes the digital data from the ADCs to the DACs. This loopback can be digitally attenuated via additional bits in the Loopback Control register. Loopback is then summed with DAC data supplied at the digital bus interface. When loopback is enabled, it will "freerun" synchronous with the sample rate. The digital loopback is shown in the CS4248 block diagram on the front page of this data sheet.

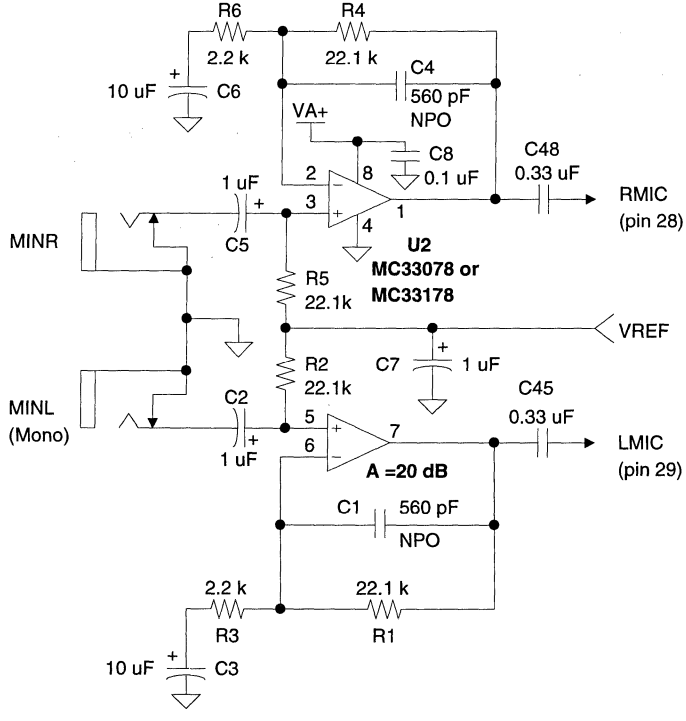


Figure 2. Optional Microphone Input Buffer.

If the sum of the loopback and bus data are greater than full scale, CS4248 will send a + or - full scale value to the DACs whichever is appropriate. (Clipping)

INITIALIZATION AND PROCEDURES

Reset and Power down

Reset and power down modes are controlled by the $\overline{\text{PDWN}}$ pin. To put the CS4248 into a power down mode, the $\overline{\text{PDWN}}$ pin is pulled low. In this state the host interface is inactive and all digital and analog circuits are turned off.

To let the CS4248 go through its reset initialization the $\overline{\text{PDWN}}$ pin should be set high. This rising edge starts the initialization process. While the CS4248 is initializing, all reads by the host computer will receive a 80 hex. All writes during initialization of the CS4248 will be ignored. At the end of the initialization, all registers are set to known values as documented in the register definition section.

Auto Calibration

The CS4248 has the ability to calibrate the ADCs and DACs. Auto-calibration is initiated when MCE goes from 1 to 0 with the ACAL bit in the Interface Configuration register set.

The completion of calibration can be determined by polling the Auto-calibrate In-Progress (ACI) bit in the Test and Initialization register. This bit will be high while the calibration is in progress and low once completed. The calibration sequence will take at least 128 sample periods. Transfers enabled during calibration will not begin until calibration has completed.

The calibration procedure is as follows:

1) Place the CS4248 in Mode Change Enable using the MCE bit of the Index register.

2) Set the ACAL bit in the Interface Configuration register.

3) Return from Mode Change Enable by resetting the MCE bit of the Index register.

4) Poll the ACI bit in the Test and Initialization register for a one (active) then poll for a zero (complete).

Changing Sampling Rate

The internal states of the CS4248 are synchronized by the selected sampling frequency defined in the Data Format register. If only one crystal is provided in hardware, it must be XTAL1. The changing of the clock source requires a special sequence for proper CS4248 operation.

1) Mute the outputs of the CS4248 and place it in Mode Change Enable using the MCE bit of the Index register.

2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock Source Select (CSL) bits of the Data Format register to the desired values.

3) The CS4248 resynchronizes its internal states to the new clock. During this time the CS4248 will be unable to respond at its parallel interface. Writes to the CS4248 will not be recognized and reads will always return the value 80 hex.

4) The host now polls the CS4248's Index register until the value 80 hex is no longer returned.

5) Once the CS4248 is no longer responding to reads with a value of 80 hex, normal operation can resume and the CS4248 can be removed from MCE.

6) If ACAL is set, proceed with Auto Calibration steps previously mentioned.

The CSL and CFS[2..0] bits cannot be changed unless the MCE bit has been set. Attempts to change the Data Format register or Interface Configuration register without MCE set, will not be recognized.

DATA STREAM DEFINITION

The CS4248 is designed for data formats which are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The CS4248 always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size. See Figures 3 through 6.

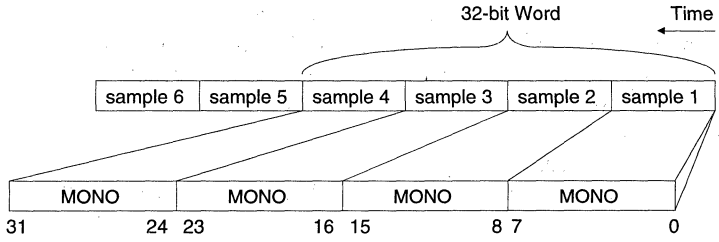


Figure 3. 8-bit Mono, Data Stream Definition.

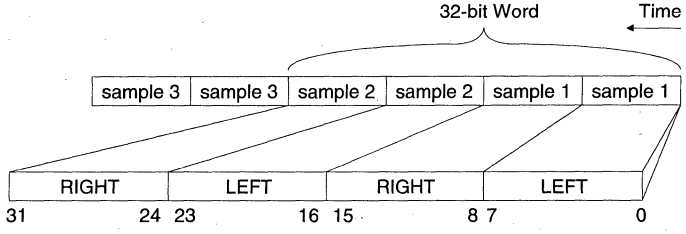


Figure 4. 8-bit Stereo, Data Stream Definition.

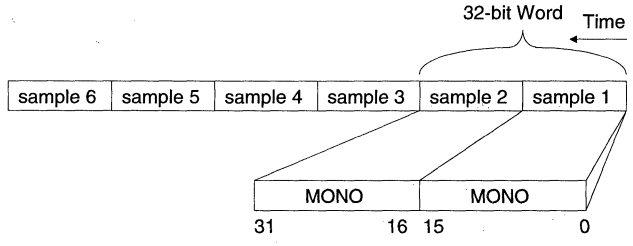


Figure 5. 16-bit Mono, Data Stream Definition.

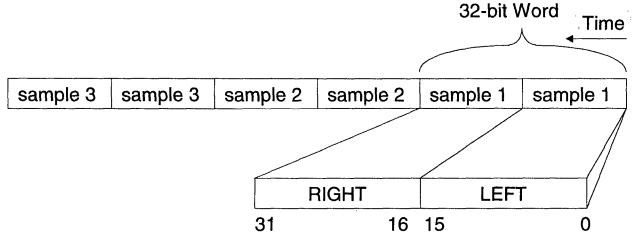


Figure 6. 16-bit Stereo, Data Stream Definition.

Data Format Definition

There are four data formats supported by the CS4248: 16-bit signed, 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law.

16-bit Signed

The 16-bit signed format (also called 16-bit two's-complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent minimum analog amplitude while 32767 (7FFFh) represents maximum analog amplitude.

8-bit Unsigned

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent minimum analog amplitude while 255 (FFh) represents maximum analog amplitude. 16-bit signed and 8-bit unsigned formats are shown in Figure 7. When using A/D converters of higher resolution (16-bits) to generate 8-bit values, truncating can produce correlated noise artifacts which can be disturbing to the listener. Once the data is truncated to 8 bits, it is impossible to remove these artifacts. The CS4248 contains an optional dither bit in indirect register 10. When the dither bit is set, a triangular pdf dither is added to the internal 16-bit ADC before truncating to the 8-bit value. Dither is only used for the ADCs when the 8-bit unsigned data format is selected. This dither removes the correlation between the noise and the signal with a slight increase in the noise floor.

8-bit Companded

The 8-bit companded formats (A-law and μ-law) come from the telephone industry. μ-law is the standard for the United States/Japan while A-law is used in Europe. Companded audio allows either 64 dB or 72 dB of dynamic range using only 8 bits per sample. This is accomplished using a non-linear companding which assigns more digital codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The μ-law and A-law formats of the CS4248 conform to the CCITT G.711 specifications. Figure 8 is a diagram of approximately how both A- and μ-law behave. Please refer to the standard mentioned above for an exact definition.

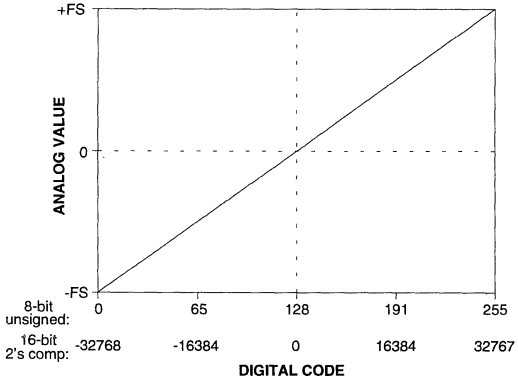


Figure 7. 16-bit Signed, 8-bit Unsigned Formats.

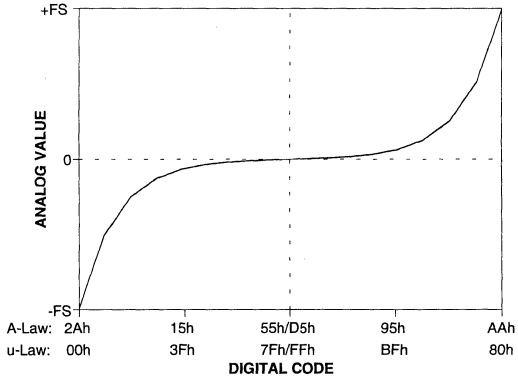


Figure 8. 8-bit A-Law, μ-Law Formats.

CS4248 REGISTER MAPPING

Addr.	Register Name
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Register

Table 1. Direct Registers

Index	Register Name
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left Output Control
7	Right Output Control
8	Data Format
9	Interface Configuration
10	Pin Control
11	Test and Initialization
12	Misc. Information
13	Loopback Control
14	Upper Base Count
15	Lower Base Count

Table 2. Indirect Registers

Physical Mapping

The control registers are mapped via partial indirect mapping. Two address bits are defined to access all of the CS4248's registers. The four direct registers are shown in Table 1. The first two direct registers are used to access 16 indirect registers as shown in Table 2. Table 3 details a summary of each bit in each register. The detailed register descriptions are described in this section. Tables 4 through 6 illustrate all the programmable gain block decodes and is included here for reference. These gain tables will be referred to under the description for the particular register.

Index Register

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	res	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the CS4248 register accessed by the Indexed Data Register. These bits are read/write.

res — Reserved for future expansion. Always write zero to this bit.

MCE — Mode Change Enable: This bit must be set whenever the current mode of the CS4248 is changed. The Data Format and Interface Configuration registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". No audio activity will occur when this bit is set.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the status register is set.

0 - Transfers Enabled (PDRQ and CDRQ occur uninhibited)
1 - Transfers Disabled (PDRQ and CDRQ only occur if INT bit is 0)

INIT — CS4248 Initialization: This bit is read as 1 when the CS4248 is in a state which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the CS4248 has left the INIT state), the state of this register is: 010X0000 (40h)

During CS4248 initialization, this register CANNOT be written and is always read 10000000 (80h)

Indexed Data Register

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 Indexed Register Data: These bits are the data the CS4248 register referenced by the Indexed Data register.

During CS4248 initialization, this register can NOT be written and is always read 10000000 (80h)

I/O Data Register

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During CS4248 initialization, this register CANNOT be written and is always read 10000000 (80h)

Capture Data Register (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register. Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, and a read of the status has occurred, the state machine and status register will point to the first byte of the new sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

During CS4248 initialization, this register can NOT be written and is always read 10000000 (80h)

Playback Data Register (Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 Playback Data Port. This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Status Register

D7	D6	D5	D4	D3	D2	D1	D0
CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT

INT — Interrupt Status: This indicates the status of the internal interrupt logic of the CS4248. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register determines whether the state of this bit is reflected on the IRQ pin of the CS4248.
Read States

0 - Interrupt pin inactive
1 - Interrupt pin active

PRDY — Playback Data Register Ready. The Playback Data register is ready for more data. This bit would be used when direct programmed I/O data transfers are desired. (This bit is Read-Only)

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

PL/$\overline{R}$ — Playback Right/Left Sample: This bit indicates whether data needed is for the Right channel or Left channel. (This bit is Read-Only)

0 - Right Channel Data
1 - Left Channel Data or Mono selected

PU/$\overline{L}$ — Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel. (This bit is Read-Only)

0 - Lower Byte Needed
1 - Upper Byte Needed or any 8-bit mode

SER — Sample Error: This bit indicates that a sample was not serviced in time and therefore an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. (This bit is Read-Only)

CRDY — Capture Data Ready. The Capture Data register contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers. (This bit is a Read-Only)

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ — Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Right channel or Left channel. (This bit is Read-Only)

0 - Right Channel Data
1 - Left Channel Data or mono

CU/$\overline{L}$ — Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel. (This bit is Read-Only)

0 - Lower byte ready
1 - Upper byte ready or any 8-bit mode

The PRDY and CRDY bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one the device is ready for more data, or when the CRDY is set to one data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

Indirect Mapped Registers

These registers are accessed by placing the appropriate index in the Index register and then accessing the Index Data register. A detailed description of each of the registers is given below. All reserved bits should be written zero and may be 0 or 1 when read back

Input Control Registers

Left Input Control (Index 0)

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0

LIG3-LIG0 Left input gain select. The least significant bit of this gain select represents 1.5 dB. See Table 4.

LMGE Left Input Mic Gain Enable: This bit will enable the 20 dB gain of the left mic input signal.

LSS1-LSS0 Left input source select. These bits select the input source for the left gain stage going to the left ADC.

0 - Left Line
1 - Left Auxiliary 1
2 - Left Microphone
3 - Left Line Output Loopback

This register's initial state after reset is: 000x0000

Right Input Control (Index 1)

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0

RIG3-RIG0 Right input gain select. The least significant bit of this gain select represents 1.5 dB. See Table 4.

RMGE Right Input Mic Gain Enable: This bit will enable the 20 dB gain of the right mic input signal.

RSS1-RSS0 Right input source select. These bits select the input source for the right channel gain stage going to the right ADC.

0 - Right Line
1 - Right Auxiliary 1
2 - Right Microphone
3 - Right Line Out Loopback

This register's initial state after reset is: 000x0000

Left Auxiliary #1 Input Control (Index 2)

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0 Left Auxiliary #1 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

LX1M Left Auxiliary #1 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #1 input source.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #1 Input Control (Index 3)

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0 Right Auxiliary #1 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

RX1M Right Auxiliary #1 Mute. This bit, when set to 1, will mute the right channel of the Auxiliary #1 input source.

This register's initial state after reset is: 1xx01000.

Left Auxiliary #2 Input Control (Index 4)

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

LX2M Left Auxiliary #2 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #2 input source.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #2 Input Control (Index 5)

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

RX2M Right Auxiliary #2 Mute. This bit, when set to 1, will mute the right channel of the Auxiliary #2 input source.

This register's initial state after reset is: 1xx01000.

Output Control Registers

Left Output Control (Index 6)

D7	D6	D5	D4	D3	D2	D1	D0
LOM	res	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0

LOA5-LOA0 Left Output Attenuate Select. The least significant bit of this attenuate select represents -1.5 dB. Full attenuation is at least -94.5 dB. See Table 6.

LOM Left Output Mute. This bit, when set to 1, will mute the left DAC channel output.

This register's initial state after reset is: 1x000000.

Right Output Control (Index 7)

D7	D6	D5	D4	D3	D2	D1	D0
ROM	res	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0

ROA5-ROA0 Right Output Attenuate Select. The least significant bit of this attenuate select represents -1.5 dB. Full attenuation must be at least -94.5 dB. See Table 6.

ROM Right Output Mute. This bit, when set to 1, will mute the right DAC output.

This register's initial state after reset is: 1x000000.

Data Format Register (Index 8)

D7	D6	D5	D4	D3	D2	D1	D0
res	FMT	C/$\overline{L}$	S/$\overline{M}$	CSF2	CFS1	CFS0	CSL

CSL Clock Source Select: These bits select the clock source used for the audio sample rates.
CAUTION: See note at end of this section about changing these bits

0 - XTAL1/ 24.576 MHz
1 - XTAL2/ 16.9344 MHz
Note: When only one crystal or clock source is provided in hardware,it must be XTAL1.

CFS2-CFS0 Clock Frequency Divide Select: These bits select the audio sample rate frequency. The actual audio sample rate depends on which Clock Source is selected and it's frequency.
CAUTION: See note below about changing bits

Divide	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

0 - Mono
1 - Stereo

C/$\overline{L}$ Companded /Linear Select: This bit selects between a linear digital representation of the audio signal or a non-linear, companded format. The type of companded format is defined by the FMT bit.

0 - Linear 1 - Companded

FMT Format Select: This bit defines the exact format of the digital audio based on the state of the C/L bit.

C/$\overline{L}$=0	C/$\overline{L}$=1
Linear	Companded
0 - 8 bit, unsigned	0 - μ-Law
1 - 16-bit, signed	1 - A-law

This register's initial state after reset is: x0000000.

Note: The Contents of this register CANNOT be changed except when the CS4248 is in Mode Change Enable (MCE) is 1. If MCE is not one, writes to this register will be ignored.

Interface Configuration Register (Index 9)

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

PEN Playback Enable. This bit enables playback. The CS4248 will generate PDRQ and respond to PDAK signals when this bit is enabled and PPIO=0. If PPIO=1, this bit enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (PDRQ and PIO inactive)
1 - Playback Enabled

CEN Capture Enabled. This bit enables the capture of data. The CS4248 will generate CDRQ and respond to CDAK signals when this bit is enabled and CPIO=0. If CPIO=1, this bit enables PIO capture mode. CEN may be changed without setting the MCE bit.

0 - Capture Disabled (CDRQ and PIO inactive)
1 - Capture Enabled

SDC Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be zero. This bit will allow the CS4248 to be used with only one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the DMA section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

ACAL Auto calibrate Enable: This bit determines whether the CS4248 performs an auto calibrate whenever returning from the Mode Change Enable (MCE) bit being asserted. If the ACAL bit is not set, previous calibration values are used, and no calibration cycle takes place. Therefore, ACAL is normally set.

0 - No auto calibration
1 - Auto calibration allowed

PPIO Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers only
1 - PIO transfers only

CPIO Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers only
1 - PIO transfers only

Note: This register, except bits CEN and PEN, can only be written while in Mode Change Enable. See section on MCE for more details.

This register's initial state after reset is: 00xx1000

Pin Control Register (Index 10)

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	res	res	DEN	res	IEN	res

IEN — Interrupt Enable: This bit enables interrupts to occur on the interrupt pin. The Interrupt pin will reflect the value of the INT bit in the status register. The interrupt pin is active high.

0 - Interrupt Disabled
1 - Interrupt Enabled

DEN — Dither Enable: When this bit is set, triangular pdf dither is added before truncating the ADC 16-bit data to 8-bit unsigned data. Dither is only active in the 8-bit unsigned data format.

0 - Dither Disabled
1 - Dither Enabled

XCTL1, XCTL0 — XCTL Control: These bits are reflected on the XCTL1,0 pins of the CS4248

0 - TTL Logic Low on XCTL1,0 pins
1 - TTL Logic High on XCTL1,0 pins

This registers initial state after reset is: 00xx0x0x

Test and Initialization Register (Index 11)

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 — Overrange Left Detect: These bits determine the overrange on the left input channel. (Read Only) These bits hold the peak value and are reset to "0" by a read of this register

0 - Greater than -1.5 dB underrange
1 - Between -1.5 dB and 0 dB underrange
2 - Between 0 dB and 1.5 dB overrange
3 - Greater 1.5 dB overrange

ORR1-ORR0 — Overrange Right Detect: These bits determine the overrange on the right input channel. (Read Only) These bits hold the peak value and are reset to "0" by a read of this register

0 - Greater than -1.5 dB underrange
1 - Between -1.5 dB and 0 dB underrange
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS — DRQ Status: This bit indicates the current status of the PDRQ and CDRQ pins of the CS4248.

0 - CDRQ AND PDRQ are presently inactive
1 - CDRQ OR PDRQ are presently active

ACI — Auto calibrate In-Progress: This bit indicates the state of auto calibration (Read-Only)

0 - Auto calibration not in progress
1 - Auto calibration is in progress

PUR — Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result the last valid sample will be sent to the DAC. This bit is sticky and will set in in an error condition. This bit is cleared by a Status register read.

COR — Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample will be ignored. This bit is sticky and will stay set in an error condition. This bit is cleared by a Status register read.

The SER bit in the Status register is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

This register's initial state after reset is: 00000000

Misc. Information Register (Index 12)

D7	D6	D5	D4	D3	D2	D1	D0
1	res	res	res	ID3	ID2	ID1	ID0

ID3-ID0 CS4248 ID: These four bits define the version of the CS4248. These bits are Read-Only

ID3-ID0 = 0001 Chip version "B"
ID3-ID0 = 1010 Chip version "C" and later.

This register's initial state after reset is: 1xxx0001 or 1xxx1010 based on chip version.

Loopback Control Register (Index 13)

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE Loopback Enable: This bit will enable the loopback mode of the CS4248 from the ADC's output to the DACs. When enabled, the data from the ADC's are digitally mixed with other data being delivered to the DACs.

0 - Loopback disabled
1 - Loopback enabled

LBA5-LBA0 Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. Each attenuation step is -1.5 dB. See Table 7.

This register's initial state after reset is: 000000x0

DMA Count Registers

The DMA Count registers allow easier integration of the CS4248 in ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Count registers provides this service. This register should be loaded with the buffer size minus one.

The Base Count register contains the number of samples which occur before an interrupt is generated on the INT pin. The act of writing a value to the Upper Base register cause both Base registers to load the current count register. Once transfers are enabled, each sample will decrement the current count registers until zero is reached. The next sample after zero generates an interrupt and reloads the count registers with the values in the Base registers. The interrupt is cleared by a write to the Status register.

The count register is only decremented when either the PEN or CEN bit is enabled AND a sample occurs.

Upper Base Register (Index 14)

D7	D6	D5	D4	D3	D2	D1	D0
UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

UB7-UB0 Upper Base Bits: This byte is the upper byte of the base count register. It represents the 8 most significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count registers cannot be read. The base register should be loaded with the buffer size minus 1.

This register's initial state after reset is: 0000000

Lower Base Register (Index 15)

D7	D6	D5	D4	D3	D2	D1	D0
LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

LB7-LB0 Lower Base Bits: This byte is the lower byte of the base count register. It represents the 8 least significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count registers cannot be read. The Base register should be loaded with the buffer size minus one.

This register's initial state after reset is: 00000000

Direct Registers:

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	INIT	MCE	TRD	-	IA3	IA2	IA1	IA0
1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
2	1	0	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
3	1	1	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	1	1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers:

IA3-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LIG3	LIG2	LIG1	LIG0
1	RSS1	RSS0	RMGE	-	RIG3	RIG2	RIG1	RIG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LOM	-	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0
7	ROM	-	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0
8	-	FMT	C/$\overline{L}$	S/$\overline{M}$	CSF2	CSF1	CSF0	CSL
9	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	-	-	DEN	-	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	-	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

Table 3. Register Bit Summary

	IG3	IG2	IG1	IG0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	1.5 dB
2	0	0	1	0	3.0 dB
3	0	0	1	1	4.5 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	18.0 dB
13	1	1	0	1	19.5 dB
14	1	1	1	0	21.0 dB
15	1	1	1	1	22.5 dB

Table 4. ADC Input Gain

	OA5	OA4	OA3	OA2	OA1	OA0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.				.			.
.				.			.
.				.			.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 6. DAC Output Attenuation

	XxG4	XxG3	XxG2	XxG1	XxG0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	0	1	0	0	0	0.0 dB
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.			.			.
.			.			.
.			.			.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 5. AUX1, AUX2 Output Mix Gain

	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.				.			.
.				.			.
.				.			.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 7. Loopback Attenuation

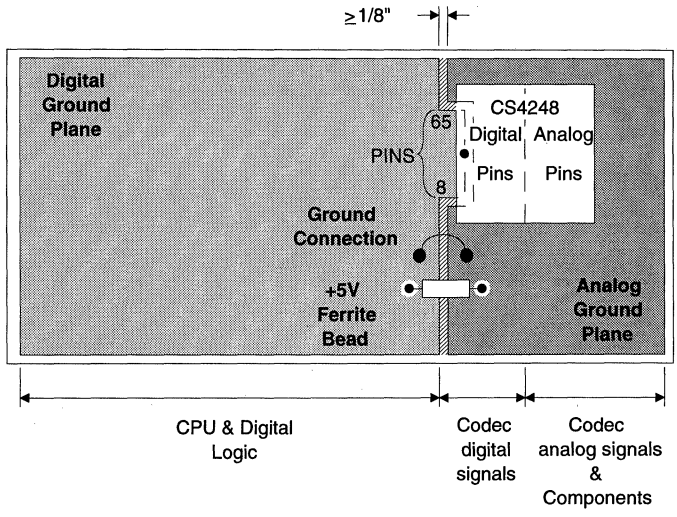


Figure 9. Suggested Layout Guideline

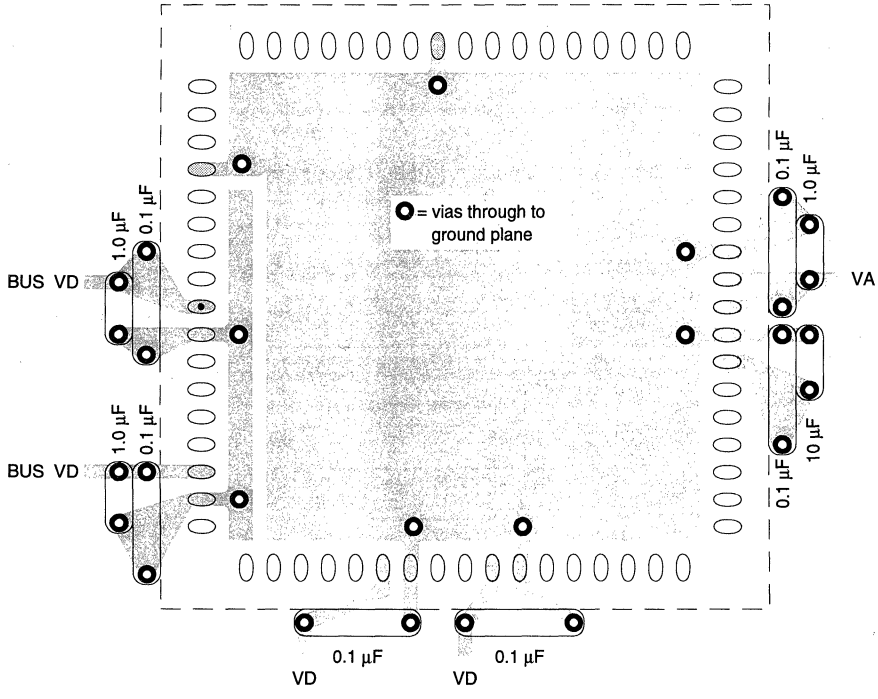


Figure 10. Recommended Decoupling Capacitor Positions

POWER SUPPLY AND GROUNDING

Figure 9 is the suggested layout for the CS4248. Similar to other Crystal codecs, it is recommended that the device be located on a separate analog ground plane. With the CS4248's parallel data interface, however, optimum performance is achieved by extending the digital ground plane across pins 65 through 68 and pins 1 through 8. Pins 2 and 8 are grounds for the data bus and are electrically connected to the digital ground plane. This minimizes the effect of the bus interface due to transient currents during bus switching. Figure 10 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the CS4248. The vias shown go through to the ground plane layer. See Crystal's layout application note for more information.

COMPATIBILITY WITH AD1848

The CS4248 is compatible with the AD1848 rev. J silicon in terms of the applications circuit. The AD1848 rev. K requires 1.0 µF capacitors (not 1000pF) on pins 26 and 31. The CS4248 requires 1000 pF NPO-type capacitors on filter pins 26 and 31 (not 1.0 µF). To achieve compatibility with the CS4248:

1. Correct spacing of pads will ensure that either 1.0 µF capacitors (for the AD1848 rev. K) or 1000 pF NPO capacitors (for the CS4248) may be installed.

2. The CS4248 does not require the input anti-aliasing filters included as an input R/C for the AD1848 (5.1kΩ and 560 pF). The additional R/C's can be used with the CS4248 if desired, with no degradation in performance.

3. Crystal recommends the ground plane as shown in Figure 9. Any ground plane scheme that achieves acceptable performance with the AD1848 should work with the CS4248.

4. The AD1848 needs extra power and ground pins. The power pins (VDD) are pins 24, 45, and 54. The ground pins (GNDD) are pins 25 and 44. The CS4248 PLCC package does not use these pins ard the appropriate power/ground connections can be made.

5. The AD1848 does not contain the selectable dither (DEN, I10).

6. The AD1848 is not avai;able in a 100-pin TQFP package.

As far as software is concerned, the CS4248 is compatible with the AD1848 rev. K in terms of the mix gain on the AUX1 and AUX2 inputs, and the position of the output mute block. The CS4248 is also software compatible with the MCE and auto-calibration functionality of the AD1848 rev. K.

ADC and DAC Filter Response Plots

Figures 11 through 16 show the overall frequency response, pass-band ripple and transition band for the CS4248 ADCs and DACs. Figure 17 shows the DACs' deviation from linear phase.

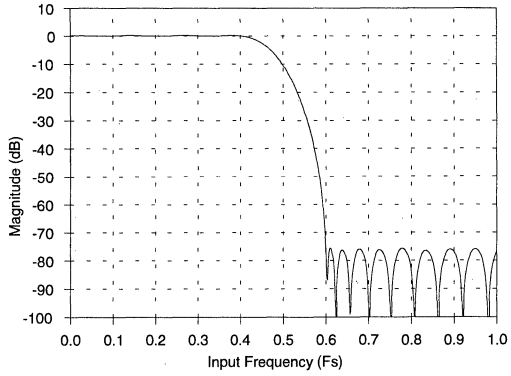


Figure 11. 16-bit ADC Filter Response.

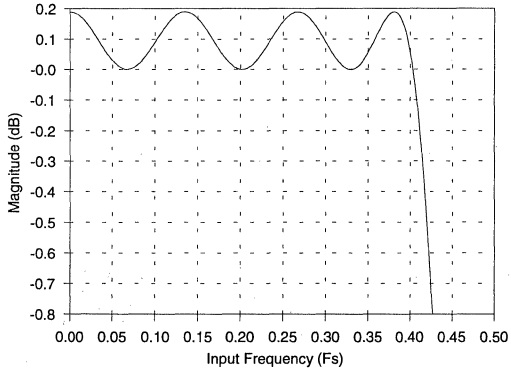


Figure 12. 16-bit ADC Passband Ripple.

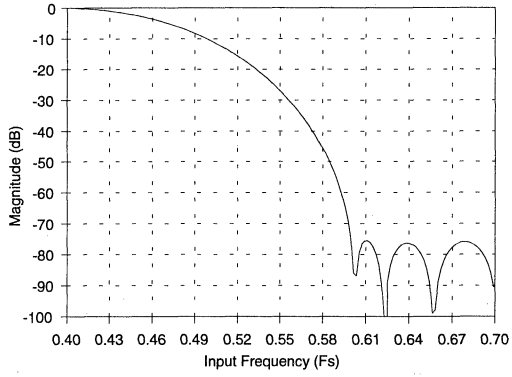


Figure 13. 16-bit ADC Transition Band.

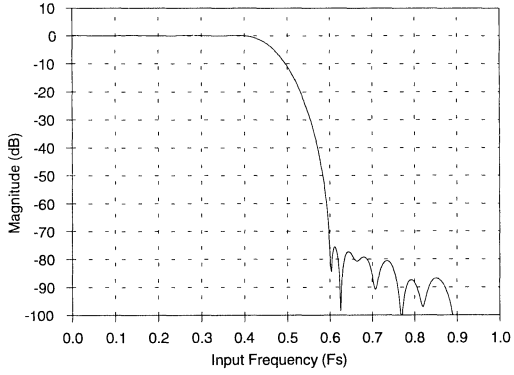


Figure 14. DAC Frequency Response

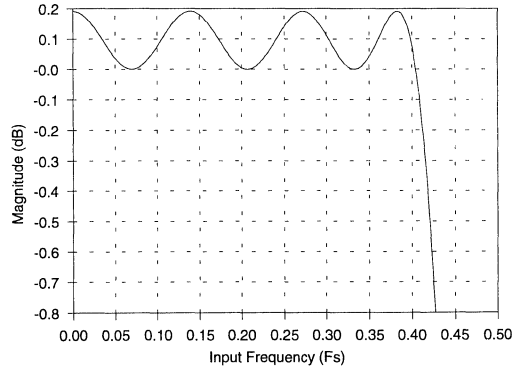


Figure 15. DAC Passband Ripple.

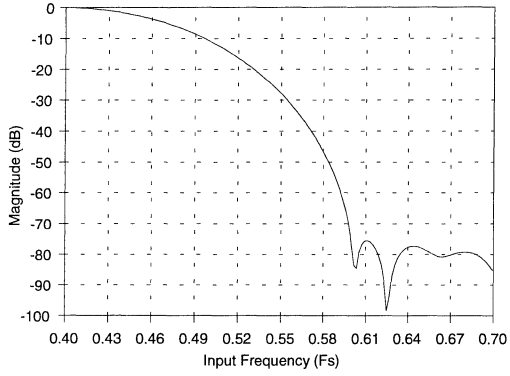


Figure 16. DAC Transition Band.

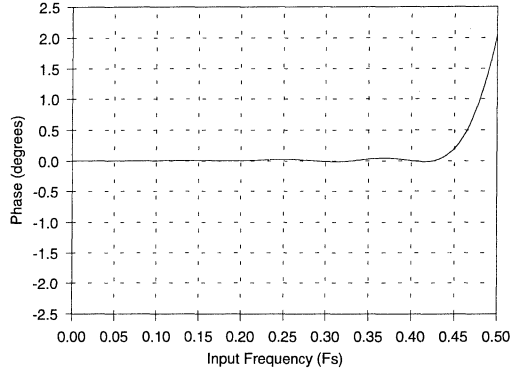
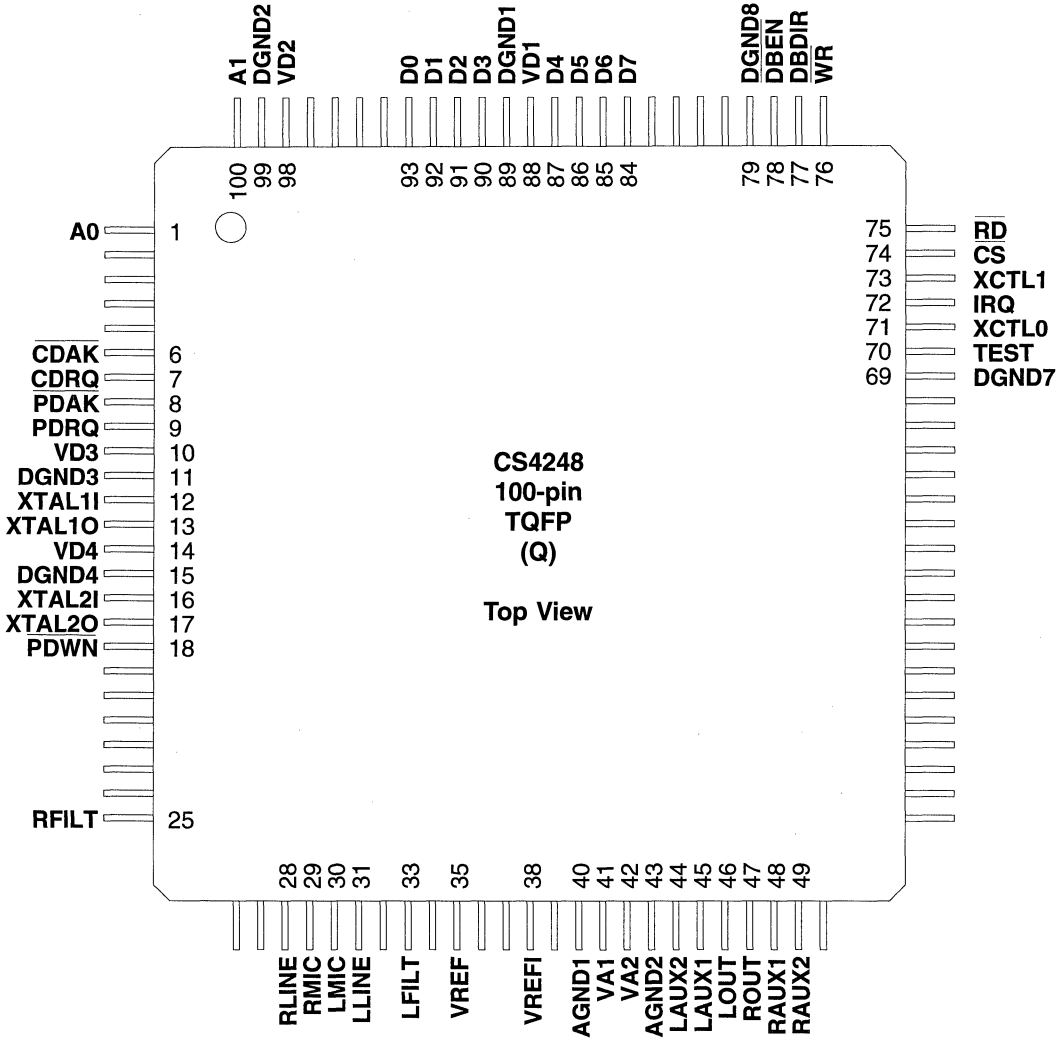
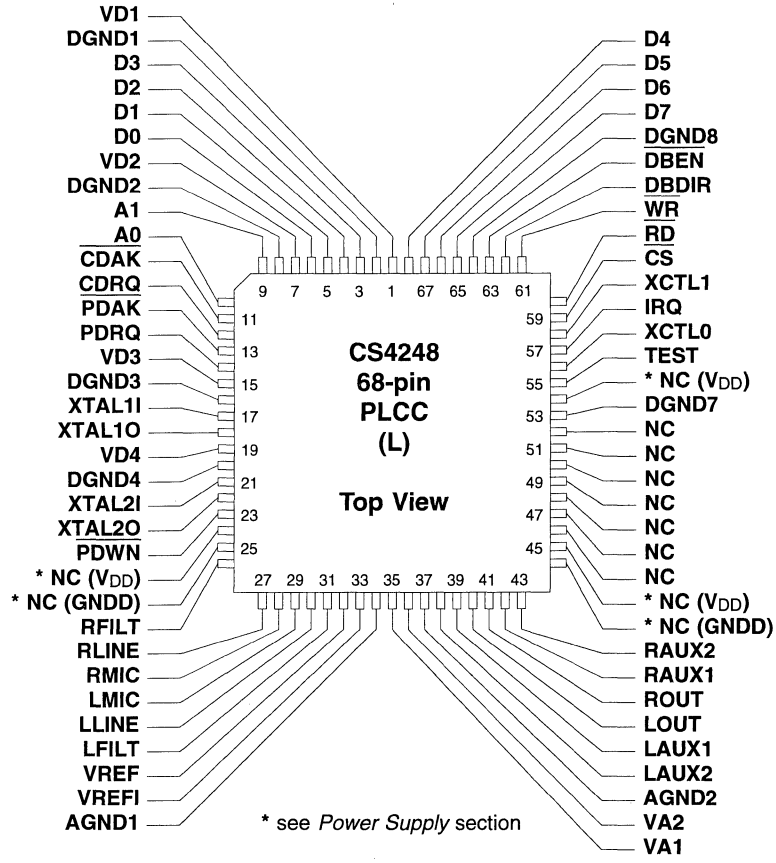


Figure 17. DAC Phase Response.

PIN DESCRIPTION





Parallel Bus Interface Pins

CDRQ - Capture Data Request, Output, Pin 12 (L), Pin 7 (Q).

The assertion of this signal indicates that the codec has a captured audio sample ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.

$\overline{\text{CDAK}}$ - Capture Data Acknowledge, Input, Pin 11 (L), Pin 6 ($\overline{\text{Q}}$).

The assertion of this active low signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.

PDRQ - Playback Data Request, Output, Pin 14 (L), Pin 9 (Q).

The assertion of this signal indicates that the codec is ready for more playback data. The signal will remain asserted until the bytes needed for a playback sample have been transferred.

$\overline{\text{PDAK}}$ - Playback Data Acknowledge, Input, Pin 13 (L), Pin 8 (Q).
The assertion of this active low signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.

A< 1:0> - Address Bus, Input, Pin 9, 10 (L), Pin 100, 1 (Q).
These address pins are read by the codec interface logic during an I/O cycle access. The state of these address lines determines which register is accessed.

$\overline{\text{RD}}$ - Read Strobe, Input, Pin 60 (L), Pin 75 (Q).
This signal defines a read cycle to the codec. The cycle may be an I/O cycle read, or the cycle could be a read from the codec's DMA sample registers.

$\overline{\text{WR}}$ - Write Strobe, Input, Pin 61 (L), Pin 76 (Q).
This signal indicates a write cycle to the codec. The cycle may be an I/O cycle write, or the cycle could be a write to the codec's DMA sample registers.

$\overline{\text{CS}}$ - Chip Select, Input, Pin 59 (L), Pin 74 (Q).
The codec will not respond to any I/O cycle accesses unless this signal is active. This signal is ignored during DMA transfers.

D< 7:0> - Data Bus, Input/Output, Pin 65-68, 3-6 (L), Pin 84-87, 90-93 (Q).
These signals are used to transfer data to and from the CS4248.

$\overline{\text{DBEN}}$ - Data Bus Enable, Output, Pin 63 (L), Pin 78 (Q).
This pin indicates that the bus drivers attached to the CS4248 should be enabled. This signal is normally high.

DBDIR - Data Bus Direction, Output, Pin 62 (L), Pin 77 (Q).
This pin indicates the direction of the data bus transceiver. High points to the CS4248, low points to the host bus. This signal is normally high.

IRQ - Host Interrupt Pin, Output, Pin 57 (L), Pin 72 (Q).
This signal is used to notify the host of events which need servicing.

Analog Inputs

LLINE - Left Line Input, Pin 30 (L), Pin 31 (Q).
Nominally 1 V_{RMS} max analog input for the Left LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I0).

RLINE - Right Line Input, Pin 27 (L), Pin 28 (Q).
Nominally 1 V_{RMS} max analog input for the Right LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I1).

LMIC - Left Mic Input, Pin 29 (L), Pin 30 (Q).
Microphone input for the Left MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (LMGE = 0) or 0.1 V_{RMS} (LMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I0).

RMIC - Right Mic Input, Pin 28 (L), Pin 29 (Q).
Microphone input for the Right MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (RMGE = 0) or 0.1 V_{RMS} (RMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I1).

LAUX1 - Left Auxiliary #1 Input, Pin 39 (L), Pin 45 (Q).
Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I2) also allows routing to the output mixer.

RAUX1 - Right Auxiliary #1 Input, Pin 42 (L), Pin 48 (Q).
Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I3) also allows routing to the output mixer.

LAUX2 - Left Auxiliary #2 Input, Pin 38 (L), Pin 44 (Q).
Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block (I4) allows routing of the AUX2 channels into the output mixer.

RAUX2 - Right Auxiliary #2 Input, Pin 43 (L), Pin 49 (Q).
Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block (I5) allows routing of the AUX2 channels into the output mixer.

Analog Outputs

LOUT - Left Line Level Output, Pin 40 (L), Pin 46 (Q).
Analog output from the mixer for the left channel. Nominally 0.707 V_{RMS} max centered around VREF.

ROUT - Right Line Level Output, Pin 41 (L), Pin 47 (Q).
Analog output from the mixer for the right channel. Nominally 0.707 V_{RMS} max centered around VREF.

Miscellaneous

XTAL1I - Crystal #1 Input, Pin 17 (L), Pin 12 (Q).
This pin will accept either a crystal with the other pin attached to XTAL1O or an external CMOS clock. XTAL1 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 24.576 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL1O - Crystal #1 Output, Pin 18 (L), Pin 13 (Q).
This pin is used for a crystal placed between this pin and XTAL1I.

XTAL2I - Crystal #2 Input, Pin 21 (L), Pin 16 (Q).
If a second crystal is used, is should be placed between this pin and XTAL2O. The standard crystal frequency is 16.9344 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL2O - Crystal #2 Output, Pin 22 (L), Pin 17 (Q).
This pin is used for a crystal placed between this pin and XTAL2I.

$\overline{\text{PDWN}}$ - Power Down Signal, Input, Pin 23 (L), Pin 18 (Q).
Places CS4248 in lowest power consumption mode. All sections of the CS4248, except the bus interface logic which reads 80h, are shut down and consuming minimal power. The CS4248 is in power down mode when this pin is logic low.

XCTL0, XCTL1 - External Control, Output, Pin 56, 58 (L), Pin 71, 73 (Q).
These signals are controlled by register bits inside the CS4248. They can be used to control external logic via TTL levels.

VREF - Voltage Reference, Output, Pin 32 (L), Pin 35 (Q).
All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered. High internal-gain microphone inputs can be slightly improved by placing a 10µF capacitor on VREF.

VREFI - Voltage Reference Internal, Input, Pin 33 (L), Pin 38 (Q).
Voltage reference used internal to the CS4248 must have a 0.1 µF + 10 µF capacitor with short fat traces to attach to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input, Pin 31 (L), Pin 33 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

RFILT - Right Channel Antialias Filter Input, Pin 26 (L), Pin 25 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

TEST - Test, Pin 55 (L), Pin 70 (Q).
This pin must be tied to ground for proper operation.

Power Supplies

VA1, VA2 - Analog Supply Voltage, Pin 35, 36 (L), Pin 41, 42 (Q).
Supply to the analog section of the codec.

AGND1, AGND2 - Analog Ground, Pin 34, 37 (L), Pin 40, 43 (Q).

Ground reference to the analog section of the codec. Internally, these pins are connected to the substrate as are DGND3/4/7/8; therefore, optimum layout is achieved with the AGND pins on the same ground plane as DGND3/4/7/8 (see Figure 10). However, other ground arrangements should yield adequate results.

VD1, VD2 - Digital Supply Voltage, Pin 1, 7 (L), Pin 88, 98 (Q).

Digital supply for the parallel data bus section of the codec.

VD3, VD4 - Digital Supply Voltage, Pin 15, 19 (L), Pin 10, 14 (Q).

Digital supply for the internal digital section of the codec (except for the parallel data bus).

DGND1, DGND2 - Digital Ground, Pin 2, 8 (L), Pin 89, 99 (Q).

Digital ground reference for the parallel data bus section of the codec. These pins are isolated from the other digital grounds and should be connected to the digital ground section of the board (see Figure 10).

DGND3, DGND4, DGND7, DGND8 - Digital Ground, Pin 16, 20, 53, 64(L), Pin 11, 15, 69, 79(Q)

Digital ground reference for the internal digital section of the codec (except the parallel data bus). These pins are connected to the substrate of the die as are the AGND pins; therefore, optimum layout is achieved by placing DGND3/4/7/8 on the analog ground plane with the AGND pins as shown in Figure 10. However, other ground arrangements should yield adequate results.

*** NC (V_{DD}) - No Connect, Pins 24, 45, 54 (L)**

These pins are no connects for the CS4248. When compatibility with the AD1848 is desired, these pins should be connected to the digital power supply. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

*** NC (GNDD) - No Connect, Pins 25, 44 (L)**

These pins are no connects for the CS4248. When compatibility with the AD1848 is desired, these pins should be connected to digital ground. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

Semiconductor Corporation

DRIVERS

CS4231 and CS4248 Device Drivers

Features

- Support wave audio capture, playback under Windows 3.1 & NT
- Highly optimized code for maximum throughput, minimum CPU utilization
- Input & Output volume/mixing control
- Support ADPCM compression & decompression
- Full Duplex audio capture & playback
- Complete with installation routines, documentation, etc.

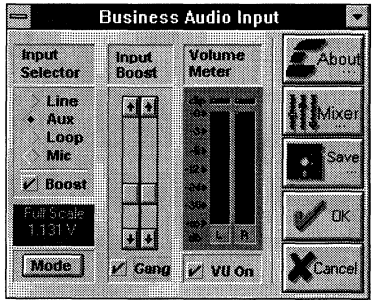
General Description

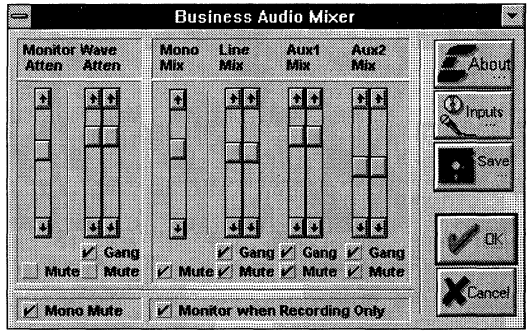
Crystal offers complete wave driver support for the Microsoft Windows 3.1 & NT environments. CS4231 drivers supports full duplex operation -- i.e. simultaneous capture and playback. Full duplex permits voice recognition to control multimedia playback. Control panel applets are provided supporting all features of the CS4248 and CS4231 devices. Functions include: 1) Input control panel used to select audio source and individually set the gain level, turn dither on/off, and visually monitor recording levels with a VU meter; 2) Output control panel used to control volume, mixer levels and loopback monitoring; 3) Recorder applet used to capture and playback .WAV files, at various sample frequencies, with compression & de-compression (ADPCM, ULaw & ALaw). The recorder is an OLE server.

All source code was developed in-house. Object code is provided without licensing fees directly by Crystal. Sample copies are available.

ORDERING INFORMATION

Contact Crystal Semiconductor





Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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Semiconductor Corporation

DIAGNOSTICS

Multimedia Audio Codec Diagnostic Software

Features

- Development and manufacturing test support for the CS4248 & CS4231
- Control over every feature & function - automated board test features
- Measure Codec performance without need of an external signal source
- Record and playback .WAV files in the DOS environment
- Real-time FFT, time and frequency-response plots

General Description

The diagnostics program for the CS4231 and CS4248 assists in every phase of PC audio sub-system design. From initial board bring-up and functional testing to factory test and field service, the diagnostics provide in-depth information to the engineer regarding audio performance and function.

Detailed reporting capabilities aid in both burn-in and board debug. The diagnostics support communication through input and output files, as well as DOS exit codes, allowing it to be spawned by another program and return meaningful results. A system-level diagnostics/factory test system could thus use the program while retaining its' own user interface routines.

The diagnostics run under DOS, and are controlled by a command line interface optimized for minimum keystrokes. Sample 'C' source code is available detailing how to call the routines from inside a host program.

All source code was developed in-house by Crystal. Object code is provided to OEMs without charge. Sample copies are available.

ORDERING INFORMATION
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Product Preview

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Semiconductor Corporation

CWMNLG

First Byte's Monologue for Windows

Features

- Monologue Text-To-Speech synthesis software from First Byte.
- Industry leading text-to-speech
- Allows Windows applications to speak
- Permits efficient proof-reading of text and numerical data
- Multilingual: French, German, Spanish and American available now; Italian, British and Japanese in development
- Transfer data through clipboard or direct DLL/DDE link

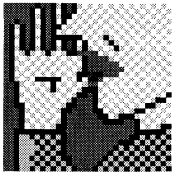
General Description

Monologue increases productivity in the business environment, allowing users to add speech capabilities to any Windows (or DOS) application. Any pronounceable combination of letters and numbers will be spoken clearly. No voice recording or speech training is necessary. Customizable speech parameters permit control of volume, pitch and speed. An exception dictionary allows the user to save preffered pronounciations of words and abbreviations.

Crystal Semiconductor has a strategic relationship with First Byte to allow OEMs to integrate speech capabilities into their products. Crystal licenses the products directly to OEMs.

Sample copies are available free of charge; license fees for production are volume dependent.

ORDERING INFORMATION
Contact Crystal Semiconductor



Monologue
16-bit

Product Preview

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Semiconductor Corporation

CWDRGNTT

Talk→To Voice Recognition from Dragon Systems

Features

- World's foremost voice recognition
- Supports popular Windows apps.
- Hands free command & control in the Windows 3.1 environment
- Reduces typing for data entry
- Speaker independent - also supports regional dialects through training
- Supports 64 active commands; context sensitive for unlimited recognition

General Description

Talk→To is a powerful and flexible voice recognition package for the Microsoft Windows 3.1 environment. Voice recognition enhances productivity by allowing users to enter simple voice commands, instead of complicated keystrokes or multiple mouse movements, to choose menu and control options. Voice recognition redefines the human/computer interface, making it truly intuitive. Talk→To is highly speaker independent, yet may be quickly trained to support an individual's speaking style, thus handling regional or foreign accents.

Crystal Semiconductor has a strategic relationship with Dragon Systems to allow OEMs to integrate voice recognition capabilities into their products. Crystal licenses the products directly to OEMs.

Sample copies are available free of charge; license fees for production are volume dependent.

ORDERING INFORMATION:

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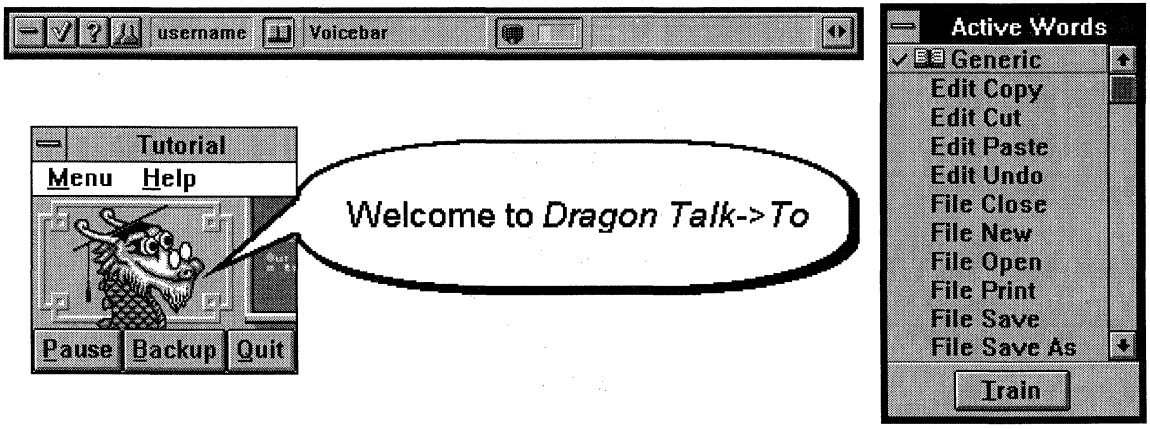

Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

CS4920 Multi-Standard Audio Decoder/DAC

The CS4920 combines a 16.5MIPS DSP with a stereo 16-bit Digital to Analog converter. In addition, a decompressed linear PCM coded digital output is available in industry standard S/PDIF format. An on-chip PLL allows very flexible clocking. DSP code for MPEG Layers 1 and 2, and Dolby AC2 decompression algorithms is provided. Targetted at TV set top audio decoder applications, this device is useful in any application where low-cost audio decompression is required.

CS8905 and CS9203 Audio Wave Table Synthesizers

The CS9203 is a wave table synthesizer which uses a set of sampled real sounds, stored in a ROM, to construct very realistic musical sounds. When teamed with a 8051 type microcontroller, a General Midi compliant synthesizer may be easily realized. Crystal can supply the CS9203, the wave table ROM information and code for the microcontroller.

The CS8905 is a programmable effects DSP which may be used to add various sound effects to the output of the CS9203 wave table synthesizer.

CONTENTS

Semiconductor Corporation

CS4920

Multi-Standard Audio Decoder - DAC

Features

- General Purpose Digital Signal Processor Optimized for Audio
  - 24 Bit Fixed Point
  - 48 Bit Accumulator
  - 16.9 MIPS @ 44.1 kHz Sample Rate
- On-Chip Functional Blocks Include:
  - -CD Quality D/A Converter
  - -Programmable PLL Clock Multiplier
  - -AES/EBU - S/PDIF Compatible Digital AudioTransmitter
  - -Audio Serial Input Port
  - -Serial Control Port
- Applications Include:
  - -Audio Decompression
  - -MPEG Layers 1 and 2
  - -Dolby AC-2
- Standard 44 pin PLCC Package

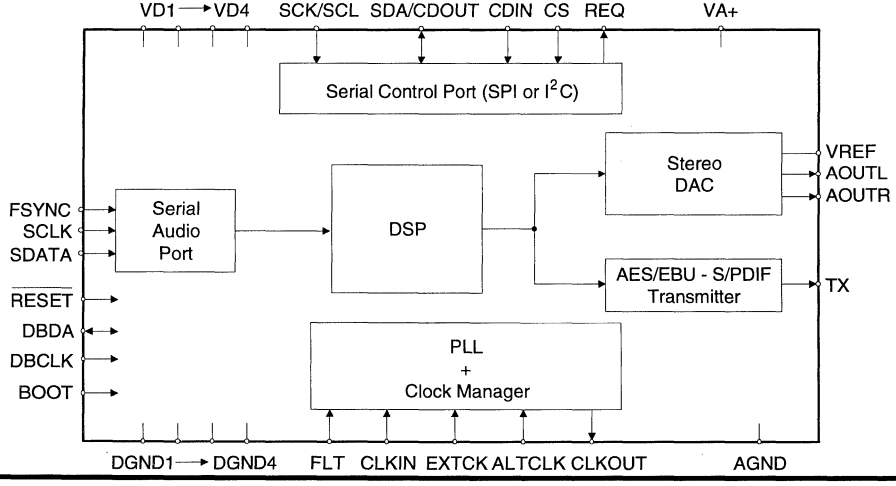
General Description

The CS4920 is a complete audio subsystem on a chip. This device contains a general purpose DSP, a CD quality stereo Digital-to-Analog Converter, a programmable PLL clock multiplier, an AES-EBU - S/PDIF compatible digital audio transmitter, an audio serial input port, and a serial control port. The CS4920 is based on a programmable DSP core and is intended to support a wide variety of digital signal processing applications which include decoding compressed digital audio. Serial audio data broadcast on networks such as cable TV, direct broadcast satellite TV, or the telephone system can be decompressed and converted to standard analog or digital signals.

Both industry standard and proprietary DSP algorithms can be supported. Software which performs industry standard MPEG layers 1 and 2 and Dolby AC-2 is available. A complete set of software development tools are available. These include an assembler, simulator, and debugger.

ORDERING INFORMATION:
CS4920-CL 44-pin PLCC
CDB4920 Evaluation Board

5



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; Full-Scale Output Sinewave, 1 kHz; Word Clock = 48 kHz (PLL in use); Logic 0 = GND, Logic 1 = VD+; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in "Typical Connection Diagram"; SPI mode, I^2S audio data; unless otherwise specified.)

Parameter*		Symbol	Min	Typ	Max	Units
Dynamic Performance						
DAC Resolution		-	16	-	-	Bits
DAC Differential Nonlinearity		-		-	±0.9	LSB
Total Harmonic Distortion	(Note 1)	THD	-	-	0.01	%
Instantaneous Dynamic Range (DAC not muted, Note 1, A weighted)		-	85	88	-	dB
Interchannel Isolation	(Note 1)	-	-	85	-	dB
Interchannel Gain Mismatch		-	-	-	0.2	dB
Frequency Response	(10 to 0.476 Fs)	-	-3.0	-	+0.2	dB
Full Scale Output Voltage	(Note 1)	-	2.66	2.88	3.1	V_{pp}
Gain Drift		-	-	100	-	ppm/°C
Deviation from Linear Phase		-	-	-	5	Deg
Out of Band Energy	(Fs/2 to 2Fs)	-	-	-60	-	dB
Analog Output Load	Resistance: Capacitance:		8 -	- -	- 100	kΩ pF
Power Supply						
Power Supply Rejection	(1 kHz)		-	40	-	dB
Power Supply Consumption	VA+	-	-	40	TBD	mA
	VD+	-	-	80	TBD	mA

Note: 1. 10 kΩ, 100pF load.

D/A Interpolation Filter Characteristics (See graphs toward the end of this data sheet)

Parameter		Symbol	Min	Typ	Max	Units
Passband (to -3 dB corner)	(Fs is conversion freq.)		0	-	0.476Fs	Hz
Passband Ripple			-	-	±0.1	dB
Transition Band			0.442Fs	-	0.567Fs	Hz
Stop Band			≥ 0.567Fs	-	-	Hz
Stop Band Rejection			50	-	-	dB
Stop Band Rejection with Ext. 2Fs RC filter			57	-	-	dB
Group Delay			-	12/Fs	-	s
Group Delay Variation vs. Frequency			-	-	TBD	µs

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	||VA+| - |VD+||		-	0.4	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD+)+0.4	V
Ambient Operating Temperature (power applied)		T_{Amax}	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

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RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0V; all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.50	5.0	5.50	V
	Positive Analog	VA+	4.50	5.0	5.50	V
	||VA+| - |VD+||		-	-	0.4	V
Ambient Operating Temperature		T_A	0	-	70	°C

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VD+ = 5V ± 10%; measurements performed under static conditions.)

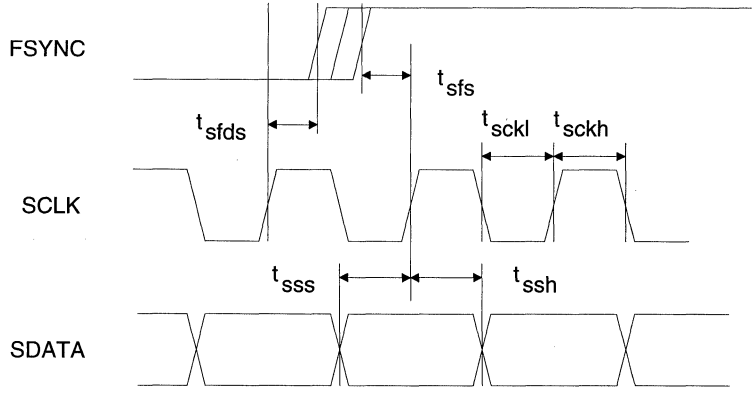
Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-		V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_o = -2.0mA	V_{OH}	2.4	-	-	V
Low-Level Output Voltage at I_o = 2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	1.0	µA.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = GND, Logic 1 = VD+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
SCLK Frequency			-	-	12.5	MHz
SCLK Pulse Width Low		t_{sckl}	25	-	-	ns
SCLK Pulse Width High		t_{sckh}	25	-	-	ns
SCLK rising to FSYNC edge delay	(Note 2)	t_{sfds}	20	-	-	ns
SCLK rising to FSYNC edge setup	(Note 2)	t_{sfs}	20	-	-	ns
SDATA valid to SCLK rising setup	(Note 2)	t_{sss}	20	-	-	ns
SCLK rising to SDATA hold time	(Note 2)	t_{ssh}	20	-	-	ns

Notes: 2. The table above assumes data is output on the falling edge and latched on the rising edge. The SCLK edge is selectable in setting the EDG bit in the ASICN register. The diagram is for EDG = 1.



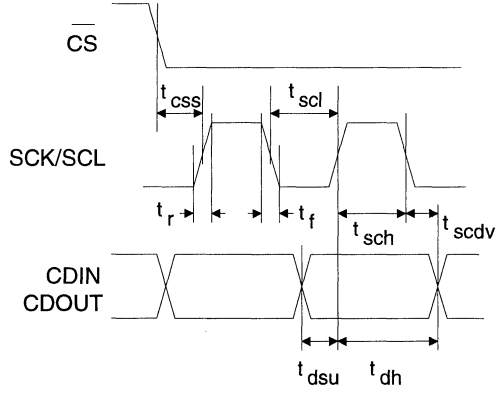
Serial Audio Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Max	Units
SPI Mode ($\overline{CS}$ = 0)				
SCK/SCL Clock Frequency	fscl	0	350	kHz
CS High Time Between Transmissions	tcsh	1.0		µs
CS Falling to SCK/SCL Edge	tcss	20		ns
SCK/SCL Low Time	tscl	1.1		µs
SCK/SCL High Time	tsch	1.1		µs
CDIN and CDOUT to SCK/SCL Rising Setup Time	tdsu	250		ns
SCK/SCL Rising to CDIN Hold Time (Note 3)	tdh	0		µs
SCK/SCL Falling to CDOUT Invalid	tscdv	300		ns
Rise Time of Both CDIN and SCK/SCL Lines	tr		1	µs
Fall Time of Both CDIN and SCK/SCL Lines	tf		300	ns

Notes: 3. Data must be held for sufficient time to bridge the 300ns transition time of SCK/SCL.



SPI Control Port Timing

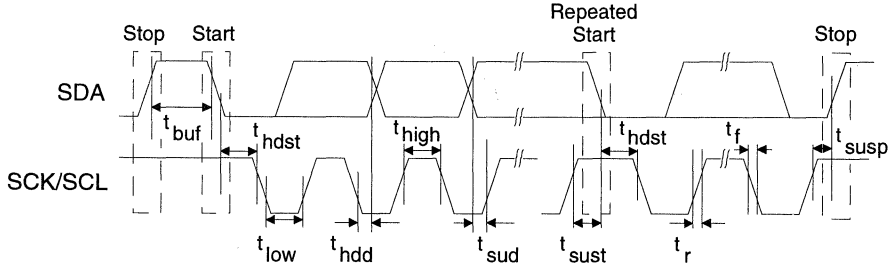
SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25 °C; VA+, VD+ = 5V; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20pF)

Parameter		Symbol	Min	Max	Units
I^2C® Mode	Note 4				
SCK/SCL Clock Frequency		fscl	0	100	kHz
Bus Free Time Between Transmissions		tbuf	4.7		µs
Start Condition Hold Time (prior to first clock pulse)		thdst	4.0		µs
Clock Low Time		tlow	4.7		µs
Clock High Time		thigh	4.0		µs
Setup Time for Repeated Start Condition		tsust	4.7		µs
SDA Hold Time from SCK/SCL Falling	Note 5	thdd	0		µs
SDA Setup Time to SCK/SCL Rising		tsud	250		ns
Rise Time of Both SDA and SCK/SCL Lines		tr		1	µs
Fall Time of Both SDA and SCK/SCL Lines		tf		300	ns
Setup Time for Stop Condition		tsusp	4.7		µs

Note: 4. Use of the I^2C bus®compatible interface requires a license from Philips. I^2C bus® is a registered trademark of Philips Semiconductors.

Note: 5. Data must be held for sufficient time to bridge the 300 ns transition time of SCK/SCL.



I^2C® Control Port Timing

THEORY OF OPERATION

Introduction

The CS4920 is a complete audio subsystem on a chip. It consists of a general-purpose Digital Signal Processor (DSP), and a number of supplementary analog and digital blocks. These supplementary blocks include a programmable PLL clock multiplier, a serial audio input port, a CD quality stereo Digital-to-Analog Converter (DAC), an AES/EBU - S/PDIF compatible digital audio transmitter, and a serial control port. Figure 1 shows a typical connection diagram for the CS4920 in which a micro controller is used for loading the program code.

The CS4920 is based on a programmable DSP core. A typical application is the decoding of a compressed digital audio signal. Serial audio data broadcast on networks such as cable TV, direct broadcast satellite TV, or the telephone system can be decompressed and converted to standard analog and digital signals. A wide variety of standard and proprietary decompression algorithms can be supported. An assembler, a simulator, and a debugger are available. CS4920 DSP code is available which performs industry standard MPEG layers 1 and 2 and Dolby AC-2.

The DSP has a 24-bit fixed point data path, 4K words of program RAM, and 2K words of data RAM. The execution unit has a 48-bit accumulator, and no input data registers. Typical ALU instructions read operands from memory and store results back to memory. Modulo and bit reverse addressing are supported. For a sample rate of 44.1 kHz, the DSP can provide 16.9 MIPS.

The CS4920 includes a flexible clock manager. This section allows clock inputs on CLKIN to range from 7 kHz to 30 MHz, while producing

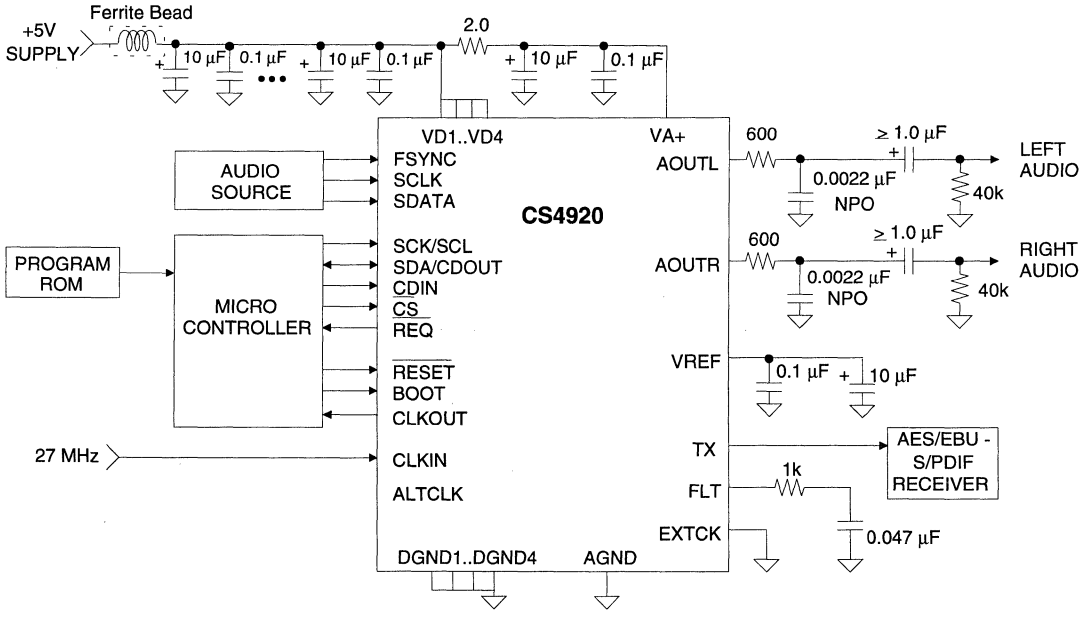


Figure 1. Typical Connection Diagram

the necessary DSP and DAC clocks through a programmable PLL.

The digital audio data is input through the serial audio port. Various formats are possible with the availability of three signal inputs and an internal control register.

For analog reproduction of the digital input, a stereo DAC using delta-sigma architecture is built-in. Switched-capacitor filters perform most of the reconstruction process. Only a simple external passive filter is needed to complete reconstruction.

In addition to the analog output, an AES/EBU - S/PDIF compatible output is provided. This allows the designer the flexibility of transmitting the audio data in a standard digital format to an external system.

To facilitate the downloading of DSP code to the CS4920, a serial control port, communicating in either I^2C® or SPI format, is used. This port may also be used in real time to issue control commands to the DSP.

PERIPHERALS

Five on-chip peripherals make the audio decoder ideal for decoding broadcast digital audio signals. It has a PLL clock manager, a CD quality DAC, a digital audio transmitter, a three pin serial port for inputting audio data, and an SPI/I^2C® port for serial control information. Each peripheral has I/O mapped data, control, and status registers. Many can also generate interrupts. A serial debug peripheral is provided to allow easy debugging of code.

Clock Manager

The clock manager consists primarily of a programmable clock multiplier circuit that takes a CLKIN input of any frequency from 7 kHz to 30 MHz and produces all the internal clocks required to run the DSP and the audio peripherals.

The clock manager generates a clock at a frequency of 128Fs (128 times the audio sample rate) or 192Fs. This clock is generated by the first PLL in the block diagram (Figure 2). It divides the CLKIN input frequency by M and multiplies it by N to produce the 128Fs (192Fs) clock. M is a 12 bit divider and N is 10 bit multiplier. The frequency range of the PLL is

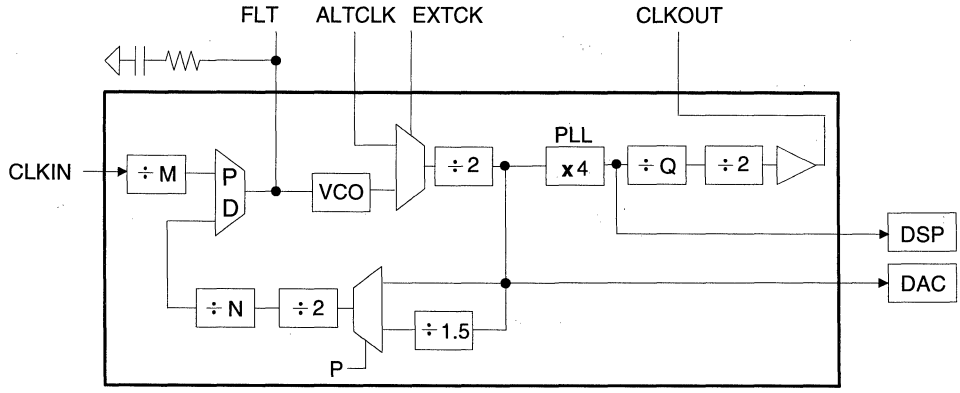


Figure 2. Clock Manager

25 kHz x 128Fs to 55 kHz x 192Fs. This corresponds to audio sample rates of approximately 25 kHz to 55 kHz.

The following table shows the proper N/M ratio to generate 128Fs or 192Fs.

CLKIN Frequency (kHz)	Fs	32 kHz	44.1 kHz	48 kHz
		128Fs or 192Fs (N/M)		
32		64/1	441/5	96/1
48		128/3	294/5	64/1
56		256/7	252/5	384/7
64		32/1	441/10	48/1
96		64/3	147/5	32/1
112		128/7	126/5	192/7
128		16/1	441/20	24/1
160		64/5	441/25	96/5
192		32/3	147/10	16/1
224		64/7	63/5	96/7
256		8/1	441/40	12/1
288		64/9	49/5	32/3
320		32/5	441/50	48/5
352		64/1	441/55	96/11
384		16/3	147/20	8/1
416		64/13	441/65	96/13
448		32/7	63/10	48/7
27000		256/3375	196/1875	128/1125
325Fs			(64/325)	

If the CLKIN input has a frequency equal to the compressed bit rate, all combinations of MPEG bit rates and sample frequencies are possible. Many other combinations are possible including CLKIN equal to 27 MHz with audio sample rates equal to 32 kHz, 44.1 kHz, and 48 kHz.

Following the generation of the 128Fs (192Fs) clock, a multiplexer places the 128Fs clock or the 192Fs clock on the internal clock line. This is selected through the P bit in the CM0 register. The resulting clock is provided to the DAC and determines the oversample ratio.

The second PLL, shown simply as a block in the figure, multiplies the 128Fs (192Fs) clock by 4 to generate the DSP clock. The PLL can produce DSP clock frequencies between 20 and 40 MHz. The following table shows some examples.

Sample Freq (kHz)	P	DSP Clock (MHz)
32	192Fs	24.576
44.1	192Fs	33.869
48	128Fs	24.576

The external clock (EXTCK) pin specifies the function of the ALTCLK. When EXTCK is low, the internal VCO of the first PLL is used to provide the 128Fs (192Fs) required. If EXTCK is high, an external oscillator connected to ALTCLK can be used to generate the 128Fs (192Fs) clock. Note the frequency of ALTCLK must be 256Fs or 384Fs due to the divide by 2 following the multiplexer controlled by EXTCK. This divide by 2 ensures a 50% duty cycle for the 128Fs (192Fs) clock generation. When an external VCO is used, the FLT pin drives an external loop filter. The filter output controls the VCO frequency and the VCO becomes the 128Fs (192Fs) clock.

CLKOUT is a divided version of the DSP clock. The DSP clock is divided by a programmable divider and an additional divide by 2 before being output. The divider value is stored in the ten bit register Q. The divide by two guarantees a 50% duty cycle. The frequency of CLKOUT can vary from the DSP frequency divided by 2 to the DSP frequency divided by 2048. CLKOUT can be used to synchronize external devices or generate most compressed bit rate clocks.

When the slow (SLW) control bit is low, the control voltage of the first PLL is pulled low. The second PLL always tracks the first PLL. After a reset, SLW must be set before the first PLL will lock. When the first PLL locks, the $\overline{\text{LOCK}}$ status bit in the Long Interrupt Register (LINT) goes low. If the first PLL loses lock, $\overline{\text{LOCK}}$ goes high. A low to high transition of $\overline{\text{LOCK}}$ gener-

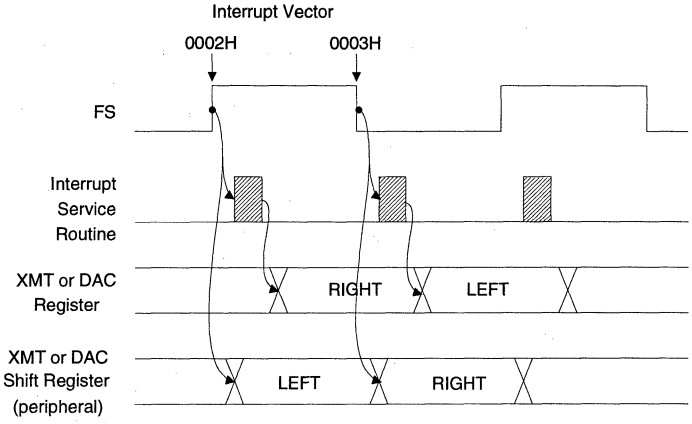


Figure 3. Transmitter Sequencing

ates interrupt 3 if the lock interrupt enable (LKIEN) bit is high.

The FS status bit is a 50% duty cycle sample rate clock. Transitions of this bit generate interrupt 0. The interrupt vector for a rising edge is 0002_H and the interrupt vector for a falling edge is 0003_H. This interrupt is used to write right and left audio data to the DAC register and the transmitter (XMT) register.

Loading of the DAC and XMT registers, and their respective shift registers, is initiated by FS transitions. Figure 3 shows the relationships. The left audio data is loaded into the shift registers on the rising edge of FS and the right audio data is loaded on the falling edge. Interrupt 0 occurs just after these shift registers are loaded. Right audio data should be loaded into the DAC and XMT registers by the instruction at 0002_H and left audio data should be loaded by the instruction at 0003_H.

FS is generated by dividing the 128Fs (192Fs) clock by 128 (192). This divider is reset when the FSRS control bit is high. The divider begins counting when FSRS goes low. This allows the programmer to control the phase relationship between input signals (FSYNC for instance) and FS.

The clock manager has two control registers, Clock Manager 0 (CM0) and Clock Manager 1 (CM1). Both registers are read/write except for the FS bit of CM0 which is read only. The following describes each bit.

Clock Manager 0 (CM0)

P: This bit is used to determine the oversample ratio of the DACs. When high, sample rate = 192Fs. When low, sample rate = 128Fs.

Q: Ten bit value which specifies the divide ratio between the DSP clock and CLKOUT.

FSRS: Sample rate clock reset. The sample rate clock, FS, is generated by the clock manager. The phase relationship between FS and external clocks such as FSYNC can be controlled by FSRS.

SLW: Slow. When low, the VCO control voltages are pulled low. This produces the lowest frequency out of the VCO's.

DACEN: DAC enable provides a zero value pattern to the DACs when this bit is low. When high, the audio to the DACs is enabled.

FS: Read only status bit which is a 50% duty cycle sample rate clock.

Clock Manager 1 (CM1)

N: Ten bit value which specifies the multiplier of the N/M ratio output to generate the 128Fs (192Fs) clock.

M: Twelve bit value used to divide the CLKIN input.

Long Interrupt Register (LINT)

$\overline{\text{LOCK}}$: Read only status bit which is low when the PLL is locked.

LKIEN: Lock interrupt enable. A rising edge of the $\overline{\text{LOCK}}$ status bit generates an interrupt if this bit is high.

Digital to Analog Converter

The digital to analog converter (DAC) is a dual channel CD quality DAC. It is designed with delta sigma architecture. The baseband audio is interpolated to 128Fs (192Fs) before going into the modulator. The modulator is third order and is followed by a 1 bit DAC/switch capacitor filter stage. An external passive filter completes the reconstruction process. The output is single ended with a drive capability of 8 kΩ. Figure 4 is a block diagram of the DAC.

The interpolation filter produces images which are attenuated by at least 56dB from .584Fs to 128Fs (192Fs). At a 48 kHz sample rate, a full scale signal at 20 kHz will produce an image at 28 kHz which is attenuated by more than 60dB.

The out-of-band quantization noise from the delta sigma modulator extends from .417Fs to 128Fs (192Fs). This noise is attenuated by the switch capacitor filter and the continuous time filters. The total quantization noise and thermal

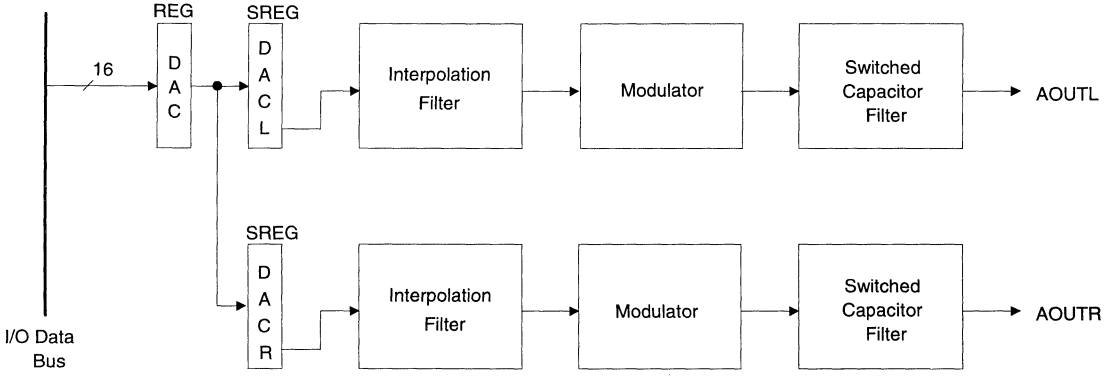


Figure 4. DAC

noise from the analog filters integrated over the .417Fs to 128Fs (192Fs) is more than 50dB below full scale power.

Left and right audio data are written to the DAC output register. This is a 16 bit write only register. The high 16 bits of the I/O data bus can be written to this register. The DACL and DACR output shift registers must be updated at the sample rate determined by the clock manager block. The FS status bit and the interrupt that it can generate can be used to time the updates of these registers.

During Power Down, the internal voltage reference is powered off. Therefore, the outputs of the DACs will not be driven during this period. The recovery of the reference from Power Down is sufficiently slow to prevent the outputs from "popping". Feeding all zeros to the DAC will produce a signal level of typically 2.1 volts.

Digital Audio Transmitter

The transmitter encodes digital audio data according to the Sony Philips Digital Interface Format (S/PDIF) or the AES/EBU interface format. The encoded data is output on the TX pin. More information on the S/PDIF and AES/EBU standards are available in the applications notes found in the back of this data book. The block diagram of the transmitter is shown in Figure 5.

The transmitter has a 24 bit write only register for audio data (XMT), a 16 bit read/write register for channel status data (XMTCS), and a read/write control register (XMTCN). The audio

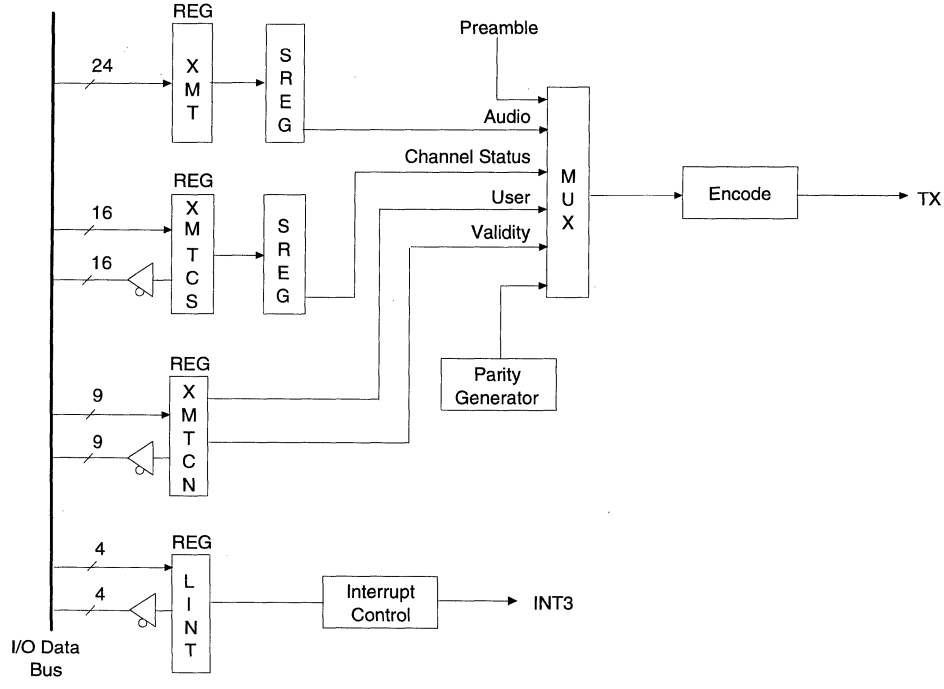


Figure 5. Digital Audio Transmitter

and channel status data are read from their registers and multiplexed with the validity and user bits from the control register, and the internally generated parity bit.

Channel status data can be input in two different modes determined by CSMD in register XMTCN. In the first mode, XMTCS stores the 16 most important channel status bits according to the S/PDIF standard. These are bits 0-5, 8-15, 24, and 25. Bit 0 must be low, this defines the consumer format for the channel status. Bit 1 defines whether the information being transferred is audio or non-audio data. Bit 2 is the copy bit. Bits 3 through 5 are the emphasis bits. Bits 8 through 15 define the category code and whether the data is from an original or copied source. Bits 24 and 25 define the sample frequency. A more detailed description of these bits is available in the application notes mentioned earlier in this section.

The XMTCS register must be loaded once by the programmer and is read once per block by the transmitter. All other bits are transmitted as zero. The LSB of the XMTCS is the LSB of the channel status bits.

The CBL status bit in LINT goes high at a channel status block boundary. XMTCS is loaded into the shift register by the transmitter at the same time. Just after this transition of CBL, interrupt 3 will be generated if the CBL interrupt enable (CBIEN) bit is set. If the interrupt is enabled, CBL is cleared only by reading LINT. If the interrupt is disabled, CBL transitions low after four left and four right bytes of channel status has been transmitted.

In the second channel status mode, all the bits in a block can be controlled. XMTCS is loaded every 16 subframes and is serially shifted into 16 transmitted subframes. This allows independent control of both channels.

The BYTCK status bit in LINT transitions high at a block boundary and every 16 subframes afterwards. XMTCS is loaded into the shift register by the transmitter at the same time. Just after this transition of BYTCK, interrupt 3 will be generated if the BYTCK interrupt enable (BYIEN) bit is set. If the interrupt is enabled, BYTCK is cleared only by reading LINT. If the interrupt is disabled, BYTCK transitions low after eight subframes of channel status have been transmitted.

The XMT register is loaded into the shift register of the transmitter at twice the sample rate specified in the clock manager. The right channel is loaded into the shift register on the falling edge of the FS status bit and the left channel is loaded on the rising edge. The XMT register is timed to be loaded by the transmitter at the same time that the DAC reads the DAC register. Interrupt 0 occurs just after a transition of FS. The interrupt vector address is different for rising and falling edges. Short interrupts can be used to write left and right audio data to the XMT register.

Audio data can be written to both DAC and XMT in the same instruction if the DADR bit in the transmit control register (XMTCN) is high. This causes XMT to respond to both DAC and XMT register addresses.

The validity (V) and user (U) bits in XMTCN are read by the transmitter at the same time XMT is read. These bits are transmitted with the audio data.

Transmitter control register (XMTCN)

XMTCN is a read/write control register. A description of each bit follows:

V: Validity bit.

U: User bit.

DADR: DAC address. When high, XMT responds to the addresses of DAC and XMT.

OE: Output Enable. When high, TX is enabled. When it is low, TX is low.

CSMD: Channel Status Mode. When low, XMTCS is read once per block. When high, XMTCS is read every 16 subframes.

BLKST: Block Start. A low to high transition specifies a new channel status block boundary.

TSTP: Test Mode. Must be set to zero for normal operation.

TSTDAC: Test DAC. When high, digital output from DAC is output through TX. Normal data transmission is disabled.

DACLRB: Left/Right bit of DAC. Special test bit intended for test purposes only.

Long Interrupt Register (LINT)

BYIEN: BYTCK Interrupt Enable. When high, a low to high transition of BYTCK generates interrupt 3.

CBIEN: CBL Interrupt Enable. When high, a low to high transition of CBL generates an interrupt 3.

BYTCK: Byte Clock. Status bit which is the channel status byte clock. It is high for 8 subframes and low for 8 subframes. See text for acknowledgment protocol of interrupts.

CBL: Channel status Block clock. Status bit which goes high at the block boundary and low 64 subframes later. See text for acknowledgment protocol of interrupts.

Audio Serial Input Port

The audio serial input port has a three pin interface consisting of FSYNC, SCLK, and SDATA. SCLK clocks SDATA (serial data input) into the 24 bit input shift register. The contents of this shift register can be loaded into the Audio Serial Input (ASI) register by transitions of FSYNC or by a counter time out. An interrupt can be generated when ASI is loaded. Figure 6 shows a block diagram of the audio port.

The pulse mode (PUL) control bit in the audio serial port control register (ASICN) specifies whether both edges (PUL=0) or one edge (PUL=1) of FSYNC loads ASI. When configured to load on both edges, normal mode, up to

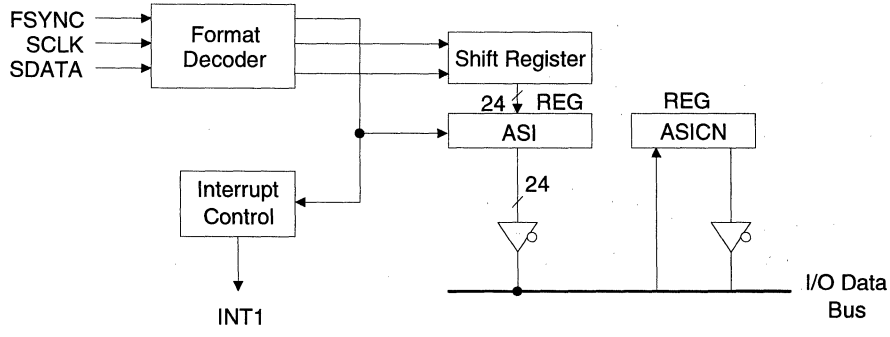


Figure 6. Audio Serial Input Port

24 bits of data after a transition of FSYNC are clocked into the shift register. The next transition of FSYNC loads ASI with the contents of the shift register. Any number of SCLK periods can occur between FSYNC edges; the first 24 bits (or less) are accepted.

When the serial port is configured to load ASI on only one FSYNC edge, pulse mode, any number of SCLK periods can occur between active edges. ASI will be loaded on the active edge of FSYNC and every 16 or 24 SCLK periods after an active edge of FSYNC. The CNT16 bit in ASICN selects between 16 and 24 SCLK's. If FSYNC never toggles, ASI will be continuously loaded every 16 or 24 SCLK periods.

The serial data is typically entered into the port MSB first. If at least 24 SCLK's occur between the times that ASI is loaded, the MSB of the input data will be loaded into the MSB of ASI. If the number of SCLK's between the times that ASI is loaded equals 24 minus N, the MSB will be loaded into the MSB minus N location in ASI. Shifting in software may be required to align the data.

The delay (DEL) bit in ASICN shifts the timing between FSYNC and SDATA by one SCLK period. When DEL is low, the MSB of the data in should occur immediately following a transition of FSYNC. When DEL is high, the MSB should occur one SCLK period after a transition of FSYNC.

The edge (EDG) bit internally inverts SCLK. When EDG is low, the falling edge of SCLK latches SDATA into the shift register. When EDG is high, the rising edge of SCLK latches SDATA.

The polarity (POL) bit in ASICN inverts FSYNC. This switches the active edge of FSYNC in pulse mode. When not in pulse mode, FSYNC can be used to identify left and right channels of stereo audio data. When POL is low, FSYNC high identifies the left channel and when POL is high, FSYNC high identifies the

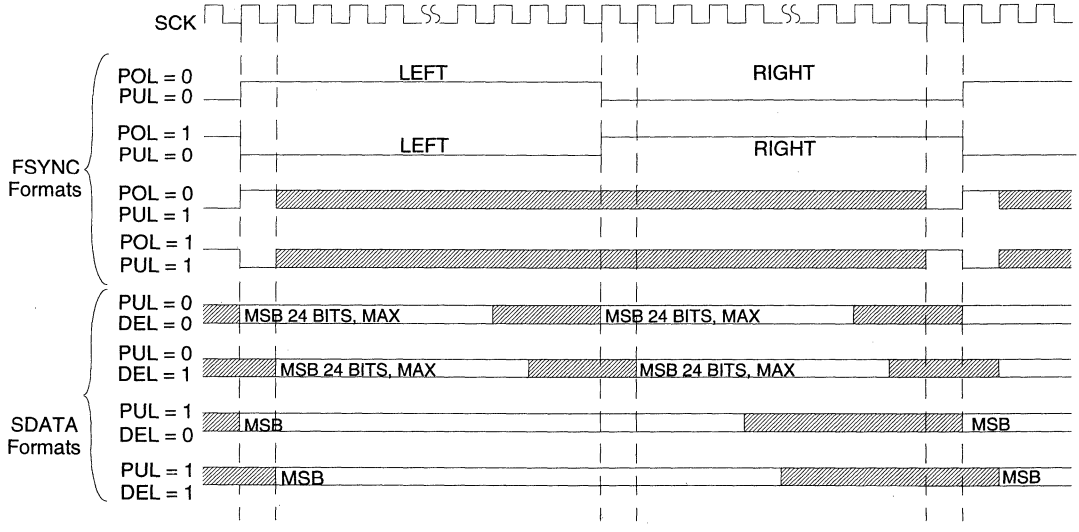


Figure 7. Audio Serial Input Formats

right channel. Figure 7 shows the timing relationships of the various formats.

Interrupt 1 (INT1) is asserted every time ASI is loaded if the interrupt enable (IEN) bit in the Control Register is high and the interrupt mask ($\overline{MSK1}$) is high. The interrupt vector address is determined by the state of FSYNC just after ASI is loaded. When the port is configured to load ASI on both edges of FSYNC, the interrupt vector for the interrupt just after a left data word is loaded into ASI is 0004_H. The interrupt vector for the interrupt just after a right data word is loaded is 0005_H. When the port is in pulse mode, the interrupt vector for an interrupt generated by a transition of FSYNC is 0004_H. The interrupt vector for an interrupt generated by the count out controlled by CNT16 is 0005_H.

Audio Serial Input Control Register (ASICN)

EDG: Edge. Specifies the SCLK edge which clocks SDATA. When low, the falling edge clocks data in.

POL: Polarity. Specifies the polarity of FSYNC. In normal mode, when POL is low, FSYNC high identifies the left channel. When POL is high, FSYNC high identifies the right channel. In pulse mode, when POL is low, the rising edge of FSYNC is active. When POL is high, the falling edge of FSYNC is active.

DEL: Delay. When DEL is low, there is no delay between an edge of FSYNC and the MSB of the audio data. When DEL is high, there is a one SCLK cycle delay between the edge of FSYNC and the MSB of the audio data.

PUL: Pulse mode. When PUL is low, FSYNC is a left/right signal. When PUL is high, FSYNC identifies the start of a frame but does not distinguish between left and right samples.

CNT16: Count 16. When high, ASI is loaded after 16 SCLK's. When low, ASI is loaded after 24 SCLK's.

FSI: Fsync internal. If the FSYNC pin is tied low and the POL bit is set low, this bit can be used to simulate FSYNC's function. A transition of this bit (controlled by software) from low to high will load the ASI register with the contents of the shift register.

Serial Control Port

The serial control port can operate in $I^2C^®$ or SPI compatible modes. In either mode, the control port performs eight bit transfers and is always configured as a slave. As a slave, it cannot drive the clock signal nor initiate data transfers. The serial control port is an asynchronous interface which provides interrupts and handshaking signals to allow communication between the on-chip DSP and an off-chip device such as a micro controller. Figure 8 shows a block diagram of the port.

The control consists of 5 pins, SCK/SCL, SDA/CDOUT, CDIN, $\overline{CS}$, and $\overline{REQ}$. SCK/SCL is the serial clock input which is always driven by an external device. SDA/CDOUT is the serial data I/O in the $I^2C^®$ compatible mode and the control data output in the SPI compatible mode. CDIN is the control data input in the SPI compatible mode. $\overline{CS}$ is the active low enable signal in the SPI compatible mode. $\overline{REQ}$ is the active low request signal. $\overline{REQ}$ goes low when the CS4920 wants to send information to an external controller.

The operating mode of the port during software execution is configured by bit M0 of the serial control port control register (SCPCN). If M0 is high, the port is SPI compatible. If M0 is low,

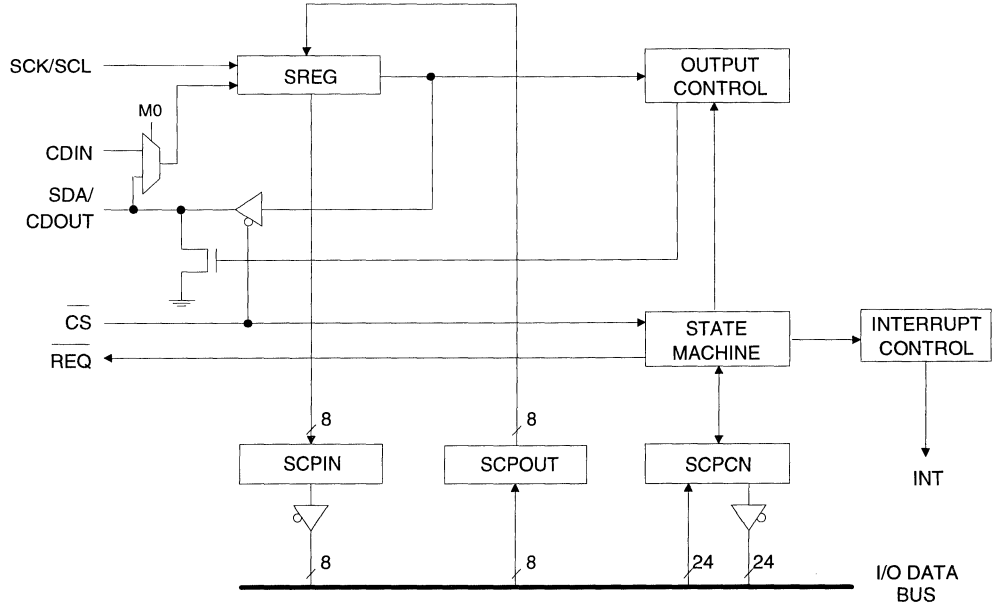


Figure 8. Serial Control Port

the port is $I^2C^®$ compatible. During a hardware or software reset, the port will be SPI compatible if $\overline{CS}$ is high and $I^2C^®$ compatible if $\overline{CS}$ is low.

As an $I^2C^®$ compatible port, data is communicated on the SDA pin and is clocked by the SCK/SCL pin. The Signetics $I^2C^®$ bus specification provides details of this interface. Figure 9 shows the basic timing relationships for data transfers. A transfer is initiated with a start condition followed by an address and a read/write bit. This address is the address of the device with which the master wants to communicate. This address is stored in SCPCN. If the addresses match, then a data transfer will occur in the direction specified by the read/write bit. If the address enable bit (AEN) is low, the address will not be checked. Following a reset, AEN is set low. This allows data to be communicated to CS4920 until the software initializes the port with a valid address.

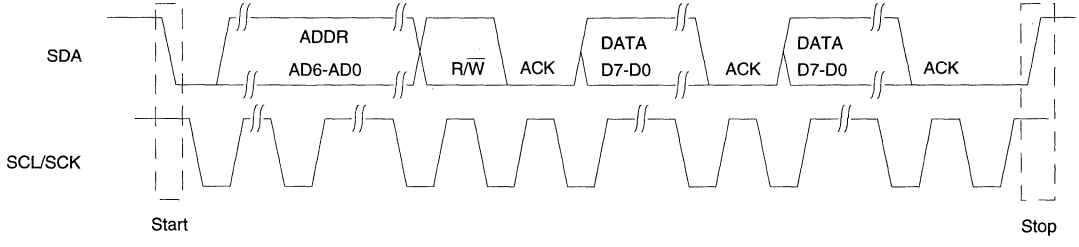


Figure 9 - Control Port Timing, $I^2C^®$ Mode

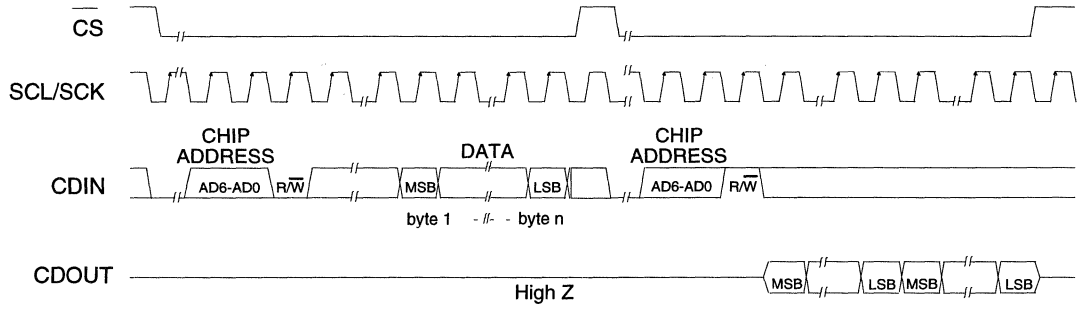


Figure 10. Control Port Timing, SPI mode

If a write to the CS4920 is specified, 8 bits of data on SDA will be shifted into the input shift register. When the shift register is full, the 8 bit data is transferred to the Serial Control Port Input register (SCPIN). An acknowledge is sent back to the master and the input ready flag (IRDY) is set. This flag generates an interrupt on interrupt line 2 if the input ready interrupt enable (IRIEN) bit is set high. The interrupt vector is 0006_H.

The master can continue to send data, but it will be rejected if the input ready (IRDY) has not yet been cleared. This flag is cleared by reading the SCPIN register. If a byte is rejected, the reject flag (REJ) in LINT is set. A rising edge of the REJ flag generates an interrupt on interrupt line 3 if the reject interrupt enable (RJIEN) bit is set high. The REJ flag is cleared by reading SCPCN.

If the DSP wants to send a byte to the master, it first writes the byte to the Serial Control Port Output register (SCPOUT). This sets the request pin ($\overline{REQ}$) and the output ready (ORDY) bit low. The master must recognize the request and issue a read command to the DSP. The serial control port must be sent the proper address (if address checking is enabled) and a read bit. After the ACK by the CS4920, the serial output register is loaded with the output data and the ORDY is set. This will generate an interrupt on interrupt line 2 if the output ready interrupt enable (ORIEN) bit is set high. The interrupt vector is 0007_H. The 8 bit value in the serial output register is then shifted out by the master. $\overline{REQ}$ will go high just prior to the last shift of the data transfer unless a new word has been loaded into the SCPOUT register.

The SPI compatible port is enabled by setting $\overline{CS}$ low. Figure 10 shows the basic timing relationships for this mode. When $\overline{CS}$ is low, data is written into the port through the CDIN pin and data is read out of the port through the CDOUT pin. The protocol, interrupts, and handshaking for the SPI mode operates the same as the $I^2C^®$ mode.

The SCPCN register is a read/write register. The following describes the function of each bit.

Serial Control Port Control Register (SCPCN)

ADDR: Address. Seven bit address of the audio decoder. (AD6 - AD0)

AEN: Address enable. When high, message address is compared to ADDR.

M0: Mode control. Low = $I^2C^®$; High = SPI.

IRIEN: Input ready interrupt enable. When high, low to high transition of IRDY generates interrupt 2. Interrupt vector = 0006_H.

ORIEN: Output ready interrupt enable. When high, low to high transition of ORDY generates interrupt 2. Interrupt vector = 0007_H.

IRDY: Input ready status bit. Read only. High when SCPIN is full.

ORDY: Output ready status bit. Read only. High when SCPOUT is empty.

FSTB: Fast mode bit. This bit is set low coming out of reset. When the bit is low, the SCP is configured to operate at much higher bit rates. This mode is useful for downloading the initial program to memory. When the bit is high the SCP conforms to the timing requirements of $I^2C^®$ and SPI formats.

Long Interrupt Register (LINT)

REJ: Reject status bit. Read only. High when input data rejected.

RJIEN: Reject interrupt enable. When high, low to high transition of REJ generates interrupt 3.

DSP ARCHITECTURE

Overview

The DSP core is a time multiplexed dual bus architecture. As shown in Figure 11, there are two static RAM blocks. The one labeled Data Memory typically contains buffered audio data and intermediate processing results. The block labeled Program Memory contains the entire program running at a particular time. Program Memory is also typically used to store filter coefficients.

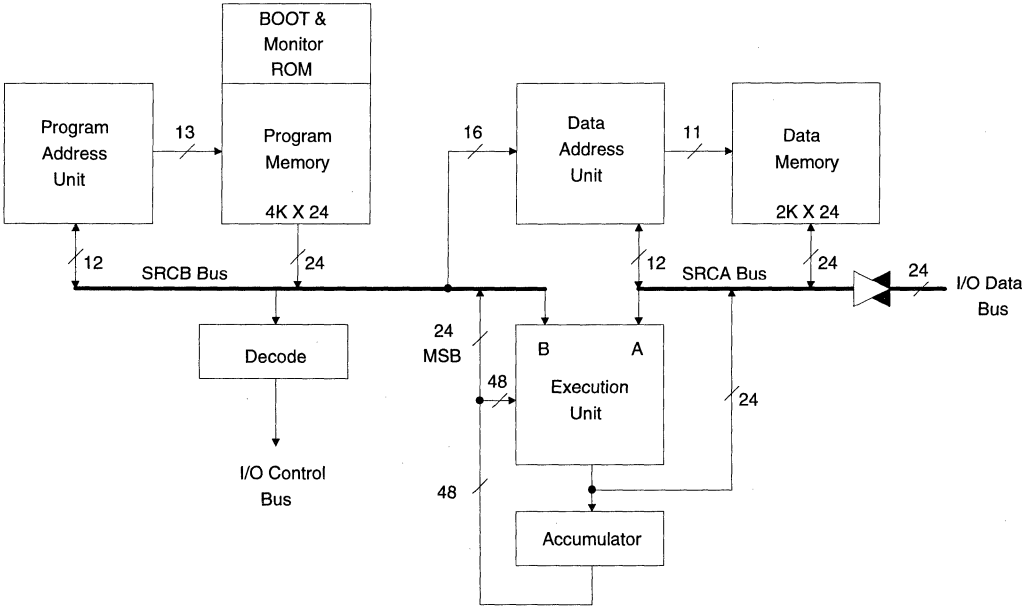


Figure 11. DSP Architecture

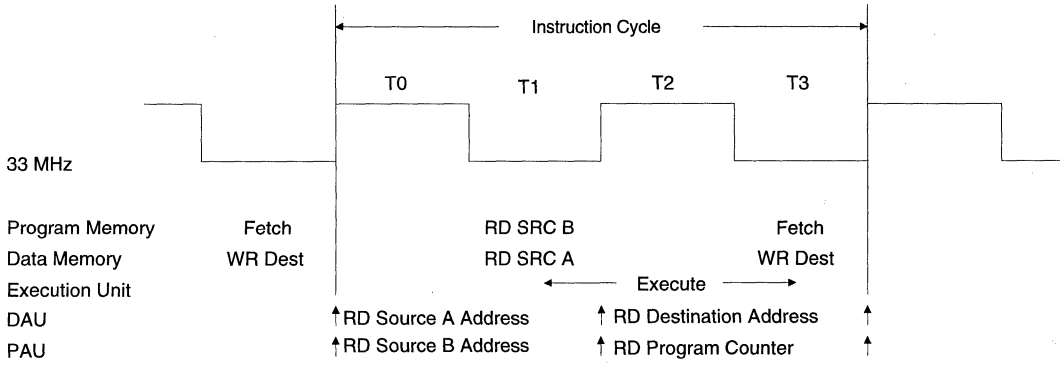


Figure 12. DSP Timing

All instructions take two clock cycles to complete. This timing is shown in Figure 12. During the first clock cycle, typically one operand is read from data memory and a second operand is read from program memory. During the second cycle, the result is stored in data memory and the next instruction is prefetched from program memory.

Results can be stored in program memory but an extra instruction is required. When a load program memory instruction (LD) is executed, the contents of the accumulator can be loaded into program space. During the first cycle of the instruction, the contents are transferred. During the second half, the next instruction is prefetched.

Processing occurs in four phases. In the first phase, the instruction in the instruction register is decoded. In the second phase, the A and B operands are read. In the third phase, the ALU operation is performed. In the fourth phase, the result is stored and the next instruction is prefetched.

Since there is no pipeline, no processing delays are seen by the programmer. The contents of an address register can be used as an indirect address during the instruction immediately after an instruction that modified the address register. Conditional jumps can occur immediately after an instruction that generated the condition code.

There are 2 busses in the DSP core, the source A--destination bus (SRCA) and the source B--instruction bus (SRCB). SRCA connects to the data memory, the data address unit (DAU), the input of the accumulator (ACC), the A input of the execution unit (EU), and the I/O data bus. SRCB connects to the program memory, the program address unit (PAU), the DAU, the output of the ACC, and the B input to the EU.

During the first half of a typical arithmetic or logical instruction, the A operand to the EU is put on the SRCA bus. This operand can come from the data memory, registers in the DAU, or I/O registers. During the second half of such an instruction, the result from the EU is put on the SRCA bus. This result can be written to a data memory location, a DAU register, an I/O register, or the ACC.

During the first half of the instruction described above, the B operand to the EU is put on the SRCB bus. This operand can come from program memory, registers in the PAU, or the ACC. During the second half of the instruction, the next instruction is fetched on the SRCB bus. Some fields of the instruction are latched and decoded in the decode block and some are latched and decoded in the DAU.

The instruction fields that are latched in the DAU specify where the A operand comes from.

It can come from registers in the DAU, data memory or I/O registers. When it comes from data memory, the DAU generates the operand's address. This address can be generated directly from bits in the instruction (direct addressing) or it can be generated from the contents of registers in the DAU (indirect addressing). Since both the address of the A operand and the destination must be provided for some instructions, the DAU can generate two addresses in one instruction cycle.

The Program Address Unit (PAU) contains registers which are used to generate program memory addresses. During the first half of an instruction, the generated address points to the B operand. During the second half of the instruction, the generated address points to the next instruction. Typically, the Program Address Registers (PAR's) are used to generate the B operand address, and the Program Counter (PC) is used to generate the next instruction address.

The Execution Unit (EU) shown in Figure 13, performs the operation specified in the instruction opcode on the A and B operands. It can perform the basic logical and arithmetic operations such as AND, OR, XOR, ADD, and SUBTRACT. For these instructions, it creates a 24 bit result from two 24 bit operands. It can also multiply, multiply and accumulate, multiply and subtract while accumulating, and perform a divide iteration. Since these instructions require double precision sources or destinations, a 48 bit accumulator register (ACC) is provided. A shifter on the output of ACC provides easy scaling operations.

5

Execution Unit

The Execution Unit (EU) is the main processing block in the DSP. As shown in Figure 13, it consists of an arithmetic logic unit (ALU), a 24 by 24 multiplier, a 48 bit adder, a 48 bit accumulator register (ACC), and a shifter. Transparent

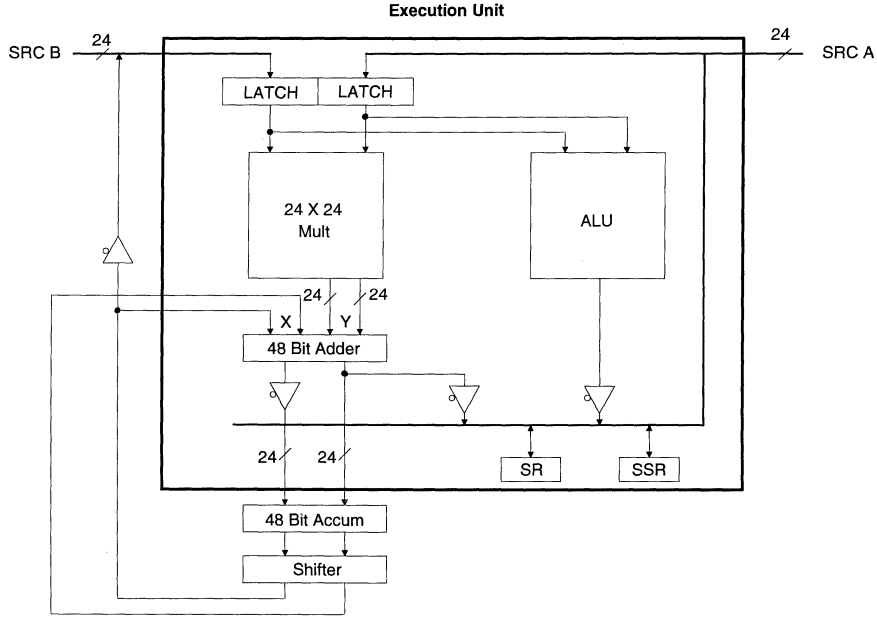


Figure 13. Execution Unit

latches and tristate buffers guide data through the EU at the proper times. There are no pipeline registers and no data registers other than ACC.

The logic unit performs AND, OR, and XOR functions. The NOT function can be performed by an XOR with $FFFFFF_H$. When a logic instruction is executed, 24 bit operands are read from the SRCA and SRCB buses and the 24 bit result is driven back onto the SRCA bus. If ACC is specified as the destination, the result gets written into the high 24 bits of ACC. The low 24 bits remain unchanged.

The high 24 bits of the adder perform the ADD, add with carry (ADDC), subtract (SUB), and subtract with carry (SUBC) instructions. The 24 bit operands are read from the SRCA and SRCB buses and the result is driven on the SRCA bus. The SUB and SUBC instructions subtract the SRCA operand from the SRCB operand. If ACC is specified as the destination, the result gets written into the high 24 bits. The low 24 bits remain unchanged.

The multiplier and adder are used in the following instructions: multiply (MPY), multiply and store low result (MPYL), multiply and add accumulator (MAC), multiply and add accumulator and store low result (MACL), multiply and subtract accumulator (MSU), and multiply and subtract accumulator and store low result (MSUL). When one of these instructions is executed, the 24 bit operands from SRCA and SRCB are first multiplied. This multiplication generates a 48 bit result. When MPY and MPYL are executed, zero is added to this 48 bit result. When MAC and MACL are executed, the 48 bit contents of ACC are added to the multiplication result. When MSU and MSUL are executed, the 48 bit result of the multiplication is subtracted from the ACC .

When ACC is specified as the destination, the low 24 bits of the result of a multiplication are always written to the low 24 bits of ACC. When MPY, MAC, and MSU are executed, the high 24 bits of the result are driven on the SRCA bus. If ACC is specified as the destination, these 24 bits get written into the high 24 bits of ACC. When MPYL, MACL, and MSUL are executed, the low 24 bits of the result of the addition are driven on the SRCA bus. If ACC is specified as the destination, the low 24 bits get written into both the high and low words of the accumulator.

The condition code flags are updated by the result of the 48 bit addition(subtraction) following the multiply, not by the data placed on SCRA or in the ACC.

The shifter on the output of ACC allows scaling of the accumulator (e.g. result of a filter convolution). The shift (SHF), and shift low (SHFL) instructions shift the 48 bit contents of ACC left by 1, 2, or 3 bits or right by one bit. The sign bit is extended during a shift right by one. When SHF is executed and ACC is the destination, the 48 bit result of the shift is stored in ACC. When SHFL is executed and ACC is the destination, the low 24 bits of the 48 bit result of the shift is written into both the low 24 bits and high 24 bits of ACC. When ACC is not the destination, the high 24 bits of the shift result are driven on SRCA during SHF and the low 24 bits during SHFL.

Barrel shifting left for 24 bit operands can be accomplished by multiplying by 2^N and storing the low result. Barrel shifting right can be accomplished by multiplying by $2^{(24-N)}$.

Divide instruction (DIV) divides the contents of the accumulator by the SRCA operand. It performs one iteration of a non restoring fractional division algorithm. DIV must be repeated 24 times to complete a 24 bit division. After 24 iterations, the high 24 bits of ACC contain the partial remainder and the low 24 bits contain the quotient.

The DIV instruction first XOR's the sign bits of SRCA and ACC. ACC is then shifted left by one bit with the carry bit (C) shifted into the LSB of ACC. Note on the first iteration, the C bit should be cleared. If the result of the previous XOR was one, SRCA is added to the high 24 bits of ACC and stored back in the high 24 bits. If the result was zero, SRCA is subtracted from the high 24 bits of ACC and stored back in the high 24 bits. The carry from the add or subtract properly sets the carry for the next iteration.

There are five status bits, V, C, Z, N, and U. These are located in the STATUS register which is described in the Control and Status Register section.

V is the overflow status bit. It is set when an addition, subtraction, or shift overflows. The V bit is cleared by writing a zero to it.

C is the carry flag. It is the carry out or borrow out of the 48 bit adder during an arithmetic instruction. The C bit is cleared by writing a zero to it.

Z is the zero flag. It is high if the result of an arithmetic or logical operation is zero. Z is updated by the 48 bit result of the multiply, divide, and shift instructions. Z is updated by the 24 bit results of the add, subtract, and logical instructions.

N is the negative flag. N is high if the MSB of the result is high. If the result represents a number, then N specifies whether it is positive or negative. During a MPYL, MACL, MSUL, or SHFL instruction, the low 24 bits of the result are put on the SRCA bus. During these instructions, N is determined by the output of the adder, not the data on the SRCA bus.

U is the unnormalized flag. U is high if the result of an arithmetic operation is unnormalized. The result is unnormalized if the MSB and the MSB minus one bits are the same. U is updated by the output of the 48 bit adder, not the data on the SRCA bus.

The following table summarizes the affected status bits by the various instructions.

	V	C	Z	N	U
AND			x	x	
ADD	x	x	x	x	x
ADDC	x	x	x	x	x
DIV		x	x	x	x
JMP					
JMPS					
LD					
MAC	x	x	x	x	x
MACL	x	x	x	x	x
MPY		0	x	x	x
MPYL		0	x	x	x
MSU	x	x	x	x	x
MSUL	x	x	x	x	x
MVD					
MVP					
NOP					
OR			x	x	
REP					
RET/RETI					
SHF	x	0	x	x	x
SHFL	x	0	x	x	x
SUB	x	x	x	x	x
SUBC	x	x	x	x	x
TRAP					
XOR			x	x	

5

Data Address Unit

As shown in Figure 14, the DAU consists of eight address registers (AR's), eight modulo address registers (MAR's), an increment/decrement unit, and part of the instruction register. Tristate buffers and multiplexors are used for data path control.

The instruction word can independently specify both the A operand and the destination. The A operand can be the contents of an AR or I/O register, or it can be a location in data memory. When it is a location in data memory, the instruction word can specify the seven LSB's of the data memory address (direct addressing) or an AR which contains the data memory address (indirect addressing).

When *direct addressing* is selected, AR0 is used as the A operand page register and AR1 is used as the destination page register. Bits 10 through 7 of the page register are used as the MSB's of the address. These four bits and the seven LSB's from the instruction word create the required eleven bit data memory address.

When *indirect addressing* is selected, the eleven LSB's of the specified AR create the required eleven bit data memory address. The twelve bit contents of the specified AR can be post incremented or post decremented. This updated value is written back into the AR at the end of the first half of the instruction cycle.

In addition, addressing may be specified to be bit reverse post increment or bit reverse post

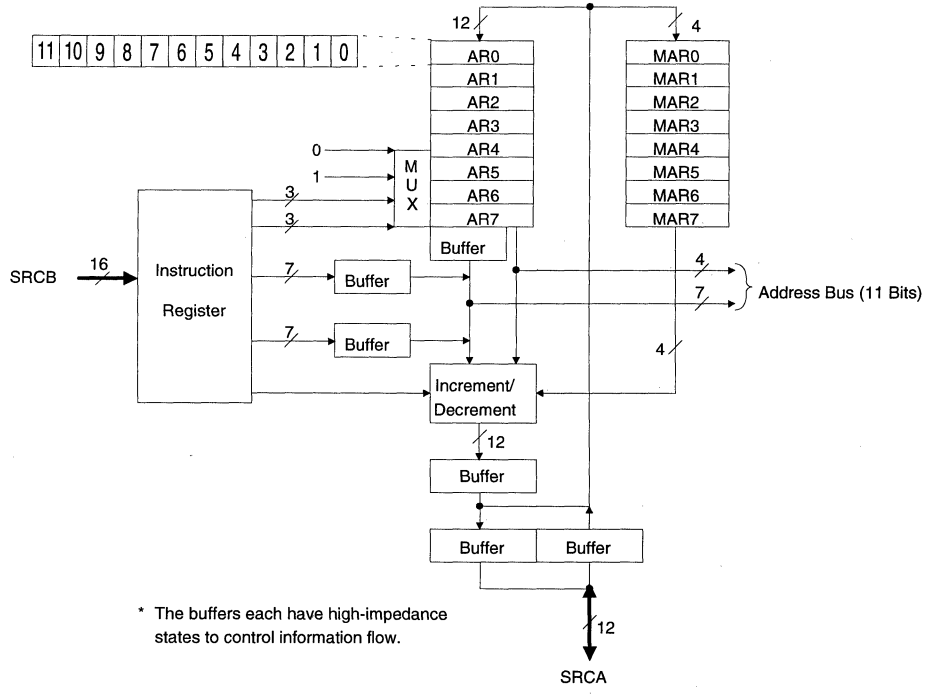


Figure 14. Data Address Unit

decrement. Bit reverse addressing is very useful for addressing the results of an FFT.

The result from the execution unit can be written to an AR, an MAR, an I/O register, the ACC, or any location in data memory. If an AR is the destination, the low twelve bits of the result are written into the 12 bit AR. If an MAR is specified as the destination, the four LSB's of the result are written into the 4 bit MAR. If the result is written to data memory, the memory address can be generated exactly the same as the A operand address. The destination address can be post modified exactly the same as the A operand address. The modified address is written back to the AR at the end of the second half of the instruction cycle.

Every address register (AR) has a corresponding modulo address register (MAR). The MAR can specify circular buffers or reverse carry address blocks. The value in the MAR specifies how many bits the carry is allowed to propagate through. When normal carry is specified, the carry propagates from the LSB to the Nth bit, where N is the value in the MAR. This means circular buffers of size 2^N that start at 2^N block boundaries can be created. When reverse carry is specified, the carry is injected at the Nth bit and propagated to the LSB. This provides reverse carry addressing to block sizes of 2^N starting at 2^N block boundaries.

All addressing options are specified in the instruction word and can be performed on the A operand address and the destination address.

Program Address Unit

The Program Address Unit (PAU) generates the 13 bit address for the program memory. It generates two addresses per instruction cycle. If the current instruction requires a source B address, the address generated during the first half is the B operand address. The address generated during the second half is the next instruction address.

Program memory consists of 4k words of RAM and 512 words of ROM. The ROM stores the boot and debug programs. The 13th address bit selects between RAM and ROM. The ROM space should not be accessed by the user.

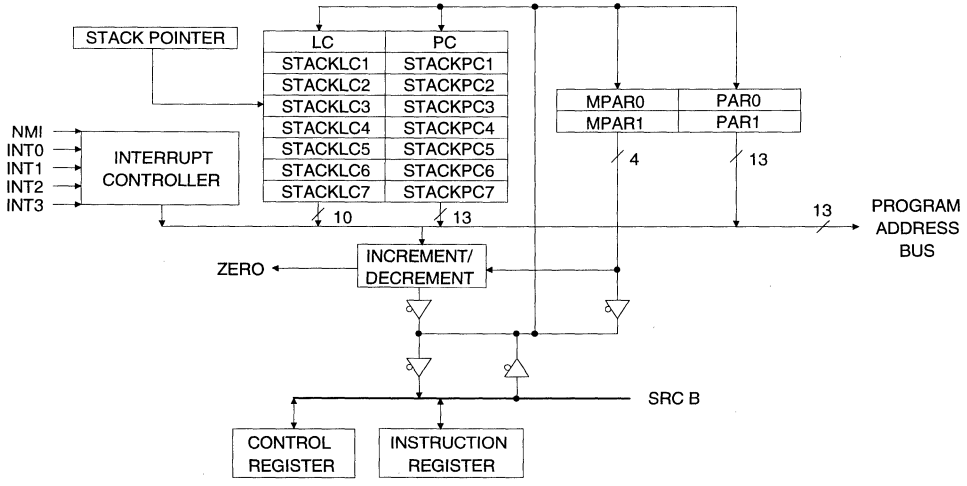


Figure 15. Program Address Unit

As shown in Figure 15, the PAU consists of two 13 bit Program Address Registers (PAR's), two 4 bit Modulo Program Address Registers (MPAR's), the 13 bit Program Counter (PC), a 10 bit Loop Counter (LC), and seven stack locations each for the PC and LC. There is also a stack pointer which points to the current PC and the current LC.

The next instruction address normally comes from the PC. After reading the instruction, the PC is incremented. During a jump instruction (JMP), the jump address comes from ACC or immediate short data. This address is loaded into the PC during the first half of the jump instruction. The next instruction is read from the new address in the PC.

When a jump-to-subroutine (JMPS) instruction is executed, the PC is incremented, the stack pointer is incremented, and the jump address is written to the new PC. When a return-from-subroutine (RET) is executed, the stack pointer is decremented and the next instruction is read from the old PC. Incrementing the stack pointer pushes the PC and LC to the stack and decrementing the stack pointer pops the PC and LC from the stack.

The load instruction (LD) and the repeat (REP) can load LC from the SRCB bus during the first half of an instruction cycle. Loading this register causes the next instruction to be repeated by the value in LC+1. Every time the next instruction is executed, LC is decremented. Since the PC does not have to be incremented, LC is decremented by the increment/decrement unit during the time which the PC is normally incremented. Instructions with immediate data cannot be repeated.

Looping can be accomplished by repeating a jump to subroutine instruction. Nested loops are possible since both the PC and LC are pushed onto the stack during a jump-to-subroutine. This type of looping has two instructions of overhead, the jump to subroutine and return instructions.

During the first half of an instruction, the B operand can be read from a program address register (PAR) or from program memory. During the second half of an instruction, the next instruction is prefetched. If the B operand comes from program memory, the address can come from the PC+1 (immediate addressing) or a PAR (indirect addressing).

If indirect addressing is specified, the contents of the specified PAR can be post modified. The value can be incremented or decremented. There is no reverse carry option. Although post modify can be specified in the instruction word, whether it is incremented or decremented is determined by the DEC bit in the control register. When DEC is high, the contents of the specified PAR is decremented.

Each PAR has an associated Modulo Program Address Register (MPAR). The MPAR's create circular buffers of length 2^N that start at 2^N block boundaries, where N is the value in the MPAR. This allows carries and borrows in the post modify increment/decrement unit to propagate from the LSB to the Nth bit only.

The PC, LC, PAR's, MPAR's, the control register, the top stack location and program memory pointed to by a PAR can be loaded from immediate data (13 bits) or from the accumulator in the Execution Unit. The LD (load) instruction loads them during the first half of an instruction cycle.

The PC, LC, PAR's, MPAR's, the control register, the top stack location and program memory pointed to by a PAR can be read by a move program (MVP) instruction.

Interrupts

There are five interrupt lines from the on-chip peripherals. They are interrupts 0 through 3 and a non-maskable interrupt. Interrupts 0 through 2 are used for outputting audio data, inputting

audio data, and transferring control information respectively. Interrupt 3 is used for reporting error conditions and updating channel status information in the digital audio transmitter. The non-maskable interrupt is used by the debugger.

Interrupts 0 through 3 can be enabled by setting the interrupt enable (IEN) bit in the control register. They can be individually disabled by clearing the corresponding mask bit ($\overline{\text{MSK}}$0-3) in the control register. The non-maskable interrupt is disabled by clearing the non-maskable interrupt enable (NMIEN) bit in the control register.

When an interrupt occurs, an interrupt vector generates the address of the next instruction. This interrupt vector address is unique for each interrupt. Interrupt 0 through 2 have two possible interrupt vector addresses.

Interrupt 0 occurs at twice the audio sample rate. The first time it occurs, the interrupt vector address is 0002_H and right audio data should be written to the DAC and the digital audio transmitter. The second time it occurs, the interrupt vector address is 0003_H and left audio data should be written to the DAC and transmitter. Refer to figure 12.

The audio data serial input port double buffers one input word. This word can contain up to 24 bits. The frame sync (FSYNC) input can differentiate between left and right data when stereo audio data is being input. When a new word is loaded into the double buffer, interrupt 1 occurs. The state of FSYNC determines whether the interrupt vector address is 0004_H or 0005_H. Typically, if left data has been loaded the address is 0004_H and if right data has been loaded, the address is 0005_H.

Interrupt 2 occurs when data is transferred through the serial control port. When data is transferred from an external micro controller to the DSP, the interrupt vector address is 0006_H. When data is transferred from the DSP to an external micro controller, the address is 0007_H.

Interrupt 3 is a wired OR of various conditions in the peripherals. The Long Interrupt Register (LINT) reports all conditions that generate interrupt 3. It also contains mask bits to individually enable each condition to generate an interrupt. The interrupt vector address is always 0008_H.

The debugger uses the non-maskable interrupt to suspend operation in the processor. When this interrupt occurs, control switches to the monitor program in ROM. The interrupt vector address is 1002_H.

The interrupts are priority encoded to prevent problems when multiple interrupts occur simultaneously. The non-maskable interrupt has a higher priority than the maskable interrupts. Of the maskable interrupts, line 0 has the highest priority and line 3 has the lowest priority.

An interrupt is detected by the program controller at the end of the instruction cycle during which the interrupt occurred. Since the next instruction has already been fetched, it is executed before the instruction at the interrupt vector location is executed. There is a one to two instruction cycle delay from the time the interrupt occurs until the instruction at the interrupt vector location is executed.

Interrupts can be long or short. A short interrupt occurs if the instruction at the interrupt vector location is anything but a JMPS(jump to subroutine). After this instruction is executed, program control switches back to normal. The instruction at the interrupt vector location cannot have immediate data.

A long interrupt occurs if the instruction at the interrupt vector address is a JMPS (jump-to-subroutine). When the jump occurs, the IEN (interrupt enable) bit in the control register is cleared. This disables interrupts. The IEN bit is

set when an RETI (return from interrupt) instruction is executed. The IEN bit can also be set and cleared by writing to the control register.

There is a hardware stack in the PAU which is 7 locations deep for both the program counter (PC) and the loop counter (LC). This allows 7 levels of subroutines and interrupts without a software stack for these counters. There is also one shadow status register which operates as a one deep hardware stack for the status register. Multiple levels of interrupts can be supported by implementing a software stack for the status register and by using short interrupts.

When a long interrupt occurs, the contents of the status register and the shadow status register swap. If a software stack is required, the contents of the shadow status register must be stored and interrupts enabled. Near the end of the interrupt service routine, interrupts must be disabled and the shadow status register restored. A RETI (return from interrupt) instruction swaps the contents of the status register and the shadow status register and enables interrupts. The status and shadow status registers do not swap when a short interrupt occurs.

If multiple levels of interrupts are not required or if the interrupt service routine does not affect the status register, the shadow status register does not have to be saved on the software stack. In this case, the contents of the status register and shadow status register are swapped when the interrupt occurs and again when the RETI is executed. Short interrupts do not swap the contents of the status and shadow status registers.

Instruction Set

The instruction set allows flexible addressing of two source operands and the destination. In one instruction the main ALU operation is performed and up to three memory address pointers can be updated.

The assembly code syntax is:

OPCODE SRCA, SRCB, DEST

For typical arithmetic and logical instructions SRCA is a location in data memory, an address register, or an I/O register. SRCB is a location in program memory, a program address register, or the accumulator. DEST is a location in data memory, an address register, an I/O register, or the accumulator.

Addressing modes can be register direct or register indirect for SRCA, SRCB, and DEST. SRCA and DEST memory locations can also be addressed directly. SRCB can also be immediate data.

The following examples of an ADD instruction illustrate possible addressing modes.

```
add *AR2+, *PAR0, *AR3+
/*SRCA=AR2 indirect with post increment;
SRCB=PAR0 indirect; DEST=AR3 indirect with
post increment*/

add *AR2, *PAR0m, *AR3
/*SRCA=AR2 indirect ; SRCB=PAR0 indirect
with post modify; DEST=AR3 indirect*/

add *AR2-, PAR0r, *AR3-
/*SRCA=AR2 indirect with post decrement;
SRCB=PAR0 register direct; DEST=AR3 indi-
rect with post decrement*/

add *AR2b+, 0x123456, *AR3b+
/*SRCA=AR2 indirect with bit reverse post in-
```

crement; SRCB=immediate; DEST=AR3 indirect with bit reverse post increment*/

add *AR2b-, ACC, *AR3b-
/*SRCA=AR2 indirect with bit reverse post decrement; SRCB=accumulator; DEST=AR3 indirect with bit reverse post decrement*/

add *AR2b-, ACC , *AR3b+
/*SRCA=AR2 indirect with bit reverse post decrement; SRCB=ACC; DEST=AR3 indirect with bit reverse post increment*/

add AR2, ACC, AR3
/*SRCA=AR2 register direct; SRCB=ACC; DEST=AR3 register direct*/

add MAR2, ACC, MAR3
/*SRCA=MAR2 register direct; SRCB=ACC; DEST=MAR3 register direct*/

add 0x19, ACC, 0x27
/*SRCA=direct address, AR0 is the page register; SRCB=ACC; DEST=direct address, AR1 is the page register*/

add 0x19, ACC, ACC
/*SRCA=direct address, AR0 is the page register; SRCB=ACC; DEST=ACC*/

Any combination of addressing modes for SRCA, SRCB, and DEST are permitted.

Figure 16 illustrates the processor programming model. It shows all registers and memory, and the bus attached to each.

All registers and memory locations on bus A can be used as the SRCA operand or as the destination. The MPAR's, the PAR's, the accumulator, and program memory space can be used as the SRCB operand.

The LD (load) instruction can write the contents of the accumulator or immediate short (13 bits) data to a PAR, an MPAR, the control register(CR), the program counter (PC), the loop counter (LC), and the last PC and REP pushed onto the stack (PC-1 and LC-1). It can also write the contents of the accumulator or immediate short data to program memory pointed to by a

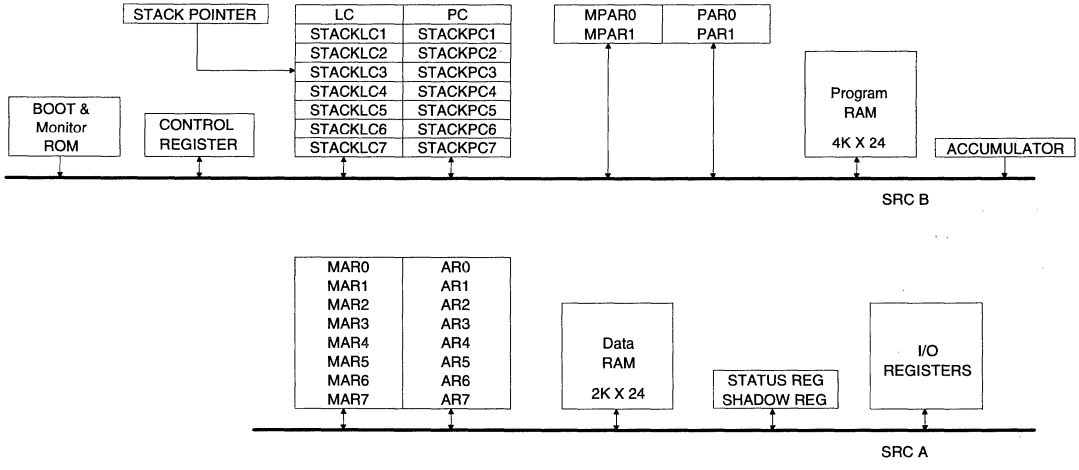


Figure 16. Programming Model

PAR. The specified PAR can be post modified or not post modified.

The MVP (move program) instruction can move immediate long data, the accumulator, a PAR, an MPAR, the CR, the PC, the LC, the PC-1, and the LC-1 to any destination described in the ADD example above. It can also move program memory pointed to by an PAR to any destination described above and any of the stack pointer locations (STACKPC[0-7] and STACKLC[0-7]). The specified PAR can be post modified or not post modified.

The contents of the stack pointer can be accessed by reading bits 5 through 7 of the Status Register. Bits 5 through 7 of the Shadow Status Register are always low.

Boot Procedure

Program and data RAM must be loaded from external memory after power up or when a new program needs to be loaded. During the loading procedure (boot), data is transferred through the serial control port to program and data memory. This procedure is controlled by a program stored internally in ROM.

Following a power up or reset, the fast mode bit (FSTB) is cleared. This places the CS4920 into a 'fast mode'. While the serial control port (SCP) still conforms to the data format determined by $\overline{CS}$ on power up, the port can be operated at much higher bit rates to facilitate faster downloading of the DSP code. Once the code has been loaded the software can set the FSTB for normal communication in either SPI or $I^2C^®$. Since the CS4920 is always a slave this fast mode will not affect the operation of other devices sharing the same communication bus.

The boot procedure is initiated by a low to high transition of the reset ($\overline{RESET}$) pin with the BOOT pin tied high. This initializes the program counter to location 1000_H, the first location in ROM. After the ROM program transfers data from the control port to memory, it issues a software reset. This is done by writing a one to the RS (reset) bit in the control register. The software reset clears all registers including the program counter, which transfers control to the new program in RAM.

A hardware reset ($\overline{RESET}$ pin toggled low) has the same affect as a software reset. During the boot procedure, all interrupts, except the debug interrupt, are disabled.

The serial control port will boot from a micro controller. When booting, it can communicate in an $I^2C^®$ or SPI format. If the $\overline{CS}$ (chip select) pin is high when boot is initiated, the port will communicate in SPI format. If the $\overline{CS}$ pin is low when boot is initiated, the port will communicate in $I^2C^®$.

Nodes in an $I^2C^®$ network have unique network addresses. A message in an $I^2C^®$ network consists of the address of the node receiving the message followed by the message data. When the control port is configured for $I^2C^®$ format, it normally compares the address to an address stored in an internal register. During the boot procedure, the control port is programmed to ignore the address.

The boot program in internal ROM expects data transferred through the control port to have the proper file format. The first two bytes contain the starting address for the following block of data. The starting address is 13 bits with the 13th bit specifying program or data memory. Therefore, the upper 3 bits of these two bytes are discarded internally. The second two bytes contain the length of the block of data. Successive bytes are concatenated into 24 bit words. These words are sequentially loaded into program and data memory beginning at the starting address.

Any number of blocks of data can be loaded. Two bytes containing FF and 3 bytes containing

a check sum must follow the last block of data. This check sum is generated by summing all the previous data, address, and length bytes and truncating to 24 bits. This check sum is compared to the value calculated internally. If they do not match, the $\overline{REQ}$ (request) pin is pulled low and the processor does not issue the software reset. It stays in a loop until boot is initiated again.

Control and Status Registers

The Status Register is connected to the SRCA bus. Since it is I/O mapped, it can be used as the SRCA operand or destination for most ALU operations. The control register is connected to the SRCB bus. It is loaded by the LD (load) instruction and can be read by the MVP instruction. The contents of each register are described below.

I/O Address Space

I/O address space consists of peripheral input and output registers, peripheral control registers, and the Status and Shadow Status Registers. These registers can be used as the SRCA operand or as the destination. The assembly language

5

Status Register

Bit	Name	Function
23-8	(undefined)	
7-5	STPTR	Stack pointer Points to the current program and repeat counters
4	N	Negative
3	Z	Zero
2	V	Overflow
1	U	Unnormalized
0	C	Carry

Control Register

Bit	Name	Function
23-10	(undefined)	(must be programmed low)
9	NMIEN	Non-maskable interrupt enable. When low, non-maskable interrupts cannot occur. NMIEN is high after a reset.
8	PWDN	Power down. Writing a one puts the chip into a power down mode. The reset pin must be toggled to clear it. In power down mode, the processor stops functioning.
7	IEN	Interrupt enable. When high, interrupt lines 0 through 3 can occur.
6	TRACE	Trace mode enable. When high, the processor will enter single step mode.
5	$\overline{RS}$	Software reset. Writing a one resets the chip. All registers are cleared.
4	DEC	Increment/decrement. When set, the program address registers are decremented when post modify is specified. When clear, they are incremented.
0-3	$\overline{MSK}$0-3	Interrupt mask bits 0 through 3. When low, the corresponding interrupt line cannot interrupt the processor.

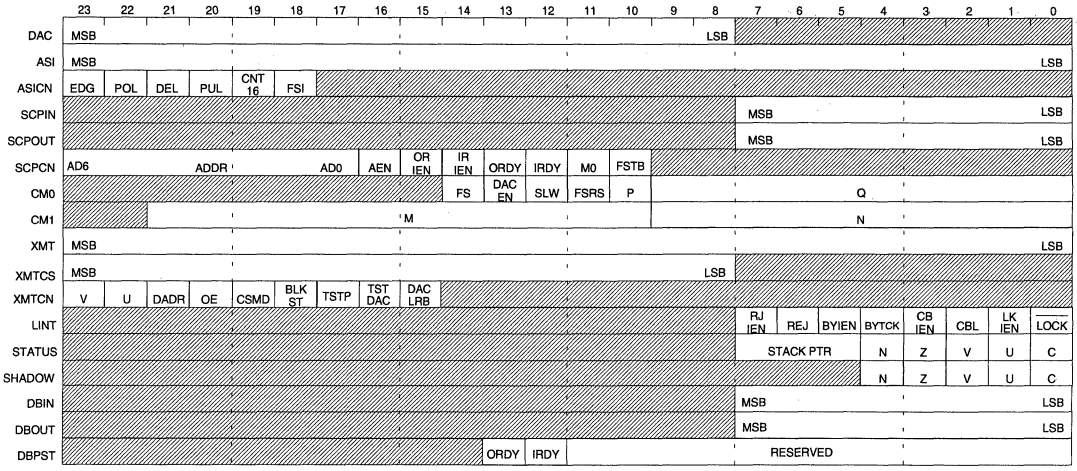


Figure 17. I/O Register Bit Map

syntax has a keyword for each register in I/O space. The following table summarizes these keywords and their respective register addresses.

Keyword	Register Addresses	Description
DAC	00000	DAC output register
ASI	00010	Serial input register
ASICN	00011	Serial input control register
SCPIN	00100	Serial control input register, read only
SCPOUT	00100	Serial control output register, write only
SCPCN	00101	Serial control port control register
CM0	00110	Clock manager control register 0
CM1	00111	Clock manager control register 1
XMT	01000	Audio transmit register
XMTCS	01001	Transmit channel status register
XMTCN	01010	Transmit control register
LINT	01011	Long interrupt register
STATUS	10000	Status register
SHADOW	10001	Shadow status register
DBIN	01100	Debug input register, read only
DBOUT	01100	Debug output register, write only
DBPST	01101	Debug port status register

Table 1. Register Summary

Figure 17 shows all I/O register bit assignments. These registers are described in the section which follows. Note that the Control Register described earlier is not included in Figure 17. This is because the Control Register is not an I/O mapped Register.

Debugger

The debugger consists of software and a cable which connects PC compatible parallel port to the debug port pins (DBCLK, DBDA), and an on-chip serial debug port and debug ROM. The computer can load programs, set breakpoints,

read and write registers and memory, and single step programs.

The debug ROM contains the interrupt service routine which interprets commands sent from the computer. Examples of these commands are "read register", "write register", or "set break point". The main program or the boot program is interrupted when the computer sends a command to the debug port. This causes program control to switch to the debug program.

This program polls the debug port for additional commands and performs the appropriate action. When a "run" command is issued, the program executes a RETI (return from interrupt) and program control switches back to the main program.

Breakpoints are set by replacing the instruction at the breakpoint location with a TRAP instruction. The TRAP instruction generates a debug interrupt when it is executed. Once the breakpoint has been set and the processors registers have been properly initialized, the user can issue a "run" command. The main program runs until the TRAP instruction is executed. Program control then switches back to the debug program.

The debug port and the TRAP instruction can generate a debug interrupt. This interrupt is a unique signal which can interrupt the processor independent of the state of the IEN control bit. This interrupt can be enabled or disabled by setting or clearing the NMIEN (non-maskable interrupt enable) control register bit. The default state is enabled. NMIEN is cleared when a debug interrupt occurs and it is set when an RTI instruction is executed. Writing to the control register can also change the state of NMIEN.

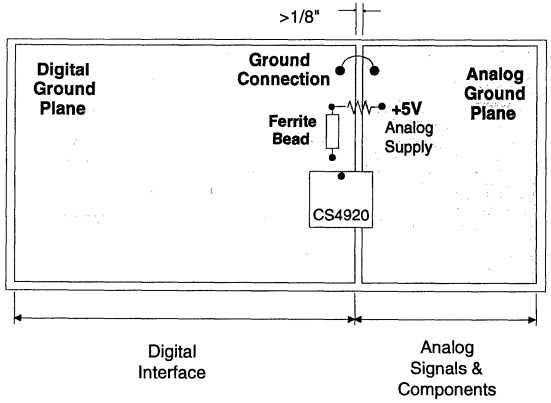
The high 32 words of data memory are used by the debug program.

5

POWER SUPPLY AND GROUNDING

When using separate supplies, the digital power should be connected to the CS4920 via a ferrite bead, positioned closer than 1" to the device (see Figure 18). The CS4920 VA+ pin should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 1.

The CS4920 should be positioned such that the analog pins (pins 29 - 39) are over the analog



Note that the CS4920 is oriented with its digital pins towards the digital end of the board.

Figure 18. CS4920 Suggested Layout

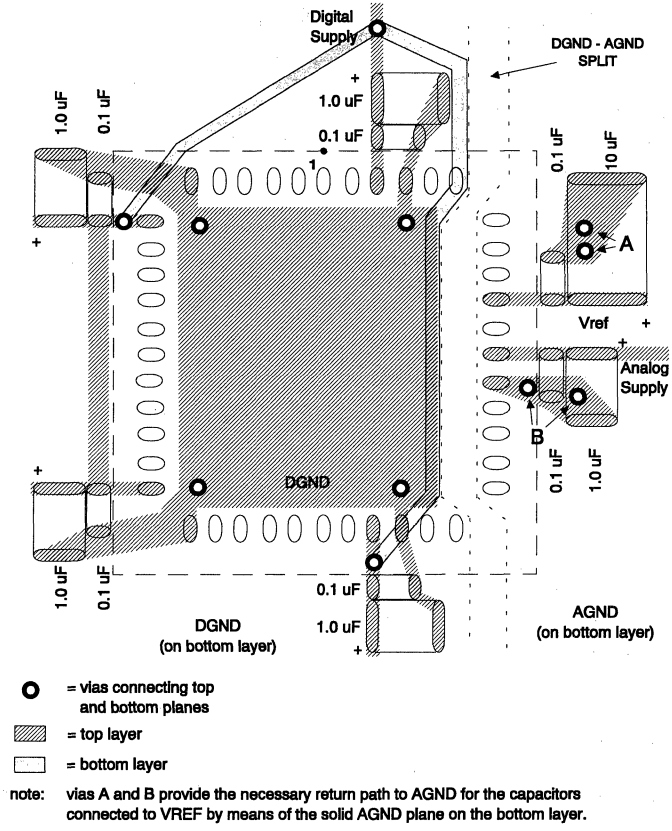


Figure 19. CS4920 Surface Mount Decoupling Layout

ground plane, while the rest of the pins lay over the digital ground plane as illustrated in Figures 18 and 19. The analog and digital grounds on the CS4920 are not connected internally; this should be accomplished externally through a point-to-point connection across the ground split as shown in Figure 18. A separate power plane for the chip is preferable.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4920 assuming a surface-mount socket and surface mount capacitors. Surface-mount sockets are useful since the pad locations are exactly the same as the actual chip; therefore, given that space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts mostly the top layer containing signal traces and assumes the bottom or inter-layer contains a solid ground plane (analog or digital), except where the digital supply needs to run to the power pins. The important points with regards to this diagram are that the ground plane is SOLID under the CS4920 and connects all ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is placed closest to the chip. Vias are placed near the AGND and DGND

pins, under the IC, and should be attached to the solid ground plane (analog or digital) on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces bringing the power to the CS4920 should be wide thereby keeping the impedance low.

If using through-hole sockets, effort should be made to find a socket with the minimum height which will minimize the socket impedance. When using a through-hole socket, the vias under the chip in Figure 19 are not needed since the pins serve the same function.

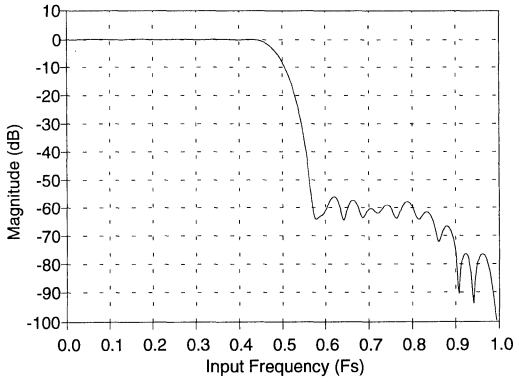


Figure 20. DAC Frequency Response.

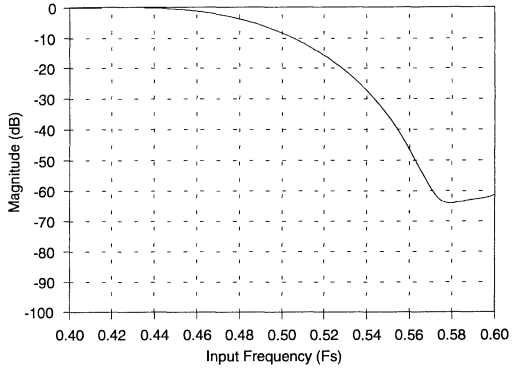


Figure 21. DAC Transition Band.

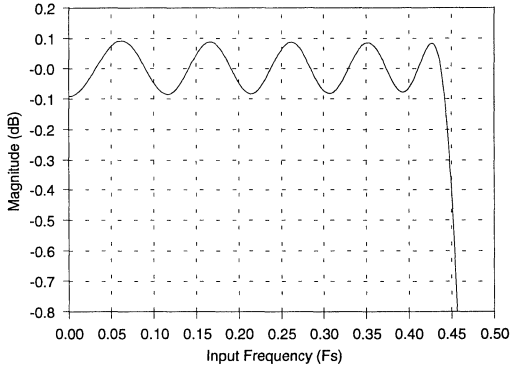


Figure 22. DAC Passband Ripple.

DAC Filter Response Plots

Figures 20 through 23 show the overall frequency response, passband ripple and transition band for the CS4920 DACs. Figure 23 shows the DACs' deviation from linear phase. Fs is the selected sample frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency. Fs is also the FSYNC frequency.

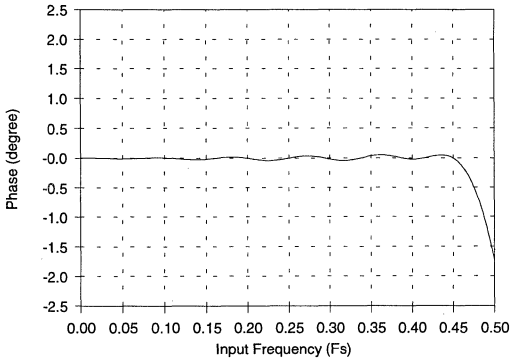
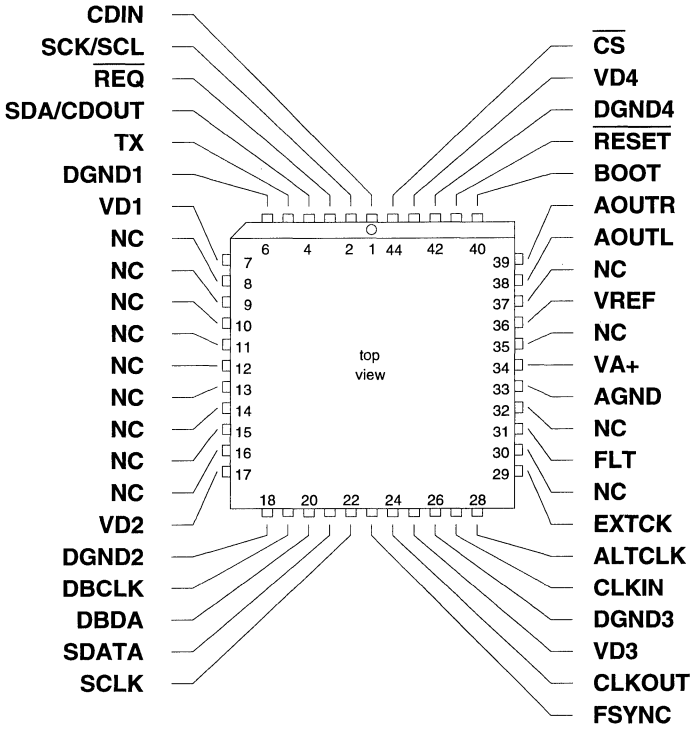


Figure 23. DAC Phase Response.

PIN DESCRIPTIONS



Power Supplies

VD1, VD2, VD3, VD4 - Positive Digital Power Supply, PINS 7, 17, 25, 43.

The +5V supply is connected to these pins to power the various digital subcircuits on the chip. See decoupling section in this data sheet for decoupling recommendations.

DGND1, DGND2, DGND3, DGND4 - Digital Ground, PINS 6, 18, 26, 42.

Digital power supply ground.

VA+ - Positive Analog Power Supply, PIN 34.

The analog +5V supply for the analog-to-digital converter and the PLL. Analog performance is highly dependent on the quality of this supply. See decoupling section in this data sheet for decoupling recommendations.

AGND - Analog Ground, PIN 33.

Analog power supply ground.

Digital-to-Analog Converter

AOUTL, AOUTR - Analog Outputs, Left and Right Channels, PINS 38, 39.

These DAC outputs are centered about the voltage at VREF. An external filter is required to diminish out-of-band noise.

VREF - DAC Voltage Reference, PIN 36.

This reference should be decoupled with 10µF and a 0.1µF capacitors to ground using minimum trace lengths. The 0.1µF capacitor should be closest to the pin.

Serial Audio Port

FSYNC - Frame Synchronization Clock Input, PIN 23,

FSYNC transitions delineate left and right audio data, or the start of a data frame, as determined by the PUL bit in the ASICN. The edge definition (left, right, or active) is determined by the POL bit.

SCLK - Serial Clock Input, PIN 22.

SCLK is used to clock the serial audio data on SDATA into the device. The EDG bit in the ASICN determines the active edge. The DEL bit can be used to delay data by one SCLK after an FSYNC transition.

SDATA - Serial Audio Data Input, PIN 21.

Audio data input to SDATA is clocked into the device by SCLK. There are several options for the relationships between SDATA, SCLK, and FSYNC.

Digital Audio Transmitter

TX - Transmit, PIN 5,

Biphase mark encoded data is output at logic levels from the TX pin. This output typically connects to the input of an RS-422 or optical transmitter. The port can support either AES/EBU or S/PDIF formats.

Clock Manager

CLKOUT - Clock Output, PIN 24.

CLKOUT can be used to synchronize peripheral devices such as a micro controller or an audio source. The clock frequency is determined by a divide by Q and a divide by 2 of the DSP clock. Q is a 10 bit register..

ALTCLK - Clock Input, PIN 28.

When EXTCK is high, ALTCLK is an input for an externally generated 128Fs or 192Fs clock.

EXTCK - External Clock Select, PIN 29.

Setting EXTCK high allows ALTCLK to be used as an input for an external VCO. Setting EXTCK low disables ALTCLK.

FLT - PLL Filter, PIN 31,

An RC low-pass filter (1.0 kΩ, 0.047μF) connected to this pin sets the control voltage for the on-chip VCO.

CLKIN - Clock Input, PIN 27.

A clock input to the CLKIN is used to synchronize the PLL's. The permissible frequency range is from 7 kHz to 30 MHz. It is typical to have SCLK for the audio data and CLKIN to be derived from the same clock source to avoid asynchronous noise between the audio source and the DSP.

Control

DBCLK, DBDA - Debug Clock, Debug Data I/O, PINS 19, 20.

These pins are used for serial port debug. DBCLK clocks the data into or out of the debug port. DBDA is a bi-directional data I/O. Software and a cable are available to interface the debug port to a PC.

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$\overline{\text{RESET}}$ - PIN 41.

The CS4920 enters a reset state while $\overline{\text{RESET}}$ is low. When in reset condition, all internal registers are set to 0, the digital audio transmitter, serial control port, and ALTCLK pin are disabled, and the stereo DAC is muted. The DAC is recalibrated and normal operation is resumed, one internal clock cycle after the rising edge of $\overline{\text{RESET}}$.

BOOT - PIN 40.

Boot enable pin. Pin must be set high to initiate the download of a program. While boot is high, $\overline{\text{RESET}}$ must be toggled low. This starts the internal boot program.

Serial Control Port

$\overline{\text{REQ}}$ - Request Output, PIN 3.

This pin is driven low when the DSP needs servicing from an external device. A write to the SCPOUT will cause the $\overline{\text{REQ}}$ to go low.

$\overline{\text{CS}}$ - Chip Select Input, PIN 44.

In SPI format, $\overline{\text{CS}}$ of the device the master wants to communicate with must be driven low. This pin also serves as the communication format select during a reset or power up. When CS is low during a reset or power up the SCP will be configured in $I^2C^®$ mode. When high, it is configured in SPI mode. The mode is selectable in software by setting the M0 bit in the SCPCN.

SCK/SCL - Serial Clock Input, PIN 2.

SCK/SCL clocks data into or out of the serial control port. This is always driven by an external device because the CS4920 is always the slave.

CDOUT/SDA - Control Data Output / Serial Data I/O, PIN 4.

In SPI mode, CDOUT is a data output for the serial control data. In I^2C interface mode, SDA is a bi-directional data I/O.

CDIN - Control Data Input, PIN 1.

In SPI mode, CDIN is the data input for the serial control port. It has no function in $I^2C^®$ mode.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth; expressed in LSBs.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Instantaneous Dynamic Range

The Signal-to-(Noise + Distortion) ratio (S/(N+D)) with a 1 kHz, -60dB from full scale DAC input signal, with 60dB added to compensate for the small signal. Use of a small signal reduces the harmonic distortion components of the noise to insignificant levels. Units are in dB.

Interchannel Isolation

The amount of 1kHz signal present on the output of the grounded input channel with 1 kHz, 0dB signal present on the other channel. Units are in dB.

Interchannel Gain Mismatch

The difference in output voltages for each channel with a full scale digital input. Units are in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Out of Band Energy

The ratio of the rms sum of the energy from 0.46×Fs to 2.1×Fs compared to the rms full-scale signal value. Tested with 48 kHz Fs giving a out-of-band energy range of 22 kHz to 100 kHz.

Semiconductor Corporation

CDB4920

CS4920 Evaluation Board

Features

- Demonstrates recommended layout and grounding arrangements
- Interfaces to parallel port of PC for easy programming and evaluation
- On-board or externally supplied system timing
- Accepts digital audio data transmitted either single-ended or RS-422
- Digital and Analog Patch Areas

General Description

The CDB4920 evaluation board provides an effective means to evaluate the CS4920 broadcast audio decoder. Compressed audio data can be input via one of two ribbon cable headers. The audio data is received either single-ended or according to the RS-422 standard. The decompressed data is output as analog and digital signals.

A ribbon cable header is provided to access the serial control port of the CS4920. Control can be accomplished by an external device, communicating in either I^2C or SPI format, such as a personal computer or micro controller. Software is available that uses the SPI format to download programs and issue control commands via the parallel port of an IBM compatible PC. An additional ribbon cable header is provided to access the CS4920's debug port.

ORDERING INFO: CDB4920

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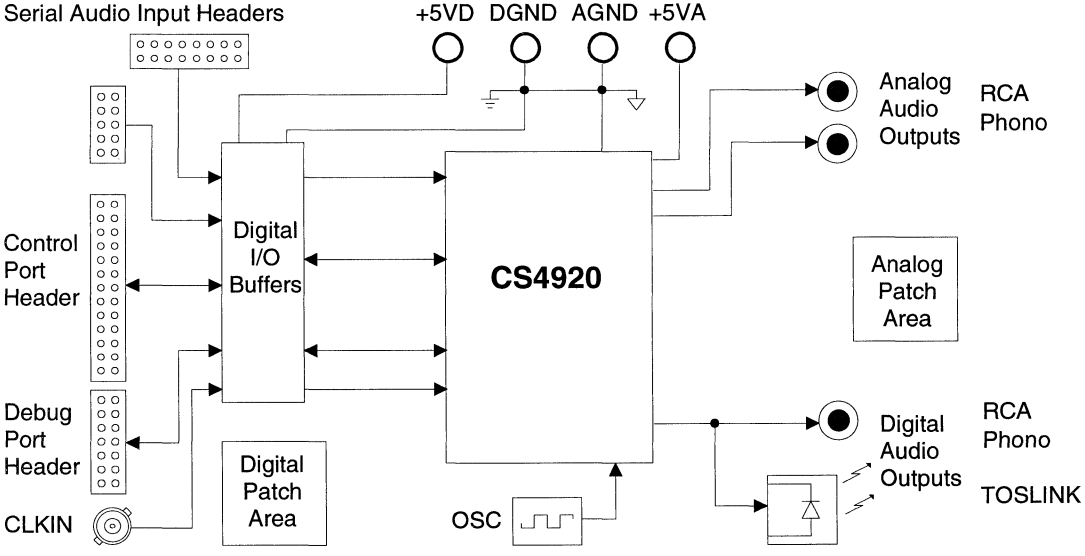

Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

• Notes •

Semiconductor Corporation

CS8905

Programmable Music Processor

Features

- Polyphonic up to 16 notes
- Multi-timbral up to 16 simultaneous timbres
- Oscillator frequencies to 48 MHz (46.875 kHz sampling rate)
- Stereo 16 bit digital audio output
- On-chip 256x15 Algorithm RAM, and 256x19 Parameter RAM
- Built-in sine and ramp data
- Addresses up to 1Mx12 sample ROM directly, 64Mx12 using paging
- Single +5V supply CMOS, 50 mW typical power dissipation
- 68 pin PLCC package

General Description

The CS8905 is a high performance programmable signal processor which is specially designed for music and sound generation applications such as music synthesis and digital effects processing. This device features 19-bit internal data paths, a 19-bit two's complement adder, a 12 x 12 two's complement multiplier, two 24-bit accumulators and a 32-bit output shift register. As a music synthesizer, the CS8905 is capable of generating 16 notes of polyphony with a high quality 16-bit stereo digital audio output at a 44.1 kHz sampling rate. For wave table synthesis applications, up to 64 Msamples of external sample memory may be addressed, and the CS8905 can generate linear envelope segments under external microprocessor control. The micro-programmable architecture of the CS8905 also makes this device well suited for use as a digital effects processing engine.

ORDERING INFORMATION

CS8905-CL 68-pin PLCC

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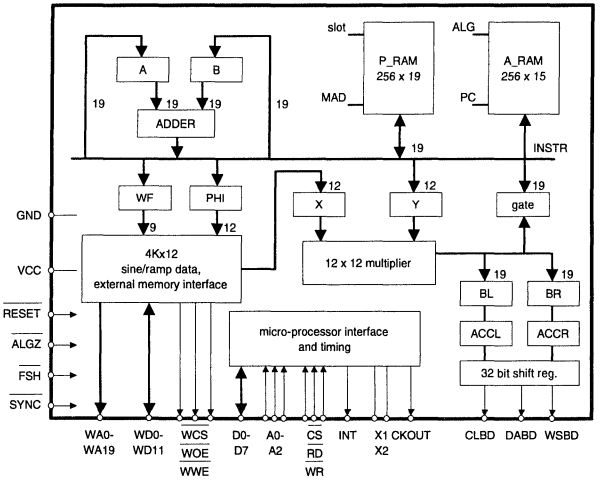

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature (Power Applied)	T_A	-40	-	+85	°C
Storage Temperature	-	-65	-	+150	°C
Voltage on any Pin	-	-0.5	-	V_{CC}+0.5	V
Supply Voltage	V_{CC}	-0.5	-	6.5	V
Maximum I_{OL} per I/O Pin	-	-	-	10	mA

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	-	5.25	V
Operating Ambient Temperature	T_A	0	-	70	°C

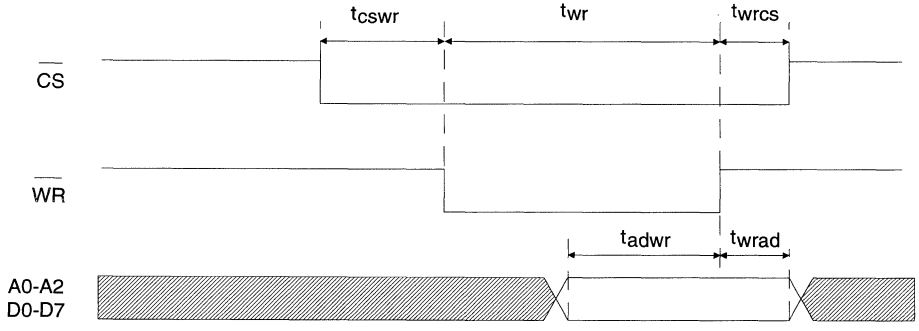
D.C. CHARACTERISTICS (T_A=25°C, V_{CC}=5V±5%)

Parameter	Symbol	Min	Typ	Max	Units
Low-Level Input Voltage	V_{IL}	-0.5	-	0.8	V
High-Level Input Voltage	V_{IH}	2.0	-	V_{CC}+0.5	V
Low-Level Output Voltage at I_{OL}=3.2 mA	V_{OL}	-	-	0.45	V
High-Level Output Voltage at I_{OH}=-0.8 mA	V_{OH}	2.4	-	-	V
Power Supply Current at Oscillator Frequency=45.1584 MHz (Note 1)	I_{CC}	-	10	25	mA

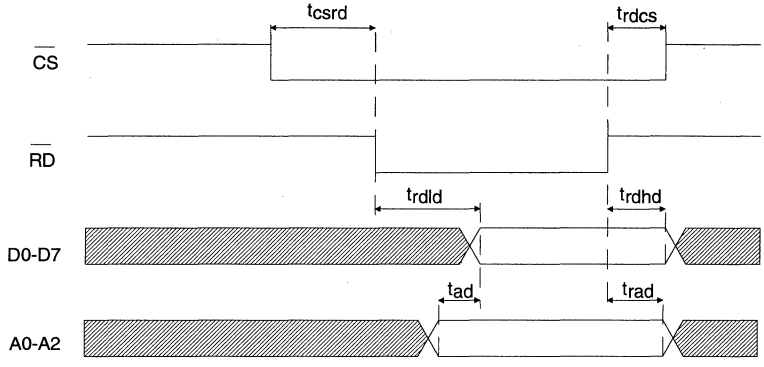
Notes: 1. Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, Power Supply Current does not include output loading

A.C. CHARACTERISTICS (T_A=25°C, V_{CC}=5V±5%, Digital Inputs at Logic "1"=Vcc; Logic "0"=DGND, load capacitance=80pF for all outputs except X2)

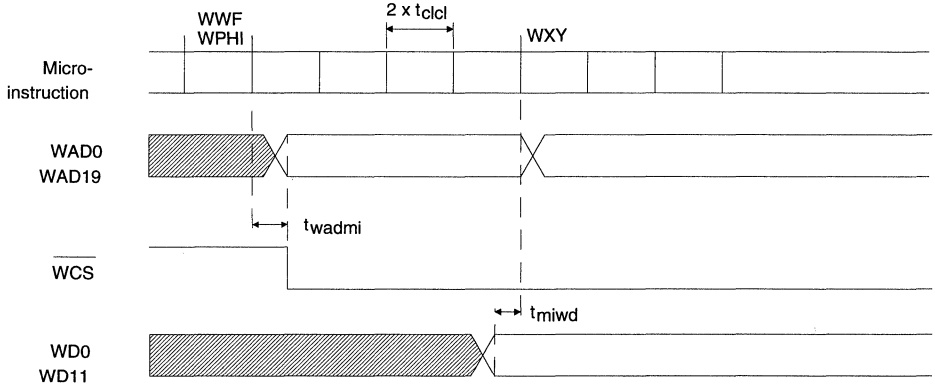
Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/tclcl	0	45.1584	48	MHz
$\overline{CS}$ Low to $\overline{WR}$ Low	tcswr	50	-	-	ns
$\overline{WR}$ High to $\overline{CS}$ High	twrcs	20	-	-	ns
A0-A2, D0-D7 Valid to Rising $\overline{WR}$	tadwr	20	-	-	ns
A0-A2, D0-D7 Valid After Rising $\overline{WR}$	twrad	10	-	-	ns
$\overline{WR}$ Pulse Width	twr	50	-	-	ns
$\overline{CS}$ Low to $\overline{RD}$ Low	tcsrd	50	-	-	ns
$\overline{RD}$ High to $\overline{CS}$ High	trdcs	20	-	-	ns
$\overline{RD}$ Active to Valid Data Out	trdld	-	-	50	ns
Data Out Hold From $\overline{RD}$	trdhd	10	-	-	ns
A0-A2 Valid to Valid Data Out	tad	-	-	50	ns
A0-A2 Hold From $\overline{RD}$	trda	10	-	-	ns
Recover From Control Write	trecover	32xtclcl+10	-	-	ns
CLBD Period	tclbd	-	32xtclcl	-	-
WAD0-19 Valid From WWF or WPHI Micro-Instruction	twadmi	-	-	10	ns
WD0-11 Valid Before WXY Micro-Instruction	tmiwd	10	-	-	ns
$\overline{WOE}$ High From RSP ClearB Micro-Instruction	twoemi	-	-	10	ns
WD0-11 Out Valid (Y Register) From $\overline{WOE}$ High	twoewd	-	tclcl	-	ns
$\overline{WWE}$ Low From $\overline{WOE}$ High	twoewe	-	2 x tclcl	-	ns
$\overline{WWE}$ High to WD0-11 High Z	twewd	-	tclcl	-	ns
$\overline{WWE}$ High to $\overline{WOE}$ Low	twewoe	-	tclcl	-	ns



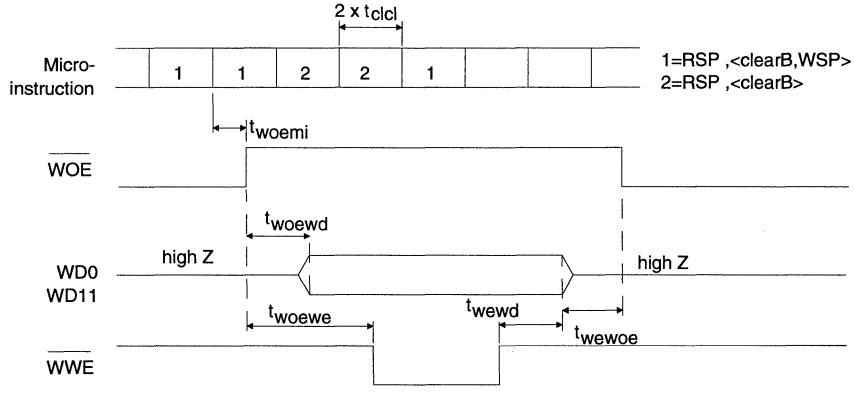
Microprocessor Write to CS8905



Microprocessor Read from CS8905



Sample Memory Read



Sample Memory Write

FUNCTIONAL DESCRIPTION

The CS8905 is a specialized high speed programmable signal processor for music and sound generation applications. The CS8905 signal processing unit includes a 19-bit two's complement adder, a 12 x 12 two's complement multiplier, two 24-bit accumulators and a 32-bit output shift register. The devices' internal data paths are 19 bits wide. Typical connections for a CS8905-based MIDI music synthesizer are indicated in Figure 1.

The CS8905 operates at one of two possible sampling rates. In the normal operating mode, the sampling rate is equal to the crystal oscillator frequency divided by 1024. In the "slow" mode, the sampling rate is the oscillator rate divided by 2048. The sample period, or synthesis frame, is divided into 16 time slots, which are referred to as synthesis slots. A sound generation algorithm for the CS8905 consists of 32 microinstructions, and one algorithm is executed during each synthesis slot.

An on-chip 256 x 15 Algorithm RAM (A-RAM) holds eight different synthesis algorithms [4 algorithms in slow mode]. A 256 x 19 Parameter RAM (P-RAM) provides 16 words of parameter data storage for each synthesis slot. The sound generation functions of the CS8905 are controlled by an external microprocessor which has access to the Algorithm RAM and the Parameter RAM. The Parameter RAM block for each synthesis slot provides a means for the external microprocessor to control the parameters of the synthesis algorithm used by the slot, and this

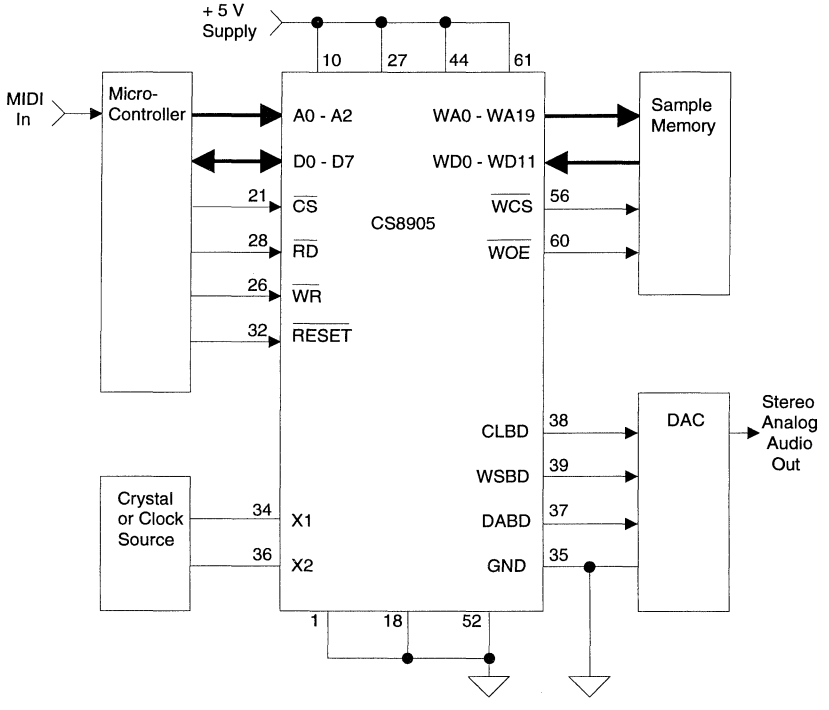


Figure 1. Typical Connection Diagram

memory block also provides working memory for the synthesis algorithm. The external microprocessor may write to either the A-RAM or the P-RAM during operation.

For music synthesis applications, each time slot is independent of the other slots, and each time slot may be used to generate one sound or note. During each slot time, one synthesis algorithm is executed and the output sample data from that algorithm is written to the left and right channel 24-bit accumulators. The signal processing unit controls the level and balance of the output from the slot by scaling the sample output to the accumulators under the control of the output mix parameters specified in the P-RAM block for that slot. The accumulators are specially designed to prevent digital overflow. At the end of each frame, the contents of the accumulators are transferred to the 32-bit output shift register and the accumulators are cleared. The shift register clocks the resulting sample data out serially to the external Digital-to-Analog Converter (DAC).

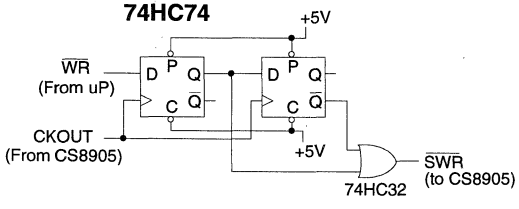
For other signal processing applications, such as generation of digital reverberation and chorus effects for musical applications, the 16 time slots available during each sample period may be used to run subroutines of a larger algorithm. In this case, parameters may be passed between time slots through the A register of the adder circuit, through the multiplier, or through external RAM.

The CS8905 can directly address up to 1 M x 12 of external memory. For high quality sampling algorithm implementations, paging techniques may be utilized to allow the CS8905 to address up to 64 Msamples of external sample memory. Sine wave and ramp data is built into the chip. The CS8905 is capable of generating linear envelope segments with a specified slope to allow creation of piecewise linear amplitude envelopes under external microprocessor control.

Microprocessor Interface

An external microprocessor controls the CS8905 synthesis functions by accessing the CS8905 Control Register, Interrupt Register, Algorithm RAM (A-RAM), and Parameter RAM (P-RAM). The Microprocessor electrical interface is a standard bus interface, comprised of the address lines A0-A2, the data lines D0-D7, the Chip Select signal $\overline{CS}$, the Write signal $\overline{WR}$, and the Read signal $\overline{RD}$.

If the external microprocessor timing and the CS8905 timing are asynchronous, then an external write synchronization circuit, such as that shown in Figure 2, should be employed to synchronize the $\overline{WR}$ signal from the external



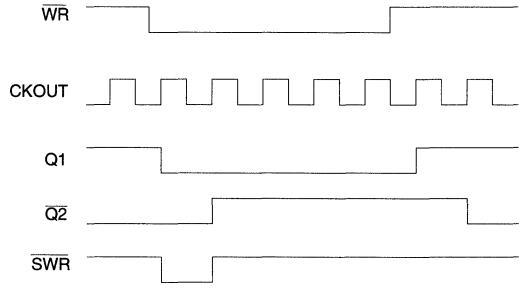


Figure 2. Write Synchronization Circuit

microprocessor with the CS8905 timing. This circuit assumes that data from the microprocessor is valid on the leading edge of $\overline{WR}$, and that the CKOUT period is shorter than the pulse width of $\overline{WR}$. If the external microprocessor timing and the CS8905 timing are derived from the same oscillator source, then the write synchronization circuit is not necessary.

The 256 x 15 Algorithm Ram (A-RAM) is organized as either 8 blocks of 32 words, or 4 blocks of 64 words in slow mode. Each word contains one micro-instruction, and each block of 32 instructions [64 in slow mode] makes up one algorithm. The last two locations in each block are reserved for microprocessor access and algorithm changes. Thus an algorithm consists of 30 micro-instructions [62 in slow mode] for sound generation. Internally, the CS8905 operates on a Master Clock, with a frequency equal to the crystal oscillator frequency divided by two. Each micro-instruction is executed in one cycle of the Master Clock.

The 256 x 19 bit Parameter RAM (P-RAM) is organized as 16 blocks of 16 words each. There is one 16 word x 19 bit block of P-RAM associated with each synthesis slot. The 16 word block of P-RAM associated with a particular synthesis slot is used to specify the synthesis algorithm number and the associated parameter data to be used for that synthesis slot. The P-RAM also functions as working RAM for the synthesis algorithm computations. The parameter types, parameter data formats and parameter addresses required for that slot depend on the specific synthesis algorithm being utilized for the slot. However, parameter location 15 in each 16-parameter block utilizes a common format which specifies the algorithm to be used for the slot. Location 15 also contains the Idle bit (I) which is used to force the associated synthesis slot to an idle mode, and the Interrupt Mask bit (M) which is used to enable/disable the generation of interrupts from that synthesis slot. Details of the CS8905 micro-instructions and associated parameter data formats are not covered in this document.

The Control Register is a 4-bit write-only register which is comprised of the following control bits:

SSR
- 0 - Set Sampling Rate = Crystal Oscillator Frequency/1024.
- 1 - Set Sampling Rate = Crystal Oscillator Frequency/2048 (SSR = 1 selects the slow mode).

IDL
- 0 - Normal Operation.
- 1 - All slots are forced to idle mode, independent of the P-RAM contents.

SEL
- 0 - Select Access to P-RAM.
- 1 - Select Access to A-RAM.

WR
- 0 - Request a Read from P-RAM or A-RAM.
- 1 - Request a Write to P-RAM or A-RAM.

The Control Register is accessed by first performing a Write operation to the CS8905 with address line A2=1 (Address lines A1 and A0 are "don't care" conditions). Note that a change of the Control Register IDL bit from 0 to 1 may take up to 1.5 µs [3 µs in slow mode] to take effect.

To write to the CS8905 P-RAM or A-RAM, the following steps must be taken:

1. Write the desired address to the CS8905
2. Write the data to the CS8905
3. Write to the CS8905 Control Register, setting WR=1
4. Allow 1.5 µs [3 µs in slow mode] for the write cycle to be completed.

To read from the CS8905 P-RAM or A-RAM, the following steps must be taken:

1. Write the desired address to the CS8905
2. Write to the CS8905 Control Register, setting WR=0
3. Allow 1.5 µs [3 µs in slow mode] for the read cycle to be completed.
4. Read the data from the CS8905

The desired address is written to the CS8905 by performing a write cycle with A2A1A0=000. The address formats for P-RAM, A-RAM (SSR bit=0), and A-RAM (SSR bit=1) are each different. These formats are given in Table 1.

The data formats for reading or writing from/to the 19 bit P-RAM and the 15-bit A-RAM are given in Table 2.

The Interrupt Register is an 8-bit read-only register which indicates the slot number and the parameter address which caused the interrupt. The parameter address identifies one parameter location within the 16-parameter P-RAM block associated with a slot. The Interrupt Register is accessed by reading from the CS8905 at address A2A1A0 = 000. Reading the Interrupt Register will not reset the interrupt cause. After initially reading the Interrupt register, the microprocessor should change the slot parameters to remove the interrupt cause, then perform a dummy read of the Interrupt Register (read the register and discard the result) to clear any possible interrupts which may be pending from the same cause. Most musical synthesis applications do not need to utilize the interrupt features of the CS8905.

Type of Address (Read/Written)	Address			Address Data Format							
	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
P-RAM Address	0	0	0	V3	V2	V1	V0	MAD3	MAD2	MAD1	MAD0
A-RAM with SSR=0	0	0	0	AL2	AL1	AL0	PC4	PC3	PC2	PC1	PC0
A-RAM with SSR=1	0	0	0	AL2	AL1	PC5	PC4	PC3	PC2	PC1	PC0

Notes: 1. V0-V3 = Synthesis Slot Number
2. MAD0-MAD3 = Address of specific parameter within the 16 word block associated with the specified slot
3. AL0-AL2 = Algorithm number
4. PC0-PC5 = Address of specified micro instruction within the 32 word block [64 word block in slow mode] associated with the specified algorithm number.

Table 1. Data Format for writing Address Information to the CS8905

Type of Data (Read/Written)	Address			Data Format							
	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
P-RAM data	0	0	1	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	0	B15	B14	B13	B12	B11	B10	B9	B8
	0	1	1	X	X	X	X	X	B18	B17	B16
A-RAM data	0	0	1	I7	I6	I5	I4	I3	I2	I1	I0
	0	1	0	X	I14	I13	I12	I11	I10	I9	I8

Notes: 1. B0-B18 = P-RAM parameter data (19 bit word)
2. I0-I14 = A-RAM micro instruction data (15 bit word)

Table 2. Data Format for reading/writing P-RAM or A-RAM data to CS8905

Sample Memory Interface

The CS8905 provides a 20 bit address bus and 12 bit wide data bus for access to external memory. The memory interface signals are output under micro-instruction control. Therefore, the timing requirements for external memory access are algorithm dependent.

The 20 bit address bus is made up of 8 bits of waveform address information from the WF register, and 12 bits of phase information from the PHI register. The upper 8 bits of the address bus, WA12-WA19, represent the 8 least significant bits of the 9 bit WF register. The lower 12 bits of the address bus, WA0-WA11, represent the 12 most significant bits of the 19 bit PHI register.

The 19 bit PHI register can be subdivided into an integer part and a fractional part. The relative sizes of the integer and fractional parts of the phase will depend on the memory size and memory addressing techniques used in an application. The integer part of the phase is that part of the PHI register which is used to address external memory (12 bits maximum). The fractional part of the phase is that part of the PHI information which does not address external memory (7 bits minimum). The size of the fractional part of the phase affects the playback frequency accuracy in wave table synthesis applications.

The CS8905 is capable of directly addressing a maximum of 1 Msample of external memory. In this case the fractional part of the phase is 7 bits. This provides sufficient frequency resolution for samples which will be replayed without pitch transposition. However, for implementations which will shift the pitch of stored samples during playback, a minimum of 9 bits of fractional phase information is recommended. This limits the memory size for direct addressing to 256 Ksamples. For larger transposable sample memories, a paged address system should be implemented. Transposable sample memory sizes of up to 64 Msamples can be implemented with excellent frequency accuracy using paging. Paging requires only one additional micro-instruction per memory access compared to direct addressing.

Figure 3 depicts a 32K x 8 RAM sampling memory which is directly addressed by the CS8905. In this case, the five lower address lines WA0-WA4 are not used to address sample memory, and the fractional part of the phase is increased to 12 bits.

Figure 4 shows a 1M x 12 bit sample memory which is organized as 4 pages of 256 Ksamples per page. Each page is divided into 512 waves of 512 samples/wave. The address lines WA12 and WA13 are used to select one of the four pages. In this case the wave number (WF register data) is output and captured from address lines WA2-WA10 by the 74HC174 latches on the falling edge of $\overline{WCS}$. The sample address within the page (the integer part of the phase) is then taken from address lines WA3-WA11. The fractional part of the phase has 10 bit resolution, allowing good frequency accuracy. Note that in this example, 12 bit samples are stored in two 8-bit wide ROMs. The smaller 4Mbit ROM holds the 4 lower data bits for two consecutive samples in each of its' 8-bit memory locations. The correct nibble is selected using the 74HC157 based on the state of address line WA3. Address lines WA14-WA19 could be utilized as additional page address bits to expand this addressing mechanism to a maximum of 256 pages (64 Msamples) while maintaining 10 bits of resolution in the fractional part of the phase.

When 8-bit sample memories are utilized, the unused data bus pins on the CS8905 should be pulled down to ground through 10 kOhm resistors.

For high quality sampling algorithms which employ paged addressing, an external buffer circuit may be added to the memory interface circuitry to allow the CS8905 to perform linear interpolation between sample values read from memory. The buffer is used to selectively gate the lower lines of the CS8905 address bus onto the data bus. This allows the synthesis algorithm to read the most significant bits of the fractional phase information via the data bus for use as a weighting constant in the interpolation calculations.

DAC Interface

The CS8905 DAC interface consists of a left/right clock signal WSBD, a bit clock CLBD and the stereo output data stream DABD. The digital audio output format for the CS8905 is shown in Figure 5. Note that the most significant bit (msb) of the sample is output from the CS8905 1/2 bit time (1/2 clock cycle of the CLBD bit clock) after the rising or falling edge of WSBD. This timing format may be converted to a more common format, wherein the msb is output one full bit time after the edge of CLBD, using either of the two circuits shown in Figure 6.

The digital audio output from the CS8905 has a positive DC offset of 5% of the full scale value. Some low cost DACs generate a considerable amount of electrical noise when transitioning

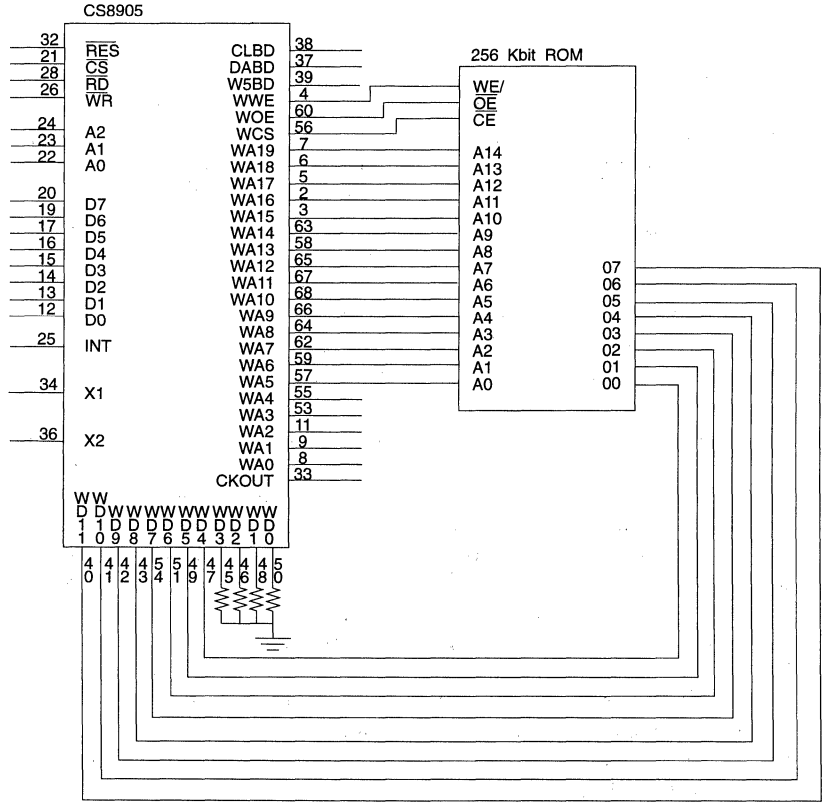


Figure 3. Direct Addressing of 32Kx8 Sample Memory

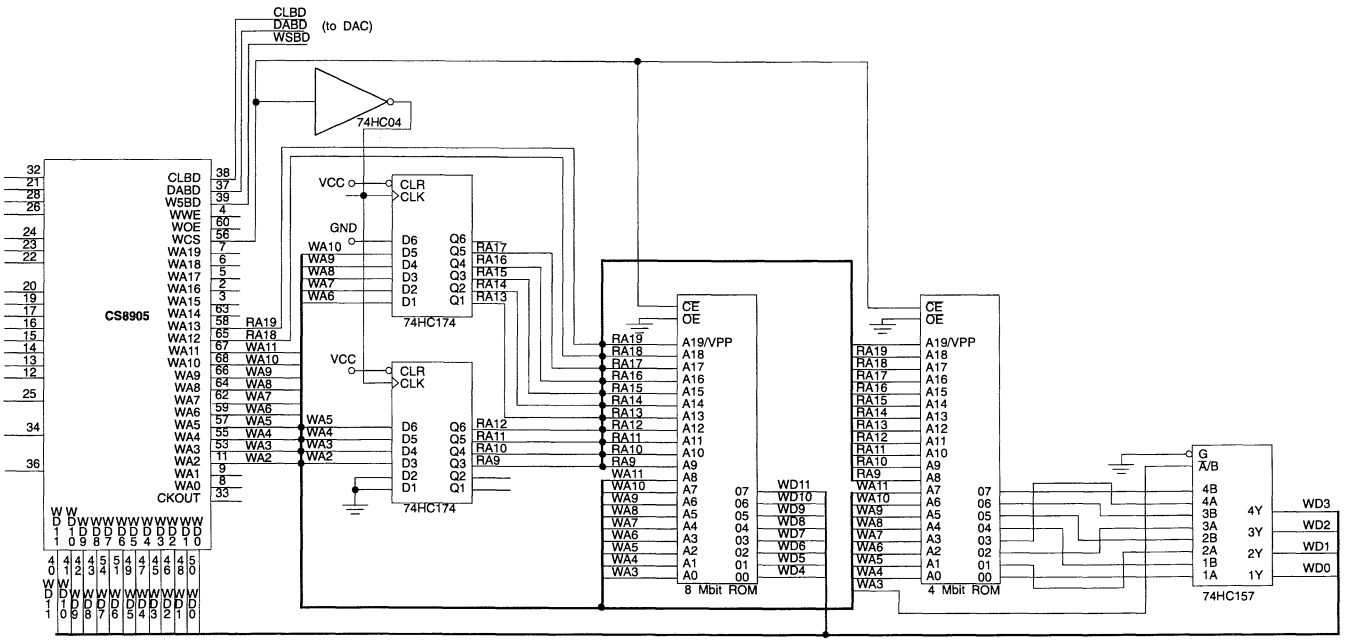


Figure 4. 1Mx12 Sample Memory Using Paging

from zero (an input code of all zeros) to minus one (an input code of all ones). The 5% DC offset can dramatically reduce the signal to noise level for small signals when using this type of DAC. If the digital output from the CS8905 is input to another digital processing device, the offset may be removed by subtracting the value 0D00 Hexadecimal from each sample received from the CS8905.

The ground reference for the DAC should be connected directly to the CS8905 GND at pin 35, and this should be the only connection between analog ground and digital ground.

Oscillator Circuit

The CS8905 timing may be generated using the internal oscillator (external crystal circuit) or using an external oscillator. Trace lengths should be kept to a minimum, and the board layout should include ground plane beneath the oscillator circuit components.

If an external oscillator circuit is utilized, shield the input trace from the oscillator to the CS8905 X1 input and keep the trace lengths to a minimum. The external clock supplied to the X1 pin should be CMOS level. Pin X2 should be left open.

Power Connections and Decoupling

All power and ground pins on the CS8905 device should be connected to the appropriate low impedance supply planes using the shortest trace lengths possible.

Recommended decoupling consists of four 0.1 uF ceramic decoupling capacitors between V_{CC} and GND, one at each of the four sides of the IC. These capacitors should be placed as close to the IC as possible. In addition, place one 10 uF Tantalum capacitor from V_{CC} to GND near the crystal oscillator circuit.

Power-up Reset

The $\overline{\text{RESET}}$ signal initializes the CS8905. The initialization includes the following:

1. Initialize internal master clock phasing
2. Select high sampling rate (sets SSR=0 in the Control Register)
3. Set the general idle bit IDL=1 in the Control Register
4. Force the micro-instruction counter to 31
5. Force the slot number to 0

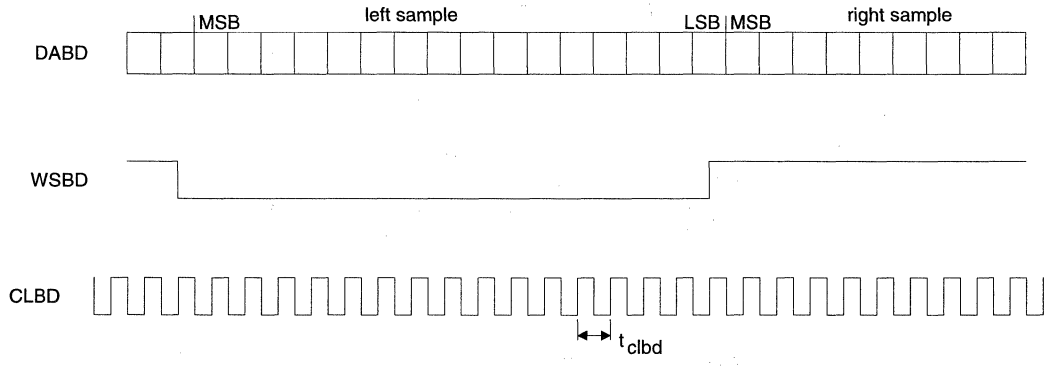


Figure 5. CS8905 Digital Audio Output Format

The $\overline{\text{RESET}}$ input must be held low until the oscillator circuit has stabilized. The CS8905 internal oscillator is enabled during $\overline{\text{RESET}}$, other functions of the device are held in an idle mode while $\overline{\text{RESET}}$ is low.

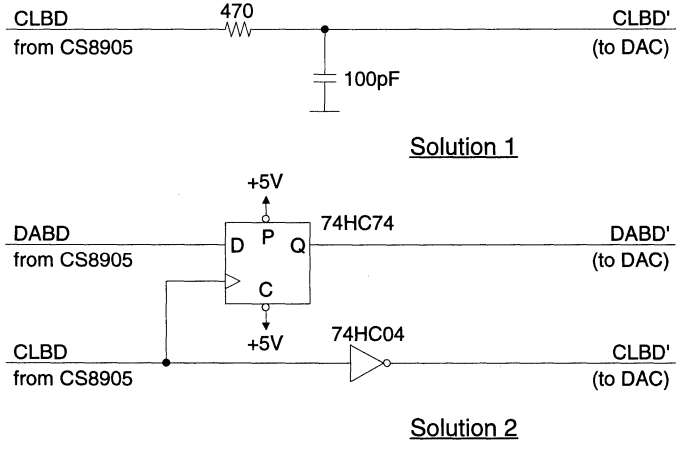
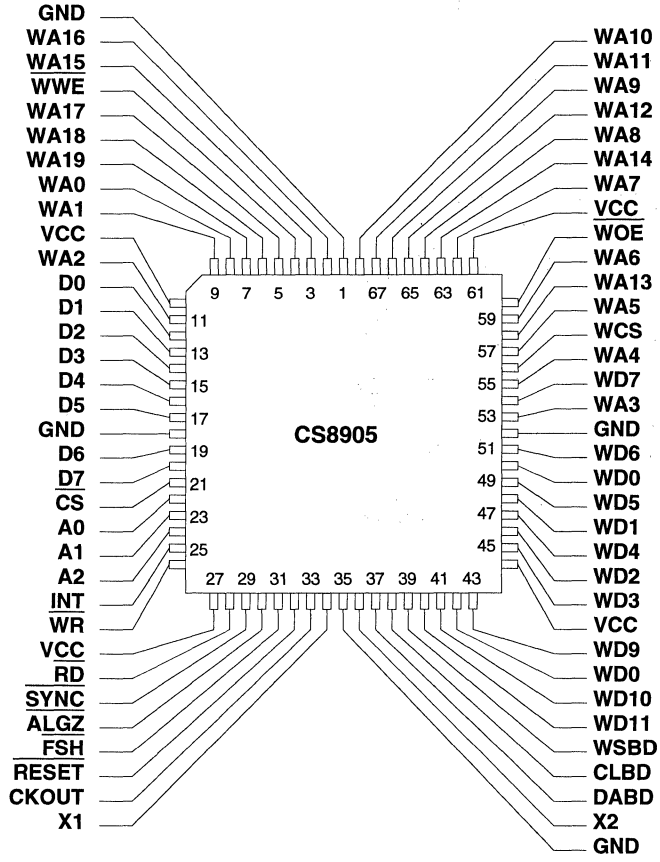


Figure 6. Digital Audio Output Format Conversion

PIN DESCRIPTIONS



Pins

GND - Ground. PINS 1, 18, 35, and 52.

Ground, all ground pins on the device must be connected to a low impedance ground.

VCC - +5V supply. PINS 10, 27, 44, and 61.

+5V supply, all VCC pins on the device must be connected to a low impedance +5V supply.

D0-D7 - Data I/O. PINS 12, 13, 14, 15, 16, 17, 19, and 20.

These bi-directional data lines are used to transfer data between an external microprocessor and the CS8905.

A0-A2 - Address Select Input from Microprocessor. PINS 22, 23, and 24.
These pins allow an external microprocessor to select the CS8905 control register or specify data registers for read/write operations.

$\overline{CS}$ - Chip Select Input. PIN 21.
This is the CS8905 chip select input from an external microprocessor. Active low.

$\overline{RD}$ - Read Strobe Input from Microprocessor. PIN 28.
This signal is the read strobe from an external microprocessor. Active low.

$\overline{WR}$ - Write Strobe Input from Microprocessor. PIN 26.
This signal is the write strobe from an external microprocessor. Active low.

$\overline{INT}$ - Interrupt Request Output to Microprocessor. PIN 25.
This output will be driven low by the CS8905 to interrupt an external microprocessor.

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X1 - Xtal or External Clock Input. PIN 34.
This is the input pin for the internal oscillator circuit. A crystal or external clock frequency of 48 MHz maximum may be connected. If an external oscillator is used, it should be CMOS logic level.

X2 - Xtal Output Connection. PIN 36.
This pin is the internal oscillator circuit output. If an external oscillator is used, this pin should be left open.

CKOUT - Output Clock. PIN 33.
This output clock has a frequency equal to the CS8905 oscillator frequency divided by four.

$\overline{RESET}$ - Chip Reset Input. PIN 32.
This active low input is used to reset and initialize the CS8905. This signal should be held low for at least 10 ms after power up.

DABD - Serial Data Out to External DAC. PIN 37.
This signal is the stereo 16-bit digital audio data output from the CS8905 to an external DAC.

CLBD - Clock Output to External DAC. PIN 38.
This output is the bit clock for the DABD signal.

WSBD - Left/Right Channel Select Output to External DAC. PIN 39.
This is the left/right word clock for the DABD signal.

WA0-WA19 - External Sampling Wave Memory Address Output. PINS 8, 9, 11, 53, 55, 57, 59, 62, 64, 66, 68, 67, 65, 58, 63, 3, 2, 5, 6, and 7
These address lines are used to address an external sample memory.

WD0-WD11 - External Sampling Wave Memory Data Output. PINS 50, 48, 46, 45, 47, 49, 51, 54, 43, 42, 41, and 40.

These data lines are used to pass sample data from/to external sample memory.

$\overline{\text{WCS}}$ - External Sampling Wave Memory Chip Select Output. PIN 56.

This is an active low chip select signal for external sample memory.

$\overline{\text{WOE}}$ - External Sampling Wave Memory Output Enable. PIN 60.

This signal is an active low output enable strobe pin for external sample memory.

$\overline{\text{WWE}}$ - External Sampling Wave Memory Write Output. PIN 4.

This signal is an active low write strobe for external RAM sample memory.

$\overline{\text{SYNC}}$ - Synchronize Input. PIN 29.

This active low signal is used for synchronization between several CS8905 devices. This signal should be tied to V_{CC} under normal operating conditions.

$\overline{\text{ALGZ}}$ - Zero Algorithm Input. PIN 30.

This active low signal will force execution of algorithm zero. This signal should be tied to V_{CC} under normal operating conditions.

$\overline{\text{FSH}}$ - Fast Shift Input. PIN 31.

This active low input signal forces the serial data DABD to be shifted out at the master clock rate rather than the CLBD rate. This signal should be tied to V_{CC} under normal operating conditions.

Semiconductor Corporation

CS9203

Advanced Music Synthesizer

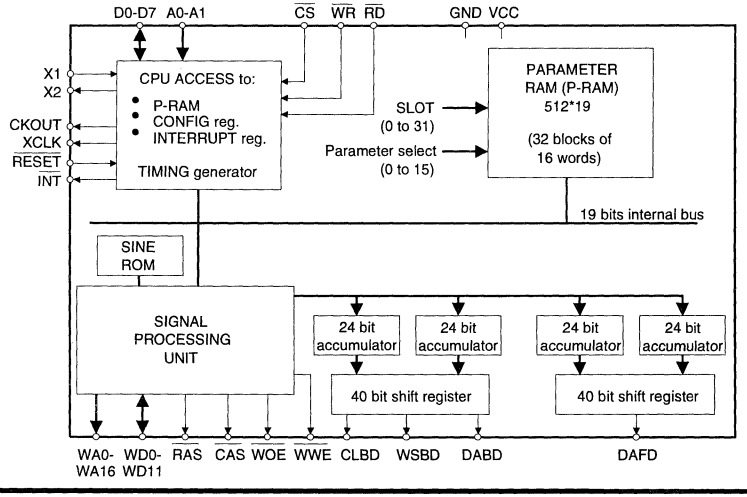
Features

- Polyphonic up to 32 notes
- Multi-timbral up to 32 simultaneous timbres
- 15 built-in synthesis algorithms
- On-chip high speed adder, multiplier, and 24 bit accumulators with overflow protection
- Built-in sine wave data
- Addresses up to 8Mx12 external sampling memory (ROM, SRAM, or DRAM)
- Two stereo 16 - 20 bit digital audio outputs (four audio outputs)
- Independent pan and volume mix assignable for each voice
- +5V supply CMOS, 50 mW power
- 68 pin PLCC package

General Description

The CS9203 is a high performance signal processor which is specially designed for high-quality music synthesis applications. Fifteen built-in music synthesis algorithms make the CS9203 extremely flexible, and the advanced features associated with it's PCM sampling algorithms, such as linear interpolation between samples, linear segment envelope generator, and 12 dB variable Q filtering, make the CS9203 a superb wave table synthesis engine. Dual stereo digital audio outputs are provided to allow the addition of an external effects processor, such as the CS8905. The 32 note polyphony and 32 part multi-timbral capabilities of the CS9203 make it an ideal choice for General MIDI (GM) synthesis applications, including musical instruments, MIDI sound modules, Karaoke machines, and high quality Personal Computer sound cards.

ORDERING INFORMATION
CS9203-CL 68-pin PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 462 2723

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ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature (Power Applied)	-	-40	-	+85	°C
Storage Temperature	-	-65	-	+150	°C
Voltage on any Pin	-	-0.5	-	V_{CC}+0.5	V
Supply Voltage	V_{CC}	-0.5	-	6.5	V
Maximum I_{OL} Per I/O Pin	-	-	-	10	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	-	5.25	V
Operating Ambient Temperature	T_A	0	-	70	°C

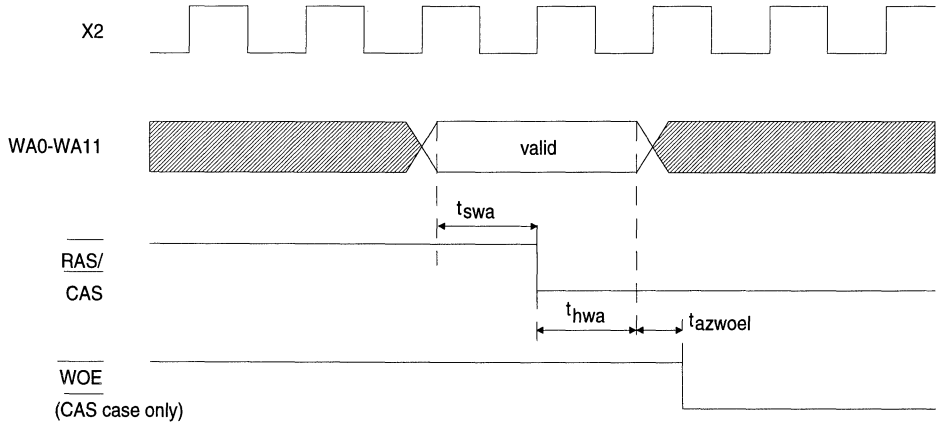
D.C. CHARACTERISTICS (T_A=25°C, V_{CC}=5V ±5%)

Parameter	Symbol	Min	Typ	Max	Unit
Low-Level Input Voltage	V_{IL}	-0.5	-	0.8	V
High-Level Input Voltage	V_{IH}	2.0	-	V_{CC}+0.5	V
Low-Level Output Voltage at I_{OL}=3.2 mA	V_{OL}	-	-	0.45	V
High-Level Output Voltage at I_{OH}=-0.8 mA	V_{OH}	2.4	-	-	V
Power Supply Current (Note 1) crystal frequency=50.000MHz	I_{CC}	-	10	25	mA

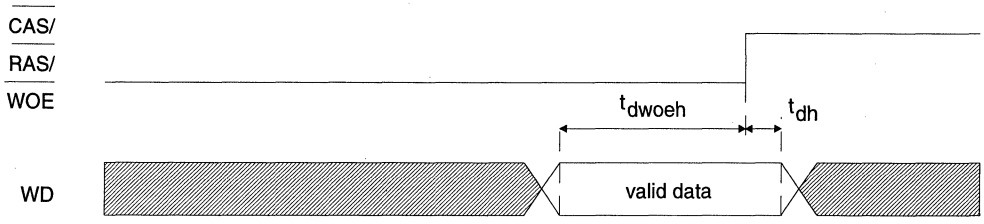
Notes: 1. Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, Power Supply Current does not include output loading

SWITCHING CHARACTERISTICS (T_A=25°C, V_{CC}=5V ±5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=80pF for all outputs except X2)

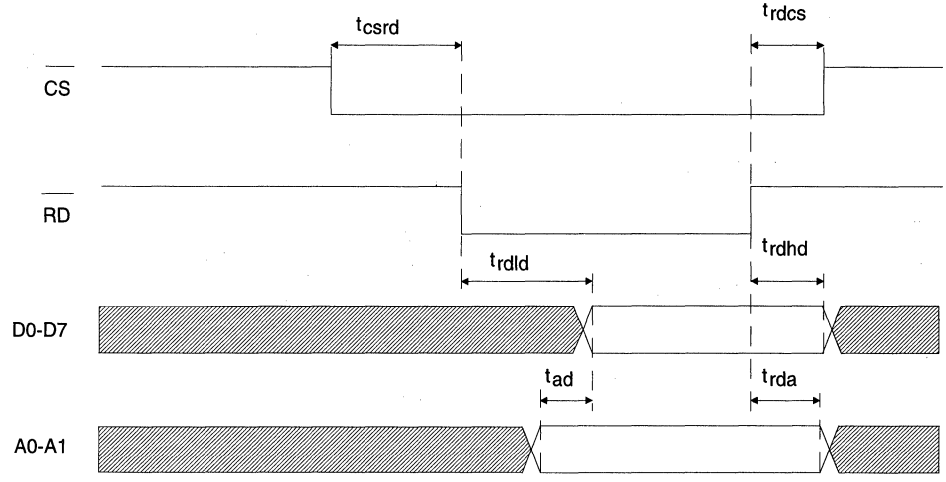
Parameter	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	$1/t_{clcl}$	0	48.0	50	MHz
$\overline{CS}$ Low to $\overline{WR}$ Low	t_{cswr}	50	-	-	ns
$\overline{WR}$ High to $\overline{CS}$ High	t_{wrcs}	20	-	-	ns
A0-A1, D0-D7 Valid before Rising $\overline{WR}$	t_{adwr}	20	-	-	ns
A0-A1, D0-D7 Valid after Rising $\overline{WR}$	t_{wrad}	0	-	-	ns
$\overline{WR}$ Pulse Width	t_{wr}	50	-	-	ns
$\overline{CS}$ Low to $\overline{RD}$ Low	t_{csrd}	50	-	-	ns
$\overline{RD}$ High to $\overline{CS}$ High	t_{rdcs}	20	-	-	ns
$\overline{RD}$ Active to Valid Data Out	t_{rdld}	-	-	50	ns
Data Out Hold from $\overline{RD}$	t_{rdhd}	10	-	-	ns
A0-A1 Valid to Valid Data Out	t_{ad}	-	-	50	ns
A0-A1 Hold from $\overline{RD}$	t_{rda}	10	-	-	ns
Recover from Control Write	$t_{recover}$	$34xt_{clcl}$+10	-	-	ns
CLBD Period	t_{clbd}	-	$34xt_{clcl}$	-	-
WA Valid before $\overline{RAS}$ or $\overline{CAS}$ H to L	t_{swa}	t_{clcl}-5	-	-	ns
WA Valid after $\overline{RAS}$ or $\overline{CAS}$ H to L	t_{hwa}	t_{clcl}-5	-	-	ns
WD Floating to $\overline{WOE}$ Low	t_{azwoel}	0	-	-	ns
Valid Data in to Rising $\overline{WOE}$	t_{dwoeh}	40	-	-	ns
Data in Hold after Rising $\overline{WOE}$	t_{dh}	0	-	-	ns



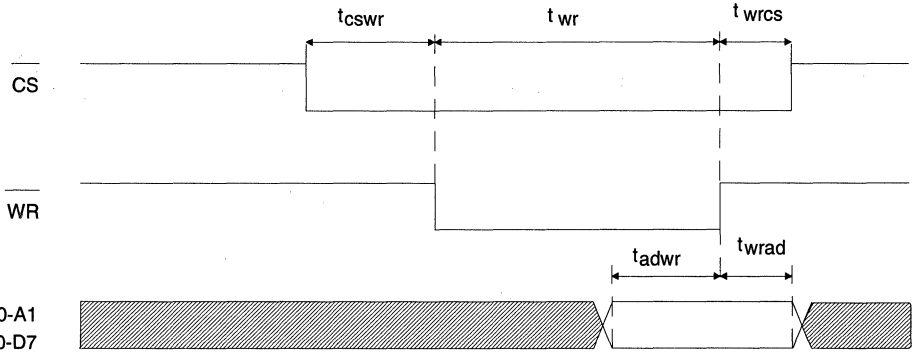
Sample Memory Address Timing



Sample Memory Data Bus Timing, Sample Memory Read



Microprocessor Read Cycle



Microprocessor Write Cycle

FUNCTIONAL DESCRIPTION

The CS9203 is a specialized high performance signal processor for music synthesis applications. The CS9203 signal processing unit includes a high speed adder, a multiplier, and specialized circuitry for phase computation, interpolation between samples, and amplitude envelope generation. The devices' internal data paths are 19 bits wide, and four 24-bit accumulators are used to generate the output samples for the four digital output channels of the device (two stereo output channels). The CS9203 has fifteen different built-in ROM-coded synthesis algorithms which can be used to generate a wide variety of sounds. A sixteenth algorithm is included for DRAM refresh in applications which store PCM sound samples in Dynamic RAM

The sample memory interface allows PCM sample-based synthesis algorithms to access sound samples stored off-chip in DRAM, SRAM, or ROM. Sine wave data is contained on-chip. An on-chip Parameter RAM (P-RAM) block provides RAM workspace for the synthesis algorithms. The CS9203 synthesis functions are controlled by an external microprocessor. Typical connections for a wavetable synthesis application are indicated in Figure 1.

The CS9203 operates on a synthesis frame timing basis. A stereo digital audio sample is output at the end of each synthesis frame. Thus the output sampling rate is the same as the synthesis frame rate. The synthesis frame is divided into a number of time slots, which are referred to as synthesis slots. One of the CS9203's 15 synthe-

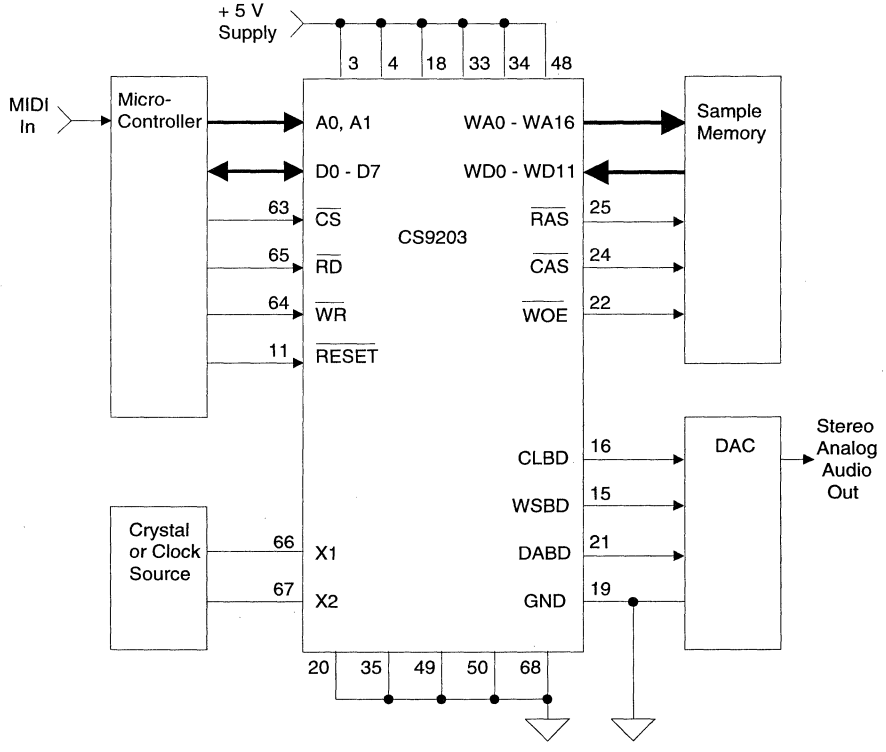


Figure 1. Typical Connection Diagram

sis algorithms is executed during each synthesis slot, and in general, each synthesis slot generates one note or voice. The number of synthesis slots in the synthesis frame can be set to any even number from 16 to 32. The length of a synthesis slot is 68 clock cycles (tclcl x 68), and the length of the frame is then (tclcl x 68 x N), where N is the number of synthesis slots per frame (N can be considered to be the number of notes of polyphony). The frame rate, or sampling rate, is the inverse of the frame length: Output Sampling Rate = 1/(tclcl x 68 x N) = Crystal Oscillator frequency/(68 x N) where N is the number of synthesis slots per frame.

The 512 x 19 bit Parameter RAM (P-RAM) is organized as 32 blocks of 16 words each. There is one 16 word x 19 bit block of Parameter RAM associated with each synthesis slot. The 16 word block of P-RAM associated with a particular slot holds all of the parameter data for that slot. The last word in the P-RAM block specifies which of the 16 built-in algorithms will be utilized for the synthesis slot. The specific data and format for the remaining 15 words of P-RAM in the block are algorithm dependent.

During each slot time, one algorithm is executed and the output sample from that algorithm is sent to the four 24-bit accumulators. The signal processing unit controls the level and balance of the output from the slot by scaling the sample output to the accumulators under the control of the mix parameters located in the P-RAM block for that slot. The accumulators are specially designed to prevent digital overflow. At the end of each frame, the contents of the accumulators are transferred to the four 20-bit output shift registers and the accumulators are cleared. The shift registers clock the resulting sample data out serially to the external Digital-to-Analog Converter(s).

Seven of the CS9203 synthesis algorithms utilize external PCM sound samples for high quality sound generation. Algorithm number 1, the High Quality Sampling algorithm, employs linear interpolation for frequency shifting, followed by a 12 dB variable-Q low-pass filter for timbre adjustment and elimination of noise which may be naturally created when transposing a samples' pitch during playback. The low-pass filter implementation has a variable cutoff frequency which may be controlled using a built-in envelope generator. A second envelope generator is utilized to control the final output amplitude for the resulting sound.

Other useful PCM sample-based algorithms include a 3X sampling algorithm for drums, a 2X sampling algorithm with 12 dB fixed-Q variable-cutoff low-pass filter, a 2X sampling algorithm with 12dB variable-Q variable-cutoff low-pass filter, a 1X sampling plus white noise algorithm with 12 dB variable-Q variable-cutoff low-pass filter, a 1X sampling algorithm with 24 dB variable-Q variable-cutoff low-pass filter, and an algorithm which combines a 1X pcm sampling operator with an algorithmic synthesis technique. The 3X sampling algorithm allows a single voice of polyphony (a single synthesis slot) to generate three simultaneous drum sounds. Separate envelope generators are used to control the output amplitude for each of the three sounds. The 2X sampling algorithm with 12 dB fixed-Q variable-cutoff low-pass filter is useful for generating "partials"-based sounds without the severe polyphony sacrifice normally associated with these techniques.

The remaining eight algorithms in the CS9203 employ algorithmic synthesis techniques which utilize the on-chip sine data rather than external PCM samples.

All of the PCM sample-based algorithms in the CS9203 support looped playback of samples. The sample memory address space is organized as 64 pages of 512 waves per page, where a wave is defined to be a block of 256 consecutive samples. A single sampled sound may occupy a maximum of one full page of sample memory

(128K samples). Three pointers are used to define the location of a sampled sound in memory. These pointers specify the Current Wave address, the End Wave address, and the Loop Wave address. Sample memory access during sound playback begins at the initial Current Wave address, and the current wave pointer is incremented during playback until the End Wave address is reached. The CS9203 supports two different loop modes for sound playback. In the more general case, when the current wave pointer value reaches the End Wave, it is automatically reloaded with the Loop Wave address. This mode of playback allows the lengths of the attack (non-looped) portion and the looped portion of the sampled sound to be optimized for the characteristics of that sound. In the "loop last wave" mode of operation, playback will always loop on the End Wave. One-shot sounds are implemented by including a blank wave at the end of the sound, and then utilizing the loop on last wave playback mode for the one-shot sound.

The pitch, or playback frequency, for playback of sampled sounds is specified by the 18 bit DPHI parameter. The upper 6 bits of the DPHI parameter are referred to as the upper phase bits, and these bits make up the six least significant bits of the sample memory address. The lower 12 bits of the DPHI parameter make up the fractional part of the phase. The frequency scaling on playback is equal to DPHI/4096. A DPHI value of 4096 (upper phase = 1, fractional part = 0) would play the samples from memory at the CS9203 output word rate. The fractional part of the phase is also used as the weighting constant for linear interpolation between samples when utilizing algorithm 1. A DPHI value of 2048 (upper phase = 0, fractional part = 2048) would play the samples from memory at one half the CS9203 word rate. In this case, every second value output from the algorithm would be an interpolated value to fill in the "missing point" midway between adjacent samples in memory.

Envelope generation in the CS9203 is of the linear segment type, allowing the creation of any piecewise linear envelope shape under external microprocessor control. The microprocessor specifies a rate of change and the amplitude endpoint for each segment, and the envelope generator will generate an interrupt to the microprocessor when the endpoint level has been reached.

Microprocessor Interface

The electrical interface between the microprocessor and the CS9203 is a standard bus interface, comprised of the address lines A0 and A1, the data lines D0-D7, the Chip Select signal $\overline{CS}$, the Write signal $\overline{WR}$, and the Read signal $\overline{RD}$. The external microprocessor controls the CS9203 synthesis functions by accessing the CS9203 Configuration Register, Interrupt Register, and Parameter RAM (P-RAM).

The Configuration Register is an 8-bit write-only control register which is comprised of the following control bits:

RUN	0 -	All slots are forced to idle mode, independent of the P-RAM contents (power-up default state).
	1 -	Synthesis slot processing is enabled as indicated by contents of the P-RAM.
OFST	0 -	The digital audio output data on DABD has no DC offset (power-up default).
	1 -	The digital audio output data on DABD includes a 5%positive DC offset.
IE	0 -	Envelope generator interrupts masked off (power-up default).
	1 -	Envelope generator interrupts enabled.
SFMT	0 -	Selects digital audio output format with idling on LSB (power-up default). See Figure 6.
	1 -	Selects digital audio output format with idling on MSB. See Figure 6.

S0 - S3 Slot Count Sequence - These 4 bits are used to select the number of synthesis slots to be used as follows:

S3	S2	S1	S0	No. Slots
1	X	X	X	16
0	0	0	0	18 (default)
0	0	0	1	20
0	0	1	0	22
0	0	1	1	24
0	1	0	0	26
0	1	0	1	28
0	1	1	0	30
0	1	1	1	32

The Control Register is accessed by first performing a Write operation to the CS9203 at Address A1A0 = 11 with data bit D6 =1 in order to set the CS9203 into the configuration mode. After setting the device to configuration mode, the configuration register data is written to address A1A0=00.

The Interrupt Register is an 8-bit read-only register which indicates the slot number and the envelope generator address within that slot which has caused the interrupt. The Interrupt Register is accessed by reading from the CS9203 at address A1A0 = 00.

The CS9203 Parameter RAM (P-RAM) is used to specify the synthesis algorithm and associated parameter data to be used for each synthesis slot. The P-RAM also functions as working RAM for the synthesis algorithm computations. There are 16 words of P-RAM associated with each synthesis slot. The P-RAM word size is 19 bits. The full address for a given P-RAM location is made up of a Page bit (P) and an 8-bit P-RAM address. The Page bit value is zero for parameters associated with slots 0 - 15, and one for slots 16-32. The 8-bit P-RAM address is comprised of a 4-bit Slot address and a 4-bit Parameter address (the 4-bit Parameter address identifies one parameter location in the 16-parameter block associated with the specified Slot). The parameter types, parameter data formats, and parameter addresses required for each slot depend on the specific synthesis algorithm being utilized for that slot. However, parameter location 15 in each 16-parameter block utilizes a common format which specifies the algorithm to be used for that slot, the output mix to be used, the phase angle constant (used by some algorithms), and the busy/idle status of the slot. Details of the sixteen synthesis algorithms and associated parameter data formats are not covered in this document. The P-RAM write sequence and P-RAM read sequence operations are indicated in Table 1 and Table 2.

Sample Memory Interface

The CS9203 can address up to 8 Msamples of external PCM sample memory. The 23-bit sample memory address is comprised of a 6-bit Page Address (PAGE0-PAGE5), a 9-bit Current Wave Address (CW0-CW8), and an 8-bit Upper Phase Address (PHI11-PHI18). This addressing technique organizes the sample memory into 64 pages, with each page containing 512 waves of 256 samples each. The Page Address bits (PAGE0-PAGE5), Current Wave Address bits (CW0-CW8), and Upper Phase Address bits (PHI11-PHI18) are output on the CS9203 Wave Address pins (WA0-WA11) in a time division multiplexed manner, using the $\overline{RAS}$ and $\overline{CAS}$ output signals as address strobes. Table 3 indicates the address bits which are available on the Wave Address signal pins (WA0-WA11) at $\overline{RAS}$ time, $\overline{CAS}$ time, and following the $\overline{CAS}$ strobe ($\overline{CAS}$+1 time). This memory addressing technique allows direct connection of large Dynamic RAMs with enable control inputs (x4 configurations). Large ROM memory configurations require external latches to capture a small subset of the address information on the Wave Address lines (WA9-WA11) during the $\overline{RAS}$ and $\overline{CAS}$ strobes. A typical external sampling memory read sequence is shown in Figure 2. Note that the cycle on which the $\overline{RAS}$ and $\overline{CAS}$ strobes occur is algorithm dependent.

Operation	Address A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
Step 1. Select P-RAM Address Inside Page ($\overline{CS}$=$\overline{WR}$=0)	0	0	P-RAM Address (8bits)							
Step 2. Write Low data Byte ($\overline{CS}$=$\overline{WR}$=0)	0	1	B7	B6	B5	B4	B3	B2	B1	B0
Step 3. Write Mid Data Byte ($\overline{CS}$=$\overline{WR}$=0)	1	0	B15	B14	B13	B12	B11	B10	B9	B8
Step 4. Write High Data Bits, Select Page P and Request Write ($\overline{CS}$=$\overline{WR}$=0)	1	1	P	0	X	X	X	B18	B17	B16

Notes: 1. Allow 68 crystal clock cycles (1.36 µs @50MHz) between step 4 and subsequent step 1 or read operations.
2. Steps 2 and 3 can be omitted when writing repetitive data.
3. Steps 1, 2 and 3 can occur in any order.
4. The page P selected on step 4 remains valid for subsequent reads.

5

Table 1. P-RAM Write Sequence

Operation	Address A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
Step 1. Select P-RAM Page ($\overline{CS}$=$\overline{WR}$=0)	1	1	P	1	X	X	X	X	X	X
Step 2. Dummy Read ($\overline{CS}$=$\overline{RD}$=0)	0	1	X	X	X	X	X	X	X	X
Step 3. Select P-RAM Address in Page and Request Read ($\overline{CS}$=$\overline{WR}$=0)	0	0	P-RAM Address (8Bits)							
Step 4. Read Low Data Byte ($\overline{CS}$=$\overline{RD}$=0)	0	1	B7	B6	B5	B4	B3	B2	B1	B0
Step 5. Read Mid Data Byte ($\overline{CS}$=$\overline{RD}$=0)	1	0	B15	B14	B13	B12	B11	B10	B9	B8
Step 6. Read High Data Byte ($\overline{CS}$=$\overline{RD}$=0)	1	1	X	X	X	X	X	B18	B17	B16

Notes: 1. Steps 1 and 2 can be omitted if the page bit P is already loaded (from a previous read or write).
2. Step 1 loads the page bit P and sets the configuration mode, this requires a dummy read on step 2.
3. At least 68 crystal clock cycles (1.36 µs @50MHz) are required between step 3 and the subsequent step.
4. Steps 4 to 6 can occur in any order.
5. Steps 4 to 6 are optional.

Table 2. P-RAM Read Sequence

Time	WA11	WA10	WA9	WA8	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
($\overline{RAS}$)	WWE	PAGE2	PAGE1	PAGE0	PHI18	PHI17	PHI16	PHI15	PHI14	PHI13	PHI12	PHI11
($\overline{CAS}$)	PAGE5	PAGE4	PAGE3	CWF8	CWF7	CWF6	CWF5	CWF4	CWF3	CWF2	CWF1	CWF0
($\overline{CAS}$+1)	CWF3	CWF2	CWF1	CWF0	PHI18	PHI17	PHI16	PHI15	PHI14	PHI13	PHI12	PHI11

Note WA12-WA16 output the following during $\overline{RAS}$, $\overline{CAS}$, and $\overline{CAS}$+1:

WA16	WA15	WA14	WA13	WA12
CWF8	CWF7	CWF6	CWF5	CWF4

Table 3. Sample Memory Address Multiplexing on WA0 - WA11

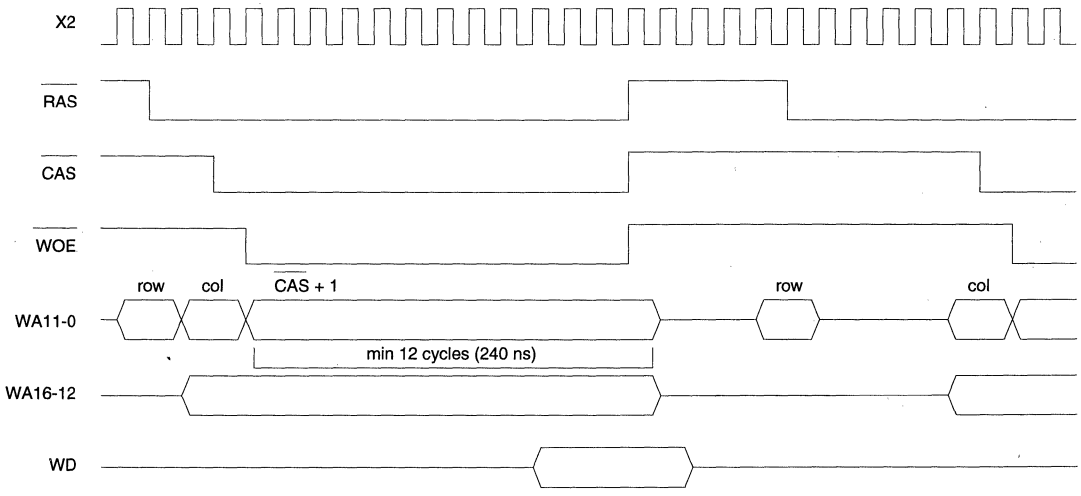


Figure 2. Typical External Memory Read Sequence

Figure 3 shows direct connection of three 4 Mbit (1Mx4) DRAM chips to form a 1Mx12 sample memory. Note that one synthesis slot can be assigned to algorithm number 16 to generate $\overline{RAS}$ before $\overline{CAS}$ refresh for Dynamic RAMs. The $\overline{CAS}$ before $\overline{RAS}$ refresh timing generated using algorithm 16 is shown in Figure 4. Note that algorithm 16 utilizes one of the synthesis slots, but this algorithm does not generate a voice. Thus, the polyphony of the CS9203 is reduced by one note when using Algorithm 16 to generate DRAM refresh.

DRAMs without enable control pins (x1 configurations) require the use of an external Flip-flop to capture the early write information (WWE) on the WA11 line at RAS time. DRAMs with static column mode access should not be used with the CS9203 because the addresses are not stable during the full CAS cycle.

Figure 5 shows the address latch circuitry required to address 8 Msamples of ROM memory. One 3-bit latch is clocked at RAS time to capture address lines WA17-WA19, the second 3-bit latch is clocked at $\overline{CAS}$ time to capture WA20-WA22. A 1Msample ROM implementation would require only the first 3-bit latch, a 128K sample ROM could be addressed directly by the CS9203.

DAC interface

The CS9203 DAC interface consists of a left/right clock signal WSBD, a bit clock CLBD and the stereo output data stream DABD or DAFD. The left/right clock signal WSBD and bit clock CLBD are common to both the main stereo serial data output DABD and the secondary stereo serial data output DAFD. The DAFD output is commonly used as a stereo effects send to an external effects processor, such as the CS8905. Two different serial DAC data formats are supported by the WSBD signal, as indicated in Figure 6. The serial DAC format is selected using the SFMT bit in the CS9203 Configuration Register. The number of data bits transmitted in the serial data output depends on the state of the SFMT bit, and on the number of synthesis slots being utilized as follows:

SFMT	Slots	Number of bits output
0	16	16
0	18	18
0	20-32	20
1	X	16

The number of bit clock (CLBD) cycles per frame is equal to two times the number of synthesis slots being used (two CLBD clock cycles per synthesis slot). When the number of synthesis slots used is larger than the number of output data bits, then the output data stream is padded with zeros as indicated in Figure 6. The most significant bit (MSB) of the left channel data is output during the slot 0 time, and the MSB of the right channel is output during the slot 8 time. The slot count sequence used in the CS9203 is represented in Figure 7. If 16 slots are utilized, the slot count sequence is straightforward (0,1, ... 15). If the slot count is greater than 16, then slots are added symmetrically after slot 7 and after slot 15. For example, if the number of slots is 20 (the number of slots is always an even number), then the slot count sequence will be (0, 1, ... 7, 16, 17, 8, 9, ... 15, 24, 25). In this case, slot numbers 18 - 23 and slot numbers 26 - 31 are not used. This allows the zero padding to be symmetrical with respect to the left channel and right channel data.

The ground reference for the DAC should be connected directly to the CS9203 GND at pin 19, and this should be the only connection between analog ground and digital ground.

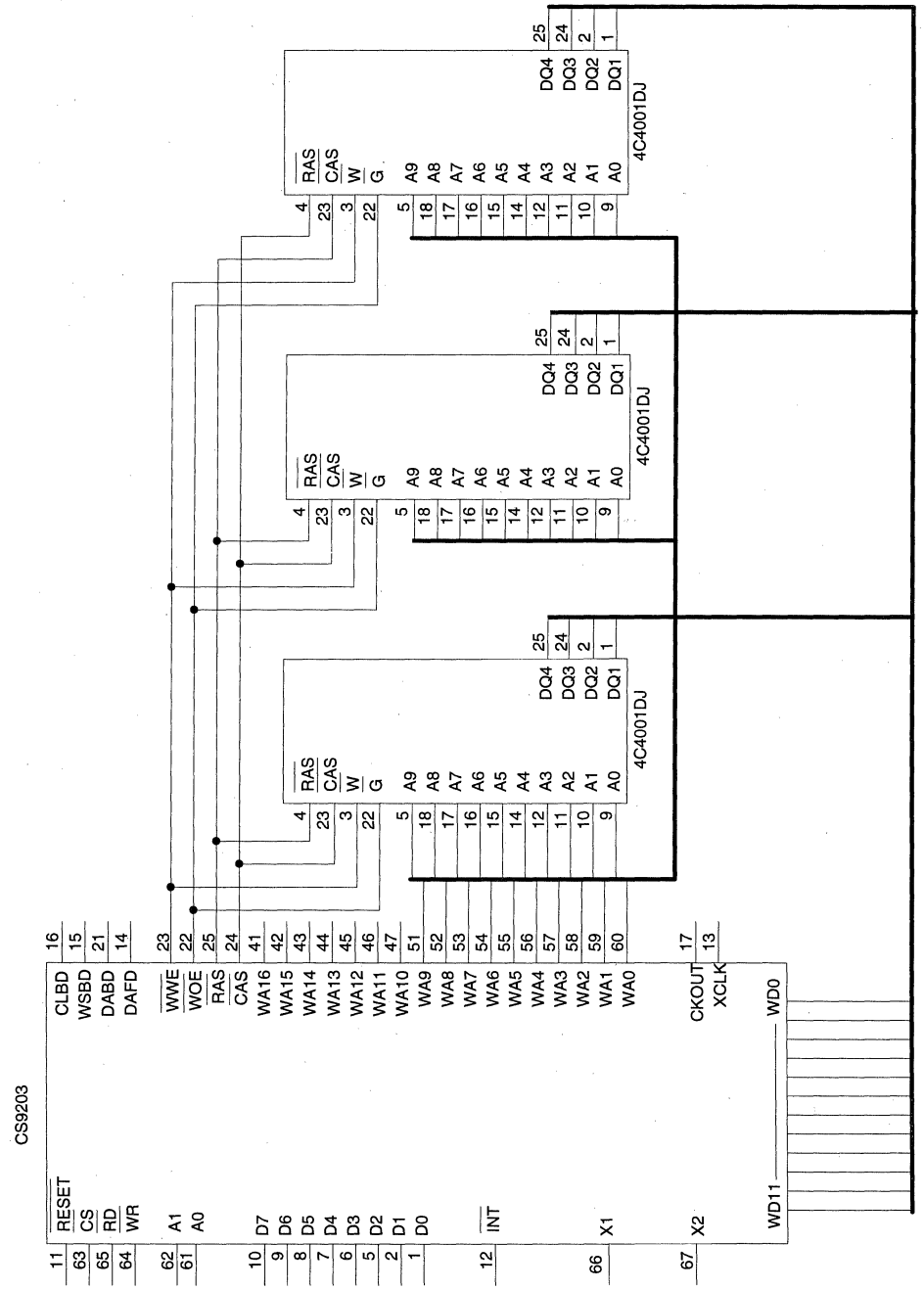


Figure 3. Direct Connection of 1M x 12 DRAM Sample Memory

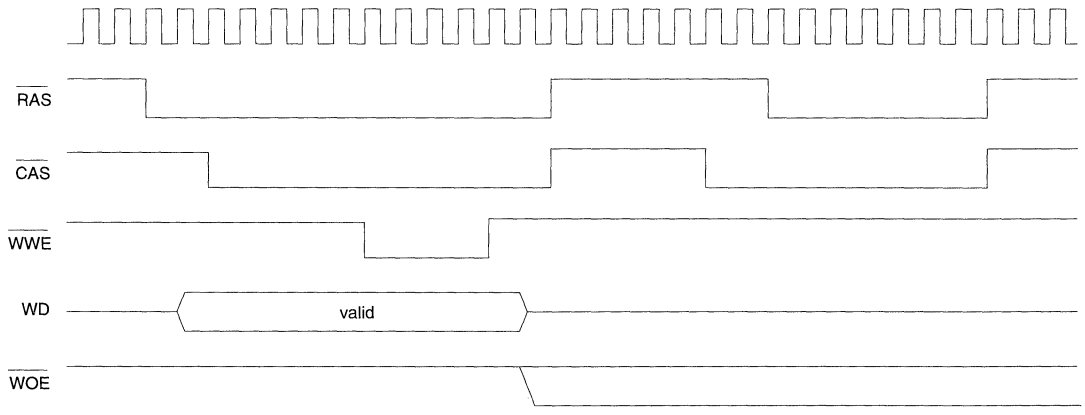


Figure 4. Algorithm 15, External RAM Write, $\overline{CAS}$ Before $\overline{RAS}$ Refresh

Oscillator Circuit

The CS9203 timing may be generated using the built-in crystal oscillator (external crystal circuit) or an external oscillator. Connections for a typical 3rd overtone series-resonant crystal oscillator circuit are shown in Figure 8. Trace lengths should be kept to a minimum, and the board layout should include ground plane beneath the oscillator circuit components.

If an external oscillator circuit in utilized, shield the input trace connecting the oscillator output to the X1 input at pin 66, and keep the trace lengths to a minimum. The ground for the oscillator circuit should be a direct connection to the CS9203 GND at pin 68.

CLKOUT and XCLK Clock Outputs

The frequency of the CKOUT output is the crystal oscillator frequency divided by four. The CKOUT output is disabled while the $\overline{RESET}$ input is low.

The XCLK output is a gated clock output which provides either 1024 or 2048 output clock pulses per synthesis frame. The period of the XCLK output pulses are the same as those of the CS9203 crystal oscillator. If the number of synthesis slots in use is less than 32, then the XCLK signal will output 64 pulses per synthesis frame for the first 16 synthesis frames executed, and then remain inactive for the balance of the frames. If the number of slots is equal to 32, then the XCLK signal will output 64 pulses dur-

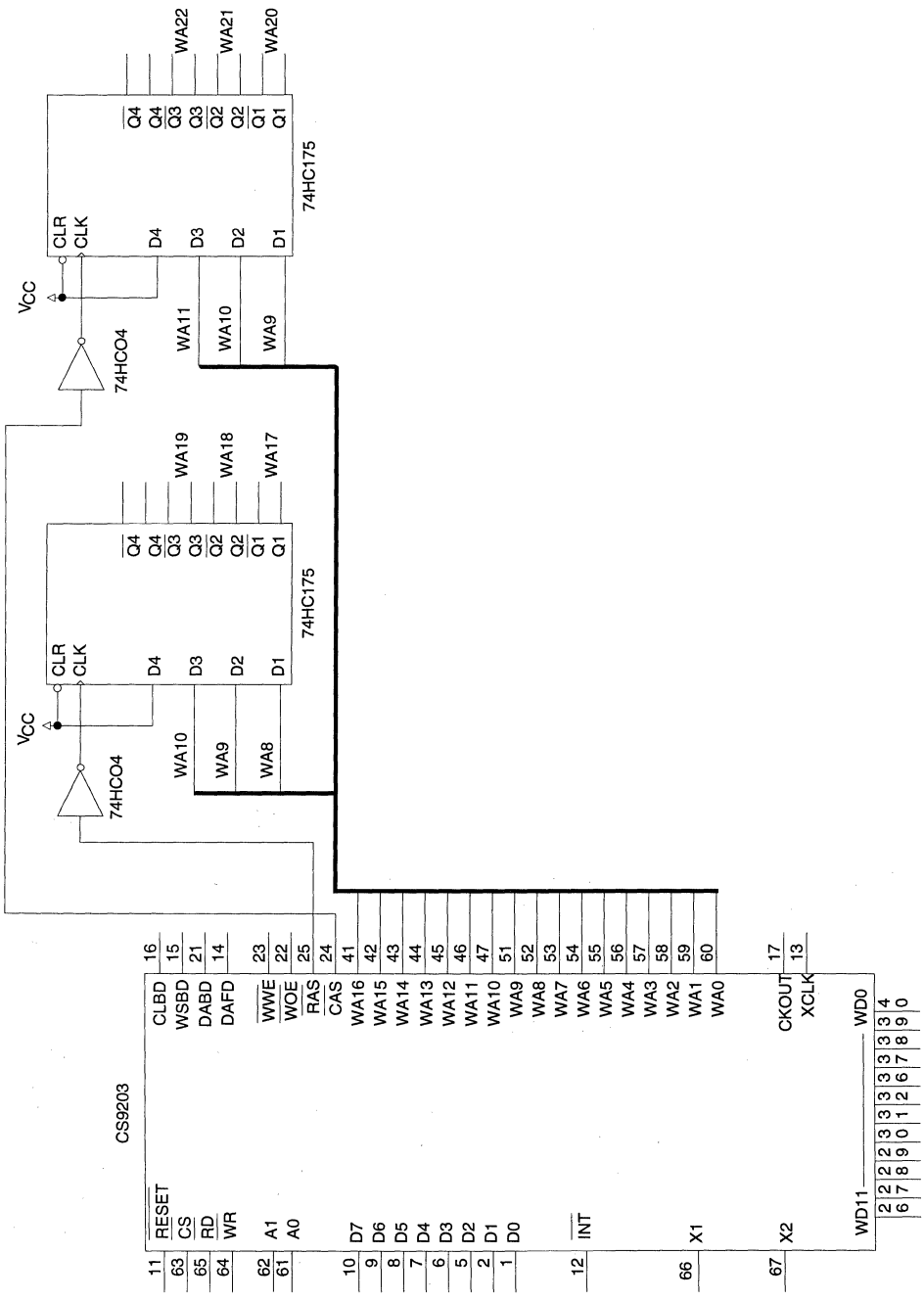


Figure 5. Address Generation for 8 Msample ROM Memory

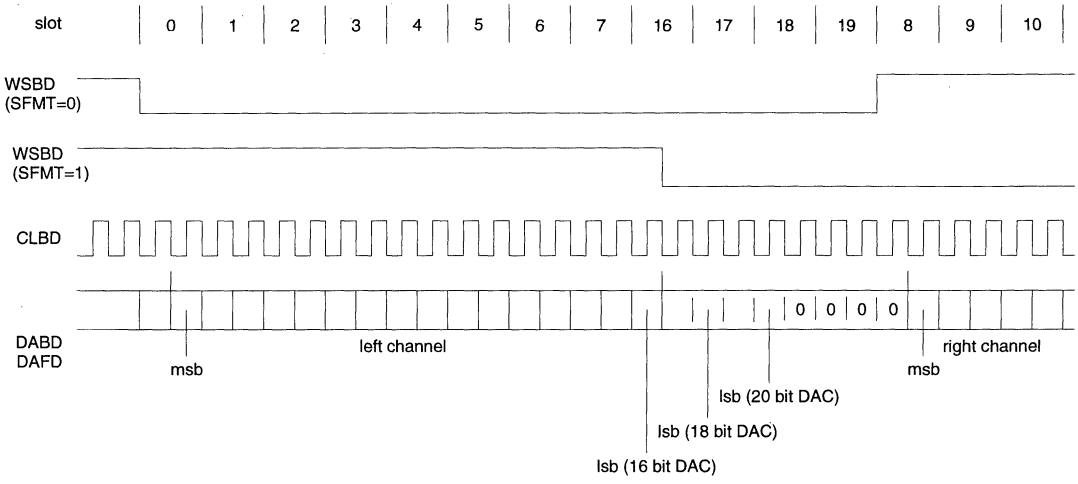


Figure 6. Typical Digital Audio Transfer Sequence (24 slots example, S3S2S1S0=1011)

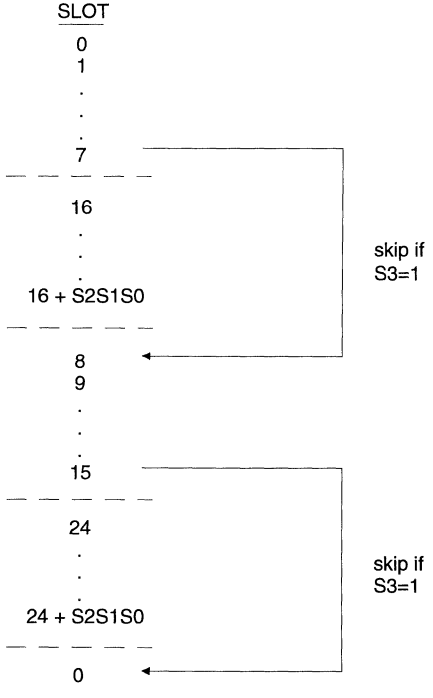


Figure 7. Slot Count Sequence

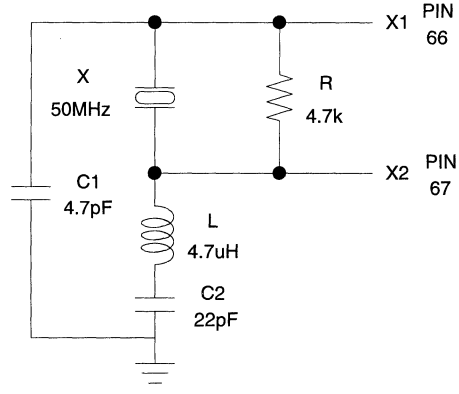


Figure 8. Typical Crystal Oscillator Component Connection

ing each of the 32 synthesis frames. Note that there are 68 crystal oscillator cycles per synthesis frame, and the XCLK output is gated 64 cycles on and 4 cycles off during each synthesis slot for which it is active. The XCLK output may be used to provide a clock input to a CS8905 when this device is used as an effects processor. The XCLK output is enabled during $\overline{\text{RESET}}$.

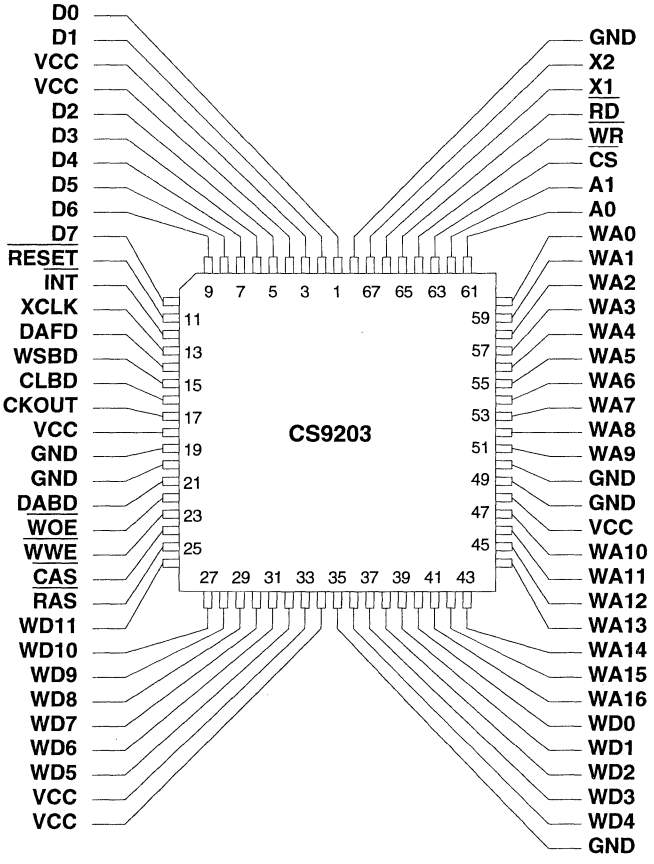
Power Connections and Decoupling

All power and ground pins on the CS9203 device should be connected to the appropriate supply planes using the shortest trace lengths possible. Recommended decoupling consists of four 0.1µF ceramic decoupling capacitors between V_{CC} and GND, one at each of the four sides of the IC. These capacitors should be placed as close to the IC as possible. In addition, place one 10µF Tantalum capacitor from V_{CC} at pin 3 to GND at pin 68 with minimum trace and lead lengths.

Power-up Reset

The $\overline{\text{RESET}}$ input must be held low until the oscillator circuit has stabilized. The CS9203 internal oscillator and the XCLK output signal are enabled during $\overline{\text{RESET}}$, other functions of the device are held in an idle mode while $\overline{\text{RESET}}$ is low.

PIN DESCRIPTIONS



Pins

D0-D7 - Bi-directional data bus to/from uP. Input/Output. PINS 1, 2, 5, 6, 7, 8, 9, and 10.

These bidirectional data lines are used to transfer data between an external microprocessor and the CS9203.

A0 and A1 - Address Bus Input from uP. PINS 61 and 62.

These pins allow an external microprocessor to select the CS9203 control register or specific data registers for read/write operations.

$\overline{CS}$ - Chip Select Input. PIN 63.

This is the CS9203 chip select input from an external microprocessor. Active low.

$\overline{WR}$ - Write to Chip Input. PIN 64.

This signal is the write strobe input to the CS9203 from an external microprocessor. This strobe is used to write to the CS9203. Active low.

$\overline{RD}$ - Read from Chip Input. PIN 65.

This signal is the read strobe input to the CS9203 from an external microprocessor. This strobe is used to read data from the CS9203. Active low.

$\overline{INT}$ - End of Envelope Interrupt Output. PIN 12.

This signal is an interrupt output from the CS9203 to an external microprocessor. Active low.

$\overline{RESET}$ - Chip Reset Input. PIN 11.

This active low input to the CS9203 is used to reset and initialize the CS9203. Active low.

X1 - Xtal Oscillator Input. PIN 66.

This signal is the input for the internal oscillator. A maximum crystal frequency of 50 MHz is supported. An external oscillator clock output signal may be connected at this pin.

X2 - Xtal Oscillator Output. PIN 67.

This signal is the internal oscillator output.

CKOUT - Clock Output. PIN 17.

This signal is an output clock. The clock frequency is the CS9203 oscillator frequency divided by four.

XCLK - External Effect Processor Clock Output. PIN 13.

This is a gated clock output. The clock period is the same as that of the CS9203 oscillator. If the number of synthesis slots being used is less than 32, then 1024 pulses will be output per synthesis frame. If 32 slots are programmed, then 2048 pulses will be output per frame.

WA0-WA16 - Multiplexed External Memory Address Output. PINS 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 47, 46, 45, 44, 43, 42, and 41.

These output address lines are used to address external sample memory.

WD0-WD11 - External Memory Data Input/Output. PINS 40, 39, 38, 37, 36, 32, 31, 30, 29, 28, 27, and 26

These bidirectional data lines are used to pass sample data between the CS9203 and external sample memory.

$\overline{CAS}$ - WA0-WA11 Column Address Strobe Output. PIN 24.

This memory address strobe output is used in conjunction with the multiplexed address output lines WA0-WA16.

$\overline{RAS}$ - WA0-WA11 Row Address Strobe Output. PIN 25.

This memory address strobe output is used in conjunction with the multiplexed address output lines WA0-WA16.

$\overline{\text{WOE}}$ - External memory Data Output Enable. PIN 22.
This signal is an output enable for external sample memory.

$\overline{\text{WWE}}$ - External Memory Write Output. PIN 23.
This signal is a write enable strobe for external sample memory.

CLBD - External DAC/Effect Serial Clock Output. PIN 16.
This signal is the bit clock for the CS9203 stereo serial digital audio outputs DABD and DAFD.

DABD - External DAC Serial Data Output. PIN 21.
This is the primary stereo serial digital audio output from the CS9203.

DAFD - External Effect Serial Data Output. PIN 14.
This is the secondary stereo digital audio output from the CS9203. This output is commonly used as an effects send to an outboard digital effects processor such as the CS8905.

WSBD - External DAC Effect Right/Left Channel Output. PIN 15.
This signal is the left/right word clock for the DABD and DAFD stereo digital audio outputs of the CS9203.

GND - Power Ground. PINS 19, 20, 35, 49, 50, and 68.
Ground pins. All ground pins should be connected to a low impedance ground plane.

VCC - Power +5V, ±5%. PINS 3, 4, 18, 33, 34, and 48.
+5V power input pins. All V_{CC} pins should be connected to a low impedance +5V supply.

• Notes •

MIDI Wavetable Synthesizer Solutions

by
Jim Heckroth

Introduction

There are a growing number of applications requiring the storage and reproduction of high quality music and sound effects in computer-based systems. These applications include the generation of sounds for multimedia presentations, computer games, and karaoke equipment. PCM formats, such as WAV files, allow storage and reproduction of high quality sound, but for lengthy pieces of music the resulting file sizes can be quite large. The Musical Instrument Digital Interface (MIDI) protocol provides an extremely efficient means of storing musical performance information, and use of the MIDI protocol for generation of sound in computer-based applications is growing rapidly.

The MIDI protocol was developed to allow musical instruments to be connected together. In MIDI systems, musical performance information is sent in the form of MIDI messages from a controlling device to a music synthesizer, which produces the sounds. The MIDI messages tell the synthesizer which sounds should be used, which notes should be played, and how loud the notes should be played. The sounds are then generated by the synthesizer. Since the MIDI data file contains these instructions, rather than the actual digitally sampled sounds, the file size is relatively small. Because the synthesizer must generate the actual sounds, the overall quality of the audio output of the system will depend largely on the quality of the MIDI synthesizer.

Two- and four-operator FM synthesizers have found widespread use in audio adapter cards for PCs because of their low cost. However, for applications requiring higher quality sound, wavetable synthesis methods are preferable. Wavetable synthesizers utilize digitally sampled sounds, and produce instrument sounds which are much more realistic than FM methods. Although wavetable methods are inherently more expensive than FM, technological advances have reduced the cost of implementing high quality wavetable synthesizers.

This paper presents an overview of two different cost effective high quality wavetable synthesis solutions, based on the Crystal Semiconductor CS9203 music synthesis chip. The first solution utilizes the CS9203 synthesizer with a two megabyte sample set. This solution provides full General MIDI (GM) compatibility at an extremely attractive price/performance ratio. The second solution also employs the CS9203 for synthesis, but the sample memory size is increased to four megabytes, and the CS8905 chip is added as a digital effects processor for the generation of reverb and chorus effects. This expanded solution is both General MIDI and Roland General Synthesizer compliant. Both

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solutions use an industry standard 80C32 microprocessor as a controller. Crystal Semiconductor support for the CS9203-based includes evaluation boards, reference designs, and complete design data. The design data available for the synthesizer solutions presented here includes full schematics and Bill of Materials (BOM), executable code for the 80C32-1 microprocessor, and the sample data for the two megabyte or four megabyte sample ROM.

CS9203 Music Synthesizer Chip

The CS9203 is a high polyphony multi-timbral digital sound generator which features built-in synthesis algorithms for musical applications. The CS9203 is capable of generating 16 to 32 notes of polyphony. The Output sampling period is divided into a corresponding number of synthesis slots, and each slot generates one note or voice. There are 16 words of on-chip private parameter data memory associated with each synthesis slot. The parameter data for each slot specifies which algorithm will be used for that slot, along with any parameters used by the algorithm. These parameters control functions such as the pitch, the digital filtering characteristics, and the output amplitude and mix for the note being produced by a slot. The synthesis parameters are dynamically written into the CS9203 parameter memory from an external processor to control the sounds being generated. The CS9203's external data bus is 12 bits wide. Internal data paths are 19 bits wide, and the final accumulators are 24 bits wide. 16 bit to 18 bit DACs are supported.

The CS9203 High-Quality Sampling Algorithm

The High-Quality Sampling algorithm is the most powerful of the CS9203 synthesis algorithms. This is a sample playback algorithm for wavetable synthesis. The algorithm supports sample looping, and variable playback rates are supported using an 18 bit address increment parameter with 12 bits of fractional address resolution. Linear interpolation is used in the pitch shifting process. A polyphonic variable-Q, variable-cutoff digital low-pass filter is implemented for timbre adjustment. Piecewise linear envelopes are generated one segment at a time by specifying the starting value and the increment/decrement to be added to this value at each frame time. Separate envelope generators are implemented for the output amplitude and for the digital filter cutoff frequency. The output mix for the two stereo digital audio output accumulators of the CS9203 are programmed independently.

A Low-Cost General MIDI Compliant Wavetable Synthesizer Design

A block diagram for a CS9203-based General MIDI wavetable synthesizer is given in Figure 1. The main components of this system are an industry standard 80C32 microprocessor with 128Kx8 external ROM and 32Kx8 external RAM, the CS9203 synthesizer with 2Mx8 external sample memory, and a 16-bit stereo DAC and the associated audio output circuitry.

The 80C32 microprocessor, running at 16 MHz, functions as the system controller. The 80C32 receives MIDI messages, interprets these messages, and then makes changes to the CS9203 parameter RAM (P_RAM) as required to generate the desired sounds. This implementation utilizes the CS9203 High Quality Sampling algorithm for virtually all of the instrument sounds. Tables containing the characteristics for each instrument are stored in the 80C32's external ROM memory. These tables identify the sample memory locations, address increment values, digital filter characteristics, envelope characteristics, and default output level and mix for each note

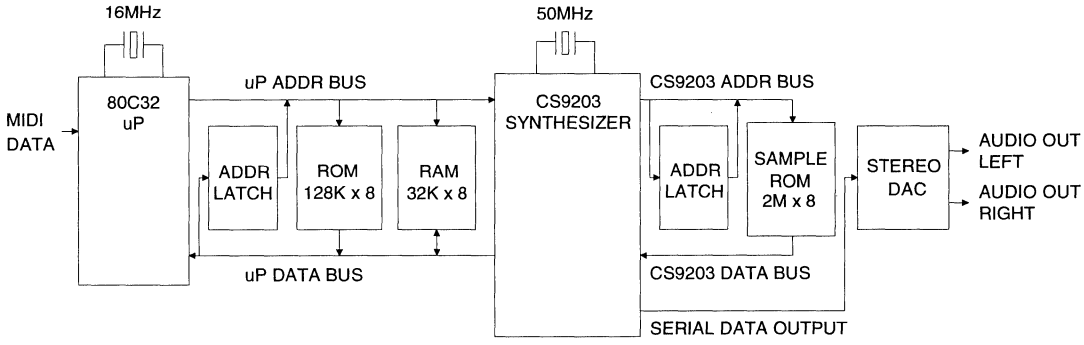


Figure 1. CS9203-based General MIDI Synthesizer Block Diagram

5

number of each instrument. When the 80C32 receives a MIDI Note On message, it looks up the parameter data for the desired note, and then writes the appropriate parameter values into the Parameter RAM memory within the CS9203. The CS9203 then generates the desired sound.

In this design, the CS9203 is configured for 24 synthesis slots per frame, allowing the generation of up to 24 simultaneous notes. The 80C32 will respond to MIDI messages on any of the 16 logical MIDI channels, so up to 16 different instrument sounds may be utilized simultaneously (the 24 notes of polyphony may be distributed among up to 16 different instruments at any given time). For a CS9203 running at 50 MHz, the output word rate (sampling rate) is 30.64 kHz.

The 2M x 8 sample set contains 263 sound samples which are used to generate 159 melodic timbres and variations, and 118 drum sounds. Critical instruments are oversampled, and amplitude envelope compression has also been employed on selected samples. Key splits and techniques such as velocity-controlled polyphonic digital filtering are employed for some instrument sounds to provide maximum realism. The resulting sound quality is excellent when using 8 bit samples. Of course, the sample word size can be increased to 12 bits for applications requiring even higher sound quality. The instrument and drum mappings comply with the General MIDI (GM) standard. Many of the General Synthesizer (GS) variation sounds, including all of the GS drum sets, are also implemented. There is an MT-32 compatible mode which maps MT-32 sounds into the GM patch set, allowing MIDI files which were generated for the popular Roland MT-32 sound module to be played back using the GM sounds.

The CS9203 digital audio output is routed to the DAC to create the analog output signal. Only one of the CS9203's two stereo 16 bit digital audio outputs is required in this application.

It should also be noted that the MIDI input to the 80C32 could be in either serial format, or in parallel format. The former case would be applicable for stand alone MIDI sound modules or for wavetable synthesizer subsystems or daughter cards for PC sound card applications. The parallel MIDI interface is useful for applications such as a wavetable synthesizer add-in card for the PC, where the 80C32 could be used to implement an MPU-401 UART mode compatible interface to the PC bus.

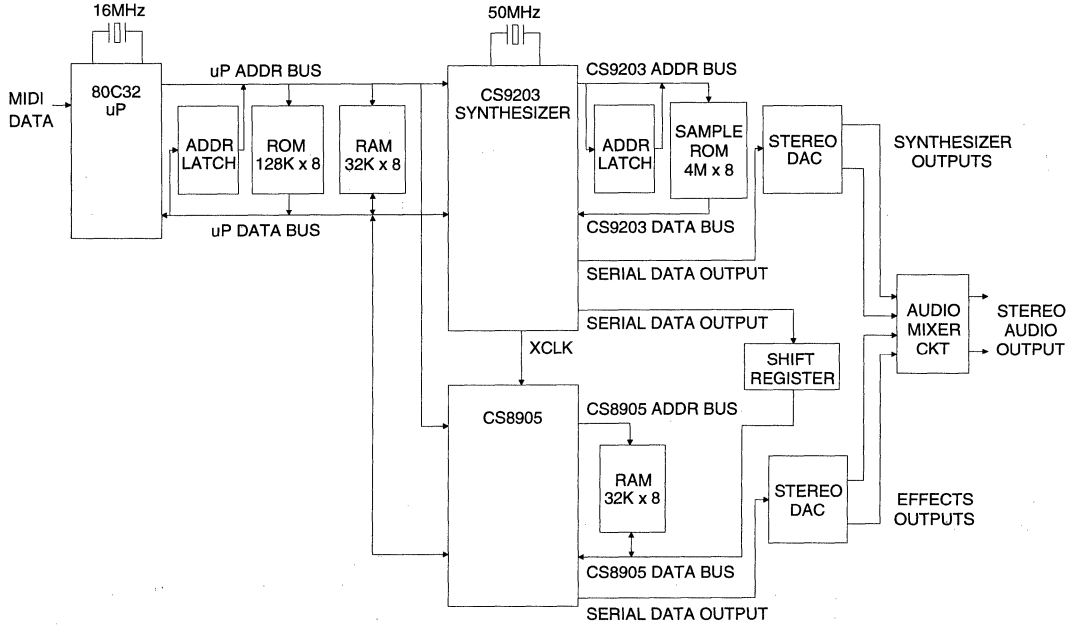


Figure 2. CS9203/CS8905-based GM and GS Compatible Synthesizer

Crystal Semiconductor can provide complete documentation and design data for this application, including executable 80C32 code and sample data for the sample ROM.

A High-Performance General MIDI and General Synthesizer Compatible Design

The block diagram given in figure 2 shows a CS9203-based wavetable synthesizer solution which employs the CS8905 chip as a digital effects processor for the generation of digital reverb and chorus effects. The CS8905 is a general purpose programmable digital sound generator which is suited for use as a digital effects processing engine. This solution complies with the General MIDI (GM) and the Roland General Synthesizer (GS) standards.

The 80C32 controller circuitry and the CS9203 synthesizer circuitry are fundamentally the same as described in the previous paragraphs, with the CS9203 sample memory size increased to 4Mx8. In this solution, however, the second stereo 16 bit digital output from the CS9203 is used as an effects send path to the CS8905. The effects processing algorithms for the CS8905 are stored in on-chip RAM Algorithm Memory. The CS8905 Parameter Memory is also on-chip RAM. The effects algorithms and associated parameter data are loaded into the CS8905's internal RAM by the 80C32 when the system is powered on.

A shift register is used to convert the serial data output from the CS9203 into parallel form for use by the CS8905. The CS8905 utilizes a 32Kx8 external RAM for the effects signal processing. The CS9203 XCLK output is used to clock the CS8905. The XCLK output is 1024x the CS9203 output word rate, and this provides

synchronization between the CS9203 and the CS8905.

The audio output from the CS9203 is a "dry output" containing instrument sounds with no effects. The CS8905 digital audio output is effects only. The outputs from the CS9203 and the CS8905 are mixed together into a stereo analog output using external operational amplifiers in a summing configuration.

The lower 2Mx8 of sample memory for the CS9203 contains the sample data for the General MIDI instrument set. Many of the General Synthesizer variation sounds, including all of the GS drum sets, are also implemented in the lower 2Mx8 sample memory. This sample data is the same data which is used for the low cost General MIDI Synthesizer solution described in the previous section. An additional 2Mx8 of sample memory has been added to complete the Roland General Synthesizer sound set and to implement additional splits for the base sounds included in the lower 2Mx8 sample memory. The resulting 4Mx8 sample set contains a total of 514 sound samples which are used to generate 191 melodic timbres and variations, 118 drum sounds, and 46 special effects sounds. The instrument and drum patch mappings are compatible with the General MIDI and General Synthesizer standards, and an MT-32 compatibility mode is also included.

This solution employs the same synthesis techniques described in the previous section, and the resulting implementation is also 16 part multi-timbral with 24 notes of polyphony. Complete design data, including 80C32 code and sample data for the CS9203 sample memory, is available from Crystal.

Summary

This paper has presented an overview of two music synthesizer implementations, based on the Crystal Semiconductor CS9203 Advanced Music Synthesizer IC. These solutions both feature high quality sounds generated using wavetable synthesis techniques, and both comply with industry standard performance requirements and instrument patch mappings. The two solutions presented provide two distinct performance points; full General MIDI compatibility or full Roland General Synthesizer compatibility, and both solutions provide excellent price/performance value. In addition, Crystal Semiconductor can provide design documentation, executable code, and sample data to help minimize time-to-market for implementation of these designs.

CDBGMR4 Music Synthesis Eval. Board

FUNCTIONAL OVERVIEW

The CDBGMR4 eval. board is a high polyphony multi-timbral wave table synthesizer with added reverb and chorus effects, implemented using the CS9203 synthesizer and the CS8905 as effects processor. The exceptional sound quality of the solution makes it suitable for business, education, entertainment, computer games, multimedia, and creative musical compositions.

The CDBGMR4 is fully General MIDI compliant (24 note polyphony, 16-part multi-timbral) and supports the General Synthesizer (GS) format. In addition, the solution is compatible to the popular Roland SCC-1 and MT-32 sound modules.

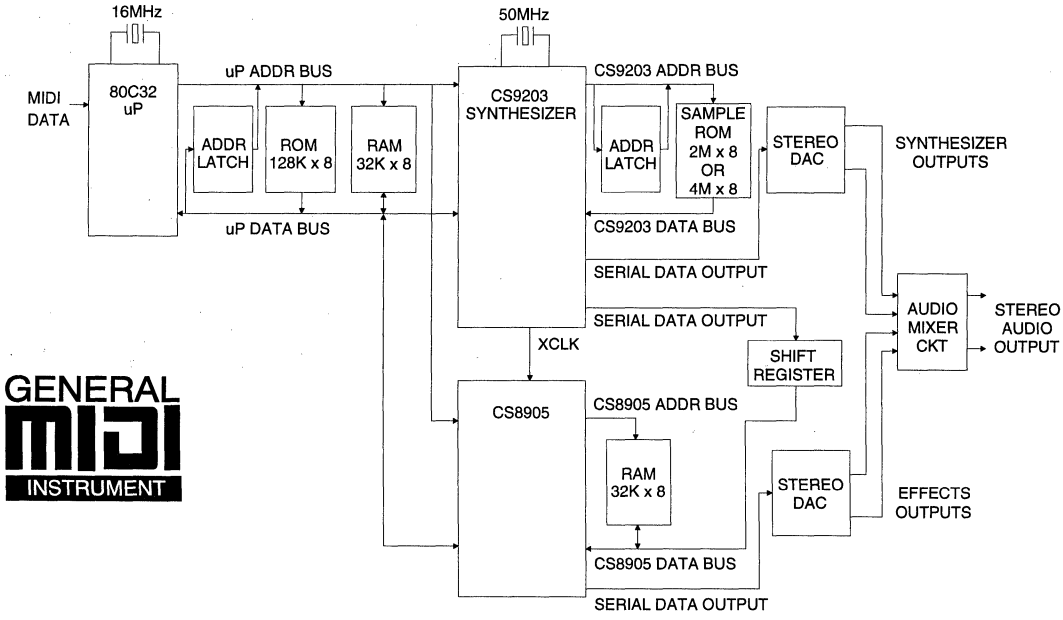
Either 2 or 4MBytes of wave table sample data may be used (supplied under license by Crystal). The 4MByte sample set can generate 191 melodic timbres and variations, 118 drum sounds, and 46 special effects.

In the design, an 80C32 micro-processor is used as the main system controller -- among other tasks, the 80c32 interprets the MIDI command stream for synthesis by the DSP. The MIDI interface is MPU-401 compatible (without tape sync., din sync or the metronome option).

The high integration ensures that the CDBGMR4 may be used in mid-range PC audio adapter boards, as well as standalone MIDI music modules.

ORDERING INFORMATION:

CDBPGMR4	PC adapter board
CDBGMR4	Stand alone MIDI module



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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Introduction

There are a growing number of applications requiring the storage and reproduction of high quality music and sound effects in computer-based systems. These applications include the generation of sounds for multimedia presentations, computer games, and karaoke equipment. PCM formats, such as WAV files, allow storage and reproduction of high quality sound, but for lengthy pieces of music the resulting file sizes can be quite large. The Musical Instrument Digital Interface (MIDI) protocol provides an extremely efficient means of storing musical performance information, and use of the MIDI protocol for generation of sound in computer-based applications is growing rapidly.

The MIDI protocol was developed to allow musical instruments to be connected together. In MIDI systems, musical performance information is sent in the form of MIDI messages from a controlling device to a music synthesizer, which produces the sounds. The MIDI messages tell the synthesizer which sounds should be used, which notes should be played, and how loud the notes should be played. The sounds are then generated by the synthesizer. Since the MIDI data file contains these instructions, rather than the actual digitally sampled sounds, the file size is relatively small. Because the synthesizer must generate the actual sounds, the overall quality of the audio output of the system will depend largely on the quality of the MIDI synthesizer.

Two- and four-operator FM synthesizers have found widespread use in audio adapter cards for PCs because of their low cost. However, for applications requiring high quality sound, wave-table synthesis methods are preferable. Wave table synthesizers utilize digitally sampled sounds, and produce sounds which are much more realistic than FM methods. Although wave table methods are inherently more expensive than FM, technological advances have reduced the cost of implementing high quality wave table synthesizers.

The CDBGMR4 Reference Design(s)

Three different cost effective General MIDI (GM) compatible wave table synthesis solutions may be implemented based on the Crystal Semiconductor CS9203 Advanced Music Synthesizer: 1) a base level solution consisting of the CS9203 with 2 Mbytes of wavetable sample data; 2) a mid-range solution, featuring higher quality sounds as well as many new sounds, may be obtained by using the CS9203 with a 4 Mbyte wavetable sample set; 3) the highest-end solution combines the CS9203 with 4 Mbytes of wavetable sample data, and the CS8905 Programmable Music Processor. The CS8905 implements reverb and chorus algorithms, compatible with the Roland SoundCanvas (GS).

All three solutions use an industry standard 80C32-1 microprocessor as a controller. The evaluation board implements the highest quality solution; a design based on the CS9203 alone may be emulated by turning off the effects processing, and disabling the upper 2 Mbytes of sample data. This is accomplished by replacing the 80C32-1 control software (alternate EPROMs included). See the hardware installation section for details.

The reference designs described here are supported with schematics and bill of materials. Floppy diskettes containing the executable code for the 80C32-1 micro-processor, wavetable sample data and eval. board schematics are available from Crystal. If you require direct technical support, please contact Crystal Semiconductor's Applications Hotline.

CS9203 Advanced Music Synthesizer

Features

The CS9203 is a high polyphony multi-timbral digital sound generator which features 16 built in synthesis algorithms for musical applications. The main features of the CS9203 include: polyphonic up to 32 notes, (single voices can generate 3 drum sounds); multi-timbral up to 32 simultaneous timbres; oscillator frequencies to 50 MHz; sampling rate of 23 kHz to 46 kHz allows polyphony vs. sampling rate trade-off; two stereo 16 bit digital audio outputs (four audio outputs); 16 built-in synthesis algorithms include high-quality sampling algorithms with interpolation; on-chip 512x19 Parameter RAM; Signal Processing Unit includes adder, multiplier, and special functions for interpolation, phase computation, and envelope generation; 24 bit accumulators with clipping circuitry; built-in sine and ramp data; addresses up to 8Mx12 external sampling memory (ROM, SRAM, or DRAM); independent pan and volume mix assignable for each sound component/algorithm; stereo effect send level and balance assignable per voice; operates from a single +5V supply; implemented in CMOS with 50 mW typical power dissipation.

Functional Description

The CS9203 synthesis algorithms are built in. Each output sample period is considered a synthesis frame, which is divided into 16 to 32 synthesis time slots. Each synthesis slot executes in 68 cycles of the crystal clock. Thus the output sample rate or frame rate is the crystal frequency divided by 68 times the number of synthesis slots in use; Sample Rate = Crystal Frequency/(68 x Number of Slots). There are 16 words of parameter data associated with each synthesis slot. The parameter data for each slot specifies which algorithm will be used for that slot, along with any parameter data used by the algorithm. The synthesis parameters are downloaded into internal RAM memory from an external processor or controller. Each synthesis slot can generate a voice, allowing up to 32 note polyphony. A given algorithm may be utilized by more than one synthesis slot, and a single algorithm may be used to generate different timbres depending on the synthesis parameter data associated with each slot using the algorithm. For example a high quality sampling algorithm may be utilized by several synthesis slots simultaneously, with each slot specifying different sound samples. Thus the CS9203 allows implementations which are up to 32 part multi-timbral. The CDBGMR4 design supports 24 note polyphony, in exchange for a higher digital audio sampling rate.

CS8905 Programmable Music Processor

Features

The CS8905 is a general purpose programmable digital sound generator, ideally suited for low cost wave table synthesis or digital effects processing. The CDBGMR4 uses the CS8905 to provide Roland SoundCanvas (GS) compatible reverb and chorus processing. The main features of the CS8905 include: polyphonic up to 16 notes, with each voice capable of generating 3 drum sounds; multi-timbral up to 16 simultaneous timbres; oscillator frequencies to 45.1584 MHz (for 44.1 kHz sampling rate); stereo 16 bit digital audio output; on-chip 256x15 Algorithm RAM, and 256x19 Parameter RAM; 19 bit internal data paths; 19 bit adder, and 12x12 multiplier; 24 bit accumulators with clipping circuitry; built-in sine and ramp data; addresses up to 1Mx12 sample ROM directly, 64Mx12 using paging; independent pan and volume mix assignable for each sound component/algorithm; operating from a single +5V supply; implemented in CMOS with 50 mW typical power dissipation.

Functional Description

The CS8905 executes instructions from an internal 256x15 RAM algorithm memory (A_RAM). This memory can be configured to accommodate either 4 or 8 effects algorithms. The CS8905 out-

puts one stereo audio sample for every 1024 cycles of the crystal clock. Each output sample period is considered an effects processing frame, which is divided into 16 effects time slots. Each effects slot executes one effects algorithm in 64 cycles of the crystal clock. An effects algorithm consists of 30 micro-instructions and each micro-instruction executes in 2 cycles of the crystal clock. The last 4 cycles of each effects slot are reserved for internal operations. There are 16 words of parameter data associated with each effects slot. The parameter data for each slot specifies which algorithm will be used for that slot, along with any parameter data used by the algorithm. The parameter data is stored in an internal 256x19 RAM parameter memory (P_RAM). The algorithms and effects processing parameter data are downloaded into internal RAM memory from an external processor or controller. A given algorithm may be utilized by more than one effects slot, and a single algorithm may be used to generate different t effects depending on the parameter data associated with each slot. With alternate program and parameter data, combined with a 1MX8 wavetable sample set, the CS8905 can perform music synthesis tasks with 16-note polyphony and up to 16 timbres.

The CDBGMR4 GM/GS Compatible Wave Table Synthesizer with Digital Effects

The block diagram given on the cover page shows a CS9203 based wave table synthesizer solution which employs the CS8905 chip as a digital effects processor to generate effects such as reverb and chorus. This solution utilizes an industry standard 80C32 processor as a system controller. The synthesis algorithms for the CS9203 are ROM-coded on-chip. The parameter data for each patch to be used is stored in the 80C32 ROM and downloaded from the 80C32 into the 512x19 Parameter RAM (P_RAM) in the CS9203. The synthesis algorithms, in combination with the associated parameter data for each slot, utilize the sample ROM to generate sounds.

The 80C32 receives MIDI messages from the host PC. The host interface implemented in the 80C32 is compatible with the UART mode of the Roland MPU-401 MIDI interface. The characteristics of each patch or sound are stored in the 80C32 memory space. These characteristics include the algorithm number and sample data to be used by the CS9203 in generation of the sound, and other parameters such as amplitude envelope information, which are used by the 80C32 to dynamically adjust the sound during synthesis. The 80C32 interprets the MIDI messages from the host and then dynamically adjusts the parameter data of the CS9203 in order to generate the appropriate sounds.

For a CS9203 running at 50 MHz, the output word rate (sampling rate) is 30.64 kHz. The primary audio output from the CS9203 is a "dry output" with no effects. The second stereo 16 bit digital output from the CS9203 is used as an effects send path to the CS8905. The effects algorithms and associated parameter data are downloaded from the 80C32 into the CS8905 internal algorithm RAM and parameter RAM. The CS8905 utilizes a 32Kx8 external RAM for the effects signal processing. A shift register is used to convert the serial data output from the CS9203 into parallel form for use by the CS8905. The CS9203 XCLK output is used to clock the CS8905. The XCLK output is 1024x the CS9203 output word rate, and this provides synchronization between the CS9203 and the CS8905. The CS8905 digital audio output is effects only. The effects output from the CS8905 and the dry output from the CS9203 are mixed together into a stereo analog output using external operational amplifiers in a summing configuration. In solutions using the CS9203 without the CS8905, the secondary audio output from the CS9203 is not used.

Crystal Semiconductor can provide executable 80C32 code and sample data for CS9203-based implementations using either 2Mx8 or 4Mx8 of sample data. Both of these approaches feature high quality sounds with 24 notes of polyphony, and both are 16 part multi-timbral.

The 2M x 8 sample set contains 263 sound samples which are used to generate 159 melodic timbres and variations, and 118 drum sounds. The instrument and drum patch mappings are compatible with the GM/GS standards, and an MT32 compatibility mode is included.

The 4M x 8 sample set contains 514 sound samples which are used to generate 191 melodic timbres and variations, 118 drum sounds, and 46 special effects sounds. The instrument and drum patch mappings are compatible with the GM/GS standards, and an MT32 compatibility mode is included. Many of the patches have "splits", wherein different samples are used for different ranges of key numbers to improve the realism of the resulting sounds. In addition, "filters" are utilized in some cases to modify the sound envelope as a function of key velocity.

Summary

This reference design manual has presented an overview of three low-cost General MIDI-compatible music synthesizer implementations, based on the Crystal Semiconductor CS8905 and CS9203 synthesis chips. All three of these solutions feature high quality sounds generated using wave table synthesis techniques. These three implementations have been selected to allow a price/performance trade-off in selecting an appropriate synthesis solution, while maintaining very high cost effectiveness at each level of performance. Design support from Crystal, including evaluation boards, executable 80C32 controller code, and sample data for the 2Mx8 and 4Mx8 sample sets, help minimize time-to-market for these approaches.

HARDWARE INSTALLATION

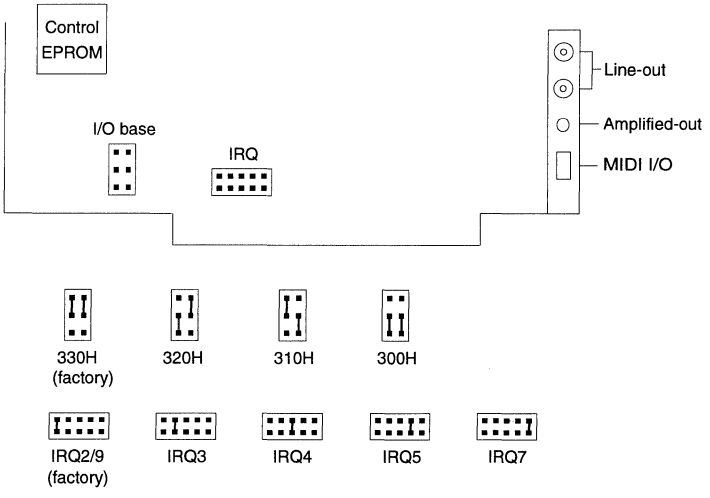
Discharge the static electricity that your body may have accumulated before removing the synthesizer adapter card from it's static-protection envelope (touch a piece of grounded bare metal). Take appropriate precautions to avoid injury due to electric shock before using.

Standalone MIDI module
The standalone version of the CDBGMR4 requires no special configuration, and is a complete MIDI music synthesizer module. The board requires a 9V AC transformer, with a rated output of at least 1.3A (the CDBGMR4 board does not require so much power, however many in-expensive power supplies drop their output voltages when placed under load. The output amplifier in this design is sensitive to such drops). With the connector side facing, the signals from left-to-right are: L & R line-out; MIDI IN, and power. Alternative designs with a PC compatible RS232 serial port interface, or MIDI IN, OUT, & THRU are available. Driver software supporting the RS232 serial port interface under Microsoft Windows 3.1 is available.

PC adapter board version
Before installing the CDBPGMR4, check whether the default **I/O address** of **330h**, or the default **IRQ** of **2/9** (standard for MPU-401) conflicts with a currently installed adapter card. If so, either the CDBPGMR4 must be changed (see below) or the conflicting adapter card must be removed.

The CDBPGMR4 requires an 8-bit PC-XT compatible slot in any ISA or EISA bus system. After choosing a slot, remove the protective cover and save for later use, insert adapter and press firmly to be sure that it is fully seated. Be sure to re-attach the bracket mounting screw. Close your computer and attach speaker/headphone cables before powering up your system.

The CDBPGMR4 may be modified to emulate a system design based solely on the CS9203, without the CS8905 acting as an effects processor. In addition, the high 2Mbytes of wavetable sample data may be disabled. Several price/performance points are thus testable. To change the function of the board: remove the control EPROM from the socket (shown below) and store it for future use; select either PCGM16 (no reverb or chorus, 2 megabyte sample set) or PCGMR16 (2 mega-



CDBPGMR4 - Jumper Settings

byte sample set with reverb and chorus) EPROM; insert the new control code into the socket (the chip cannot be inserted incorrectly); re-install adapter card in your computer. No further configuration will be necessary.

SOFTWARE INSTALLATION

DOS Environment (games)

No special configuration is necessary to support software in the DOS environment. DOS based MIDI sequencers and games software generally recognize the Roland MPU-401 interface to MIDI synthesizers. Games software requiring either MT-32, MPU-401, Roland (LAPC-1), Roland SoundCanvas, SCC-1 or General MIDI can be supported by the CDBGMR4.

The General MIDI standard was adapted in early 1991, games written prior to that support older standards such as MT-32. If you know that you will be using the CDBGMR4 in its MT-32 compatibility mode, a DOS based configuration utility (supplied) may be used to set the CDBGMR4 to MT-32 mode. The sound mapping in MT-32 mode is somewhat similar to General MIDI, so even if the configuration utility is not used, many sounds will be adequately reproduced.

Microsoft Windows™ Environment

The CDBGMR4 fully supports Microsoft Windows 3.1/NT and is compliant with the Extended Multitimbral specification for Multimedia Personal Computers Level 2. For details on this standard, please contact the MPC Marketing Council in Washington, D.C.

MPU-401 driver software is not part of the kit supplied by Crystal, and must be installed separately. The driver is included as part of the retail version of Microsoft Windows 3.1. To install: run the Windows Control Panel; then the Drivers applet; choose Add; select Roland MPU-401; configure to proper address and IRQ; OK to end. After installation, you must restart Windows 3.1 for the change to take effect.

After MPU-401 installation, the MIDI Mapper program must be run. To configure: run the Windows Control Panel, then the MIDI Mapper applet, select NEW, and choose the MPU-401 interface for the first 10 channels. The other channels are not generally used in the Windows environment, though they are supported by the CDBGMR4 board. Channels 13-16 are most often used by FM synthesizers -- if you have a Sound Blaster or compatible board in your system, then configure those channels for AdLib or Voyetra OPL3 support. It is OK to configure all channels to use the MPU-401 interface.

As soon as the MIDI Mapper is configured, you are ready to play MIDI files. A sequencer is necessary -- the Media Player has basic sequencing functions built in and may be used to play *.MID files. More comprehensive MIDI sequencers are available from several vendors, some supporting musical staff notation. It is recommended that such a sequencer be obtained, as well as additional MIDI data files.

MIDI IMPLEMENTATION CHART

Function		Transmitted	Recognized	Remark
Basic	Default	1-16	1-16	
Channel	Changed	-	-	
	Default	yes	3	
Mode	Message	yes	3-4 (m=1)	Recognize as m=1 even if m != 1
	Altered			
Note	True	yes	0-127	
Number	Voice	yes	0-127	
Velocity	note ON	yes	yes	
	note OFF	yes	no	
After	Keys	yes	no	
Touch	Channels	yes	yes	
Pitch Bender		yes	yes	
	6	yes	yes	data entry
	100	yes	yes	RPCL, RPCH
	98,99	yes	yes	NRPCL,NRPCH
	0	yes	yes	bank select
Control	64,66,67	yes	yes	hold, sostenuto, soft pedals
Change	1	yes	yes	modulation
	5	yes	yes	portamento value
	65	yes	yes	portamento yes/no
	7,10,11	yes	yes	track volume, pan, expression
	80,81	yes	yes	reverb program, chorus program
	91,93	yes	yes	reverb send, chorus send levels
	120	yes	yes	all sounds off
	123	yes	yes	all notes off
	121	yes	yes	reset all controllers
	126	yes	yes	track mono mode on
	127	yes	yes	track poly mode on
Program				
Change	True number	yes	0-127	1-128 program number
System Exclusive				
System	:Song pos	yes	no	
	:Song sel	yes	no	
Common	:tune	yes	no	
System	:Clock	yes	no	
Real Time	:Commands	yes	no	
Aux	:Local ON/OFF	yes	no	
Messages	:All notes OFF	yes	yes (123-125)	
	:Active sense	yes	yes	
	:System reset	yes	yes	

Notes:
Mode 1: OMNI ON, POLY Mode 2: OMNI ON, MONO
Mode 3: OMNI OFF, POLY Mode 4: OMNI OFF, MONO
Midi controls 5 and 65 (portamento time and portamento on/off) are effective only if channel is in mono mode.

GENERAL MIDI SOUND SET (MIDI Program Numbers 1 - 128) (all channels except 10):

Prog#	Instrument Name	Prog#	Instrument Name	Prog#	Instrument Name
1	Acoustic Grand Piano	44	Contrabass	87	Lead 7 (fifths)
2	Bright Acoustic Piano	45	Tremolo Strings	88	Lead 8 (bass + lead)
3	Electric Grand Piano	46	Pizzicato Strings	89	Pad 1 (new age)
4	Honky-tonk Piano	47	Orchestral Harp	90	Pad 2 (warm)
5	Electric Piano 1	48	Timpani	91	Pad 3 (polysynth)
6	Electric Piano 2	49	String Ensemble 1	92	Pad 4 (choir)
7	Harpsichord	50	String Ensemble 2	93	Pad 5 (bowed)
8	Clavi	51	SynthStrings 1	94	Pad 6 (metallic)
9	Celesta	52	SynthStrings 2	95	Pad 7 (halo)
10	Glockenspiel	53	Choir Aahs	96	Pad 8 (sweep)
11	Music Box	54	Voice Oohs	97	FX 1 (rain)
12	Vibraphone	55	Synth Voice	98	FX 2 (soundtrack)
13	Marimba	56	Orchestra Hit	99	FX 3 (crystal)
14	Xylophone	57	Trumpet	100	FX 4 (atmosphere)
15	Tubular Bells	58	Trombone	101	FX 5 (brightness)
16	Dulcimer	59	Tuba	102	FX 6 (goblins)
17	Drawbar Organ	60	Muted Trumpet	103	FX 7 (echoes)
18	Percussive Organ	61	French Horn	104	FX 8 (sci-fi)
19	Rock Organ	62	Brass Section	105	Sitar
20	Church Organ	63	SynthBrass 1	106	Banjo
21	Reed Organ	64	SynthBrass 2	107	Shamisen
22	Accordion	65	Soprano Sax	108	Koto
23	Harmonica	66	Alto Sax	109	Kalimba
24	Tango Accordion	67	Tenor Sax	110	Bag pipe
25	Acoustic Guitar (nylon)	68	Baritone Sax	111	Fiddle
26	Acoustic Guitar (steel)	69	Oboe	112	Shanai
27	Electric Guitar (jazz)	70	English Horn	113	Tinkle Bell
28	Electric Guitar (clean)	71	Bassoon	114	Agogo
29	Electric Guitar (muted)	72	Clarinet	115	Steel Drums
30	Overdriven Guitar	73	Piccolo	116	Woodblock
31	Distortion Guitar	74	Flute	117	Taiko Drum
32	Guitar harmonics	75	Recorder	118	Melodic Tom
33	Acoustic Bass	76	Pan Flute	119	Synth Drum
34	Electric Bass (finger)	77	Blown Bottle	120	Reverse Cymbal
35	Electric Bass (pick)	78	Shakuhachi	121	Guitar Fret Noise
36	Fretless Bass	79	Whistle	122	Breath Noise
37	Slap Bass 1	80	Ocarina	123	Seashore
38	Slap Bass 2	81	Lead 1 (square)	124	Bird Tweet
39	Synth Bass 1	82	Lead 2 (sawtooth)	125	Telephone Ring
40	Synth Bass 2	83	Lead 3 (calliope)	126	Helicopter
41	Violin	84	Lead 4 (chiff)	127	Applause
42	Viola	85	Lead 5 (charang)	128	Gunshot
43	Cello	86	Lead 6 (voice)		

MT-32 COMPATIBILITY MODE (MIDI CHANNELS 1-9 11-16)
Variation (MIDI control 0) : 127

Note: This mode ensures only basic compatibility with MT32 by mapping GM instruments onto the MT32 sounds lists.

PC#	Instrument name	PC#	Instrument name	PC#	Instrument name	PC#	Instrument name
1	Piano 1	2	Piano 2	3	Piano 3	4	Detuned EP 1
5	E. Piano 1	6	E. Piano 2	7	Detuned EP2	8	Honky-Tonk Piano
9	Organ 1	10	Organ 2	11	Organ 3	12	Detuned Or. 1
13	Church Organ 2	14	Church Organ	15	Church Org.	16	Accordion Fr.
17	Harpsichord	18	Coupled Hps.	19	Coupled Hps.	20	Clav.
21	Clav.	22	Clav.	23	Celesta	24	Celesta
25	Synth Brass 1	26	Synth Brass 2	27	Synth Brass 3	28	Synth Brass 4
29	Synth Bass 1	30	Synth Bass 2	31	Synth Bass 3	32	Synth Bass 4
33	Fantasia	34	Syn Calliope	35	Choir Aahs	36	Bowed Glass
37	Soundtrack	38	Atmosphere	39	Crystal	40	Bag Pipe
41	Tinkle Bell	42	Ice Rain	43	Oboe	44	Pan Flute
45	Saw Wave	46	Charang	47	Tubular Bells	48	Square Wave
49	Strings	50	Tremolo Str.	51	Slow Strings	52	Pizzicato Str.
53	Violin	54	Viola	55	Cello	56	Cello
57	Contrabass	58	Harp	59	Harp	60	Nylon-str. Gt.
61	Steel-Str. Gt.	62	Chorus Gt.	63	Funk Gt.	64	Sitar
65	Acoustic Bs.	66	Fingered Bs.	67	Picked Bs.	68	Fretless Bs.
69	Slap Bs. 1	70	Slap Bs. 2	71	Fretless Bs.	72	Fretless Bs.
73	Flute	74	Flute	75	Piccolo	76	Piccolo
77	Recorder	78	Pan Flute	79	Soprano Sax	80	Alto Sax
81	Tenor Sax	82	Baritone Sax	83	Clarinet	84	Clarinet
85	Oboe	86	English Horn	87	Bassoon	88	Harmonica
89	Trumpet	90	Muted Trumpet	91	Trombone	92	Trombone
93	French Horn	94	French Horn	95	Tuba	96	Brass
97	Brass 2	98	Vibraphone	99	Vibraphone	100	Kalimba
101	Tinkle Bell	102	Glockenspiel	103	Tubular-Bell	104	Xylophone
105	Marimba	106	Koto	107	Taisho Koto	108	Shakuhachi
109	Whistle	110	Whistle	111	Bottle Blow	112	Pan Flute
113	Timpani	114	Melo Tom	115	Concert BD	116	Synth Drum
117	Melo Tom	118	Taiko	119	Taiko	120	Reverse Cym.
121	Castanets	122	Tinkle Bell	123	Orchestra Hit	124	Telephone
125	Bird	126	Helicopter	127	Bowed Glass	128	Ice Rain

DRUM SET TABLE (MIDI CHANNEL 10)

	Prog 1,33: STANDARD SET	Prog 9: ROOM SET	Prog 17: POWER SET	Prog 25: ELEC. SET	Prog 26: TR-808 SET	Prog 41: BRUSH SET	Prog 49: ORCHESTRA SET
27 - D#1	High Q						Closed Hi Hat
28 - E1	Slap						Pedal Hi-Hat
29 - F1	Scratch Push						Open Hi-Hat
30 - F#1	Scratch Pull						Ride Cymbal
31 - G1	Sticks						
32 - G#1	Square Click						
33 - A1	Metronome Click						
34 - A#1	Metronome Bell						
35 - B1	Bass Drum 2 (acoust)						Concert BD2
36 - C2	Bass Drum 1 (Rock)		Power Kick	Elec BD	808 Bass Drum		Concert BD1
37 - C#2	Side Stick				808 Rim Shot		
38 - D2	Snare Drum 1		Gated Snare	Elec SD	808 Snare Drum	Brush Tap	Concert SD
39 - D#2	Hand Clap					Brush Slap	Castanets
40 - E2	Snare Drum 2			Gate Snare		Brush Swirl	Concert SD
41 - F2	Low Floor Tom	Room Low Tom2	Room Low Tom2	Elec Low Tom2	808 Low Tom2		Timpani F
42 - F#2	Closed Hi Hat [EXC1]				808CHH [EXC1]		Timpani F#
43 - G2	High Floor Tom	Room Low Tom1	Room Low Tom1	Elec Low Tom1	808 Low Tom2		Timpani G
44 - G#2	Pedal Hi-Hat [EXC1]				808 CHH [EXC1]		Timpani G#
45 - A2	Low Tom	Room Mid Tom2	Room Mid Tom2	Elec Mid Tom2	808 Mid Tom2		Timpani A
46 - A#2	Open Hi-Hat [EXC1]				808 OHH [EXC1]		Timpani A#
47 - B2	Low-Mid Tom	Room Mid Tom1	Room Mid Tom1	Elec Mid Tom1	808 Mid Tom1		Timpani B
48 - C3	Hi Mid Tom	Room Hi Tom2	Room Hi Tom2	Elec Hi Tom2	808Hi Tom2		Timpani C
49 - C#3	Crash Cymbal 1				808 Cymbal		Timpani C#
50 - D3	High Tom	Room Hi Tom1	Room Hi Tom1	Elec Hi Tom1	808 Hi Tom1		Timpani D
51 - D#3	Ride Cymbal 1						Timpani D#
52 - E3	Chinese Cymbal			Reverse Cymbal			Timpani E
53 - F3	Ride Bell						Timpani F
54 - F#3	Tambourine						
55 - G3	Splash Cymbal						

DRUM SET TABLE (cont.)

	Prog 1,33: STANDARD SET	Prog 9: ROOM SET	Prog 17: POWER SET	Prog 25: ELEC. SET	Prog 26: TR-808 SET	Prog 41: BRUSH SET	Prog 49: ORCHESTRA SET
56 - G#3	Cowbell				808 Cowbell		
57 - A3	Crash Cymbal 2						Concert Cymbal 2
58 - A#3	Vibraslap						
59 - B3	Ride Cymbal 2						Concert Cymbal 1
60 - C4	Hi Bongo						
61 - C#4	Low Bongo						
62 - D4	Mute Hi Conga				808 High Conga		
63 - D#4	Open Hi Conga				808 Mid Conga		
64 - E4	Low Conga				808 Low Conga		
65 - F4	High Timbale						
66 - F#4	Low Timbale						
67 - G4	High Agogo						
68 - G#4	Low Agogo						
69 - A4	Cabasa						
70 - A#4	Maracas				808 Maracas		
71 - B4	Short Whistle [EXC2]						
72 - C5	Long Whistle [EXC2]						
73 - C#5	Short Guiro [EXC3]						
74 - D5	Long Guiro [EXC3]						
75 - D#5	Claves				808 Claves		
76 - E5	Hi Wood Block						
77 - F5	Low Wood Block						
78 - F#5	Mute Cuica [EXC4]						
79 - G5	Open Cuica [EXC4]						
80 - G#5	Mute Triangle [EXC5]						
81 - A5	Open Triangle [EXC5]						
82 - A#5	Shaker						
83 - B5	Jingle Bell						
84 - C6	Belltree						
85 - C#6	Castanets						
86 - D6	Mute Surdo [EXC6]						
87 - D#6	Open Surdo [EXC6]						
88 - E6							Applause

Notes: Blank: Same sound as "Standard Set"
[EXC]: Sounds with same EXC number are mutually exclusive

SOUND VARIATIONS (all channels except 10)

PROG #	CAPITAL (PAGE=0)	VARIATION FOR PAGE=8	VARIATION FOR PAGE=16
5	Electric Piano 1	Detuned E. Piano 1	
6	Electric Piano 2	Detuned E. Piano 2	
7	Harpsichord	Coupled Harpsichord	
15	Tubular Bells	Church Bells	
17	Drawbar Organ	Drawbar Tremolo Organ	
18	Percussive Organ	Tremolo Perc Organ	
20	Church Organ	Church Organ 2	
22	Accordion	Italian Accordion	
25	Acoustic Guitar (Nylon)	Ukulele	Spanish Guitar (1)
26	Acoustic Guitar (Steel)	12 Strings Guitar	Mandolin
27	Electric Guitar (Jazz)	Hawaiian Guitar	
28	Electric Guitar (Clean)	Chorus Guitar	Rock Guitar
29	Electric Guitar (Muted)	Funk Guitar	
31	Distortion Guitar	Feedback Guitar	
32	Guitar Harmonics	Guitar Mic. Feed-back	
39	Synth Bass 1	Synth Bass 3	
40	Synth Bass 2	Synth Bass 4	
49	String Ensemble 1	Orchestra	
51	Synth Strings 1	Synth Strings 3	
62	Brass Section	Brass Section 2	
63	Synth Brass 1	Synth Brass 3	
64	Synth Brass 2	Synth Brass 4	
67	Tenor Sax	Night Sax (1)	
81	Lead 1 (Square)	Sine	
108	Koto	Taisho Koto	
116	Woodblock	Castanets	
117	Taiko Drum	Concert Bass Drum	
118	Melodic Tom	Melodic Tom 2	
119	Synth Drum	808 Tom	

Notes: (1) Additional sounds
-Spanish Guitar: another type of acoustic guitar, very good for solos
-Rock Guitar: 60's type electric guitar
-Night Sax: soft blown tenor sax, for slow melodies

LIST OF SOUNDS REQUIRING TWO VOICES/NOTE

Capital (Variation 0): 4, 22, 24, 52, 61, 63, 64, 77, 81 to 89, 91, 93, 94, 95, 97 to 102, 104, 124, 127.
Variation #8: 5, 6, 7, 17, 18, 20, 22, 26, 28, 31, 40, 49, 51, 62, 63, 108.

SFX SET
(MIDI Channel 10, Program #57)

MIDI Note #	Prog 57: SFX SET
39 - D#2	High Q
40 - E2	Slap
41 - F2	Scratch Push
42 - F#2	Scratch Pull
43 - G2	Sticks
44 - G#2	Square Click
45 - A2	Metronome Click
46 - A#2	Metronome Bell
47 - B2	Guitar Slide
48 - C3	Guitar Cut Noise (down)
49 - C#3	Guitar Cut Noise (up)
50 - D3	Double Bass Slap
51 - D#3	Key Click
52 - E3	Laughing
53 - F3	Screaming
54 - F#3	Punch
55 - G3	Heart Beat
56 - G#3	Footsteps 1
57 - A3	Footsteps 2
58 - A#3	Applause
59 - B3	Door Creaking
60 - C4	Door Closing
61 - C#4	Scratch

MIDI Note #	Prog 57: SFX SET
62 - D4	Wind Chime
63 - D#4	Car Engine Start
64 - E4	Car Breaking
65 - F4	Car Pass
66 - F#4	Car Crash
67 - G4	Police Siren
68 - G#4	Train
69 - A4	Jet Take-off
70 - A#4	Helicopter
71 - B4	Starship
72 - C5	Gun Shot
73 - C#5	Machinegun
74 - D5	Lasergun
75 - D#5	Explosion
76 - E5	Dog
77 - F5	Horse Gallop
78 - F#5	Birds
79 - G5	Rain
80 - G#5	Thunder
81 - A5	Wind
82 - A#5	Sea Shore
83 - B5	Stream
84 - C6	Bubble

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SFX VARIATIONS
(all channels except 10)

PROG #	PAGE 0	PAGE 1	PAGE 2	PAGE 3	PAGE 4	PAGE 5	PAGE 6	PAGE 7	PAGE 8	PAGE 9
121	Guitar Fret Noise	Guitar Cut Noise	Double Bass Slap							
123	Seashore	Rain	Thunder	Wind	Stream	Bubble				
124	Bird Tweet	Dog	Horse Gallop							
125	Teleph. Ring	Teleph. Ring2	Door Creaking	Door Closing	Scratch	Wind-chime				
126	Heli-copter	Car Engine Start	Car Braking	Car Pass	Car Crash	Police Siren	Train	Jet Takeoff	Starship	Burst Noise
127	Applause	Laughing	Scream-ing	Punch	Heart Beat	Footstep				
128	Gunshot	Machine Gun	Lasergun	Explosion						

Note : To select a variation, first send PAGE number (Controller #0) then send program change number.

CM-64/MT-32 SET
(MIDI Channel 10, Program #128)

MIDI Note #	Prog 128: CM-64/MT-32 SET
35 - B1	Bass Drum 2 (Acoustic)
36 - C2	Bass Drum 1 (Rock)
37 - C#2	Side Stick
38 - D2	Snare Drum 1
39 - D#2	Hand Clap
40 - E2	Snare Drum 2
41 - F2	Low Floor Tom
42 - F#2	Closed Hi Hat [EXC1]
43 - G2	High Floor Tom
44 - G#2	Pedal Hi-Hat [EXC1]
45 - A2	Low Tom
46 - A#2	Open Hi-Hat [EXC1]
47 - B2	Low-Mid Tom
48 - C3	Hi-Mid Tom
49 - C#3	Crash Cymbal
50 - D3	High Tom
51 - D#3	Ride Cymbal 1
52 - E3	-
53 - F3	-
54 - F#3	Tambourine
55 - G3	-
56 - G#3	Cowbell
57 - A3	-
58 - A#3	-
59 - B3	-
60 - C4	Hi Bongo
61 - C#4	Low Bongo
62 - D4	Mute Hi Conga
63 - D#4	Open Hi Conga
64 - E4	Low Conga
65 - F4	High Timbale
66 - F#4	Low Timbale
67 - G4	High Agogo
68 - G#4	Low Agogo
69 - A4	Cabasa
70 - A#4	Maracas
71 - B4	Short Whistle
72 - C5	Long Whistle
73 - C#5	Short Guiro
74 - D5	-
75 - D#5	Claves
76 - E5	Laughing
77 - F5	Screaming
78 - F#5	Punch
79 - G5	Heartbeat
80 - G#5	Footsteps 1
81 - A5	Footsteps 2
82 - A#5	Applause
83 - B5	Door Creaking
84 - C6	Door Closing
85 - C#6	Scratch
86 - D6	Windchime
87 - D#6	Car Engine Start
88 - E6	Car Breaking
89 - F6	Car Pass
90 - F#6	Car Crash
91 - G6	Police Siren
92 - G#6	Train
93 - A6	Jet Take-off
94 - A#6	Helicopter
95 - B6	Starship
96 - C7	Gun Shot
97 - C#7	Machinegun
98 - D7	Lasergun
99 - D#7	Explosion
100 - E7	Dog
101 - F7	Horse
102 - F#7	Birds
103 - G7	Rain
104 - G#7	Thunder
105 - A7	Wind
106 - A#7	Sea Shore
107 - B7	Stream
108 - C8	Bubble

Notes: [EXC]: Sounds with same EXC number are mutually exclusive
: MT-32 percussion map

SYSTEM EXCLUSIVE MESSAGES

EXCLUSIVE DATA FORMAT : F0H 00H 20H 00H 00H 00H COMMAND <DATA> CHECKSUM F7H

Exclusive status
Dream MMA code
Device id
Model id

COMMAND = 00H - DOWN-LOAD OF INSTRUMENT SOUND

Down-loaded sound is selected on track by sending Control channel # 0 value 64 decimal, then program change 0.

COMMAND = 12 - GS COMPATIBILITY MODE

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In this case
<DATA> = addressMSB I address I addressLSBI <GS_DATA>

AddressGS_Data (H)ParameterDescriptionDefault value (H)
<REVERB> 40 01 3000-07REVERB TYPE00 : Room104 01 : Room2 02 : Room3 03 : Hall1 04 : Hall2 05 : Plate 06 : Delay 07 : Panning Delay
note : Reverb type can also be set with Control # 80
40 01 3800-7FREVERB LEVEL40
<CHORUS> 40 01 3800-07CHORUS TYPE00 : Chorus 102 01 : Chorus 2 02 : Chorus 3 03 : Chorus 4 04 : Feedback Chorus 05 : Flanger 06 : Short Delay 07 : Short delay with feed-back
note : Chorus type can also be set with Control # 81

AddressGS Data(H)ParameterDescriptionDefault value (H)
<MIDI CHANNEL TO PART ASSIGN, n is part> Part numbering : Part 1 (default MIDI channel = 1)n=1 . . Part 9 (default MIDI channel = 9)n=9 Part 10 (default MIDI channel = 10)n=0 Part 11 (default MIDI channel = 11)n=A . . Part 16 (default MIDI channel = 16)n=F Part OFFn=10 40 1n 0200-10Rx CHANNEL00(1) OF(16) 10(OFF)same as the Part#
<PART TO RHYTHM ALLOCATION> 40 1n 1500-02Rhythm assign00 (sound part)00 for n<>0 01, 02 (rhythm part)01 for n=0 (part 10)
<SCALE TUNING, n is part, no effect on rhythm part> 40 1n 4000-7F (12)SCALE TUNE-64 +63 (cent)40, 40, ..., 40 (12 values)
note: 40 1n 40 followed by 12 values (one value for each semi-tone, starting with C)
<MIDI VELOCITY CONTROL> 40 1n 1A00-7FVelocity depth (velocity slope)40 40 1n 1B00-7FVelocity offset40
<MODULATION PITCH DEPTH> 40 2x 0300-7FMOD WHEEL RATE (common to all tracks)3C 40 2n 0400-11MOD WHEEL DEPTH0A

RPN - Registered Parameter Number

RPN #0 = pitch bend sensitivity
#1 = fine tuning
#2 = coarse tuning

NRPN - Non Registered Parameter Number

NRPN	MSB	LSB
	01H	08H:Vibrate rate (-50,0,+50) [0 = 40H]
	01H	09H:Vibrate depth (-50,0,+50)
	01H	0AH:Vibrate delay (-50,0,+50)
	01H	20H:TVF cutoff frequency (-50,0,+16)
	01H	21H:TVF resonance (-50,0,+50)
	01H	63H:Environment attack time (-50,0,+50)
	01H	64H:Environment decay time (-50,0,+50)
	01H	66H:Environment release time (-50,0,+50)
	18H	rrH:Pitch coarse of drum instrument note rr (-64,0,+63 semitones)
	1AH	rrH:Level of drum instrument note rr (0,+127)
	1CH	rrH:Pan of drum instrument (-64,0,+63)
	1DH	rrH:Reverb send level of drum instrument (0,+127)
	1EH	rrH:Chorus send level of drum instrument (0,+127)

PC INTERFACE SPECIFICS

I/O base address can be jumper selected to 300H, 310H, 320H, 330H (default setting is 330H).

Interrupt can be jumper selected to 2/9, 3, 4, 5, 7 (default setting IRQ2/9).

After power-up or software reset, the board is in stand-alone mode:

Channels 1-9: instruments
Channel 10: drums
Channels 11-16: instruments
MIDI IN connected to synthesis and MIDI OUT
PC interrupt disconnected
No data transmitted to PC

In stand-alone mode, the only MPU-401 command processed are:

3FH: set UART mode
This command is acknowledged by the data OFEH on data port

In UART mode:

Interrupt (as selected by jumper) is connected to PC
Data received from MIDI IN is transmitted to PC
Data received from the PC is transmitted to synthesis and MIDI OUT

The only command recognized in UART mode is:

OFFH: reset (resume stand-alone mode)
this command is not acknowledged

Interrupts are generated only in UART mode, when a character is pending (board to PC).

Hardware handshake

Address base + 1

read: status
bit 7: DSR* (0 = data pending)
bit 6: DRR* (0 = ready to accept data or command)

write: command
command will be accepted only if DRR* = 0.
command write sets DRR* to 1.
DRR* will return to zero after completion by the board.

Address base + 0

read: data (valid when DSR* = 0)
data read will set DSR* to 1

write: data (ready for write when DRR* returns to zero when the board finishes processing the data.

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• Notes •

CS8401A, CS8402A AES/EBU & S/PDIF Transmitters

The CS8401A & CS8402A accept digital audio in many standard formats and generate an AES/EBU or S/PDIF compatible data stream. The CS8401A is software programmable for mode and for channel status and user data. The CS8402A is pin programmable.

CS8411, CS8412 AES/EBU and S/PDIF Receivers

The CS8411 and CS8412 digital audio receivers accept AES/EBU or S/PDIF signals and generate digital audio in many standard formats. A low jitter PLL recovers a clean clock for system use. The CS8411 is software readable for channel status and user data. The CS8412 is pin programmable

CS8425 A-LAN - Audio Local Area Network Transceiver

The CS8425 is an S/PDIF transceiver with on-chip low jitter PLL. A ring of CS8425 devices forms an Audio Local Area Network, where user data bits may be used for system messages between nodes. Intended for automotive applications, the device finds use wherever audio and some additional low bandwidth information needs to be communicated between multiple devices.

CONTENTS

Semiconductor Corporation

CS8401A CS8402A

Digital Audio Interface Transmitter

Features

- Monolithic Digital Audio Interface Transmitter
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver
- Configurable Buffer Memory (CS8401A)
- Transparent Mode Allows Direct Connection of CS8402A and CS8412 or CS8401A and CS8411A

General Description

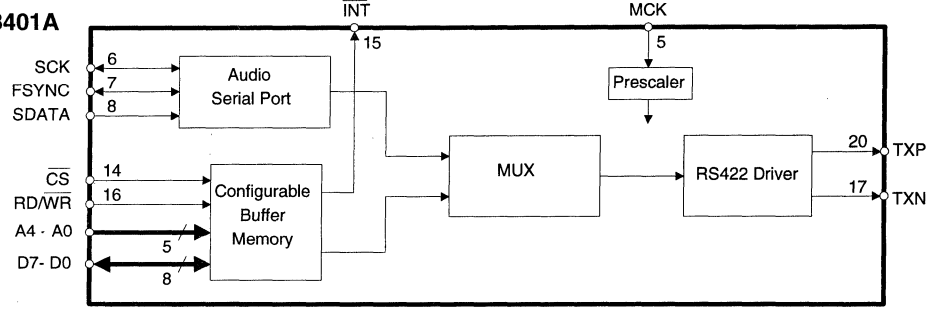
The CS8401/2A are monolithic CMOS devices which encode and transmit audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8401/2A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8401A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

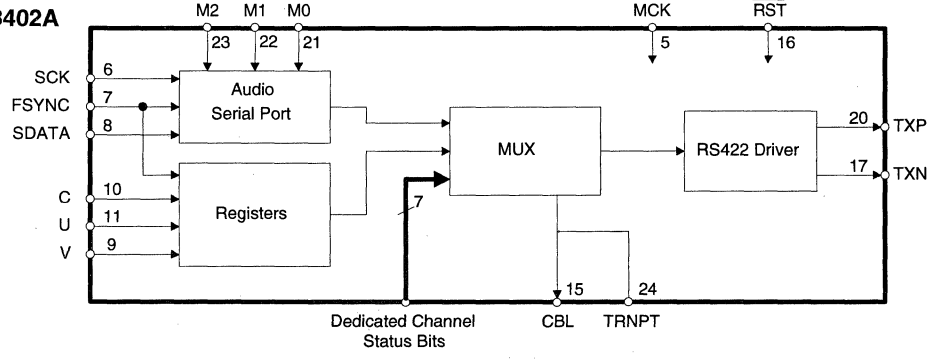
The CS8402A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

6

CS8401A



CS8402A



ABSOLUTE MAXIMUM RATINGS (GND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supply		VD+		6.0	V
Input Current, Any Pin Except Supply	Note 1	I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VD+	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND = 0V; all voltages with respect to ground)

Parameter			Symbol	Min	Typ	Max	Units
DC Voltage			VD+	4.5	5.0	5.5	V
Supply Current		Note 2	I_{DD}		1.5	5	mA
Ambient Operating Temperature:	CS8401/2A-CP or -CS	Note 3	T_A	0	25	70	°C
	CS8401/2A-IP or -IS			-40		85	°C
Power Consumption		Note 2	P_D		7.5	25	mW

Notes: 2. Drivers open (unloaded). The majority of power is used in the load connected to the drivers.
3. The '-CP' and '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only. The '-IP' and '-IS' parts are tested over the full -40 to 85 °C temperature range.

DIGITAL CHARACTERISTICS

(T_A = 25 °C for suffixes 'CP' & 'CS', T_A = -40 to 85 °C for 'IP' & 'IS'; VD+ = 5V ± 10%)

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage			V_{IH}	2.0		V_{DD}+0.3	V
Low-Level Input Voltage			V_{IL}	-0.3		+0.8	V
High-Level Output Voltage	(I_O = 200µA)		V_{OH}	V_{DD}-1.0			V
Low-Level Output Voltage	(I_O = 3.2mA)		V_{OL}			0.4	V
Input Leakage Current			I_{in}		1.0	10	µA
Master Clock Frequency:	CS8401A	Note 4	MCK			22	MHz
	CS8402A	Note 4				7.1	MHz
Master Clock Duty Cycle	CS8401/2A			40		60	%

Notes: 4. MCK for the CS8401 must be 128, 192, 256, or 384× the input word rate based on M0 and M1 in control register 2. MCK for the CS8402A must be 128× the input word rate, except in Transparent Mode where MCK is 256x the input word rate.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS - RS422 DRIVERS

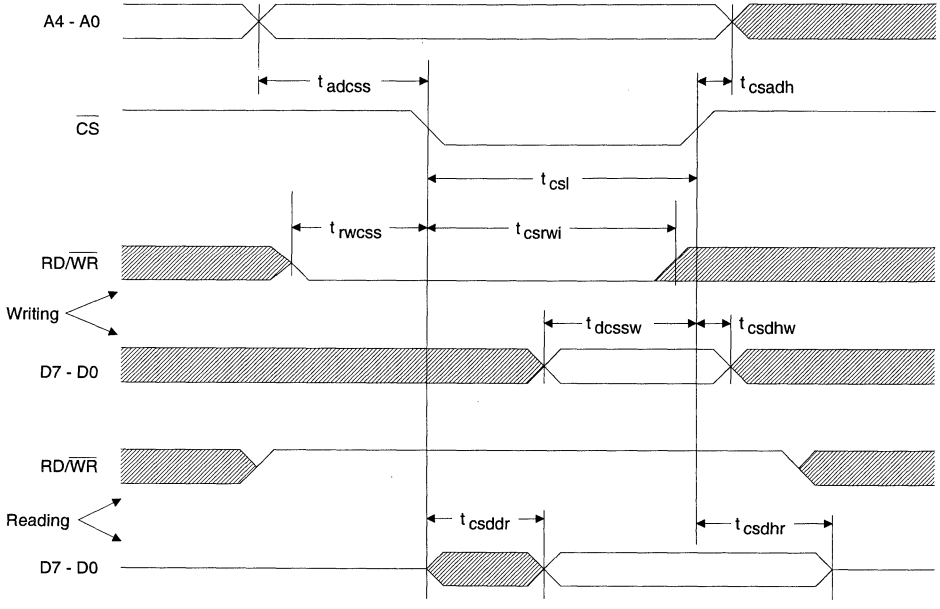
(TXP, TXN pins only; VD+ = 5V ±10%)

Parameter		Symbol	Min	Typ	Max	Units
Output High Voltage	I_{OH} = -30 mA	V_{OH}	VD+- 0.7	VD+ - 0.4		V
Output Low Voltage	I_{OL} = 30 mA	V_{OL}		0.4	0.7	V

SWITCHING CHARACTERISTICS - CS8401A PARALLEL PORT

(T_A = 25 °C for suffixes '-CP' and '-CS'; T_A = -40 to 85 °C for suffixes '-IP' and '-IS')

Parameter		Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{CS}$ low		t_{adcss}	13.5			ns
$\overline{CS}$ high to ADDRESS invalid		t_{csadh}	0			ns
RD/$\overline{WR}$ valid to $\overline{CS}$ low		t_{rwcss}	10			ns
$\overline{CS}$ low to RD/$\overline{WR}$ invalid		t_{csrwi}	35			ns
$\overline{CS}$ low		t_{csl}	35			ns
DATA valid to $\overline{CS}$ rising	RD/$\overline{WR}$ low (writing)	t_{dcssw}	32			ns
$\overline{CS}$ high to DATA invalid	RD/$\overline{WR}$ low (writing)	t_{csdhw}	0			ns
$\overline{CS}$ falling to DATA valid	RD/$\overline{WR}$ high (reading)	t_{csddr}			35	ns
$\overline{CS}$ rising to DATA Hi-Z	RD/$\overline{WR}$ high (reading)	t_{csdhr}	5			ns



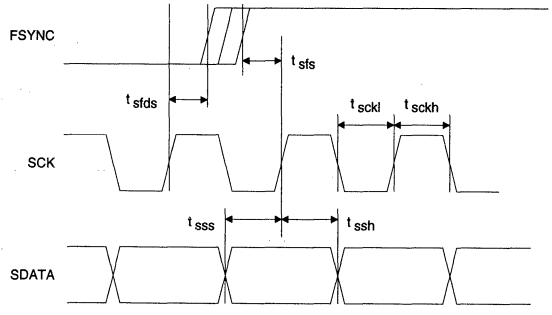
CS8401A Parallel Port Timing

SWITCHING CHARACTERISTICS - SERIAL PORTS

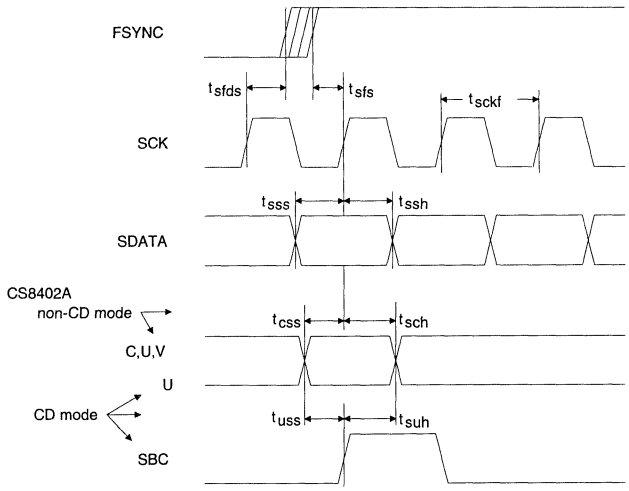
(T_A = 25 °C for suffixes '-CP' and '-CS'; T_A = -40 to 85 °C for suffixes '-IP' and '-IS';
Inputs: Logic 0 = GND, logic 1 = VD+; C_L = 20 pF)

Parameter			Symbol	Min	Typ	Max	Units
SCK Frequency	Master Mode	Notes 5,6	t_{sckf}		IWRx64		Hz
	Slave Mode	Note 6				12.5	MHz
SCK Pulse Width Low	Slave Mode	Note 6	t_{sckl}	25			ns
SCK Pulse Width High	Slave Mode	Note 6	t_{sckh}	25			ns
SCK rising to FSYNC edge delay		Notes 6,7	t_{sfds}	20			ns
SCK rising to FSYNC edge setup		Notes 6,7	t_{sfs}	20			ns
SDATA valid to SCK rising setup		Note 7	t_{sss}	20			ns
SCK rising to SDATA hold time		Note 7	t_{ssh}	20			ns
C, U, V valid to SCK rising setup	CS8402A non-CD Mode	Notes, 7,8	t_{css}	0			ns
SCK rising to C, U, V hold time	CS8402A non-CD mode	Notes 7, 8	t_{scs}	50			ns
U valid to SBC rising setup	CS8402A, CD mode	Note 8	t_{uss}	0			ns
SBC rising to U hold time	CS8402A, CD mode	Note 8	t_{suh}	80			ns
$\overline{RST}$ Pulse Width	CS8402A			150			ns

Notes:
5. The input word rate, IWR, refers to the frequency at which stereo audio input samples are input to the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample.
6. Master mode is defined as SCK and FSYNC being outputs. In Slave mode they are inputs. In the CS8401A, control reg. 3 bit 1, MSTR, selects master. In the CS8402A, only format 0 is master.
7. The table above assumes data is output on the falling edge and latched on the rising edge. In both parts the edge is selectable. The table is defined for the CS8401A with control reg. 3 bit 0, SCED, set to one, and for the CS8402A in formats 4 through 7. For the other formats, the table and figure edges must be reversed (ie. "rising" to "falling" and vice versa).
8. The diagrams show SBC rising coincident with the first rising edge of SCK after FSYNC transitions. This is true for all modes except FSF0 & 1 both equal 1 in the CS8401A, and format 4 in the CS8402A. In these modes SBC is delayed one full SCK period.



Serial Input Timing - Slave Mode



Serial Input Timing - Master Mode & C, U, V Port

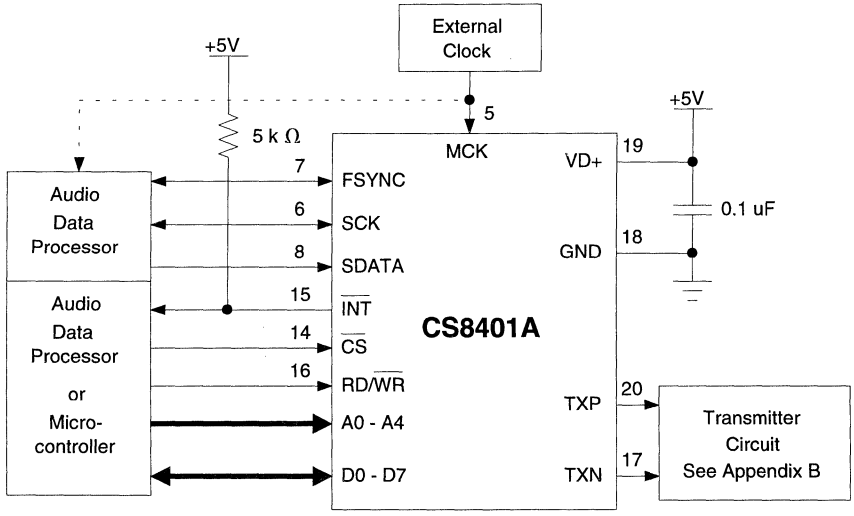


Figure 1. CS8401A Typical Connection Diagram

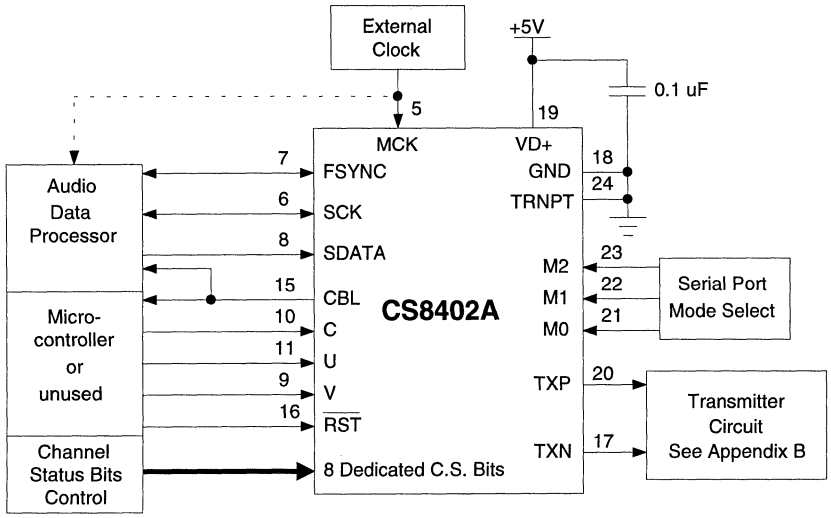


Figure 2. CS8402A Professional & Consumer Modes Typical Connection Diagram

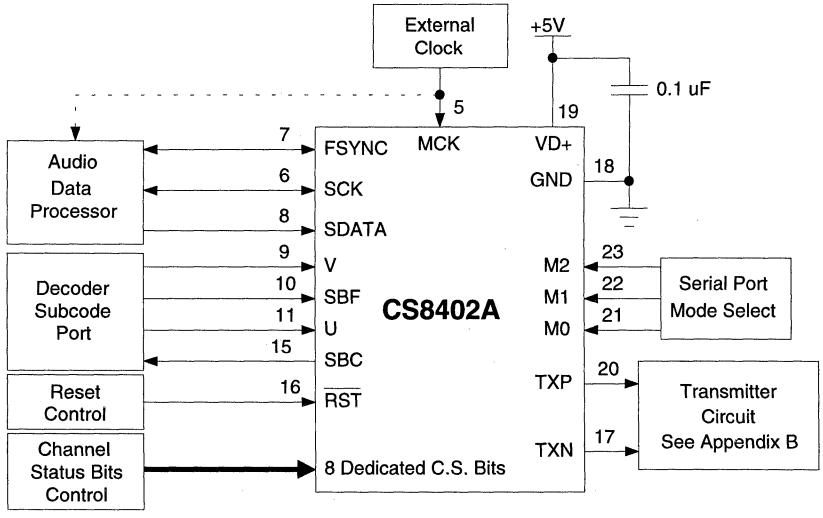


Figure 3. Consumer CD Submode Typical Connection Diagram

GENERAL DESCRIPTION

The CS8401A/2A are monolithic CMOS circuits that encode and transmit audio and digital data according to the AES/EBU, IEC 958 (S/PDIF), and EIAJ CP-340 interface standards. Both chips accept audio and control data separately; multiplex and biphase-mark encode the data internally; and drive it, directly or through a transformer, to a transmission line. The CS8401A is fully software programmable through a parallel port and contains buffer memory for control data, while the CS8402A has dedicated pins for the most important control bits and a serial input port for the C, U, and V bits.

Familiarity with the AES/EBU and IEC 958 specifications are assumed throughout this data sheet. Many terms such as channel status, user data, auxiliary data, professional mode, etc. are not defined. The Application Note, Overview of AES/EBU Digital Audio Interface Data Structures, provides an overview of the AES/EBU and IEC 958 specifications and is included for clarity; however, it is not meant to be a complete reference, and the complete standards should be obtained from the Audio Engineering Society or ANSI for the AES/EBU document, and the International Electrotechnical Commission for the IEC document.

Line Drivers

The RS422 line drivers for both the CS8401A and CS8402A are low skew, low impedance, differential outputs capable of driving 110 Ω transmission lines with a 4 volt peak-to-peak signal when configured as shown in Appendix A. To prevent possible short circuits, both drivers are set to ground when no master clock (MCK) is provided. They can also be disabled by resetting the device ($\overline{RST}$ = low). Appendix A contains more information on the line drivers. A 0.1 µF capacitor, with short leads, should be placed as close as possible to the VD+ and GND pins.

CS8401A DESCRIPTION

The CS8401A accepts 16- to 24-bit audio samples through a configurable serial port, and channel status, user, and auxiliary data through an 8-bit parallel port. The parallel port allows access to 32 bytes of internal memory which is used to store control information and buffer channel status, user, and auxiliary data. This data is multiplexed with the audio data from the serial port, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver. A block diagram of the CS8401A is shown in Figure 4. In accordance with the professional definition of channel status, the CRCC code (C.S. byte 23) can be internally generated.

Parallel Port

The parallel port accesses one status register, three control registers, and 28 bytes of dual port buffer memory. The address bus, and RD/$\overline{WR}$ line must be valid when $\overline{CS}$ goes low. If RD/$\overline{WR}$ is low, the value on the data bus will be written into the buffer memory at the specified address. If RD/$\overline{WR}$ is high, the value in the buffer memory, at the specified address, is placed on the data bus. The detailed timing for reading and writing the CS8401A can be found in the Digital Switching Characteristics table. The memory space is allocated as shown in Figure 5. There are three defined buffer memory modes selectable by two bits in control register 2.

Status and Control Registers

Upon power up the CS8401A control registers contain all zeros. Therefore, the part is initially in reset and is muted. One's must be written to control register 2, bits $\overline{RST}$ and $\overline{MUTE}$, before the part will transmit data. *The remaining registers are not initialized on power-up and may contain random data.*

The first register, shown in Figure 6, is the status register in which only three bits are valid. The lower three bits contain flags indicating the position of the transmit pointer in the buffer memory. These flags

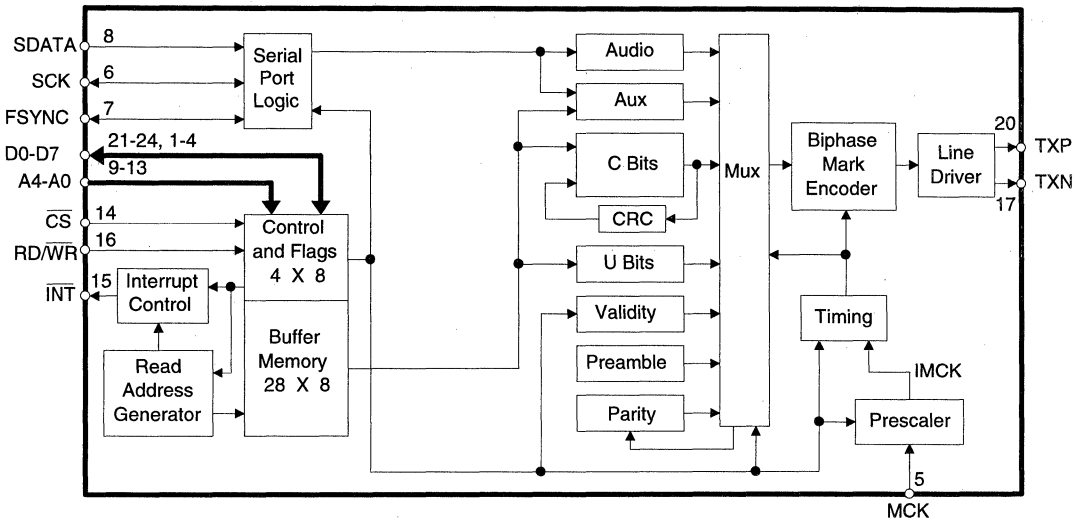


Figure 4. CS8401A Block Diagram

may be used to avoid contention between the transmit pointer reading the data and the user updating the buffer memory. Besides indicating the byte location being transmitted, the flags indicate the block of memory the part is currently addressing, thereby telling the user which block is free to be written to. Each flag has a corresponding mask bit (control register 1) which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. Flag 0 and flag 1 cause interrupts on both edges whereas flag 2 causes an interrupt only on the rising edge. Timing and further explanation of the flags can be found in the buffer memory section.

The two most significant bits of control register 1, BKST and TRNPT, are used for Transparent Mode operation of the CS8401A. Transparent Mode is used for those applications where it is useful to maintain frame alignment between the received and transmitted audio data signals. In Transparent Mode (TRNPT = "1") the MCK, FSYNC, SCK and SDATA inputs of the CS8401A can be connected to their corresponding outputs of the CS8411. In Transparent Mode, FSYNC synchronizes the transmitter and the receiver. The data delay through the CS8401A is set so that three frame delays occur from the input of the CS8411 to the output of the CS8401A. In Transparent Mode, 32 SCK's are required per subframe.

Channel status block alignment between the CS8411 and the CS8401A is accomplished by setting BKST high at the occurrence of the Flag 2 rising edge of the CS8411. If FSYNC is a left/right signal, BKST is sampled once per frame; if FSYNC is a word clock, BKST is sampled once per subframe. A low to high transition of BKST (based on two successive internal samples) resets the channel status block boundary to the beginning.

Control register 2, shown in Figure 8, contains various system level functions. The two most significant bits, M1 and M0, select the frequency at the MCK pin as shown in Table 1. As an example, if the audio sample frequency is 44.1 kHz and M0 and M1 are both zero, MCK would then be 128× the audio sample rate or 5.6448 MHz. The next bit (5) in control register 2, V, indicates the validity of the current audio sample. According to the

digital audio specifications, V = 0 signifies the audio signal is suitable for conversion to analog. B1 and B0 select one of three modes for the buffer memory. The different modes are shown in Figure 5 and the bit combinations in Table 2. More information on the different modes can be found in the *Buffer Memory* section. Bit 2, CRCE, is the channel status CRCC enable and should only be used in professional mode. When CRCE is high, the

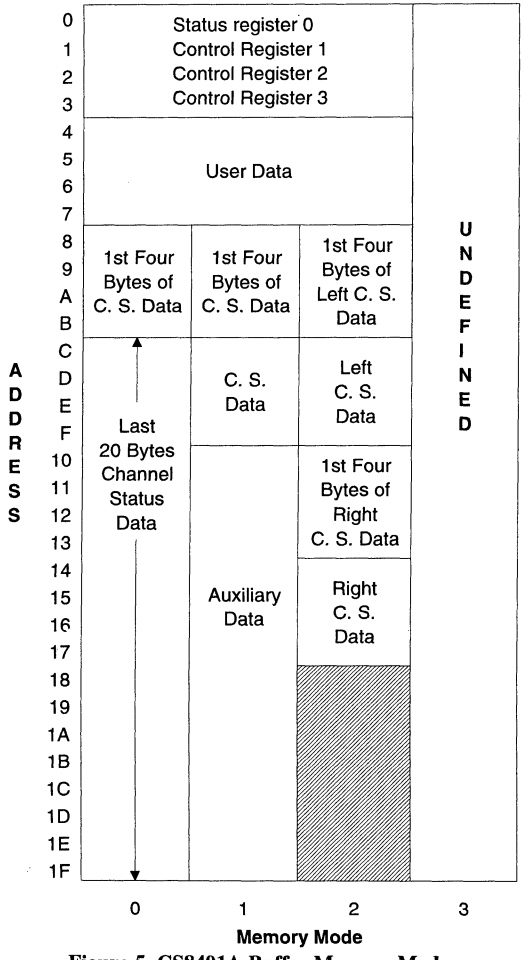
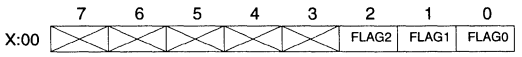
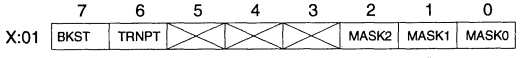


Figure 5. CS8401A Buffer Memory Modes



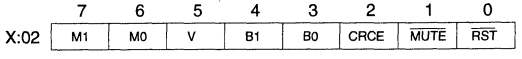
FLAG2: High for first four bytes of channel status
FLAG1: Memory mode dependent - See figure 11
FLAG0: High for last two bytes of user data.

Figure 6. Status Register



BKST: Causes realignment of data block when set to "1".
TRNPT: Selects Transparent Mode appropriately setting data delay through device
MASK2: Interrupt mask for FLAG2. A "1" enables the interrupt.
MASK1: Interrupt mask for FLAG1.
MASK0: Interrupt mask for FLAG0.

Figure 7. Control Register 1



M1: with M0, selects MCK frequency.
M0: with M1, selects MCK frequency.
V: Validity bit of current sample.
B1: with B0, selects the buffer memory mode.
B0: with B1, selects the buffer memory mode.
CRCE: Channel status CRC Enable. Professional mode only.
$\overline{\text{MUTE}}$: When clear, transmitted audio data is set to zero.
$\overline{\text{RST}}$: When clear, drivers are disabled, frame counters cleared.

Figure 8. Control Register 2

M1	M0	MCLK
0	0	128× Input Word Rate
0	1	192× Input Word Rate
1	0	256× Input Word Rate
1	1	384× Input Word Rate

Table 1. MCLK Frequencies

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 2. Buffer Memory Modes

channel status data cyclic redundancy check characters are generated independently for channels A and B and are transmitted at the end of the channel status block. When $\overline{\text{MUTE}}$ (bit 1) is low, the transmitted audio data is forced to zero. Both $\overline{\text{RST}}$ and $\overline{\text{MUTE}}$ are set to zero upon power up.

When $\overline{\text{RST}}$ is low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the rest of the CS8401A to the audio serial port, the transmit timing counters, which include the flags in the status register, are not enabled after $\overline{\text{RST}}$ is set high until eight and one half SCK periods after the active edge (first edge after reset is exited) of FSYNC.

When FSYNC is configured as a left/right signal (FSF1 = 1), the counters and flags are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and Channel B is right as per the digital audio interface specs.

Control register 3 contains format information for the serial audio input channel. The MSB is unused and the next three bits, SDF2-SDF0, select the format for the serial input data with respect to FSYNC. There are five valid combinations of these bits as shown in Figure 10. The next two bits, FSF1 and FSF0, select the format of FSYNC. Two

	7	6	5	4	3	2	1	0
X:03		SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

SDF2: with SDF0 & SDF1, select serial data format.
SDF1: with SDF0 & SDF2, select serial data format.
SDF0: with SDF1 & SDF2, select serial data format.
FSF1: with FSF0, select FSYNC format.
FSF0: with FSF1, select FSYNC format.
MSTR: When set, SCK and FSYNC are outputs.
SCED: When set, rising edge of SCK latches data.
When clear, falling edge of SCK latches data.

Figure 9. Control Register 3

of the formats delineate each channel's data and do not indicate the particular channel. The other two formats also indicate the specific channel. The formats are shown in Figure 10. Bit 1, MSTR, determines whether FSYNC and SCK are inputs, MSTR low, or outputs, MSTR high. Bit 0, serial clock edge select, SCED, selects the edge that audio data gets latched on. When SCED is low, the falling edge of SCK latches data in the chip and when SCED is high, the rising edge is used.

The multitude of combinations allow for a zero glue logic interface to almost all DSP's, encoder chips, and standard serial data formats.

Serial Port

The serial port is used to enter audio data and consists of three pins: SCK, SDATA, and FSYNC. The serial port is double buffered with SCK clocking in the data from SDATA, and FSYNC delineating audio samples and may define the particular channel, left or right.

Control register 3, shown in Figure 9, configures the serial port. All the various formats are illustrated in Figure 10. When FSF1 is low, FSYNC only delineates audio samples. When FSF1 is high, it delineates audio samples and specifies the channel. When FSF1 is low and the port is a master (MSTR = 1), FSYNC is a square wave output. When FSF1 is low and the port is a slave (input), FSYNC can be a square wave or a pulse provided the active edge, as defined in Figure 10, is properly positioned with respect to SDATA.

Bits 4, 5, and 6, SDF0-SDF2, define the format of SDATA and is also described in Figure 10. The five allowable formats are MSB first, MSB last, 16-bit LSB last, 18-bit LSB last, and 20-bit LSB last. The MSB first and MSB last formats accept any word length from 16 to 24 bits. The word length is controlled by providing trailing zeros in MSB first mode and leading zeros in

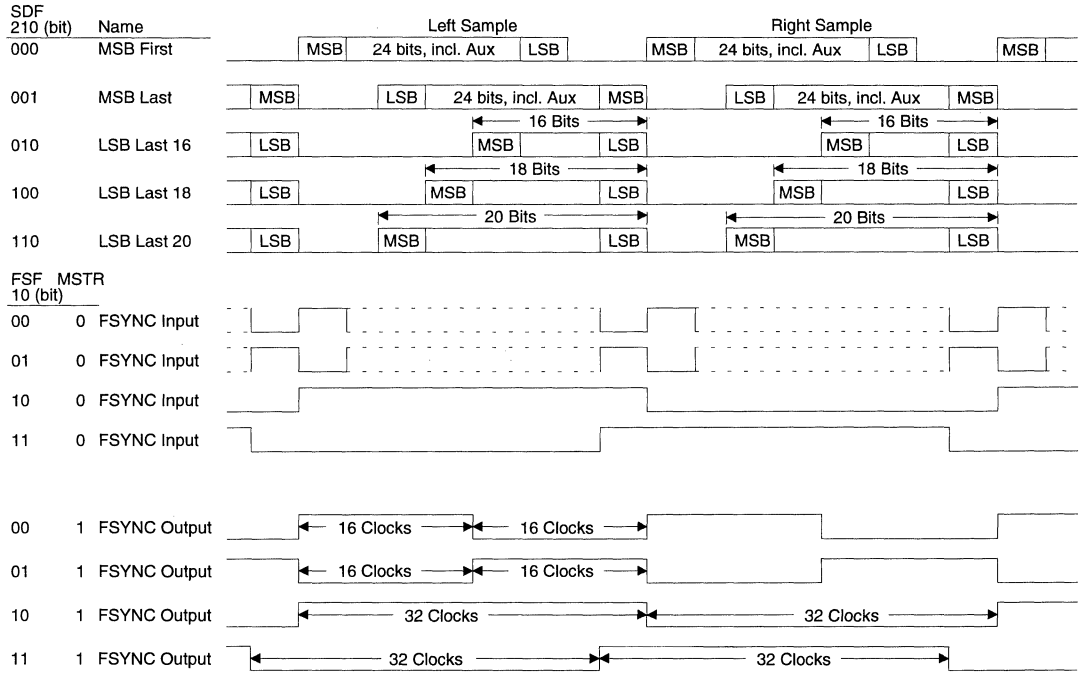


Figure 10. CS8401A Serial Port SDATA and FSYNC Timing

MSB last mode, or by restricting the number of SCK periods between samples to the sample word length. The 16-, 18-, and 20-bit LSB-last modes require at least 16, 18, or 20 SCK periods per sample respectively. As a master, 32 SCK periods are output per sample.

FSYNC must be derived from MCK via a DSP using the same clock or by external counters. If FSYNC moves (jitters) with respect to MCK by more than 4 MCK periods, the CS8401A may reset the channel status block and flags. Appendix C contains more information on the relationship of FSYNC and MCK.

Buffer Memory

In all buffer modes, the status register and control registers are located at addresses 0-3 respectively, and the user data is buffered in locations 4-7. The parallel port can access any location in the user data buffer at any time; however, care must be taken not to modify a location when that location is being read internally. This internal reading is done through the second port of the buffer and is done in a cyclic manner.

Reset initializes the internal pointer to 04H (Hex). Data is read from this location and stored in an 8-bit shift register which is shifted once per audio sample. (An audio sample is defined as a single channel, not a stereo pair.) The byte is transmitted LSB first, D0 being the first bit. After transmitting 8 samples, i.e. 8 user bits, the address pointer is incremented and the next byte of user data is loaded into the shift register. After transmitting all four bytes, 32 audio sam-

ples, the user read pointer is reset to 04H (Hex) and the cycle repeats.

Flag 0 in the status register monitors the position of the internal user data read pointer. When the first byte, location 04H, is read, flag 0 is set low and when the third byte, location 06H, is read, flag 0 is set high. If mask 0 in control register 1 is set, a transition of flag 0 will generate a low pulse on the interrupt pin. The value of flag 0 indicates which two bytes the part will read next, thereby indicating which two bytes are free to be updated.

Flag 1 is mode dependent, changing with buffer memory configuration, and is discussed in the individual buffer mode sections.

Flag 2 is set high when byte 0 of the channel status, address 08H, is read, and set low when byte 4, address 0BH, is read. Therefore, flag 2 high indicates the part is reading the first four bytes of channel status, and the last 20 bytes are free to update. If the interrupt mask bit for flag 2 is set, the rising edge will cause an interrupt indicating the beginning of a channel status block as shown in Figure 11. Although a falling edge

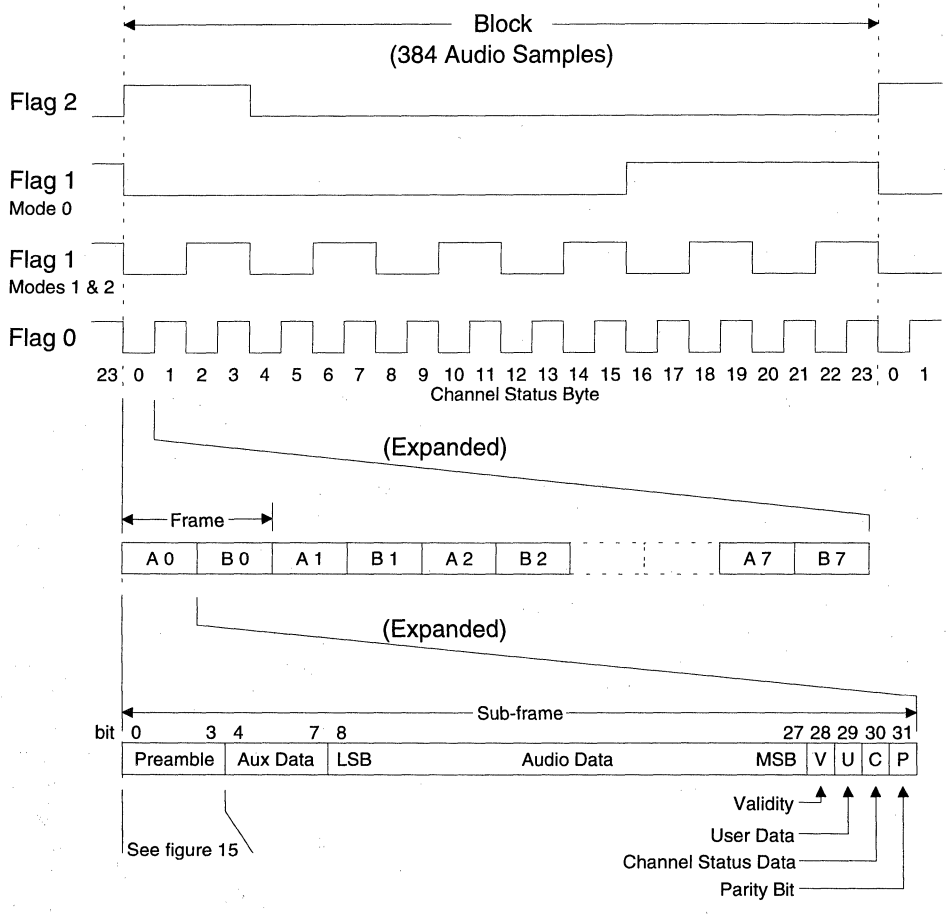


Figure 11. CS8401A Status Register Flag Timing

on flag 0 and flag 1 may cause an interrupt, the falling edge of flag 2 will not.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of channel status data and 384 audio samples. (This figure assumes the channel status bit is the same for the audio pair.) The lower portion of Figure 11 expands the first byte of channel status showing eight pairs of data with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits as per the AES/EBU specifications (see Appendix A). When transmitting stereo, channel A is left and channel B is right. The preamble at the bottom of Figure 11 is expanded in Figure 15 to show the exact timing between flags, the interrupt pin, and internal buffer-read timing.

Buffer Mode 0

In buffer mode 0, in addition to the user-data buffer previously discussed, one entire block of channel status data is buffered in 24 memory locations from address 08H to 1FH. This block will be transmitted in both channel A and channel B, one bit per frame. Like the user-data buffer, the parallel port can access any location in this buffer at any time. The transmitter section reads this buffer in a cyclic non-destructive manner and stores the byte in an 8-bit shift register that is shifted once per two transmitted audio samples (once per frame).

Flag 1 in the status register can be used to monitor the channel status buffer. In mode 0, flag 1 is set low when byte 0, location 08H, is read, and set high when byte 16, location 18H, is read. If mask 1 in control register 1 is set, a transition on flag 1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory read sequence for buffer mode 0 along with the flag timing. The arrows on the flags indicate an interrupt if the appropriate mask bit is set. Flag 0 can cause an interrupt on either edge, which is shown only in the expanded portion of the Figure for clarity. The expanded section also shows that the user buffer is reread when location 0AH of the channel status is read.

Buffer Mode 1

In buffer mode 1, eight bytes are allocated for channel status data and 16 bytes for auxiliary data as shown in Figure 5. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to

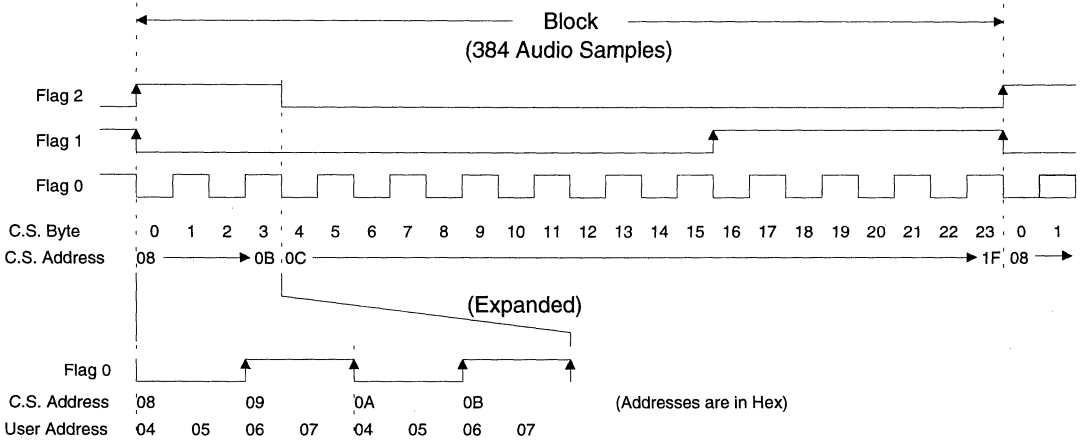


Figure 12. CS8401A Buffer Memory Read Sequence - MODE 0

mode 0, and are read once per channel status block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data.

Similar to mode 0, transmitted channel status data will be the same for channel A and channel B (one channel status bit per frame). Flag 1 and flag 2 can be used to monitor this buffer. Flag 1 is set low when byte 0 of channel status data, location 08H, is read and is toggled when every other byte is read. As shown in Figure 13, flag 2 is set high when byte 0, location 08H, is read and set low when byte 4, location 0CH, is read. Flag 2 determines whether the channel status pointer is reading the first four-byte section or the second four-byte section, while flag 1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is read in a cyclic manner similar to the data buffer; however, four auxiliary data bits are transmitted per audio sample (sub-frame). Since the auxiliary buffer must be read four times as often as the user data buffer and is four times as large, flag 0 can be used to monitor both.

Buffer Mode 2

In buffer mode 2, two 8-byte buffers are available for buffering both channel A and channel B channel status data independently. Both buffers are identical to the channel status buffer in mode 1 except that each channel can have unique channel status data. The two buffers are read simultaneously with locations 08H to 0FH transmitted in channel A and locations 10H to 17H transmitted in channel B. Figure 5 contains the buffer memory modes and Figure 14 illustrates the buffer read sequence for mode 2.

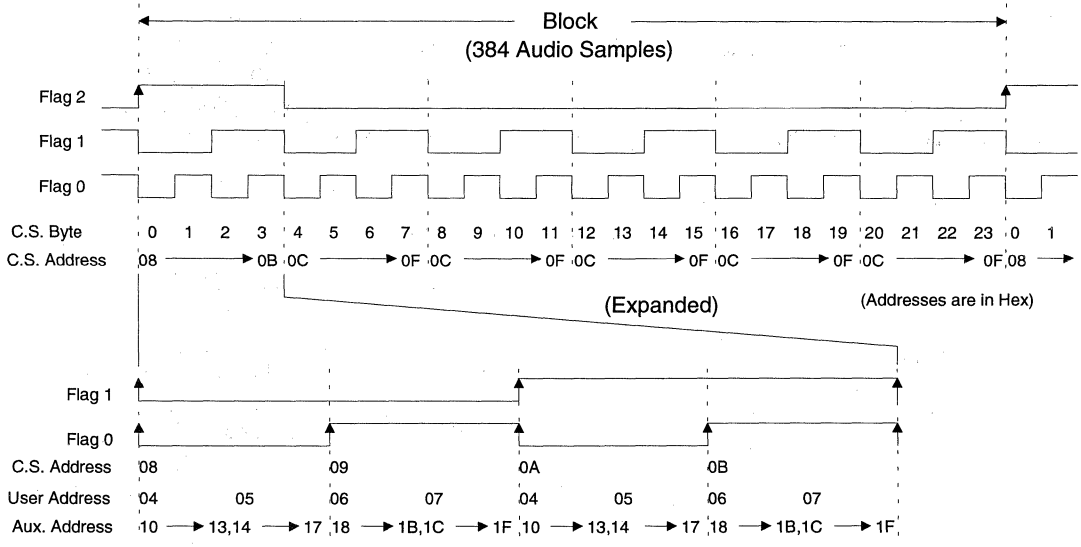


Figure 13. CS8401A Buffer Memory Read Sequence - MODE 1

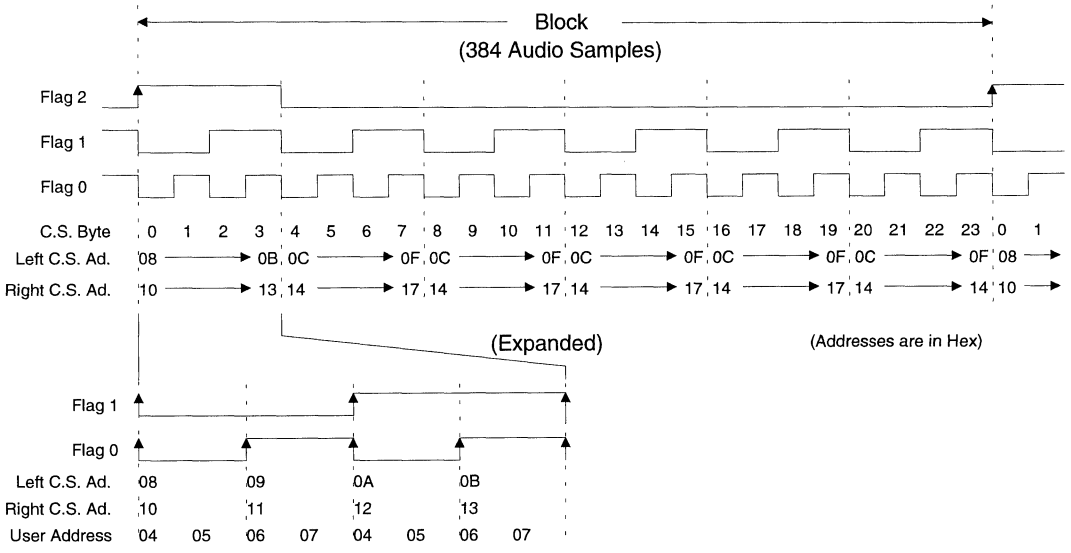


Figure 14. CS8401A Buffer Memory Read Sequence - MODE 2

6

Buffer-Read and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally writing to the buffer ram and the CS8401A internally reading bytes of ram for transmission may be averted by using the flag levels to avoid the section currently being addressed by the part. Interrupts occur at flag edges indicating the exact byte that the part is currently reading. Utilizing $\overline{INT}$ along with the flags, the byte currently being read by the part can be avoided allowing access to all other bytes instead of just a section. Figure 15 illustrates the timing between flags, $\overline{INT}$, and the internal reading of the buffer for transmission. The master clock IMCK is shown as 128×Fs. Other MCK frequencies are initially divided to obtain 128×Fs, defined as IMCK (internal MCK), which is then used for all internal timing, so the timing in Figure 15 is valid for all MCK frequencies. When the parity bit (P) is transmitted, a transition on a flag causes $\overline{INT}$ to go low if the appropriate mask bit is set. Concurrently, the part starts reading from the internal buffer. Writing to the buffer ram location being read by the part should be avoided while the internal "ram read" signal is high.

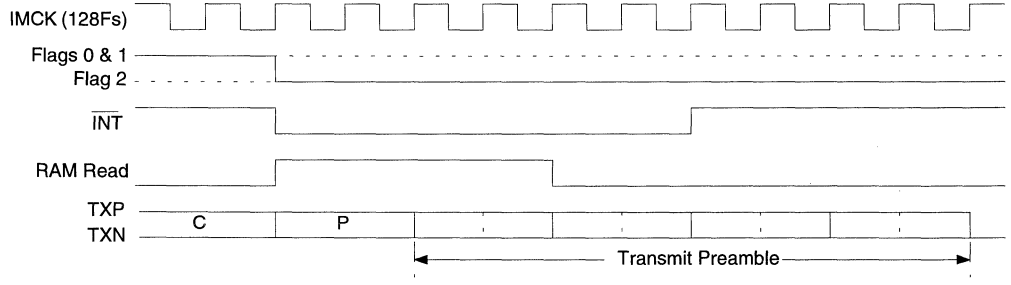
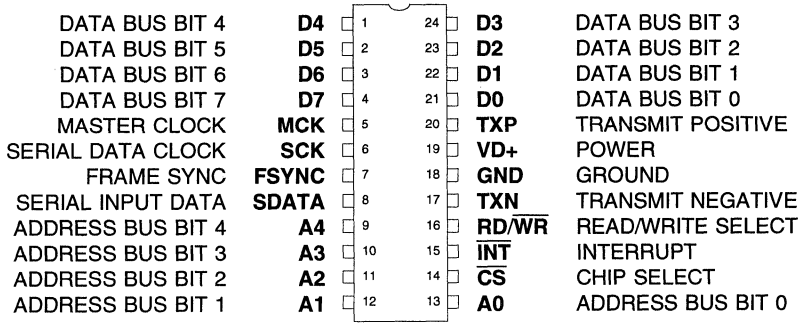


Figure 15. RAM/Buffer-Read and Interrupt Timing

PIN DESCRIPTIONS

CS8401A



Power Supply Connections

VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

GND - Ground, PIN 18.

Ground for the digital section.

Audio Input Interface

SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via control register 3) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 3.

SDATA - Serial Data, PIN 8.

Audio data serial input pin.

Parallel Interface

$\overline{CS}$ - Chip Select, PIN 14.

This input is active low and allows access to the 32 bytes of internal memory. The address bus and RD/WR must be valid while CS is low.

RD/WR - Read/Write, PIN 16.

If RD/WR is low when CS goes active (low), the data on the data bus is written to internal memory. If RD/WR is high when CS goes active, the data in the internal memory is placed on the data bus.

A4-A0 - Address Bus, PINS 9-13.

Parallel port address bus that selects the internal memory location to be read from or written to.

D0-D7 - Data Bus, PINS 21-24, 1-4.

Parallel port data bus used to check status, write control words, or write internal buffer memory.

INT - Interrupt, PIN 15.

Open drain output that can signal the state of the internal buffer memory. A 5kΩ resistor to VD+ is typically used to support logic gates. All bits affecting INT are maskable allowing total control over the interrupt mechanism.

Transmitter Interface

MCK - Master Clock, PIN 5.

Clock input which defines the transmit timing. It can be configured, via control register 2, for 128, 192, 256, or 384 times the sample rate.

TXP, TXN - Differential Line Drivers, PINS 20, 17.

RS422 compatible line drivers. Drivers are pulled low when part is in reset state.

CS8402A DESCRIPTION

The CS8402A accepts 16- to 24-bit audio samples through a serial port configured in one of seven formats; provides several pins dedicated to particular channel status bits; and allows all channel status, user, and validity bits to be serially input through port pins. This data is multiplexed, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver.

The CS8402A operates as a professional or consumer interface transmitter selectable by pin 2, $\overline{\text{PRO}}$. As a professional interface device, the dedicated channel status input pins are defined according to the professional standard, and the CRC code (C.S. byte 23) can be internally generated.

As a consumer device, the dedicated channel status input pins are defined according to the consumer standard. A submode provided under the consumer mode is compact disk, CD, mode. When transmitting data from a compact disk, the CD subcode port can accept CD subcode data, extract channel status information from it, and transmit it as user data.

The master clock, MCK, controls timing for the entire chip and must be 128×Fs. As an example, if stereo data is input to the CS8402A at 44.1 kHz, MCK input must be 128 times that or 5.6448 MHz.

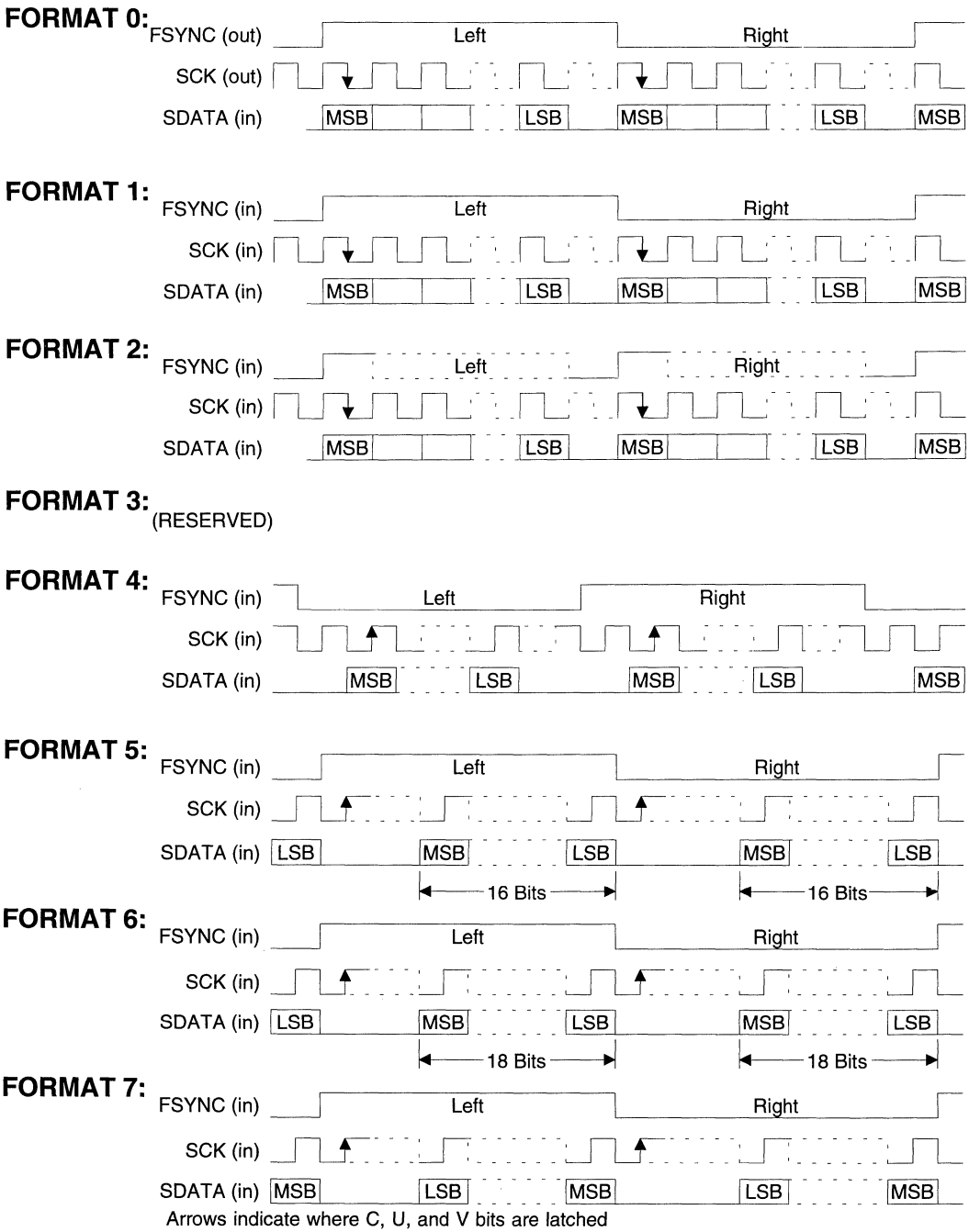
Audio Serial Port

The audio serial port is used to enter audio data and consist of three pins: SCK, SDATA, and FSYNC. SCK clocks in SDATA, which is double buffered, while FSYNC delineates the audio samples and may indicate the particular channel, left or right. To support many different interfaces, M2, M1, and M0 select one of seven different formats for the serial port. The coding is shown in Table 3 while the formats are shown in Figure 16. Format 0 and 1 are designed to interface with Crystal ADCs. Format 2 communicates with Motorola and TI DSPs. Format 3 is reserved. Format 4 is compatible with the I^2S standard. Formats 5 and 6 make the CS8402A look similar to existing 16- and 18-bit DACs, and interpolation filters. Format 7 is an MSB-last format and is conducive to serial arithmetic. SCK and FSYNC are outputs in Format 0 and inputs in all other formats. In Format 2, the rising edge of FSYNC delineates samples and the falling edge must occur a minimum of one bit period before or after the rising edge. In all formats except 2, FSYNC contains left/right information requiring both edges of FSYNC to delineate samples. Formats 5 and 6 require a minimum of 16- or 18-bit audio words respectively. In all formats other than 5 and 6, the CS8402A can accept any word length from 16 to 24 bits by adding leading zeros in format 7 and trailing zeros in the other formats, or by restricting the number of SCK periods between active edges of FSYNC to the sample word length.

FSYNC must be derived from MCK, either through a DSP using the same clock, or using counters. If FSYNC moves (jitters) with respect to MCK by four MCK periods, the internal counters and CBL may be reset. Appendix B contains more information on the relationship between FSYNC and MCK.

M2	M1	M0	Format
0	0	0	0 - FSYNC & SCK Output
0	0	1	1 - Left/Right, 16-24 Bits
0	1	0	2 - Word Sync, 16-24 Bits
0	1	1	3 - Reserved
1	0	0	4 - Left/Right, I^2S Compatible
1	0	1	5 - LSB Justified, 16 Bits
1	1	0	6 - LSB Justified, 18 Bits
1	1	1	7 - MSB Last, 16-24 Bits

Table 3. CS8402A Audio Port Modes



Arrows indicate where C, U, and V bits are latched

Figure 16. CS8402A Audio Serial Port Formats

C, U, V Serial Port

The serial input pins for channel status (C), user (U), and validity (V) are sampled during the first bit period after the active edge of FSYNC for all formats except Format 4, which is sampled during the second bit period (coincident with the MSB). In Figure 16, the arrows on SCK indicate when the C, U, and V bits are sampled. The C, U, and V bits are transmitted with the audio sample entered before the FSYNC edge that sampled it. The V bit, as defined in the audio standards, is set to zero to indicate the audio data is suitable for conversion to analog. Therefore, when the audio data is errorred, or the data is not audio, the V bit should be set high. The channel status serial input pin (C) is not available in consumer mode when the CD subcode port is enabled (FC1 = FC0 = high). Any channel status data entered through the channel status serial input (C) is logically OR'ed with the data entered through the dedicated pins or internally generated.

$\overline{RST}$ and CBL (TRNPT is low)

When $\overline{RST}$ goes low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the CS8402A to the audio serial port, the transmit timing counters, which include CBL, are not enabled after $\overline{RST}$ goes high until eight and one half SCK periods after the active edge (first edge after reset is exited) of FSYNC. When FSYNC is configured as a left/right signal (all defined formats except 2), the counters and CBL are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and channel B is right as per the digital audio interface specs.

As shown in Figure 17, CBL, channel block start output, can assist in serially inputting the C, U and V bits as CBL goes high one bit period before the first bit of the preamble of the first sub-frame of the channel status block is trans-

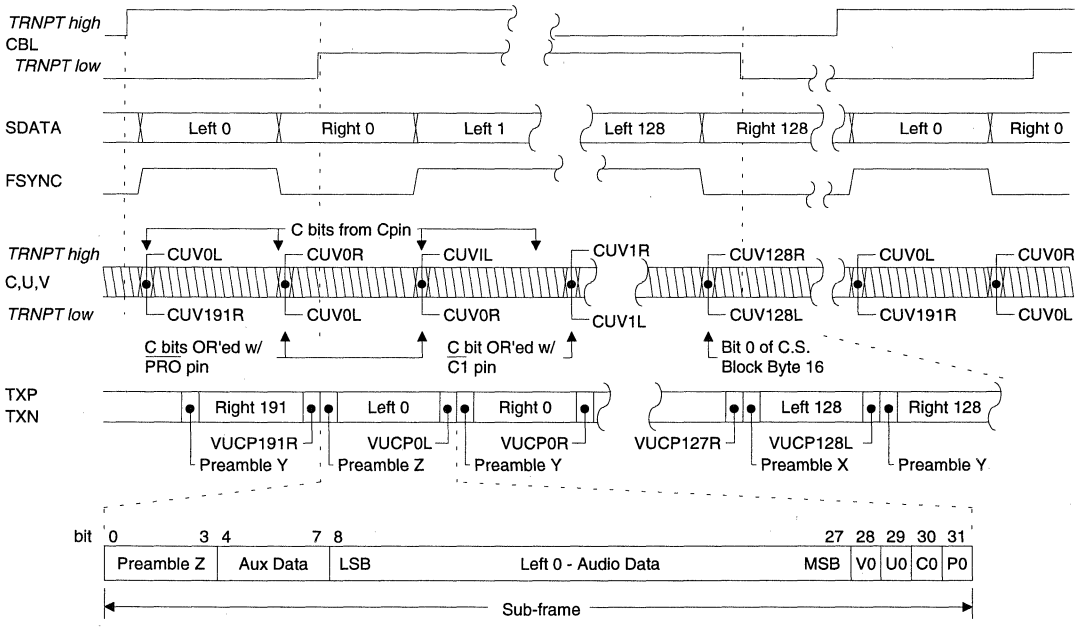


Figure 17. CBL and Transmitter Timing

mitted. This sub-frame contains channel status byte 0, bit 0. CBL returns low one bit period before the start of the frame that contains bit 0 of channel status byte 16. CBL is the exact inverse of flag 1 in mode 0 on the CS8401 (see Figure 11). CBL is not available when the CD subcode port is enabled.

Figure 17 illustrates timing for stereo data input on the audio port. Notice how CBL rises while the right channel data (Right 0) is input, but the previous left channel data (Left 0) is being transmitted as the first sub-frame of the channel status block (starting with preamble Z). The C, U, and V input ports only need to be valid for a short period after FSYNC changes. A sub-frame includes one audio sample while a frame includes a stereo pair. A channel status (C.S.) block contains 24 bytes of channel status and 384 audio samples (or 192 stereo pairs, or frames, of samples).

Figure 17 shows the CUV ports as having left and right bits (e.g. CUV0L, CUV0R). Since the C.S. block is defined as 192 bits, or one bit per frame, there are actually 2 C.S. blocks, one for channel A (left) and one for channel B (right). When inputting stereo audio data, both blocks normally contain the same information, so C0L and C0R from the input port pin are both channel status bit 0 of byte 0, which is defined as professional/consumer. These first two bits from the port, C0L and C0R, are logically OR'ed with the inverse of $\overline{PRO}$, since $\overline{PRO}$ is a dedicated channel status pin defined as C.S. bit 0. Also, if in professional mode, $\overline{C1}$, $\overline{C6}$, $\overline{C7}$ and $\overline{C9}$ are dedicated C.S. pins. The inverse of $\overline{C1}$ is logically OR'ed with channel status input port bits C1L and C1R. In similar fashion, $\overline{C6}$, $\overline{C7}$ and $\overline{C9}$ are OR'ed with their respective input bits. Also, the C bits in CUV128L and CUV128R are both channel status block bit 128, which is bit 0 of channel status byte 16.

Transparent Mode

In certain applications it is desirable to receive digital audio data with the CS8412 and retransmit it with the CS8402A. In this case, channel status, user and validity information must pass through unaltered. For studio environments, AES recommends that signal timing synchronization be maintained throughout the studio. Frame synchronization of digital audio signals input to and output from a piece of equipment must be within ±5%.

The transparent mode of the CS8402A is selected by setting TRNPT, pin 24, high. In this mode, the CBL pin becomes an input, allowing direct connection of the outputs of the CS8412 to the inputs of the CS8402A as shown in Figure 18. The transmitter and receiver are synchronized by the FSYNC signal. CBL specifies the start of a new channel status block boundary, allowing the transmit block structure to be slaved to the block structure of the receiver. In the transparent mode, C, U, and V are now transmitted with the current audio sample as shown in Figure 17 (TRNPT high), and the dedicated channel status pins are ignored. When in the transparent mode, the propagation delay of data through the CS8402A is set so that the total propagation delay from the receive inputs of the CS8412 to the transmit outputs of the CS8402A is three frames.

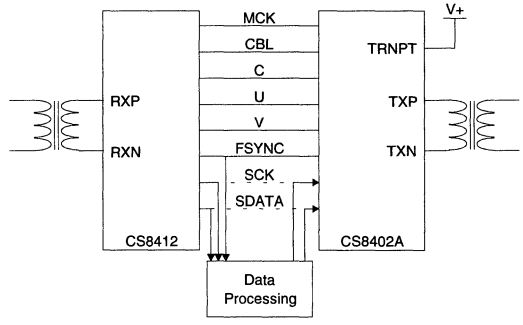


Figure 18. Transparent Mode Interface

When FSYNC is a word clock (Format 2), CBL is sampled when left C,U,V are sampled. When FSYNC is Left/Right, CBL is sampled when left C,U,V are sampled. The channel status block boundary is reset when CBL transitions from low to high (based on two successive samples of CBL). MCK for the CS8402A is normally expected to be 128 times the sample frequency, in the transparent mode MCK must be 256 Fs.

Professional Mode

Setting $\overline{PRO}$ low places the CS8402A in professional mode as shown in Figure 19. In professional mode, channel status bit 0 is transmitted as a one and bits 1, 2, 3, 4, 6, 7, and 9 can be controlled via dedicated pins. The pins are actually the inverse of the identified bit. For example, tying the $\overline{C1}$ pin low places a one in channel status bit 1. As shown in the Application Note, Overview of AES/EBU Digital Audio Interface Data Structures, C1 indicates audio/non-audio; C6 and C7 determine the sample frequency; and C9 allows the encoded channel mode to be stereophonic. EM1 and EM0 determine emphasis and encode C2, C3, C4 as shown in Table 4. The dedicated channel status pins are read at the appropriate time and are logically OR'ed with data input on the channel status port, C. In Transparent Mode, these dedicated channel status pins are ignored; and channel status bits are input at the C pin.

The channel status data cyclic redundancy check character (C.S. byte 23) is always generated independently for channels A and B and is transmitted at the end of the channel status block.

Data should not be input through the channel status port, C, during the CRCC byte time frame, since inputs on C are logically OR'ed with internally generated data.

Consumer Mode

Setting $\overline{PRO}$ high places the CS8402A in consumer mode which redefines the pins as shown in Figure 20. In consumer mode, channel status bit 0 is transmitted as a zero and channel status bits 2, 3, 8, 9, 15, 24, and 25 are controlled via dedicated pins. The pins are actually the inverse of the bit so if pin

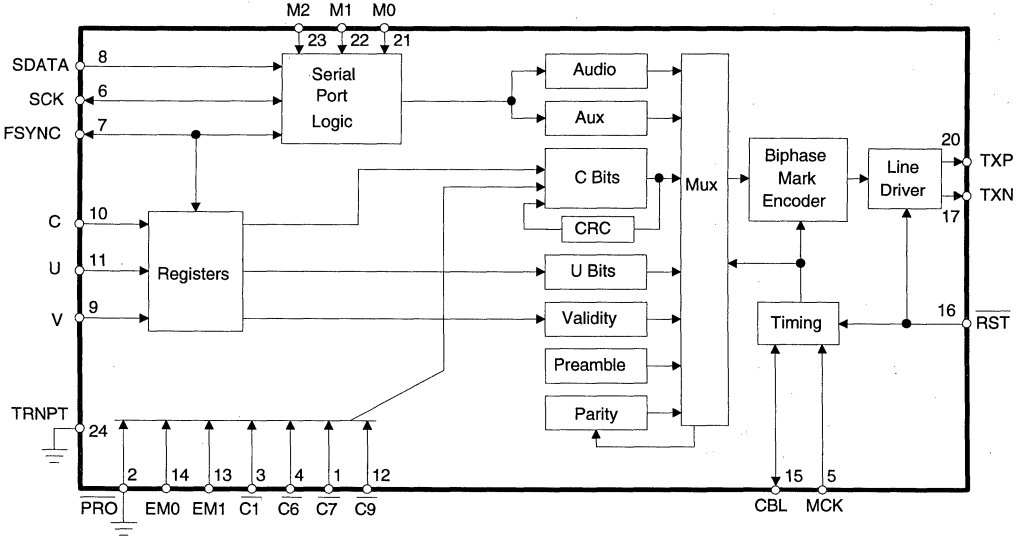


Figure 19. CS8402A Block Diagram - Professional Mode

$\overline{C2}$ is tied high, channel status bit 2 will be transmitted as a zero. Also, FC0 and FC1 are encoded versions of channel status bits 24 and 25, which define the sample frequency. When FC0 and FC1 are both high, the part is placed in a CD submode which activates the CD subcode port. This submode is described in detail in the next section. Table 5 describes the encoding of C24 and C25 through the FC1 and FC0 pins. According to AES/EBU standards, C2 is copy prohibit/permit, C3 specifies pre-emphasis, C8 and C9 define the category code, and C15 identifies the generation status of the transmitted material (i.e.. first generation, second generation).

Consumer - CD Submode

The consumer CD submode is invoked by placing the part in consumer mode ($\overline{PRO}$ = high) and setting both FC1 and FC0 high. This mode redefines some of the pins for a CD subcode port as shown in Figure 21. The CD subcode port pins, SBF and SBC, replace the C and CBL pins respectively. The user data input, U, becomes the CD subcode input. Figure 22 describes the timing for the CD subcode port. When SBF is low, SBC becomes active, clocking in the subcode bits. SBF goes high for one SCK period, one half SCK period after the active edge of FSYNC for all formats (except format 4, which will be one and a half SCK periods after the active edge of FSYNC). SBF high for more than 16 SBC periods indicates the start of a subcode block. The first, third, and fourth Q bits after the start of a subcode block become channel status bits 5, 2, and 3 respectively. Channel status bits are set by the dedicated pins; the category code is forced to CD.

EM1	EM0	C2	C3	C4
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

Table 4. Emphasis Encoding

FC1	FC0	C24	C25	Comments
0	0	0	0	44.1 kHz
0	1	0	1	48.0 kHz
1	0	1	1	32.0 kHz
1	1	0	0	44.1 kHz, CD Mode

Table 5. Sample Frequency Encoding

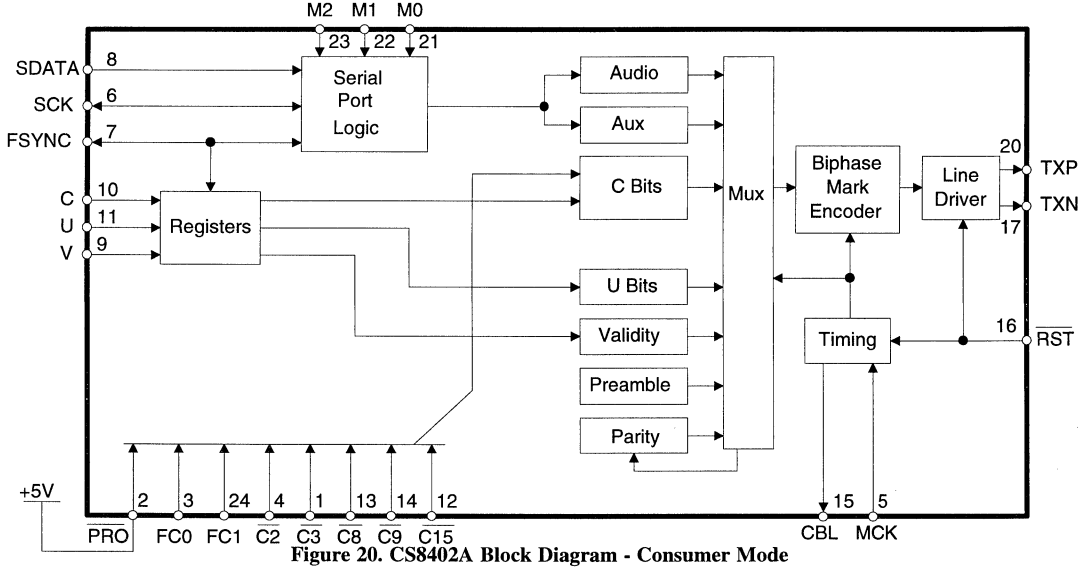


Figure 20. CS8402A Block Diagram - Consumer Mode

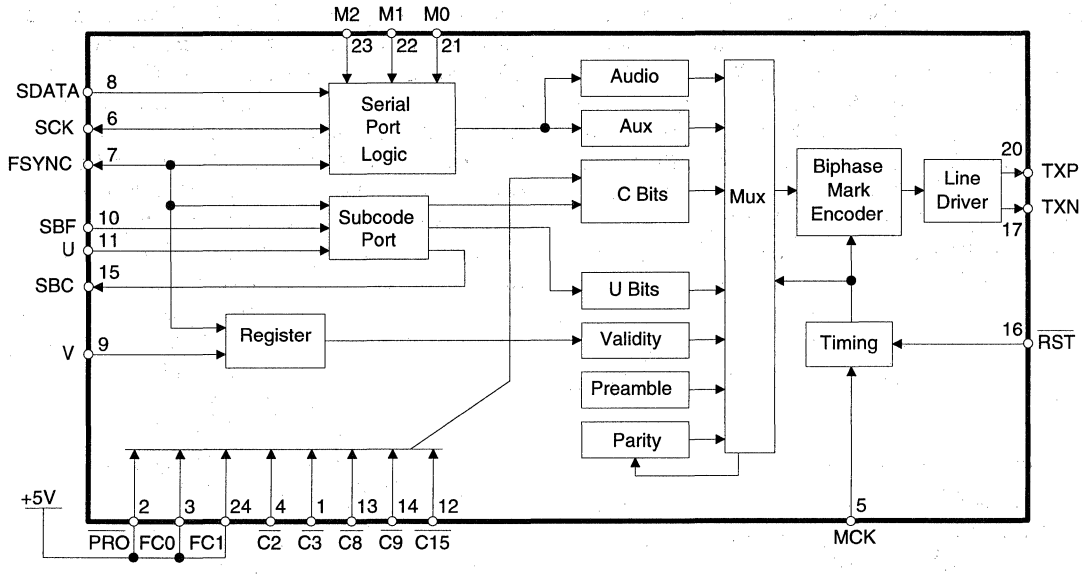


Figure 21. CS8402A Block Diagram - Consumer Mode, CD Submode

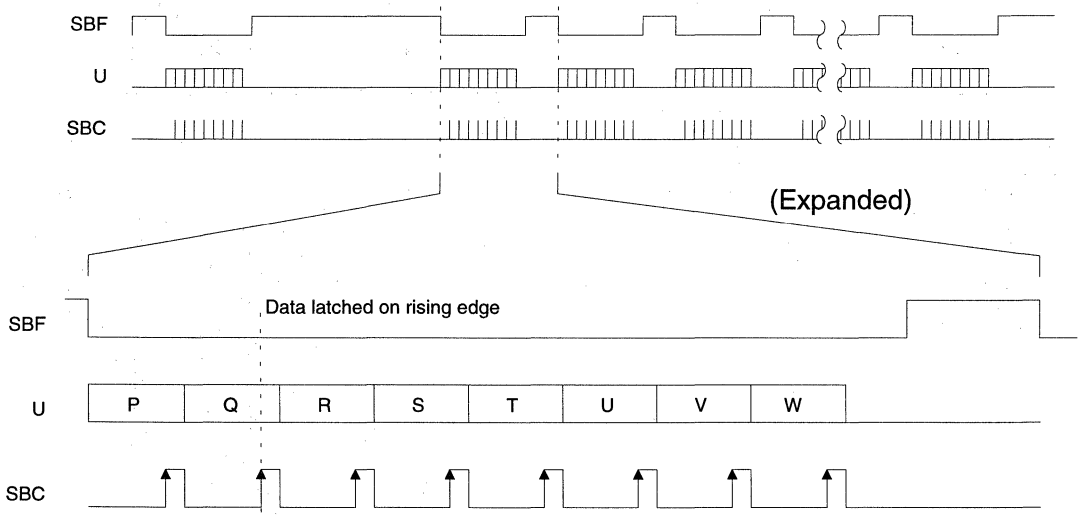
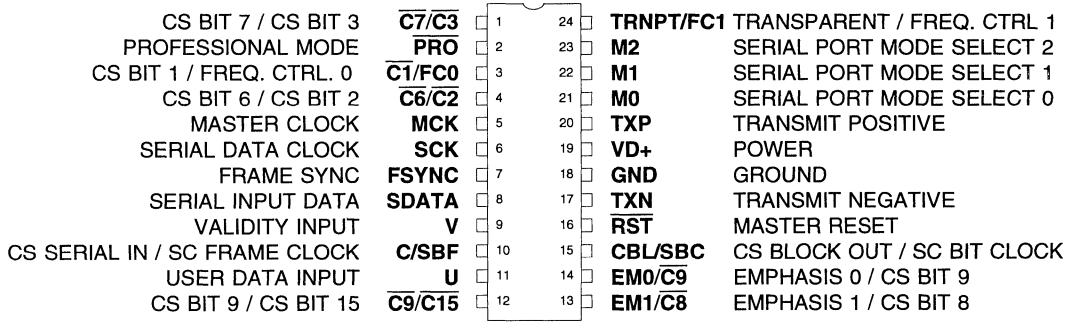


Figure 22. CD Subcode Port Timing

PIN DESCRIPTIONS

CS8402A



Power Supply Connections

VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

GND - Ground, PIN 18.

Ground for the digital section.

Audio Input Interface

SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via the M0, M1, and M2 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, and M2 pins.

SDATA - Serial Data, PIN 8.

Audio data serial input pin.

M0, M1, M2 - Serial Port Mode Select, PINS 21, 22, 23.

Selects the format of FSYNC and the sample edge of SCK with respect to SDATA.

Control Pins

$\overline{\text{RST}}$ - Master Reset, PIN 16.

When low, all internal counters are reset and the line drivers are disabled, pulling low.

V - Validity, PIN 9.

Validity bit serial input port. This bit is defined according to the digital audio standards wherein V = 0 signifies the audio signal is suitable for conversion to analog. V = 1 signifies the audio signal is not suitable for conversion to analog, i.e. invalid. V is sampled once per subframe

U - User Bit, PIN 11.

User bit serial input port is sampled once per subframe.

$\overline{\text{PRO}}$ - Professional/Consumer Select, PIN 2.

Selects between professional mode (PRO low) and consumer mode ($\overline{\text{PRO}}$ high). This pin defines the functionality of the next seven pins. PRO must be low for Transparent Mode, but will have no effect on the channel status bits.

C9/$\overline{\text{C15}}$ - Channel Status Bit 9 / Channel Status Bit 15, PIN 12.

In professional mode, C9 is the inverse of channel status bit 9 (bit 1 of byte 1). In consumer mode, C15 is the inverse of channel status bit 15 (bit 7 of byte 1). C9/C15 are ignored in Transparent Mode.

EM0/$\overline{\text{C9}}$ - Emphasis 0 / Channel Status Bit 9, PIN 14.

In professional mode, EM0 and EM1 encode channel status bits 2, 3, and 4. In consumer mode, C9 is the inverse of channel status bit 9 (bit 1 or byte 1). EMO/C9 are ignored in Transparent Mode.

EM1/$\overline{\text{C8}}$ - Emphasis 1 / Channel Status Bit 8, PIN 13.

In professional mode, EM0 and EM1 encode channel status bits 2, 3, and 4. In consumer mode, C8 is the inverse of channel status bit 8 (bit 0 of byte 1). EM1/C8 are ignored in Transparent Mode.

$\overline{\text{C7}}$/$\overline{\text{C3}}$ - Channel Status Bit 7 / Channel Status Bit 3, PIN 1.

In professional mode, C7 is the inverse of channel status bit 7. In consumer mode, $\overline{\text{C3}}$ is the inverse of channel status bit 3. C7/C3 are ignored in Transparent Mode.

$\overline{\text{C6}}$/$\overline{\text{C2}}$ - Channel Status Bit 6 / Channel Status Bit 2, PIN 4.

In professional mode, C6 is the inverse of channel status bit 6. In consumer mode, $\overline{\text{C2}}$ is the inverse of channel status bit 2. C6/C2 are ignored in Transparent Mode.

$\overline{\text{C1}}$/FC0 - Channel Status Bit 1 / Frequency Control 0, PIN 3.

In professional mode, C1 is the inverse of channel status bit 1. In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected. C1/FC0 are ignored in Transparent Mode.

TRNPT/FC1 - Transparent Mode / Frequency Control 1, PIN 24.

In professional mode, setting TRNPT low selects normal operation & CBL is an output. Setting TRNPT high, allows the CS8402A to be connected directly to a CS8412. In transparent mode, CBL is an input & MCK must be at 256 Fs.

In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25. When FC0 and FC1 are both high, CD mode is selected.

C/SBF - Channel Status Serial Input / Subcode Frame Clock, PIN 10.

In professional and consumer modes this pin is the channel status serial input port. In CD mode this pin inputs the CD subcode frame clock.

CBL/SBC - Channel Status Block Output / Subcode Bit Clock, PIN 15.

In professional and consumer modes, the channel status block output is high for the first 16 bytes of channel status. In CD mode, this pin outputs the subcode bit clock.

Transmitter Interface

MCK - Master Clock, PIN 5.

Clock input at 128× Fs the sample frequency which defines the transmit timing. In transparent mode, MCK must be 256× Fs.

TXP, TXN - Differential Line Drivers, PINS 20, 17.

RS422 compatible line drivers. Drivers are pulled to low when part is in reset state.

Appendix A: RS422 Driver Information

The RS422 drivers on the CS8401A and CS8402A are designed to drive both the professional and consumer interfaces. The AES/EBU specification for professional/broadcast use calls for a 110Ω source impedance and a balanced drive capability. Since the transmitter impedance is very low, a 110Ω resistor should be placed in series with one of the transmit pins. (A 110Ω resistor in parallel with the transformer would, with the receiver impedance of 110Ω, provide a 55Ω load to the part which is too low.) The specifications call for a balanced output drive of 2-7 volts peak-to-peak into a 110Ω load with no cable attached. Using the circuit in Figure A1, the output of the transformer is short-circuit protected, has the proper source impedance, and provides a 5 volt peak-to-peak signal into a 110Ω load. Lastly, the two output pins should be attached to an XLR connector with male pins and a female shell, and with pin 1 of the connector grounded.

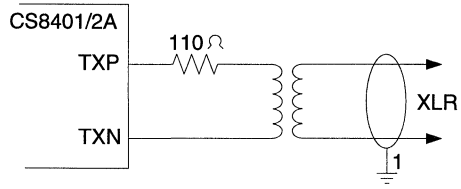


Figure A1. Professional Output Circuit

In the case of consumer use, the specifications call for an unbalanced drive circuit with an output impedance of 75Ω and a output drive level of 0.5 volts peak-to-peak ±20% when measured across a 75Ω load using no cable. The circuit

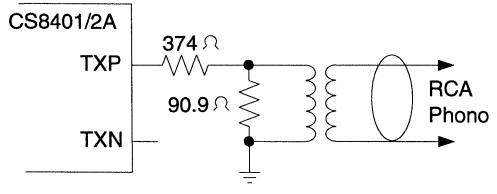


Figure A2. Consumer Output Circuit

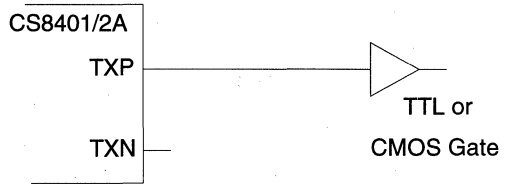


Figure A3. TTL/CMOS Output Circuit

shown in Figure A2 only uses the TXP pin and provides the proper output impedance and drive level using standard 1% resistors. The connector for consumer would be an RCA phono socket. This circuit is also short circuit protected.

The TXP pin may be used to drive TTL or CMOS gates as shown in Figure A3. This circuit may be used for optical connectors for digital audio since they are usually TTL compatible. This circuit is also useful when driving multiple digital audio outputs since RS422 line drivers have TTL interfaces.

The transformer should be capable of operating from 1.5 to 7 MHz, which is the audio data rate of 25 kHz to 55 kHz after biphase-mark encoding. Transformers provide isolation from ground loops, 60 Hz noise, and common mode noise and interference. One of the important considerations when choosing transformers is minimizing shunt capacitance between primary and secondary windings. The higher the shunt capacitance, the lower the isolation between primary and secondary, and the more coupling of high frequency energy. This energy appears in the form of common mode noise on the receive side ground and has the potential to degrade analog performance. Therefore, for best performance, shielded transformers optimized for minimum shunt capacitance should be used. The following are a few typical transformers:

Pulse Engineering
Telecom Products Group
7250 Convoy Ct.
San Diego, CA 92111

(619) 268-2400
Part Number: PE65612

Schott Corporation
1000 Parkers Lane Rd.
Wayzata, MN 55391
(612) 475-1173
FAX (612) 475-1786
Part Number:
67125450 - compatible with Pulse
67128990 - lower cost
67129000 - surface mount
67129600 - single shield

Scientific Conversions Inc.
42 Truman Drive
Novato, CA. 94947
(415) 8922323
Part Number:
SC916-01 - single shield
SC916-02 - surface mount

Appendix B: MCK and FSYNC Relationship

FSYNC should be derived either directly or indirectly from MCK. The indirect case could be a DSP, providing FSYNC through its serial port, using the same master oscillator that generates MCK. In either case, FSYNC's relationship to MCK is fixed and does not move. Since this appendix provides information on what would happen if FSYNC did move with respect to MCK, it does not apply to the majority of users.

All internal timing is derived from MCK. On the CS8402A, MCK is always 128×Fs. On the CS8401A, the external MCK is programmable and is initially divided to 128×Fs before being used by the part. The internal clock IMCK used in the following discussion is always 128×Fs regardless of the external MCK pin.

After $\overline{\text{RST}}$, the CS8401A and CS8402A synchronize the internal timing to the audio data port, more specifically FSYNC, to guarantee that channel A is left channel data and channel B is right channel data as per the AES/EBU specification. If FSYNC moves with respect to IMCK, the transmitter could lose synchronization, which causes an internal reset.

Figure B1 shows the structure of the serial port input, to the transmitter output. The audio data is serially shifted into R1. PLD is an internal signal that parallel loads R1 into the R2 buffer, and, at the same time, the C, U, and V bits are latched. On the CS8401A, the C, U, and V bits are held in RAM, whereas on the CS8402A, they are latched from external pins. The PLD signal rises on the first SCK edge that can latch data. This is coincident with the latching of the MSB of audio data in MSB-first, left-justified modes. PLD stays high for one SCK period. In the CS8402A section, the arrows on SCK in Figure 16 indicate when PLD goes high. Also, SBC in the CS8402A CD submode is an external version of PLD gated by the SBF input.

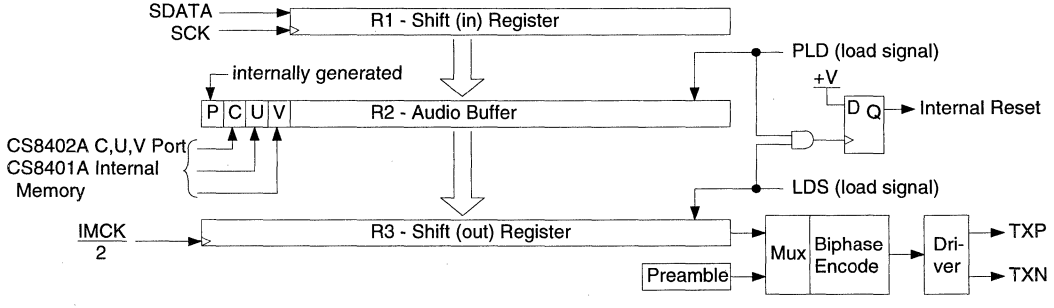


Figure B1. Serial Port-to-Transmitter Block Diagram

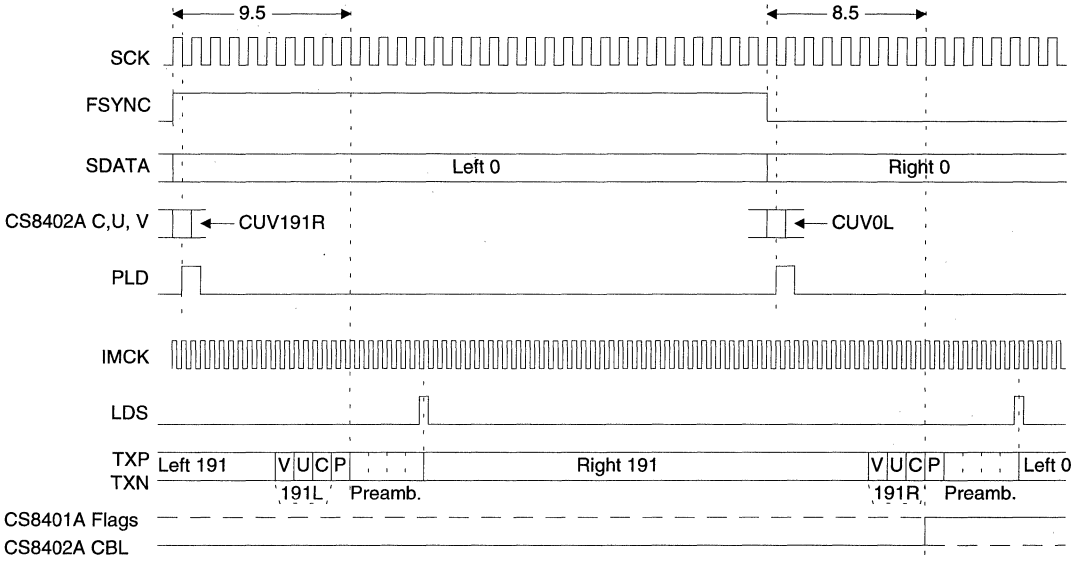


Figure B2. Serial Ports-to-Transmitter Timing (slave mode)

When the part is finished transmitting the preamble of a sub-frame, the internal signal LDS rises to parallel-load R2 into R3 for transmission. After $\overline{RST}$, the part synchronizes the audio port to IMCK as shown in Figure B2. Since PLD is based on FSYNC and LDS is based on IMCK, if FSYNC moves with respect to IMCK until PLD and LDS occur at the same time, the data would not be properly loaded into R3. If LDS and PLD overlap, an internal reset is initiated causing the timing to return to the initial state shown in Figure B2.

Ordering Guide

Model	Temperature Range	Package
CS8401A-CP	0 to 70 °C*	24-Pin Plastic .3" DIP
CS8401A-IP	-40 to 85 °C	24-Pin Plastic .3" DIP
CS8401A-CS	0 to 70 °C*	24-Pin Plastic SOIC
CS8401A-IS	-40 to 85 °C	24-Pin Plastic SOIC
CS8402A-CP	0 to 70 °C*	24-Pin Plastic .3" DIP
CS8402A-IP	-40 to 85 °C	24-Pin Plastic .3" DIP
CS8402A-CS	0 to 70 °C*	24-Pin Plastic SOIC
CS8402A-IS	-40 to 85 °C	24-Pin Plastic SOIC

* Although the '-CP' and '-CS' suffixed parts are guaranteed to operate over 0 to 70 °C, they are tested at 25 °C only. If testing over temperature is desired, the '-IP' and '-IS' suffixed parts are tested over their specified temperature range.

TABLE OF CONTENTS:

•Notes•

Digital Audio Interface Receiver

Features

- Monolithic CMOS Receiver
- Low-Jitter, On-Chip Clock Recovery
  256×Fs Output Clock Provided
- Supports: AES/EBU, IEC 958,
  S/PDIF, & EIAJ CP-340
  Professional and Consumer Formats
- Extensive Error Reporting
  Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Configurable Buffer Memory (CS8411)

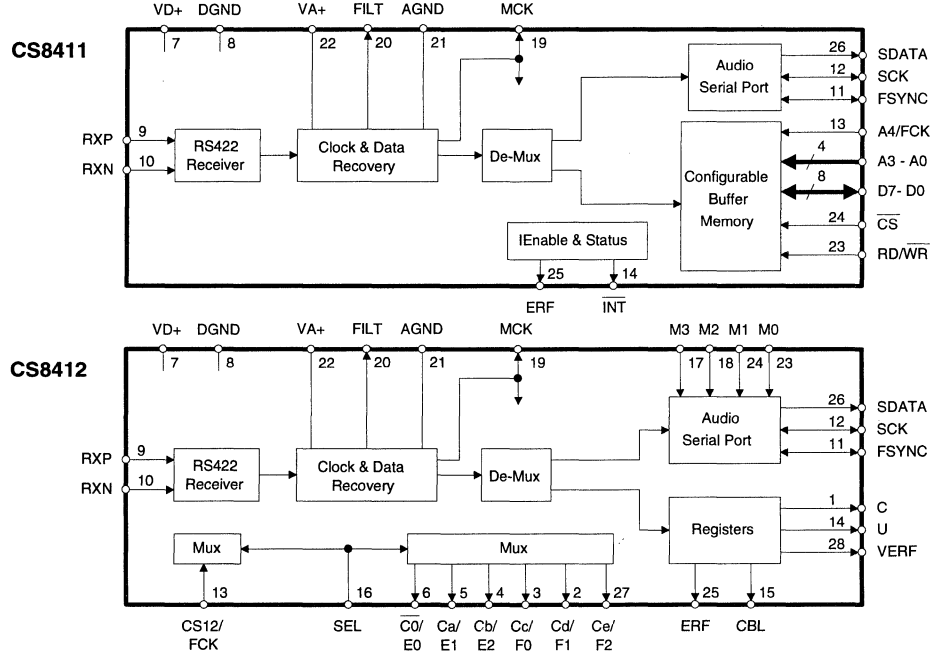
General Description:

The CS8411/12 are monolithic CMOS devices which receive and decode audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8411/12 receive data from a transmission line, recover the clock and synchronization signals, and de-multiplex the audio and digital data. Differential or single ended inputs can be decoded.

The CS8411 has a configurable internal buffer memory, read via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8412 de-multiplexes the channel, user, and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

ORDERING INFORMATION: page 6-67
TABLE OF CONTENTS: page 6-68



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

ABSOLUTE MAXIMUM RATINGS (GND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		VD+, VA+		6.0	V
Input Current, Any Pin Except Supply	Note 1	I_{in}		±10	mA
Input Voltage, Any Pin except RXP, RXN		V_{IN}	-0.3	VD+ + 0.3	V
Input Voltage, RXP and RXN		V_{IN}	-12	12	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		VD+, VA+	4.5	5.0	5.5	V
Supply Current	VA+	I_A		20	35	mA
	VD+	I_D		7	10	mA
Ambient Operating Temperature:	CS8411/12-CP or -CS Note 2	T_A	0	25	70	°C
	CS8411/12-IP or -IS		-40		85	°C
Power Consumption		P_D		135	248	mW

Notes: 2. The '-CP' and '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only. The '-IP' and '-IS' parts are tested over the full -40 to 85 °C temperature range.

DIGITAL CHARACTERISTICS

(T_A = 25 °C for suffixes '-CP' & '-CS', T_A = -40 to 85 °C for '-IP' & '-IS'; VD+, VA+ = 5V ± 10%)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	except RXP, RXN	V_{IH}	2.0			V
Low-Level Input Voltage	except RXP, RXN	V_{IL}			+0.8	V
High-Level Output Voltage	(I_O = 200µA)	V_{OH}	VD+ - 1.0			V
Low-Level Output Voltage	(I_O = -3.2mA)	V_{OL}			0.4	V
Input Leakage Current		I_{in}		1.0	10	µA
Input Sample Frequency (Note 3)	CS8411/12-CP or -CS	F_S	25		55	kHz
	CS8411/12-IP or -IS	F_S	30		50	kHz
Master Clock Frequency	Note 3	MCK	6.4	256×F_S	14.08	MHz
MCK Clock Jitter		t_j		200		ps RMS
MCK Duty Cycle (high time/cycle time)				50		%

Notes: 3. F_S is defined as the incoming audio sample frequency per channel.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS - RS422 RECEIVERS

(RXP, RXN pins only; VD+, VA+ = 5V ± 10%)

Parameter			Symbol	Min	Typ	Max	Units
Input Resistance	(-7V < V_{CM} < 7V)	Note 4	Z_{IN}		10		kΩ
Differential Input Voltage, RXP to RXN (-7V < V_{CM} < 7V)		Note 4,5	V_{TH}	200			mV
Input Hysteresis			V_{HYST}		50		mV

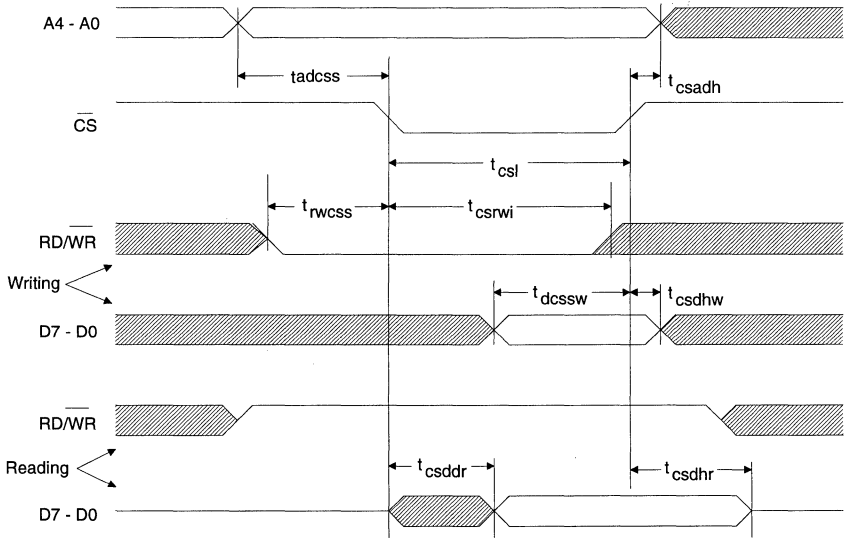
Notes: 4. V_{CM} - Input Common Mode Range

5. When the receiver inputs are configured for single ended operation (e.g. consumer configuration) the signal amplitude must exceed 400mVp-p for the differential voltage on RXP to RXN to exceed 200mV. This represents

SWITCHING CHARACTERISTICS - CS8411 PARALLEL PORT

(T_A = 25 °C for suffixes '-CP' and '-CS'; T_A = -40 to 85 °C for suffixes '-IP' and '-IS';
VD+, VA+ = 5V ± 10%; Inputs: Logic 0 = DGND, logic 1 = VD+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{CS}$ low		t_{adcss}	13.5			ns
$\overline{CS}$ high to ADDRESS invalid		t_{csadh}	0			ns
RD/$\overline{WR}$ valid to $\overline{CS}$ low		t_{rwcss}	10			ns
$\overline{CS}$ low to RD/$\overline{WR}$ invalid		t_{csrwi}	35			ns
$\overline{CS}$ low		t_{csl}	35			ns
DATA valid to $\overline{CS}$ rising	RD/$\overline{WR}$ low (writing)	t_{dcssw}	32			ns
$\overline{CS}$ high to DATA invalid	RD/$\overline{WR}$ low (writing)	t_{csdhw}	0			ns
$\overline{CS}$ falling to DATA valid	RD/$\overline{WR}$ high (reading)	t_{csddr}			35	ns
$\overline{CS}$ rising to DATA Hi-Z	RD/$\overline{WR}$ high (reading)	t_{csdhr}	5			ns



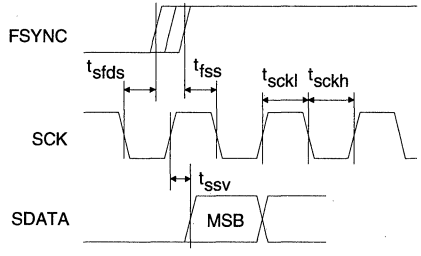
CS8411 Parallel Port Timing

SWITCHING CHARACTERISTICS - SERIAL PORTS

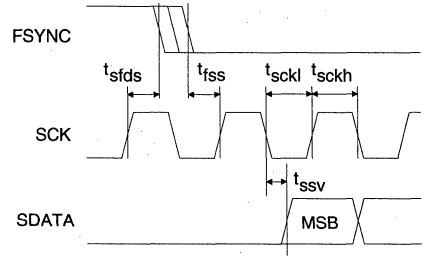
(T_A = 25 °C for suffixes '-CP' and '-CS'; T_A = -40 to 85 °C for suffixes '-IP' and '-IS';
VD+, VA+ = 5V ± 10%; Inputs: Logic 0 = DGND, logic 1 = VD+; C_L = 20 pF)

Parameter			Symbol	Min	Typ	Max	Units
SCK Frequency	Master Mode	Notes 5,6	f_{sck}		OWR×32		Hz
	Slave Mode	Note 6			OWR×32	TBD	Hz
SCK falling to FSYNC delay	Master Mode	Notes 6,7	t_{sfdm}	-20		20	ns
SCK Pulse Width Low	Slave Mode	Note 6	t_{sckl}	40			ns
SCK Pulse Width High	Slave Mode	Note 6	t_{sckh}	40			ns
SCK rising to FSYNC edge delay	Slave Mode	Notes 6,7	t_{sfds}	20			ns
FSYNC edge to SCK rising setup	Slave Mode	Notes 6,7	t_{fss}	20			ns
SCK falling (rising) to SDATA valid			Note 7	t_{ssv}			20ns
C, U, CBL valid to FSYNC edge	CS8412	Note 7	t_{cuvf}		$1/f_{sck}$		s
MCK to FSYNC edge delay	FSYNC from RXN/RXP		t_{mfd}		15		ns

Notes:
5. The output word rate, OWR, refers to the frequency at which an audio sample is output from the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample. In Slave mode 32 SCK periods must be provided in most serial port formats.
6. In master mode SCK and FSYNC are outputs. In Slave mode they are inputs. In the CS8411, control reg. 2 bit 1, MSTR, selects master. In the CS8412, formats 1 & 3 are slaves.
7. The table above assumes data is output on the falling edge and latched on the rising edge. With both parts the edge is selectable. The table is defined for the CS8411 with control reg. 2 bit 0, SCED, set to one, and for the CS8412 in formats 2, 3, 5 - 7. For the other formats, the table and figure edges must be reversed (i.e.. "rising" to "falling" and vice versa).

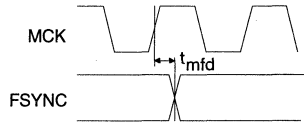


Mode 1

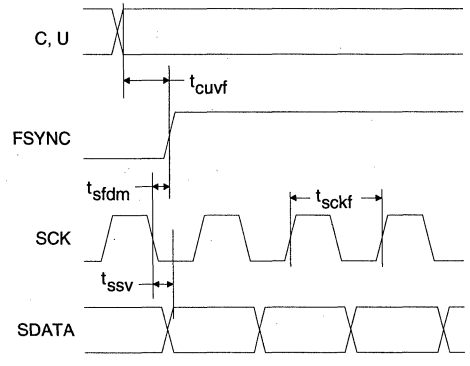


Mode 3

Serial Output Timing - Slave Mode



FSYNC Generated From Received Data



Serial Output Timing - Master Mode & C, U Port

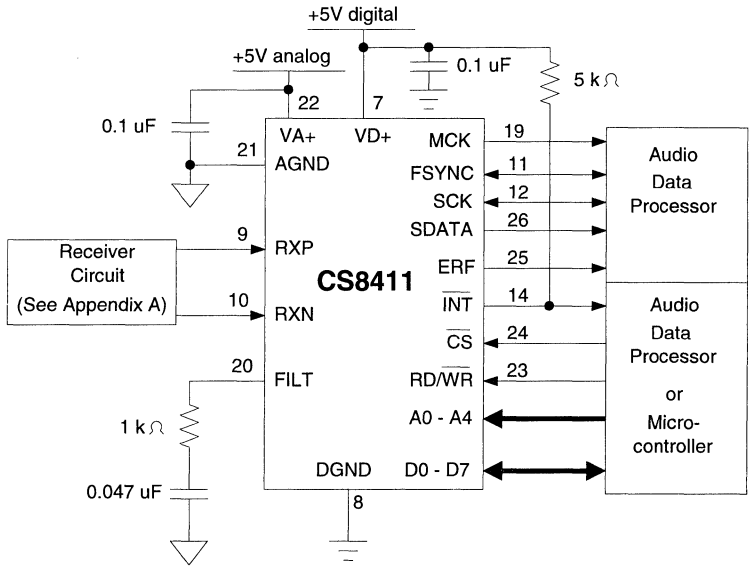


Figure 1. CS8411 Typical Connection Diagram

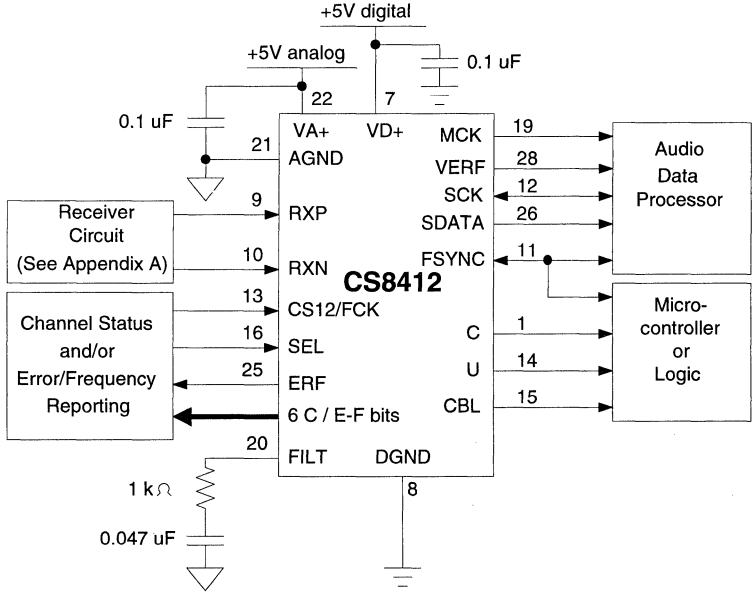


Figure 2. CS8412 Typical Connection Diagram

GENERAL DESCRIPTION

The CS8411/12 are monolithic CMOS circuits that receive and decode audio and digital data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 interface standards. Both chips contain RS422 line receivers and Phase-Locked Loops (PLL) that recover the clock and synchronization signals, and de-multiplex the audio and digital data. The CS8411 contains a configurable internal buffer memory, read via a parallel port, which can buffer channel status, user, and optionally auxiliary data. The CS8412 de-multiplexes the channel status, user, and validity information directly to serial output pins with dedicated pins for the most important channel status bits. Both chips also contain extensive error reporting as well as incoming sample frequency indication for auto-set applications.

Familiarity with the AES/EBU and IEC 958 specifications are assumed throughout this document. The App Note, Overview of Digital Audio Interface Data Structures, contains information on digital audio specifications; however, it is not meant to be a complete reference. To guarantee compliance, the proper standards documents should be obtained. The AES/EBU standard, AES3-1985, should be obtained from the Audio Engineering Society or ANSI (ANSI document # ANSI S4.40-1985); the IEC 958 standard from the International Electrotechnical Commission; and the EIAJ CP-340 standard from the Japanese Electronics Bureau.

Line Receiver

The RS422 line receiver can decode differential as well as single ended inputs. The receiver consists of a differential input Schmitt trigger with 50mV of hysteresis. The hysteresis prevents noisy signals from corrupting the phase detector. Appendix A contains more information on how to configure the line receivers for differential and single ended signals.

Clocks and Jitter Attenuation

The primary function of these chips is to recover audio data and low jitter clocks from a digital audio transmission line. The clocks that can be generated are MCK (256×F_S), SCK (64×F_S), and FSYNC (F_S or 2×F_S). MCK is the output of the voltage controlled oscillator which is a component of the PLL. The PLL consists of phase and frequency detectors, a second-order loop filter, and a voltage controlled oscillator. All components of the PLL are on chip with the exception of a resistor and capacitor used in the loop filter. This filter is connected between the FILT pin and AGND. The closed-loop transfer function, which specifies the PLL's jitter attenuation characteristics, is shown in Figure 3. The loop will begin to attenuate jitter at approximately 25 kHz with another pole at 80 kHz, and will have 50 dB of attenuation by 1MHz. Since most data jitter introduced by the transmission line is high in frequency, it will be strongly attenuated.

Multiple frequency detectors are used to minimize the time it takes the PLL to lock to the incoming data stream and to prevent false lock conditions. When the PLL is not locked to the incoming data stream, the frequency detectors pull the VCO frequency within the lock range of the PLL. When no digital audio data is present, the VCO frequency is pulled to its minimum value.

As a master, SCK is always MCK divided by four, producing a frequency of 64×F_S. In the CS8411, FSYNC can be programmed to be a divided version of MCK or it can be generated directly from the incoming data stream. In the CS8412, FSYNC is always generated from the incoming data stream. When FSYNC is generated from the data, its edges are extracted at times when intersymbol interference is at a minimum. This provides a sample frequency clock that is as spectrally pure as the digital audio source clock for moderate length transmission lines. For long transmission lines, the CS8411 can be pro-

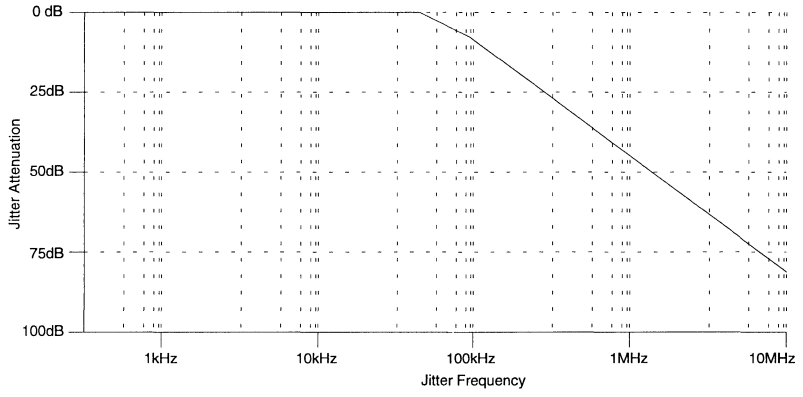


Figure 3. Jitter Attenuator Characteristics

grammed to generate FSYNC from MCK instead of from the incoming data.

CS8411 DESCRIPTION

The CS8411 is more flexible than the CS8412 but requires a microcontroller or DSP to load internal registers. The CS8412 does not have internal registers so it may be used in a stand-alone mode where no microprocessor or DSP is available.

The CS8411 accepts data from a transmission line coded according to the digital audio interface standards. The I.C. recovers clock and data, and separates the audio data from control information. The audio data is output through a configurable serial port and the control information is stored in internal dual-port RAM. Extensive error reporting is available via internal registers with the option of repeating the last sample when an error occurs. A block diagram of the CS8411 is shown in Figure 4

Parallel Port

The parallel port accesses two status registers, two interrupt enable registers, two control registers, and 28 bytes of dual-port buffer memory. The status registers and interrupt enable registers occupy the same address space. A bit in control register 1 selects the two registers, either status or interrupt enable, that occupy addresses 0 and 1 in the memory map. The address bus and the RD/$\overline{WR}$ line should be valid when $\overline{CS}$ goes low. If RD/$\overline{WR}$ is low, the value on the data bus will be written into the buffer memory at the specified address. If RD/$\overline{WR}$ is high, the value in the buffer memory, at the specified address, is placed on the data bus. Detailed timing for the parallel port can be found in the *Switching Characteristics - Parallel Port* table.

The memory space on the CS8411 is allocated as shown in Figure 5. There are three defined buffer modes selectable by two bits in control register 1. Further information on the buffer modes can be found in the *Control Registers* section.

Status and IEnable Registers

The status and interrupt enable registers occupy the same address space. The IER/$\overline{SR}$ bit in control register 1 selects whether the status registers (IER/$\overline{SR}$ = 0) or the IEnable registers (IER/$\overline{SR}$ = 1) occupy addresses 0 and 1. Upon power-up, the control and IEnable registers contain all zeros; therefore, the status registers are visible and all interrupts are disabled. The IER/$\overline{SR}$ bit must be set to make the IEnable registers visible.

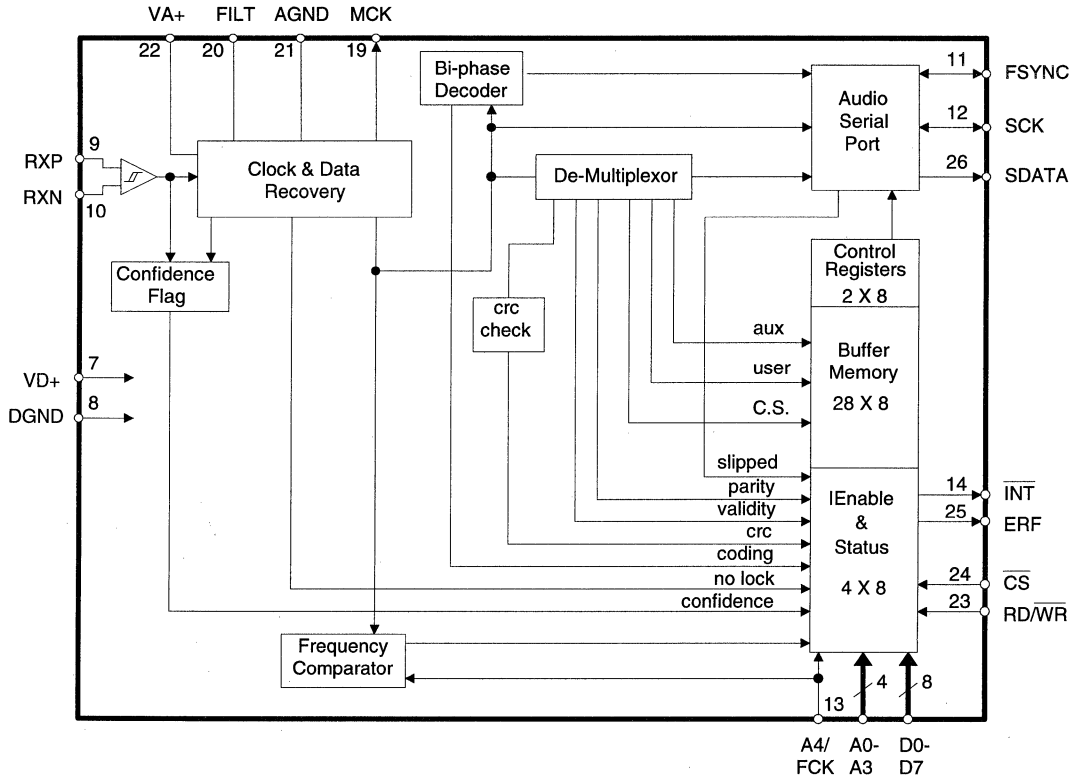


Figure 4. CS8411 Block Diagram

Status register 1 (SR1), shown in Figure 6, reports all the conditions that can generate a pulse of four SCLK cycles on the interrupt pin ($\overline{INT}$). The three least significant bits, FLAG2-FLAG0, are used to monitor the ram buffer. These bits continually change and indicate the position of the buffer pointer which points to the buffer memory location currently being written. Each flag has a corresponding interrupt enable bit in IEnable register 1 which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. FLAG0 and FLAG1 cause interrupts on both edges whereas FLAG2 causes an interrupt on the rising edge only. Further information, including timing, on the flags can be found in the *Buffer Memory* section.

The next five bits; ERF, SLIP, CCHG, CRCE/CRC1, and CSDIF/CRC2, are latches which are set when their corresponding conditions occur, and are reset when SR1 is read. Interrupt pulses are generated the first time that condition occurs. If the status register is not read, further instances of that same condition will not generate another interrupt. ERF is the error flag bit and is set when the ERF pin goes high. It is an OR'ing of the errors listed in status register 2, bits 0 through 4, AND'ed with their associated interrupt enable bits in IEnable register 2.

SLIP is only valid when the audio port is in slave mode (FSYNC and SCK are inputs to the CS8411). This flag is set when an audio sample is dropped or reread because the audio data output from the part is at a different frequency than the

data received from the transmission line. CCHG is set when any bit in channel status bytes 0 through 3, stored in the buffer, changes from one block to the next. In buffer modes 0 and 1, only one channel of channel status data is buffered, so CCHG is only affected by that channel. (CS2/$\overline{CS1}$ in CR1 selects which channel is buffered.) In buffer mode 2 both channels are buffered, so both channels affect CCHG. This bit is updated after each byte (0 to 3) is written to the buffer. The two most significant bits in SR1, CRCE/CRC1 and CSDIF/CRC2, are dual function flags. In buffer modes 0 and 1, they are CRCE and CSDIF, and in buffer mode 2, they are CRC1 and CRC2. In buffer modes 0 and 1, the channel selected by the CS2/$\overline{CS1}$ bit is stored in RAM and CRCE indicates that a CRC error occurred in that channel. CSDIF is set if there is any difference between the channel status bits of each channel. In buffer mode 2 channel status from both channels is buffered, with CRC1 indicating a CRC error in channel 1 and CRC2 indicating a CRC error in channel 2. CRCE, CRC1, and CRC2 are updated at the block boundary. Block boundary violations also cause CRC1,2 or CRCE to be set.

IEnable register 1, which occupies the same address space as status register 1, contains interrupt enable bits for all conditions in status register 1. A "1" in a bit location enables the same bit location in status register 1 to generate an interrupt pulse. A "0" masks that particular status bit from causing an interrupt.

Status register 2 (SR2) reports all the conditions that can affect the error flag bit in SR1 and the error pin (ERF), and can specify the received clock frequency. As previously mentioned, the first five bits of SR2 are AND'ed with their interrupt enable bits (in IER2) and then OR'ed to create ERF. The V, PARITY, CODE, LOCK, and

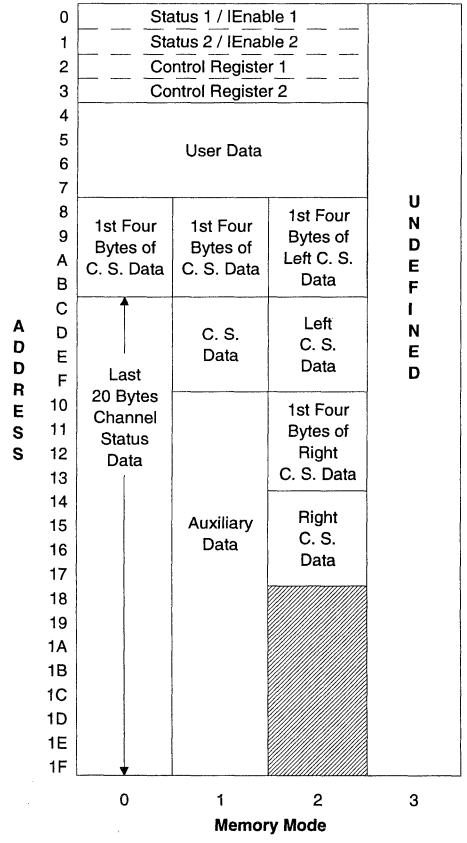


Figure 5. CS8411 Buffer Memory Map

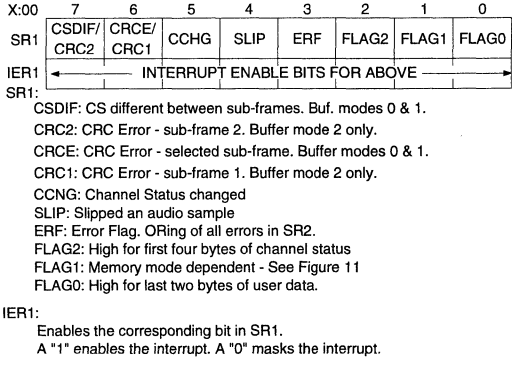
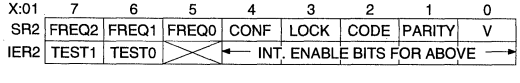


Figure 6. Status/IEnable Register 1

CONF bits are latches which are set when their corresponding conditions occur, and are reset when SR2 is read. The ERF pin is asserted each time the error occurs assuming the interrupt enable bit in IER2 is set for that particular error. When the ERF pin is asserted, the ERF bit in SR1 is set. If the ERF bit was not set prior to the ERF pin assertion, an interrupt will be generated (assuming bit 3 in IER1 is set). Although the ERF pin is asserted for each occurrence of an enabled error condition, the ERF bit will only cause an interrupt once if SR1 is not read.

V is the validity status bit which is set any time the received validity bit is high. PARITY is set when a parity error is detected. CODE is set when a biphase coding error is detected. LOCK is asserted when the receiver PLL is not locked and occurs when there is no input on RXP/RXN, or if the received frequency is out of the receiver lock range (25 kHz to 55 kHz). Lock is achieved after receiving three frame preambles followed by one block preamble, and is lost after four consecutive frame preambles are not received. CONF is the confidence flag which is asserted when the received data eye opening is less than half a bit period. This indicates the transmission link is poor and does not meet specifications.



SR2:
FREQ2: The 3 FREQ bits indicate incoming sample freq.
FREQ1: (must have 6.144 MHz clock on FCK pin
FREQ0: and FCEN must be "1")
CONF: Confidence error
LOCK: Out-of-Lock error
CODE: Coding violation
PARITY: Parity error
V: Validity bit high

IER2:
TEST1,0: (0 on power-up) Must stay at "0".
INT. ENABLES: Enables the corresponding bit in SR2.
A "1" enables the interrupt. A "0" masks the interrupt.

Figure 7. Status/IEnable Register 2

The upper three bits in SR2, FREQ2-FREQ0, can report the receiver frequency when the receiver is locked. These bits are only valid when FCEN in control register 1 is set, and a 6.144 MHz clock is applied to the FCK pin. When FCEN is set, the A4/FCK pin is used as FCK and A4 is internally set to zero; therefore, only the lower half of the buffer can be accessed. Table 2 lists the frequency ranges reported. The FREQ bits are updated three times per block and the clock on the FCK pin must be valid for two thirds of a block for the FREQ bits to be accurate. The vast majority of audio systems must meet the 400 ppm tolerance listed in the table. The 4% tolerance is provided for unique situations where the approximate frequency needs to be known, even though that frequency is outside the normal audio specifications.

IEnable register 2 has corresponding interrupt enable bits for the first five bits in SR2. A "1" enables the condition in SR2 to cause ERF to go high, while a "0" masks that condition. Bit 5 is unused and bits 6 and 7, the two most significant bits, are factory test bits and must be set to zero when writing to this register. The CS8411 sets these bits to zero on power-up.

Control Registers

The CS8411 contains two control registers. Control register 1 (CR1), at address 2, selects system level features, while control register 2 (CR2), at address 3, configures the audio serial port.

In control register 1, when $\overline{\text{RST}}$ is low, all outputs are reset except MCK (FSYNC and SCLK are high impedance). After the user sets $\overline{\text{RST}}$ high, the CS8411 comes fully out of reset when the block boundary is found. The serial port, in master mode, will begin to operate as soon as $\overline{\text{RST}}$ goes high. B0 and B1 select one of three buffer modes listed in Table 1 and illustrated in Figure 5. In all modes four bytes of user data are stored. In mode 0, one entire block of channel status is stored. In mode 1 eight bytes of channel status

and sixteen bytes of auxiliary data are stored. In mode 2, eight bytes of channel status from each sub-frame are stored. The buffer modes are discussed in more detail in the *Buffer Memory* section. The next bit, CS2/$\overline{CS1}$, selects the particular sub-frame of channel status to buffer in modes 0 and 1, and has no effect in mode 2. When CS2/$\overline{CS1}$ is low, sub-frame 1 is buffered, and when CS2/$\overline{CS1}$ is high, sub-frame 2 is buffered. IER/$\overline{SR}$ selects which set of registers, either IEnable or status, occupy addresses 0 and 1. When IER/$\overline{SR}$ is low, the status registers occupy the first two addresses, and when IER/$\overline{SR}$ is high, the IEnable registers occupy those addresses. FCEN enables the internal frequency counter. A 6.144 MHz clock must be connected to the FCK pin as a reference. The value of the FREQ bits in SR2 are not valid until two thirds of a block of data is received. Since FCK and A4, the most significant address bit, occupy the same pin, A4 is internally set to zero when FCEN is high. Since A4 is forced to zero, the upper half of the buffer is not accessible while using the frequency compare feature. FPLL determines how FSYNC is derived. When FPLL is low, FSYNC is derived from the incoming data, and when FPLL is high, it is derived from the internal phase-locked loop.

Control Register 2 configures the serial port which consists of three pins: SCK, SDATA, and FSYNC. SDATA is always an output, but SCK and FSYNC can be configured as inputs or outputs. FSYNC and SDATA can have a variety of relationships to each other, and the polarity of SCK can be controlled. The large variety of audio data formats provides an easy interface to most DSPs and other audio processors. SDATA is normally just audio data, but special modes are provided that output received biphase data, or received NRZ data with zeros substituted for preamble. Another special mode allows an asynchronous SCK input to read audio data from the serial port without slipping samples. In this mode FSYNC and SDATA are outputs synchronized to the SCK input. Since SCK is asynchronous to the received clock, the number of SCK cycles between FSYNC edges will vary.

X:02	7	6	5	4	3	2	1	0
CR1	FPLL	FCEN	IER/$\overline{SR}$	CS2/$\overline{CS1}$	B1	B0	X	$\overline{RST}$

FPLL: 0 - FSYNC from RXP/RXN, 1 - FSYNC from PLL
FCEN: enables freq. comparator (FCK must be 6.144 MHz).
IER/$\overline{SR}$: [X:00,01] 0 - status, 1 - interrupt enable registers.
CS2/$\overline{CS1}$: ch. status to buffer; 0 - sub-frame 1, 1 - sub-frame 2.
B1: with B0, selects the buffer memory mode.
B0: with B1, selects the buffer memory mode.
$\overline{RST}$: Resets internal counters. Set to "1" for normal operation.

Figure 8. Control Register 1

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 1. Buffer Memory Modes

X:03	7	6	5	4	3	2	1	0
CR2	ROER	SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

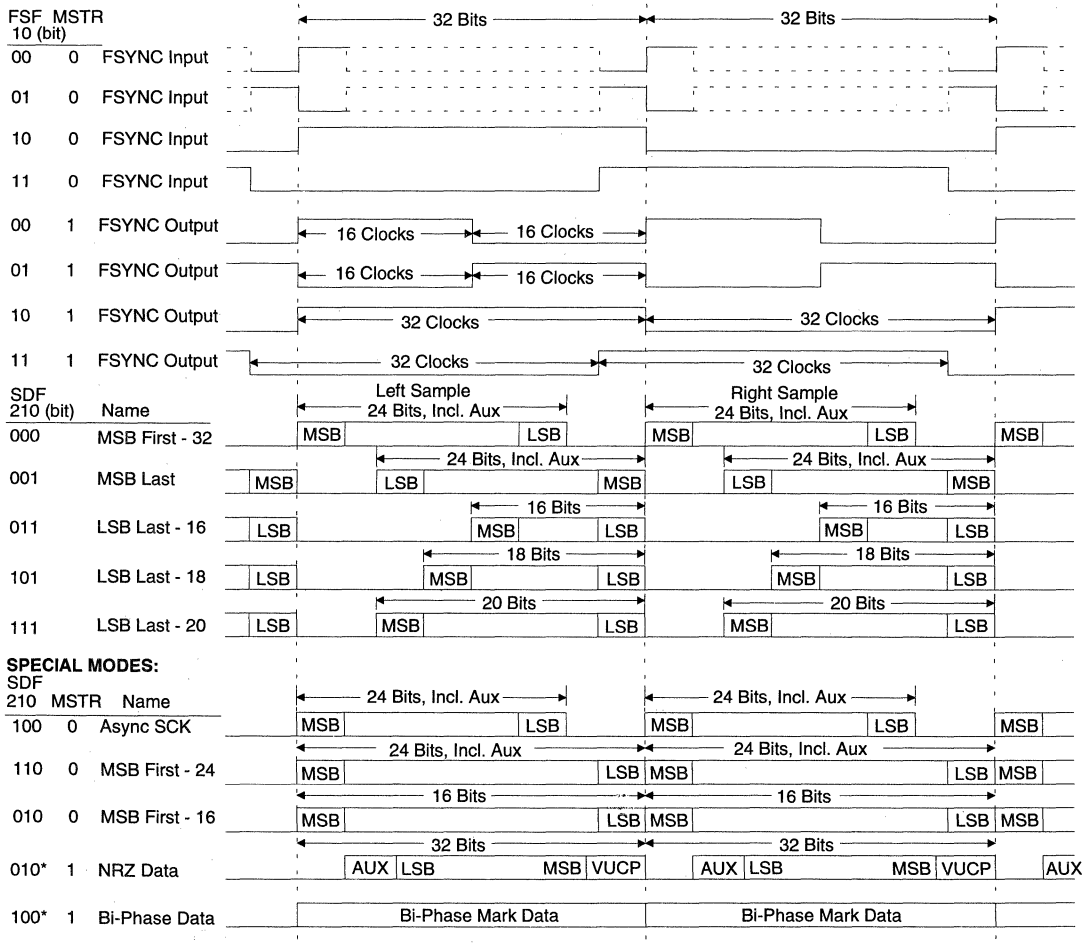
ROER: Repeat previous value on error (audio data)
SDF2: with SDF0 & SDF1, select serial data format.
SDF1: with SDF0 & SDF2, select serial data format.
SDF0: with SDF1 & SDF2, select serial data format.
FSF1: with FSF0, select FSYNC format.
FSF0: with FSF1, select FSYNC format.
MSTR: When set, SCK and FSYNC are outputs.
SCED: When set, falling edge of SCK outputs data.
When clear, rising edge of SCK outputs data.

Figure 9. Control Register 2

FREQ2	FREQ1	FREQ0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz ± 4%
0	1	0	44.1 kHz ± 4%
0	1	1	32 kHz ± 4%
1	0	0	48 kHz ± 400 ppm
1	0	1	44.1 kHz ± 400 ppm
1	1	0	44.056 kHz ± 400 ppm
1	1	1	32 kHz ± 400 ppm

Table 2. Incoming Sample Frequency Bits

ROER, when set, causes the last audio sample to be reread if the error pin, ERF, is active. When out of lock, the CS8411 will output zeros if ROER is set and output random data if ROER is not set. The conditions that activate ERF are those reported in SR2 and enabled in IER2. Figure 10 illustrates the modes selectable by SDF2-SDF0 and FSF1-FSF0. MSTR, which in most applications will be set to one, determines whether FSYNC and SCK are outputs (MSTR = 1) or inputs (MSTR = 0). When FSYNC and SCK are inputs (slave mode) the audio data can be read twice or missed if the device controlling FSYNC and SCK is on a different time-base than the CS8411. If the audio data is read twice or missed, the SLIP bit in SR1 is set. SCED selects the SCK edge to output data on. SCED high causes data to be output on the falling edge, and SCED low causes data to be output on the rising edge.



* Error flags are not accurate in these modes

Figure 10. CS8411 Serial Port SDATA and FSYNC Timing

Audio Serial Port

The audio serial port outputs the audio data portion from the received data and consists of three pins: SCK, SDATA, and FSYNC. SCK clocks the data out on the SDATA line. The edge that SCK uses to output data is programmable from CR2. FSYNC delineates the audio samples and may indicate the particular channel, left or right. Figure 10 illustrates the multitude of formats that SDATA and FSYNC can take.

NORMAL MODES

SCK and FSYNC can be inputs (MSTR = 0) or outputs (MSTR = 1), and are usually programmed as outputs. As outputs, SCK contains 32 periods for each sample and FSYNC has four formats. The first two output formats of FSYNC (shown in Figure 10) delineate each word and the identification of the particular channel must be kept track of externally. This may be done using the rising edge of FLAG2 to indicate the next data word is left channel data. The last two output formats of FSYNC also delineate each channel with the polarity of FSYNC indicating the particular channel. The last format has FSYNC change one SCK cycle before the frame containing the data and may be used to generate an I^2S compatible interface.

When SCK is programmed as an input, 32 SCK cycles per sample must be provided. (There are two formats in the *Special Modes* section where SCK can have 16 or 24 clocks per sample.) The four modes where FSYNC is an input are similar to the FSYNC output modes. The first two require a transition of FSYNC to start the sample frame, whereas the last two are identical to the corresponding FSYNC output modes. If the circuit generating SCK and FSYNC is not locked to the master clock of the CS8411, the serial port will eventually be reread or a sample will be missed. When this occurs, the SLIP bit in SR1 will be set.

SDATA can take on five formats in the normal serial port modes. The first format (see Figure 10), MSB First, has the MSB aligned with the start of a sample frame. Twenty-four audio bits are output including the auxiliary bits. This mode is compatible with many DSPs. If the auxiliary bits are used for something other than audio data, they must be masked off. The second format, MSB Last, outputs data LSB first with the MSB aligned to the end of the sample frame. This format is conducive to serial arithmetic. Both of the above formats output all audio bits from the received data. The last three formats are LSB Last formats that output the most significant 16, 18, and 20 bits respectively, with the LSB aligned to the end of the sample frame. These formats are used by many interpolation filters.

SPECIAL MODES

Five special modes are included for unique applications. In these modes, the master bit, MSTR, must be defined as shown in Figure 10. In the first mode, Asynchronous SCK, FSYNC (which is an output in this mode) is aligned to the incoming SCK. This mode is useful when the SCK is locked to an external event and cannot be derived from MCK. Since SCK is asynchronous, the number of SCK cycles per sample frame will vary. The data output will be MSB first, 24 bits, and aligned to the beginning of a sample frame. The second and third special modes are unique in that they contain 24 and 16 SCK cycles respectively per sample frame, whereas all normal modes contain 32 SCK cycles. In these two modes, the data is MSB first and fills the entire frame. The fourth special mode outputs NRZ data including the V, U, C, and P bits and the preamble replaced with zeros. SCK is an output with 32 SCK cycles per sample frame. The fifth mode outputs the biphase data recovered from the transmission line with 64 SCK cycles output per sample frame, with data changing on the rising edge.

Normally, data recovered by the CS8411 is delayed by two frames in propagating through the part, but in the fourth and fifth special modes, the data is delayed only a few bit periods before being output. However, error codes, and the C, U and V bits follow the normal a pathway with a two frame delay (so that the error code would be output with the offending data in the other modes). As a result, in special modes four and five, the error codes are nearly two frames behind the data output on SDATA.

Buffer Memory

In all buffer modes, the status, mask, and control registers are located at addresses 0-3, and the user data is buffered at locations 4 through 7. The parallel port can access any location in the user data buffer at any time; however, care should be taken not to read a location when that location is being updated internally. This internal writing is done through a second port of the buffer and is done in a cyclic manner. As data is received, the bits are assembled in an internal 8-bit shift register which, when full, is loaded into the buffer memory. The first bit received is stored in D0 and, after D7 is received, the byte is written into the proper buffer memory location.

The user data is received one bit per sub-frame. At the channel status block boundary, the internal pointer for writing user data is initialized to 04H (Hex). After receiving eight user bits, the byte is written to the address indicated by the user pointer which is then incremented to point to the next address. After receiving all four bytes of user data, 32 audio samples, the user pointer is set to 04H again and the cycle repeats. FLAG0, in SR1 can be used to monitor the user data buffer. When the last byte of the user buffer, location 07H, is written, FLAG0 is set low and when the second byte, location 05H, is written, FLAG0 is set high. If the corresponding bit in the interrupt enable register (IER1, bit 0) is set, a transition of FLAG0 will generate a low pulse on the interrupt pin. The level of FLAG0 indicates which two bytes the part will write next, thereby indicating which two bytes are free to be read.

FLAG1 is buffer mode dependent and is discussed in the individual buffer mode sections. A transition of FLAG1 will generate an interrupt if the appropriate interrupt enable bit is set.

FLAG2 is set high after channel status byte 23, the last byte of the block, is written and set low after channel status byte 3 is written to the buffer memory. FLAG2 is unique in that only the rising edge can cause an interrupt if the appropriate interrupt enable bit in IER1 is set.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of channel status data per channel and 384 audio samples. The lower portion of Figure 11 expands the first byte of channel status showing eight pairs of data, with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits defined as per the digital audio standards. When receiving stereo, channel A is left and channel B is right.

For all three buffer modes, the three most significant bits in SR1, shown in Figure 6, can be used to monitor the channel status data. In buffer mode 2, bits 7 and 6 change definition and are described in that section. Channel status data, as described in the standards, is independent for each channel. Each channel contains its own block of channel status data, and in most systems, both channels will contain the same channel status data. Buffer modes 0 and 1 operate on one block of channel status with the particular block selected by the CS2/$\overline{\text{CS1}}$ bit in CR1. CSDIF, bit 7 in SR1, indicates when the channel status data for each channel is not the same even though only one channel is being buffered. CRCE, bit 6 in SR1, indicates a CRC error occurred in the buffered channel. CCHG, bit 5 in SR1, is set when any bit in the buffered channel status bytes 0 to 3, change from one block to the next.

BUFFER MODE 0

The user data buffer previously described is identical for all modes. Buffer mode 0 allocates the rest of the buffer to channel status data. This mode stores an entire block of channel status in 24 memory locations from address 08H to 1FH. Channel status (CS) data is different from user data in that channel status data is independent for each channel. A block of CS data is defined as one bit per frame, not one bit per sub-frame; therefore, there are two blocks of channel status. The CS2/$\overline{CS1}$ bit in CR1 selects which channel is stored in the buffer. In a typical system sending stereo data, the channel status data for each channel would be identical.

FLAG1 in status register 1, SR1, can be used to monitor the channel status buffer. In mode 0, FLAG1 is set low after channel status byte 23 (the last byte) is written, and is set high when channel status byte 15, location 17H is written. If the corresponding interrupt enable bit in IER1 is set, a transition of FLAG1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory write sequence for buffer mode 0 along with flag timing. The arrows on the flag timing indicate when an interrupt will occur if the appropriate interrupt enable bit is set. FLAG0 can cause an interrupt on either edge, which is only shown in the expanded portion of the figure for clarity.

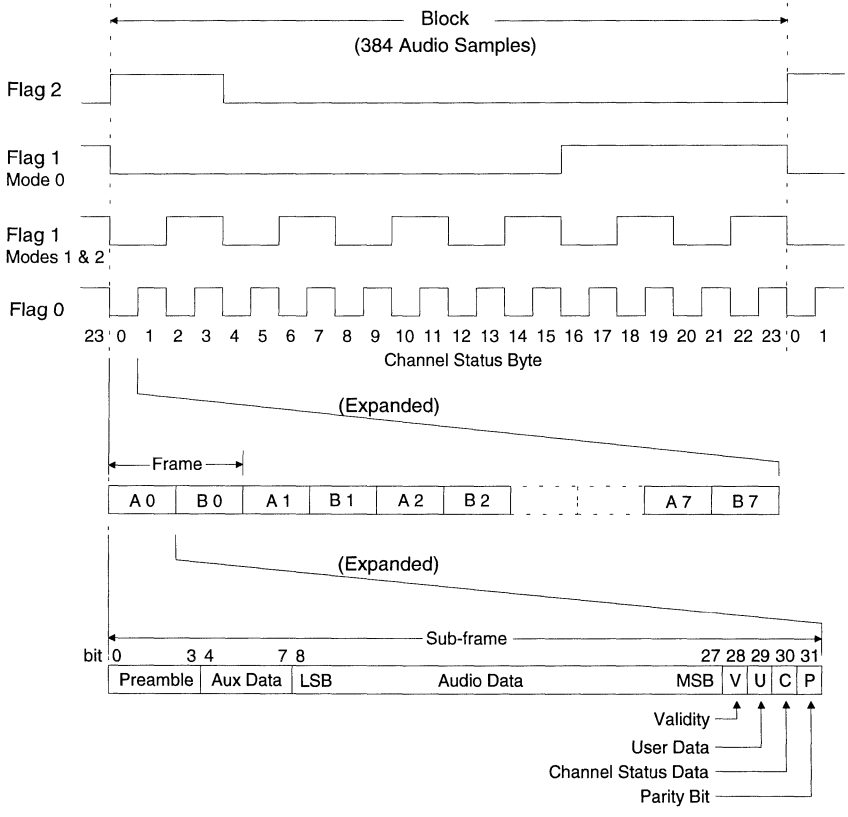


Figure 11. CS8411 Status Register Flag Timing

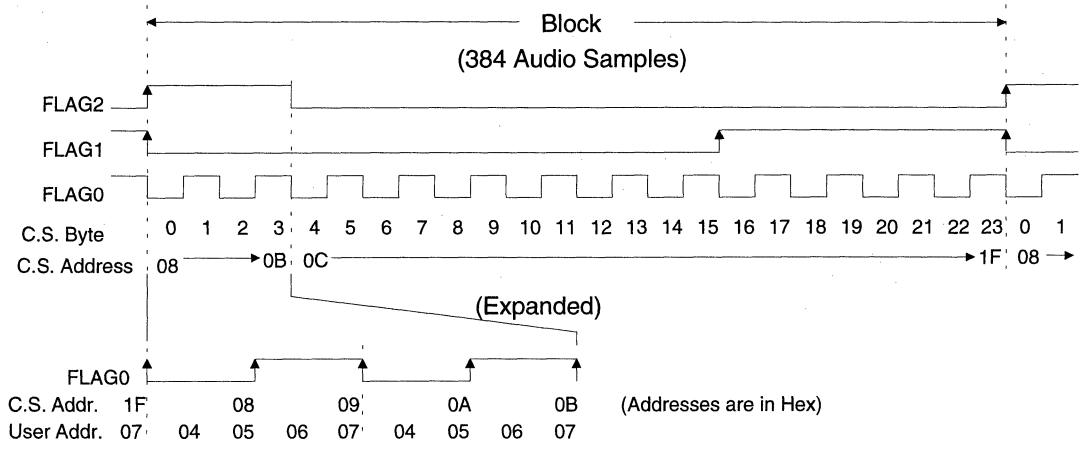


Figure 12. CS8411 Buffer Memory Write Sequence - MODE 0

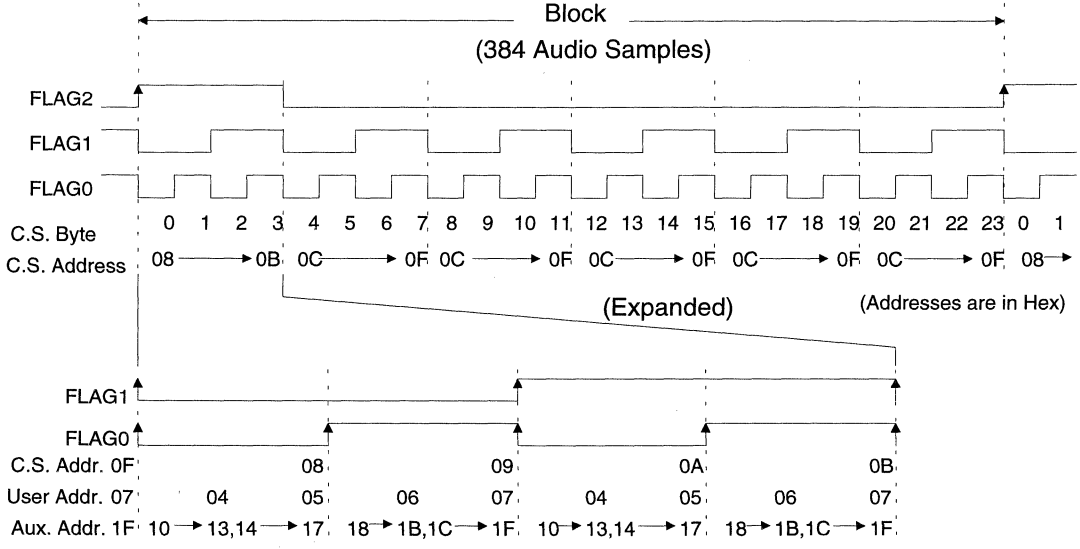


Figure 13. CS8411 Buffer Memory Write Sequence - MODE 1

BUFFER MODE 1

In buffer mode 1, eight bytes are allocated for channel status data and sixteen bytes for auxiliary data as shown in Figure 5. The user data buffer is the same for all modes. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are written once per channel status block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data. The channel status buffer is divided in this fashion because the first four bytes are the most important ones; whereas, the last 20 bytes are often not used (except for byte 23, CRC).

FLAG1 and FLAG2 can be used to monitor this buffer as shown in Figure 13. FLAG1 is set high when CS byte 1, location 09H, is written and is toggled when every other byte is written. FLAG2 is set high after CS byte 23 is written and set low after CS byte 3, location 0BH, is written. FLAG2 determines whether the channel status pointer is writing to the first four-byte section of the channel status buffer or the second four-byte section, while FLAG1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is written to in a cyclic manner similar to the other buffers. Four auxiliary data bits are received per audio sample (sub-frame) and, since the auxiliary data is four times larger than the user data, the auxiliary data buffer on the CS8411 is four times larger allowing FLAG0 to be used to monitor both.

BUFFER MODE 2

In buffer mode 2, two 8-byte buffers are available to independently buffer each channel of channel status data. Both buffers are identical to the channel status buffer in mode 1 and are written to simultaneously, with locations 08H to 0FH containing CS data for channel A and locations 10H to 17H containing CS data for channel B. Both

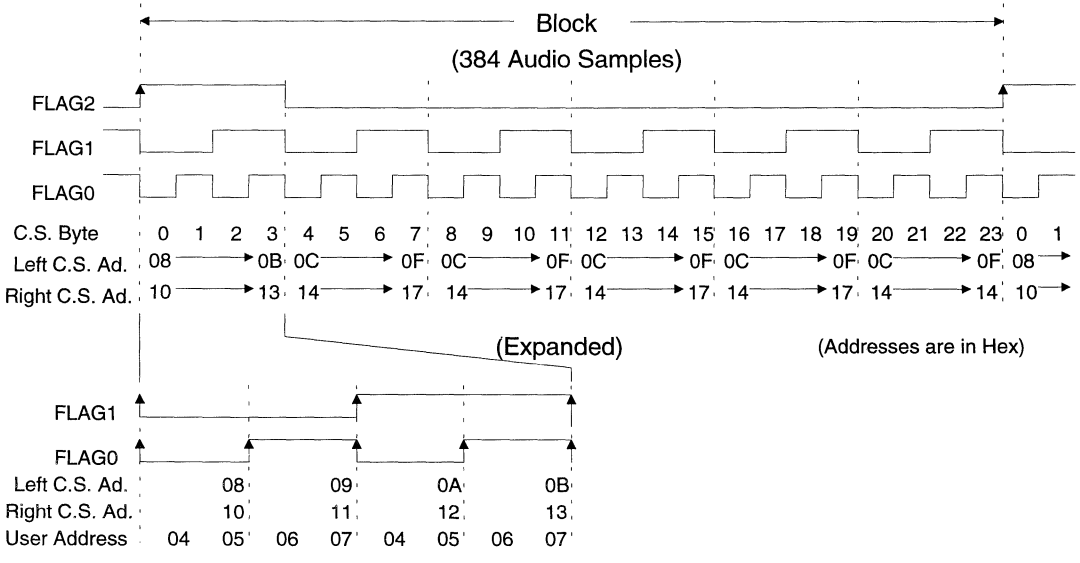


Figure 14. CS8411 Buffer Memory Write Sequence - MODE 2

CS buffers can be monitored using FLAG1 and FLAG2 as described in the *BUFFER MODE 1* section.

The two most significant bits in SR1 change definition for buffer mode 2. These two bits, when set, indicate CRC errors for their respective channels. A CRC error occurs when the internal calculated CRC for channel status bytes 0 through 22 does not match channel status byte 23. CCHG, bit 5 in SR1, is set when any bit in the first four channel status bytes of either channel changes from one block to the next. Since channel status doesn't change very often, this bit may be monitored rather than checking all the bits in the first four bytes. These bits are illustrated in Figure 6.

Buffer Updates and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally reading the buffer RAM and the CS8411 internally writing to it may be averted by using the flag levels to avoid the section currently being addressed by the part. However, if the interrupt line, along with the flags, is utilized, the actual byte that was just updated can be determined. In this way, the entire buffer can be read without concern for internal updates. Figure 15 shows the detailed timing for the interrupt line, flags, and the RAM write line. SCK is 64 times the incoming sample frequency, and is the same SCK output in master mode. The FSYNC shown is valid for all master modes except the I^2S compatible mode. The interrupt pulse is shown to be 4 SCK periods wide and goes low 5 SCK periods after the RAM is written. Using the above information, the entire data buffer may be read starting with the next byte to be updated by the internal pointer.

ERF Pin Timing

ERF signals that an error occurred while receiving the audio sample that is currently being read from the serial port. ERF changes with the active edge of FSYNC and is high during the errorred sample. ERF is affected by the error conditions reported in SR2: CONF, LOCK, CODE, PARITY, and V. Any of these conditions may be masked off using the corresponding bits in IER2. The ERF pin will go high for each error that occurs. The ERF bit in SR1 is different from the ERF pin in that it only causes an interrupt the first time an error occurs until SR1 is read. More information on the ERF pin and bit is contained at the end of the *Status and IEnable Registers* section.

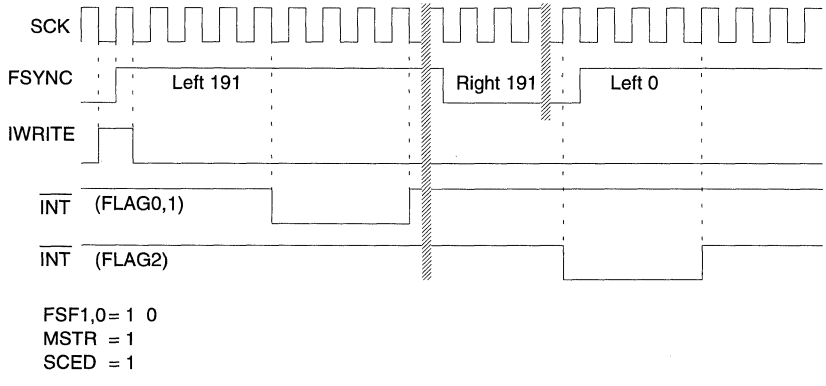
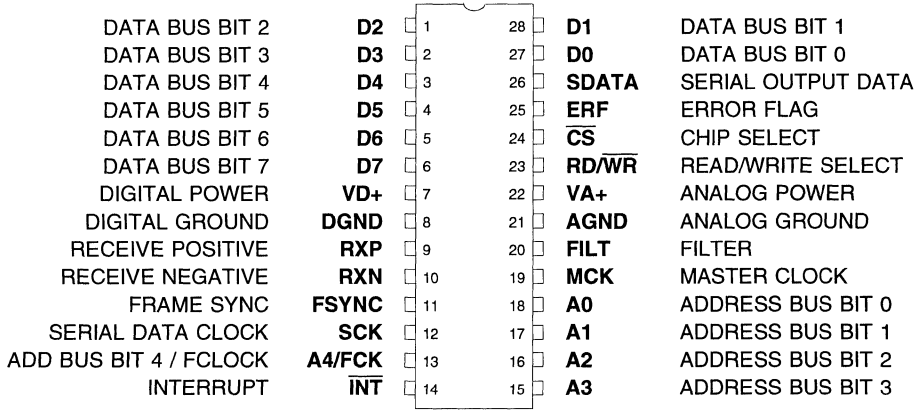


Figure 15. RAM/Buffer-Write and Interrupt Timing

PIN DESCRIPTIONS:

CS8411



6

Power Supply Connections

VD+ - Positive Digital Power, PIN 7.

Positive supply for the digital section. Nominally +5 volts.

VA+ - Positive Analog Power, PIN 22.

Positive supply for the analog section. Nominally +5 volts. This supply should be as quiet as possible since noise on this pin will directly affect the jitter performance of the recovered clock.

DGND - Digital Ground, PIN 8.

Ground for the digital section. DGND should be connected to same ground as AGND.

AGND - Analog Ground, PIN 21.

Ground for the analog section. AGND should be connected to same ground as DGND.

Audio Output Interface

SCK - Serial Clock, PIN 12.

Serial clock for SDATA pin which can be configured (via control register 2) as an input or output, and can sample data on the rising or falling edge. As an input, SCK must contain 32 clocks for every audio sample in all normal audio serial port formats.

FSYNC - Frame Sync, PIN 11.

Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 2.

SDATA - Serial Data, PIN 26.

Audio data serial output pin.

ERF - Error Flag, PIN 25.

Signals that an error has occurred while receiving the audio sample currently being read from the serial port. The errors that cause ERF to go high are enumerated in status register 2 and enabled by setting the corresponding bit in IEnable register 2.

A4/FCK - Address Bus Bit 4/Frequency Clock, PIN 13.

This pin has a dual function and is controlled by the FCEN bit in control register 1. A4 is the address bus pin as defined below. When used as FCK, an internal frequency comparator compares a 6.144 MHz clock input on this pin to the received clock frequency and stores the value in status register 1 as three FREQ bits. These bits indicate the incoming frequency as well as the tolerance. When defined as FCK, A4 is internally set to 0.

Parallel Interface

$\overline{CS}$ - Chip Select, PIN 24.

This input is active low and allows access to the 32 bytes of internal memory. The address bus and RD/$\overline{WR}$ must be valid while $\overline{CS}$ is low.

RD/$\overline{WR}$ - Read/Write, PIN 23.

If RD/$\overline{WR}$ is low when $\overline{CS}$ goes active (low), the data on the data bus is written to internal memory. If RD/$\overline{WR}$ is high when $\overline{CS}$ goes active, the data in the internal memory is placed on the data bus.

A4-A0 - Address Bus, PINS 13, 15-18.

Parallel port address bus that selects the internal memory location to be read from or written to. Note that A4 is the dual function pin A4/FCK as described above.

D0-D7 - Data Bus, PINS 27-28, 1-6.

Parallel port data bus used to check status, read or write control words, or read internal buffer memory.

$\overline{\text{INT}}$ - Interrupt, PIN 14.

Open drain output that can signal the state of the internal buffer memory as well as error information. A 5kΩ resistor to VD+ is typically used to support logic gates. All bits affecting $\overline{\text{INT}}$ are maskable to allow total control over the interrupt mechanism.

Receiver Interface

RXP, RXN - Differential Line Receivers, PINS 9, 10.

RS422 compatible line receivers. Described in detail in Appendix A.

Phase Locked Loop

MCK - Master Clock, PIN 19.

Low jitter clock output of 256 times the received sample frequency.

FILT - Filter, PIN 20.

An external 1kΩ resistor and 0.047µF capacitor are required from the FILT pin to analog ground.

CS8412 DESCRIPTION

The CS8412 does not need a microprocessor to handle the non-audio data (although a micro may be used with the C and U serial ports). Instead, dedicated pins are available for the most important channel status bits. The CS8412 is a monolithic CMOS circuit that receives and decodes digital audio data which was encoded according to the digital audio interface standards. It contains an RS422 line receiver and clock and data recovery utilizing an on-chip phase-locked loop. The audio data is output through a configurable serial port that supports 14 formats. The channel status and user data have their own serial pins and the validity flag is OR'ed with the ERF flag to provide a single pin, VERF, indicating that the audio output may not be valid. This pin may be used by interpolation filters that provide error correction. A block diagram of the CS8412 is illustrated in Figure 16.

The line receiver and jitter performance are described in the sections directly preceding the CS8411 sections in the beginning of this data sheet.

Audio Serial Port

The audio serial port is used primarily to output audio data and consists of three pins: SCK, FSYNC, and SDATA. These pins are configured via four control pins: M0, M1, M2, and M3. M3 selects between eight normal serial formats (M3 = 0), and six special formats (M3 = 1).

NORMAL MODES (M3 = 0)

When M3 is low, the normal serial port formats shown in Figure 17 are selected using M2, M1, and M0. These formats are also listed in Table 3, wherein the first word past the format number (Out-In) indicates whether FSYNC and SCK are

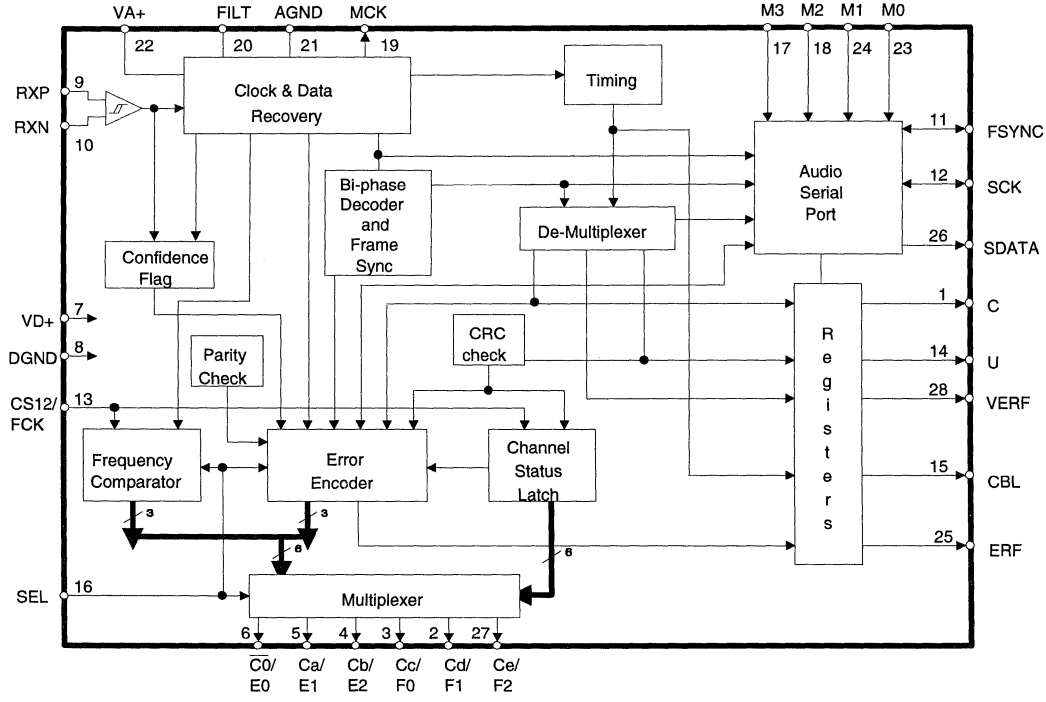


Figure 16. CS8412 Block Diagram

outputs from the CS8412 or are inputs. The next word (L/R-WSYNC) indicates whether FSYNC indicates the particular channel or just delineates each word. If an error occurs (ERF = 1) while using one of these formats, the previous valid audio data for that channel will be output. As long as ERF is high, that same data word will be output. If the CS8412 is not locked, it will output all zeroes. In some modes FSYNC and SCK are outputs and in others they are inputs. In Table 3, LSBJ is short for *LSB justified* where the LSB is justified to the end of the audio frame and the MSB varies with word length. As outputs the CS8412 generates 32 SCK periods per audio sample (64 per stereo sample) and, as inputs, 32 SCK periods must be provided per audio sample. When FSYNC and SCK are inputs, one stereo sample is double buffered. For those modes which output 24 bits of audio data, the auxiliary bits will be included. If the auxiliary bits are not used for audio data, they must be masked off.

SPECIAL MODES (M3 = 1)

When M3 is high, the special audio modes described in Table 4 are selected via M2, M1, and M0. In formats 8, 9, and 10, SCK, FSYNC, and SDATA are the same as in formats 0, 1, and 2 respectively; however, the recovered data is output as is even if ERF is high, indicating an error. (In modes 0-2 the previous valid sample is output.) Similarly, when out of lock, the CS8412 will still output all the recovered data, which should be zeros if there is no input to the RXP, RXN pins.

M2	M1	M0	Format
0	0	0	0 - Out, L/R, 16-24 Bits
0	0	1	1 - In, L/R, 16-24 Bits
0	1	0	2 - Out, L/R, I^2S Compatible
0	1	1	3 - In, L/R, I^2S Compatible
1	0	0	4 - Out, WSYNC, 16-24 Bits
1	0	1	5 - Out, L/R, 16 Bits LSBJ
1	1	0	6 - Out, L/R, 18 Bits LSBJ
1	1	1	7 - Out, L/R, MSB Last

Table 3. Normal Audio Port Modes (M3=0)

Format 11 is similar to format 0 except that SCK is an input and FSYNC is an output. In this mode FSYNC and SDATA are synchronized to the incoming SCK, and the number of SCK periods between FSYNC edges will vary since SCK is not synchronous to received data stream. This mode may be useful when writing data to storage.

Format 12 is similar to format 7 except that SDATA is the entire data word received from the transmission line including the C, U, V, and P bits, with zeros in place of the preamble. In format 13 SDATA contains the entire biphase encoded data from the transmission line including the preamble, and SCK is twice the normal frequency. The normal two frame delay of data from input to output is reduced to only a few bit periods in formats 12 and 13. However, the C, U, V bits and error codes follow their normal pathways and therefore follow the output data by nearly two frames. Figure 18 illustrates formats 12 and 13. Format 14 is reserved and not presently used, and format 15 causes the CS8412 to go into a reset state. While in reset all outputs will be inactive except MCK. The CS8412 comes out of reset at the first block boundary after leaving the reset state.

C, U, VERF, ERF, and CBL Serial Outputs

The C and U bits and CBL are output one SCK period prior to the active edge of FSYNC in all serial port formats except 2 and 3 (I^2S modes). The active edge of FSYNC may be used to latch C, U, and CBL externally. In formats 2 and 3,

M2	M1	M0	Format
0	0	0	8 - Format 0 - No repeat on error
0	0	1	9 - Format 1 - No repeat on error
0	1	0	10 - Format 2 - No repeat on error
0	1	1	11 - Format 0 - Async. SCK input
1	0	0	12 - Received NRZ Data
1	0	1	13 - Received Bi-phase Data
1	1	0	14 - Reserved
1	1	1	15 - CS8412 Reset

Table 4. Special Audio Port Modes (M3=1)

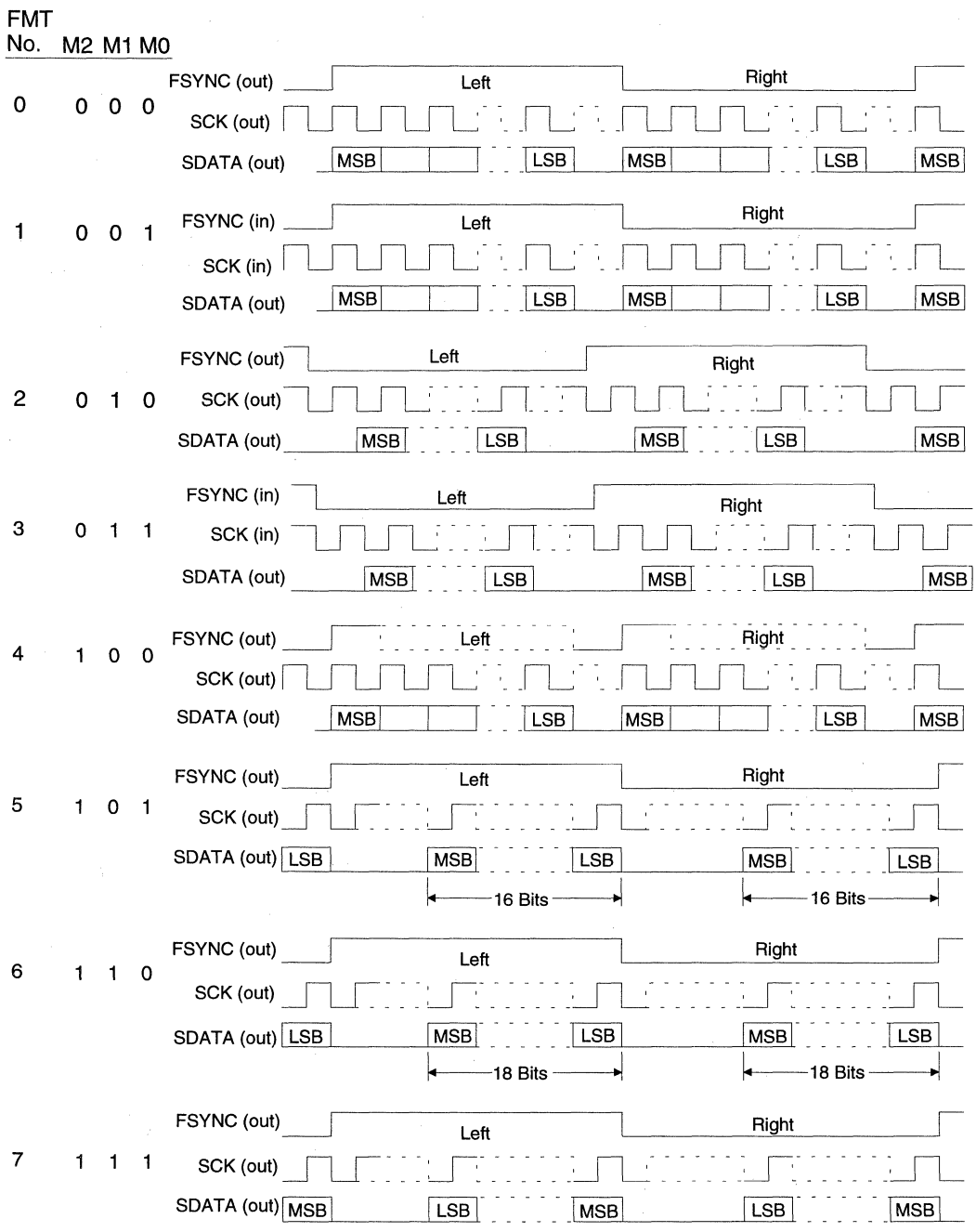


Figure 17. CS8412 Audio Serial Port Formats

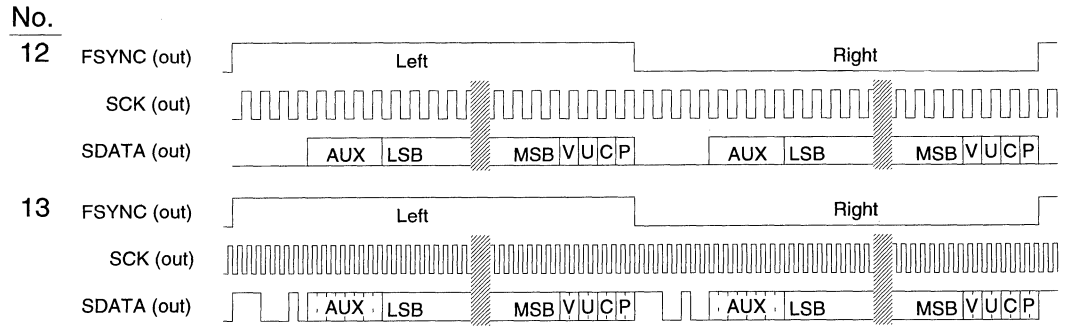


Figure 18. Special Audio Port Formats 12 and 13

the C and U bits and CBL are updated with the active edge of FSYNC. The validity + error flag (VERF) and the error flag (ERF) are always updated at the active edge of FSYNC. This timing is illustrated in Figure 19.

The C output contains the channel status bits with CBL rising indicating the start of a new channel status block. CBL is high for the first four bytes of channel status (32 frames or 64 samples) and low for the last 20 bytes of channel status (160 frames or 320 samples). The U output contains the User Channel data. The V bit is OR'ed with the ERF flag and output on the VERF pin. This indicates that the audio sample may be in error and can be used by interpolation filters to interpolate through the error. ERF being high indicates a serious error occurred on the transmission line. There are three errors that cause ERF to go high: a parity error or biphase coding violation during that sample, or an out of lock PLL receiver. Timing for the above pins is illustrated in Figure 19.

Multifunction Pins

There are seven multifunction pins which contain either error and received frequency information, or channel status information, selectable by SEL.

ERROR AND FREQUENCY REPORTING

When SEL is low, error and received frequency information are selected. The error information is encoded on pins E2, E1, and E0, and is decoded

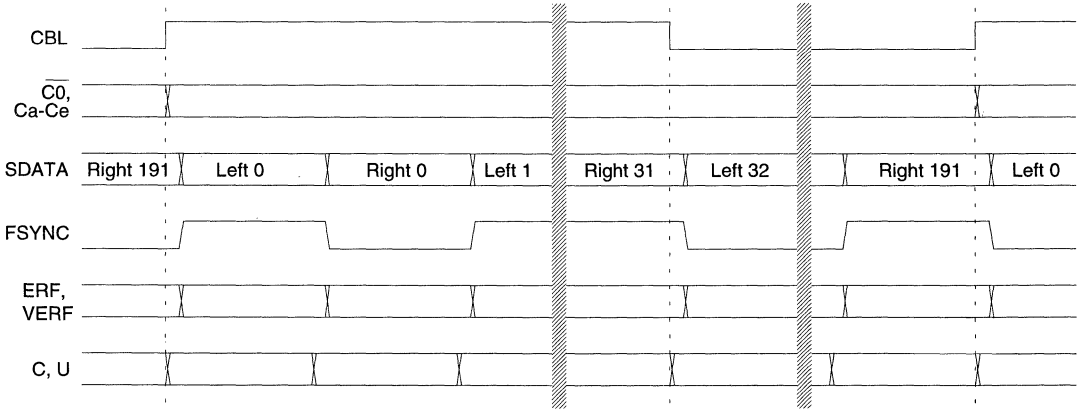


Figure 19. CBL Timing

as shown in Table 5. When an error occurs, the corresponding error code is latched. Clearing is then accomplished by bringing SEL high for more than eight MCK cycles. The errors have a priority associated with their error code, with validity having the lowest priority and no lock having the highest priority. Since only one code can be displayed, the error with the highest priority that occurred since the last clearing will be selected.

The validity flag indicates that the validity bit for a previous sample was high since the last clearing of the error codes. The confidence flag occurs when the received data eye opening is less than half a bit period. This indicates that the quality of the transmission link is poor and does not meet the digital audio interface standards. The slipped sample error can only occur when FSYNC and SCK of the audio serial port are inputs. In this case, if FSYNC is asynchronous to the received data rate, periodically a stereo sample will be dropped or reread depending on whether the read rate is slower or faster than the received data rate. When this occurs, the slipped sample error code will appear on the 'E' pins. The CRC error is updated at the beginning of a channel status block, and is only valid when the professional format of channel status data is received. This error is indicated when the CS8412 calculated CRC value does not match the CRC byte of the channel status block or when a block boundary changes (as in removing samples while editing). The parity error occurs when the incoming sub-frame does not have even parity as specified by the standards. The biphase coding error indicates a biphase coding violation occurred. The no lock error indicates that the PLL is not locked onto the incoming data stream. Lock is achieved after receiving three frame preambles then one block preamble, and is lost after not receiving four consecutive frame preambles.

The received frequency information is encoded on pins F2, F1, and F0, and is decoded as shown in Table 6. The on-chip frequency comparator compares the received clock frequency to an externally supplied 6.144 MHz clock which is input on the FCK pin. The 'F' pins are updated three times during a channel status block including prior to the rising edge of CBL. CBL may be used to externally latch the 'F' pins. The clock on FCK must be valid for two thirds of a block for the 'F' pins to be accurate.

CHANNEL STATUS REPORTING

When SEL is high, channel status is displayed on $\overline{C0}$, and Ca-Ce for the channel selected by CS12. If CS12 is low, channel status for sub-frame 1 is displayed, and if CS12 is high, channel status for sub-frame 2 is displayed. The contents of Ca-Ce depend upon the $\overline{C0}$ professional/consumer bit. The information reported is shown in Table 7.

E2	E1	E0	Error
0	0	0	No Error
0	0	1	Validity Bit High
0	1	0	Confidence Flag
0	1	1	Slipped Sample
1	0	0	CRC Error (PRO only)
1	0	1	Parity Error
1	1	0	Bi-Phase Coding Error
1	1	1	No Lock

Table 5. Error Decoding

F2	F1	F0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz ± 4%
0	1	0	44.1kHz ± 4%
0	1	1	32kHz ± 4%
1	0	0	48kHz ± 400 ppm
1	0	1	44.1kHz ± 400 ppm
1	1	0	44.056kHz ± 400 ppm
1	1	1	32kHz ± 400 ppm

Table 6. Sample Frequency Decoding

Professional Channel Status ($\overline{C0}$ = 0)

When $\overline{C0}$ is low, the received channel status block is encoded according to the professional/broadcast format. The Ca through Ce pins are defined for some of the more important professional bits. As listed in Table 7, Ca is the inverse of channel status bit 1. Therefore, if the incoming channel status bit 1 is 1, Ca, defined as $\overline{C1}$, will be 0. $\overline{C1}$ indicates whether audio ($\overline{C1}$ = 1) or non-audio ($\overline{C1}$ = 0) data is being received. Cb and Cc, defined as EM0 and EM1 respectively, indicate emphasis and are encoded versions of channel status bits 2, 3, and 4. The decoding is listed in Table 8. Cd, defined as $\overline{C9}$, is the inverse of channel status bit 9, which gives some indication of channel mode. (Bit 9 is also defined as bit 1 of byte 1.) When Ce, defined as $\overline{CRCE}$, is low, the CS8412 calculated CRC value does not match the received CRC value. This signal may be used to qualify Ca through Cd. If Ca through Ce are being displayed, Ce going low can indicate not to update the display.

Consumer Channel Status ($\overline{C0}$ = 1)

When $\overline{C0}$ is high, the received channel status block is encoded according to the consumer format. In this case Ca through Ce are defined differently as shown in Table 7. Ca is the inverse of channel status bit 1, $\overline{C1}$, indicating audio ($\overline{C1}$ = 1) or non-audio ($\overline{C1}$ = 0). Cb is defined as the inverse of channel status bit 2, $\overline{C2}$, which indicates copy inhibit/copyright information. Cc, defined as $\overline{C3}$, is the emphasis bit of channel status, with $\overline{C3}$ low indicating the data has had pre-emphasis added.

Pin	Professional	Consumer
$\overline{C0}$	0 (low)	1 (high)
Ca	$\overline{C1}$	$\overline{C1}$
Cb	EM0	$\overline{C2}$
Cc	EM1	$\overline{C3}$
Cd	$\overline{C9}$	$\overline{ORIG}$
Ce	$\overline{CRCE}$	IGCAT

Table 7. Channel Status Pins

The audio standards, in consumer mode, describe bit 15, L, as the generation status which indicates whether the audio data is an original work or a copy (1st generation or higher). The definition of the L bit is reversed for three category codes: two broadcast codes, and laser-optical (CD's). Therefore, to interpret the L bit properly, the category code must be decoded. The CS8412 does this decoding internally and provides the $\overline{ORIG}$ signal that, when low, indicates that the audio data is original over all category codes.

SCMS

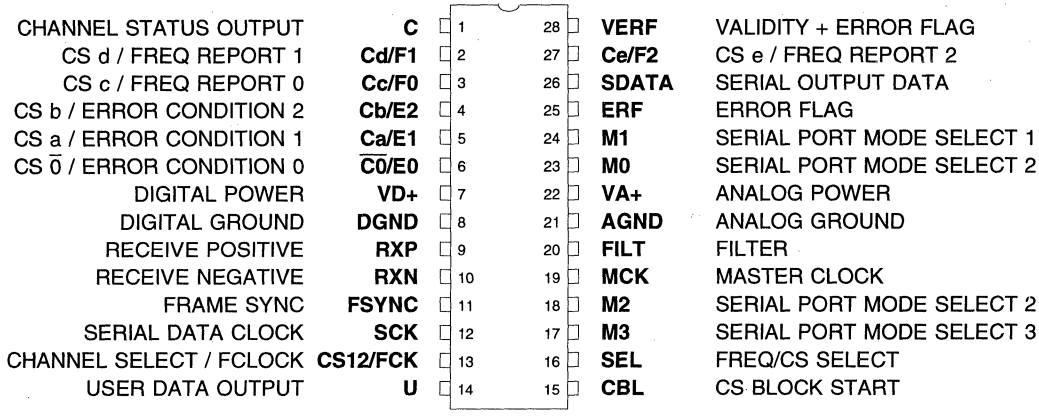
The consumer audio standards also mention a serial copy management system, SCMS, for dealing with copy protection of copyrighted works. SCMS is designed to allow unlimited duplication of the original work, but no duplication of any copies of the original. This system utilizes the channel status bit 2, Copy, and channel status bit 15, L or generation status, along with the category codes. If the Copy bit is 0, copyright protection is asserted over the material. Then, the L bit is used to determine if the material is an original or a duplication. (As mentioned in the previous paragraph, the definition of the L bit can be reversed based on the category codes.) There are two category codes that get special attention: general and A/D converters without C or L bit information. For these two categories the SCMS standard requires that equipment interfacing to these categories set the C bit to 0 (copyright protection asserted) and the L bit to 1 (original). To support this feature, Ce, in the consumer mode, is defined as IGCAT (ignorant category) which is low for the "general" (0000000) and "A/D converter without copyright information" (01100xx) categories.

EM1	EM0	C2	C3	C4
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

Table 8. Emphasis Encoding

PIN DESCRIPTIONS:

CS8412



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.

Positive supply for the digital section. Nominally +5 volts.

VA+ - Positive Analog Power, PIN 22.

Positive supply for the analog section. Nominally +5 volts.

DGND - Digital Ground, PIN 8.

Ground for the digital section. DGND should be connected to same ground as AGND.

AGND - Analog Ground, PIN 21.

Ground for the analog section. AGND should be connected to same ground as DGND.

Audio Output Interface

SCK - Serial Clock, PIN 12.

Serial clock for SDATA pin which can be configured (via the M0, M1, M2, and M3 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will generate 32 clocks for every audio sample. As an input, 32 SCK periods per audio sample must be provided in all normal modes.

FSYNC - Frame Sync, PIN 11.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, M2, and M3 pins.

SDATA - Serial Data, PIN 26.
Audio data serial output pin.

M0, M1, M2, M3 - Serial Port Mode Select, PINS 23, 24, 18, 17.
Selects the format of FSYNC and the sample edge of SCK with respect to SDATA. M3 selects between eight normal modes (M3 = 0), and six special modes (M3 = 1).

Control Pins

VERF - Validity + Error Flag, PIN 28.
A logical OR'ing of the validity bit from the received data and the error flag. May be used by interpolation filters to interpolate through errors.

U - User Bit, PIN 14.
Received user bit serial output port. FSYNC may be used to latch this bit externally.

C - Channel Status Output, PIN 1.
Received channel status bit serial output port. FSYNC may be used to latch this bit externally.

CBL - Channel Status Block Start, PIN 15.
The channel status block output is high for the first four bytes of channel status and low for the last 16 bytes.

SEL - Select, PIN 16.
Control pin that selects either channel status information (SEL = 1) or error and frequency information (SEL = 0) to be displayed on six of the following pins.

$\overline{C0}$, Ca, Cb, Cc, Cd, Ce - Channel Status Output Bits, PINS 2-6, 27.
These pins are dual function with the 'C' bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.

CS12 - Channel Select, PIN 13.
This pin is also dual function and is selected by bringing SEL high. CS12 selects sub-frame 1 (when low) or sub-frame 2 (when high) to be displayed by channel status pins $\overline{C0}$ and Ca through Ce.

FCK - Frequency Clock, PIN 13.
Frequency Clock input that is enabled by bringing SEL low. FCK is compared to the received clock frequency with the value displayed on F2 through F0. Nominal input value is 6.144 MHz.

E0, E1, E2 - Error Condition, PINS 4-6.

Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bring SEL high for more than 8 MCK cycles.

F0, F1, F2 - Frequency Reporting Bits, PINS 2-3, 27.

Encoded sample frequency information that is enabled by bringing SEL low. A proper clock on FCK must be input for at least two thirds of a channel status block for these pins to be valid. They are updated three times per block, starting at the block boundary.

ERF - Error Flag, PIN 25.

Signals that an error has occurred while receiving the audio sample currently being read from the serial port. Three errors cause ERF to go high: a parity or biphase coding violation during the current sample, or an out of lock PLL receiver.

Receiver Interface

RXP, RXN - Differential Line Receivers, PINS 9, 10.

RS422 compatible line receivers.

Phase Locked Loop

MCK - Master Clock, PIN 19.

Low jitter clock output of 256 times the received sample frequency.

FILT - Filter, PIN 20.

An external 1kΩ resistor and 0.047µF capacitor is required from FILT pin to analog ground.

APPENDIX A: RS422 Receiver Information

The RS422 receivers on the CS8411 and CS8412 are designed to receive both the professional and consumer interfaces, and meet all specifications listed in the digital audio standards. Figure A1 illustrates the internal schematic of the receiver portion of both chips. The receiver has a differential input. A Schmitt trigger is incorporated to add hysteresis which prevents noisy signals from corrupting the phase detector.

Professional Interface

The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110Ω ± 20% impedance. (The XLR connector on the receiver should have female pins with a male shell.) Since the receiver has a very high impedance, a 110Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in Figure A2, and, since the part has internal biasing, no external biasing network is needed. If some isolation is desired without the use of transformers, a 0.01µF capacitor should be placed on the input of each pin (RXP and RXN) as shown in Figure A3. However, if transformers are not used, high frequency energy could be coupled between transmitter and receiver causing degradation in analog performance.

Although transformers are not required by AES they are strongly recommended. The EBU requires transformers. Figures A2 and A3 show an optional DC blocking capacitor on the transmission line. A 0.1 to 0.47µF ceramic capacitor may be used to block any DC voltage that is accidentally connected to the digital audio receiver. The use of this capacitor is an issue of robustness as the digital audio transmission line does not have a DC voltage component.

Grounding the shield of the cable is a tricky issue. In the configuration of systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could result when boxes with different ground potentials are connected. Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantagous to have the ground of two boxes held to the same potential, and the cable shield might be depended upon to make that electrical connection. Generally, it

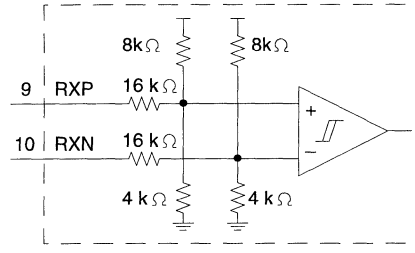


Figure A1. RS422 Receiver Internal Circuit

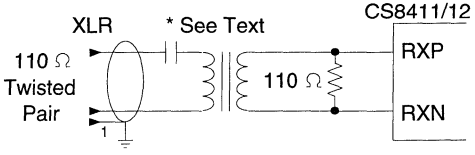


Figure A2. Professional Input Circuit

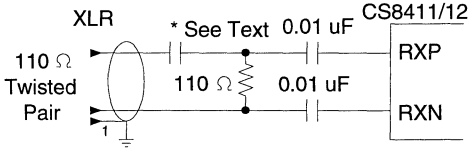


Figure A3. Transformerless Professional Circuit

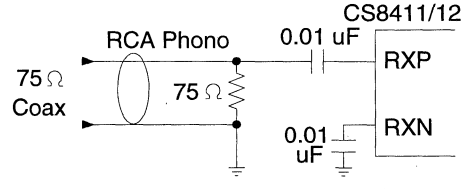


Figure A4. Consumer Input Circuit

may be a good idea to provide the option of grounding or capacitively coupling to ground with a "ground-lift" circuit.

Consumer Interface

In the case of the consumer interface, the standards call for an unbalanced circuit having a receiver impedance of 75Ω ±5%. The connector for the consumer interface is an RCA phono plug (fixed socket described in Table IV of IEC 268-11). The receiver circuit for the consumer interface is shown in Figure A4.

TTL/CMOS Levels

The circuit shown in Figure A5 may be used when external RS422 receivers or TTL/CMOS logic drive the CS8411/12 receiver section.

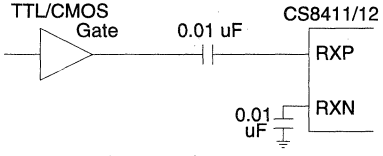


Figure A5. TTL/CMOS Interface

Transformers

The transformer used in the professional interface should be capable of operation from 1.5 to 7 MHz, which is the audio data rate of 25 kHz to 55 kHz after biphase-mark encoding. Transformers provide isolation from ground loop, 60 Hz noise, and common mode noise and interference. One of the important considerations when choosing transformers is minimizing shunt capacitance between primary and secondary windings. The higher the shunt capacitance, the lower the isolation between primary and secondary and the more coupling that can occur for high frequency energy. This energy appears in the form of common mode noise on the receive side ground and has the potential to degrade analog performance. Therefore, shielded transformers optimized for minimum primary to secondary capacitance may be desirable.

The following are a few typical transformers:

Pulse Engineering
Telecom Products Group
7250 Convoy Ct.
San Diego, CA 92111
(619) 268-2400
Part Number: PE65612

Schott Corporation
1000 Parkers Lane Rd.
Wayzata, MN 55391
(615) 889-8800
Part Number: 67125450
67128990 - lower cost
67129000 - surface mount
67129600 - single shield

Scientific Conversions Inc.
42 Truman Dr.
Novato, CA 94947
(415) 892-2323
Part Number: SC916-01 - single shield
SC916-01A - improved version
SC937-01 - low profile
SC937-02 - surface mount

ORDERING GUIDE

Model	Temperature Range	Package
CS8411-CP	0 to 70 °C*	28-Pin Plastic .6" DIP
CS8411-IP	-40 to 85 °C	28-Pin Plastic .6" DIP
CS8411-CS	0 to 70 °C*	28-Pin Plastic SOIC
CS8411-IS	-40 to 85 °C	28-Pin Plastic SOIC
CS8412-CP	0 to 70 °C*	28-Pin Plastic .6" DIP
CS8412-IP	-40 to 85 °C	28-Pin Plastic .6" DIP
CS8412-CS	0 to 70 °C*	28-Pin Plastic SOIC
CS8412-IS	-40 to 85 °C	28-Pin Plastic SOIC

* Although the '-CP' and '-CS' suffixed parts are guaranteed to operate over 0 to 70 °C, they are tested at 25 °C only. If testing over temperature is desired, the '-IP' and '-IS' suffixed parts are tested over their specified temperature range.

TABLE OF CONTENTS:

Semiconductor Corporation

CS8425

A-LAN - Audio Local Area Network Transceiver

Features

- Monolithic Digital Audio Transceiver for Point-to-Point Transmission of Audio Data
- Supports D2B OPTICAL
- User Channel Used for Communication of System Messages Between Nodes
- Configurable Interface Port Supports SPI, I^2C Bus®, Parallel Interface, or the CS8425 Operates as Stand-alone Unit
- Supports Large Number of Nodes per Network
- Also Applicable as General Purpose IEC-958 Digital Audio Transceiver

General Description

The A-LAN chip is a monolithic CMOS circuit that implements the physical layer of an Audio Local Area Network. The A-LAN allows numerous pieces of audio equipment such as CD players, digital equalizers, digital tape decks, DACs, amps, etc. to be connected in a ring topology, sharing audio data from a designated source. Control and configuration messages are passed between nodes via a unique application of the user channel.

Audio data is transmitted using the format specified by IEC-958, and can be generated by any one of multiple nodes on the A-LAN. External drivers and receivers are required for interface to the transmission media.

ORDERING INFORMATION

CS8425-CL,	0°C to 70°C	44-pin PLCC
CS8425-IL,	-40°C to 85°C	44-pin PLCC

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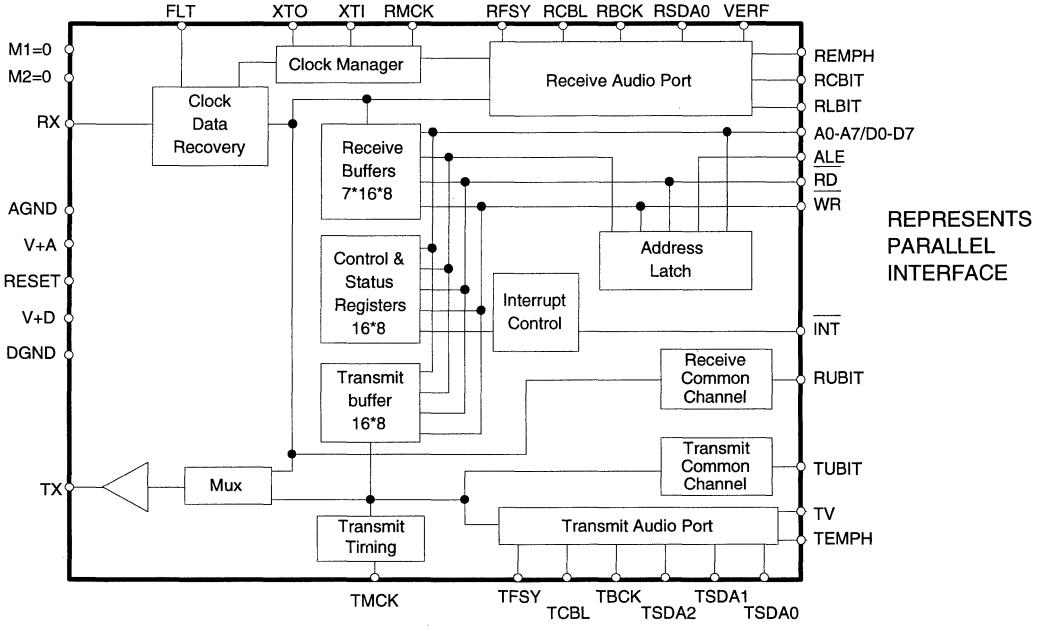


Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		VA+, VD+	0	6.0	V
Input Current, Any Pin Except Supply	Note 1	I_{IN}		±10	mA
Input Voltage, All Pins		V_{IN}	-0.3	VD+ + 0.3	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient Currents of up to 100mA will not cause SCR latch-up.

WARNING: Operating the part beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(GND = 0V; all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		VD+, VA+	4.5	5.0	5.5	V
Supply Current	VA+ VD+	I_A I_D		20 12	35 18	mA mA
Ambient Operating Temperature	CS8425-CL CS8425-IL	T_A	0 -40		70 85	°C
Power Consumption	Note 2			160	292	mW

Notes: 2. Power consumption is measured with inputs at VD+ or GND, and outputs floating.

DIGITAL CHARACTERISTICS

(T_A = 25°C for '-CL' suffix; T_A = -40°C - 85°C for '-IL' suffix; VD+, VA+ = 5V±10%)

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Except XTI)		V_{IH}	2.0			V
Low-Level Input Voltage	(Except XTI)		V_{IL}			0.8	V
High-Level Input Voltage	XTI		V_{IH}	.9VD+			V
Low-Level Input Voltage	XTI		V_{IL}			.1VD+	V
High-Level Output Voltage	(I_O = 200µA)	(Except XTO)	V_{OH}	VD+ -1.0			V
Low-Level Output Voltage	(I_O = -3.2mA)	(Except XTO)	V_{OL}			0.4	V
Input Leakage Current		(Except XTI & M1)	I_{in}		1.0	10	µA
Received Serial Data Sample Frequency			F_S	30		50	kHz
Master Clock Frequency, RMCK, TMCK*				6.4		21.120	MHz
RMCK Clock Jitter			tj		200		psRMS
RMCK Duty Cycle	Slave Modes Master Mode	Note 3		 30	50 50		% %
Crystal Oscillator Frequency			fOSC	9.60		21.12	MHz
$\overline{\text{RESET}}$ Low Time			tRST	200			ns

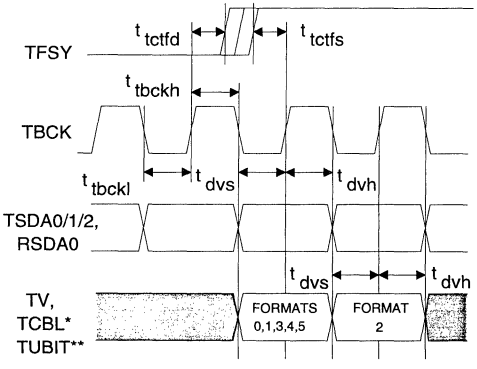
Notes: 3. RMCK is 33% duty cycle in master mode when the crystal is divided by 1.5. Otherwise, RMCK is 50% duty cycle.

SWITCHING CHARACTERISTICS - SERIAL AUDIO DATA PORTS

(T_A = 25°C for '-CL' suffix; T_A = -40°C - 85°C for '-IL' suffix; VD+, VA+ = 5V±10%;
Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 20pF)

Parameter		Symbol	Min	Typ	Max	Units
Bit Clock Frequency, TBCK, RBCK	Note 4	f_{bck}		64FS	15	MHz
TBCK Pulse Width Low		t_{tbckl}	30			ns
TBCK Pulse Width High		t_{tbckh}	30			ns
TBCK Edge to TFSY Edge Delay	Note 5	t_{tctfd}	20			ns
TBCK Edge to TFSY Edge Setup	Note 5	t_{tctfs}	20			ns
TSDA0/1/2, TCBL, TV Valid to TBCK Edge Setup	Note 5, 6	t_{dvs}	20			ns
TSDA0/1/2, TCBL, TV Valid to TBCK Edge Hold	Note 5, 6	t_{dvh}	20			ns
RBCK Edge to RFSY & VERF Edge	Note 5	t_{rcrf}	-20		20	ns
RBCK Edge to RCBL Rising	Note 5	t_{rcrcbr}	-20		20	ns
RSDA0 & TSDA2 Valid to RBCK Edge Setup	Note 5, 7	t_{rdrcs}	20			ns
RSDA0 & TSDA2 Valid to RBCK Edge Hold	Note 5, 7	t_{rdrch}	20			ns
RCBIT, RLBIT, RUBIT, RSF0 & RSF1 Setup to RFSY Edge Setup	Note 5, 8	t_{csrfs}	200			ns

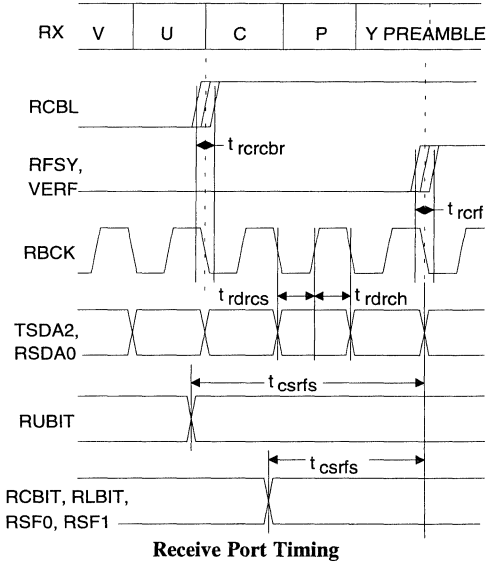
Notes:
4. There can be 16, 24, or 32 TBCK cycles per sample. Typ value assumes 32 TBCK cycles per sample.
5. The "Edge" of TBCK, RBCK, TFSY & RFSY refers to the active edge of these signals which is determined by the selected serial data format.
6. TCBIT and TLBIT are available as dedicated pins in the stand-alone configuration.
7. TSDA2 is a receive data output in receive format 5 only.
8. RUBIT will transition a bit period before RCBIT, RLBIT, RSF0, and RSF1.



* TCBL is sampled along with TV in Format 1, and half as much in all other formats

**TUBIT sampled here in General Purpose modes only

Transmit Port Timing

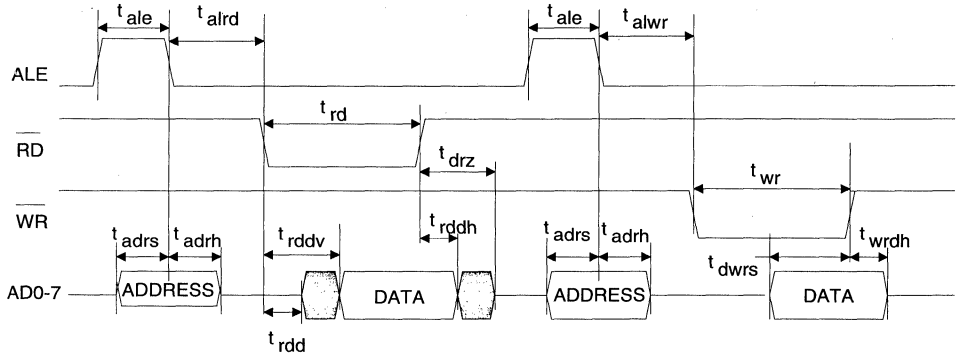


Receive Port Timing

SWITCHING CHARACTERISTICS - PARALLEL PORT

(T_A = 25°C for '-CL' suffix; T_A = -40°C - 85°C for '-IL' suffix; VD+, VA+ = 5V±10%;
Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Max	Units
ALE High	t_{ale}	40		ns
Address Valid to ALE Falling Setup	t_{adrs}	20		ns
ALE Falling to Address Hold	t_{adrh}	20		ns
ALE Falling to $\overline{RD}$ Falling	t_{alrd}	40		ns
$\overline{RD}$ Low	trd	80		ns
$\overline{RD}$ Falling to AD0-7 Driven	t_{rdd}	0		ns
$\overline{RD}$ Falling to AD0-7 Valid	t_{rddv}		80	ns
$\overline{RD}$ Rising to AD0-7 Hold	t_{rddh}	5		ns
$\overline{RD}$ Rising to AD0-7 Hi-Z	t_{rdz}		20	ns
ALE Falling to $\overline{WR}$ Falling	t_{alwr}	40		ns
$\overline{WR}$ Low	t_{wr}	80		ns
AD0-7 Valid to $\overline{WR}$ Rising Setup	t_{dwrs}	80		ns



SWITCHING CHARACTERISTICS - SERIAL PERIPHERAL PORTS

(T_A = 25°C for '-CL' suffix; T_A = -40°C - 85°C for '-IL' suffix; VD+, VA+ = 5V±10%;
Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 20pF)

Parameter		Symbol	Min	Max	Units
SPI Mode (I^2C/SPI = 1)					
SCK Clock Frequency		f_{sck}	0	100	kHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
$\overline{CS}$ Falling to SCK Edge		t_{css}	20		ns
SCK Low Time		t_{scl}	1.1		µs
SCK High TIme		t_{sch}	1.1		µs
SDI and SDO to SCK Rising Setup Time		t_{dsu}	250		ns
SCK Rising to DATA Hold Time	SDI (Note 9)	t_{dh}	50		ns
SCK Falling to DATA Invalid	SDO	t_{scdv}	300		ns
Rise Time of Both SDI and SCK Lines		t_r		1	µs
Fall Time of Both SDI and SCK Lines		t_f		300	ns

Notes: 9. Data must be held for sufficient time to bridge the transition time of SCK.

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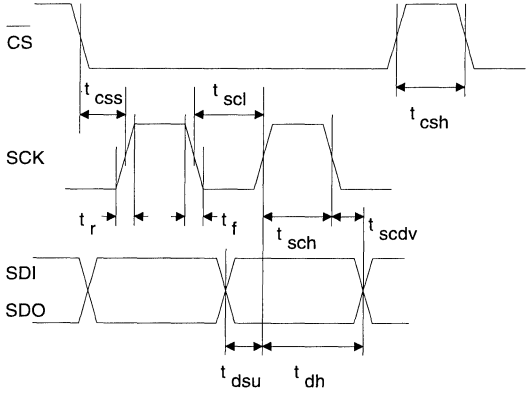
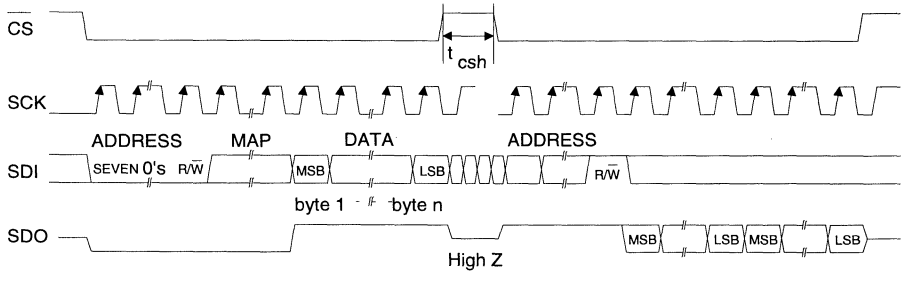


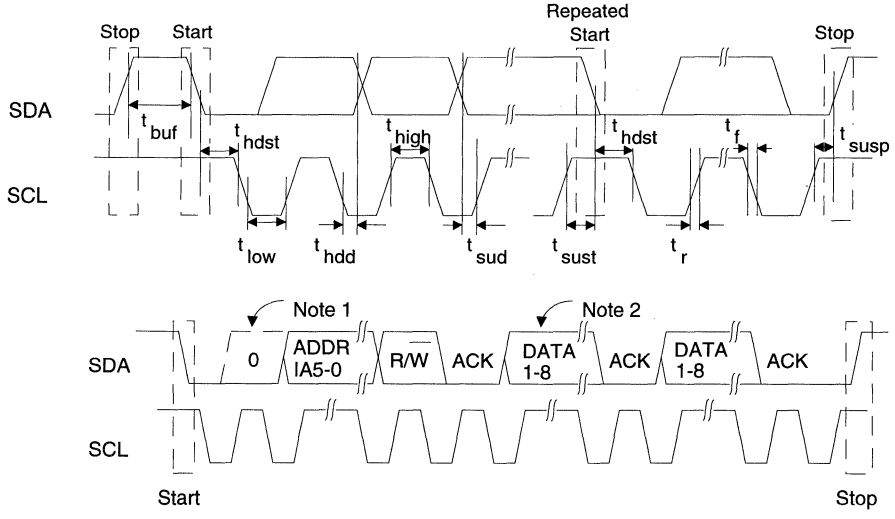


SWITCHING CHARACTERISTICS - SERIAL PERIPHERAL PORTS

(T_A = 25°C for '-CL' suffix; T_A = -40°C - 85°C for '-IL' suffix; VD+, VA+ = 5V±10%;
Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 20pF)

Parameter	Symbol	Min	Max	Units
I^2C Mode (I^2C/SPI = 0)				
SCL Clock Frequency	f_{scl}	0	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0		µs
Clock Low Time	t_{low}	4.7		µs
Clock High TIme	t_{high}	4.0		µs
Setup Time for Repeated Start Condition	t_{sust}	4.7		µs
SDA Hold Time from SCL Falling Note 9	t_{hdd}	0		µs
SDA Setup Time to SCL Rising	t_{sud}	250		ns
Rise Time of Both SDA and SCL Lines	t_r		1	µs
Fall Time of Both SDA and SCL Lines	t_f		300	ns
Setup Time for Stop Condition	t_{susp}	4.7		µs

Notes: 9. Data must be held for sufficient time to bridge the 300ns transition time of SCL.



Note 1: The first address bit for the CS8425 must be a zero.

Note 2: If operation is a write, this byte contains the Memory Address Pointer, MAP.

FUNCTIONAL DESCRIPTION

Introduction

The CS8425 is a monolithic, CMOS, digital audio data transceiver which implements the physical layer of an Audio-Local Area Network, A-LAN. The CS8425 can also be applied as a general-purpose transceiver. In A-LAN applications, several CS8425s can be connected in a ring or multi-ring topology of point-to-point IEC-958 links. The digital audio data is transmitted and received through TTL compatible buffers. The transmission media can be optical, co-ax or twisted pair cable.

Audio data can be generated from any one of multiple nodes on the ring, and passed from node to node. The U (user) channel is time division multiplexed into nine channels and used for message passing of control information between nodes. Message passing is not required of all nodes.

The CS8425 can be set to operate as a master, slave, slave processor, or as a stand-alone unit. An A-LAN must have one master node to establish the network timing, and set the frame and block structures. The remaining nodes slave their timing to the master. A master or a slave processor can source, alter, or pass along audio data. A slave node passes audio data unaltered, operating as a monitor for an audio data destination such as an amplifier. As a stand-alone unit, the CS8425 can be set to be a master, slave or slave-processor, but has limited message passing capabilities.

The CS8425 supports several different interface configurations for controlling the device. There are three peripheral configurations: Intel compatible parallel port, I^2C serial port, and SPI serial port. In the peripheral configurations, device operation is determined through internal registers. There are also stand-alone configurations in which the CS8425 is controlled by dedicated pins.

In addition, there are two operational modes for the CS8425 in which it functions as a general-purpose stand-alone transceiver. In one mode, transmit timing is independent of receive timing; in the other mode, transmit timing is slaved to the receive timing. Message passing is not supported in the general-purpose modes.

Ring Topology

The orientation of nodes performing different functions on the ring should be considered in a ring design. An important consideration in ring topology is the functionality of the master. Since the master generates the ring timing, its ability to pass audio data from its receive input to transmit output is compromised. The optimal configuration would have a master followed by slave processors which are then followed by slave nodes. Such a configuration would allow any of the slave processors or the master to serve as an audio data source, and not require the master to pass audio data through.

For the example shown in Figure 1, the CD player is the master. The signal processor could

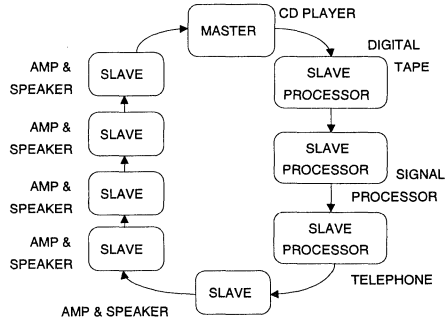


Figure 1 - Example of Audio LAN Topology

Supply of the CS8425 for use in a D2B application does not convey any license whatsoever, nor imply a right under any patent.

be a digital graphic equalizer which regenerates audio data. If the Digital Tape player becomes the audio data source, that node could reconfigure as the master and the CD player would become a slave. Alternatively the tape player could slave its timing to the master CD player, and input its audio data on to the ring.

Figure 2 shows a block diagram of a node that could be used as a master or a slave processor. The example shown operates in conjunction with a microcontroller. A slave node would have only

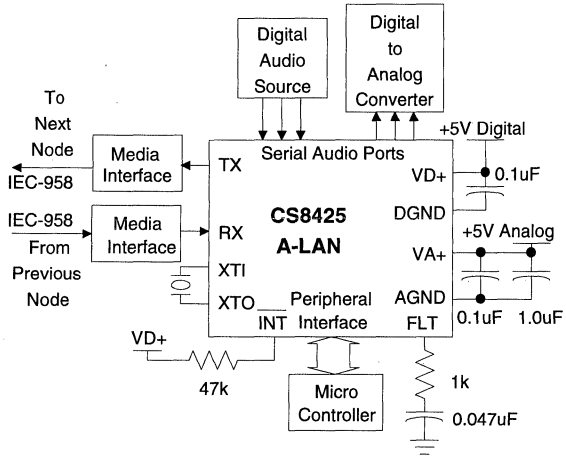


Figure 2 - Block Diagram of Typical Node

the DAC functionality.

Clocks

The clock frequency for the entire ring is always established by the master. The master's clock source can be either the on chip crystal oscillator or an external clock input to the TMCK pin. If a 384Fs crystal is used, RMCK and TMCK can be connected together. In the slave or slave processor modes, the transmit clock is always derived from the recovered clock, and TMCK is ignored.

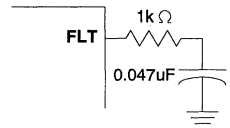


Figure 3 - PLL Filter

The recovered clock is derived from the incoming data stream by an on-chip PLL. An external loop filter of 1kΩ and .047µF to ground is required as shown in Figure 3. When no signal is applied to RX, the VCO will be pulled to its minimum frequency.

In peripheral configurations, numerous clock dividers are available to provide a variety of possible frequencies at the RMCK output. These dividers are controlled by FR0 and FR1 of Control Register 0 as shown in Table 1. The frequencies at RMCK and TMCK can be 128,

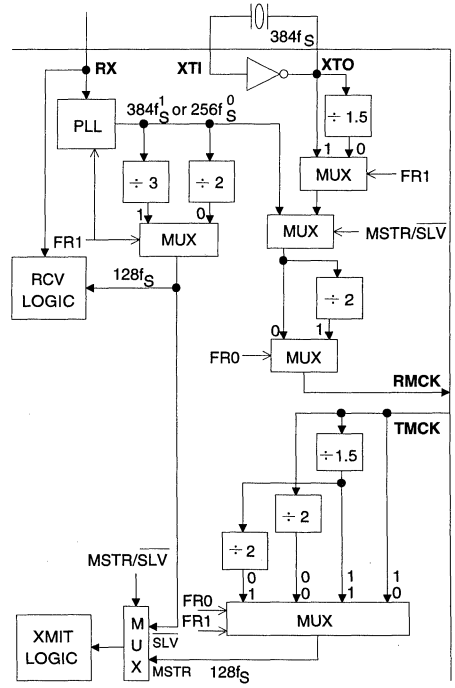


Figure 4 - Internal Clock Routing and Divide Circuitry

192, 256, or 384 times the audio sample rate. Alternatively, the TMCK input can be connected directly to the XTO pin. FR0 and FR1 affect the clock dividers immediately after being set. Changing dividers may cause momentary glitches on RMCK and TX.

FR0	FR1	Frequency
0	1	384Fs
0	0	256Fs
1	1	192Fs
1	0	128Fs

Table 1 - Master Clock Settings for Peripheral Configurations

Figure 4 shows the internal clock routing and divide structure. In stand-alone configurations, the clock dividers are set for RMCK of 256Fs, and TMCK is divided by two. The divide by 1.5 circuits will produce a 33% duty cycle. The internal transmit clock must always be 128Fs (this clock can be 33% duty cycle).

Serial Port Formats

The serial ports are for I/O of audio data. Each port consists of a frame sync, a bit clock and data signals. There are six serial port formats which select the relationship of the clock, data and frame sync signals input to and output from the CS8425. These formats are selected by setting TF0, TF1 and TF2 for the transmit side and RF0, RF1 and RF2 for the receive side. In stand-alone modes, the formats are selected via dedicated pins. In the peripheral modes, the formats are selected via the Serial Port Control register.

TRANSMIT SERIAL PORT

The six input formats are shown in Figure 5. The frame sync input, TFSY, separates the audio data words, and can specify left and right samples. The selected format determines the edge on which the bit clock, TBCK, latches data into the part. In peripheral configurations, data may be input through three pins, TSDA0, TSDA1, and TSDA2. In formats 0 through 4, stereo audio data is read through one pin, as specified by the Source Switch Control, SSC, register. In stand-alone configurations, data is always read through TSDA0. In format 5, 16 bit stereo data is read through one pin, and 16 bit mono data is read through TSDA1. These three 16 bit channels are multiplexed into the two 24 bit channels of the SPDIF as shown in Figure 6.

The number of TBCKs between TFSY edges can be 16, 24, or 32. The device counts these clock cycles and configures itself accordingly. Any time the number of clocks changes between samples, an incorrect audio sample may be transmitted, but the chip will adapt to the new clock count. Eighteen or twenty bit data can be input in Formats 0, 1, and 2, using either 24 or 32 TBCKs (24 bits of audio data are input in the 24 and 32 TBCK modes). The trailing bits should be input as zeros.

A frame of audio data is input to a shift register as shown in Figure 7. An internally generated "latch" signal transfers the audio data to a temporary register. Then an internal "load" signal loads the data into another shift register from which data is clocked to the biphase encoder and transmitted. Load (determined by internal transmit timing) and latch (determined by TFSY) must not be coincident. Timing is shown in Figure 8.

The validity bit can be entered on a per sample basis through pin TV. TV is sampled after either edge of TFSY in all formats except format 1 where it is sampled after the rising edge only. In all formats except format 2, TV is sampled ½ TBCK samples after the edge of TFSY. In format 2, TV is sampled 1½ TBCK samples after the TFSY edge. TV for a channel is sampled along with the audio data being input through the serial port at the same time.

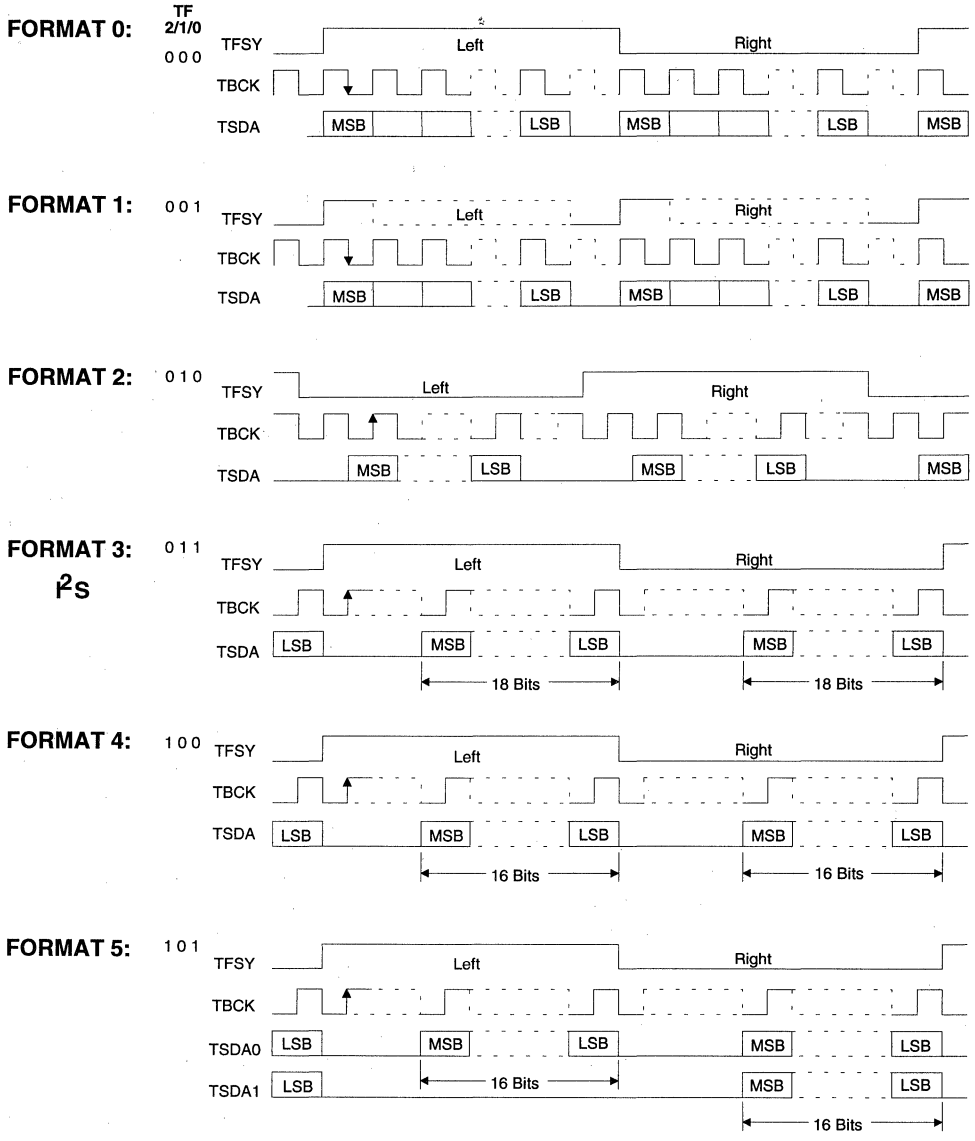


Figure 5 - Input Formats for Transmit Data

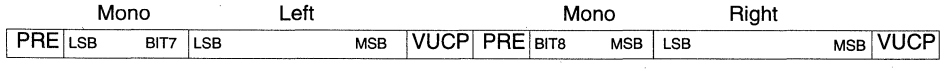


Figure 6 - Data Channel Configuration for Three Channel Operation

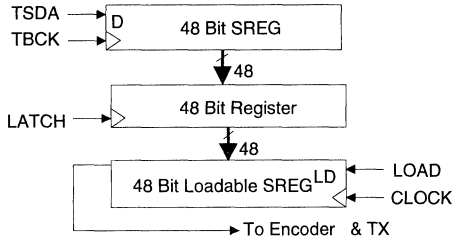


Figure 7 - Transmit Input Registers

The channel status block timing can be altered without affecting the frame and subframe timing. TCBL is sampled, along with TV, just after the rising edge of TFSY in all formats (falling edge in format 2). Input format 1 does not specify which channel is left or right. The first channel input after a low to high transition of TCBL is the left channel. In format 1, the CS8425 will not exit reset until a change on TCBL is detected. Block timing is established by a low to high transition of TCBL (on successive samples). Once block timing is established, TCBL can remain in either logic state.

RECEIVE SERIAL PORT

The receive serial port consists of a frame sync, RFSY, a bit clock, RBCK, and data outputs. The desired format is selected by setting RF0, RF1, and RF2. In stand-alone configurations the RF0/1/2 are dedicated pins; in the peripheral mode, RF0/1/2 are control register bits. The relationships between RFSY, RBCK and output data are shown in Figure 9. Formats 0 - 4 are stereo formats with stereo data output on pin RSDA0. Format 5 is a three channel format with stereo data output on pin RSDA0, and mono data output on pin TSDA2. All 24 bits of audio data are output in formats 0, 1, and 2.

The receive port has 24 bit shift registers for reversing the order of the received audio data. Consequently, there is one subframe of delay

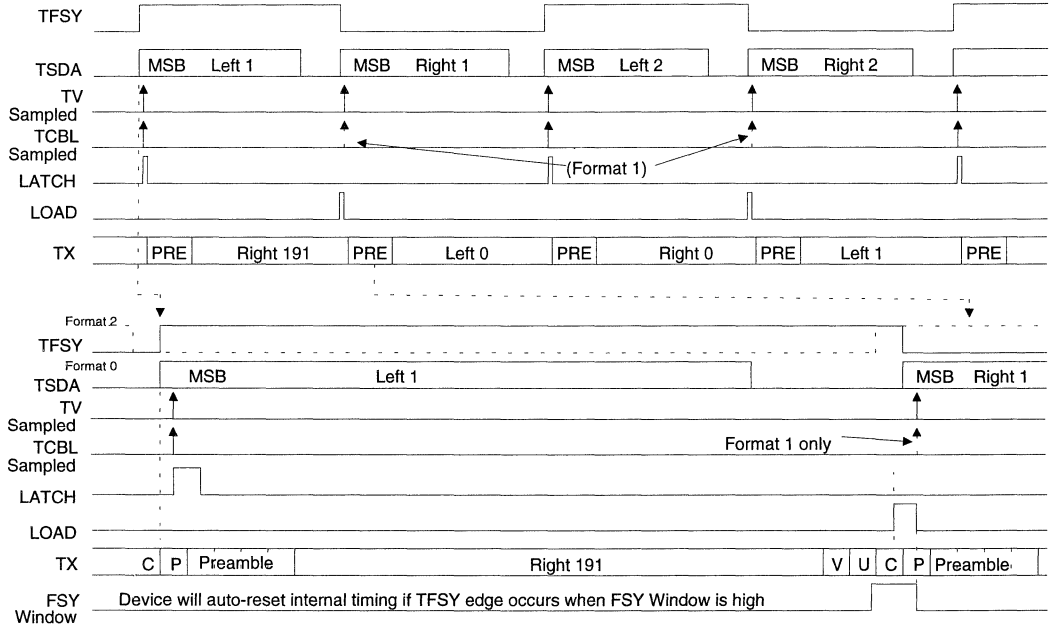


Figure 8 - Detailed Transmitter Timing Information

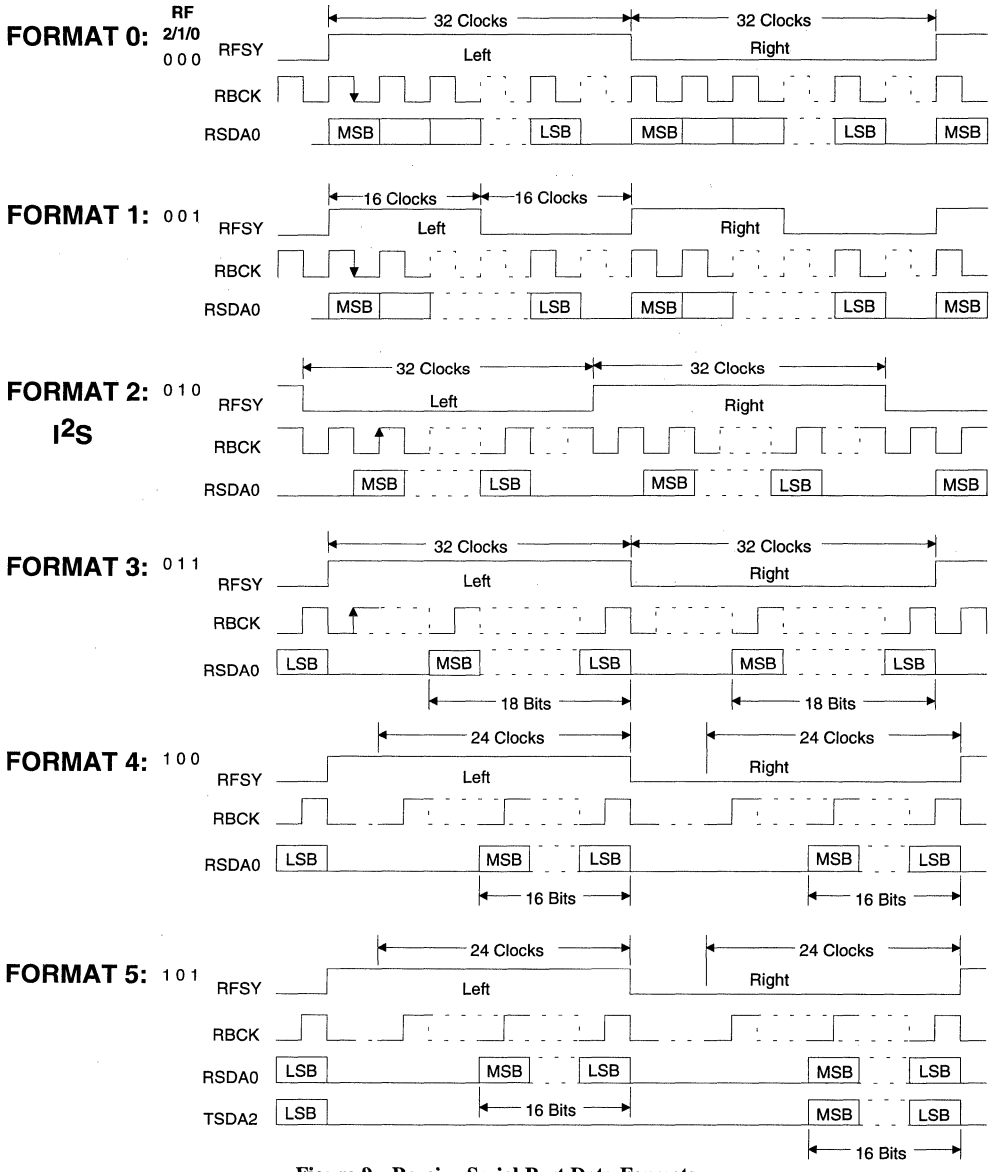


Figure 9 - Receive Serial Port Data Formats

through the receive serial port. In all formats, RFSY changes one bit period after the start of a preamble on RX.

In slave mode, received audio data is always retransmitted. The transmitted data signal is delayed 2.5 biphase bit periods relative to the received audio data as shown in Figure 10.

A slave processor node can retransmit audio data if the received audio data is sent back to the transmit port. The timing for a slave processor with the receive serial port driving the transmit serial port is shown in Figure 11. The frame and block structure of the IEC-958 data is delayed 2.5 biphase bit periods and the audio data is delayed an additional two frames. The bit clock and frame sync can be internally looped back by setting the Source Switch Control register appropriately.

In some cases, it may be required to pass data through a master. This can be done by first establishing ring timing, then switching the transmit serial port inputs from external signals to the receive serial port outputs. One audio sample may be corrupted when the switch is made. Configuring a master to pass through received data is risky and generally not recommended. The ring clock source is no longer controlled, and should ring timing be interrupted for any reason, the ring will not resync without reconfiguration of the master.

The RCBL output identifies block boundaries of the received data. RCBL transitions high three RBCK cycles before the RFSY edge that identi-

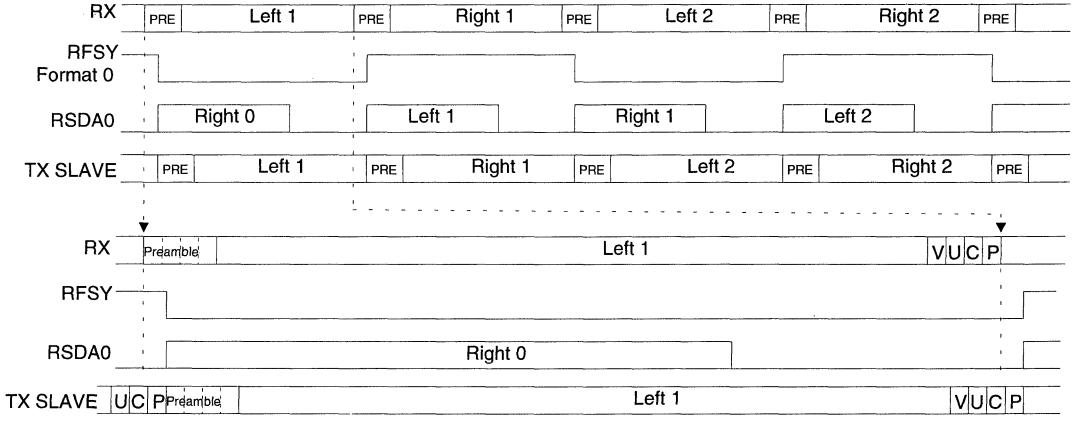


Figure 10 - Slave Mode Receive to Transmit Timing

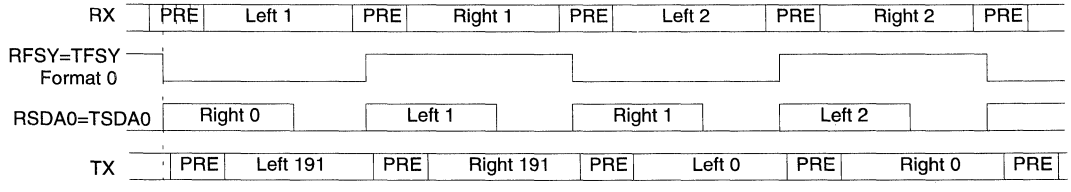


Figure 11 - Slave Processor Timing with Receive Serial Port Driving Transmit Serial Port

fies the first audio sample of a block. RCBL remains high for 32 frames, and is then low for 160 frames. RCBL remains low when the receiver is not locked.

The pin VERF can output the received validity bit and identify errored audio samples. In stand-alone configurations, VERF is high if the receiver is not in lock, a parity or line coding error is detected, or the received validity bit is high. In peripheral configurations, the Status Register Enable/Mask register determines which conditions affect VERF. Transitions on VERF occur coincident with the edges of RFSY that identify the start of the errored audio sample. When the device is in the master or slave processor modes and it is configured to retransmit received audio data, VERF can be connected to TV to properly retransmit the validity bit.

Device Configurations

The CS8425 can be set to interface as a peripheral, operate as a stand-alone unit, or function as a general-purpose transceiver. The configuration is set by the mode pins, M1 and M2 as shown in Table 2.

M1	M2	Mode	Configurations
0	0	1	Peripheral - Parallel Port
0	1	2	Peripheral - I^2C/SPI Bus
1	0	3	Stand-alone - Master
1	1	4	Stand-alone - Slave/Slave Pro
float	0	5	General-Purpose 0, GP0
float	1	6	General-Purpose 1, GP1

Table 2 - Operating Modes

Peripheral Configurations

As a peripheral, internal buffer memory allows the device to send and receive messages, and 16 control and status registers allow flexible management of the device and the network. Modes 1 and 2 allow selection of three different CS8425 configurations for interface with peripheral processors: parallel interface, I^2C and SPI. Figure 12 shows a block diagram and the different peripheral interfaces.

PARALLEL INTERFACE

Selecting mode 1 (pins M1/M2 = 0/0) configures the part for parallel interface. The parallel port consists of an eight bit multiplexed address/data bus, AD0-AD7, an address latch enable, ALE, a read signal, $\overline{RD}$, and a write signal, $\overline{WR}$. An address present on AD0 - AD7 will be latched into the part on the falling edge of ALE. The addressed register is read by setting $\overline{RD}$ low. The bus will be tristated shortly after $\overline{RD}$ goes high. A register is written by setting $\overline{WR}$ low.

SERIAL INTERFACES

Mode 2 (pins M1/M2 = 0/1) configures the part for serial interface. Either I^2C or SPI interface is selected by the $I^2\overline{C}$/SPI pin. When transmitting data to the transceiver in either serial interface format, the first byte after the slave address is written to the memory address pointer, MAP. Successive bytes are written to the address in MAP. If CR1.3, INC, is set, the MAP will automatically increment after each memory access, thus allowing blocks of data to be efficiently accessed. If a read operation is specified, successive bytes are read from the address in MAP. Unless the proper address resides in MAP, a write operation must precede a read.

I^2C Interface

The I^2C interface is selected by setting the $I^2\overline{C}$/SPI pin low. This interface consists of a serial clock, SCL, serial data, SDA, and five node address pins, IA0 - IA3, IA5. IA4 is set to zero, and the MSB of the address is internally set to zero. The CS8425 is configured as a slave, and has an eight bit memory address pointer, MAP, which must be loaded prior to memory access.

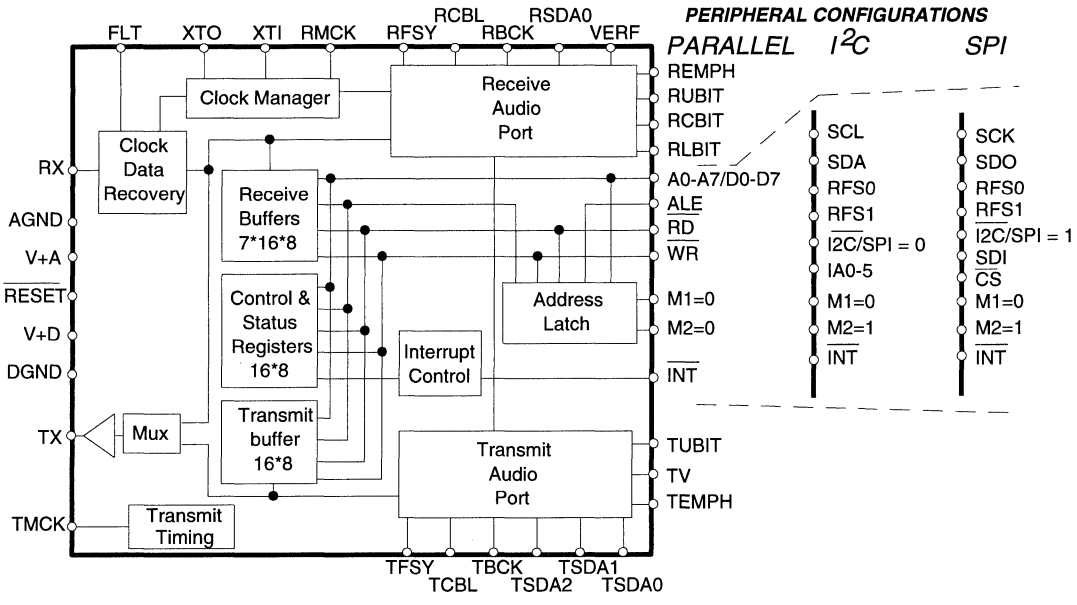


Figure 12 - Block Diagram Showing the Three Peripheral Interfaces

SPI Interface

The SPI interface is selected by setting the $\overline{I^2C}$/SPI pin high. The SPI interface consists of a chip select, $\overline{CS}$, a clock, SCK, a serial data in, SDIN, and a serial data out, SDOUT. Data is transferred in a SPI system by swapping the contents of eight bit shift registers in two devices. Each of two devices has an eight bit shift register. The output of each shift register is connected to the input of the other part's shift register. Both registers share a common clock. After eight clock pulses, the contents of both registers have been switched.

Chip select initiates a transfer. The eighth bit of the first byte transferred to the CS8425 after $\overline{CS}$ goes low specifies whether the operation is a read or write; zero for a write, one for a read. The data transfer is terminated by setting $\overline{CS}$ high.

Stand-Alone Modes

The stand-alone device configuration is shown in Figure 13. In Mode 3 (pins M1/M2 = 1/0), the device operates as a stand-alone master. In mode 4 (pins M1/M2 = 1/1), TSDA1, pin 3, determines whether the CS8425 will operate in slave mode (TSDA1 high), or slave-processor mode (TSDA1 low). If serial port Format 5 is selected, the circuit operates as a slave-processor. In the stand-alone modes, the internal registers are not accessible and message passing capabilities are limited. The common message channel can still be accessed through the RUBIT and TUBIT pins.

In stand-alone modes, the CS8425 is controlled by dedicated pins. Transmit and Receive data formats are set by TF0, TF1 and TF2, and RF0, RF1 and RF2 respectively. RMCK is set for 256Fs in the stand-alone configuration.

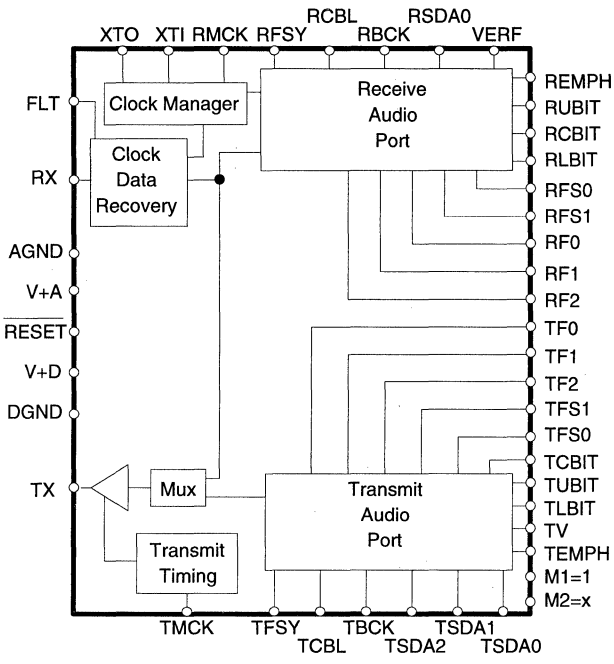


Figure 13 - Block Diagram and Interface for Stand-alone Mode

Channel Status bits for the sample frequency are input and output through dedicated pins. For a master, TFS0 and TFS1 are used to input the CS sample frequency bits 24 and 25 (byte 3). Similarly, RSF0 and RFS1 output the received CS sample frequency bits. As in other modes, TCBIT/RCBIT and TLBIT/RLBIT are for input/output of the copy and generation bits.

General-Purpose Modes

In the general-purpose modes the CS8425 functions as a stand-alone transceiver. There are two stand-alone general-purpose modes which are selected by floating the M1 pin (connecting a capacitor between M1 and ground will prevent spurious signals from coupling into the M1 input), and using the M2 pin to select the desired mode. When M2 is low (0), the transmit and receive sections are independent. When M2 is high (1), the transmitter derives its timing from the receiver.

Alternatively, the CS8425 can be set for general-purpose operation while in a peripheral configuration by setting MS0 and MS1, CR0.4 and CR0.5 to 1,1. When general-purpose operation is selected while in peripheral configuration, BYPS, CR0.6, determines the transmit clock source. When BYPS is set to 0, the recovered clock is output through RMCK and the transmitter is driven by TMCK. When BYPS is set to 1, transmitter timing is slaved to receive timing, and TMCK is ignored.

The U Channel in General-Purpose Modes

In the general-purpose modes, the message passing capability is disabled. The TUBIT pin is used to input all U bits,

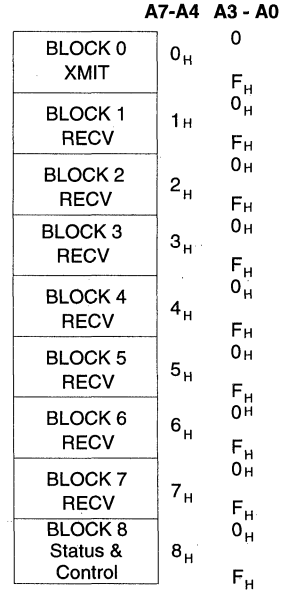


Figure 14 - Internal Memory Blocks

and all received U bits are output from RUBIT. User data entered on TUBIT is sampled ½ TBCK cycle after the active edges of TFSY (1½ TBCK cycles for format 2), and transmitted with the audio data that is being input when TUBIT is sampled. The received RUBIT is buffered and output along with its accompanying audio data. RUBIT is updated two RBCK cycles before the edges of RFSY.

Internal Buffers

Internal memory is divided into nine blocks of 16 bytes as shown in Figure 14. The first eight blocks are used for message passing, and the ninth block contains status and control registers. These eight memory blocks are made with dual-port RAM and can be simultaneously accessed internally and externally. In serial port modes, bit 7 is written first, bit 0 is last.

The contents of the 16 status and control registers is illustrated in Figure 15. The first four registers are status registers, and the following 12 are control registers. Power on and hardware reset will clear all registers. $\overline{RST}$, CR0.0, must be set high after power on or hardware reset. All unused registers (indicated by "X" in Figure 15) should be set to zero.

Events associated with the Status Register and the Buffer Full register can generate interrupts if the corresponding bit in the Status Register Enable/Mask and Buffer Full Enable registers are set. When an interrupt is generated, the $\overline{INT}$ pin pulses low for four 64Fs clock periods. The

	7	6	5	4	3	2	1	0	ADDRESS	
Status Register (SR)	V	ERR	LOCK	X	VERF	TBLK	REJ	RCV	80_H	RD Only
Buffer Full (BF)	7	6	5	4	3	2	1	0	81_H	RD Only
Received Channel Status 0 (RCS0)	CS25	CS24	X	CS4	CS3	CS2	CS1	CS0	82_H	RD Only
Received Channel Status 1 (RCS1)	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8	83_H	RD Only
Status Register Enable/Mask (SRE/M)	7_M	6_M	5_M	X	3_E	2_E	1_E	0_E	84_H	RD/WR
Buffer Full Enable (BFE)	7	6	5	4	3	2	1	0	85_H	RD/WR
Transmit Channel Status 0 (TCS0)	CS25	CS24	X	CS4	CS3	CS2	CS1	X	86_H	RD/WR
Transmit Channel Status 1 (TCS1)	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8	87_H	RD/WR
Control Register 0 (CR0)	CCEN	BYPS	MS1	MS0	FR1	FR0	OE	$\overline{RST}$	88_H	RD/WR
Overwrite Protect Mask (OPM)	7	6	5	4	3	2	1	X	89_H	RD/WR
Serial Port Control (SPC)	X	RF2	RF1	RF0	X	TF2	TF1	TF0	$8A_H$	RD/WR
Source Switch Control (SSC)	X	X	X	Q4	Q3	Q2	Q1	Q0	$8B_H$	RD/WR
Address Register (ADR)	X	X	GA1	GA0	X	NA2	NA1	NA0	$8C_H$	RD/WR
Transmit Target Address (TTA)	X	X	5	4	3	2	1	0	$8D_H$	RD/WR
Transmit Message Length (TML)	X	X	X	X	3	2	1	0	$8E_H$	RD/WR
Control Register 1 (CR1)	TSTP	LOOP	TST1	CLRU	INC	TCBL	TV	$\overline{MUT}$	$8F_H$	RD/WR

Figure 15 - Memory Block 8, Control and Status Registers

BLOCK 8, Status & Control Registers

Status Register (SR)

7	6	5	4	3	2	1	0
V	ERR	LOCK	x	VERF	TBLK	REF	RCV

V — Indicates received validity bit. If SRE/M.5 = 0, VERF will go high and issue an interrupt (if enabled). V is cleared when the SR is read.

ERR — Indicates parity or line coding error. If SRE/M.6 = 0, VERF will go high and issue an interrupt (if enabled). ERR is cleared when the SR is read.

LOCK — Indicates loss of lock. If SRE/M.5 = 0, VERF will go high and issue an interrupt (if enabled). LOCK is cleared when the SR is read (unless the loss of lock condition persists).

VERF — VERF can signal loss of lock, receive errors, and/or the received validity bit. An interrupt will be generated if enabled by setting SRE/M.3 = 1. VERF is cleared when the SR is read.

TBLK — Transmit Block - TBLK is low while the first four bytes of Channel Status are being transmitted. If enabled by SRE/M.2 = 1, an interrupt will be generated on the rising edge of TBLK.

REJ — Reject - Goes high if the returned acknowledge bit of a transmitted message is set. An interrupt will be issued if enabled by SRE/M.1 = 1. REJ is cleared when the SR is read.

RCV — Receiving - Goes high when a message is acknowledged. An interrupt will be generated if enabled by SRE/M.0 = 1. RCV goes low just after the last message bit is written to memory.

Note: ERR and V will remain high for the entire subframe that the errored data is being output from the receive serial port, regardless of read activity.

Buffer Full (BF)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

BF.1 - BF.7 — The bit corresponding to a particular channel is set high after an entire message is received and stored. An interrupt will be issued if the corresponding BFE.x bit is set.

BF.0 — High when CS8425 is in the process of sending a message. An interrupt will be issued after the last data byte of the message is sent if BFE.0 is high.

Received Channel Status 0 (RCS0)

7	6	5	4	3	2	1	0
CS25	CS24	x	CS4	CS3	CS2	CS1	CS0

CS.x — Received Channel Status bits.

Received Channel Status 1 (RCS1)

7	6	5	4	3	2	1	0
CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8

CS.x — Received Channel Status bits.

Status Register Enable/Mask (SRE/M)

7	6	5	4	3	2	1	0
7	6	5	x	3	2	1	0

SRE/M.5-7 — Mask - Correspond to Status Register bits 5, 6 &7. This register can be used to select the combination of LOCK, ERR, and V that cause VERF to be set (Both the pin and the register bit). Setting these bits high masks the error condition.

SRE/M.0-3 — Enable - Setting these bits high enables an interrupt when the corresponding Status Register bit goes high.

Buffer Full Enable (BFE)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

BFE.1-7 — When high, an interrupt will be issued when the corresponding Buffer Full bit goes high.

BFE.0 — When high, an interrupt will be issued when BF.0 goes low.

Transmit Channel Status 0 (TCS0)

7	6	5	4	3	2	1	0
CS25	CS24	x	CS4	CS3	CS2	CS1	x

CS.x These Channel Status bits are transmitted in their proper CS bit position.

Transmit Channel Status 1 (TCS1)

7	6	5	4	3	2	1	0
CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8

CS.x These Channel Status bits are transmitted in their proper CS bit position.

Control Register 0 (CR0)

7	6	5	4	3	2	1	0
CCEN	BYPS	MS1	MS0	FR1	FR0	OE	$\overline{RST}$

CCEN Common Channel Clock Enable
When in A-LAN modes, setting CCEN high enables a common channel clock output from TSDA2. Data changes while this clock is low.
In General-Purpose modes, when CCEN is high, TSDA1 & TSDA2 are used for inputting and outputting Channel Status data, respectively. If CCEN is low, TSDA2 can be used for a serial port.

BYPS Bypass
As a MASTER, Channel Status is read from TCS0 & TCS1 registers when BYPS is low, and is passed through when BYPS is high. Channel Status for the left channel only will be delayed by one block when passed through a master.
As a SLAVE or SLAVE PROCESSOR, Channel Status is generated when BYPS is high and passed through when BYPS is low.
In GENERAL-PURPOSE modes, General-Purpose mode 0, GP0, is selected when BYPS is low and GP1 is selected when BYPS is high.

MS0, MS1 Mode Selection

MS0	MS1	MODE
0	0	Slave
0	1	Slave Processor
1	0	Master
1	1	General Purpose

FR0, FR1 Frequency Selection. See Figure 4.

FR0	FR1	FREQUENCY
0	0	256Fs
0	1	384Fs
1	0	128Fs
1	1	192Fs

OE Output Enable - The transmitter output, TX, is held low when OE is low.

$\overline{RST}$ Reset - Setting $\overline{RST}$ low resets the internal logic of the part. The registers will remain unchanged.

Overwrite Protect Mask (OPM)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	x

OPM.1 - 7 When high, incoming messages on the corresponding message channel are rejected if the corresponding buffer is full.

Serial Port Control (SPC)

7	6	5	4	3	2	1	0
x	RF2	RF1	RF0	x	TF2	TF1	TF0

RF0-2 Receive Serial Data Format Selection See Figure 9.

TF0-2 Transmit Serial Data Format Selection See Figure 5.

Source Switch Control (SSC)

7	6	5	4	3	2	1	0
x	x	x	Q4	Q3	Q2	Q1	Q0

Q0 - Q4 Set muxes which control the routing of signals between the receive and transmit serial ports. See Figure 16.

Address Register (ADR)

7	6	5	4	3	2	1	0
x	x	GA1	GA0	x	NA2	NA1	NA0

GA0,1 Group Addresses 1 - 3

NA0-2 Node Addresses 0 - 7

6

Transmit Target Address (TTA)

7	6	5	4	3	2	1	0
x	x	5	4	3	2	1	0

TTA.0 - 5 Target address for message to be transmitted.

TTA .5	.4	.3	.2	.1	.0	NA
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7
						Group Calls
0	0	1	1	1	1	All Nodes
0	1	x	x	x	x	Group 1
1	0	x	x	x	x	Group 2
1	1	x	x	x	x	Group 3

Transmit Message Length (TML)

7	6	5	4	3	2	1	0
x	x	x	x	3	2	1	0

TML.0 - 3 Length in number of bytes of message to be transmitted.

TML.3	TML.2	TML.1	TML.0	Number of Bytes
0	0	0	0	1
.	.	.	.	.
.	.	.	.	.
1	1	1	1	16

Control Register 1 (CR1)

7	6	5	4	3	2	1	0
TSTP	LOOP	TST1	CLRU	INC	TCBL	TV	$\overline{\text{MUT}}$

TSTP Test mode. Must be set to 0 for normal operation.

LOOP Loopback - When high, the received data is looped back through the transmitter. In addition, the node transmits messages to its Network Address (TTA = NA) in its message channel and in its message channel + 1.

TST1 Test mode. Must be set to 0 for normal operation.

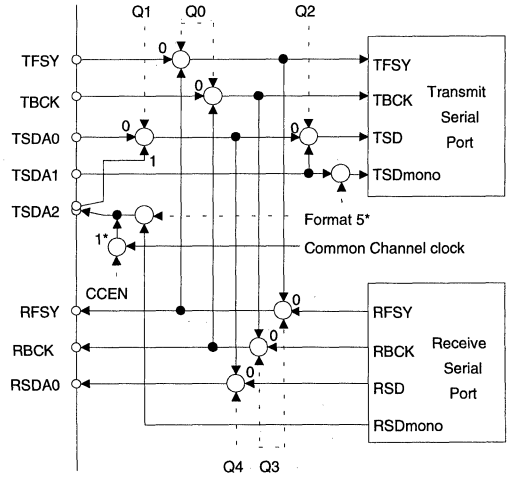
CLRU Clear U Channel - When CLRU is high, the transmitted U bits are all set to 0.

INC Increment MAP - Setting INC high enables the auto increment function of MAP for SPI and I^2C interface modes.

TCBL Transmit Channel Block - A low to high transition of this bit (based on two successive samples) sets the next frame as the beginning of a channel block. The TCBL pin is OR'ed with this register.

TV Transmitted Validity bit. This register and the TV pin are sampled at the same time and OR'ed together.

$\overline{\text{MUT}}$ Sets all transmitted data to 0's when low. Transmitted audio data is muted immediately upon setting bit to zero (could be middle of audio sample).



*Format 5 overrides CCEN and SSC "Q" settings

Figure 16 - Signal Muxes Controlled by SSC Register

mask bits corresponding to LOCK, ERR, and V also determine which condition(s) are required to set the VERF pin high.

Message Passing

The CS8425 establishes communication between nodes via the U (User) data channel. The U channel is time division multiplexed into nine channels, each of which is assigned a time slot. Each node is assigned one of eight network addresses, NA, which specifies the time slot in which it can transmit. The ninth channel is a common channel which is accessed through the TUBIT and RUBIT pins. This common message channel is inserted at every 12th U bit position as shown in Figure 18, and Table 4.

The CS8425 must be in peripheral configuration to fully use the message passing capabilities. Messages can be transmitted on the user channel from any one node to any other node or group of nodes. Communication of messages is synchronized to block boundaries. The 384 user bits per block are divided between the eight message and one common channels, with 44 bits per message channel and 32 bits for the common channel. Messages can be up to 16 bytes in length, taking up to four blocks. The structure of a message is shown in Figure 17.

Messages travel around the ring and back to the originator. All nodes simply monitor and pass along all messages sent on channels other than the one specified by its NA. Stand-alone configurations do not have a NA nor message processing capabilities, although messages are

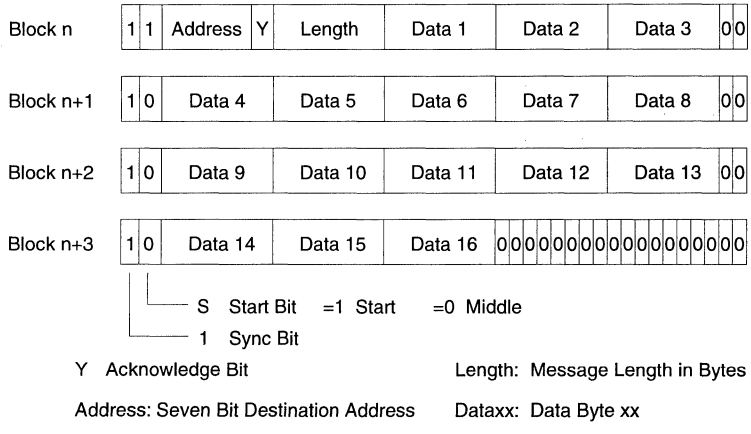


Figure 17 - Message Structure

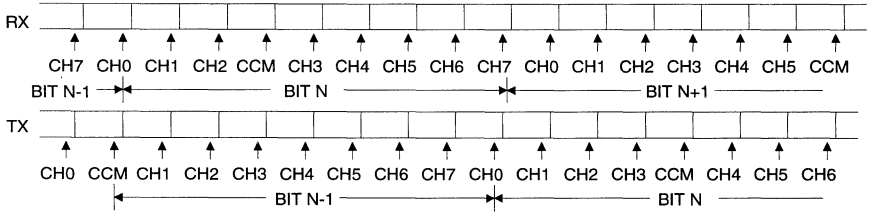


Figure 18 - Message Time Slots when Passing Through a Master.

passed through. In all cases, Common Channel messages are passed along by connecting the RUBIT and TUBIT pins together.

Since the master establishes the frame and block structures for the entire network, a message initiated by another node will arrive at the master after the master has transmitted that time slot (since the master had initiated that time slot earlier). The master will put the message in the next available time slot, the second time slot, for that message, hence a message is delayed by one time slot through the master as shown in Figure 18. As a result, a received message will start in either the first or second time slot of the message channel. (The maximum allowable data delay around a ring is limited to 31 bit periods, so data initiated by the master will have returned to the master before the next message time slot is to be transmitted.)

The CS8425 has eight memory blocks for buffering messages. Block 0 is used to store the message to be transmitted. Blocks 1 through 7 buffer the seven receive channels. The transmit port is read/write and the receive ports are read only. Successive receive channels are buffered in successive blocks. Table 3 shows the block assignments for NA = 2 (channel 2 is the transmit channel).

NA2	NA1	NA0	Transmit Channel	Subframes
0	0	0	0	1, 9, 18,...
0	0	1	1	2, 10, 19,...
0	1	0	2	3, 11, 20,...
0	1	1	3	4, 13, 21,...
1	0	0	4	5, 14, 22,...
1	0	1	5	6, 15, 23,...
1	1	0	6	7, 16, 25,...
1	1	1	7	8, 17, 26,...

Table 4 - Message Channel and Subframe Assignments.

CHANNEL	0	1	2	3	4	5	6	7
BLOCK	1	2	0	3	4	5	6	7

Table 3 - Message Block Assignments for NA = 2

The registers used for messages are the Transmit Target Address, TTA, the Transmit Message Length, TML, and the Address Register, ADR. The Status Register bit REJ, the Buffer Full, BF, and Buffer Full Enable, BFE, registers are also used. Address Register bits NA2, NA1 and NA0 specify the Network Address determining the message channel used by the device. Table 4 shows the transmit channel and subframe used for each NA for message passing.

TRANSMITTING MESSAGES

To send a message, the TTA, TML, and the transmit buffer (memory block 0) must first be loaded. The destination of a message is loaded into the TTA register. The TTA contains six bits which can address a particular node by specifying its NA, a group of nodes by specifying a group address or all nodes by specifying the general call address. The message length, ranging from one to sixteen bytes, is loaded in to the TML register. The transmit buffer contains the message itself.

Once the registers have been loaded, setting BFE.0 from low to high sets BF.0 high (BFE.0 must be low or high for a minimum of two biphase bit periods to be detected). Transmission of the message begins at the next falling edge of TBLK (the beginning of the next data block). BF.0 high indicates that the node is currently sending a message. Following the transmission of the last data byte, BF.0 is cleared. If BFE.0 is high when this occurs, an interrupt will be generated. The timing for BF.0 and the interrupt is shown in Figure 19.

The node transmitting a message sends the sync bit, the start bit, the target address, the acknowledge bit, the message length, and the message

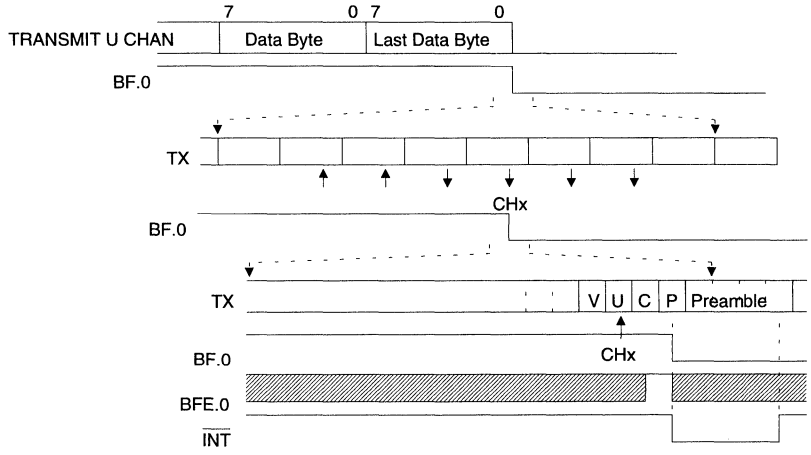


Figure 19 - Timing Details of BF.0, BFM.0 and the Associated Interrupt

of one to 16 bytes. The address and length bytes are structured as shown in Tables 5 and 6. The message travels around the ring and back to the originating node where the acknowledge bit, Y, is monitored. If Y is a 1, SR.1, REJ, is set high, and an interrupt is issued if SRE/M.1 is set. On a group or general call, any or all of the nodes can set the Y bit, rejecting the message. If a message is rejected, the entire message is still transmitted.

7	6	5	4	3	2	1	0
0	TTA.5	TTA.4	TTA.3	TTA.2	TTA.1	TTA.0	Y

Table 5 - Transmit Target Address ($8D_H$) Bit Order

7	6	5	4	3	2	1	0
0	0	0	0	TML.3	TML.2	TML.1	TML.0

Table 6 - Transmit Message Length ($8E_H$) Bit Order

RECEIVING MESSAGES

A node continuously monitors all channels except its own channel and the common channel for incoming messages. A node accepts messages sent to its General Call Address, Group Address and Network Address. An incoming message is stored in the buffer allocated for that channel. Setting the Overwrite Protect Mask, OPM, bit for a message channel will prevent incoming messages from overwriting a message stored in the receive buffer. If the OPM is set and the buffer is full, a message is rejected (and the "Y" bit of the message address byte is set). If the buffer is clear, the message, is accepted and the receive status bit, RCV, SR.0, is set. An interrupt is generated if the RCV enable bit, SRE/M.0, is set. Message address structures are shown in Table 7.

Bit #	7	6	5	4	3	2	1	0
Net Addr	x	0	0	0	NA2	NA1	NA0	Y
Group Addr	x	GA1	GA0	x	x	x	x	x
General Call	x	0	0	1	1	1	1	1

Table 7 - Message Addresses ($8C_H$)

After identifying a message, the device stores the message length in an internal temporary register. The first data byte is stored in memory location 0_H, and the message length is decremented. Successive bytes are written into the memory block until the received message length is decremented to zero. After the entire message is stored, the bit corresponding to that channel in the Buffer Full,

BF, register is set. An interrupt will be generated if the corresponding bit in the Buffer Full Enable, BFE, register is set. Bits in the BF register are cleared by a low to high transition on the corresponding BFE bit (bit must be high for two 64Fs bit periods).

User (message) data on all *receive* channels is always retransmitted. Messages sent to a node pass through that node and on to the sender. Data is written into memory one bit at a time. RCV goes high just after the last address bit is received, and stays high until the last message bit is written into memory. Figure 20 shows internal message receive timing relative to the transmit timing of TX.

Networks which have more than eight nodes will have nodes which share network addresses. Each of these nodes will receive messages sent to its NA, and any node can set the REJ flag. Messages will not pass through a node which shares the same network address as the node generating the message.)

Common Channel Message

The common channel can be used to pass global messages to all nodes in a ring. This message channel is not buffered by internal memory. It is accessed through pins TUBIT and RUBIT in all configurations. TUBIT is sampled and RUBIT is updated 32 times per block. When TUBIT is connected to RUBIT, data on this channel passes through the node. This data will be delayed by one U-bit position when passing through a master. Timing is shown in Figure 21.

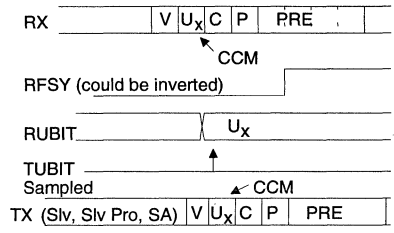


Figure 21 - RUBIT to TUBIT Timing

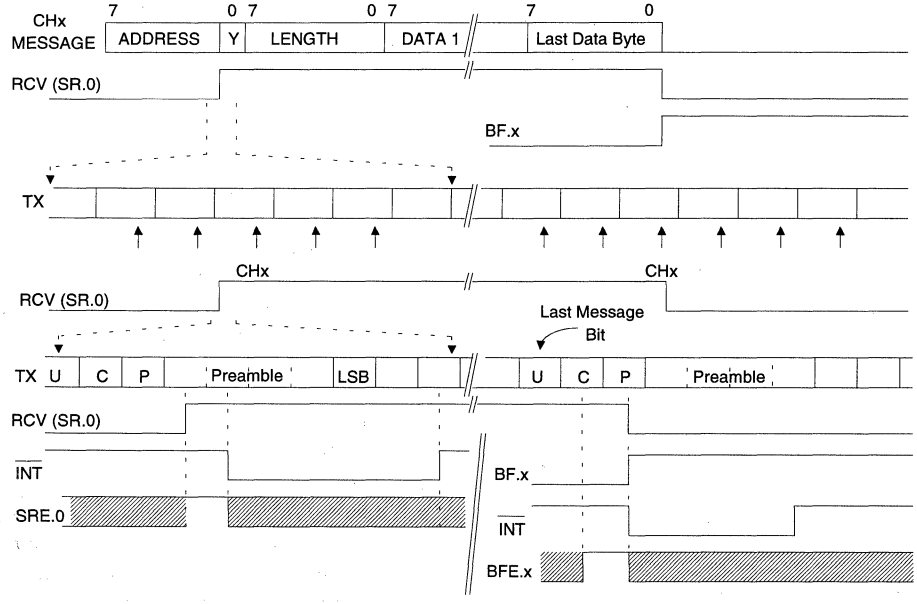


Figure 20 - Receive Message Timing

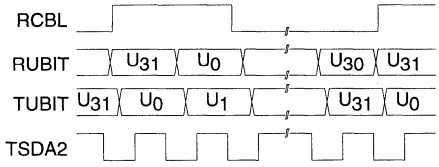


Figure 22 - Common Message Channel Clock

The CS8425 can be configured to output a clock in association with data at the TUBIT and RUBIT pins. Setting CCEN, CR0.7 to one causes the TSDA2 pin to output an I^2C type clock. The clock and data relationships are shown in Figure 22. Data setup and hold times relative to clock edges should exceed a millisecond.

Channel Status

Channel status bits are used to identify certain characteristics about the audio data. Channel status is tied to the block structure of the data, resulting in 192 CS bits per block, per channel. The CS8425 supports channel status according to IEC-958 specifications. IEC-958 specifications represent "consumer" applications (not professional), hence the CS8425 does not support CRC codes. Channel status is transmitted one bit per subframe, and can be independent for both channels.

The CS8425 has dedicated pins for input and output of some important CS bits in all operating modes. When the device is configured as a peripheral, two registers are dedicated for generating many more transmit CS bits, and there are two registers for monitoring certain received CS bits.

Table 8 shows the bit definitions for the channel status registers. The transmit and receive registers are the same except for bit 0 for RCS0. CS bit 0 specifies whether channel status conforms to the professional or consumer definition of channel status. The CS8425 is only capable of supporting the consumer definition of channel

CS0 0 - Consumer
1 - Professional
CS8425 supports Consumer Mode

CS1 0 - Audio Data
1 - Nonaudio Data

CS2 0 - Copy Inhibited / Copyright Asserted
1 - Copy permitted / Copyright Not Asserted
TCS0.2 bit OR'ed with input to pin, TCBIT.

CS3,4 Emphasis
0, 0 - None - 2 channel audio
1, 0 - 50/15µs
0, 1 - Reserved - 2 channel audio
1, 1 - Reserved - 2 channel audio

CS24, 25 Sample Frequency
0, 0 - 44.1kHz
0, 1 - 48kHz
1, 1 - 32kHz
All other states reserved

CS8 - CS14 Category Code
See IEC 958 and Crystal App Note "Overview of Digital Audio Interface Data Structures"

CS15 Generation Status
See IEC 958 and Crystal App Note "Overview of Digital Audio Interface Data Structures"
TCS1.7 bit OR'ed with input to pin, TLBIT.

Table 8 - Channel Status Bits

status. The CS8425 can receive professional Channel Status, but the bit definitions are different, and it does not generate nor check CRC. Professional channel status passes through a node when the node is configured as: a peripheral, master with BYPS, CR0.6=1, a peripheral, slave with BYPS=0, a stand-alone slave with TCBIT and TLBIT connected to RCBIT and RLBIT. As a master, the channel status bits are read from the receive CS buffers, when BYPS is set, so only those CS bits are passed. (Note: CS0 exists in the RCS0 buffer)

In all cases, received channel status comes from the left channel. The transmit channel status pins and TCS register bits are sampled for both left and right channels. When the CS bit is available

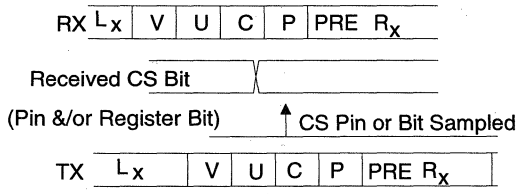


Figure 23 - Received C-bit Timing for All Modes *Except* Master

from both the register and a pin, the contents of the register and the input to the pin are OR'ed. The bits are sampled just before they are transmitted as shown in Figure 23. Register bit TBLK, SR.2, goes low during the transmission of the first preamble of a block and TBLK goes high 32 frames later. While TBLK is high, the channel status registers are not accessed.

Normally a master node generates channel status for the ring and all other nodes pass it on unaltered. This role can be reversed by setting BYPS, CR0.6 to 1. When set for bypass, a master will pass channel status and a slave or slave processor will generate it.

As a master, channel status is read from TCS0, TCS1 and TEMPH when BYPS is low. Received channel status from the left channel only is stored in RCS0 and RCS1. When BYPS is high, channel status for both transmitted channels is read from RCS0 and RCS1 and passed on. Because of the delay around the ring, left channel status will be delayed by one block when passing through a master, but right channel status will pass through without delay.

In stand-alone configurations, CS is always generated by a master and passed by a slave or slave processor. An exception is the copy protect bit, CBIT, and the generation status bit, LBIT, which are generated by each node in all stand-alone configurations. The received CBIT and LBIT are output on RCBIT and RLBIT. The transmit bits are input through TCBIT and TLBIT. If the transmit and receive pins are connected together, the CBIT and LBIT will be passed through the node. When these pins are interconnected, these bits will pass through a slave without delay as in Figure 23; the left channel will be delayed by one block by a master as in Figure 24. Figure 24 also shows the delay of data as it passes around a multinode ring. Note that the delay for a four node ring is 3¾ bit periods, and that the master has already transmitted the left channel CS bit before the new left CS bit is received from a subsequent node.

Channel Status in General-Purpose Modes

When the CS8425 is configured for stand-alone, general-purpose operation the TSDA1 and TSDA2 pins are used for inputting and outputting channel status data respectively. Similarly, in Peripheral configurations, setting CCEN, CR0.7, high configures the part to use TSDA1 and TSDA2 for channel status. The contents of the channel status registers, TCS0 and TCS1, is ignored when TSDA1 is used to input CS data. These pins can be used for channel status for Formats 0-4 only. TSDA2 outputs the third audio channel in Format 5. In Format 5, the internal registers are used for channel status. In stand-

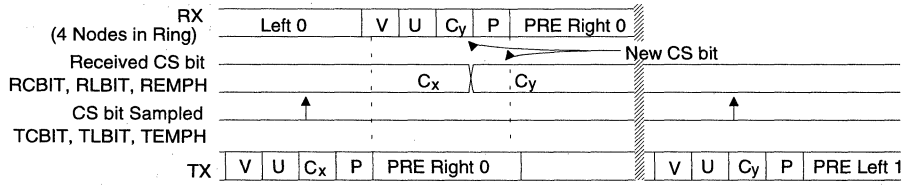


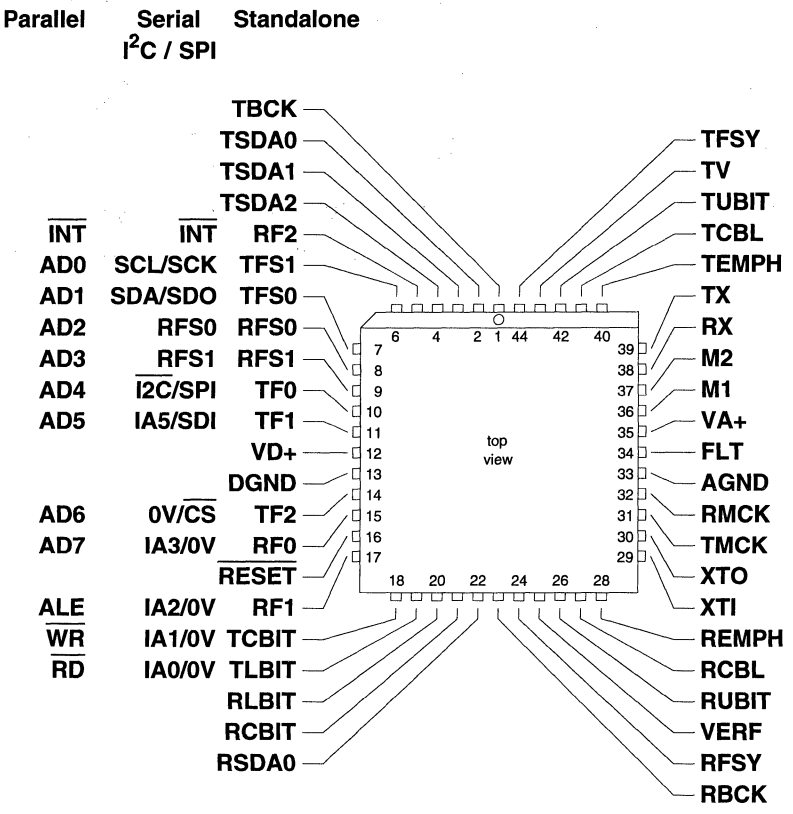
Figure 24 - Channel Status bit delay when passing through a Master in Stand-alone Mode

alone modes, channel status is not available in Format 5.

When used for channel status, TSDA1 is sampled ½ TBCK samples after the edge of TFSY. In format 2, TSDA1 is sampled 1½ TBCK samples after the TFSY edge. TSDA1 is read for both left and right channels. TSDA2 is updated 2 RBCK cycles before the RFSY edge which corresponds to the output audio sample on RSDA0.

PIN DESCRIPTIONS

CS8425



Power Supply Connections

VA+ - Positive Analog Power, PIN 35.

Power supply for the analog circuitry; nominally 5 volts. VA+ should be decoupled to AGND with 1.0µF and 0.1µF capacitors.

VD+ - Positive Digital Power, PIN 12.

Power supply for the digital circuitry; nominally 5 volts.VD+ should be decoupled to DGND with a 0.1µF capacitor.

AGND, DGND - Analog and Digital Supply Grounds, PINS 33 &13.

Power supply grounds for the analog and digital supplies. AGND and DGND should be connected to the same potential off chip.

PLL, Oscillator & Clocks

FLT - Filter for PLL, PIN 24.

An external 1kΩ resistor and 0.047μF capacitor are required from the FLT pin to analog ground.

XTI, XTO - Crystal Oscillator, PINS 29 & 30.

A crystal can be connected to these pins, and used as a timing reference. XTO has limited drive capability, but is capable of driving a single pin, such as TMCK.

TMCK - Transmit Master Clock Input, PIN 31

In the master mode, TMCK must be generated by the oscillator, or input from an external clock source. Generally, TMCK is either connected to the oscillator output at RMCK. If necessary, TMCK can be directly connected to the XTO pin of the oscillator. In peripheral configurations, internal clock dividers can be set via Control Register 0. TMCK is ignored in the slave or slave processer modes where transmit timing is generated from the PLL.

RMCK - Receive Master Clock Output, PIN 32.

RMCK can be generated by either the recovered clock in the slave or slave processor modes, or the crystal oscillator in the master mode. The oscillator output can be divided by 1, 1.5, 2, or 3 and output at RMCK. In standalone modes, RMCK is 256F_S. If the crystal frequency is 384F_S, TMCK may be connected to RMCK.

6

Audio Data Interface

Dedicated Transmit Pins

TBCK - Transmit Bit Clock Input, PIN 1.

Audio data input to TSDA0, TSDA1, and TSDA2 is latched by TBCK. The latch edge is determined by the selected format. There must be either 16, 24 or 32 TBCKs per subframe.

TSDA0, TSDA1, TSDA2 - Transmit Audio Data Inputs 1, 2 & 3, PINS 2, 3 & 4.

Audio data input to these pins is sampled by TBCK. The edge of TBCK on which data is latched, and the relationship to TFSY is determined by the format selected by TF0/1/2. In a peripheral mode, the Source Switch Control Register specifies which pin(s) is used for the input. In standalone mode stereo audio data is always input to TSDA0.

When M1 and M2 are high, (stand-alone configuration) setting TSDA1 low selects the slave processor mode; setting TSDA1 high selects the slave mode (except in Format 5).

In Format 5, stereo data is input to TSDA0, mono data is input to TSDA1, and received mono data is output on TSDA2.

In A-LAN, peripheral modes, when using serial port Formats 0 - 4, setting CCEN, CR0.7, high causes a clock to be generated and output from TSDA2 for input and output of Common Channel message bits.

In General Purpose, peripheral modes when CCEN, CR0.7 = 1, and General Purpose stand alone mode TSDA1 and TSDA2 are dedicated Channel Status input and output respectively (except for format 5).

TX - Transmitter Output, PIN 39.

TX is a logic level output for the transmitted digital audio data stream, and is intended for connection to a media interface device such as a transmitter LED or RS-422 driver.

TEMPH - Transmit Emphasis Input, PIN 40.

Channel Status Emphasis bit, bit 3, is set by the TEMPH input. In the peripheral configurations when BYPS, CR0.6, is low, TEMPH is OR'ed with the contents of register TCS0.3.

TCBL - Transmit Channel Block Input, PIN 41.

The SPDIF block timing can be determined by TCBL. TCBL is sampled along with the TV bit once a frame in all serial port formats except Format 1 where it is sampled once per subframe. A low to high transition on TCBL during a frame (subframe) identifies that channel as the first channel of a block. Block timing can be altered without affecting the frame or subframe timing.

TUBIT - Transmit U Bit, PIN 42.

The common channel message is input only through the TUBIT pin. TUBIT is sampled 32 times per message block. TUBIT may be connected to RUBIT to pass the common message channel through a node. Data will be delayed by one bit when passing through a master.

In the general purpose modes, TUBIT is used to input all U bits. TUBIT is sampled just after the active edge of TFSY and is output with the audio data being sampled concurrently.

TV - Transmit Validity Bit Input, PIN 43.

The validity bit for the audio sample being input to the serial port is sampled 1½ TBCK cycles after either edge of TFSY for all serial port formats except Format 1 where TV is sampled 2½ cycles after the rising edge of TFSY. TV can be connected to VERF to retransmit the received validity bit. (The SRE/M register must be appropriately set to select the desired conditions for which the VERF pin is set.)

TFSY - Transmit Frame Sync Input, PIN 44.

Frame or word synchronization is controlled by TFSY. Its function is controlled by the format selected on TM0/1/2. TFSY functions as a left-right signal in all formats except format 1, where it functions as a word clock.

Standalone Interface Configuration - Transmit Inputs

TCBIT - Transmit Copy Bit, PIN 18.

TCBIT sets the copy bit, the C bit, of the Channel Status block. When TCBIT is connected to RCBIT, the C bit is passed through without delay in slave modes, and is delayed by one block in the master mode.

TLBIT - Transmit Generation Bit, PIN 19

TLBIT sets the generation bit, the L bit, of the Channel Status block. When TLBIT is connected to RLBIT, the L bit is passed through without delay in slave modes, and is delayed by one block in the master mode.

Standalone Interface Configuration - Transmit Control

TSF0, TSF1 - Transmit Sample Frequency Inputs 0 & 1, PINS 7 & 6

TSF0 and TSF1 correspond to the sample frequency bits 25 and 26 (byte 3) of Channel Status.

TF0, TF1 & TF2 - Transmit Format Control 1, 2 & 3, PINS 10, 11 & 14.

The six transmit formats are selected by these pins. These formats establish the polarity and timing relationships between TBCK, TFSY & TSDA0/1/2.

Dedicated Receive Pins

RSF0, RSF1 - Receive Sample Frequency Outputs 0 & 1. PINS 8 & 9.

The received channel status sample frequency bits 25 and 26, are output on RFS0 and RFS1. These pins are not available in the peripheral configuration for parallel interface.

RLBIT - Receive Generation Bit, PIN 20.

The received Channel Status copy Generation Bit is output on RLBIT.

RCBIT - Received Copy Bit, PIN 21.

The received Channel Status Copy Bit is output on RCBIT.

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RSDA0 - Receive Audio Data Output, PIN 22.

Recovered audio data is output with RBCK. The edge of RBCK on which data is valid and stable is determined by the receive format selected by RF0/1/2.

RBCK - Receive Bit Clock Output, PIN 23.

Data output on RSDA0 is clocked by RBCK.

RFSY - Receive Frame Sync Output, PIN 24.

Edges of RFSY delineate the subframes of the received data. The relationship of RFSY to RBCK and RSDA0 is determined by the receive format selected by RF0/1/2.

VERF - Validity Error Flag Output, PIN 25.

VERF outputs the received validity bit to indicate errored audio samples. In Standalone Configurations, VERF is high when the receiver is out of lock, a parity or line coding error is detected, or received validity bit is high. In peripheral configurations, Status Register Enable/Mask register determines which of these errors can affect the VERF pin. Transitions on VERF are coincident with the edges of RFSY which delineate the errored audio sample.

RUBIT - Receive U Bit Output, PIN 26.

The received common message channel data is output on RUBIT. RUBIT is updated 32 times per message block. RUBIT may be connected to TUBIT to pass common message channel data through a node. Data will be delayed one cycle when passing through a master.

In general purpose modes, all U bits are output at RUBIT.

RCBL - Receive Channel Block Output, PIN 27.

RCBL identifies the block boundaries of the received data. RCBL transitions high three RBCK cycles before the RFSY edge that identifies the first frame of a block. RCBL remains high for 32 frames and is low for 160 frames.

REMPH - Receive Emphasis Output, PIN 28.

The received Channel Status Emphasis bit, bit 3, is output on REMPH.

RX - Receive Input, PIN 38.

RX is a logic level input for the IEC-958 data stream, and is intended for connection to a media interface device such as a receiver LED.

Standalone Interface Configuration - Receive Control Pins

RF0, RF1 & RF2 - Receive Format Control 1, 2 & 3, PINS 15, 17 & 5.

Six formats determining the relationship between RCK, RSDA0 and RFSY are established by these pins.

Mode

M1, M2 - Mode Selection, Pins 36 & 37.

The mode selection determines the configuration of the CS8425. See Table 2 for the six configurations.

Parallel Interface (M1 = 0, M2 = 0)

AD0 - AD7 - Address 0 - 7 and Data 0 - 7, PINS 7 - 11, 14, & 15.

Parallel address or data bus.

ALE - Address Latch Enable, PIN 17.

The falling edge of ALE will latch the contents of the bus into an internal address register.

$\overline{\text{WR}}$ - $\overline{\text{Write}}$, PIN 18.

Data is output to the bus by setting $\overline{\text{WR}}$ low.

$\overline{\text{RD}}$ - $\overline{\text{Read}}$, PIN 19.

Data is read from the bus by setting $\overline{\text{RD}}$ low. Data is latched on the rising edge of $\overline{\text{RD}}$.

I^2C Bus Interface (M1 = 0, M2 = 1; $I^2\overline{C}$/SPI = 0)

IA0, IA1, IA2, IA3, IA5 - I^2C Bus Address Inputs, PINS 19, 18, 17, 15, 14 & 11.

The lower 7 bits bits of the I^2C address are set by these pins. The remaining address bit, the MSB (first bit in) is internally set to 0. Address IA4 is 0.

Note: At least one of IA3, 5 or 6 must be set to 1 (but not all) for a usable and valid I^2C address.

0V - Pin 14

0V must be set low in I^2C mode.

$\overline{\text{INT}}$ - $\overline{\text{Interrupt}}$, PIN 5.
$\overline{\text{INT}}$ pulls low to interrupt a host processor. $\overline{\text{INT}}$ must be pulled to the supply by an external 47k resistor.

SCL - Serial Clock Input, PIN 6.
Clock associated with data transferred over the I^2C bus. SCL must be pulled to the power supply by an external 47k resistor.

SDA - Serial Data I/O, PIN 7.
Serial data is input to and output from the SDA pin. SDA must be pulled to the VD+ supply by an external 47k resistor.

Serial Port Interface, SPI, (M1 = 0, M2 = 1; $\overline{I^2C}$ /SPI = 1)
SCK - Serial Clock Input, PIN 6.
Data transfers on SDO and SDI are clocked by SCK.

SDO - Serial Data Out, PIN 7.
Output data from internal registers changes on the falling edge of SCK.

SDI - Serial Data In, PIN 11.
Data input to internal registers is sampled on the rising edge of SCK.

$\overline{\text{CS}}$ - $\overline{\text{Chip Select}}$, PIN 14.
Setting $\overline{\text{CS}}$ low activates the serial port.

$\overline{\text{INT}}$ - $\overline{\text{Interrupt}}$, PIN 5.
$\overline{\text{INT}}$ pulls low to interrupt a host processor. $\overline{\text{INT}}$ must be pulled to the VD+ supply by an external 47k resistor.

0V - PINS 15, 17, 18, and 19.
These pins are unused and should be tied to ground when configured for SPI interface.

Miscellaneous

$\overline{\text{RESET}}$ - PIN 16.
Pulling $\overline{\text{RESET}}$ low resets the entire part, including the data registers and the internal logic.

• Notes •

CS1232 Power Monitor and Watchdog Timer

The CS1232 compares the system power supply to an on-chip, band-gap voltage reference and signals if the supply falls below 4.6 volts. This permits the host microprocessor to power down the system gracefully before the supply fails. Critical system parameters can be saved in non-volatile memory for re-initialization when the power supply returns to rated levels. The CS1232 also contains a watchdog timer and push-button reset circuit.

CS3310 Volume Control

The CS3310 is a stereo analog volume control, allowing volume level adjustment from -98dB to +30dB in 0.5dB steps. The volume level is changed via a simple serial digital control bus, which is cascadeable for multiple parts. Low glitch circuit design ensures no "zipper" noise during volume changes. Exceptionally low THD and noise allow use in consumer and professional applications.

CDBCAPTURE Data Capture System for A/D Converters

CDBCAPTURE is a small circuit card that captures up to 8K x 24 words from any serial output A/D converter. The captured data is then sent to any IBM compatible PC via a serial port. National Instruments LabWindows based software is provided to perform FFT, time domain and noise histogram analysis.

CONTENTS

Semiconductor Corporation

CS1232

Micromonitor

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- 8-pin Mini-DIP or 16-pin SOIC
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

The power status (V_{CC}) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when V_{CC} goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after V_{CC} returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

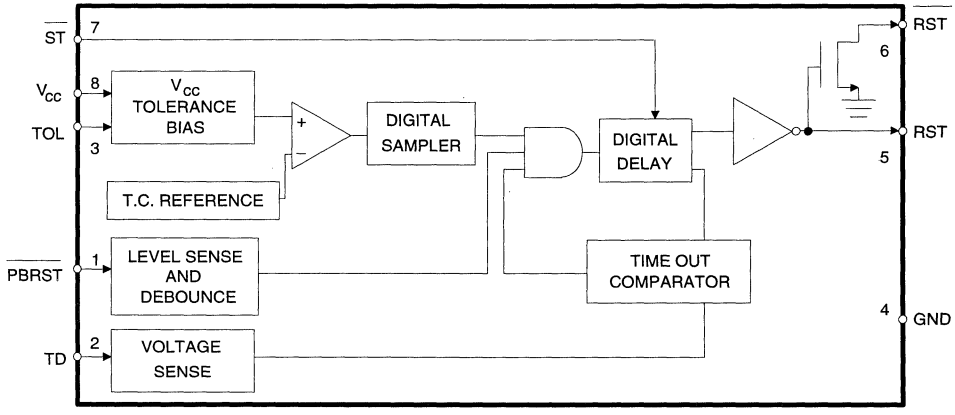
The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

A surface mount 16-pin SOIC is available, as well as an 8-pin Plastic DIP.

ORDERING INFORMATION:

Model	Temp. Range	Package
CS1232-CP	0 °C to 70 °C	8-pin Plastic DIP
CS1232-IP	-40 °C to +85 °C	8-pin Plastic DIP
CS1232-CS	0 °C to 70 °C	16-pin SOIC
CS1232-IS	-40 °C to +85 °C	16-pin SOIC
Die Only:		
CS1232-YU		Unpackaged Die

7



ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter			Symbol	Min	Typ	Max	Units
V_{CC} Trip Point	(Note 1)	TOL = GND	V_{CCTP}	4.50	4.62	4.74	V
		TOL = V_{CC}	V_{CCTP}	4.25	4.37	4.49	V
Operating Current	(Note 2)		I_{CC}	-	0.4	2.0	mA

Notes: 1. All voltages referenced to ground.
2. Measured with outputs open.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
Operating Temperature	CS1232		0	-	+70	°C
	CS1232-I		-40	-	+85	°C
Supply voltage	(Note 1)	V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter		Symbol	Min	Typ	Max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	(Note 1)	V_{IH}	2.0	-	V_{CC}+0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	(Note 1)	V_{IL}	-0.3	-	+0.8	V
Output High Current at 2.4 V RST only		I_{OH}	-8.0	-10.0	-	mA
Output High Voltage at -500 µA RST only	(Note 3)	V_{OH}	V_{CC}-0.5	V_{CC}-0.1	-	V
Output Low Current at 0.4 V RST, $\overline{RST}$		I_{OL}	8.0	10.0	-	mA
Input Leakage	(Note 4)	I_{IL}	-1.0	-	+1.0	µA
Input Capacitance	T_A = 25°C	C_{IN}	-	-	5	pF
Output Capacitance	T_A = 25°C	C_{OUT}	-	-	7	pF

Notes: 3. On power-down, RST typically remains within 0.5V of V_{CC} (and $\overline{RST}$ typically remains within 0.5V of GND) until V_{CC} falls below 2.0V.
4. $\overline{PBRST}$ is internally pulled up to V_{CC} with a 100 kΩ resistor. TD is internally pulled up to V_{CC} with a 100 kΩ resistor and pulled down to ground with a 100 kΩ resistor.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Typ	Max	Units
Voltage on Any Pin Relative to Ground	-1.0	-	+7.0	V
Input Current	-	-	±10	mA
Storage Temperature	-55	-	+125	°C
Soldering Temperature	260 °C for 10 sec			

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter			Symbol	Min	Typ	Max	Units
$\overline{PBRST}$ = V_{IL}			t_{PB}	-	20	-	ms
RESET Active Time			t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width			t_{ST}	20	-	-	ns
V_{CC} Detect to RST and $\overline{RST}$			t_{RPD}	-	-	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V			t_F	300	-	-	µs
V_{CC} Detect to RST and $\overline{RST}$		(Note 5)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V			t_R	0	-	-	ns
$\overline{ST}$ Pulse Period	(Note 6)	TD pin at Ground	t_{TD}	50.0	150	250	ms
		TD pin floating	t_{TD}	250	600	1000	ms
		TD pin connected to V_{CC}	t_{TD}	400	1200	2000	ms

Note: 5. t_R = 5 µs
6. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.
7. $\overline{RST}$ is an N-channel open drain output.

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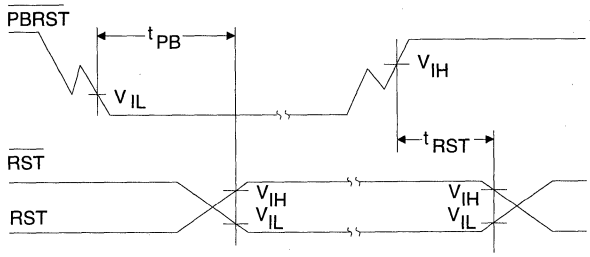
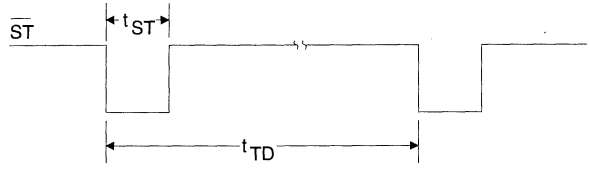
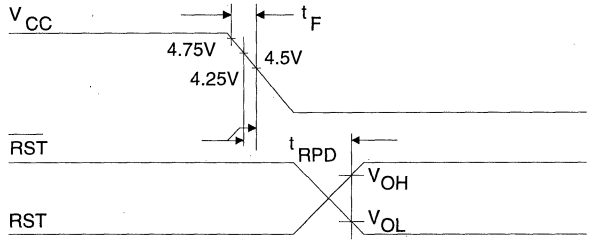


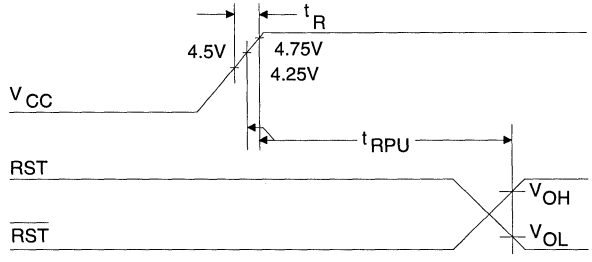
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

POWER SUPPLY MONITOR

The CS1232 will detect out-of-tolerance power supplies for processor-based systems as well as warn of an impending power failure. The TOL digital input pin defines the threshold level for V_{CC}; when the V_{CC} level drops below the TOL defined level, the CS1232 asserts the signals RST and $\overline{RST}$. The threshold level is set to typically 4.37 V if TOL is connected to V_{CC}, and is set to typically 4.62 V if TOL is connected to GND. The processor is allowed to continue until the last possible moment that V_{CC} is valid. Upon return of power, RST and $\overline{RST}$ are active for 250 ms (minimum) to allow stabilization.

PUSHBUTTON RESET CONTROL

$\overline{PBRST}$ is normally connected to a reset pushbutton (see Figure 1). This active low signal is debounced and timed to generate signals of 250 ms (minimum) for RST and $\overline{RST}$. The delay begins when $\overline{PBRST}$ is released from from the low state. $\overline{PBRST}$ has an internal 100 kΩ pull-up resistor.

WATCHDOG TIMER

When RST and $\overline{RST}$ become inactive (normal CPU operation), the watchdog timer starts timing out, using the time set by TD. RST and $\overline{RST}$ are forced active when $\overline{ST}$ is not stimulated for this predetermined time. TD sets the time to be: 150 ms if TD is connected to ground, 600 ms is TD is not connected, or 1.2 seconds with TD connected to V_{CC}. RST and $\overline{RST}$ are driven active for 250 ms (minimum) if no high-to-low transition occurs on the $\overline{ST}$ input pin before time out. Microprocessor address signals, data signals, control signals, and output port bits can be used for the $\overline{ST}$ input pin. These signals cause the watchdog timer to be reset prior to time out indicating normal function of the microprocessor (see Figure 2).

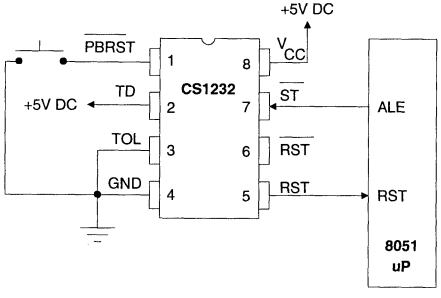


Figure 1. Pushbutton Reset

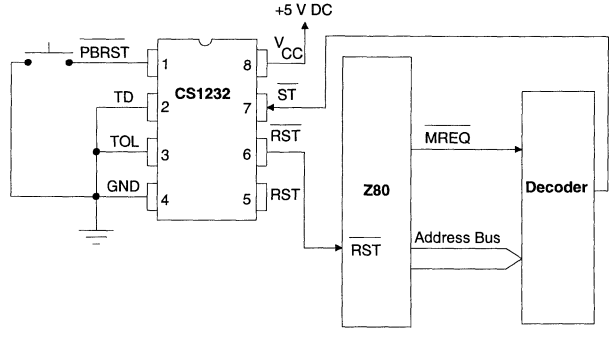


Figure 2. Watchdog Timer

PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	1	8	V_{CC}	+5 VOLT POWER
TIME DELAY SET	TD	2	7	$\overline{\text{ST}}$	STROBE INPUT
SELECTS V_{CC} DETECT LEVEL	TOL	3	6	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain)
GROUND	GND	4	5	RST	RESET OUTPUT (Active High)

NO CONNECTION	NC	1	16	NC	NO CONNECT
PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	2	15	V_{CC}	+5 VOLT POWER
NO CONNECT	NC	3	14	NC	NO CONNECTION
TIME DELAY SET	TD	4	13	$\overline{\text{ST}}$	STROBE INPUT
NO CONNECT	NC	5	12	NC	NO CONNECT
SELECTS V_{CC} DETECT LEVEL	TOL	6	11	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain)
NO CONNECT	NC	7	10	NC	NO CONNECT
GROUND	GND	8	9	RST	RESET OUTPUT (Active High)

DIE INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

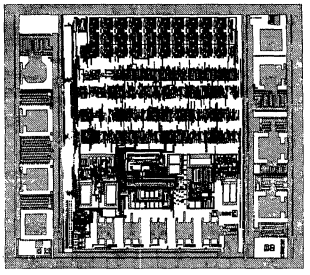
1. Die size: 0.061" by 0.069" (± 0.002").

2. The die is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to V_{CC}.

3. Die thickness shall be 0.0175" ± 0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 100.

5. The cavity dimensions for each die within the waffle pack are 0.080" by 0.080" (Waffle Pack Type H20-080).

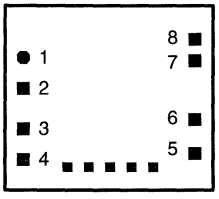


6. The CS1232-YU requires no particular bonding sequence.

7. Each pin of the CS1232 has ESD and latch-up protection circuitry.

8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

CS1232-YU Bonding Diagram



1 -	$\overline{\text{PBRST}}$	5 -	RST
2 -	TD	6 -	$\overline{\text{RST}}$
3 -	TOL	7 -	$\overline{\text{ST}}$
4 -	GND	8 -	VCC

•Notes•

Semiconductor Corporation

CS3310

Stereo Digital Volume Control

Features

- Complete Digital Volume Control
  - 2 Independent Channels
  - Serial Control
  - 0.5 dB Step Size
- Wide Adjustable Range
  - -95.5 dB Attenuation
  - +31.5 dB Gain
- Low Distortion & Noise
  - 0.001% THD+N
  - 116 dB Dynamic Range
- Noise Free Level Transitions
- Channel-to-Channel Crosstalk Better Than 110 dB

General Description

The CS3310 is a complete stereo digital volume control designed specifically for audio systems. It features a 16-bit serial interface that controls two independent, low distortion audio channels.

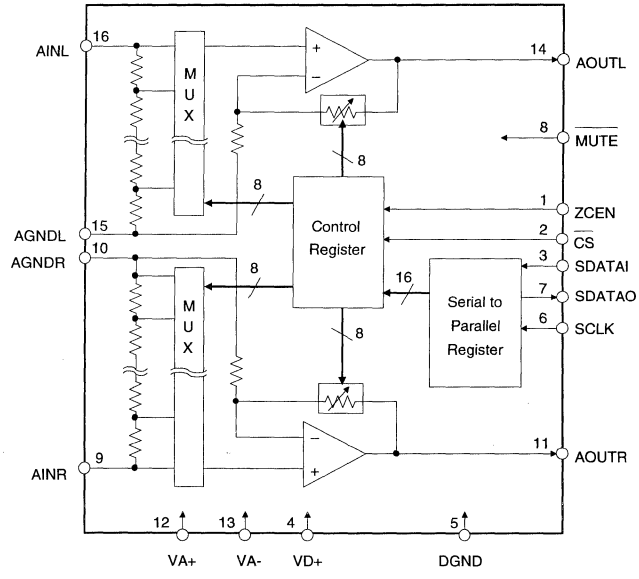
The CS3310 includes an array of well-matched resistors and a low noise active output stage that is capable of driving a 600 Ω load. A total adjustable range of 127 dB, in 0.5 dB steps, is achieved through 95.5 dB of attenuation and 31.5 dB of gain.

The simple 3-wire interface provides daisy-chaining of multiple CS3310's for multi-channel audio systems.

The device operates from ±5V supplies and has an input/output voltage range of ±3.75V.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS3310-KP	0° to 70° C	16-pin plastic DIP
CS3310-KS	0° to 70° C	16-pin plastic SOIC



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Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
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ANALOG CHARACTERISTICS

(T_A = 25 °C, VA+, VD+ = 5V ± 5%; VA- = -5V ± 5%; R_L = 2kΩ ; C_L = 20 pF;
10 Hz to 20 kHz Measurement Bandwidth ; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
DC Characteristics					
Step Size		-	0.5	-	dB
Gain Error (31.5 dB Gain)		-	±0.05	-	dB
Gain Matching Between Channels		-	±0.05	-	dB
Input Resistance	RIN	-	10	-	kΩ
Input Capacitance	C_{IN}	-	10	-	pF
AC Characteristics					
Total Harmonic Distortion plus Noise (V_{in} = $2V_{rms}$, 1 kHz)	THD+N	-	0.001	.0025	%
Dynamic Range		110	116	-	dB
Input/Output Voltage Range		(VA-)+1.25	-	(VA+)-1.25	V
Output Noise (Note 1)		-	4.2	8.4	µVrms
Digital Feedthrough (Peak Component)		-80	-	-	dB
Interchannel Isolation (1kHz)		-100	-110	-	dB
Output Buffer					
Offset Voltage (Note 1)	V_{OS}	-	0.25	0.75	mV
Load Capacitance		-	-	100	pF
Short Circuit Current		-	20	-	mA
Unity Gain Bandwidth, Small Signal (Note 2)		2	-	-	MHz
Power Supplies					
Supply Current (No Load, AIN = 0V)	IA+	-	5.0	8.0	mA
	IA-	-	5.0	8.0	mA
	ID+	-	350	800	µA
Power Consumption	P_D	-	52.0	84.0	mW
Power Supply Rejection Ratio (250 Hz)	PSRR	-	80	-	dB

NOTE: 1. Measured with input grounded and Gain = 1. Will increase as a function of Gain settings >1.
2. This parameter is guaranteed by design and/or characterization.

DIGITAL CHARACTERISTICS

(T_A = 25 °C, VA+ , VD+ = 5V ± 5%, VA- = -5V ± 5%)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	VD+0.3	V
Low-Level Input Voltage		V_{IL}	-0.3	-	+0.8	V
High-Level Output Voltage	(I_O = 200µA)	V_{OH}	VD-1.0	-	-	V
Low-Level Output Voltage	(I_O = 3.2mA)	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	1.0	10	µA

SWITCHING CHARACTERISTICS

(T_A = 25 °C; VA+, VD+ = +5V ± 5%; VA- = -5V ± 5%; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
Serial Clock		SCLK	0	-	4.2	MHz
Serial Clock	Pulse Width High	t_{ph}	80	-	-	ns
	Pulse Width Low	t_{pl}	80	-	-	ns
$\overline{MUTE}$	Pulse Width Low	-	2.0	-	-	ms
Input Timing						
SDATAI Set Up Time		t_{SDVS}	20	-	-	ns
SDATAI Hold Time		t_{SDH}	20	-	-	ns
$\overline{CS}$ Valid to SCLK Rising		t_{CSVS}	30	-	-	ns
SCLK Falling to $\overline{CS}$ High		t_{LTH}	35	-	-	ns
Output Timing						
$\overline{CS}$ Low to Output Active		t_{CSH}	-	-	35	ns
SCLK Falling to Data Valid		t_{SSD}	-	-	60	ns
$\overline{CS}$ High to SDATAO Inactive		t_{CSDH}	-	-	100	ns

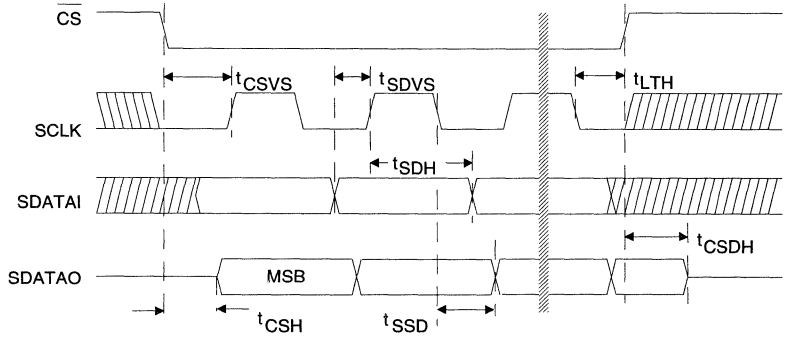


Figure 1. Serial Port Timing Diagram

RECOMMENDED OPERATING CONDITIONS

(DGND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital	VD+	4.75	5.0	VA+	V
Positive Analog	VA+	4.75	5.0	5.25	V
Negative Analog	VA-	-4.75	-5.0	-5.25	V
Ambient Operating Temperature:	T_A	0	25	70	°C

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies:				
Positive Digital	VD+	-0.3	(VA+)+ 0.3	V
Positive Analog	VA+	-0.3	6.0	V
Negative Analog	VA-	0.3	-6.0	V
Input Current, Any Pin Except Supply	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature (power applied)	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

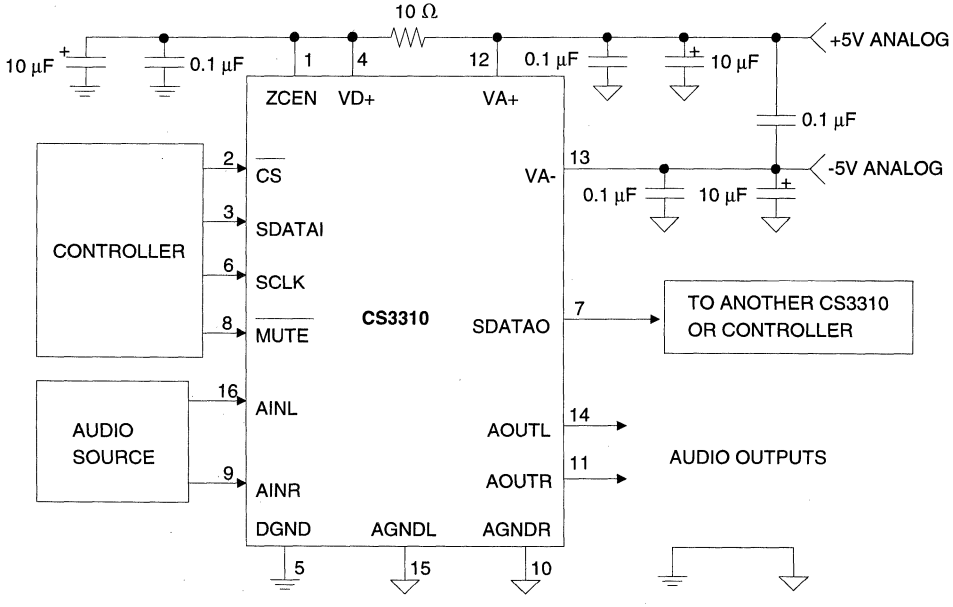


Figure 2. Recommended Connection Diagram

GENERAL DESCRIPTION

The CS3310 is a stereo, digital volume control designed for audio systems. The levels of the left and right analog input channels are set by a 16-bit serial data word; the first 8 bits address the right channel and the remaining 8 bits address the left channel. Resistor values are decoded to 0.5 dB resolution by an internal multiplexer for a total attenuation range of -95.5 dB. An output amplifier stage provides a programmable gain of up to 31.5 dB in 0.5 dB steps. This results in an overall 8-bit adjustable range of 127 dB.

The CS3310 operates from ±5V supplies and accepts inputs up to ±3.75V. Once in operation, the CS3310 can be brought to a muted state with the mute pin, $\overline{\text{MUTE}}$, or by writing all zeros to the volume control registers. The device contains a simple three wire serial interface which accepts 16-bit data. This interface also supports daisy-chaining capability.

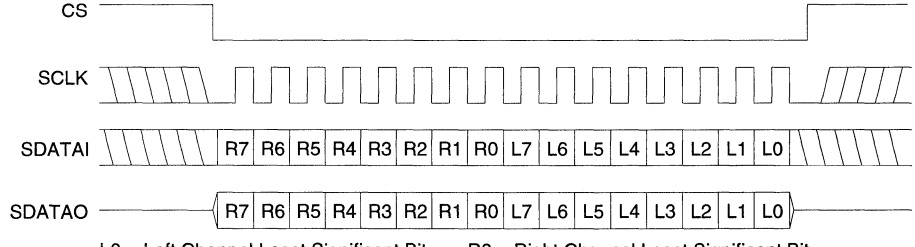
SYSTEM DESIGN

Very few external components are required to support the CS3310. Normal power supply decoupling components are all that is required, as shown in Figure 2.

Serial Data Interface

The CS3310 has a simple, three wire interface that consists of three input pins: SDATAI, serial data input; SCLK, serial data clock and $\overline{\text{CS}}$, the chip select input. SDATAO, serial data output, enables the user to read the current volume setting or provide daisy-chaining of multiple CS3310's.

The 16-bit serial data is formatted MSB first and clocked into SDATAI by the rising edge of SCLK with $\overline{\text{CS}}$ low as shown in Figure 3. The data is latched by the rising edge of $\overline{\text{CS}}$ and the analog output levels of both left and right channels are set. The existing data in the volume control data register is clocked out SDATAO on the falling edge of SCLK. This data can be used to read current gain/attenuation levels or to daisy chain multiple CS3310's. See Figure 1 for proper setup and hold times for $\overline{\text{CS}}$, SDATAI, SCLK, and SDATAO. SCLK and SDATAI should be active only during volume setting operations to achieve optimum dynamic range



L0 = Left Channel Least Significant Bit R0 = Right Channel Least Significant Bit
L7 = Left Channel Most Significant Bit R7 = Right Channel Most Significant Bit
SDATAI is latched internally on the rising edge of SCLK
SDATAO transitions after the falling edge of SCLK
SDATAO bits reflect the data previously loaded into the CS3310

Figure 3. Serial Port Timing

Daisy-chaining

Digitally controlled, multi-channel audio systems often result in complex address decoding which complicates PCB layout. This is greatly simplified with the daisy-chaining capability of the CS3310.

In single device operation, volume control data is loaded into the 16-bit shift register by holding the $\overline{CS}$ pin low for sixteen SCLK pulses and then latched on the rising edge of $\overline{CS}$. The previous contents of the shift-register are shifted through the register and out SDATAO during the process.

Multi-channel operation can be implemented as shown in Figure 4 by connecting the SDATAO of device #1 to the SDATAI pin of device #2. In this manner multiple CS3310s can be loaded from a single serial data line without complex addressing schemes. Volume control data is loaded by holding $\overline{CS}$ low for 16 x N SCLK pulses, where N is the number of devices in the chain. The 16 bits clocked into device #1 on SCLK pulses 1-16 are clocked into device #2 on SCLK pulses 17-32. The CS3310s are simultaneously updated on the rising edge of $\overline{CS}$ following 16 x N SCLK pulses.

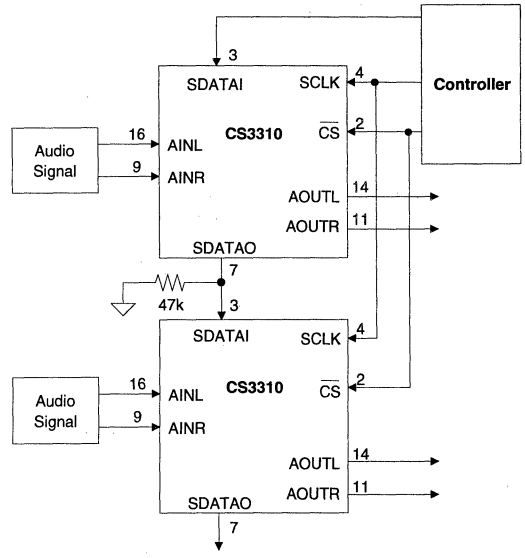


Figure 4. Daisy Chaining Diagram

Changing the Analog Output Level

Care has been taken to ensure that there are no audible artifacts in the analog output signal during volume control changes. The gain/attenuation changes of the CS3310 occur at zero crossings to eliminate glitches during level transitions. The zero crossing for the left channel is the voltage potential at the AGNDL pin; the voltage potential at the AGNDR pin defines the right channel zero crossing.

A volume control change occurs after chip select latches the data in the volume control data register and two zero crossings are detected. If two zero crossings are not detected within 100ms of the change in $\overline{CS}$, the new volume setting is implemented. The zero crossing enable pin, ZCEN, enables or disables the zero crossing detection function as well as the 100ms timeout circuit.

Input Code (Left or Right Channel)	Gain or Attenuation (dB)
11111111	+31.5
11111110	+31.0
•	•
•	•
11000000	0
•	•
00000010	-95.0
00000001	-95.5
00000000	Software Mute

Figure 5. Input Code Definition

Analog Inputs and Outputs

The maximum input level is limited by the common-mode voltage capabilities of the internal op-amp. Signals approaching the analog supply voltages may be applied to the AIN pins if the internal attenuator limits the output signal to within 1.25 volts of the analog supply rails.

The outputs are capable of driving 600 ohm loads to within 1.25 volts of the analog supply rails and are short circuit protected to 20 mA.

As with any adjustable gain stage the affects of a DC offset at the input must be considered. Capacitively coupling the analog inputs may be required to prevent "clicks and pops" which occur with gain changes if an appreciable offset is present.

Mute

Muting can be achieved by either hardware or software control. Hardware muting is accomplished via the $\overline{\text{MUTE}}$ input and software muting by loading all zeroes into the volume control register.

$\overline{\text{MUTE}}$ disconnects the internal buffer amplifiers from the output pins and terminates AOUTL and AOUTR with 10kΩ resistors to ground. The mute is activated with a zero crossing detection or a 100ms timeout to eliminate any audible "clicks" or "pops". $\overline{\text{MUTE}}$ also initiates an internal offset calibration.

A software mute is implemented by loading all zeroes into the volume control register. The internal amplifier is set to unity gain with the amplifier input connected to the maximum attenuation point of the resistive divider, AGND.

A "soft mute" can be accomplished by sequentially ramping down from the current volume control setting to the maximum attenuation code of all zeroes.

Power-Up Considerations

Upon initial application of power, the $\overline{\text{MUTE}}$ pin of the CS3310 should be set low to initiate a power-up sequence. This sequence sets the serial shift register and the volume control register to zero and performs an offset calibration. The device should remain muted until the supply voltages have settled to ensure an accurate calibration.

The offset calibration minimizes internally generated offsets and ignores offsets applied to the AIN pins. External clocks are not required for calibration.

Although the device is tolerant to power supply variation, the device will enter a hardware mute state if the power supply voltage drops below approximately ±3.5 volts. A power-up sequence will be initiated if the power supply voltage returns to greater than ±3.5 volts.

Grounding and Power Supply Decoupling

As with any high performance device which contains both analog and digital circuitry, careful attention to power supply and grounding arrangements must be observed to optimize performance. Figure 2 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply and VA- connected to a clean -5 volt supply. VD+ powers the digital interface circuitry and should be powered from VA+ as shown to minimize latch-up possibilities. Decoupling capacitors should be located as near to the CS3310 as possible, see Figure 6.

The printed circuit board layout should have separate analog and digital regions with individual ground planes. The CS3310 should straddle the ground plane break with pins 1-8 residing in

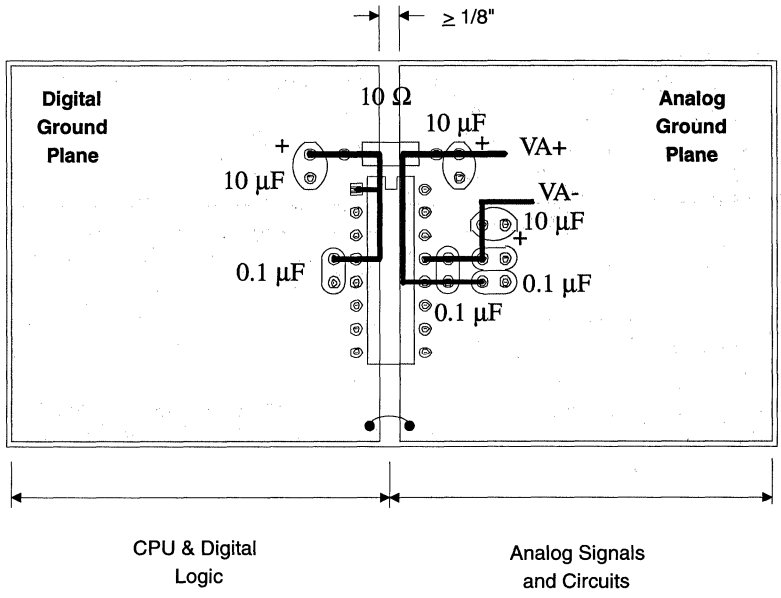


Figure 6. Recommended 2-Layer PCB Layout

the digital region and pins 9-16 residing in the analog region as shown in Figure 6. Care should be taken to ensure that there is minimal resistance in the analog ground leads to the device to prevent any change in the defined attenuation settings. Extensive use of ground plane fill on both the analog and digital sections of the circuit board will yield large reductions in radiated noise effects. An applications note "*Layout and Design Rules for Data Converters*" is printed in the Application section of the Crystal data book and contains many guidelines for the optimum layout of mixed signal devices.

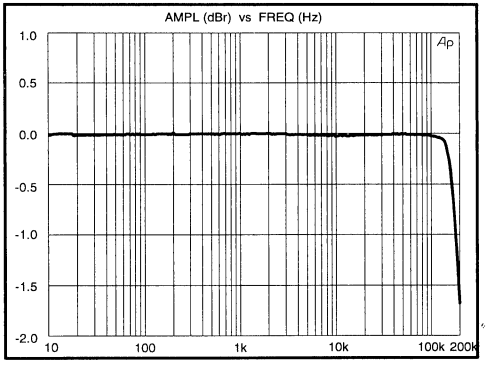


Figure 7. Frequency Response Full scale Input

Figure 7 displays the CS3310 frequency response with a 3.75 Vp output.

Figure 8 shows the frequency response with a .375 Vp output.

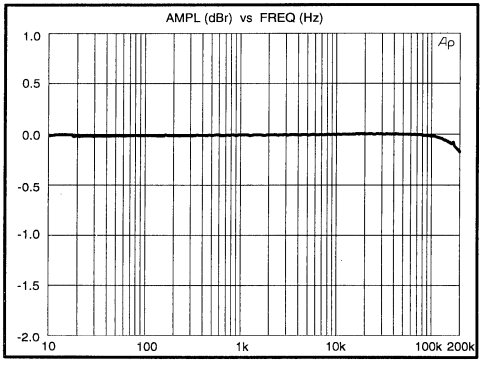


Figure 8. Frequency Response -20 dB Input

Figure 9 is the Total Harmonic Distortion + Noise vs amplitude at 1 kHz. The upper trace is the THD+N vs amplitude of the CS3310.

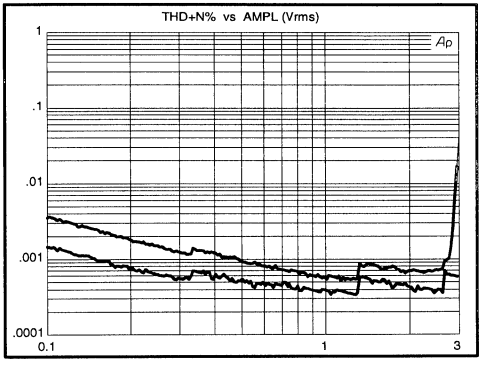


Figure 9. THD+N vs AMP

The lower trace is the THD+N of the Audio Precision System One generator output connected directly to the analyzer input. The System One panel settings are identical to the previous test. This indicates that the THD+N contribution of the Audio Precision actually degrades the measured performance of the CS3310 below 2.7 Vrms signal levels.

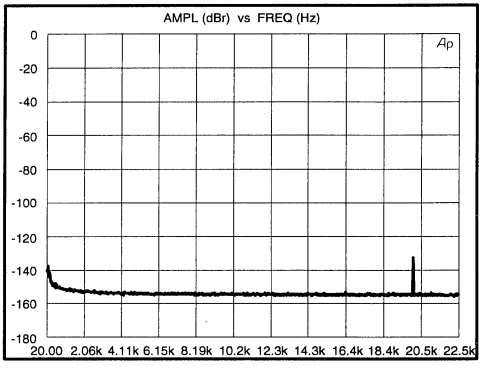


Figure 10. 20 kHz Crosstalk

Figure 10 is a 16k FFT plot demonstrating the crosstalk performance of the CS3310 at 20 kHz. Both channels were set to unity gain. The right channel input is grounded with the left channel driven to 2.65 Vrms output at 20 kHz. The FFT plot is of the right channel output. This indicates channel to channel crosstalk of -130 dB at 20 kHz.

7

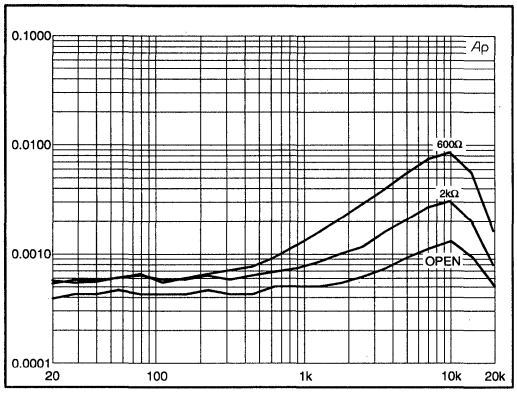


Figure 11. THD+N vs. Frequency
LOAD = 600 ohm, 2 kohm, open ckt

Figure 11 is a series of plots which display the unity-gain THD+N vs Frequency for 600 ohm, 2 kohm and infinite load conditions. The output was set to 2 Vrms. The Audio Precision System One was bandlimited to 22 kHz.

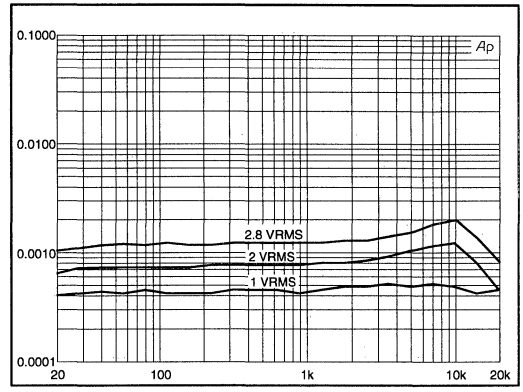
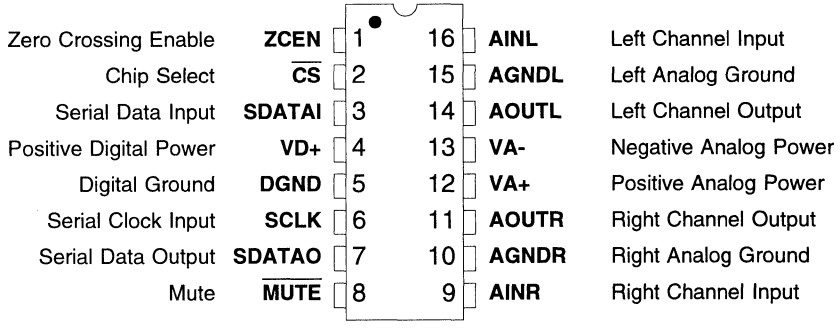


Figure 12. THD+N vs. Frequency
Output levels of 1, 2 and 2.8 Vrms

Figure 12 is a series of plots which display the unity-gain THD+N vs Frequency for 1, 2 and 2.8 Vrms output levels. The output load was open circuit. The Audio Precision System One was bandlimited to 22 kHz.

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, Pin 12.
Positive analog supply. Nominally +5 volts.

VA- - Negative Analog Power, Pin 13.
Negative analog supply. Nominally -5 volts.

AGNDL - Left Channel Analog Ground, Pin 15.
Analog ground reference for the left channel.

AGNDR - Right Channel Analog Ground, Pin 10.
Analog ground reference for the right channel.

VD+ - Positive Digital Power, Pin 4.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, Pin 5.
Digital ground for the digital section.

Analog Inputs and Outputs

AINL, AINR - Left and Right Channel Analog Inputs, Pins 16, 9.
Analog input connections for the left and right channels. Nominally ±3.75 volts for a full scale input.

AOUTL, AOUTR - Left and Right Channel Analog Outputs, Pins 14, 11.
Analog outputs for the left and right channels. Nominally ±3.75 volts for a full scale output.

Digital Pins

SDATAI - Serial Data Input, Pin 3.

Serial input data that sets the analog output level of the left and right channels. The data is formatted in a 16-bit word. The first eight bits clocked into this pin control the analog output level for the right channel, and the second eight bits clocked into the device control the analog output level for the left channel. The data is clocked into the CS3310 by the rising edge of SCLK.

SDATAO - Serial Data Output, Pin 7.

Serial output data that provides daisy-chaining of multiple CS3310's. This serial output will output the previous sixteen bits of volume control data that were clocked into the SDATAI pin.

SCLK - Serial Input Clock, Pin 6.

Serial clock that clocks in the individual bits of serial data from the SDATAI pin. This clock is also used to clock out the individual bits from the SDATAO pin. The SDATAI data is latched on the rising edge, and SDATAO data is clocked out on the falling edge.

$\overline{\text{CS}}$ - Chip Select, Pin 2.

When high, the SDATAO output is held in a high impedance state. A falling transition defines the start of the 16-bit volume control word into the device. The 16-bit input data is latched into the control register on the rising edge of $\overline{\text{CS}}$.

$\overline{\text{MUTE}}$ - Mute, Pin 8.

Forces both the left and right analog output channels to ground. An offset calibration is initiated following the low transition of $\overline{\text{MUTE}}$. Calibration requires a minimum mute period of 2ms.

ZCEN - Zero Crossing Enable , Pin 1.

This pin enables or disables the zero crossing detection and timeout function used during analog output level transitions. A high level on this pin enables the zero crossing detection function. A low level on this pin disables the zero crossing detection.

PARAMETER DEFINITIONS

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth with the input grounded. Units in decibels.

Total Harmonic Distortion plus Noise - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

CRYSTAL
Semiconductor Corporation

CDB3310

Evaluation Board for CS3310

Features

- Demonstrates recommended layout and grounding arrangements
- On-board or externally supplied system control
- Buffered PC Control Interface
- Digital and Analog Patch Areas

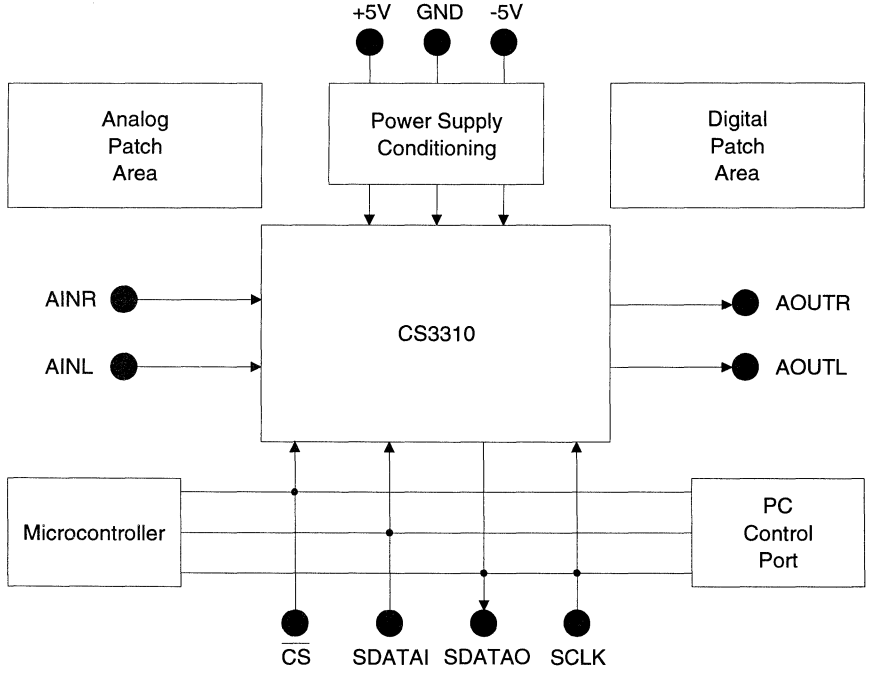
General Description

The CDB3310 evaluation board allows fast evaluation of the CS3310 stereo digital volume control. The board generates all control signals. Evaluation requires a low-distortion signal source and a power supply.

The evaluation board may be configured to accept external timing signals for operation in a user application during system development. The CDB3310 also provides a PC compatible control port for user software development.

Analog inputs and outputs are standard RCA phono plugs.

ORDERING INFORMATION: CDB3310



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CDBCAPTURE

Data Capture and Interface Board for a PC

Features

- Measurement Tool used for the evaluation of Crystal Semiconductor Analog to Digital Converters.
- Easy interface to a PC Compatible computer.
- LabWindows® evaluation software for data analysis.
- Includes time domain, FFT and noise distribution histograms.
- Can be used to evaluate the ADC in your equipment.

General Description

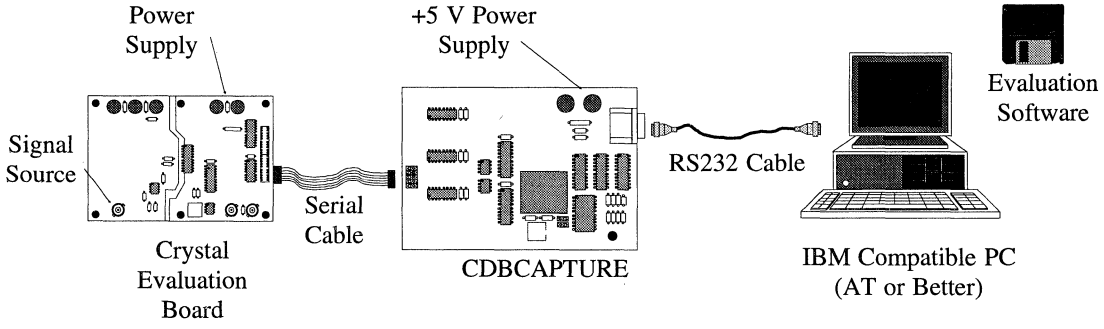
The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor analog to digital converter to a PC compatible computer. Digital data is collected in a high speed digital FIFO, then transferred to the PC over a serial COM port. Evaluation software is included to analyze the data and demonstrate the analog to digital converter's performance.

The CAPTURE interface board is designed to be easily interfaced to Crystal Semiconductor Evaluation boards. Application software is loaded via the PC's serial COM port. The software adjusts the CAPTURE interface board for the appropriate signal timing and polarity, coding format and number of bits, thus allowing the same hardware to be used with a variety of Crystal Semiconductor ADCs.

Evaluation software is included with the CAPTURE interface board. The software is developed with LabWindows, a software development system for instrument control, data acquisition, and analysis applications. The evaluation software permits time domain, frequency domain and histogram analysis.

Ordering Information: CDBCAPTURE

7



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

OVERVIEW

The CAPTURE interface board captures a block of A/D converter output data, which is then transferred to the PC. The CAPTURE board buffers the high speed digital data in a FIFO and transfers the data to the PC via the COM port. Figure 1 is a functional block diagram which illustrates the data acquisition process.

The setup for the CAPTURE board is simple. A serial cable is connected from the evaluation board to the CAPTURE board. An RS232 cable is connected from the CAPTURE board to a PC COM port. A +5V power supply is required. Upon reset, the microcontroller (uC) on the CAPTURE board begins executing boot code from its internal EPROM. The boot code monitors the uC's serial port for application software from the PC and stores the application software in SRAM. The application software is specific for the type of A/D converter being used. When the transfer is complete, the uC executes program code out of the SRAM and turns on the LED.

With the uC running the application software, the data collection process can begin. The collection process is started by a command sent from the PC to the CAPTURE board. When the collection command is received, the CAPTURE board synchronizes itself to the FRAME signal and begins capturing data from the ADC. The serial cable signals are optically isolated for optimum noise isolation and the data is stored in a serial FIFO. The writing to the FIFO is controlled by the µC and Counter/Control circuit.

When the data sample set has been collected and stored in the serial FIFO, the uC reads the data out of the FIFO and converts the format to 2's complement if required. The data in 2's complement format is then transferred to the PC via the RS232 cable connected the PC's COMM port.

The evaluation software developed with LabWindows performs post processing of the digitized signal (source code included). Time plots, FFT analysis and noise analysis are included. The software operates upon sample sets as large as 8192. For more sophisticated analysis, the LabWindows development system can be purchased from National Instruments (512-794-0100).

CS5012A	CS5126	CS5336	CS5503
CS5014	CS5317	CS5338	CS5505
CS5016	CS5322	CS5339	CS5506
CS5030	CS5326	CS5345	CS5507
CS5031	CS5327	CS5349	CS5508
CS5101A	CS5328	CS5389	
CS5102A	CS5329	CS5501	

Crystal Parts Supported by Capture Board
***Future products will be added with software updates**

Packaging List: CDBCAPTURE Interface Board
Serial Cable
EIA232 Cable (RS232)
3.5" 1.44 MB Software Diskette

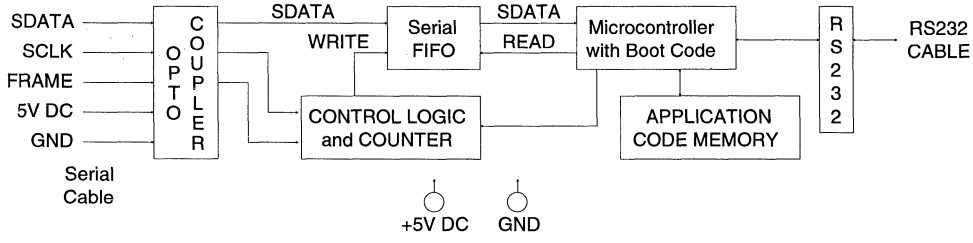


Figure 1. Functional Block Diagram

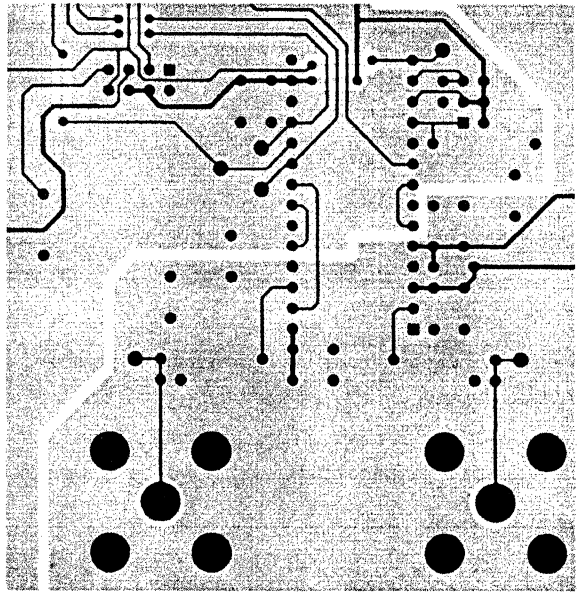
This section contains a collection of Audio Engineering Society (AES) papers, application notes and other papers, all authored by Crystal engineers. Much useful information is presented here. If you are considering using a Crystal Semiconductor audio product, please read the relevant papers presented below.

CONTENTS

Application Note

Layout and Design Rules for Data Converters

by
Ron Knapp & Steven Harris



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Here is a list of guidelines for optimum printed circuit board layout for Crystal ADC's, DAC's, and codecs. Use these pages as a checklist during and after layout by checking the boxes when each line item is OK. Remember, Crystal offers a free schematic and layout review service. Try hard to use this service before building your first prototype board. Comments or additional items are very welcome.

☐ 1) Partition the board with all analog components grouped together in one area and all digital components in the other. Common power supply related components should be centrally located.

☐ 2) Have separate analog and digital ground planes on the same layer, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes should be >1/8".

☐ 3) Mixed signal components, including the data converters, should bridge the partition in the ground plane with only analog pins in the analog area, and only digital pins in the digital area. Rotating the data converter can often make this task easier.

For our serial codecs, the device should be placed over the analog ground plane, positioned next to the ground plane split. The digital pins should be next to the split, with the digital traces crossing directly over into the digital region of the board. The analog ground pins and digital ground pins should be connected with zero impedence (same ground plane). See the CS4215 and CS4216, CDB4215 and CDB4216 data sheets for examples.

☐ 4) Analog and digital ground planes should only be connected at one point (in most cases). Have vias available in the board to allow alternative connection points.

☐ 5) The analog to digital ground plane connection should be near to the power supply, or near to the power supply connections to the board, or near to the data converter. In the case of multiple converters, leave jumper options at each converter.

☐ 6) Analog power and analog signal traces should be over the analog ground plane.

☐ 7) Digital power and digital signal traces should be over the digital ground plane.

☐ 8) Keep digital signal traces, especially the clock, as far away from analog input and voltage reference pins as possible.

☐ 9) Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connection to pins with wide traces to reduce impedance (for example, between pins 1 and 28 at the top end of the IC package in the case of the VREF decoupling capacitors for the CS5326 family, the CS5336 family and the CS4328).

☐ 10) If both large electrolytic and small ceramic capacitors are recommended, make the small ceramic capacitor closest to the IC pins. For multi-layer pc boards, make the connections to the converter and to the capacitors on the same layer (this avoids the additional impedence of vias).

☐ 11) All filtering capacitors in the signal path should be NPO/COG dielectric. BX/X7R dielectric is OK for DC voltages where voltage coefficient is not a factor.

☐ 12) All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors are OK for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor. Avoid wire wound resistors and potentiometers.

☐ 13) Avoid multiple crystal oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D or D/A sampling clock.

☐ 14) When using converters with DSP IC's, operate everything from one crystal using dividers if necessary.

☐ 15) In systems requiring multiple crystals for selectable sampling frequencies, enable only one at a time. Shut off all other oscillators by removing power. Make sure other oscillators are off either with an active crowbar on Vcc or very high impedance switch. Often the leakage from a transistor or FET which is not completely off is sufficient for the oscillator to produce a low level output frequency.

☐ 16) When using DC-DC switching regulators, synchronize the switching frequency to the A/D if possible. This applies to CMOS chopper amplifiers as well.

☐ 17) Avoid connecting the clock source oscillator to the converter sampling clock input through analog multiplexers, PAL's, gate arrays, opto-couplers or circuits which can cause jitter.

☐ 18) Locate the crystal or oscillator close to the converter. Avoid overshoot and undershoot on the master clock for the converter. This is particularly important for the CS5326 family, where the master clock (CLKIN) goes directly into the analog modulator die.

☐ 19) Use buffers for digital signals directly to or from the converter to connectors which go off the board.

☐ 20) In the case of piggy-back boards, or boards which plug into a slot adjacent to other boards, consider the circuits which will be above or below the converter as sources of interference. A mu-metal screen may be required.

☐ 21) For delta sigma converters, make sure that potential interfering clocks are not in sensitive frequency regions. Sensitive regions are defined as ± passband either side of multiples of the input sample rate. Two examples are : a) for a CS5336 operating at 48 kHz word rate, the frequencies to avoid are (N X 3.072MHz) ±24 kHz. b) for a CS5501 with a 4 MHz crystal, the frequencies to avoid are (N X 16 kHz) ± 10 Hz. Frequencies which are synchronous to the input sample rate will not cause problems, since they will be converted to dc, and calibrated out.

☐ 22) For boards with more than 2 layers, do not overlap analog related and digital related planes. Do not have a plane which crosses the split between the analog ground plane region and the digital ground plane region.

☐ 23) For CS5326, CS5336 & CS5349 families, supply VD+ to the device via a separate trace connected to where the +5V digital supply enters the board. Connect no other logic to this trace. Alternatively, provide a 10 µH inductor in series with VD+, near to the ADC.

☐ 24) For boards with both A/D converters and D/A converters, provide a means for testing each function separately. Possible methods include providing a header to allow access to the digital data paths, and allowing for easy attachment of a CS8402 and CS8412 AES/EBU transmitter and receiver parts.

☐ 25) Terminate unused op-amps in dual and quad packs by grounding the + input and connecting the - input to the output.

☐ 26) Digital control lines which must cross into the analog region should be as short as possible and should be mostly static. For example, digital gain and analog mux control lines.

☐ 27) Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane. These regions should not be left floating, which only make the interference worse. Using ground plane fill has been shown to reduce digital to analog coupling by up to 30 dB.

☐ 28) The pins of DIP or SOIC packages should not have ground plane in between adjacent pins.

☐ 29) In systems using a delta-sigma converter, then avoid the use of clocks (particularly the serial bit clock) at half the frequency of the input sample rate. If this frequency interferes with the voltage reference, then tones can occur.

☐ 30) Do not surround the analog region with digital components. Do not surround the digital region with the analog region

Application Note

ADC Input Buffer and Protection Techniques

by
Steven Green

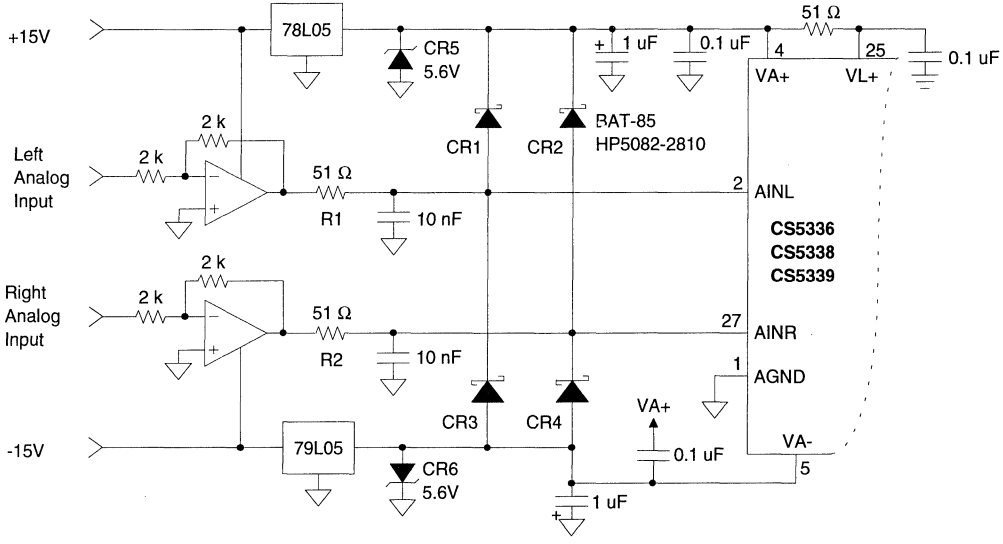

Figure 1. ADC Input Protection ±15V Op-Amp

Introduction

The design of input buffer and protection circuits for analog-to-digital-converters (ADC) is critical to an optimized and reliable data acquisition system. The Crystal Semiconductor application note "ADC Input Buffers" covered this area well and the system designer should review this information. Since the publication of "ADC Input Buffers" there have been many requests for additional information and circuits relating to ADC input protection. This application note describes suitable buffer/protection circuits for the CS5336 family of converters. The techniques described are equally applicable to the other families of Crystal analog-to-digital converters.

SCR Latch-up

SCR latch-up has been defined as "the creation of a low impedance path between the power supply rails by the triggering of parasitic, four-layer bipolar structures (SCR's) inherent in CMOS input and output circuitry." This is a self-sustaining condition and once latched, a CMOS device will remain so regardless of the I/O pin voltages until the power supply voltages are removed. The excessive power dissipation during latch-up may also damage the device. Latch-up is most often caused by forcing current into the inputs or outputs of a CMOS device by applying voltages greater than the power supply rails. When powered, Crystal Semiconductor

ADC's are extremely immune to latch-up because of the amount of current required to initiate a latch. Problems can arise when input voltages greater than the instantaneous power supply voltages are applied during power-up. A less common but equally damaging SCR condition can occur when power-supply voltages exceed the absolute maximum specified value. There are several protection techniques available to the designer each with their own advantages and disadvantages.

Protection Techniques

The goal of input protection is to guarantee that the ADC input voltage never exceeds the supply voltages of the converter. This is accomplished with an op-amp buffer between the "outside" world and the ADC input, then limiting the ADC input voltage excursions to the range bounded by the converter power supply voltages.

Method I

There are many high quality op-amps available to the design engineer for use as input buffers and the majority of these have been designed to operate from power supplies greater than ±5V. The use of the required multiple supplies presents potential problems. It is possible for the ADC analog input to experience voltages greater than the ADC supplies either during signal amplitude excursions, transient power-on conditions or op-amp failure. Several methods are available to clamp the ADC input voltage and are discussed in detail in references 1-7. Figure 1 shows a diode-clamped input buffer circuit utilizing multiple supplies. The type of diode selected for CR1-CR4 is crucial and must be evaluated using the following criteria:

1) Forward-biased voltage characteristics. Schottky diodes are preferred due to their low forward-biased voltage characteristics.
2) Reverse-bias leakage current. The effects of voltage dependent leakage currents are proportional to circuit impedences and can cause distortion. Leakage currents will also vary with temperature and must be evaluated over the intended temperature operating range.
3) Reverse-bias capacitance. Voltage dependent junction capacitance can cause distortion and must be insignificant in comparison to the circuit component values.

Figure 2 is a comparison %THD plot of the circuit of Figure 1 with and without 1N5818 Schottky diodes installed for CR1-CR4. Note the increase in %THD resulting from diode capacitance. Figure 3 is a comparison %THD plot of the circuit of Figure 1 with and without Philips BAT-85 Schottky diodes. Note the lack of distortion produced by the addition of suitable protection components. Hewlett-Packard 5082-2810 diodes give similar results.

Notes for Method 1

The values of R1 and R2 were selected to optimize the source impedance for the CS5336 and utilize the current limiting characteristics of the op-amp.

Clamping circuits with diodes in the feedback loop of the op-amp work well for signal clamping but are not effective for power-on transient or op-amp failure conditions. These circuits are not recommended for protection.

ADC Power Supply Overvoltage

Standard 3-terminal regulators are designed to either source (78L05) or sink (79L05) current but not both. It is possible to raise the ADC supply voltage above the regulation voltage through the Schottky diodes during error conditions. The 5.6V zener diodes CR5 and CR6 are included to prevent the supply voltages from exceeding the maximum specified value and damaging the converter.

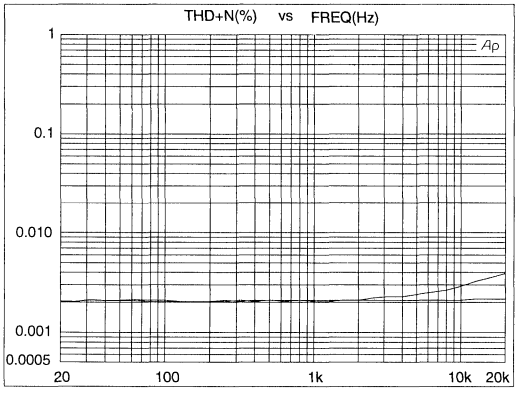

Figure 2. %THD Effects of 1N5818 Schottky Diodes with NE5532 Op-amp

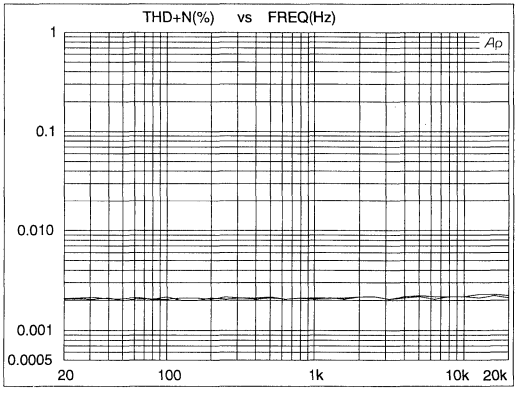

Figure 3. %THD Effects of BAT-85 Schottky Diodes with NE5532 Op-amp

Method II

The goals of input protection can also be achieved by powering the input buffer from the same supplies as the converter as shown in Figure 4. This circuit requires fewer components than the circuit of Figure 1 and the use of common power supplies guarantees that the op-amp output will not exceed the ADC supply voltages. However, the required analog voltage to achieve full scale digital output for the CS5336 is typically ±3.68 V and the majority of op-amps do not have this output capability with ±5V supplies.

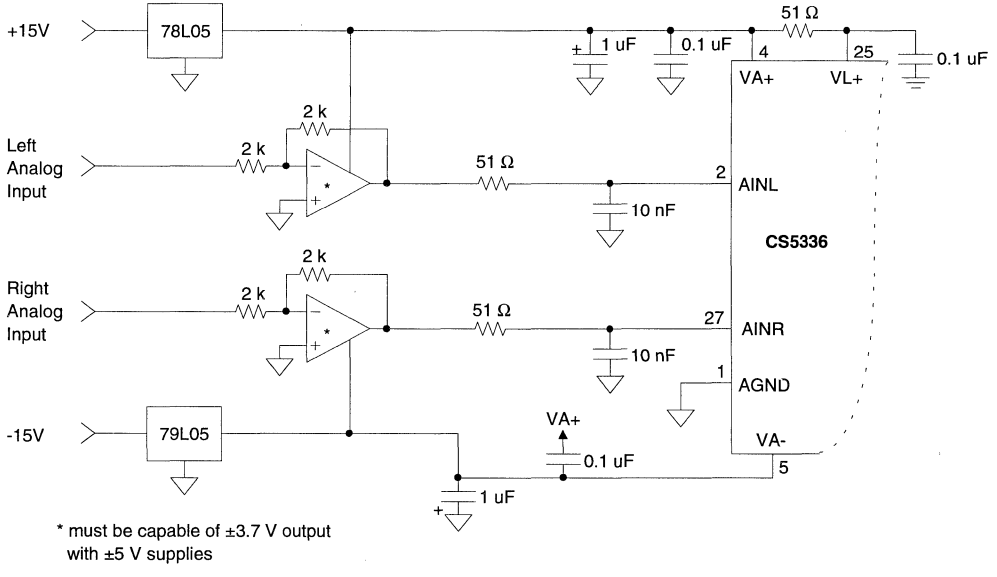

Figure 4. ADC Input Protection ±5V Op-Amp

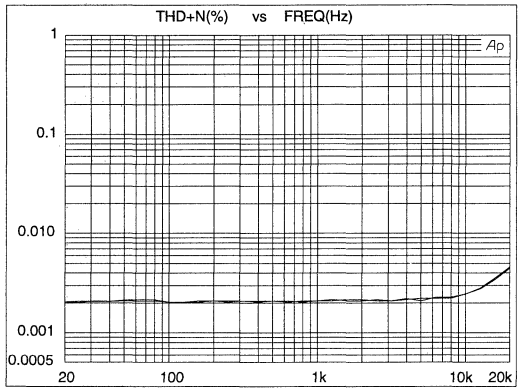

Figure 5. %THD Effects of Power Supply Variation for MC33078 at ±15V and ±5V

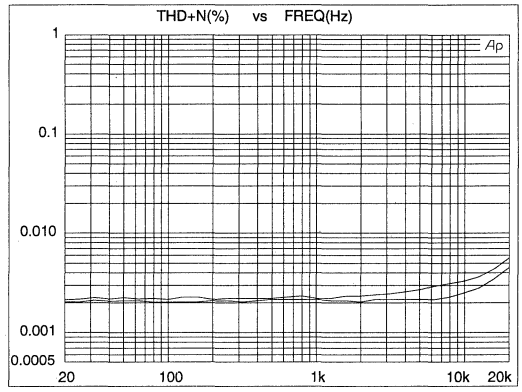

Figure 6. %THD Effects of Power Supply Variation for MC33078 at ±15V and ±4.75V

The Motorola MC33078/9 is a viable contender for this application. Figure 5 shows the %THD vs Frequency of the MC33078 with ±15 and ±5V supplies operating at 3.68 Vp. Note the lack of performance degradation resulting from the reduced supplies.

The power supply voltages could be as low as 4.75V due to the 5% tolerance of the 78L05/79L05. Figure 6 shows the increased %THD of the MC33078 at this supply voltage.

Due to the transient nature of audio signals, digital audio systems are generally operated at average levels 10 to 20 dB below full scale. This is to allow sufficient headroom to handle high amplitude transient signals. The increase in distortion at full scale due to regulator tolerances could be considered insignificant. If required, 2% regulators will avoid this increase in distortion.

Conclusion

Two circuits have been described which utilize effective protection techniques. Use of either of these circuits or the techniques described will insure that the performance and reliability of a data acquisition system will not be limited by the input buffer and protection circuits.

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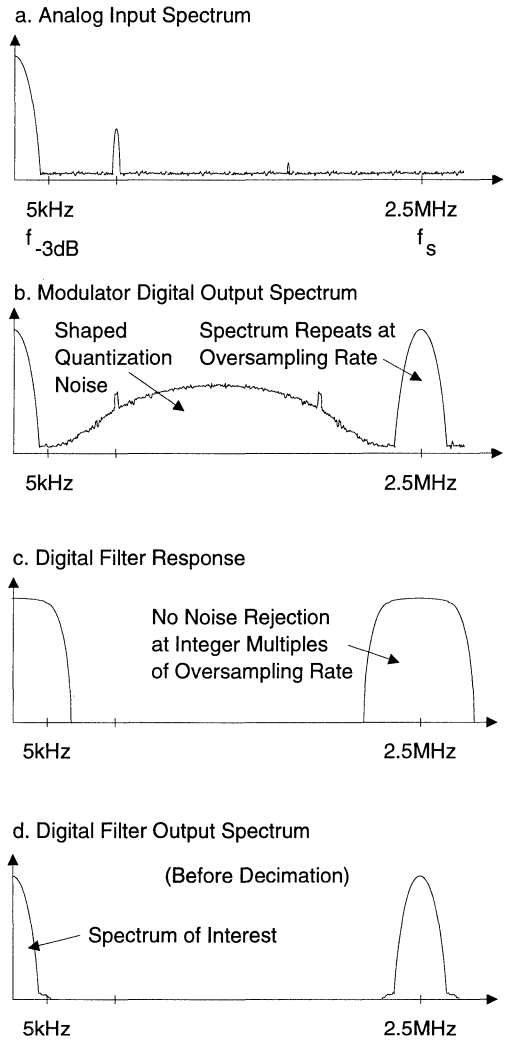
Delta Sigma A/D Conversion Technique Overview



8

SECTION A

OVERVIEW: DELTA-SIGMA MODULATION

Although developed over two decades ago, delta-sigma modulation has only recently achieved commercial implementation. The technique utilizes oversampling and digital filtering to achieve high performance in both A/D conversion and filtering at low cost. The advent of commercial delta-sigma converters is due in most part to recent advances in mixed analog-digital VLSI technology. Precision analog circuitry can now be integrated on the same chip with powerful digital filters.

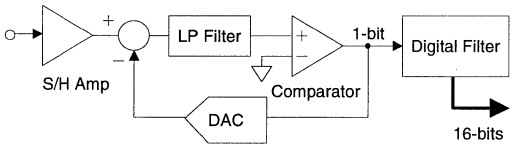


Figure A1. Delta-Sigma ADC

In a delta-sigma ADC, the same digital filter used in the A/D conversion process can perform system-level filtering with performance unachievable in analog form. Therefore, the first commercial delta-sigma converters have been targeted at applications demanding high-performance filtering (high-end modems, digital audio, geophysical exploration, etc).

This application note uses the CS5317 voice band A/D converter for examples. See the end of this application note for implementation details for the CS5317, CS5501, CS5326 A/D converters.

Fundamentals

A delta-sigma ADC consists of two basic blocks: an analog modulator and a digital filter (see Figure A1). The fundamental principle behind the modulator is that of a single-bit A/D converter embedded in an analog negative feedback loop with high open loop gain. The modulator loop oversamples and processes the analog input at a rate much higher than the bandwidth of interest. The modulator's output provides small packages of information (that is, 1-bit) at a very high rate and in a format that the digital filter can process to extract higher resolution (such as 16-bits) at a lower rate.

The delta-sigma converter's basic operation can be analyzed in either the time domain, or (more conventionally) in the frequency domain.

Time-Domain Analysis

The basic operation of a delta-sigma modulator can be understood more intuitively by demonstration. A simple, first-order modulator (that is, a conventional voltage-to-frequency converter) is shown in Figure A2. (Note: a modulator's order indicates the number of orders of analog filtering - or integration - in the loop). Full-scale inputs are ± 1V and three nodes are labeled V_1, V_2, and V_3. The output of the comparator, node V_3, is the output of the loop and is also converted by the 1-bit DAC into plus or minus full-scale (+1V or -1V).

At the differential amplifier, the +1V or -1V is subtracted from the analog input voltage. The result, the voltage at node V_1, is input to the integrator. The integrator acts as an analog accumulator; ie. the input voltage at node V_1 is added to the voltage on node V_2 which becomes the new voltage on node V_2. Node V_2 is then com-

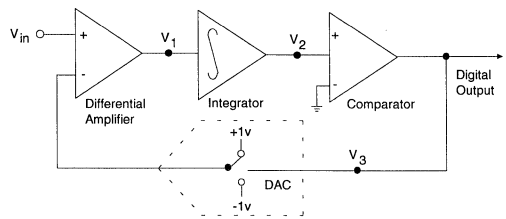


Figure A2. 1st-order Delta-Sigma Modulator

pared to ground. If it is greater than ground, node V_3 becomes +1V; if it is less than ground, V_3 becomes -1V. Each operation occurs once during each clock cycle.

In the example shown in Table A1, all nodes are initially set to zero, and the analog input voltage is assumed to be 0.6V. Since all nodes are identical in clock cycles two and seven, the period defined by cycles two to six will repeat if the analog input remains unchanged. The average value of modulator outputs (at node V_3) during that period, 0.6, yields a numerical representation of the analog input.

Clock Period	V_1	V_2	V_3	Period Avg
0	0	0	0	
1	0.6	0.6	1	
2	-0.4	0.2	1	
3	-0.4	-0.2	-1	
4	1.6	1.4	1	0.6
5	-0.4	1.0	1	
6	-0.4	0.6	1	
7	-0.4	0.2	1	
8	-0.4	-0.2	-1	

Table A1. Modulator Walk-Through

With conventional voltage-to-frequency converters a digital counter is used to extract the information in the VFC's 1-bit output. Pulses are counted over a specified period, effectively creating a digital averaging (or integrating) filter. The final count represents the average analog input value during the integrating period.

Advanced delta-sigma converters use higher-order modulators and more powerful digital filters. For example, the CS5317 uses a second-order modulator. The pattern of transitions in its 1-bit output provides more useful information regarding higher resolution at higher frequencies.

However, a more sophisticated digital filter than a counter is needed to interpret that information. A digital FIR filter is basically a rolling, weighted average of consecutive samples (see Appendix B). An averaging filter weights all samples equally. By applying a more sophisticated weighting function to the 1-bit signal, a digital FIR filter can assemble an N-bit output (with 2^N possible values) *without having to wait for 2^N samples.*

The Charge-Balance Name

Delta-sigma ADC's are also known by other names - sigma delta and charge-balance are two examples. The *Charge-Balance* name derives from the fact that the modulator tries to *balance* the analog input with the DAC's output in the negative feedback loop. The charge injected onto the integrator's capacitor from sampling the analog input (see Figure A2) is therefore balanced by the charge injected by the DAC's output. Modulators have been implemented in both switched-capacitor and continuous-time form.

Frequency-Domain Analysis

Since filtering plays a key role in a delta-sigma ADC, it is easier to understand the converter's operation by analyzing it in the frequency domain.

Overview

An A/D converter's resolution determines its dynamic range (or signal-to-noise ratio). Conversely, one can improve a converter's signal-to-noise ratio and thereby increase its effective resolution. The fundamental concept behind delta-sigma converters is to perform a simple, low-resolution A/D conversion and reduce the resulting "quantization noise" (without affecting the frequency band of interest) using analog and digital filtering.

Quantization Noise

The comparator in the delta-sigma modulator loop plays the role of a 1-bit A/D converter. Any A/D converter can represent a continuous analog input by one of only a *finite* number of codes, giving rise to an uncertainty, or quantization error, of up to ± 1/2 LSB. For a consecutive sequence of samples in a waveform, these quantization effects can be modeled as a random noise source under conditions commonly encountered in signal processing applications. (These conditions hold true for delta-sigma modulators). The rms value of the noise source relative to a full-scale input can be shown to equal - (6.02 N + 1.76) dB, for an N-bit resolution converter. Since this error "signal" is totally random (or uncorrelated with the input) it can be assumed to be white, with its energy spread uniformly over the band from dc to one-half the sampling rate.

As a 1-bit ADC, the comparator in a delta-sigma modulator offers (an almost comical) 7.78 dB signal-to-noise ratio. However, the input signal is grossly oversampled (2.5 MHz in the CS5317), thus spreading the quantization noise over a wide bandwidth (1.25 MHz). The noise density in the bandwidth of interest (5 kHz) is therefore reduced.

Noise Shaping

Analog filtering is used in the modulator loop to further reduce noise density in the frequency band of interest by shaping the quantization noise spectrum. The spectrum of the input signal, meanwhile, remains unaltered. Figure A3 shows a modulator loop with analog and digital circuit differences ignored. The comparator is simply shown as a (quantization) noise source, and the analog filtering, which is simply an integrator, assumes the filter response H(f). If the analog input equals zero, then

$$D_{out} = Q(n) - H(f)\, D_{out}$$

$$D_{out} = \frac{Q(n)}{1 + H(f)}$$

The quantization noise at the output is reduced by the open-loop gain of the integrator. At low frequency, the integrator is designed for high open-loop gain, so that quantization noise is reduced. As shown in Figure A4b, the integrator effectively pushes the quantization noise out of the bandwidth of interest and into higher frequencies. Digital lowpass filtering then removes the quantization noise at the higher frequencies without affecting the low-frequency spectrum of interest.

The spectral characteristics of the analog loop filtering dictates the delta-sigma converter's resolution/bandwidth ratio. Higher-order integrators improve noise shaping and allow for higher resolutions at wider bandwidths. The CS5317 uses a second-order modulator for superior noise shaping.

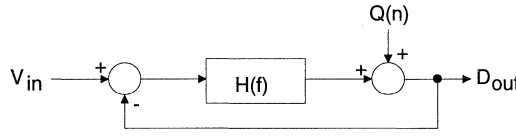


Figure A3. Analog Modulator Model

Digital Filtering

The spectral characteristics of the back-end digital filtering also affects the delta-sigma converter's resolution/bandwidth ratio. Faster roll-off and greater stopband rejection reduces residual quantization noise. Section B offers a detailed explanation of the theory behind digital filtering.

Anti-Alias Requirements

As shown in Figure A4, the input and digital filtering spectrum of any ADC repeats around integer multiples of its sampling rate. A delta-

sigma ADC thus does not provide noise rejection in the region around integer multiples of the sampling rate (± 5 kHz around 2.5 MHz, 5 MHz, 7.5 MHz...). If noise exists in the system in these narrow bands, analog filtering is needed to remove it at the converter's input otherwise it will alias and pass unfiltered to the converter's output.

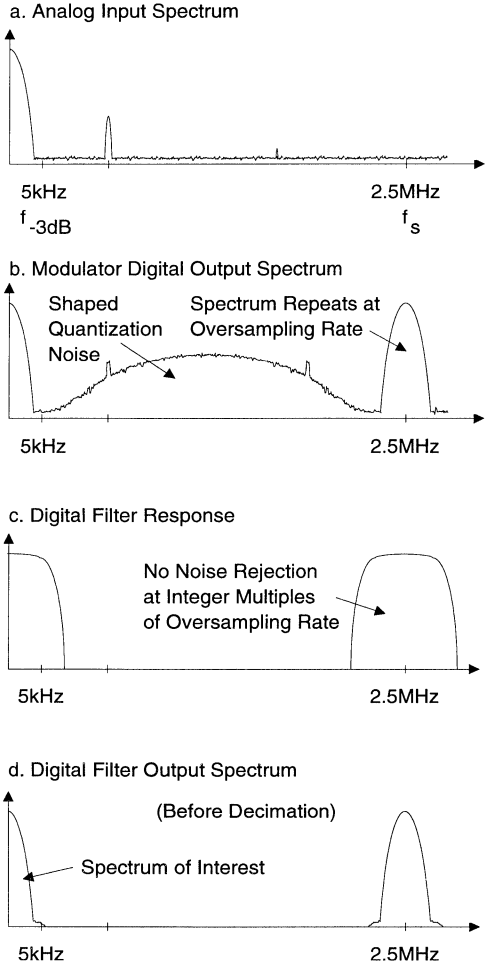


Figure A4. Delta-Sigma Spectral Analysis (Using frequencies taken from the CS5317 A/D Converter)

Since delta-sigma ADC's are grossly oversampled, anti-alias filtering requirements are often trivial. For instance, the CS5317 provides a factor of 500 of oversampling (2.5 MHz/5 kHz). A single-pole, passive RC filter at the CS5317's input is therefore sufficient in most applications.

Decimation

Even though the delta-sigma ADC oversamples and processes analog samples at a frequency well above the bandwidth of interest, it will generally offer its high-resolution output at a much-lower system sampling rate. Any reduction in sampling rate is termed *decimation*. The output can be further decimated at the system level by selectively reading a fraction of the available samples (for instance, every tenth sample). Independent of the decimation ratio, the converter's noise performance (and effective resolution) remains unchanged.

Conversion Accuracy/Performance

Like integrating ADC's and V/F converters, a delta-sigma ADC does not contain any source of nonmonotonicity and thereby offers "theoretically perfect" DNL with no missing codes. The ADC in the modulator is simply a comparator, and the DAC is the positive and negative voltage references. No precision ratio matching is needed as in other medium- or high-speed A/D conversion techniques such as successive-approximation. Useful resolution is limited only by residual quantization noise which, in turn, is determined by coarse analog and high-performance digital filtering.

Linearity error is limited only by imperfections in the input sample/hold. The CS5317 achieves typical nonlinearity of just ± 0.003 % through the use of high-quality on-chip silicon dioxide capacitors with low capacitor voltage coefficient.

SECTION B

OVERVIEW: DIGITAL FILTERING

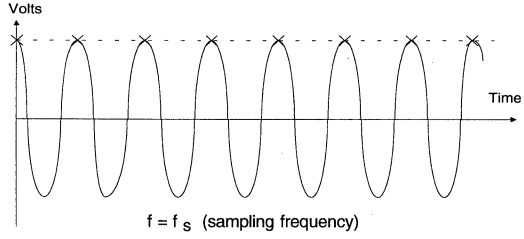
A conventional analog filter implements a mathematical equation using reactive components (capacitors and inductors). A digital filter can implement the same filter equation using two fundamental arithmetic operations: multiplication and addition (or accumulation). A digital filter considers a consecutive sequence of digitized samples a "waveform." It analyzes the relationship between samples, processes the data, and outputs an adjusted waveform.

Digital filters offer ideal stability, repeatability, and potentially perfect performance (linear phase, etc.). Digital filters also remain impervious to environmental conditions, thus providing superior reliability over time and temperature. The major difference compared to analog filters, though, is that digital filters operate on a signal in sampled form.

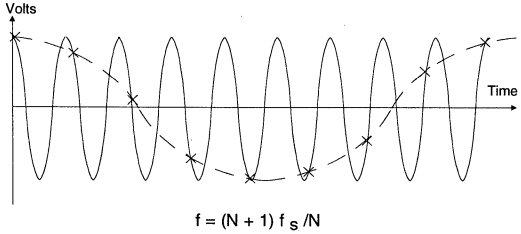
Sampled-Data Theory

A fundamental phenomenon in sampled-data systems is an effect called "aliasing." Basically, *once an analog signal is sampled, its frequency components are no longer uniquely distinguishable.* Figure B1a shows a special case called "dc aliasing." If a signal is sampled precisely at its fundamental frequency, it will always be sampled at the same point on the waveform. It thus becomes indistinguishable from a dc input. Likewise, a signal at twice the sampling frequency (or any integer multiple of f_S) would appear as dc as well. Figure B1b illustrates a more general case of aliasing. Again, two signals at different frequencies become indistinguishable once sampled.

The effect of aliasing in the frequency domain is illustrated in Figure B2. The baseband spectrum (dc to one-half the sampling rate) also "appears" around integer multiples of the sampling rate, *and vice-versa*. In signal processing applications,

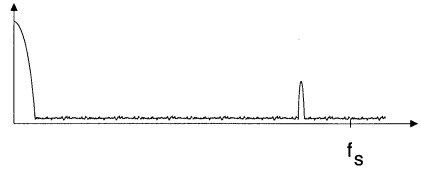


a. dc Aliasing

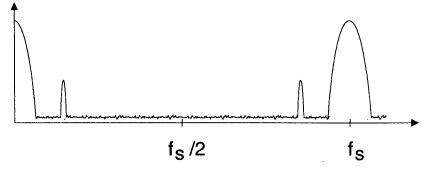


b. General Aliasing

Figure B1. Aliasing in Sampled-Data Systems



a. Continuous-Time Input Spectrum



b. Sampled-Data Spectrum

Figure B2. Sampled-Data Spectrum

anti-alias filtering is used to bandlimit the analog signal before it is sampled. This removes out-of-band components which could be mistaken for important information in the band of interest.

Aliasing is critical in digital filtering. A digital filter is incapable of distinguishing signals in its passband from signals aliasing from around its sampling frequency. Its passband spectrum therefore repeats around integer multiples of the sampling frequency. Take for instance the case of dc aliasing shown in Figure B1a. A digital low-pass filter would treat the signal at f_S as a dc input and pass it with no attenuation. Similarly, if the filter would attenuate the lower-frequency signal in Figure B1b by 10 dB, the higher-frequency signal would receive the same 10 dB of attenuation. The higher-frequency signals in both cases could be selectively filtered only by analog anti-alias filtering *before the signal is sampled.*

Sampling rates are usually set high enough that analog anti-alias requirements become trivial (or perhaps eliminated). Higher oversampling ratios offer greater bandwidth to roll off between the passband and sampling frequency. Noise in the digital domain can be analyzed just as it is in the analog domain. Limiting a system's bandwidth will reduce noise and improve dynamic range.

Digital Filtering

The most popular digital filtering technique is averaging. A sequence of digital samples are simply collected and averaged to produce an output. This reduces noise by limiting the effective noise bandwidth. Averaging yields a (sin x)/x (or sinc) filter response as shown in Figure B3. The zeroes of infinite rejection (at f_S/N, $2f_S/N$, $3f_S/N$, etc.) can be strategically placed by selecting f_S and the number of samples averaged, N, to average over an integral number of periods of critical frequencies (50 Hz, 60 Hz, etc.). Of course, this same principle lies at the heart of integrating ADC's, but the averaging is done in analog form. In both cases greater dynamic range (or resolution) can be achieved by increasing integration time. The trade-off is bandwidth.

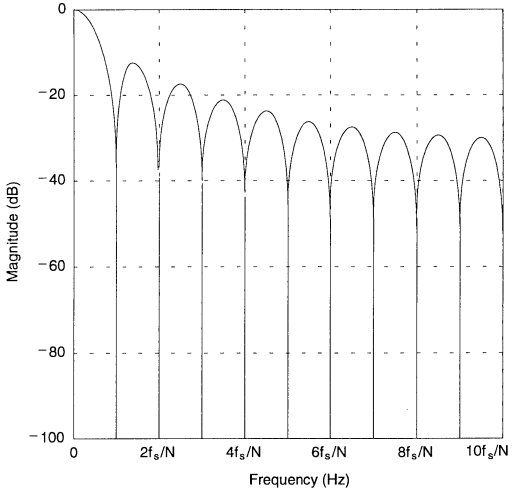


Figure B3. Averaging Filter Response

FIR Filters

Averaging is an elementary example of FIR, or *Finite Impulse Response*, digital filtering. Finite Impulse Response indicates that the filter considers only a *finite* number of inputs to calculate each output. The number of samples determines the *impulse response duration.* For example, a filter which averages ten samples has an impulse response duration of ten. Longer durations indicate more information is considered for each calculation, resulting in a more powerful filter response.

A digital filter's *impulse response* is what determines its filter function. It is basically a weighting function applied to the sequence of samples being considered. The averaging filter is an elementary example of an FIR filter because it uses equal weighting (weight = 1/N where N = # samples). More sophisticated impulse responses extract the information contained in the *relation-*

8

ship between samples. Averaging filters ignore this information.

Figure B4 illustrates how an FIR filter actually implements the impulse response. The two basic operations are multiplication (indicated by ⊗) and addition - or accumulation - (indicated by Σ). Filter coefficients a_0 to a_3 represent the impulse response. The three unit delay elements insure that each output is calculated using the current input sample and the three previous samples. The filter's input, x(n), and output, y(n), are digital words of any length. (For the CS5317, x(n) is 1-bit and y(n) is 16-bits). Each digital output requires one complete *convolution.* For the 4^{th}-order filter shown in Figure B4, one convolution consists of four multiplications and the accumulation of the four products.

FIR filters are often described in terms of *taps.* This terminology hails back to analog transversal filters, which were basically analog implementations of the filter in Figure B4. The analog delay elements were termed taps. The number of taps indicated the filter's impulse duration. The longer the duration, the more powerful the filter.

Decimation

Digital filters often operate with input sampling rates well above the bandwidth of interest. This serves to minimize analog anti-alias filtering requirements. The filter's output rate, however, is generally dropped to a more manageable system sampling rate. Any reduction in sampling rate is termed *decimation.*

To illustrate the decimation process lets return to averaging. A filter which collects ten samples and then averages them to produce one output *decimates by ten.* That is, for an input rate of f_S, the output rate is $f_S/10$. Alternatively, one could use a "rolling average." For each input sample received, an output would be calculated using that sample and the nine previous samples. The sampling rate would therefore remain at f_S with no decimation.

The 4th-order FIR filter in Figure B5 exhibits the same filter response as that in Figure B4, but decimates by a factor of four. In this case, only one multiplication is performed per input cycle. Without any delay elements, the accumulator needs four input cycles to complete one convolution. Output samples are therefore produced at $f_S/4$. Decimation clearly relaxes computational complexity.

Decimation does not affect overall signal-to-noise or dynamic range. For this reason, one can decimate the CS5317's 20 kHz output (by selectively reading a fraction of the available samples) without affecting the converter's noise. However, a digital signal is normally not decimated if additional filtering is to be used to increase dynamic range (and resolution). All noise energy in a sam-

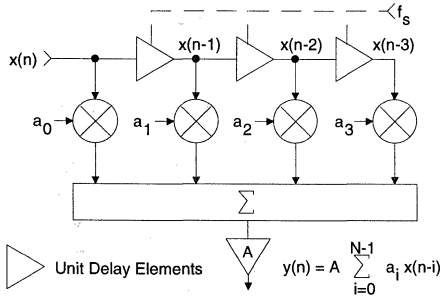


Figure B4. 4^{th}-order FIR Filter

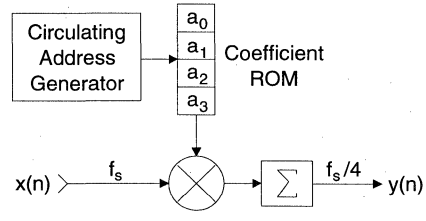


Figure B5. 4^{th}-order FIR Filter with 4X Decimation

pled signal lies between dc and one-half the sampling rate. Lower sampling rates therefore exhibit larger noise *densities* in the bandwidth of interest for a given amount of noise energy due to aliasing.

FIR Characteristics

The only source of inaccuracy in digital filters is rounding errors due to finite word lengths in the computations. If properly designed, a digital filter will not induce linearity, offset, or gain errors.

Aside from their simplicity, FIR filters' most popular characteristic is their ability to implement perfectly linear phase filters. The effect of every input sample on the output is always seen a *fixed* number of cycles later. This processing delay from input to output is termed the filter's *group delay*, and can be shown to equal one-half the impulse response duration.

Unfortunately, FIR filters can only implement zeroes, no poles. Roll-off is therefore limited. Of course, this limitation can be overcome by cascading FIR filters to produce an extraordinarily long impulse duration. (Fortunately stability is not an issue with FIR filters). The trade-off, though, is an extraordinarily long group delay.

IIR Filters

Infinite Impulse Response filters, on the other hand, can implement zeroes *and poles* to achieve high roll-off. Unlike FIR filters, which use previous inputs to calculate an output, IIR filters also utilize *historical output information* to calculate each new output. In this manner, IIR filters can implement mathematical filter equations with variables in the denominator (that is, poles).

The only drawback to IIR filters is their computational complexity. Since their computations use historical information on their past outputs, *each output must be calculated.* That is, unlike FIR filters an IIR filter cannot decimate to reduce computational complexity. Therefore, IIR filters generally operate with lower sampling rates.

The CS5317 Voice-band A/D Converter Implementation

The CS5317 uses oversampling, decimation, and FIR filtering to implement its digital filter. The CS5317 samples its analog input at 2.5 MHz (for a full-rated 5 MHz master clock). This high oversampling ratio of 500:1 (2.5 MHz sampling/5 kHz bandwidth) reduces external analog anti-alias requirements.

The FIR filter decimates the sampling rate from 2.5 MHz to 20 kHz to reduce computational complexity. The filter features an impulse response duration of 384 x 2.5 MHz and a decimation ratio of 128 (2.5 MHz:20 kHz). Since the filter does not decimate by 384 as shown in Figure B5, multiple convolutions must be in process concurrently. To achieve this, the CS5317 uses three accumulators working from a single 384-word coefficient memory. The three convolutions are spaced to begin and end 128 samples apart. Thus, a new 16-bit output sample becomes available every 128 input samples (for a decimation ratio of 128) whereas each 16-bit output is calculated using 384 input samples (for an impulse response duration of 384).

The CS5501 dc Measurement A/D Converter Implementation

The CS5501 uses oversampling, decimation, and both FIR and IIR filtering to implement its 6-pole Gaussian filter. The CS5501 samples its analog input at 16kHz (for a full-rated 4.096MHz master clock). This high oversampling ratio of 1600:1 (16kHz sampling/10Hz bandwidth) reduces *and most often eliminates* external analog anti-alias requirements.

The FIR filter is used to decimate the sampling rate from 16kHz to 4kHz to reduce computational complexity in the subsequent IIR filter. The

FIR filter response is not especially critical. Its only goal is to reject energy within ±10Hz bands around integer multiples of 4kHz, the IIR filter's sampling rate.

The IIR filter is needed to implement the poles in the 6^{th}-order Gaussian filter and achieve high roll-off of 120dB/decade. Its baseband filter characteristics are shown on page 4. Note that the filter's entire frequency response can be scaled by adjusting the master clock. The converter's sampling rate simply scales accordingly. With its cut-off frequency set at 10Hz (4.096MHz master clock) for maximized settling, the CS5501 offers 55dB rejection at 60Hz. With a 5Hz cut-off, though, 60Hz rejection increases to greater than 90dB. Master clocks as low as 40.96kHz are acceptable, yielding cut-off frequencies as low as 0.1Hz.

The CS5326 Digital Audio A/D Converter Implementation

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit, 3.072 MHz outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit, 48kHz results.

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. Modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise, and out-of-band input signals, into the converter noise floor. Filter orders are 27 and 30, respectively.

A third stage, FIR3, performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to ±0.001dB from dc to 22kHz. The passband compensation function prevents the use of a half-band filter for FIR3. Data is truncated to 16 bits at the output, and this operation is the major noise contributor in the system.

FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from 26kHz to 3046kHz are attenuated by at least 86dB. Phase response is precisely linear.

CS5326 to DSP56000 Interface

By Clif Sanchez

This application note describes the interface needed to connect the CS5326 to the Motorola DSP56000 Digital Signal Processor.

Since the CS5326 is a stereo delta-sigma oversampled analog-to-digital converter, it requires three clocks: a master clock to sample the analog input, a serial clock to shift out data, and a left/right clock to select the channel. The 74HC590 synchronous counter from TI, along with a couple of inverters, provide all the clocks that the CS5326 requires. The output previous to $\overline{L/R}$, Q_F, is used as a frame sync for the DSP56000 and connects to SC2 which is configured as FSr. For the DSP56000, the FSL bit must be set equal to zero.

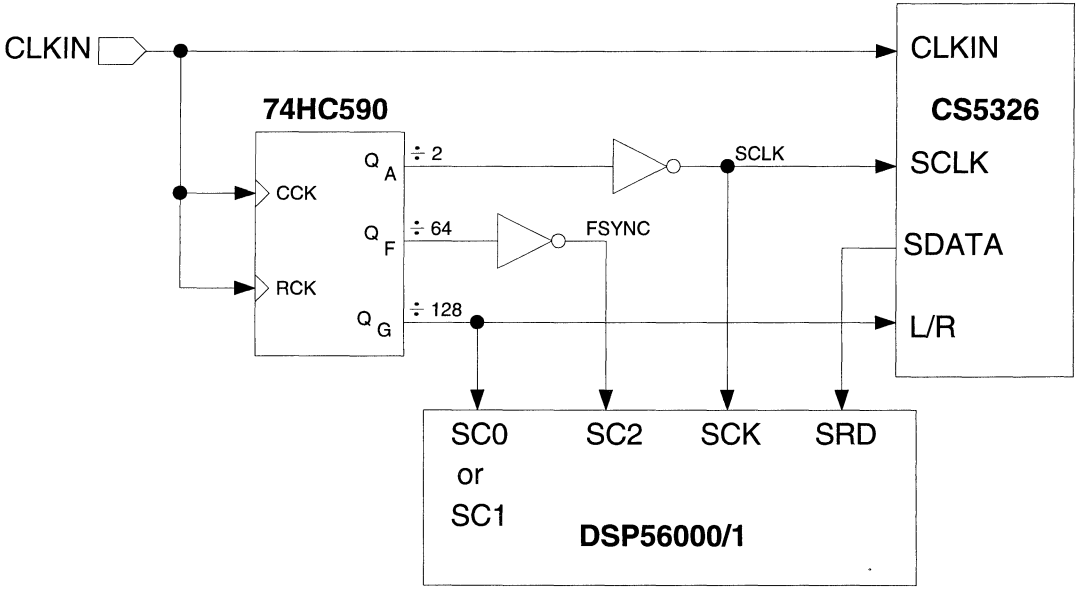


Figure 1. CS5326 to DSP56000 Connection Diagram

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If the DSP56000 serial port is in the synchronous mode, then the serial port transmit and receive sections used the same serial clock. This releases two pins, SC0 and SC1, and one can be configured as an input flag indicating the channel, left or right. They are latched in the DSP56000 at the same time as the MSB (see Figure 2) and can be used to synchronize left/right pairs.

If a synchronous counter is not available, a similar circuit can be constructed from a ripple counter and latch as shown in Figure 3. Since the D flip-flops provide inverted outputs, the output inverters are not needed. But the 74HC4040 ripple counter's clock must be inverted to give it enough time, one full clock instead of one half clock, to settle before the flip-flops latch the data.

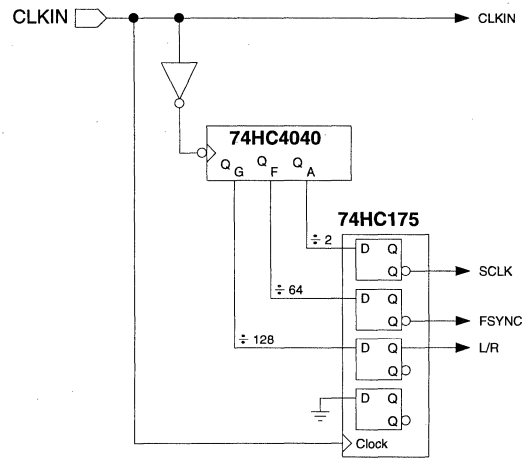


Figure 3. Alternate to 74HC590

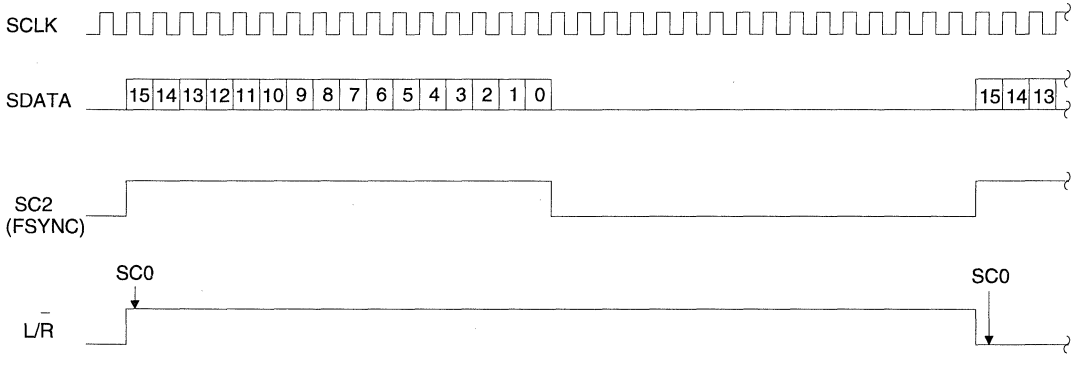
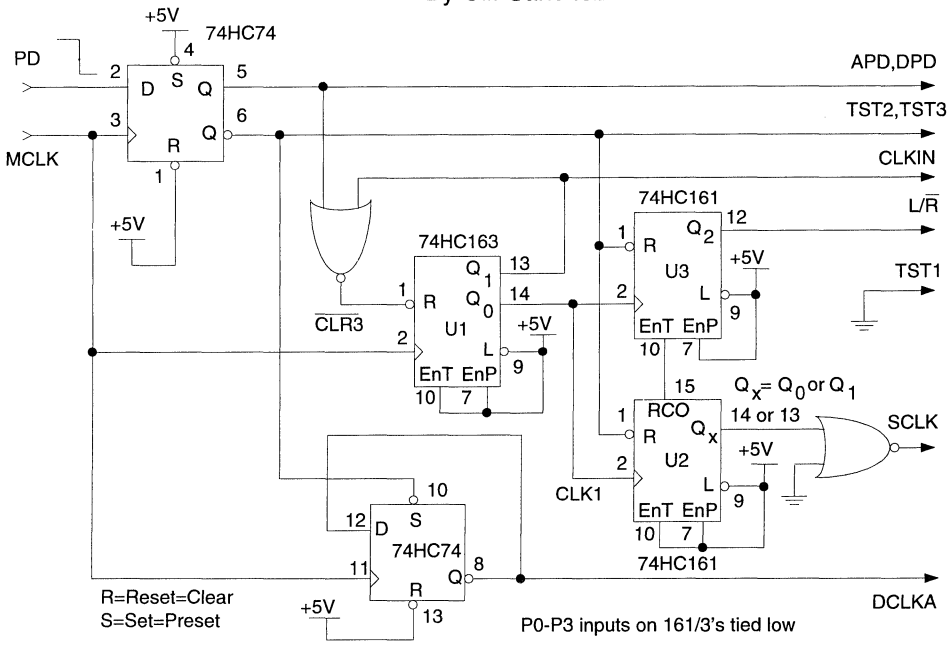


Figure 2. CS5326 to DSP56000 Timing Diagram

Application Note

CS5326/7/8/9 Low Frequency Operation

By Clif Sanchez



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This circuit places the CS5326/7/8/9 in test mode 6 and provides clocks with the proper frequencies and relative phases to operate the converter at speeds lower than specification.

In normal operation (i.e., not in a test mode), the CS5326/7/8/9 utilizes a phase lock loop circuit to implement a 3X clock frequency multiplier, the output of which paces the digital filter/ decimators. The limited range of the PLL results in a lower bound to the speed of operation. The ACLKA output is normally connected to the DCLKA input, and it is this clock signal that is the input to the 3X frequency multiplier.

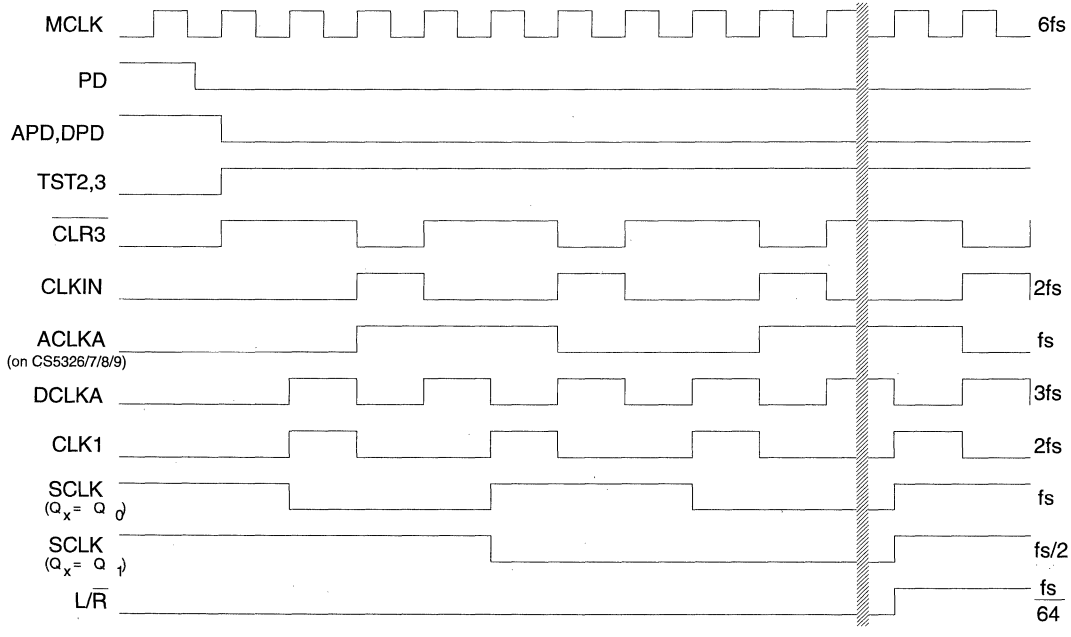
In test mode 6, the 3X multiplier is disabled, and the clock required for the digital filter/decimators is instead received directly on the DCLKA pin. The lower bound on the speed of operation is dramatically reduced (still non-zero due to internal dynamic logic), but the DCLKA signal frequency must be appropriately generated. The requisite frequency is 1.5X the frequency of the CLKIN signal. This ratio mimics the combination of the divide-by-two between CLKIN and ACLKA/DCLKA and the multiply-by-three between ACLKA/DCLKA and the filter/decimators' clock that occurs in normal operation.

The master clock signal MCLK is used to drive a divide-by-two counter to generate DCLKA and a divide-by-three counter to generate CLKIN, and to synchronize the PD (Power-Down) signal. The latter is used to appropriately reset the phase of

the counters as well as that of the delta-sigma modulators in the CS5326/7/8/9 (this is done through the use of the APD signal). In addition, when PD falls, the complementary output of the synchronizing flip-flop places the converter in test mode 6 through the use of the TST2 and TST3 pins. Note that the CS5326/7/8/9 should not be placed in test mode 6 in the absence of active clocks. In addition to powering down the analog section, APD is used to synchronize the start of ACLKA. DPD initiates an offset calibration and can be controlled separately from APD. Since APD powers down the reference, DPD should only occur at the same time or (at any time) after APD is released. In test mode 6, *the serial data output during calibration is not all zeros.*

An additional divider is used to generate the SCLK and L/R signals which are derived from CLKIN. The SCLK signal may be an inversion of either Q0 or Q1. Using Q1, though, results in an SCLK frequency that can slightly raise the noise floor of the CS5326/7/8/9 through interference effects with the modulators. If receive circuitry speed permits, Q0 should be used to clock out the serial output data.

The resulting phases of the various clocks generated by this circuitry is such that rising SCLK edges and all L/R edges occur at falling edges of DCLKA, as can be seen by referring to the timing diagram. Furthermore, 1-bit data transfers between the modulators and the filter/decimators are correctly timed. In normal mode, this transfer is synchronized by the ACLKA signal. In test mode 6, though, ACLKA is not used (and should be left open), and the correct timing is attained by setting the modulator phase with APD, as described above. As a check, it can be observed that falling edges of ACLKA occur at rising edges of DCLKA.



Notes:
1. $Q_X = Q_0$ is recommended for SCLK to avoid adverse analog interference effects caused by fs/2 signals.
2. L/R is a square wave with edges coincident with SCLK rising edges.
3. fs is analog sampling frequency.

An 18-Bit Dual Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example

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ABSTRACT

The architecture and performance of a stereo 18-bit delta-sigma analog-to-digital converter are discussed. This 28-pin device contains dual delta-sigma modulators and dual digital filters/decimators. Special emphasis is placed on applications examples using the A/D converter in various common audio environments including AES/EBU integrated circuits and digital signal processors. In addition, an example application is discussed in which the dual channel 18-bit part is configured as a single 19-bit A/D converter yielding a dynamic range of 100 dB.

0 INTRODUCTION

The benefits of using digital to store and process audio information are well documented[1]; however, the number of bits required to reproduce the analog signal to an acceptable level is still in flux. Consumer products are standardizing on the 16-bit level[2] while professional equipment manufacturers are asking for more[3,4].

Sec. 1 describes the architecture of the CS5328, a stereo 18-bit delta-sigma analog-to-digital (A/D) converter. Sec. 2 illustrates the performance of the A/D converter under a variety of test conditions. Also discussed is a 19-bit monaural example in which both input channels are tied together and the output words are summed, achieving a dynamic range of 100 dB over the 0-20 kHz audio band. Sec. 3 describes interfaces to common audio environments such as AES/EBU integrated circuits and the Philips I^2S bus, while Sec. 4 discusses DSP interfaces. Sec. 5 discusses a method of attaching the channel indication, left or right, as a tag to the end of the serial data stream.

1 ARCHITECTURE

The architecture of the CS5328, as seen in Figure 1, consists of two one-bit delta-sigma modulators[5] that oversample the analog input at a frequency that is 64 times the output word rate. Each delta-sigma modulator is followed by a 3-stage FIR filter. Dividing the filtering function into three

stages allows for an overall reduction in the number of required taps and incremental decimation to arrive at the output word rate. The output of each channel is latched and multiplexed on the SDATA pin under control of the L/$\overline{R}$ (left/$\overline{right}$) signal. L/$\overline{R}$ also starts the convolution for the FIR filters.

The digital filter response is illustrated in Figure 2 for a 48 kHz output word rate and has a stopband rejection of greater than 86 dB. Since the filter is digital, the frequency response will scale with clock frequency allowing the use of other sample frequencies. Table 1 lists the master clock frequency, passband edge, -3 dB point, and stopband edge for typical digital audio frequencies. An expanded view of the passband showing less than 0.001 dB passband ripple appears in Figure 3 while the transition band is expanded in Figure 4.

2 PERFORMANCE

To test the A/D converter, the analog input of a CDB5328 evaluation board[6] is driven with a signal generator having distortion lower than the A/D converter's noise floor. Any distortion produced from such a setup is assumed to be from the A/D converter[7]. For the FFT tests produced in this paper, the analog input is either a Krohn-Hite Model 4400A or a Brüel & Kjær Type 1051. The data is collected for 1024 consecutive samples. The FFT expects the sample set to be periodic; therefore, if the samples at each end of the sample set do not align exactly, the FFT will produce distortion products that don't exist in the analog input. If the A/D converter were synchronized to the analog input, the end points could be aligned, but to align to the 18-bit level is very difficult. Since the analog input is not synchronized to the A/D converter, the time-domain samples are windowed to avoid discontinuities at the end points. Windowing drives the end points to zero making the first point and last point is the sample set equal. The window is a minimum 5-term which widens the fundamental and harmonics, but doesn't affect the specifications being tested such as S/N+D and dynamic range[8]. Since the noise is uncorrelated, sample sets of points can be averaged to produce a plot in which the noise shape and low level harmonics are distinguishable. The noise spreads itself equally among the frequency bins while the fundamental, harmonics, and tones present, if any, remain unchanged. The data for this paper was gathered with a personal computer which also calculates the FFT[9].

2.1 CS5328 Results

A plot of 100 sample sets averaged, using the previously mentioned setup with an analog input at full scale, appears in Figure 5. A full-scale input is not the optimum test for digital audio since any excursions above full scale cause clipping and large distortions. Digital audio equipment usually defines -10 dB as a maximum signal level to guardband against clipping. A signal 10 dB below full scale would be a better test of an A/D converter for this environment. As can be seen from Figure 6, a -10 dB signal shows slightly better performance than the full scale signal and the harmonics are practically below the noise floor. In Figure 7 the input signal is 80 dB down from full scale and is considered a more difficult test of A/D converter performance[10]. On-chip dither minimizes tones that are normally associated with delta-sigma A/D converters. Figure 8 plots input signal level versus signal-to-(noise+distortion) for a 1, 10, and 20 kHz input signal. This plot illustrates the CS5328's lack of significant distortion for low signal levels over the entire audio band.

2.2 19-Bit Monaural Mode

The hardware illustrated in Figure 9 ties the two analog inputs together and adds the two 18-bit outputs, generating a 19-bit number. Utilizing the CDB5328 evaluation board, the serial data for each channel is shifted into the serial-to-parallel converter during the first 18 serial clocks after L/$\overline{R}$ changes state and is then latched on the parallel output. The serial-to-parallel converter has a separate shift register and latch so the parallel output is valid until the next parallel latch update. On the evaluation board, the left channel data is latched 14 serial clocks before L/$\overline{R}$ falls and the adder circuitry latches the left channel on the falling edge of L/$\overline{R}$. The right channel is latched on the evaluation board 14 serial clocks before L/$\overline{R}$ rises. The two 18-bit numbers propagate through the adder during the latter 14 serial clocks of the L/$\overline{R}$ low time and the 19-bit result is latched when L/$\overline{R}$ rises.

The FFT plot in Figure 10 shows an improvement of approximately 3 dB using summed channels over the single channel approach. The extra bit generates a 6 dB improvement since the signal level is doubled, but the noise from the second channel invokes a 3 dB penalty. Figure 11 illustrates a 19-bit FFT with the analog input down 60 dB. Notice the dynamic range for the 19-bit mono mode is 100 dB over the 0-20 kHz audio bandwidth.

3 TIMING IN AUDIO ENVIRONMENTS

In a typical audio environment such as CD, DAT, or digital audio workstations, the traditional analog front end consists of an 11th-order Chebyshev anti-aliasing filter[11], followed by a sample-and-hold (S/H), and completed by an A/D converter for each channel as shown in Figure 12a. The timing section is required to synchronize the S/H, A/D converter, output multiplexer, and digital signal processing system. If oversampling is utilized, the diagram would look more like Figure 12b in which oversampling by two decreases the anti-alias filter requirements to a 7th-order Butterworth[11]. This anti-aliasing filter provides better group delay characteristics than the traditional approach. In 2X oversampling the A/D converter and S/H must be capable of operating twice as fast as the traditional approach, and the timing section has to accommodate the decimation filter between the A/D converter and the system. Figure 12c shows the analog front end using the CS5328 that oversamples the analog input by 64 generating a sample frequency, Fs, of 64×OWR (output word rate). The CS5328 requires frequencies of 128×OWR for the master clock, 2×OWR for the serial data clock, and OWR for the L/$\overline{R}$ signal indicating the channel: left or right. The anti-aliasing filter requirements are minimized to a single pole passive filter and the group delay characteristics for this approach provide a flat delay over the entire passband. The high frequency clocks required are usually available for other system functions and can be derived from a 74HC590 synchronous counter.

3.1 Philips I^2S Bus

The "inter-IC sound" bus is a digital audio interface as defined by Philips[12]. The I^2S interface uses word select, WS, (inverted L/$\overline{R}$) to indicate both the channel and start of data. The data is output on the falling edge of SCK one SCK cycle after WS changes state. In the configuration illustrated in Figure 13, the 74HC590 counter is considered the master since it provides the word select and serial

data clocks. The data output by the CS5328 must be delayed one SCLK cycle and is considered 32 bits in length with the receiving device ignoring unused bits as defined by the interface specifications.

3.2 Sony Digital Interface

Both the CX23033 and CXD1211 from Sony Corp. are digital transmitting chips designed to send data in a format similar to the AES/EBU specifications[13]. The CS5328 interface for these chips would be straightforward if the A/D converter was only 16 bits because both interface ICs provide a 16-bit MSB-first format. Figure 14 illustrates the circuitry needed to connect the CS5326, a 16- bit A/D converter, to the Sony chips. Since the CS5238 outputs 18 bits, the 24-bit format of both interface chips must be used, and that format only accepts data LSB first. If the interface chips allowed the specification of the MSB/LSB-first option separate from the 16-bit/24-bit option, the interface would be greatly simplified. Another feature of the interface chips is that the data must be right justified in the channel, whereas the data output from the CS5328 is left justified. Using the 16-bit format as an example, the 16 bits *preceding* LRCK ($L/\overline{R}$) changing state are latched for right-justified data, whereas the 16 bits *following* LRCK changing state are latched for left-justified data. Figure 15 illustrates a method of converting from MSB-first to LSB-first using three cascaded 74HC299 shift registers oscillating between channels. When the right channel is shifting into the shift registers from the A/D converter, the left channel is shifting out of the shift registers to the digital interface chip and vice versa. LRCK for the CXD1211 has the same polarity as the CS5328, high for the left channel and low for the right channel, whereas LRCK in the CX23033 has the opposite polarity. Figure 16 illustrates the flow of serial data for each channel. While the CS5328 is clocking left-channel data into the 24-bit shift register via pin 'A', the shift register is clocking the previous right-channel data out of the $Q_{H'}$ pin and through a multiplexer into the interface chip. In Figure 16b the shift register's shifting direction is reversed and still contains the left-channel data. When the CS5328 starts shifting right-channel data into the shift register via pin 'H', the left-channel data contained in the shift register is clocked out of the $Q_{A'}$ pin and through the multiplexer into the interface chip. The multiplexer is needed to select the appropriate output of the 24-bit shift register to input to the interface chip, whereas the two inputs to the shift register may be tied directly together. The shift register clocks are disabled for eight serial clock cycles since only 24 bits of the 32 bit-periods in a channel are stored. Since the CS5328 outputs zeros after the 18 data bits, the shift register stores six zeros. In the timing diagram shown in Figure 17, the 'z's reflect the stored zeros. All combinational logic can be programmed into a PAL for compactness. To configure the interface chips for the 24-bit format, MSBF is set to zero for the CXD1211, whereas the CX23033 is used in operation mode 1 or, if a microcontroller is present, mode 3 with control register bits D7 and D6 both set to one.

4 INTERFACING TO DIGITAL SIGNAL PROCESSORS

Digital signal processors are used extensively in digital audio environments[14]. Although the digital signal processors, DSPs, discussed below are not an exhaustive set of DSPs capable of handling greater than 16 bits, they do illustrate the circuitry needed to interface to common serial ports.

4.1 Motorola DSP56000

The interface for the DSP56000 is straightforward as shown in Figure 18 with the timing diagram appearing in Figure 19. The counter needed for the various timing signals on the CS5328 provides other divided outputs that can be used by the DSP56000. The counter output previous to L/$\overline{R}$, FSYNC, is twice the frequency of L/$\overline{R}$ and can be used to indicate the beginning of a word. This output will rise concurrently with L/$\overline{R}$ changing state; however, FSYNC will fall after the 16th data bit is output. This is not a concern since the DSP56000 only uses FSYNC to start a serial data transmission and stops transmission when the specified number of bits are received. The DSP56000's serial port is configured to receive 24 bits (WL1,WL0 = 1,1), normal operation (MOD = 0), continuous clock (GCK = 0), and word-length frame sync (FSL1 = 0). If the transmit and receive ports are synchronous (SYN = 1), L/$\overline{R}$ can be used as a serial port flag indicating the channel. Section 5 has more information on the serial port flag.

4.2 Texas Instruments TMS320C30

The TMS320C30 has an interface similar to the DSP56000, with the exception of serial port flags. Figure 20 shows the interface diagram and Figure 21 illustrates the timing. If L/$\overline{R}$ must be known to the DSP, one of the alternate methods described in Section 5 must be employed. The interface diverges from previous TI DSPs but has become more flexible in the process. For the serial port, the variable data rate mode with 24 or 32 bits is utilized. In this scenario, FSR goes active concurrently with the MSB of the data. (In fixed data rate mode, FSR goes active one CLKR cycle before data.) The DSP also inputs the programmed number of bits after FSR indicates the start of serial data transmission. The polarity of CLKR and FSR are programmable, thereby eliminating one inverter from the previous DSP interface.

4.3 AT&T DSP32/DSP32C

The DSP32 incorporates the data skewing technique utilized in the Philips I^2S interface although there is no provision for stereo. The delay is one ICK (serial data clock) cycle on the ILD pin. ILD is a word sync as opposed to an WS signal which indicates the channel: left or right. The DSP32 accepts 32 bits, whereas the DSP32C can accept 24 or 32 bits, and both latch data on the rising edge of ICK. As with the two previous DSPs, ILD is only used to start serial data transmission. Figure 22 shows the connection diagram while Figure 23 illustrates the timing.

5 CHANNEL INDICATION

Many systems do similar processing to both left and right channels; therefore, the DSP may not need to know which channel it is currently operating on. The channel indication, L/$\overline{R}$, may be connected to the A/D converter and digital out or D/A converter, thereby synchronizing the input and output, without connecting to the DSP. However, if the processing is different for each channel, the DSP must know which channel it is operating on. As this function is only needed at initialization, an interrupt line could be utilized, with the interrupt being disabled after synchronization is achieved. This method requires a dedicated interrupt line which is usually in short supply. Another common

method is to map L/$\overline{R}$ to a memory location allowing the DSP to read that location while in the serial port service routine, thereby determining the channel. This method requires address decode logic and a high impedance latch to connect L/$\overline{R}$ to the data bus. A third method connects L/$\overline{R}$ to a general purpose input pin on the DSP if any exist.

If the serial port transmitting and receiving sections are synchronous on the DSP56000 from Motorola, two pins are liberated and can be configured as serial port flags. One of these flags can be utilized to capture the L/$\overline{R}$ signal. As shown in Figure 19, the SC0 flag is latched concurrently with the MSB of the serial data. This flag can be tested on initialization to determine the channel.

Since all the DSP serial ports mentioned require a minimum of 24 bits, and the CS5328 is only 18 bits, 6 trailing bits are unused. If L/$\overline{R}$ is appended to the serial data, the DSP could read the lower bits which identify the channel. The DSP could subsequently mask the lower bits or ignore them since they appear as a DC offset at a minimum of the 19-bit level. The circuit in Figure 24 appends L/$\overline{R}$ to the serial data stream by ORing L/$\overline{R}$ with the zeros output after the 18-bit serial word. The alternate circuit provides a single-chip-package implementation that multiplexes between SDATA and L/$\overline{R}$. Since the CS5328 outputs 18 bits, a flip-flop is needed to delay the rising edge of the Q_F (which rises after the 16th bit) until the 19th bit. A benefit produced by this configuration is that a larger-divide output of the 74HC590 can delay the L/$\overline{R}$ "tag" information until later bit times making the DC offset less significant. Figure 24 shows two configurations for adding the L/$\overline{R}$ tag to the data. In the "bit-19 tag" configuration, the L/$\overline{R}$ tag immediately follows the data, whereas in the "bit-21 tag" configuration the tag doesn't appear until the 21st-bit position. Figure 25 illustrates timing for the "bit-21 tag" configuration. Notice that the left channel data is followed by two zeros, then twelve ones; therefore, the first "one" of the channel tag is in the 21st-bit position. If the DSP's serial port is configured for 32 bits, a "bit-25 tag" could be generated by using the Q_E output of the 74HC590 counter as the clock input to the flip-flop.

6 CONCLUSION

The architecture and performance of the CS5328 18-bit dual channel delta-sigma A/D converter were discussed along with detailed interface and timing diagrams to AES/EBU chips, the I^2S bus, and a number of DSPs. A method of adding a channel identifier to the serial data stream was also explored.

Low input signal levels were shown not to degrade performance, and an example application using both 18-bit channels to generate a single 19-bit part was shown to improve the dynamic range to 100 dB over the audio band.

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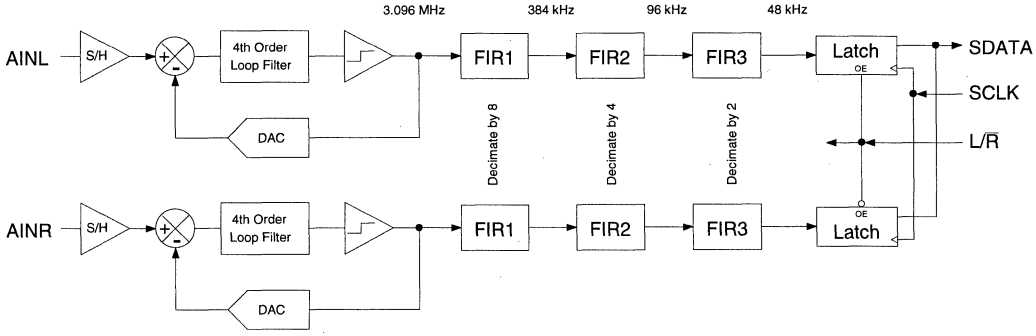


Figure 1. CS5328 Block Diagram

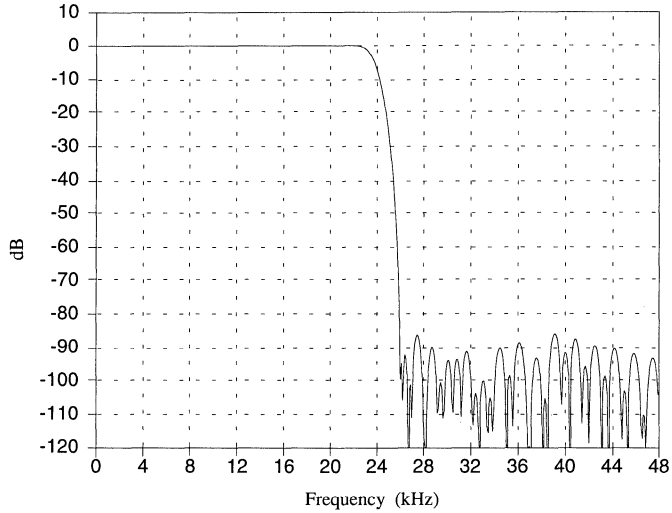


Figure 2. Frequency Response

Output Word Rate	CLKIN Frequency	Passband Edge	-3 dB Point	Stopband Edge
32 kHz	4.096 MHz	14.5 kHz	15.6 kHz	17.3 kHz
44.1 kHz	5.6448 MHz	20.0 kHz	21.6 kHz	23.9 kHz
48 kHz	6.144 MHz	21.8 kHz	23.5 kHz	26.0 kHz

Table 1. Audio Output Word Rates

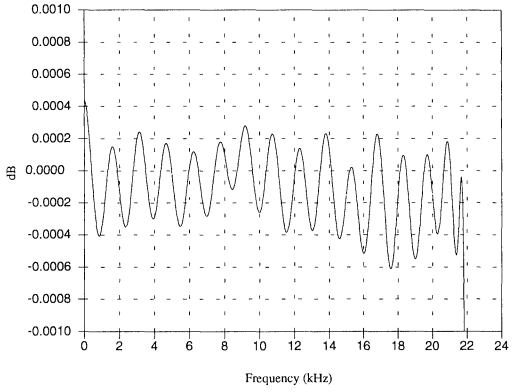


Figure 3. CS5328 Passband Ripple

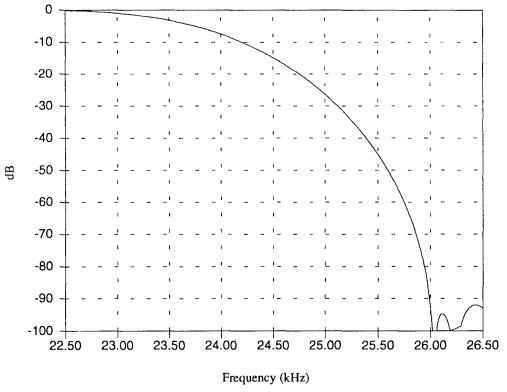


Figure 4. CS5328 Transition Band

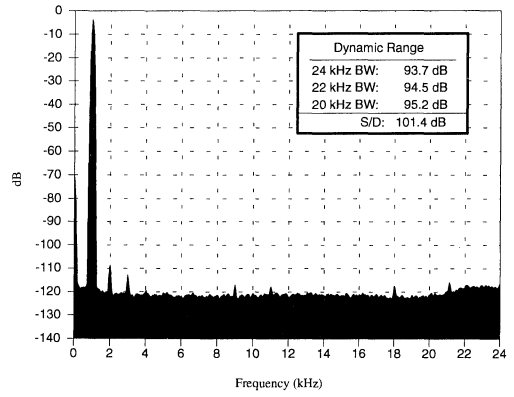


Figure 5. CS5328, Full Scale Analog Input

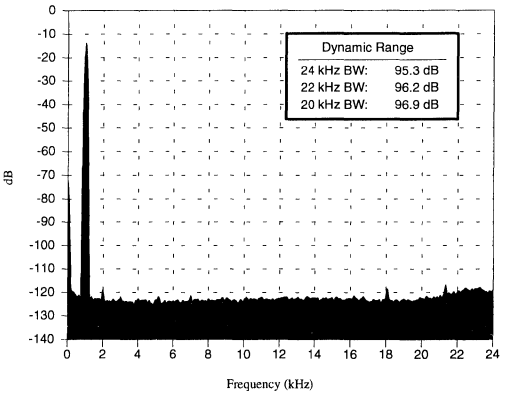


Figure 6. CS5328, -10dB Analog Input

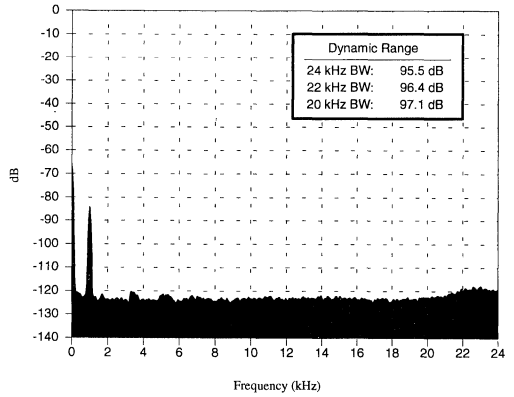


Figure 7. CS5328, -80 dB Analog Input

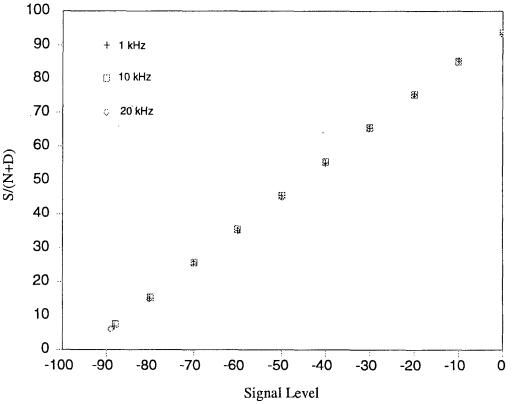


Figure 8. Signal-to-Noise vs. Signal Level

8

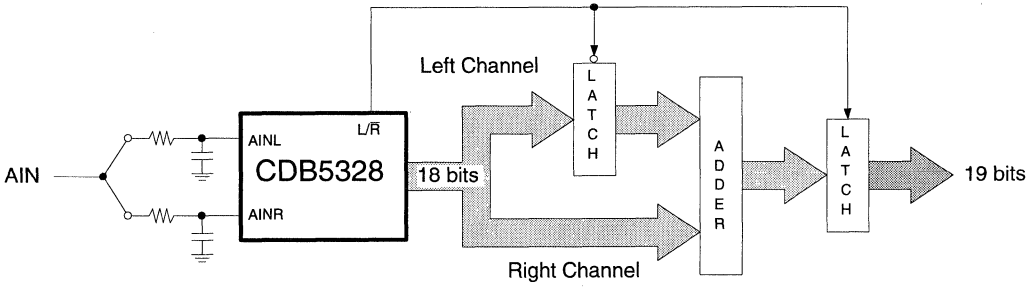


Figure 9. 19-Bit Hardware Configuration

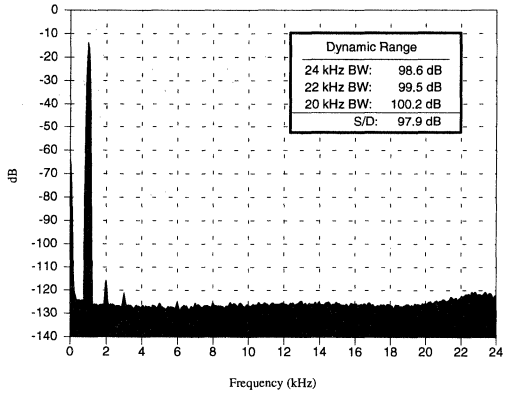


Figure 10. 19-Bit FFT, -10dB Analog Input

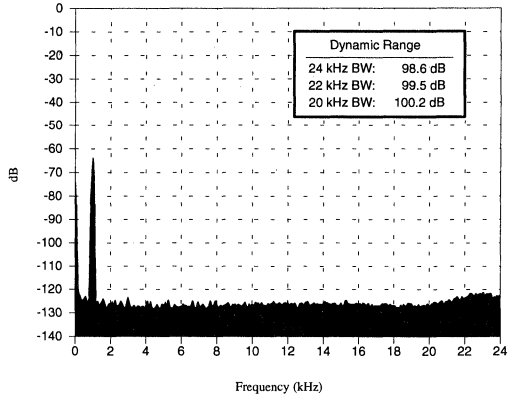
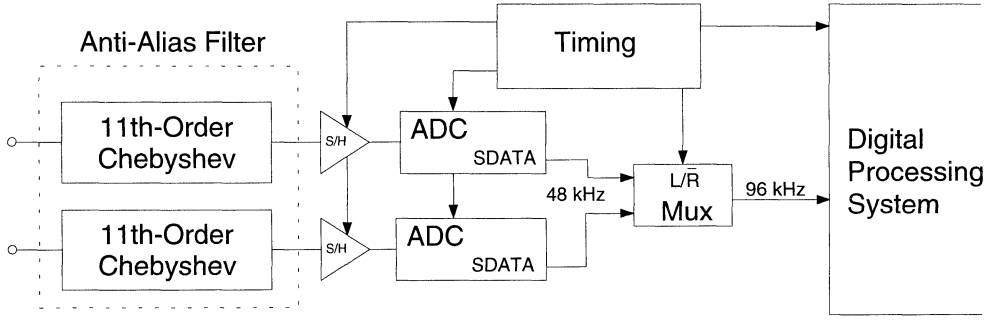
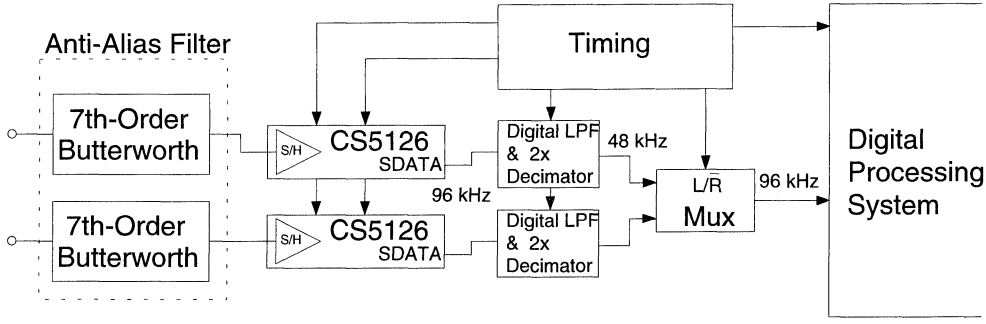


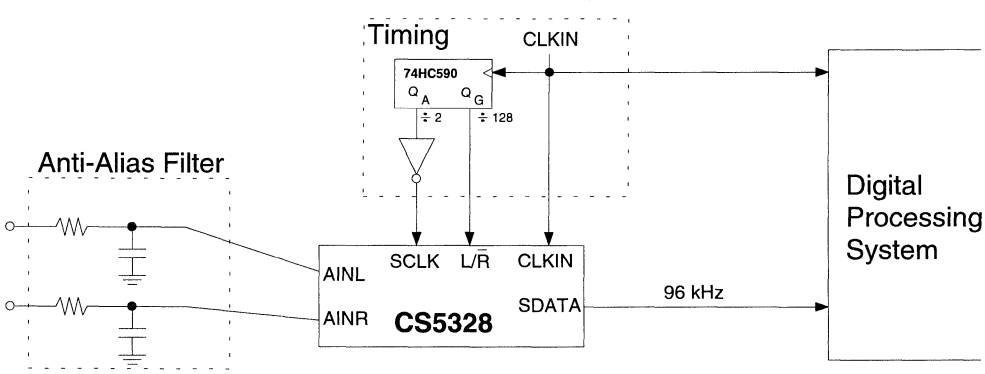
Figure 11. 19-Bit FFT, -60dB Analog Input



a. Traditional Approach



b. 2x Oversampling



c. 64x Oversampling

Figure 12. Analog Front End

8

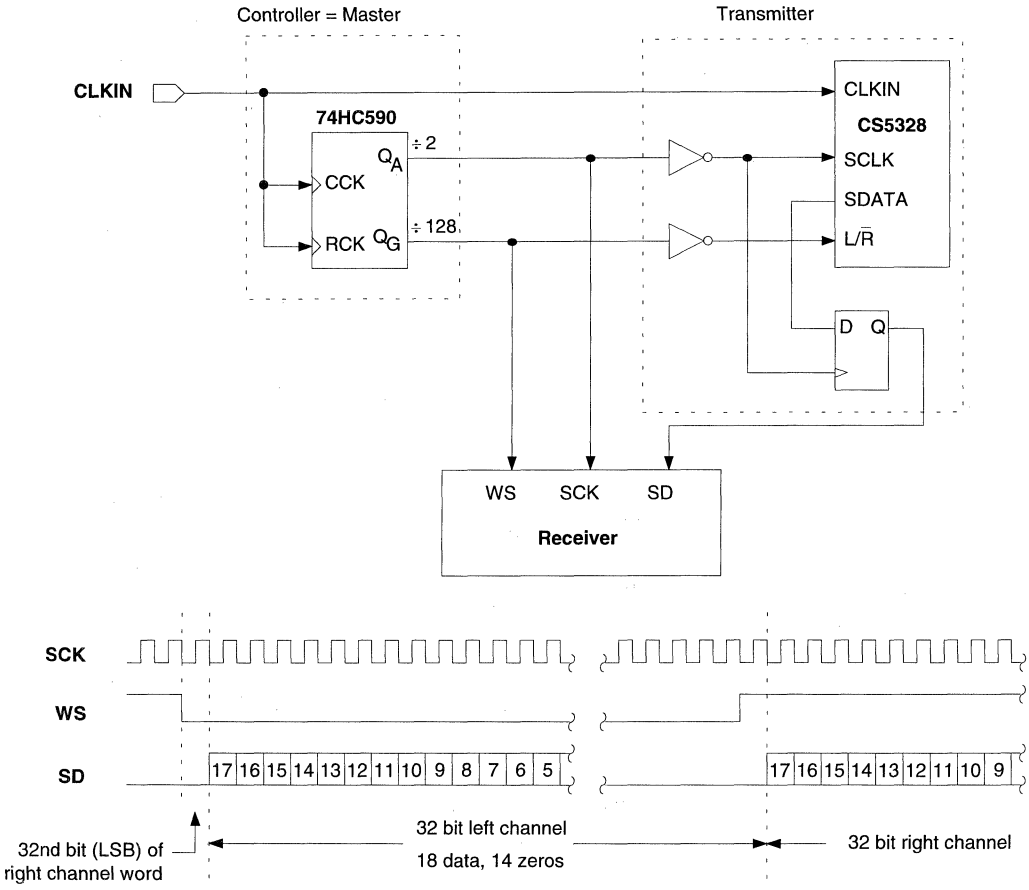


Figure 13. Philips I^2S Bus

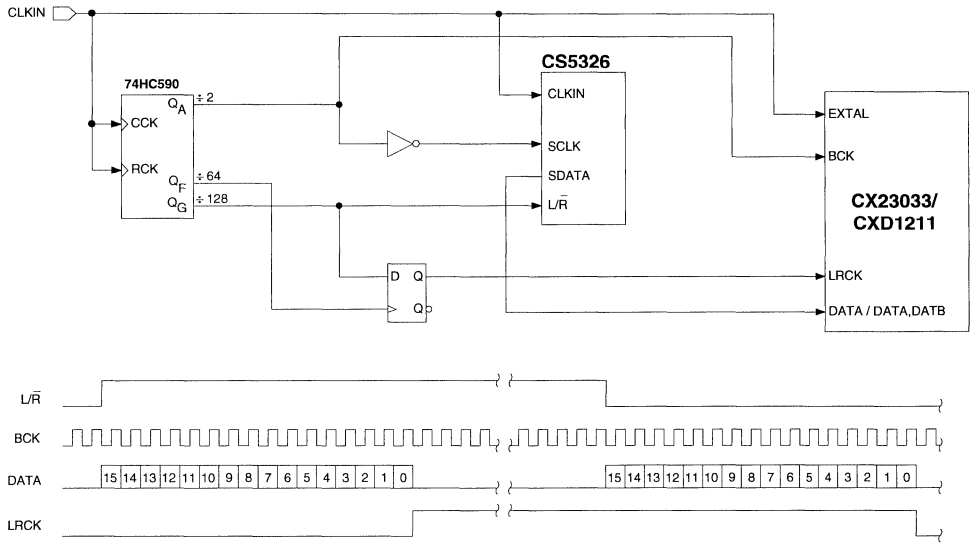


Figure 14. Sony Digital Interface, 16-bit Format

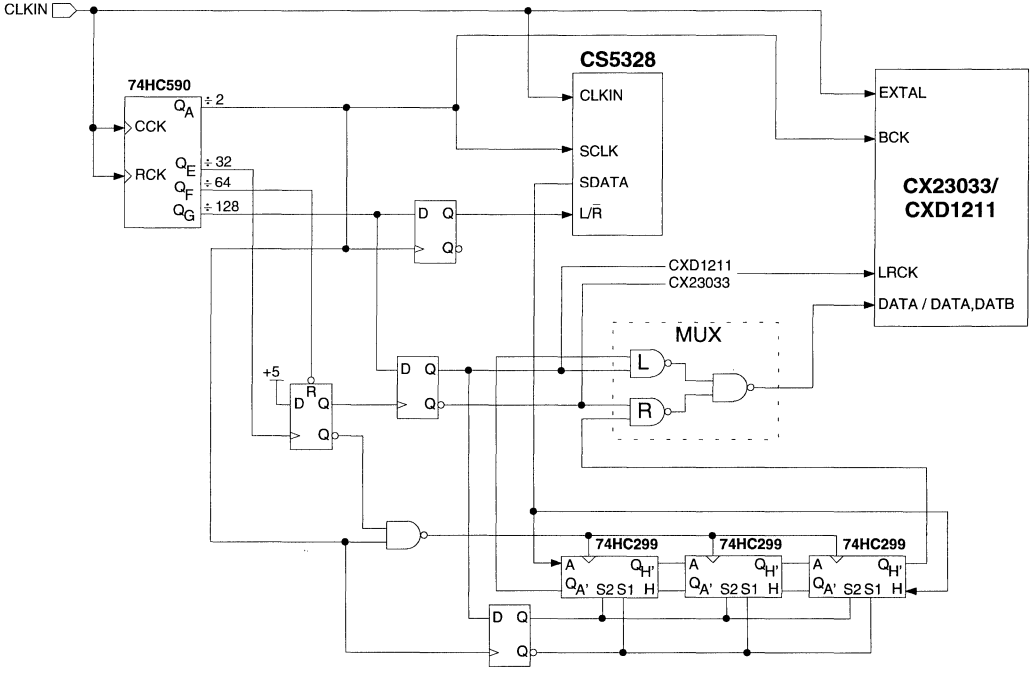
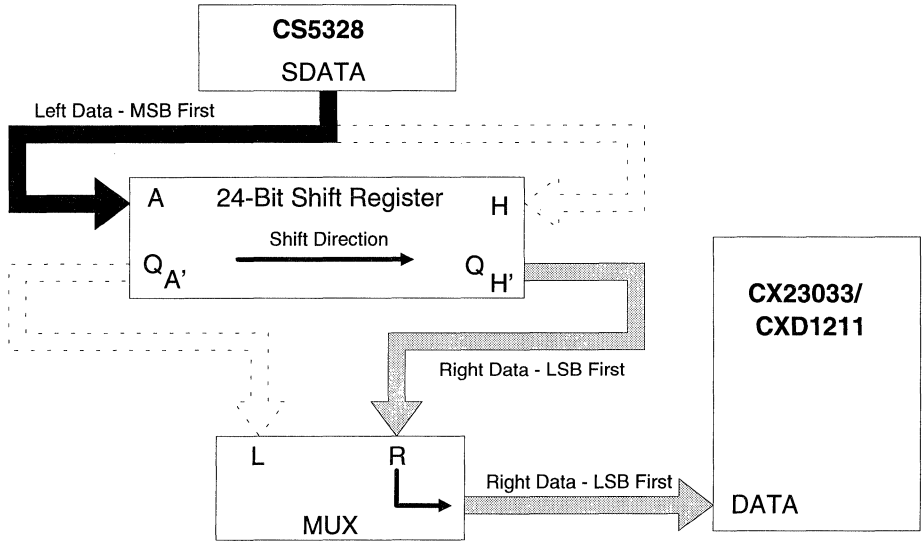
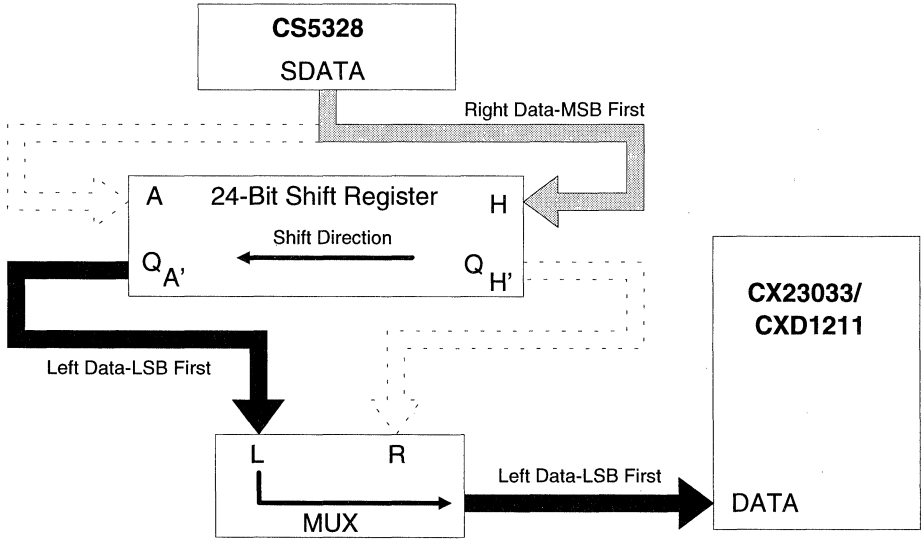


Figure 15. Sony Digital Interface, 24-Bit Format

8



a. First Channel



b. Second Channel

Figure 16. Sony Interface Serial Data Flow

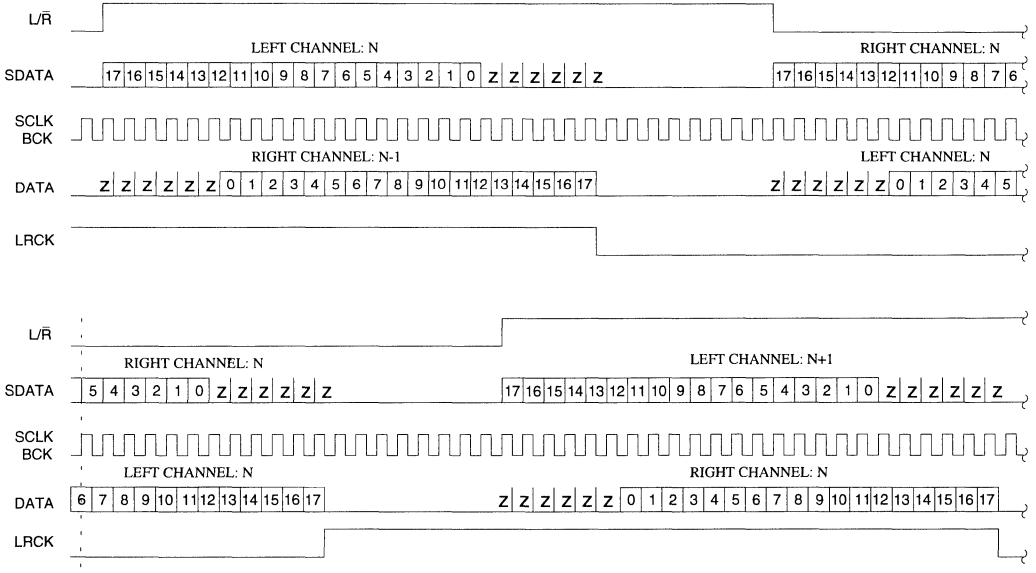


Figure 17. Sony Digital Interface Timing Diagram, 24-bit Format

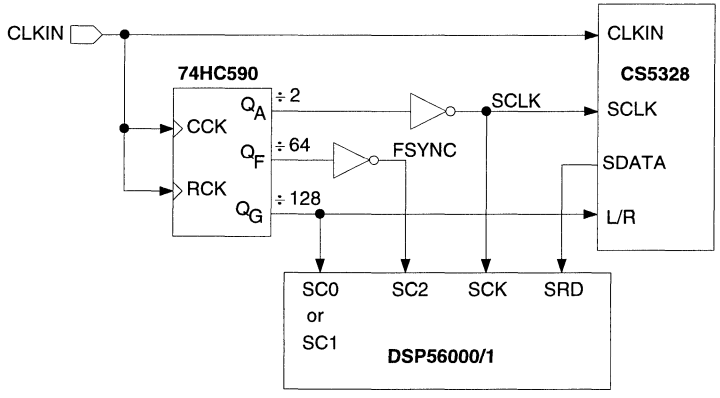


Figure 18. DSP56000 Connection Diagram

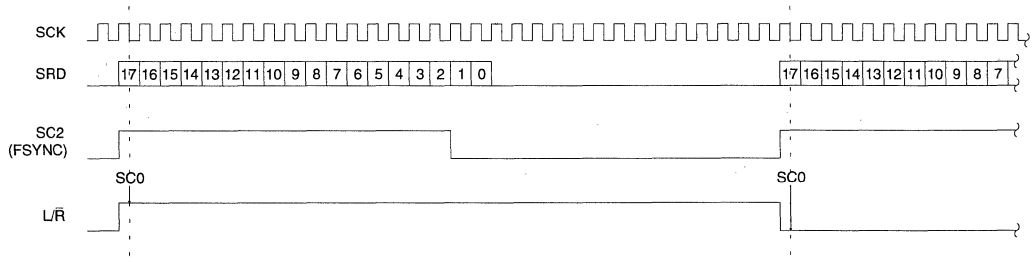


Figure 19. DSP56000 Timing Diagram

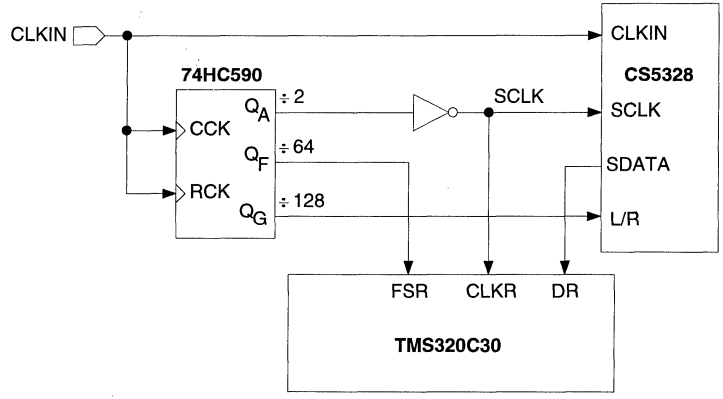


Figure 20. TMS320C30 Connection Diagram

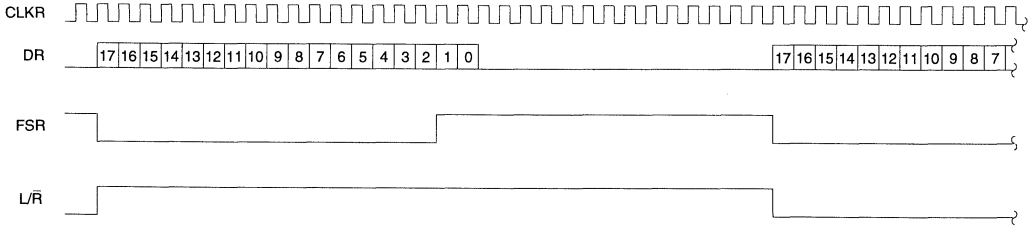


Figure 21. TMS320C30 Timing Diagram

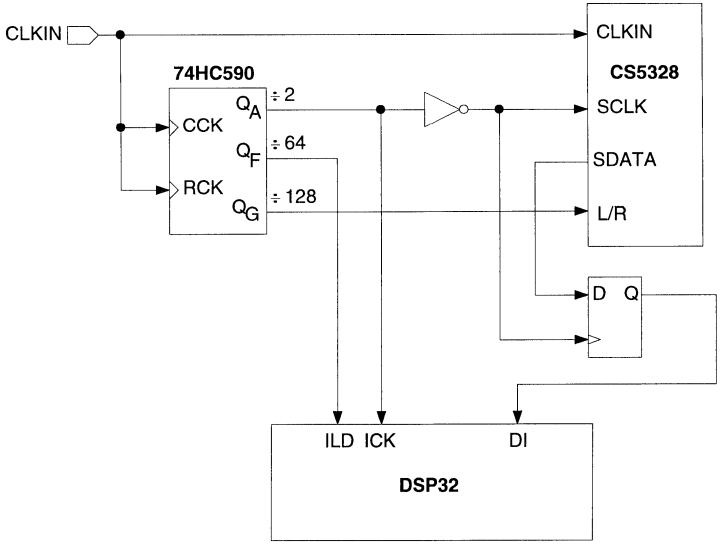


Figure 22. DSP32 Connection Diagram

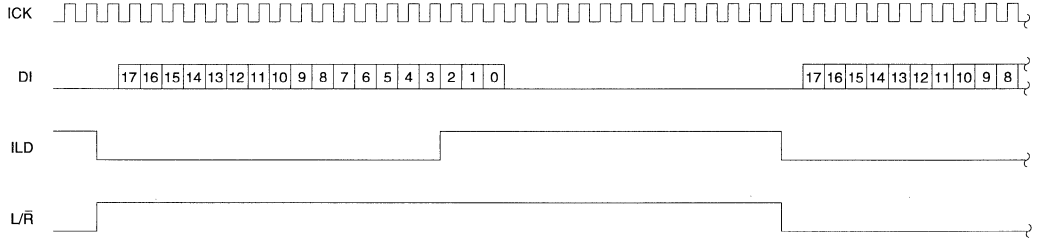


Figure 23. DSP32 Timing Diagram

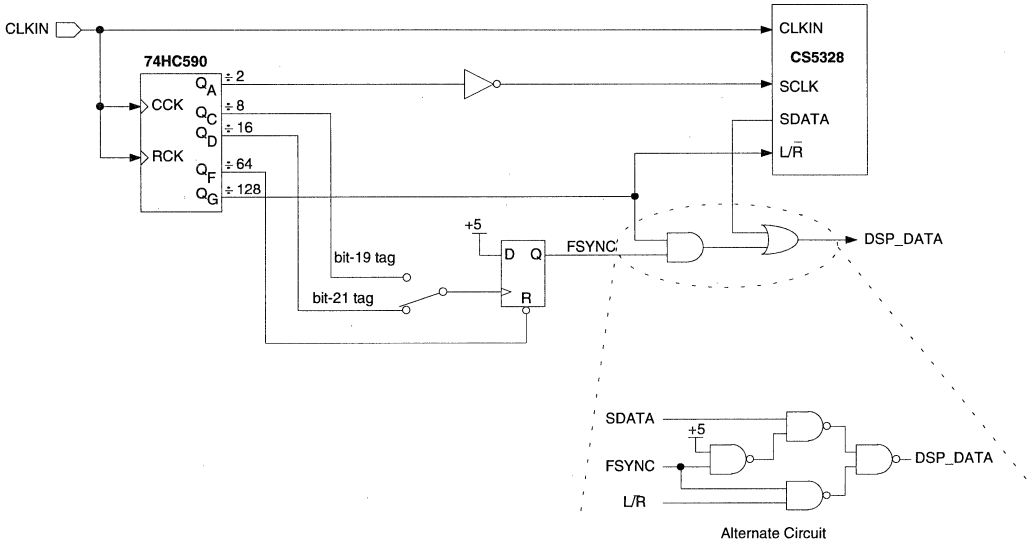
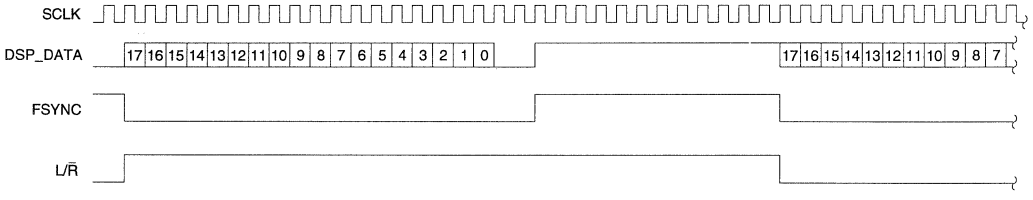
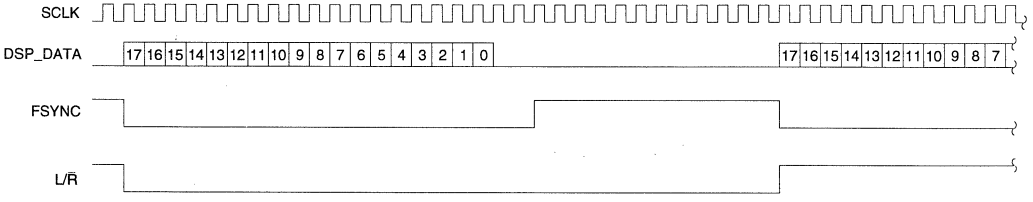


Figure 24. Channel Tag



a. Left Channel



b. Right Channel

Figure 25. Channel Tag Timing Diagram (bit-21 tag)

A Stereo 16-Bit Delta-Sigma A/D Converter for Digital Audio

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AND

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Asahi Kasei Microsystems, Inc., Tokyo, Japan

A two channel 16-bit A/D converter employing oversampling techniques has been developed. The device contains two fourth order delta-sigma modulators with 1-bit outputs, each followed by a digital finite impulse response filter/decimator. The analog inputs are sampled at 3.072 MHz and the digital words are output at 48 kHz.

0. INTRODUCTION

The emergence of digital audio has increased the demand for high performance A/D converters. Delta-sigma conversion has been gaining recognition as having advantages over more classical audio band conversion techniques. In particular, it obviates the need for sample and hold amplifiers, eases the design of anti-aliasing filters, and is free of differential non-linearity errors that distort low level signals.

This paper discusses the development of a two channel 16-bit audio band delta-sigma converter featuring a high degree of integration and suitable for use in stereo digital audio applications. Section 1 gives an overview of the concepts pertaining to delta-sigma conversion. The device architecture and a functional partitioning strategy are presented in Section 2 Sections 3 and 4 discuss design of the two major functional blocks, and measured results are presented in Section 5.

1. DELTA-SIGMA CONVERSION

1.1 Quantization Noise

Analog to digital conversion is a process that necessarily introduces errors into a signal due to quantization. The difference between the output of an otherwise perfect converter (or "quantizer") and that which might be expected of a converter with unlimited resolution can be modeled as an additive noise signal. The level of this "quantization noise" is reduced in converters of higher resolution with finer quantization levels, but nonetheless must remain non-zero. If the analog input is sufficiently large and/or if the input is sufficiently random, the spectrum of the quantization noise can be approximated as white [1] with its energy equally distributed between dc and $f_S/2$, where f_S is the sampling and conversion rate (it is assumed the signal is sampled before it is converted). The effective resolution of a converter can be increased by filtering the output and thereby reducing the level of the quantization noise. A commensurate reduction in the available signal bandwidth must be accepted as a consequence of the filtering, but may prove acceptable if the conversion rate is high. The sampling and conversion of a signal at a rate much higher than the signal frequency is a technique termed "oversampling". The "oversampling ratio" is the ratio of the actual sampling rate to the Nyquist rate (i.e., twice the highest signal frequency of interest).

This process is illustrated in Figure 1, where an analog sinusoid of frequency f_O is converted to a digital, quantized sinusoid at a rate f_S by a linear

pulse-code modulation (PCM) converter. The input spectrum is shown in Figure 1A, and Figure 1B shows the effects of the quantization process with the addition of white noise (this and following spectra repeat at multiples of f_s, of course, due to the discrete time nature of the sampled signal). Processing by a digital filter with a baseband cutoff frequency of f_b as illustrated in Figure 1D yields the output spectrum in Figure 1E. The baseband cutoff frequency f_b is presumed to be equal to the highest signal frequency of interest. The remaining quantization noise voltage level will be lower than the original level by a factor of sqrt($f_s/2f_b$) (the quantization noise *energy* is lowered directly by the oversampling ratio $f_s/2f_b$).

The utility of this technique when applied to audio signals with a baseband frequency of f_b = 20kHz is questionable. To obtain the equivalent of 16-bit performance from, say, a 12-bit converter, the 12-bit quantization noise would have to be lowered by 2^4=16. This would in turn require an oversampling ratio of $f_s/2f_b$ = 256, or $f_s \cong 10$MHz.

Delta-sigma conversion is a technique that employs oversampling to obtain high resolution (low quantization noise) digital signals from low resolution (high quantization noise) quantizers. As will be shown below, the delta-sigma converter contrasts with the previous example in that the quantization noise *at the output* of the low resolution quantizer is not white, but rather frequency "shaped", such that noise in the baseband ($f<f_b$) is suppressed at the expense of slightly higher out-of-band ($f>f_b$) noise. The power of digital filtering can then be applied to the resultant spectrum to pass the signal (and the residual baseband quantization noise) while rejecting the out-of-band quantization noise.

The converter consists of a modulator and a digital filter. As can be seen in Figure 2, embedded in the modulator is the low resolution N-bit quantizer, around which frequency dependent feedback is applied by means of a N-bit DAC and an analog filter. The analog filter has a frequency response of H(f). The analog input is summed into

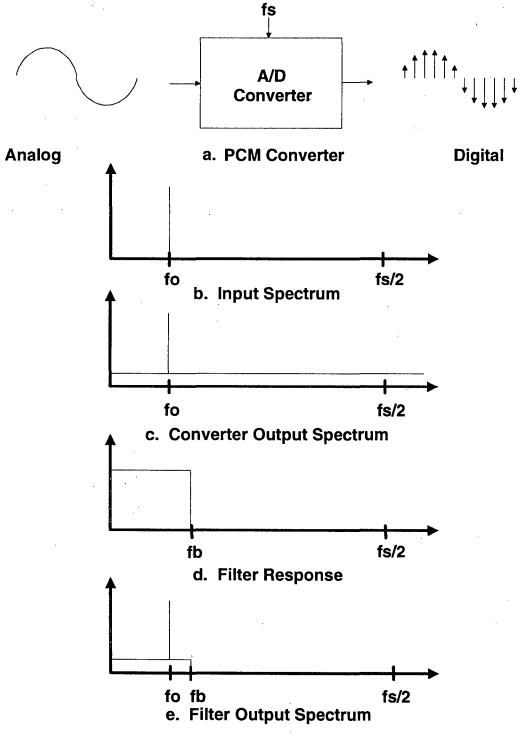

Figure 1. Increasing Resolution with Filtering

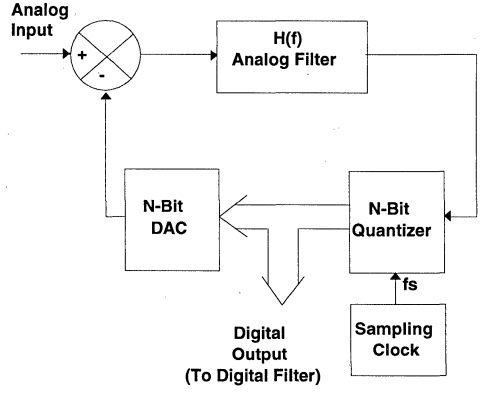

Figure 2. Delta-sigma modulator

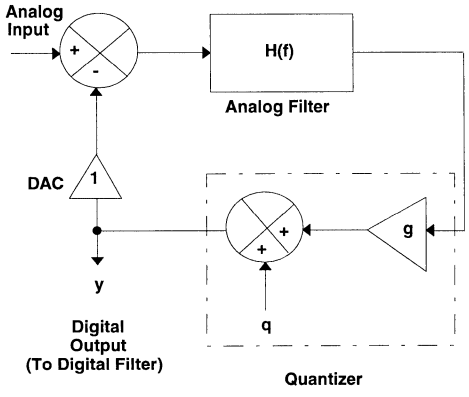

Figure 3. Linearized delta-sigma modulator

the modulator loop at a point where, for frequencies with high loop gain, the output of the DAC will be substantially equal to the input. To the extent that the DAC faithfully reproduces the quantizer digital output, this signal, too, must be substantially representative of the analog input again, for frequencies with high loop gain.

1.2 Loop Analysis

The presence of the non-linear quantizer renders exact analysis of the loop difficult. A typical and useful approach is to linearize the quantizer by replacing it with a gain stage and a quantization noise source [2]. Again, the latter is only a contrivance to account for the difference between the quantized output and the amplified input. This is illustrated in Figure 3. The DAC has been replaced by a unity gain stage, as its function is irrelevant for analyzing the effects of quantization noise. Note, though, that non-idealities in the DAC can be the chief limitation to the modulator's performance [3].

The actual value of the gain g and the rms value of the quantization noise signal q need not be known to obtain an understanding of how the modulator shapes the quantization noise. It must be assumed, however, that successive values of the quantization error are uncorrelated — i.e., the quantization noise spectrum is white. The validity of this assumption is borne out empirically.

The modulator output signal y is a function of the analog input x and quantization noise q, as follows:

$$y = (x\text{-}y)\ \mathrm{H(f)}g + q$$

$$y\,[1 + \mathrm{H(f)}g] = x\mathrm{H(f)}g + q$$

$$y = \frac{\mathrm{H(f)}gx}{1 + \mathrm{H(f)}g} + \frac{q}{1 + \mathrm{H(f)}g}$$

If the loop gain $\mathrm{H(f)}g >> 1$, then

$$y \cong x + \frac{1}{\mathrm{H(f)}g}\ q$$

That is, the output will be the sum of the input and the quantization noise spectrally shaped by the inverse of the analog filter frequency response.

A glance at the approximate expression for y may lend hope to the prospect of reducing quantization noise by increasing the value of H at all frequencies. However, the effective value of g would change to compensate such a maneuver. Reducing q by introducing a higher resolution quantizer would indeed offer improved performance. But the most effective method of achieving lower baseband quantization noise (for a given oversampling rate) is the selection of filter function H(f) that possesses high in-band gain and high out-of-band attenuation, thereby shaping the quantization noise spectrum advantageously. Note that the poles of the filter are zeros of the noise transfer function.

1.3 Integrator

A simple integrator has the desired spectral qualities for a filter. A cascade of two integrators would appear more attractive, and indeed such a "second order" filter more effectively shifts quantization noise to out-of-band frequencies than the "first order" filter. Extension to higher order filters is problematic, though, due to stability considerations. A second-order design requires the placement of a single zero in the filter response to obtain a well-behaved modulator.

Higher- order filters can also have zeros included as an aid to stability, but even so they are conditionally stable due to the high phase shift at baseband frequencies. Conditionally stable loops can become unstable if a frequency independent gain parameter in the loop is reduced. The effective quantizer gain g is such a parameter and is subject to change under varying operating conditions. As such, stability of modulators with third and higher order filters is at risk. Nevertheless, the attractiveness of higher order filters has led to a number of solutions to the stability problem [4],[5]. The device discussed in this paper utilizes a fourth-order filter. Stability will be discussed below.

Another approach that leads to performance similar to higher-order modulators without the attendant stability question has been reported [6]. This architecture has cascaded lower order modulators, with successive modulators measuring the residual in-band quantization noise of previous modulators. The various modulator outputs are digitally processed to lower overall in-band noise. However, accurately matched components and high gain integrators are necessary to achieve the desired performance.

1.4 Filtering and Decimation

Once the quantization noise has been appropriately shaped, it remains the task of the digital filter to remove the out-of-band quantization noise. A straightforward approach of synthesizing a low pass filter with sufficient stop-band attenuation and acceptable pass-band response would prove inefficient. Instead, a strategy of staged filtering and decimation can be adopted to ease the computational burden [7]. Decimation is the process of sampling a discrete time signal at a rate lower than its own. The advantage of decimation is that signal processing after decimation can proceed at the lower rate. As a sampling process, though, decimation is subject to the ill effects of aliasing.

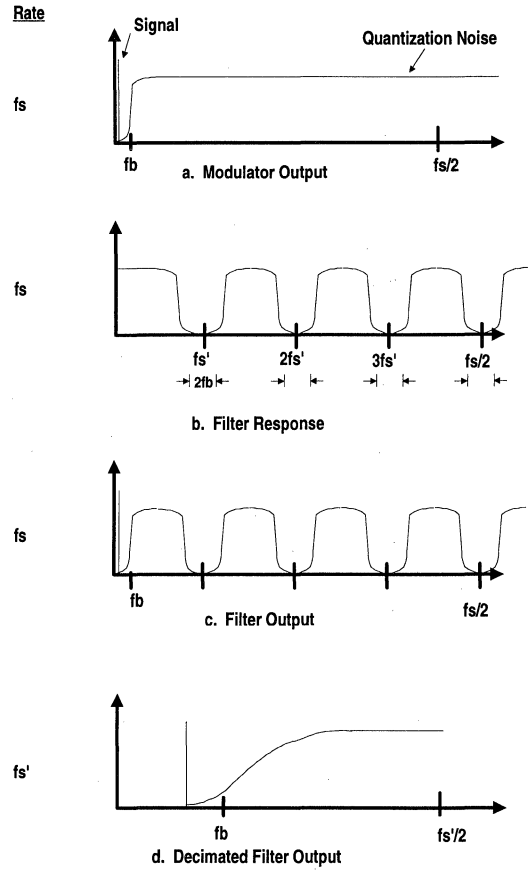

Figure 4. Filter Strategy

In this application, each stage of filtering need only reject signals that will be aliased into the baseband by the immediately subsequent decimation process, since later filter stages will reject signals aliased elsewhere. Figure 4 illustrates this approach. A signal with a spectrum characteristic of a modulator output signal is input to a filter at a rate f_S. The output of this filter is to be deci-

mated to a new rate f_S', where $f_S = Nf_S'$, before being processed further. Aliasing will occur throughout the spectrum, but only components within $\pm f_b$ of integer multiples of f_S' will get aliased into the baseband. A filter designed to have rejection only in these frequency "pockets" requires much less computation than one with rejection across the entire stop-band. As the sampling rate gets lower, of course, the pockets become proportionately wider and the filters become more complex. However, they can proceed with their computations at a more leisurely pace.

The final filter stage, operating at the slowest rate, can be a true low pass filter, eliminating the accumulated out-of-band quantization noise. In addition, it can "tweak" the frequency response of the pass-band if previous filter stages, the modulator, or even analog processing prior to the modulator have warped the response.

The need to reject the out-of-band quantization noise also represents a benefit. Namely, signals outside the baseband up to half the modulator sampling frequency do not get aliased by the modulator and are rejected by the digital filter. Indeed, spurious input signals approaching the sampling frequency do not get aliased into the baseband unless they are within $\pm f_b$ of f_S, and are likewise rejected. This characteristic can greatly relax analog anti-aliasing requirements and, for some applications, stands as one of the leading benefits of delta-sigma conversion.

2. ARCHITECTURE

2.1 Overall Architecture

The device described in this paper contains two delta-sigma converters suitable for stereo digital audio applications. It is packaged in a 28 pin dual-in-line package with a standard 0.600 inch wide footprint. The cavity of the package is occupied by two silicon dice. One die contains the two modulators, a voltage reference (the value of which determines full scale signal level), clocking circuitry, and a small amount of digital housekeeping circuitry. The second die contains the digital filter/decimators.

2.2 Reasons for Two Die

Partitioning of the system in such a fashion was motivated by the following considerations:

1) The complexity of the digital filter necessarily creates a large amount of electrical noise during normal operation. Placing this circuitry on a silicon substrate separate from the modulators eases the task of preventing this noise from interfering with the modulators' analog signal processing.

2) The great majority of the silicon area is occupied by the digital filter/decimators, and the manufacturing cost is dominated by this circuitry. Shrinking of the geometries comprising this circuitry as the product matures can lead to cost reductions without affecting performance. Shrinking of analog circuitry is risky and difficult; hence, the advantage of removing this circuitry from the more cost-sensitive digital die.

3) With separate die, different processes can be used to fabricate the analog and digital portions on the converters.

Regarding the last item, the digital die is manufactured using a standard 5V, 2 micron double-metal digital CMOS process. A 10V process was chosen for the analog die to allow more headroom for the analog signals. CMOS was chosen to support the switched capacitor design discussed in the next section. The selected process has 3 micron line widths, double polysilicon layers for capacitors, and a single metal layer.

2.3 Shared Functions

To a large extent, the two channels function independently. However, some circuit blocks are shared. On the analog die, all clocking is common between the two channels to facilitate simultaneous sampling of the left and right channel signals. Additionally, a single voltage reference circuit is utilized by both channels. The voltage reference

employs both lateral and vertical bipolar *npn* transistors (both of which are useful parasitics in this process) in a bandgap configuration. Its output is connected to a pin so that it can be capacitively bypassed to reduce crosstalk between the two channels. This capacitor and two simple RC antialias filters are all the external elements required of the device other than standard power supply decoupling elements.

The two digital filter/decimators also have common clocking. The various filter coefficients are stored in a single ROM which is accessed by both right and left channels.

3. MODULATOR

3.1 Major Characteristics

The major characteristics that need be determined in the design of a delta-sigma modulator are filter technology, oversampling ratio, quantizer resolution, and filter order.

3.2 Discrete Time Implementation

Although continuous time filters can be employed in the implementation of a delta-sigma modulator (sampling occurs at the quantizer only), three considerations dictated the choice of sampled data filters for use in the product. First is the ease with which sampled data filters can be integrated in comparison to continuous time filters. Second is that continuous time filters are sensitive to timing errors in the feedback of the modulator's DAC signal [3], whereas sampled data filters are not. Third, with proper design care sampled data circuits can provide greater isolation between channels in a stereo application since signal currents are transient. They can be made quite small at the sampling instances and are of no consequence at other times (both technologies are subject to capacitive crosstalk). Thus, sampled data switched capacitor technology was chosen for the design of the modulator.

3.3 Oversampling Ratio

The oversampling ratio is limited by the achievable settling time of analog components as well as the maximum computation rate of the digital filter. It is also preferable that the oversampling ratio be a factor of 2^N to ease applications. With a standard baseband of 24kHz, the oversampling ratio of 64 was chosen for a sampling rate of 3.072MHz. In a switched capacitor network each cycle is divided into two phases. With design margin, all modulator circuit blocks were designed to settle in 100ns to 0.1%.

3.4 1-bit Quantizer

As was mentioned in Section 1, higher resolution quantizers embedded in the modulator loop yield lower levels of in-band quantization noise. However, a 1-bit quantizer (i.e., a comparator) is simple to implement and minimizes the number of connections between the modulators and their digital filters. More importantly, a very attractive attribute of the use of a 1-bit quantizer is that errors in the 1-bit feedback DAC are not sources of distortion and/or excess noise, but only gain and offset errors [8]. Therefore, no precision components are necessary. Further, a one bit output simplifies the design of the first (and highest speed) digital filter stage.

3.5 Modulator Filter Order

The selection of a 1-bit quantizer operating at an oversampling rate of 64 requires at least a third order modulator filter to obtain 16-bit performance at the digital filter output. The addition of other noise sources (e.g., quantization effects in the digital filter) eliminated the candidacy of a third order filter. A fourth order modulator filter comprised of four cascaded integrators would provide sufficient rejection of baseband quantization noise. However, the modulator's baseband quantization noise can be rendered insignificant by optimization of a fourth order filter, as follows.

In Section 1 it was noted that the poles of the modulator filter are the zeros of the quantization noise transfer function. A filter with four cascaded

integrators results in a noise transfer function with four zeros at dc. Lee and Sodini [9] found that spreading these zeros by application of local feedback around the integrators was effective in lowering the total baseband quantization noise output by the modulator. Optimal placement of all four zeros (two conjugate pairs) results in an 11dB improvement in baseband quantization noise rejection. Optimal placement of a single conjugate pair with two zeros left at dc results in a 10dB improvement.

Implementation of the two-conjugate-pair filter requires feedback to the input summing junction. This requirement has associated undesirable consequences (PSRR degradation, for example) and the two pair configuration offers little additional noise shaping improvement above the single pair. So, the single conjugate pair configuration was adopted.

3.6 Modulator Design

Figure 5 is a block diagram of the modulator. Coefficient *b* is fed back around the third and fourth integrators to form the conjugate pair of poles in the filter transfer function. The analog input is represented by *x*, and the single bit digital output is *y* (which is inverted and summed with *x* in analog form). The feedforward coefficients a_1 through a_4 are necessary (although not sufficient) for stable operation. The value of one coefficient is arbitrary. The value of the other three coefficients determine the location of filter zeros, but the effect of these on modulator operation is not easily predictable. Higher ratios of a_1 to a_4 lead to more stable, noisier operation.

3.7 Stability Considerations

As was mentioned in Section 1, low values of the "effective gain" of the quantizer (in this case comparator) *g* can lead to instability. Since the output levels of the comparator are fixed, and since in an unstable mode the integrator output levels can be expected to grow, any linearization criterion for evaluating *g* should lead to an ever

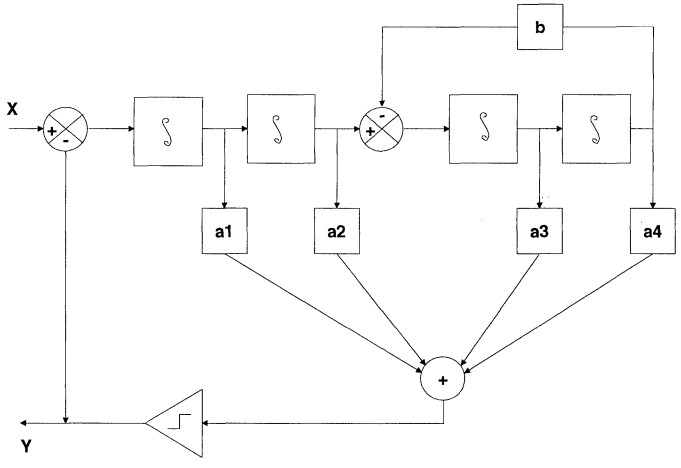

Figure 5. Modulator Block Diagram

decreasing value. Similarly, it would not be unreasonable to expect that large values of the input would lead to small effective values of g, initiating instability.

Simulation and laboratory experience has shown that the modulators do indeed exhibit this behavior. Fortunately, stable regions of operation also exist. The strategy adopted in the design of these modulators is to allow normal operation only well within the stable state space. Circuitry is provided to detect excessively high integrator levels as an indication of unstable operation. If such levels are detected, the integrators are reset to a stable condition. In practice, the reset circuitry is never utilized except at power-up (whereupon the modulator filter may or may not be in a stable state) or during periods when the input is excessively high. "Excessively high" means much higher than full scale, in which case the converter's digital output would be clipped and occasional modulator resets would be of no consequence. As the input returns to a level near full scale, the latest reset event leaves the modulator in a stable state.

3.8 Measured Spectra

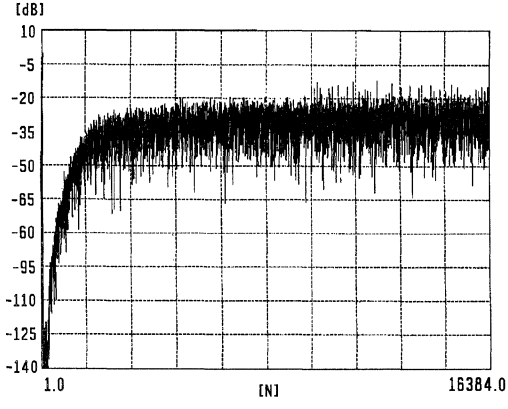

Figure 6. Simulated modulator output spectrum

Figure 6 shows a typical spectrum of a simulated modulator including a sinusoid input signal (very close to dc on the linear frequency scale) plus the quantization noise from dc to $f_S/2$. An expansion of the low frequency portion of this figure is shown in Figure 7. Here, the effect of the conjugate pair of quantization noise zeros is evident, as well as that of the pair at dc.

4. FILTER/DECIMATOR

4.1 Overall Architecture

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit, 3.072MHz outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit, 48kHz results. A functional block diagram of the digital die appears in Figure 8. Timing, control, and coefficient ROMs (FIR2 and FIR3) are shared by the two channels. Left and right channel data paths operate independently. FIR2 and FIR3 use a per-channel multiplier/accumulator.

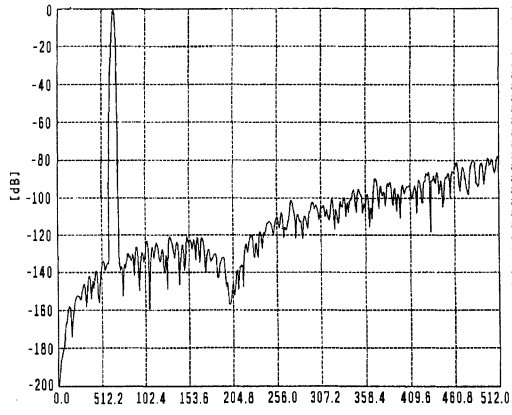

Figure 7. Expanded simulated modulator output spectrum

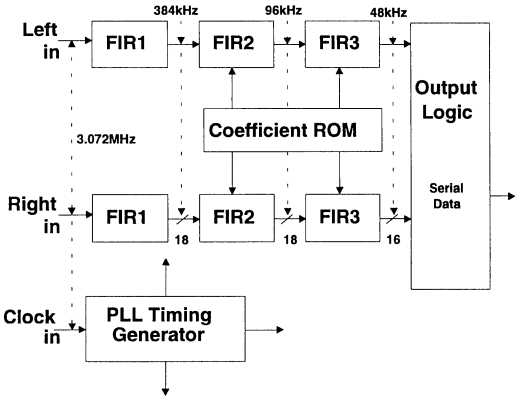

Figure 8. Filter/decimator block diagram

4.2 Decimation

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. As Figure 6 shows, modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise — and out-of-band input signals — into the converter noise floor. Filter orders are 27 and 30, respectively. Data is processed with 18-bit fixed point arithmetic.

4.3 Passband Shaping

FIR3 performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to ±0.001dB from dc to 22kHz. The passband compensation function prevents the use of a half-band filter for FIR3. The filter has 124 non-zero, 18-bit coefficients. Again, data is processed with 18-bit fixed point arithmetic. Data is truncated to 16 bits at the output, and this operation is the major noise contributor in the system.

4.4 Antialiasing Filtering

As indicated in Section 1, FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from 26kHz to 3046kHz are attenuated by at least 86dB. The magnitude response of the complete modulator/decimator from dc to 48kHz is shown in Figures 9 and 10. Phase response is precisely linear.

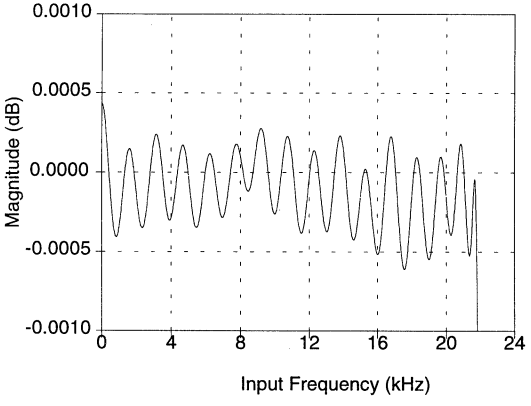

Figure 9. Filter passband ripple

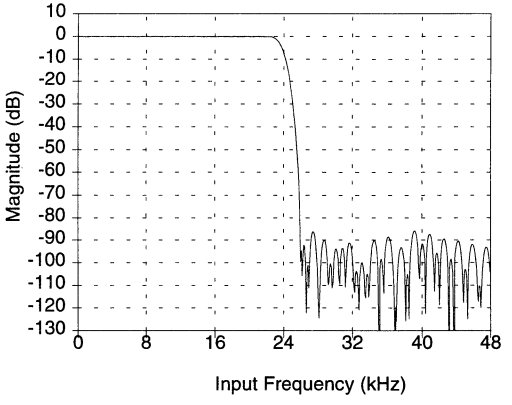

Figure 10. Filter frequency response

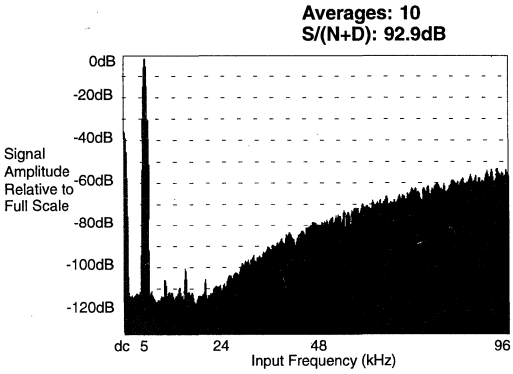

Figure 11. Partial 16K point FFT of modulator output

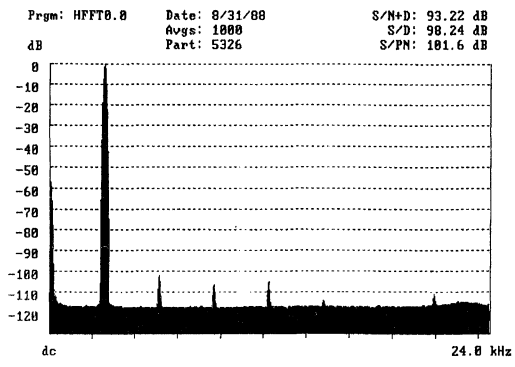

Figure 12. 1000 averaged FFTs of A/D converter

5. RESULTS

5.1 Modulator Output

Testing of the key specification parameters was performed with the aid of Fast Fourier Transform (FFT) routines. Figure 11, for instance, shows the low frequency portion of an FFT performed on a modulator's single bit output. The quantization noise shaping is evident in this plot. Absent, however, is the null due to the conjugate pair noise shaping zeros that is visible in Figure 6. The quantization noise of the modulator is masked by the device's more classical noise mechanisms. Quantization noise can only be seen rising out of the thermal noise floor at frequencies above the audio band.

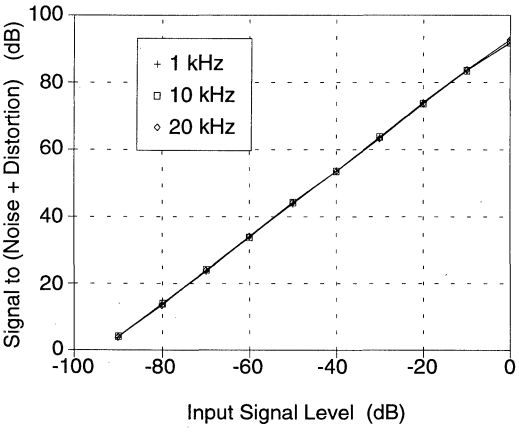

Figure 13. Signal-to-noise ratio versus signal level

5.2 Digital Filter Output

Figure 12 shows a plot of the result of an average of one thousand FFT's performed on the 16-bit words output by the digital filter. Averaging of numerous FFT's serves only to cosmetically smooth the noise floor and does not change the ratio of the signal to noise level. The width of the fundamental is due to the application of a low side-lobe window to the data stream [10].

In addition to the noise floor and the fundamental, dc and harmonic distortion components are visible. Close inspection reveals a 1/f noise corner in the area of 300Hz and a bump in the noise floor in the area of 23kHz. The latter is caused by the rising modulator quantization noise in concert with the falling digital filter characteristic.

Figure 13 is a plot of measured signal-to-noise plus distortion ratio versus signal level for 1kHz and 10kHz input frequencies. High-level performance appears slightly better for the 10kHz signal because all but the second-harmonic distortion components fall outside the baseband.

5.3 Specifications

Table 1 lists the key specifications and their measured values.

Oversampling ratio	64X
Signal-to-noise plus distortion	92 dB
Dynamic range	94 dB
Filter passband ripple	<0.001 dB
Filter stop-band rejection	>86 dB
Calibration error	5 LSB
Channel-to-channel crosstalk	-103 dB at 20 kHz
Channel-to-channel gain mismatch	0.04 dB
Gain temperature coefficient	80 ppm/°C
PSRR	50 dB
Power dissipation	450 mW

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•Notes•

The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's.

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Abstract

Sampling clock jitter is inevitable in a digital studio environment. This paper discusses the audio effects of clock jitter on an Analog-to-Digital Converter (ADC). The clock jitter sensitivity of a conventional Nyquist sampling ADC is compared and contrasted to that of a 3 MHz 64X oversampling delta sigma ADC.

0 INTRODUCTION

The increasing density of digital equipment in studios has prompted much discussion on synchronization of multiple items of digital audio equipment. The distribution of a master clock, for example via the AES/EBU interface, will inevitably add jitter to the clock. Each item of digital audio equipment that contains an analog-to-digital converter (ADC), or a digital-to-analog converter (DAC), will require a stable sampling clock, which is frequency locked to the distributed master clock. This paper investigates the amount and nature of jitter that an ADC can tolerate.

Included in the paper are a theoretical analysis of the effect of clock jitter on the sampling process, the results of a computer simulation, and measured results taken from actual ADC's with deliberately jittered clocks. Different types and amplitudes of jitter are investigated. In addition, the jitter sensitivity of a 76.8 kHz sampling ADC is compared and contrasted to that of a 3 MHz oversampling delta sigma ADC.

1 Clock Jitter Theory

The effects on ADC performance of jittering the sampling clock bear a strong resemblance to classical FM modulation. The input frequency is equivalent to the carrier frequency, and the clock jitter frequency (or spectrum) is equivalent to the modulation frequency. For simplicity of initial analysis, consider an ADC with a sine wave input signal, and a sampling clock time modulated (jittered) by a low frequency sine function. If a record of data is taken from the ADC and analyzed using Fourier analysis, then the effect of the clock jitter is to reduce the height of the input sine component, and to introduce sideband frequency components. The sideband frequencies are equally spaced either side of the input component, at a distance equal to multiples of the jitter frequency. The amplitude of the sidebands varies with the amount of clock jitter. However clock jitter is not precisely FM modulation; there are some important behavioral differences. The equation for sinusoidal sampling clock time jitter is:

$$v(t) = A \cos[\omega_i(t + J \sin \omega_j t)] \quad (1)$$

where A is the ADC input signal amplitude, ω_i is the input signal frequency, J is the peak amplitude of the jitter, and ω_j is the jitter frequency. Notice that if ω_i is increased then the contribution of the jitter term also increases. This agrees with the intuitive reasoning that if the slew rate of the input signal increases, then the amplitude error caused by clock jitter will increase. Notice also that the units of J is time, in seconds.

Equation (1) may be re-written as:

$$v(t) = A \cos[\omega_i t + J\omega_i \sin \omega_j t)]$$

Substituting $\beta = J \omega_i$ gives:

$$v(t) = A \cos[\omega_i t + \beta \sin \omega_j t)] \quad (2)$$

Equation (2) is the classical FM modulation equation, where β is the modulation index. Analysis of the height of sidebands in terms of β is well documented using Bessel functions [1], where $J_0(\beta)$ is the relative amplitude of the input frequency component, and $J_1(\beta)$ is the relative amplitude of the first pair of sidebands. Since we are only concerned with small amounts of clock jitter, and therefore small β, only the first pair of sidebands are significant.

As an example of using these formulae, let's set the input frequency to 10900 Hz, and the clock jitter peak amplitude to 1 ns. Therefore, since $\beta = J \omega_i$, $\beta = 6.848 \times 10^{-5}$ radians. Unfortunately, commonly available tables of Bessel functions have $J_0(\beta)$ and $J_1(\beta)$ values for $\beta = 0$, and then for $\beta = 0.1$, and are therefore useless for determining sideband heights for very small β. However, as a result of previous work at Crystal Semiconductor concerning testing T1 line interface parts for very low jitter specifications [2], a useful relationship between β and $J_1(\beta)/J_0(\beta)$ was noticed:

$$J_1(\beta)/J_0(\beta) = \beta/2 \quad \text{(only for very small } \beta) \quad (3)$$

This relationship is also confirmed by approximations for Bessel coefficients given in [3].

Using (3) gives us a $J_1(\beta)/J_0(\beta)$ ratio of 3.424×10^{-5}, which is -89.3 dB. Quantization noise for a 16-bit, Nyquist sampling ADC is -122 dB peak with respect to a 0 dB full scale input. Assuming the ADC is normally run at -10 dB input level for full amplitude music, then the sidebands have to be -112 dB down to guarantee non-audibility. Therefore for our example, the sidebands may be audible (ignoring masking effects of the ear).

How much clock jitter will cause a sideband to rise above the quantization noise floor, and therefore be potentially audible? Using the above equations, and for an input frequency of 10900 Hz, assuming a 16-bit ADC, the answer is 232 ps peak clock jitter. This result aligns well with previously published estimates [4].

2 Clock Jitter Simulations

In order to facilitate the understanding of the effects of clock jitter, a simulation program was written, shown in Figure 1. Line 160 through line 210 form the main program loop, which increments the time sample count, G, by one for each pass. Line 170 calculates the jitter amplitude for each sample. Line 180 simulates a pure cosine input signal, jittered by an amount of time, J. Notice the use of double precision arithmetic. Lines 185 and 200 quantize the output values to X bits. The output of the program is a set of numbers which are written to a file.

To confirm the accuracy of the simulation compared to theory, the program was run with the same input conditions as used in the theory example. The resulting file of numbers was then processed by a standard FFT analysis and display program in routine use at Crystal Semiconductor for testing all types of ADCs [5]. Figure 2 shows the resulting spectrum. The two sidebands are 89.66 dB down from the input frequency amplitude, which agrees closely with the theoretical result.

Modifying line 170 allows changing the nature of the clock jitter. Changing line 180 allows investigation of different ADC input signals.

3 Measured Results

A CS5101 sampling successive approximation ADC was used to verify the theoretical and simulation results. Figure 3 shows the test set-up. A 6.144 MHz clock was used to allow later substitution of an alternate delta-sigma ADC. Using a 6.144 MHz clock determines the sample rate of 76.8 kHz. Figure 4 shows the Phase Lock Loop (PLL) circuit used to inject clock jitter. The set-up was verified to introduce no additional distortion compared to a jitter free crystal based clock source. Clock jitter is added by injecting the desired jitter modulation signal into the Voltage Controlled Oscillator (VCO) of the PLL.

Using the same conditions as used for the theoretical and simulation example, the sidebands were shown to be 89.74 dB down from the input frequency component, shown in Figure 5. This validates the theory and simulation results. The clock jitter was checked by displaying a divided down version of the jittered clock on a delayed time base oscilloscope. Figure 6 shows a rising edge of the divided clock, corrupted by 1 ns peak jitter. This measurement was taken at the same time as the Figure 5 test result plot.

Correlation between clock jitter amplitude and side-band height has previously been verified at Crystal Semiconductor by compared the jitter readings of an HP 3785A jitter test unit with the same clock jittering an ADC sampling clock [2].

4 Oversampling ADC Clock Jitter Sensitivity

Oversampling delta-sigma ADC's have several advantages over more traditional Nyquist sampling successive approximation ADC's and are also becoming more available [6] . The CS5326 from Crystal Semiconductor has an oversampling ratio of 64, sampling the input at 3 MHz. The output of the delta sigma modulator is a 3 MHz serial bit stream which is then digitally filtered (dc to 22 kHz) and decimated to produce 16-bit numbers at a 48 kHz word rate. How sensitive is such an ADC to clock jitter?

As a proportion of clock period, a given amount of jitter is more significant to a 3 MHz sampling clock, compared to a 50 kHz sampling clock. However the amount of amplitude error resulting from the clock jitter is the same in both cases, since the slew rate of the input signal is the same. Also, for noise induced jitter, the extra noise induced by the jitter will be spread out between dc and 1.5 MHz, and then low pass filtered by the 22 kHz cut-off digital filter. Thus it is reasonable to speculate that an oversampling delta-sigma ADC will be no more sensitive to clock jitter than a Nyquist sampling ADC. To prove this hypothesis, a theoretical simulation was performed, along with measured results.

Figure 7 shows the results of the CS5326 oversampled ADC simulation program. The input conditions were the same as previously used, that is an input frequency of 10900 Hz, 1 ns peak sinusoidal 980 Hz jitter, and -10 dB input amplitude. The difference in amplitude between the fundamental and the jitter induced sidebands is 89 dB, which is the same result as obtained in the Nyquist sampling case. The lack of low frequency noise in Figure 7 is because the simulation did not include the final truncation to 16-bits after the filter.

Figure 8 shows the measured results from the CS5326 oversampled ADC. The test conditions were the same as above, and the test set-up was the same as shown in Figure 3, using a CDB5326 evaluation board. The plot shows that the difference in amplitude between the fundamental and the jitter induced sidebands is 89.5 dB, which agrees well with the oversampled ADC simulation results, and with the previously given non-oversampled ADC test results.

The above results confirm that an oversampled delta-sigma ADC has the same sensitivity to clock jitter as a Nyquist sample rate ADC.

5. Non Sinusoidal Jitter

In practical hardware, clock jitter will not be sinusoidal. It is likely to consist of noise components and some periodic components. To investigate the effects of white noise jitter, the simulation program given in Figure 1 was modified, replacing the sine jitter equation with a random number generator equation (Figure 9).

A number of simulations were run which show that white noise clock jitter results in an overall elevation of the noise floor of the ADC system. This will degrade the available dynamic range. For example, 2 ns peak white noise clock jitter will degrade a perfect 16-bit ADC from a dynamic range of 98 dB to 91 dB (Figures 10 &11). To reduce clock jitter effects to less than 0.5 dB impact on dynamic range, the peak jitter amplitude has to be less than 400 ps (Figure 12).

For oversampling ADC's, we speculated that the effects of clock jitter noise would be treated like quantization noise, that is spread out between DC and half the input sample rate, and then filtered by the audio bandwidth digital filter. Figure 13 shows the results of a delta sigma ADC simulation, with 2 ns peak white noise clock jitter. Compared to Figure 11, this confirms that the delta sigma ADC is much less sensitive to white noise clock jitter. As with Figure 7, Figure 13 does not include 16-bit quantization noise.

6. Conclusions

A combination of theoretical analysis, computer simulations and practical measurements has allowed the confident prediction of the audible effects of sampling clock jitter. As the resolution, and therefore dynamic range, of ADC's and DAC's increase beyond 16-bits, sampling clock jitter will become more significant. The analysis techniques presented allow maximum allowable levels of clock jitter to be determined.

It has been demonstrated that delta-sigma oversampling ADC's are no more or less susceptible to the effects of clock jitter than Nyquist sampling architectures. It has also been shown that delta-sigma oversampling ADC's are less sensitive to random noise clock jitter than Nyquist sampling ADC's.

7. Acknowledgments

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```
10 REM  ADC SIMULATION PROGRAM "JITSINE"     Steven Harris  8/3/89

95 INPUT "Number of samples in output file ?",SIZE
96 REM Set X = to # of bits in ADC
97 LET X = 16
100 PRINT "JITSINE generates ";SIZE;" numbers quantized to ";X;" bits"
102 PRINT "Random phase offset added to simulate asynchronous sampling"
103 PRINT "Sine wave jitter is added to the sampling clock"
110 REM The numbers are dumped in a file as 5 digit decimal values
112 INPUT "File name to write numbers ? ",F$
113 OPEN "O",#1,F$
116 Offset=RND
117 Offsetj=RND
135 LET PI#=3.141592654
143 INPUT "Sample Frequency ?",FS#
145 INPUT "Input Signal Frequency ?", FIN#
146 INPUT "Input Signal Amplitude relative to full scale (=1) ", INAMP#
147 INPUT "Jitter Frequency ?",FJ#
149 INPUT "Peak amplitude of clock jitter in seconds ?",JPA#
160 FOR G = 1 TO SIZE
168 REM Form jitter amplitude for this time sample
170 LET J# = JPA#*SIN(Offsetj + ((G-1)*2*PI#*FJ#/FS#))
172 REM Form unquantized clock jittered cosine value for this sample
180 LET A# =INAMP#*COS(2*PI#*FIN#*(((G-1)/FS#)+J#)+Offset)
182 REM Scale to X bits
185 LET A# = A#*(((2^X)/2)-1)
198 REM Quantize levels (round to nearest integer)
200 LET S = CINT(A#)
205 REM PRINT "#="G;"Value=";A#;"Quantized value=";S
207 PRINT #1, USING "######";S
210 NEXT G
220 CLOSE #1
```

Figure 1. BASIC program which simulates a perfect N-bit ADC with sinusoidal clock jitter

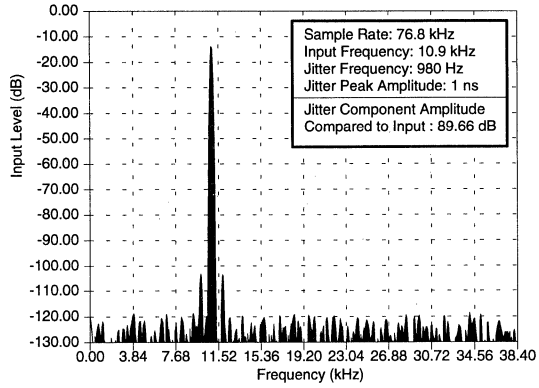

Figure 2. Nyquist Sampling ADC Simulation with 1 ns Peak Sine Clock Jitter

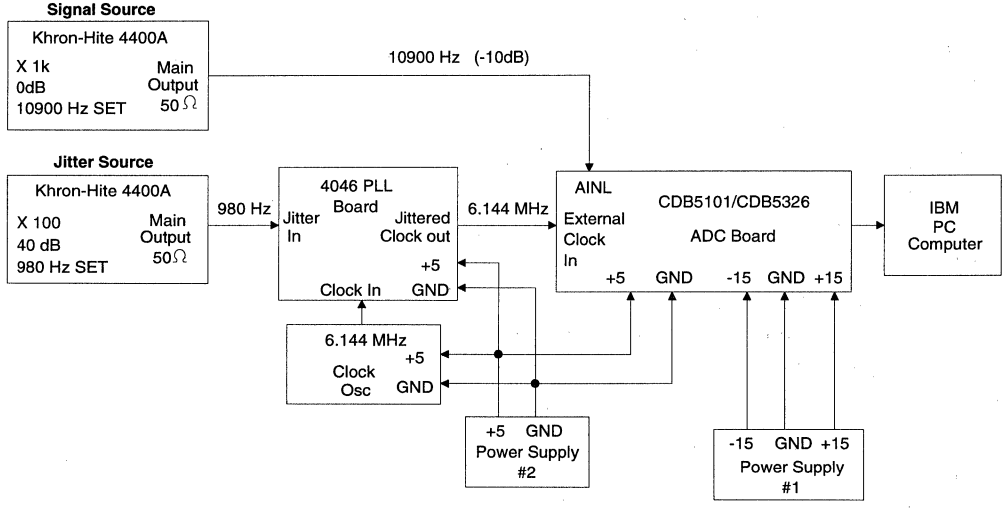

Figure 3. Jitter Experiments Test Set-up

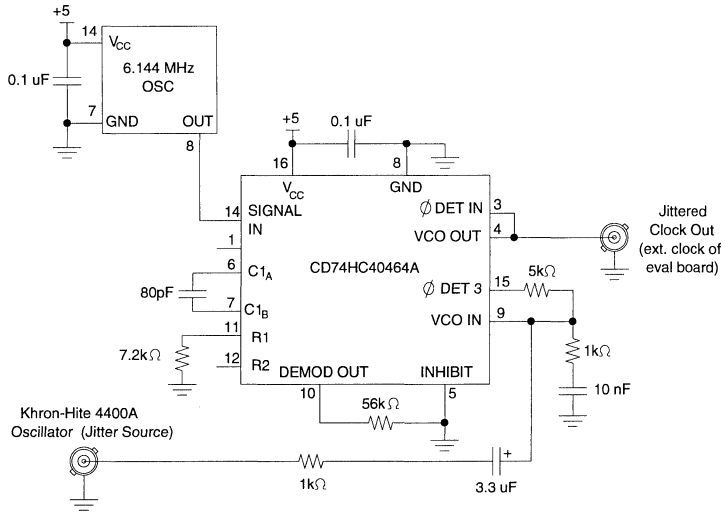

Figure 4. Phase Locked Loop Jitter Generator Schematic

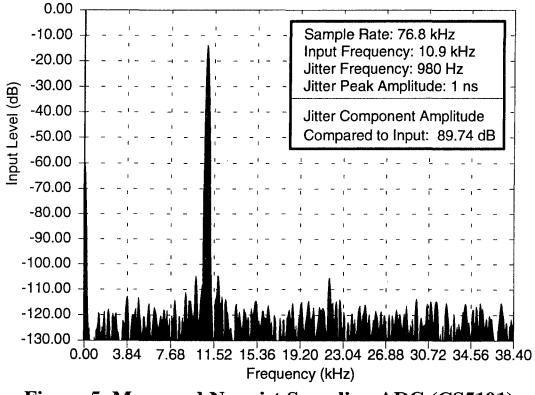

Figure 5. Measured Nyquist Sampling ADC (CS5101) with 1 ns Peak Sine Clock Jitter

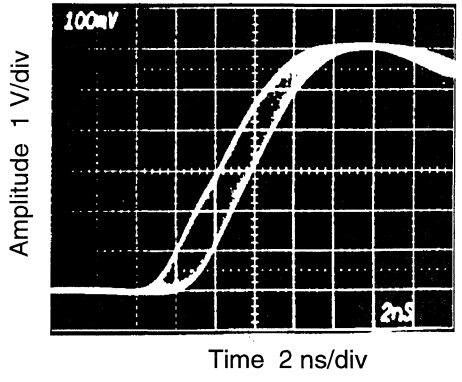

Figure 6. ADC Sampling Clock Jitter Measured at the Output of the Clock Jitter Generator Shown in Figure 4

8

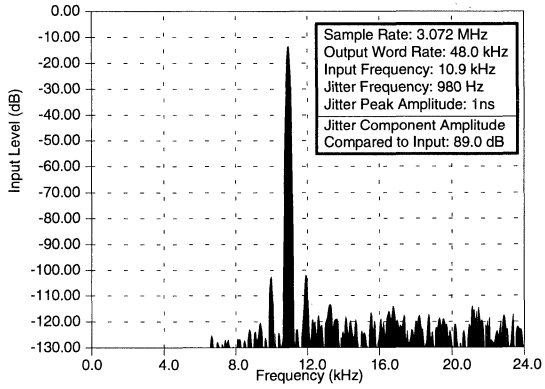

Figure 7. Simulated 64x Oversampling Delta Sigma ADC with 1 ns Peak Sine Clock Jitter

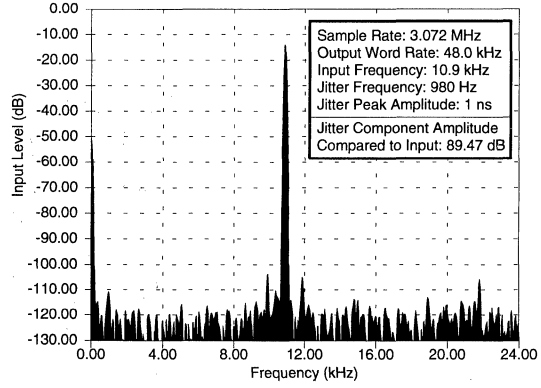

Figure 8. Measured 64x Oversampling Delta-Sigma ADC (CS5326) with 1 ns Peak Sine Clock Jitter

```
10 REM  ADC SIMULATION PROGRAM  "JITNOISE"  Steven Harris 8/3/89

95 INPUT "Number of samples in output file ?",SIZE
96 REM Set X = to # of bits in ADC
97 LET X = 16
100 PRINT "JITNOISE generates ";SIZE;" numbers quantized to ";X;" bits"
102 PRINT "Random phase offset added to simulate asynchronous sampling"
103 PRINT "White noise jitter is added to the sampling clock"
110 REM The numbers are dumped in a file as 5 digit decimal values
112 INPUT "File name to write numbers ? ",F$
113 OPEN "O",#1,F$
116 Offset=RND
117 Offsetj=RND
135 LET PI#=3.141592654
143 INPUT "Sample Frequency ?",FS#
145 INPUT "Input Frequency ?", FIN#
146 INPUT "Input signal amplitude relative to full scale (=1) ?", INAMP#
149 INPUT "Peak amplitude of clock jitter in seconds ?",JPA#
160 FOR G = 1 TO SIZE
169 LET NOISE=RND
170 LET J# = JPA#*(NOISE*2-1)
172 REM Form perfect clock jittered sine
180 LET A# = INAMP#*COS(2*PI#*FIN#*(((G-1)/FS#)+J#)+Offset)
182 REM Scale to X bits
185 LET A# = A#*(((2^X)/2)-1)
198 REM Quantize levels (round to nearest integer)
200 LET S = CINT(A#)
205 REM PRINT "#="G;"Value=";A#;"Quantized value=";S
207 PRINT #1, USING "######";S
210 NEXT G
220 CLOSE #1
230 GOTO 95
```

Figure 9. BASIC program which simulates a perfect N-bit ADC with noise jittered clock

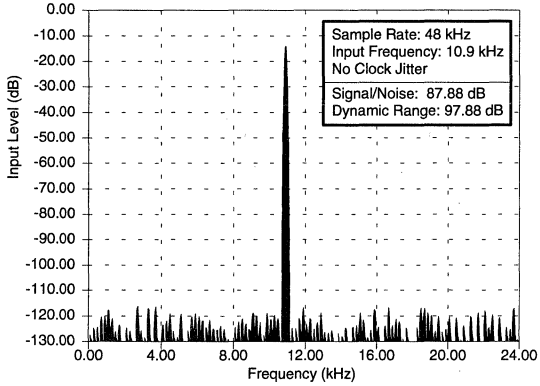

Figure 10. Nyquist Sampling ADC Simulation with No Clock Jitter

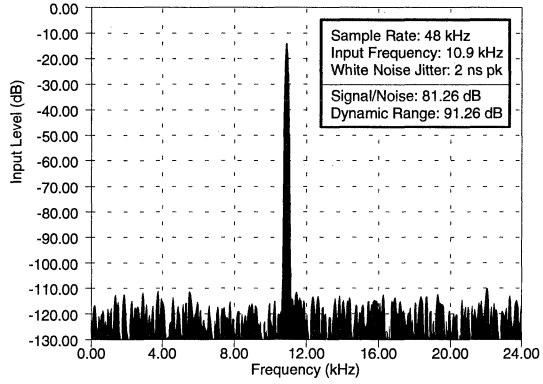

Figure 11. Nyquist Sampling ADC Simulation with 2 ns Peak White Noise Clock Jitter

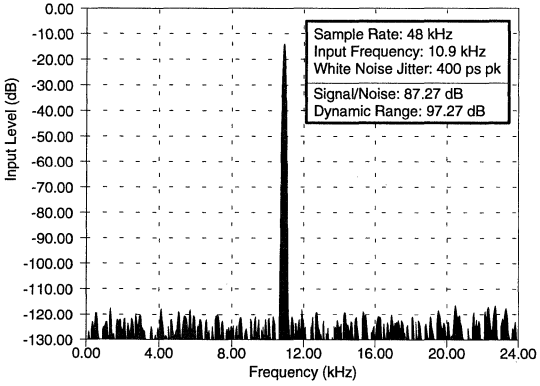

Figure 12. Nyquist Sampling ADC Simulation with 400 ps Peak White Noise Clock Jitter

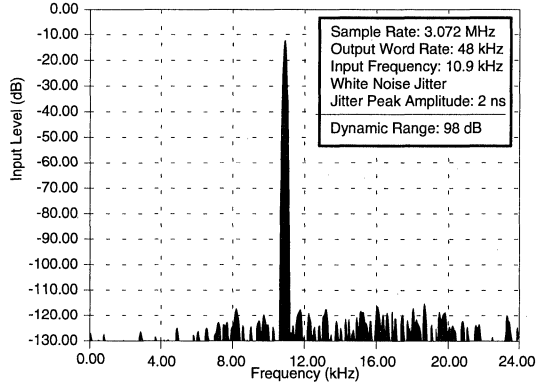

Figure 13. Simulated 64x Oversampling Delta-Sigma ADC with 2 ns Peak White Noise Clock Jitter

18-BIT STEREO D/A CONVERTER WITH INTEGRATED DIGITAL AND ANALOG FILTERS.

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ABSTRACT

This paper describes an integrated digital audio Digital-to-Analog output system. The circuit consists of an 8x digital interpolation filter followed by a 64x oversampled Delta-Sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low pass filter. The total D/A system provides a linear phase response.

INTRODUCTION

Delta-sigma modulation has become the conversion technology of choice for audio-band data converters. Analog-to-Digital converters using the delta-sigma conversion principle have been available for many years. The several advantages of delta-sigma modulation already demonstrated for A/D converters also apply to D/A converters. The benefits of delta-sigma modulators over conventional laser trimmed converters include:

1. No differential linearity error.
2. No distortion mechanisms due to component mismatch.
3. No laser trimming.
4. No linearity error drift over time and temperature.

Previous delta-sigma audio D/A converter implementations have either not integrated the analog filter or required several external filter components [1],[2]. These implementations require component value changes for large variations in conversion rate. This paper presents an 18-bit stereo D/A converter employing delta-sigma modulation that integrates digital and analog filters that track the conversion rate. No external components are required.

The block diagram of the complete system is shown in figure 1. An 8x interpolation filter removes out-of-band images. The output of the interpolator is held for eight, $64f_S$ cycles and fed into a 5th order delta-sigma modulator. An analog filter removes high frequency quantization noise in the modulator output and presents a signal suitable for playback. The interpolation filter and modulator

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are implemented on a 1.6 µm double metal CMOS chip. The analog filter is implemented in a 3 µm CMOS chip. Both chips are packaged in one 28-pin DIP.

INTERPOLATION FILTER

The purpose of the digital interpolation filter is to remove images of the baseband audio signal that exist in the sampled data signal. Figure 2a shows the spectrum of the sampled data signal that is input to the D/A converter. The spectrum (chosen here to have near uniform frequency content) has images of the baseband audio signal that repeat at the input sample rate (f_S) of the D/A converter. Although the frequency content of the images is above the human hearing range (20kHz), inevitable nonlinearities downstream from the D/A converter require removal of these images. Intermodulation of the signals above the audio band by these nonlinearities can result in audible by-products. Figure 2f is the desired signal that should be output by the D/A converter.

The interpolation filter is implemented in three consecutive interpolate by 2 stages as shown in Figure 3. This three stage FIR architecture meets two design goals. The first goal is adequate image rejection. The second design goal is to implement two channels of interpolation filters with a single hardware multiplier that operates at a maximum clock rate of $256f_S$ (12.288MHz for sampling rate of 48kHz).

The first stage of interpolation is a 125 tap half-band FIR filter (i.e. every other coefficient except for the center coefficient is zero) [3]. The half-band topology is well suited for 2x interpolation and decimation filters since it provides rejection above one fourth the filter's sample rate reference. The spectrum at the output of the first stage is shown in figure 2b. Note that the first image is removed by this stage of filtering. The first stage is the most difficult of the three interpolation stages since it requires the steepest roll-off characteristics.

The second interpolate by two stage is a 24 tap FIR filter. The third interpolate stage is a 4 tap FIR filter. The spectra at the output of the second and third stages are shown in figure 2c and 2d, respectively. Note that the complete interpolation filter provides less attenuation for higher frequencies than for frequencies just outside the audio band. This is done with the knowledge that the analog filter will easily attenuate signals at higher frequencies but will have difficulty filtering signals just above the audio band.

Eighteen bit wide data paths with 19-bit coefficients are used throughout the interpolation filter. The S/N for a full scale sinewave (noise due to truncation) of the interpolation filter is over 107dB in the audio band.

DELTA-SIGMA MODULATOR

The fifth-order delta-sigma modulator shown in figure 4 is used to convert the output of the interpolation filter into a 1-bit stream. The signal is converted to a 1-bit stream so that an inherently linear 1-bit D/A converter can be used. The modulator is sampled at $64f_S$. The output of the interpolation filter is held for eight consecutive modulator clock cycles yielding a sinc filter characteristic. The

spectrum of the signal at the input to the modulator is shown in figure 2e. The fifth order modulator was chosen to keep all inband quantization noise peaks well below -130dB, and is similar to other high order modulator topologies [4]. The spectrum at the output of the modulator is shown in figure 5 for a modulator sample rate of 3.072MHz. This figure is a simulation of the modulator alone and does not include any effects of the digital or analog filters. The S/N of the modulator in the 20kHz audio band is 120dB.

1-BIT D/A

The many advantages of 1-bit D/A conversion can only be enjoyed if the D/A converter has only two distinct output levels. Errors in the two output levels caused by noise, interference, or dependence on previous states can substantially degrade the S/N ratio of the D/A converter. Many delta-sigma D/A converters perform the 1-bit conversion by holding an output voltage level for a finite duration of time defined by periods of a master clock source[1]. This waveform is then filtered by a continuous-time analog filter. The resulting output is highly dependent on purity of the clock signal used to gate the output voltage level. Jitter in the clock source directly translates to errors in the 1-bit D/A output.

The requirement for a low jitter clock can be essentially eliminated by the use of a switched capacitor structure. A switched capacitor filter processes packets of charge. The 1-bit D/A converter is implemented by charging a capacitor to a voltage reference and choosing the appropriate polarity of the charge by one of two switching arrangements. As long as the voltage reference value settles on the capacitor, the magnitude of the charge packet will be independent of the clock jitter.

ANALOG FILTER

The block diagram of the analog filter is shown in figure 6. The first switched-capacitor filter has fourth-order Butterworth response with a -3dB frequency of 25kHz. The topology of the fourth-order switched capacitor filter is shown in figure 7. The multiple feedback loop topology is chosen over the traditional cascaded biquad configuration for its high noise rejection of integrators 2, 3, and 4. The sampling rate of the switched capacitor filter is $64f_S$, identical to that of the delta-sigma modulator.

Switched capacitor filters have generally been used in telecommunications circuits for their precise frequency response characteristics and their unique ability to scale frequency response directly with the clock rate. Switched-capacitor structures used as 1-bit D/A post filters offer the further benefit of easing the delicate transition from discrete-time to continuous-time processing. With the exception of the final stage, signal processing in a switched-capacitor filter is performed entirely in the sampled-data domain where nonlinear opamp settling behavior cannot distort signals of interest. Consequently, the strong high frequency energy of the 1-bit pattern is substantially reduced before it has the opportunity to excite any dynamic nonlinearities in subsequent continuous-time filtering.

The use of switched-capacitor filters in audio applications has been quite limited because of their traditionally inadequate dynamic range. The economics of integration have historically restricted switched capacitors to values that realize relatively high effective impedances. The result is a high

thermal noise floor in the frequency range of interest. In this design, dynamic range is extended to 97dB (A-weighted) by appropriate selection of loop topology, opamp topology and capacitor values.

The distortion mechanisms traditionally associated with switched-capacitor structures have further limited their use in high performance applications. Distortion in switched capacitor filters is primarily caused by nonlinear charge injection during sampling, opamp dc nonlinearities and slewing of the final stage output waveform between settled output levels [5]. In this design charge injection is kept independent of input signal levels by appropriate switch phasing, and dc opamp nonlinearity is made negligible by sufficient open loop gain.

The third distortion mechanism, arising from opamp output slew limiting, is generally the most difficult to control. Since the output of the switched capacitor filter is being treated as a continuous-time waveform, the exact nature of the transition from one settled value to the next is critical in achieving a low distortion waveform. Nonlinear behavior in this transition must be avoided.

To ease the transition between the switched-capacitor domain and the continuous-time domain the switched-capacitor to continuous-time buffer of figure 8 is used. This buffer samples the output of the switched capacitor filter after it is settled and provides a continuous-time waveform free from distortion artifacts. The switching arrangement ensures that the charge transfer from C1 to C2 is done passively and not with the assistance of the amplifier. The amplifier only supplies the charge to the output load capacitance, which at low frequencies is minimal. This buffer has a single pole response with a -3dB frequency of 50kHz.

A continuous-time filter is used to remove the remaining images at multiples of the switched capacitor sample rate ($64f_S$). The continuous-time filter has a second order butterworth response with a -3dB frequency of 80kHz. The output stage of the continuous-time filter is capable of driving a 600Ω load with less than 0.0015% THD at 10kHz.

MAGNITUDE AND PHASE RESPONSE

Although the magnitude response of the analog filter is fairly flat due to the Butterworth response, it is not sufficient for digital audio quality. To achieve greater flatness the response of the analog filters is compensated in the digital interpolation filter. FIR2, the second stage of interpolation, performs the magnitude compensation. The total calculated magnitude response of the D/A system is shown in figure 9.

Since the nonlinear phase response of the analog filter is also a concern, the phase response of the analog filter is also equalized in the digital interpolation filter. Again, FIR2 is used for phase equalization. Figure 10 plots the deviation from linear phase for the analog filter, digital filter and the combined D/A system. Total deviation from linear phase is kept to less than 0.7° in the audio band. Since the frequency response of the analog filter is dominated by the switched capacitor filter, the magnitude and phase equalization will be valid at any sample rate of the D/A converter.

OFFSET CALIBRATION

In any integrated analog filter significant dc offsets can be generated. In this design offset calibration is performed to lower the effective offset to approximately 20 µV. A comparator measures the analog output of the filter with respect to ground and a successive approximation search is used to find the offset at the input to the delta-sigma modulator. Since the comparator does not band limit at 20kHz, its decisions are impacted by the entire out-of-band quantization noise left at the output of the analog filter. To achieve repeatable and accurate calibration the output of the comparator is averaged for 1024 cycles before a successive approximation decision is made.

The actual implementation of the comparator is shown in figure 11. The output stage of the continuous-time filter is disconnected from the chip output and is used as a comparator. This eliminates the need to design a zero offset comparator and also isolates the chip output from any audible clicks that may be generated by the successive approximation search.

Audio systems are susceptible to pops and clicks generated by active circuitry during power-up and power-down transients. This design incorporates a low power supply detect circuit which holds the output shorted to ground (i.e., same as calibration mode) until the supplies are sufficiently high to allow the remainder of the analog filter to operate correctly. Hysteresis in the low supply detect circuit prevents rapid toggling of the switches near the trip point. As a result, turn-off and turn-on power transients are inaudible even for loud listening levels.

MEASURED RESULTS

The D/A has been characterized using a CBS Test Disk 1 and an Audio Precision System One. The measured magnitude response of the complete D/A system is shown in figure 12. The slight peaking near 20kHz of 0.1dB is due to a systematic mismatch of capacitors in the switched-capacitor filter. Unweighted THD+N (0-22kHz) versus input sinewave level is shown in figure 13. A considerable portion of the output noise is concentrated near the upper end of the audio range. Dynamic range from 0-20kHz is 93.8dB and A-Weighted dynamic range is 97dB. Figure 14 is a plot of the output spectrum of a -90dB dithered sinewave at 1kHz. Because of the ideal differential nonlinearity of the 1-bit D/A, the noise floor is quite smooth. A key test of D/A converters is the fade-to-noise linearity test shown in figure 15. A monotonically decreasing sinewave is fed into the D/A converter. The energy of the output sinewave is compared with the energy of the input. Deviations from 0dB are a result of differential nonlinearity or noise. The D/A exhibits excellent performance down to -95dB where the residual output noise starts to dominate the measurement. Figure 16 is a plot of the idle channel output spectrum from 0 to 100kHz showing the relatively low level of out-of-band quantization noise. The total energy from 0-100kHz is 78dB below full scale. Table 1 is a summary of the system performance specifications.

CONCLUSION

An 18-bit D/A converter using delta-sigma modulation has been presented. The design integrates an 8x interpolation filter with a fifth order delta-sigma modulator. On a separate chip an analog filter using a combination of switched-capacitor and continuous-time filters is implemented.

Switched-capacitor filters have the ability to change bandwidths without changing component values. One bit D/A converters implemented with switched-capacitors offer excellent clock jitter tolerance. The design difficulties associated with high quality switched-capacitor filters have been mastered. In the future even higher dynamic range switched-capacitor filters can be expected.

REFERENCES

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[4] W.L.LEE and C.G. SODINI, "A Topology for Higher Order Interpolative Coders," ISCAS Digest, 1987, pp.459-462.

[5] K.LEE and R.G.MEYER, "Low-Distortion Switched-Capacitor Filter Design Techniques," IEEE J. Solid-State Circuits, vol.SC-20 no.6, pp.1103-1113, December 1985.

TABLE 1

Dynamic range A-weighted (18-bit mode)	97dB
S/THD 1kHz	92dB
Interchannel Isolation 1kHz	-110dB
Power Consumption	
Digital	150mW
Analog	420mW
Deviation from flat magnitude	
Total D/A System	0.1dB
Deviation From Linear Phase Total D/A System	< 0.7°
Digital Filter Stop Band Attenuation	90dB
Digital Filter Pass Band Ripple	0.001dB

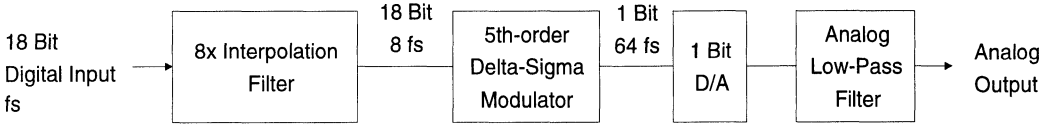


Figure 1. 18 Bit D/A Converter Architecture

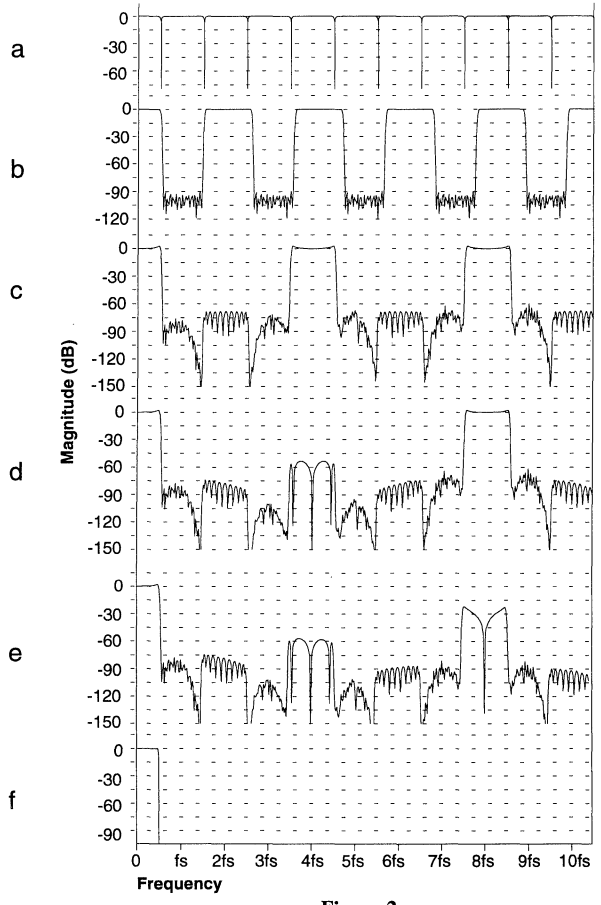


Figure 2.

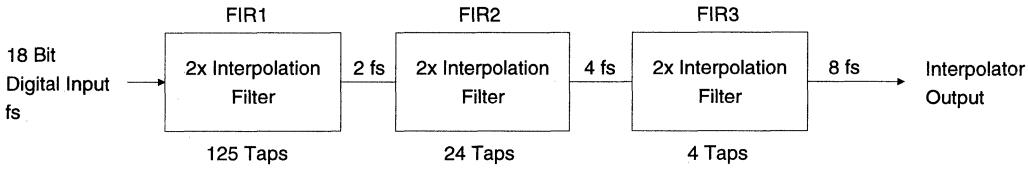


Figure 3. Interpolation Filter Architecture

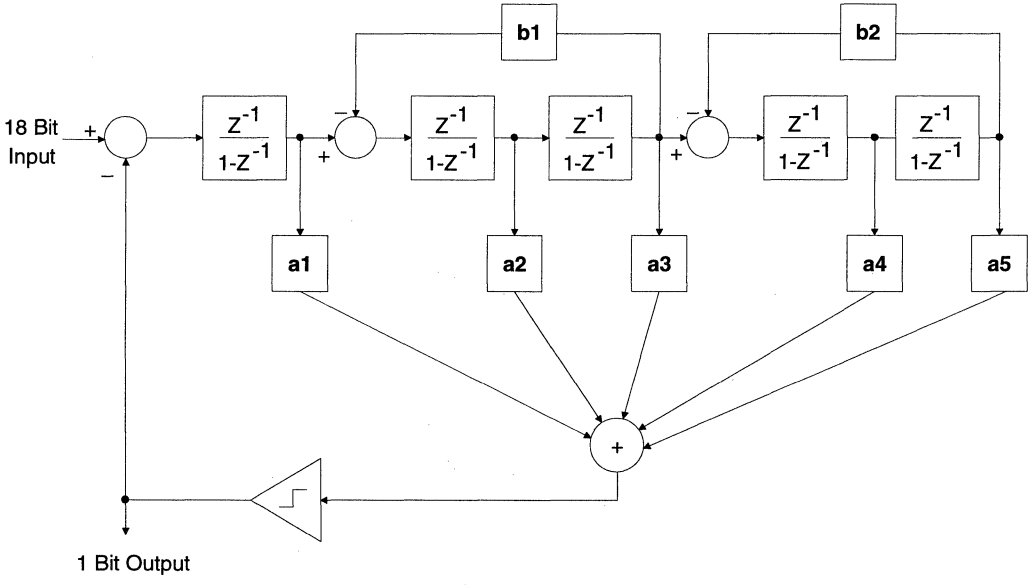


Figure 4. Digital Delta-Sigma Modulator

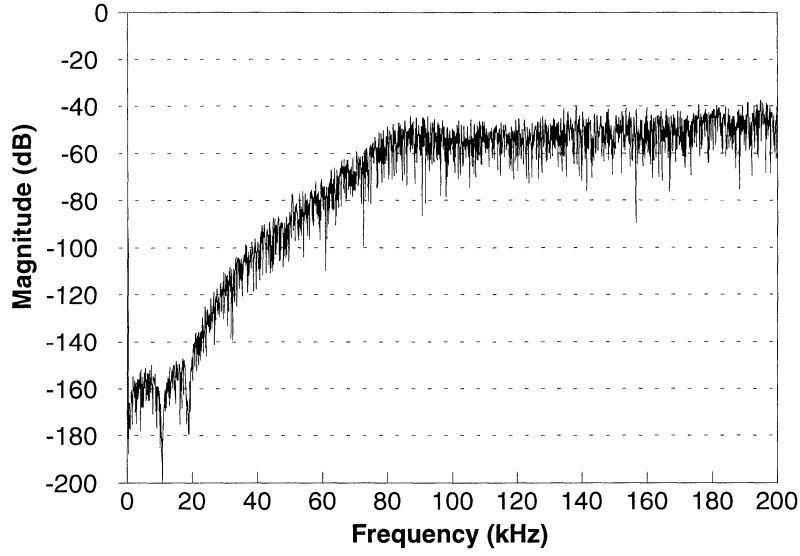


Figure 5a. Modulator Output Spectrum

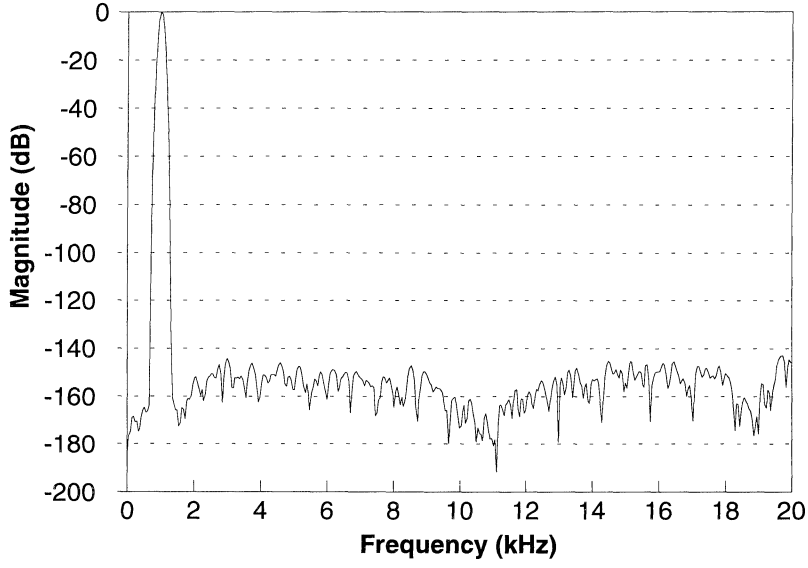


Figure 5b. Expanded Modular Output Spectrum

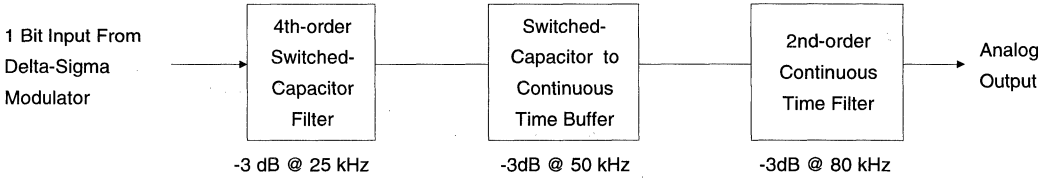
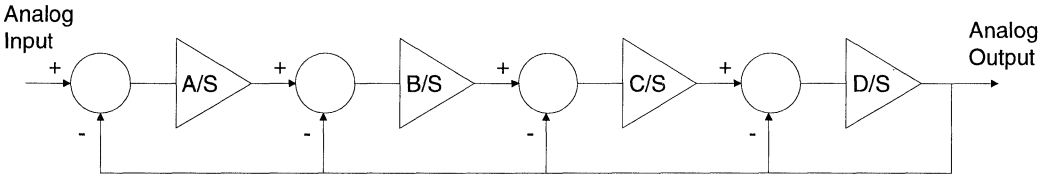


Figure 6. Analog Filter Architecture



$$\frac{Vo(s)}{Vin(s)} = \frac{ABCD}{S^4 + DS^3 + CDS^2 + BCDS + ABCD}$$

Figure 7. Switched Capacitor Filter Topology

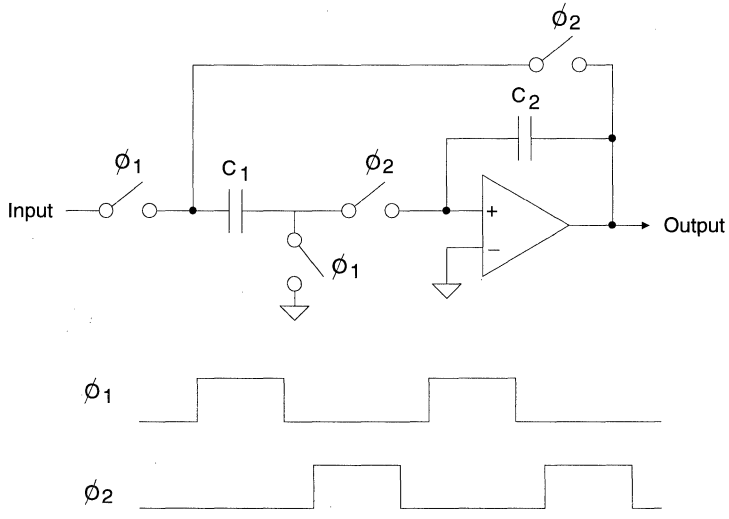


Figure 8. Switched-Capacitor to Continuous Time Buffer

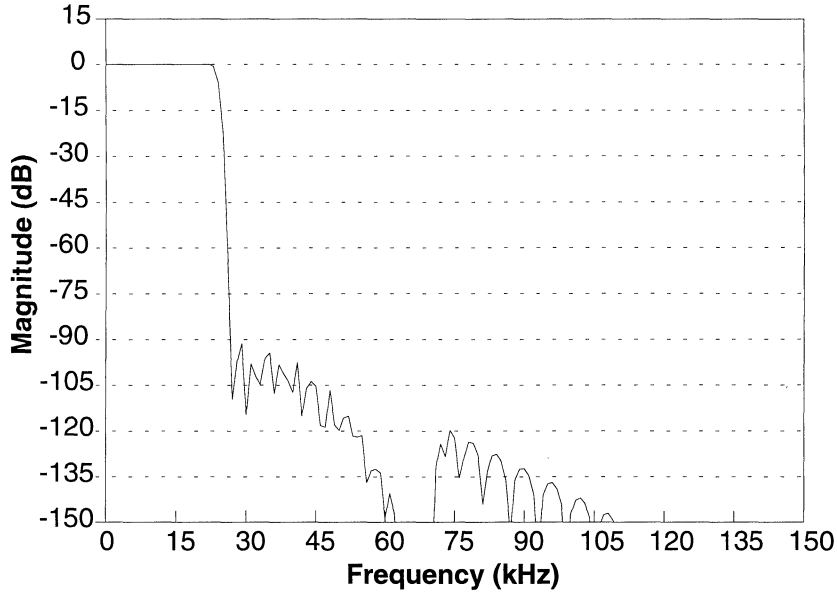


Figure 9. Total D/A System Magnitude Response

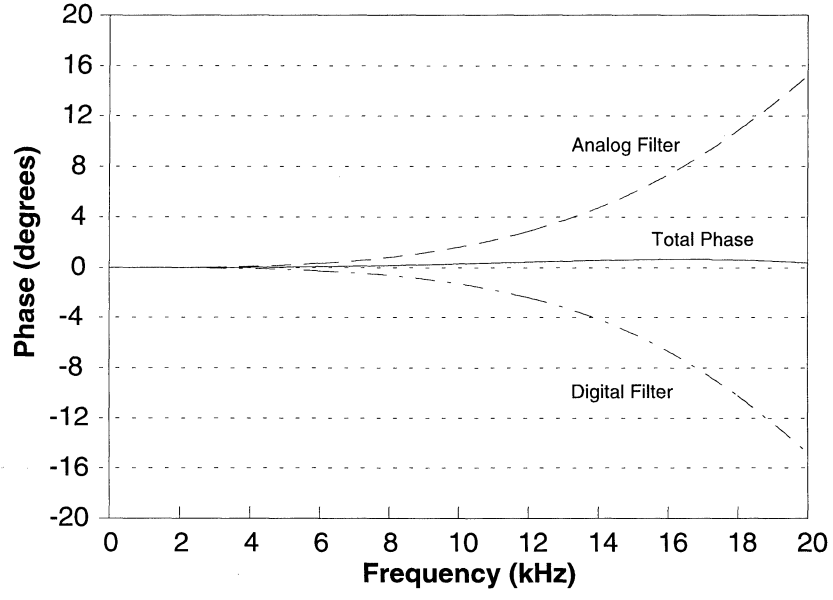


Figure 10. Deviation From Linear Phase

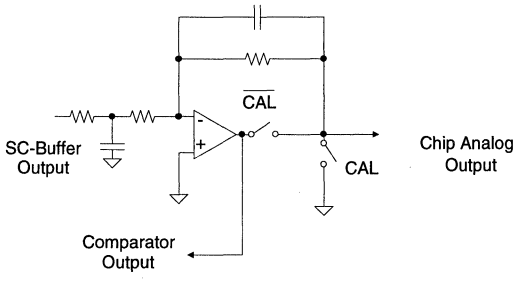


Figure 11. Offset Comparator

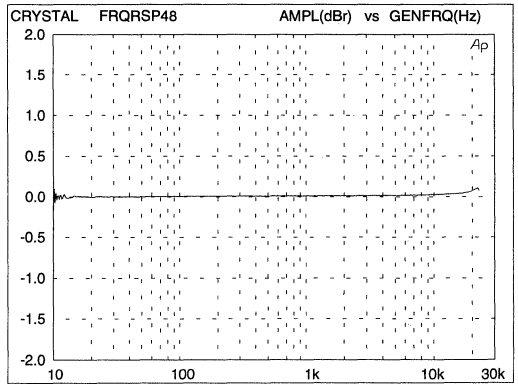


Figure 12. Frequency Response (48 kHz word rate)

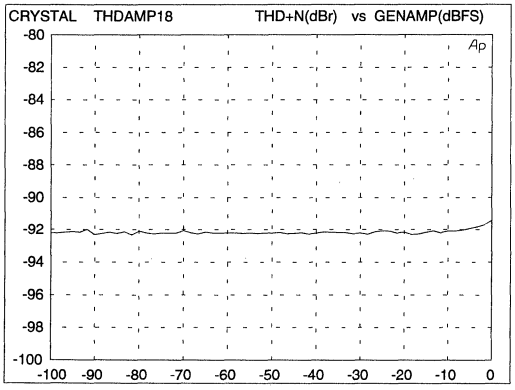


Figure 13. THD+N vs 18-bit Input Signal Level

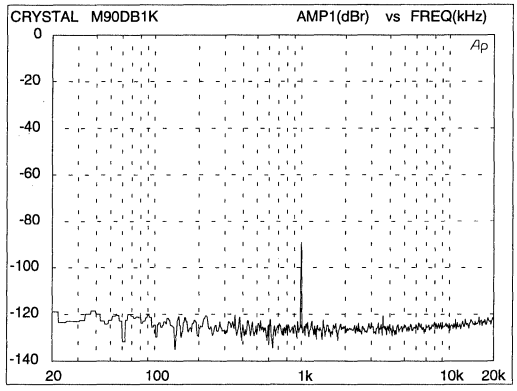


Figure 14. 1 kHz, -90dB Input FFT Plot

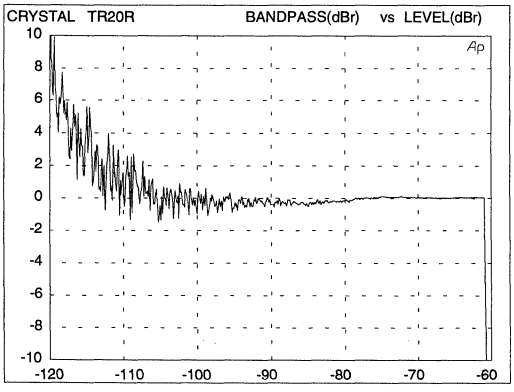


Figure 15. Fade-to-Noise Linearity

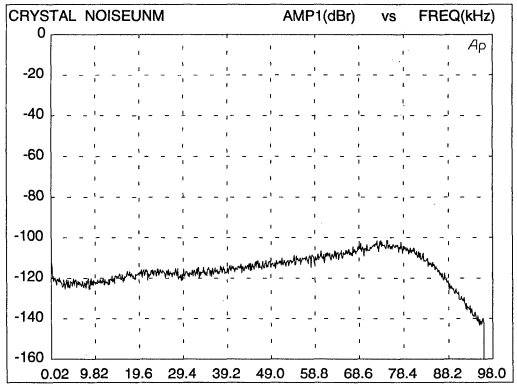


Figure 16. Unmuted Idle Channel Noise

A Family of AES-EBU Interface Devices

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ABSTRACT

This paper describes a family of digital audio transmitters and receivers which conform to the AES-EBU interface standard. Different versions are used to control the interface to various levels of complexity. Few external components are required to create a complete transmission link. The paper introduces the AES-EBU standard and illustrates the chip architectures.

0 INTRODUCTION

"The AES-EBU digital audio interface has been slow to gain market acceptance, partly because of interface complexity, specification ambiguities, lack of commercial IC's, and the effort required for discrete implementations." [1] To alleviate these problems and promote widespread use of the interface, Crystal Semiconductor has defined a family of integrated circuits that will facilitate the implementation of the AES-EBU standard. These IC's are general purpose, providing compatibility as the specifications mature, support the similar consumer-style interface, and consist of two versions of transmitters and receivers. Since the transmitters are commercially available today and the receivers are still in development, this paper will primarily discuss the transmitters, following a brief overview of the interface specifications.

1 AES-EBU SPECIFICATIONS

The AES-EBU interface, described in AES3-1985 [2], is a means for serially communicating digital audio data through a single transmission line. It provides 2 channels for audio data, a method for communicating control information, and some error detection capabilities. This control information is transmitted 1 bit per sample and accumulates in a block structure. Data is biphase encoded, which enables the receiver to extract a clock from the data, with coding violations identifying sample and block boundaries. The electrical specifications for the AES-EBU interface are compatible with RS-422 [3].

The structure of the serial word, called a subframe, is illustrated in Figure 1. The subframe consists of 4 bits of preamble, 4 bits of auxiliary data, 20 bits of audio data, a parity bit, and 3 bits called validity, user, and channel status. The preamble contains biphase coding violations and identifies the start of a subframe. The audio sample word length can vary up to 24 bits. If the word length is greater than 20 bits, the sample occupies both the audio and auxiliary data fields. If it is 20 bits or less, the auxiliary field can be used for other applications such as a voice channel. The parity bit generates even parity and can be used to detect an odd number of transmission errors. If an even number of bit errors occurred, the received parity will remain even and the errors will not be identi-

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fied. The validity bit indicates if the audio sample is secure and error free. In some applications it identifies samples that have been interpolated due to errors. The user and channel status bits are sent once per sample and when accumulated over a number of samples can be used to transmit blocks of data. The user bit channel is undefined and is available to the user for any purpose. The channel status channel is defined and conveys important information about the audio data and transmission link. Each of the two audio channels has its own channel status channel with a block structure that repeats every 192 samples.

As shown in Figure 2, two subframes, one each from channels 1 and 2, create a frame and 192 frames generate a block. The preambles that identify the start of a subframe are unique for each channel with another third pattern identifying the beginning of channel status block. The 192 channel status bits in a block can be arranged as 24 bytes and are defined according to the AES-EBU standard as shown in Figure 3. Bytes 0 to 3 contain specific bits of information about the data and the link, bytes 4 and 5 are presently undefined, bytes 6 to 13 can be used for networking, bytes 14 to 17 function as a recording index counter by counting the number of transmitted blocks, bytes 18 to 21 record the time the signal was source encoded, byte 22 identifies which bytes of the block are valid, and byte 23 is a cyclic redundancy check character generated from the previous 23 channel status bytes (provides some error detection).

The primary difference between the AES-EBU interface and the consumer interface is the definition of the channel status bits. The definition for the consumer interface is illustrated in Figure 4. Bytes 0 to 3 contain specific bits of information about the data and the link, and bytes 4 to 23 can be used for music program production. More information on these bytes is available in the EIAJ CP-340 document [4].

The channel coding used in the AES-EBU and the consumer interface is biphase mark. As shown in the example given in Figure 5, this means there is a transition at every data cell boundary and another transition in the middle of the data cell when transmitting a one. There is no transition in the middle of a data cell when transmitting a zero. Recovering a clock from data encoded this way is simpler than other coding schemes due to the frequent transitions. Biphase coding also has no dc content, which allows ac coupling, and is immune to polarity inversions. Synchronization is achieved by producing biphase coding violations in the preambles. A violation occurs when there is no transition at a data cell boundary and the patterns used to identify subframe, frame, and block boundaries are shown in Figure 6.

The electrical specifications of the AES-EBU interface require encoded data to be transmitted as a differential signal on a shielded twisted pair cable. The signal voltage can be 3 to 10 volts peak to peak when measured across a 110 ohm resistor. The consumer interface allows electrical or optical communication. As an electrical link, data is transmitted as a single ended signal on a coaxial cable with a signal amplitude of .5 volts +/- 20%, when measured across a 75 ohm load.

2 THE AES-EBU CHIP FAMILY

Our AES-EBU IC'S are general purpose, support both the AES-EBU and consumer interfaces, and consist of two transmitters and two receivers. Having the line drivers on the transmitters and the line receivers and clock recovery circuits on the receivers, they provide a complete transmission link with minimal external components. Providing control of and access to all the user and channel status bits, these devices will remain compatible with the specifications as the standard matures. The two transmitter and receiver versions are appropriate for different applications. Both versions have serial ports for audio data. The first version, which consists of the CS8401 transmitter and the CS8411 receiver, has a buffer memory with a parallel port for storing control information and most of the non-audio subframe data, and should be driven by a processor. The second version, which consists of the CS8402 transmitter and the CS8412 receiver, will operate without a processor. This version is controlled by dedicated pins, and can accept and provide the non-audio data on a sample basis through serial input and output pins. Both transmitters, whose pinouts are shown in Figures 13 and 14, are available in 24 pin DIP's and SOIC's. The receivers will be available in similar 28 pin packages. Figure 7 illustrates the basic differences between the two transmitters.

Both transmitters, having RS422 differential line drivers, are compatible with the AES-EBU interface. To make these parts compatible with the consumer interface for an electrical link, the non-inverting driver output can be attenuated by an external resistive divider. This will provide the necessary single ended signal with the appropriate amplitude.

3 THE CS8401 TRANSMITTER

As shown in Figure 8, the CS8401 has control registers, a status register, and a 28 byte buffer memory, which are all accessible through an 8 bit parallel port. The buffer memory holds channel status, user, and auxiliary data, and can be monitored by the status register and the interrupt pin. The device supports both the AES-EBU and the consumer interfaces by setting the channel status buffer according to the appropriate standard. When complying with the AES-EBU specification, the CS8401 can automatically generate the local sample address, the reliability flag, and the CRC character. The parity bit is always generated and audio data is entered through a serial port configured by a control register.

The buffer memory can operate in three modes. The address maps for these modes are shown in Figure 9 and are selectable by a control register. In all modes, 4 bytes of user data are buffered. This data is read cyclicly and shifted out one bit per audio sample, allowing user data to be different in channels 1 and 2. Consequently, this buffer must be reloaded every 32 samples. In buffer mode 0, in addition to the user data buffer, one entire block of channel status data is buffered. This block will be transmitted in both channel 1 and channel 2. Since an entire block is stored, only the data that changes from one block to the next needs to be updated.

In buffer mode 1, eight bytes are allocated for channel status data and 16 bytes for auxiliary data. The channel status buffer is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are read once per channel status block. The second four locations provide a cyclic buffer for the last 20 bytes of channel status data. Similar to mode 0, transmitted channel status data will be the same for channel 1 and channel 2. The

auxiliary data buffer is read in a cyclic manner similar to the user data buffer; however, four auxiliary data bits are transmitted per audio sample. Since the auxiliary buffer must be read four times as often as the user data buffer and is four times as large, they both need to be updated at the same rate.

In buffer mode 2, two 8-byte buffers are available for buffering both channel 1 and channel 2 channel status data independently. Both buffers are identical to the channel status buffer in mode 1, except that each channel can have unique channel status data. All modes use the status register and the interrupt pin to monitor the buffers. They can identify when the buffers are half full and empty.

When operating a digital audio interface according to the AES-EBU standard, the CS8401 can automatically generate channel status bytes 14 to 17, the local sample address, byte 22, the reliability flag, and byte 23, the CRC character, by setting the appropriate bits in a control register. The local sample address can be generated by a 32 bit counter incremented at every block boundary, the reliability flag can be transmitted with bits 5 and 7 set indicating that bytes 6 to 13 and bytes 18 to 21 are unreliable, and the CRC character can be generated independently for channel 1 and channel 2.

The serial port is used to enter audio data and consists of three pins: SCK, SDATA, and FSYNC. The serial port is double buffered with SCK clocking in data from SDATA, and FSYNC delineating audio samples and may define the particular channel, 1 or 2. A large number of input formats is supported to provide zero glue-logic interfaces to many DSP's, encoder chips, and standard audio interfaces. This port is configured by 7 bits in a control register allowing SCK and FSYNC to inputs or outputs, and allowing SDATA to sampled on the rising or falling edge of SCK and be entered MSB first, MSB last, or LSB last. In most modes audio data of 16 to 24 bits may be accepted.

4 THE CS8402 TRANSMITTER

The CS8402, since it is controlled by dedicated pins, can operate without the assistance of a microprocessor or DSP. The device accepts audio samples, through a serial port similar to the CS8401, in a limited number of formats. Several pins are dedicated to the most critical channel status bits, and all channel status, user, and validity bits can be serially input through serial port pins. The parity bit is always generated, and data is biphase mark encoded and driven through an RS422 line driver. The CS8402 can operate as an AES-EBU or consumer interface transmitter. As an AES-EBU interface device, the dedicated channel status input pins are defined according to that standard, the CRC characters are generated, and the local sample address and the reliability flag can be generated. As a consumer device, the dedicated channel status input pins are defined according to the consumer standard. When transmitting data from a compact disk, a CD subcode port can accept CD subcode data, extract channel status information from it, and transmit it as user data. Figures 10, 11, and 12 are block diagrams of Professional (AES-EBU) Mode, Consumer Mode, and CD Mode, respectively.

The audio serial port, consisting of SCK, SDATA, and FSYNC, is configured by three format control pins, and is double buffered. Like the CS8401, SCK clocks in SDATA while FSYNC delineates audio samples and may indicate the particular channel, 1 or 2. The format control pins select one of seven different formats for the serial port, which allow zero glue-logic interfaces to many data converters, DSP's, and standard audio interfaces.

Channel status, user, and validity bits can be entered through three serial port pins, which are sampled by FSYNC on a per sample basis. Any channel status data entered serially is logically OR'ed with data entered though the dedicated pins or internally generated.

Although channel status can always be entered serially, Professional, Consumer, and CD Modes offer different ways in which it can be generated. In Professional Mode, audio/non-audio mode, emphasis, sampling frequency, and some channel modes can be controlled by dedicated pins, CRC characters are inserted independently for both channels, and the local sample address and reliability flag byte can be generated. As in the CS8401, when this option is enabled, bits 5 and 7 of the reliability flag are set. In Consumer Mode and CD Mode, the copy bit, emphasis, some category codes, the generation status, and the sampling frequency can be controlled by dedicated pins. In CD Mode only, the copy bit, emphasis, and the 2 channel/4 channel bit are extracted from the CD subcode entered as user data.

5 THE CS8411 AND CS8412 RECEIVERS

The CS8411 and CS8412 are receivers being developed to complement the CS8401 and CS8402, respectively. The CS8411 has a buffer memory and parallel port for control by a processor. The CS8412 is controlled by dedicated pins and operates as a stand alone device. Both parts will require only external capacitors for the clock recovery, and will be able to lock to audio sample rates of 25kHz to 55kHz. They will have schmitt trigger line receivers and will detect and report various errors conditions and information about the link, such as recovered clock frequency.

6 SUMMARY

To eliminate some of the practical problems of implementing an AES-EBU digital audio interface, Crystal Semiconductor has defined integrated circuits which will permit economical and timely designs. Each version, consisting of a transmitter chip and a receiver chip, is targeted for a different application. The first version, with a parallel port and internal buffer memory, is aimed at systems requiring control of many aspects of the interface. The second version, while still able to implement the entire interface, is more suitable for systems requiring minimal control. Presently, the transmitters are available and the receivers are defined and being developed.

7 ACKNOWLEDGMENT

The author would like to thank Clif Sanchez and the rest of the applications department at Crystal Semiconductor for their help in defining these products and preparing this document. Mike Callahan and Jeff Scott, also of Crystal, provided valuable assistance in circuit design.

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[2] Audio Engineering Society,Inc(author),"AES Recommended Practice for Digital Audio Engineering - Serial Transmission Format for Linearly Represented Digital Audio Data,"AES3-1985(ANSI S4.40-1985)

[3] EIA Standard RS422A,"Electrical Characteristics of Balanced Voltage Digital Interface Circuits,"Electronic Industries Assoc.,Washington,DC,1978 Dec.

[4] Electronic Industries Assoc. of Japan(author),"Digital Audio Interface," CP-340,September,1987

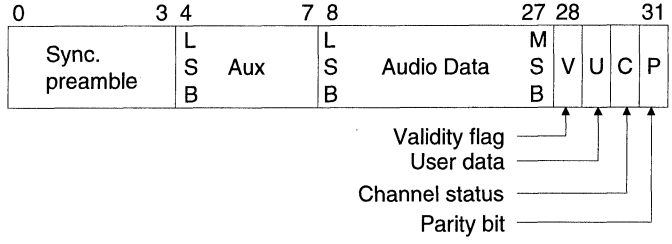


Figure 1. Subframe Format

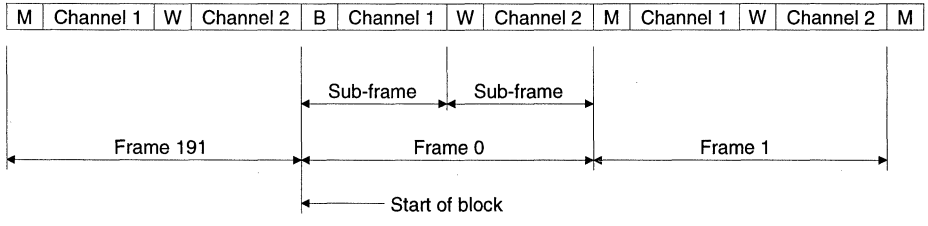
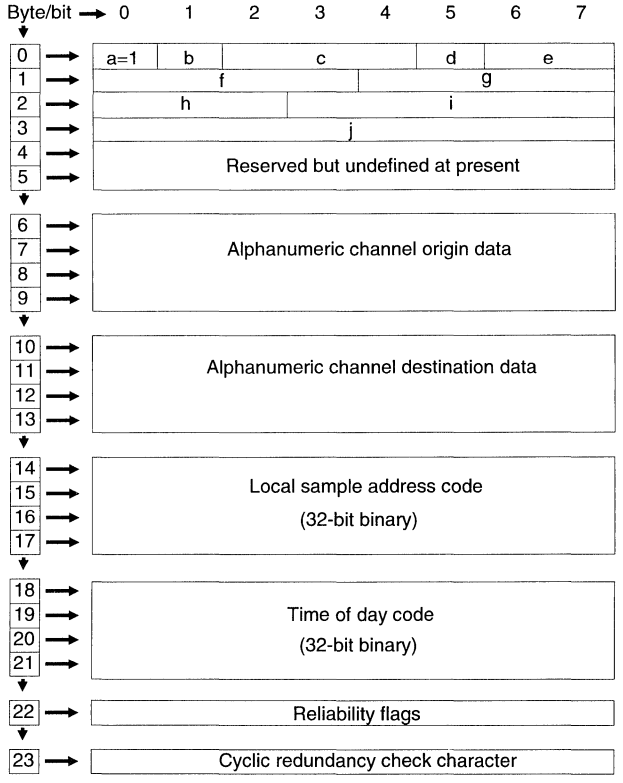
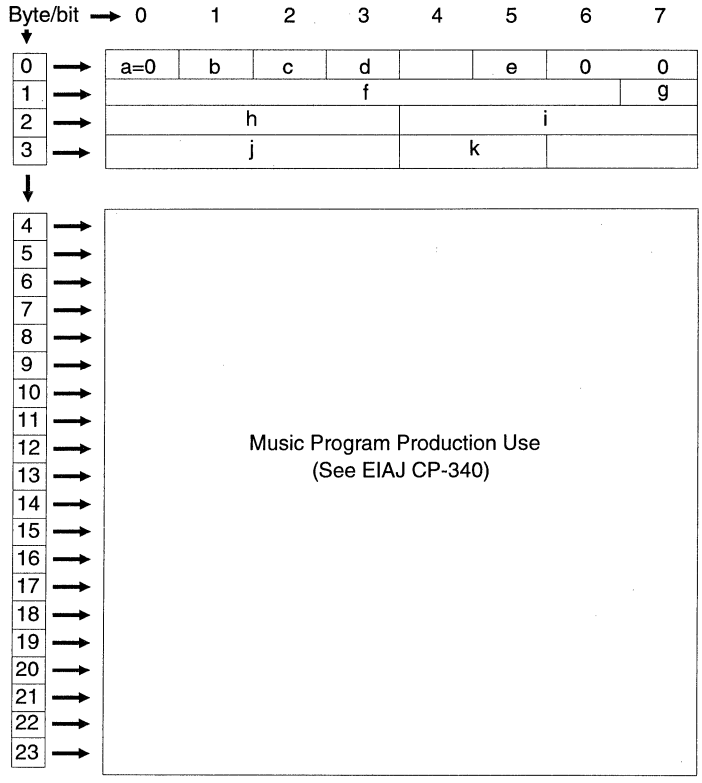


Figure 2. Frame Format



a: Use of channel status block.
b: Audio/Non-audio mode.
c: Audio signal emphasis.
d: Locking of source sampling frequency.
e: Sampling frequency.
f: Channel mode.
g: User bits management.
h: Use of auxiliary sample bits.
i: Source word length and source encoding history.
j: Future multichannel function description.

Figure 3. AES-EBU Channel Status Data Format



a: Use of channel status block
b: Audio/Non-audio mode
c: Copy permitted
d: Pre-emphasis
e: 2 Channel/ 4 Channel
f: Category code
g: Generation status
h: Source number
i: Channel number
j: Sampling frequency
k: Clock accuracy

Figure 4. Consumer Channel Status Data Format

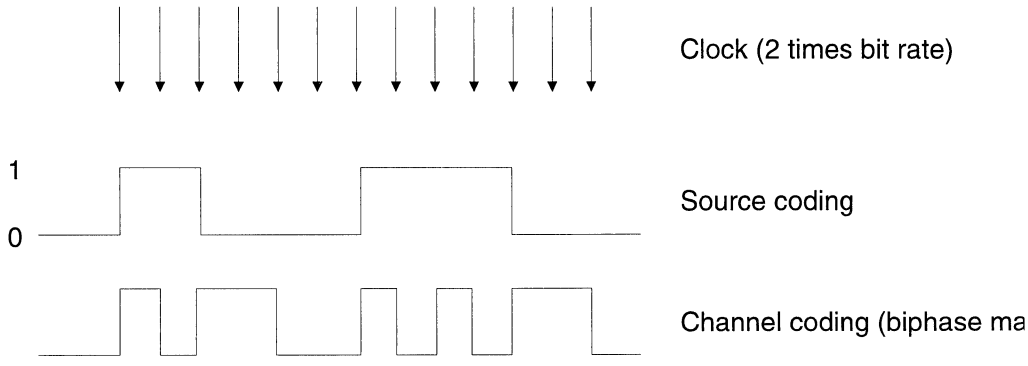


Figure 5. Channel Coding

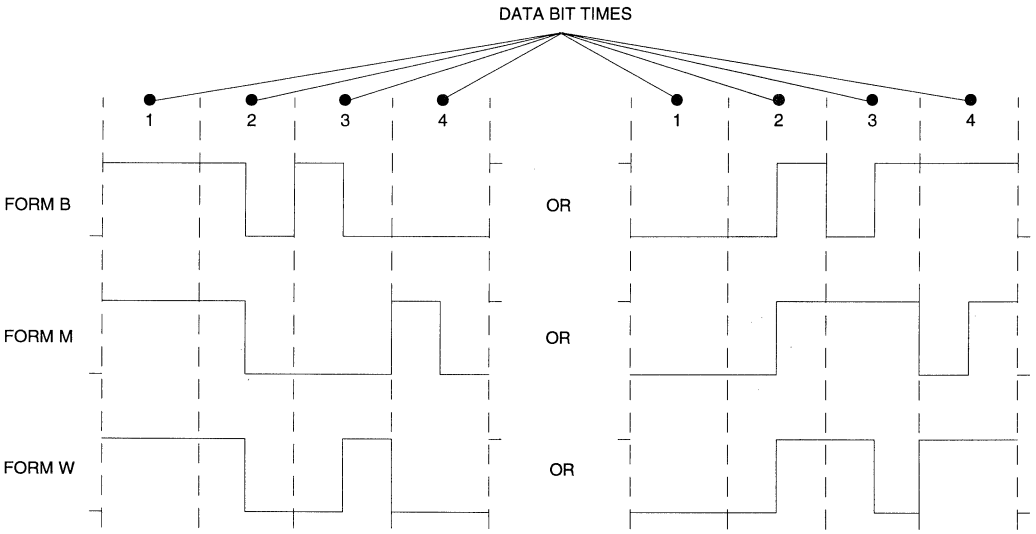


Figure 6. Preamble forms. Three types sample preamble used are B) channel 1, subframe, and block synchronizing; M) channel 1, otherwise; W) channel 2.

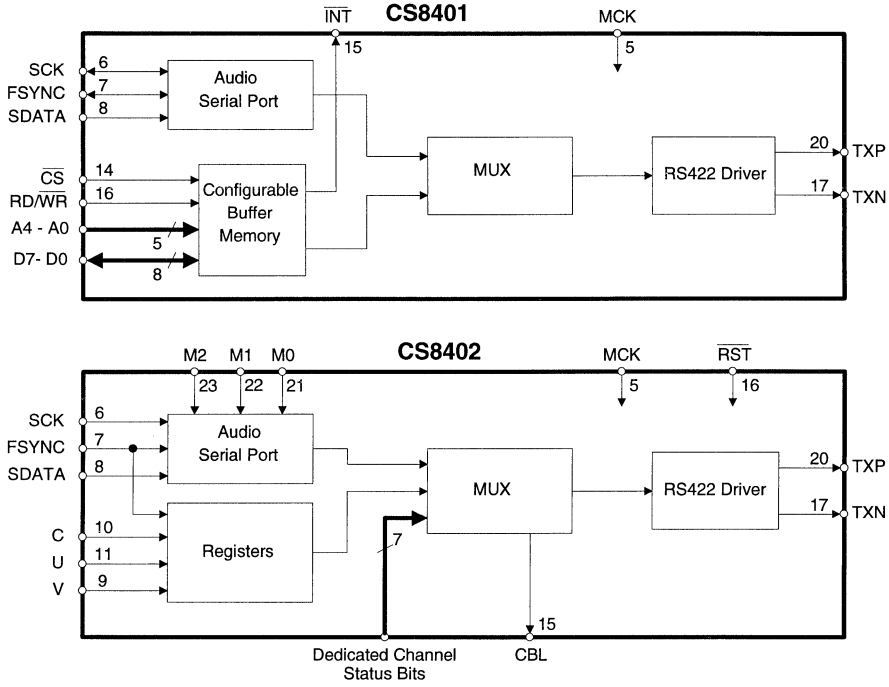


Figure 7. General Description

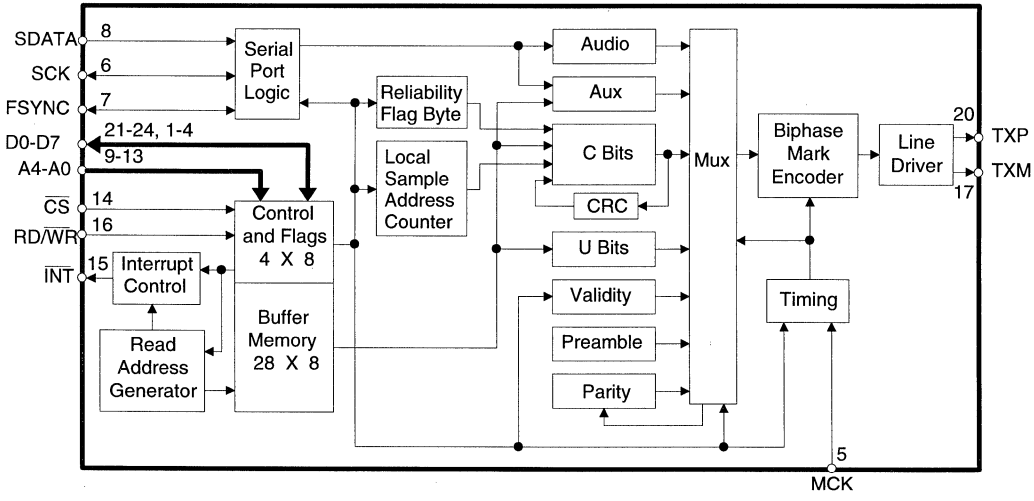


Figure 8. CS8401 Block Diagram

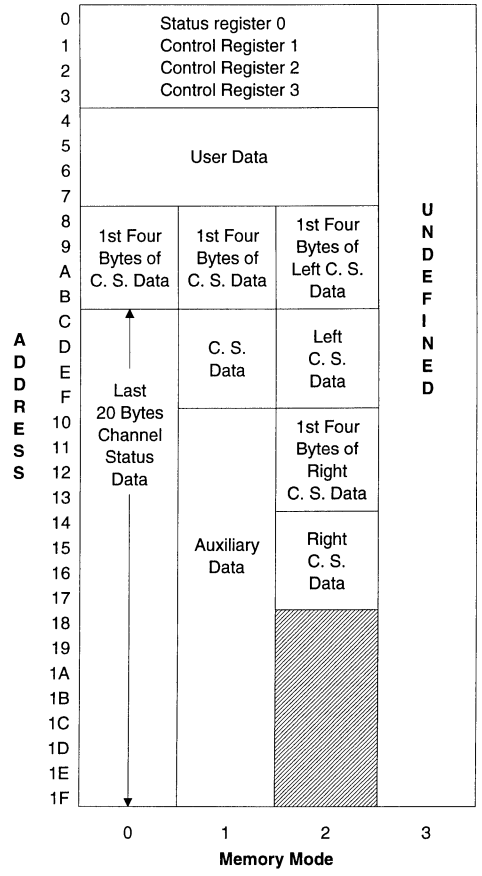


Figure 9. CS8401 Buffer Memory Modes

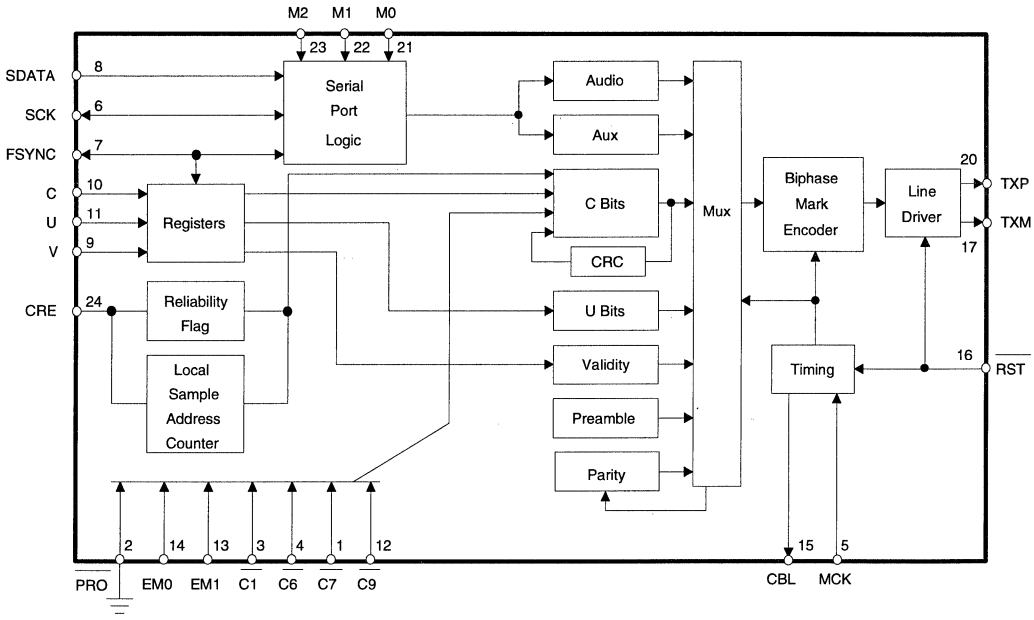


Figure 10. CS8402 Block Diagram-Professional Mode

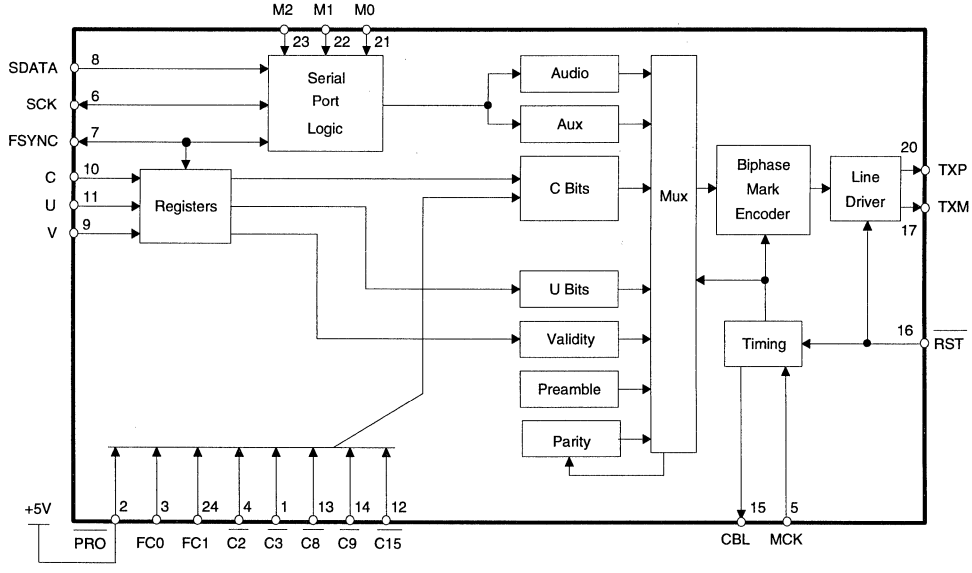


Figure 11. CS8402 Block Diagram-Consumer Mode

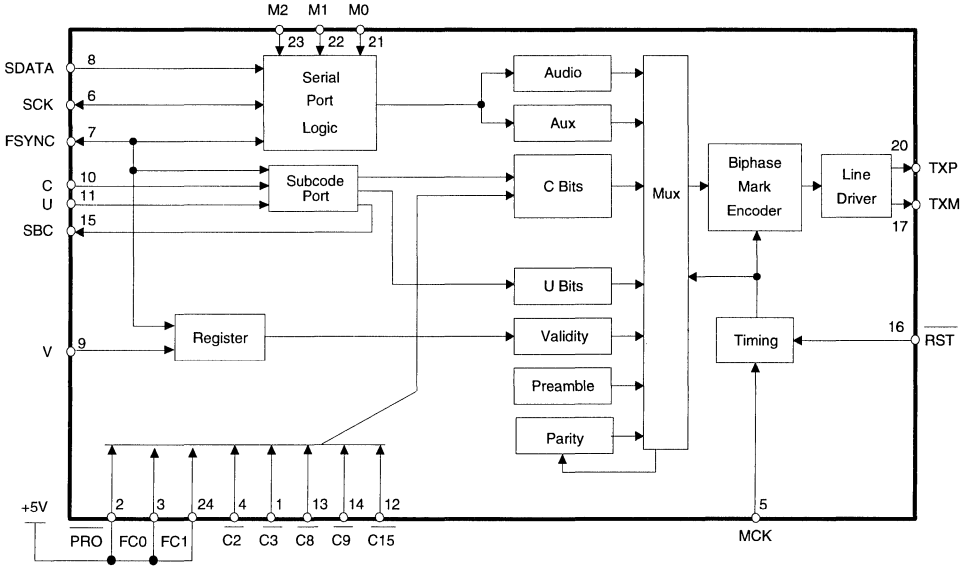


Figure 12. CS8402 Block Diagram-Consumer Mode, CD Submode

DATA BUS BIT 4	**D4**	1	24	**D3**	DATA BUS BIT 3
DATA BUS BIT 5	**D5**	2	23	**D2**	DATA BUS BIT 2
DATA BUS BIT 6	**D6**	3	22	**D1**	DATA BUS BIT 1
DATA BUS BIT 7	**D7**	4	21	**D0**	DATA BUS BIT 0
MASTER CLOCK	**MCK**	5	20	**TXP**	TRANSMIT POSITIVE
SERIAL DATA CLOCK	**SCK**	6	19	**VD+**	POWER
FRAME SYNC	**FSYNC**	7	18	**GND**	GROUND
SERIAL INPUT DATA	**SDATA**	8	17	**TXN**	TRANSMIT NEGATIVE
ADDRESS BUS BIT 4	**A4**	9	16	**RD/WR**	READ/WRITE SELECT
ADDRESS BUS BIT 3	**A3**	10	15	**INT**	INTERRUPT
ADDRESS BUS BIT 2	**A2**	11	14	**CS**	CHIP SELECT
ADDRESS BUS BIT 1	**A1**	12	13	**A0**	ADDRESS BUS BIT 0

Figure 13. CS8401 Pinout

CS BIT 7 / CS BIT 3	**C7/C3**	1	24	**TST/FC1**	SAMPLE ADDR. / FREQ. CTRL 1
PROFESSIONAL MODE	**PRO**	2	23	**M2**	SERIAL PORT MODE SELECT 2
CS BIT 1 / FREQ. CTRL. 0	**C1/FC0**	3	22	**M1**	SERIAL PORT MODE SELECT 1
CS BIT 6 / CS BIT 2	**C6/C2**	4	21	**M0**	SERIAL PORT MODE SELECT 0
MASTER CLOCK	**MCK**	5	20	**TXP**	TRANSMIT POSITIVE
SERIAL DATA CLOCK	**SCK**	6	19	**VD+**	POWER
FRAME SYNC	**FSYNC**	7	18	**GND**	GROUND
SERIAL INPUT DATA	**SDATA**	8	17	**TXN**	TRANSMIT NEGATIVE
VALIDITY INPUT	**V**	9	16	**RST**	MASTER RESET
CS SERIAL IN / SC FRAME CLOCK	**C/SBF**	10	15	**CBL/SBC**	CS BLOCK OUT / SC BIT CLOCK
USER DATA INPUT	**U**	11	14	**EM0/C9**	EMPHASIS 0 / CS BIT 9
CS BIT 9 / CS BIT 15	**C9/C15**	12	13	**EM1/C8**	EMPHASIS 1 / CS BIT 8

Figure 14. CS8402 Pinout

•Notes•

Semiconductor Corporation

Application Note

Overview of Digital Audio Interface Data Structures

Clif Sanchez & Roger Taylor

The following information is provided for convenience, but by no means constitutes the entire specification. Also included is information from the IEC 958 and the new AES3-199x and TC84 documents. The AES3-199x and TC84 documents have not received approval as of the printing of this data sheet. To guarantee conformance, a copy of the actual specification should be obtained from the Audio Engineering Society or ANSI (ANSI S4.40-1985) for the AES3 document, and the International Electrotechnical Commission for the IEC 958 document.

The AES/EBU interface is a means for serially communicating digital audio data through a single transmission line. It provides two channels for audio data, a method for communicating control information, and some error detection capabilities. The control information is transmitted as one bit per sample and accumulates in a block structure. The data is biphase encoded, which enables the receiver to extract a clock from the data. Coding violations, defined as preambles, are used to identify sample and block boundaries.

Frames Sub-frames and Blocks

An audio sample is placed in a structure known as a sub-frame. The sub-frame, shown in Figure 1, consists of 4 bits of preamble, 4 bits of auxiliary data, 20 bits of audio data, 3 bits called validity, user, and channel status, and a parity bit. The preamble contains biphase coding violations and identifies the start of a sub-frame. The audio sample word length can vary up to 24 bits and is transmitted LSB first. If the word length is greater than 20 bits, the sample occupies both the audio

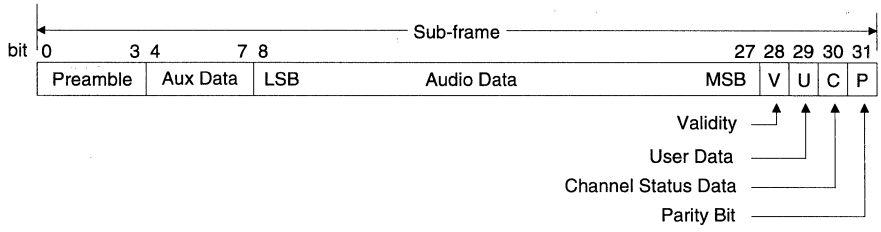


Figure 1. Sub-frame Format

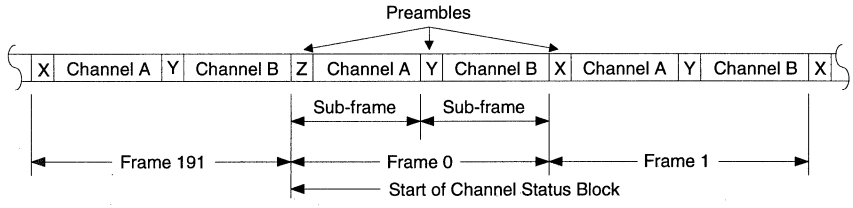


Figure 2. Frame/Block Format

and auxiliary data fields. If it is 20 bits or less, the auxiliary field can be used for other applications such as voice. The parity bit generates even parity and can detect an odd number of transmission errors in the sub-frame. The validity bit, when low, indicates the audio sample is fit for conversion to analog. The user and channel status bits are sent once per sample and, when accumulated over a number of samples, define a block of data. The user bit channel is undefined and available to the user for any purpose. The channel status bit conveys, over an entire block, important information about the audio data and transmission link. Each of the two audio channels has its own channel status data with a block structure that repeats every 192 samples.

As shown in Figure 2, two consecutive sub-frames are defined as a frame, containing channels A and B, and 192 frames define a block. The preambles that identify the start of a sub-frame are different for each of the two channels with another unique one identifying the beginning of a channel status block.

Modulation and Preambles

The data is transmitted with biphase-mark encoding to minimize the DC component and to allow clock recovery from the data. As illustrated in Figure 3, the 1's in the data have transitions in the center, and the 0's do not, after biphase-mark encoding. Also, the biphase-mark data switches polarity at every data bit boundary. Since the value of the data bit is determined by whether their is a transition in the center of the bit, the actual polarity of the signal is irrelevant.

Each sub-frame starts with a preamble. This allows a receiver to lock on to the data within one sub-frame. There are three defined preambles:

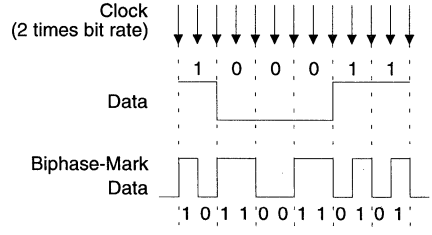


Figure 3. Biphase-Mark Encoding

	Biphase Patterns	Channel
X	11100010 or 00011101	Ch. A
Y	11100100 or 00011011	Ch. B
Z	11101000 or 00010111	Ch. A & C.S. Block Start

Table 1. Preambles

one for each channel and one to indicate the beginning of a channel status block (which is also channel A). To distinguish the preambles from arbitrary data patterns, the preambles contain two biphase-mark violations. Biphase-mark data is required to transition at every bit period, but each preamble violates that requirement twice. In Figure 3 each bit boundary, indicated by the dashed lines, contains a transition in the biphase

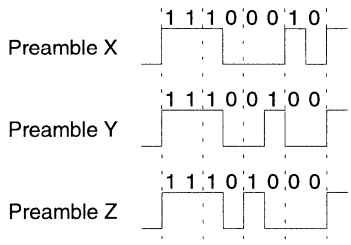


Figure 4. Preamble Forms

data. Each preamble shown in Figure 4 has two bit boundaries with no transition, which enables the receiver to recognize the data as a preamble. Table 1 lists the preamble biphase-mark data pat-

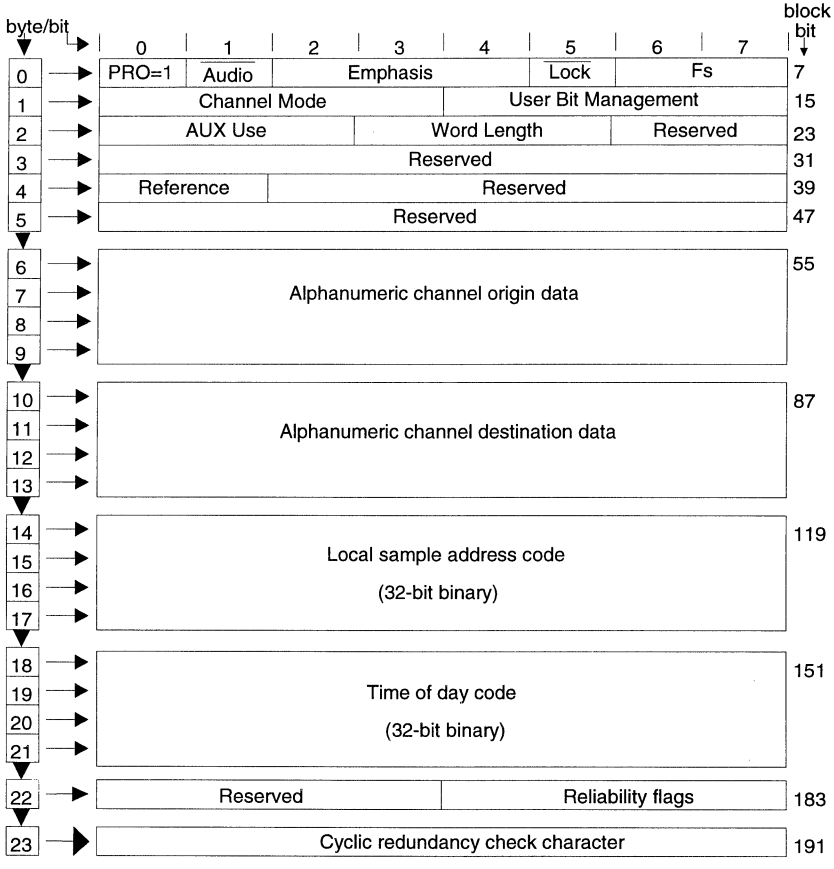


Figure 5. Professional Channel Status Block Structure

terns and what each designates. Since biphase-mark encoding is not polarity conscious, both phases are shown in the table. Preambles "X" and "Y" indicate a sub-frame containing channels A and B respectively. Preamble "Z" replaces preamble "X" once every 192 frames to indicate the start of a channel status block.

There are two channel status blocks, one for channel A and one for channel B. Since there are 192 frames in a block, each channel has a channel status block 192 bits long. These 192 channel status bits in a block can be arranged as 24 bytes. The blocks have one of two formats, professional or consumer. The first bit of the channel status block defines the format with 0 indicating consumer and 1 indicating professional.

Channel Status Block - Professional Format

Setting the first bit of channel status high designates the professional or broadcast format. The channel status block structure for the professional format is illustrated in Figure 5 and shows bit 0 of byte 0, PRO, to contain a one. Tables 2 and 3 list the bits in each byte and their meaning. The areas designated "reserved" in the figures and tables, are currently not specified and must be set to 0 when transmitting. Most of the professional format data was obtained from the AES3-1985 document, and information from AES3-199x. Since the AES specification is currently being updated, the accuracy of this data is not guaranteed.

BYTE 0	
bit 0	PRO = 1
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	$\overline{\text{Audio}}$
0	Normal Audio
1	Non-Audio
bits 2 3 4	Encoded audio signal emphasis
0 0 0	Emphasis not indicated. Receiver defaults to no emphasis with manual override enabled
1 0 0	None. Rec. manual override disabled
1 1 0	50/15 µS. Rec. manual override disabled
1 1 1	CCITT J.17 . Rec. man. override disabled
X X X	All other states of bits 2-4 are reserved
bit 5	$\overline{\text{Lock}}$: Source Sample Frequency
0	Locked - default
1	Unlocked
bits 6 7	Fs: Sample Frequency
0 0	Not indicated. Receiver default to 48 kHz and manual override or auto set enabled
0 1	48 kHz. Man. override or auto disabled
1 0	44.1 kHz. Man. override or auto disabled
1 1	32 kHz. Man. override or auto disabled

BYTE 1	
bits 0 1 2 3	Channel Mode
0 0 0 0	Mode not indicated. Receiver default to 2-channel mode. Manual override enabled
0 0 0 1	Two-channels. Man. override disabled
0 0 1 0	Single channel. Man. override disabled
0 0 1 1	Primary/Secondary (Ch. A is primary). Manual override disabled
0 1 0 0	Stereophonic. (Ch. A is left) Manual override disabled.
0 1 0 1	Reserved for user defined applications
0 1 1 0	Reserved for user defined applications
1 1 1 1	Vector to byte 3. Reserved
X X X X	All other states of bits 0-3 are reserved.
bits 4 5 6 7	User bits management
0 0 0 0	Default, no user info indicated
0 0 0 1	192 bit block structure Preamble 'Z' starts block
0 0 1 0	Reserved
0 0 1 1	User defined application
X X X X	All other states of bits 4-7 are reserved.

Table 2. Professional Channel Status bytes 0-1

BYTE 2		
bits 0 1 2	AUX: Use of auxiliary sample bits	
0 0 0	Not defined. Maximum audio word length is 20 bits	
0 0 1	Used for main audio. Maximum audio word length is 24 bits	
0 1 0	Single coordination signal. Max. audio word length is 20 bits	
0 1 1	User defined application	
X X X	All other states of bits 0-2 are reserved	
bits 3 4 5	Source word length Max. audio based on bits 0-2 above	
	Max audio 24 bits	Max audio 20 bits
0 0 0	Not Indicated	Not Indicated (default)
0 0 1	23 bits	19 bits
0 1 0	22 bits	18 bits
0 1 1	21 bits	17 bits
1 0 0	20 bits	16 bits
1 0 1	24 bits	20 bits
X X X	All other states of bits 3-5 are reserved	
bits 6 7		
X X	Reserved	

BYTE 3	
bits 0-7	Vectored target byte
XXXXXXX	Reserved

BYTE 4	
bits 0 1	Digital audio reference signal per AES11-1990
0 0	Not reference signal (default)
0 1	Grade 1 reference signal
1 0	Grade 2 reference signal
1 1	Reserved
bits 2-7	
XXXXXX	Reserved

BYTE 5	
bits 0-7	
XXXXXXX	Reserved

BYTES 6 - 9
Alphanumeric channel origin data
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 6. LSB's are transmitted first.

BYTES 10 - 13
Alphanumeric channel destination data
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 10. LSB's are transmitted first.

BYTES 14 - 17
Local sample address code (32-bit binary)
Value is of first sample of current block. LSBs are transmitted first.

BYTES 18 - 21
Time-of-day sample address code (32-bit binary)
Value is of first sample of current block. LSBs are transmitted first.

BYTE 22	
bits 0 1 2 3	
X X X X	Reserved
bit 4	Channel status bytes 0 to 5
0	Reliable
1	Unreliable
bit 5	Channel status bytes 6 to 13
0	Reliable
1	Unreliable
bit 6	Channel status bytes 14 to 17
0	Reliable
1	Unreliable
bit 7	Channel status bytes 18 to 21
0	Reliable
1	Unreliable

BYTE 23
CRCC: Cyclic redundancy check character
CRCC for channel status data block that uses bytes 0 to 22 inclusive. Generating polynomial is $G(x) = X^8 + X^4 + X^3 + X^2 + 1$ with an initial state of all ones.

Table 3. Professional Channel Status Bytes 2-23

Channel Status Block - Consumer Format

Setting the first bit of channel status low designates the consumer format. The channel status block structure for the consumer format is illustrated in Figure 6 with the bit descriptions in Tables 4 and 5. All areas listed as "reserved" must be transmitted as a 0. The data for this format was obtained from the EIAJ CP-340 and the IEC 958 with some information from TC84 which is a proposed amendment to IEC 958 and has not received approval yet. As with the professional format, since this format is currently changing, the accuracy of the data listed cannot be guaranteed.

In the consumer format, bit 0 must be 0. If bit 1 is set to 1 defining the data as non-audio, then bits 3-5 are redefined (see Table 4, byte 0). Bits 6 and 7 of byte 0 define the mode, and only one mode is presently defined, mode = 00. This mode defines the next three bytes as listed in Figure 6. Most of byte 1 defines the category code. The first 3 to 5 bits define the general category. Under the laser-optical category is compact disk (cat. code 1000000). This format defines some of the U channel bits and the CD subcode port. More information can be obtained from the CP-340 or IEC 958 documents.

Currently the standards committees are trying to define a minimum implementation as well as levels of implementation of channel status data.

A scheme for providing copy protection is also currently being developed. It includes knowing

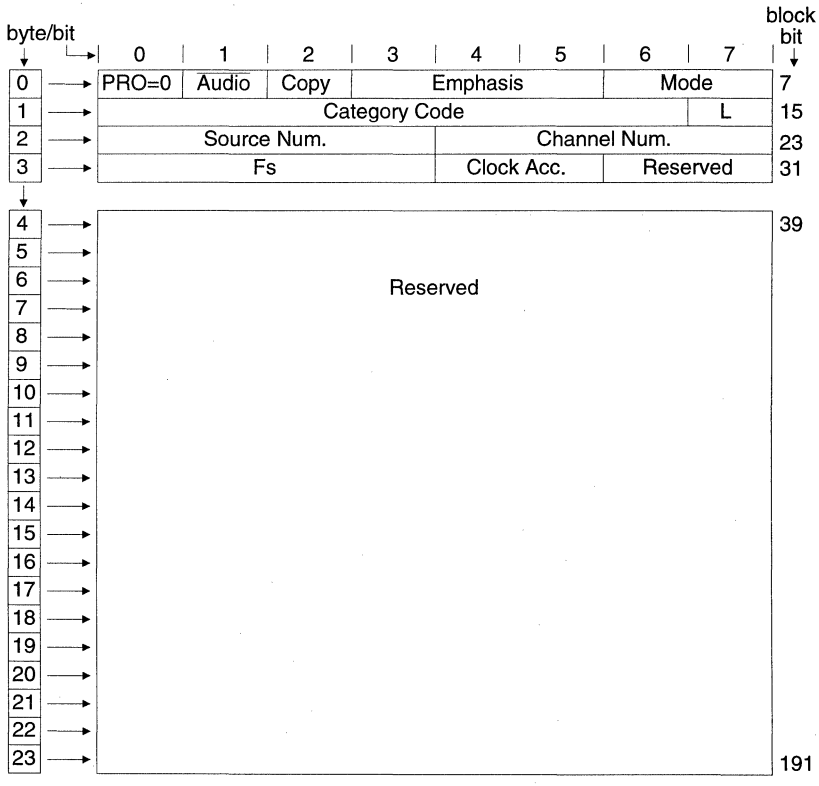


Figure 6. Consumer Channel Status Block Structure

BYTE 0	
bit 0	PRO = 0 (consumer)
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	$\overline{\text{Audio}}$
0	Digital Audio
1	Non-audio
bit 2	Copy / Copyright
0	Copy inhibited / copyright asserted
1	Copy permitted / copyright not asserted
bits 3 4 5	Pre-emphasis - if bit 1 is 0 (dig. audio)
0 0 0	None - 2 channel audio
1 0 0	50/15 µs - 2 channel audio
0 1 0	Reserved - 2 channel audio
1 1 0	Reserved - 2 channel audio
X X 1	Reserved - 4 channel audio
bits 3 4 5	if bit 1 is 1 (non-audio)
0 0 0	Digital data
X X X	All other states of bits 3-5 are reserved
bits 6 7	Mode
0 0	Mode 0 (defines bytes 1-3)
X X	All other states of bits 6-7 are reserved

BYTE 1 - Category Code 001	
bits 3 4 5 6	Broadcast reception of digital audio
* 0 0 0 0	Japan
* 0 0 1 1	United States
* 1 0 0 0	Europe
* 0 0 0 1	Electronic software delivery
X X X X	All other states are reserved

BYTE 1 - Category Code 100	
bits 3 4 5 6	Laser Optical
0 0 0 0	CD - compatible with IEC-908
* 1 0 0 0	CD - not comp. with IEC-908 (magneto-optical)
X X X X	All other states are reserved

BYTE 1		
bits 0 1 2 3	4 5 6	Category Code
0 0 0 0	0 0 0	General
*	0 0 1	Experimental
	X X X	Reserved
* 0 0 0 1	X X X	Solid state memory
* 0 0 1 X	X X X	Broadcast recep. of digital audio
0 1 0 X	X X X	Digital/digital converters
* 0 1 1 0	0 X X	A/D converters w/o copyright
*	1 X X	A/D converters w/ copyright (using Copy and L bits)
* 0 1 1 1	X X X	Broadcast recep. of digital audio
1 0 0 X	X X X	Laser-optical
* 1 0 1 X	X X X	Musical Instruments, mics, etc.
1 1 0 X	X X X	Magnetic tape or disk
1 1 1 X	X X X	Reserved
bit 7		L: Generation Status.
		Only category codes: 001XXXX, 0111XXX, 100XXXX
* 0		Original/Commercially pre-recorded data
* 1		No indication or 1st generation or higher
		All other category codes
* 0		No indication or 1st generation or higher
* 1		Original/Commercially pre-recorded data
The subgroups under the category code groups listed above are described in tables below. Those not listed are reserved.		
The Copy and L bits form a copy protection scheme for original works. Further explanations can be found in the proposed amendment (TC84) to IEC-958.		

BYTE 1 - Category Code 010	
bits 3 4 5 6	Digital/digital conv. & signal processing
0 0 0 0	PCM encoder/decoder
* 0 0 1 0	Digital sound sampler
* 0 1 0 0	Digital signal mixer
* 1 1 0 0	Sample-rate converter
X X X X	All other states are reserved

Table 4. Consumer Channel Status Bytes 0 and 1

BYTE 1 - Category Code 101					
bits	3	4	5	6	Musical Instruments, mics, etc.
*	0	0	0	0	Synthesizer
*	1	0	0	0	Microphone
	X	X	X	X	All other states are reserved

BYTE 1 - Category Code 110					
bits	3	4	5	6	Magnetic tape or disk
	0	0	0	0	DAT
*	1	0	0	0	Digital audio sound VCR
	X	X	X	X	All other states are reserved

BYTE 2					
bit	0	1	2	3	Source Number
	0	0	0	0	Unspecified
	1	0	0	0	1
	0	1	0	0	2
	1	1	0	0	3
	0	0	1	0	4 to
	0	1	1	1	14 (binary - 0 is LSB, 3 is MSB)
	1	1	1	1	15
bit	4	5	6	7	Channel Number
	0	0	0	0	Unspecified
	1	0	0	0	A (Left in 2 channel format)
	0	1	0	0	B (Right in 2 channel format)
	1	1	0	0	C to
	0	1	1	1	N (binary - 4 is LSB, 7 is MSB)
	1	1	1	1	O

BYTE 3					
bits	0	1	2	3	Fs: Sample Frequency
	0	0	0	0	44.1 kHz
	0	1	0	0	48 kHz
	1	1	0	0	32 kHz
	X	X	X	X	All other states of bits 0-3 are reserved
bits	4	5			Clock Accuracy
	0	0			Level II, ±1000 ppm (default)
	0	1			Level III, variable pitch
	1	0			Level I, ±50 ppm - high accuracy
	1	1			Reserved
bits	6	7			
	X	X			Reserved

BYTES 4 - 23
Reserved

* - Data from draft of IEC 958 proposed amendment (from TC84). Has not received approval yet.

Table 5. Consumer Channel Status Bytes 1-23

the category code and then utilizing the Copy and L bits to determine if a copy should be allowed. Digital processing of data should pass through the copy and L bits as defined by their particular category code. If mixing inputs, the highest level of protection of any one of the sources should be passed through. If the copy bit indicates no copy protection (copy = 1), then multiple copies can be made. If recording audio data to tape or disk, and any source has copy protection asserted, then the L bit must be used to determine whether the data can be recorded.

The L bit determines whether the source is an original (or prerecorded) work, or is a copy of an original work (first generation or higher). The actual meaning of the L bit can only be determined by looking at the category code since certain category codes reverse the meaning.

If the category code is CD (1000000) and the copy bit alternates at a 4 to 10 Hz rate, the CD is a copy of an original work that has copy protection asserted and no recording is permitted.

An 18-Bit Delta-Sigma D/A Processor System Achieving full-scale THD+N >100 dB

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A recently released low distortion and high dynamic range Delta-Sigma DAC achieves a dynamic range of 107 dB and full-scale Total Harmonic Distortion + Noise (THD+N) of 101 dB. This level of performance can be achieved with an understanding of 1-bit technology and thoughtful system design. The development of a DAC system employing this device will be discussed including the use of optocouplers, clock jitter attenuator, off-chip 1-bit latch and analog filtering.

1.0 Introduction

The performance capabilities of integrated audio Digital-to-Analog-Converters (DAC) continues to advance. Achieving these capabilities in a system requires attention to details that only a few years ago were inconsequential. To put this into perspective it is interesting to compare the noise requirements of analog and digital systems. The dynamic range of analog systems can often exceed 110 dB with output capabilities of 20 dBV or greater, equating to a system noise floor of approximately 30 μV. Integrated DACs generally have a maximum analog output of 6 dBV which requires a noise floor of 10 μV to achieve a 106 dB dynamic range. Not only is this less than one-third of the total noise allowable for a 110 dB analog system but must also be accomplished in the presence of MHz region sampling clocks.

The CS4303, Figure 1, is an example of a high performance DAC capable of a 107 dB dynamic range. The goal was to develop a complete DAC system incorporating a CS8412 AES/SPDIF Digital Audio receiver which would realize the performance capabilities of the CS4303. This paper will present critical design considerations and the DAC system architecture including jitter attenuation, optocoupling and analog filtering. The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of laser trimmed resistive DAC architectures [1] by using an

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inherently linear 1-bit DAC [2]. The advantages of a 1-bit DAC include:

1. Ideal differential linearity
2. No distortion mechanisms due to resistor matching errors
3. No linearity drift over time and temperature due to variations in resistor values.

2.0 1-Bit Conversion and the CS4303

The CS4303 DAC includes a digital interpolation filter, a delta-sigma modulator and a 1-bit DAC as shown in Figure 2. An understanding of the operation and capabilities of each stage is crucial to an optimum design and define the system performance goals.

2.1 Digital Interpolation Filter

Audio data is input to the digital interpolation filter which increases the sample rate by a factor of 8 and eliminates images of the baseband audio signal which exist at multiples of the input sample rate, Fs (Figure 3a). This allows for the selection of a less complex analog filter based on out-of-band noise attenuation requirements rather than anti-image filtering. Following the interpolation filter, the resulting frequency spectrum (Figure 3b) has images of the input signal at multiples of eight times the input sample rate, 8Fs. These images are removed by the analog filter required to filter the 1-bit data.

The dynamic range of an interpolation filter is limited by a finite number of data bits which is the source of truncation and quantization noise. The CS4303 interpolation filter data paths are 18-bit with 19-bit filter coefficients which equates to a dynamic range of better than 107 dB over the audio bandwidth. The interpolation filter has a -3 dB point of 0.4896Fs (23.5kHz for Fs equal to 48kHz) with a maximum passband ripple of +/- 0.0002 dB. It achieves this amplitude response while maintaining perfectly linear phase throughout the passband. Any deviation of the system from flat amplitude and linear phase response will originate in the analog filter.

2.2 Delta-Sigma Modulator

The interpolation filter is followed by a fifth-order delta-sigma modulator which converts the 8Fs multi-bit interpolation filter output into 1-bit data at 64 times Fs (64Fs). The ratio of the number of ones to the number of zeroes in the output is referred to as the one's density. The one's density will track the input code between the extremes of 70% for positive and 30% for negative full-scale with a mid-scale of 50%. The frequency spectrum of the 1-bit delta-sigma modulator output is shown in Figure 4 for an Fs of 48 kHz. Note that the inband noise peaks are well below -130 dB and yield a 120 dB dynamic range over the 20kHz audio bandwidth.

2.3 1-Bit DAC

This is the point where the signal returns to the analog domain, albeit in the MHz range. There are several important considerations since the ultimate performance of a delta-sigma DAC is dependent on the purity of the 1-bit data. The signal from the 1-bit DAC is filtered by an external analog

filter to produce the audio output and any errors that are introduced into the 1-bit signal due to noise from the voltage references or clock jitter will degrade the performance.

The delta-sigma modulator 1-bit output and the master clock control the switching between two reference voltages. Since these reference voltages are directly connected to the output of the DAC, any noise or interference on the references will be directly applied to the analog filter. Harris [3] discusses the effects of voltage reference noise for converters.

There is also an interesting relationship between variations in the amplitude of the reference voltages due to the 1-bit data. If the reference voltages are allowed to be modulated by the 1-bit data due to loading on the output or insufficient power supplies, second harmonic distortion and possibly tones will be generated. It is therefore critical that the reference voltages be stable and free from noise to achieve optimum performance.

To minimize distortion it is critical that the energy within each pulse be independent of a previous or next state. In Figure 5a, notice that the energy within the bit-period is affected by finite rise and fall time while in Figure 5b, the energy is not affected by either. To prevent this type of error the CS4303 utilizes return-to-zero coding where each occurrence of a 1 is 75% high and returns low for 25% of the bit period as shown in Figure 5c. This technique ensures that the energy within each 1 includes the effects of finite rise and fall times regardless of the previous or next state.

There is an additional situation that can add uncertainty to the energy contained in each occurrence of a 1. Each data bit is output from the 1-bit DAC for a period of time which is defined by the master clock. Variations in this timing due to clock jitter will lead to variations in the energy within pulses and directly translate to errors in the integrated signal. Harris [4] investigated the affects of clock jitter for analog-to-digital-converters and these effects are also applicable to digital-to-analog-converters. The CS4303 incorporates a differential output to maximize the output level and minimize the amount of gain required in the analog filter. Figure 7 shows each output as well as the differentially summed output for an arbitrary 1-bit data stream.

3.0 System Design

To obtain maximum performance from the CS4303, exceptionally clean references for the analog signal and a very low jitter clock are mandatory. Since the output stage on the CS4303 is on the same die as the interpolation filter and other logic, corruption of the output stage supplies and degradation of the clock edges is likely. To avoid these effects, optocouplers are used to create a completely isolated set of one's density data. This data is re-timed using a CMOS latch, clocked by a very low jitter clock. The power supplies to the latch are independent and very clean. Figure 7 shows the block diagram of the entire D/A processor board.

3.1 CS8412 Digital Audio Receiver

The system receives and decodes standard AES/EBU and S/PDIF data formats using a CS8412 Digital Audio Receiver. The output from the CS8412 is a serial bit clock, serial data, a word clock and a 256Fs master clock. The operation of this device is covered in detail in Reference [5].

3.2 Optocouplers

Optocouplers provide effective isolation between the analog circuitry and digital circuit noise. Hewlett-Packard HCPL-7101 optocouplers were chosen since they have built in CMOS input buffers and operate at 40MHz. The high output slew rate yields minimum corruption of the signal edges and low jitter on the clock. The input side of the optocouplers is well decoupled, since the LED's create significant current spikes. The output side of the optocouplers is referenced to analog ground, and has it own +5V power regulator. A large physical gap between the pins of each side of the optocoupler package was maintained on the circuit board, with no traces or ground plane reducing the physical spacing. This ensures maximum digital to analog isolation.

3.3 1-Bit Latch

The external CMOS latch used to time the data is a 74AC11074 from Texas Instruments. This dual D-type flip-flop was chosen because of its center power and ground connections, which reduce internal inductances and the possibility of the supplies being modulated by the output signal. The device also has a high output drive capability, which is important since we wish to minimize the input impedance of the analog filter for noise considerations.

The supplies to the latch are the voltage references for the 1-bit data. Extreme care must be taken to optimize the supply decoupling with low value high frequency capacitors positioned very close to the supply and ground pins. High value capacitors significantly reduce low frequency noise in the latch output data. The capacitors not only act as decoupling for the latch but also serve as a power supply noise filter.

Good latch supply decoupling is also important to minimize 2nd harmonic distortion. As the one's density of the data varies, then the loading on the latch supply varies. If the supply is inadequately decoupled then the supply voltage will change in sympathy with the signal. This is effectively multiplying the signal by itself, yielding 2nd harmonic distortion.

There are significant advantages in the use of a dual flip-flop. Due to the differential nature of the DAC output, it is possible to minimize thermal gradients within the latch and improve distortion performance. This can be accomplished by using a separate dual latch for each channel.

The latch clock rising edge is timed so that the set-up and hold time requirements for the data inputs are met with a generous margin.

3.4 Clock Jitter Attenuator / VCXO

Clock jitter can originate from the original AES/EBU signal, the VCO in the CS8412, and from the optocouplers. To reduce the clock jitter as much as possible prior to the latch, a Phase Lock Loop (PLL) is used as a jitter attenuator. Figure 8 shows the schematic of the latch clock generator/jitter attenuator. The PLL consists of a phase detector, a voltage controlled oscillator and a loop filter.

The phase detector was implemented using an 74AC11086 exclusive or gate. This phase detector introduces a 90 degree phase shift, which results in the correct timing of the output clock for the latch. The phase detector is also inherently free from hysteresis improving jitter performance.

The requirement for a low jitter clock led to the choice of a voltage controlled crystal oscillator (VCXO). Devices made by Raltron have been shown to have low intrinsic jitter. This allows the use of a low frequency loop filter, since the PLL is not required to reduce inherent jitter in the oscillator.

The loop filter is a single pole RC network. The design procedure is as follows:

1) A phase margin of 60 degrees is chosen. This yields a critically damped response.

2) The PLL open loop gain is calculated, by multiplying the phase detector gain and the VCXO gain. G = Kd. Ko = Vcc/π . 2π (615) = 6150 rad/sec. This is the unity gain frequency.

3) Using an RC time constant equal to the inverse of the unity gain frequency will yield a 45 degree phase margin. A 60 degree phase margin is 15 degrees greater than 45 degrees. The slope of the single pole RC filter is 45 degrees/decade. Therefore, the corner frequency of the loop filter needs to be increased by a factor of 15/45 decades. This yields a corner frequency of 2.38 kHz.

4) A 0.1 µF capacitor was chosen because capacitors behave most ideally at that value. This leads to choosing a 681 ohm resistor.

Power for the phase detector and VCXO must be very clean in order to avoid output clock jitter. Independent +5V regulators for the VCXO and phase detector ensure no coupling between the VCXO and phase detector output transitions via the supply. The layout of the PLL should be such that the loop filter is close to the VCXO. This minimizes the possibility of induced noise into the control pin on the VCXO.

3.5 Analog Filter

The selection of the analog filter transfer function is based on the optimization of out-of-band noise attenuation, passband amplitude and phase requirements. The filter must be implemented not only to minimize noise and distortion but also to properly load the DAC and to accept the high frequency 1-bit data avoiding slew rate limitations. The primary function of the analog filter is to attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The computer simulated frequency spectrum of the 1-bit delta-sigma modulator output is shown in Figure 4 for an Fs of 48 kHz. Note that the out-of-band noise begins to increase beyond 20 kHz and it is the attenuation of this out- of-band noise which must be considered. Due to the sharp increase in noise near the passband, a compromise must be made between the goals of linear phase, a flat passband and the attenuation of out-of-band noise.

A Butterworth function has the desired maximally flat passband response, out-of-band attenuation and acceptable phase characteristics. Figures 9-11 show the results of computer simulations dem-

onstrating the out-of-band noise attenuation of 3, 5 and 7 pole Butterworth filters where the filter corner frequencies were selected to achieve a maximum attenuation of .2 dB at 20kHz.

The circuit of Figure 12 is a 5-pole Butterworth modified to realize a 6-pole response. The real pole of the standard Butterworth configuration has been altered and complemented with an additional real pole. These poles have been positioned for the frequency response of Figure 13-14 and the group delay of Figure 15. The out-of-band noise attenuation is demonstrated in the system performance plot of Figure 16. Notice that the noise peaks remain well below 100 dB. Implementing a pole as a passive RC in the input of the analog circuit along with the 40 V/μs slew rate of the Burr-Brown OP-627 op-amp, eliminates slew rate related distortion. The architecture of Figure 12 also provides matched loading for the latch outputs, as well as adding the noise-free pole for additional out-of-band noise attenuation.

4.0 System Performance Measurements

Figures 9-11 raise an interesting question concerning Dynamic Range and THD+N specifications. The specifications for each plot over a 20kHz bandwidth are identical, but the dynamic range differs by 46 dB over the 120kHz bandwidth. Therefore, the filter used to band-limit the measurement will greatly affect the results. As an example, the 22kHz band-limiting filter of the Audio Precision System One is insufficient to compare the in-band performance between either a 3, 5 or 7 pole system. The dynamic range and THD+N specifications for the CS4303 DAC system were obtained by digitizing the output with a CS5327 ADC and performing an FFT on the data. This allows the measurement bandwidth to be set precisely at 20kHz and remove out-of-band influences.

The following collection of CS4303 measurement plots (IWR = 48 kHz) were taken with an Audio Precision Dual Domain System One. All FFT plots are 16,384 point. Several of the plots are influenced by inadequate dithering of the test signal. Lipshitz [9] discusses these effects.

Figure 16 shows the **unmuted noise**. This data was taken by feeding the CS4303 all zero's. This plot shows the noise shaping characteristics of the delta-sigma modulator combined with the analog filter.

Figure 17 shows the system **frequency response** with a 48 kHz input word rate. The 0.2 dB rise at 18 kHz is the result of component tolerances.

Figure 18 shows the A-weighted **THD+N vs signal amplitude** for a dithered 1kHz input signal. The small variations in THD + N at around -70 dB are caused by inadequate dithering of the test signal. The System One was set to 18-bit triangular dither.

Figures 19 and 20 show the **fade-to-noise linearity**. The input test signal is a dithered 500 Hz sine wave which gradually fades from -60 dB level to -120 dB. During the fading, the output level from the CS4303 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs of -90 dB. The gradual shift of the plot away from zero at signal levels < -100 dB is caused by the background noise starting to dominate the

measurement. Figure 19 shows the result with 18-bit dithered data. The 1 dB shift at -95 dB is due to inadequate dither. Figure 20 shows the result with 16-bit dithered data.

Figure 21 shows a 16K **FFT plot result, with a 1 kHz -100 dB 17-bit dithered input**. Notice the lack of distortion components.

Figure 22 shows the **monotonicity test** result plot. The input data to the CS4303 is +1 LSB, -1 LSB four times, then +2 LSB, -2 LSB four times and so on, until +10 LSB, -10 LSB. This data pattern is taken from track 21 of the CD-1 test disk. Notice the increasing staircase envelope, with no decreasing elements. Notice also the clear resolution of the LSB. For this test, one LSB is a 16-bit LSB.

The following tests were done by filtering the analog output of the CS4303 with the System One analyzer 1 kHz notch filter to reduce the peak signal level. The resulting signal was then amplified and applied to the DSP module, avoiding distortion in the System One A/D converter.

Figure 23 shows a **16K FFT Plot with a 1 kHz, 0 dB** input. Notice the low order harmonic distortion at < -100 dB.

Figure 24 shows a **16K FFT Plot with a 1 kHz, -10 dB** input. Notice the almost complete absence of distortion, with a small residual 2nd harmonic below -120 dB.

5.0 Conclusion

An 18-bit delta-sigma DAC system achieving 104 dB dynamic range and a full-scale THD+N of 101 dB has been discussed. Many subtle implementation details have also been revealed. Measurements and listening tests confirm state-of-the-art performance.

6.0 Acknowledgments

Many thanks to Eric Swanson and Jeff Scott of Crystal Semiconductor for their invaluable insights, suggestions and encouragement. Jamie Dugan for his patience through the many edits and revisions.

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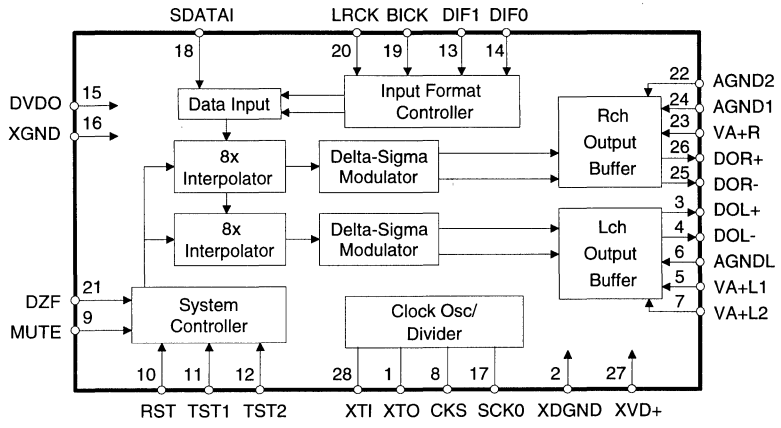

Figure 1. CS4303 Block Diagram

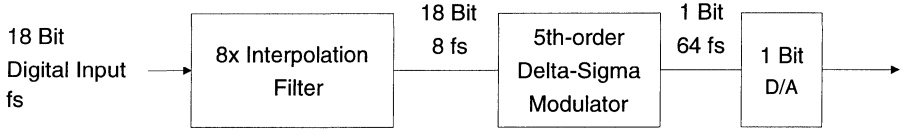

Figure 2. CS4303 Architecture

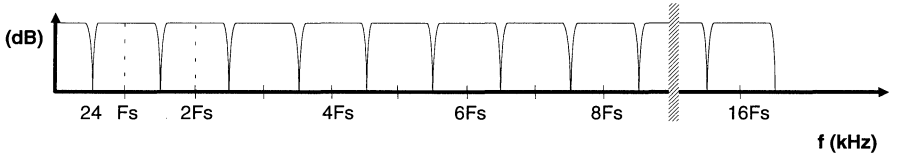

Figure 3a. Interpolation Filter Input Spectrum

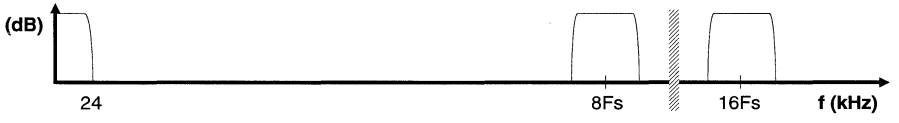

Figure 3b. Interpolation Filter Output Spectrum

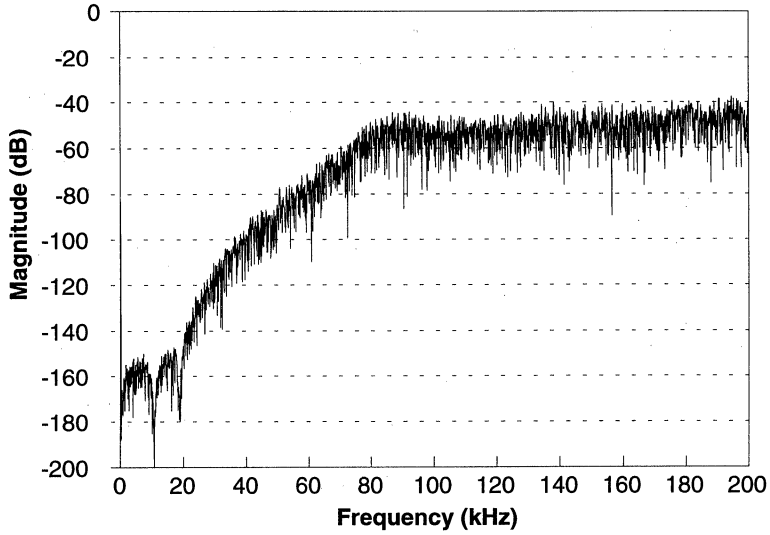

Figure 4. 48 kHz Delta-Sigma Modulator Output Spectrum

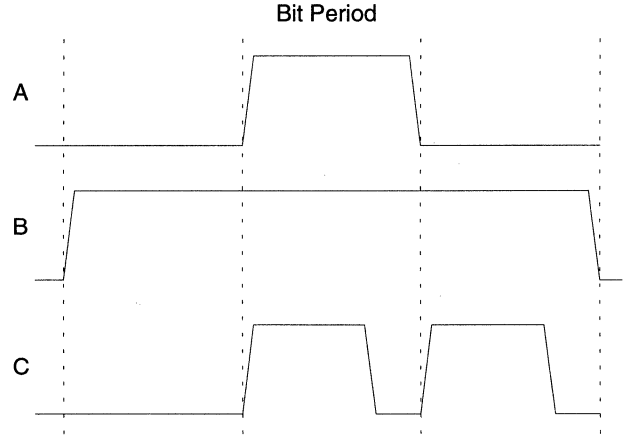

Figure 5. Bit Period Energy Effects.

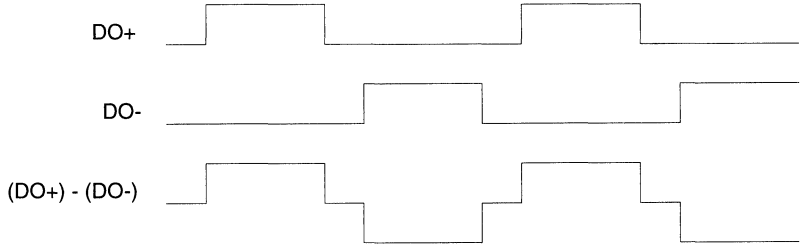

Figure 6. CS4303 Differential Output

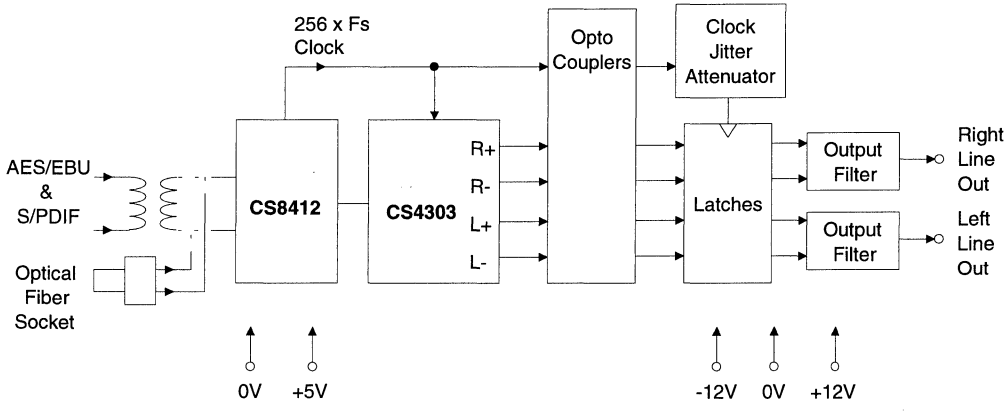

Figure 7. CS4303 Evaluation Board Block Diagram

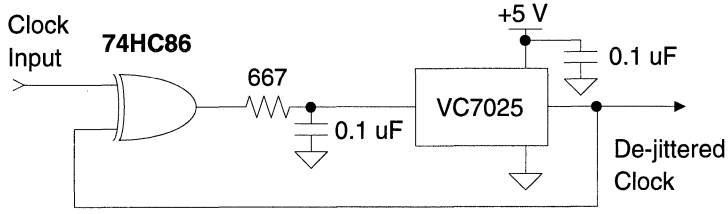

Figure 8. Clock Jitter Attenuator/PLL Schematic

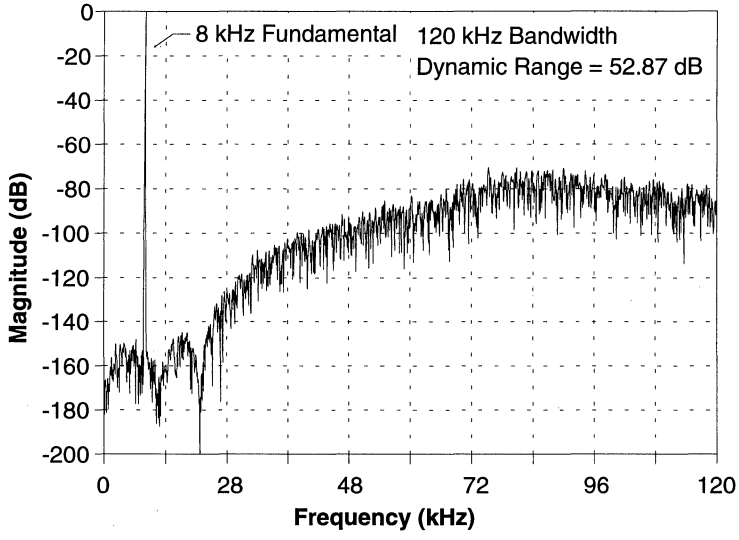

Figure 9. Filtered Modulator Output Spectrum
3rd Order -3 dB @ 33.28 kHz (Simulated)

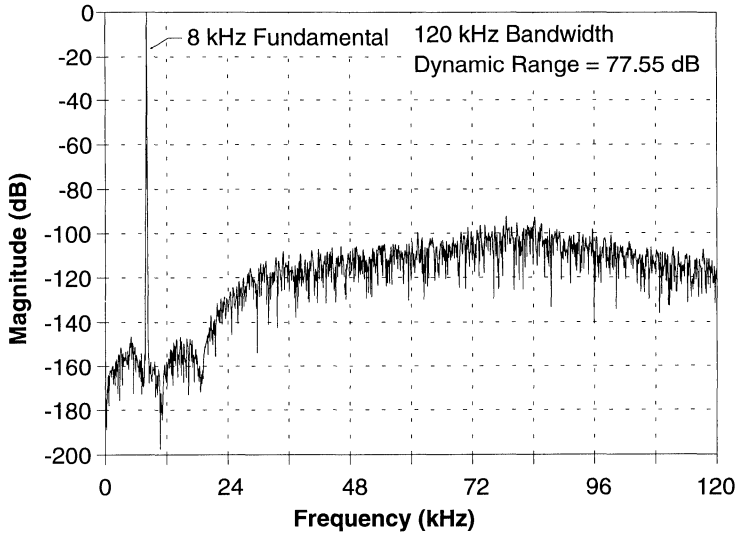

Figure 10. Filtered Modulator Output Spectrum 5th Order -3 dB @ 27.15 kHz (Simulated)

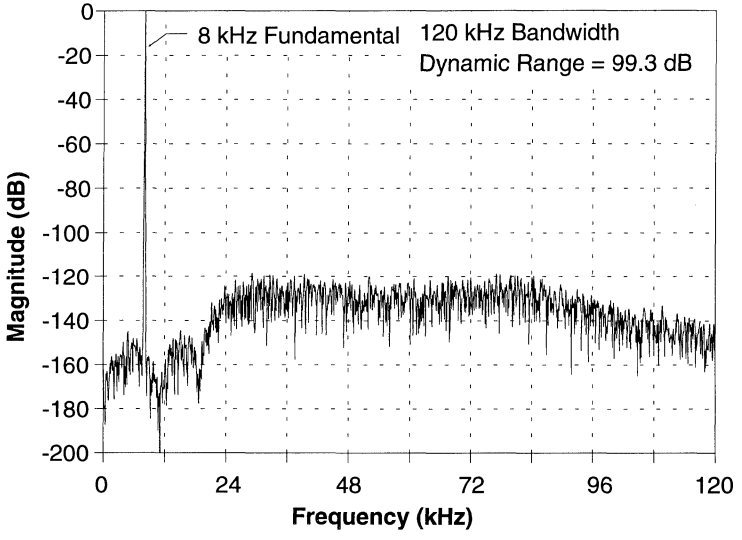

Figure 11. Filtered Modulator Output Spectrum 7th Order -3 dB @ 24.88 kHz (Simulated)

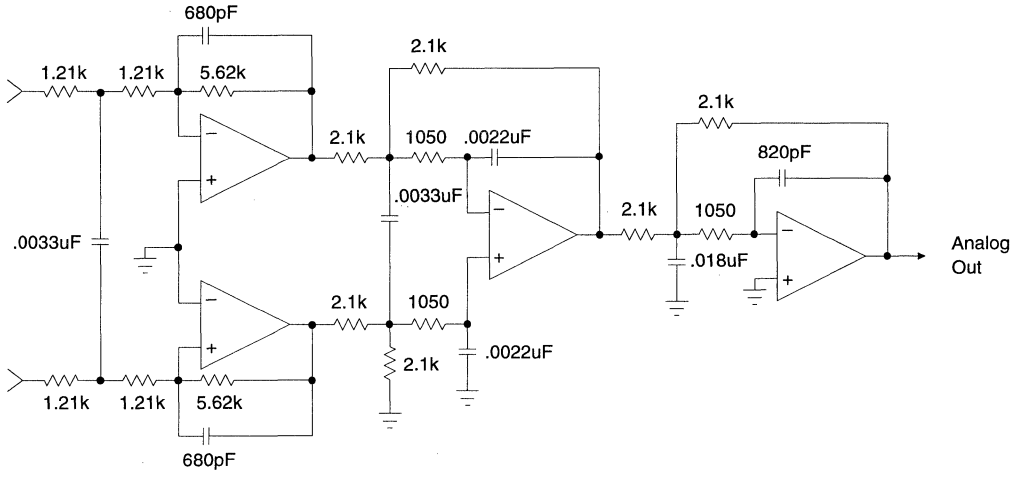

Figure 12. Analog Filter Schematic

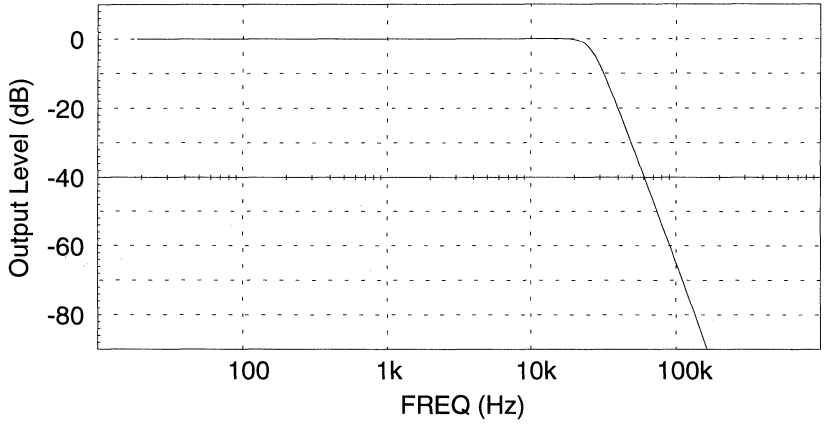

Figure 13. Simulated Analog Filter Frequency Response.

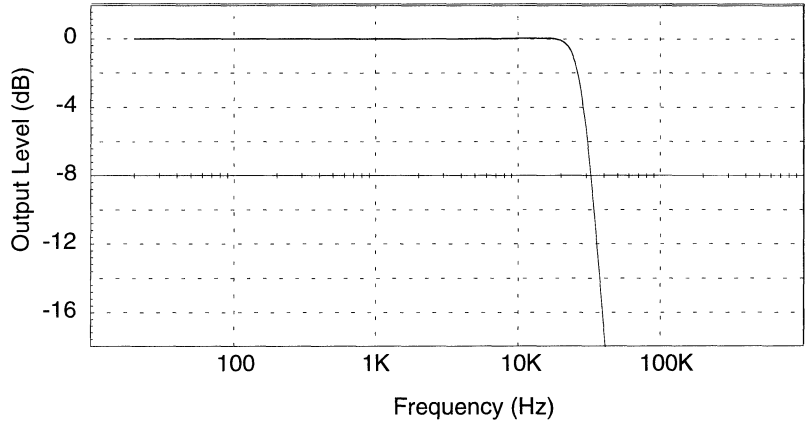

Figure 14. Simulated Analog Filter Frequency Response Expanded Scale

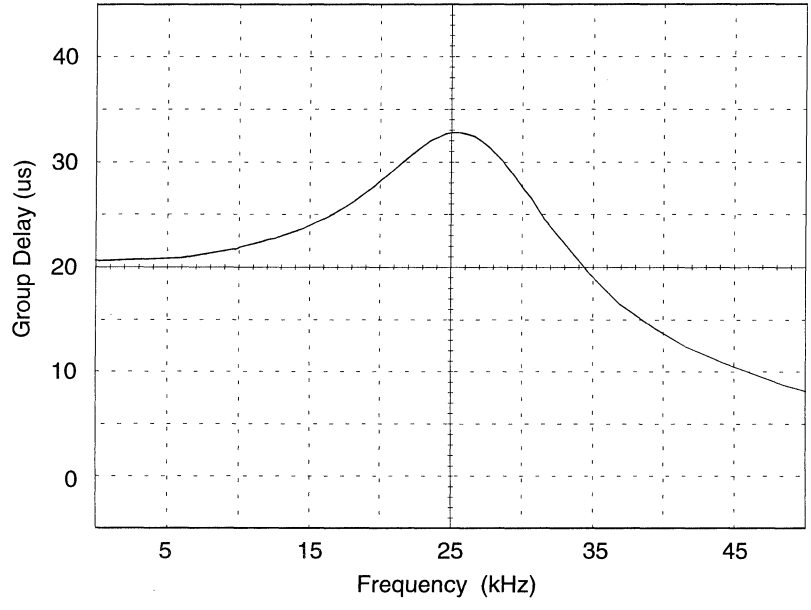

Figure 15. Simulated Analog Filter Group Delay

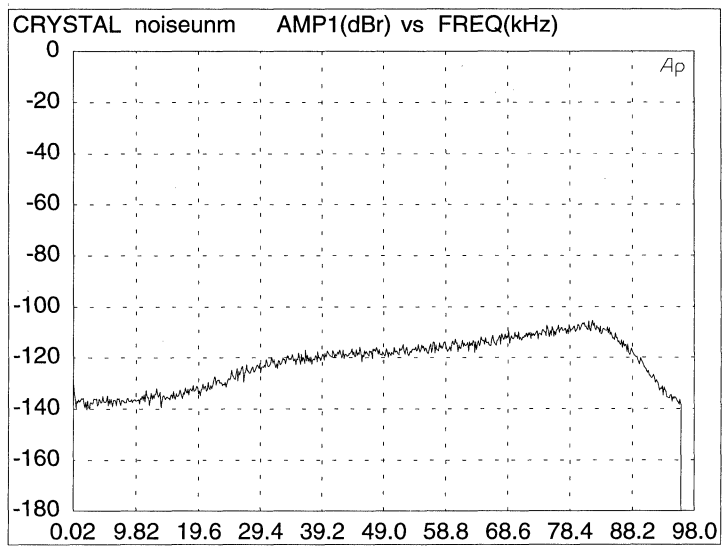

Figure 16. Unmuted Noise

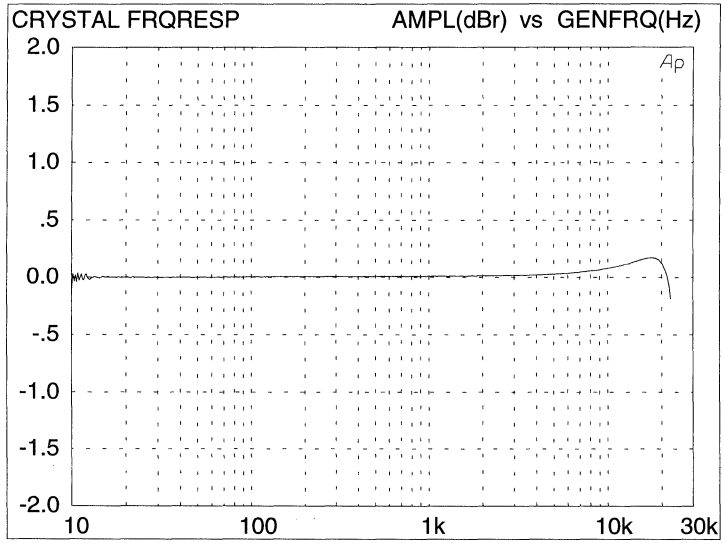

Figure 17. System Frequency Response

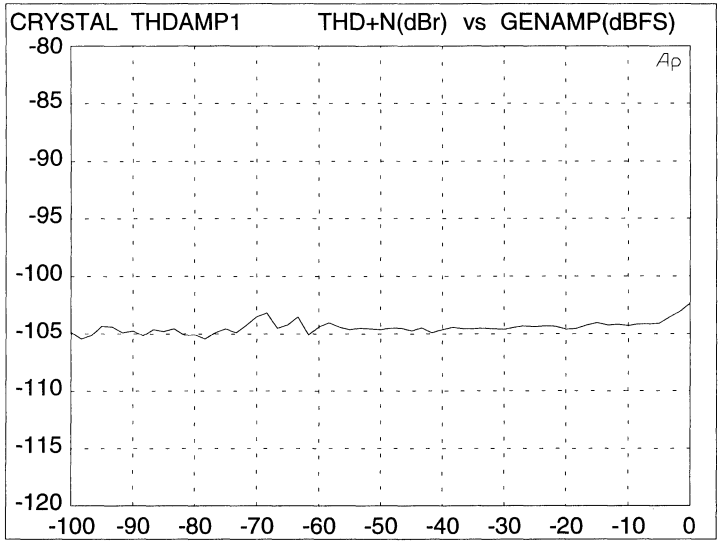

Figure 18. 1 kHz A-weighted THD + N vs Level

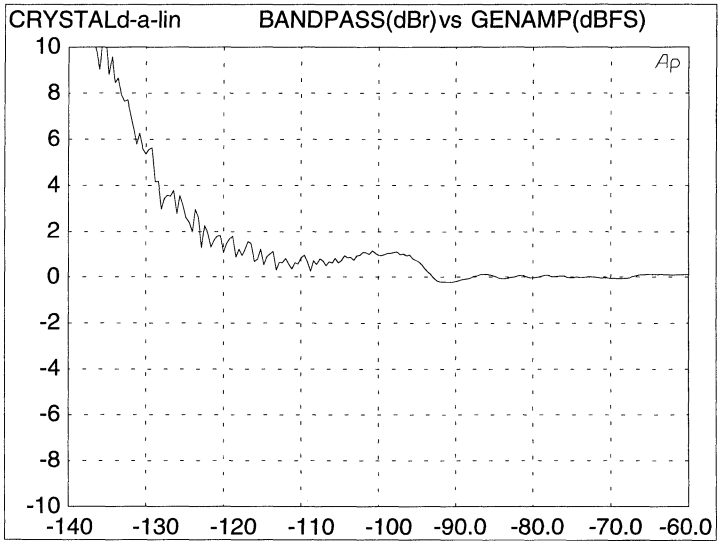

Figure 19. Fade to Noise Dithered 18-bit Linearity

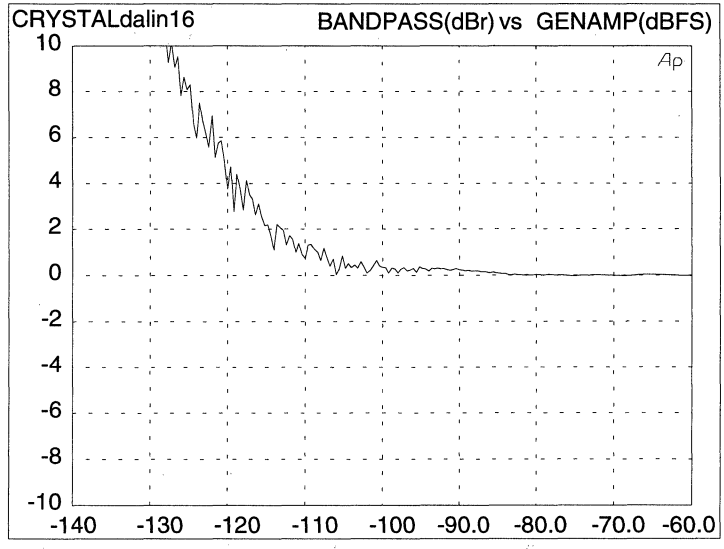

Figure 20. Fade to Noise Dithered 16-bit Linearity

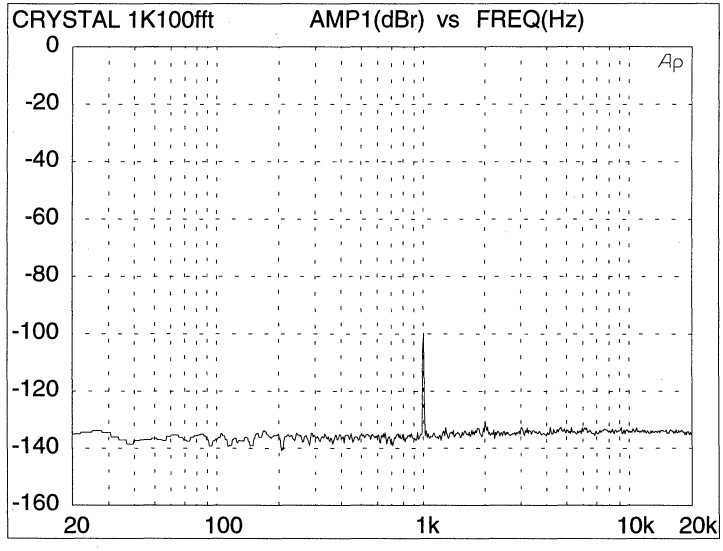

Figure 21. 1 kHz -100 dB FFT

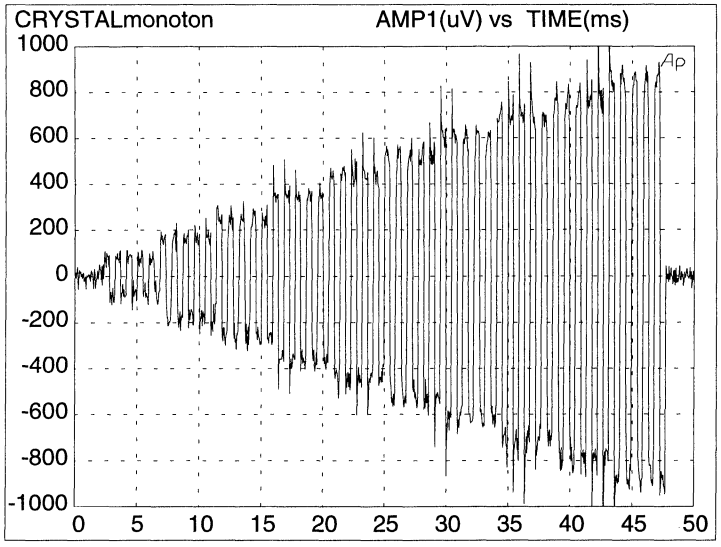

Figure 22. Monotonicity Test (16-bit Data)

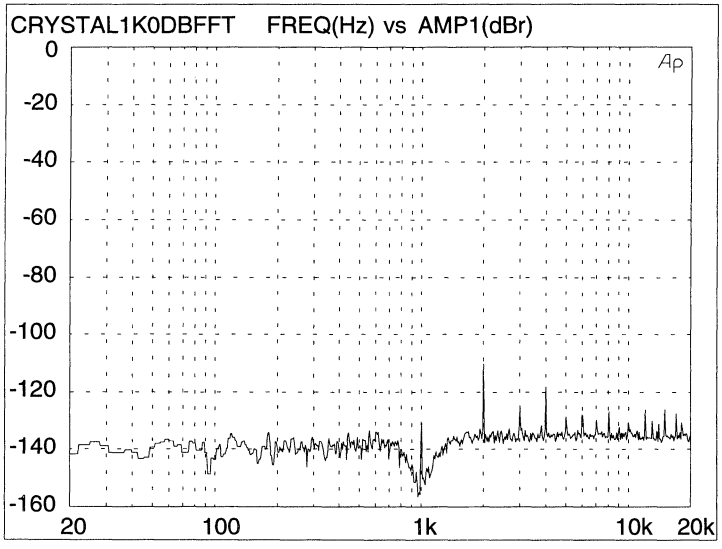

Figure 23. 1kHz 0 dB FFT

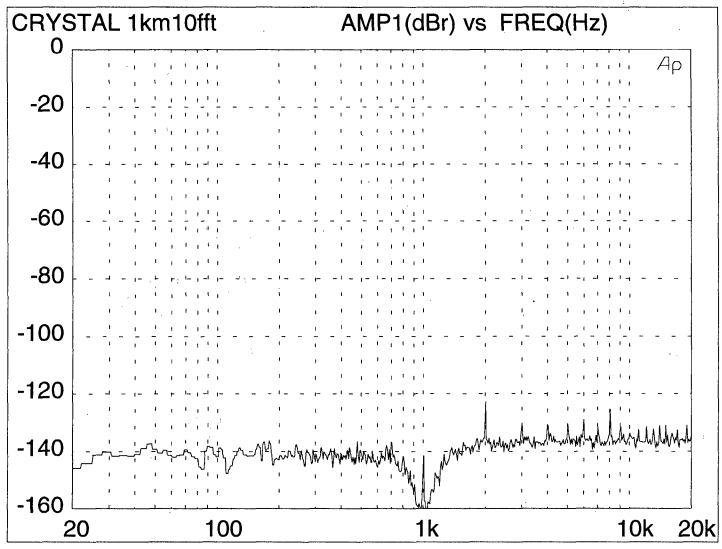

Figure 24. 1 kHz -10 dB FFT

How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters

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Modern delta-sigma A/D & D/A converters are capable of very high levels of performance. Realizing the full potential from this class of converters requires attention to many details. This paper discusses these details which include clock jitter and interference effects, ground plane techniques, minimizing power supply coupling and reducing tone effects. The paper concludes with a checklist of rules, which, if followed, will ensure optimal converter operation.

1.0 Delta-Sigma Converters - Fundamentals

Delta-sigma analog-to-digital and digital-to-analog converters (ADCs and DACs) offer the digital audio equipment designer many benefits, including freedom from complex analog anti-aliasing and reconstruction filters, perfect differential non linearity, high integration and low cost. A study of the theory of operation of such converters reveals some particular sensitivities, which, if not taken into account during equipment design, can lead to degraded performance. In order to understand these degrading mechanisms, several fundamental concepts need to be reviewed. These are oversampling, noise shaping, aliasing and the multiplicative nature of the voltage reference input of a converter.

1.1 Oversampling

To digitize and subsequently reconstruct a signal, it must be sampled with a sampling frequency (Fs) of at least twice the maximum signal frequency (Fb). Sampling at exactly 2Fb is known as Nyquist rate sampling. Oversampling is when Fs is greater than 2Fb.

When a large signal is digitized, the signal to quantization noise ratio is approximately 6 times the number of bits in the digitizer. The quantization noise is white and is equally spread between dc and Fs/2. Delta-sigma converters internally quantize the signal with a resolution of 1-bit, yielding a signal to noise ratio of approximately 6dB. Using an Fb of 24kHz, and a 64X oversampling ratio, the input sample rate is very high at 3.072MHz; therefore, the quantization noise is spread out between dc and 1.536MHz. Subsequent digital filtering removes the noise between 24kHz and

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1.536MHz. This greatly improves the signal to noise ratio in the frequency band of interest, dc to 24kHz. However, even 64 times oversampling is insufficient to yield an acceptable signal to noise ratio, so noise shaping is used to further lower the noise.

1.2 Noise Shaping

The quantizer in a delta sigma converter has a noise floor which is shaped such that most of the quantization noise is out of the frequency band of interest (dc to 24 kHz), yielding very low noise in the audio band. Such quantizers are known as delta-sigma modulators, and may be realized in analog form for an ADC, and in digital form for a DAC. Welland [1] and Sooch [2] papers contain excellent analyses of delta-sigma conversion for both ADCs and DACs.

1.3 Aliasing

Aliasing occurs when a high frequency signal is translated to a lower frequency by sampling the signal at a frequency less than 2Fb. For example, if a 47kHz signal is presented to a Nyquist rate converter sampling at 48kHz, then a 1kHz digital signal will be the result. With delta-sigma converters, the input sample rate is very high. With an input sample rate of 3.072MHz, aliasing occurs at frequencies greater than 1.536 MHz. For example, a 3.062MHz input into the converter will appear at 10kHz in the output spectrum. Thus, delta-sigma converters require particular attention to interfering frequencies in the MHz range, of which there are many in today's digital equipment.

1.4 Voltage Reference Input to an ADC/DAC

The transfer function of a 16-bit ADC is N = 32767xVin/Vref, where Vin is the input voltage, N is the output word and Vref is the dc voltage reference. For a 16-bit DAC, the transfer function is Vout = NxVref/32767, where N is the input word, Vout is the output voltage and Vref is the dc voltage reference. Notice in both cases, the voltage reference, Vref, has a multiplicative relationship with the output. In theory, the voltage reference is only a dc voltage, with no AC component. In reality, the voltage reference will have some noise, and it may also have some discrete frequencies present caused by interference. These AC components are multiplied by the input signal, yielding sum and difference frequency components in the output, since signal multiplication causes amplitude modulation.

In the case of a delta sigma converter, there is significant energy in the shaped quantization noise at high frequencies, which when amplitude modulated by high frequency interference on the reference, results in an elevation of the noise floor of the converter in the audio band (Figure 1). Thus a single interfering high frequency, if inadequately decoupled from the voltage reference, has the somewhat surprising result of an elevated noise floor in the audio band.

2.0 Converter Artifacts

This paper studies 2 kinds of converter artifacts: noise and discrete frequencies. Noise effects elevate the noise floor of the converter from its expected level. Discrete frequencies are particularly troublesome, since the ear is remarkably good at detecting single frequencies out of the noise floor [3].

The common measurement tool for measuring these artifacts is the spectrum analyzer, often using a Fast Fourier Transform (FFT) technique. An FFT performed on the output of a converter allows the noise floor to be measured and tones to be revealed. High resolution FFTs, for example 16K points, are required to yield sufficiently low noise content of each frequency bin to allow barely audible tones to be measured. The Audio Precision System One is an example of measuring equipment using this technique [Reference 4].

3.0 Clock Jitter Effects

Wide dynamic range audio converters are sensitive to clock jitter. Harris [Reference 5] explored the effects of clock jitter. In summary, if the clock edges running the converter vary in time about their nominal position in a random fashion, then the noise floor of the converter will elevate. If the clock jitter is periodic in nature, then FM modulation occurs, and sideband tones will appear equally spaced either side of the signal frequency. Clock jitter greater than 50 ps rms can be unacceptable in some high quality audio converters. The best way to avoid these effects is to use a crystal oscillator to generate the sampling clock. Typical jitter from such an oscillator is under 10ps rms. The oscillator should have a clean power supply, and should be positioned close to the ADC and/or DAC. The rest of the audio system should then be locked to this oscillator. This architecture will make sure that clock jitter at the converter is minimized.

An example of this is the separation of a CD transport from the DAC function. Several manufacturers use a crystal oscillator in the DAC box which runs the DAC. An AES/EBU signal derived from this clock is then transmitted to the transport unit. The transport electronics are operated from the recovered 256xFs clock from an AES/EBU receiver chip. The CD transport audio data is transmitted back to the DAC box, using the same clock, for conversion to audio. New AES/EBU devices [Reference 6] allow whole networks to be run synchronously, with the timing master being resident in the converter unit, thus minimizing clock jitter effects on the converter.

4.0 Power Supply Rejection of Delta Sigma Converters

One mechanism by which high frequencies can interfere with the operation of a delta-sigma converter is via the power supply. Figure 2b shows what happens when a high frequency near to the input sample rate is deliberately injected into the supply. The injected high frequency is not a pure sine wave; harmonics are present. Therefore the shape of the resulting interference is not a tone, but a collection of tones. Notice how the higher harmonic interference has the same shape as the lower

frequency, but is more spread out. This is because the harmonics of the interference are proportionally further removed in frequency away from multiples of the input sample rate. This yields a characteristic cluster of tones. System clocks are square waves, often yielding clusters of tones which contain odd harmonics.

If the interfering frequency is changed and the ability of the converter to reject the frequency is measured, then Figure 3 is the result. Notice the approximately 50dB of power supply rejection in the audio band, then the very steep improvement coincident with the transition band of the output filter of the converter. Between 24 kHz and 3.072MHz - 24kHz, the power supply rejection is very good, in fact it is difficult to measure reliably because of the effectiveness of the digital filter. At exactly 3.072MHz - 24kHz, the power supply rejection becomes much worse, in fact only around 20dB. The window of poor rejection lasts until 3.072MHz + 24kHz. Similar 48kHz wide windows of poor rejection occur around multiples of the input sample rate. If the sample rate of the converter is changed, then the power supply rejection against frequency plot scales with the change in frequency. Thus in systems which switch between 32kHz, 44.1kHz and 48kHz operation, there are a number of sensitive frequency regions.

There are many board level coupling mechanisms that will be discussed later, but careful attention to the choice of system clock frequencies can result in more robust system performance by avoiding the sensitive frequency regions.

5.0 Synchronous Clock Effects

An effect peculiar to delta-sigma converters becomes apparent after close study of the output spectrum of a delta-sigma modulator. Figure 4 shows the output spectrum of a delta-sigma modulator with an input voltage which yields exactly 50% ones density output. Notice the shaped quantization noise, with a tone at exactly half the input sample rate (IFs/2). This is present because of the high number of occurrences of 010101 sequences, which have a fundamental frequency of IFs/2.

In a real system, the modulator input circuitry and any external circuitry will have voltage offsets. In a digital modulator, the digital data may not be centered on the mid-scale code. Figure 5 shows the output spectrum in the presence of a small dc offset. Notice a frequency component at a small displacement frequency (Fd). This frequency is caused by occasional occurrences of 00 and 11 amongst the occurrences of 010101. The frequency with which the pairs of zeros or pairs of ones occur is Fd, and is proportional to the dc offset. This tone, slightly displaced from IFs/2 is, in itself, not a problem, since it will be filtered out along with the quantization noise.

However, if a signal of exactly IFs/2 is coupled onto the voltage reference, then, because of the multiplicative nature of the voltage reference, sum and difference frequencies occur. The difference between IFs and IFs/2 - Fd is Fd, which could lie in the audio band. The IFs/2 frequency may well be present in a system, since IFs/2 is an integer divide ratio from the master sampling clock. Thus, the combination of dc offset, and IFs/2 coupling onto the reference, yields an audible tone. Figure 6

shows such a tone, with 50mV input dc offset and 2mV of IFs/2 deliberately injected onto the voltage reference. The resulting tone is clearly evident.

The behavior of such tones with varying dc offset can be seen in Figure 7. Notice the linear behavior. The serial bit clock for a 2-channel 16-bit converter naturally calculates out to be IFs/2 for some converters (16 right bits + 16 left bits = 32 bits per word period = IFs/2 for a 64 X oversampled converter). A robust system design will avoid the use of clocks with a frequency of IFs/2, typically using IFs for the serial bit clock instead.

6.0 Coupling Mechanisms

In a real system, various mechanisms exist which can couple interfering energy into the ADC or DAC. These coupling mechanisms can be classified into direct, capacitive, magnetic and radio frequency. A short study of the characteristics of each mechanism will allow us to design systems which minimize unwanted coupling.

6.1 Direct Coupling

The most common form of direct coupling is the mixing of ground return currents through a common ground connection. It is particularly damaging if digital currents find their way into analog signal paths.

The usual way of preventing direct coupling is to use entirely separate connections for digital ground and analog ground. The two grounds are then connected together at one place. Common choices for the connection point are next to the power connector on the printed circuit board, at the power supply and at the converter. Experienced designers allow for all three possibilities, the best place being determined by performance measurements.

6.2 Capacitive Coupling

Stray capacitance between circuit elements and connections will couple unwanted signals into sensitive nodes. Figure 8 shows a model of this mechanism, along with a frequency response plot. From this model we can deduce several guidelines to reduce this effect. Firstly, minimize the size of the stray capacitance by reducing the area of the plates. This normally involves minimizing the length of sensitive PCB traces. Also the spacing between the plates of the stray capacitor must be as large as possible, leading to physical separation between digital and analog circuits. A floating metal region between circuit elements can greatly increase coupling, and should be avoided. From the frequency response plot, it follows that low frequency noise sources cause less interference than high frequency. Therefore slowing down fast digital signal edges can often result in reduced interference. Lowering the impedance of the sensitive traces to ground reduces the magnitude of the coupled voltage.

6.3 Magnetic Coupling

Magnetic coupling is a current related effect, as shown in Figure 9. The induced noise voltage is dependent on the rate of change of the current, the mutual inductance and the orientation of the transmitter with respect to the receiver. The mutual inductance is dependent on the spacing between the transmitter and the receiving loop, and on the loop area. Therefore to minimize the coupling, physical separation should be large, current rise times should be slow, loop area should be small and the relative orientation should be perpendicular. Figure 10 shows the small loop area that occurs when a ground plane is used for the return connection.

6.4 Radio Frequency Interference and Electric Field Effects

Digital audio equipment often has to operate in an environment where there is much RF energy, for example in a broadcast studio or in satellite TV stations. The goal of the equipment designer is to reduce the susceptibility to RF pickup. This is accomplished largely by using the correct power supply, input and reference decoupling components, and by minimizing the decoupling capacitors' total loop area. The use of both surface mount packages for the converter ICs and surface mount decoupling components is highly recommended. Also, there should be no large areas of copper plane either floating or attached to the reference or input of the converter. An additional low impedance path at high frequency between the analog and digital ground pins of the converter can often reduce the effects of RF fields. This may be achieved by a wire link or a small value capacitor.

7.0 Ground Planes

Ground planes in the digital region minimize ground return current loop area, since the return current will follow under the associated trace at high frequencies (Reference [5]). Figure 11 shows how the radiated magnetic field is reduced. The return current magnetic field cancels the primary current magnetic field for distances much greater than the board thickness.

Ground plane fill in the analog region acts as a magnetic field shield by causing the field to be absorbed, since the ground plane fill acts as a shorted turn (Figure 12). The secondary current induced in the ground fill generates a magnetic field. This field induces a voltage in the conductor of interest that tends to cancel the voltage induced by the primary current.

Measuring the coupling between adjacent traces with and without ground plane fill revealed that up to 30dB reduction of coupling is possible. Thus using ground plane fill is a very effective technique for reducing digital to analog interference. Remember to fill in the digital regions to reduce the transmission of noise, in addition to filling in the analog regions to reduce the reception of noise. These two effects add in dB, and are therefore very effective when used together.

8.0 Distortion Mechanisms

Modern delta-sigma converters achieve distortion figures of better than 0.001%. It is quite easy to degrade the converter performance by using non-optimal external circuits. The most common cause of excessive large signal distortion is the use of incorrect filter capacitors. Any capacitor which is between the signal path and ground should be a low voltage coefficient type, for example NPO or COG. Normal ceramic decoupling types, for example X7R, are not suitable, and will result in severe harmonic distortion at full scale.

Another potential effect is illustrated in Figure 13. Here the use of a non inverting amplifier configuration has caused excess distortion. The distortion is caused by common mode stress of the input stage as the input voltage varies. The use of an inverting configuration removes this effect, since both input terminals of the op-amp stay at zero volts.

9.0 A Checklist of Layout and Design Rules

Extensive experience of system designs has led to a list of recommended design techniques. If these are studied and followed, then optimum ADC and DAC performance is assured.

a) Partition the board with all the analog components grouped together in one area and all the digital components in the other. Do not surround the digital area with the analog area or vice versa. Position components to minimize the return current path and loop area. Do not allow high current returns to mix with sensitive signal paths.

b) Have separate analog and digital ground planes on the same layer, with the digital components over the digital plane, and analog components, including the analog power regulators, over the analog plane. The split between the planes should be 1/8 inch.

c) Mixed signal components, including the data converters, should bridge the partition in the ground plane with only analog pins in the analog area, and only digital pins in the digital area. Rotating the converter package can often make this much easier.

d) Analog and digital grounds should only be connected at one point. The best alternative points are at the power supply, where the supplies enter the board and at the converter. Provide facilities for alternative connection points.

e) Analog power and signal traces should be over the analog ground plane. Digital power and signal traces should be over the digital ground plane. No traces should cross the gap between the two planes.

f) Keep digital signal traces away from the analog supply, voltage reference and analog pins of the converter.

g) Bypassing capacitors should be close to the converter IC pins, and positioned for the shortest possible signal connections. For example, the voltage reference decoupling capacitor should be surface mount, and there should be only a very short trace from the reference pin to the capacitor. The 0V end of the capacitor should be directly attached to the analog ground plane.

h) If both large and small decoupling capacitors are recommended, then the small one should be nearest to the IC. For multi-layer boards, make the connections to the IC and the capacitor on the same layer.

i) For boards with more than 2 layers, do not overlap analog and digital ground planes. Do not have a plane which crosses the split between the analog and digital ground planes.

j) Avoid multiple crystal oscillators or asynchronous clocks. When using converters with DSPs or microcontrollers, operate everything from one oscillator using dividers.

k) In systems requiring multiple crystals for selecting alternative sampling rates, enable only one oscillator at a time. Shut off unused oscillators by removing power.

l) When using switching power supplies, DC to DC converters or chopper stabilized amplifiers, lock the switching frequency to the ADC and/or DAC sampling frequency.

m) Do not connect the sampling clock to the converter via a PAL, analog multiplexer, opto-coupler, gate array or other circuits which can cause clock jitter.

n) Locate the crystal oscillator for the sampling clock close to the converter. Avoid overshoot and undershoot on the sampling clock, which can inject transients into the converter.

o) Do not drive signals off the circuit board directly from converter digital signals. Excessive current transients can occur when driving capacitative cables. Always use a buffer, which will prevent the current transients interfering with the converter.

p) When converters are used in a particularly hostile environment, for example inside a personal computer, then a metal screen on both sides of the board will reduce radiated interference effects. The screen should enclose the entire converter and associated analog components.

q) Make sure that any potentially interfering clocks are not in the sensitive frequency regions exhibited by delta-sigma converters.

r) Make sure that the digital supply decoupling for the converter is such that the loop area is minimized. A small ferrite bead close to the converter, and before the decoupling capacitor, will prevent the digital current loop area extending beyond the immediate vicinity of the converter, Reference [6].

s) Do not have clocks in the equipment at 1/2 the input sample rate of the converter. If an IFs/2 frequency clock couples into the voltage reference, then tones can occur. Odd order sub-multiples of IFs/2 are also potentially dangerous, since clocks will have odd harmonics. For example, IFs/6 clocks will have a strong component at IFs/2.

t) Empty regions between printed circuit board traces should be filled with copper. The filled regions should be electrically attached to the appropriate ground plane (digital in the digital region, analog in the analog region). This technique reduces the electromagnetic radiation from the digital section, and reduces the sensitivity of the analog traces to radiated effects.

10.0 Debugging Checks

Three simple tests can help to identify the source of excess noise in an ADC/DAC system.

1) If the noise floor is modulated by dc input amplitude, then the excess noise originates in the voltage reference.

2) If the noise floor is modulated by the input frequency, then there is excessive clock jitter.

3) If the noise floor is not modulated by amplitude or frequency, then the excess noise is present in the input signal. Noise at high frequencies can be aliased into the audio band.

11.0 Conclusions

A number of sensitivities of delta-sigma converters have been explored. Various coupling mechanisms which could excite those sensitivities have been listed. Finally, a list of guidelines is enumerated, which, if followed, will help ensure the best possible performance from delta-sigma converters.

12.0 Acknowledgments

My sincere thanks go to Jeff Scott, Ron Knapp, Eric Swanson and Harold Bogard for their contributions to this paper.

13.0 References

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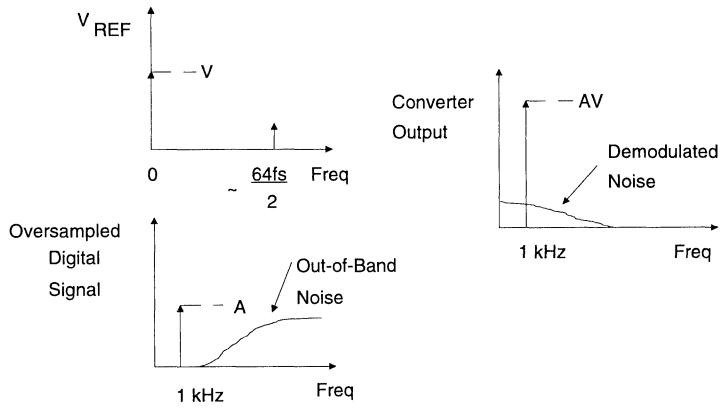

Figure 1. How High Frequency Interference on Vref can Elevate the Noise Floor

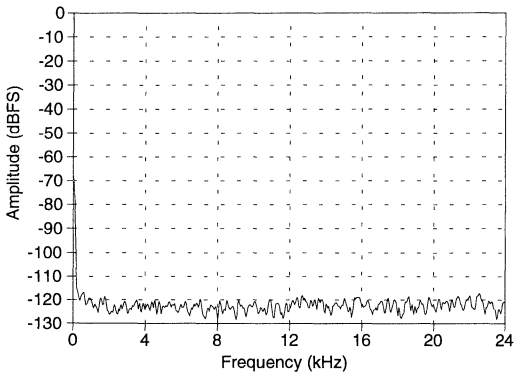

Figure 2a Normal ADC Noise Floor

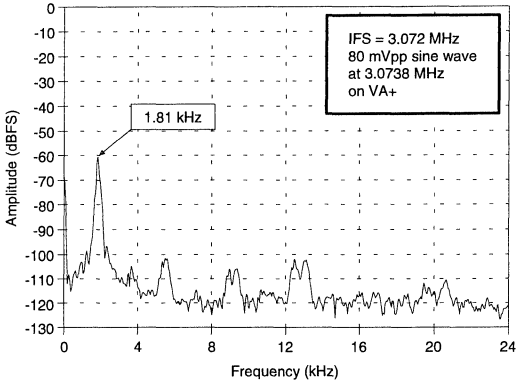

Figure 2b ADC Noise Floor with Power Supply Interference at a Sensitive Frequency

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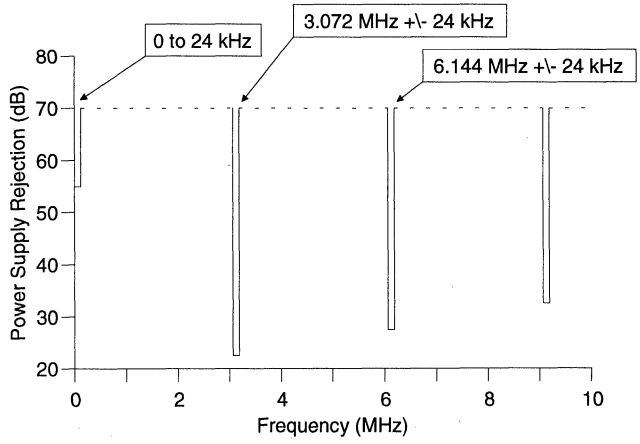

Figure 3. ADC Power Supply Rejection vs. Frequency Showing Sensitive Frequency Windows

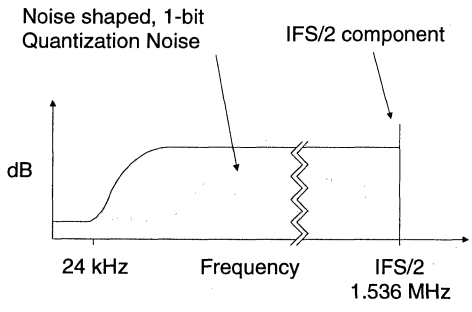

Figure 4. Delta-Sigma Modulator Output Spectrum

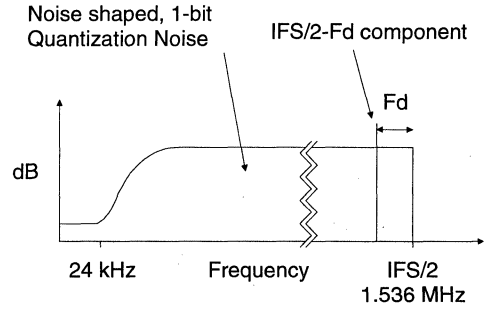

Figure 5. Delta-Sigma Modulator Output Spectrum with a Small dc Offset Applied to the Input

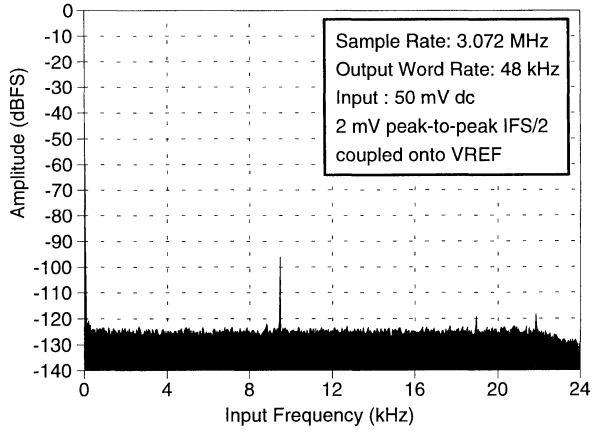

Figure 6. Example of a Tone Caused by IFs/2 Interference on Vref with a Small dc Offset Applied to the Input

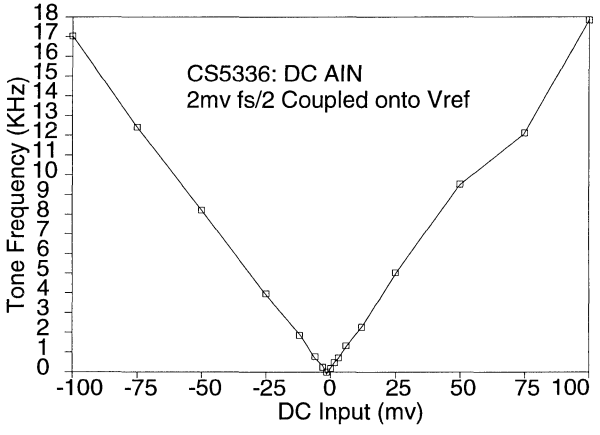

Figure 7. How a IFs/2 Induced Tone Behaves with Varying dc Offset Applied to the Input

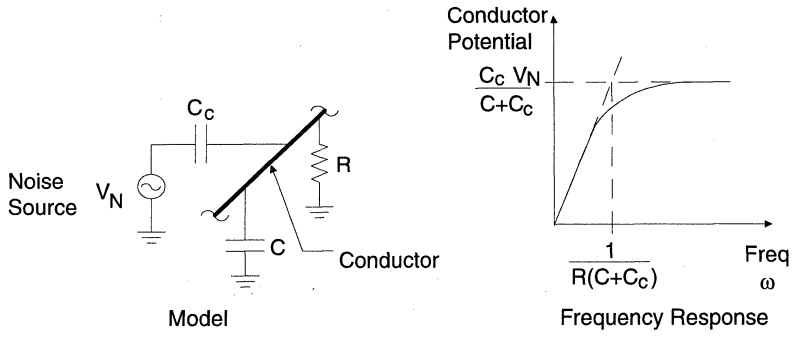

Figure 8. Capacitive Coupling Mechanism

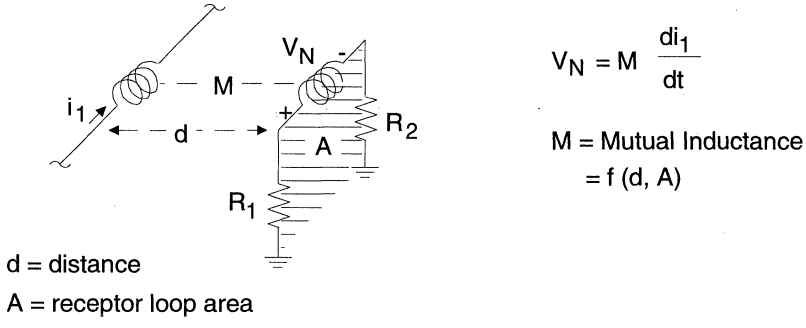

Figure 9. Inductive Coupling Mechanism

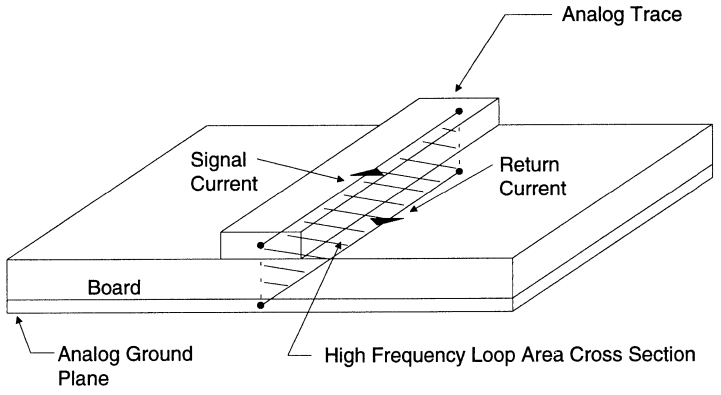

Figure 10. How A Ground Plane Reduces the Loop Area

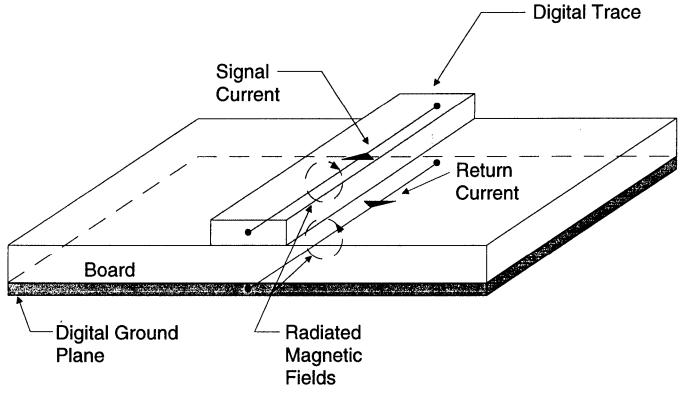

Figure 11. How a Ground Plane Reduces Magnetic Radiation

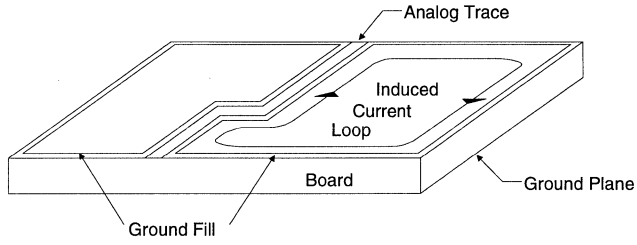

Figure 12. How Ground Plane Fill Acts as a Magnetic Shield

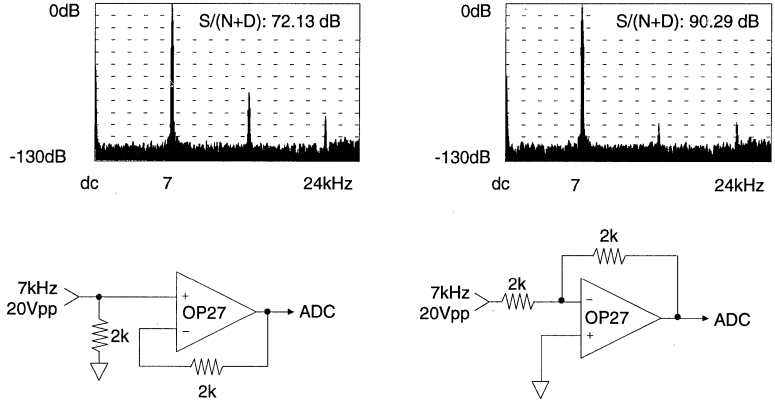

Figure 13. A Non-Inverting Op-Amp Can Cause Distortion

A Single-Chip Stereo 16-bit A/D Converter and Quad 16-bit D/A Converter for Automotive and Consumer Applications

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A single CMOS chip has been realized which includes two 16-bit A/D converters and four 16-bit D/A converters. Also included is an adjustable input gain section, as well as an adjustable output level section. An on-chip PLL allows the device to be clocked by an audio sample rate clock (for example 44.1 kHz). Topics discussed include design trade-offs in filter performance to achieve low cost, and novel techniques used to achieve a low-jitter integrated PLL.

1.0 Device Overview

Delta-sigma analog-to-digital and digital-to-analog converters (ADC's and DAC's) offer the digital audio equipment designer many benefits, including freedom from complex analog anti-aliasing and reconstruction filters, perfect differential non linearity, high integration and low cost. Welland [1] and Sooch [2] papers contain excellent analyses of delta-sigma conversion for both ADC's and DAC's. This paper discusses a combined ADC and DAC device which brings a much greater level of integration to the system designer. This single chip CMOS device contains 2 delta-sigma, 16-bit, ADC's, 4 delta-sigma, 16-bit, DAC's, adjustable input gain stage, adjustable output level stage, a crystal oscillator, a Phase Lock Loop (PLL) and an auxiliary 12-bit ADC. The device has 3 pairs of analog inputs, 1 auxiliary digital input, 4 analog outputs, an audio DSP port and a low speed control port (Figure 1). The device operates from a +5 V power supply.

The intended application for this device is automotive sound systems where each DAC drives one speaker, located in each corner of the automobile interior. Additional applications include low cost surround systems and home theater systems.

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2.0 Input Level Adjustment

A programmable gain block is provided prior to the ADCs. The range of adjustment is 0dB to +46.5 dB in 1.5 dB steps. The gain is adjusted in 2 stages. Firstly, a standard op-amp based stage implements coarse gain steps of 6dB. Secondly, fine gain steps of 1.5dB are implemented by small changes in the value of the input sampling capacitor to the delta-sigma modulator.

Changing the gain of the input circuit at a random time can cause a step function in the output signal. The magnitude of the step function will depend on the instantaneous value of the signal at the time the gain is changed. A series of such gain changes can result in an objectionable audible sound, commonly known as "zipper noise". To overcome this effect, changes in gain are only allowed to occur on zero crossings of the analog signal. This is achieved using a comparator, which monitors the analog signal and compares it to "zero". (Since this device runs from a power supply voltage of +5V, signal zero is actually ~2.5V). If the signal is very small, or has a small DC offset, it is possible that no zero crossings occur. If no zero crossings occur, then the level change is implemented after a time out period of 511 samples (11.6ms at an audio sample rate (Fs)=44.1kHz).

3.0 ADC Architecture

The ADC's use 4th order, switched-capacitor delta-sigma modulators. Capacitor sizes are chosen to yield a dynamic range of 85 dB, while requiring minimum silicon die area. High frequency anti-alias filtering is achieved by including a series resistor on the silicon immediately prior to each modulator sampling capacitor. The modulator side of this resistor is brought out to a pin, where the addition of an external 0.01uF NPO or COG capacitor completes a single pole RC filter. This architecture avoids the need to have an RC filter on each one of the 6 analog input pins, thereby reducing the external component count and complexity.

The modulator is followed by a single stage 1024 tap FIR filter, similar in architecture to [3]. This filter has a passband of DC to 0.454 Fs (-3dB), passband ripple of $<\pm 0.1$dB, and stopband rejection of >75d B. Figures 2, 3 and 4 show the filter response. The filter also includes a "near to clipping" indicator. Bits in the status register are set if the signal is >-6dB, >-3dB and $\geq$0dB (clipping) with respect to full scale. This gives the system designer a low overhead method of detecting an almost clipping situation.

The ADC offset is calibrated by internally zeroing the input signal and noting the output of the digital filter. This output is then subtracted from all future readings to compensate for the modulator offset. This calibration is done after the end of the reset period.

4.0 DAC Architecture

Each of the four DACs consists of a digital interpolation filter, a digital delta sigma modulator and a one-bit DAC feeding a switched capacitor output smoothing filter.

The digital interpolation filter uses the silicon efficient multiplier free architecture previously described by Scott [4], where the Finite Impulse Response (FIR) coefficients are reduced to -1,0,+1. Compact disk de-emphasis can be selected and is implemented by selecting an alternate distribution of -1,0,+1 coefficients for the FIR filter. This avoids the possible truncation and dithering concerns that have plagued Infinite Impulse Response (IIR) digital filter implementations of de-emphasis. The de-emphasis magnitude and phase requirements are accurately realized over the entire audio band. The interpolation filter also compensates for imperfections in the phase response of the analog switched capacitor filter, yielding an overall linear phase response within ±0.5 ° out to 0.45Fs (Figure 5).

The third order digital delta-sigma modulator accepts the interpolated data and outputs a 1-bit data stream at 192Fs or 256Fs. This data stream is then filtered by a 1 pole switched capacitor filter, whose architecture is inherently tolerant of clock jitter [2]. Figures 6, 7 & 8 show the overall response of the DAC. The passband is DC to 0.476Fs (-3dB), the passband ripple is ± 0.1dB and the stopband rejection is >57 dB, with an external 2Fs time constant RC filter.

The DAC outputs are calibrated to yield a low output offset voltage. The uncalibrated DAC offset is measured with the previously calibrated ADC. The digital input value required to achieve zero offset is then stored in an offset calibration register, and is subsequently used to correct all future conversions.

The DAC output mutes after the occurrence of 512 consecutive zeros, yielding a very quiet (-100dB) background noise in the absence of signal. The DAC also has a "hold on error" function. If a digital value is presented to the DAC's that is flagged as invalid, then the output of the DAC will stay held at the previously valid level. This is much better than allowing a potentially damaging full scale excursion through to the DAC. Another possibility is a linear interpolation of up to 8 consecutive erroneous samples [5], however this requires significant die area to achieve. The frequency spectrum of a signal with a held region is similar to the spectrum of a signal with a linear interpolated region, particularly if the region is small, which is the case here. Thus there is little audible difference between hold and linear interpolation.

5.0 Output Level Adjustment

Each of the DAC outputs is followed by an adjustable output level attenuator whose range is 0dB to -117dB in 1.0dB steps. The attenuator is implemented in 2 stages. The first stage is a coarse digital attenuator prior to the DAC. The step size of the coarse attenuator is 6dB, which is implemented simply by shifting the data by one bit location. The fine attenuator (1dB steps) is implemented in

the analog switched capacitor output filter by scaling the capacitor values. The first 32dB of attenuation is implemented entirely by the analog attenuator. This causes the background noise to be attenuated along with the signal, thus the attenuator behaves and sounds like a resistive potential divider type of volume control. Once the analog attenuator has reached -32dB, then the residual noise is so low that subsequent changes made in the digital domain do not cause audible changes in the noise floor.

The output attenuator also implements zero crossing switching, thereby minimizing "zipper noise" in a similar fashion to the input gain stage.

6.0 Clocking Requirements and Phase Locked Loop Architecture

Oversampled converters require high frequency clocks to operate the digital filters and the switched capacitor circuits. As well as the usual pins to attach an external high frequency clock or crystal, an on-chip Phase Locked Loop (PLL) has been provided. This allows the device to lock onto an external audio sample rate clock source, such as a CD transport, and generate the necessary high frequency clocks internally. The latest DSP for audio from Motorola, the 56004, also has an on-chip PLL, thus allowing a system where no external high frequency clocks are present on the circuit board. This reduces radio frequency emissions.

Low clock jitter is important to preserve signal fidelity in ADC's [6]. However PLL's can add jitter, particularly with high multiply ratios. The DAC's require a 256Fs clock, resulting in a X256 multiply ratio from the sample rate clock (Fs) in the PLL. The resulting jitter is primarily the product of VCO phase noise not being filtered by the PLL. How much jitter is acceptable ? Considering only gaussian noise jitter, then the signal to noise ratio (SNR) caused by jitter alone is:

$$SNR_{dB} = 20 \log_{10} (1/(2\pi f\sigma)) \qquad [7]$$

where f = the frequency of the signal (Hz) and σ = the rms jitter amplitude (seconds). The SNR specification for this device is 85 dB. If we assume a worst case audio signal of 0dB (full scale for the converters) at 20kHz, then $\sigma \leq 447$ps to achieve 85 dB SNR. This is a very aggressive target for a X256 PLL, however a 20kHz full scale signal very rarely occurs in actual music signals.

To allow maximum flexibility, the device can be clocked in 3 ways: a) Using a high frequency external crystal oscillator, or using the on-chip high frequency crystal oscillator. This results in negligible clock jitter impact on SNR. b) Using the serial bit clock from a remote audio source. This clock will be at 32 or 64X Fs. The chip's internal PLL will only have to multiply this by 4 or 8, thus introducing minimal extra jitter. c) Using an external word clock at Fs. The internal PLL has to multiply this by 256, thus there is the possibility of introducing jitter which will cause measurable degradation in SNR (with full scale, 20kHz signals). Whether this results in any audible artifacts with music signals is beyond the scope of this paper.

Figure 9 shows the overall clock generation function on the chip. Inputs are a high frequency clock at 256, 384 or 512 Fs, or a serial bit clock at 32 Fs or 64 Fs, or a low frequency clock at Fs. Outputs are a high frequency (256 Fs or 192 Fs) analog quality clock for the DAC's, a medium frequency (64 Fs) analog quality clock for the ADC's, a high frequency (512 Fs) digital quality clock for the DAC interpolation filters and a selection of clocks connected to the CLKOUT pin for driving external devices. To generate the 512 Fs digital clock, a simple delay locked loop (DLL) multiplies the 64 Fs analog clock up to 512 Fs.

The PLL consists of a phase detector, charge pump, loop filter, Voltage Controlled Oscillator (VCO) and divider (Figure 10). The charge pump has a deliberate constant current sink (i_{leak}), which forces the phase detector to always operate in a linear region. Careful choice of i_{leak} removes the "dead zone" problem of the phase detector, while keeping the introduced deterministic phase jitter below that of the random phase jitter introduced by the VCO. The loop filter consists of a 4kohm internal resistor with a 0.2 uF external capacitor to ground. There is an additional 20 pF capacitor close to the input of the VCO. Reference [8] discusses the trade-offs in choosing loop filter components.

Figure 11 shows the VCO design. To minimize pull range for different clock modes, the ring oscillator operates with a variable number of delay elements. For 384Fs clock modes, the VCO is operated at 192Fs and 9 delay elements are used. For 256 & 512 Fs clock modes, the VCO is operated at 256 Fs and 7 delay elements are used.

Two internal inverters are provided for use as the amplifier in a crystal oscillator clock source. One inverter is set up for use with high frequency crystals. The other inverter is set up for use with low frequency crystals (~44.1 kHz). Inverter selection is achieved using a control bit.

7.0 12-bit ADC

An auxiliary 12-bit ADC is provided to allow the background noise inside the automobile to be measured. This allows the possibility of simple output level adjustments based on the ambient noise, as well as more sophisticated noise cancellation algorithms.

The 12-bit converter uses a 2nd order switched capacitor modulator followed by a $sinc^3$ response decimation filter [9]. This filter completely decimates to the same audio sample rate (Fs) as the 16-bit converters. The resolution over 0 to Fs/2 bandwidth is limited to 11.5 bits, but the user may apply subsequent additional filtering to realize higher precision over lower bandwidths. This allows users to customize an external low-pass digital filter to suit their particular requirements. The output noise of the on-chip filter is shown in Figure 12.

8.0 Audio Data Formats

Figure 13 shows the formats for the DAC input data and for the ADC output data. Format 0 is compatible with the I^2S format. Format 1 is compatible with many converters. Format 2 is compatible with many Compact Disc decoders. Format 3 is compatible with general purpose DSP's, where the LRCK signal is a positive pulse at the beginning of each 16-bit word.

9.0 Control Port Formats

The internal operating modes of the device can be set in 3 ways: hardware, SPI compatible serial control port and I^2C compatible serial control port. In hardware mode, only limited functionality is possible; for example, the input gain cannot be changed, and neither can the output level.

Up to 4 devices can be controlled by the same serial control lines. Each chip has its own unique address, which is set by connecting the chip address pins to a particular binary pattern. The SPI and I^2C control modes have a chip address field included in the command protocol. The control port is also compatible with Crystal's Audio Local Area Network (A-LAN) chip, previously described in [10]

10.0 Applications Schematic and Board Layout

Figure 14 shows the recommended connection diagram for the device. Notice the lack of required external components. All the analog inputs and outputs are internally biased to ~0.5 the power supply (+5V), therefore DC blocking capacitors are required if the analog signals are referenced around 0V.

The grounding and layout arrangements around this device must be correct in order to achieve the best performance. Figure 15 shows an overall board layout, with the chip package (44 pin PLCC) mounted over the analog ground plane. Notice that the package is oriented with the digital pins close to the digital section of the board. Figure 16 shows an enlarged view of just the decoupling capacitor arrangements. Notice that the smaller capacitors are shown close to the device package. Harris [11] has previously discussed how to get the best performance from delta sigma converters. Crystal offers a free schematic and layout review service, which is best used before the first prototype is built.

11.0 Specification Summary

Analog Inputs & ADC

ADC resolution	16 bits
Dynamic Range	85dB
THD+N	85dB
Frequency Response	0 to 0.454Fs
Phase response	<0.5°
Input gain	0 to 46.5dB
Step size	1.5dB

DAC & Analog Outputs

DAC resolution	16-bits
Total Dynamic Range	100dB
Instantaneous Dynamic Range	88dB
Frequency Response	0 to 0.476Fs
Phase response	<0.5°
Output Attenuator	0 to 117dB
Step size	1.0dB

Global Specifications

Sample rate	4kHz to 50kHz
Power supply voltage	+5V
Power supply current	120mA
Full scale signal level	1 V_{rms}

All dynamic range specifications are A-weighted. Total dynamic range is the ratio between the full scale output of the chip and the noise floor when maximum attenuation is selected. Instantaneous dynamic range is the DAC dynamic range with the output attenuator set to 0dB.

12.0 Conclusions

A single chip containing two 16-bit ADC's, four 16-bit DAC's, a programmable input gain stage and a programmable output attenuator stage has been presented. This device will allow the next generation of automotive sound systems to be realized in a cost-effective manner. Novel techniques in filter design yield a small die area. The inclusion of a PLL for high frequency clock generation frees the system designer from having to route high frequency clocks around the system.

13.0 References

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[8] "CS5317 data sheet DS27F2, MARCH 1992", Crystal Semiconductor

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[10] D.J. Knapp, H. Hetzel, "Audio Local Area Network Chip for Cars", AES 92nd Convention, Vienna, March 1992.

[11] S. Harris, "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" , AES 93rd Convention, San Francisco,October 1992.

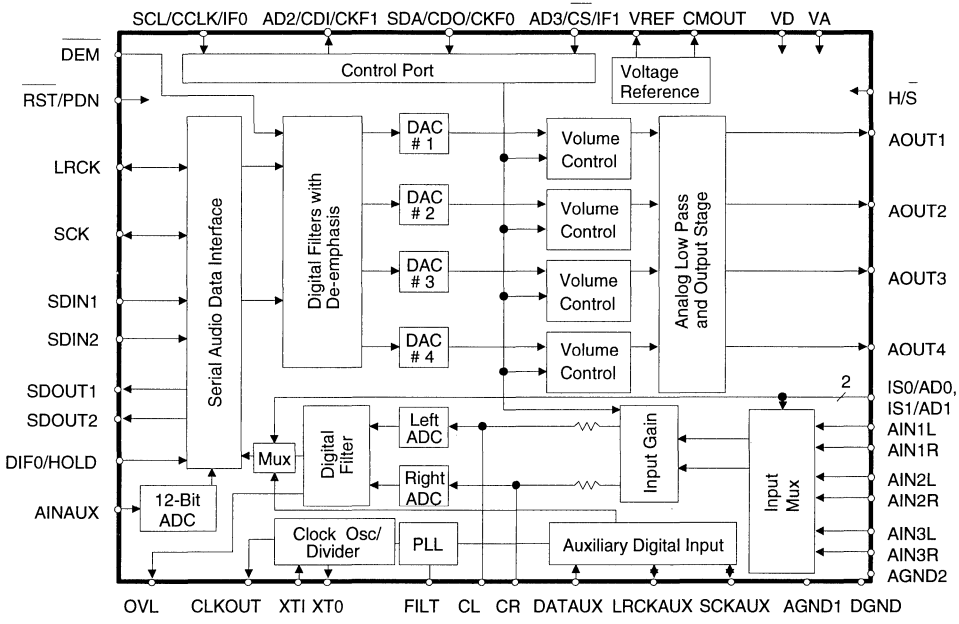

Figure 1. Chip Block Diagram

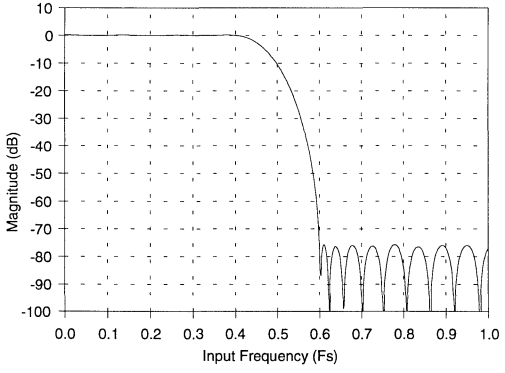

Figure 2. ADC Filter Response

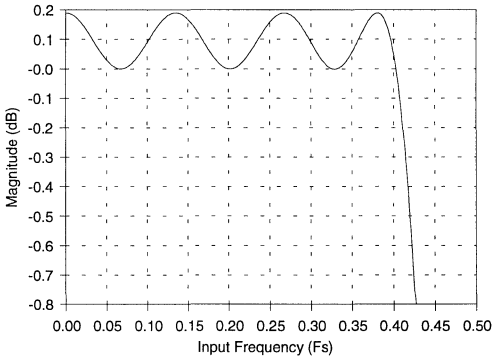

Figure 3. ADC Passband Ripple

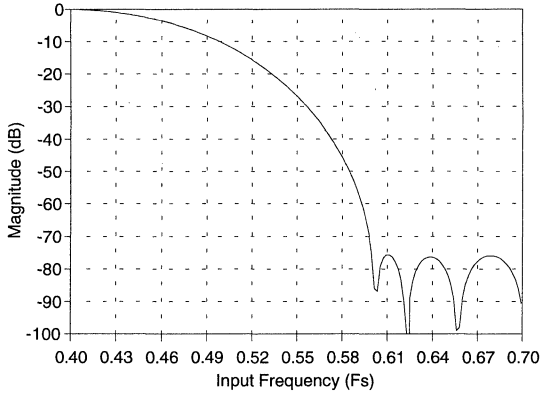

Figure 4. ADC Transition Band

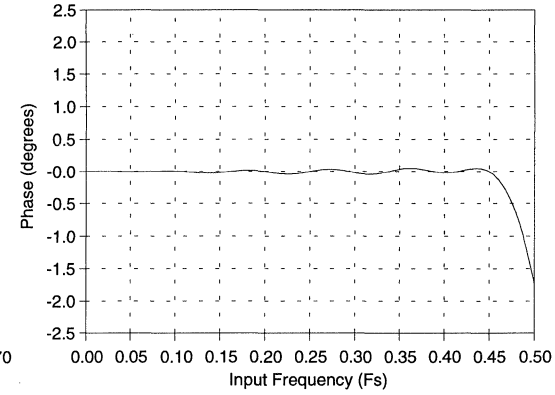

Figure 5. DAC Phase

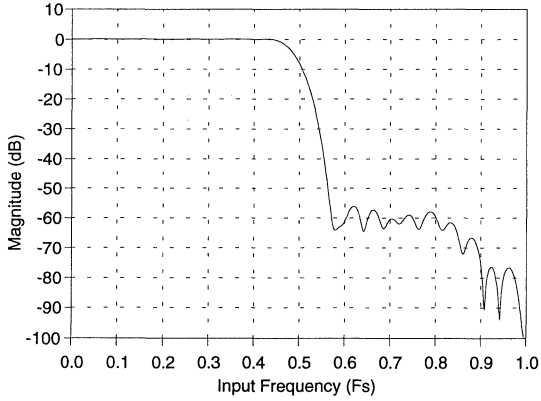

Figure 6. DAC Frequency Response

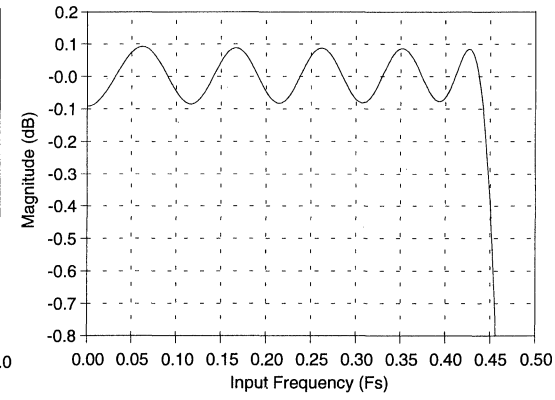

Figure 7. DAC Passband Ripple

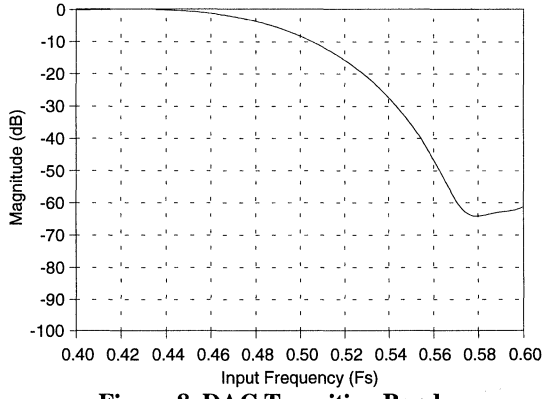

Figure 8. DAC Transition Band

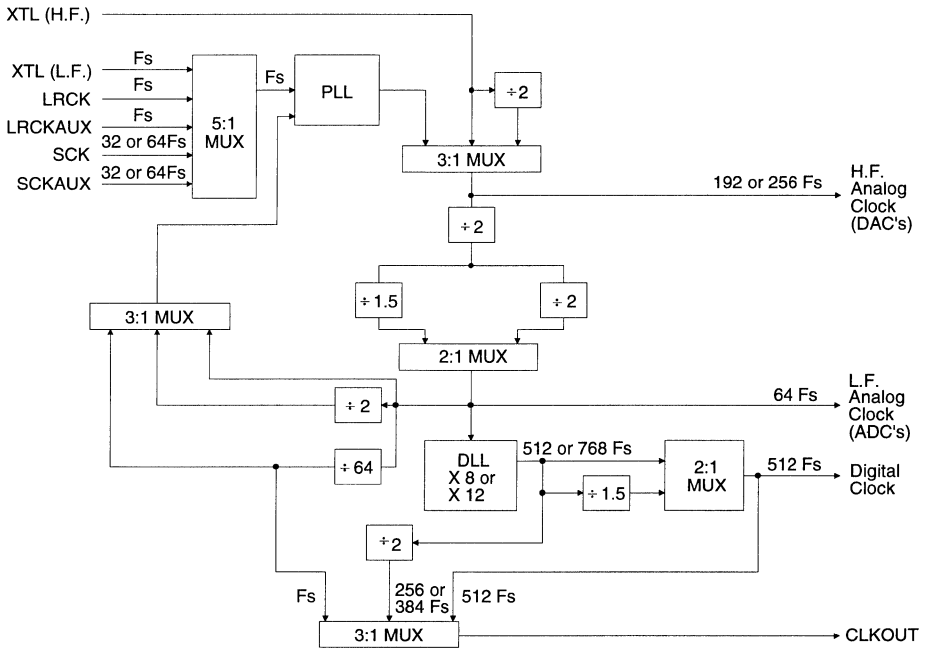

Figure 9. Chip Clock Generation Block Diagram

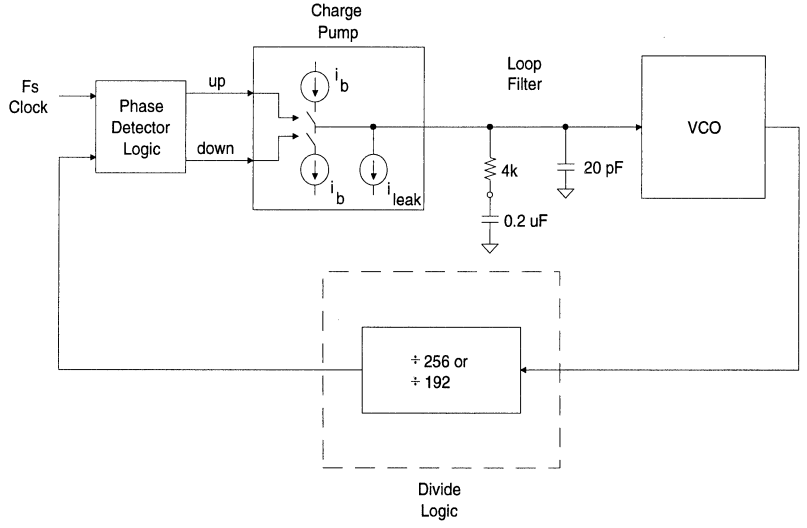

Figure 10. Phase Lock Loop

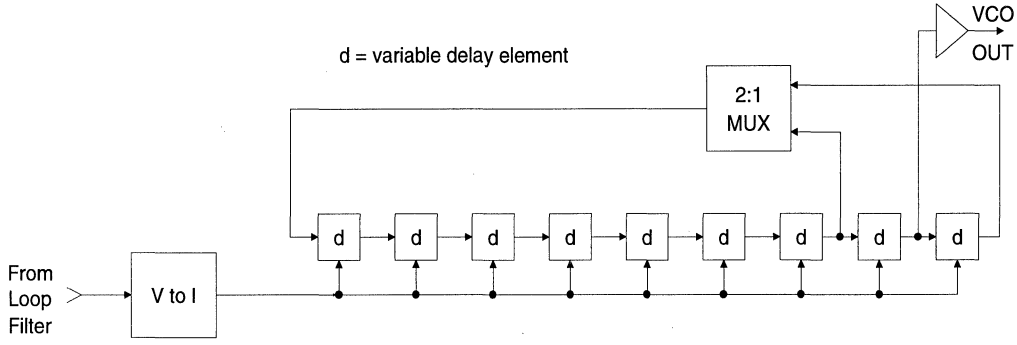

Figure 11. Voltage Controlled Oscillator

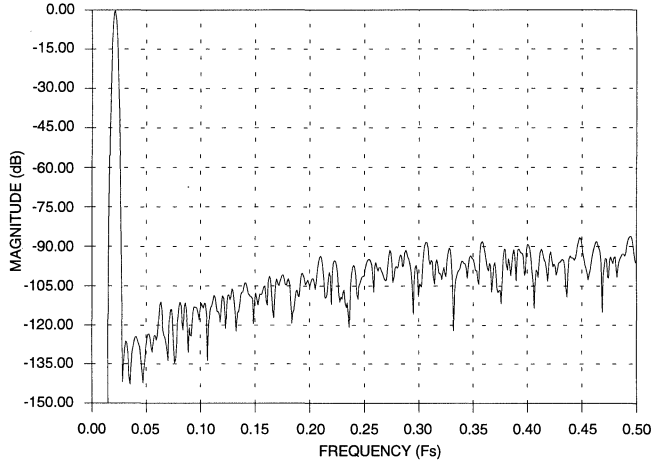

Figure 12. 12-bit ADC Output Spectrum with Full Scale Signal

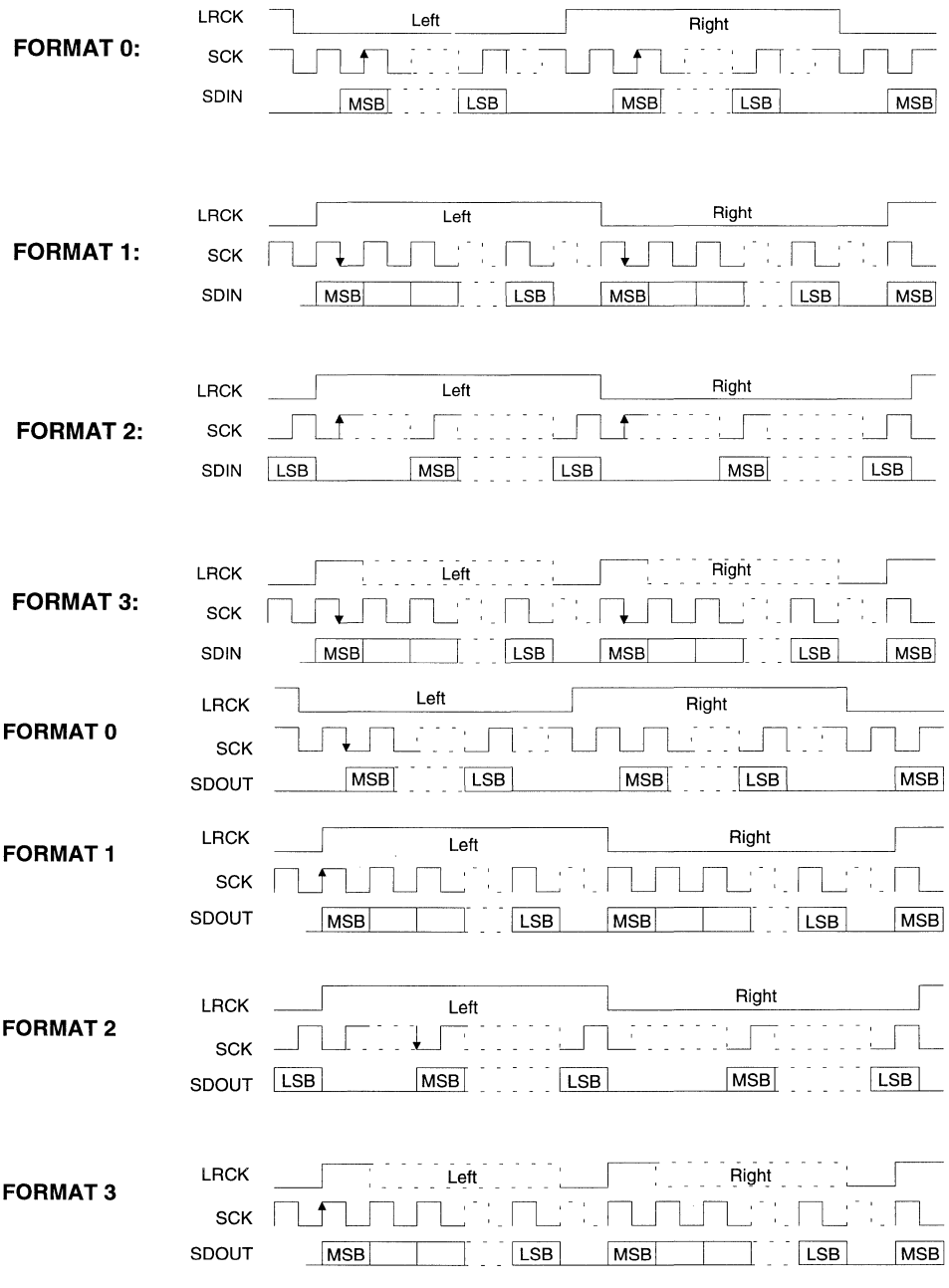

Figure 13. Audio Input and Output Data Formats

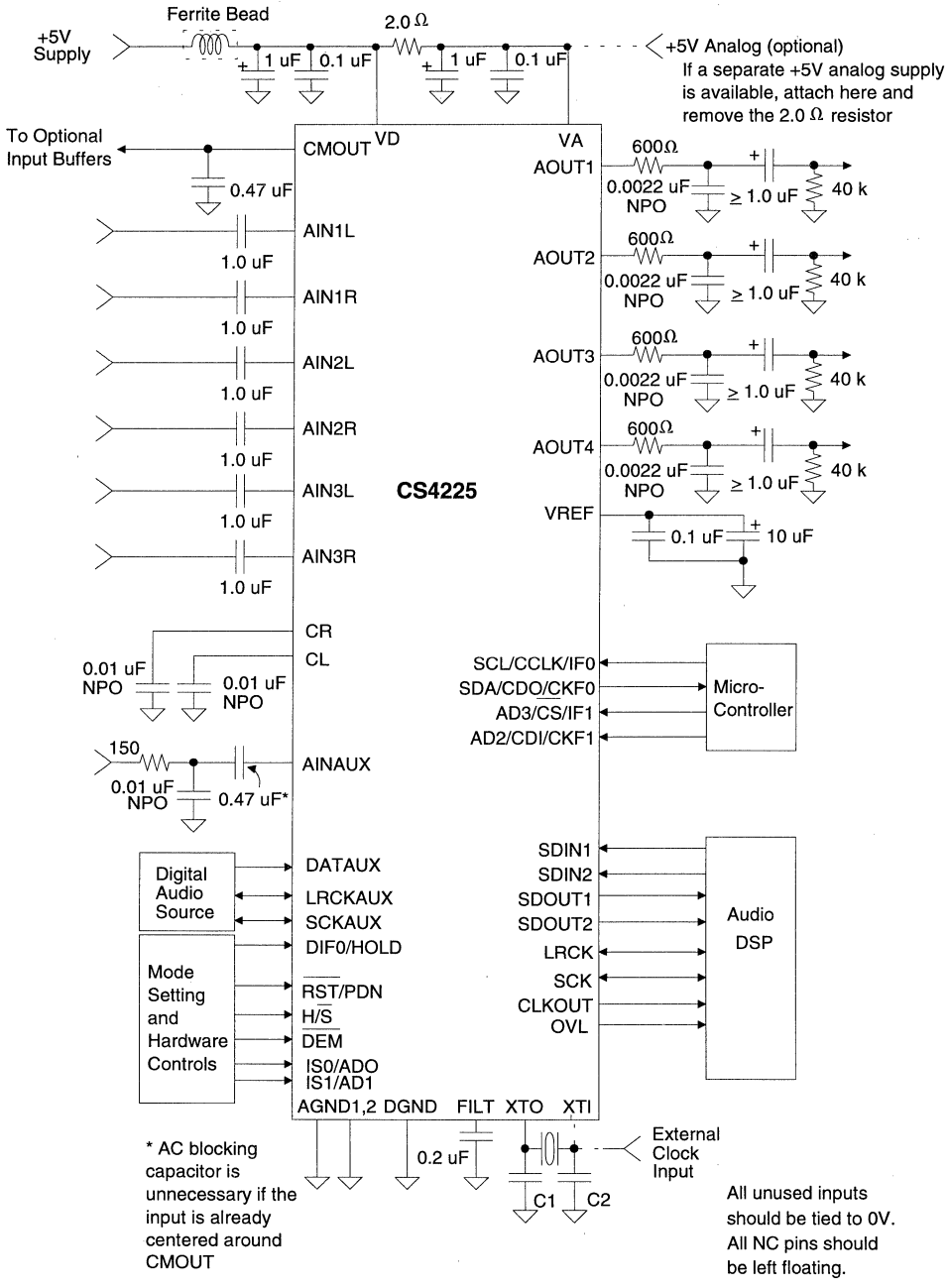

Figure14. External Components

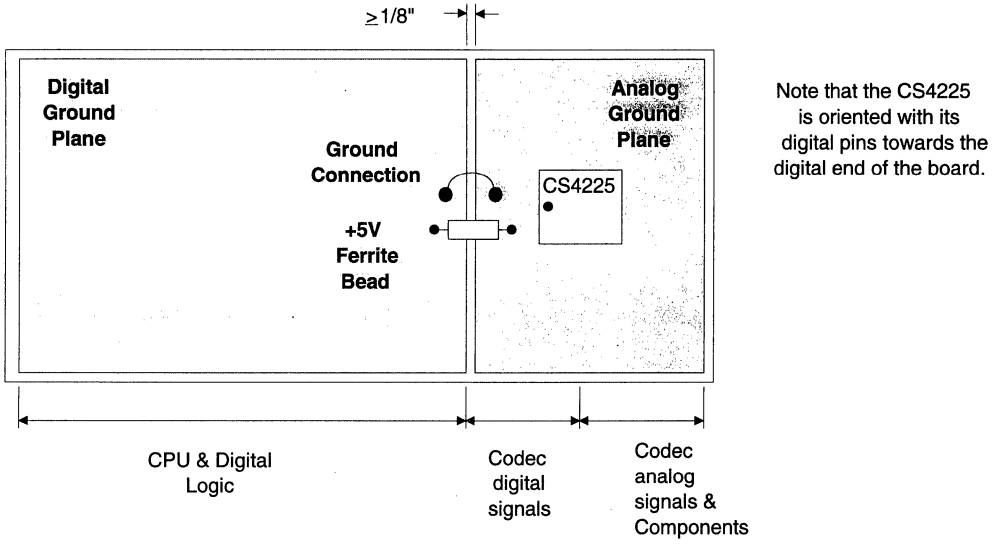

Figure 15. Suggested Layout Guideline

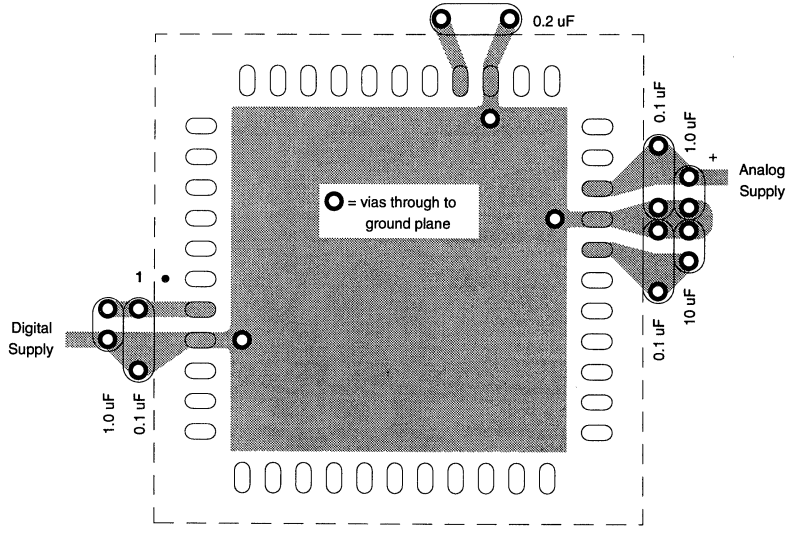

Figure 16. Recommended Decoupling Capacitor Layout

•Notes•

An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission.

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ABSTRACT

The Serial Copy Management System, referred to as SCMS, provides protection from prolific unauthorized digital duplication of copyrighted material. This protection is achieved through the use of channel status bits in the "consumer" digital audio interface standard. Any piece of equipment, either professional or consumer, containing a "consumer" digital audio interface will be required to support the SCMS protocol. This paper explains the SCMS protocol in detail, and presents several easy methods of implementation.

0 INTRODUCTION

With the advent of digital audio and a transmission standard for digital audio [1], [2], the ability to make perfect copies of an original work deprives the recording artist and record companies of potential revenue. The Serial Copy Management System, SCMS, was designed to eliminate unauthorized prolific digital duplication of copyrighted material. The SCMS standard is being added to IEC-958 [1] as Amendment No. 1 [3] and will be required on all consumer interfaces. In the United States, the "Audio Home Recording Act of 1992" [4] was passed by Congress to protect copyrighted works. The Act requires all equipment containing a consumer interface to support the SCMS protocol. This includes - but is not limited to - consumer equipment containing a digital audio interface, professional equipment containing a consumer digital audio interface, and equipment that translates digital audio from one standard to another.

While the standards stipulate that professional equipment containing a consumer interface is required to support the SCMS protocol, professionals owning the copyright and engaging in lawful business are allowed to circumvent the SCMS system.

1 DIGITAL AUDIO INTERFACE OVERVIEW

The digital audio interface provides a means to transmit digital audio information over a single transmission line from one transmitter to one receiver. The transmission consists of timing information, as well as up to 24 bits/channel/sample period, control information, user information, and some error detection capability. The control information is transmitted as one bit per audio sample, with each channel of the stereo signal containing independent control data. The control information accumulates

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in a block structure and contains all the information needed to implement the SCMS protocol. The digital audio data is biphase encoded which allows the receiver to extract a clock from the data. Special biphase codes, defined as preambles, delineate the audio samples.

An audio sample is placed in a structure called a sub-frame. The sub-frame, shown in Figure 1, consists of four bits of preamble, four bits of auxiliary data, twenty bits of audio data, and four individual bits called validity, user, channel status, and parity. A frame consists of two sub-frames and contains channel A and channel B. When the interface is defined for stereo data, channel A is left and channel B is right. As shown in Figure 1, 192 frames are considered a channel status block with the "Z" preamble indicating the start of the block. Since channel status data is independent for each channel, 192 bits, or 24 bytes, make up each channel status block.

The preamble indicates the start of a sub-frame and contains biphase coding violations that render the preamble unique when compared to the rest of the data. These violations enable the digital audio receiver to quickly locate and lock onto the data stream. Three unique preamble codes indicate the start of: a channel A sub-frame, a channel B sub-frame, and a channel status block (which is also the start of a channel A sub-frame).

The next four bits are auxiliary bits and may be used to extend the audio data to 24 bits. Another use of the auxiliary bits in the professional mode is a single coordination signal [2]. This audio signal uses 12-bit words and spans three consecutive sub-frames (4 auxiliary bits per sub-frame).

The next portion of the sub-frame is a 20-bit field for audio data that is transmitted LSB first. As previously mentioned, if the audio data is greater than 20 bits, the auxiliary field may be used to expand the audio data to 24 bits.

V is the validity bit and indicates whether the audio sample is "suitable for conversion to an analog signal." For example, since data must be continually transmitted in the digital audio data stream, if a CD decoder chip has an unrecoverable error, the erroneous data could be sent with the V bit for that sample set, indicating that the data may be corrupted. The receiver, upon receiving the audio data plus the V bit, could try patching the data. Some examples of patching the data include: interpolating through the erroneous data, reusing the last valid sample (which is only 3 dB worse than interpolation), or muting the DACs.

The parity bit, P, at the end of the sub-frame, is a simplistic error detection mechanism defined for even parity; therefore, a sub-frame should always contain an even number of one's. Given a single parity bit, the receiver can only detect when an odd number of bits are in error.

The U bit is defined as the user bit and has no strict definition. This bit gives the interface a user-defined data channel providing flexibility to adapt to different requirements. This flexibility can be seen in some of the uses to date: DCC systems send textual data such as titles and captions in this channel [5]; the AES has defined a protocol which passes messages in this channel using a unidirectional HDLC format [6]; and some systems use the channel as an audio LAN [7] to send messages around a ring of devices in an automotive or home environment.

The most important bit for implementing copy protection is the C or channel status bit. The C bit is strictly defined and contains all the SCMS information in the consumer version of the interface. This bit is unique for each channel and is accumulated over the 192-frame block. The channel status block is delineated by a unique preamble that replaces the preamble indicating channel A once every 192 frames. The channel status block is the same length for professional and consumer interfaces but the bit definitions are different with the exception of the first bit in the block. The first bit indicates whether the rest of the channel status block is defined according to the consumer or the professional format.

2 PROFESSIONAL/CONSUMER DIFFERENCES

The standards for professional and consumer interfaces are very similar and are listed under various organizations and titles as seen in Figure 2. A few digital audio interfaces predate the sub-frame structure previously mentioned. One of the original formats for digital audio communications was based on the internal serial audio bus structure of the Sony PCM-F1 digital audio processor [8]. This interconnect format consisted of three signal pins: a data pin containing two channels, a bit clock, and a word clock indicating the particular channel - left or right. Another early format was SDIF-2 (Sony Digital InterFace) which was used on the PCM1610/1630 transports [8]. The SDIF-2 format also consisted of three signals: left channel data, right channel data, and a word clock. The SDIF-2 format comes closer to the current digital audio interface since it contains 32 bits per word (albeit each word has its own line), and contains control and user bits. This format appears to be where the Copy bit, labeled "Dubbing-prohibition bit", originated.

The main digital interfaces to come after the SDIF-2 format were the S/PDIF (Sony/Philips Digital InterFace) and the AES/EBU specifications. The AES/EBU format [2] was designed for professional use. It became a standard in 1985, and was updated in 1992. The S/PDIF was designed as a consumer format and was included on many early CD players. Both of these digital interface formats were standardized in Japan in 1987 by the EIAJ as the CP-340 *Digital Audio Interface* specification [9]. The AES/EBU professional format was labeled Type I or Broadcast, and the S/PDIF format was labeled Type II or Consumer. In 1989, the International Electrotechnical Commission in Europe issued the same standard under the IEC-958 *Digital Audio Interface* specification [1] with some clarifications. Updates to the IEC-958 standard include the SCMS protocol [3]. The IEC-958 standard is currently the most up-to-date specification for consumer equipment. In October 1992, the United States Congress passed an Act [4] requiring the SCMS protocol on all equipment containing a consumer interface. Other professional organizations such as the CCIR [10] and the EBU [11] have released their own versions of the professional format. Consequently, although digital audio interfaces have many titles, there are basically two formats: professional and consumer.

2.1 Specifications.

In the professional world, digital audio data may need to travel throughout an entire building. In the consumer environment equipment is normally localized in one area, so the distance the digital audio interface needs to traverse is shorter. The professional format is designed to transmit data over a minimum of 100 meters, whereas the consumer format is specified for only 10 meters. The specifications were also designed to use an existing transmission medium. The professional interface uses

balanced, shielded twisted-pair, 110 Ω cable with XLR connectors, i.e. microphone cable. The consumer interface uses single-ended, 75 Ω coax cable with RCA connectors, i.e. home audio cable. Since the professional interface transmits over longer distances, 5 Vpp is typically used, whereas the consumer environment is more concerned with EMI and shorter transmission distances so 0.5 Vpp is used. The consumer standard also allows an optical interface [12] where data is transmitted over fiber optic cable. The most common form of optical connector is the rectangular version listed in [12]. The coding for the channel status block is also different, with the first bit determining whether the rest of the block is defined as professional or consumer.

2.2 Professional Channel Status

Professional channel status is indicated by the first bit in the channel status block being one. The rest of the channel status block differs from the consumer definition. Since professional equipment is designed for use in studios, and the business of professionals is to create and work with copyrighted material, no copy protection scheme exists in the professional environment. The channel status block structure for the professional mode is shown in Figure 3. Since this paper is focused on the SCMS protocol in the consumer interface, detailed definitions for the professional channel status block are omitted. A general purpose guideline for both the professional and consumer interfaces can be found in [13]. The standards containing the professional definition are [1], [2], [9], [10], and [11], with [2] being the most up to date as of the writing of this paper.

2.3 Consumer Channel Status

Consumer channel status is indicated by the first bit, PRO, in the channel status block being zero. This defines the rest of the channel status block as shown in Figure 4. The channel status (CS) block for consumer stereo is usually the same for both left and right channels. When designing a consumer digital audio interface, the following bits must be implemented.

Bit 1, $\overline{\text{Audio}}$, specifies whether the data is audio (0) or non-audio (1). Although the consumer interface was designed to transmit digital audio, C1 provides an indication that digital data replaces the audio data. Bit 2 is the copyright assertion bit which indicates whether the material is copy protected (0) or can be copied freely (1). If C1 is defined as audio data, and C4 and C5 are zero (indicating 2-channel audio) then C3 indicates the audio data has been emphasized. Bits 6 and 7 indicate the mode which defines the interpretation of channel status bytes 1 through 3. The only currently defined mode is 0, C6 = C7 = 00. Channel status bits 8 through 14, defined as the category code, indicate the type of equipment sending the digital audio transmission. The last bit of interest is channel status bit 15, the generation or L bit, which indicates whether the data is original or a copy. A full definition of all the bits in the consumer interface is shown in Figure 5 and can be found in [1], [9], and [13]. The areas of interest to the SCMS protocol are the Copy bit (C2), the Category Code (C8 - C14), and the Generation or L bit (C15).

Bits not defined or defined as reserved must be transmitted as zero for future compatibility. Bit combinations that are not explicitly defined must not be used (i.e. undefined category codes).

3 GENERAL SCMS

The SCMS protocol allows consumers to make copies of a prerecorded, copyrighted work. The original prerecorded work can always be copied, but SCMS will block home recordings of copyrighted material from further copying. The copy of the original work is called a first generation copy. A copy made from the first generation copy is labeled a second generation copy and so on. SCMS allows first generation copies of copyrighted works but prohibits second generation or higher copies. This system gives the consumer the ability to make a copy, change the order, or merge audio thereby conforming the data to the consumer's tastes. It also gives some degree of protection to the copyright owners since the original work is needed to make a copy and any copies of the work (first generation) will be protected.

SCMS uses a combination of channel status bits in the consumer interface to determine if the audio or digital data is copyright protected; and, if copyright protected, then whether the data is an original or a copy.

3.1 Copy Bit - C2

The first bit of interest is the Copy bit which is channel status bit 2 (C2) and indicates whether copyright has been asserted over the material. When Copy = 1, the material is not copyrighted and it may be freely copied. When Copy = 0, copyright is either asserted over the material, or no copyright information is available and copyright is assumed to be asserted.

3.2 Generation Status Bit - C15

The next bit used in the SCMS protocol is the "generation status" or "L" bit and is channel status bit 15 (C15 or byte 1, bit 7) which is used only if copyright is asserted (Copy = 0). The L bit indicates whether the data is original or a copy of an original. Original data is defined as data which is published by or with the authority of the copyright owner, such as commercially released prerecorded compact discs or digital audio tapes. A copy of an original is considered a first generation copy, such as a home recording of a commercially available CD. The Copy and the L bits give the basic information needed to implement the SCMS protocol. The L bit would be simple to use except that the polarity of the L bit changes depending on the type of equipment sending the data.

3.3 Category Codes - Bits C8 - C14

A code defining the type of equipment sending the data is contained in channel status bits 8 through 14 (C8-C14 or byte 1, bits 0-6) and is called "Category Code." The list of defined category codes is shown on the right side of Figure 5. Reserved category codes must not be used. This includes both entire groups (Solid State Memory, 111xxxx, etc.) and combinations not explicitly listed in the specifications. Equipment for which an exact category code does not exist should use the most appropriate, explicitly defined code.

If the category code is Broadcast Reception or Laser-Optical, L = 0 is defined as *original* or commercial prerecorded work, and L = 1 is a *first generation or higher copy*. Broadcast Reception is category code 001xxxx (0111xxx is also Broadcast Reception but is currently reserved) and Laser-Optical is category code 100xxxx. All other category codes reverse the L bit definition, with L = 1 defined as an *original* or commercial prerecorded work, and L = 0 defined as a *first generation or higher copy*. Therefore, in the SCMS protocol, the category code must be used to interpret the meaning of the L bit.

3.4 Exceptions

Two exceptions to the above protocol exist. The first is that two categories are unable to indicate Copy and L bit information. The categories are *General* (0000000) and *A/D Converters without copy protection information* (01100xx). When either of these two categories is received, the received Copy and L bits should be ignored and the receiving equipment must force the Copy bit to 0 (indicating that the work is *copyright protected*) and the L bit to *original* (with the polarity of the L bit determined by the category code of the receiving equipment).

The second exception occurs when receiving data from a CD player, category code 1000000. Since CD players have been around much longer than the SCMS protocol and have already been standardized, the SCMS protocol has to fit into the standard CD format as defined in IEC 908 [14]. Although the Copy bit is defined in IEC 908 [14], the L bit is not. Therefore, a different method is needed to indicate generation status. For this category code (1000000), the Copy bit is used to indicate both copyright and generation status. If Copy = 1, then the disc is *not copyrighted*. If Copy = 0 the disc is *copyright protected* and is *original*. If Copy alternates between 0 and 1 at a 4 to 10 Hz rate then the disc is *copyrighted* and is a *first generation or higher copy*.

4 SCMS IMPLEMENTATIONS

Different types of equipment are required to react differently to the SCMS protocol. This section describes a few category groups and their response to SCMS. Devices which do not store, decode, or interpret the data stream are considered totally transparent from input to output and do not need to implement the SCMS protocol. Examples of this type of equipment are digital amplifiers, digital frequency equalizers, and digital routers. This does not include pass-through equipment (as defined in the next section) configured to pass the input to the output without modification since pass-through equipment decodes the digital audio data stream.

The SCMS protocol specifies that if the copyright status is ambiguous, then the Copy bit should be set to *copyright asserted* (0) and the L bit should be set to *original*. This includes the *General* (0000000) and *A/D Converters without copy protection information* (01100xx) categories, except as noted below for pass-through devices. It is assumed that devices which convert from the professional to the consumer interface fall into this group. Since a professional interface does not include copyright information, the Copy bit should be set to *copyright asserted* (0), and the L bit should be set to *original* in lieu of other inputs to the device indicating copyright status. Since this is only an interpretation of the specifications, the specifications may later show that conversion between professional and consumer interfaces is not allowed.

The *General* category code (0000000) was used in older equipment that did not fully support the Consumer interface. Any SCMS device receiving the *General* category should force the Copy bit to 0 (*copyright protected*) and the L bit to *original*. For example, the *General* category was used in some Japanese digital audio broadcast receivers that did not include any copyright information. The *General* category should not be used in newly designed equipment. The *Experimental* category should be used in experimental equipment that is not commercially available.

4.1 Pass-Through Devices

Pass-through devices receive and decode a digital input, then encode and transmit a digital output without a permanent storage ability. These devices come under the category code of *Digital-to-Digital Converters*, 010xxxx. For digital-to-digital converters, if ALL digital inputs come from the category code *A/D Converters without copyright information* (01100xx), then the category code at the digital audio output may remain at 01100xx. This category allows an extra generation copy since the receiving device should respond to this category code by setting the Copy bit to *copyright asserted* and the L bit to *original*. If the pass-through device uses its own category code, it must set the Copy bit to *copyright asserted* and the L bit to *original*. Then the receiving device will change the L bit to indicate *first generation or higher*, and no more copies will be allowed. If the digital input contains any category code other than 01100xx, the pass-through device must use its own category code, 010xxxx, and interpret and output the Copy and L bits appropriately, regardless of whether the device is configured to modify the incoming data or not.

4.1.1 Digital Sound Samplers

Digital Sound Samplers, category code 0100010, sample portions of a digital input and assemble the digital samples into one or more digital outputs. The standard rules of SCMS for pass-through devices must be applied if ANY digital input is sampled for more than one second.

4.1.2 Digital Signal Mixers

Digital signal mixers, category code 0100100, mix one or more digital inputs and output one or more digital outputs. The exception listed above for A/D converters with category codes 01100xx applies only if ALL inputs are from that category. If ANY input has the Copy bit set to *copyright asserted*, then the digital output must set the Copy bit to *copyright asserted* with the exception of category codes 0000000 and 01100xx as previously mentioned. Also, if ANY input has the Copy bit set to *copyright asserted* and the L bit set to *first generation or higher*, then the output must also be set to *first generation or higher*. Therefore, a digital audio output must contain the highest level of protection of any one of the digital audio inputs used to create that output.

4.2 Digital Audio Recorders

Digital audio recorders, DARs, are defined as devices that can store data for later retrieval. This includes the *Laser-Optical* category (100xxxx) and *Magnetic Media* category (110xxxx) with the exception of the DAT category code 1100000 which is discussed in *Section 4.3*. Although *Solid State Memory* (0001xxx) could be considered a digital audio recorder, this entire category code group is reserved and cannot be used.

Digital audio recorders should store channel status information pertinent to the data, such as the Professional/Consumer, Audio/Non-audio, and Emphasis bits. When the data received from a digital audio interface is in the consumer format, the DAR must store the Copy and L bits as per the SCMS standard. This information will be needed by devices receiving the recorded data from the DAR. The only exception is the CD category of 1000000 which cannot store the L bit and was previously described in *Section 3.4.* When recording from an internal A/D converter, information regarding the copyright status of the analog signal is usually unavailable. In this scenario the DAR should interpret the data as if it were coming from category code 0110000, *A/D Converters without copyright information*, unless explicit copyright information is available. Therefore, the data is assumed *copyright protected* and *original.*

DARs designed exclusively for receiving the consumer digital audio interface should not store data received from a professional device. DARs capable of receiving both professional and consumer interfaces must be able to distinguish between the two. Although not explicitly stated in the standards, if no copyright information exists when converting a professional interface to a consumer interface, the data should be assumed *copyright protected* and *original.* Part of the conversion should include other channel status information such as Audio/Non-audio, Emphasis, and Sample frequency.

4.3 Digital Audio Tape Recorders

Consumer digital audio tape recorders, DATRs, containing the SCMS protocol have an explicitly defined algorithm as defined in [15]. Professionals using consumer DAT players need to understand how the DATR will respond to an incoming digital audio transmission. This algorithm is illustrated in Figure 6 and describes the order of questions to be asked, whether the data can be stored on the DAT recorder, and if the data can be stored, the setting of the Copy and L bits to be stored with the data.

The SCMS protocol for DATRs applies to consumer interfaces (PRO = 0) containing audio data ($\overline{\text{Audio}}$ = 0). If either of the first two channel status bits are not zero (either professional or Non-audio), then the DATR should not store the data onto tape. If the category code is undefined, the DATR stores the data and assumes the data is *copyright protected* and a *first generation or higher* (i.e. *not original*). Since this data is stored as *not original*, no further copies can be made from this tape. If the category code is *General* or *A/D Converters without copyright information*, then the DATR stores the data and assumes the data is *copyright protected* and an *original.* Since this data is stored as *original*, a copy of this recording can be made through the digital audio output. If the category code is *CD compatible with IEC-908* (1000000), and the Copy bit is alternating between 4 and 10 Hz, then the received data is coming from a home-recorded (*not original*) CD and the DATR should not store the data onto tape.

At this point in the algorithm, the Copy and L bits are assumed to be implemented accurately. If the Copy bit indicates that copyright has not been asserted, the data is stored on tape and limitless copies can be made through the digital audio interface. If the Copy bit is set to *copyright asserted*, then the L bit must be used to determine if the incoming information is original, or a copy of original data. If the L bit is set to *first generation or higher*, the DATR will not store the data on tape. If the incoming data is designated *original*, the DATR will store the data and store an indication that the data is *copyright protected* and *not original* (a copy). Therefore, no further copies can be made from this recording.

When the DATR is recording from its internal A/D converter, it responds as if the data were coming from the *A/D Converters without copyright information* category (01100xx) and sets the Copy bit to *copyright asserted* and the L bit to *original.*

5 CIRCUITS TO ACCOMPLISH SCMS

There are numerous ways to implement the SCMS protocol. Systems containing processors could use digital audio transmitters and receivers that attach to the processor's bus as peripherals. Using this approach, the SCMS protocol could be implemented through software on the processor. Systems without processors could use stand-alone transmitters and receivers with external decode logic to implement the SCMS protocol. The decode logic described below is implemented using 16V8 programmable logic devices (PLDs) for ease of use. Even though these PLDs are fairly inexpensive, the designs can be converted to even lower cost PLDs such as 16R4s or 16R8s. Separate circuits are used to implement each section of the SCMS protocol. In this way, only the circuits needed for a particular application have to be implemented. Also, the circuits described below could be combined into larger PLDs for a lower chip count, albeit usually at a higher cost. All files used to program the PLDs are listed at the end of this paper.

5.1 Transmitters

If the system contains a processor, then the CS8401 Digital Audio Transmitter [16] can be attached to the processor's parallel bus as a peripheral (as shown in Figure 7). The CS8401 internally buffers an entire block of channel status data (24 bytes) allowing all channel status bits to be controlled by the processor. Since the internal buffer is circular, the processor only needs to write the channel status data when a change is desired. Using the CS8401, the SCMS algorithm is written entirely in software on the processor.

The CS8402 Digital Audio Transmitter [16] is a stand-alone transmitter that does not need a processor to implement a digital audio interface. To keep the cost of the CS8402 low, only the most important channel status bits are available on pins. The other channel status bits can, if desired, be entered through the C input pin. The channel status bits available on pins are logically OR'ed at the proper time to the data entered on the C pin. One of the channel status pins - $\overline{\text{PRO}}$, which is the Professional/Consumer bit - C0, determines the function of the other five channel status pins. When $\overline{\text{PRO}}$ = 1 (consumer) the channel status pins of interest to the SCMS protocol are $\overline{\text{C2}}$ (Copy), $\overline{\text{C15}}$ (L), and $\overline{\text{C8}}$/$\overline{\text{C9}}$ (two MSBs of the category code). If any of the other category code bits (C10-C14) need to be set, they must be entered on the general purpose channel status input pin C. Figure 8 illustrates a simple method of entering channel status bits C10 through C14 using an inexpensive 16V8 labeled TX_CAT. The CBL pin output from the CS8402 indicates the start of the channel status block. This PLD counts up from CBL rising to the proper location of C10 through C14 at which time the C10 through C14 inputs to the PLD are multiplexed onto the C pin.

Although TX_CAT gets the extra category code bits from pins, the category code bits could be internally generated allowing for future software updates by reprogramming the PLD. The equation for COUT can be modified so that the terms used to create COUT consist only of the counter values when a "1" in the category code is desired. This method is illustrated at the end of the TX_CAT.PDS file in commented form.

5.2 Receivers

When a processor is available, the CS8411 Digital Audio Receiver [17] provides the most flexible approach to implementing the SCMS protocol. The CS8411 internally holds an entire block of channel status data (24 bytes). This receiver can also interrupt the host processor if any of the important data in bytes 0 to 3 change, thereby greatly reducing the processor overhead. Since the SCMS protocol is implemented entirely in software, any changes to the specifications become a software update. The CS8411 circuit is illustrated in Figure 9.

The CS8412 Digital Audio Receiver [17] is a stand-alone receiver that does not require a processor to implement the digital audio interface standards. All channel status bits are serially output from the C pin. The start of the channel status block is indicated on the CBL pin which can be used to locate the channel status bits of interest. The CS8412 also outputs six of the most important channel status bits, recovered from the received digital audio data, to pins. These pins are multiplexed with error and frequency information. Although the pins do not need to be dedicated for channel status, the following circuits assume the multiplexed pins are in the channel status mode while CBL is high.

The $\overline{C0}$ output contains the first channel status bit (PRO) and determines the function of the other five outputs. When $\overline{C0}$ = 1, the data received is from a consumer interface and the other five pins are defined as: Ca = $\overline{C1}$ = Audio/Non-audio, Cb = $\overline{C2}$ = Copyright asserted/Copyright not asserted, Cc = $\overline{C3}$ = No Emphasis/Emphasis Added, Cd = $\overline{ORIG}$ = Original/Copy, Ce = $\overline{IGCAT}$ = 0000000 or 01100xx category codes/all other category codes. The last two pins, $\overline{ORIG}$ and $\overline{IGCAT}$, are decoded channel status bits. $\overline{ORIG}$ is a decoded version of the L bit. Since the L bit definition is inverted for certain category codes, $\overline{ORIG}$ takes the category codes into account such that $\overline{ORIG}$ is always low if the L bit indicates *original*. There are two category codes that cannot indicate copyright status: *General* - 0000000, and *A/D Converters without copyright information* - 01100xx. When either of these categories is received, the Copy and L bits should be ignored and the Copy bit forced to *copyright asserted* and the L bit to *original*. $\overline{IGCAT}$ is low when the incoming channel status indicates either of these two category codes, thereby giving the system the ability to act accordingly.

The amount of information needed to implement the SCMS protocol varies based on the type of equipment being designed (category codes). Although the CS8412 does some decoding in the $\overline{ORIG}$ and $\overline{IGCAT}$ pins, more decoding is necessary to implement the entire SCMS protocol. The following circuits are divided into three sections that can be optionally implemented based on the type of equipment being designed. The three circuits are labeled: CONVERT, which fully decodes the Copy and L bits and indicates when data storage is prohibited; RX_CAT, which indicates when an unknown category code has been received; and CD_DECOD, which checks for the Copy bit alternating at a frequency of 4 to 10 Hz indicating that the data received is from a CD player and is *not original* (a copy or *first generation or higher*).

The first CS8412 circuit, shown in Figure 10, uses one 16V8 PLD labeled CONVERT, and provides the following fully decoded SCMS outputs: $\overline{C2}$, $\overline{C15}$, and COPYPROH. $\overline{C2}$ indicates the Copy bit, $\overline{C15}$ indicates the generation status or L bit, and COPYPROH high indicates that the incoming data should not be stored. If either the "unknown category code" or "CD copy" circuits are not implemented, the corresponding inputs, UNKCAT and CDCOPY respectively, should be tied low. The CBLD output is only needed if the CD_DECOD circuit is used. Since extra space is available in the PLD, other

channel status bits provided by the CS8412 ($\overline{C0}$, $\overline{C1}$, and $\overline{C3}$) are latched for convenience. This allows the CS8412 channel status pins to be used for error and frequency reporting when CBL is low.

The second CS8412 circuit, shown in Figure 11, is labeled CD_DECOD and checks for the Copy bit (C2) alternating between 0 and 1 at a 4 to 10 Hz rate. This circuit is also comprised of one 16V8 PLD. If available, the category code received should be input to the PLD; otherwise, the C8 through C14 pins should be set to the CD category code (1000000) since this is the only category where the Copy bit can alternate. Since the frequency of the Copy bit is extremely low, CBL, which only rises once every 192 frames, is used as an input to the internal counter which divides CBL by 32. Then CD_DECOD checks for a transition from 0-to-1 or 1-to-0. The CDCOPY output is updated at the end of the counting interval and is set high if a transition occurred at any time during the interval.

The third CS8412 circuit, shown in Figure 12, is labeled RX_CAT and checks for a valid category code. This circuit is comprised of two ICs: an HCT595 shift register and latch, and a 16V8 PLD. The HCT595 shift register continually loads channel status bits from the C pin. RX_CAT counts channel status bits from the start of the channel status block (CBL going high) and signals the HCT595 to latch the category code. RX_CAT then compares the latched category code to an internal list of valid category codes and the UNKCAT output goes high if the category code is undefined. As the standards are updated and new category codes are defined, RX_CAT can be reprogrammed to include the new category codes.

5.3 Transceivers

The CS8401 transmitter shown in Figure 7, and the CS8411 receiver shown in Figure 9 can be connected together on the same bus with different decodes for the chip selects ($\overline{RD}$ and $\overline{WR}$). This arrangement gives the processor total control of the SCMS protocol, since each chip stores an entire block of channel status data.

The CS8412 receiver and the CS8402A transmitter can be combined with minor changes to the PLDs. For example, Figure 13 illustrates a digital audio transceiver circuit that implements the entire SCMS protocol for a pass-through device. Support for the professional interface has also been included. The previous PLD used to transmit category codes (TX_CAT) has been modified (and renamed TX_CAT2) to allow professional channel status to pass from the receiver to the transmitter unhindered. When receiving the consumer format, TX_CAT2 loads the entire device category code from inside the PLD and the $\overline{C8}$ and $\overline{C9}$ pins on the CS8402A are not used. When the *A/D Converters without copyright information* (01100xx) category code is received, TX_CAT2 transmits the same category code (IGCAT and C9 indicate that particular category code). Since this PLD has to count from CBL rising to get the category code locations and since there are extra inputs on TX_CAT2, C1 from the receiver is input to the PLD and multiplexed into the channel status output COUT at the proper time.

The second PLD changed for the CS8412/02A transceiver circuit is RX_CAT which verifies the category code received from the CS8412. This receiver PLD has been changed from a 16V8 to a 22V10 PLD to allow for professional mode support. The new PLD, labeled RX_CAT2, still decodes unused categories, and also decodes sample frequency pins FC1 and FC0 on the CS8402A. The sample frequency channel status bits are C24 and C25 which are received by RX_CAT2 and encoded onto the FC1 and FC0 pins. When a received digital audio interface indicates the professional format ($\overline{C0}$ = 0),

FC1 is set high, placing the CS8402A in transparent mode and TX_CAT2 allows the received channel status to flow through to the transmitter. A MODE0 output is also included on RX_CAT2 since extra space is available. This output should always be high since Mode = 0 is the only mode defined in the consumer interface. Since this transceiver circuit is designed for a pass-through device and unknown category codes are not supposed to be used (according to the digital audio interface standards), the category code portion, along with the HCT595, could be eliminated and the PLD changed back to a 16V8.

The CS8425 [7] is a digital audio transceiver that supports both a software/peripheral and a hardware/stand-alone mode. Although the CS8425 is designed primarily for the consumer interface, the professional interface can be minimally supported. The CS8425 can be configured to run the transmitter and receiver independently, or to lock the transmitter to the receiver. When using the CS8425 with a processor (see Figure 14), the CS8425 stores two bytes worth of channel status for both the transmitter and the receiver including all the bits necessary to implement the SCMS protocol. The channel status bits stored are C0-C4, C8-C15, C24, and C25 and are illustrated in Figure 15.

The CS8425 can be configured as a stand-alone transceiver that does not need a processor. In this mode channel status bits can be entered/received through a serial port, but no decoded parallel bits are available as in the CS8402 transmitter and the CS8412 receiver. Therefore, more decode logic would be needed to support the full SCMS protocol.

6 CONCLUSION

This paper is intended as a guide to understanding the SCMS protocol. A detailed view of the SCMS protocol as well as an overview of the digital audio transmission standards and differences have been presented. Circuits to implement the SCMS protocol were also presented to aid in the understanding of the requirements of an SCMS equipped digital audio system.

Although every effort has been made to verify the data presented in this paper, some of the specifications are ambiguous for certain applications and some specifications are still in the draft stage. The standards are subject to revision and could be amended at any time. Also, this paper does not address the royalty provisions listed in some specifications [4]. Those wishing to guarantee compliance should obtain the latest standards information from the appropriate standards organizations.

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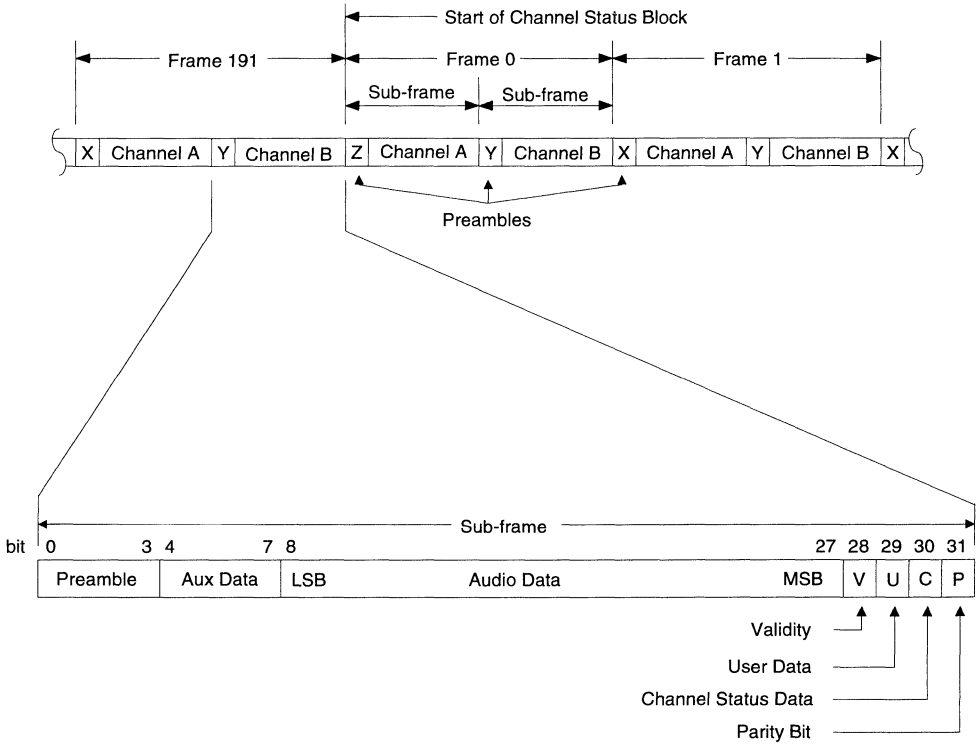

Figure 1. Digital Audio Transmission Format

Professional		Consumer
	Standards	
AES3-1992		S/PDIF
CP-340: Type I		CP-340 Type-II
IEC-958 Broadcast		IEC-958 Consumer
CCIR 647		
EBU 3250		
	Hardware	
5 Vpp		0.5 Vpp
Balanced		Single Ended
110 Ω Twisted Pair		75 Ω Coax
XLR Connectors		RCA/Phono or Optical
	Software	
Channel Status Bits		Channel Status Bits

Figure 2. Professional/Consumer Differences

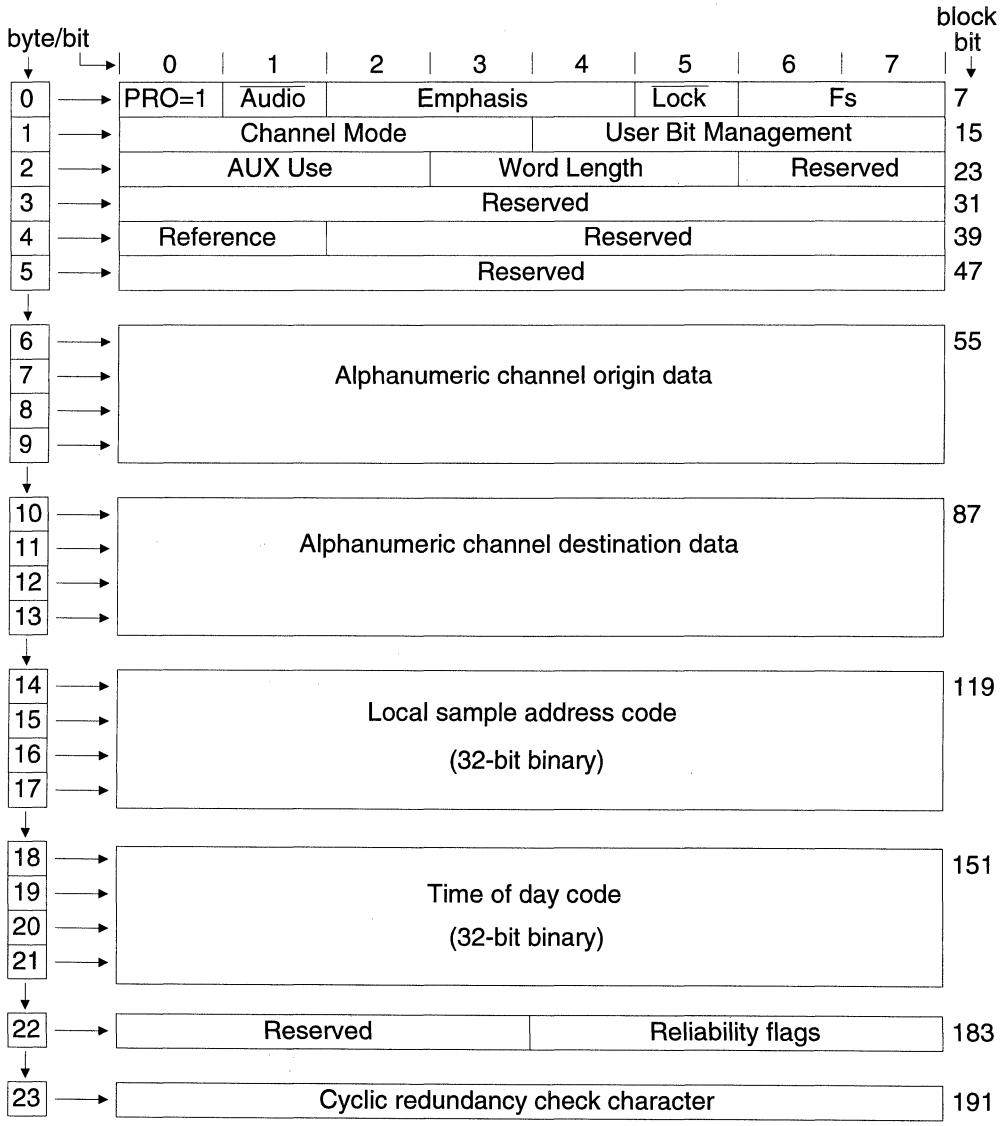

Figure 3. Professional Channel Status Block Structure

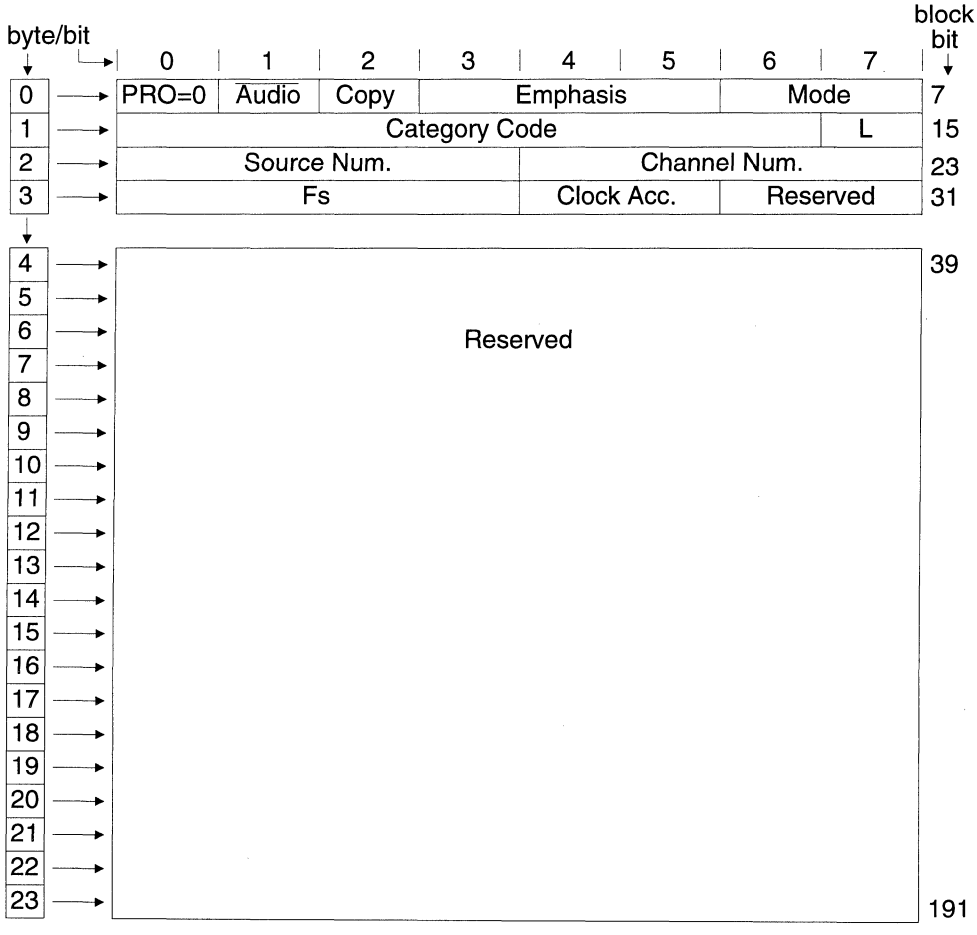

Figure 4. Consumer Channel Status Block Structure

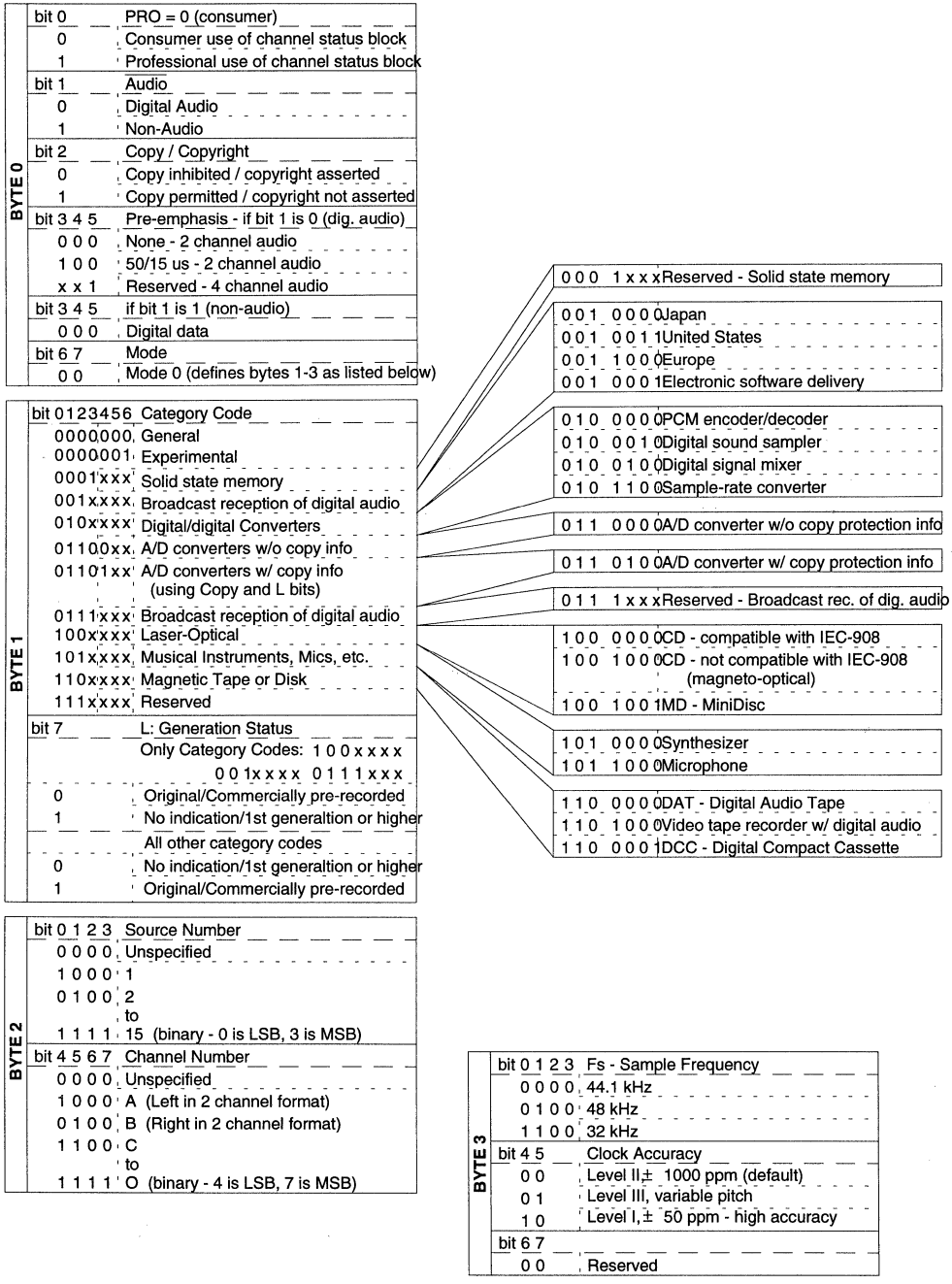

Figure 5. Consumer Channel Status Details

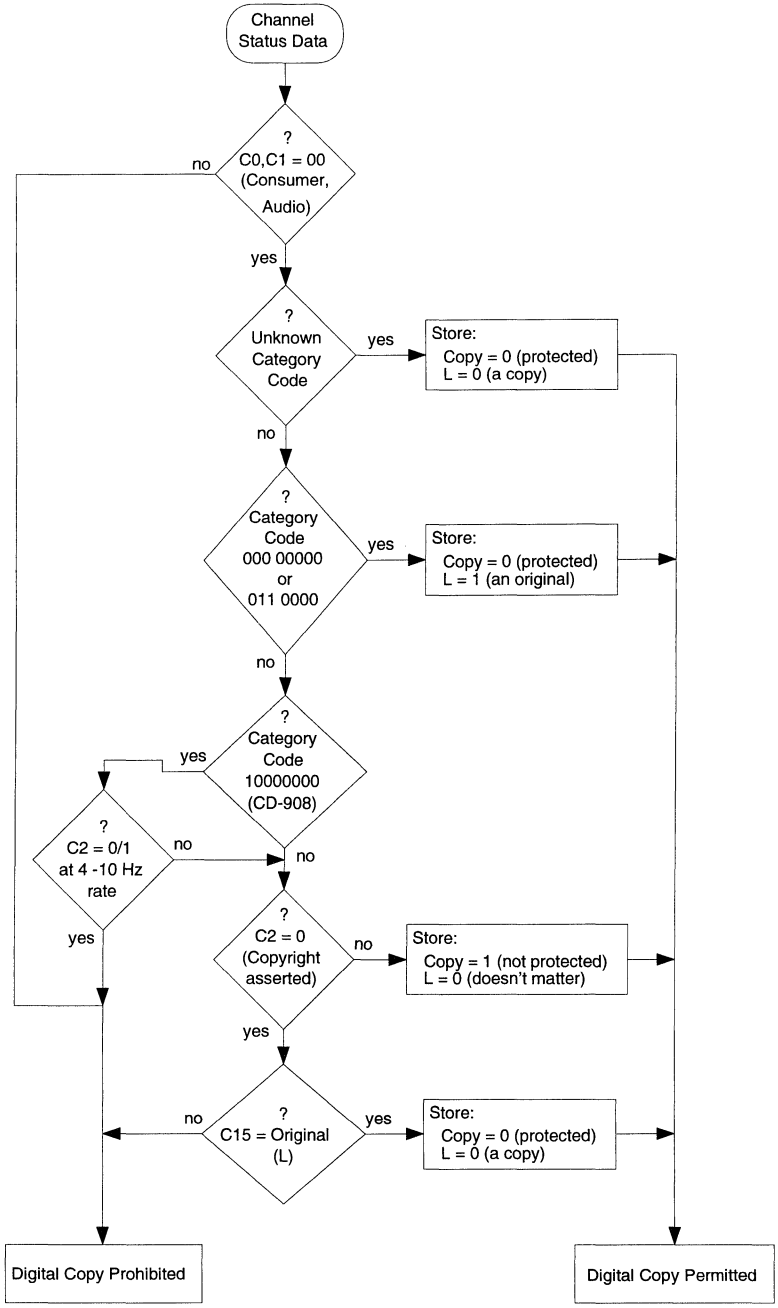

Figure 6. DAT SCMS Response

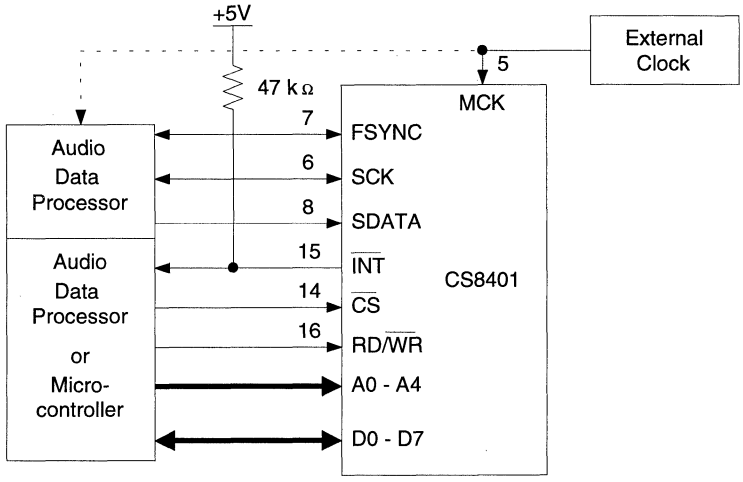

Figure 7. CS8401 Transmitter, Software SCMS

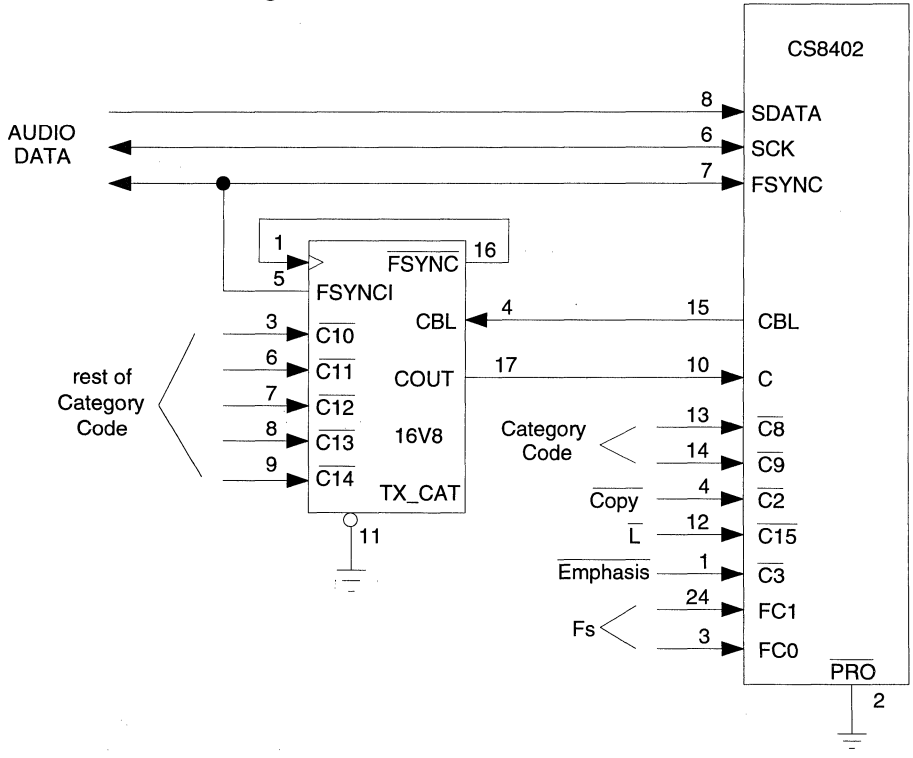

Figure 8. CS8402 Transmitter - Category Codes

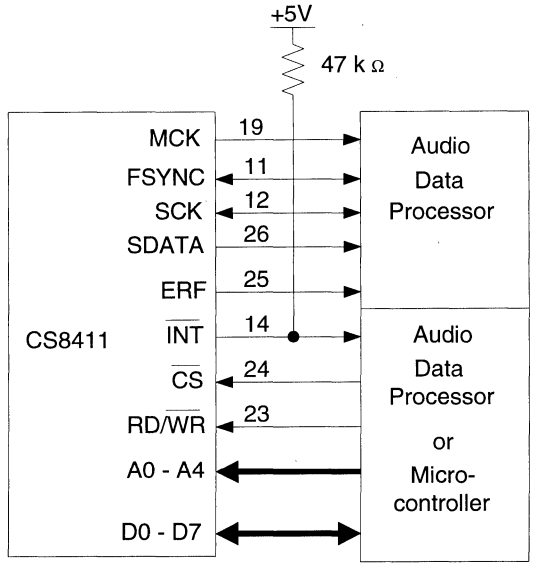

Figure 9. CS8411 Receiver, Software SCMS

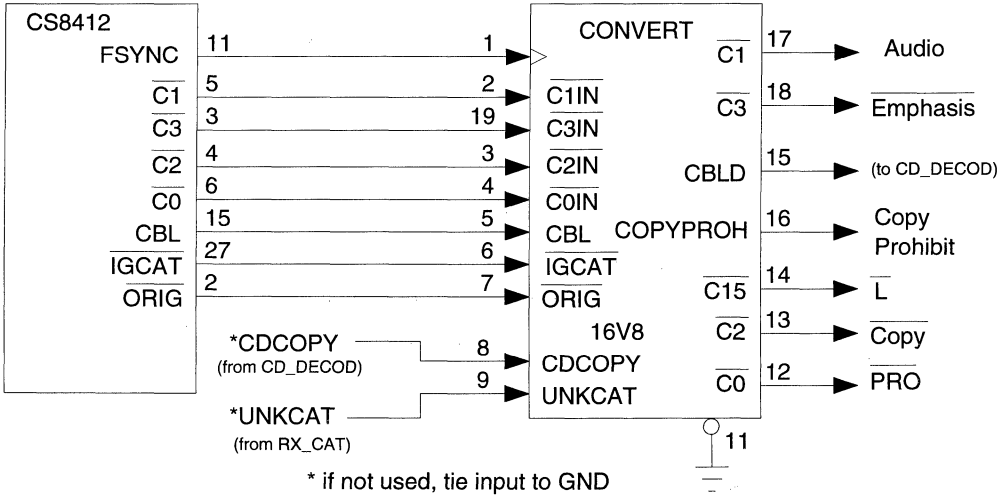

Figure 10. CS8412 Receiver - SCMS Decode

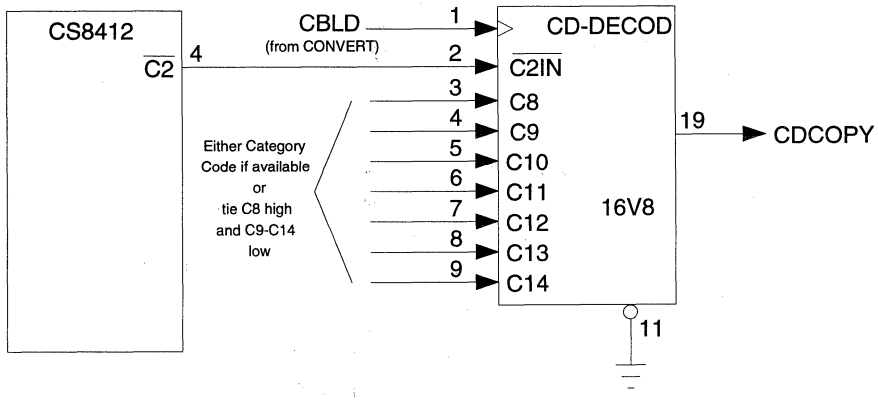

Figure 11. CS8412 Receiver - CD Copy (4-10 Hz) Decode

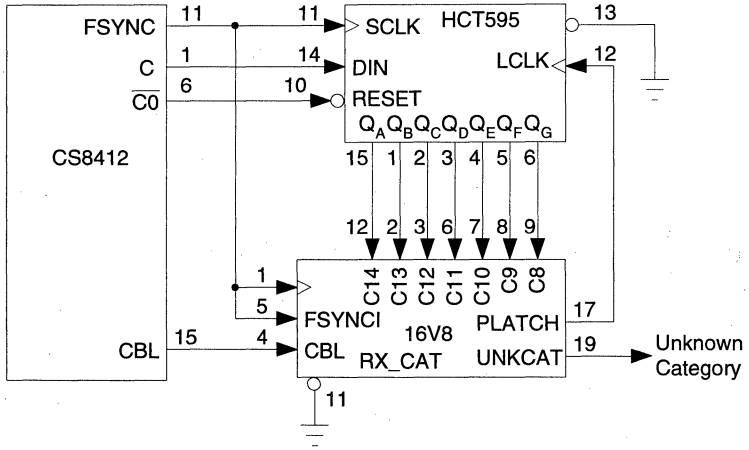

Figure 12. CS8412 Receiver - Unknown Category Decode

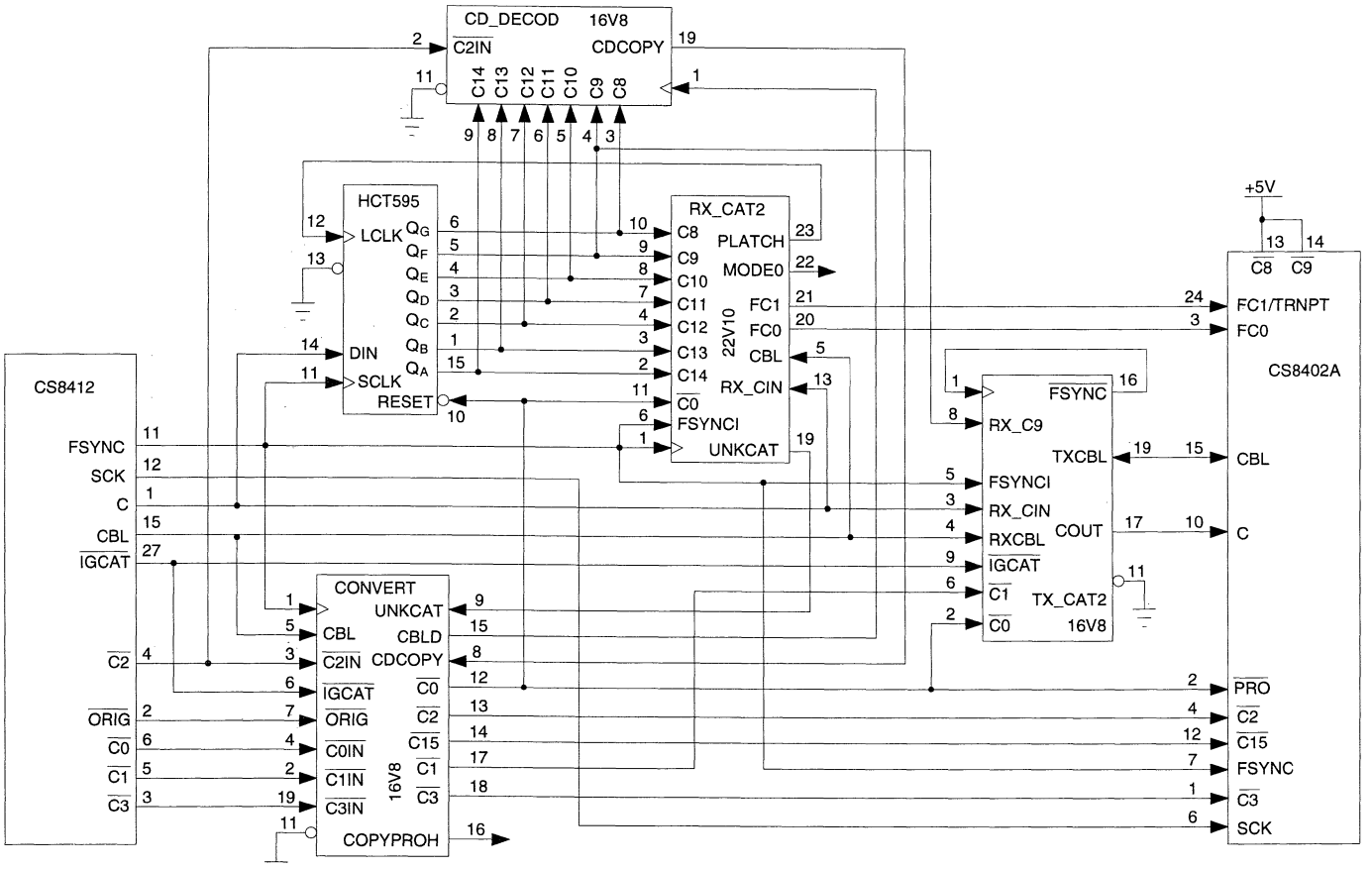

Figure 13. CS8412/02 Transceiver - Pass Through Design

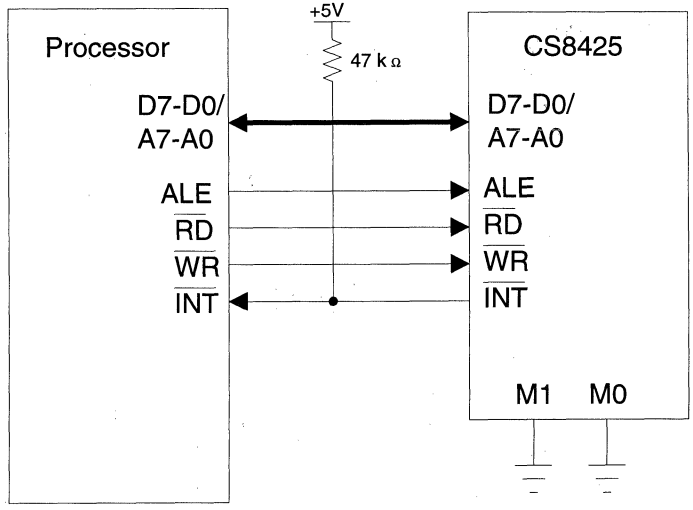

Figure 14. CS8425 Transceiver - Software SCMS Decode

	0	1	2	3	4	5	6	7	
RCS0	CS0	CS1	CS2	CS3	CS4	x	CS24	CS25	Receiver
RCS1	CS8	CS9	CS10	CS11	CS12	CS13	CS14	CS15	
TCS0	x	CS1	CS2	CS3	CS4	x	CS24	CS25	Transmitter
TCS1	CS8	CS9	CS10	CS11	CS12	CS13	CS14	CS15	

Figure 15. CS8425 Transceiver - Channel Status Register Set

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE    Transmit Full Category Codes
PATTERN  TX_CAT
REVISION 1.0
AUTHOR   Clif Sanchez
COMPANY  Crystal Semiconductor
DATE     1/10/93

CHIP  _tx_cat  PALCE16V8

; (C) 1993 Crystal Semiconductor Corp.
;---------------------------------- PIN Declarations ---------------
PIN  1          FSYNCB          ; IN - /FSYNC must be L/R and not I2S format
                                ;           if I2S pin 1 must be FSYNC
;PIN  2          not used        ; IN -
PIN  3          /C10            ; IN - Category code (byte 1, bit 2)
PIN  4          CBL             ; IN - Channel status block start signal
PIN  5          FSYNCI          ; IN - FSYNC - must be L/R and not I2S format
PIN  6          /C11            ; IN - Category code (byte 1, bit 3)
PIN  7          /C12            ; IN - Category code (byte 1, bit 4)
PIN  8          /C13            ; IN - Category code (byte 1, bit 5)
PIN  9          /C14            ; IN - Category code (byte 1, bit 6)
PIN  10         GND
PIN  11         /OE             ; IN - Output Enable for regs, not used
PIN  12         A3              ; OUT - MSB of 4 bit synchronous counter
PIN  13         A2              ; OUT -    This counter counts
PIN  14         A1              ; OUT -    channel status bits
PIN  15         A0              ; OUT - LSB of 4 bit synchronous counter
PIN  16         /FSYNC          ; OUT - /FSYNC - for clock (pin 1)
PIN  17         COUT            ; OUT - Channel status output
;PIN  18         not used        ; could be used to enter other channel
;PIN  19         not used        ; status bits not supported by the CS8402
PIN  20         VCC

STRING  FINISH  'A3 * A2 * A1 * A0'
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

;  A3 - A0 are a synchronous counter that counts up and stops at all ones.
;  CBL low clears counter, CBL high allows counter to count up.

A0 := (/A0 + FINISH) * CBL

A1 := (/A1 * A0 + A1 * /A0 + FINISH) * CBL

A2 := (/A2 * A1 * A0 + A2 * (/A1 + /A0) + FINISH) * CBL

A3 := (A2 * A1 * A0 + A3) * CBL
```

PAL 1.1 TX_CAT.PDS - Transmit Category Codes

```
/FSYNC = /FSYNCI                          ; connected to clock - pin 1

;       C8 and C9 are entered on CS8412

COUT =  C10 * A3 * /A2 *  A1 * /A0
      + C11 * A3 * /A2 *  A1 *  A0
      + C12 * A3 *  A2 * /A1 * /A0
      + C13 * A3 *  A2 * /A1 *  A0
      + C14 * A3 *  A2 *  A1 * /A0

; C8 - C14 can be internally fixed by entering the counter codes where a
; category code bit should equal 1. Using this method, if the category
; code has to be updated in the future, this PLD just needs to be
; reprogrammed and no hardware needs to be changed.
;
; As an example, if the category code is 101 1000 - microphone
; Then the equation for COUT is:
;
;COUT =  A3 * /A2 * /A1 * /A0            ; C8  on (don't use C8 on CS8402)
;      + A3 * /A2 *  A1 * /A0            ; C10 on
;      + A3 * /A2 *  A1 *  A0            ; C11 on - all others off by default
```

PAL 1.2 TX_CAT.PDS - Transmit Category Codes

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE    Receive and convert Copy, L, and Copy Prohibit Flags
PATTERN  CONVERT
REVISION 1.1
AUTHOR   Clif Sanchez
COMPANY  Crystal Semiconductor
DATE     1/13/93

CHIP  _convert PALCE16V8

; (C) 1993 Crystal Semiconductor Corp.
;---------------------------------- PIN Declarations ---------------
PIN  1          FSYNC           ; IN - FSYNC must be L/R and not I2S format
                                ;           if I2S, pin 1 must be /FSYNC
PIN  2          /C1IN           ; IN - Channel Status bit 1 - CS8412, Ca
PIN  3          /C2IN           ; IN - Channel Status bit 2 - CS8412, Cb
PIN  4          /C0IN           ; IN - Channel Status bit 0 - CS8412, /C0
PIN  5          CBL             ; IN - Channel status block start signal
PIN  6          /IGCAT          ; IN - two category codes - CS8412, Ce
PIN  7          /ORIG           ; IN - decoded L bit - CS8412, Cd
PIN  8          CDCOPY          ; IN - C2 at 4-10Hz rate (CD_DECOD.PDS)
PIN  9          UNKCAT          ; IN - undefined category code (RX_CAT.PDS)
PIN  10         GND
PIN  11         /OE             ; IN - Output Enable for regs, not used
PIN  12         /C0             ; OUT - Latched /C0 bit = /PRO
PIN  13         /C2             ; OUT - decoded copyright bit
PIN  14         /C15            ; OUT - decoded generation status (L) bit
PIN  15         CBLD            ; OUT - CBL delayed by FSYNC rising
PIN  16         COPYPROH        ; OUT - copy prohibit signal
PIN  17         /C1             ; OUT - Latched /C1 bit = Audio
PIN  18         /C3             ; OUT - Latched /C3 bit = /Pre-Emphasis
PIN  19         /C3IN           ; IN - Channel Status bit 3 - CS8412, Cc
PIN  20         VCC

STRING  ENAB    'CBL * /CBLD'
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

CBLD := CBL                     ; (also used by CD_DECOD.PDS)

; if (received C2 == 1
;      && (category code != (0000000 || 01100xx))      /*  IGCAT = 0  */
;      && (C0 != Professional) )
;  then C2 out = 1              /* copyright not asserted */
;  else C2 out forced to 0      /* copyright asserted  */

C2 := C2IN * /IGCAT * /CDCOPY * /C0IN * ENAB
        + C2 * CBL * CBLD
        + C2 * /CBL
```

PAL 2.1 CONVERT.PDS - Convert SCMS Bits

```
; The Following C15 definitions assumes this PLD IS NOT attached to the
;       following category codes: 001xxxx, 0111xxx, 100xxxx

C15 := ORIG * /CDCOPY * ENAB     ; C15 = 1 if original & !CDCOPY
       + IGCAT * ENAB            ;           or if ignorant category
       + C0IN * ENAB             ;           or if professional
       + C15 * CBL * CBLD
       + C15 * /CBL

; The Following C15 definitions assumes this PLD IS attached to the
;       following category codes: 001xxxx, 0111xxx, 100xxxx
;
;/C15 := ORIG * /CDCOPY * ENAB     ; C15 = 0 if original & !CDCOPY
;        + IGCAT * ENAB           ;           or if ignorant category
;        + C0IN * ENAB            ;           or if professional
;        + C15 * CBL * CBLD
;        + C15 * /CBL

;   COPYPROH = TRUE if {
;          (C2 == copy protected && L == 1st generation && !ignorant category)
;               || C0 == professional channel status (optional)
;               || CD - C2 alternating between 4 and 10 Hz rate (copy)
;          }

COPYPROH := /C2IN * /ORIG * /IGCAT * ENAB
;        + /C0IN * ENAB            ; add if professional should not be copied
       + CDCOPY * ENAB
       + COPYPROH * CBL * CBLD
       + COPYPROH * /CBL

;  The following bits are not needed for the SCMS system and they provide a
; latched version of the bits on the CS8412. They are latched from the CS8412
; when CBL goes high. In this way, CBL can be connected to SEL, and the
; error and frequency reporting features of the CS8412 may be used when CBL
; is low.

/C0 := /C0IN * ENAB              ; latched version of /C0: C0 - PRO bit
       + /C0 * CBL * CBLD
       + /C0 * /CBL

/C1 := /C1IN * ENAB              ; latched version of /C1: C1 - /Audio
       + /C1 * CBL * CBLD
       + /C1 * /CBL

/C3 := /C3IN * ENAB              ; latched version of /C3: C3 - Pre-Emphasis
       + /C3 * CBL * CBLD
       + /C3 * /CBL
```

PAL 2.2 CONVERT.PDS - Convert SCMS Bits

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE    Decodes C2 Alternating Between 4 and 10 Hz
PATTERN  CD_DECOD
REVISION 1.1
AUTHOR   Clif Sanchez
COMPANY  Crystal Semiconductor
DATE     1/15/93

CHIP  _cd_decod  PALCE16V8

; (C) 1993 Crystal Semiconductor Corp.
;---------------------------------- PIN Declarations ---------------
PIN  1          CBLD            ; IN - CBL delayed (from CONVERT.PDS)
PIN  2          /C2IN           ; IN - Channel Status bit 2 - Copyright bit
PIN  3          C8              ; IN - Category Code (byte 1, bit 0)
PIN  4          C9              ; IN - Category Code (byte 1, bit 1)
PIN  5          C10             ; IN - Category Code (byte 1, bit 2)
PIN  6          C11             ; IN - Category Code (byte 1, bit 3)
PIN  7          C12             ; IN - Category Code (byte 1, bit 4)
PIN  8          C13             ; IN - Category Code (byte 1, bit 5)
PIN  9          C14             ; IN - Category Code (byte 1, bit 6)
PIN  10         GND
PIN  11         /OE             ; IN - Output Enable for regs, not used
PIN  12         A4              ; OUT - MSB of 5 bit synchronous counter
PIN  13         A3              ; OUT -
PIN  14         A2              ; OUT -    counts CBLs (~230 Hz)
PIN  15         A1              ; OUT -
PIN  16         A0              ; OUT - LSB of 5 bit synchronous counter
PIN  17         CSTART          ; OUT - C2 at start of sequence
PIN  18         CCNG            ; OUT - C2 changed during sequence
PIN  19         CDCOPY          ; OUT - CCNG at end of sequence
PIN  20         VCC

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

; A4 - A0 are a synchronous counter that counts up and rolls over.
; CBL (delayed) is the clock which at Fs = 44.1 kHz produces CBL = ~230 Hz
; Therefore the counter rolls over at a frequency of 230/32 = 7 Hz

; CCNG is looking for a transition on C2 - in either direction.
; C2 frequency will be between 4 and 10 Hz which mean a transition will
; occur at double that rate or 8 to 20 Hz.

; Since CDCOPY is checking for a transition at a 7 Hz rate, CDCOPY should
; catch the minimum of 8 Hz.

A0 := /A0

A1 := /A1 * A0 + A1 * /A0

A2 := /A2 * A1 * A0 + A2 * (/A1 + /A0)

A3 := /A3 * A2 * A1 * A0 + A3 * (/A2 + /A1 + /A0)

A4 := /A4 * A3 * A2 * A1 * A0 + A4 * (/A3 + /A2 + /A1 + /A0)
```

PAL 3.1 CD_DECOD.PDS - Decode CD, C2 changing at 4 to 10 Hz

```
; CSTART stores the value of C2IN at the beginning of the counting interval.

CSTART := C2IN * A4 * A3 * A2 * A1 * /A0
        + CSTART * (/A4 + /A3 + /A2 + /A1 + A0)

; CCNG = 1 if C2IN changes with respect to CSTART at any time during the
;               counting interval.

CCNG := CSTART * /C2IN + /CSTART * C2IN
        + CCNG * (/A4 + /A3 + /A2 + /A1 + /A0)

; CDCOPY latches CCNG at the end of the counting interval. If C2IN is changing
; at a 4 to 10 Hz rate, then CCNG should go high at least once every counting
; interval and, since CDCOPY latches CCNG at the end of the interval, CDCOPY
; should stay high.

CDCOPY := CCNG * A4 * A3 * A2 * A1 * A0
        * C8 * /C9 * /C10 * /C11 * /C12 * /C13 * /C14   ; cat. code 100 0000
        + CDCOPY * (/A4 + /A3 + /A2 + /A1 + /A0)

;       If C8 - C14 are not available, tie C8 high and C9 - C14 low.
```

PAL 3.2 CD_DECOD.PDS - Decode CD, C2 changing at 4 to 10 Hz

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE    Receive Category codes and verify
PATTERN  RX_CAT
REVISION 1.0
AUTHOR   Clif Sanchez
COMPANY  Crystal
DATE     1/2/93

CHIP  _rx_cat  PALCE16V8

; (C) 1993 Crystal Semiconductor Corp.
;---------------------------------- PIN Declarations ---------------
PIN  1          FSYNC           ; IN - FSYNC must be L/R and not I2S format
                                ;          if I2S pin 1 must be /FSYNC
PIN  2          C13             ; IN - Category code (byte 1, bit 5)
PIN  3          C12             ; IN - Category code (byte 1, bit 4)
PIN  4          CBL             ; IN - Channel status block start signal
PIN  5          FSYNCI          ; IN - FSYNC - must be L/R and not I2S format
PIN  6          C11             ; IN - Category code (byte 1, bit 3)
PIN  7          C10             ; IN - Category code (byte 1, bit 2)
PIN  8          C9              ; IN - Category code (byte 1, bit 1)
PIN  9          C8              ; IN - Category code (byte 1, bit 0)
PIN  10         GND
PIN  11         /OE             ; IN - Output Enable for regs, not used
PIN  12         C14             ; IN - Category code (byte 1, bit 6)
PIN  13         A3              ; OUT - MSB of 4 bit synchronous counter
PIN  14         A2              ; OUT -    This counter counts
PIN  15         A1              ; OUT -    channel status bits
PIN  16         A0              ; OUT - LSB of 4 bit synchronous counter
PIN  17         PLATCH          ; OUT - parallel latch signal for HC595
PIN  18         KNOWN           ; OUT - some of the valid category codes
PIN  19         UNKCAT          ; OUT - all unknown category codes
PIN  20         VCC

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

; A3 - A0 form a synchronous counter that counts up to all ones and stops.
; CBL low resets counter which waits for CBL high to start counting again.

A0 := (/A0 + PLATCH) * CBL

A1 := (/A1 * A0 + A1 * /A0 + PLATCH) * CBL

A2 := (/A2 * A1 * A0 + A2 * (/A1 + /A0) + PLATCH) * CBL

A3 := (A2 * A1 * A0 + A3) * CBL

; PLATCH should rise after channel status bit 15 is latched by the serial
; shift register of the HCT595. PLATCH rising causes the HCT595 to internally
; parallel load the latch register of the HCT595 from its shift register.
; Therefore the HCT595 outputs always contain the category codes.

PLATCH = (A3 * A2 * A1 * A0 * /FSYNCI + PLATCH) * CBL
```

PAL 4.1 RX_CAT.PDS - Receive Category Codes

```
; UNKCAT is the inverse of all known category codes. Since the 16V8 PLD allows
; a maximum of 7 OR terms, the total defined category codes must be split over
; two output cells, UNKCAT and KNOWN. The actual product terms have been
; minimized such that most product terms incorporate two known category codes
; as shown in the comment section to the right of each term.

/UNKCAT = KNOWN
        + /C8 * /C9 * /C10 * /C11 * /C12 * /C13          ; 000 000x  (2)
        + /C8 * /C9 *  C10         * /C12 * /C13 * /C14  ; 001 x000  (2)
        + /C8 * /C9 *  C10 * /C11 * /C12         *  C14  ; 001 00x0  (2)
        + /C8 *  C9 * /C10 * /C11 * /C12         * /C14  ; 010 00x0  (2)
        + /C8 *  C9 * /C10         *  C12 * /C13 * /C14  ; 010 x100  (2)
        + /C8 *  C9 *  C10 * /C11         * /C13 * /C14  ; 011 0x00  (2)

; Since KNOWN is OR'd into UNKCAT, KNOWN's product terms are just an
; extension of UNKCAT's product terms.

KNOWN   =  C8 * /C9 * /C10 * /C11 * /C12 * /C13 * /C14  ; 100 0000  (1) CD
        +  C8 * /C9 * /C10 *  C11 * /C12 * /C13         ; 100 100x  (2)
        +  C8 * /C9 *  C10         * /C12 * /C13 * /C14  ; 101 x000  (2)
        +  C8 *  C9 * /C10 * /C11 * /C12 * /C13         ; 110 000x  (2)
        +  C8 *  C9 * /C10 *  C11 * /C12 * /C13 * /C14  ; 110 1000  (1) VTR

;     Since each output can handle up to seven product terms, KNOWN has room for
;     two more terms if the defined category code list is updated.
```

PAL 4.2 RX_CAT.PDS - Receive Category Codes

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE    Receive Category codes & verify, rec. Fs, and Mode
PATTERN  RX_CAT2
REVISION 1.1
AUTHOR   Clif Sanchez
COMPANY  Crystal
DATE     1/16/93

CHIP  _rx_cat2  PALCE22V10

; (C) 1993 Crystal Semiconductor Corp.
;---------------------------------- PIN Declarations ---------------
PIN  1          FSYNC           ; IN - FSYNC must be L/R and not I2S format
                                ;           if I2S pin 1 must be /FSYNC
PIN  2          C14             ; IN - Category code (byte 1, bit 6)
PIN  3          C13             ; IN - Category code (byte 1, bit 5)
PIN  4          C12             ; IN - Category code (byte 1, bit 4)
PIN  5          CBL             ; IN - Channel status block start signal
PIN  6          FSYNCI          ; IN - FSYNC - must be L/R and not I2S format
PIN  7          C11             ; IN - Category code (byte 1, bit 3)
PIN  8          C10             ; IN - Category code (byte 1, bit 2)
PIN  9          C9              ; IN - Category code (byte 1, bit 1)
PIN  10         C8              ; IN - Category code (byte 1, bit 0)
PIN  11         /C0             ; IN - Channel Status bit 0 - PRO
PIN  12         GND
PIN  13         RX_CIN          ; IN - Channel Status from CS8412, C pin
PIN  14         A0              ; OUT - LSB of 4 bit synchronous counter
PIN  15         A1              ; OUT -
PIN  16         A2              ; OUT -    This counter counts
PIN  17         A3              ; OUT -    channel status bits
PIN  18         A4              ; OUT - MSB of 4 bit synchronous counter
PIN  19         UNKCAT          ; OUT - all unknown category codes
PIN  20         FC0             ; OUT - rx Fs (C24, C25) for CS8402
PIN  21         FC1             ; OUT - rx Fs (C24, C25) + Transparent mode
PIN  22         MODE0           ; OUT - C6 = C7 = 0 - mode 0 (only 1 defined)
PIN  23         PLATCH          ; OUT - parallel latch signal for HC595
PIN  24         VCC

;-------------------------------------------------------------------------
; RX_CAT2 replaces RX_CAT in pass through designs that support both
; professional and consumer interfaces.
;
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

; A4 - A0 form a synchronous counter that counts up to all ones and rolls
; over.
; CBL low resets counter which waits for CBL high to start counting again.

A0 :=  /A0 * CBL

A1 := (/A1 * A0 + A1 * /A0) * CBL

A2 := (/A2 * A1 * A0 + A2 * (/A1 + /A0)) * CBL
```

PAL 5.1 RX_CAT2.PDS - Rec. Category Codes, Pass Thru Design

8

```
A3 := (/A3 * A2 * A1 * A0 + A3 * (/A2 + /A1 + /A0)) * CBL

A4 := (/A4 * A3 * A2 * A1 * A0 + A4 * (/A3 + /A2 + /A1 + /A0)) * CBL

; PLATCH should rise after channel status bit 15 is latched by the serial
; shift register of the HCT595. PLATCH rising causes the HCT595 to internally
; parallel load the latch register of the HCT595 from its shift register.
; Therefore the HCT595 outputs always contain the category codes.

PLATCH = (/A4 * A3 * A2 * A1 * A0 * /FSYNCI + PLATCH) * CBL

; UNKCAT is the inverse of all known category codes. Since the center
; product terms of the 22V10 PLD allows a maximum of 16 OR terms, the total
; defined category codes can be contained in one output cell, UNKCAT.
; The actual product terms have been minimized such that most product terms
; incorporate two known category codes as shown in the comment section to the
; right of each term.

/UNKCAT =
          /C8 * /C9 * /C10 * /C11 * /C12 * /C13          ; 000 000x  (2)
        + /C8 * /C9 *  C10         * /C12 * /C13 * /C14  ; 001 x000  (2)
        + /C8 * /C9 *  C10 * /C11 * /C12         *  C14  ; 001 00x0  (2)
        + /C8 *  C9 * /C10 * /C11 * /C12         * /C14  ; 010 00x0  (2)
        + /C8 *  C9 * /C10         *  C12 * /C13 * /C14  ; 010 x100  (2)
        + /C8 *  C9 *  C10 * /C11         * /C13 * /C14  ; 011 0x00  (2)
        +  C8 * /C9 * /C10 * /C11 * /C12 * /C13 * /C14  ; 100 0000  (1) CD
        +  C8 * /C9 * /C10 *  C11 * /C12 * /C13          ; 100 100x  (2)
        +  C8 * /C9 *  C10         * /C12 * /C13 * /C14  ; 101 x000  (2)
        +  C8 *  C9 * /C10 * /C11 * /C12 * /C13          ; 110 000x  (2)
        +  C8 *  C9 * /C10 *  C11 * /C12 * /C13 * /C14  ; 110 1000  (1) VTR

;    UNKCAT has room for five more terms if needed

; FC1 and FC0 are used by the CS8402 in consumer mode to set the channel
; status bits C24 and C25, sample frequency. When PRO mode is received
; C0 = 1, FC1 on the CS8402 is defined as TRNPT which defines transparent
; mode. In this mode, all parallel channel status inputs are ignored and all
; channel status data comes from the C input pin. This PLD uses transparent
; mode when professional channel status is received.

FC1 := RX_CIN * A4 * A3 * /A2 * /A1 * /A0       ; store C24
       + FC1 * (/A4 + /A3 + A2 + A1 + A0)       ; any other time, remember FC1
       + C0                                     ; set TRNPT = 1 when C0 = 1

FC0 := /FC1 * RX_CIN * A4 * A3 * /A2 * /A1 * A0 ; set if C24 = 1 and C25 = 1
       + FC0 * (/A4 + /A3 + A2 + A1 + /A0)      ; any other time, remember FC0

; MODE 0 is defined in consumer channel status as C6 = C7 = 0. This is the
; only mode currently defined. The following output indicates when mode 0
; is received; however, since both C6 and C7 cannot be stored by one output
; cell, this pin will go high for one channel status bit period (C6) and then
; return low if C6 = 0 and C7 = 1.

/MODE0 := RX_CIN * /A4 * /A3 * A2 * A1 * /A0     ; store C6
       + /MODE0 * (A4 + A3 + /A2 + /A1 + A0)     ; any other time remember C6
       + RX_CIN * /A4 * /A3 * A2 * A1 * A0       ; if C7 = 1, set /MODE0
```

PAL 5.2 RX_CAT2.PDS - Rec. Category Codes, Pass Thru Design

```
;PALASM Design Description
;---------------------------------- Declaration Segment ------------
TITLE    Transmit Category Codes, allow A/D exception, pass thru PRO
PATTERN  TX_CAT2
REVISION 1.2
AUTHOR   Clif Sanchez
COMPANY  Crystal Semiconductor
DATE     1/16/93

CHIP  _tx_cat2  PALCE16V8

; (C) 1993 Crystal Semiconductor Corp.
;---------------------------------- PIN Declarations ---------------
PIN  1          FSYNCB          ; IN - /FSYNC must be L/R and not I2S format
                                ;          if I2S pin 1 must be FSYNC
PIN  2          /C0             ; IN - CS bit 0 - PRO - for pass thru mode
PIN  3          RX_CIN          ; IN - Receive serial channel status line
PIN  4          RXCBL           ; IN - CS block start signal from CS8412
PIN  5          FSYNCI          ; IN - FSYNC - must be L/R and not I2S format
PIN  6          /C1             ; IN - Channel Status bit 1, /Audio/Non-audio
;PIN  7          unused          ; IN -
PIN  8          RX_C9           ; IN - CS bit 9 used in conjunction w/ IGCAT
PIN  9          /IGCAT          ; IN - used with C9 to find A/D w/o copy cat.
PIN  10         GND
PIN  11         /OE             ; IN - Output Enable for regs, not used
PIN  12         A3              ; OUT - MSB of 4 bit synchronous counter
PIN  13         A2              ; OUT -    This counter counts
PIN  14         A1              ; OUT -    channel status bits
PIN  15         A0              ; OUT - LSB of 4 bit synchronous counter
PIN  16         /FSYNC          ; OUT - /FSYNC - for clock (pin 1)
PIN  17         COUT            ; OUT - Channel status output
PIN  18         CAT_CODE        ; OUT - this equip. category code
PIN  19         TXCBL           ; I/O - CS block start signal for CS8402A
PIN  20         VCC

STRING  FINISH  'A3 * A2 * A1 * A0'
;---------------------------------------------------------------------
; TX_CAT2 replaces TX_CAT in pass through designs that want to support the
; professional mode. Also, a CS8402A is needed since only the "A" version
; supports transparent mode.
;
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

;  A3 - A0 are a synchronous counter that counts up and stops at all ones.
;  TXCBL low clears counter, TXCBL high allows counter to count up.

A0 := (/A0 + FINISH) * TXCBL

A1 := (/A1 * A0 + A1 * /A0 + FINISH) * TXCBL

A2 := (/A2 * A1 * A0 + A2 * (/A1 + /A0) + FINISH) * TXCBL

A3 := (A2 * A1 * A0 + A3) * TXCBL
```

PAL 6.1 TX_CAT2.PDS - Tx Category Codes, Pass Thru Design

```
; TXCBL is an input from the CS8402A in consumer, and an output (RXCBL) when
; in professional mode

TXCBL = RXCBL * C0
TXCBL.TRST = C0

/FSYNC = /FSYNCI                          ; connected to clock - pin 1

;       if (Professional)
;         COUT = received channel status data, i.e. pass through
;       else if (received category code != 01100xx)
;              COUT = CAT_CODE, which is specified category code
;            else   (received category code == 01100xx)
;              COUT = 0110000 category code


COUT    =  RX_CIN * C0                    ; if PRO - pass thru rec'd CIN
        + C1 * /A3 * /A2 * /A1 * A0       ; /Audio, Non-Audio
        + CAT_CODE * /IGCAT * /C0
        + CAT_CODE * IGCAT * /RX_C9 * /C0
        + A3 * /A2 * /A1 *  A0 * IGCAT * RX_C9 * /C0 ; set to category code
        + A3 * /A2 *  A1 * /A0 * IGCAT * RX_C9 * /C0 ; 0110000 if same rec.

; If the CS8412 SEL pin changes between channel status and error/frequency
; reporting, IGCAT must be latched.

; C8 - C11 & C14  are internally fixed by entering the counter codes only
; Do not use category code bits C8 and C9 on CS8402 (tie high)
; The category code set below is 0100000 - PCM encoder/decoder. If other
; codes are desired, remove semicolon (comment) from start of line for bits
; that need to be a one.

CAT_CODE =
              A3 * /A2 * /A1 *  A0        ; C9 = 1
;           + A3 * /A2 * /A1 * /A0        ; add if C8  needs to be a 1
;           + A3 * /A2 *  A1 * /A0        ; add if C10 needs to be a 1
;           + A3 * /A2 *  A1 *  A0        ; add if C11 needs to be a 1
;           + A3 *  A2 * /A1 * /A0        ; add if C12 needs to be a 1
;           + A3 *  A2 * /A1 *  A0        ; add if C13 needs to be a 1
;           + A3 *  A2 *  A1 * /A0        ; add if C14 needs to be a 1
```

PAL 6.2 TX_CAT2.PDS - Tx Category Codes, Pass Thru Design

A Single Chip Stereo Audio Codec for PC Multimedia Applications

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A system solution has been realized consisting of a single CMOS chip and associated software providing complete audio capabilities for a multimedia enabled computer. Topics covered in this paper include design trade-offs between feature implementation in hardware or software, computer performance issues (sound quality and throughput), chip features and low cost implementation.

1.0 System Architecture

In multimedia computer implementations both software and hardware are required. In this solution, software components provided include device drivers and input/output control applications. The hardware features in this mixed signal implementation include stereo delta-sigma analog-to-digital and digital-to-analog converters (ADC's and DAC's), analog input and output controls, 4 stereo/1 monophonic channel mixer, parallel computer bus support and hardware data compression and decompression. Figure 1 illustrates the block diagram of the chip.

2.0 Software Architecture

Figure 2 shows the general architecture of the audio software support. The application programming interface (API) provides a hardware independent functional interface for application writers. The device driver for a particular hardware solution interprets the API interface calls and invokes the appropriate hardware function. Figure 3 shows an example multimedia programming environment for Microsoft Windows 3.1. In this case the application programming interface is called a Media Control Interface or MCI.(Microsoft [1])

In multimedia computer implementations optimized software and hardware architectures are required for the lowest cost, highest quality implementation. These trade-offs include sound quality, system throughput, feature set and cost. Performance design goals highlight the requirements on system architecture and the importance of efficient software. Audio is a real-time process, however most applications and operating systems today are non real-time. Therefore, most applications simply slow down when the performance capacity of the computer is exceeded. Since audio is a real-time process, it cannot slow down; therefore, discontinuities will be inserted into the

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data stream. This results in audible errors such as "stutters" or "popping and clicking". System failures of this nature are very annoying and reduce the usefulness of audio in computing applications. Careful hardware design and high quality software can minimize these affects for computer audio applications.

Software applications provide the user interface for the chip feature set. An input and output control application is provided for this solution with visual control of the volume, input/output selection, muting and special features such as dither.

3.0 Analog Input and Control

The analog input has a 4-way multiplexer to select the ADC input. Three of the inputs to the chip are analog and the final input is the output of the mixer. A programmable gain stage is provided at the input of the ADC providing a 0 to +22.5dB gain adjustment of the signal in 1.5dB steps. In addition, a 20dB gain block is provided on the microphone input stage to minimize the external gain required.

Changing the gain of the input circuit at a random time can cause a step function in the output signal. The magnitude of the step function will depend on the instantaneous value of the signal at the time the gain is changed. A series of such gain changes can result in an objectionable audible sound, commonly know as "zipper noise". To overcome this effect, changes in gain are only allowed to occur on zero crossings of the analog signal. This is achieved using a comparator which monitors the analog signal and compares it to "zero". (Since this device runs from a power supply voltage of +5V, signal zero is approximately 2.10 V.) If the signal does not have a zero crossing the volume level change will occur after a time out period of between 512 and 1024 samples.

4.0 ADC Architecture

Each ADC uses a 4th-order, switched-capacitor delta-sigma modulator, similar in architecture to that described by Welland et al [2]. Capacitor sizes are chosen to minimize die area and yield a typical dynamic range of 85dB. High frequency anti-alias filtering is achieved by including a series resistor on the silicon immediately prior to each modulator sampling capacitor. The modulator side of this resistor is brought out to a pin, where the addition of an external 1000pf NPO capacitor completes a single pole RC filter. This architecture avoids the need to have a RC filter on each one of the 3 analog inputs to the input multiplexer, thereby significantly reducing the external component count. In addition, the location of the filter allows the mixer output to be filtered before it is digitized by the ADC.

Following the modulator is a 1024-tap FIR filter. This filter has a passband of DC to 0.4 Fs, passband ripple of 0.1 dB and a stopband rejection of 74 dB. Figures 4, 5 and 6 show the filter response. The ADC offset is calibrated by a reference "zero" signal being sent to the ADC and capturing the resulting output code. All subsequent operations with the ADC will have this value

subtracted to remove the offset. To totally eliminate DC offset for all input conditions, a digital high pass filter option is controllable at the software interface. This approach eliminates all DC offsets at all gain settings.

5.0 DAC Architecture

The components of the DACs are a digital interpolation filter, a digital delta-sigma modulator and a one-bit DAC feeding a switched capacitor output smoothing filter, as previously described by Sooch et al [3].

The digital interpolation filter uses the silicon efficient multiplier free architecture where the Finite Impulse Response (FIR) coefficients are reduced to -1,0,+1. (Scott [4]) Compensation for imperfections in the phase response of the analog switched capacitor filter are also accomplished by the interpolation filter. This approach yields an overall linear phase response within ±0.50 degrees out to 0.4Fs (Figure 7).

The DAC also uses a 4th-order digital delta-sigma modulator accepting interpolated data and outputting a 1-bit data stream at 64 Fs or 128 Fs. The higher output 1-bit data stream is used at the lower sampling rates to minimize the noise of the modulator in the audible frequency range. This data stream is then filtered by a 3-pole Butterworth switched-capacitor filter. Figures 8, 9 and 10 show the overall response of the DAC. The passband is DC to 0.4Fs, the passband ripple is ±0.1dB, and the stopband rejection is 74dB, with an external 2Fs time constant RC filter.

DAC outputs are calibrated to yield a low output offset voltage. The uncalibrated DAC offset is measured with the previously calibrated ADC. The digital input value required to achieve zero offset is then stored in an offset calibration register, and is subsequently used to correct all future conversions.

In the computer environment, data underrun or overrun error conditions will occur when the system is overloaded. To help avoid audible artifacts during underrun conditions, the DAC will hold the last sample transmitted to the device. This results in an almost inaudible recovery from this type of error, particularly if only a few samples are affected.

6.0 Mixer

Three of the stereo inputs (line, aux1 and aux2) and the monophonic input are controlled by independent volume controls and are mixed with the output of the DAC. The volume control on each of the stereo inputs is controlled by 5-bit volume control registers. The range on the volume controls is from +12dB gain to -34.5dB attenuation in 1.5dB steps. A mute is also included for each channel. These inputs are provided to mix other stereo input sources in a multimedia computer such as a music synthesizer, CD ROM audio output and an auxiliary input from an external source such as a cassette or video player. The monophonic input is provided to mix the

internal monophonic "PC speaker" sound that is provided by most computers. This input has a 4-bit attenuator, providing the control for proper mixing with the other audio signals. Each volume control level represents 3dB of attenuation. All stereo volume controls contain zero crossing detectors, thereby minimizing "zipper noise" in a similar fashion to the input gain stage. The output of the mixer is stereo and monophonic. The stereo output is a line level signal for use as a high quality output. The monophonic output is the mix of the left and right channels and is provided as a output for an internal PC speaker. For this use a amplifier of the appropriate size is selected for the computer system and driven by the monophonic signal. This mixer provides a single control point for all the audio in a personal computing environment.

An additional feature of the mixer is calibration. During a full calibration cycle each op amp is calibrated individually. This procedure provides for minimum offsets throughout the mixer eliminating most pops and clicks.

7.0 Data Format Encode/Decode

A data format block provides support for several data types and compression/decompression. The data types supported are 8-bit linear data unsigned format(Figure 11) and 16-bit linear in two's-complement format. In addition, the 16-bit data stream supports low byte first (little endian) or high byte first formats (big endian). In the 8-bit linear modes dither can be optionally selected. When selected, a triangular probability distribution of random noise is added to the signal prior to quantization. This results in the elimination of artifacts such as the "crunching noise" associated with quantization.

Data compression (for the ADC output) and decompression (for the DAC input) is also supported in the form of companding using the CCITT G.711 μ-law and A-law formats (Figure 12) and Adaptive Differential Pulse Code Modulation (ADPCM) that is compliant with the Interactive Multimedia Association (IMA) definition. The ADPCM reduces the bus data rate and disk storage requirements by 4:1, providing near 16-bit quality with only 4 bits per sample.

8.0 Computer Parallel Bus Interface Architecture

The bus interface supports many parallel architectures such as the Industry Standard Architecture (ISA), Micro Channel and PC98. In addition, the feature set includes 3rd party Direct Memory Access (DMA), I/O access to control ports, full duplex operation, synchronization timer, 16 sample First In First Out (FIFO) buffers on input and output and 16 milliamp current drivers for lower cost implementation. DMA support is provided to minimize the amount of storage required on the audio device. This is accomplished by allowing the audio device to control data movement in and out of the host memory using the DMA controller on the host computer. Simultaneous operation of DMA channels is provided to support full duplex operation (simultaneous capture and playback). The data format control on capture and playback is controlled independently. This feature allows applications such as voice control of the PC and audio playback to run together.

Maximum DMA latency represents the time required to move the required audio data to or from the device. If the amount of time is exceeded, loss of data on capture or an audible defect on playback will result. For example, if there is a single sample buffer and the sample rate is 44.1kHz the latency would be 22 microseconds. In a computer environment this short period of time can result in errors. To minimize this effect two 16-sample FIFO buffers are provided. This additional buffering provides enough latency so that this error condition is virtually eliminated.

The final two features include the synchronization timer and electrical bus drive. The synchronization timer is provided to aid in the multimedia application execution, particularly the timing of multiple real time data streams. The timer has a resolution of 10 microseconds and maximum time of 650 milliseconds. The parallel data path has a bus drive capability of 16 mA enabling its use without bus driver chips in many applications.

9.0 Application Schematic and Board Layout

The PC environment is extremely sensitive to implementation cost and printed circuit board layout area. As shown in the recommended connection diagram in Figure 13, both items are optimized with this device. All internal signals are internally biased to approximately 2.10 V and require AC coupling capacitors on all input and output signals.

Printed circuit board layout and grounding are critical items in the use of this device to provide optimal performance. Figure 14 shows the layout of the printed circuit board around the device, with the majority of the chip over the analog ground plane and the parallel bus pins over the digital ground plane. Figure 15 shows the recommended grounding and decoupling capacitor arrangements. Two important points to notice in this figure are the short decoupling paths and the component placement of the smaller capacitors, which are as close to the device package as possible. Crystal offers a free schematic and layout review service, which is best used before the first prototype circuit board is built. Harris[5] has previously discussed optimum clock choices and layout guidelines for delta-sigma converters.

10.0 Typical Specification Summary

Analog Inputs & ADC		DAC & Analog Outputs	
ADC resolution	16 bits	DAC resolution	16 bits
Total Dynamic Range	95dB	Total Dynamic Range	95dB
Instantaneous		Instantaneous	
Dynamic Range	85dB	Dynamic Range	85dB
Frequency Response	0 to 0.40Fs	Frequency Response	0 to 0.4Fs
Input Gain	0 to 22.5dB	DAC Attenuator	0 to 94.5dB
Step Size	1.5dB		

Mixer	
Gain/Attenuation	+12 to -34.5dB
Step Size	1.5dB

Global Specifications	
Sample Rate	5.5kHz to 48kHz
Digital Power Supply	+5V or +3.3V
Analog Power Supply	+5V
Power Supply Current	110 mA (+5V)
Full Scale Signal Level	1 Vrms

All dynamic range specifications are A-weighted. Total dynamic range of the DAC is the ratio between the full scale output of the chip and the noise floor when the maximum attenuation is selected. Total dynamic rage of the ADC is the ratio between the full scale input and the noise floor. The instantaneous dynamic range of the ADC and DAC is measured with the gain and attenuator set to 0dB.

11.0 Conclusions

A complete audio solution has been presented including software and a single chip computer audio integrated circuit. Complete system design will allow high quality, low cost audio to be easily and quickly implemented in computing environments.

12.0 References

[1] Microsoft Corporation, "Microsoft Windows Multimedia Programmer's Workbook", Microsoft Press, 1991.

[2] D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, and K. Takasuka, "A Stereo 16-Bit Delta-Sigma A/D Converter for Digital Audio", JAES, Vol 37, No.6, June 1989.

[3] N.S.Sooch, J.W.Scott, T.Tanaka, T. Sugimoto, C. Kubomura, "18- Bit Stereo D/A Converter with Integrated Digital and Analog Filters", 91st AES Convention, October 1991, New York, Pre-print #3113(y-1).

[4] J.W. Scott, "Multiplier-Free Interpolation for Oversampled Digital-to-Analog Conversion", 92nd AES Convention, March 1992, Vienna, Pre-print #3317.

[5] S. Harris, "How to Achieve Optimum Performance form Delta-Sigma A/D & D/A Converters", AES 93rd Convention, San Francisco, October 1992.

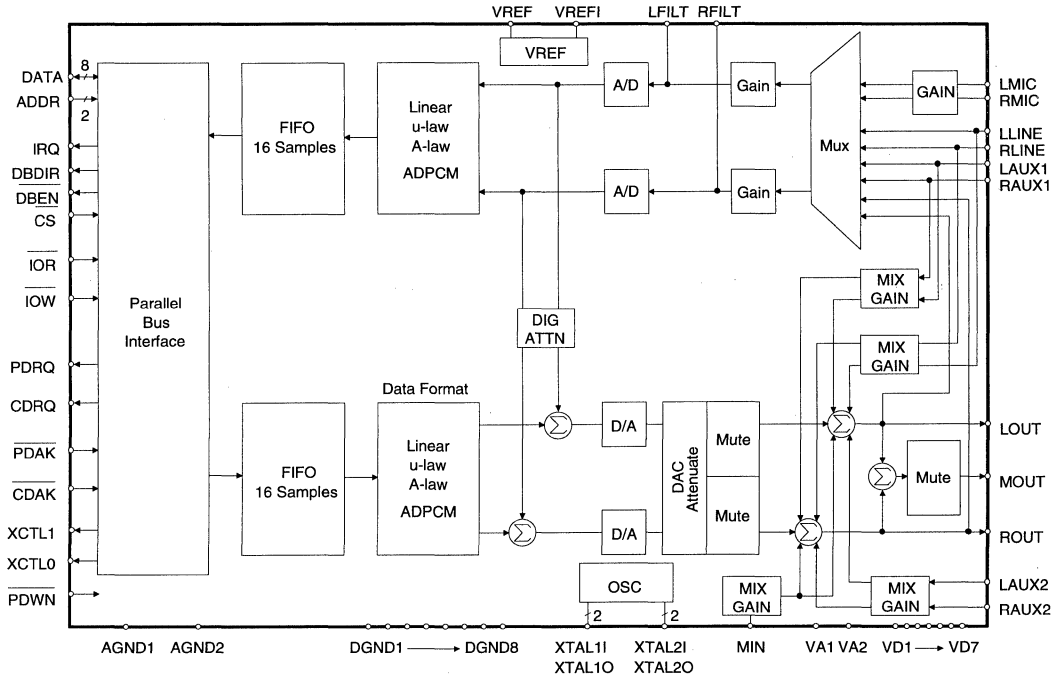

Figure 1. Chip Block Diagram

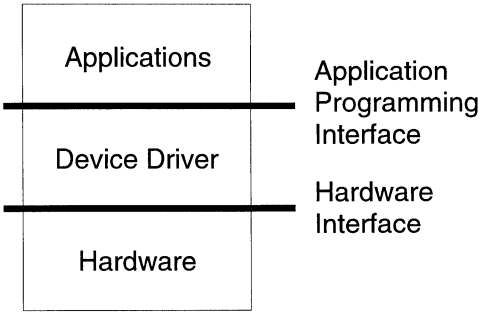

Figure 2. Systems Architecture.

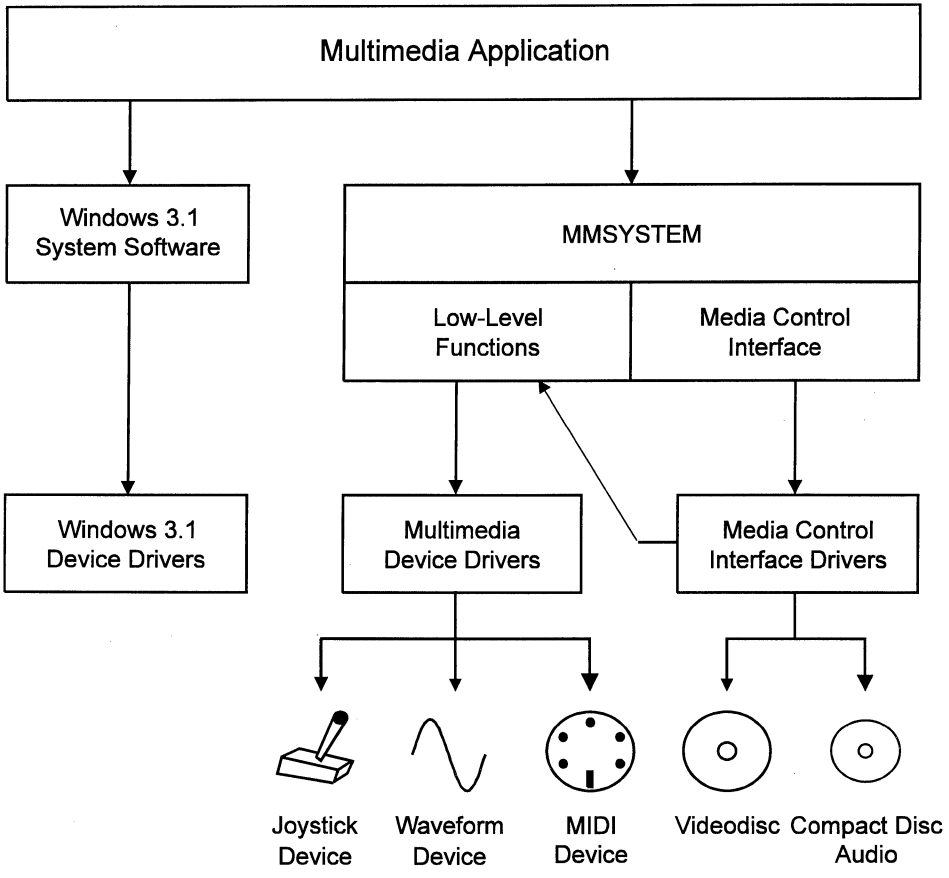

Figure 3. Window 3.1 Multimedia Architecture.

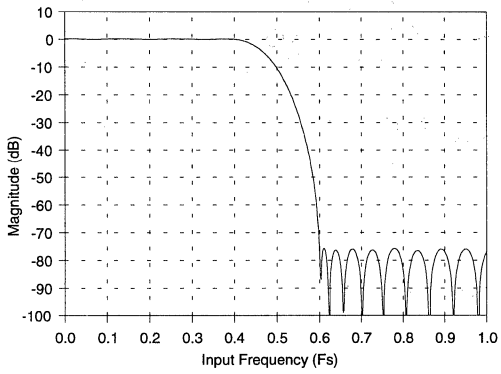

Figure 4. ADC Filter Response

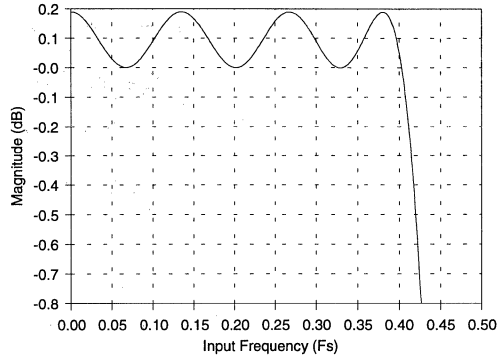

Figure 5. ADC Passband Ripple

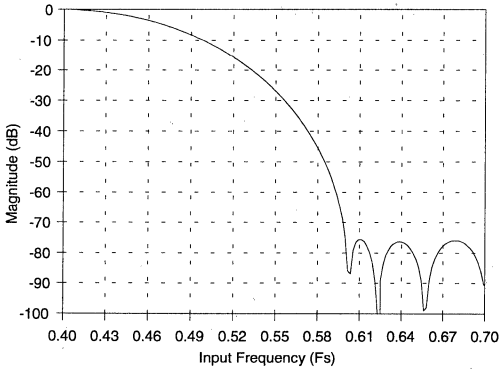

Figure 6. ADC Transition Band

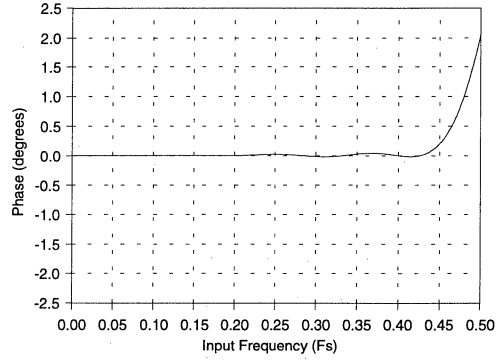

Figure 7. DAC Phase

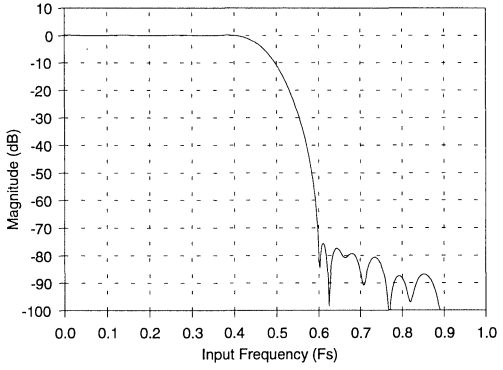

Figure 8. DAC Frequency Response

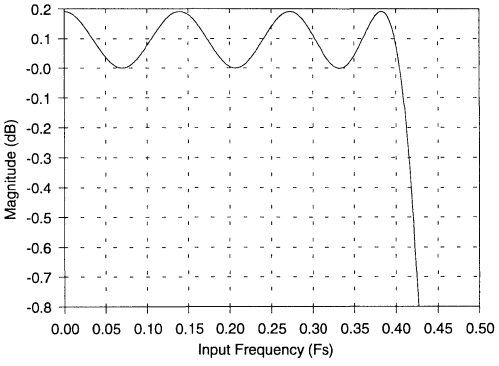

Figure 9. DAC Passband Ripple

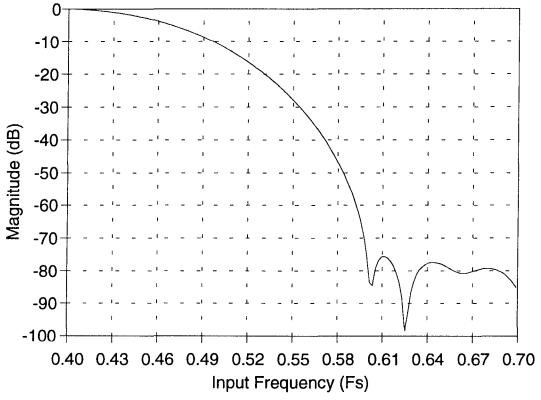

Figure 10. DAC Transition Band

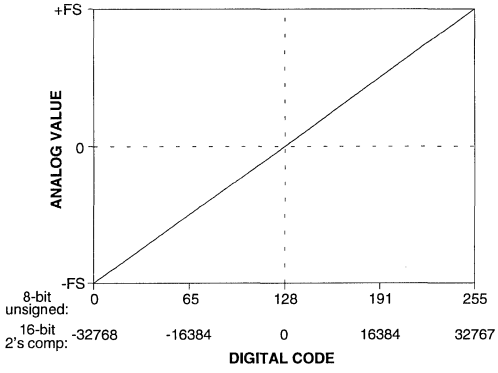

Figure 11. Linear Transfer Functions

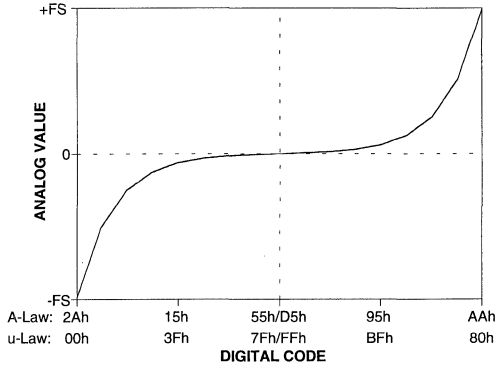

Figure 12. Companded Transfer Functions

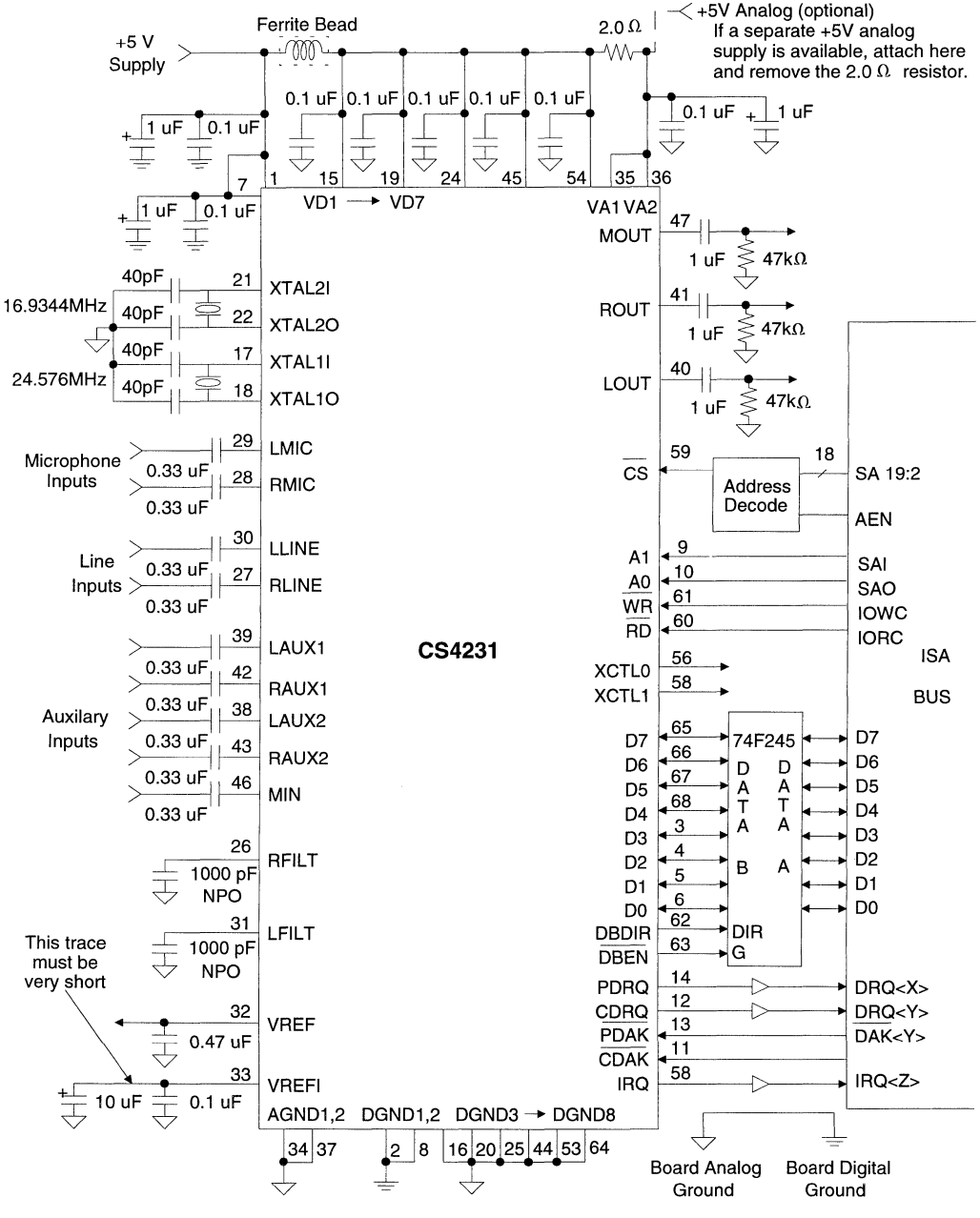

Figure 13. Typical Connection Diagram

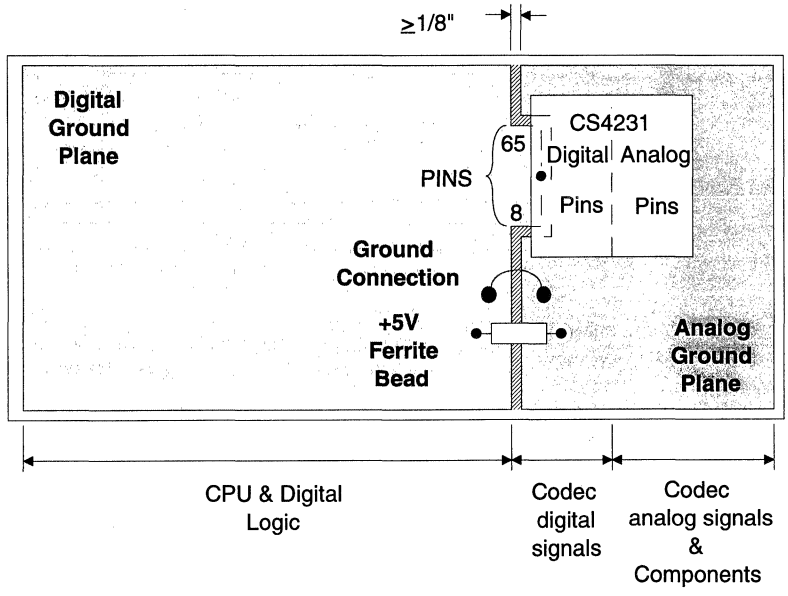

Figure 14. Suggested Layout Guideline

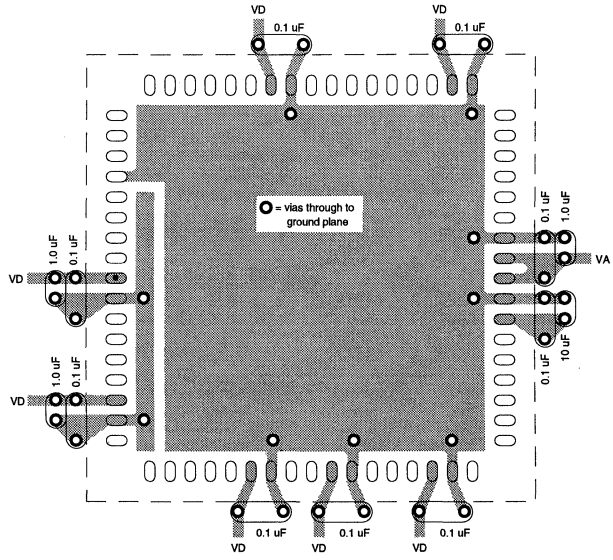

Figure 15. Recommended Decoupling Capacitor Layout

A Single-Chip Stereo Volume Control

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A CMOS stereo volume control has been designed specifically for micro-processor controlled audio systems. It features a 16-bit serial interface that controls two independent audio channels with a total adjustable range of 127dB in steps of 0.5dB. The range is divided into 95.5dB of attenuation and 31.5dB of gain. The part is capable of driving a load of 600 ohms in parallel with a 100pF capacitor and achieves 0.0007% THD over a 20Hz to 20kHz bandwidth.

1.0 INTRODUCTION

Digitally controlled, analog signal path volume controls have historically either been large in size compared to other components in an audio system, or have been small in size with very poor distortion and noise performance. An example of a large size solution is a stepper motor driving a wire wound potentiometer. While this solution has very low THD, the potentiometer must be buffered with a high quality audio amplifier and drive circuits for the stepper motor are necessary. An example of a small size solution is a multiplying Digital-to-Analog Converter. For a 1kHz signal which is fed into the reference input, the distortion of a multiplying DAC is typically limited to 86dB to 88dB.

New digital audio products address the size problem by implementing volume control in the digital domain. All digital volume controls reduce the output signal but do not reduce the noise. Therefore, as the signal is attenuated, the signal to noise ratio becomes worse. To address these problems, an audio volume control, complete with mute functions, and two independent analog audio channels, has been designed. This part is packaged in a 16 pin SOIC. The part achieves 0.0007% THD over the audio band, has a total integrated noise of 10μV rms over the audio band, and has virtually no clicks or pops during volume changes.

As can been seen in Figure 1, the part consist of two completely independent analog channels with a common digital control port and associated digital control logic to set the volume of the two analog channels. The analog section is operated from ±5V supplies while the digital section is operated from 0V to 5V supplies.

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2.0 ANALOG SIGNAL PATH

The analog signal path of the chip contains two independent channels. Each channel contains an input attenuator and a non-inverting buffer amplifier. The non-inverting buffer amplifier has an attenuator in the feedback path. This feedback path attenuator allows the gain of the non-inverting buffer amplifier to be adjusted from unity gain to +31.5dB in steps of 0.5dB. The input attenuator adjustable range is from 0dB down to -95.5dB.

Special care in the design and layout of the attenuators insures that minimal distortion and noise is introduced into the audio path due to the intrinsic non-linear nature of integrated circuit resistors. The resistor material used is heavily doped polysilicon (approximately 80 ohms per square). To shield the polysilicon from digitally induced noise present in the substrate, a Pwell is placed underneath each resistor. The input and output resistor attenuators are laid out in segments of 16dB.

The Pwell shield of the first 16dB input attenuator segment is driven directly by the analog input. The Pwell shield of the second 16dB input attenuator is driven by a buffered version of the -16dB analog signal. The Pwell shield of the remaining 16dB input attenuator segments are tied to analog ground. The technique of driving the Pwell of the first two 16dB attenuators reduces depletion width modulation of the polysilicon resistors. This technique also bootstraps the non-linear polysilicon to Pwell capacitance [1], [2]. The output feedback attenuator is similar in construction to the first two 16dB input attenuator segments, except that the Pwell of the first 16dB output attenuator is driven by the output of the non-inverting buffer amplifier.

The buffer amplifier is a class A-B amplifier that contains an input common-mode feedback loop and an offset calibration circuit. A simplified schematic of the buffer amplifier without the common-mode feedback loop is shown in Figure 2.

The input stage is a conventional folded-cascade design with the addition of a common-mode current feedback loop. Since this class A-B amplifier is operated in a non-inverting mode, the amplifier needs to have very high input common-mode rejection. Figure 3 shows a simplified schematic of the input stage which includes the common-mode current feedback loop. The input common-mode rejection is improved by the gain of this feedback loop. This feedback loop is a single pole circuit with the node at which the dominant pole is located being outside of the main analog signal path. Therefore, the common-mode current feedback has a much higher bandwidth than the analog signal path, thus allowing good input common-mode rejection even at relatively high frequencies.

The output stage of the class A-B amplifier is a composite design. The output pull-down n-channel transistor is driven by the output of the first stage buffered by a n-channel source follower. The output pull-up p-channel transistor is driven by a composite amplifier. This composite amplifier contains a common gate n-channel transistor driven by a common collector p-channel transistor. The gate of the common collector p-channel is connected to the output of the first stage. The drain of the common gate n-channel is connected to a p-channel diode that drives the output p-channel

pull-up transistor. The dc bias voltage of the common gate n-channel transistor determines the crossover characteristics of the output push-pull stage [3]. This amplifier also has a short circuit current limit of ±20mA.

The offset of the amplifier is calibrated to less than 200μV. A calibration is invoked when the "MUTE" pin is taken to +5v. In hardware mute mode, the output of the amplifier is disconnected from the output bond pad by turning off a series pass gate. The compensation of the amplifier is switched out of the circuit and the amplifier is operating as a high gain comparator. An offset calibration current is injected into the first stage p-channel current sources with the output of the amplifier itself indicating the polarity of the offset. The digital control logic of the calibration forces the calibration current to servo out the offset of the open-loop amplifier. When the mute pin is taken back low, the part holds the state of the servo controller thus maintaining a very low offset for the amplifier [4].

As with any precision analog circuit, the on chip power bus routing is of extreme importance to insure the channel to channel cross talk is minimized along with keeping artifacts of the digital control signals out of the analog signal paths. Each analog channel has a separate ground pin which further improves channel to channel cross talk.

3.0 DIGITAL CONTROL

The digital control port interface is a 3 pin interface consisting of a Chip Select pin, a Serial Data Input pin, and a Serial Clock pin. There is also a Serial Data Output pin to allow easy daisy chaining of several volume control parts. This is achieved by connecting together the Chip Select pin on all of the parts. The Serial Clock pin must also be connected together on all of the parts. The Serial Data Output pin of the first unit in the chain is connected to the Serial Data Input of the second unit in the chain. Likewise, the Serial Data Output pin of the second unit in the chain is connected to the Serial Data Input of the third unit in the chain. This sequence continues on until all units are connected. This is a very useful feature in multi-channel mixing boards, or in distributed speaker based intercom/music system, where the individual speaker volume can be tailored to the environment. Figure 4 is a diagram showing 3 volume control parts connected in a daisy chain.

To change the volume setting of the part, a 16 bit word must be written to the volume control registers via the control port. To write a new volume setting the Chip Select pin is held low, then the Serial Data Clock strobes in a 16 bit Serial Data Input word one bit at a time. Figure 5 shows the timing diagram. After the new volume setting is written to the control port, the Chip Select pin must be taken back high and held there. In order to allow correct timing in "daisy chained" parts, the Serial Data Input is latched into the part on rising edges of Serial Clock while the Serial Data Output changes value on the falling edges of the Serial Clock. Serial Data Output has a 16 bit data latency from a Serial Data Input.

4.0 MISCELLANEOUS FUNCTIONS

A common problem with digitally controlled analog circuits is zipper noise. Zipper noise is a "pop" or "click" introduced into the audio channel caused by steps in amplitude during volume control changes. There is a pin selectable feature on the part that only allows analog channel volume changes to occur when the audio signal is passing through a zero crossing or when a built in timer times out 0.1 seconds. The built in timer is to insure that the volume setting will change even when there is no zero crossing of the analog signal. The two analog channels have separate zero crossing detectors to insure that volume changes to each channel will occur independently. To reduce digital noise, the built in timer is only operational during changes in the volume setting. The built in timer and zero crossing detectors are disabled when the zipper noise reduction feature is not selected. When the zipper noise reduction feature is not selected, the analog volume setting will change immediately after the Chip Select pin is taken high.

When the part is initially powered up, a power-on-reset circuit is activated which clears all registers to an all zero's state. This all zero's state is also known as "soft mute". In "soft mute" mode the input to the buffer amplifier is connected to "analog ground". This prevents any audible audio signal from being passed from the analog input, through the buffer amplifier, to the analog output. This "soft mute" mode is also activated when a volume control setting of all zero's is written to the control port.

5.0 MEASURED RESULTS

The data presented in Figures 6 & 7 was generated by an Audio Precision System One analyzer. The bandwidth of the analyzer was limited to 22kHz with a sample rate of 44.1kHz. The part was placed into unity gain for these tests and has an output load capacitance of 100pF.

Figure 6 is a plot of three curves showing total harmonic distortion + noise vs. frequency for a 2V rms input. The first curve (best THD) is for an open circuit load, the second curve is for a load of 2k ohms, the third curve (worst THD) is for a load of 600 ohms.

Figure 7 is a family of curves showing output total harmonic distortion + noise vs. frequency for three different input amplitudes. The input amplitudes were 1V rms, 2V rms, and 2.8V_{rms}. All these curves were for an open circuit load.

Figure 8 is a plot of output attenuation amplitude vs. input code. This data was generated using a precision 7 digit DVM and a precision low noise dc voltage source. The deviation of the lab data from that of the ideal line at high attenuation is due to series ground resistance in the analog ground leads.

Table 1 show all the critical analog characteristics for the part.

6.0 CONCLUSION

A digitally controlled single chip stereo volume control has been discussed. The performance levels, cost and power consumption achieved make this device suitable for a wide variety of applications.

7.0 ACKNOWLEDGMENTS

We would like to thank Dave Souydalay and Pat Radzik for the layout of the chip, A. Ganesan for the design of the chip's master current bias generator and help in review of this paper, Mark Hagen and Joel George for taking lab data, and Steve Harris for help in review of this paper and help in preparing a print quality manuscript.

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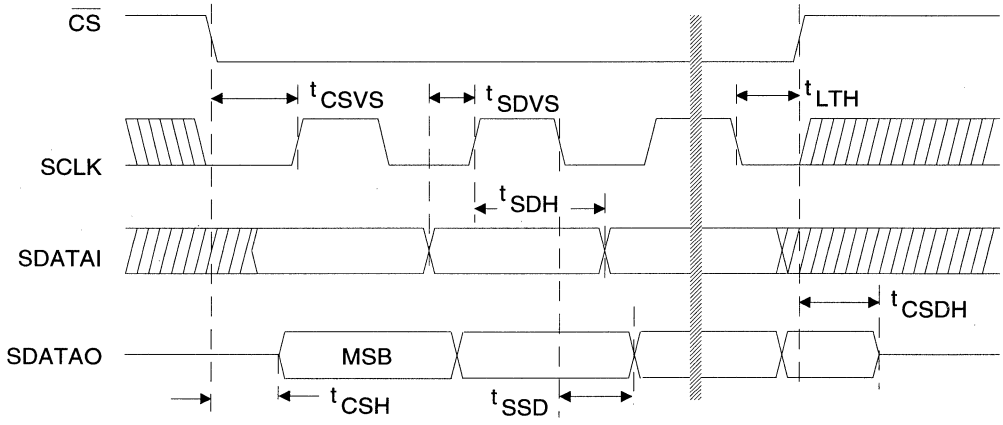

Figure 5. Digital Timing Diagram

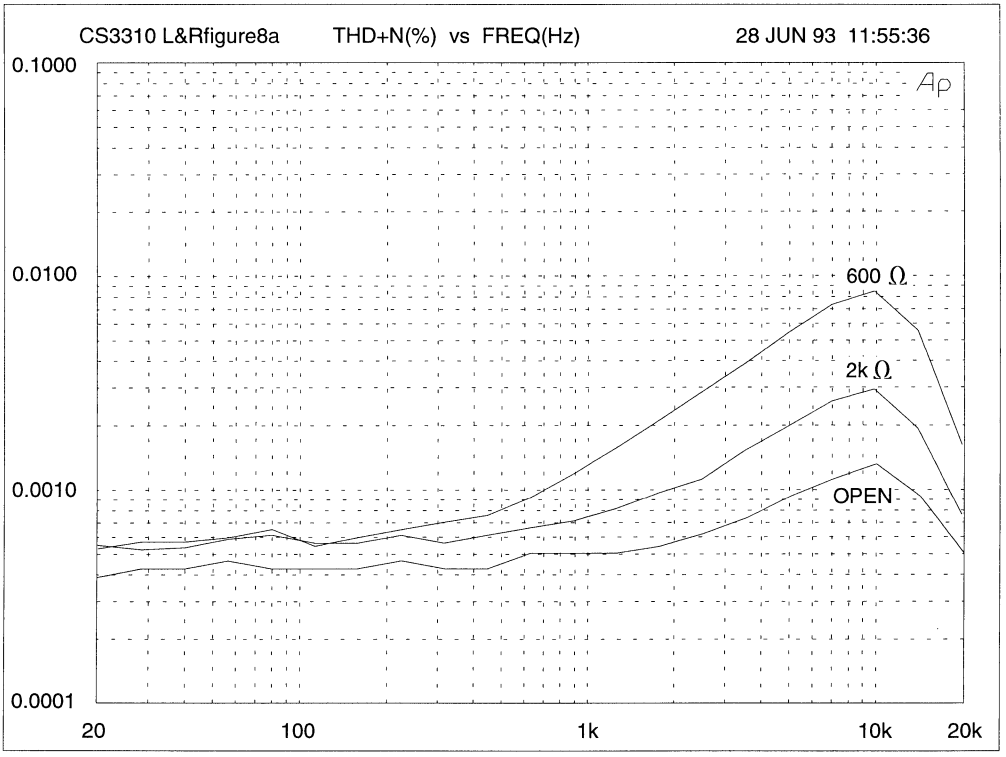

Figure 6. THD+N vs. Frequency
$2V_{RMS}$ Ouptut Signal, Volume Set to 0 dB
LOAD = 600 ohm, 2 kohm, open ckt

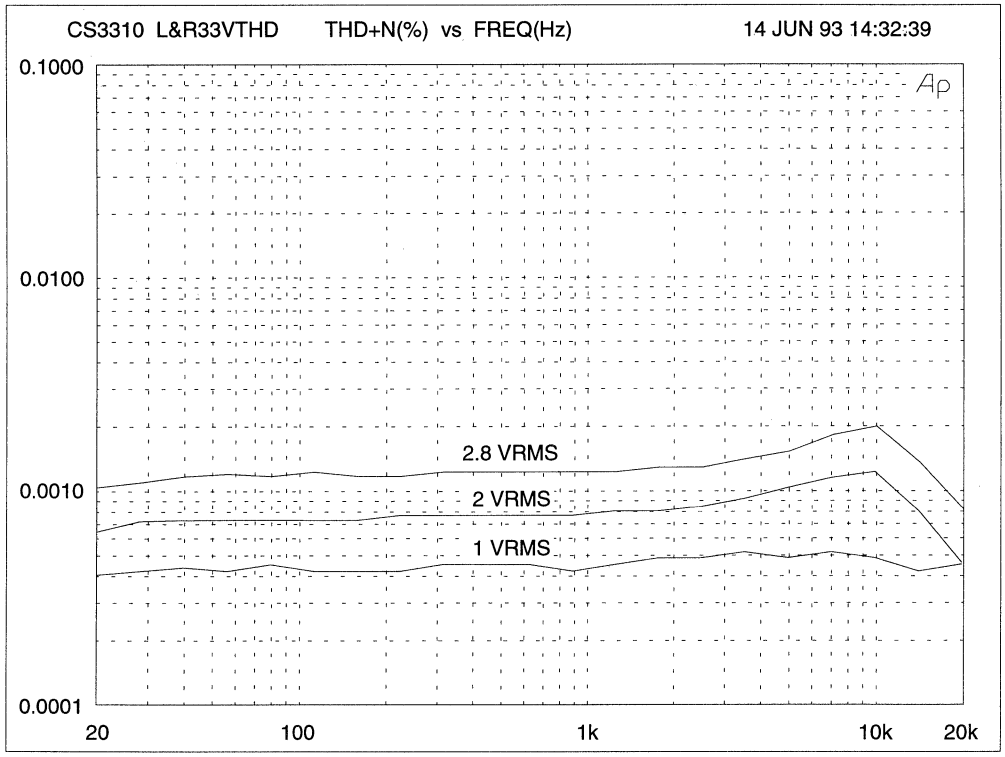

Figure 7. THD+N vs. Frequency
Volume Set to 0 dB, LOAD = open ckt,
Signal = 1 V_{RMS}, 2 V_{RMS}, 2.8 V_{RMS}

ANALOG CHARACTERISTICS

(T_A = 25 °C, VA+, VD+ = 5V ± 5%; VA- = -5V ± 5%; R_L = 2kΩ ; C_L = 20 pF;
10 Hz to 20 kHz Measurement Bandwidth ; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
DC Characteristics					
Step Size		-	0.5	-	dB
Gain Error (31.5 dB Gain)		-	±0.05	-	dB
Gain Matching Between Channels		-	±0.05	-	dB
Input Resistance	RIN	-	10	-	kΩ
Input Capacitance	C_{IN}		25		pF
AC Characteristics					
Total Harmonic Distortion plus Noise (V_{in} = 2V_{rms}, 1 kHz)	THD+N	-	0.001	0.0025	%
Dynamic Range		105	110	-	dB
Input/Output Voltage Range		(VA-)+1.25	-	(VA+)-1.25	V
Output Noise (Note 1)		-	8.4	15	µVrms
Digital Feedthrough (Peak Component)		-80	-	-	dB
Interchannel Isolation (1 kHz)		-100	-110	-	dB
Output Buffer					
Offset Voltage (Note 1)	V_{OS}	-	0.25	0.75	mV
Load Capacitance		-	-	100	pF
Short Circuit Current		-	20	-	mA
Unity Gain Bandwidth, Small Signal (Note 2)		2	-	-	MHz
Power Supplies					
Supply Current (No Load, AIN = 0V)	IA+ IA- ID+	- - -	5.0 5.0 350	8.0 8.0 800	mA mA µA
Power Consumption	P_D	-	52.0	84.0	mW
Power Supply Rejection Ratio (250 Hz)	PSRR	-	80	-	dB

Notes: 1. Measured with input grounded and Gain = 1. Will increase as a function of Gain settings >1.
2. This parameter is guaranteed by design and/or characterization.

8

Table 1. Analog Characteristics

•Notes•

A Tutorial on MIDI and Wavetable Music Synthesis

by
Jim Heckroth

Introduction

The Musical Instrument Digital Interface (MIDI) protocol has been widely accepted and utilized by musicians and composers since its conception in the 1982/1983 time frame. MIDI data is a very efficient method of representing musical performance information, and this makes MIDI an attractive protocol for computer applications which produce sound, such as multimedia presentations or computer games. However, the lack of standardization of synthesizer capabilities hindered applications developers and presented MIDI users with a rather steep learning curve to overcome. Fortunately, thanks to the publication of the General MIDI System specification, wide acceptance of the most common PC/MIDI interfaces, support for MIDI in Microsoft WINDOWS, and the evolution of low-cost high-quality wavetable music synthesizers, the MIDI protocol is now seeing widespread use in a growing number of applications. This paper gives a brief overview of the standards and terminology associated with the generation of sound using the MIDI protocol and wavetable music synthesizers.

Use of MIDI in Multimedia Applications

Originally developed to allow musicians to connect synthesizers together, the MIDI protocol is now finding widespread use in the generation of sound for games and multimedia applications. There are several advantages to generating sound with a MIDI synthesizer rather than using sampled audio from disk or CD-ROM. The first advantage is storage space. Data files used to store digitally sampled audio in PCM format (such as .WAV files) tend to be quite large. This is especially true for lengthy musical pieces captured in stereo using high sampling rates. MIDI data files, on the other hand, are extremely small when compared with sampled audio files. For instance, files containing high quality stereo sampled audio require about 10 MBytes of data per minute of sound, while a typical MIDI sequence might consume less than 10 KBytes of data per minute of sound. This is because the MIDI file does not contain the sampled audio data, it contains only the instructions needed by a synthesizer to play the sounds. These instructions are in the form of MIDI messages, which instruct the synthesizer which sounds to use, which notes to play, and how loud to play each note. The actual sounds are then generated by the synthesizer.

The smaller file size also means that less of the PCs bandwidth is utilized in spooling this data out to the peripheral which is generating sound. Other advantages of utilizing MIDI to generate sounds include the ability to easily edit the music, and the ability to change the playback speed and the pitch or key of the sounds independently. This last point is particularly important in synthesis applications such as

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karaoke equipment, where the musical key and tempo of a song may be selected by the user.

MIDI Systems

The Musical Instrument Digital Interface (MIDI) protocol provides a standardized and efficient means of conveying musical performance information as electronic data. MIDI information is transmitted in "MIDI messages", which can be thought of as instructions which tell a music synthesizer how to play a piece of music. The Synthesizer receiving the MIDI data must generate the actual sounds. The MIDI 1.0 Detailed Specification, published by the International MIDI Association, provides a complete description of the MIDI protocol.

The MIDI data stream is a unidirectional asynchronous bit stream at 31.25 kbits/sec. with 10 bits transmitted per byte (a start bit, 8 data bits, and one stop bit). The MIDI interface on a MIDI instrument will generally include three different MIDI connectors, labeled IN, OUT, and THRU. The MIDI data stream is usually originated by a MIDI controller, such as a musical instrument keyboard, or by a MIDI sequencer. A MIDI controller is a device which is played as an instrument, and it translates the performance into a MIDI data stream in real time (as it is played). A MIDI sequencer is a device which allows MIDI data sequences to be captured, stored, edited, combined, and replayed. The MIDI data output from a MIDI controller or sequencer is transmitted via the devices' MIDI OUT connector.

The recipient of this MIDI data stream is commonly a MIDI sound generator or sound module, which will receive MIDI messages at its MIDI IN connector, and respond to these messages by playing sounds. Figure 1 shows a simple MIDI system, consisting of a MIDI keyboard controller and a MIDI sound module. Note that many MIDI keyboard instruments include both the keyboard controller and the MIDI sound module functions within the same unit. In these units, there is an internal link between the keyboard and the sound module which may be enabled or disabled by setting the "local control" function of the instrument to ON or OFF respectively.

The single physical MIDI channel is divided into 16 logical channels by the inclusion of a 4 bit channel number within many of the MIDI messages. A musical instrument keyboard can generally be set to transmit on any one of the sixteen MIDI channels. A MIDI sound source, or sound module, can be set to receive on specific MIDI channel(s). In the system depicted in Figure 1, the sound module would have to be set to receive the channel which the keyboard controller is transmitting on in order to play sounds.

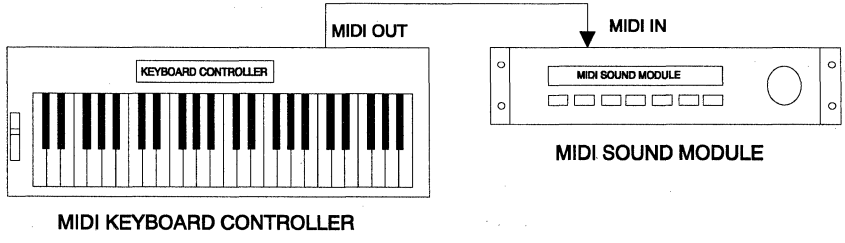

Figure 1: A Simple MIDI System

Information received on the MIDI IN connector of a MIDI device is transmitted back out (repeated) at the devices' MIDI THRU connector. Several MIDI sound modules can be daisy-chained by connecting the THRU output of one device to the IN connector of the next device downstream in the chain.

Figure 2 shows a more elaborate MIDI system. In this case, a MIDI keyboard controller is used as an input device to a MIDI sequencer, and there are several sound modules connected to the sequencer's MIDI OUT port. A composer might utilize a system like this to write a piece of music consisting of several different parts, where each part is written for a different instrument. The composer would play the individual parts on the keyboard one at a time, and these individual parts would be captured by the sequencer. The sequencer would then play the parts back together through the sound modules. Each part would be played on a different MIDI channel, and the sound modules would be set to receive different channels. For example, Sound module number 1 might be set to play the part received on channel 1 using a piano sound, while module 2 plays the information received on channel 5 using an acoustic bass sound, and the drum machine plays the percussion part received on MIDI channel 10.

In the last example, a different sound module is used to play each part. However, sound modules which are "multi-timbral" are capable of playing several different parts simultaneously. A single multi-timbral sound module might be configured to receive the piano part on channel 1, the bass part on channel 5, and the drum part on channel 10, and would play all three parts simultaneously.

Figure 3 depicts a PC-based MIDI system. In this system, the PC is equipped with an internal MIDI interface card which sends MIDI data to an external multi-timbral MIDI synthesizer module. Application software, such as Multimedia presentation packages, educational software, or games, send information to the MIDI interface card over the PC bus. The MIDI interface converts this information into MIDI messages which are sent to the sound module. Since this is a multi-timbral module, it can play many different musical parts, such as piano, bass and drums, at the same time. Sophisticated

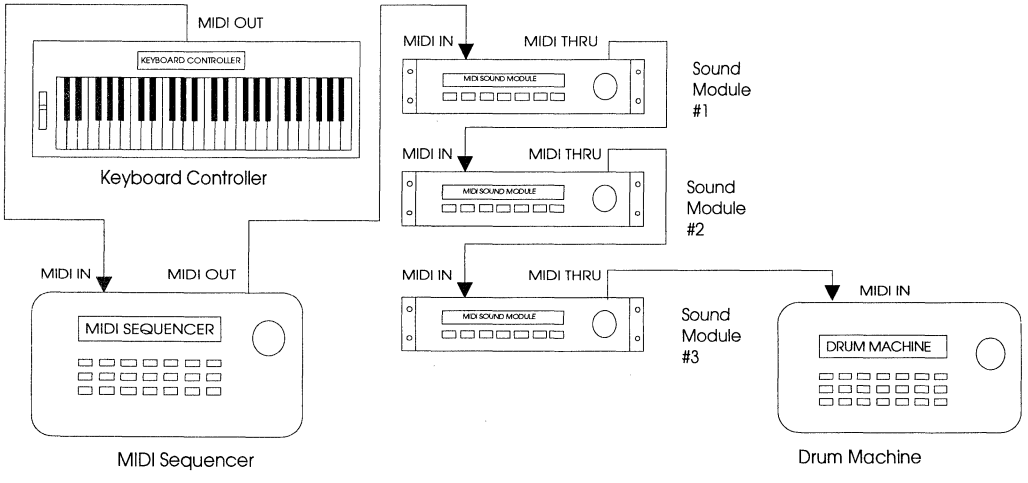

Figure 2: An Expanded MIDI System

MIDI sequencer software packages are also available for the PC. With this software running on the PC, a user could connect a MIDI keyboard controller to the MIDI IN port of the MIDI interface card, and have the same music composition capabilities discussed in the last paragraph.

There are a number of different configurations of PC-based MIDI systems possible. For instance, the MIDI interface and the MIDI sound module might be combined on the PC add-in card. In fact, the Microsoft Multimedia PC (MPC) Specification states that a PC add-in sound card must have an on-board synthesizer in order to be MPC compliant. Until recently, most MPC compliant sound cards included FM synthesizers with limited capabilities and marginal sound quality. With these systems, an external wavetable synthesizer module might be added to get better sound quality. Recently, more advanced sound cards have been appearing which include high quality wavetable music synthesizers on-board, or as a daughter-card options. With the increasing use of the MIDI protocol in PC applications, this trend is sure to continue.

MIDI Messages

A MIDI message is made up of an eight bit status byte which is generally followed by one or two data bytes. There are a number of different types of MIDI messages. At the highest level, MIDI messages are classified as being either Channel Messages or System Messages. Channel messages are those which apply to a specific channel, and the channel number is included in the status byte for these messages. System messages are not channel specific, and no channel number is indicated in their status bytes. Channel Messages may be further classified as being either Channel Voice Messages, or Mode Messages. Channel Voice Messages carry musical performance data, and these messages comprise most of the traffic in a typical MIDI data stream. Channel Mode messages affect the way a receiving instrument will respond to the Channel Voice messages. MIDI System Messages are classified as being System Common Messages, System Real Time

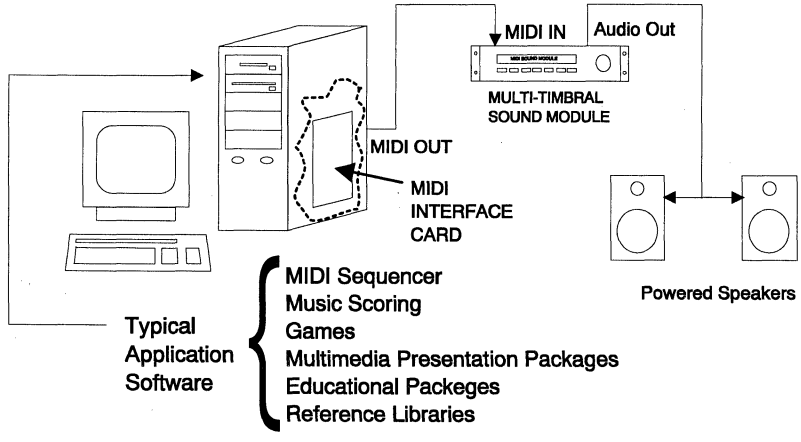

Figure 3: PC-Based MIDI System

Messages, or System Exclusive Messages. System Common messages are intended for all receivers in the system. System Real Time messages are used for synchronization between clock-based MIDI components. System Exclusive messages include a Manufacturer's Identification (ID) code, and are used to transfer any number of data bytes in a format specified by the referenced manufacturer. The various classes of MIDI messages are discussed in more detail in the following paragraphs.

Channel Voice Messages

Channel Voice Messages are used to send musical performance information. The messages in this category are the Note On, Note Off, Polyphonic Key Pressure, Channel Pressure, Pitch Bend Change, Program Change, and the Control Change message.

In MIDI systems, the activation of a particular note and the release of the same note are considered as two separate events. When a key is pressed on a MIDI keyboard instrument or MIDI keyboard controller, the keyboard sends a Note On message on the MIDI OUT port. The keyboard may be set to transmit on any one of the sixteen logical MIDI channels, and the status byte for the Note On message will indicate the selected channel number. The Note On status byte is followed by two data bytes, which specify key number (indicating which key was pressed) and velocity (how hard the key was pressed). The key number is used in the receiving synthesizer to select which note should be played, and the velocity is normally used to control the amplitude of the note. When the key is released, the keyboard instrument or controller will send a Note Off message. The Note Off message also includes data bytes for the key number and for the velocity with which the key was released. The Note Off velocity information is normally ignored.

Some MIDI keyboard instruments have the ability to sense the amount of pressure which is being applied to the keys while they are depressed. This pressure information, commonly called "aftertouch", may be used to control some aspects of the sound produced by the synthesizer (vibrato, for example). If the keyboard has a pressure sensor for each key, then the resulting "polyphonic aftertouch" information would be sent in the form of Polyphonic Key Pressure messages. These messages include separate data bytes for key number and pressure amount. It is currently more common for keyboard instruments to sense only a single pressure level for the entire keyboard. This "channel aftertouch" information is sent using the Channel Pressure message, which needs only one data byte to specify the pressure value.

The Pitch Bend Change message is normally sent from a keyboard instrument in response to changes in position of the pitch bend wheel. The pitch bend information is used to modify the pitch of sounds being played on a given channel. The Pitch Bend message includes two data bytes to specify the pitch bend value. Two bytes are required to allow fine enough resolution to make pitch changes resulting from movement of the pitch bend wheel seem to occur in a continuous manner rather than in steps.

The Program Change message is used to specify the type of instrument which should be used to play sounds on a given channel. This message needs only one data byte which specifies the new program number.

MIDI Control Change messages are used to control a wide variety of functions in a synthesizer. Control Change messages, like other MIDI channel messages, should only affect the channel number indicated in the status byte. The control change status byte is followed by one data byte indicating the "controller number", and a second byte which specifies the "control value". The controller number identifies which

function of the synthesizer is to be controlled by the message.

Controller Numbers 0 - 31 are generally used for sending data from switches, wheels, faders, or pedals on a MIDI controller device such as a musical instrument keyboard. Control numbers 32 - 63 are used to send an optional Least Significant Byte (LSB) for control numbers 0 through 31, respectively. Some examples of synthesizer functions which may be controlled are modulation (controller number 1), volume (controller number 7), and pan (controller number 10). Controller numbers 64 through 67 are used for switched functions. these are the sustain/damper pedal (controller number 64), portamento (controller number 65), sostenuto pedal (controller number 66), and soft pedal (controller number 67). Controller numbers 16-19 and 80-83 are defined to be general purpose controllers, and controller numbers 48-51 may be used to send an optional LSB for controller numbers 16-19. Several of the MIDI controllers merit more detailed descriptions, and these controllers are described in the following paragraphs.

Controller number zero is defined as the bank select. The bank select function is used in some synthesizers in conjunction with the MIDI Program Change message to expand the number of different instrument sounds which may be specified (the Program Change message alone allows selection of one of 128 possible program numbers). The additional sounds are commonly organized as "variations" of the 128 addressed by the Program Change message. Variations are selected by preceding the Program Change message with a Control Change message which specifies a new value for controller zero (see the Roland General Synthesizer Standard topic covered later in this paper).

Controller numbers 91 through 95 may be used to control the depth or level of special effects, such as reverb or chorus, in synthesizers which have these capabilities.

Controller number 6 (Data Entry), in conjunction with Controller numbers 96 (Data Increment), 97 (Data Decrement), 98 (Registered Parameter Number LSB), 99 (Registered Parameter Number MSB), 100 (Non-Registered Parameter Number LSB), and 101 (Non-Registered Parameter Number MSB), may be used to send parameter data to a synthesizer in order to edit sound patches. Registered parameters are those which have been assigned some particular function by the MIDI Manufacturers Association (MMA) and the Japan MIDI Standards Committee (JMSC). For example, there are Registered Parameter numbers assigned to control pitch bend sensitivity and master tuning for a synthesizer. Non-Registered parameters have not been assigned specific functions, and may be used for different functions by different manufacturers. Parameter data is transferred by first selecting the parameter number to be edited using controllers 98 and 99 or 100 and 101, and then adjusting the data value for that parameter using controller number 6, 96, or 97.

Controller Numbers 121 through 127 are used to implement the MIDI "Channel Mode Messages". These messages are covered in the next section.

Channel Mode Messages

Channel Mode messages (MIDI controller numbers 121 through 127) affect the way a synthesizer responds to MIDI data. Controller number 121 is used to reset all controllers. Controller number 122 is used to enable or disable Local Control (In a MIDI synthesizer which has it's own keyboard, the functions of the keyboard controller and the synthesizer can be isolated by turning Local Control off). Controller numbers 124 through 127 are used to select between Omni Mode On or Off, and to

select between the Mono Mode or Poly Mode of operation.

When Omni mode is On, the synthesizer will respond to incoming MIDI data on all channels. When Omni mode is Off, the synthesizer will only respond to MIDI messages on one channel. When Poly mode is selected, incoming Note On messages are played polyphonically. This means that when multiple Note On messages are received, each note is assigned its own voice (subject to the number of voices available in the synthesizer). The result is that multiple notes are played at the same time. When Mono mode is selected, a single voice is assigned per MIDI channel. This means that only one note can be played on a given channel at a given time. Most modern MIDI synthesizers will default to Omni On/Poly mode of operation. In this mode, the synthesizer will play note messages received on any MIDI channel, and notes received on each channel are played polyphonically. In the Omni Off/Poly mode of operation, the synthesizer will receive on a single channel and play the notes received on this channel polyphonically. This mode is useful when several synthesizers are daisy-chained using MIDI THRU. In this case each synthesizer in the chain can be set to play one part (the MIDI data on one channel), and ignore the information related to the other parts.

Note that a MIDI instrument has one MIDI channel which is designated as its "Basic Channel". The Basic Channel assignment may be hard-wired, or it may be selectable. Mode messages can only be received by an instrument on the Basic Channel.

System Common Messages

The System Common Messages which are currently defined include MTC Quarter Frame, Song Select, Song Position Pointer, Tune Request, and End Of Exclusive (EOX). The MTC Quarter Frame message is part of the MIDI Time Code information used for synchronization of MIDI equipment and other equipment, such as audio or video tape machines.

The Song Select message is used with MIDI equipment, such as sequencers or drum machines, which can store and recall a number of different songs. The Song Position Pointer is used to set a sequencer to start playback of a song at some point other than at the beginning. The Song Position Pointer value is related to the number of MIDI clocks which would have elapsed between the beginning of the song and the desired point in the song. This message can only be used with equipment which recognizes MIDI System Real Time Messages (MIDI Sync).

The Tune Request message is generally used to request an analog synthesizer to retune its' internal oscillators. This message is generally not needed with digital synthesizers.

The EOX message is used to flag the end of a System Exclusive message, which can include a variable number of data bytes.

System Real Time Messages

The MIDI System Real Time messages are used to synchronize all of the MIDI clock-based equipment within a system, such as sequencers and drum machines. Most of the System Real Time messages are normally ignored by keyboard instruments and synthesizers. To help ensure accurate timing, System Real Time messages are given priority over other messages, and these single-byte messages may occur anywhere in the data stream (a Real Time message may appear between the status byte and data byte of some other MIDI message). The System Real Time messages are the Timing Clock, Start, Continue, Stop, Active Sensing, and the System Reset message. The Timing Clock message is the master clock which sets the

tempo for playback of a sequence. The Timing Clock message is sent 24 times per quarter note. The Start, Continue, and Stop messages are used to control playback of the sequence.

The Active Sensing signal is used to help eliminate "stuck notes" which may occur if a MIDI cable is disconnected during playback of a MIDI sequence. Without Active Sensing, if a cable is disconnected during playback, then some notes may be left playing indefinitely because they have been activated by a Note On message, but will never receive the Note Off. In transmitters which utilize Active Sensing, the Active Sensing message is sent once every 300 ms by the transmitting device when this device has no other MIDI data to send. If a receiver who is monitoring Active Sensing does not receive any type of MIDI messages for a period of time exceeding 300 ms, the receiver may assume that the MIDI cable has been disconnected, and it should therefore turn off all of its' active notes. Use of Active Sensing in MIDI transmitters and receivers is optional.

The System Reset message, as the name implies, is used to reset and initialize any equipment which receives the message. This message is generally not sent automatically by transmitting devices, and must be initiated manually by a user.

System Exclusive Messages

System Exclusive messages may be used to send data such as patch parameters or sample data between MIDI devices. Manufacturers of MIDI equipment may define their own formats for System Exclusive data. Manufacturers are granted unique identification (ID) numbers by the MMA or the JMSC, and the manufacturer ID number is included as the second byte of the System Exclusive message. The manufacturers ID byte is followed by any number of data bytes, and the data transmission is terminated with the EOX message. Manufacturers are required to publish the details of their System Exclusive data formats, and other manufacturers may freely utilize these formats, provided that they do not alter or utilize the format in a way which conflicts with the original manufacturers specifications.

There is also a MIDI Sample Dump Standard, which is a System Exclusive data format defined in the MIDI specification for the transmission of sample data between MIDI devices.

Running Status

MIDI data is transmitted serially. Musical events which originally occurred at the same time must be sent one at a time in the MIDI data stream, and therefore these events will not actually be played at exactly the same time. However, the resulting delays are generally short enough that the events are perceived as having occurred simultaneously. The MIDI data transmission rate is 31.35 kbit/s with 10 bits transmitted per byte of MIDI data. Thus, a 3 byte Note On or Note Off message takes about 1 ms to be sent. For a person playing a MIDI instrument keyboard, the time skew between playback of notes when 10 keys are pressed simultaneously should not exceed 10 ms, and this would not be perceptible. However, MIDI data being sent from a sequencer can include a number of different parts. On a given beat, there may be a large number of musical events which should occur simultaneously, and the delays introduced by serialization of this information might be noticeable.

To help reduce the amount of data transmitted in the MIDI data stream, a technique called "running status" may be employed. It is very common for a string of consecutive messages to be of the same message type. For instance, when a chord is played on a keyboard, 10 successive Note On messages may be generated,

followed by 10 Note Off messages. When running status is used, a status byte is sent for a message only when the message is not of the same type as the last message sent on the same channel. The status byte for subsequent messages of the same type may be omitted (only the data bytes are sent for these subsequent messages). The effectiveness of running status can be enhanced by sending Note On messages with a velocity of zero in place of Note Off messages. In this case, long strings of Note On messages will often occur. Changes in some of the the MIDI controllers or movement of the pitch bend wheel on a musical instrument can produce a staggering number of MIDI channel voice messages, and running status can also help a great deal in these instances.

MIDI Sequencers and Standard MIDI files

MIDI messages are received and processed by a MIDI synthesizer in real time. When the synthesizer receives a MIDI "note on" message it plays the appropriate sound. When the corresponding "note off" message is received, the synthesizer turns the note off. If the source of the MIDI data is a musical instrument keyboard, then this data is being generated in real time. When a key is pressed on the keyboard, a "note on" message is generated in real time. In these real time applications, there is no need for timing information to be sent along with the MIDI messages. However, if the MIDI data is to be stored as a data file, and/or edited using a sequencer, then some form of "time-stamping" for the MIDI messages is required.

The International MIDI Association publishes a Standard MIDI Files specification, which provides a standardized method for handling time-stamped MIDI data. This standardized file format for time-stamped MIDI data allows different applications, such as sequencers, scoring packages, and multimedia presentation software, to share MIDI data files.

The specification for Standard MIDI Files defines three formats for MIDI files. MIDI sequencers can generally manage multiple MIDI data streams, or "tracks". MIDI files having Format 0 must store all of the MIDI sequence data on a single track. This is generally useful only for simple "single track" devices. Format 1 files, which are the most commonly used, store data as a collection of tracks. Format 2 files can store several independent patterns.

Synthesizer Polyphony and Timbres

The polyphony of a sound generator refers to its ability to play more than one note at a time. Polyphony is generally measured or specified as a number of notes or voices. Most of the early music synthesizers were monophonic, meaning that they could only play one note at a time. If you pressed five keys simultaneously on the keyboard of a monophonic synthesizer, you would only hear one note. Pressing five keys on the keyboard of a synthesizer which was polyphonic with four voices of polyphony would, in general, produce four notes. If the keyboard had more voices (many modern sound modules have 16, 24, or 32 note polyphony), then you would hear all five of the notes.

The different sounds that a synthesizer or sound generator can produce are often referred to as "patches", "programs", "algorithms", sounds, or "timbres". Modern synthesizers commonly use program numbers to represent different sounds they produce. Sounds may then be selected by specifying the program numbers (or patch numbers) for the desired sound. For instance, a sound module might use patch number 1 for its acoustic piano sound, and patch number 36 for

its fretless bass sound. The association of patch numbers to sounds is often referred to as a patch map. A MIDI Program Change message is used to tell a device receiving on a given channel to change the instrument sound being used. For example, a sequencer could set up devices on channel 4 to play fretless bass sounds by sending a Program Change message for channel four with a data byte value of 36 (this is the General MIDI program number for the fretless bass patch).

A synthesizer or sound generator is said to be multi-timbral if it is capable of producing two or more different instrument sounds simultaneously. Again, if a synthesizer can play five notes simultaneously, then it is polyphonic. If it can produce a piano sound and an acoustic bass sound at the same time, then it is also multi-timbral. A synthesizer or sound module which has 24 notes of polyphony and which is 6 part multi-timbral (capable of producing 6 different timbres simultaneously) could synthesize the sound of a 6 piece band or orchestra. A sequencer could send MIDI messages for a piano part on channel 1, bass on channel 2, saxophone on channel 3, drums on channel 10, etc. A 16 part multi-timbral synthesizer could receive a different part on each of MIDI's 16 logical channels.

The polyphony of a multi-timbral synthesizer is usually allocated dynamically among the different parts (timbres) being used. In our example, at a given instant five voices might be used for the piano part, two voices for the bass, one for the saxophone, and 6 voices for the drums, leaving 10 voices free. Note that some sounds utilize more than one voice, so the number of notes which may be produced simultaneously may be less than the stated polyphony of the synthesizer, depending on which sounds are being utilized.

The General MIDI (GM) System

At the beginning of a MIDI sequence, a Program Change message is usually sent on each channel used in the piece in order to set up the appropriate instrument sound for each part. The Program Change message tells the synthesizer which patch number should be used for a particular MIDI channel. If the synthesizer receiving the MIDI sequence uses the same patch map (the assignment of patch numbers to sounds) that was used in the composition of the sequence, then the sounds will be assigned as intended. Unfortunately, prior to General MIDI, there was no standard for the relationship of patch numbers to specific sounds for synthesizers. Thus, a MIDI sequence might produce different sounds when played on different synthesizers, even though the synthesizers had comparable types of sounds. For example, if the composer had selected patch number 5 for channel 1, intending this to be an electric piano sound, but the synthesizer playing the MIDI data had a tuba sound mapped at patch number 5, then the notes intended for the piano would be played on the tuba when using this synthesizer (even though this synthesizer may have a fine electric piano sound available at some other patch number).

The General MIDI (GM) Specification, published by the International MIDI Association, defines a set of general capabilities for General MIDI Instruments. The General MIDI Specification includes the definition of a General MIDI Sound Set (a patch map), a General MIDI Percussion map (mapping of percussion sounds to note numbers), and a set of General MIDI Performance capabilities (number of voices, types of MIDI messages recognized, etc.). A MIDI sequence which has been generated for use on a General MIDI Instrument should play correctly on any General MIDI synthesizer or sound module.

The General MIDI system utilizes MIDI channels 1-9 and 11-16 for chromatic instrument sounds, while channel number 10 is utilized for "key-based" percussion sounds. The General MIDI Sound set for channels 1-9 and 11-16 is given in table 1. These instrument sounds are grouped into "sets" of related sounds. For example, program numbers 1-8 are piano sounds, 6-16 are chromatic percussion sounds, 17-24 are organ sounds, 25-32 are guitar sounds, etc.

For the instrument sounds on channels 1-9 and 11-16, the note number in a Note On message is used to select the pitch of the sound which will be played. For example if the Vibraphone instrument (program number 12) has been selected on channel 3, then playing note number 60 on channel 3 would play the middle C note (this would be the default note to pitch assignment on most instruments), and note number 59 on channel 3 would play B below middle C. Both notes would be played using the Vibraphone sound.

The General MIDI percussion map used for channel 10 is given in table 2. For these "key-based" sounds, the note number data in a Note On message is used differently. Note numbers on channel 10 are used to select which drum sound will be played. For example, a Note On message on channel 10 with note number 60 will play a Hi Bongo drum sound. Note number 59 on channel 10 will play the Ride Cymbal 2 sound.

It should be noted that the General MIDI system specifies sounds using program numbers 1 through 128. The MIDI Program Change message used to select these sounds uses an 8-bit byte, which corresponds to decimal numbering from 0 through 127, to specify the desired program number. Thus, to select GM sound number 10, the Glockenspiel, the Program Change message will have a data byte with the decimal value 9.

The General MIDI system specifies which instrument or sound corresponds with each program/patch number, but General MIDI does not specify how these sounds are produced. Thus, program number 1 should select the Acoustic Grand Piano sound on any General MIDI instrument. However, the Acoustic Grand Piano sound on two General MIDI synthesizers which use different synthesis techniques may sound quite different.

The Roland General Synthesizer (GS) Standard

The Roland General Synthesizer (GS) functions are a superset of those specified for General MIDI. The GS system includes all of the GM sounds (which are referred to as "capital instrument" sounds), and adds new sounds which are organized as variations of the capital instruments.

Variations are selected using the MIDI Control Change message in conjunction with the Program Change message. The Control Change message is sent first, and it is used to set controller number 0 to some specified nonzero value indicating the desired variation (some capital sounds have several different variations). The Control Change message is followed by a MIDI Program Change message which indicates the program number of the related capital instrument. For example, Capital instrument number 25 is the Nylon String Guitar. The Ukulele is a variation of this instrument. The Ukulele is selected by sending a Control Change message which sets controller number 0 to a value of 8, followed by a program change message on the same channel which selects program number 25. Sending the Program change message alone would select the capital instrument, the Nylon String Guitar. Note also that a Control Change of controller number 0 to a value of 0 followed by a Program Change message would also select the capital instrument.

Prog#	Instrument Name	Prog#	Instrument Name	Prog#	Instrument Name
1	Acoustic Grand Piano	44	Contrabass	87	Lead 7 (fifths)
2	Bright Acoustic Piano	45	Tremolo Strings	88	Lead 8 (bass + lead)
3	Electric Grand Piano	46	Pizzicato Strings	89	Pad 1 (new age)
4	Honky-tonk Piano	47	Orchestral Harp	90	Pad 2 (warm)
5	Electric Piano 1	48	Timpani	91	Pad 3 (polysynth)
6	Electric Piano 2	49	String Ensemble 1	92	Pad 4 (choir)
7	Harpsichord	50	String Ensemble 2	93	Pad 5 (bowed)
8	Clavi	51	SynthStrings 1	94	Pad 6 (metallic)
9	Celesta	52	SynthStrings 2	95	Pad 7 (halo)
10	Glockenspiel	53	Choir Aahs	96	Pad 8 (sweep)
11	Music Box	54	Voice Oohs	97	FX 1 (rain)
12	Vibraphone	55	Synth Voice	98	FX 2 (soundtrack)
13	Marimba	56	Orchestra Hit	99	FX 3 (crystal)
14	Xylophone	57	Trumpet	100	FX 4 (atmosphere)
15	Tubular Bells	58	Trombone	101	FX 5 (brightness)
16	Dulcimer	59	Tuba	102	FX 6 (goblins)
17	Drawbar Organ	60	Muted Trumpet	103	FX 7 (echoes)
18	Percussive Organ	61	French Horn	104	FX 8 (sci-fi)
19	Rock Organ	62	Brass Section	105	Sitar
20	Church Organ	63	SynthBrass 1	106	Banjo
21	Reed Organ	64	SynthBrass 2	107	Shamisen
22	Accordion	65	Soprano Sax	108	Koto
23	Harmonica	66	Alto Sax	109	Kalimba
24	Tango Accordion	67	Tenor Sax	110	Bag pipe
25	Acoustic Guitar (nylon)	68	Baritone Sax	111	Fiddle
26	Acoustic Guitar (steel)	69	Oboe	112	Shanai
27	Electric Guitar (jazz)	70	English Horn	113	Tinkle Bell
28	Electric Guitar (clean)	71	Bassoon	114	Agogo
29	Electric Guitar (muted)	72	Clarinet	115	Steel Drums
30	Overdriven Guitar	73	Piccolo	116	Woodblock
31	Distortion Guitar	74	Flute	117	Taiko Drum
32	Guitar harmonics	75	Recorder	118	Melodic Tom
33	Acoustic Bass	76	Pan Flute	119	Synth Drum
34	Electric Bass (finger)	77	Blown Bottle	120	Reverse Cymbal
35	Electric Bass (pick)	78	Shakuhachi	121	Guitar Fret Noise
36	Fretless Bass	79	Whistle	122	Breath Noise
37	Slap Bass 1	80	Ocarina	123	Seashore
38	Slap Bass 2	81	Lead 1 (square)	124	Bird Tweet
39	Synth Bass 1	82	Lead 2 (sawtooth)	125	Telephone Ring
40	Synth Bass 2	83	Lead 3 (calliope)	126	Helicopter
41	Violin	84	Lead 4 (chiff)	127	Applause
42	Viola	85	Lead 5 (charang)	128	Gunshot
43	Cello	86	Lead 6 (voice)		

Table 1: General MIDI Sound Set (All Channels Except 10)

Note #	Drum Sound	Note #	Drum Sound	Note #	Drum Sound
35	Acoustic Bass Drum	51	Ride Cymbal 1	67	High Agogo
36	Bass Drum 1	52	Chinese Cymbal	68	Low Agogo
37	Side Stick	53	Ride Bell	69	Cabasa
38	Acoustic Snare	54	Tambourine	70	Maracas
39	Hand Clap	55	Splash Cymbal	71	Short Whistle
40	Electric Snare	56	Cowbell	72	Long Whistle
41	Low Floor Tom	57	Crash Cymbal 2	73	Short Guiro
42	Closed Hi-Hat	58	Vibraslap	74	Long Guiro
43	High Floor Tom	59	Ride Cymbal 2	75	Claves
44	Pedal Hi-Hat	60	Hi Bongo	76	Hi Wood Block
45	Low Tom	61	Low Bongo	77	Low Wood Block
46	Open Hi-Hat	62	Mute Hi Conga	78	Mute Cuica
47	Low Mid Tom	63	Open Hi Conga	79	Open Cuica
48	Hi Mid Tom	64	Low Conga	80	Mute Triangle
49	Crash Cymbal 1	65	High Timbale	81	Open Triangle
50	High Tom	66	Low Timbale		

Table 2: General MIDI Percussion Map (Channel 10)

The GS system also includes adjustable reverberation and chorus effects. The effects depth for both reverb and chorus may be adjusted on an individual MIDI channel basis using Control Change messages. The type of reverb and chorus sounds employed may also be selected using System Exclusive messages.

Synthesizer Implementations: FM vs. Wavetable

There are a number of different technologies or algorithms used to create sounds in music synthesizers. Two widely used techniques are Frequency Modulation (FM) synthesis and Wavetable synthesis. FM synthesis techniques generally use one periodic signal (the modulator) to modulate the frequency of another signal (the carrier). If the modulating signal is in the audible range, then the result will be a significant change in the timbre of the carrier signal. Each FM voice requires a minimum of two signal generators. These generators are commonly referred to as "operators", and different FM synthesis implementations have varying degrees of control over the operator parameters. Sophisticated FM systems may use 4 or 6 operators per voice, and the operators may have adjustable envelopes which allow adjustment of the attack and decay rates of the signal. Although FM systems were implemented in the analog domain on early synthesizer keyboards, modern FM synthesis implementations are done digitally.

FM synthesis techniques are very useful for creating expressive new synthesized sounds. However, if the goal of the synthesis system is to recreate the sound of some existing instrument, this can generally be done more accurately with digital sample-based techniques. Digital sampling systems store high quality sound samples digitally, and then replay these sounds on demand. Digital sample-based synthesis systems may employ a variety of special techniques, such as sample looping, pitch shifting, mathematical interpolation, and

polyphonic digital filtering, in order to reduce the amount of memory required to store the sound samples (or to get more types of sounds from a given amount of memory). These sample-based synthesis systems are often called "wavetable" synthesizers (the sample memory in these systems contains a large number of sampled sound segments, and can be thought of as a "table" of sound waveforms which may be looked up and utilized when needed). A number of the special techniques employed in this type of synthesis are discussed in the following paragraphs.

Wavetable Synthesis Techniques

Looping and Envelope Generation

One of the primary techniques used in wavetable synthesizers to conserve sample memory space is the looping of sampled sound segments. For a large number of instrument sounds, the sound can be modeled as consisting of two major sections, the attack section and the sustain section. The attack section is the initial part of the sound, where the amplitude and the spectral characteristics of the sound may be changing very rapidly. The sustain section of the sound is that part of the sound following the attack, where the characteristics of the sound are changing less dynamically. Figure 4 shows a waveform with portions which could be considered the attack and the sustain sections indicated. In this example, the spectral characteristics of the waveform remain constant throughout the sustain section, while the amplitude is decreasing at a fairly constant rate. This is an exaggerated example, in most natural instrument sounds, both the spectral characteristics and the amplitude continue to change through the duration of the sound. The sustain section, if one can be identified, is that section for which the characteristics of the sound are relatively constant.

A great deal of memory can be saved in wave-table synthesis systems by storing only a short segment of the sustain section of the waveform, and then looping this segment during playback. Figure 5 shows a two period segment of the sustain section from the waveform in Figure 4, which has been looped to create a steady state signal. If the original sound had a fairly constant spectral content and amplitude during the sustained section, then the sound resulting from this looping operation should be a good approximation of the sustained section of the original.

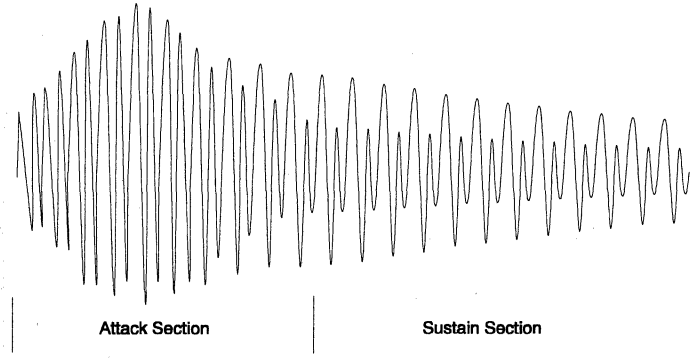

Figure 4: Attack and Sustain Portions of a waveform

For many acoustic string instruments, the spectral characteristics of the sound remain fairly constant during the sustain section, while the amplitude of the signal decays. This can be simulated with a looped segment by multiplying the looped samples by a decreasing gain factor during playback to get the desired shape or envelope. The amplitude envelope of a sound is commonly modeled as consisting of some number of linear segments. An example is the commonly used four part piecewise-linear Attack-Decay-Sustain-Release (ADSR) envelope model. Figure 6 depicts a typical ADSR envelope shape, and Figure 7 shows the result of applying this envelope to the looped waveform from Figure 5.

A typical wavetable synthesis system would store separate sample segments for the attack section and the looped section of an instrument. These sample segments might be referred to as the initial sound and the loop sound. The initial sound is played once through, and then the loop sound is played repetitively until the note ends. An envelope generator function is used to create an envelope which is appropriate for the particular instrument, and this envelope is applied to the output samples during playback. Playback of the initial wave (with the the Attack portion of the envelope applied) begins when a Note On message is received. The length of the initial sound segment is fixed by the number of samples in the segment, and the length of the Attack and Decay sections of the envelope are generally also fixed for a given instrument sound. The sustain section will continue to repeat the loop samples while applying the Sustain envelope slope (which decays slowly in

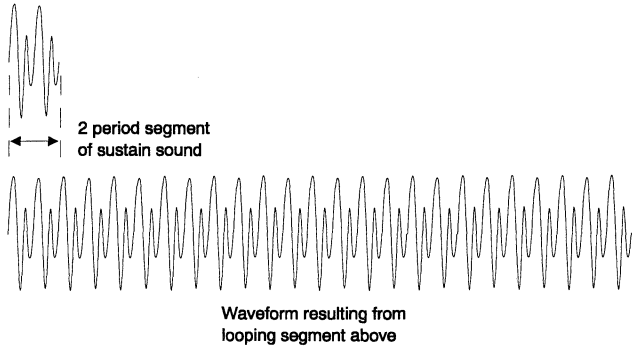

Figure 5: Looping a Sound Segment

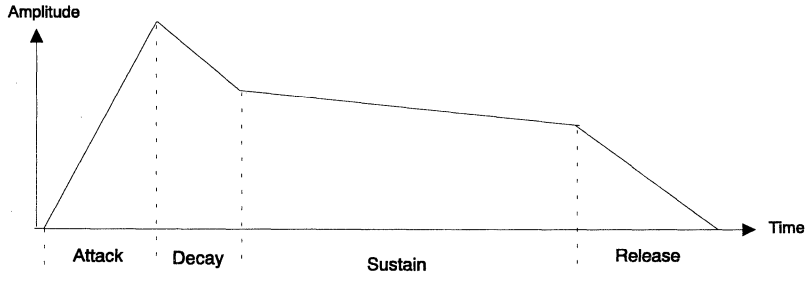

Figure 6: A Typical ADSR Amplitude Envelope

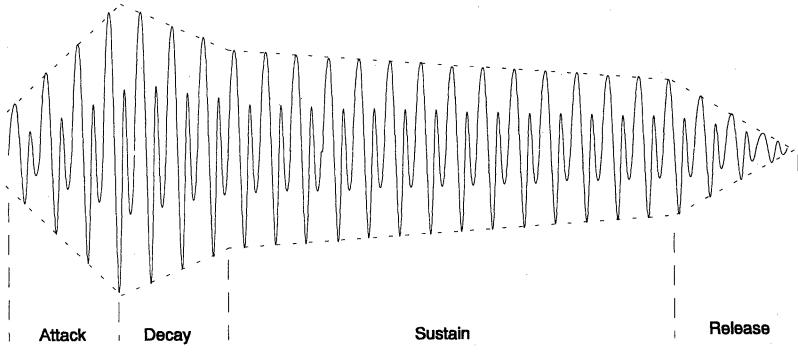

Figure 7: ADSR Envelope Applied to Looped Sound Segment

our examples), until a Note Off message is applied. The Note Off message triggers the beginning of the Release portion of the envelope.

Loop Length

The loop length is measured as a number of samples, and the length of the loop should be equal to an integral number of periods of the fundamental pitch of the sound being played (if this is not true, then an undesirable "pitch shift" will occur during playback when the looping begins). Of course, the length of the pitch period of a sampled instrument sound will generally not work out to be an integral number of sample periods. Therefore, it is common to perform a "resampling" process on the original sampled sound, to get new a new sound sample for which the pitch period is an integral number of sample periods.

In practice, the length of the loop segment for an acoustic instrument sample may be many periods with respect to the fundamental pitch of the sound. If the sound has a natural vibrato or chorus effect, then it is generally desirable to have the loop segment length be an integral multiple of the period of the vibrato or chorus.

One-Shot Sounds

The previous paragraphs discussed dividing a sampled sound into an attack section and a sustain section, and then using looping techniques to minimize the storage requirements for the sustain portion. However, some sounds, particularly sounds of short duration or sounds whose characteristics change dynamically throughout their duration, are not suitable for looped playback techniques. Short drum sounds often fit this description. These sounds are stored as a single sample segment which is played once through with no looping. This class of sounds are referred to as "one-shot" sounds.

Sample Editing and Processing

There are a number of sample editing and processing steps involved in preparing sampled sounds for use in a wave-table synthesis system. The requirements for editing the original sample data to identify and extract the initial and loop segments, and for resampling the data to get a pitch period length which is an integer multiple of the sampling period, have already been mentioned.

Editing may also be required to make the endpoints of the loop segment compatible. If the

amplitude and the slope of the waveform at the beginning of the loop segment do not match those at the end of the loop, then a repetitive "glitch" will be heard during playback of the looped section. Additional processing may be performed to "compress" the dynamic range of the sound to improve the signal/quantizing noise ratio or to conserve sample memory. This topic is addressed next.

When all of the sample processing has been completed, the resulting sampled sound segments for the various instruments are tabulated to form the sample memory for the synthesizer.

Sample Data Compression

The signal-to-quantizing noise ratio for a digitally sampled signal is limited by sample word size (the number of bits per sample), and by the amplitude of the digitized signal. Most acoustic instrument sounds reach their peak amplitude very quickly, and the amplitude then slowly decays from this peak. The ear's sensitivity dynamically adjusts to signal level. Even in systems utilizing a relatively small sample word size, the quantizing noise level is generally not perceptible when the signal is near maximum amplitude. However, as the signal level decays, the ear becomes more sensitive, and the noise level will appear to increase. Of course, using a larger word size will reduce the quantizing noise, but there is a considerable price penalty paid if the number of samples is large.

Compression techniques may be used to improve the signal-to-quantizing noise ratio for some sampled sounds. These techniques reduce the dynamic range of the sound samples stored in the sample memory. The sample data is decompressed during playback to restore the dynamic range of the signal. This allows the use of sample memory with a smaller word size (smaller dynamic range) than is utilized in the rest of the system. There are a number of different compression techniques which may be used to compress the dynamic range of a signal.

For signals which begin at a high amplitude and decay in a fairly linear fashion, a simple compression technique can be effective. If the slope of the decay envelope of the signal is estimated, then an envelope with the complementary slope (the negative of the decay slope) can be constructed and applied to the original sample data. The resulting sample data, which now has a flat envelope, can be stored in the sample memory, utilizing the full dynamic range of the memory. The decay envelope can then be applied to the stored sample data during sound playback to restore the envelope of the original sound.

Note that there is some compression effect inherent in the looping techniques described earlier. If the loop segment is stored at an amplitude level which makes full use of the dynamic range available in the sample memory, and the processor and D/A converters used for playback have a wider dynamic range than the sample memory, then the application of a decay envelope during playback will have a decompression effect similar to that described in the previous paragraph.

Pitch Shifting

In order to minimize sample memory requirements, wavetable synthesis systems utilize pitch shifting, or pitch transposition techniques, to generate a number of different notes from a single sound sample of a given instrument. For example, if the sample memory contains a sample of a middle C note on the acoustic piano, then this same sample data could be used to generate the C# note or D note above middle C using pitch shifting.

Pitch shifting is accomplished by accessing the stored sample data at different rates during playback. For example, if a pointer is used to address the sample memory for a sound, and the pointer is incremented by one after each access, then the samples for this sound would be accessed sequentially, resulting in some particular pitch. If the pointer increment was two rather than one, then only every second sample would be played, and the resulting pitch would be shifted up by one octave (the frequency would be doubled).

Frequency Accuracy

In the previous example, the sample memory address pointer was incremented by an integer number of samples. This allows only a limited set of pitch shifts. In a more general case, the memory pointer would consist of an integer part and a fractional part, and the increment value could be a fractional number of samples. The integer part of the address pointer is used to address the sample memory, the fractional part is used to maintain frequency accuracy. For example if the increment value was equivalent to 1/2, then the pitch would be shifted down by one octave (the frequency would be halved). When non-integer increment values are utilized, the frequency resolution for playback is determined by the number of bits used to represent the fractional part of the address pointer and the address increment parameter.

Interpolation

When the fractional part of the address pointer is non-zero, then the "desired value" falls between available data samples. Figure 8 depicts a simplified addressing scheme wherein the Address Pointer and the increment parameter each have a 4-bit integer part and a 4-bit fractional part. In this case, the increment value is equal to 1 1/2 samples. Very simple systems might simply ignore the fractional part of the address when determining the sample value to be sent to the D/A converter. The data values sent to the D/A converter when using this approach are indicated in the Figure 8, case I. A slightly better approach would be to use the nearest available sample value. More sophisticated systems would perform some type of mathematical interpolation between available data points in order to get a value to be used for playback. Values which might be sent to the D/A when interpolation is employed are shown as case II. Note that the overall frequency accuracy would be the same for both cases indicated, but the output is severely distorted in the case where interpolation is not used.

There are a number of different algorithms used for interpolation between sample values. The simplest is linear interpolation. With linear interpolation, interpolated value is simply the weighted average of the two nearest samples, with the fractional address used as a weighting constant. For example, if the address pointer indicated an address of (n+K), where n is the integer part of the address and K is the fractional part, than the interpolated value can be calculated as $s(n+K) = (1-K)s(n) + (K)s(n+1)$, where s(n) is the sample data value at address n. More sophisticated interpolation techniques can can be utilized to further reduce distortion, but these techniques are computationally expensive.

Oversampling

Oversampling of the sound samples may also be used to improve distortion in wavetable synthesis systems. For example, if 4X oversampling were utilized for a particular instrument sound sample, then an address increment value of 4 would be used for playback with no pitch shift. The data points chosen during playback will be closer to the "desired values", on the average, than they would be if no oversampling were utilized because of the

increased number of data points used to represent the waveform. Of course, oversampling has a high cost in terms of sample memory requirements.

In many cases, the best approach may be to utilize linear interpolation combined with varying degrees of oversampling where needed. The linear interpolation technique provides reasonable accuracy for many sounds, without the high penalty in terms of processing power required for more sophisticated interpolation methods. For those sounds which need better accuracy, oversampling is employed. With this approach, the additional memory required for oversampling is only utilized where it is most needed. The combined effect of linear interpolation and selective oversampling can produce excellent results.

Splits

When the pitch of a sampled sound is changed during playback, the timbre of the sound is changed somewhat also. For small changes in pitch (up to a few semitones), the timbre change is generally not noticed. However, if a large pitch shift is used, the resulting note will sound unnatural. Thus, a particular sample of an instrument sound will be useful for recreating a limited range of notes using pitch shifting techniques. To get coverage of the entire instrument range, a number of different samples of the instrument are used, and each of these

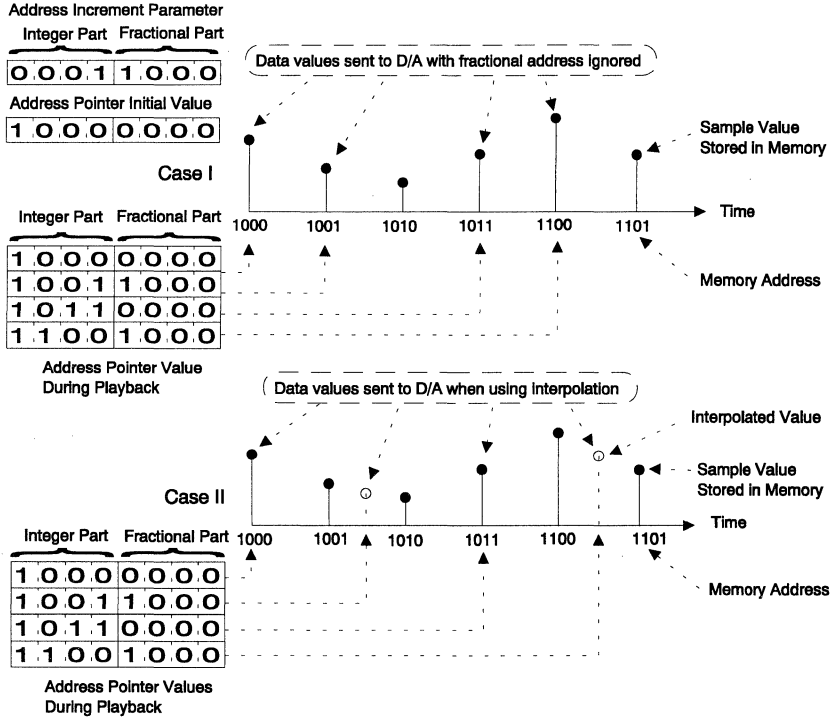

Figure 8: Sample Memory Addressing and Interpolation

samples is used to synthesize a limited range of notes. This technique can be thought of as splitting a musical instrument keyboard into a number of ranges of notes, with a different sound sample used for each range. Each of these ranges is referred to as a split, or key split.

Velocity splits refer to the use of different samples for different note velocities. Using velocity splits, one sample might be utilized if a particular note is played softly, where a different sample would be utilized for the same note of the same instrument when played with a higher velocity.

Note that the explanations above refer to the use of key splits and velocity splits in the sound synthesis process. In this case, the different splits utilize different samples of the same instrument sound. Key splitting and velocity splitting techniques are also utilized in a performance context. In the performance context, different splits generally produce different instrument sounds. For instance, a keyboard performer might want to set up a key split which would play a fretless bass sound from the lower octaves of his keyboard, while the upper octaves play the vibraphone. Similarly, a velocity split might be set up to play the acoustic piano sound when keys are played with soft to moderate velocity, but an orchestral string sound plays when the keys are pressed with higher velocity.

Aliasing Noise

The previous paragraph discussed the timbre changes which result from pitch shifting. The resampling techniques used to shift the pitch of a stored sound sample can also result in the introduction of aliasing noise into an instrument sound. The generation of aliasing noise can also limit the amount of pitch shifting which may be effectively applied to a sound sample. Sounds which are rich in upper harmonic content will generally have more of a problem with aliasing noise. Low-pass filtering applied after interpolation can help eliminate the undesirable effect of aliasing noise. The use of oversampling also helps eliminate aliasing noise.

LFOs for vibrato and tremolo

Vibrato and tremolo are effects which are often produced by musicians playing acoustic instruments. Vibrato is basically a low-frequency modulation of the pitch of a note, while tremolo is modulation of the amplitude of the sound. These effects are simulated in synthesizers by implementing low-frequency oscillators (LFOs) which are used to modulate the pitch or amplitude of the synthesized sound being produced. Natural vibrato and tremolo effects tend to increase in strength as a note is sustained. This is accomplished in synthesizers by applying an envelope generator to the LFO. For example, a flute sound might have a tremolo effect which begins at some point after the note has sounded, and the tremolo effect gradually increases to some maximum level, where it remains until the note stops sounding.

Layering

Layering refers to a technique in which multiple sounds are utilized for each note played. This technique can be used to generate very rich sounds, and may also be useful for increasing the number of instrument patches which can be created from a limited sample set. Note that layered sounds generally utilize more than one voice of polyphony for each note played, and thus the number of voices available is effectively reduced when these sounds are being used.

Polyphonic Digital Filtering for Timbre Enhancement

It was mentioned earlier that low-pass filtering may be used to help eliminate noise which may be generated during the pitch shifting process. There are also a number of ways in which digital filtering is used in the timbre generation process to improve the resulting instrument sound. In these applications, the digital filter implementation is polyphonic, meaning that a separate filter is implemented for each voice being generated, and the filter implementation should have dynamically adjustable cutoff frequency and/or Q.

For many acoustic instruments, the character of the tone which is produced changes dramatically as a function of the amplitude level at which the instrument is played. For example, the tone of an acoustic piano may be very bright when the instrument is played forcefully, but much more mellow when it is played softly. Velocity splits, which utilize different sample segments for different note velocities, can be implemented to simulate this phenomena. Another very powerful technique is to implement a digital low-pass filter for each note with a cutoff frequency which varies as a function of the note velocity. This polyphonic digital filter dynamically adjusts the output frequency spectrum of the synthesized sound as a function of note velocity, allowing a very effective recreation of the acoustic instrument timbre.

Another important application of polyphonic digital filtering is in smoothing out the transitions between samples in key-based splits. At the border between two splits, there will be two adjacent notes which are based on different samples. Normally, one of these samples will have been pitch shifted up to create the required note, while the other will have been shifted down in pitch. As a result, the timbre of these two adjacent notes may be significantly different, making the split obvious. This problem may be alleviated by employing a polyphonic digital filter which uses the note number to control the filter characteristics. A table may be constructed containing the filter characteristics for each note number of a given instrument. The filter characteristics are chosen to compensate for the pitch shifting associated with the key splits used for that instrument.

It is also common to control the characteristics of the digital filter using an envelope generator or an LFO. The result is an instrument timbre which has a spectrum which changes as a function of time. For example, It is often desirable to generate a timbre which is very bright at the onset, but which gradually becomes more mellow as the note decays. This can easily be done using a polyphonic digital filter which is controlled by an envelope generator.

The PC to MIDI Interface and the MPU-401

To use MIDI with a personal computer, a PC to MIDI interface product is generally required (there are a few personal computers which come equipped with built-in MIDI interfaces). There are a number of MIDI interface products for PCs. The most common types of MIDI interfaces for IBM compatibles are add-in cards which plug into an expansion slot on the PC bus, but there are also serial port MIDI interfaces (connects to a serial port on the PC) and parallel port MIDI interfaces (connects to the PC printer port). The fundamental function of a MIDI interface for the PC is to convert parallel data bytes from the PC data bus into the serial MIDI data format and vice versa (a UART function). However, "smart" MIDI interfaces may provide a number of more sophisticated functions, such as generation of MIDI timing data, MIDI data buffering, MIDI message filtering, synchronization to external tape machines, and more.

The defacto standard for MIDI interface add-in cards for the PC is the Roland MPU-401 interface. The MPU-401 is a smart MIDI interface, which also supports a dumb mode of operation (often referred to as "pass-through mode" or "UART mode"). There are a number of MPU-401 compatible MIDI interfaces on the market. In addition, many add-in sound cards include built-in MIDI interfaces which implement the UART mode functions of the MPU-401.

Compatibility Considerations for MIDI Applications on the PC

There are two levels of compatibility which must be considered for MIDI applications running on the PC. First is the compatibility of the application with the MIDI interface being used. The second is the compatibility of the application with the MIDI synthesizer. Compatibility considerations under DOS and the Microsoft Windows operating system are discussed in the following paragraphs.

DOS Applications

DOS applications which utilize MIDI synthesizers include MIDI sequencing software, music scoring applications, and a variety of games. In terms of MIDI interface compatibility, virtually all of these applications support the MPU-401 interface, and most utilize only the UART mode. These applications should work correctly if the PC is equipped with a MPU-401, a full-featured MPU-401 compatible, or a sound card with a MPU-401 UART-mode capability. Other MIDI interfaces, such as serial port or parallel port MIDI adapters, will only work if the application provides support for that particular model of MIDI interface.

A particular application may provide support for a number of different models of synthesizers or sound modules. Prior to the General MIDI standard, there was no widely accepted standard patch set for synthesizers, so applications generally needed to provide support for each of the most popular synthesizers at the time. If the application did not support the particular model of synthesizer or sound module that was attached to the PC, then the sounds produced by the application might not be the sounds which were intended. Modern applications can provide support for a General MIDI (GM) synthesizer, and any GM-compatible sound source should produce the correct sounds. Some other models which are commonly supported are the Roland MT-32, the Roland LAPC-1, and the Roland Sound Canvas. The Roland MT-32 was an external MIDI sound module which utilized Roland's Linear Additive (LA) synthesis, and the MT-32 combined with an MPU-401 interface became a popular MIDI synthesis platform for the PC. The LAPC-1 was a PC add-in card which combined the MT-32 synthesis function with the MPU-401 MIDI interface. The Sound Canvas is Roland's General Synthesizer (GS) sound module, and this unit has become an industry standard.

Microsoft Windows and the Multimedia PC (MPC)

The number of applications for high quality audio functions on the PC (including music synthesis) grew explosively after the introduction of Microsoft Windows 3.0 with Multimedia Extensions ("Windows with Multimedia") in 1991. The Multimedia PC (MPC) specification, originally published by Microsoft in 1991 and now published by the Multimedia PC Marketing Council (a subsidiary of the Software Publishers Association), specifies minimum requirements for multimedia-capable Personal Computers. A system which meets these requirements will be able to take full advantage of Windows with Multimedia. Note that many of the functions originally included in the Multimedia Extensions

have been incorporated into the Windows 3.1 operating system.

The audio capabilities utilized by Windows 3.1 or Windows with Multimedia include audio recording and playback (linear PCM sampling), music synthesis, and audio mixing. In order to support the required music synthesis functions, MPC-compliant audio adapter cards must have on-board music synthesizers.

The MPC specification defines two types of synthesizers; a "Base Multitimbral Synthesizer", and an "Extended Multitimbral Synthesizer". Both the Base and the Extended synthesizer must support the General MIDI patch set. The difference between the Base and the Extended synthesizer requirements is in the minimum number of notes of polyphony, and the minimum number of simultaneous timbres which can be produced. Base Multitimbral Synthesizers must be capable of playing 6 "melodic notes" and "2 percussive" notes simultaneously, using 3 "melodic timbres" and 2 "percussive timbres". The formal requirements for an Extended Multitimbral Synthesizer are only that it must have capabilities which exceed those specified for a Base Multitimbral Synthesizer. However, the "goals" for an Extended synthesizer include the ability to play 16 melodic notes and 8 percussive notes simultaneously, using 9 melodic timbres and 8 percussive timbres.

The MPC specification also includes an authoring standard for MIDI composition. This standard requires that each MIDI file contain two arrangements of the same song, one for Base synthesizers and one for Extended synthesizers. The MIDI data for the Base synthesizer arrangement is sent on MIDI channels 13 - 16 (with the percussion track on channel 16), and the Extended synthesizer arrangement utilizes channels 1 - 10 (percussion is on channel 10). This technique allows a single MIDI file to play on either type of synthesizer.

Windows applications generally address hardware devices such as MIDI interfaces or synthesizers through the use of drivers. The drivers provide applications software with a common interface through which hardware may be accessed, and this simplifies the hardware compatibility issue. Before a synthesizer is used, a suitable driver must be installed using the Windows Driver applet within the Control Panel. The device drivers supplied with Windows 3.1 include a driver for the MPU-401/LAPC-1 MIDI interface, and a driver for the original AdLib FM synthesizer card. Most other MIDI interfaces and/or synthesizers are shipped with their own Windows drivers.

When a MIDI interface or synthesizer is installed in the PC and a suitable device driver has been loaded, the Windows MIDI Mapper applet will appear within the Control Panel. MIDI messages are sent from an application to the MIDI Mapper, which then routes the messages to the appropriate device driver. The MIDI Mapper may be set to perform some filtering or translations of the MIDI messages in route from the application to the driver. The processing to be performed by the MIDI Mapper is defined in the MIDI Mapper Setups, Patch Maps, and Key Maps.

MIDI Mapper Setups are used to assign MIDI channels to device drivers. For instance, If you have an MPU-401 interface with a General MIDI synthesizer and you also have a Creative Labs Soundblaster card in your system, you might wish to assign channels 13 to 16 to the Ad Lib driver (which will drive the Base-level FM synthesizer on the Soundblaster), and assign channels 1 - 10 to the MPU-401 driver. In this case, MPC compatible MIDI files will play on both the General MIDI synthesizer and the FM synthesizer at the same time. The General MIDI synthesizer will play the Extended arrangement on MIDI channels 1 - 10, and the FM synthesizer will play the Base arrangement on channels 13-16. The MIDI Mapper Setups can

also be used to change the channel number of MIDI messages. If you have MIDI files which were composed for a General MIDI instrument, and you are playing them on a Base Multitimbral Synthesizer, you would probably want to take the MIDI percussion data coming from your application on channel 10 and send this information to the device driver on channel 16.

The MIDI Mapper patch maps are used to translate patch numbers when playing MPC or General MIDI files on synthesizers which do not use the General MIDI patch numbers. Patch maps can also be used to play MIDI files which were arranged for non-GM synthesizers on GM synthesizers. For example, the Windows-supplied MT-32 patch map can be used when playing GM-compatible .MID files on the Roland MT-32 sound module or LAPC-1 sound card.

The MIDI Mapper key maps perform a similar function, translating the key numbers contained in MIDI Note On and Note Off messages. This capability is useful for translating GM-compatible percussion parts for playback on non-GM synthesizers or vice-versa. The Windows-supplied MT-32 key map changes the key-to-drum sound assignments used for General MIDI to those used by the MT-32 and LAPC-1.

Some MIDI applications, such as MIDI sequencer software packages, can be set to make use of the MIDI Mapper, or to address the device driver directly (bypassing the MIDI Mapper). Other Windows applications always utilize the MIDI Mapper.

Summary

The MIDI protocol provides an efficient format for conveying musical performance data, and the Standard MIDI Files specification ensures that different applications can share time-stamped MIDI data. The storage efficiency of the MIDI file format makes MIDI an attractive vehicle for generation of sounds in multimedia applications, computer games, or high-end karaoke equipment. The General MIDI system provides a common set of capabilities and a common patch map for high polyphony, multi-timbral synthesizers. General MIDI-compatible Synthesizers employing high quality wavetable synthesis techniques provide an ideal MIDI sound generation facility for multimedia applications.

DESIGN TECHNIQUES FOR CD-QUALITY AUDIO IN MULTIMEDIA COMPUTER SYSTEMS

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Background

With the advent of new data conversion architectures, particularly "delta-sigma", or "1-bit DAC" technology, it is now possible to integrate high resolution analog-to-digital (A/D) and digital-to- analog (D/A) converters into VLSI digital integrated circuits (IC's). The result has been many IC's recently introduced which allow CD-quality audio record and playback capability to be added to personal computers (PC's) and workstations with as little as one IC (Fig. 1). Already the PC market has seen a wide variety of sound cards which plug into the computer bus, but the high level of integration which reduces the number of components, and therefore the space required, can now allow computer designers to integrate the audio function into the computer motherboard. This, together with low cost below a critical threshold, is radically changing the whole computer market with a frenzy of multimedia activity which will change the way we use and communicate with computers forever. PC designers, who are under intense pressure to respond to these demands, need to be able to quickly and easily design these audio IC's into their add-on boards or motherboards. With nearly all the analog circuits contained in a comprehensive, mixed-signal IC which includes all the digital interface and control functions, the design job, which previously would be reserved for only experienced analog engineers, can now be done by computer designers with little analog experience.

However, to achieve CD-quality audio, the physical layout and interconnects of the analog section are extremely critical. The harsh environment of the computer system contains high frequency digital signals which can interfere with the audio in many ways. There are a number of analog design rules and circuit techniques which will result in multimedia designs that work first time with full data sheet performance.

Ground Planes

The most fundamental rule in audio designs is the use of separate analog and digital ground planes (Fig. 2). All the analog components and associated circuits should be placed exclusively over the analog ground plane while the digital components and pc board traces should be restricted exclusively to the digital ground plane. In computer systems, there are high speed digital signals with fast edges that will couple onto the ground plane. Ground planes provide a convenient way of distributing a low impedance, low inductance ground reference over a wide area, but they should not be considered incorruptible. The impedance may be very close to zero at dc, but may increase significantly at high frequency. Fast edges of high speed logic contain high frequency components that may be much higher than the fundamental data or clock frequency. If the digital traces were to run over the analog ground plane, capacitive coupling occurs. It is easy to calculate just how much by taking the area, A, of the trace and the thickness, d, of the layers separating the two. Obtaining the dielectric constant, e, of the pc board material from

the manufacturer, one can calculate the capacitance by C=Ae/d. Notice that the capacitance is inversely proportional the thickness, so that if a situation makes this unavoidable, the coupling can be minimized by placing as many layers as possible between the trace and the ground plane.

An equivalent argument applies to analog traces which extend over the digital ground plane. Anyone who has measured the quality of the ground plane in a computer with an oscilloscope knows that there is a great deal of noise. This is why the ground clip on the probe must be very close to the component being measuring to get a clean waveform. PC chips sets in a computer can dump a lot of high speed, high current transients into ground that modulate the ground plane voltage. This "signal" can couple onto the traces which are over the ground plane. Keep in mind that "CD quality" requires a signal-to-noise ratio (S/N) of 80dB, or one part in 10,000. With 1Vrms audio signals, or 2.8Vp-p, the noise floor level is around 280uV. It doesn't take very much coupling to transfer tens of millivolts of signal from the digital ground plane onto the sensitive analog traces. One of the worst things to do is to overlap the analog and digital ground planes because the intersecting area could be large, creating significant capacitance.

Power Planes

For similar reasons, power planes should be used with care. They are not always necessary, since in analog design it is often good practice to provide separate power supply traces from the regulator or power supply to each of the critical analog components, rather than "daisy-chain" the supply or make a power grid. If there is any ripple or high frequency glitches from transient currents, power planes can easily couple this into the analog traces. If used, never bridge the split between the analog and digital ground planes. Keep the analog supply plane entirely under (over) the analog ground plane. Power planes can even add crosstalk and interaction within the analog section. The power plane forms a common capacitor plate between two analog traces. While this occurs on the ground planes as well, ground is much lower impedance than the power, which often comes from an IC regulator. Since the analog components usually have a high degree of power supply rejection built in, it is sufficient to simply provide wide traces to each of the analog supply pins, and let the bypass capacitors do their job.

Ground Plane Connections

If there were no ground planes, all the ground connections would be returned to one single "star ground" point, normally at the power supply, voltage regulator, or the power connector (Fig. 2). Using ground planes, there should be only one connection between the analog and digital planes, at this star point to avoid any ground loops. There are sometimes exceptions to this rule. If you have control over the whole system, it may be possible to provide separate analog and digital power supply and ground wires from each board to the power supply. The star ground point in this case is the power supply. Because there are many variables in analog circuit design which cannot be anticipated or calculated, having several options for ground connections is the safest thing to do. It is advisable to have a few jumper options at different places to connect the analog and digital ground planes, either at the power connector, voltage regulator, close to the data converter, or none, allowing separate wires back to the power supply. In through hole boards, add plated through via holes attached to each plane directly across the separation between the planes. Later, the jumper wire can be eliminated by a metal layer change to short the two. Adding additional drilled holes is usually a costly change. On surface mount boards, plan for zero ohm resistors at each option point. This component can be replaced with a short on a subsequent layer revision. This sort of empirical design is normal for high accuracy analog design, usually done

with breadboard experiments. Time to market, cost, and complexity of computer design, especially motherboards, does not allow breadboards. Going directly to Rev.0 product means that any breadboarding must be done with manufacturing options.

Ground Plane Split

There are most likely very high transient currents at high frequency on the digital ground plane. Even though the ground plane is low impedance, significant IR voltage drops can occur. These transient voltages can couple across the isolation barrier to the analog ground plane. The analog ground plane may have very low DC impedance, but it may not be nearly as good at high frequencies, making it susceptible to coupling from the adjacent digital ground plane. With both ground planes on the same layer, the cross sectional area is small because the metal layers are thin, but the total area significantly adds up over the long length of peripheral distance across the board. For this reason, provide a generous separation between the analog and digital ground planes. If possible, 1/8" is recommended (Fig. 2), but at least 1/16" is required.

Ground Plane Fill

Most of the interference on the PC board comes from the digital section into the analog section laterally across the board. Experimental data has shown that adding a ground plane fill in the analog section helps to form a guard around the sensitive analog traces and can reduce coupling from digital to analog by as much as 30dB. Rather than leave the area between the traces empty, fill in these spaces, as much as the design rules will allow, with solid pieces of metal, connected to the main ground plane with vias (Fig. 3). Avoid any unconnected, floating pieces of fill, which can enhance the coupling mechanism, worse than not having any fill at all.

Although not always possible, ground plane fill is recommended between the digital traces as well to reduce digital interference transmitted into the analog section.

Ground Plane Shields

For a good analog design, two layers is adequate for ground plane and traces. Additional layers can add more variables to an already complex situation. However, for high density, most computer designs require multilayer pc boards with 4-8 layers in add-on cards, and 8-16 layers in the case of motherboards. There is no particular advantage to multilayer analog designs other than it may be desirable to have more than one ground plane, and to shield the analog traces on the inner layers between ground planes on each surface. This may be especially important for plug-in cards, where an analog audio card could be plugged into a slot adjacent to a card containing graphics, video, disk controller, or other high speed digital circuits that can radiate interference into the sensitive analog circuit. There is not much that can be done to protect the components and exposed pins, but at least the analog traces can be protected by sandwiching them between ground planes.

Location on the Board

In most CMOS analog IC's, both positive and negative power supplies are required to obtain the most operating voltage range and highest signal to noise (S/N) ratio. It is normal to find the substrate connected to the most positive power supply. In these IC's, strict adherence to good analog to digital isolation demands that the split between analog and digital ground planes run directly under the data conversion IC's between the groups of digital and analog pins.

In computer systems, negative supply voltages are usually not available on the bus. Rather than require an extra negative supply or a DC-DC converter, multimedia analog components have been designed to work on a single positive

power supply, normally +5V. The negative power input, therefore, is ground. These analog IC's for single supply systems are designed with the substrate connection to ground, with analog and digital grounds internally connected to the substrate. Although there are both analog and digital ground pins, both must be connected to the analog ground plane for best results. Also, bypass capacitor return current must be referenced to the analog ground as well. As such, it is better to place the whole IC over a single, analog ground plane, even though some of the basic design rules are violated.

Place the IC as close to the digital ground split as possible to minimize the distance the digital traces must cross the analog ground plane (Fig. 2). Rotate the IC so that the digital pins face the digital ground plane and the analog pins face away, toward the analog I/O connectors. For IC's that have an integrated ISA bus interface, the bus drivers may have significant current capability, up to 24mA. These buffers have separate ground returns and separate power supply connections to isolate these high transients which are most likely asynchronous to the sample rate of the A/D and D/A converters within the IC. In this case, extend the digital ground plane partially under the IC, only enough to separate the analog ground plane from the bus data, control, and supply pins (Fig. 4).

For PC plug-in cards (Fig. 2), the normal I/O connectors for audio LINE IN, LINE OUT, and MIC IN are on a bracket mounted on the rear of the card sliding into the rear of the chassis. This dictates that the analog section for the audio should be at the rear of the card to minimize the analog connections. For motherboards, the best place for the analog section is to reserve a corner of the board at the rear to allow the audio I/O connectors mounted on the board to align with holes in the rear panel (Fig. 5). Avoid placing the analog in the middle of the board with digital surrounding it. Also avoid long buses, like SCSI, or ISA bus from running adjacent to the analog ground plane. If this is unavoidable, at least separate the bus and analog ground plane with a piece of digital ground plane as a guard.

Power Supply Bypassing

Adequate bypass capacitors between the power supply pins and appropriate ground are mandatory. It is critical to connect these capacitors as close to the pins of the IC as possible. The efficiency of the capacitor will be lost if there is too much resistance or inductance in series with it. Usually two capacitors are recommended for each supply pin, a small 0.01uF-0.1uF ceramic capacitor together with a 1uF-10uF tantalum capacitor. Because the small capacitor handles the high frequency transients, it needs to be the closer of the two, while the larger one can afford to be further away. On surface mount boards (Fig. 6), the capacitors should be on the component side so that a direct connection can be made to the pins of the IC without going through vias, which add impedance to the connection. A simple test can be performed to see if the capacitor connection can be improved by soldering the small capacitors directly to the IC pins. If the performance changes, most likely the capacitors connections are not optimum.

Power Supplies

The are at least two separate power supplies required for multimedia audio IC's, analog and digital. There are several options to generate each +5V input. The safest and preferred method is to use a higher voltage, such as +12V, which sometimes is available on the bus, to generate a quiet, clean, +5V analog voltage using a linear, three terminal IC regulator for the +5V analog supply. Use this output through a small resistor and filter capacitors for the digital supply (Fig. 7a). Even though the digital input is for the digital circuits, it is on a sensitive analog IC. Excessive noise not filtered by the bypass capacitors could couple through the substrate into the analog part of the IC. By deriving the digital from analog supply, a relatively low noise digital supply is assured. Any transient current

which feeds back into the analog supply is synchronous to the A/D, and will not be a problem.

The second option is to use a regulator for the analog supply as above, but use the main digital supply from the computer for the IC digital input (Fig. 7b). There is a risk that noise could degrade performance, but a much smaller regulator can be used since the analog supply is usually only a fraction of the digital supply. In this case, do not install a resistor between the analog and digital supply pins, but include a ferrite bead in series with the digital supply. Ferrite bead selection is made more by size and current capability than by value. Although impedance vs. frequency curves are given, the choice is somewhat empirical, by trying different ones. Most manufacturers offer a kit with many sizes and types to find the most effective one.

A third option is to use the computer supply for everything, with no regulator. In this case, connect the +5V from the bus through a ferrite bead first to the digital supply pin with associated bypass capacitors, then connect this pin through a small resistor to the analog pin and its bypass capacitors, which form an extra filter (Fig. 7c).

Some IC's have a second digital supply for the interface logic, which can have high current buffers that switch asynchronously to the A/D and D/A operation, causing excessive interference. Isolate this from the other power pins by connecting it directly to the +5V on the bus, with a ferrite bead between it and the other digital supply pins on the IC (Fig. 7d).

Voltage Reference

The voltage reference output is often the most sensitive analog pin on an A/D. External bypass capacitors are necessary to make sure this voltage is stable. It is critical to position these capacitors as close to the pins as possible, again the smaller value closer to the chip. Any high frequency signals or noise injected into this pin can either produce tones in the audible range or elevate the entire noise floor, or both. It is important to keep all dynamic signals, both analog and digital, away from this pin.

Minimum Analog Trace Length

The pc board trace lengths connecting the analog inputs from the card-edge connectors, through any input amplifiers, to the analog input on the IC, should be made as short and direct as possible. Rotate the input amplifiers in 90 degree increments to the best orientation to accomplish this. Pay special attention to keep high impedance lengths as short as possible, like the summing junction of op amps. Low impedance output sources are less susceptible to noise and coupling.

Distortion Effects

Avoid non-inverting amplifier configurations. All op amps have circuits on the input that attempt to maintain the offset voltage and offset current constant over the specified input voltage range. However, the residual common mode rejection ratio (CMRR) is not perfect, and can contribute a significant signal dependent error. This non-linearity results in distortion in high quality audio circuits. Sometimes non-inverting amplifiers are necessary when driving from a high impedance source, like a resistor divider. If possible always use inverting amplifier configurations where the summing junction of the input is held at a virtual ground. In this case the CMRR is not a factor, or a second order effect at most.

Use only metal film resistors in the analog signal path. Carbon resistors can add noise and distortion from voltage coefficient effects. Use only NPO (COG) dielectric ceramic capacitors in the analog signal path as well. Capacitors made with Z5U or X7R material can have a high degree of dielectric absorption, causing non-linearity and distortion.

Aliasing

In order to correctly digitize an audio signal, the A/D must sample at least twice the highest signal frequency. This minimum requirement is called the Nyquist rate, with the sample rate frequency, Fs, equal to or above twice the maximum frequency in the input bandwidth, Fb. Any signal which is higher than Fb and within a window of Fs plus or minus Fb will be translated to a lower frequency equal to the absolute difference from Fs. In an audio example, it is common to sample at the same rate used in CD players, Fs=44.1kHz. This is slightly more than adequate to meet the Nyquist criteria for the audio bandwidth with Fb=20kHz. An A/D operating at the minimum Nyquist rate is said to have no oversampling. In this case, any noise that may be at 45.1kHz, a 1kHz difference, will appear as a 1kHz tone. This repeats at all the multiples of the sample rate as well, in this example at 88.2kHz, 132.3kHz, 176.4kHz, etc., all with windows of susceptibility of 20kHz above and below each one.

Delta-sigma converters make the A/D much less susceptible to noise because they take advantage of very high oversampling rates, much higher than the Nyquist minimum. It is common for the A/D's in multimedia IC's to operate at 64x oversampling ratio. Using the example above, with Fb=20kHz, the input audio signal is actually sampled at 64xFs, or about 2.8MHz. Digital filters inside the A/D process all these samples to produce an output word rate (OWR) equal to the Nyquist rate, or 44.1kHz. The digital filters also have sharp cutoff characteristics just above Fb, attenuating everything up to Fb below the 64xFs frequency. Delta-sigma A/D's can reject any noise or interference over this wide band. However, there are narrow windows of susceptibility at all the multiples of the oversampling rate, 20kHz above and below each one. Only noise around 2.8MHz, 5.6MHz, 8.4MHz, 11.2MHz, etc., can alias down to the audio range. This can be a problem in computer systems, because it is unavoidable to have frequencies, or harmonics of these frequencies, in this range. Proper layout and bypassing can minimize aliased noise which could couple through the power supply pins and voltage reference.

High frequency energy within the oversampling windows that may be present on the analog audio input must be filtered with an external anti-alias filter. With no oversampling, a high-order active filter with sharp cutoff characteristics in necessary. Using a delta-sigma converter with a high oversampling rate, this anti-alias filter requirement is greatly reduced. In the above example, with 20kHz bandwidth, Fb, and 64x oversampling ratio, a filter with -3dB bandwidth just above Fb can roll off gradually (Fig. 8). The attenuation at the first oversampling window must be below the noise floor of the converter. With 64x oversampling, a simple, single pole, RC passive filter is sufficient to attenuate any high frequencies on the input to less than -80dB at a frequency of (64xFs)-Fb, or

(64x44.1kHz)-20kHz =
2.8224MHz-20kHz =
2.8024MHz.

Aliasing can be avoided by synchronizing all the digital systems to the A/D sample rate. If there is coupling at exactly 64xFs, it will alias to a frequency of zero, becoming a DC offset, which can be compensated for electrically, by software, or using autocalibration if available by the A/D. The problem with computer systems is that synchronization of the different parts of the PC is not possible. The graphics and video, the disk controller, the CPU, the communications ports, all need to have particular frequencies of operation. Other than avoiding these oversampling windows, separation and shielding are the best means to minimize interference.

Summary

By following the layout and design techniques described above, CD- quality audio can be designed into personal computers and workstations for multimedia applications. As out-

lined in the checklist below, proper grounding, bypassing, and isolation of digital and analog circuits are critical. Experience has shown that strict adherence to these rules will result in a high rate of success of audio systems with low noise and free of digital interference.

Layout and Design Rules:

1. Split analog and digital ground planes.
2. Separation between ground planes 1/8".
3. Analog signals only over analog ground plane.
4. Digital signals only over digital ground plane.
5. Analog and digital ground planes linked on only one place.
6. Use of ground plane fill.
7. Ground plane shields.
8. Locate analog section away from high speed digital circuits.
9. Position bypass capacitors as close as possible to supply and voltage reference pins.
10. Mount surface mount bypass capacitors on component side, with direct connection to pins.
11. Place smallest bypass capacitor closest to IC pin.
12. Separate linear regulator recommended for analog supply with digital supply derived from analog supply.
13. Minimum trace length for analog inputs and outputs.
14. Use inverting amplifier configuration.
15. Use metal film resistors and NPO capacitors in analog signal path.
16. Synchronize A/D and D/A converters to digital circuit clock frequencies.

Acknowledgments

The author would like to thank Steve Harris, Applications Manager at Crystal Semiconductor, for his valuable contribution to this paper and for preparing most of the figures.

8

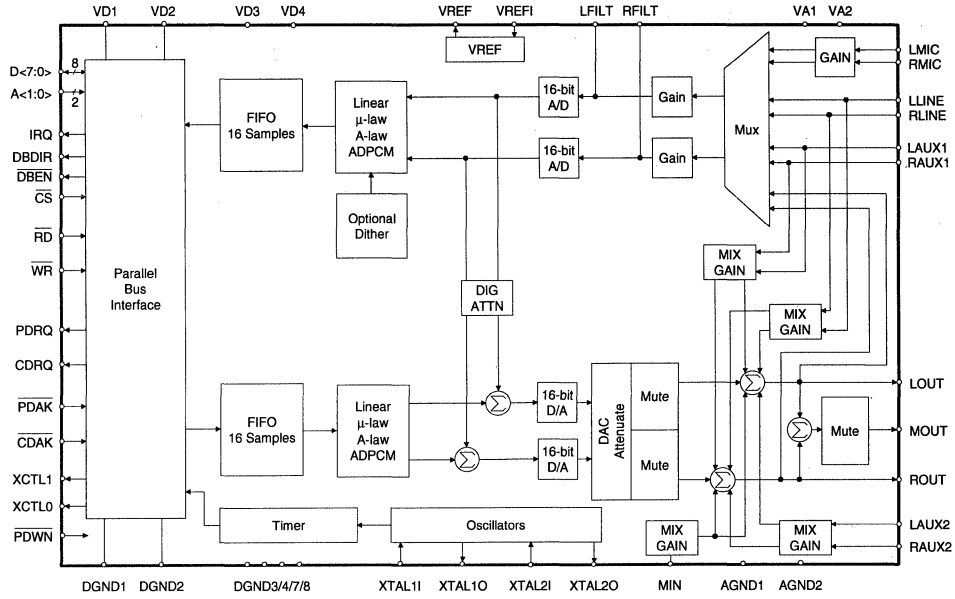


Figure 1. Parallel interface multimedia audio subsystem IC.

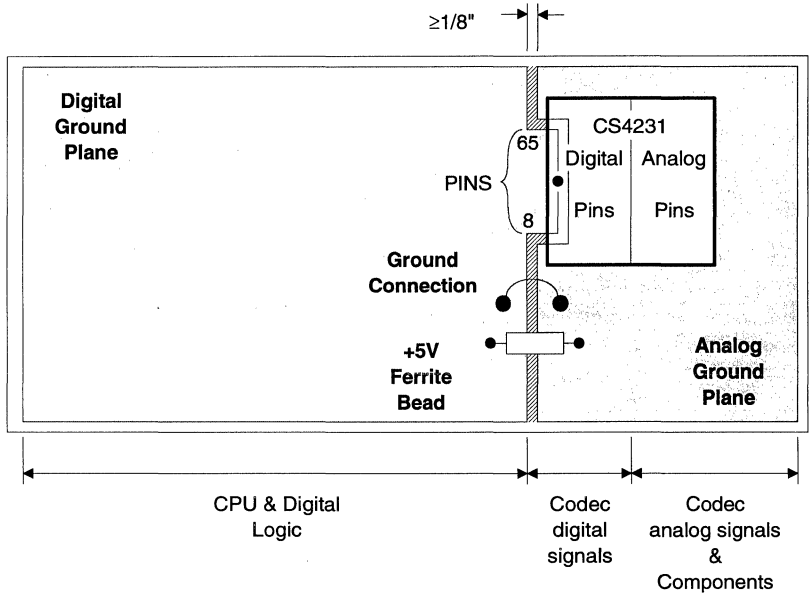


Figure 2. Isolated digital and analog traces over separate ground planes.

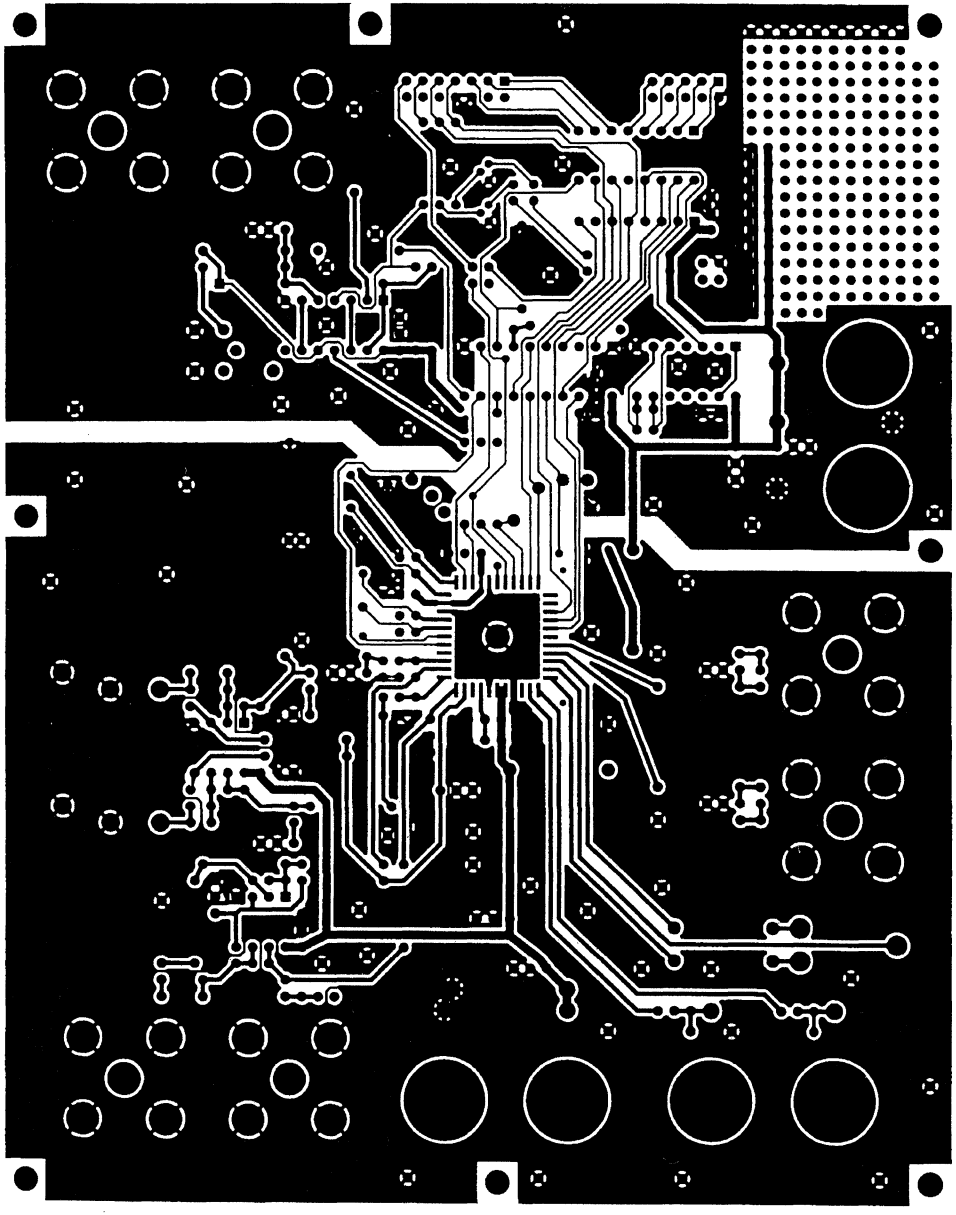


Figure 3. Example of ground plane fill. Traces are surrounded by ground plane (dark area), except for high density digital lines in the center.

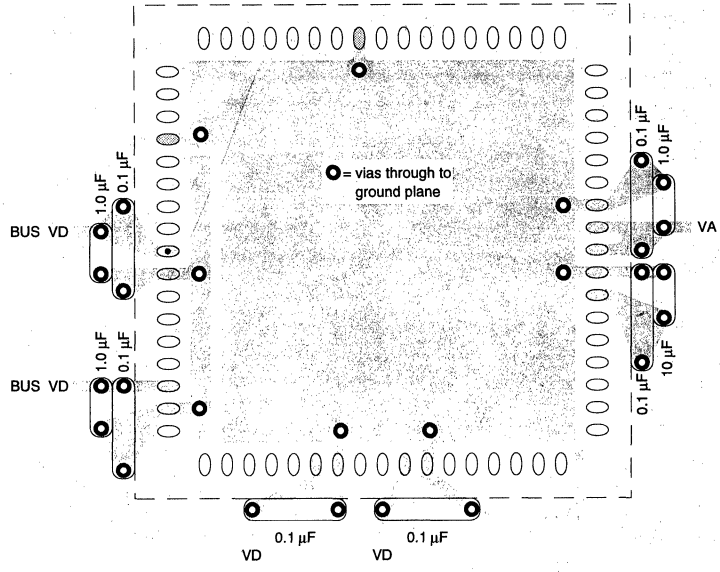


Figure 4. Analog ground plane under entire IC, except for digital ground plane along 13 bus interface pins

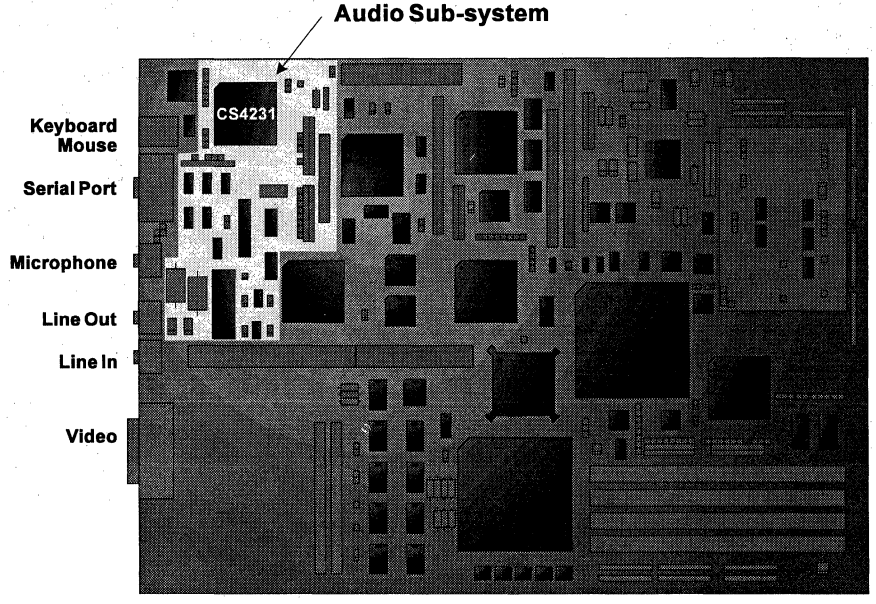


Figure 5. Multimedia audio IC mounted on motherboard.

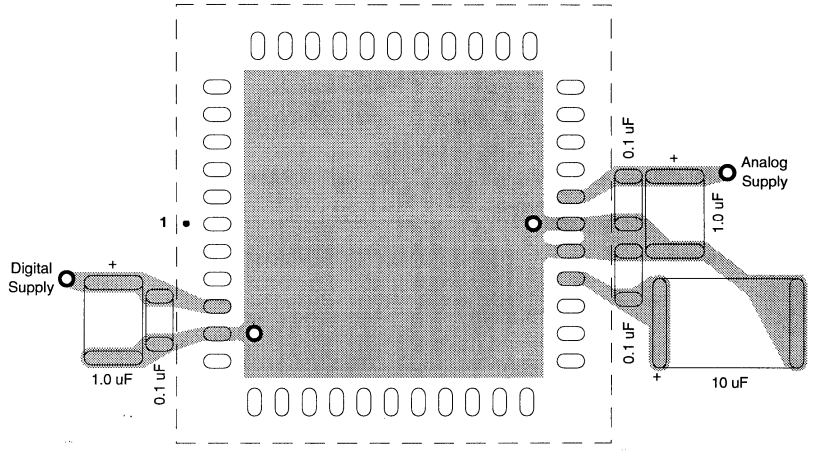


Figure 6. Surface mount bypass capacitors connect directly to the 44PLCC pins on the componenet side of board. The smaller value is closer to the IC pin.

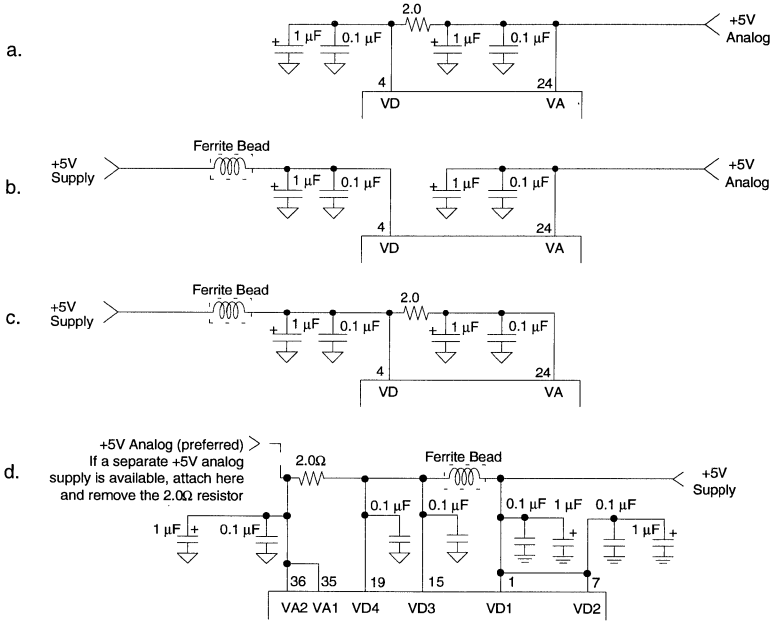


Figure 7. a) Digital +5V derived from analog +5V, b) separate digital and analog supplies, c) analog +5V derived from digital +5V, and d) separate digital supply for interface (pins 1, 7) and audio logic and control supply (pins 15, 19, 24, 25, and 54).

8

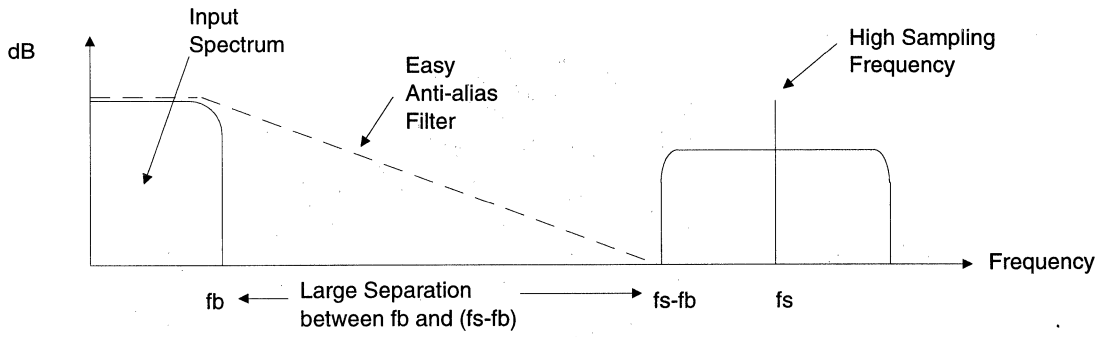


Figure 8. In delta-sigma A/D's, digital filters reject frequencies between Fb and Fs-Fb. A simple anti-alias filter is also needed on the input to make sure there is no energy above Fs-Fb.

INTRODUCTION

Using SMART Analog technology, Crystal Semiconductor has created a family of CMOS A/D Converters which feature patented on-chip, self-calibrating architectures to maintain accuracy and linearity over their full temperature range and device lifetime. Each of our A/D Converters features an on-chip sample and hold, and is manufactured in low-power CMOS. Most devices include a power-down sleep mode.

CS5012A, CS5014, CS5016 SAR Family

The CS5012A, CS5014 and CS5016 converters have 12, 14 & 16 bits of resolution respectively, with conversion times of 7 µs to 16 µs. The converters are tested for static and dynamic performance, at full rated conversion speed. On-chip self-calibration ensures that linearity, offset and full-scale errors remain with specification, with no missing codes. Specifications are maintained over the full temperature range.

CS5030, CS5031 12-bit 500kHz ADCs

The CS5030 family features an on-chip reference which is very stable over temperature. This yields a 12-bit ADC which has a total unadjusted error(including reference error) of <± 0.5 LSB over the military temperature range.

CS5101A, CS5126 16-bit 100 kHz ADC

The CS5101A is a 16-bit ADC capable of converting in 8 µs, yielding sample rates of 100 kHz. A 2-channel analog input mux is included. Output data is available serially, with 4 interface modes. An on-chip crystal oscillator is provided, along with a power-down control. The CS5126 is a low-cost version of the CS5101A, intended for audio signal processing applications.

CS5102A 16-bit 20 kHz Low Power ADC

The CS5102A is a low power version of the CS5101A. Requiring only 44 mW from ±5 V supplies, along with a 1 mW power down mode, the CS5102A is ideal for battery powered applications.

CS5412 12-bit, 1 MHz ADC

Using a 2-step flash approach, the CS5412 achieves 12-bit performance at 1 MHz sample rate. Self calibration insures accuracy over time and the military temperature range. Available in both DIP and J-lead LCC packages, with on-chip S/H, the IC offers a very compact ADC solution.

CS5501, CS5503 16/20-bit DC Measurement ADC

The CS5501 and CS5503 feature an on-chip, 6-pole, low-pass filter, with adjustable corner frequencies from 0.1 Hz to 10 Hz. The ADC's achieve linearity errors of 0.0007%, with no missing codes. A highly flexible serial interface, along with 25 mW power consumption, all in a 20 pin package, make the parts ideal for weigh scale and process control applications. The CS5503 is the 20-bit version of the CS5501, offering increased dynamic range, often removing the need for external gain scaling.

CS5504/5/6/7/8/9 1,2 & 4-channel, 16/20-bit DC Measurement ADC

Very low power consumption of 1.5 mW, along with an optional 2 or 4-channel input mux, make this part ideal for process control and hand held meter applications. These ADC's are available in 16 or 20 bit versions, with single channel, 2 channel or 4 channel inputs, and DIP or surface mount packages.

CS5516,CS5520 16/20-bit Bridge Transducer ADC

The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells and pressure transducers. Any family of mV output transducers, including those needing bridge excitation, can be directly interfaced to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier, choice of AC or DC bridge excitation, software selectable reference and signal demodulation.

Specifications	CS5012A CS5014 CS5016	CS5030 CS5031	CS5101A CS5102A CS5126	CS5317	CS5321 CS5322 CS5323 CS5324	CS5326/7 CS5328/9 CS5336/7 CS5338/9	CS5345 CS5349	CS5389 CS5390	CS5412	CS5501 CS5503	CS5504 CS5505 CS5506 CS5507 CS5508 CS5509	CS5516 CS5520
Application	GP	GP	GP	Modem	Seismic	Audio	Audio	Audio	GP Fast	DC Measurement		
Resolution (bits)	12/14/16	12	16	16	24	16/18	16	18/20	12	16/20	16/20	16/20
Conversion Time (us)	7/14/16	2	8/40	-	-	-	-	-	1.25	-	-	-
Throughput (kHz)	100/56/50	500	100/20	20	-	50	50	50	1 MHz	4	60/100Hz	60Hz
Number of Inputs	1	1	2	1	1	2	2	2	1	1	1/2/4	1
Input Bandwidth	-	-	-	10 kHz	500 Hz	22/20 kHz	22 kHz	22kHz	4 MHz	10Hz	10 Hz	12Hz
Integral Non-Linearity	.006/.002/.001 %	.25LSB	.0015%	-	-	-	-	-	.01 %	.0007 %	.0015 %	.0007 %
Differential (± LSB) Non-Linearity	0.25/0.25/NMC	0.5	NMC	NMC	NMC	NMC	NMC	NMC	0.9	0.125/NMC	0.125	0.5
No Missing Codes	12/14/16	12	16	16	20	16/18	16	18/20	12	16/20	16/18	16/20
Total Harmonic Distortion (%)	.008/.003/.001	-80 dB	.001	.007	.0003	.0015	.0015	.0015	.02	-	-	-
Signal-to-Noise plus Distortion (dB)	73/83/92	72	92	80	-	92	87	105/110	70	-	-	-
Dynamic Range (dB)	73/83/92	72	92	84	120	95/100*	90	105/110	70	-	-	-
Power Needed (mW)	150	50	280/44	220	150	450/400	100/325	550	750	25	3	30
Conversion Method	Succ. Approx.	Succ. Approx.	Succ. Approx.	Delta Sigma	Delta Sigma	Delta Sigma	Delta Sigma	Delta Sigma	2-Step Flash	Delta Sigma	Delta Sigma	Delta Sigma
Power Down Mode			√		√	√	√	√		√	√	√
On-Chip Sample and Hold	√	√	√	√	√	√	√	√	√	√	√	√
On-Chip V. Ref		√		√		√	√	√			√	√
On-Chip Filtering				√	√	√	√	√		√	√	√
Statically Tested	√	√	√						√	√	√	√
Dynamically Tested	√	√	√	√	√	√	√	√	√			
Temperature Range	Com Ind Mil	Com Ind Mil	Com Ind Mil	Com Ind Mil	Com Ind	Com Ind Mil	Com Ind	Com	Com Ind Mil	Com Ind Mil	Ind Mil	Ind Mil
Number of Pins (DIP)	40	24	28	18	28	28	28	28	40	20	20/24	24
Packages	DIP PLCC LCC	DIP SOIC	DIP PLCC LCC	DIP SOIC	PLCC	DIP SOIC	DIP SOIC	DIP	DIP JLCC	DIP SOIC	DIP SOIC	DIP SOIC

NMC=No Missing Codes * CS5328 In Mono Mode GP=General Purpose

9

CS5321, CS5322, CS5323, CS5324, 24-bit Variable Band width ADC

The CS5323 or CS5321 modulator, combined with the CS5322 digital filter, offers >120 dB dynamic range in the DC to 1500 Hz frequency band. Seven different filter corner frequencies and output update rates are offered, allowing the ADC to be optimized for different types of seismic measurements. The CS5324 includes a modulator and the first stage of digital filtering, allowing users to implement their own final filter stage.

CS5317 16-bit Voice Band ADC

The CS5317 is well suited for a wide range of voiceband applications, from speech recognition to passive sonar. An on-chip PLL/Clock generator makes the part perfect for high-performance modems. The device features a 20 kHz word rate, a 10 kHz band width, 84 dB dynamic range and 80 dB THD.

CS5336 Audio Bandwidth ADC's

Selected members of our audio ADC family are now available in industrial or military versions (See the Digital Audio A/D Converter Section).

For complete data sheets on the products in this chapter, see the Crystal Semiconductor Data Acquisition data book, or contact Crystal.

CONTENTS

16, 14 & 12-Bit, Self-Calibrating A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12, 14 and 16-Bit Precision
- Conversion Times:

CS5016	16.25 µs
CS5014	14.25 µs
CS5012A	7.2 µs

- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 150 mW
- Low Distortion

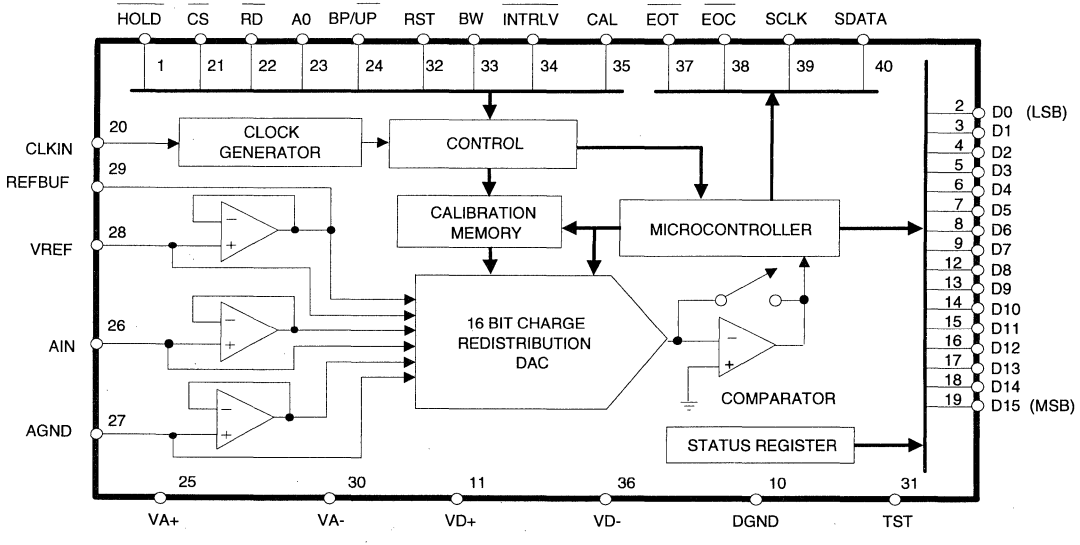
General Description

The CS5012A/14/16 are 12, 14 and 16-bit monolithic analog to digital converters with conversion times of 7.2µs, 14.25µs and 16.25µs. Unique self-calibration circuitry insures excellent linearity and differential nonlinearity, with no missing codes. Offset and full scale errors are kept within 1/2 LSB (CS5012A/14) and 1 LSB (CS5016), eliminating the need for calibration. Unipolar and bipolar input ranges are digitally selectable.

The pin compatible CS5012A/14/16 consist of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the devices' sampling architecture, acquires the input signal after each conversion using a fast slewing on-chip buffer amplifier. This allows throughput rates up to 100 kHz (CS5012A), 56 kHz (CS5014) and 50 kHz (CS5016).

An evaluation board (CDB5012/14/16) is available which allows fast evaluation of ADC performance.

ORDERING INFORMATION:
Contact Crystal Semiconductor



Semiconductor Corporation

CS5030 CS5031

12-Bit, 500 kHz, Sampling A/D Converters

Features

- Monolithic CMOS A/D Converter
  - 0.5µs Track/Hold Amplifier
  - 2µs A/D Converter
  - 2.5V Voltage Reference
  - Flexible Parallel, Serial and Byte interface
- 12-Bit ADC and Reference Accuracy
  - Total Unadjusted Error: ±1/2 LSB
  - Ref Tempco: 1ppm/°C
- Low Distortion
  - Signal-to-Noise Ratio: 72 dB
  - Total Harmonic Distortion: 0.01%
  - Peak Harmonic or Noise: 0.01%
- Low Power: 50mW

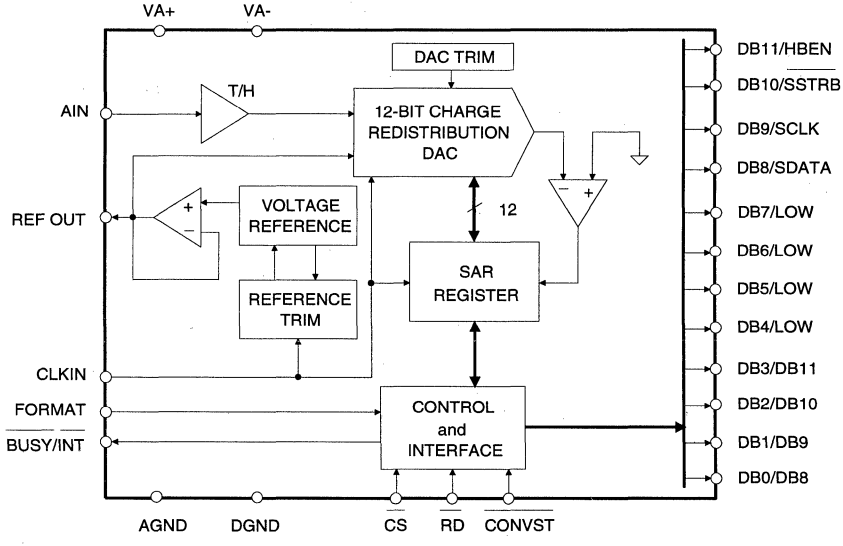
General Description

The CS5030, and CS5031 are complete monolithic CMOS analog-to-digital converters capable of 500 kHz throughput. On-chip calibration circuitry achieves true 12-bit accuracy for the ADC and on-chip reference over the full operating temperature range without external adjustments.

The CS5030/CS5031 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS5030/CS5031 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

ORDERING INFORMATION:
Contact Crystal Semiconductor



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

CRYSTAL
Semiconductor Corporation

CS5101A
CS5102A

16-Bit, 100 kHz/20 kHz A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 92 dB
  - THD: 0.001%
- Conversion Time
  - CS5101A: 8 µs
  - CS5102A: 40 µs
- Linearity Error: ± 0.001% FS
  - Guaranteed No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption
  - CS5101A: 320 mW
  - CS5102A: 44 mW
  - Power-down Mode: < 1 mW
- Evaluation Board Available

General Description

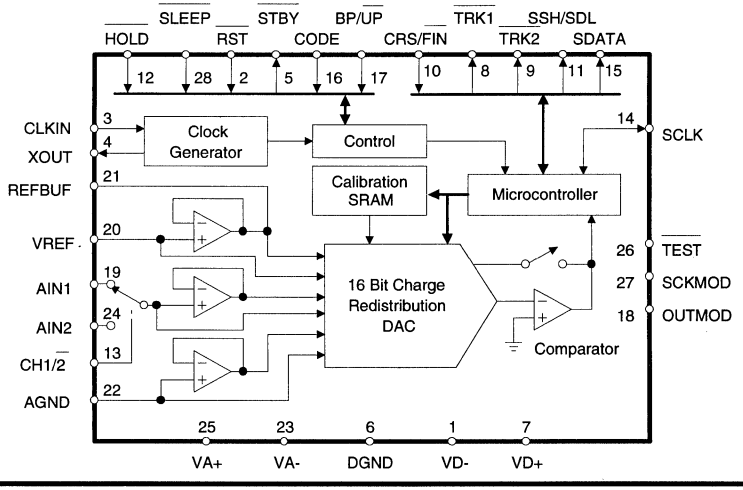
The CS5101A and CS5102A are 16-bit monolithic CMOS analog-to-digital converters capable of 100 kHz (5101A) and 20 kHz (5102A) throughput. The CS5102A's low power consumption of 44 mW, coupled with a power down mode, makes it particularly suitable for battery powered operation.

On-chip self-calibration circuitry achieves nonlinearity of ±0.001% of FS and guarantees 16-bit no missing codes over the entire specified temperature range. Superior linearity also leads to 92 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are minimized during the calibration cycle, eliminating the need for external trimming.

The CS5101A and CS5102A each consist of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The inherent sampling architecture of the device eliminates the need for an external track and hold amplifier.

The converters' 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION:
Contact Crystal Semiconductor



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Semiconductor Corporation

CS5126

16-Bit, Stereo A/D Converter for Digital Audio

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Stereo or Monaural Capability
  - Serial Output
- Monaural Sampling Rates up to 100 kHz
  - 50 kHz/Channel Stereo Sampling
- Signal-to-(Noise+Distortion): 92 dB
- Dynamic Range: 92 dB
  - 95dB in 2X Oversampling Schemes
- Interchannel Isolation: 90 dB
- 2's Complement or Binary Coding
- Low Power Dissipation: 260 mW
  - Power Down Mode for Portable Applications
- Evaluation Board Available

General Description

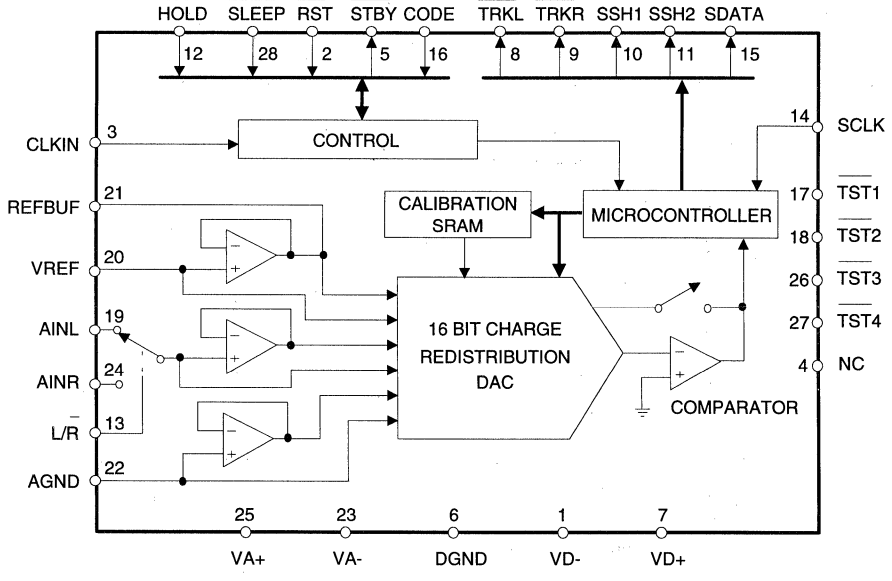
The CS5126 CMOS analog-to-digital converter is an ideal front-end for stereo or monaural digital audio systems. The CS5126 can be configured to handle two channels at up to 50kHz sampling per channel, or it can be configured to sample one channel at rates up to 100kHz.

The CS5126 executes a successive approximation algorithm using a charge redistribution architecture. On-chip self-calibration circuitry has 18-bit resolution thus avoiding any degradation in performance with low-level signals. The charge redistribution technique also provides an inherent sampling function which avoids the need for external sample/hold amplifiers.

Signal-to-(noise+distortion) in stereo operation is 92dB, and is dominated by internal broadband noise (1/2 LSB rms). When the CS5126 is configured for 2X oversampling, digital post-filtering bandlimits this white noise to 20kHz, increasing dynamic range to 95dB.

ORDERING INFORMATION: (was CSZ5126-KP)

CS5126-KP	0 °C to 70 °C	28-Pin Plastic DIP
CS5126-KL	0 °C to 70 °C	28-Pin PLCC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 TWX: 910-874-1352

Semiconductor Corporation

CS5317

16-Bit, 20 kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

General Description

The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

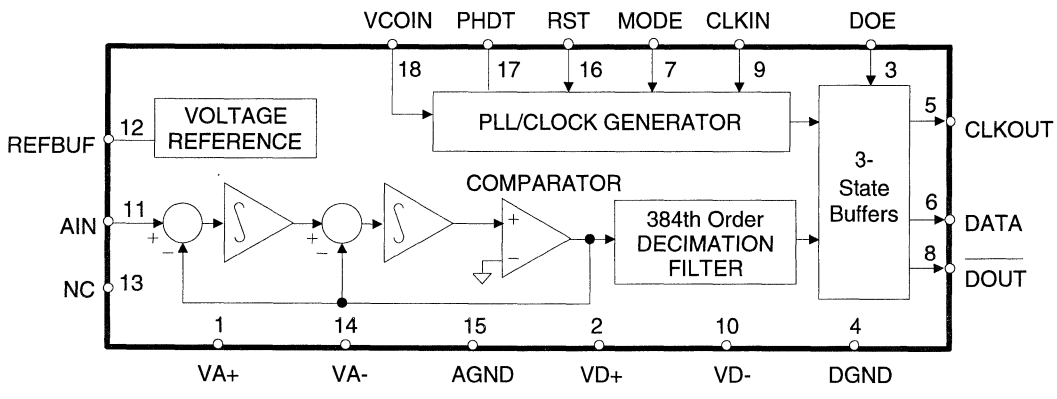
An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION:
Contact Crystal Semiconductor

Block Diagram



9

Semiconductor Corporation

CS5321

High Dynamic Range Delta-Sigma Modulator

FEATURES

- Delta-Sigma Architecture
  - Fourth-Order Modulator
  - Variable Sample Rate
  - Internal Track-and-Hold Amplifier
- Dynamic Range
  - 124 dB @ 411 Hz Bandwidth
  - 121 dB @ 822 Hz Bandwidth
- Signal-to-Distortion: 115 dB
- Input Range: ± 4.5V
- Low Power Dissipation:
  - Normal Mode: 40 mW
  - Low Power: 20 mW

DESCRIPTION

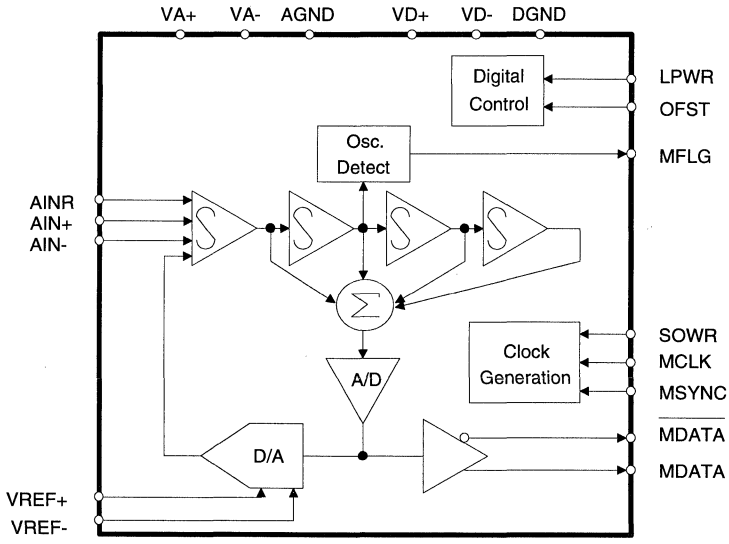
The CS5321 is a high dynamic range, fourth-order delta-sigma modulator intended for geophysical and sonar applications. Used in combination with the CS5322 digital FIR filter, a unique high resolution A/D system results.

The CS5321 provides an oversampled serial bit stream at 256 Kbits per second (SOWR=1) and 128Kbits per second (SOWR=0) operating with a clock rate of 1.024 MHz.

The monolithic CMOS design of the CS5321 insures high reliability while minimizing power dissipation.

ORDERING INFORMATION:

CS5321-BL	-55°C to +85°C	28-pin PLCC
CDB5321	Evaluation Board	



Preliminary Product Information

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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS5322/CS5323

24-Bit Variable Bandwidth A/D Converter

Features

- Monolithic CMOS A/D Converter
- Dynamic Range
  - 130dB @ 25 Hz Bandwidth
  - 120dB @ 411 Hz Bandwidth
- Delta-Sigma Architecture
  - Variable Oversampling: 64X to 4096X
  - Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  - Hardware or Software Selectable Options
  - Seven Selectable Filter Corner (-3dB) Frequencies: 25, 51, 102, 205, 411, 824 and 1650 Hz
- Low Power Dissipation: < 100mW

General Description

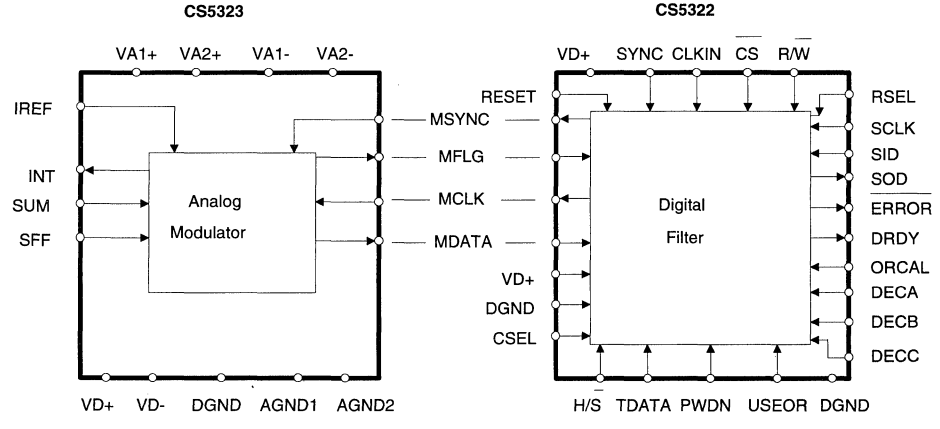
The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation.

ORDERING INFORMATION

CS5322-KL	0 to +70 °C	28-pin PLCC
CS5322-BL	-40 to +85 °C	28-pin PLCC
CS5323-KL	0 to +70 °C	28-pin PLCC
CS5323-BL	-40 to +85 °C	28-pin PLCC
CDB5322/3	Evaluation Board	



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS5324

120 dB, 500 Hz Oversampling A/D Converter

Features

- Monolithic CMOS A/D converter
- 120dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - —256X Oversampling
  - —Linear Phase Digital Filter
  - —Output Word Rate 32 kHz
- Low Power Dissipation: 150 mW
- Evaluation Board Available

General Description

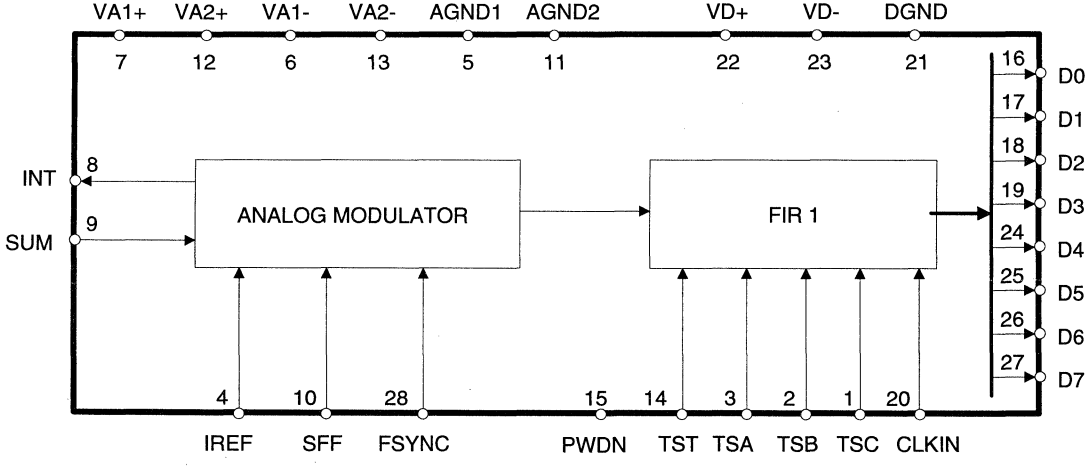
The CS5324 analog to digital converter is a unique, very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

ORDERING GUIDE:

CS5324-KL	0° to 70°C	28-pin PLCC
CS5324-BL	-40° to +85°C	28-pin PLCC
CDB5324	Evaluation Board	



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Crystal Semiconductor Corporation
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August '91
DS36PP3

Semiconductor Corporation

CS5412

12-Bit, 1MHz Self-Calibrating A/D Converter

Features

- Monolithic CMOS Sampling ADC
  On-Chip Track and Hold Amplifier
  Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  Typical Nonlinearity: 3/4 LSB
  No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

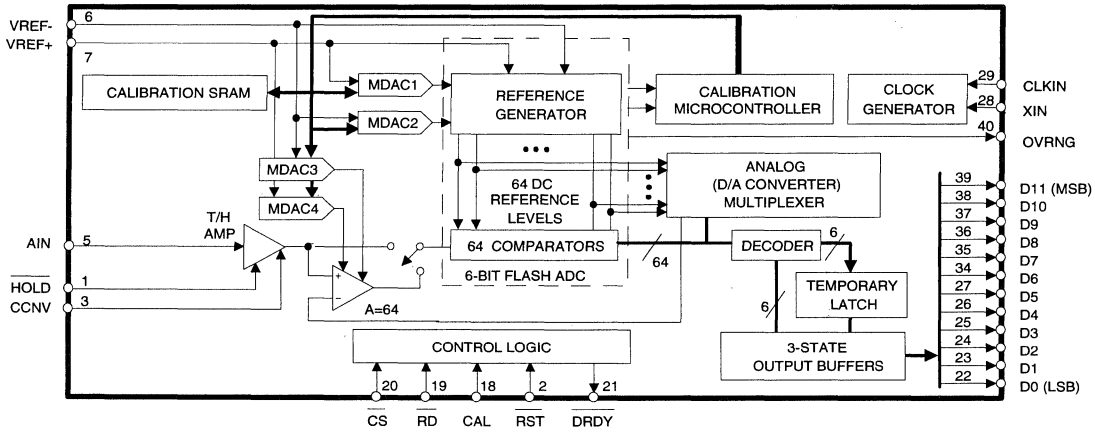
The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acquisition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

ORDERING INFORMATION:
Contact Crystal Semiconductor



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS5501
CS5503

Low-Cost, 16 & 20-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering 6-Pole, Low-Pass Gaussian Filter
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  - Linearity Error: ±0.0003%
  - Differential Nonlinearity:
    CS5501: 16-Bit No Missing Codes (DNL ±1/8LSB)
    CS5503: 20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  - µC-Compatible Formats
  - 3-State Data and Clock Outputs
  - UART Format (CS5501 only)
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  - 10µW Sleep Mode for Portable Applications
- Evaluation Boards Available

General Description

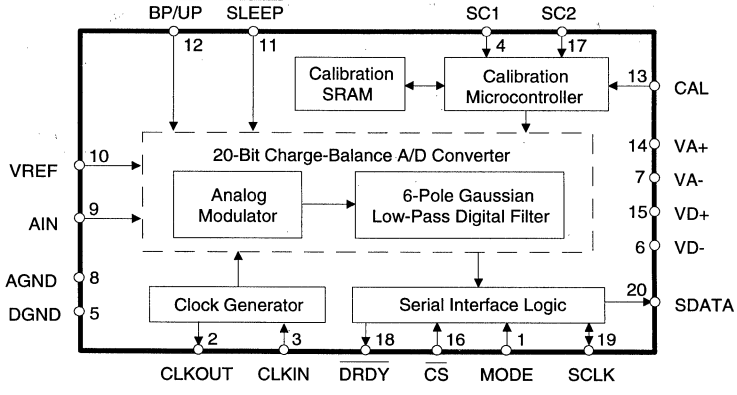
The CS5501 and CS5503 are low-cost CMOS A/D converters ideal for measuring low-frequency signals representing physical, chemical, and biological processes. They utilize charge-balance techniques to achieve 16-bit (CS5501) and 20-bit (CS5503) performance with up to 4kHz word rates at very low cost.

The converters continuously sample at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The converters' low-pass, 6-pole Gaussian response filter is designed to allow corner frequency settings from .1Hz to 10Hz in the CS5501 and .5Hz to 10Hz in the CS5503. Thus, each converter rejects 50Hz and 60Hz line frequencies as well as any noise at spurious frequencies.

The CS5501 and CS5503 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB for the CS5501 and less than 4LSB for the CS5503. The devices can also be applied in system calibration schemes to null offset and gain errors in the input channel.

Each device's serial port offers two general purpose modes of operation for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. In addition, the CS5501's serial port offers a third, UART-compatible mode of asynchronous communication.

ORDERING INFORMATION:
Contact Crystal Semiconductor



Crystal Semiconductor Corporation
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Semiconductor Corporation

CS5504

Low Power, 20-Bit A/D Converter

Features

- Offers superior performance to VFCs and dual-slope integrating ADCs
- On-Chip Self-Calibration Circuitry
- Two Differential Inputs
- Output update rates up to 100/second
- Pin-Selectable Unipolar/Bipolar Ranges
- Linearity Error: ±0.0015% FS
- 20-bit No Missing Codes
- Common Mode Rejection: 120 dB
- Low Power Consumption: 1.5 mW

General Description

The CS5504 is a 2-channel, fully differential 20-bit, serial-output CMOS A/D converter. The CS5504 uses charge-balanced (delta-sigma) techniques to provide a low cost, high resolution measurement at output word rates up to 100 samples per second.

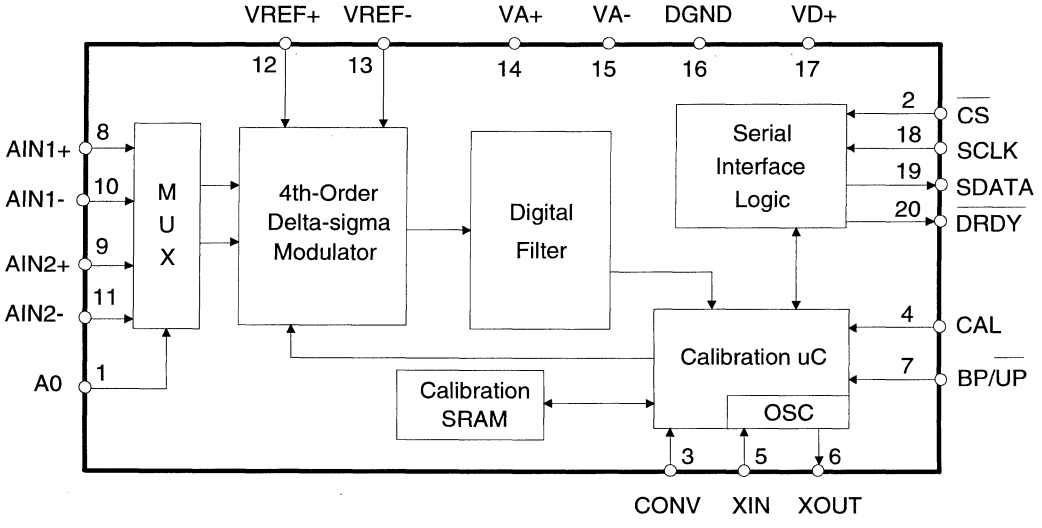
The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5504 has on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

Low power, high resolution and small package size make the CS5504 an ideal solution for loop-powered transmitters, panel meters, weigh scales and battery-powered instruments.

Ordering Information:

CS5504-BP	-40°C to +85°C	20-pin PDIP
CS5504-BS	-40°C to +85°C	20-pin SOIC



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS5505 CS5506
CS5507 CS5508

Very Low Power, 16-Bit and 20-Bit A/D Converters

Features

- Very Low Power Consumption
  Single supply +5V operation: 1.5 mW
  Dual supply ±5V operation: 3.0 mW
- Offers superior performance to VFCs and multi-slope integrating ADCs
- Differential Inputs
  Single Channel and Four-Channel pseudo-differential versions
- On Chip Self-Calibration Circuitry
- Linearity Error: ±0.0015% FS
- Output update rates up to 100/second
- Flexible Serial Port
- Pin-Selectable Unipolar/Bipolar Ranges

General Description

The CS5505/6/7/8 are a family of low power CMOS A/D converters which are ideal for measuring low-frequency signals representing physical, chemical, and biological processes.

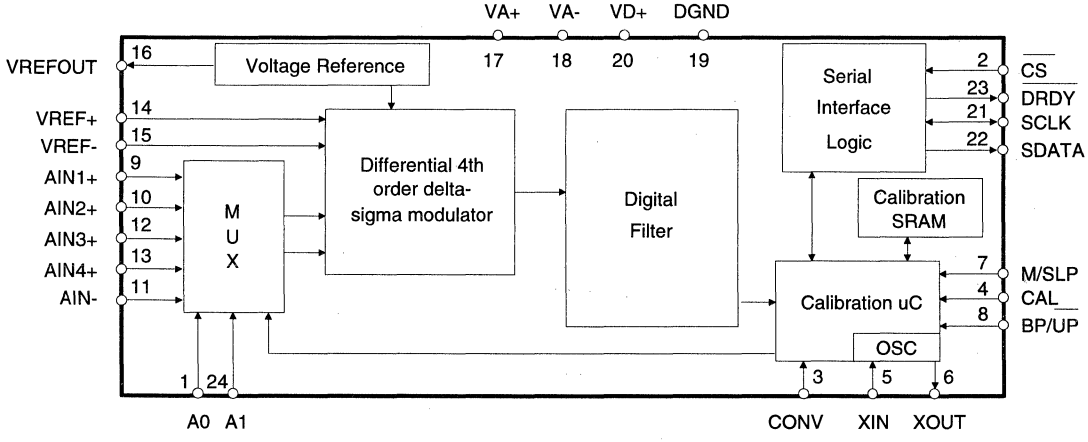
The CS5507/8 have single-channel differential analog and reference inputs while the CS5505/6 have four pseudo-differential analog input channels. The CS5505/7 have a 16-bit output word. The CS5506/8 have a 20-bit output word. The CS5505/7 sample upon command up to 100 output updates per second. The CS5506/8 sample up to 60 updates per second.

The on chip digital filter offers superior line rejection at 50 and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5505/6/7/8 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

The CS5505/6/7/8 serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

Ordering Information:
Contact Crystal Semiconductor



The CS5505/6 are illustrated. The CS5507/8 are single-channel differential input devices.

Semiconductor Corporation

CS5509

Single Supply, 16-Bit A/D Converter

Features

- Offers superior performance to VFCs and dual-slope integrating ADCs
- On-Chip Self-Calibration Circuitry
- Differential Input
- Output update rates up to 100/second
- Pin-Selectable Unipolar/Bipolar Ranges
- Linearity Error: ±0.0015% FS
- Differential Nonlinearity: ±1/2 LSB
- Common Mode Rejection: 120 dB
- Low Power Consumption: 1.5 mW

General Description

The CS5509 is a single supply, 16-bit, serial-output CMOS A/D converter. The CS5509 uses charge-balanced (delta-sigma) techniques to provide a low cost, high resolution measurement at output word rates up to 100 samples per second.

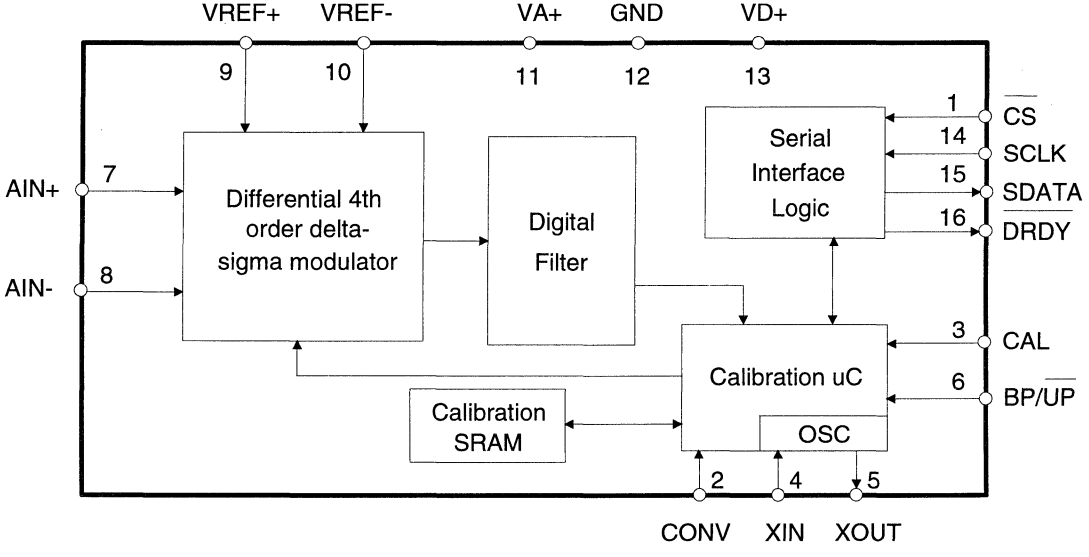
The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5509 has on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

Low power, high resolution and small package size make the CS5509 an ideal solution for loop-powered transmitters, panel meters, weigh scales and battery powered instruments.

Ordering Information:

CS5509-BP	-40°C to +85°C	16-pin PDIP
CS5509-BS	-40°C to +85°C	16-pin SOIC



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS5516
CS5520

16-Bit/20-Bit Bridge Transducer A/D Converters

Features

- On-chip Instrumentation Amplifier
- On-chip Programmable Gain Amplifier
- On-Chip 4-Bit D/A For Offset Removal
- Dynamic Excitation Options
- Linearity Error: ±0.0015% FS Max
  Offset and Full-Scale Errors: ±8 LSB_{20}
  20-Bit No Missing Codes
- CMRR at 50 / 60Hz >200dB
- System Calibration Capability with calibration read/write option
- 3, 4 or 5 wire Serial Communications Port
- Low Power Consumption: under 30mW
  10µW Standby Mode for Portable applications

General Description

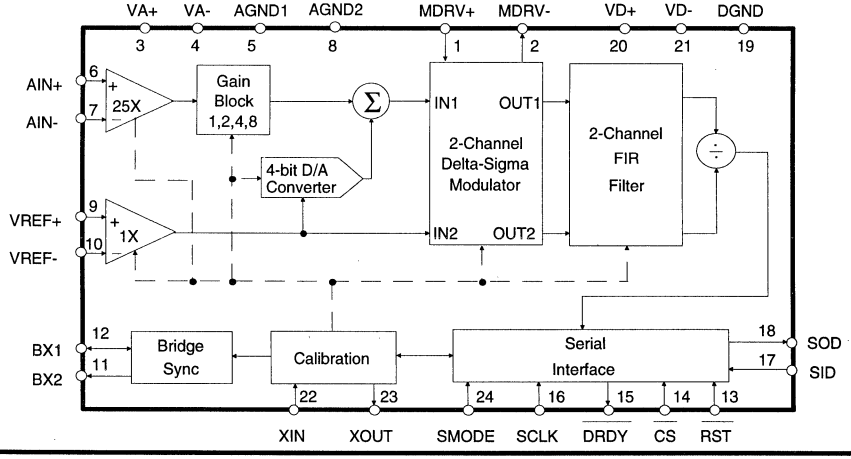
The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells, and pressure transducers. Any family of mV output transducers, including those requiring bridge excitation, can be interfaced directly to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier block, choice of DC or AC bridge excitation, and software selectable reference and signal demodulation.

The CS5516 uses delta-sigma modulation to achieve 16-bit resolution at output word rates up to 60Hz. The CS5520 achieves 20-bit resolution at word rates up to 60Hz.

The CS5516 and CS5520 sample at a rate set by the user in the form of either an external CMOS clock or a crystal. On-chip digital filtering provides rejection of all frequencies above 12Hz for a 4.096 MHz clock.

The CS5516 and CS5520 include system calibration to null offset and gain errors in the input channel. The digital values associated with the system calibration can be written to, or read from, the calibration RAM locations at any time via the serial communications port. The 4-bit DC offset D/A converter, in conjunction with digital correction, is initially used to zero the input offset value.

ORDERING INFORMATION:
Contact Crystal Semiconductor



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 : Fax (512) 445-7581

Low Power T1, E1 and ISDN Primary Rate Line Interface Circuits

Crystal Semiconductor offers a broad family of low power CMOS PCM line interface circuits, with each device optimized for a unique system application. The CS6152, CS61535A, CS61574A and CS61575 are recommended for use in new designs. Since introducing the industry's first T1 and E1 line interface circuits (the CS61534 and CS61544), we have shipped more CMOS PCM line interface ICs than any other vendor worldwide. Crystal Semiconductor's leadership continues with the best in pulse shapes, jitter attenuation, jitter tolerance and low power consumption.

Product	CS6152	CS61535A	CS61574A	CS61575
Rate	T1	T1/E1	T1/E1	T1/E1
Receiver Functions	Data Slicer	Clock/Data Recovery	Clock/Data Recovery & Jitter Atten.	Clock/ Data Recovery & Jitter Atten.
Transmitter Functions	Driver	Jitter Atten. & Driver	Driver	Driver
Serial Control Port	-	✓	✓	✓
DIP Package	24-pin, .3"	28-pin, .6"	28-pin, .6"	28-pin, .6"
Surface Mount	28-pin PLCC	28-pin PLCC	28-pin PLCC	28-pin PLCC
AMI/B8ZS/ HDB3 Coder	-	✓	✓	✓
Jitter Tolerance of Receiver	> 300 UI	> 300 UI	28 UI	138 UI

Line Interface Comparison Table

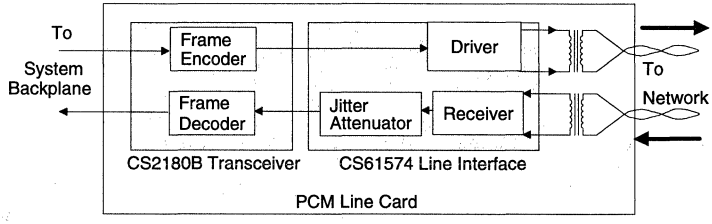
CS6152: Basic DSX-1 driver and receive buffer. For low power cards using digital-ASIC clock recovery. Ideal for trunk card bays where T1 density is limited by heat dissipation.

CS61535A: Enhanced transmit-side jitter attenuator supports SONET VT1.5 and VT2, and other high speed transmission systems such as digital microwave radio and M13 multiplexers.

CS61574A and CS61575: Receive-side jitter attenuation supports loop-timing in customer-premises equipment and in channel banks. In the presence of large amplitudes of received jitter, the CS61575 provides more jitter attenuation than any device in the industry, and is ideal for AT&T 62411 applications.

T1 Transceiver

Our CS2180B T1 Transceiver is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (D4, SLC-96 and T1DM and ESF). Serial interface and control registers make it simple to configure from a microprocessor, including per channel control options. Packages available include 40-pin DIP or 44-lead PLCC.



The CS2180B is ideal for use with Crystal's family of line interface IC's

Quartz Crystals

To complement our family of T1 Line Interface circuits, Crystal Semiconductor supplies pullable quartz crystals. The CXT6176 (for T1 applications at 1.544 Mbps) and CXT8192 (for E1 applications at 2.048 Mbps) are designed for 100% compatibility with our PCM line interface and jitter attenuator circuits.

Modem Analog Front End

Crystal's CS6453 provides the industry's first analog front end designed to support data and voice communications. The CS6453 is optimized for PC modem cards that implement telephone set, answering machine emulation, and need to support business audio IO. In addition to providing an 84dB ADC and DAC for connection to the Data Access Arrangement, the CS6453 includes a 125 ohm earphone driver, an 8 ohm speaker driver, and interface circuitry for an electret microphone. The CS6453 can operate with either 3.3V or 5.0V power supplies.

Acoustic Echo Cancellers

Crystal's CS6400 and CS6401 provide the industry's first echo cancellers optimized for cost sensitive applications. The CS6400 is an echo canceling codec that includes a 16-bit voiceband codec plus a application-specific DSP that provides 30 dB of echo return loss for echo tails of up to 64 ms in length. The DSP implements a fully adaptive, least mean square update algorithm with graded beta normalization. Proprietary algorithms also provide outstanding voice quality in environments with echo tails longer than 64 ms.

The CS6401 is a programmable echo canceller which can be used to develop algorithms for the CS6400.

Ethernet

Crystal is the first company to bring the benefits of low-power CMOS technology to Ethernet/Cheapernet transceivers. The CS83C92C uses up to 40% less power than the DP8392A and DP8392B. This translates into increased reliability and compatibility with surface mount technology. The CS83C92C is the first Ethernet transceiver which is fully compliant with ISO/IEEE 802.3.

In 1994, Crystal will be introducing a broad family of highly-integrated 10Base-T products.

DTMF Receivers

Crystal has improved on industry standard DTMF receiver ICs while maintaining 100% pin compatibility. Our device features on-chip filters which offer the best possible signal-to-noise ratio allowing highly accurate decoding of telephone tones.

Jitter Attenuation Circuits

Our jitter attenuation technology is available stand-alone for a wide variety of applications. The CS61600 is ideal for T1 and E1 applications while the CS80600 attenuates jitter in T2, 2nd-level CEPT lines and Token Ring LANs. Both attenuators can be used with external divide circuits to handle low frequencies.

CONTENTS

See the Crystal Telecommunications Data Book
for the complete data sheets on the above products

T1 Transceivers

Features

- Monolithic T1 Framing Device
- Both Transceivers support D4 and ESF framing formats
- CS2180B also supports SLC-96 and T1DM framing formats
- CS2180B has updated AIS and Carrier Loss detection criteria
- CS2180B is Pin Compatible with CS2180A, DS2180A and DS2180

General Description

The CS2180A and CS2180B are monolithic CMOS devices which encode and decode T1 framing formats. The devices support bit-seven and B8ZS zero suppression, and bit-robbed signaling. Clear channel mode can be selected on a per channel basis.

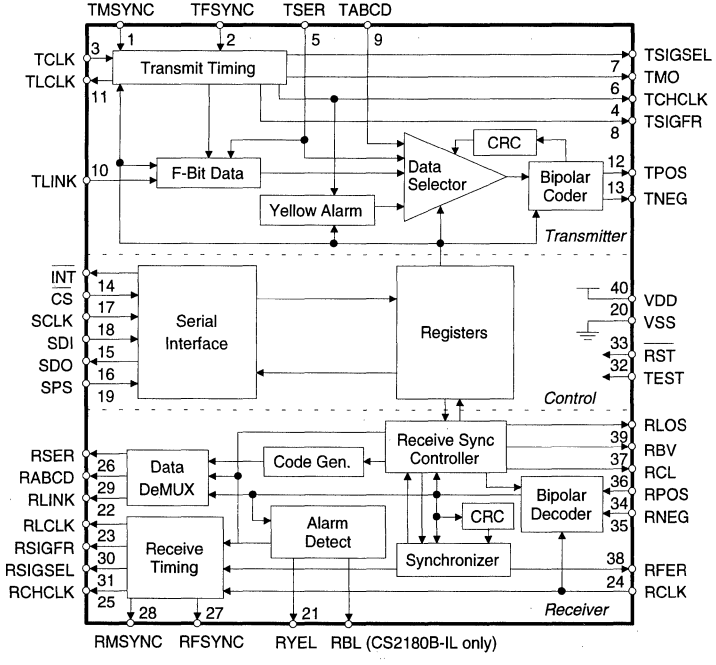
The serial interface has been enhanced to allow the CS2180A and CS2180B to share a chip select signal and register address space with the CS61535A, CS61574A and CS61575 PCM Line Interface ICs.

Applications

- T1 Line Cards
- ISDN Primary Rate Line Cards

Ordering Information:

CS2180B-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180B-IL	44 Pin PLCC	-40 to 85 °C
CS2180A-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180A-IL	44 Pin PLCC	-40 to 85 °C



Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS6152

Low Power T1 Analog Interface

Features

- Provides Analog T1 Line Interface
- Low Power Consumption (normally 180 mW)
- EXPERT *Pulse* ™ Programmable Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer Which Compliments Digital Gate Array Clock-Recovery Circuits
- Driver Performance Monitor
- Minimal External Components

General Description

The CS6152 combines the analog transmit and receive line interface functions for T1 system interface in one device. The T1 analog interface operates from a 5 Volt supply, and is transparent to the T1 framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. The device provides the ideal front-end to digital gate array based clock recovery circuits.

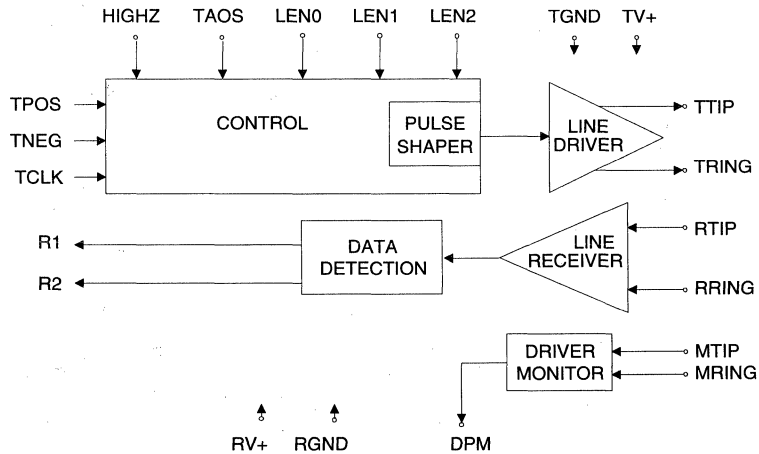
Applications

- Interfacing Network Equipment such as Multiplexer, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexer, Data PBX's and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS6152A-IP	-	24 Pin Plastic, 300 mil DIP
CS6152-IL	-	28 Pin J-lead PLCC

Block Diagram



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(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS61535A

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes

General Description

The CS61535 and CS61535A combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device. The line interface unit (LIU) operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. The transmitter uses a 32-bit elastic store to remove jitter from the transmit data.

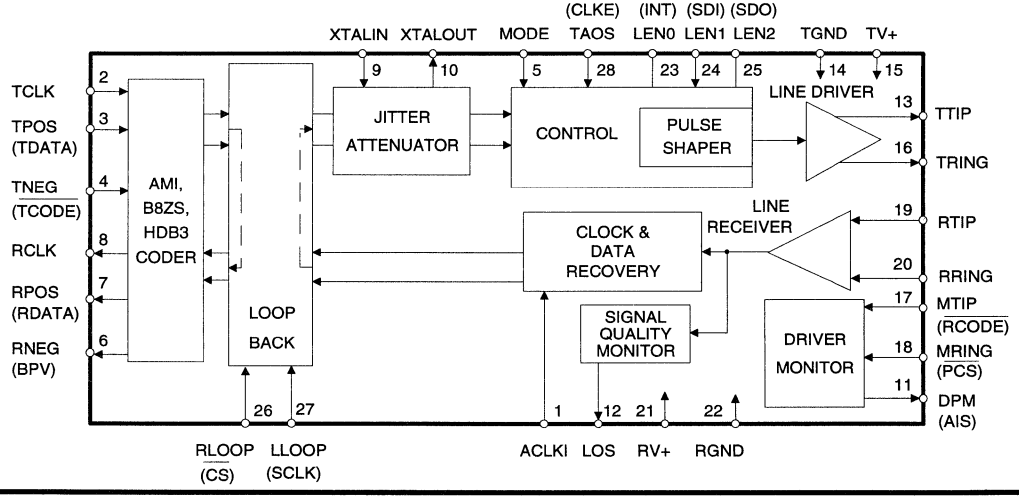
Applications

- Interfacing network transmission equipment such as SONET multiplexer and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to PCM-30 links.

Ordering Information

CS61535A-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS61535A-IL1	28 Pin PLCC (j-leads)	T1 & PCM-30
CS61535-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS61535-IL1	28 Pin PLCC (j-leads)	T1 & PCM-30

Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS61575 CS61574A CS61574

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, Jitter Attenuation & Clock Recovery Functions
- Fully Compliant with AT&T 62411 (1990 Version) Jitter/Synchronizer (Stratum 4, Type II) Requirements
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss

General Description

The CS61575, CS61574A and CS61574 combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device.

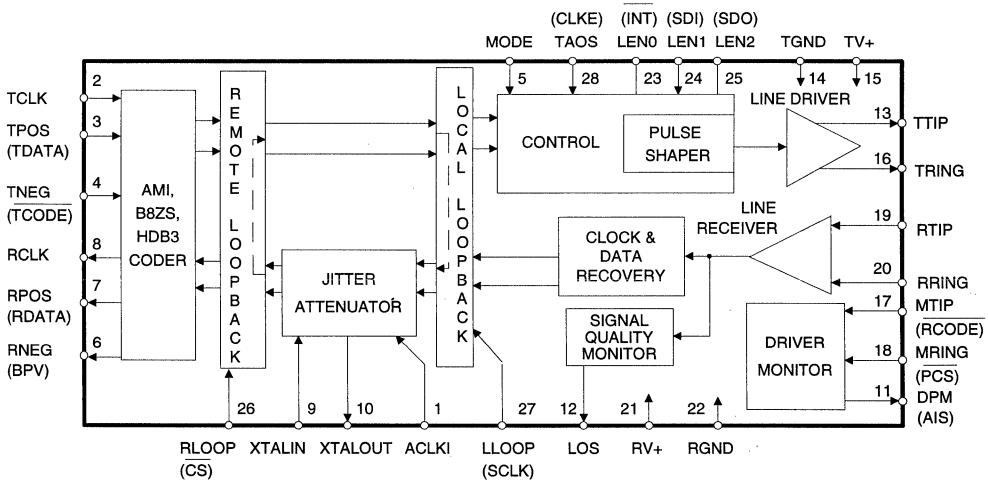
The line interface unit (LIU) operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. The CS61575 receiver uses a 128-bit elastic store to remove jitter from the incoming data. The CS61574A and CS61574 employ a 32-bit elastic store.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION -
Contact Crystal Semiconductor

Block Diagram



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Crystal Semiconductor Corporation
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(512) 445-7222 FAX:(512) 445-7581

Semiconductor Corporation

CS61600

PCM Jitter Attenuator

Features

- Unique Clock-Tracking Circuitry Filters 50 Hz or Higher Frequency Jitter for T1 and PCM-30 Applications
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS61600 from Crystal Semiconductor accepts T1 (1.544 Mb/s) or CCITT standard (2.048 Mb/s) data and clock inputs, and tolerates at least 7 (and up to 14) unit intervals, peak-to-peak, of jitter. Before outputting data and clock, jitter is attenuated using an internal clock-tracking variable oscillator and a 16 bit FIFO elastic store.

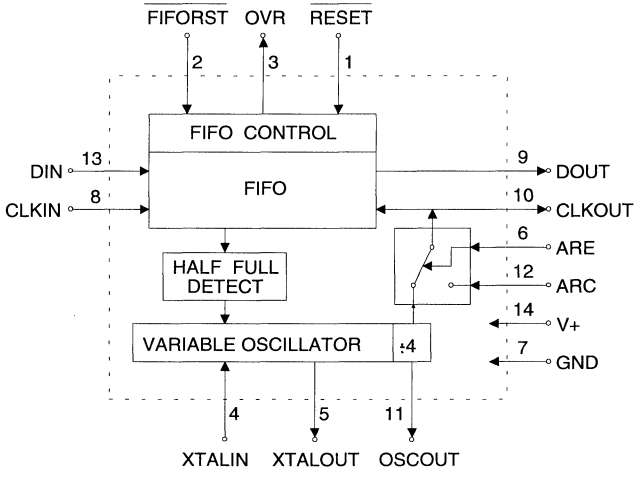
The jitter attenuation function can be determined by appropriate specification of the external crystal.

The CS61600 is transparent to data format, and is intended for application in carrier systems, switching systems, Local Area Network gateways and multiplexers.

ORDERING INFORMATION

CS61600-ID1 - 14 Pin CERDIP; T1 and 2.048 MHz
CS61600-IP1 - 14 Pin Plastic DIP; T1 and 2.048 MHz

Block Diagram



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Semiconductor Corporation

CXT6176
CXT8192

Pullable Quartz Crystals

Features

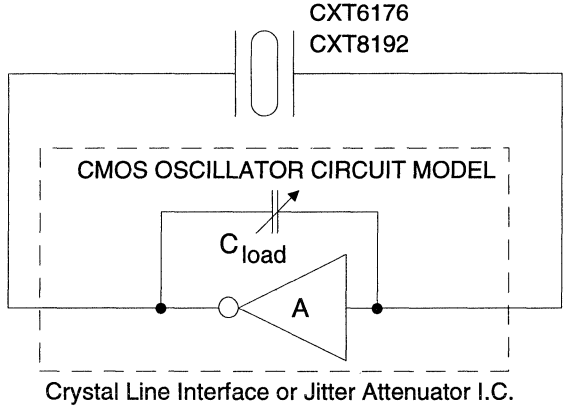
- Complements CS61534, CS61535, CS61535A, CS61544, CS61574, CS61574A, and CS61575 PCM Line Interface integrated circuits and CS61600 PCM Jitter Attenuator.

Description

Crystal Semiconductor's line interface and jitter attenuator IC's require unique performance specifications for the crystals. The CXT6176 and CXT8192 are built to meet Crystal's specifications for T1 and PCM-30 applications respectively.

Ordering Information

CXT6176	Crystal for T1 Applications
CXT8192	Crystal for PCM-30 Applications



Crystal Line Interface or Jitter Attenuator I.C.

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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS6400

Echo-Cancelling Codec

Features

- Applicable in:
  - Digital-Cellular Hands Free
  - Analog-Cellular Hands Free
  - Office Speaker Phones
  - Desktop & Video Teleconferencing
  - Noise Cancellation
  - Network/Base Station
- Echo Cancellation
  - 512 Tap (64 ms at 8 kHz Fs)
  - Split Mode For Two ECs
  - Cascadable For Longer Response
  - Coefficient Dump/Restore
  - No Signal Delay
- Zero-Glue Serial Data/Control Interface
- On-Chip Codec
  - > 80 dB Dynamic Range
  - > 70 dB S/(N+D)
  - 300-3400 Hz Bandwidth
- Optional Supplementary Voice Switching

General Description

The CS6400 is an application-specific digital signal processor optimized for acoustic echo and noise cancellation applications. A high-quality codec is integrated with the processor to provide a complete, low-cost echo and noise-cancellation solution.

The CS6400 is a fully independent processor that requires no signal processing support to implement its cancellation functions. Volume control, mute, sleep, and two loopback functions are also provided.

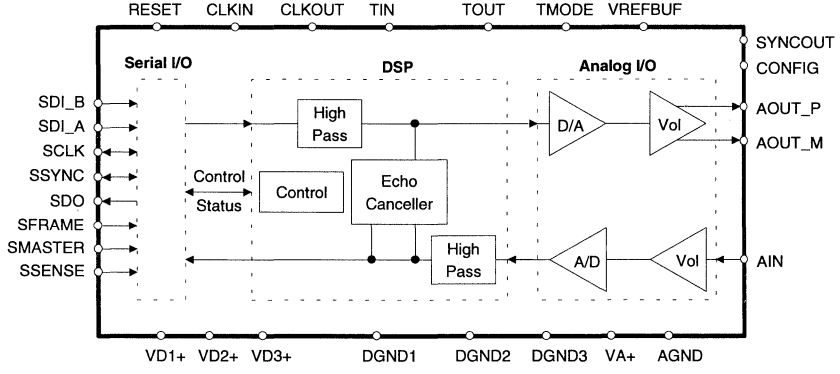
The on-chip A/D and D/A converters employ oversampling technology, which eliminates the need for complex external anti-aliasing and reconstruction filters, further reducing system cost.

The CS6400 has a zero glue-logic serial interface that is compatible with most DSPs. A clock and sync line control the transfer of serial data via the separate serial data-in and data-out pins. Both 15-bit audio data and control/status information are multiplexed on this serial channel using a steering bit.

The CS6400 can easily be tailored to special applications via metal-mask options. Custom development services for producing such derivatives are available from Crystal.

The CS6400 is packaged in a 28-pin PLCC.

ORDERING INFORMATION: CS6400



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS6401

Programmable Echo Canceller

Features

- For All Echo Canceller Applications
  - Digital Cellular Network Equipment
  - Analog Cellular Hands Free
  - Digital Cellular Hands Free
  - Office Speaker Phones
  - Desktop Teleconferencing
  - Long Distance Network Equipment
- Echo Cancellation
  - 8 kHz Sampling Rate
  - 512 tap (64 ms)
  - Split Mode for Two ECs (total taps = 512)
- Cascadable For Longer Impulse Response

General Description

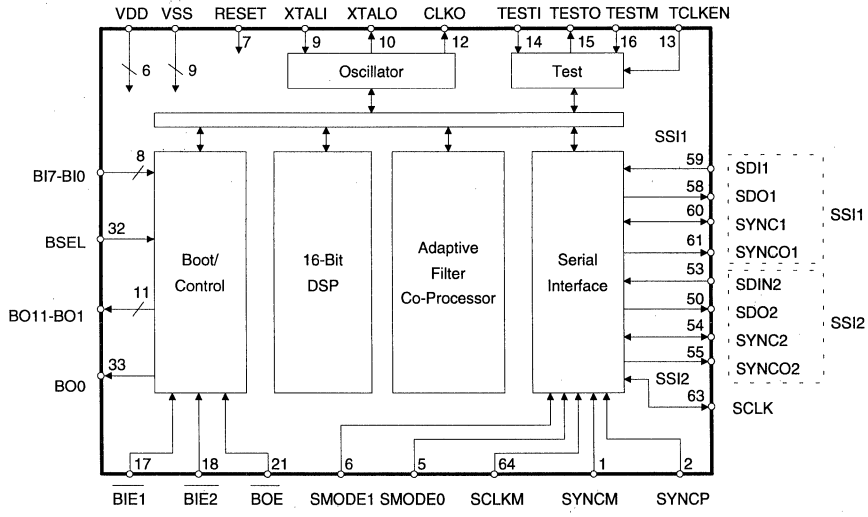
The CS6401 is a digital signal processor optimized for acoustic and/or network echo cancellation algorithms. The CS6401 implements all the adaptive filtering and control algorithms needed for high quality echo cancellation for a variety of applications. Crystal has developed the echo cancellation algorithms, and provides the DSP object code with the evaluation board. Custom algorithm development services are available from Crystal.

The CS6401 contains four main blocks:

- 16 MIPS, 16-Bit Programmable DSP
- 512-tap Adaptive FIR Filter Hardware Accelerator
- Data I-O Serial Interface
- Boot/Control Interface

ORDERING INFORMATION

CS6401-CQ	64-pin Plastic QFP
CDB6401	Evaluation Board with object code



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS6453

Modem and Audio Analog Front End

Features

- Complete Voiceband DSP Front-End
  - 24-Bit A/D Converter
  - 18-Bit D/A Converter
- 84 dB Dynamic Range and 80 dB Signal-to-Distortion (at full scale)
- Supports telephone emulation
- Supports business audio
- On-chip speaker driver for modem monitoring
- Supports PCMCIA digital speaker signal
- 3.0 to 5.5V power supply range

General Description

The CS6453 is a high-resolution analog-to-digital and digital-to-analog converter for V.fast, V.32bis, V.32 and other high performance modems.

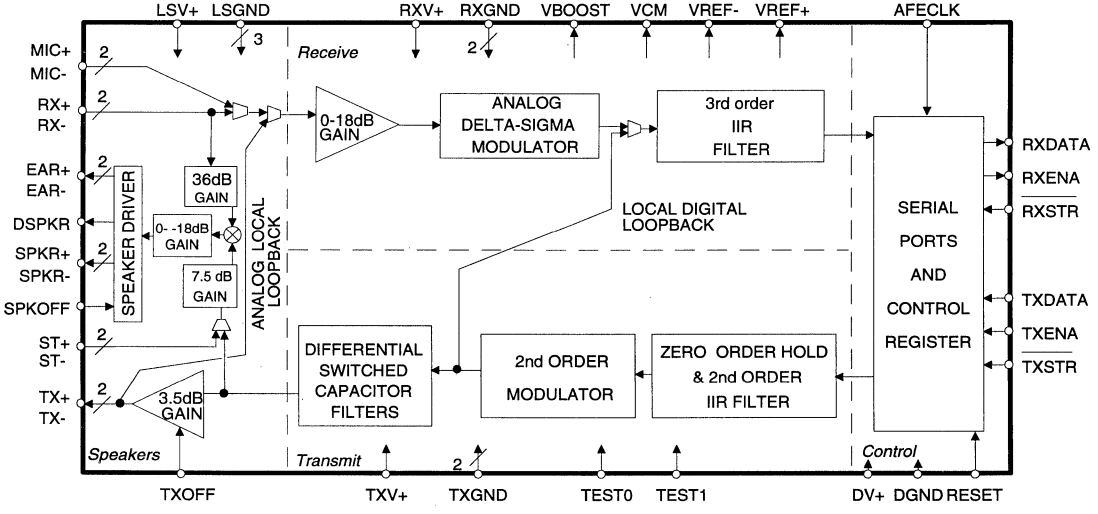
The CS6453 also supports telephone emulation. In telephone emulation the CS6453 and external DSP collectively implement both modem and telephone set capabilities. This allows an end-user to connect a handset to the "modem" card, and alternatively use the telephone connection for voice and data.

The CS6453 has 5 kHz bandwidth for modem and telephone applications, and 10 kHz bandwidth for business audio applications. The business audio capability allows the modem to playback and input audio files.

The CS6453 also supports the digital speaker signal of the PCMCIA interface standard. The modem can transfer the modem monitor signal via PCMCIA to the system speaker.

ORDERING INFORMATION:

CS6453-CQ 44-Pin QFP package



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS80600

High Speed Jitter Attenuator

Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs and removes up to ±3 data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

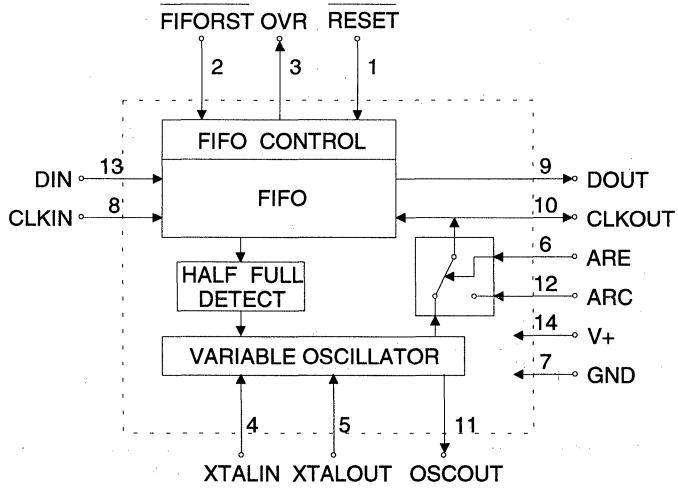
Applications

- **Token Ring:** The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adapter cards, in active wiring concentrators, and in repeaters.
- **PCM:** TIC, T2, and CEPT2 and second order multiplexers.

ORDERING INFORMATION

CS80600-P - 14 Pin Plastic DIP

Block Diagram



Crystal Semiconductor Corporation
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Semiconductor Corporation

CS83C92A
CS83C92C

Coaxial Transceiver Interface

Features

- Implemented in High Voltage, Low Power CMOS
- Compatible with National's DP8392A
- CS83C92C is Compliant With ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Transceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive & Transmit Mode Collision Detection
- Standard 16-pin DIP Package & 28 pin PLCC

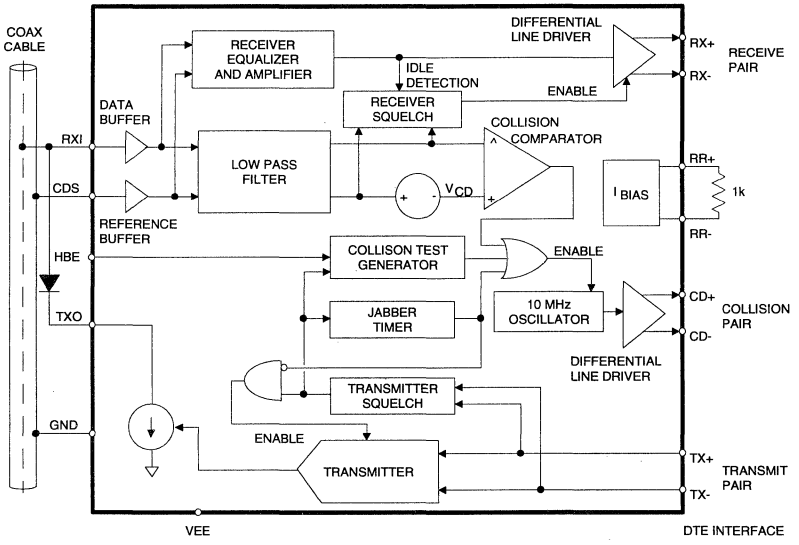
General Description

The CS83C92 Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 Ethernet Data Link Controller and the CS8023A Manchester Code Converter. The CS83C92A is fully compatible with the DP8392A but the CS83C92A is built in CMOS technology (hence the 83"C"92). The CS83C92C is a higher performance grade which is compliant with IEEE 802.3 specifications.

For Ethernet applications, the CS83C92 is mounted on the COAX cable, and connects to the station equipment via an AUI cable. In a Cheapernet network, the CS83C92 is usually mounted on the LAN adapter card in the station equipment where it connects to the thin COAX through a BNC connector.

ORDERING INFORMATION:

CS83C92A-CP	PDIP	CS83C92C-CP	PDIP
CS83C92A-CL	PLCC	CS83C92C-CL	PLCC



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Crystal Semiconductor Corporation
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(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS8870

DTMF Receiver

Features

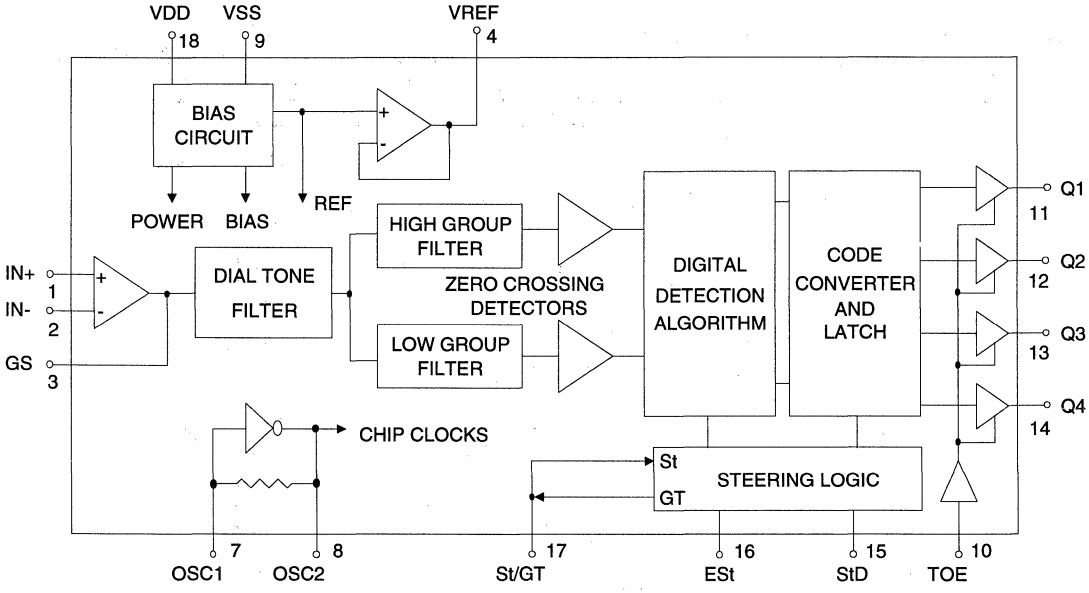
- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitivity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870B

General Description

The CS8870 is a fully integrated DTMF (Dual Tone Multifrequency) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using Crystal's CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

ORDERING INFORMATION
CS8870-IP - 18 Pin Plastic DIP

Block Diagram



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CONTENTS

PRODUCT CATEGORY LEVELS

Crystal's integrated circuit (IC) products are fabricated, assembled and tested either in-house or through one or more subcontractors. Qualification and manufacturability criteria are defined for each of four product category levels achievable during the product life cycle of an IC. Products are classified by the most stringent category level requirements met. Crystal's goal is to achieve Level I (World-Class) status for the majority of its product families. The product category levels are:

Level IV:	Engineering Prototype (EP) Release
Level III:	Production Level III
Level II:	Production Level II
Level I:	World Class

Level IV -- Engineering Prototype Qualification (EP)

Level IV is the first qualification level for IC products. It is used for early sampling and risk production builds. Qualification tests to achieve Level III begin shortly after the receipt of first functional devices. Level IV packaged devices are marked with an additional "EP".

Level III -- Production Level III

Level III is the second qualification level for IC products. This level is applicable to devices which are on track to achieving a Production Level II qualification and provides an interim reduction in the risk of substandard product shipments to customers. Comprehensive production test programs (with guardbands) are used for testing Level III products. Characterization of initial products is complete. Qualification tests have been completed per the criteria shown in the Qualification Criteria Table at the front of this databook.

Level II -- Production Level II

Level II is the high volume production qualification level for IC products. Level II products have met the goals for sustainable manufacturability and reliability by passing a comprehensive series of qualification tests, completing product documentation, and demonstrating product performance through detailed characterization.

Level I -- World Class Products

Level I is the highest level attainable for any product family. Qualification tests for Level I involve routine monitoring of ramped product families over a period of time to measure increasingly stringent reliability and quality levels that require a substantial number of devices and device-hours. Additionally, sources of variation throughout the manufacturing process (fab, assembly and test) are monitored and reduced over time following industry standard learning curves. This provides a statistical, pro-active approach to direct improvements in reliability performance and outgoing quality. It is the goal of every product family to achieve Level I status.

DEFINITION OF DATA SHEET TYPES

Each product developed by Crystal will be supported by technical literature where the data sheets progress through the following levels of refinement:

I. Product Preview

This is a 1-to-4 page document which describes the main features and specifications for a product that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

II. Preliminary Product Information

This is the first document completely describing a new product. It contains an overview, specifications, timing diagrams, theory of operation, pinout diagram, applications information, ordering guide and mechanical information. The numbers in this data sheet are based on prototype silicon performance and on worst-case simulation models. The specifications represent the designer's best estimate for the "real" numbers. Min and max values are included where possible. The purpose of this document is to provide system designers with technical information sufficiently detailed to guarantee that they can safely begin active development.

III. Final Data Sheet

This is an updated version of the preliminary data sheet reflecting actual production performance of the final product. Updates include tighter specifications, more min and max values, and any application information that has arisen during the early life of the part. The purpose of this document is to communicate the confirmed performance of products which have passed qualification, been fully characterized, and are in production.

RADIATION RESISTANCE PERFORMANCE

Crystal products are manufactured using various CMOS technologies. While not able to withstand large doses of radiation, our products are suitable for operation in low dose applications. Indeed, the self calibrating architecture of many of the A/D Converters is able to compensate for the effects of radiation.

Crystal will assist customers to test parts for radiation resistance by supplying free, data-logged parts. In exchange, we would like the parts returned to us, so that we can measure their post-radiation performance. In addition, we would like a copy of any report that is generated, along with permission to publish the report for other customer's information.

Several customer's have already undertaken radiation testing of our A/D Converters. Please contact the factory for the latest information and copies of the radiation performance reports.

RELIABILITY METHODS

I. CONCEPT OF RELIABILITY

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in a more quantitative sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can best be summarized by the reliability life or "bathtub" curve (Figure 1). The reliability performance is characterized by three phases: infant mortality, useful life, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period is aptly named wearout. Using proper design guidelines and device applications, this period is shifted well beyond the lifetime required by the user.

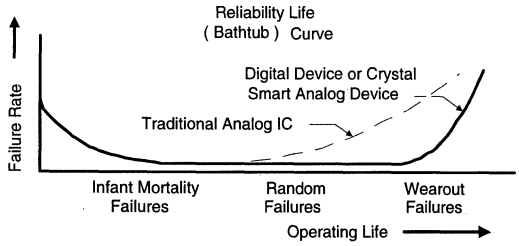

Figure 1.

An item of great importance in evaluating reported reliability characteristics is the definition of a failure. Crystal's definition of a failure is any device that fails to meet ANY data sheet parameter. Crystal's digital self-calibration techniques provide stable performance over temperature and life. Traditional Analog IC's and hybrids exhibit wearout mechanisms very early in the life of the product. One competitor's analog-to- digital converter's linearity error stability is specified at ± .00075 % per 1000 hours at 25 °C. Stability degradation at 70 °C is unspecified and is likely to be accelerated greatly as temperature increases. The dashed line of Figure 1 is typical of the wearout seen in a competitor's Analog IC or hybrid. As you can see, wearout begins much earlier than a digital device or a mixed analog and digital chip utilizing Crystal's SMART analog design architecture and CMOS wafer technology.

II. CRYSTAL SEMICONDUCTOR RELIABILITY STRESSING

These stresses are done on every new product, assembly house or fabrication subcontractor. Some of Crystal's acceptance criteria and goals are as described in the Qualification Criterion Table in section 1 of this data book.

Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate thermally-activated failure mechanisms through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level to further stress the oxides of the device. All devices used in life stress are sampled directly from the production flow with no special processing or prescreening. Stressing is performed per MIL STD 883, method 1015, condition D (dynamic signals). These dynamic conditions simulate as much as possible actual operating conditions in an application.

Infant mortality (48 hrs at 125 °C), early operating life stress (168 hrs at 125 °C) and long term operating life (typically 1000 hrs at 125 °C) are reported . Infant mortality life simulates approximately 3-4 months in the field at 55 °C and is reported as a percent. Early and Long term life simulate the total failures seen in the field and are expressed in FITS (failures in time). 1 FIT = 1 failure per billion device-hours. Derating of early and long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60 % upper confidence limit (UCL) and .7 electron volts (eV) activation energy are used in this calculation.

85 °C/85% R.H.

85 °C/ 85% R.H. is an environmental stress performed at a temperature of 85 °C and at a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal-voltage static bias is applied, with minimum power consumption, to the device, to accelerate the electrolytic corrosion of the metallization. Failures are expressed in % /time with 168, 500, and 1000 hour cumulative results reported.

Autoclave

Autoclave is also an environmental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are 121 °C, 100% relative humidity, and 1 atmosphere of pressure (15 psig), with no bias applied to the circuit. Corrosion of the die is the expected failure mechanism. Stressing is usually performed for 144 hours. Failures are expressed in %/time with 48, 96, and 144 hour results reported.

Temperature Cycling

Temperature cycling typically accelerates the effects of the thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010, Condition B (-55 °C to +125 °C) or C (-65 °C to +150 °C). Stressing is done in an air environment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in %/cycles, with 100, 500, and 1000 cycle results reported.

Thermal Shock

The objective of thermal shock is basically the same as that of temperature cycling - to exercise the difference in thermal expansion coefficients within the integrated circuit package and die. Thermal shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, method 1011, Condition B (-55 °C to +125 °C). In one cycle of thermal shock, devices are placed in a fluorocarbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with fluorocarbon at 125 °C for five minutes. Stressing is performed for 500 cycles. Failures are expressed in %/cycles, with results reported at 100, 200, and 500 cycles.

Electrostatic Discharge

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883 method 3015, which simulates the resistance (1500Ω) and capacitance (100 pF) of the human body. Also the machine model test is performed with a 0Ω resistance and a capacitance of 200 pF to simulate, as its name implies, a typical insertion tool, handler, etc. that comes in contact with the leads of a semiconductor device.

Latchup

Latchup testing is performed to ascertain whether a device can sustain SCR latchup due to a DC current input. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a positive and negative DC current forced into it. This test is performed per the standard test procedure recognized by JEDEC.

C dv/dt Latchup Testing

This test is performed to evaluate the susceptibility of a CMOS device's power pin to instantaneous ESD discharge into a power supply pin or a rapid ramp of a power pin during power up. Positive and negative pulses are supplied to the power supply pins with a change in voltage of greater than 500 V/µs and a 0 to 5 V risetime of less than 15 ns. Ground, V_{SS}, and the pin under test are connected to ground. The supply current is monitored for excessive current.

III. FAILURE RATE CALCULATIONS

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. Thermally accelerated failure rates can be derated to actual operating conditions by commonly accepted mathematical models.

Operating life stress is usually reported in the derated form. That is, operating life is performed at 125 °C and results are reported for an equivalent time at a typical operating stress temperature for an application, generally 25 °C, 55 °C, or 70 °C. Failure rates for other temperatures are calculated using a computed acceleration factor.

There are many probability models used in reliability analysis for calculating failure rates. The simplest form of calculating a failure rate (F.R.) would be to divide the number of failures observed after test (N) by the number of device-hours of stress.

$$\text{F.R.} = \frac{N}{D \bullet H} \qquad (1)$$

where D is the number of devices stressed and H is the number of stress hours. If this number is multiplied by 10^9 we obtain the failure rate expressed as Failure In Time (FIT). FITS are expressed as failures per billion device operating hours.

$$\text{FITS} = (\text{F.R.})(10^9) \qquad (2)$$

However, using equation (1) allows only for a failure rate calculation at the stress temperature. In order to apply the equation to the desired use temperature we use the well-known Arrhenius relationship to determine the thermal acceleration factor, F_a. One hour of device operation at temperature T_1 is equivalent to F_a hours of operation at temperature T_2. The activation energy, EA, is an important parameter in the Arrhenius equation and is discussed below. The Arrhenius equation is:

$$F_a(T_1 \rightarrow T_2) = e^{-\frac{EA}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \qquad (3)$$

where k = Boltzman's Constant (8.63×10^{-5} eV/°K) and T_1 is the accelerated stress junction temperature and T_2 is the desired use operating junction temperature in degrees Kelvin.

Junction temperatures, T_1 and T_2, should be used in determining acceleration factors. This temperature can be obtained from the equation below.

$$T_j = T_a + \theta_{ja} P_d \qquad (4)$$

where T_a is the operating ambient temperature

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and θ_{ja} is the package thermal dissipation (°C/ W) and P_d is the device power dissipation.

Crystal utilizes a low power CMOS process which typically raises the junction temperature about 7 to 15 °C, whereas analog bipolar IC's and hybrids can have power dissipations in the 1 W range. These differences in device junction operating temperatures can greatly affect the acceleration factors. For example, let's calculate the acceleration factors of a device with a power dissipation of 1 watt packaged in a 40 pin ceramic package. This is equivalent to a junction temperature change from 160 °C to 60 °C and from Table 2 the acceleration factor is 277. A typical Crystal device junction temperature is 10 °C higher than the ambient which results in a junction temperature change from 135 °C to 35 °C. This results in an acceleration factor of 636, as shown in Table 2. By comparing the results in Table 2 one can see how derating to a lower use temperature or failing to consider junction temperature when calculating acceleration factors can result in greatly differing failure rates.

TEMPERATURE CHANGE	TYPICAL ACCELERATION FACTOR (.7 E.A.)
125 → 70 °C	26.3
125 → 55 °C	77.5
125 → 25 °C	933.0
135 → 35 °C	636
160 → 60 °C	277

TABLE 2
ACCELERATION FACTORS FOR DIFFERENT TEMPERATURES (E.A. = .7 eV)

E.A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

TABLE 3
ACCELERATED FACTORS FOR DIFFERENT ACTIVATION ENERGIES (125 °C → 70 °C)

Table 3 compares acceleration factors for different activation energies. Using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal uses an activation energy of .7 eV, a conservative value, compared to the .8 eV to 1.0 eV used by some other analog IC vendors.

We now take the failure rate equation (1) at accelerated temperatures expressed in FITS and factor in the acceleration factors from the Arrhenius relationships considering junction temperatures and arrive at the equation below.

$$FITS = \frac{10^9 N}{DHF_a} \quad (5)$$

Using composite Crystal data through the 1st quarter of 1988, a failure rate at 25°C can be calculated by substituting in equation (5) above:

N = 108
D•H = 28,475,272
Fa = 641 (Assuming .7 eV and stress temperature of 125°C, using junction temperature derating)

D•H is the summation of the devices stressed at each readpoint multiplied by that number of stress hours.

Substituting we get:

$$FITS\ 25°C = \frac{(10^9)(108)}{(28{,}475{,}272)(641)} = 5.9\ FITS$$

The Weibull distribution is often used for product life predictions because it can describe increasing and decreasing failure rates. Also the Weibull distribution has both a shape parameter, β, and a scaling parameter, α. This is very useful in accurately describing the shape and scaling of the "bathtub" curve. These more accurate descriptions of the failure rate of the Weibull distribution make

this method superior to the uniform failure distribution described in Equation (1). The Weibull probability distribution function (PDF) f(t) is the probability of failure between time t and t + dt.

$$f(t) = \frac{\beta}{\alpha} t^{(\beta-1)} e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (6)$$

The Weibull PDF can also be expressed as a function of the Reliability function, R(t), and the instantaneous failure rate function, h(t), therefore:

$$f(t) = h(t)R(t) \qquad (7)$$

The Reliability function is found by integrating the Weibull PDF from t to ∞. This function is the probability that a device will survive to time t.

$$R(t) = \int_{t}^{\infty} f(t')dt' = e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (8)$$

The instantaneous failure rate function is the probability that a device will fail between time t and t+dt:

$$h(t) = -\frac{1}{R}\frac{dR}{dt} = \frac{\beta}{\alpha} t^{(\beta-1)} \qquad (9)$$

The Reliability function is used to calculate the shape parameter, β, and the time scale parameter, α. The shape parameter is the key function in shaping the infant mortality portion of the "bathtub" curve. A β of 1 indicates a uniform failure rate, β > 1 indicates wearout and β < 1 indicates a declining failure rate. To use Weibull statistics, failures that occur during operating life stresses are used to produce values of R(t). Failure times and R(t) values can be combined to estimate α and β. We first take the natural logarithm of both sides of equation (8).

$$\ln\left(\frac{1}{R(t)}\right) = \frac{t^{\beta}}{\alpha}$$

We again take the natural logarithm and obtain:

$$\ln\left[\ln\frac{1}{R(t)}\right] = \beta \ln(t) - \ln(\alpha) \qquad (10)$$

This last equation is now in the form of a linear function. Using linear regression techniques or Weibull plotting paper we obtain the Weibull shape and scale parameter. Some semiconductor manufacturers perform a burn-in screening on devices to insure that the end customer receives a population of devices that have minimal infant mortality and are from the useful life period of the reliability "bathtub" curve. It is very important to include this data for the entire lifetime of the device to obtain an accurate curve fit for obtaining α and β.

Once the parameters α and β for the Weibull distribution are known we utilize R(t) to calculate FITS. Crystal uses a 10 year lifetime in its FIT calculations and typically uses a 48 hour burn-in at 125 °C hence:

t_{10} = 10 yrs = 87,600 hours
t_1 = 48 hours

The number of devices that will fail in the ten year lifetime following burn-in is given by:

$$N = D\,[R(t_1) - R(t_1 + t_{10})] \qquad (11)$$

where D is the total number of devices stressed. The number of device-hours accumulated in 10 years can be estimated by counting the devices surviving after 10 years.

$$DH \geq D \bullet R(t_1+t_{10}) \bullet t_{10} \qquad (12)$$

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Using equation (2) for expressed failures in FITS we obtain the equation below for a Weibull distribution

$$FITS \leq 10^9 \frac{D\,[\,R(t_1) - R(t_1 + t_{10})]}{D \bullet R(t_1 + t_{10}) \bullet (t_{10})}$$

$$= \frac{10^9\,[\,R(t_1) - R\,(t_1+t_{10})]}{R(t_1+ t_{10}) \bullet (t_{10})} \qquad (13)$$

The above equation applies only at the stress temperature. In order to apply the equation to the desired use temperature we factor in the acceleration factors, F_a, from the Arrhenius relationship as it relates to time in the reliability function. Therefore in equation (12) above we replace $R(t_1 + t_{10})$ by $R(t_1 + t_{10}/Fa)$. Note that the device lifetime t_{10} is still 10 years but the reliability function must have the acceleration factor considered for derating to use temperature. Using composite Crystal data through the second quarter of 1993, yields a failure rate at 25 °C of 8.7 FITS.

This failure rate is a more accurate measure of Crystal reliability than that provided by the constant failure rate model of equation (5).

Reliability evaluations involve only samples of an entire population of devices. Therefore a confidence level, (CL), should be placed on the average failure rate. At any time a sample is stressed from a population there exists a finite chance of failures. If many separate samples were stressed from the same population and failure rates plotted, a normal distribution of failure rates would occur. Therefore, valid statistical methods for a normal distribution should be used to determine the desired CL. Confidence levels for reliability analysis are expressed in upper confidence levels (UCL), typically at 60% or 90% depending on the criticality of the device's application. The total sample size stressed is critical in defining the UCL. Therefore rather large sample sizes must be stressed to more accurately demonstrate the true failure rate. A larger spread will exist between the 60% and 90% UCL distribution for smaller sample sizes due to the greater probability that the sample stressed was not representative of the entire population.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85°C/85%R.H., usually have their actual results reported, due to the lack of widely recognized derating models. These stresses are experiments in which a given device will either pass or fail. Test results can be expressed as a simple failure rate - the number of failing devices divided by the total number of devices. However, the true failure rate is usually very small, so often there will be no failures observed. Instead of reporting an observed failure rate of zero, a confidence bound on the true failure rate is determined. Crystal uses a 90% confidence level in a standard formula to determine the test results for environmental stresses.

$$FR = \frac{\chi^2\,(2f+2)}{2n} \qquad (14)$$

The failure rate, FR, is computed by finding an upper bound confidence interval from a standard chi-squared table and dividing it by 2n, where n is the number of parts in the test, and f is the number of failures observed. $\chi^2(2f+2)$ is the right endpoint of the interval starting at zero which spans 90% of the area under the chi-squared curve with $2f+2$ degrees of freedom. This formula results from a Poisson approximation to the Binomial distribution, which is appropriate when the Binomial distribution is heavily skewed towards zero. A chi-squared value arises as an easy way to compute Poisson probabilities. This calculation agrees with the widely accepted lot

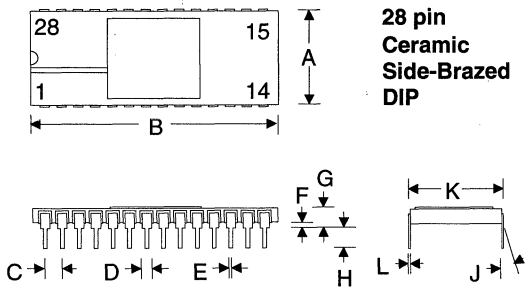
tolerance percent defective, LTPD, plans that are based on 90 % upper confidence.

Of course it is not satisfactory to have accurate methods on reporting failure rates without having programs and methods in place to continuously improve the reliability of the product. Crystal uses methodologies in every level of the company to provide the highest possible quality and reliability standards of its products.

In summary Crystal Semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability of its devices and has active programs in place to continuously improve the quality and reliability of its devices.

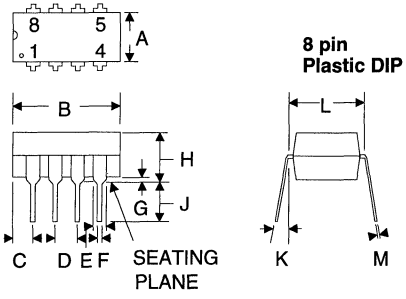
For further information on a summary of Crystal's methods of insuring high quality and reliability standards see the Quality and Reliability information in section 1 of this data book, or contact Crystal's Reliability and Quality Assurance Department at the factory.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

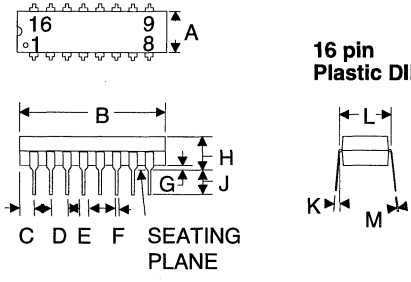
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

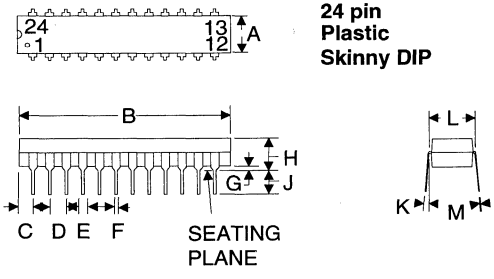
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

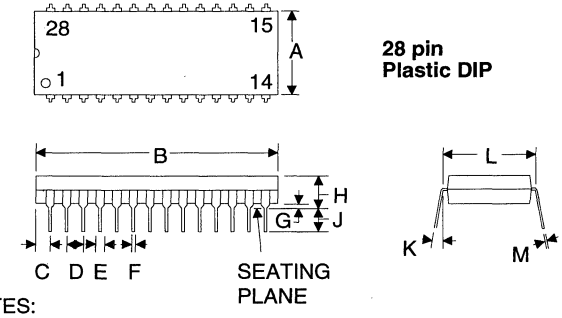
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

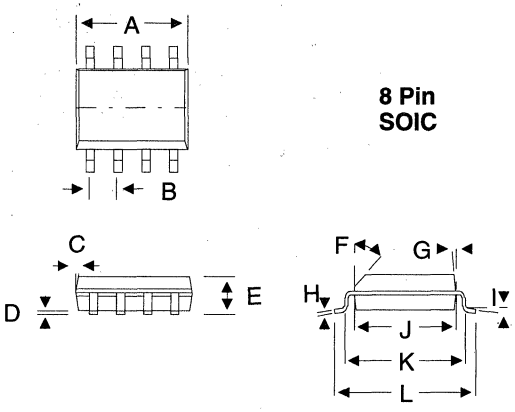
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

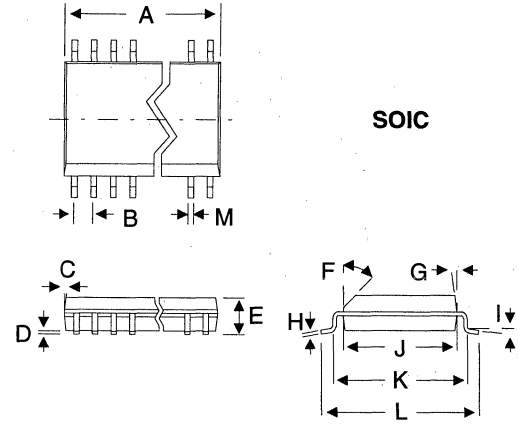
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

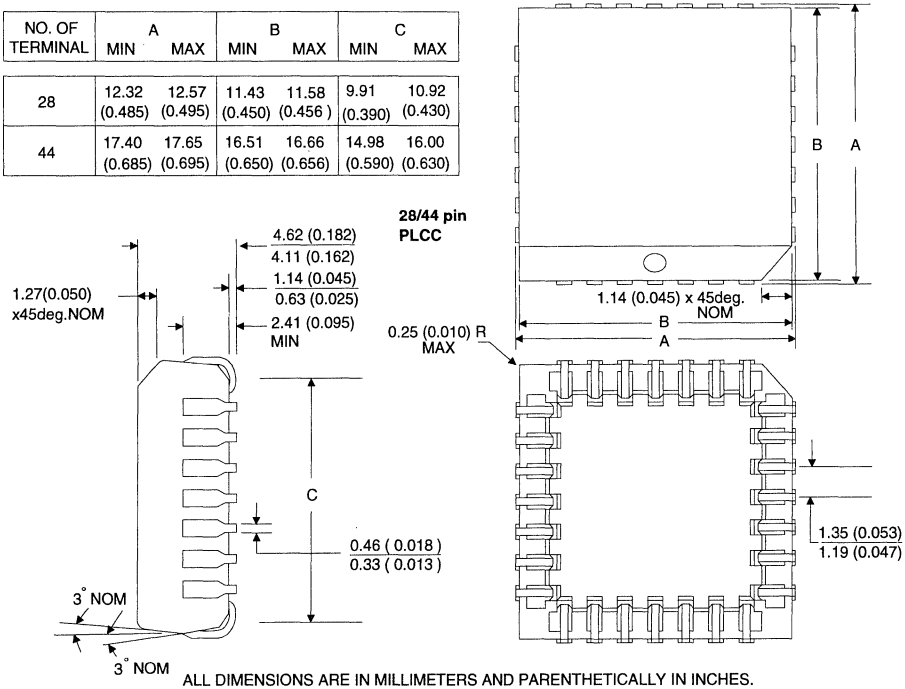


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

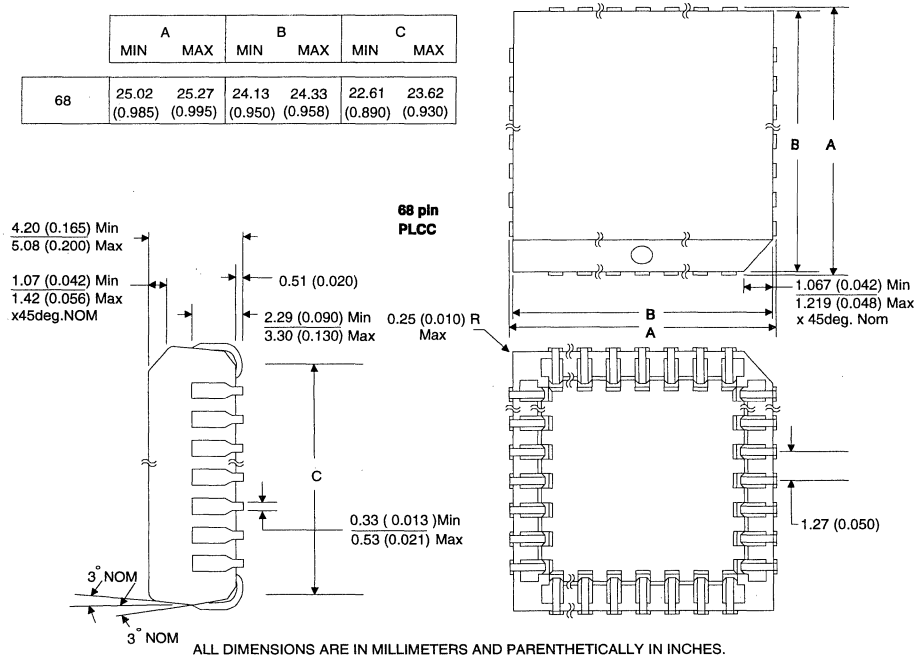
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

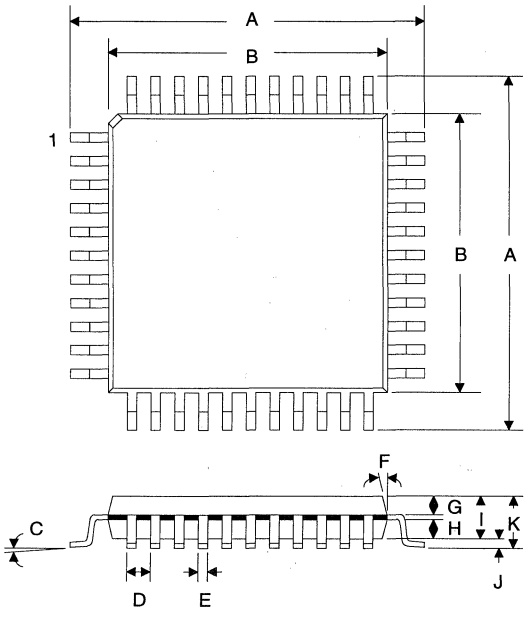
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



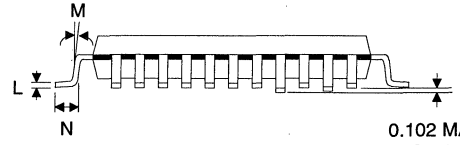
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

11

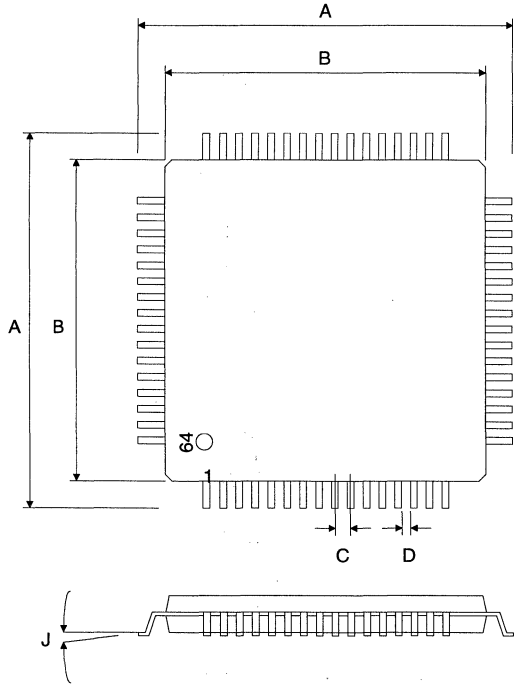
44 PIN QUAD FLATPACK

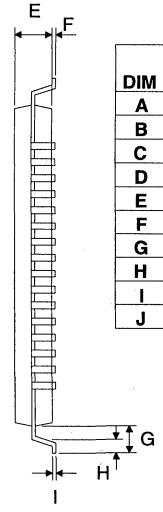


	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026



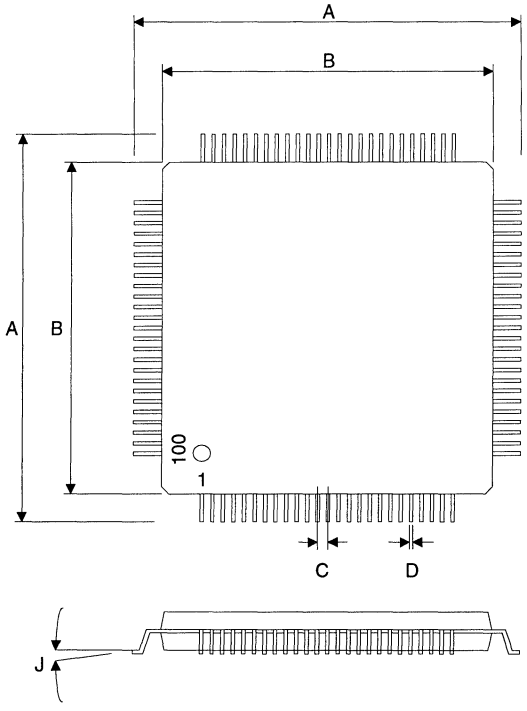
0.102 MAX
Lead Coplanarity

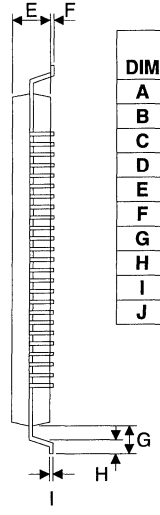




64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

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• Notes •

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